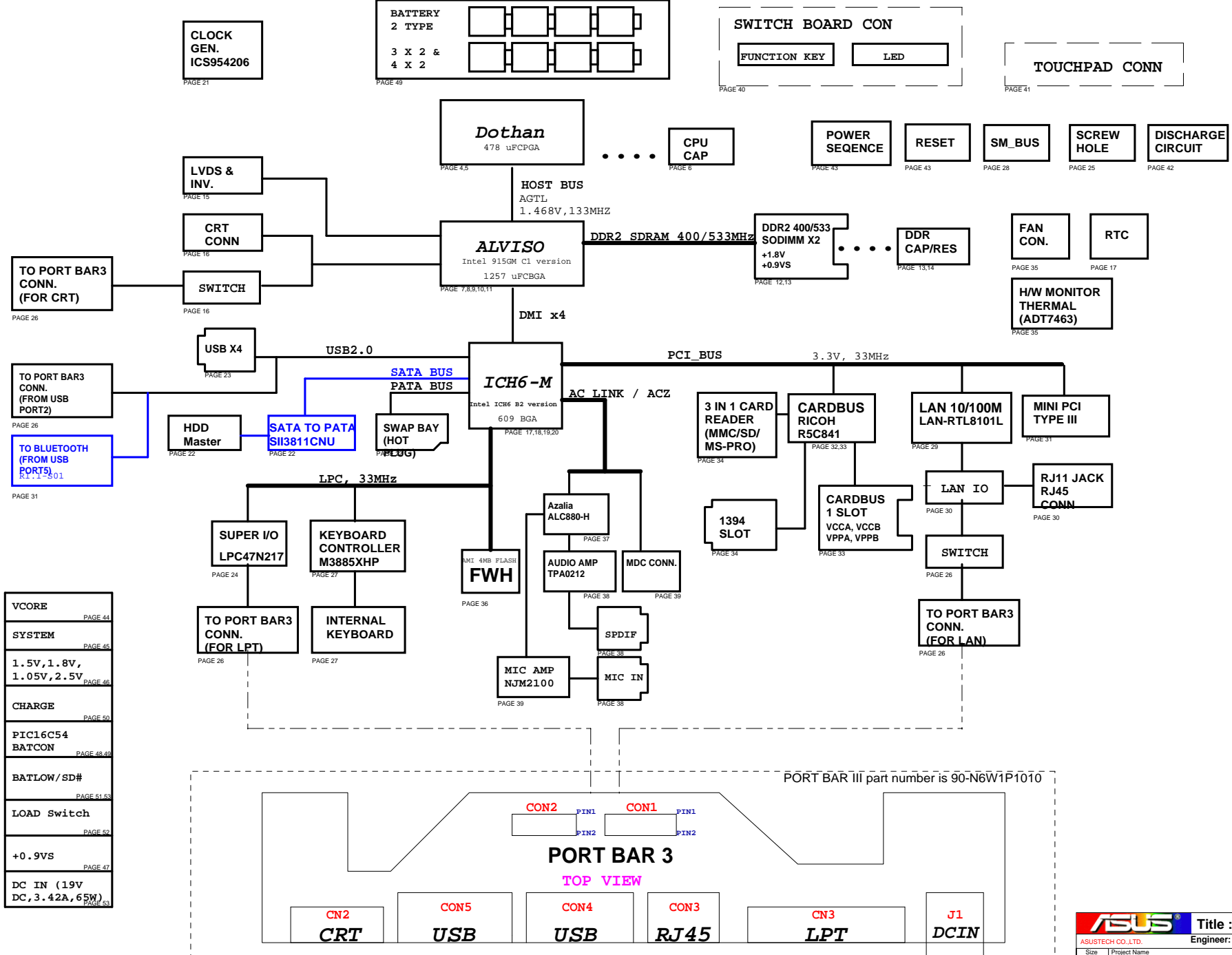


Z61Ae SCHEMATIC V2.0

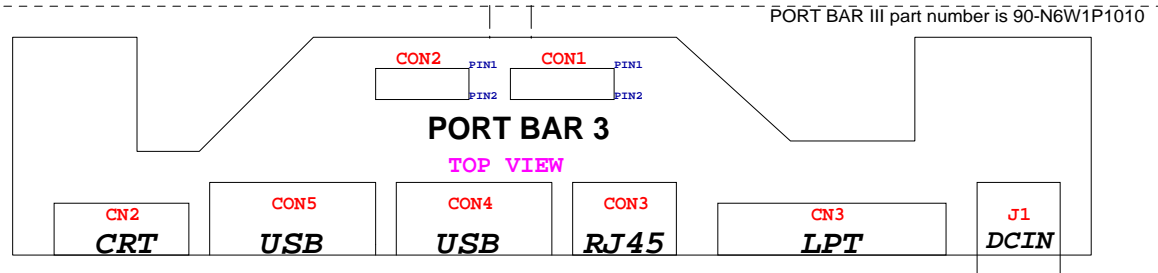
PAGE	Content	PAGE	Content	Notice
	SYSTEM PAGE REF.		POWER PAGE REF.	
4	DOTHAN CPU-1	43	POWER-ON SEQUENCE	01 The Z61Ae project code is ?
5	DOTHAN CPU-2	44	VCORE ADP3205	02 CON17/CON19 are SMT Level(SMT Request);DC Jack J6 is DIP Level.
6	CPU CAP & THERMAL SENSOR	45	SYSTEM	03 CN1/J1/U23 are changed to DIP Level(They will drop in SMT reflow). J4 is changed to DIP.Due to it will broken in reflow.
7	ALVISO: CPU	46	2.5V & 1.5V & 1.8V & 1.05V	04 Need to add ME and Power 59 level BOM in EE 60 BOM
8	ALVISO: DDR2 & DMI & PEG	47	1.5VA & DDR2	05 Check FWH IC 05-001017122 in BOM.
9	ALVISO: DDR2	48	PIC16C54/PWROK	06 Alviso U49 need to be changed to C1 version 02-010002640 (INTEL ALVISO-GM SL8G2),second source is 02-010002610(C0 version)
10	ALVISO: POWER & Caps	49	BATCONN	07 AMI BIOS LABEL P/N:15-135001010. It need to add in P/R 59-MID BOM by ME.
11	ALVISO: GND & NCTF & Straps	50	CHARGER	08 J2 need to be unmounted at PR stage for ATS power test
12	DDR2 SO-DIMM_0	51	BATLOW/SD#	09 R501(255 ohm) 10G213255013010 need to add second source 10-003412515.
13	DDR2 SO-DIMM_1	52	LOAD SWITCH	10 Add ACCL PCB Vendor 08-26ZA0020W???-->Need to create in SMT level. Need add other PCB vendors by document manager.
14	DDR2 ADDRESS TERMINATION	53	+5VLCM	11 All 0.01uF/25V/X7R (P/N:11-034110320) need to add 11-034110323 into second source.
15	LVDS & INVERTER CONNECTOR			12 MINIPCI Connector (P/N:12-023511240) need to add 12-023521243 into second source.
16	CRT			13 All CHIP RES. ARRAY 10 OHM(0402) 8R16P (P/N:10-124901000) need to add 10-12490100A into second source.(ECR is NA12958)
17	ICH6M--SATA/LPC/IDE/PM (1)			14 If delete debug card function,R876 and R628 mount 0 ohm.
18	ICH6M--PCI/DMIUSB/PCIE (2)			15 If use another power switch method.D30 unmount.
19	ICH6M--PWR/GND(3)			16 If use another power switch method.C616 mount 0.1uF/0402
20	ICH6M--PULL UP/STRAP (4)			
21	CLOCK ICS954206			
22	HDD & SWAP BAY CONN			
23	USB PORTS			
24	SUPER I/O LPC47N217			
25	SCREW HOLE			
26	PORT BAR 3			
27	KBC 38857			
28	SM BUS & POWER PORT			
29	LAN-RTL8101L			
30	RJ45 / RJ11			
31	MINIPCI			
32	PCI CARDBUS R5C841			
33	PCI PCMCIA SOCKET A			
34	PCI IEEE1394A & 3 IN1 CON			
35	FAN CONTROL			
36	FWH BIOS/Bluetooth Conn.			
37	AUDIO CODEC ALC880			
38	AUDIO_AMP_MB (TPA0212)			
39	MIC AMP & MDC Conn.			
40	LED BOARD			
41	TP CONN			
42	DISCHARGE MOS/EMI			

Z61Ae: DOTHAN/ALVISO-GM BLOCK DIAGRAM

Main Battery is Li-ION 8 cells(4*2),16.8V(4.2V*4),4400mAh(2200mAh*2),65W(3.7V*4cell*4.4A) battery pack.
 Second battery is Li-ION 6 cells(3*2),12.6V(4.2*3),3600mAh(1800mAh*2),40W(3.7V*3 cells*3.6A)battery pack.



VCORE	PAGE 44
SYSTEM	PAGE 45
1.5V, 1.8V, 1.05V, 2.5V	PAGE 46
CHARGE	PAGE 50
PIC16C54 BATCON	PAGE 48,49
BATLOW/SD#	PAGE 51,53
LOAD Switch	PAGE 52
+0.9VS	PAGE 47
DC IN (19V DC, 3.42A, 65W)	PAGE 53



*****GPIO setting is not final in this page.*****
 *****Please reference Z61Ae GPIO setting document.*****

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B,D	
LAN-RTL8101L	AD16	0	C	
CardBus	AD17	1	B	
1394	AD17	1	A	
3 IN 1		1	C	

Azalia : PCI_INTB#
 USB 0,1 : PCI_INTA#
 USB 2,3 : PCI_INTD#
 USB 4,5 : PCI_INTC#

SMBUS ADDRESS : CLK = 1101001x (D2)
 DDR_SODIMM0 = 1010010x (A4)
 DDR_SODIMM1 = 1010000x (A0)

ICH6M_GPIO	Use As	Signal Name	Power
GPI 00	GPI	KBDDT0	
GPI 01	GPI	KBDDT1	
GPI 02	GPI	N/A (PIRQE#)	
GPI 03	GPI	N/A (PIRQF#)	
GPI 04	GPI	N/A (PIRQG#)	
GPI 05	GPI	N/A (PIRQH#)	
GPI 06	GPI	BMBUSY#	
GPI 07	GPI		
GPI 08	GPI	EXT_SMI#_3A	
GPI 09	GPI	N/A (USB_OC#4)	
GPI 10	GPI	N/A (USB_OC#5)	
GPI 11	GPI	LID_ICH_3A	
GPI 12	GPI	KBDSCT_3	
GPI 13	GPI	BAT1_LLOW#_ICH6	
GPI 14	GPI	BAT2_LLOW#_ICH6	
GPI 15	GPI		
GPO 16	GPO		
GPO 17	GPO		
GPO 19	BLINK		
GPO 21	GPO	BACK_OFF#	
GPO 23	GPO	FWH_WP#	
GPIO24	GPO	CB_SD#	
GPIO25	GPO	IHZ_ICH6	
GPI 26	GPI		
GPIO27	GPI	PCB_VID0	
GPIO28	GPI	PCB_VID1	
GPI 29	GPI	PCB_VID2	
GPI 30	GPI		
GPI 31	GPI	ACIN_OC_3	
GPIO33	GPO		
GPIO34	GPO	OP_SD#	
GPI 40	GPI	PCB_VID3	
GPI 41	GPI	BATSEL_2P	
GPO 48	GPO		
GPO 49	GPO	N/A (CPUPWRGD)	

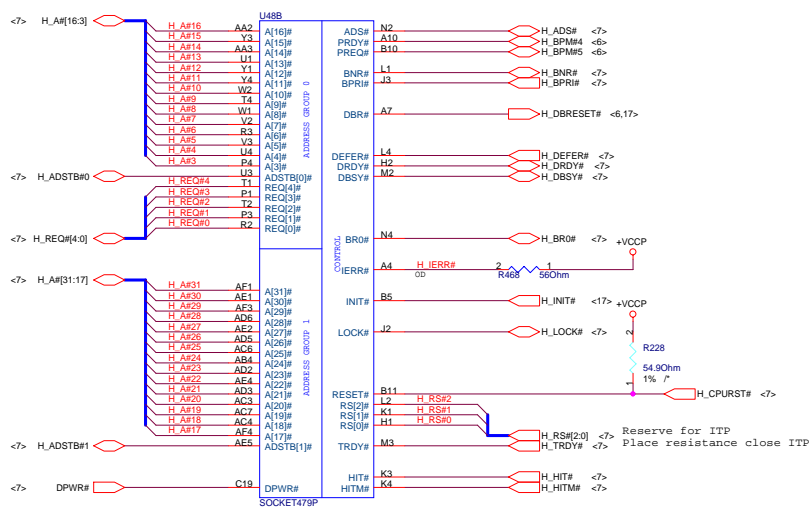
M38857_GPIO	USE_AS	SIGNAL_NAME
P23	GPO	
P22	GPO	BAT_LEARN
P21	GPO	BAT_SEL
P20	GPO	KBCRSM
P42	GPO	WATCHDOG
P43	GPI	CHG_FULL_OC
P44	GPO	KBCDFURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPO	BAT_LOW#_KBC
P51	GPO	XIDE_EN#_3
P52	GPO	BAYDOCK_IN#
P53	GPO	BT_ON
P54	GPI	BAY_RST
P55	GPI	BAT1_IN#_OC
P56	GPO	
P57	GPO	ADJ_BL
P67	GPI	BAT2_IN#_OC
P66	GPI	DISTP#
P65	GPI	MARATHON_#
P64	GPI	ACIN_OC
P63	GPI	LID_ICH#_3
P62	GPI	802_ON
P61	GPI	INTERNET#
P60	GPI	EMAIL#
P76	GPIO	SMD_BAT
P77	GPIO	SMC_BAT

M38857_GPIO	USE_AS	SIGNAL_NAME
P27	GPO	SCROLLOCK#
P26	GPO	NUM_LED#
P25	GPO	CAP_LED#
P24	GPO	SET_PCIRSTNS#
P41	GPO	EMAIL_LED#
P40	GPO	KBC_EXTSMI

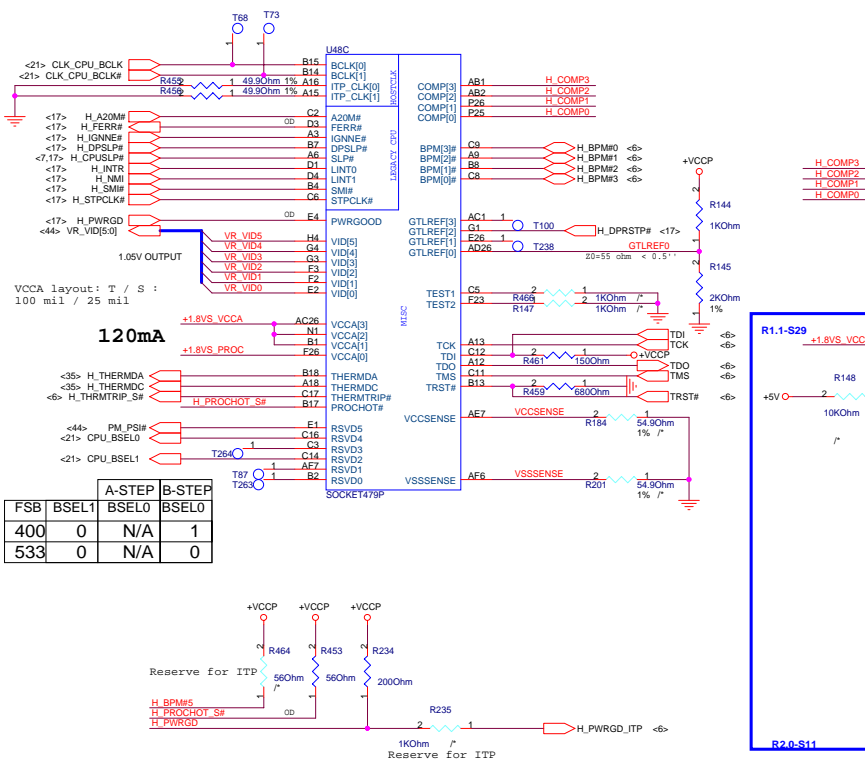
R5C593_GPIO	USE_AS	SIGNAL_NAME
IRQ3	GPO	
IRQ4	GPO	
IRQ5	GPO	
IRQ7	GPO	

47N217_GPIO	USE_AS	SIGNAL_NAME
GPI23	GPI	
GPI40	GPI	PID_0
GPI41	GPI	PID_1
GPI42	GPI	
GPI43	GPI	
GPI44	GPI	BAY_IN0
GPI45	GPI	BAY_IN1
GPI46	GPO	
GPI47	GPO	

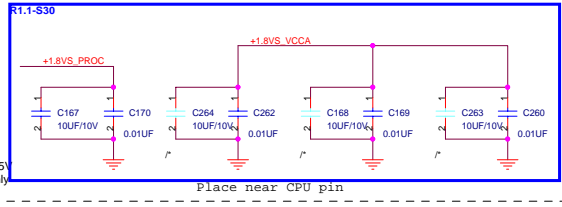
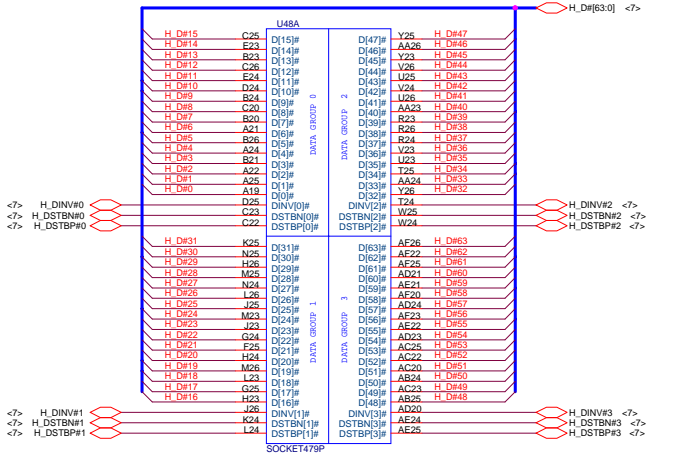
CPU Socket P/N : 12-046004791



P/N : 12-046004791

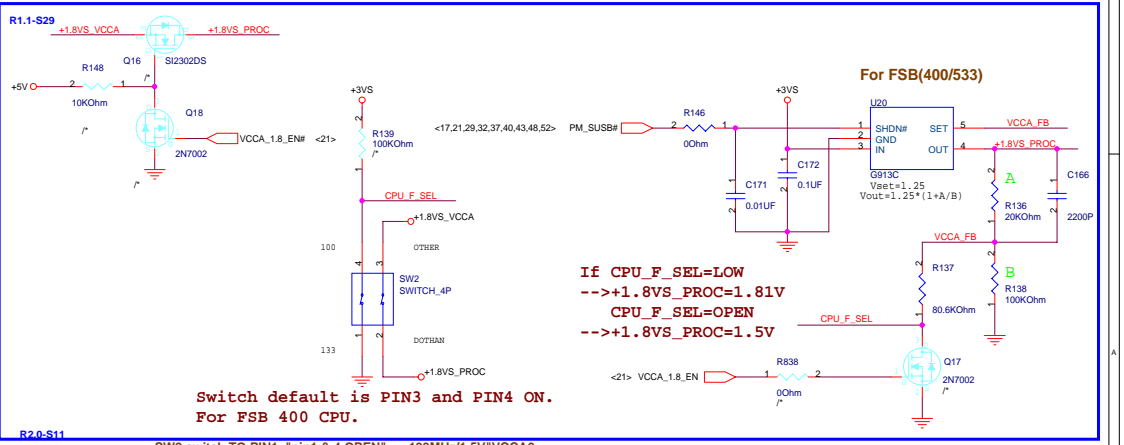


	A-STEP	B-STEP
FSB	BSEL1	BSELO
400	0	N/A
533	0	N/A



- H_COMP5 R232 2 1 54.90hm 1%
- H_COMP2 R233 2 1 54.90hm 1%
- H_COMP1 R233 2 1 54.90hm 1%
- H_COMP0 R142 2 1 54.90hm 1%

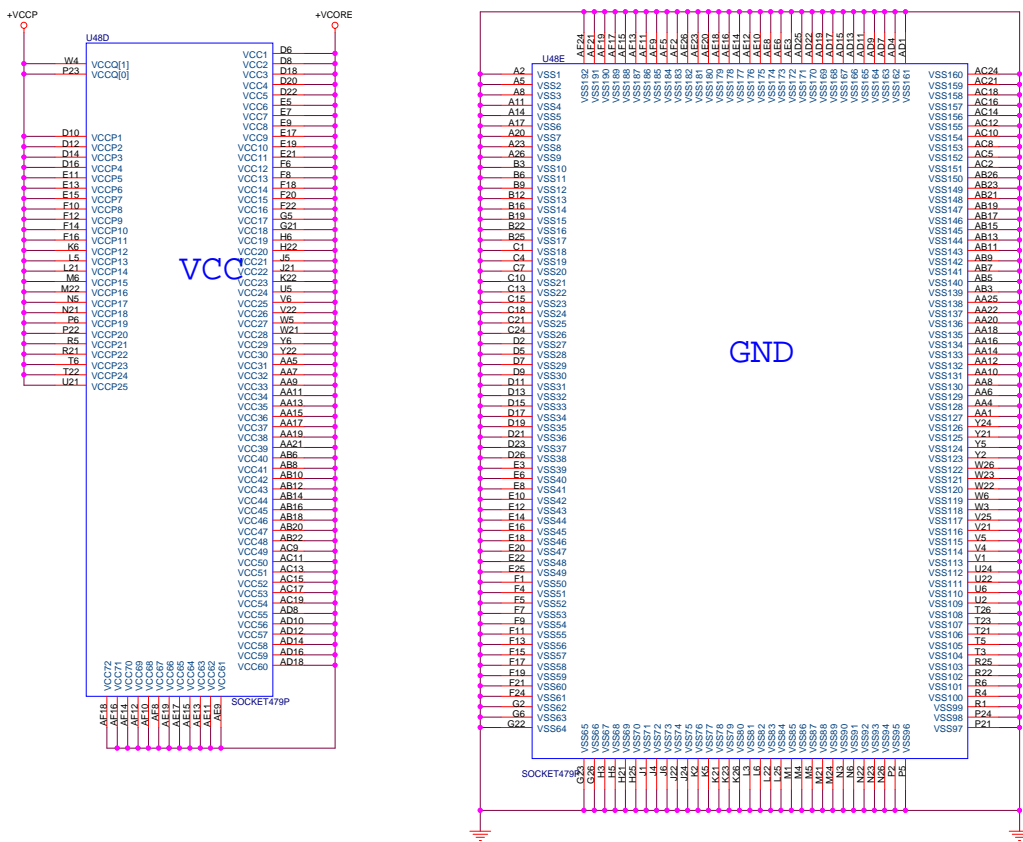
Layout note:
 COMP0 and COMP2 need to be Zo=27.4ohm traces.
 Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
 Traces should be shorter than 0.5". Refer to latest CS layout
 COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"



Switch default is PIN3 and PIN4 ON.
 For FSB 400 CPU.

SW2 switch to PIN1 "pin1 & 4 OPEN"==>133MHz/1.5V"VCCA0
 SW2 switch to PIN4 "pin1 & 4 SHORT"==>100MHz/1.8V"VCCA0

SW2 switch to PIN2 "pin2 & 3 OPEN"==>DOTHAN 533
 SW2 switch to PIN3 "pin2 & 3 SHORT"==>CELERON/BANIAS/DOTHAN400



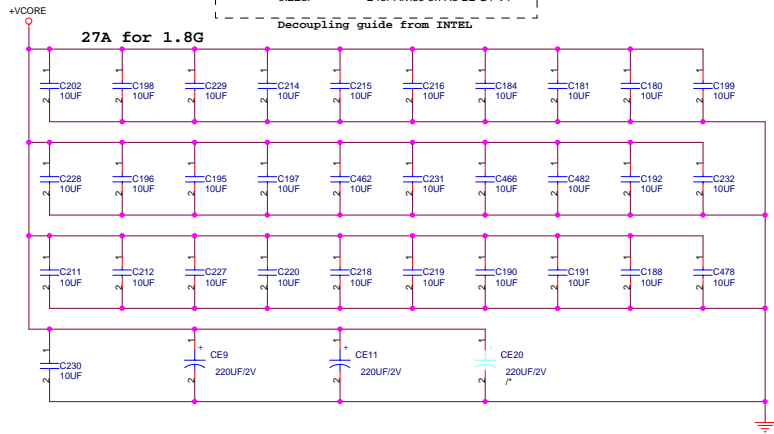
MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

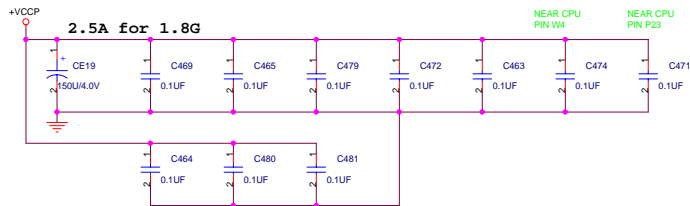
**+V CORE 10uF is
/6.3V/0805/X5R as
M7V R2.0**

V CORE 10uF/10V* 35	
220uF/2V	* 4
VCCP 0.1uF	* 10 for CPU
150uF	* 1 for CPU
0.1uF	* 10 for Alviso
150uF	* 2 for Alviso
4.7uF	* 1 for Alviso
2.2uF	* 1 for Alviso
0.47uF	* 2 for Alviso on A6 B2 G1 V1
0.22uF	* 2 for Alviso on A6 B2 G1 V1

R1.1-S32

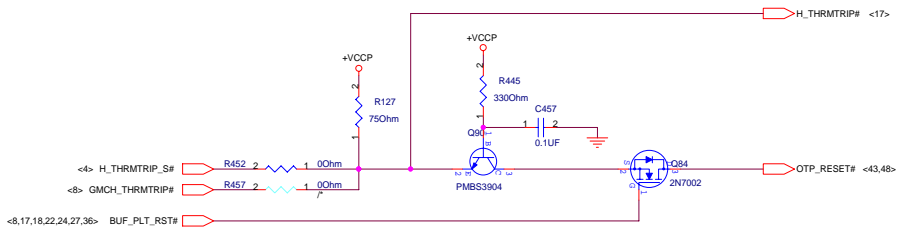
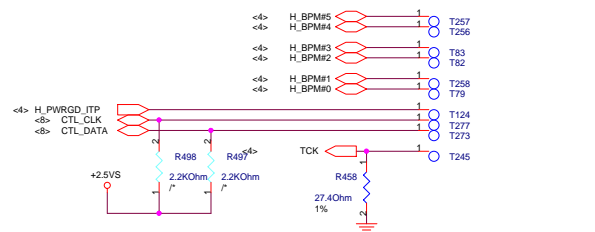
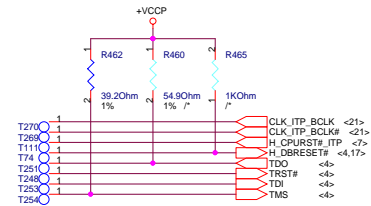


R1.1-S32

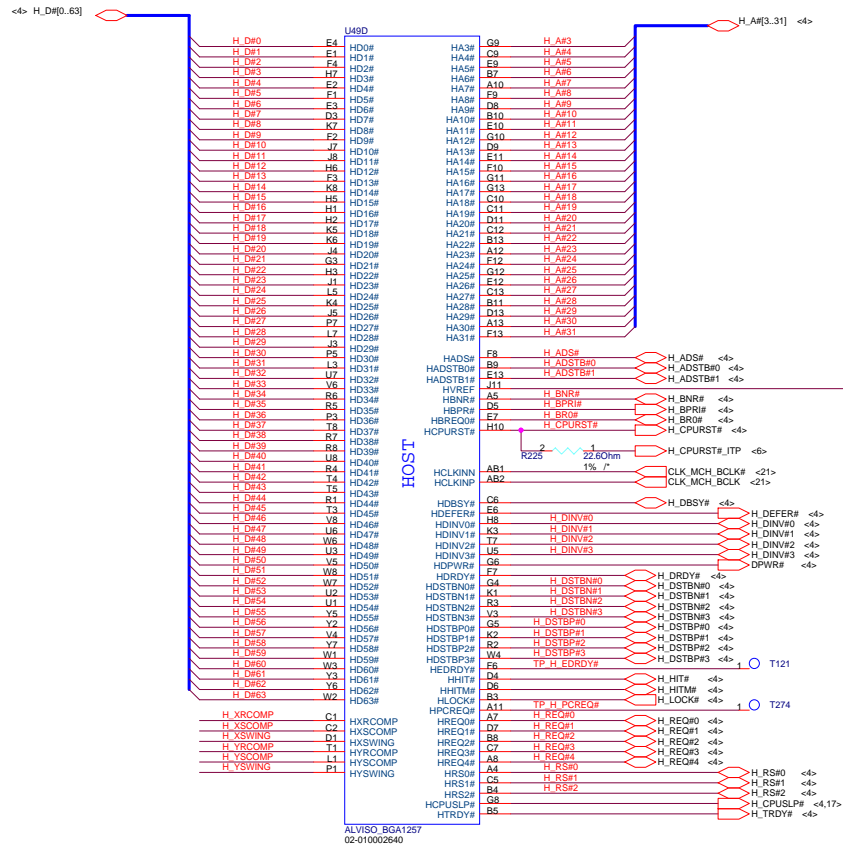
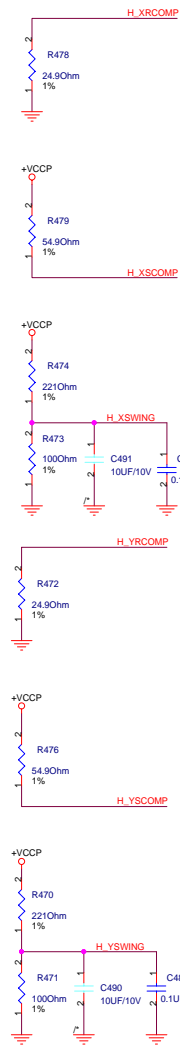


DO THAN VID TABLE

CPU FREQ.	HPM VOLTAGE	1.6G	1.4G	1.2G	1G	LPM 0.6G	C3/C4
1.80	1.308V	1.292V	1.260V	1.228V	1.196V	0.844V	0.748V
1.70							

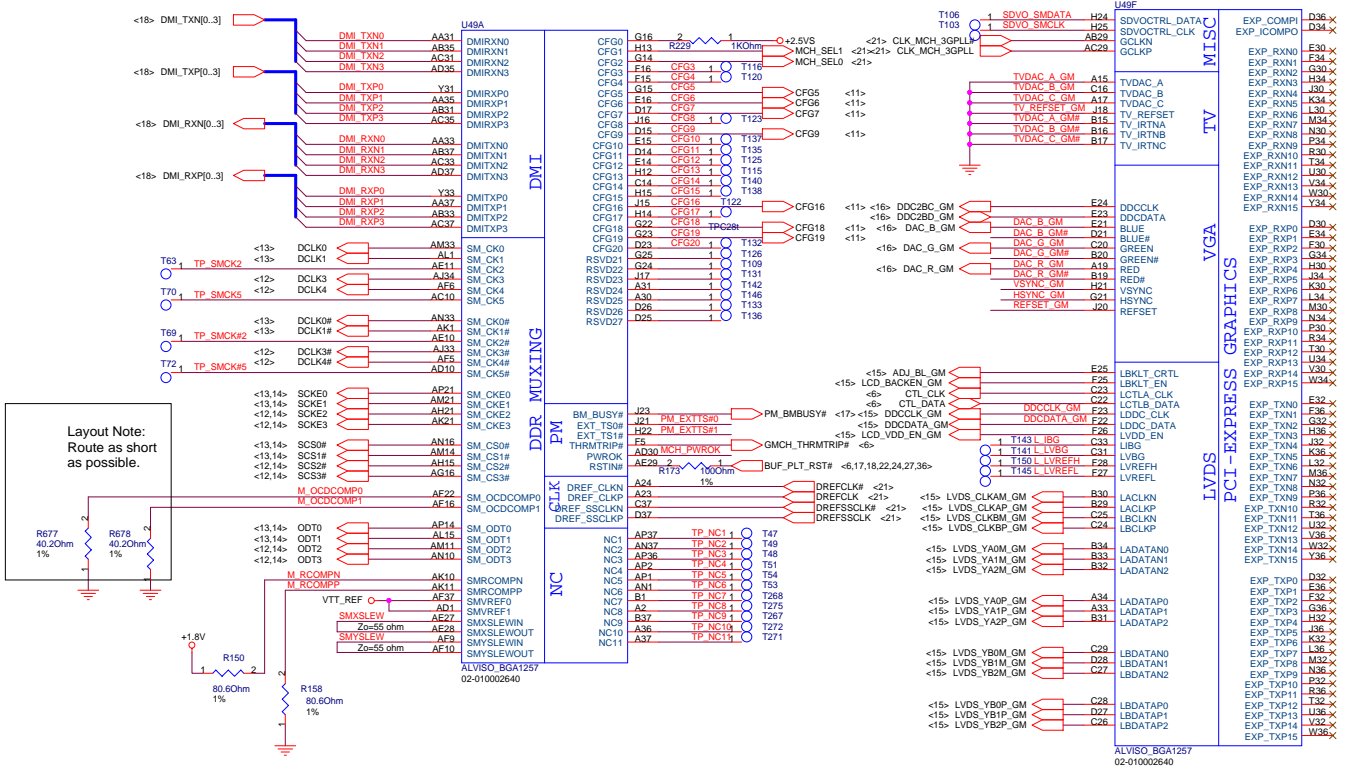


U49 Original P/N is 02-010002600(ALVISO-PM)
 Z61AE R1.0 use C0 version part number is 02-010002610 (ALVISO GM)
 U49 need to change to new C1 version 02-010002640 (INTEL ALVISO-GM SL8G2)
 R1.1 has changed it in symbol.

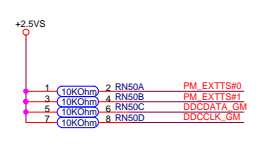
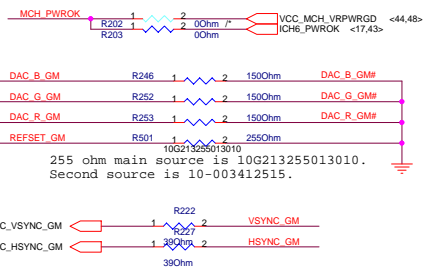
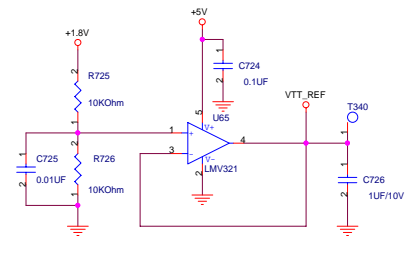


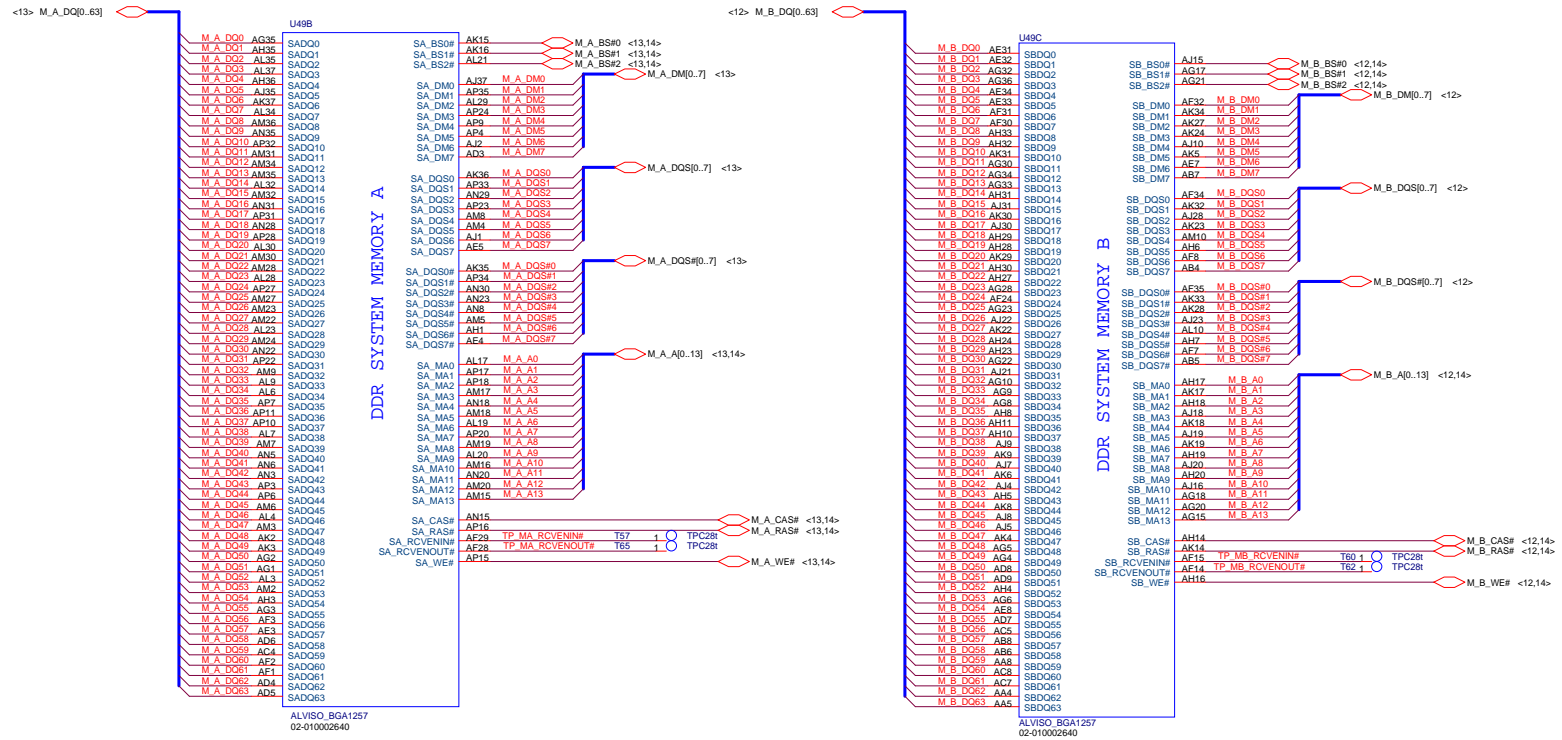
SDVOCTRL_DATA Int PD1
 0 : No SDVO device
 1 : SDVO device present

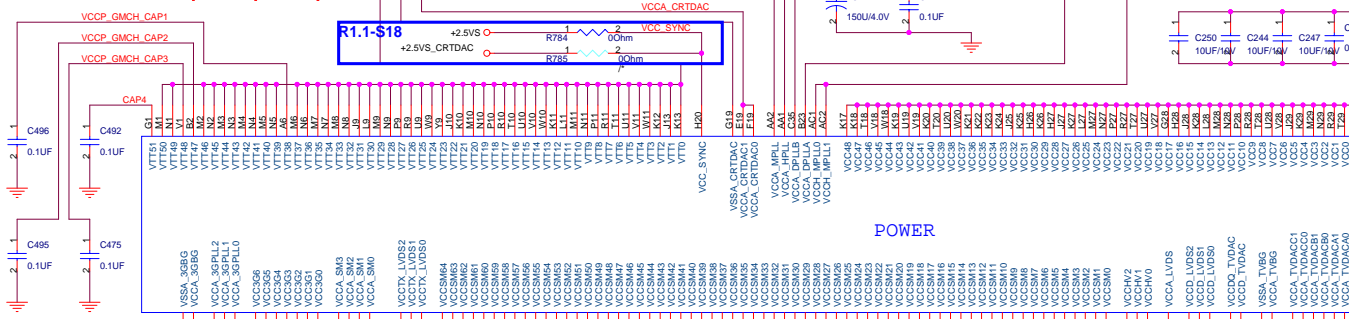
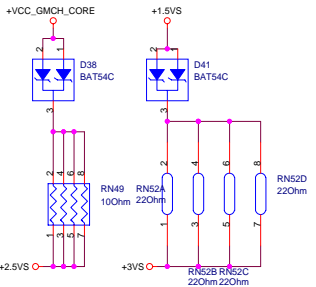
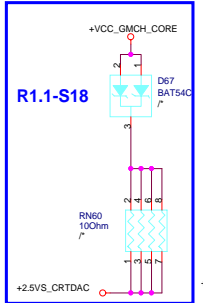
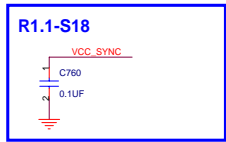
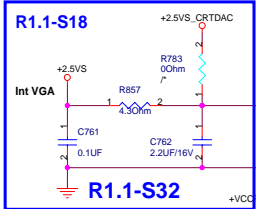
Disable TV_OUT :
 TVDAC A/B/C and TVIRTN A/B/C and TV_RESET
 and VCCTA_TV DAC A/B/C ... (ALL TV POWER)
 connect to GND



PCI-E signals can be left NC, if unused.







POWER

Note: All VCCSM pins shorted internally.

Note: All VCCSM pins shorted internally.

V1.8 DDR CAP6
V1.8 DDR CAP4
V1.8 DDR CAP9

V1.8 DDR CAP5
V1.8 DDR CAP2
V1.8 DDR CAP1

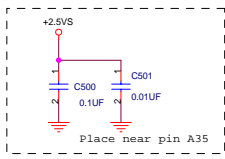
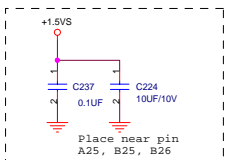
U49G ALVISO_BGA1257 02-010002640

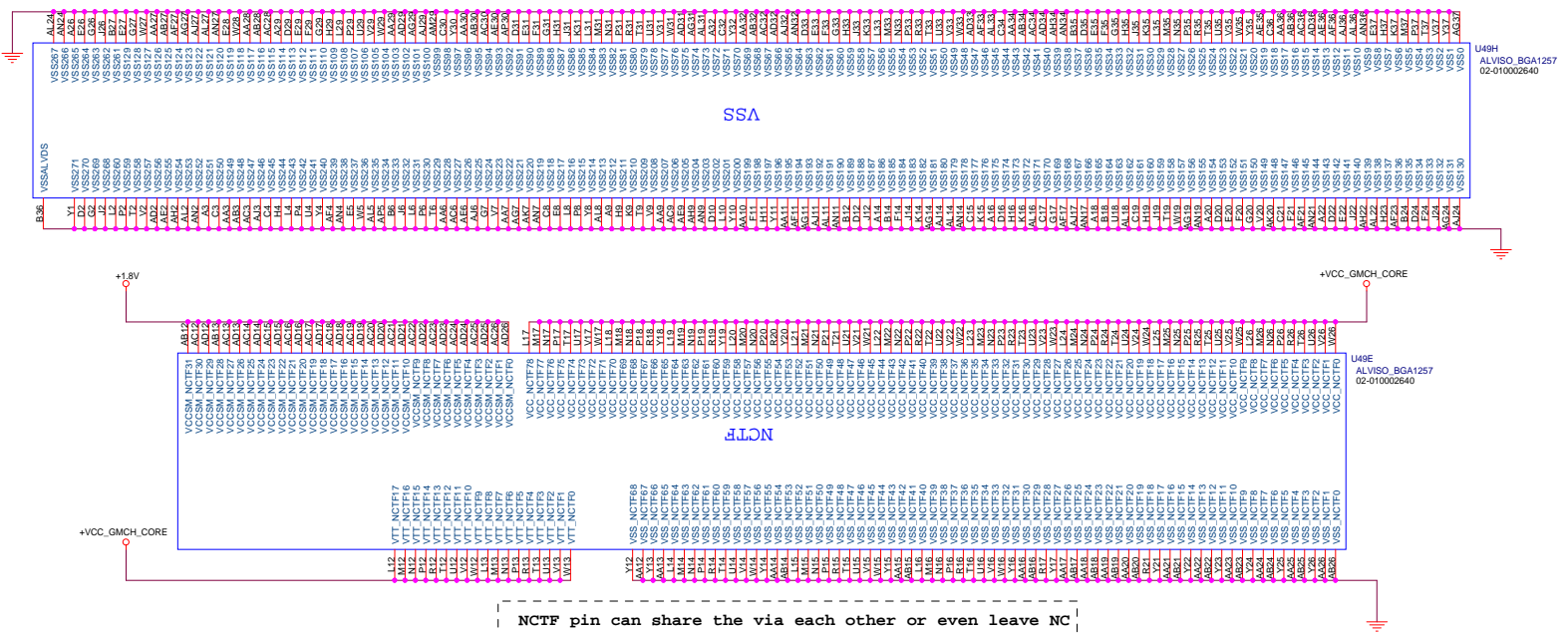
1.8V: 1A for DDR2 400 1 channel
2A for DDR2 400 2 channel
1.3A for DDR2 533 1 channel
2.7A for DDR2 533 2 channel

1.05VS: 850mA for CPU
310mA for external gfx

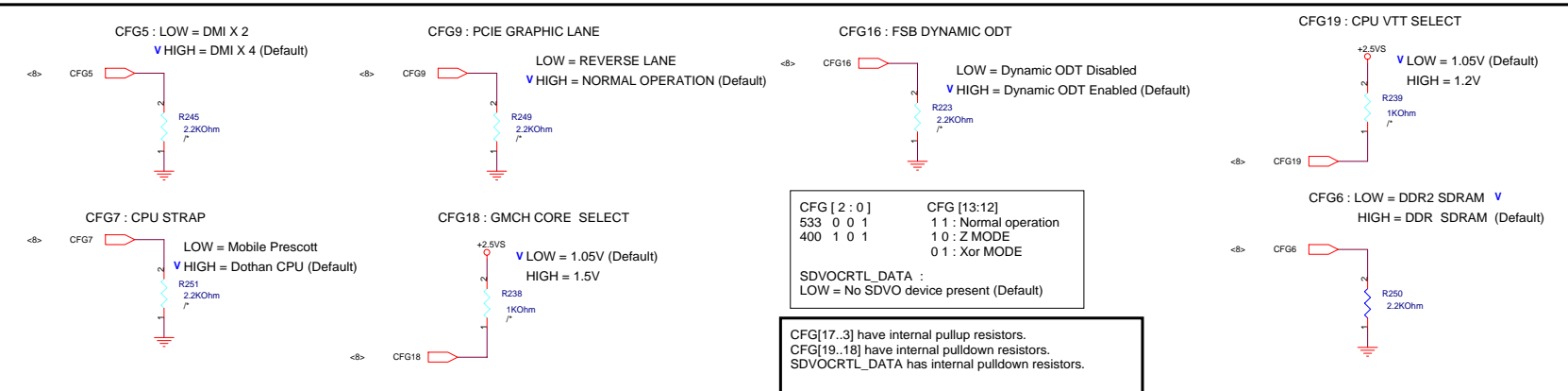
1.5VS: 1264mA
2.5VS: 293mA
3VS: 120mA

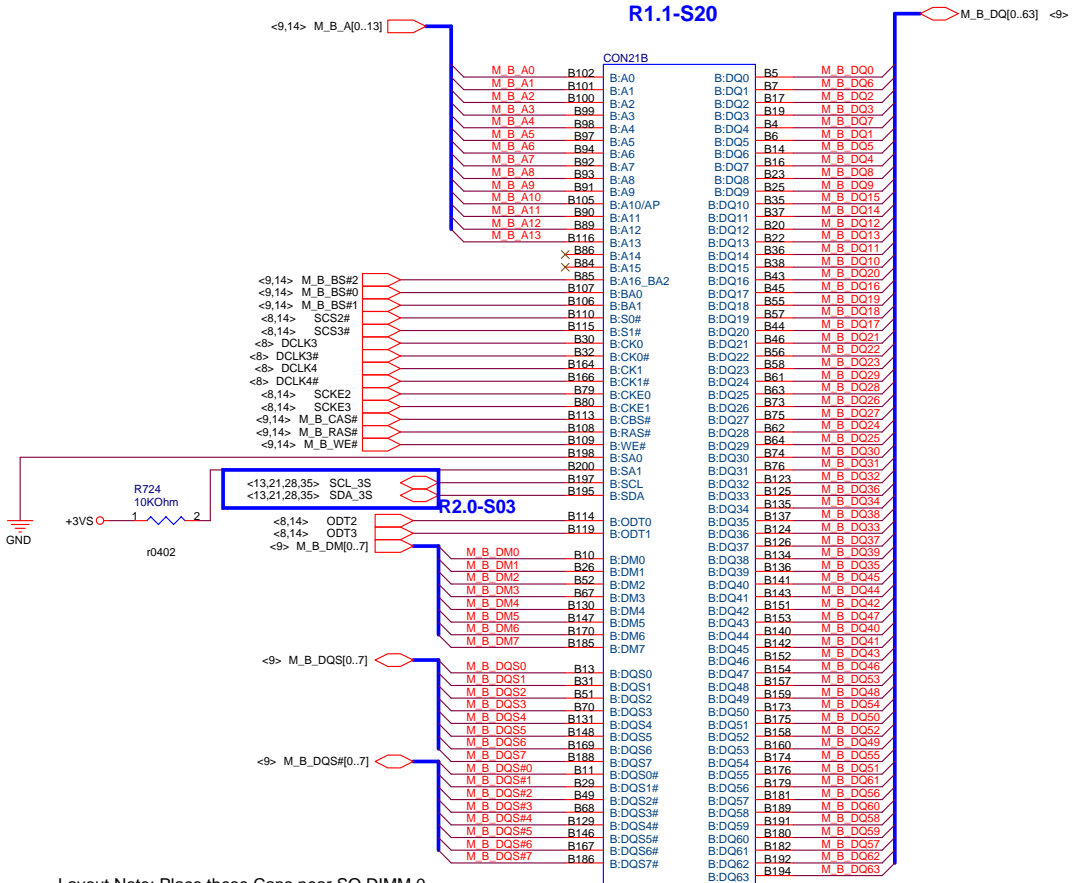
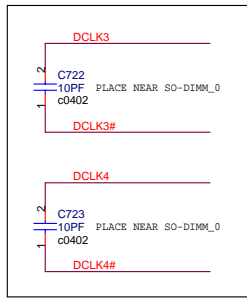
Disable TV_OUT
=> All TV POWER short to GND



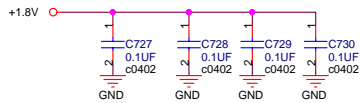


NCTF pin can share the via each other or even leave NC

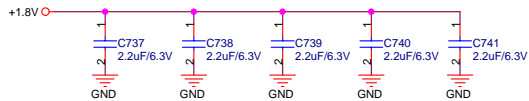




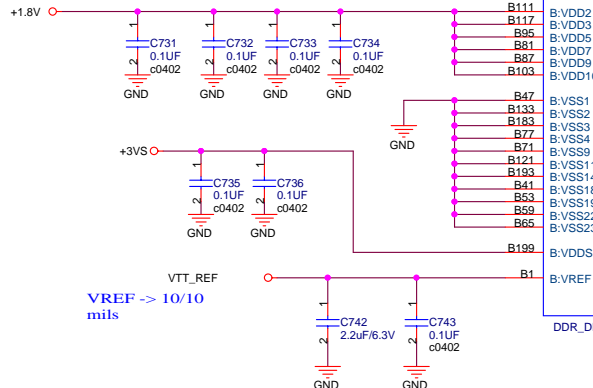
Layout Note: Place these High-Freq decoupling Caps near the GMCH



Layout Note: Place these resistors near the GMCH

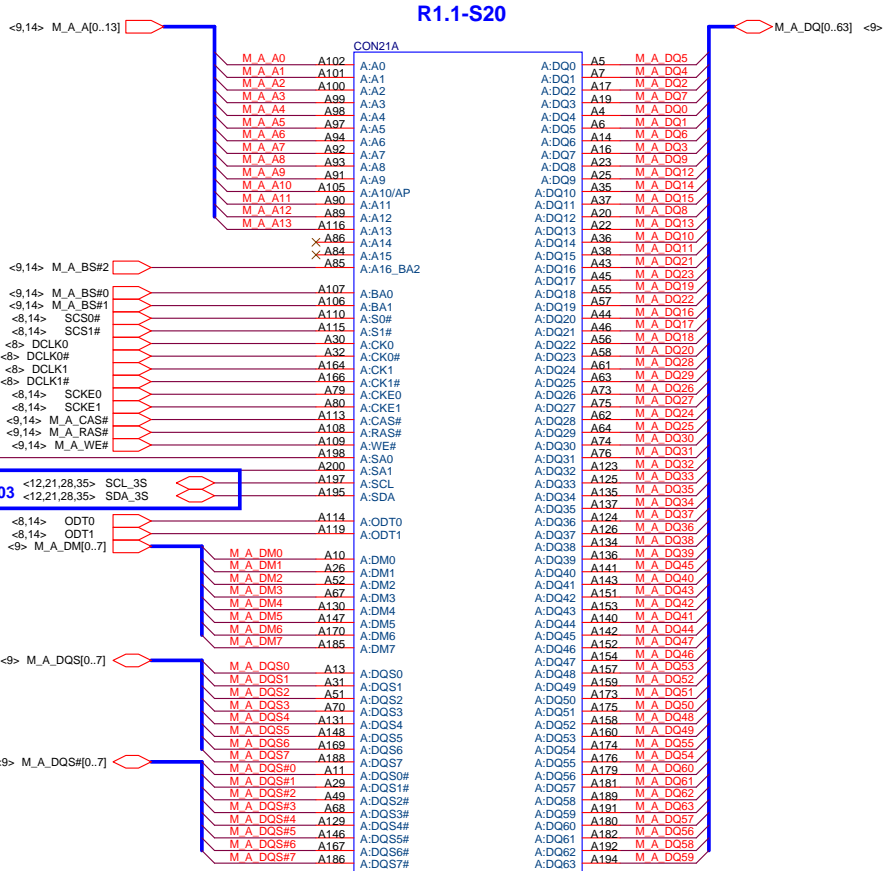
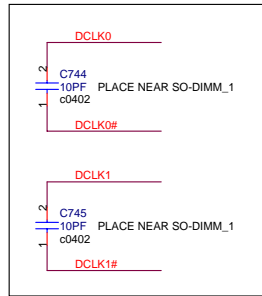


Layout Note: Place these Caps near SO DIMM 0

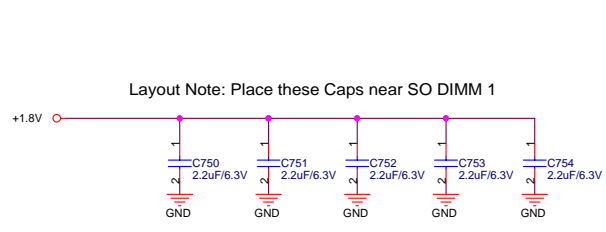


Layout Note: Place these Caps near SO DIMM 0

DDR2 DIMM SOCKET and SCHEMATIC is the same as A6V.



Layout Note: Place these Caps near SO DIMM 1

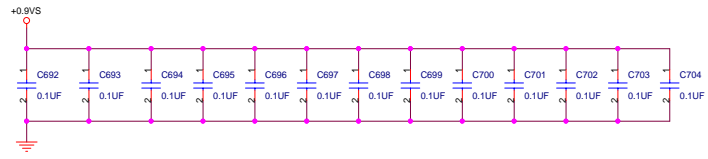


SO-DIMM 1 is placed father from the GMCH than SO-DIMM 0

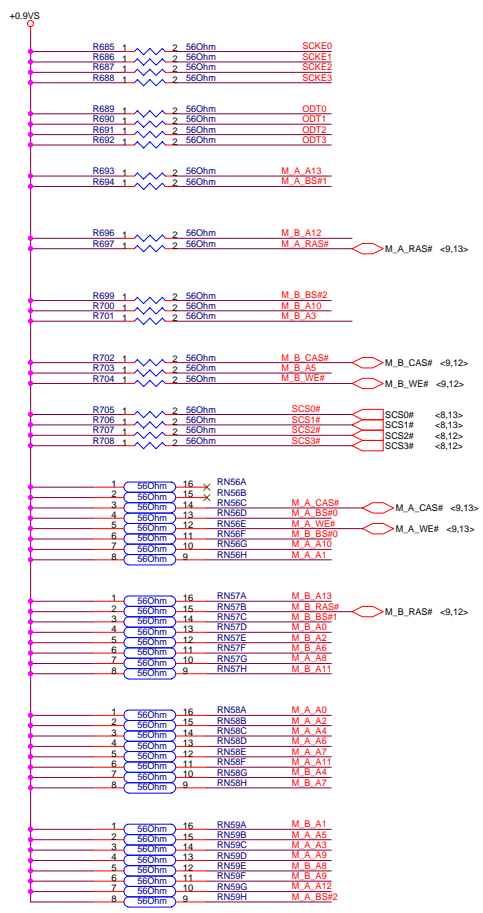
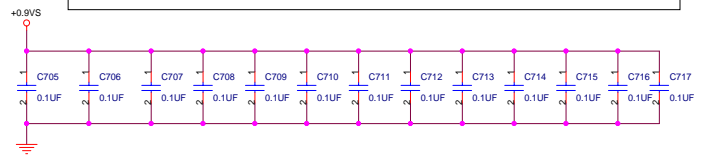
DDR2 DIMM SOCKET and SCHEMATIC is the same as A6V.

R1.1-S28

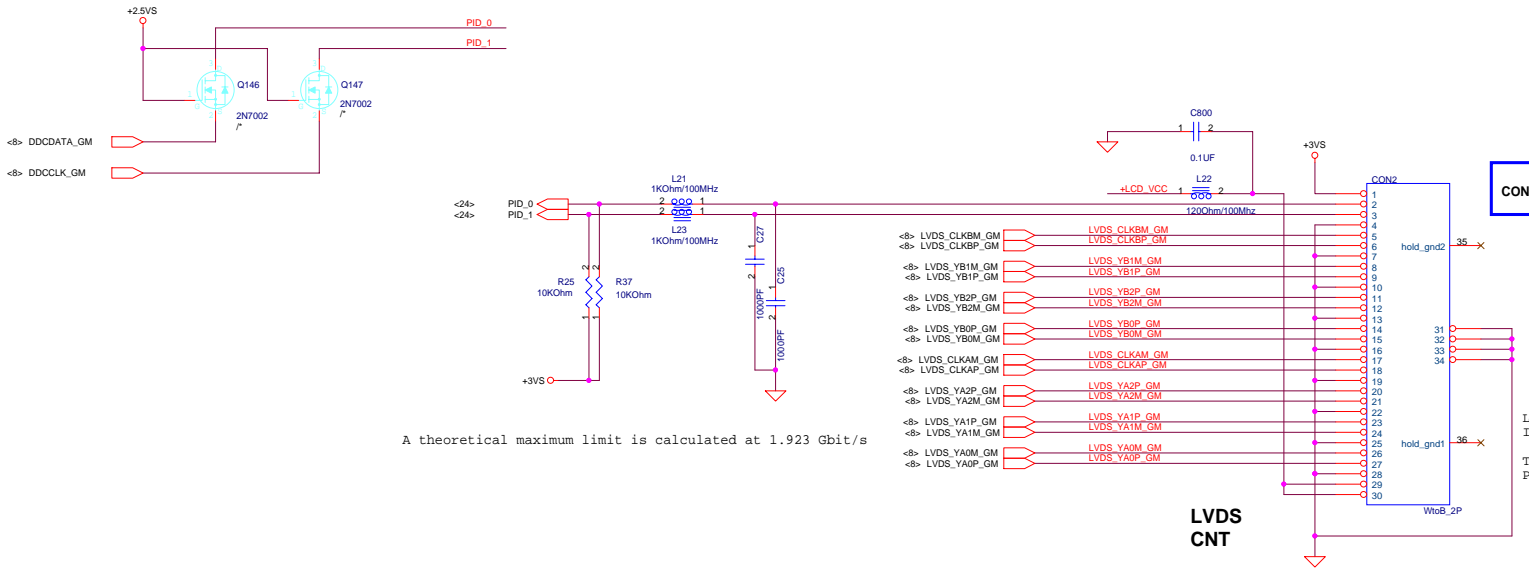
- M_A_A[0..13] <-9,13>
- M_A_BS#[0..2] <-9,13>
- M_B_A[0..13] <-9,12>
- M_B_BS#[0..2] <-9,12>
- SCKE[0..3] <-8,12,13>
- ODT[0..3] <-8,12,13>



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



TO SUPPORT SPWG PANEL(EDID)

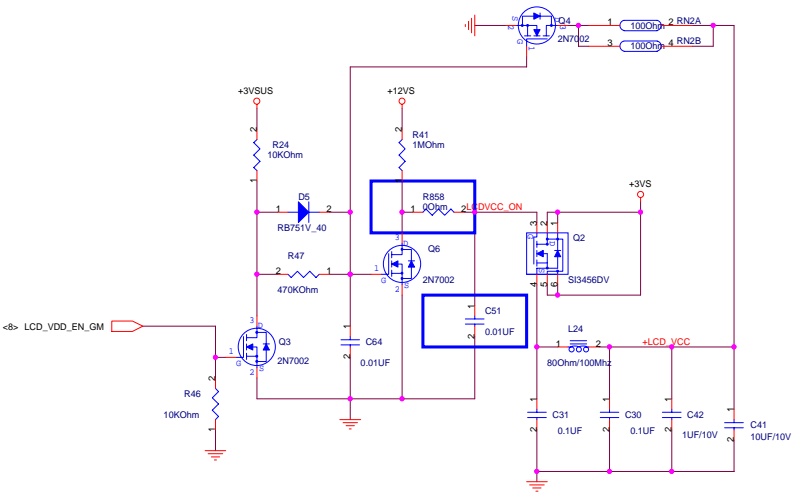


Panel Size	Resolution	Pixels	Aspect Ratio
14.1"	XGA	1024 x 768	4:3
14.1"	SXGA+	1400 x 1050	4:3
14.1"	UXGA	1600 x 1200	4:3

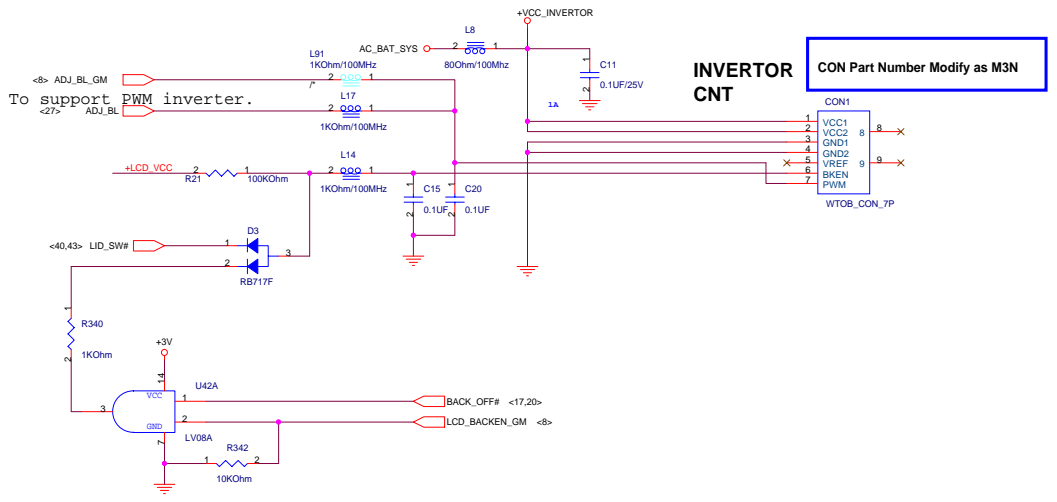
LVDS default Cable is 08-20C28012N.(None EDID function)
It default PID setting is PID_0 = 1 and PID_1 = 0 on cable.
To support EDID function that need new cable.
Panel ID is LCD vendor apply to system

A theoretical maximum limit is calculated at 1.923 Gbit/s

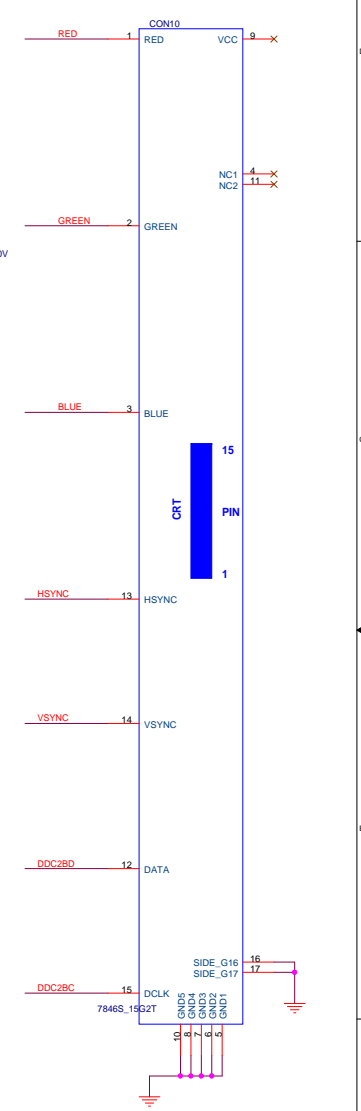
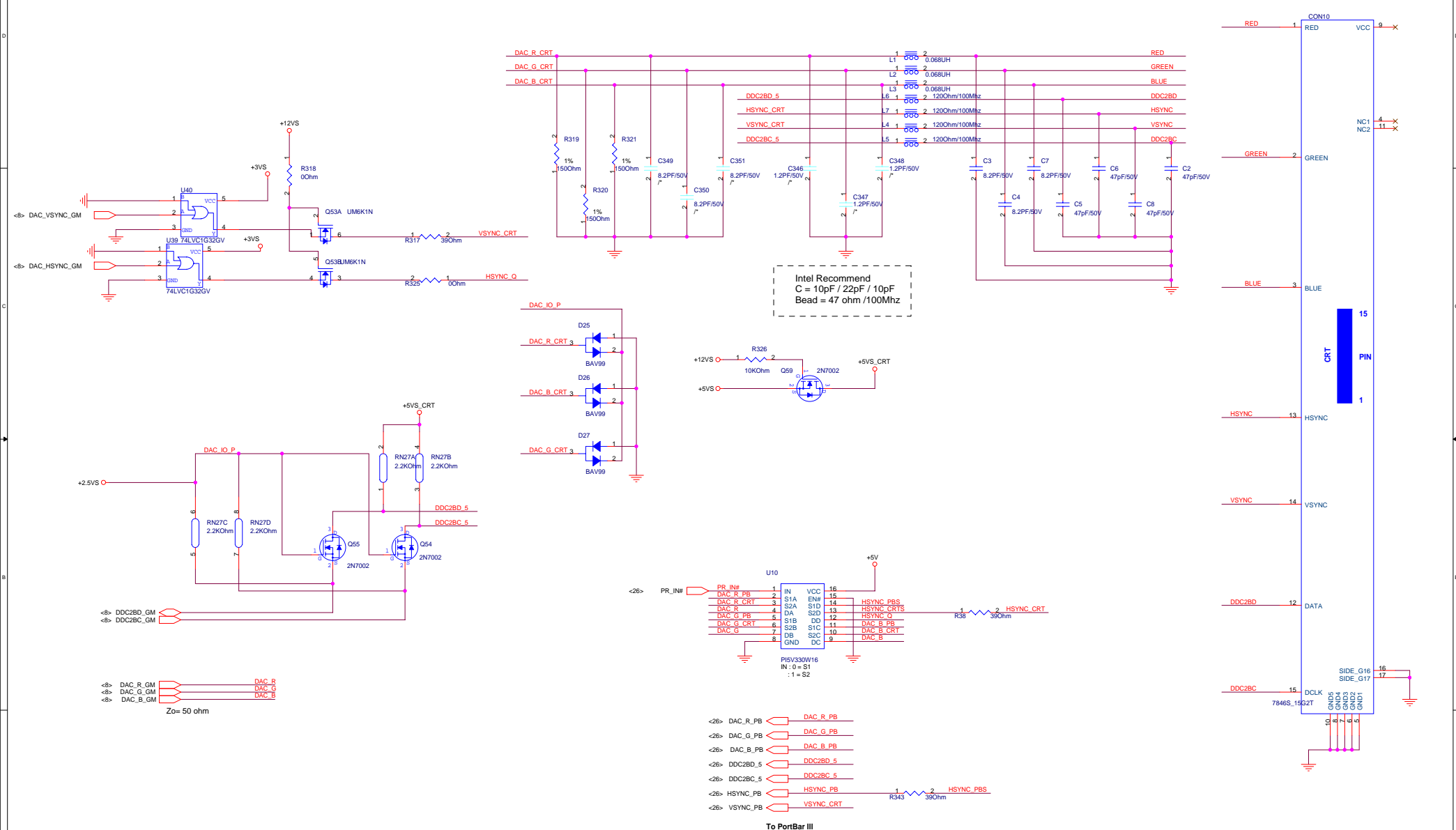
LVDS CNT



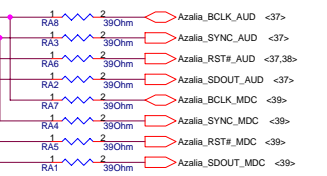
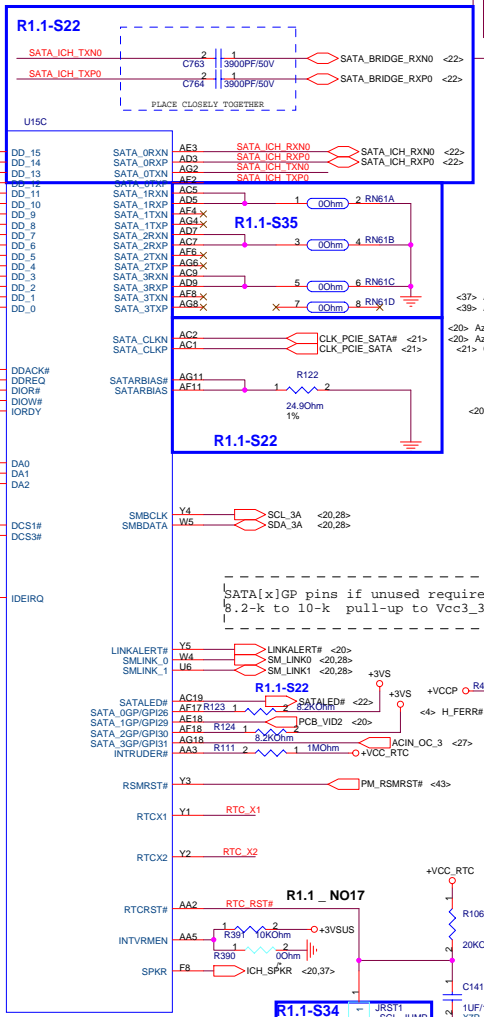
To support PWM inverter.



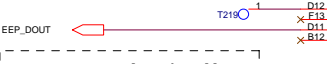
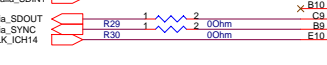
CON Part Number Modify as M3N



U15 Original P/N is 02-010002500(ICH6-M-None MP Version)
 U15 (SB) need to change to 02-010004402(ICH6-M-MP B2 Version)
 R1.1 has changed it in symbol.



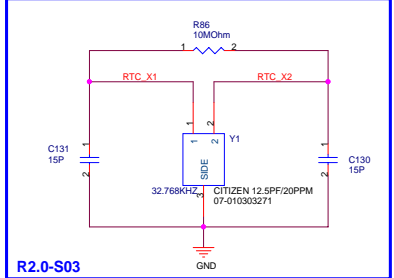
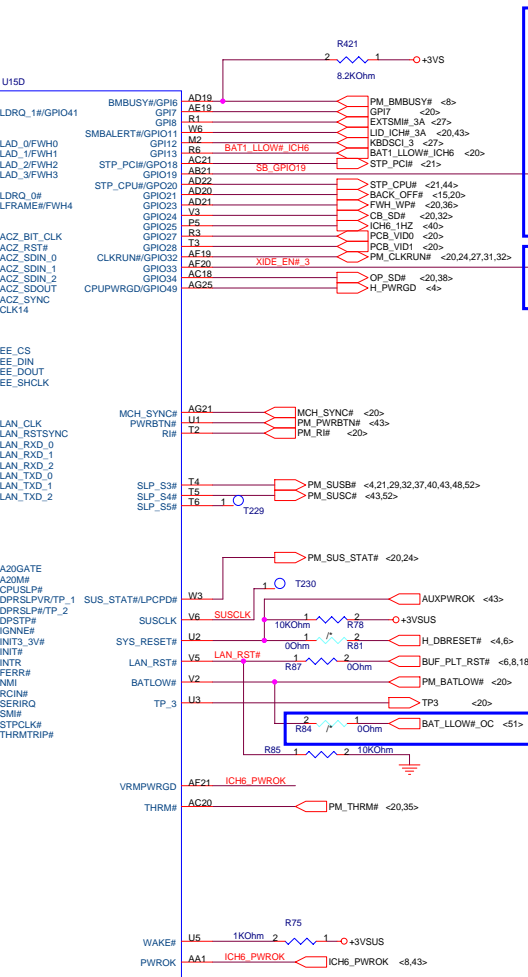
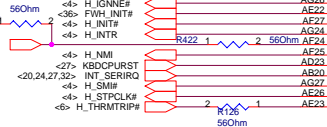
Unused SATA pin
 - Connect RX, RBIAS, CLK to GND
 - Leave TX, LED# as NC



EE_DOUT: Internal weak pull up
 EE_CS: Internal weak pull down

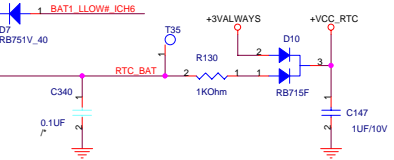
H_CPLUSP# R94 : B STEP NO STUFF
 H_DPRSTP# R95 : A STEP NO STUFF

SATA[x]GP pins if unused require
 8.2-k to 10-k pull-up to Vcc3_3.

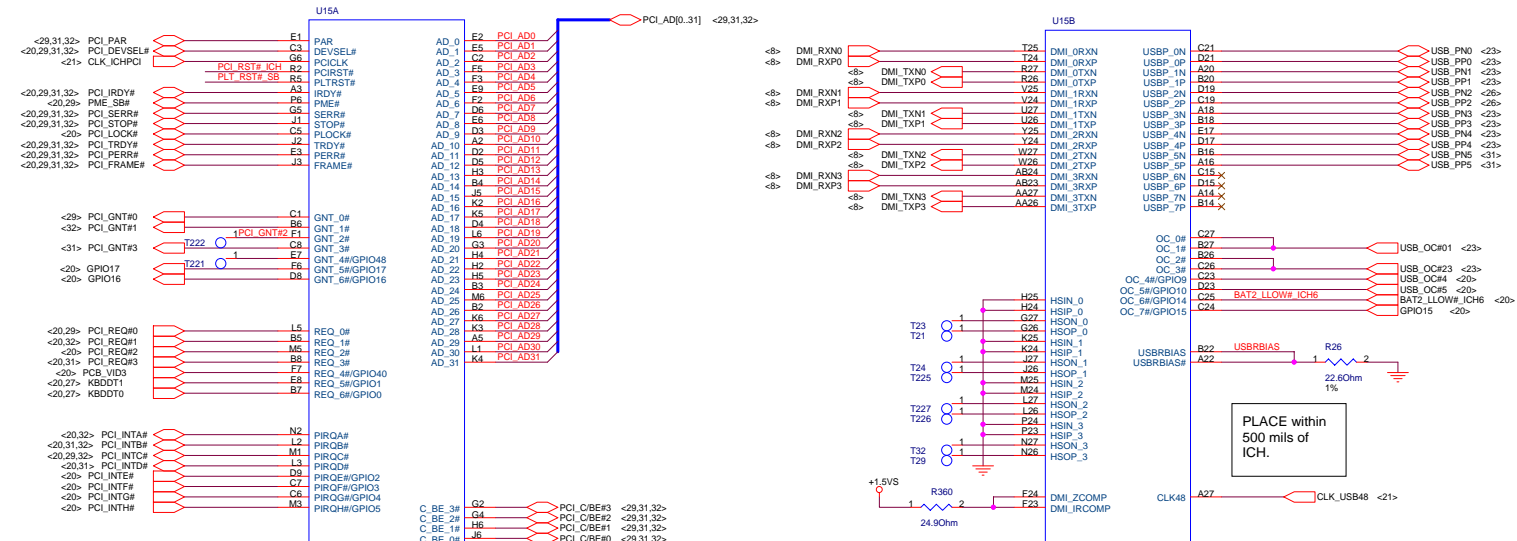


RTC CMOS CLEAR (RTC CLR)

CON Part Number Modify as ME



RTC BAT



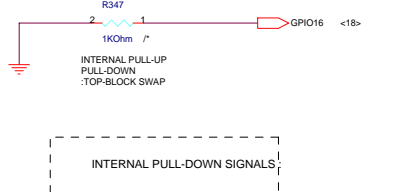
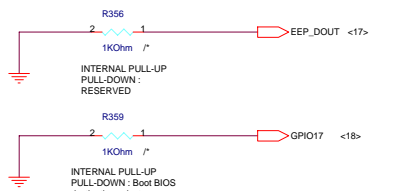
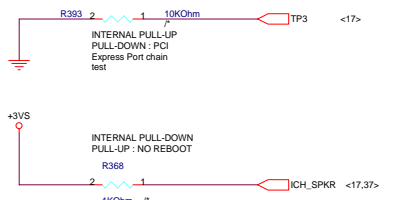
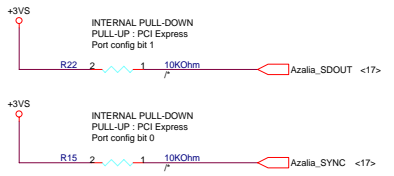
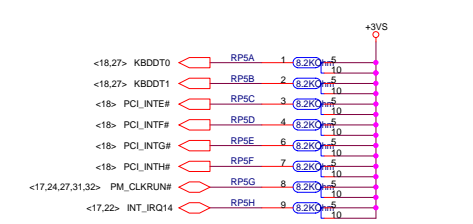
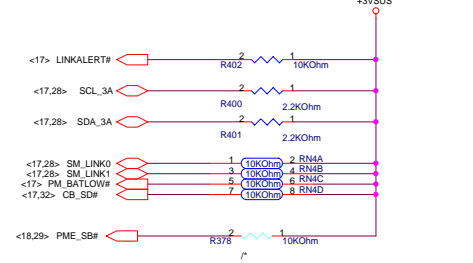
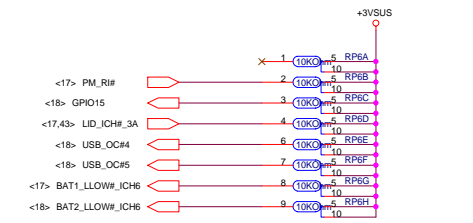
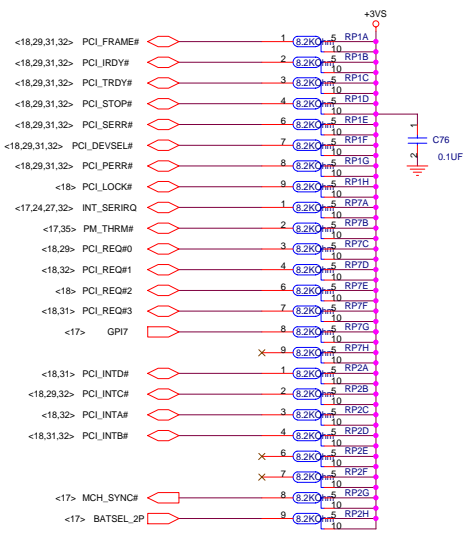
PLACE within 500 mils of ICH.

PLACE within 500 mils of ICH.

Can be issue SCI or SMI List: GPIO0-GPIO15
Resume Power Well GPIO List: GPIO8, 11, 13, 14, 15, 24, 25, 27, 28

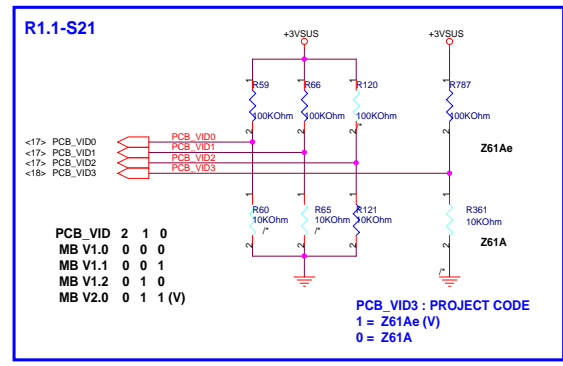
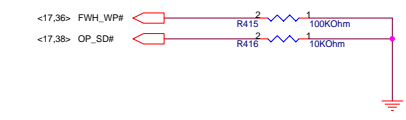
Only GPI Pin: GPIO-8, 11-15, 26, 29, 30, 31, 40(5V), 41
Only GPO Pin: GPIO16-17, 19, 21, 23, 48
Can be GPIO: GPIO24, 25, 27, 28, 33, 34

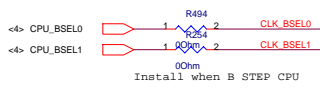
Resume Power Input Pin List:
BATLOW#, AC_SDIN[0:1], LAN_RST#,
OC[7:0]#, PME#, PWRBTN#, RI#, SMBALERT#, SYS_RESET#, USBRBIAS#



INTERNAL PULL-DOWN SIGNALS:
 AC_BITCLK, AC_RST#, AC_SDIN[2:0],
 AC_SDOUT, AC_SYNC, DPSPVPVR,
 LAN_CLK, PDD[7], PDDREQ, SPKR,
 USB[7:0][P,N]

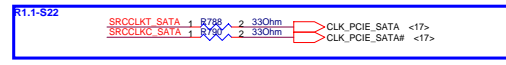
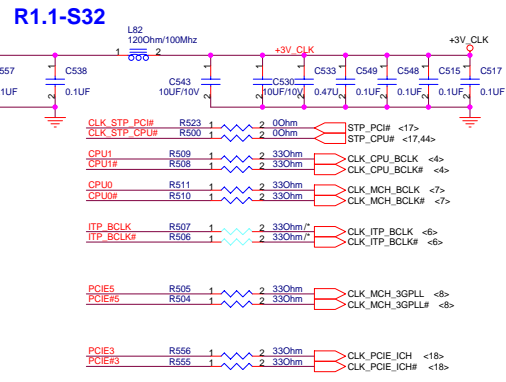
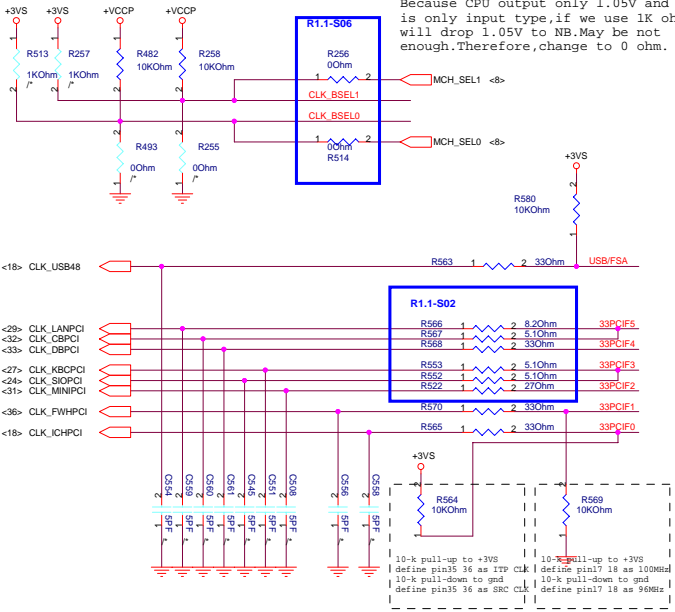
INTERNAL PULL-UP SIGNALS:
 EE_DIN, EE_DOUT, EE_CS,
 GPIO[17:16], LAD[3:0]#,
 LDRQ[0:1], LAN_RXD[2:0],
 PME#, PWRBTN#, TP3,
 SATALED#,
 GNT[4:0]



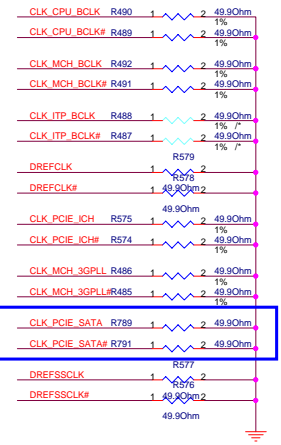


B STEP		
CPU_BSEL0	CPU_BSEL1	HOST CLOCK
0	0	133
1	0	100

Because CPU output only 1.05V and NB is only input type, if we use 1K ohm will drop 1.05V to NB. May be not enough. Therefore, change to 0 ohm.



PLACE termination close to clock gen.

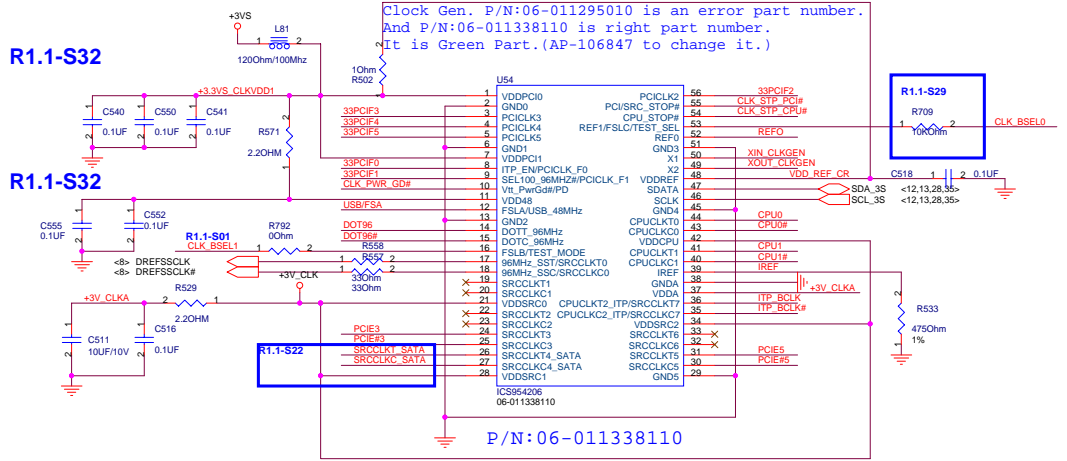


ICS ICS954206 FREQUENCY TABLE

FS_C	FS_B	FS_A	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266	100	33.33	14.318	48.00	96.00
0	0	1	133	100	33.33	14.318	48.00	96.00
0	1	0	200	100	33.33	14.318	48.00	96.00
0	1	1	166	100	33.33	14.318	48.00	96.00
1	0	0	333	100	33.33	14.318	48.00	96.00
1	0	1	100	100	33.33	14.318	48.00	96.00
1	1	0	400	100	33.33	14.318	48.00	96.00
1	1	1				reserved	14.318	48.00

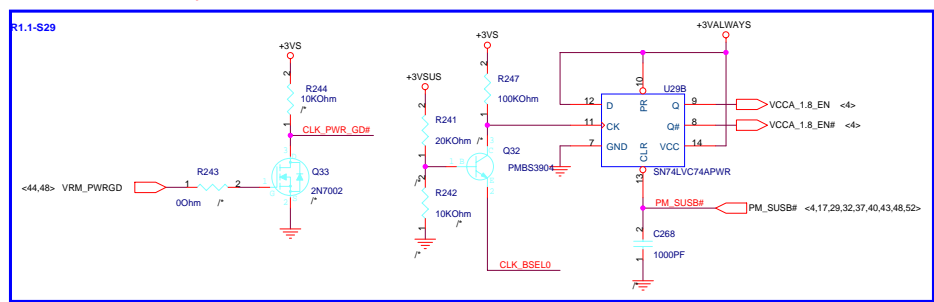
R1.1-S32

R1.1-S32



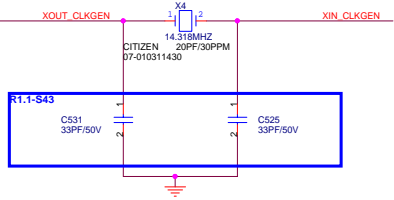
Clock Gen. P/N:06-011295010 is an error part number. And P/N:06-011338110 is right part number. It is Green Part. (AP-106847 to change it.)

P/N:06-011338110

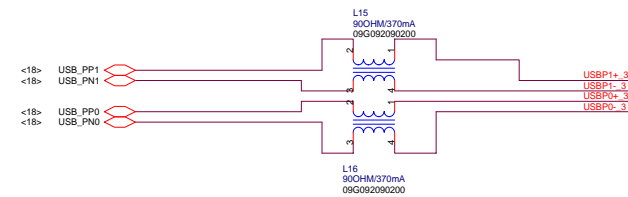
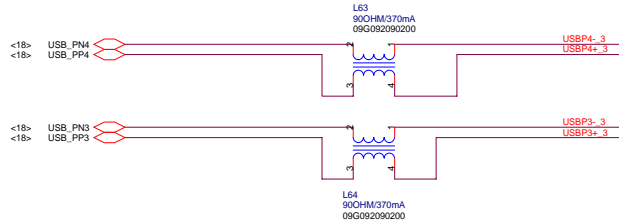
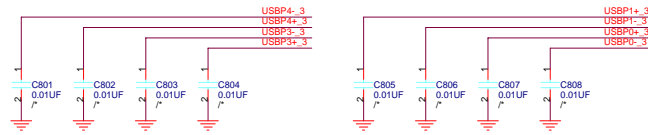


74HC74 TRUTH TABLE

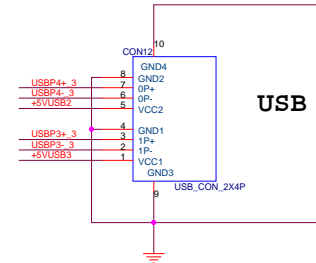
PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'



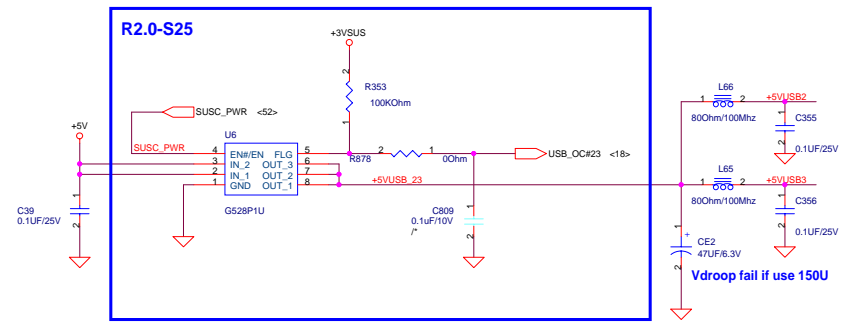
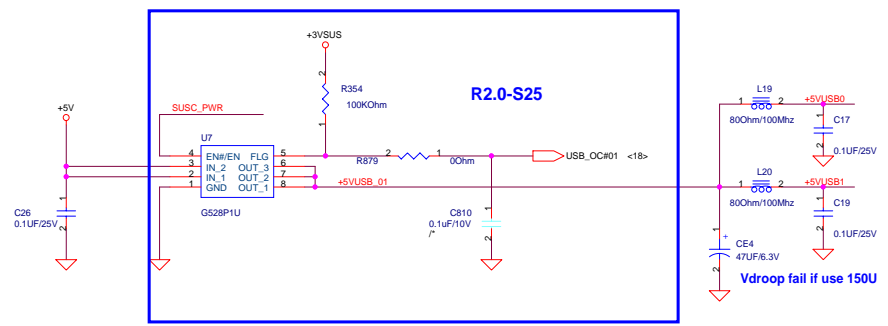
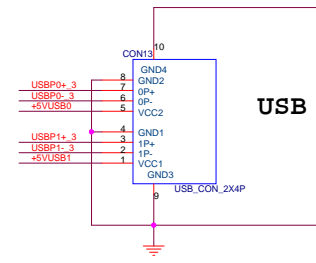
RESERVE 0402 PAD for USB ESD diode.



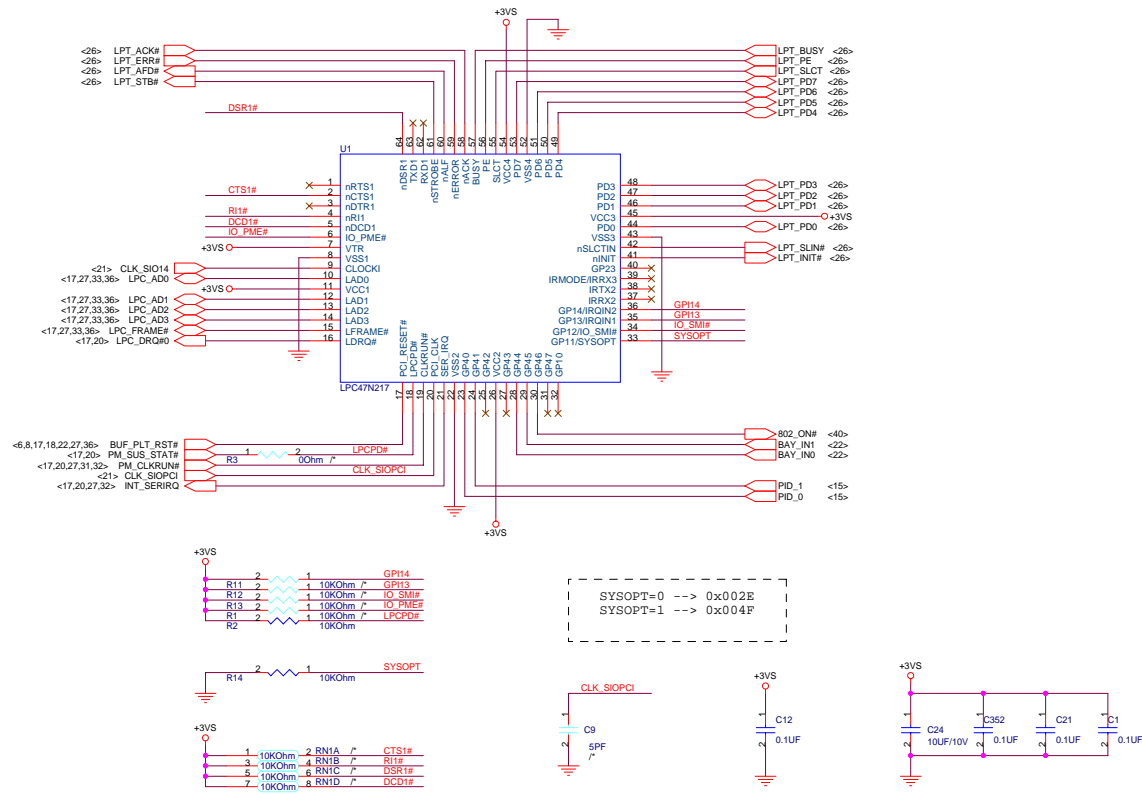
CON Part Number Modify as ME

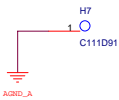
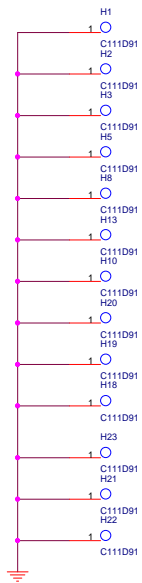


CON Part Number Modify as ME



Super I/O

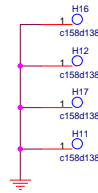




FIXED HOLE



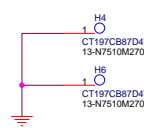
CPU



R1.1-S13

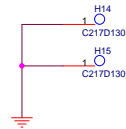
Need to change part number in BOM to 13-N7510M270. R1.1 has changed it in symbol.

MDC_NUT



MDC_NUT
Type:SMD TOP SIDE
Part Number :13-N7510M270

North bridge heatsink nut



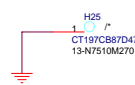
North bridge heatsink nut
Type:SMD TOP SIDE
Part Number :13-N9980M100

R1.1-S16

EMI request.

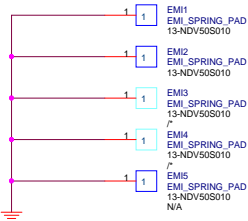
Need to change part number in BOM to 13-N7510M270. R1.1 has changed it in symbol.

Place Below X1



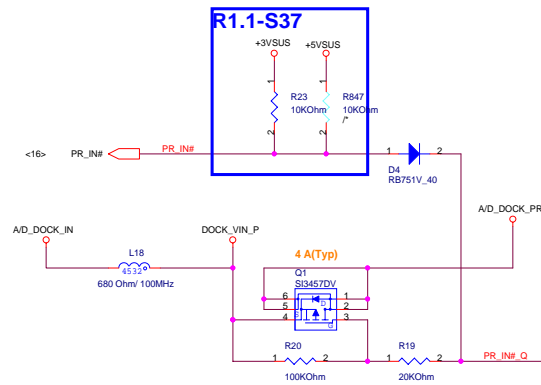
For EMI DDR Finger spring.
Need to add part number.

R2.0-S20
EMI request.

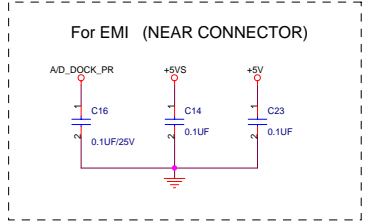


EMI SPRING
Type:SMD BOTTOM SIDE
Part Number :13-NDV50S010

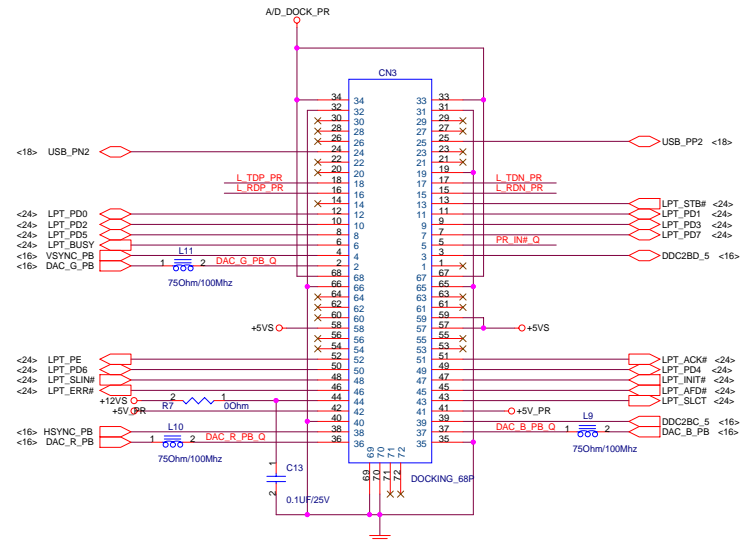
← FOR TOP EMI SPRING.



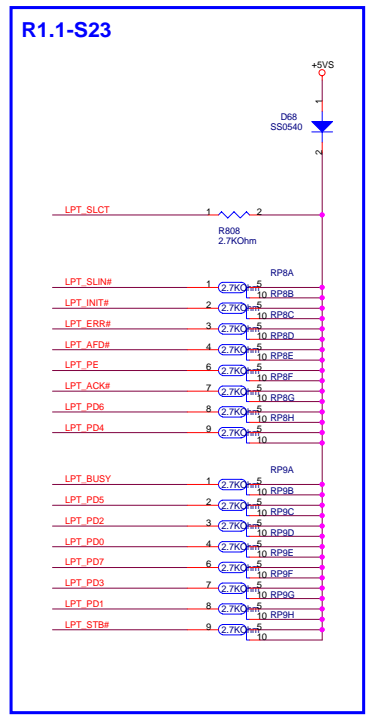
R1.1-S04



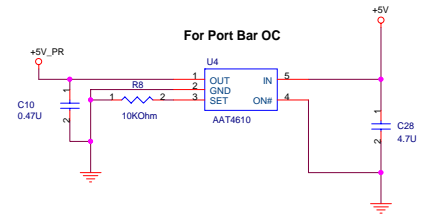
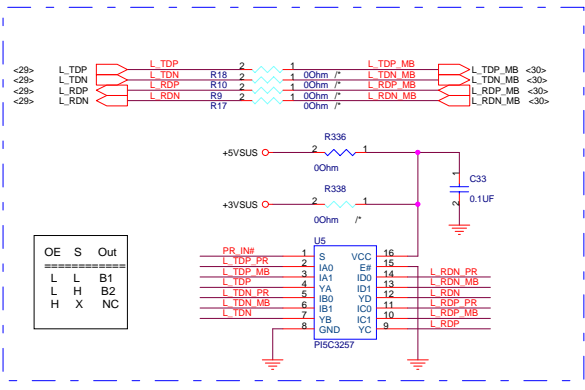
For EMI (NEAR CONNECTOR)



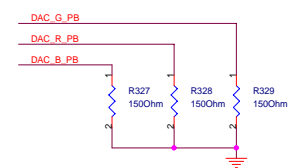
PORT BAR III



R1.1-S23



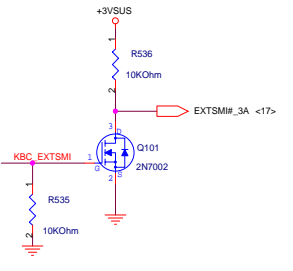
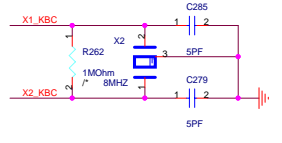
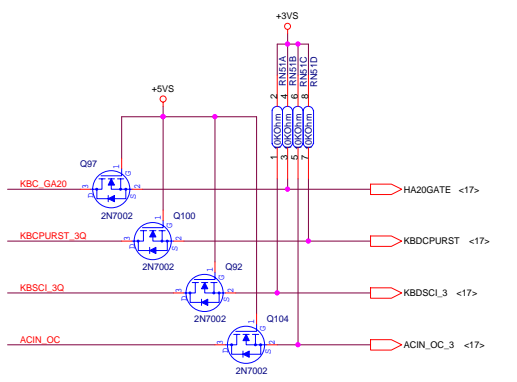
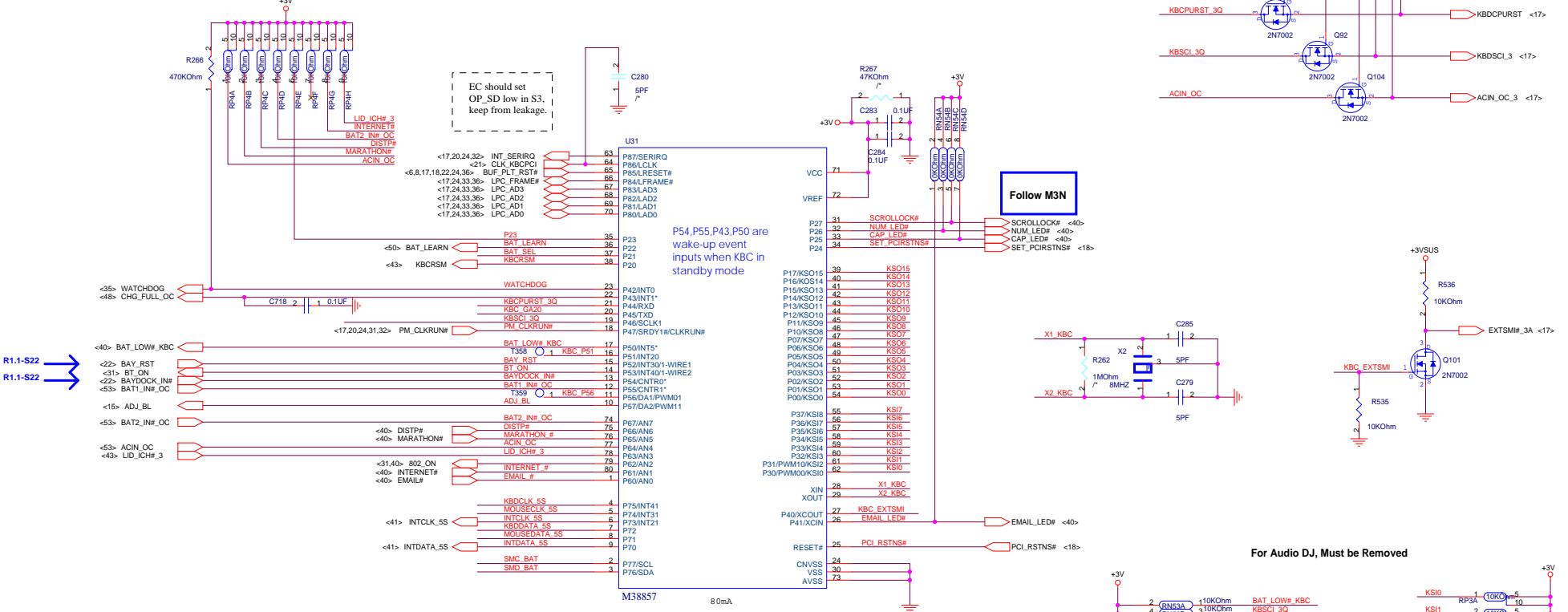
For Port Bar OC



P2.1 Low : Power Button Override disable
 Input Event only at P54, P55, P60 - P67

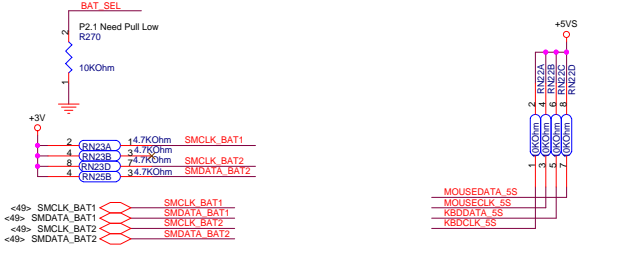
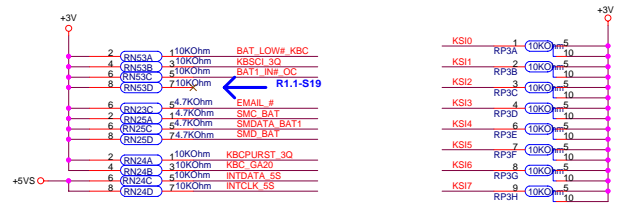
P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set
 OP_SD low in S3,
 keep from leakage.



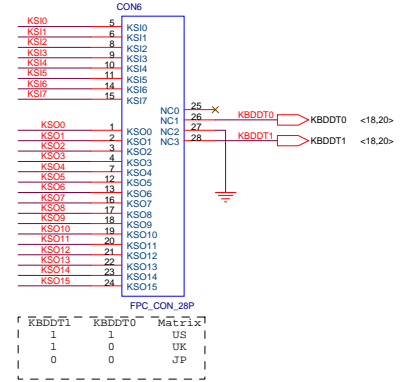
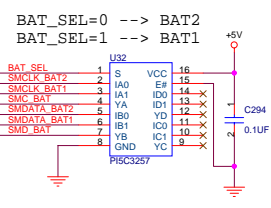
R1.1-S22
 R1.1-S22

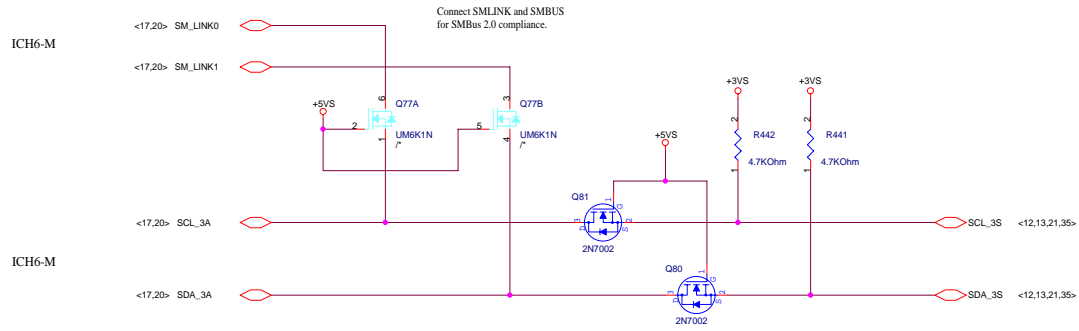
For Audio DJ, Must be Removed



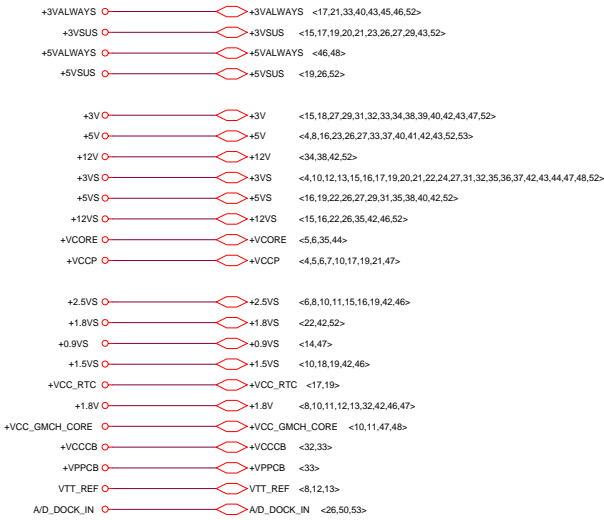
KEYBOARD CONN

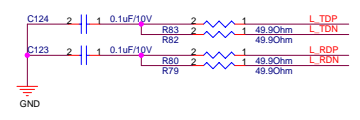
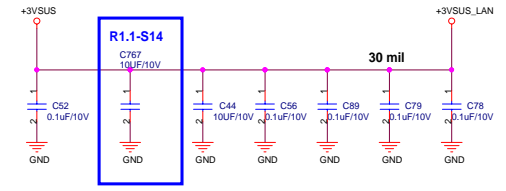
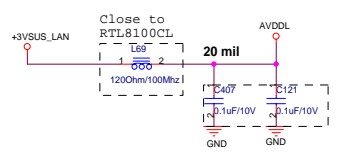
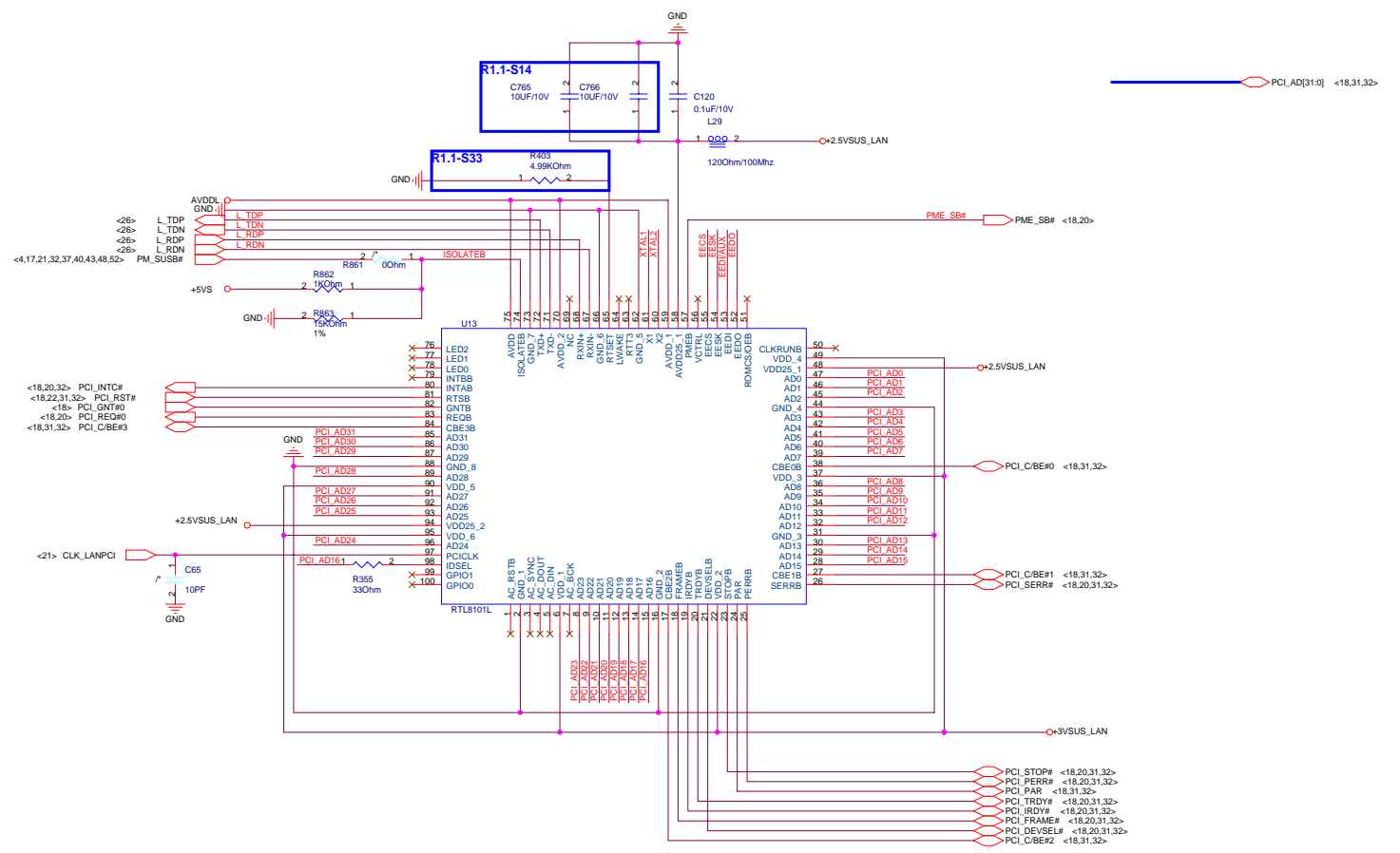
CON Part Number Modify as M3N



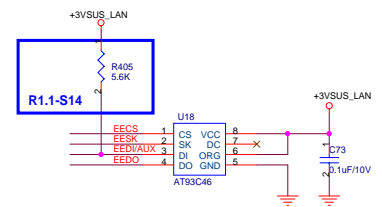
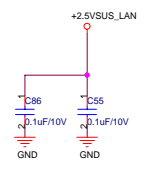


Thermal Sensor,
Clock Generator
DDR2 SO-DIMM
TPM

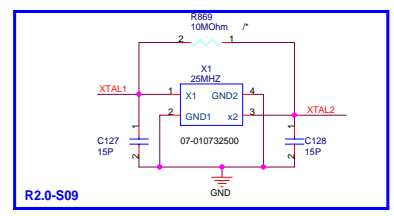




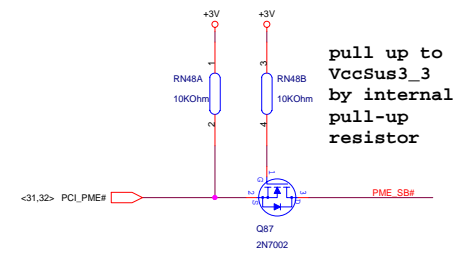
R1.1-S32



The Crystal should be placed far away from I/O ports, important or High Frequency signal traces (Tx, Rx, power), magnetics or board edges.



X1 Main Source is 07-010732500 (Fujicom)
 Second source is 07-010212500 (TXC)
 Symbol is changed to 07-010732500.



pull up to VccSus3.3 by internal pull-up resistor

TO MDC CONN.

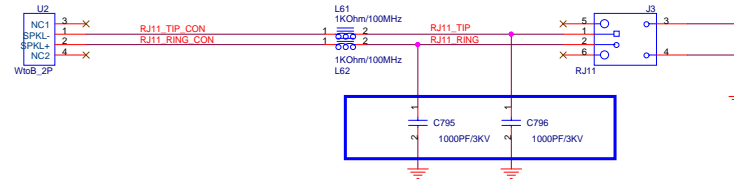
P/N:12-17000021

CON Part Number Modify as ME

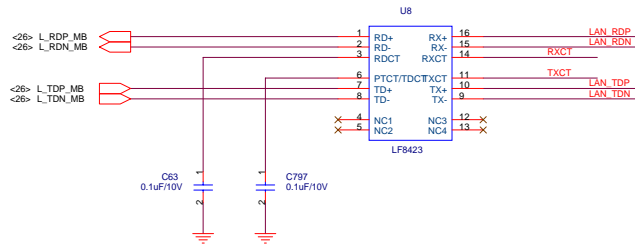
RJ11 CONNECTOR

P/N:12-142111060

CON Part Number Modify as ME

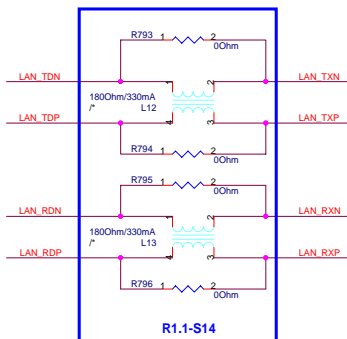


The 10/100M magnetics U3701 should be placed as close as possible to the J3701 connector.



To improve symmetry.

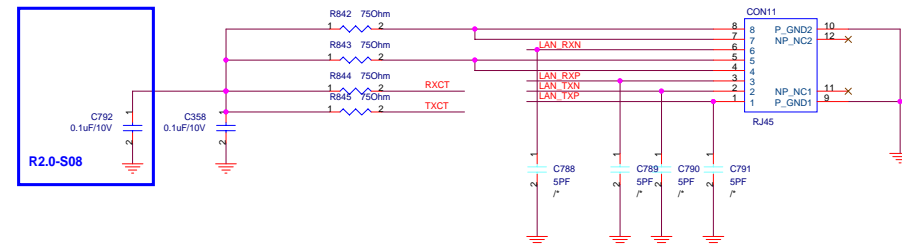
FOR EMI



LAN RJ45 CONNECTOR

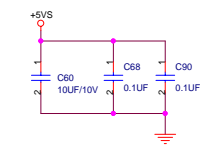
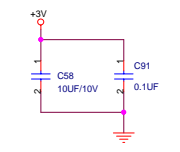
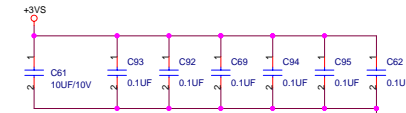
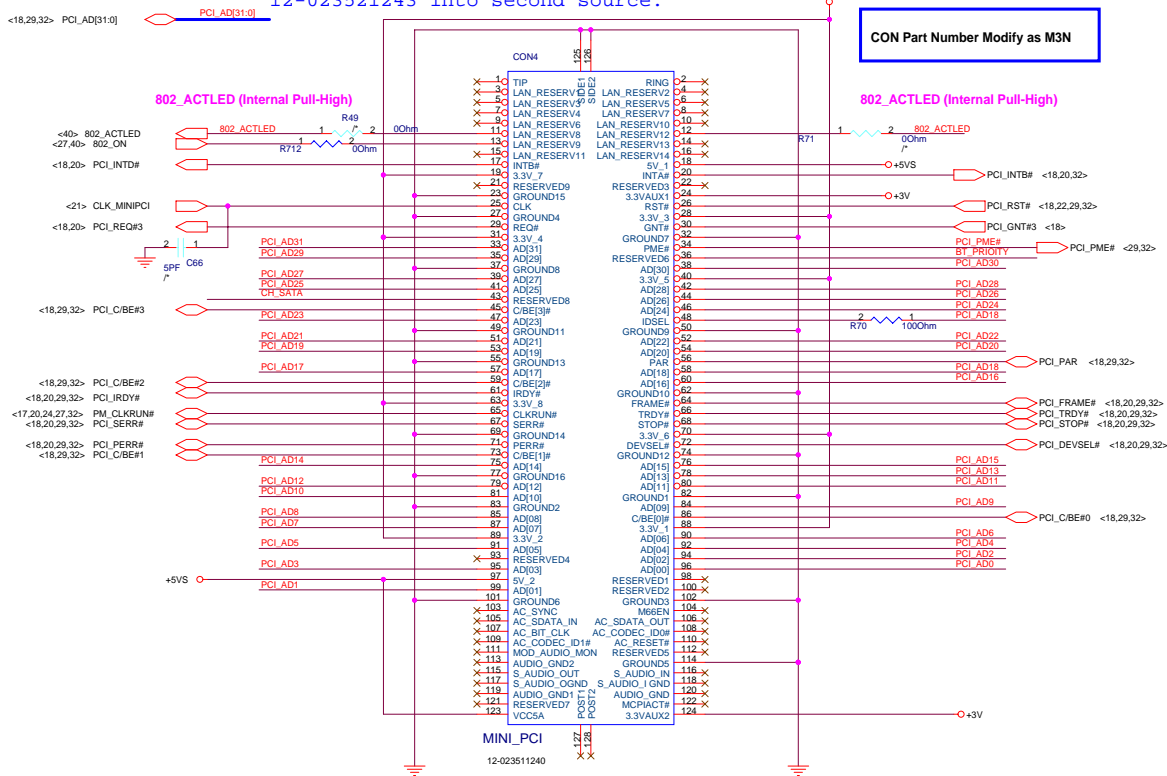
P/N:12-140111080

CON Part Number Modify as ME

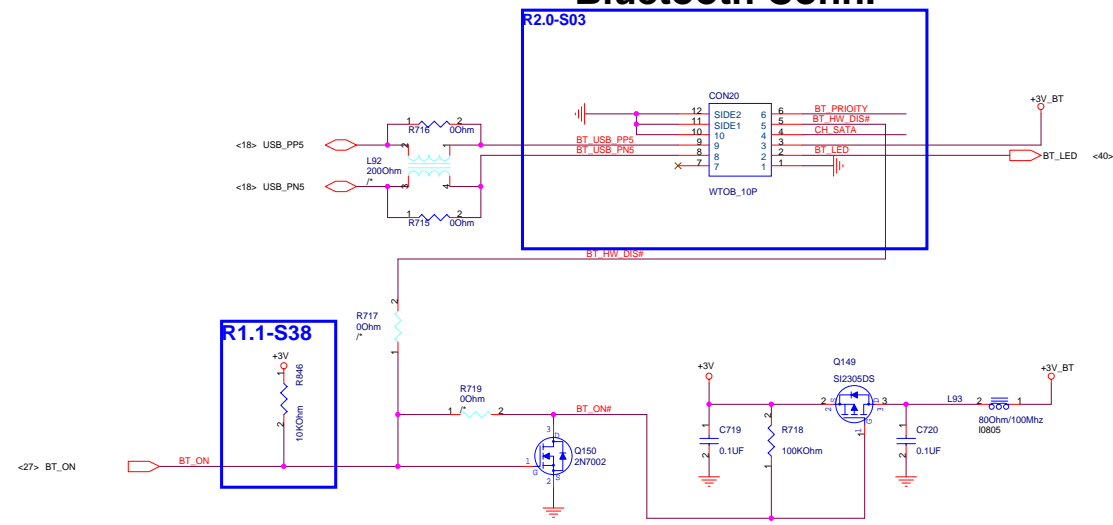


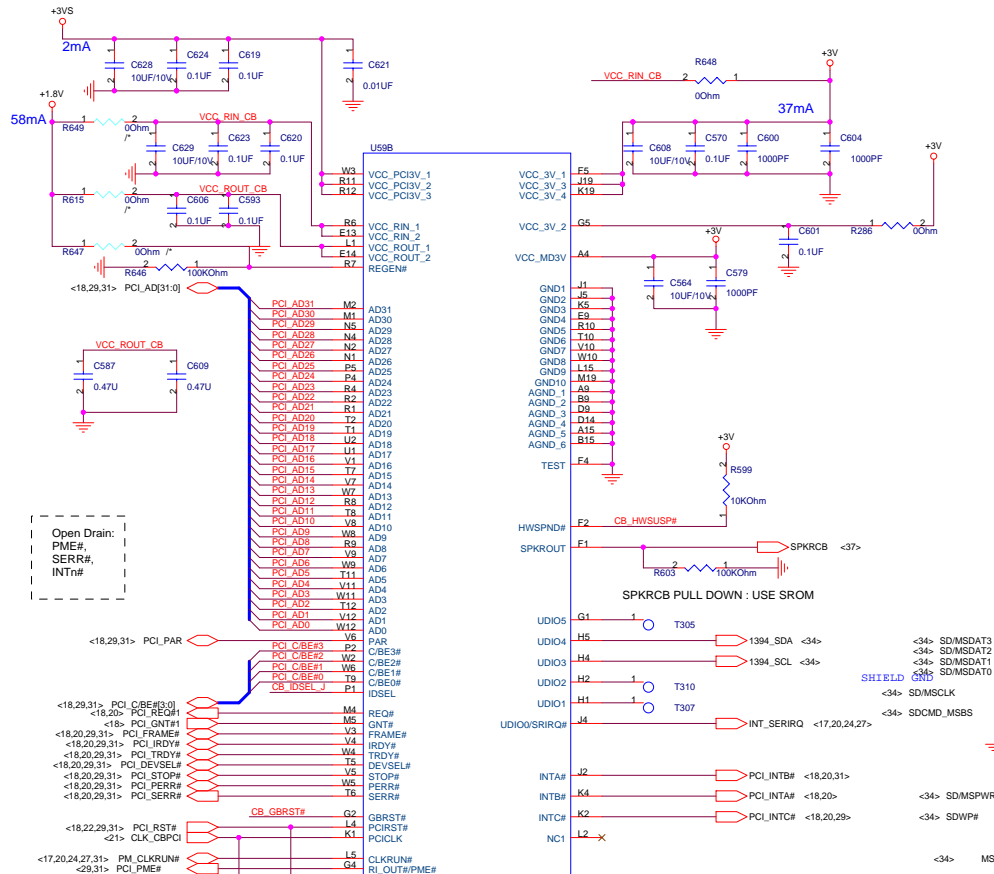
MINIPCI CONNECTOR

MINIPCI Connector (P/N:12-023511240) need to add 12-023521243 into second source.



Bluetooth Conn.





Open Drain:
PME#,
SERR#,
INTn#

VCC_3V POWER :
PME#, SPKR_OUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1#, VS2#
TEST, VCC5EN, VCC3EN#,
VPPEN0, VPPEN1, SD/MS I/F

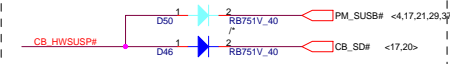
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO, CSTSCHG



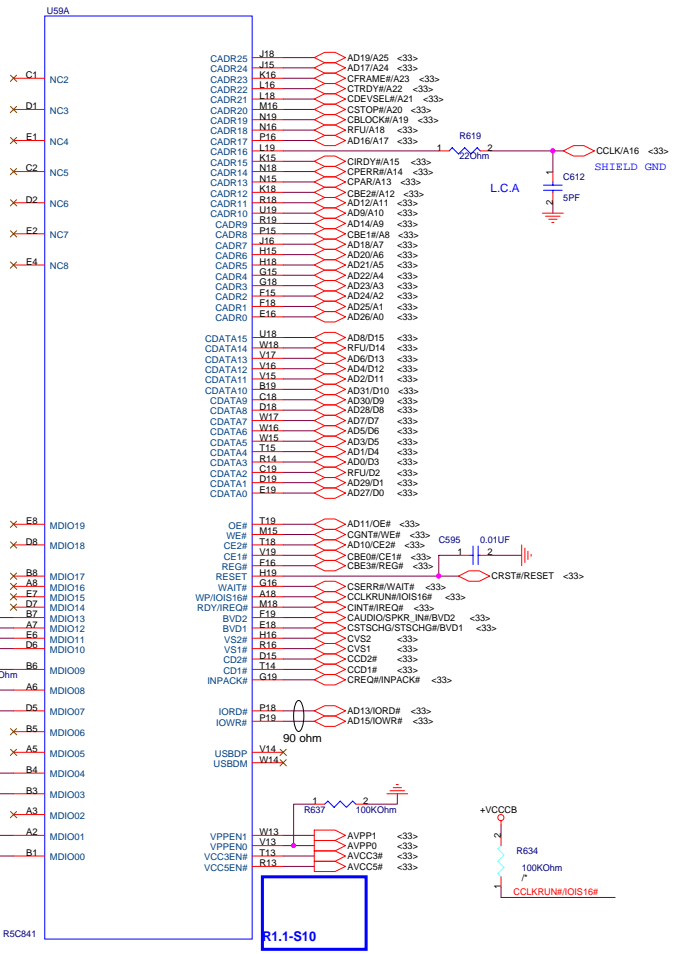
MDIO00->	SD Card Detect
MDIO01->	MS Card Detect
MDIO02->	XD Card Enable
MDIO03->	SD Write Protect, XD Card Ready/Busy#
MDIO04->	SD/MS/XD Card Power0 Control
MDIO05->	XD Card Write Protect
MDIO06->	SD/MS/XD LED
MDIO07->	SD/MS External Clock
MDIO08->	SD Command/MS Bus State /XD Card Write Enable
MDIO09->	SD/MS Clock /XD Card Read Enable
MDIO10->	SD/MS/XD Data 0
MDIO11->	SD/MS/XD Data 1
MDIO12->	SD/MS/XD Data 2
MDIO13->	SD/MS/XD Data 3
MDIO14->	XD Data 4
MDIO15->	XD Data 5
MDIO16->	XD Data 6
MDIO17->	XD Data 7
MDIO18->	XD Card Command Latch
MDIO19->	XD Card Address Latch

GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==> PCIIRST#

HW SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO ==> PCIIRST# LO ==> +3VS OFF
RESUME : +3VS ON ==> PCIIRST# HI ==> CB_HWSUSP# HI



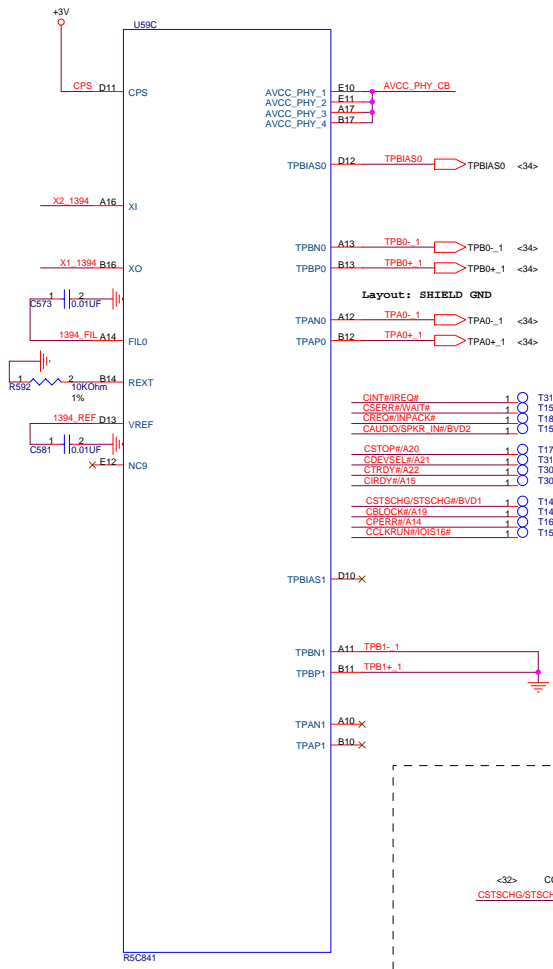
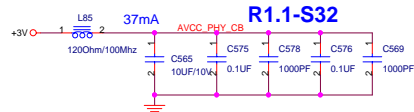
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 L : Disable XD



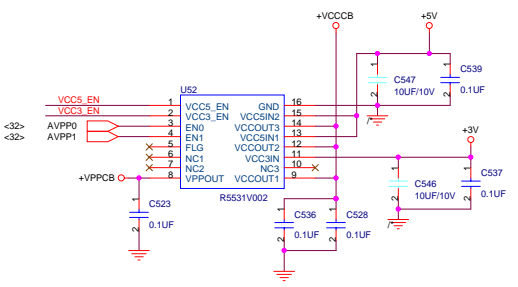
CRST#/RESET <-33>



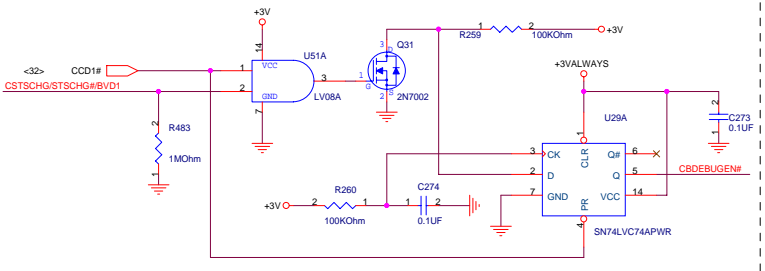
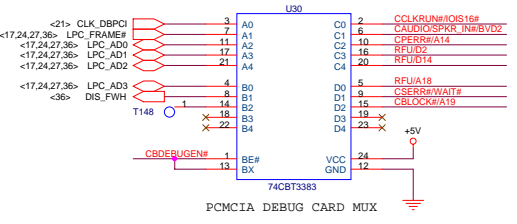
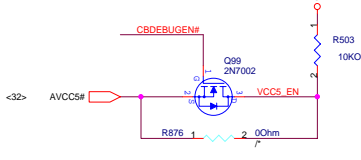
AVCC_PHYCB: Must not be off on the suspend mode because of the power supply for Cable interface block



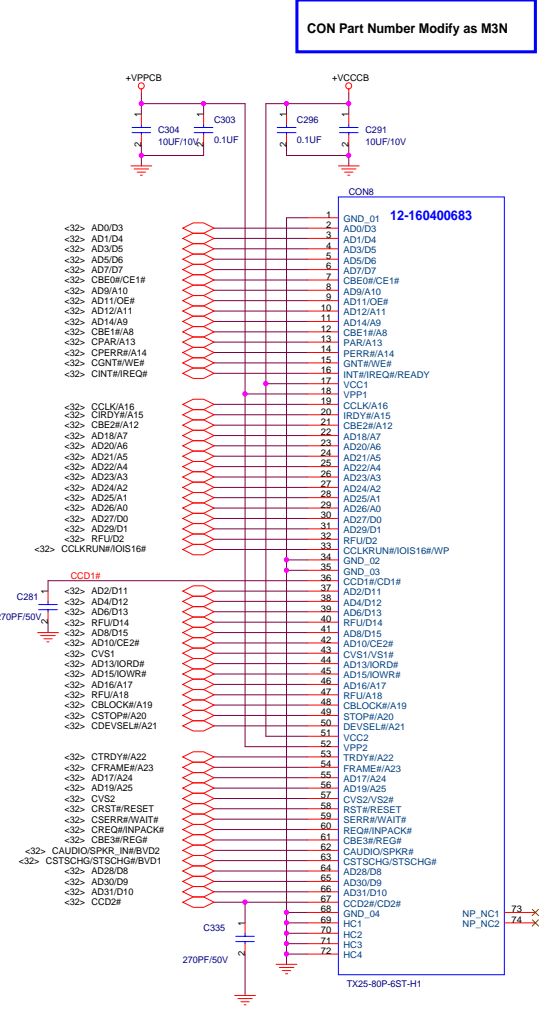
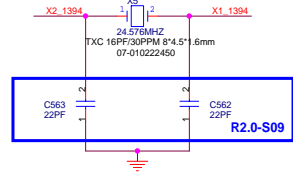
CINT#/#A20	1	T172
CDESEL#/#A21	1	T313
CTRDY#/#A22	1	T308
CRDY#/#A15	1	T303
CSTSCHG#/STSCHG#/#BVD1	1	T147
CBLOCK#/#A19	1	T149
CPERR#/#A14	1	T162
CCLKRUN#/#IOIS16#	1	T157



FOR PCMCIA DEBUG CARD
If delete debug card function, R876 and R628 mount 0 ohm.

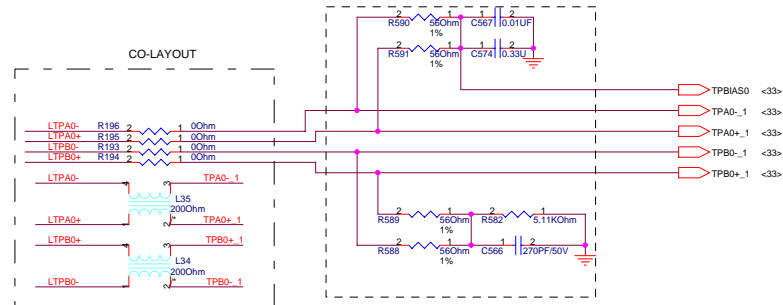
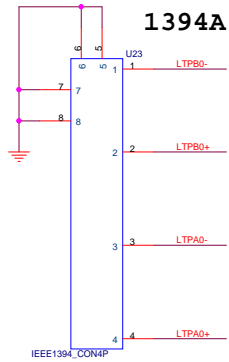


X5 Main Source is 07-010222450 (TXC)
Second source is 07-010722451 (Fujicom)

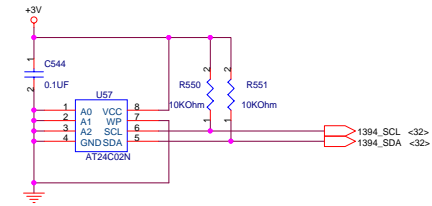


PCMCIA
 CCD1# CCD2#
 L L 16bit
 OTHER 32bit
 CL

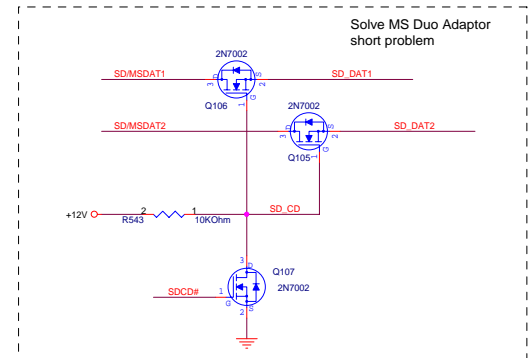
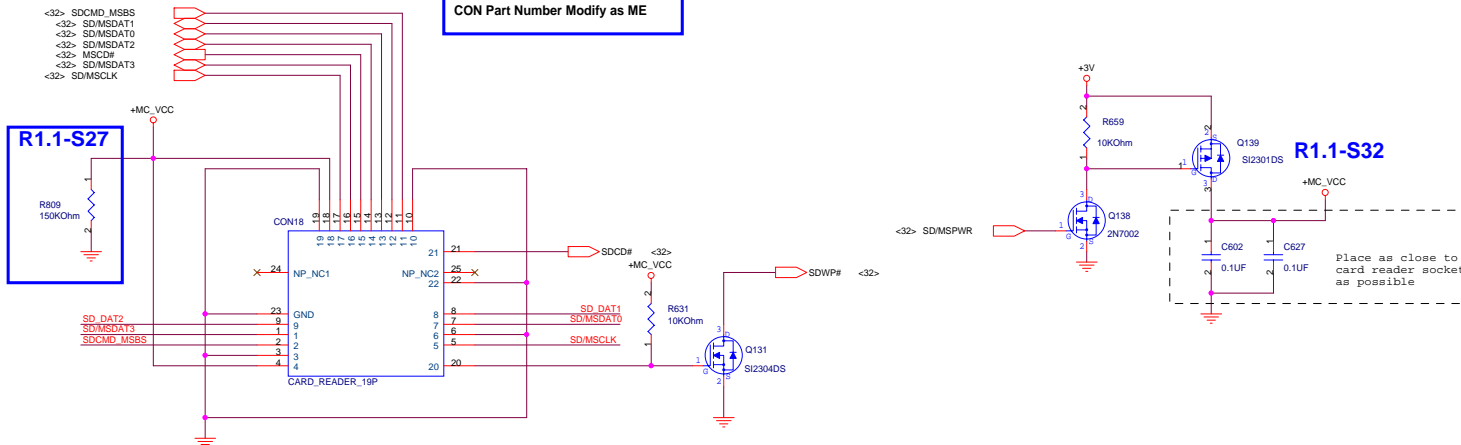
CON Part Number Modify as M3N

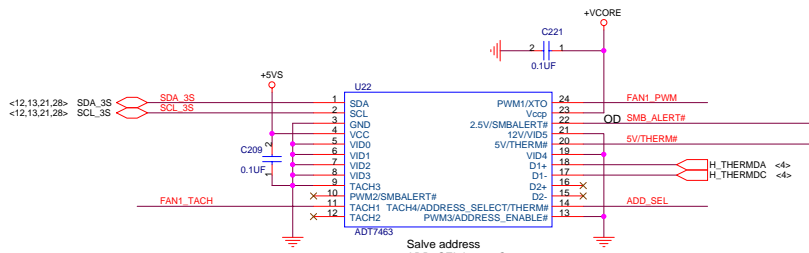


1. CLOSE TO R5C592
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend, maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm



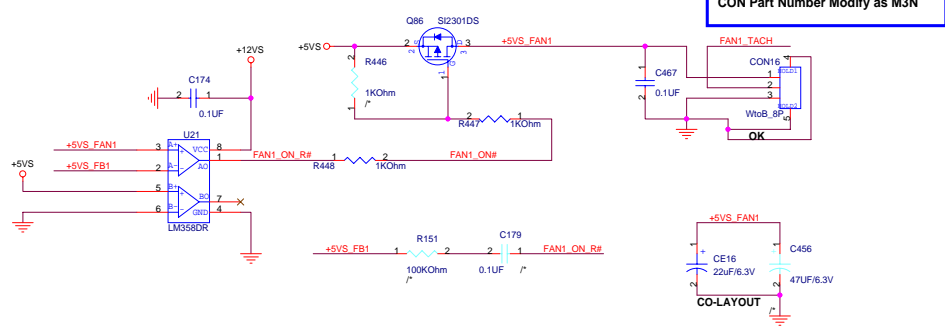
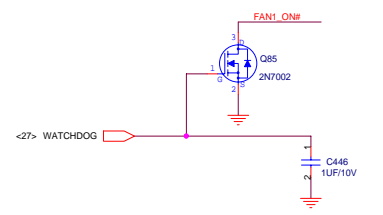
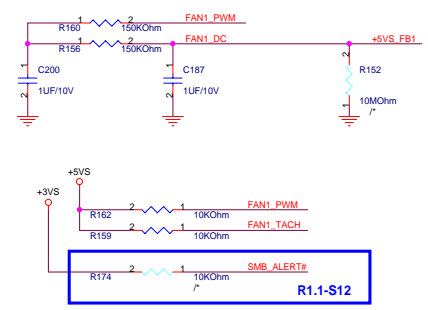
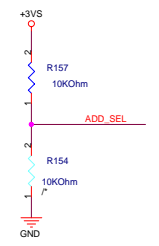
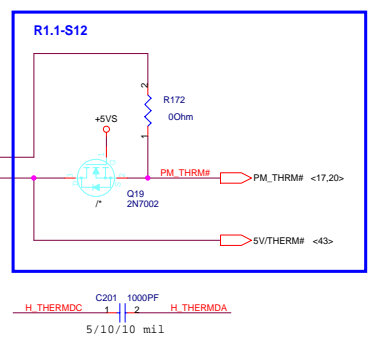
CON Part Number Modify as ME



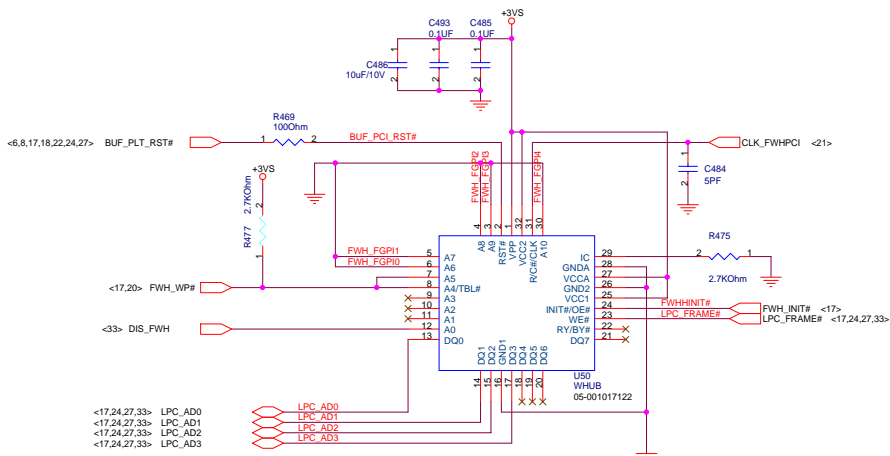


BIOS setting:
 105 degree will down CPU frequency.
 110 degree will shutdown system.

- PM_THRM# function select one
1. Fan full speed
 2. Fan full speed & Throttling function
 3. Fan full speed & Critical Shutdown



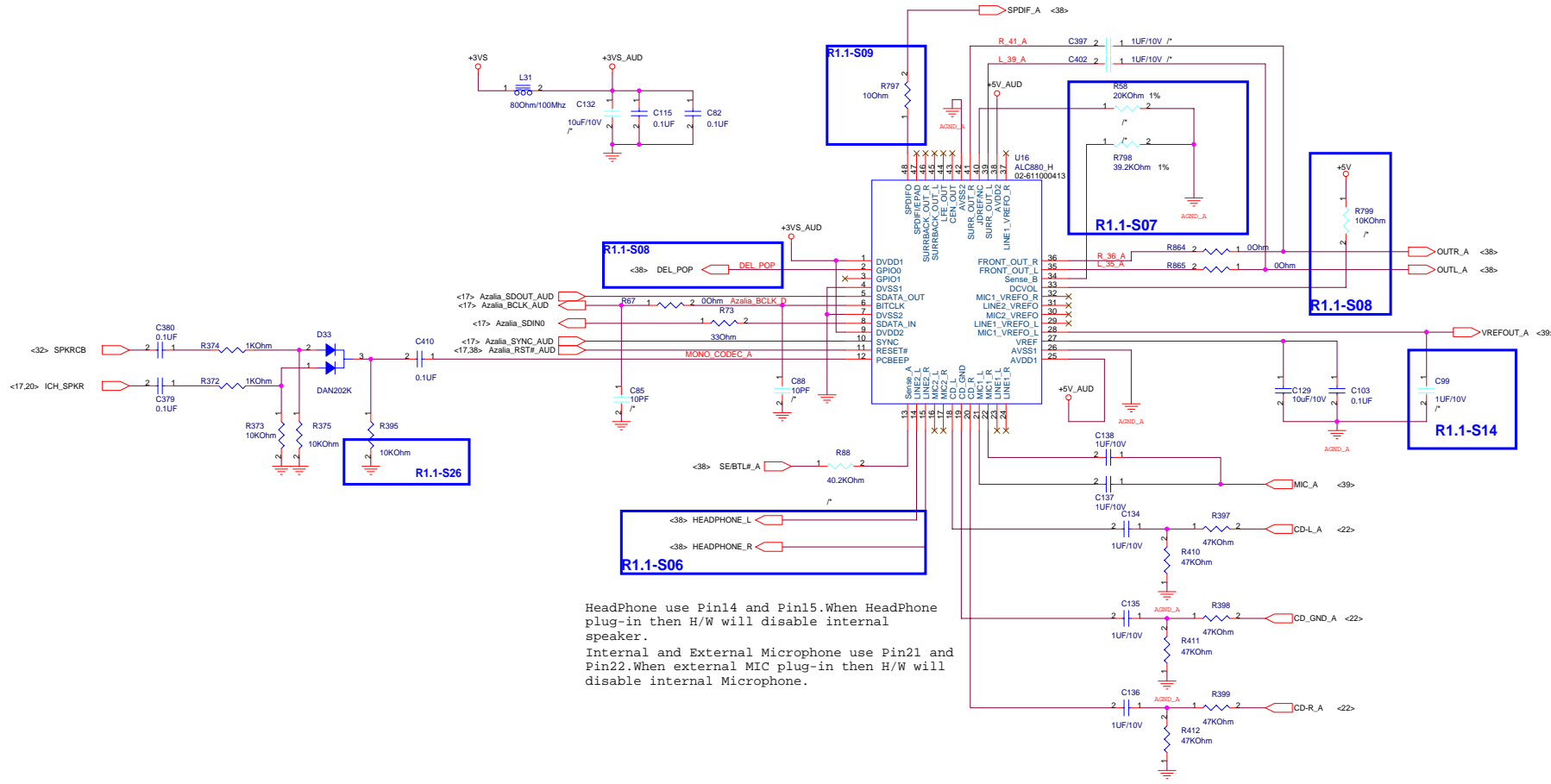
FWH BIOS SOCKET



FWH SOCKET(S/R and E/R use it.)
 Part Number :12-043000321
 FWH IC (P/R use it.)
 SST 49LF004A-33-4C-N
 Part Number :05-001017122

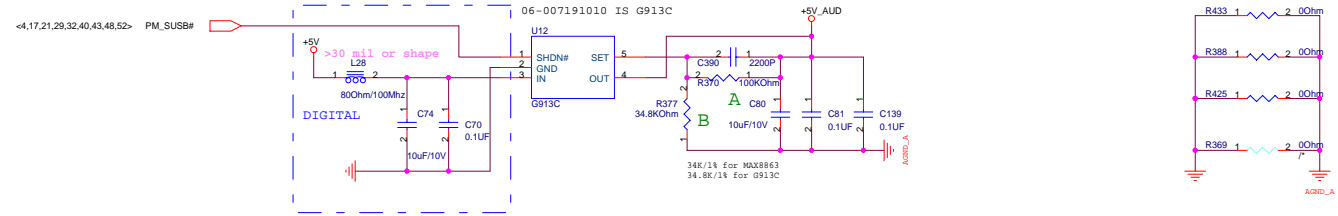
R2.0 has changed WHUB socket symbol
 to BIOS IC 05-001017122.

AMI BIOS LABEL P/N:15-135001010.
 It need to add in P/R 59-MID BOM by ME.



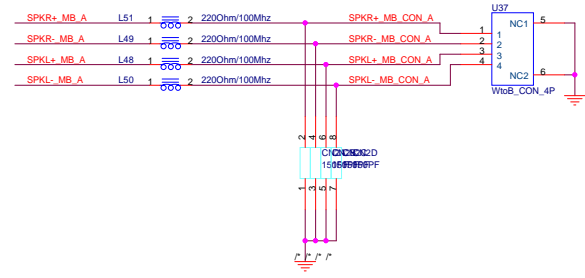
HeadPhone use Pin14 and Pin15. When HeadPhone plug-in then H/W will disable internal speaker.
 Internal and External Microphone use Pin21 and Pin22. When external MIC plug-in then H/W will disable internal Microphone.

$$V_{out} = 1.250 \cdot (1 + A/B) = 4.842$$

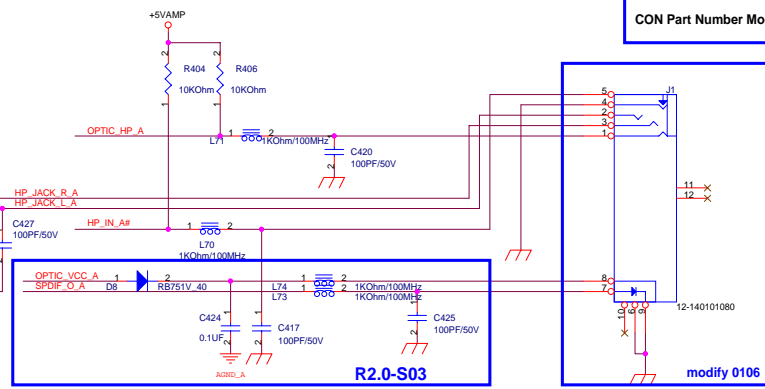


CON Part Number Modify as ME

GAIN0	GAIN1	SE/BTL#	AV (V/V)
0	0	0	-2 (DEFAULT)
0	1	0	-6
1	0	0	-12
1	1	0	-24
X	X	1	-1



CON Part Number Modify as ME

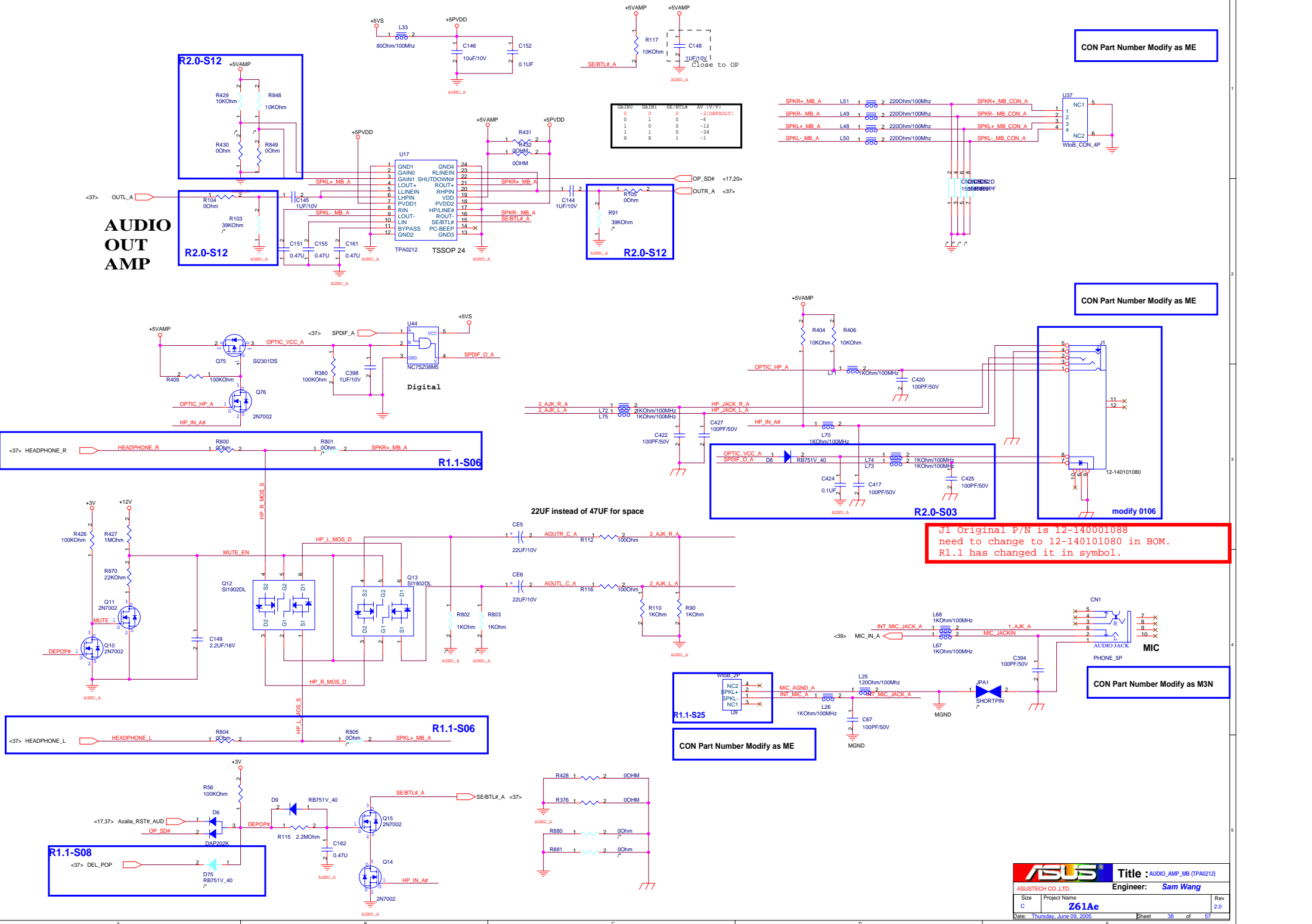


J1 Original P/N is 12-140001088 need to change to 12-140101080 in BOM. R1.1 has changed it in symbol.

CON Part Number Modify as M3N

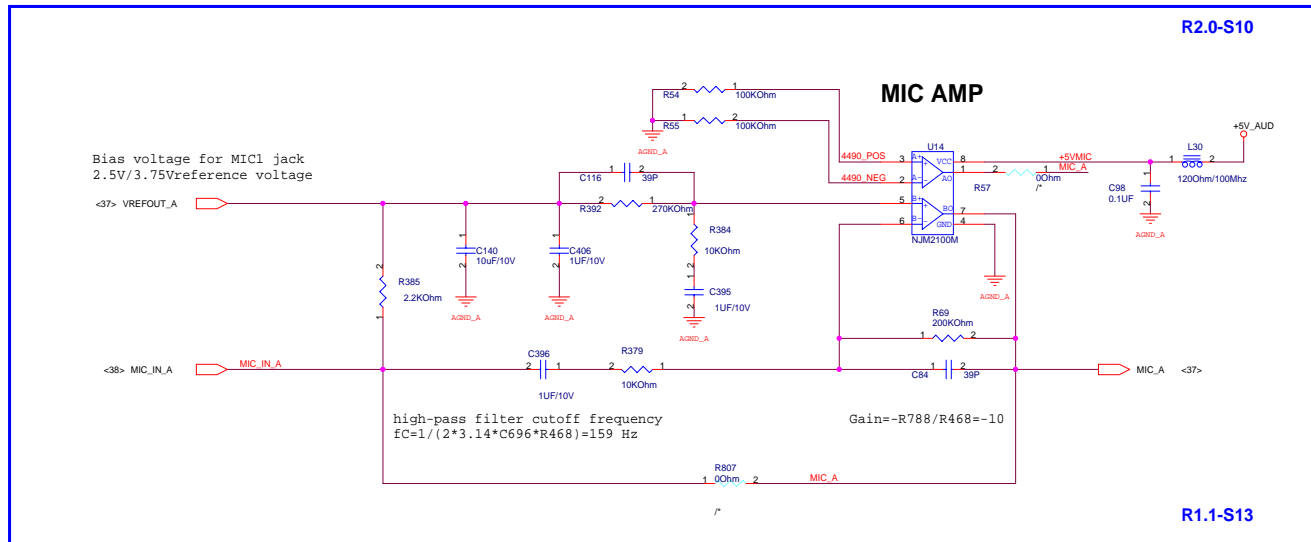
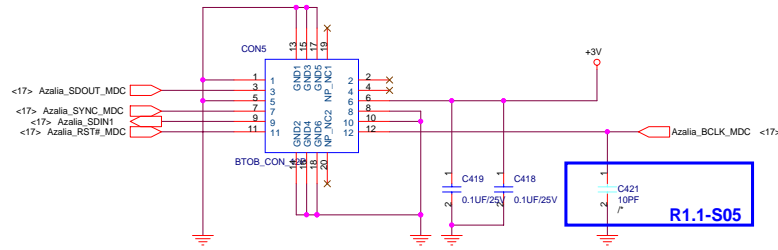
CON Part Number Modify as ME

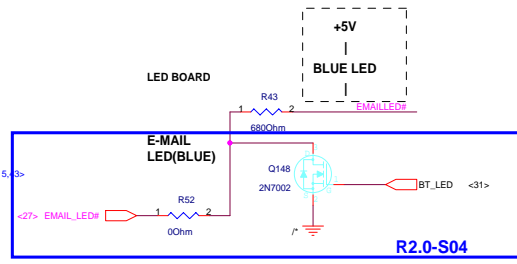
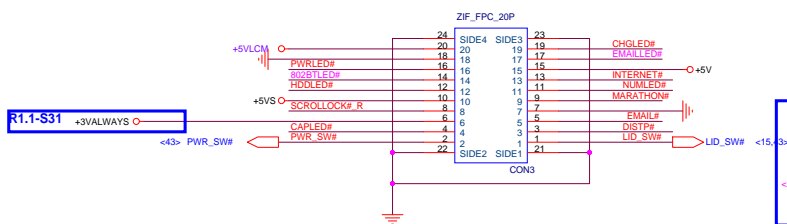
AUDIO OUT AMP



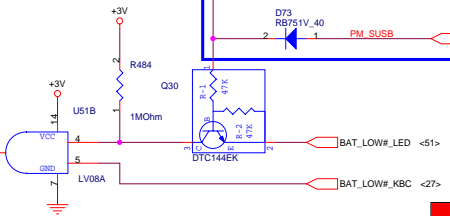
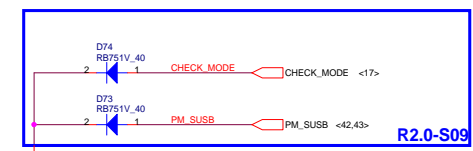
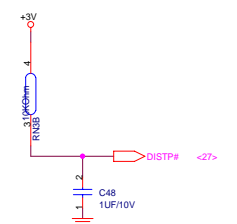
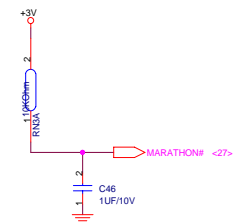
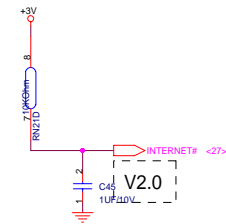
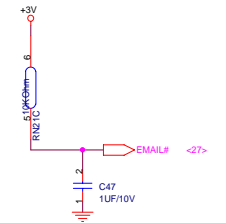
Azalia MDC MODEM

CON Part Number Modify as A4S

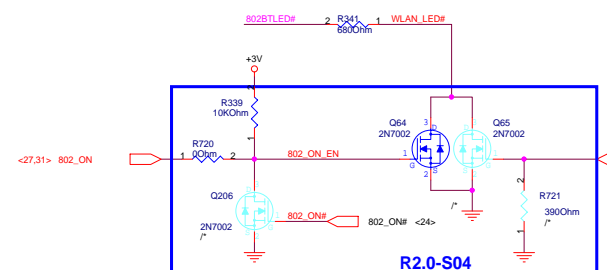
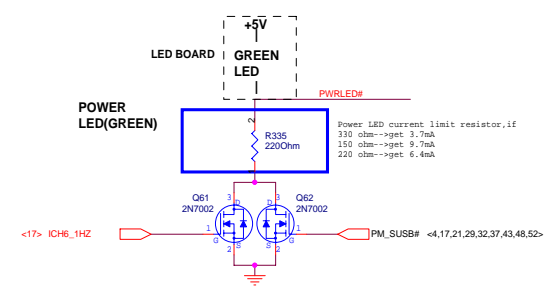
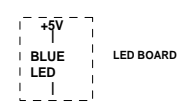
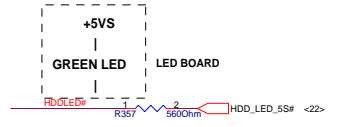
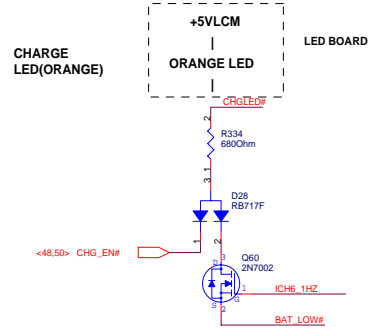
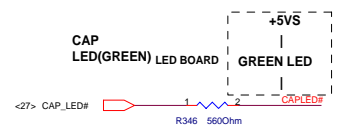
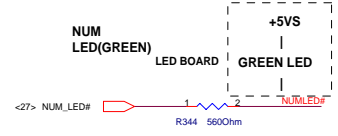
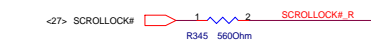




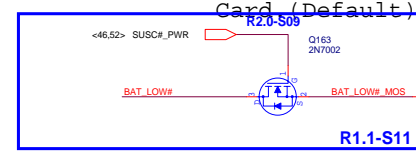
INSTANT KEY

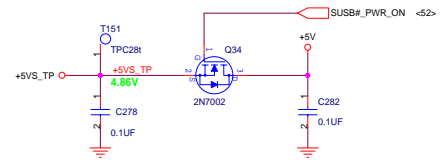


LED



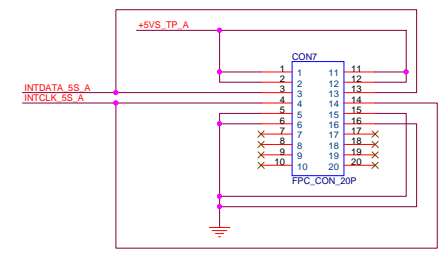
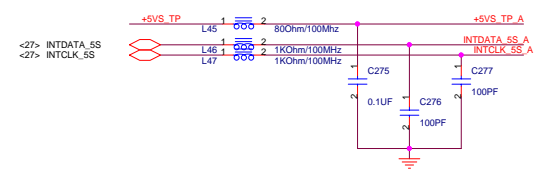
For ASUS WLAN Card. For Intel WLAN Card (Default)



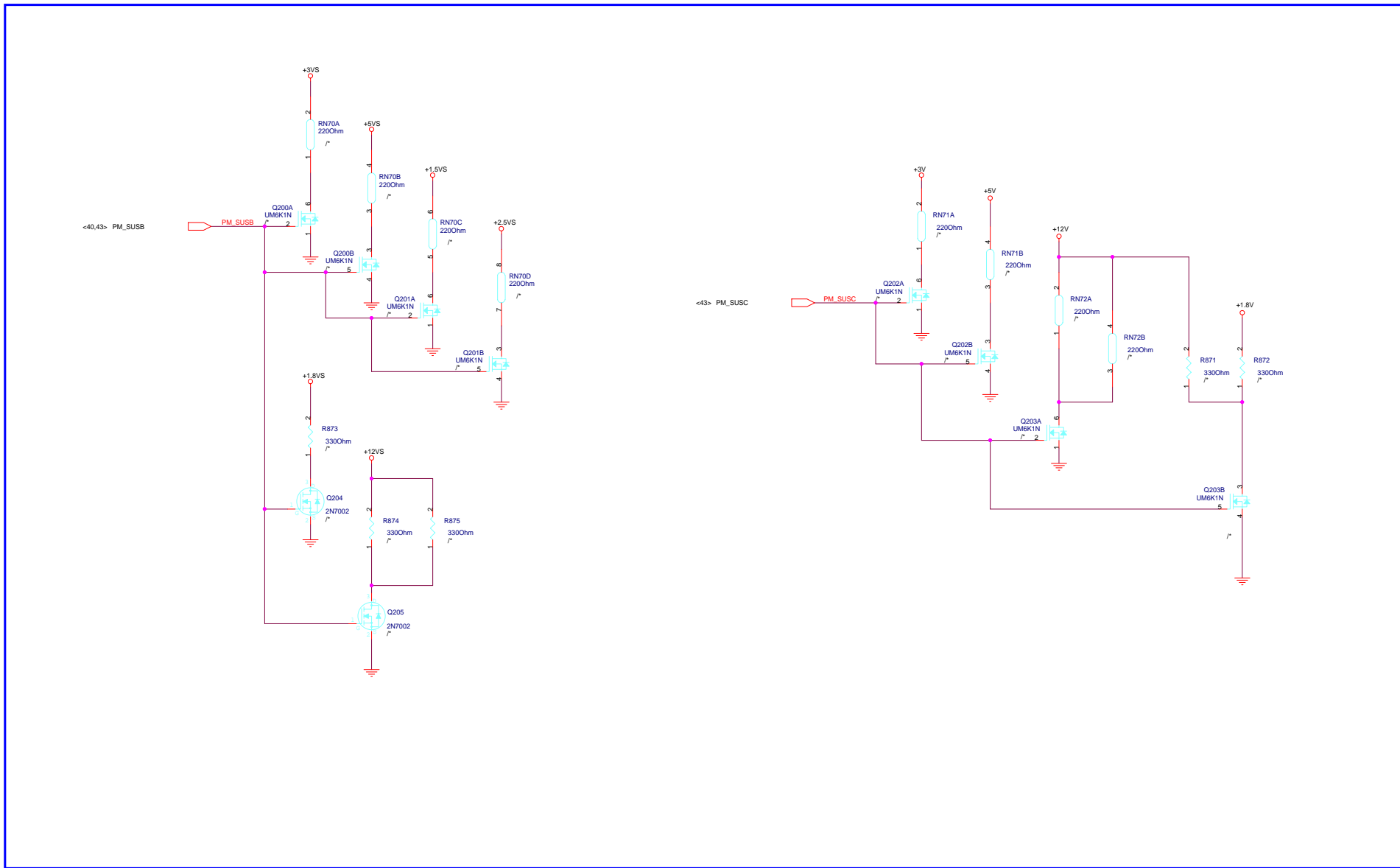


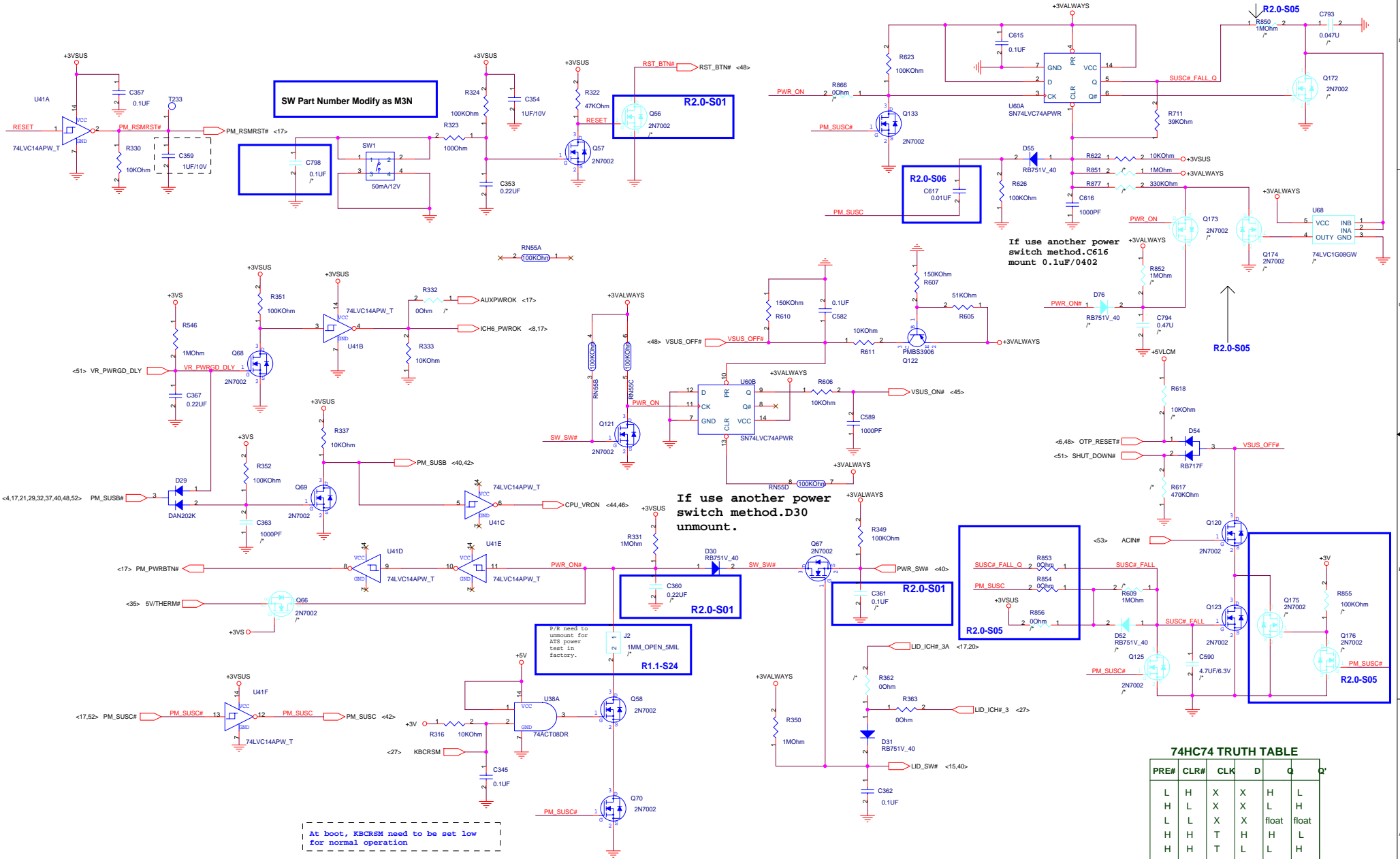
CON Part Number Modify as M3N

TOUCH PAD CNT



POWER DISCHARGE CIRCUIT





SW Part Number Modify as M3N

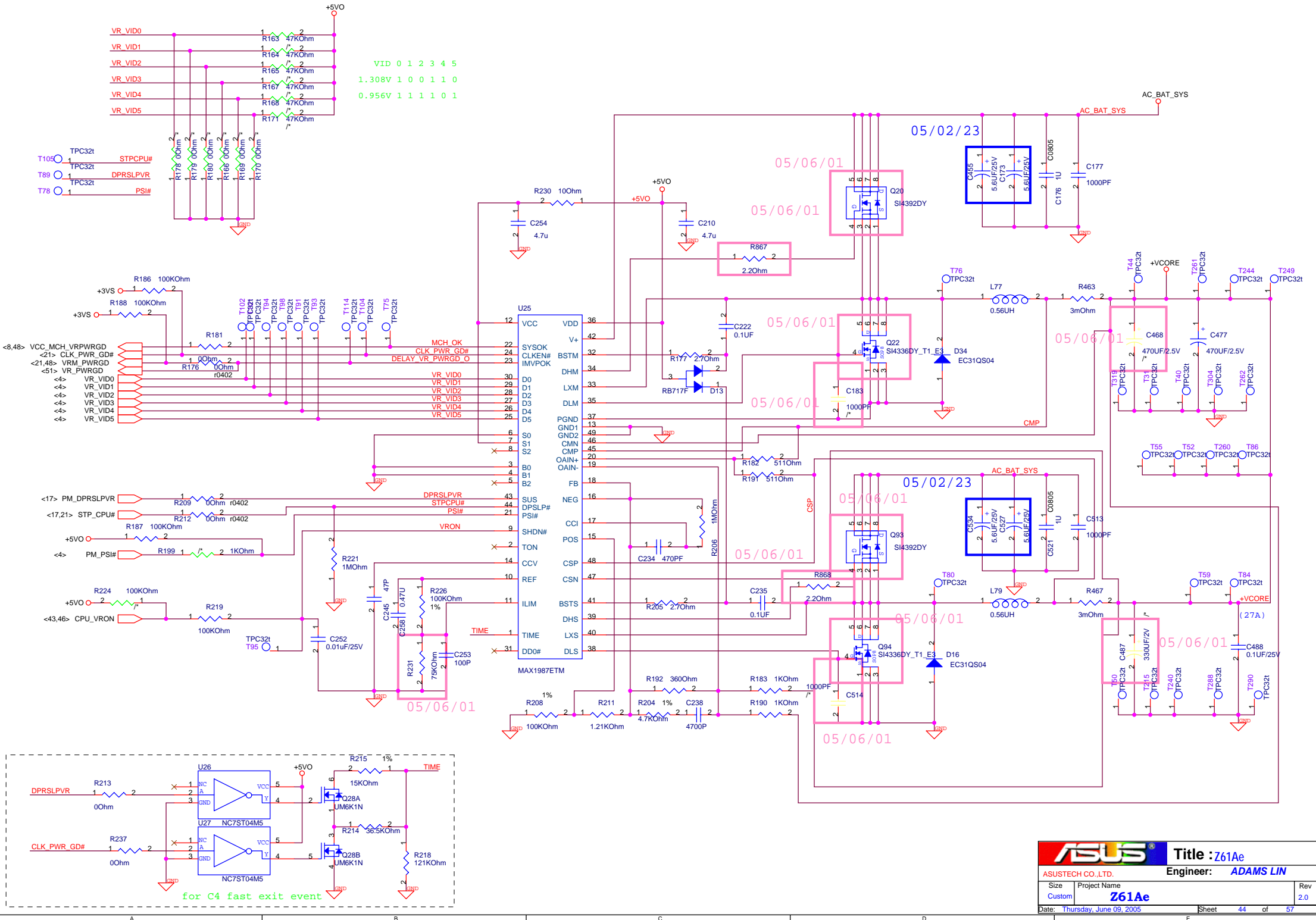
If use another power switch method.D30 unmount.

If use another power switch method.C616 mount 0.1uF/0402

At boot, KBCRSM need to be set low for normal operation

74HC74 TRUTH TABLE

PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

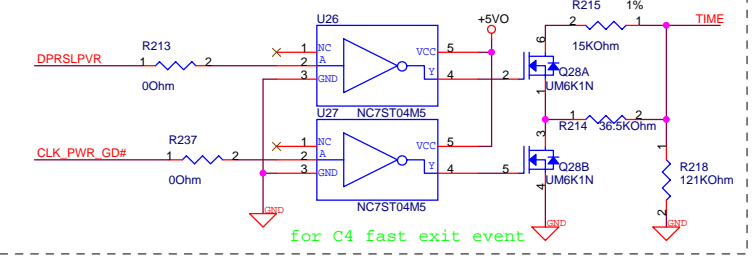


VID 0 1 2 3 4 5
 1.308V 1 0 0 1 1 0
 0.956V 1 1 1 1 0 1

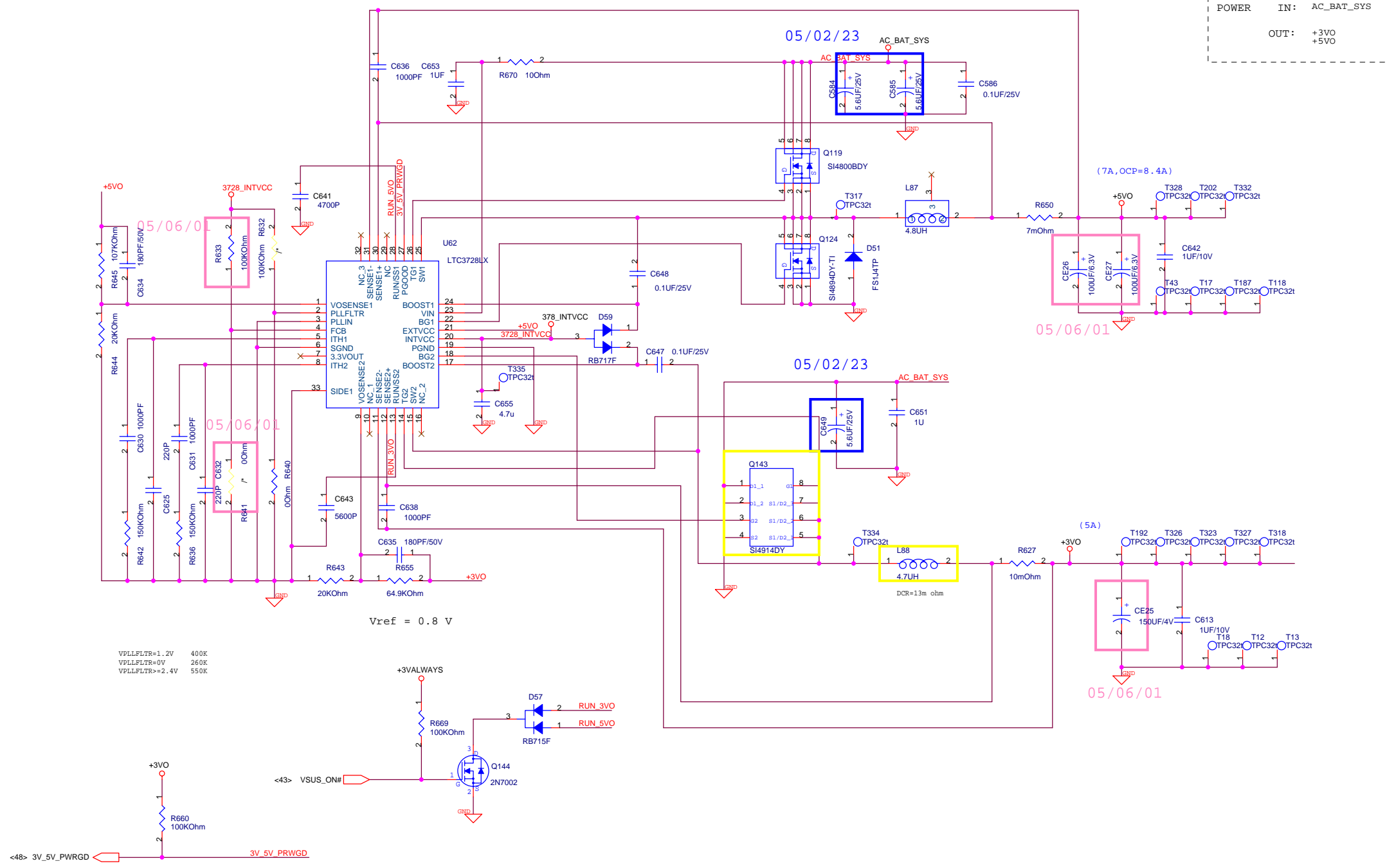
T105 TPC321 STPCPU#
 T89 TPC321 DPRSLPVR
 T78 TPC321 PSI#

<8,48> VCC_MCH_VRPWRGD
 <21> CLK_PWR_GD#
 <21,48> VRM_PWRGD
 <51> VR_PWRGD
 <4> VR_VID0
 <4> VR_VID1
 <4> VR_VID2
 <4> VR_VID3
 <4> VR_VID4
 <4> VR_VID5

<17> PM_DPRSLPVR
 <17,21> STP_CPU#
 +5V PM_PSI#
 +5V CPU_VRON



SIGNAL IN: VSUS_ON#
 POWER IN: AC_BAT_SYS
 OUT: +3VO
 +5VO



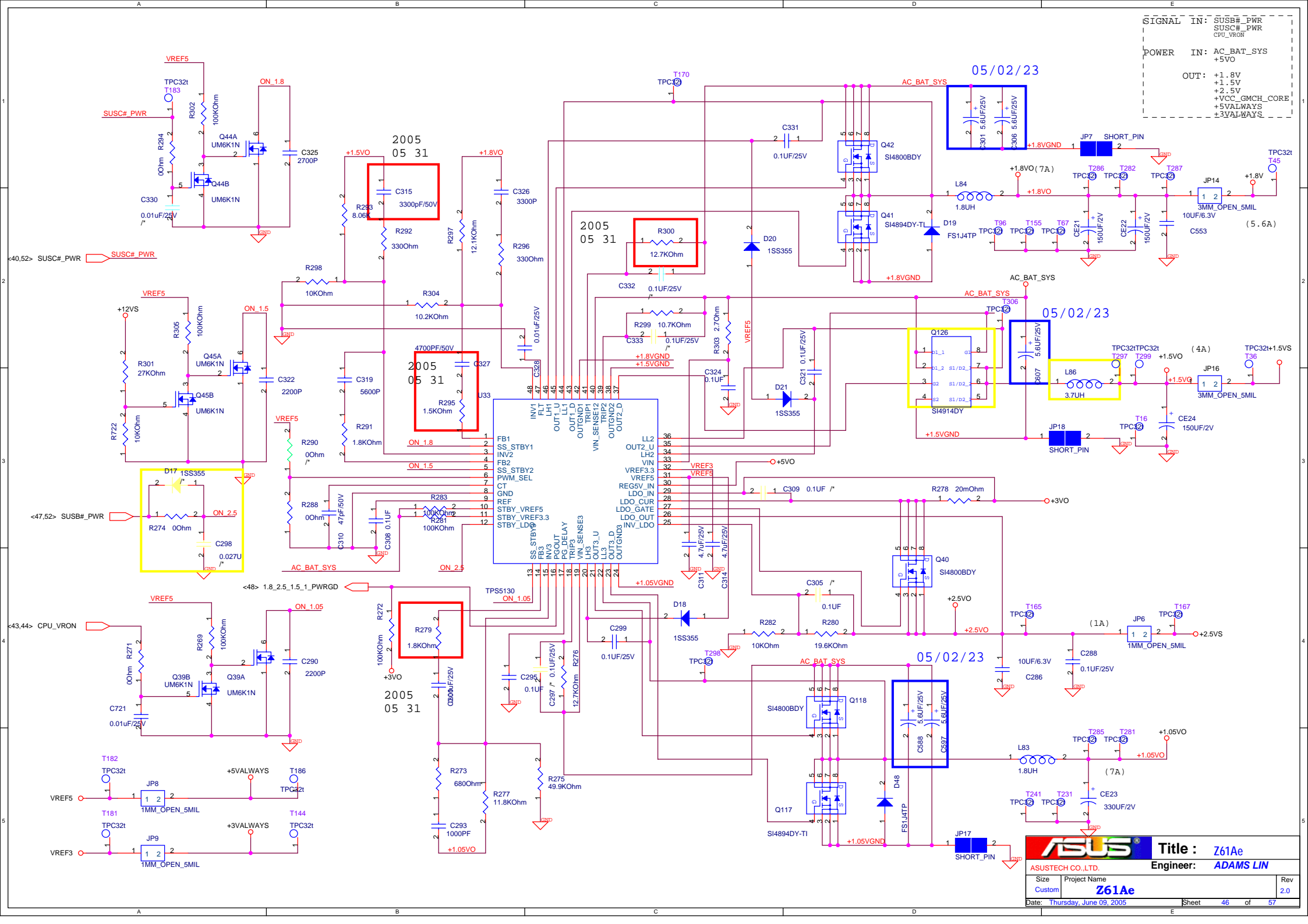
VLLFLTR=1.2V 400K
 VLLFLTR=0V 260K
 VLLFLTR=2.4V 550K

ASUS		Title : Z61Ae
ASUSTECH CO.,LTD.		Engineer: ADAMS LIN
Size Custom	Project Name Z61Ae	Rev 2.0
Date: Thursday, June 09, 2005	Sheet 45	of 57

SIGNAL IN: SUSB#_PWR
 SUSB#_PWR
 CPU_VRON

POWER IN: AC_BAT_SYS
 +5V0

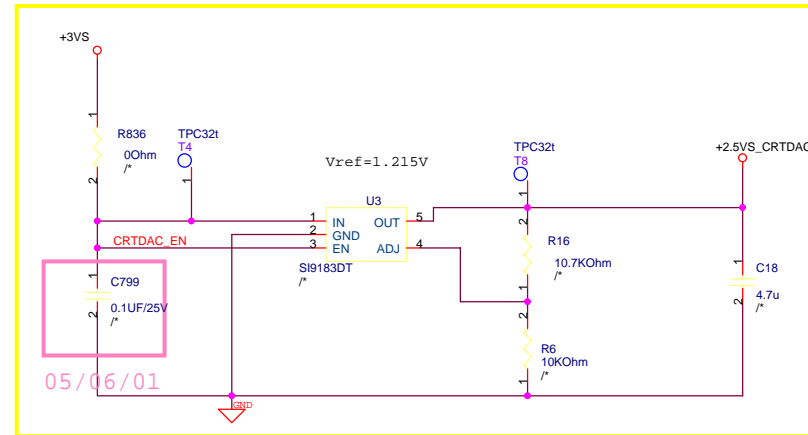
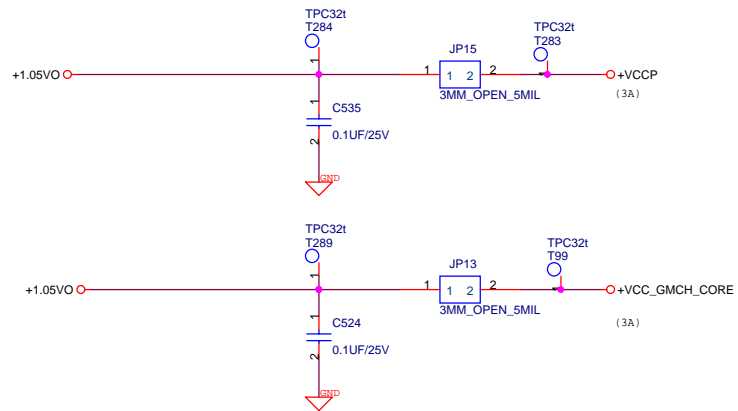
OUT: +1.8V
 +1.5V
 +2.5V
 +VCC_GMCH_CORE
 +5VALWAYS
 +3VALWAYS



ASUS Title: Z61Ae
 ASUSTECH CO., LTD. Engineer: ADAMS LIN

Size	Project Name	Rev
Custom	Z61Ae	2.0

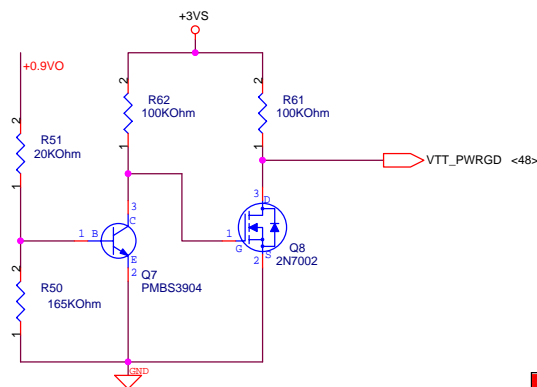
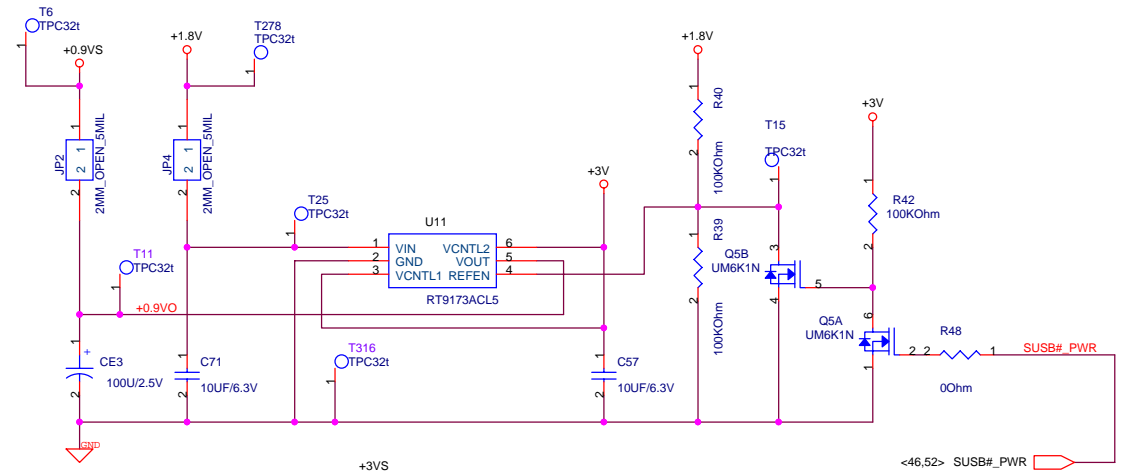
Date: Thursday, June 09, 2005 Sheet 46 of 57

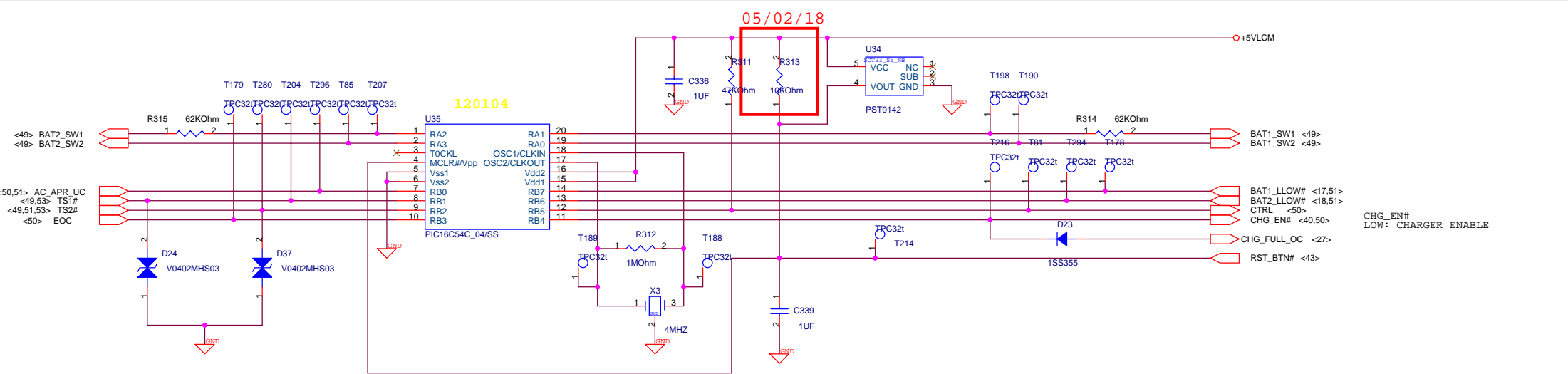


SIGNAL IN: SUSB#_PWR
CPU_VRON

POWER IN: +3VSUS
+3V
+1.8V

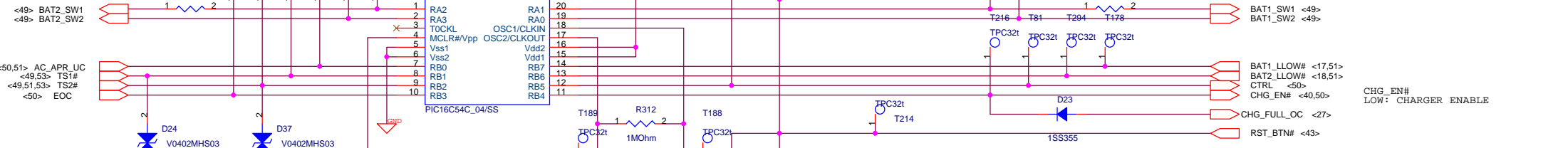
OUT: +0.9VS
+1.5VSUS
+VCCP
+VCC_GMCH_CORE



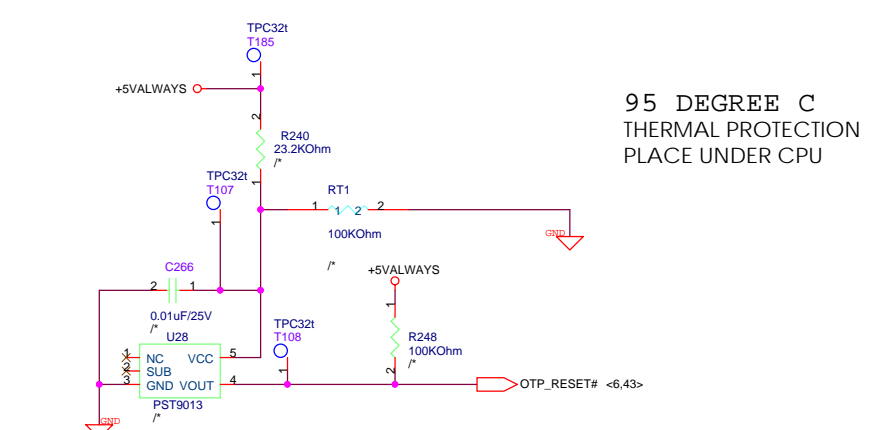


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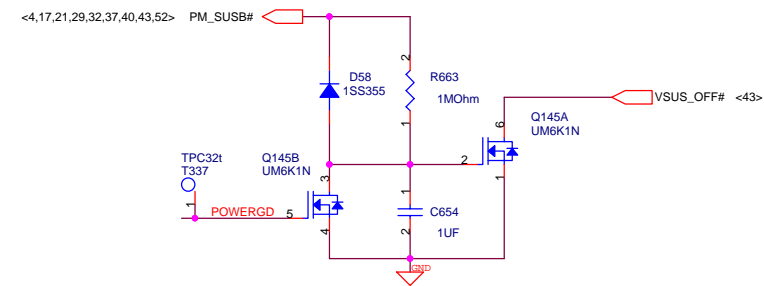
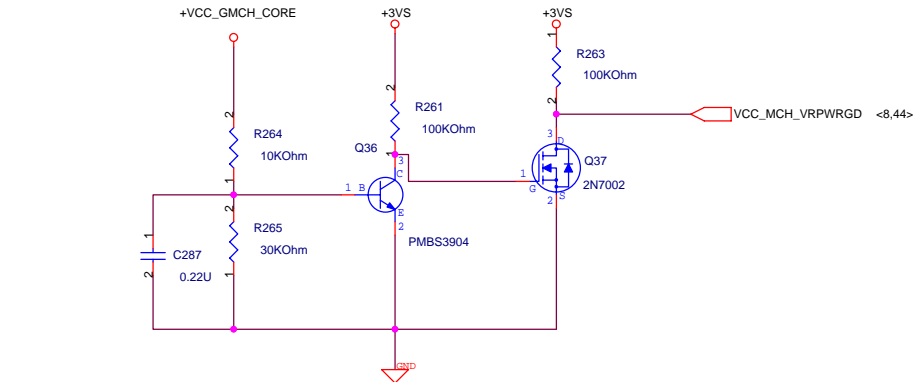
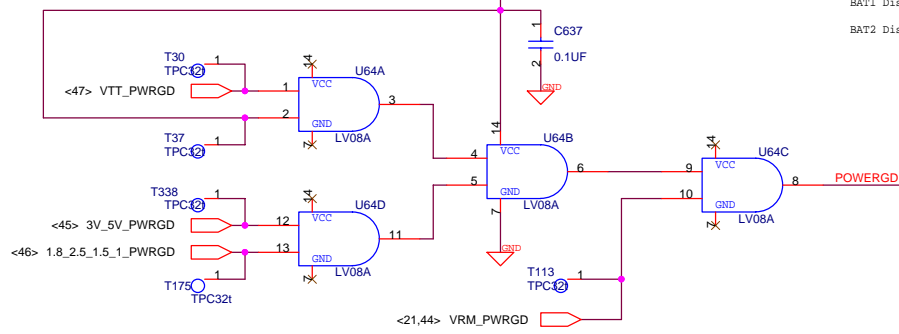
CHG_EN#
LOW: CHARGER ENABLE

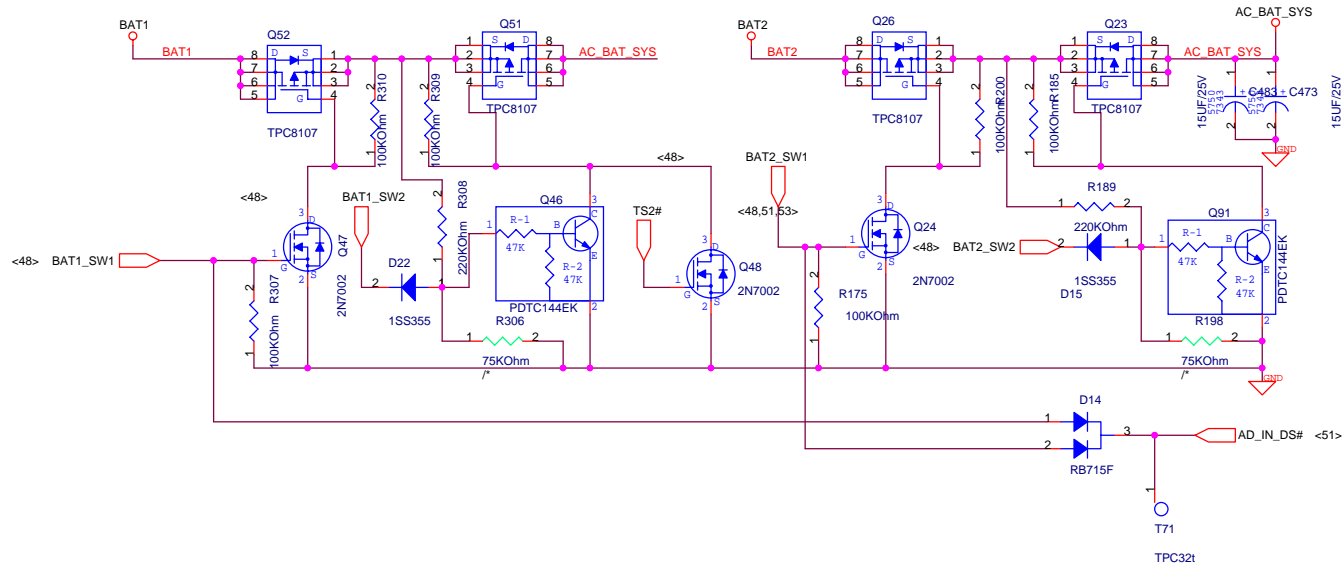


95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU

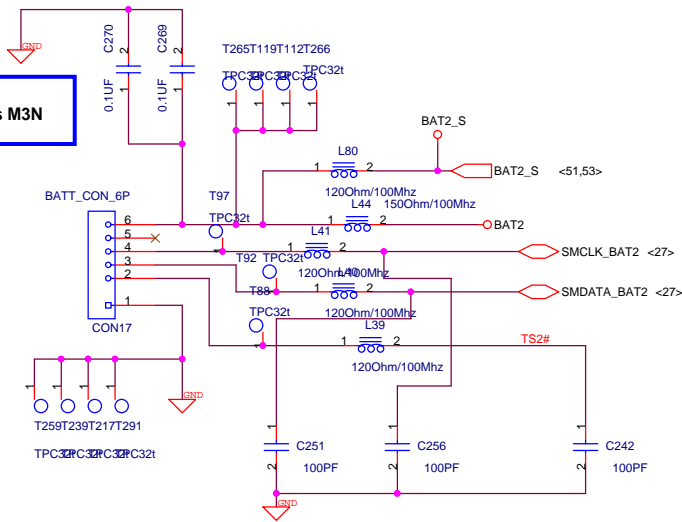
Charge/Discharge Pins logic table

	BAT1_SW1	BAT1_SW2	BAT2_SW1	BAT2_SW2	CTRL
Adapter mode	L	H	L	H	H
BAT1 charge	L	H	L	H	H
BAT2 charge	L	H	L	H	L
BAT1 Discharge	H	H	L	L	H
BAT2 Discharge	L	L	H	H	L

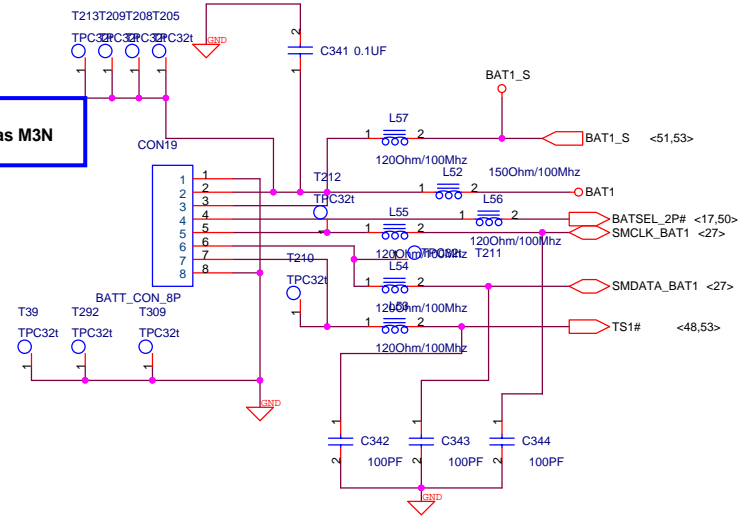


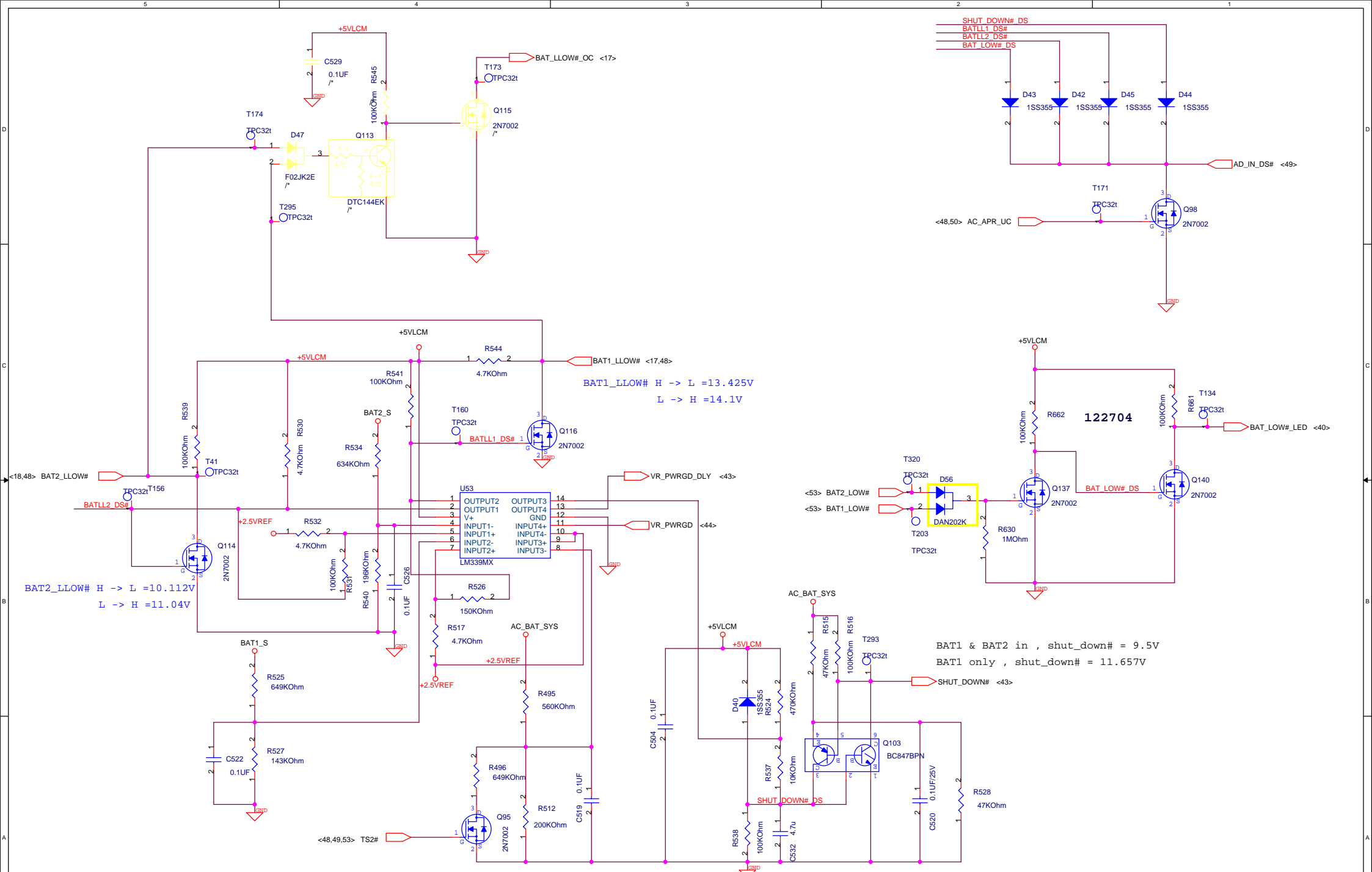


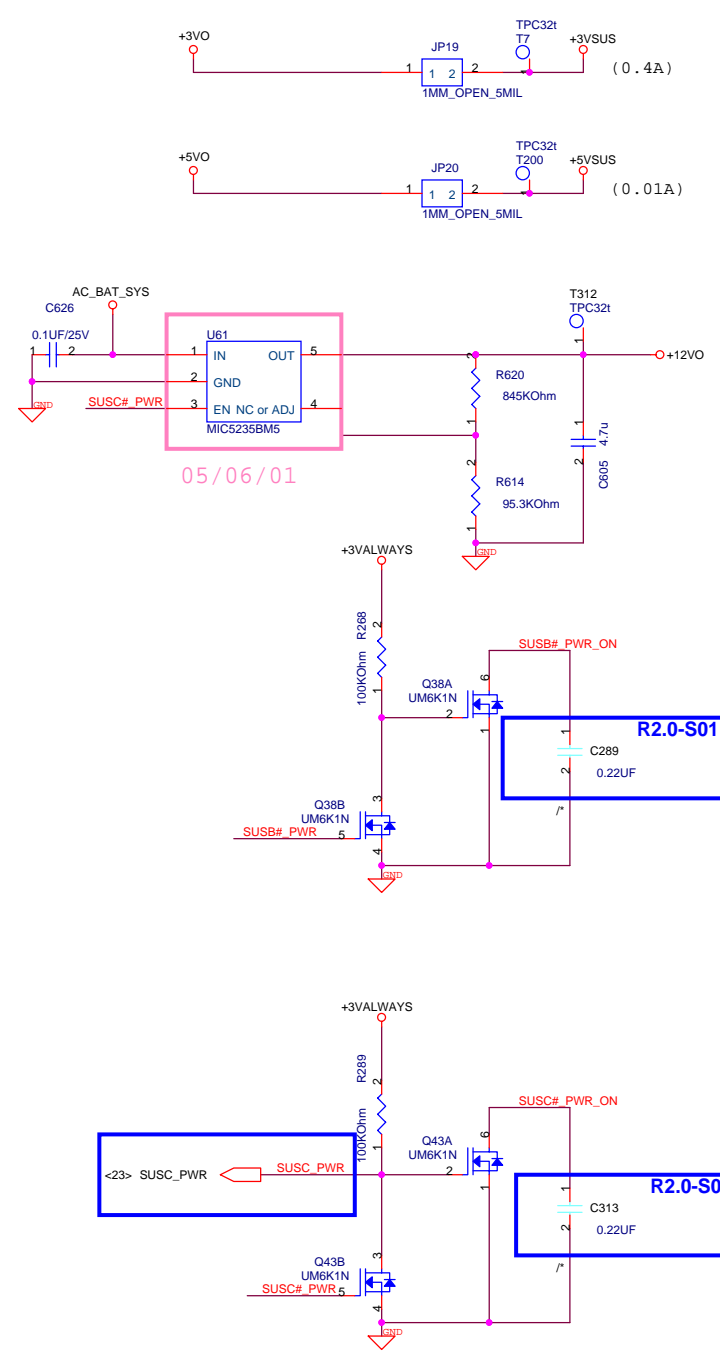
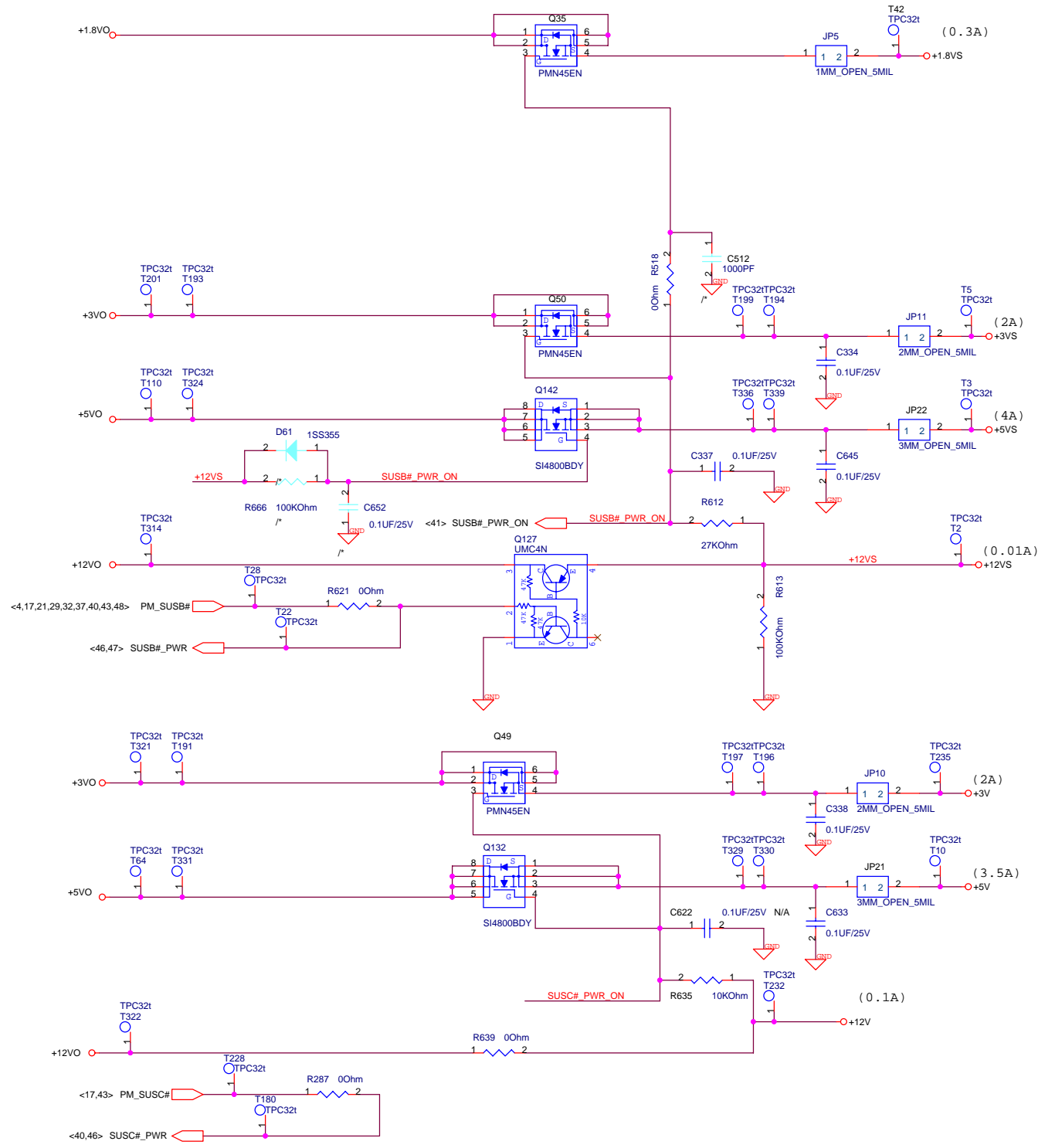
CON Part Number Modify as M3N

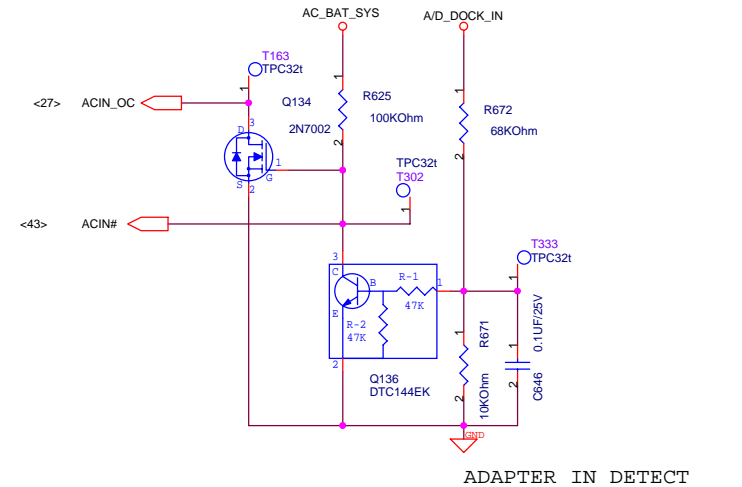
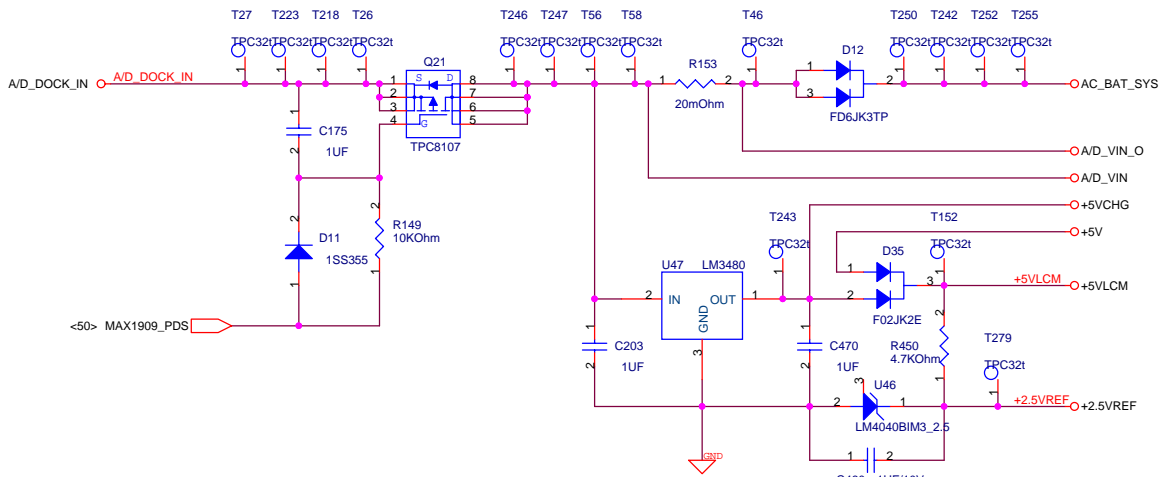


CON Part Number Modify as M3N

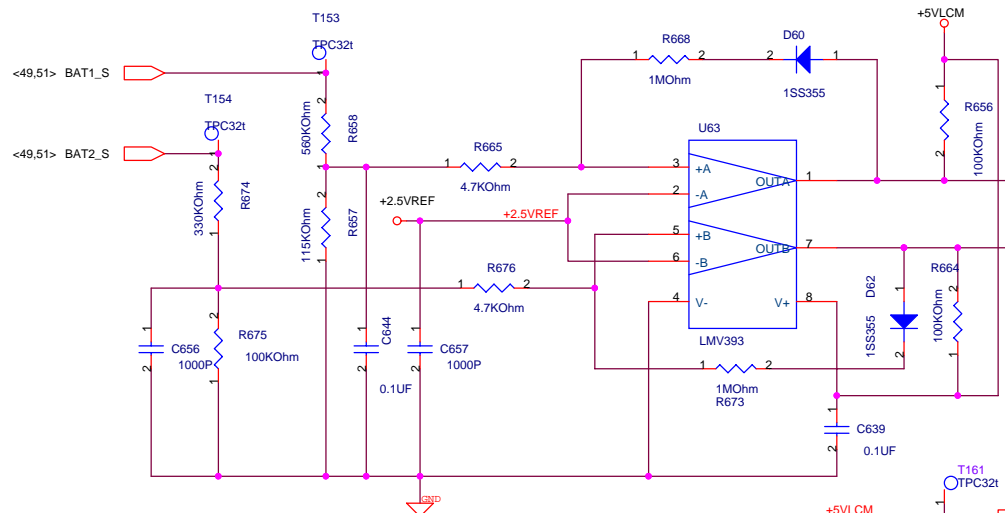








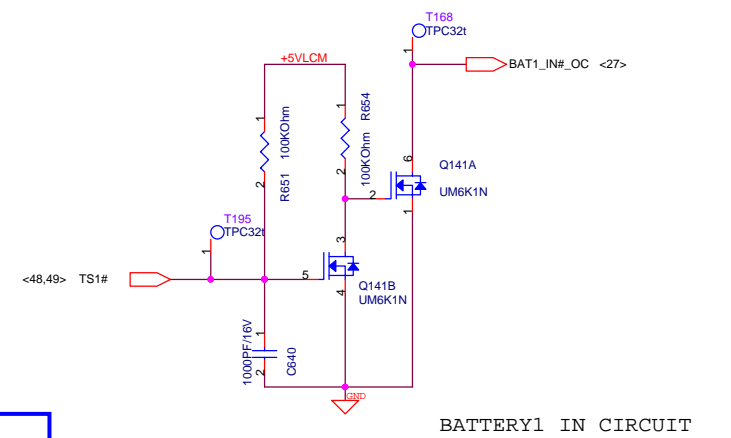
1. ADAPTER IN CIRCUIT
2. +5VCHG
3. +5VLCM & +2.5VREF



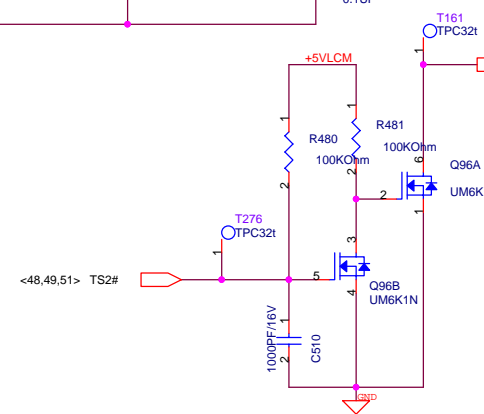
BAT1_LOW# (H--L) =
 BAT1_LOW# (L--H) = 14.67V

BAT2_LOW# (H--L) =
 BAT2_LOW# (L--H) = 10.75V

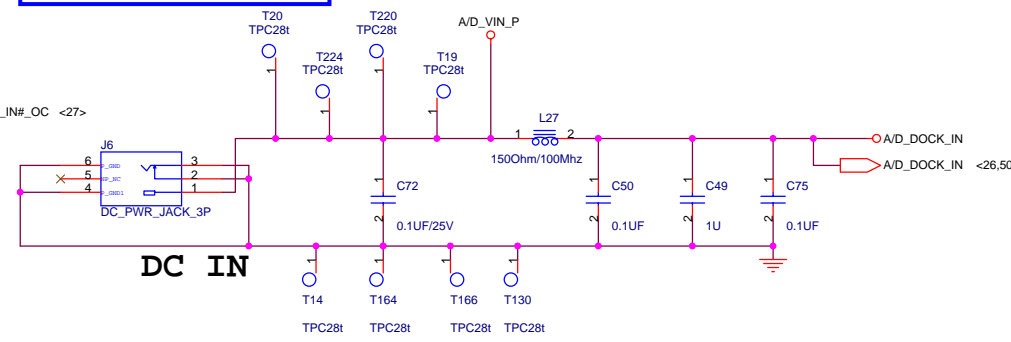
CON Part Number Modify as ME



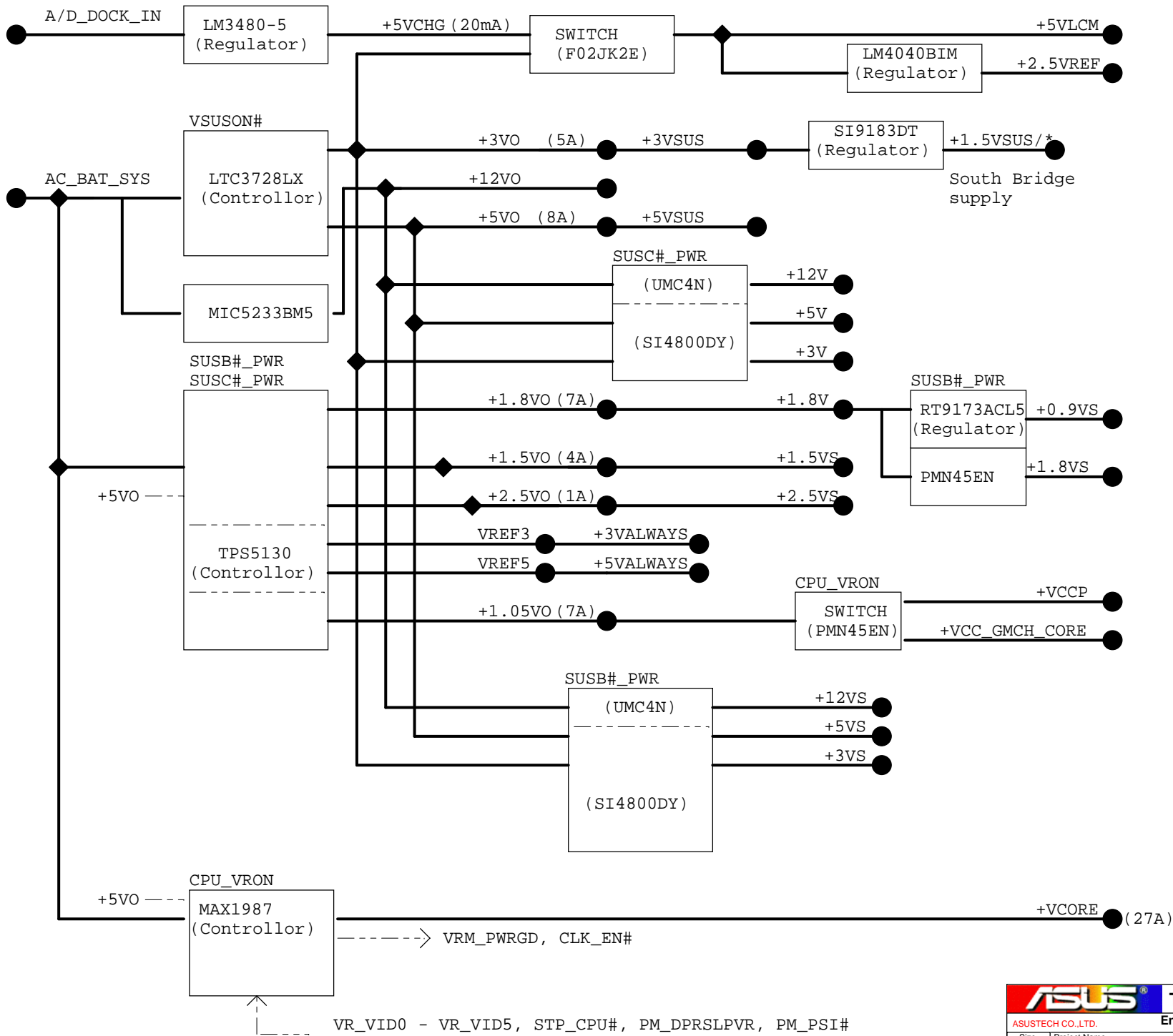
BATTERY1 IN CIRCUIT

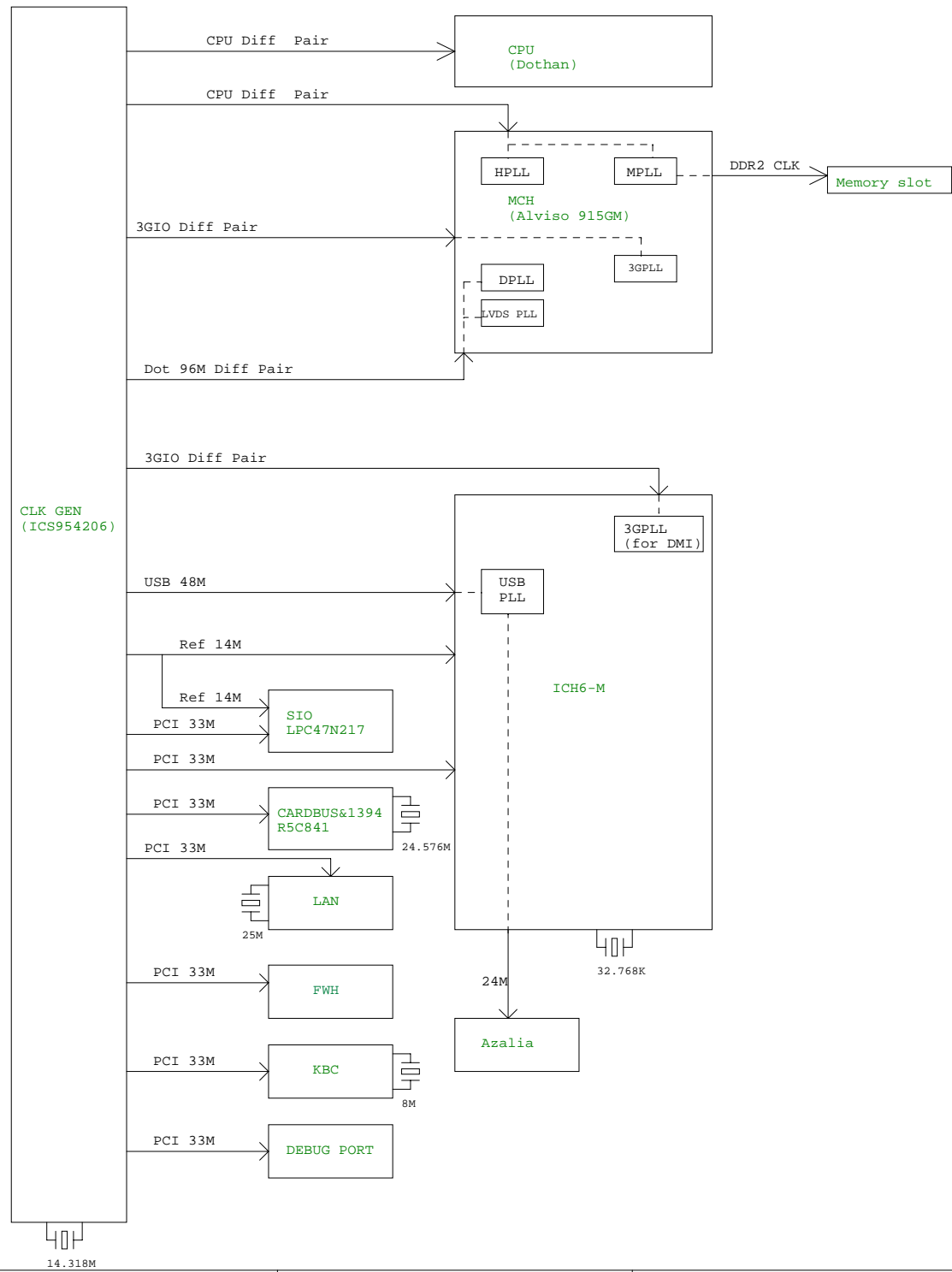


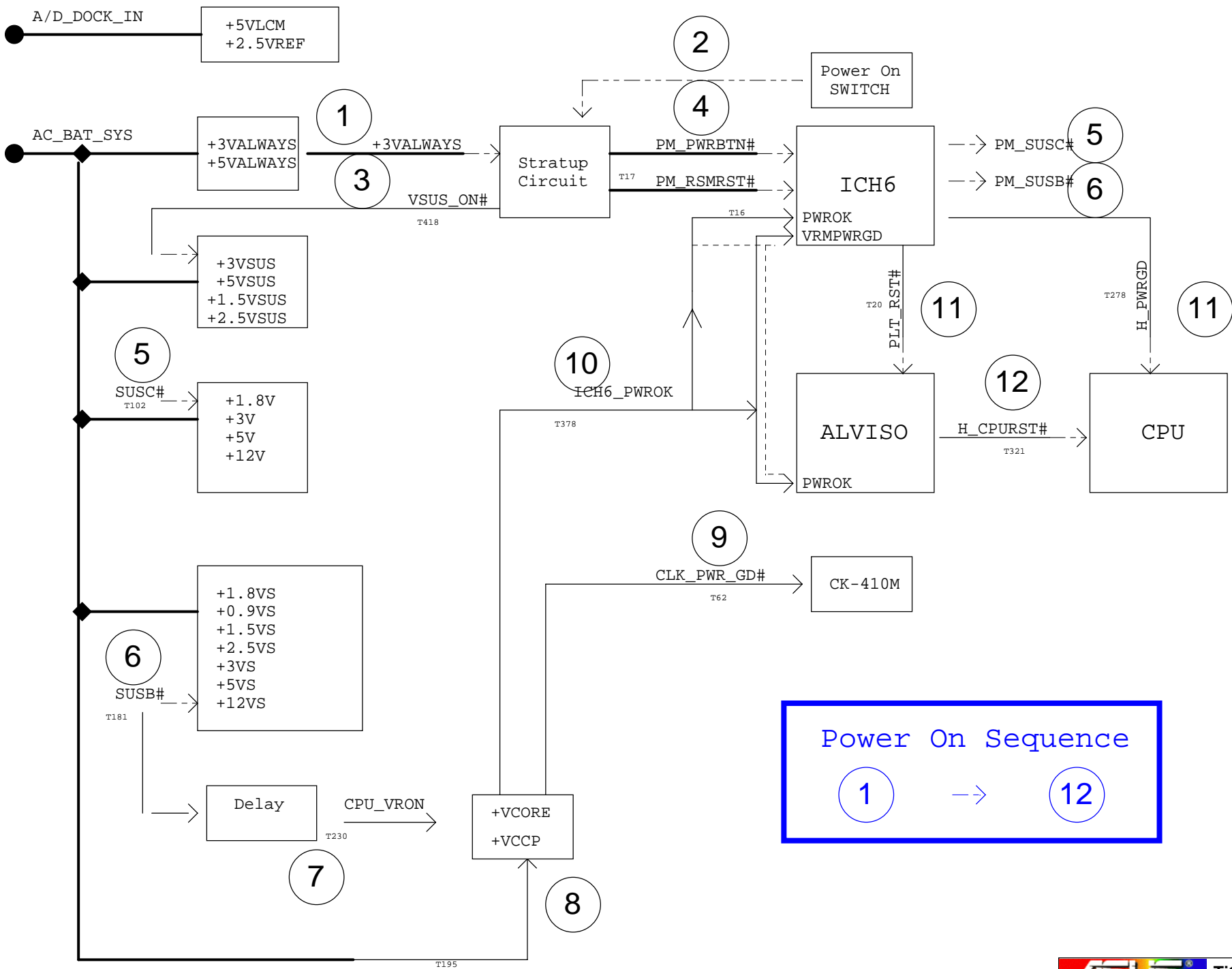
BATTERY2 IN CIRCUIT



DC IN







Power On Sequence
 1 → 12

Power

Revision History

R1.0

System

R1.1

- R1.1-S01 --> To fine tune power sequence and power select.
- R1.1-S02 --> To fine tune clock quality.
- R1.1-S03 --> ME change H4 & H6 & H25 to 13-N7510M270 (It need to modify in BOM by self.)
- R1.1-S04 --> CE1 not used, Release space for bluetooth.
- R1.1-S05 --> Follow M3V R2.1
- R1.1-S06 --> RealTek suggestion.(To support MicroSoft new HCT12.1 test program.)
- R1.1-S07 --> RealTek suggestion.To support Software Jack Detect(JD) function.
- R1.1-S08 --> To avoid PCB sound when system BOOT.
- R1.1-S09 --> To fine tune SPDIF A signal quality.
- R1.1-S10 --> unmount R629.(Due to dual pull low with R637.)
- R1.1-S11 --> To avoid charge LED flash when adapter in and remove battery.
- R1.1-S12 --> To support alert by BIOS control and delete R174 dual pull high.
- R1.1-S13 --> Bypass MIC amplifier to improve MIC signal quality.
- R1.1-S14 --> Realtek suggestion.
- R1.1-S15 --> To use thinner than before.
- R1.1-S16 --> Follow M6V/A R2.1
- R1.1-S17 --> For factory testing, Software can use the GPIO into test mode.
- R1.1-S18 --> To solve CRT ripple problem.
- R1.1-S19 --> Delete BAYDOCK LNH pull high. Due to dual pull high with RN26.
- R1.1-S20 --> Change DDR2 SODIMM to DUAL DDR2 DIMM.
- R1.1-S21 --> Update PCB VID.
- R1.1-S22 --> To support HDD/ODD Hot SWAP.
- R1.1-S23 --> To solve OTC bug for PRINTER PORT fail.(Run QA+PRO V)
- R1.1-S24 --> For factory ATS power test at P/R stage.
- R1.1-S25 --> To match ME new MIC cable definition.
- R1.1-S26 --> Change to digital ground.To avoid noise.
- R1.1-S27 --> RICOH suggestion.
- R1.1-S28 --> Del unused Components and Net to release free space.
- R1.1-S29 --> To avoid VCCA wrong Value.
- R1.1-S30 --> delete unmount part to release MB space.
- R1.1-S31 --> Due to KB Cover shut down cause Sys. Power on.
- R1.1-S32 --> Unmount C for Cost down.
- R1.1-S33 --> Fine tune LAN driving.
- R1.1-S34 --> Change JRS1T PCB footprint for Layout suggestion.
- R1.1-S35 --> Change R to RPACK for Cost down.
- R1.1-S36 --> Fine tune -R value.
- R1.1-S37 --> For Port Bar LAN Wake-up.
- R1.1-S38 --> Give BT_ON signal a default state.

R2.0

- R2.0-S01 --> To fine tune power sequence.
- R2.0-S02 --> To fine tune crystal FPM.
- R2.0-S03 --> To modify some mistake in V1.1.
- R2.0-S04 --> To Re-define LED.
- R2.0-S05 --> To get power switch signal when end-user press power key quickly.(over 30ms then PWR_ON# will be low.)
- R2.0-S06 --> To avoid +3VSUS sometimes re-start in battery mode then loss 10mA around.(Add 39K ohm can make +3VSUS low faster and U60 IC will shutdown faster.)
- R2.0-S07 --> To solve can not resume when battery low.
- R2.0-S08 --> To add 0.1u by SMI request.
- R2.0-S09 --> To check O/S or DOS mode.To control power LED flash when battery low about 10%.DOS mode H/W detect battery then flash LED.O/S mode S/W detect 10% from gauge then inform LED to flash.
- R2.0-S10 --> Mount MIC amplifier to improve MIC volume.
- R2.0-S11 --> To set Switch default for Dothan.
- R2.0-S12 --> To fine tune Speaker volume.
- R2.0-S13 --> Fine tune CH_GBRSTW timing.
- R2.0-S14 --> To solve USB device leakage to +5V in S3.When use USB HDD storage that need power adapter.