

2012 S-Series Richie 13.3" UMA/DIS Muxless Schematic

Intel Chief River Platform
Ivy Bridge (rPGA989)
Panther Point PCH

REV:-1
2012-03-15

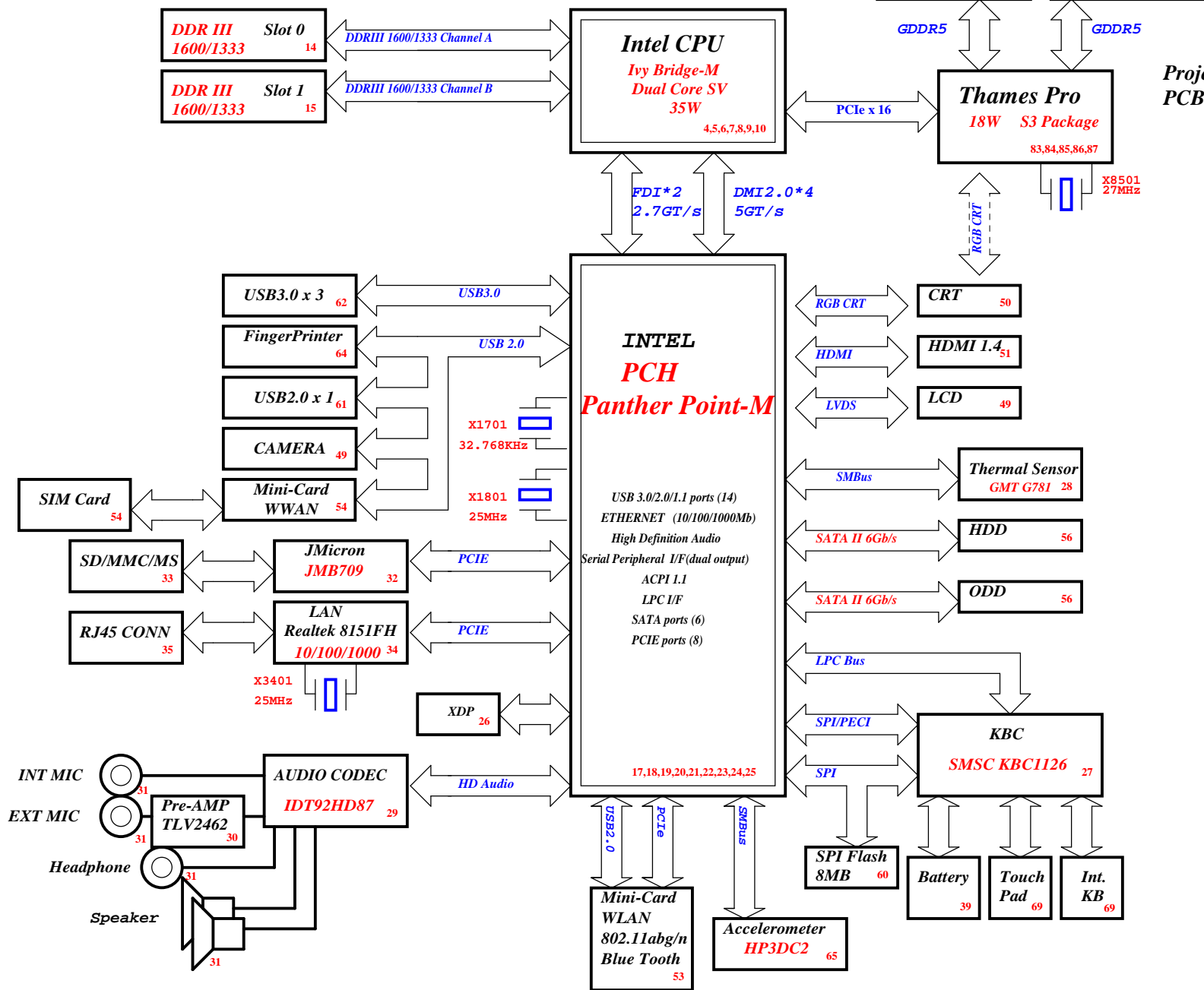
DY:No stuff
DIS_PX:Only DIS install

<Core Design>

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Title			
Cover Page			
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S-Series Richie Block Diagram

(Muxless)



Project code:91.4RS01.001
PCB P/N:11241

SYSTEM DC/DC TPS51461RGER 48		CPU DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	+VCCSA	DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51211DSCR 45		SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D05V_S0	DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC TPS51216RUKR 46		GFX DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3	DCBATOUT	VCC_GFXCORE
VGA UP1527QQDD 92		CHARGER BQ24736RGR 40	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VGA_CORE	AD+ BT+	DCBATOUT
SYSTEM DC/DC RT8068AZQWID 47		SYSTEM DC/DC FDMC7696 93	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
3D3V_S5	1D8V_S0	1D5V_S3	1V_VGA_S0
Switches			
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0		
PCB LAYER			
L1:Top	L5:Vcc	L2:GND	L6:Signal
L3:Signal	L7:GND	L4:Signal	L8:Bottom

PCB 8 LAYER

- L1: Top
- L2: GND
- L3: Signal
- L4: Signal
- L5: VCC
- L6: Signal
- L7: GND
- L8: Bottom

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT{3:0}# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TV5	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation DF_TV5 needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel® HD Audio dock signals to the corresponding Cougar Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. Note: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1K ohm resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2] CFG2 is for the 16x	PCIe Static x16 Lane Numbering Reversal.	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	1
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull down to GND through a 1KΩ ± 5% resistor to enable port	1
CFG[6:5]	PCIe Port Bifurcation Straps	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	11
CFG[17:7]	Reserved configuration lands. A test point may be placed on the board for these lands.		

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCC2A 0D75V_S0 VCC_CORE VCC_GFXCORE VGA_CORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
1D5V_S3 DDR_VREF_S3	5V 1.5V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-14.1V 9V-19.5V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

PCIe Routing

LANE1	X
LANE2	X
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	LAN
LANE7	X
LANE8	X

USB 2.0 Table USB3.0 Table

Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	N/A
3	N/A
4	N/A
5	N/A

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	Chief River CRV
Device	Address	Hex Bus
DIMM1 DIMM2 Touch-Pad		PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA
N/A		PCH_SMB0_CLK/PCH_SMB0_DATA
KBC G781_Thermal IC GPU_Thermal PRO G-Sensor	1001100 0X41 0X52	PCH_SMB1CLK/PCH_SMB1DATA PCH_SMB1CLK/PCH_SMB1DATA PCH_SMB1CLK/PCH_SMB1DATA

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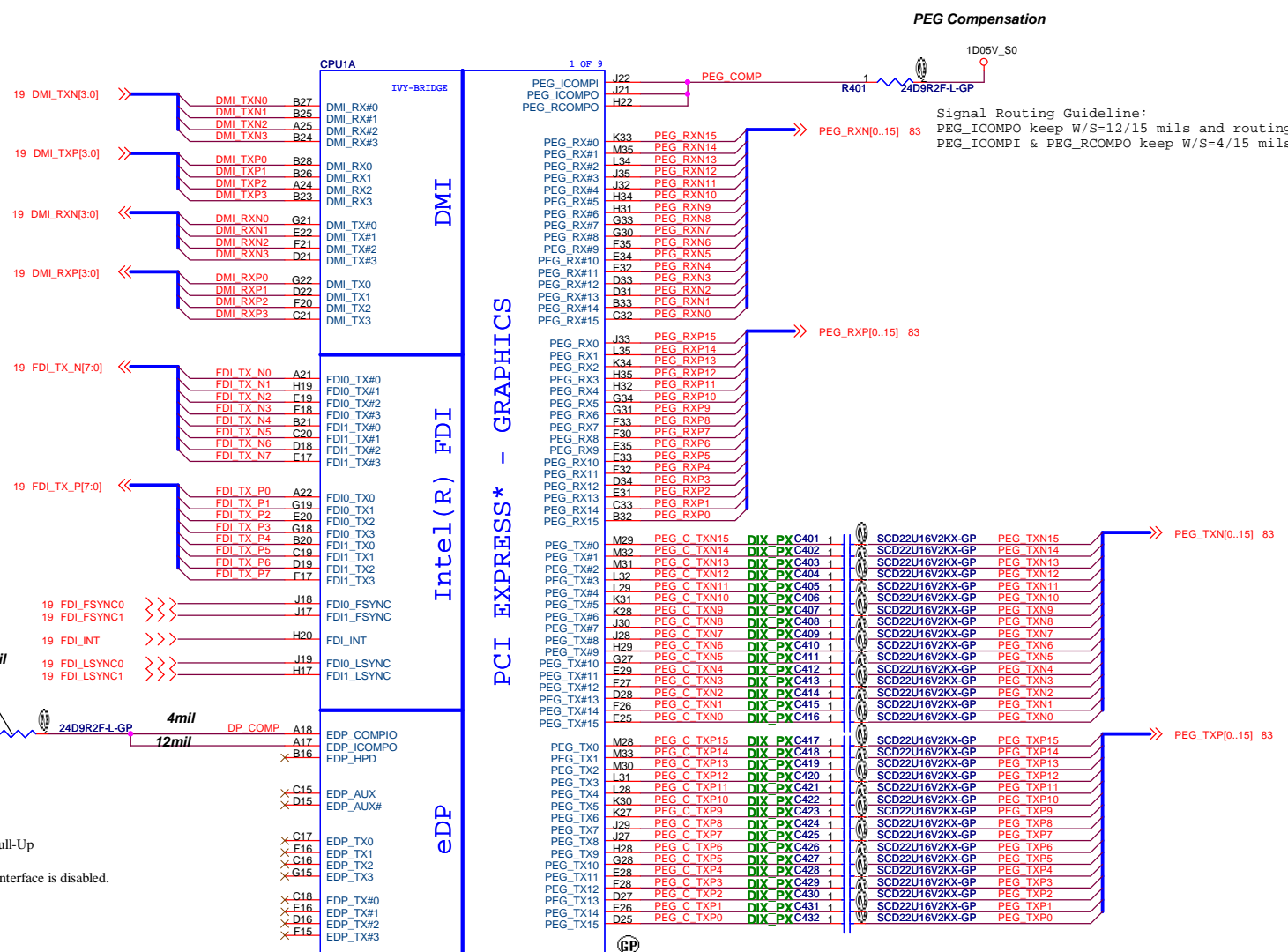
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CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)



Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

NOTE: EDP_HP
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

62.10040.821
1st = 62.10055.551
2nd = 62.10055.321
3rd = 62.10055.731

BOM Note: 1st/2nd/3rd Add in BOM

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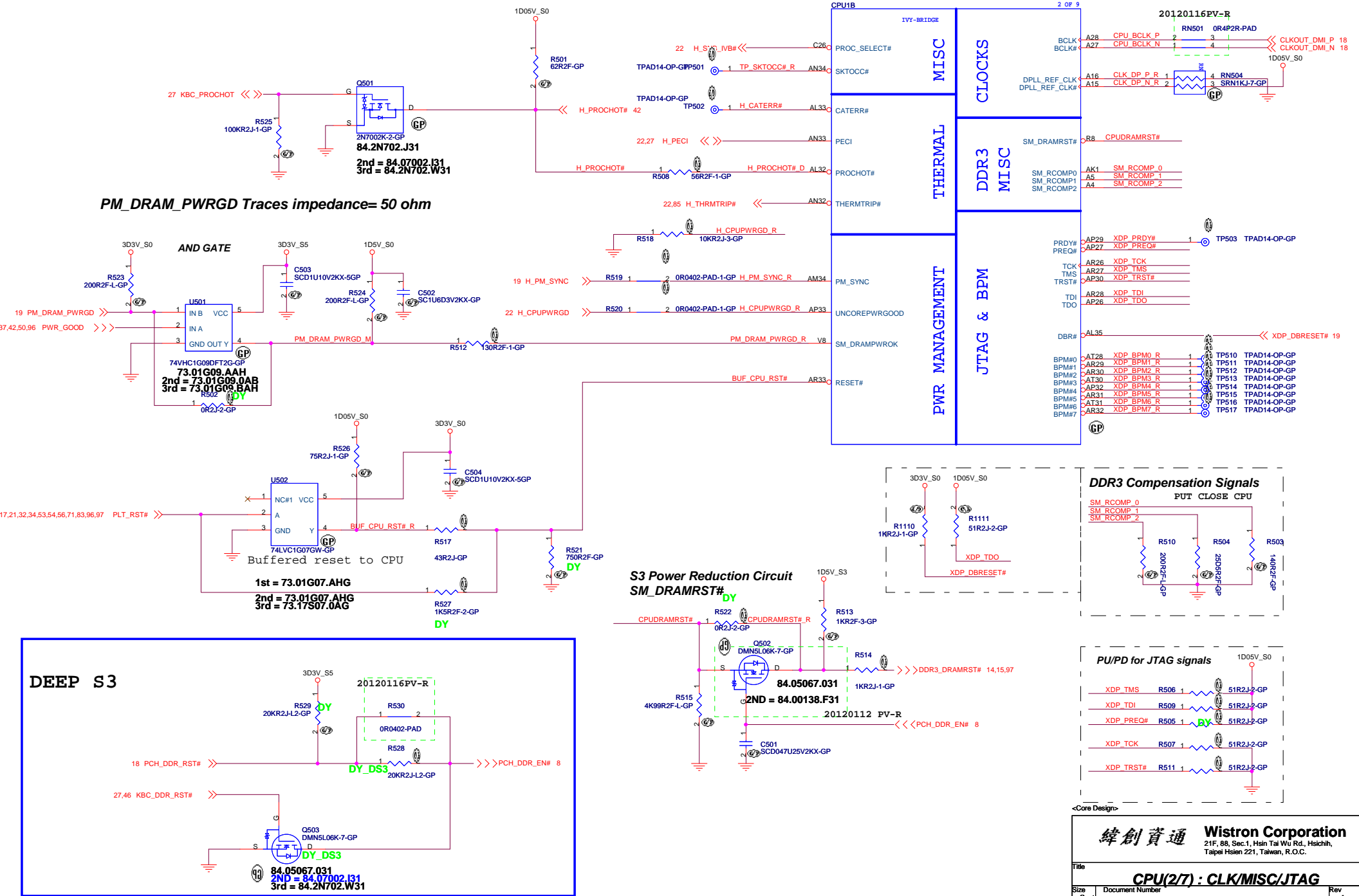
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Size: A3 Document Number: **2012 S-Series Richie 13.3** Rev: -1

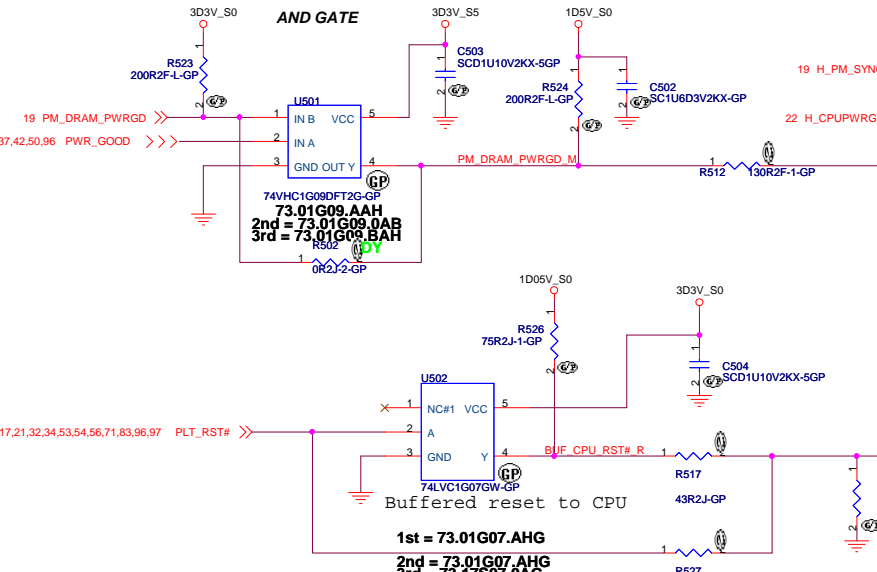
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CPU(2/7)

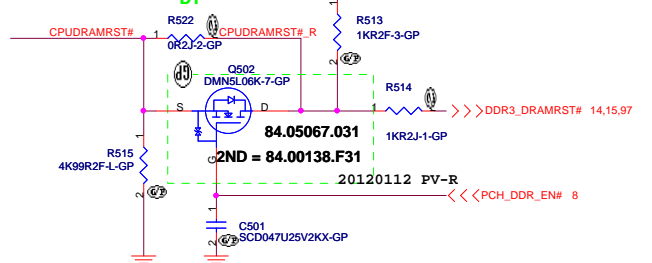
IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



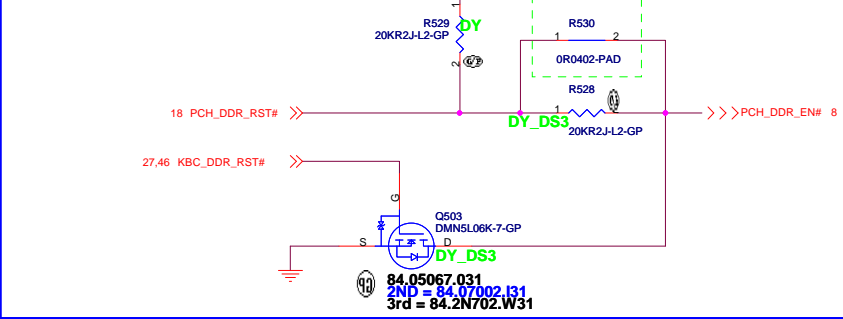
PM_DRAM_PWRGD Traces impedance= 50 ohm



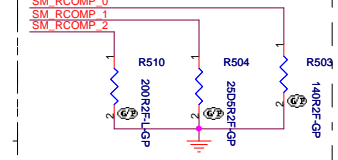
S3 Power Reduction Circuit SM_DRAMRST#



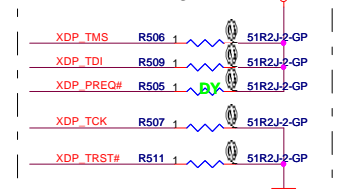
DEEP S3



DDR3 Compensation Signals



PUPD for JTAG signals

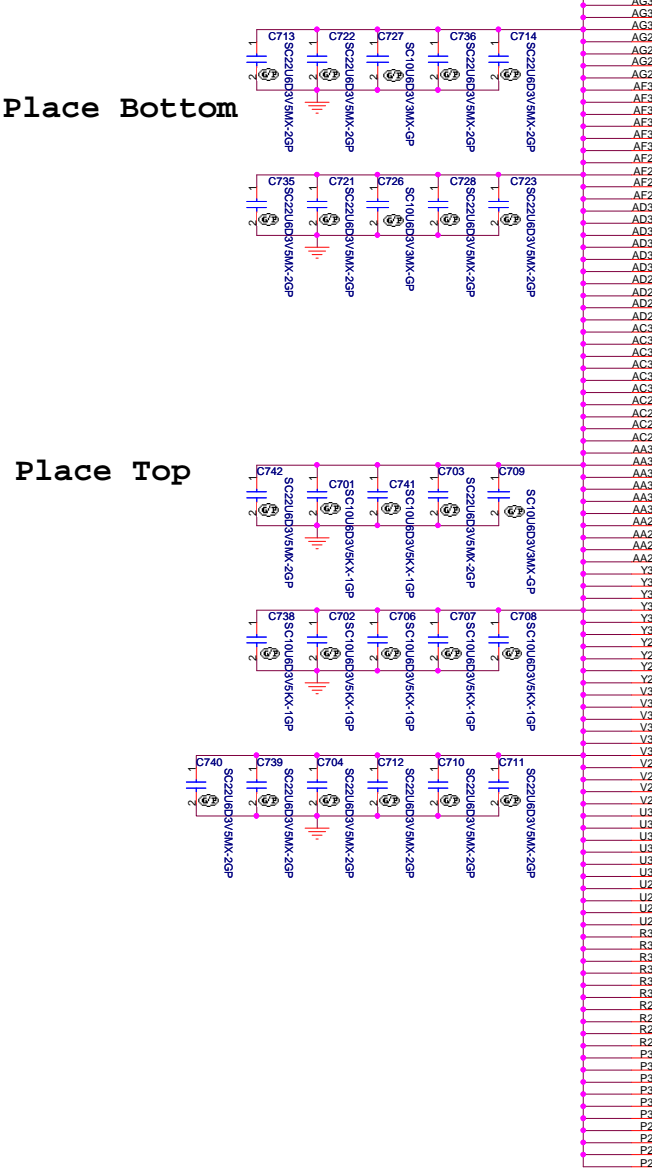


CPU(4/7) IVY BRIDGE PROCESSOR (POWER)

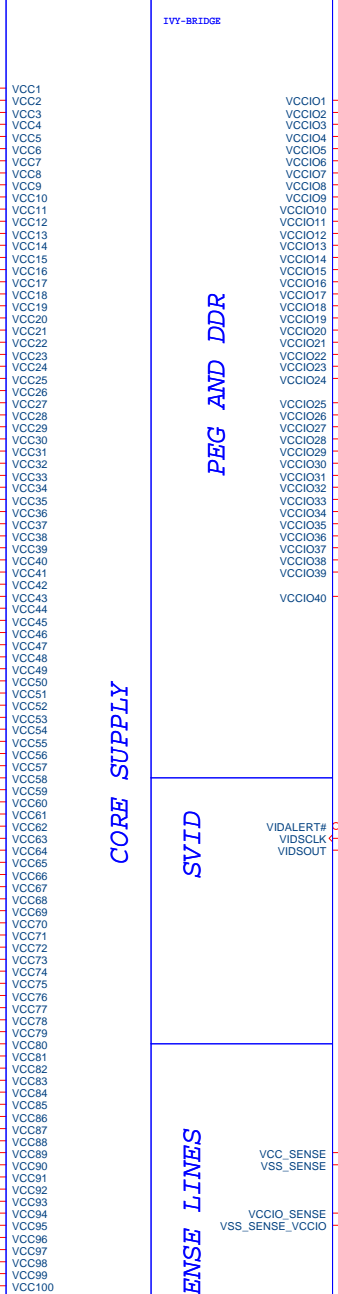
PROCESSOR CORE POWER

Place Bottom

Place Top



POWER

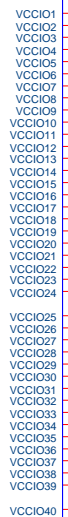


POWER



PROCESSOR UNCORE POWER

8.5A
1D05V_S0

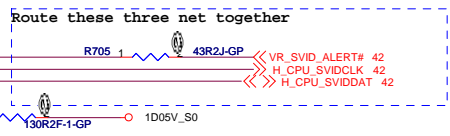


PEG AND DDR

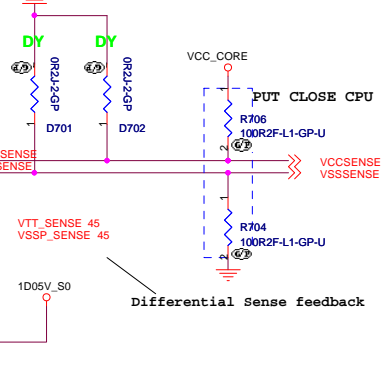
CORE SUPPLY

SVID

SENSE LINES



reserve PAD for ESD

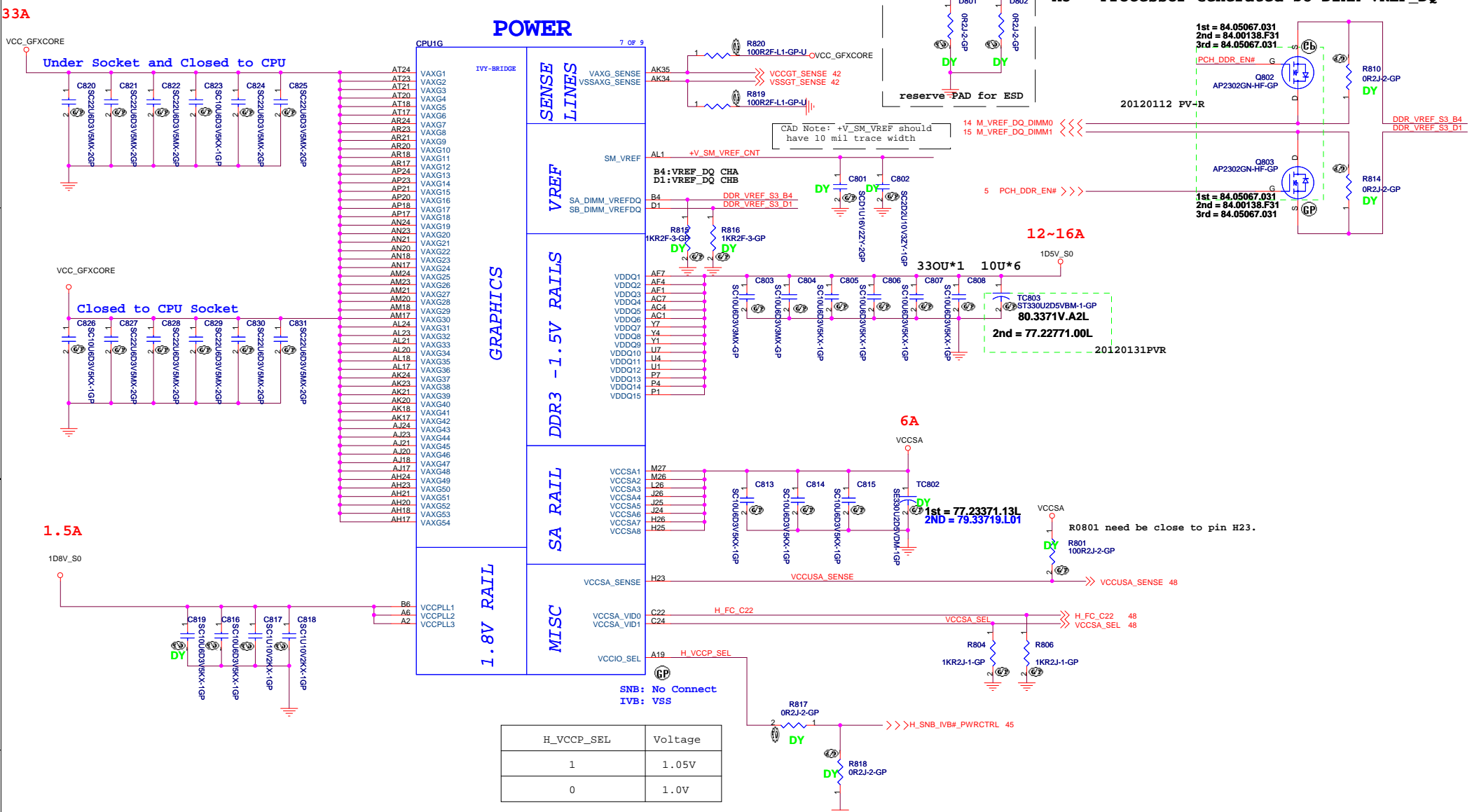


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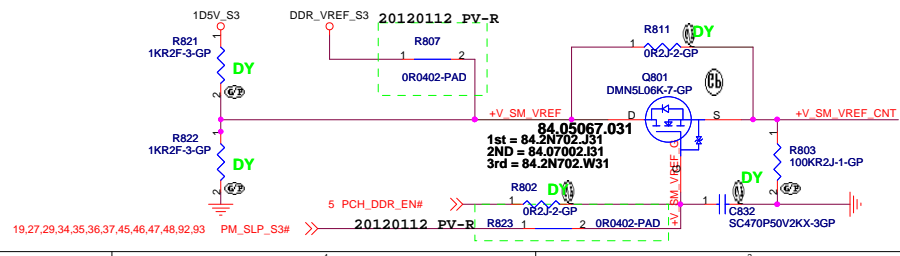
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CPU(5/7) IVY BRIDGE PROCESSOR (GRAPHICS POWER)



S3 Power Reduction Circuit Processor VREF_DQ Implementation



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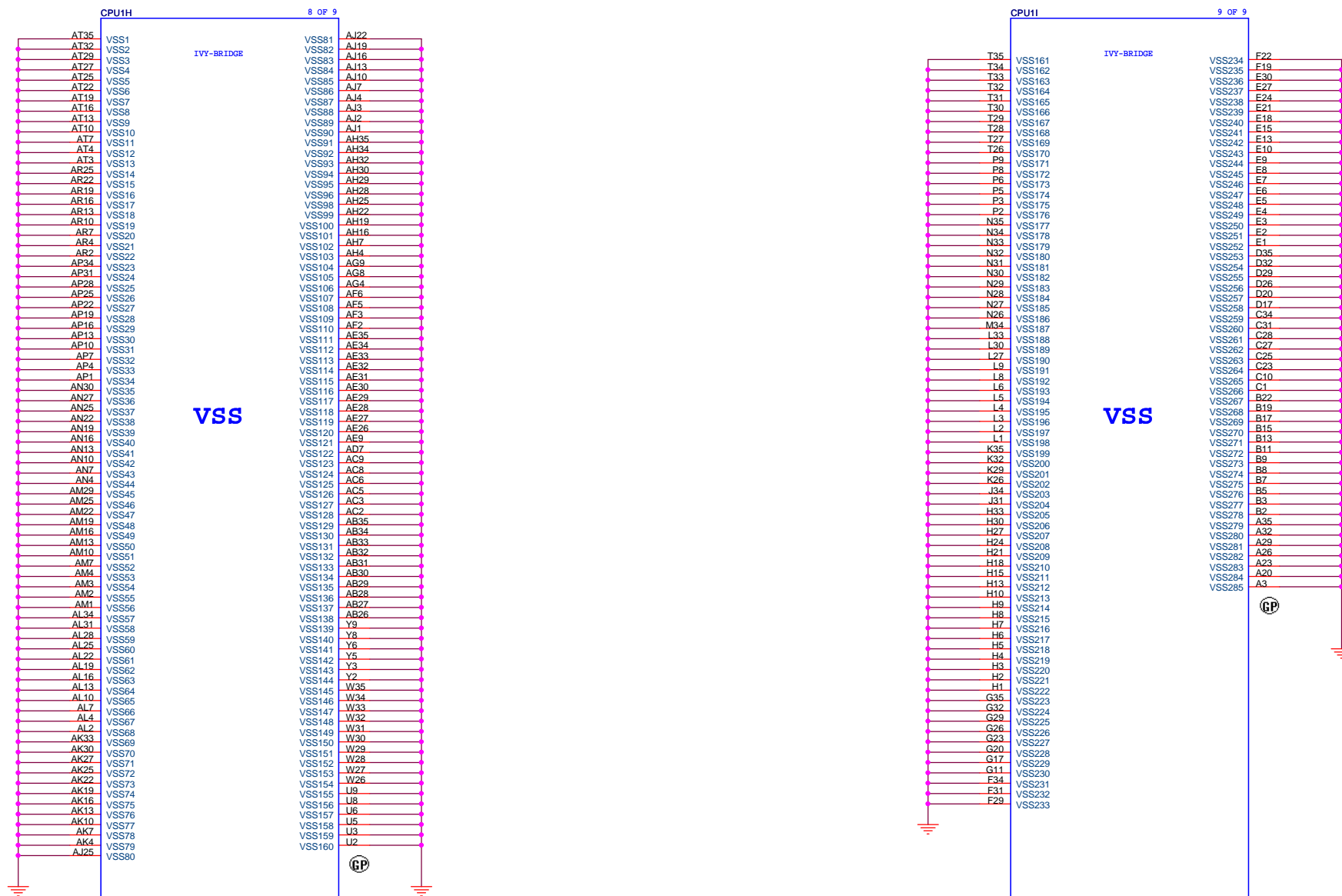
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Title		
CPU(5/7) : GFX/PWR		
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CPU(6/7)

IVY BRIDGE PROCESSOR (GND)



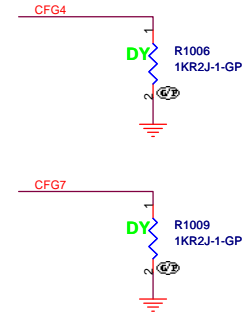
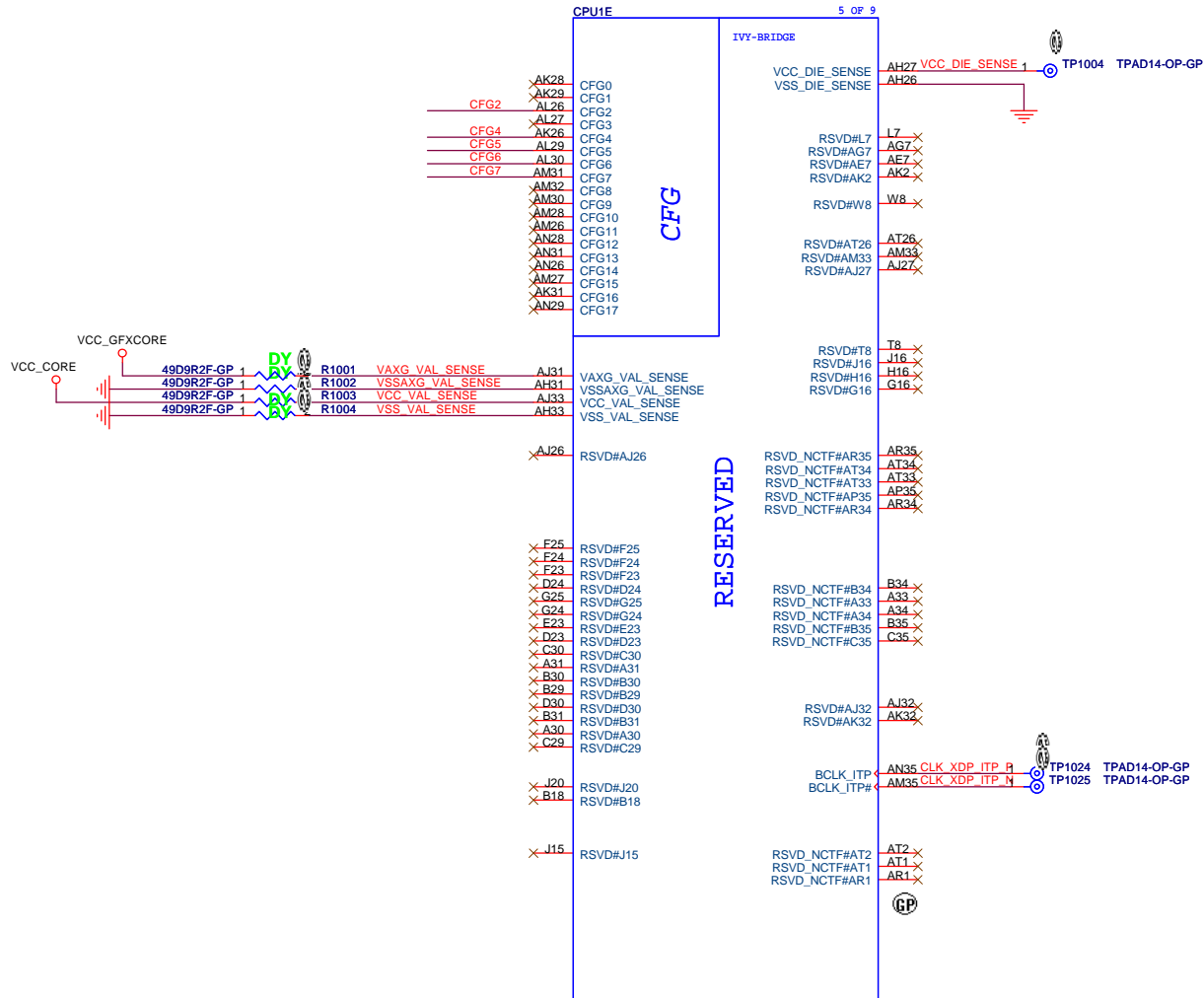
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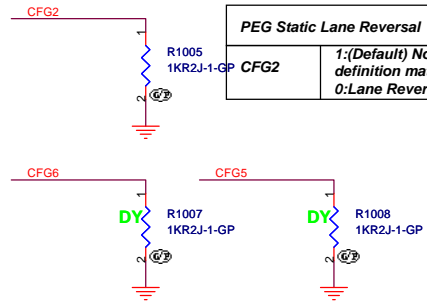
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)



Display Port Presence Strap	
CFG4	0: Enable eDP 1: (Default) Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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CPU XDP			
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Title

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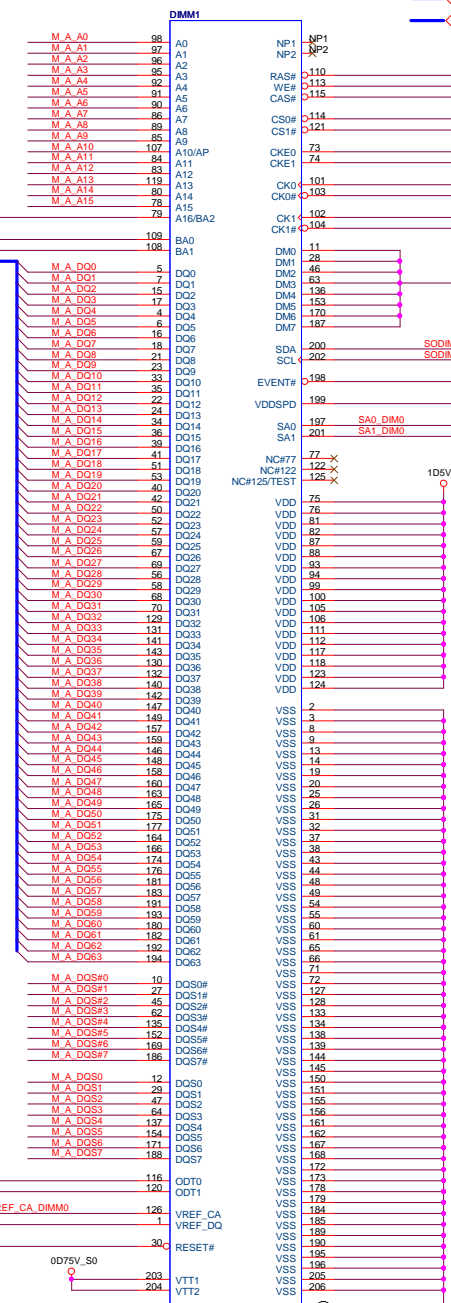
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DIMM1

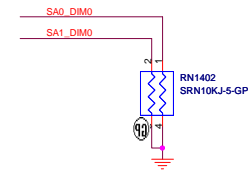
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— << M_A_DQS#[7:0] 6
— << M_A_A[15:0] 6



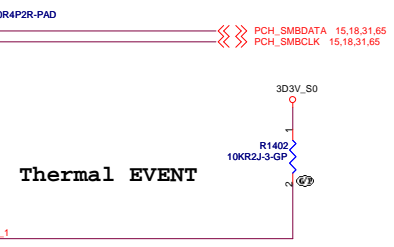
6 M_A_BS2 >>>
 6 M_A_BS0 >>>
 6 M_A_BS1 >>>
 6 M_A_DQ[63:0] >>>

6 M_A_DIM0_ODT0 >>>
 6 M_A_DIM0_ODT1 >>>
 M_VREF_CA_DIMM0 >>>
 8 M_VREF_DQ_DIMM0 >>>
 5,15,97 DDR3_DRAMRST# >>>

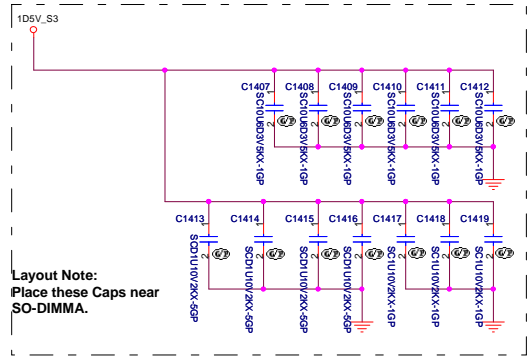
Bom Not: 1st/2nd/3rd Add in BOM
 1st = 62.10024.H91
 2nd = 62.10017.U01
 3rd = 62.10024.H81
 H=9.2mm



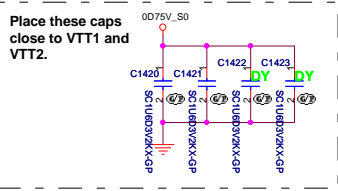
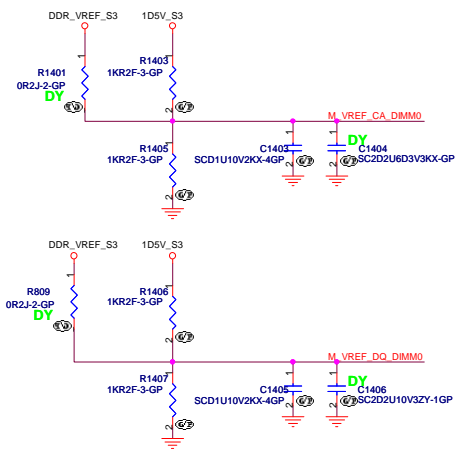
Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30
 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32



SODIMM A DECOUPLING



Layout Note:
 Place these Caps near SO-DIMMA.



Place these caps close to VTT1 and VTT2.

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Title
 DDR3 SO-DIMM1

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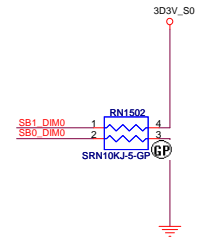
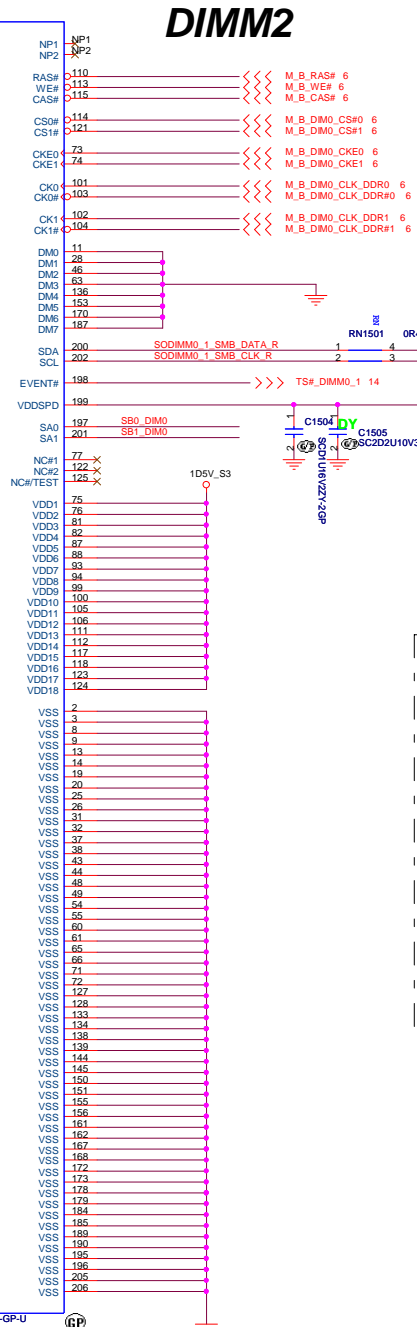
DIMM2

6 M_B_A[15:0] <<>>
 6 M_B_DQS#[7:0] <<>>
 6 M_B_DQS#[7:0] <<>>

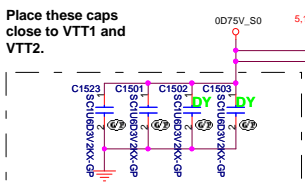
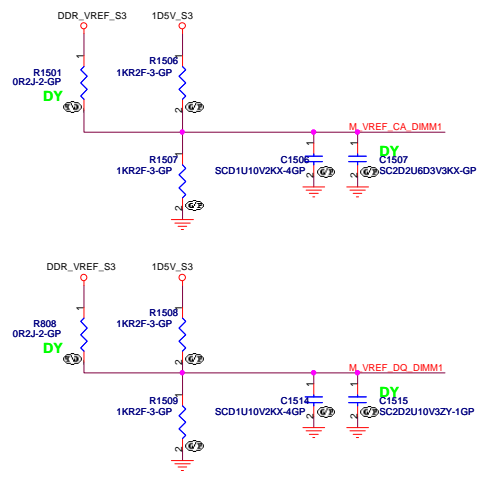
6 M_B_BS2 >>>>
 6 M_B_BS0 >>>>
 6 M_B_BS1 >>>>
 6 M_B_DQ[63:0] >>>>

6 M_B_DM0_ODT0 >>>>
 6 M_B_DM0_ODT1 >>>>
 8 M_VREF_DQ_DIMM1 >>>>
 5,14,97 DDR3_DRAMRST# >>>>

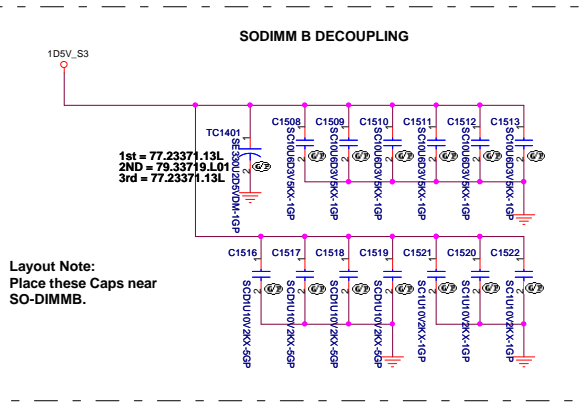
M_B_A0	98	A0
M_B_A1	97	A1
M_B_A2	96	A2
M_B_A3	95	A3
M_B_A4	94	A4
M_B_A5	93	A5
M_B_A6	92	A6
M_B_A7	91	A7
M_B_A8	90	A8
M_B_A9	89	A9
M_B_A10	88	A10
M_B_A11	87	A10/AP
M_B_A12	86	A11
M_B_A13	85	A12
M_B_A14	84	A13
M_B_A15	83	A14
M_B_A16/BA2	82	A15
BA0	79	BA0
BA1	109	BA1
M_B_DQ0	5	DQ0
M_B_DQ1	7	DQ1
M_B_DQ2	15	DQ2
M_B_DQ3	17	DQ3
M_B_DQ4	4	DQ4
M_B_DQ5	6	DQ5
M_B_DQ6	16	DQ6
M_B_DQ7	21	DQ7
M_B_DQ8	23	DQ8
M_B_DQ9	22	DQ9
M_B_DQ10	33	DQ10
M_B_DQ11	35	DQ11
M_B_DQ12	22	DQ12
M_B_DQ13	24	DQ13
M_B_DQ14	34	DQ14
M_B_DQ15	36	DQ15
M_B_DQ16	39	DQ16
M_B_DQ17	41	DQ17
M_B_DQ18	51	DQ18
M_B_DQ19	53	DQ19
M_B_DQ20	40	DQ20
M_B_DQ21	42	DQ21
M_B_DQ22	50	DQ22
M_B_DQ23	52	DQ23
M_B_DQ24	57	DQ24
M_B_DQ25	59	DQ25
M_B_DQ26	67	DQ26
M_B_DQ27	69	DQ27
M_B_DQ28	56	DQ28
M_B_DQ29	58	DQ29
M_B_DQ30	68	DQ30
M_B_DQ31	70	DQ31
M_B_DQ32	129	DQ32
M_B_DQ33	131	DQ33
M_B_DQ34	141	DQ34
M_B_DQ35	143	DQ35
M_B_DQ36	130	DQ36
M_B_DQ37	132	DQ37
M_B_DQ38	140	DQ38
M_B_DQ39	142	DQ39
M_B_DQ40	147	DQ40
M_B_DQ41	149	DQ41
M_B_DQ42	157	DQ42
M_B_DQ43	159	DQ43
M_B_DQ44	146	DQ44
M_B_DQ45	148	DQ45
M_B_DQ46	158	DQ46
M_B_DQ47	160	DQ47
M_B_DQ48	163	DQ48
M_B_DQ49	165	DQ49
M_B_DQ50	175	DQ50
M_B_DQ51	177	DQ51
M_B_DQ52	164	DQ52
M_B_DQ53	166	DQ53
M_B_DQ54	174	DQ54
M_B_DQ55	176	DQ55
M_B_DQ56	181	DQ56
M_B_DQ57	183	DQ57
M_B_DQ58	191	DQ58
M_B_DQ59	193	DQ59
M_B_DQ60	180	DQ60
M_B_DQ61	182	DQ61
M_B_DQ62	192	DQ62
M_B_DQ63	194	DQ63
M_B_DQS#0	10	DQS#0
M_B_DQS#1	27	DQS#1
M_B_DQS#2	45	DQS#2
M_B_DQS#3	62	DQS#3
M_B_DQS#4	156	DQS#4
M_B_DQS#5	152	DQS#5
M_B_DQS#6	169	DQS#6
M_B_DQS#7	186	DQS#7
M_B_DQS#8	12	DQS#8
M_B_DQS#9	29	DQS#9
M_B_DQS#10	47	DQS#10
M_B_DQS#11	64	DQS#11
M_B_DQS#12	137	DQS#12
M_B_DQS#13	154	DQS#13
M_B_DQS#14	171	DQS#14
M_B_DQS#15	188	DQS#15
ODT0	116	ODT0
ODT1	120	ODT1
VREF_CA_DIMM1	126	VREF_CA
VREF_DQ_DIMM1	1	VREF_DQ
RESET#	30	RESET#
VTT1	203	VTT1
VTT2	204	VTT2



Note:
 SO-DIMMB SPD Address is 0xA4
 SO-DIMMB TS Address is 0x34



Place these caps close to VTT1 and VTT2.



Layout Note:
 Place these Caps near SO-DIMMB.

1st = 77.23371.13L
 2ND = 79.33719.L01
 3rd = 77.23371.13L

62.10017.U21 H=5.2mm
 2nd = 62.10017.T91
 3rd = 62.10024.I61

<Core Design>

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DDR3 SO-DIMM2			
Title	Document Number		
Size	Customer		
Date	Date		
2012 S-Series Richie 13.3		Rev	-1
Date: Wednesday, March 14, 2012		Sheet	15 of 103

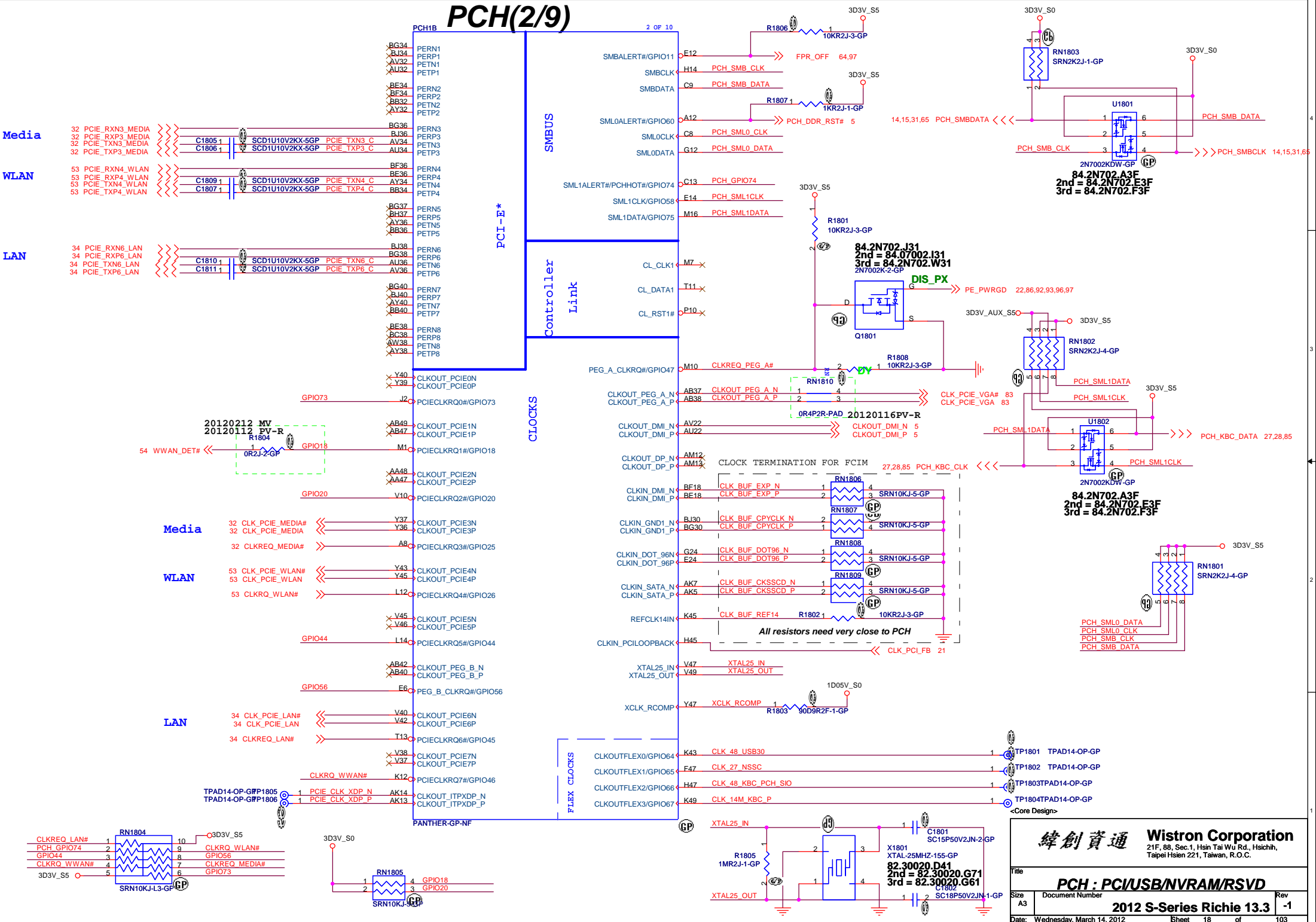
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Title		
RESERVED		
Size	Document Number	Rev
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Date: Wednesday, March 14, 2012		Sheet 16 of 103

PCH(2/9)



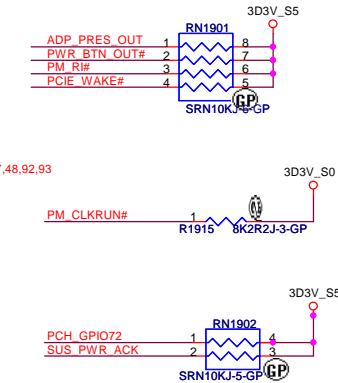
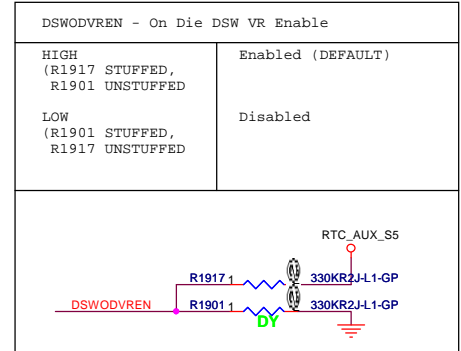
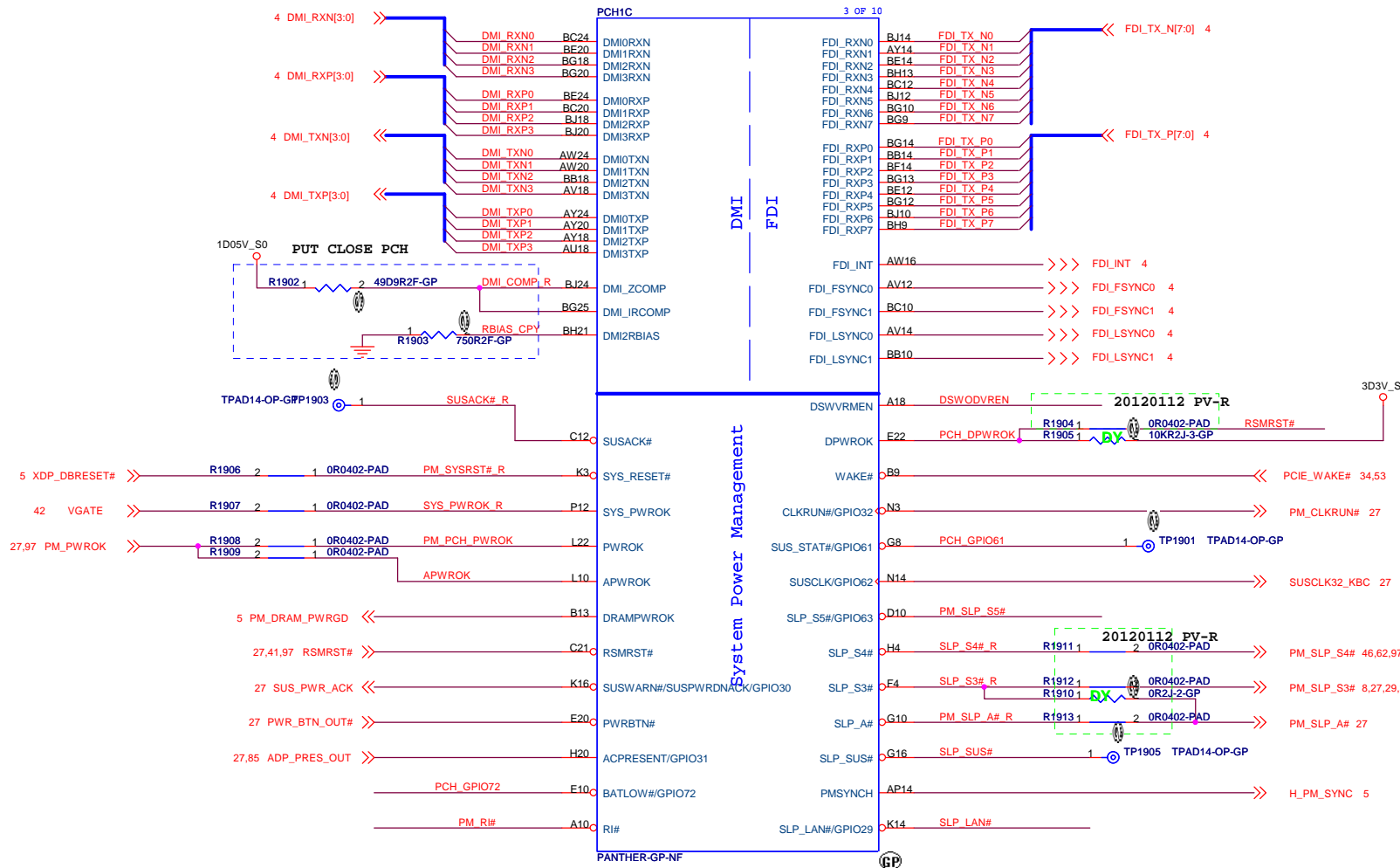
緯創資通 Wistron Corporation
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File: **PCH : PCI/USB/NVRAM/RSVD**

Size: A3 Document Number: **2012 S-Series Richie 13.3** Rev: -1

Date: Wednesday, March 14, 2012 Sheet 18 of 103

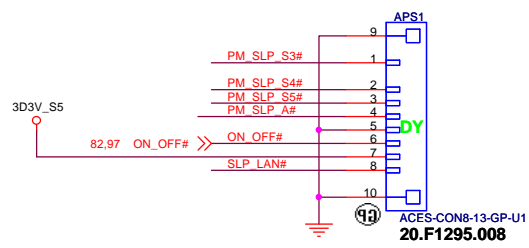
PCH(3/9)



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespective.

AMT/ME COMPLIANCY TEST CONN.



<Core Design>

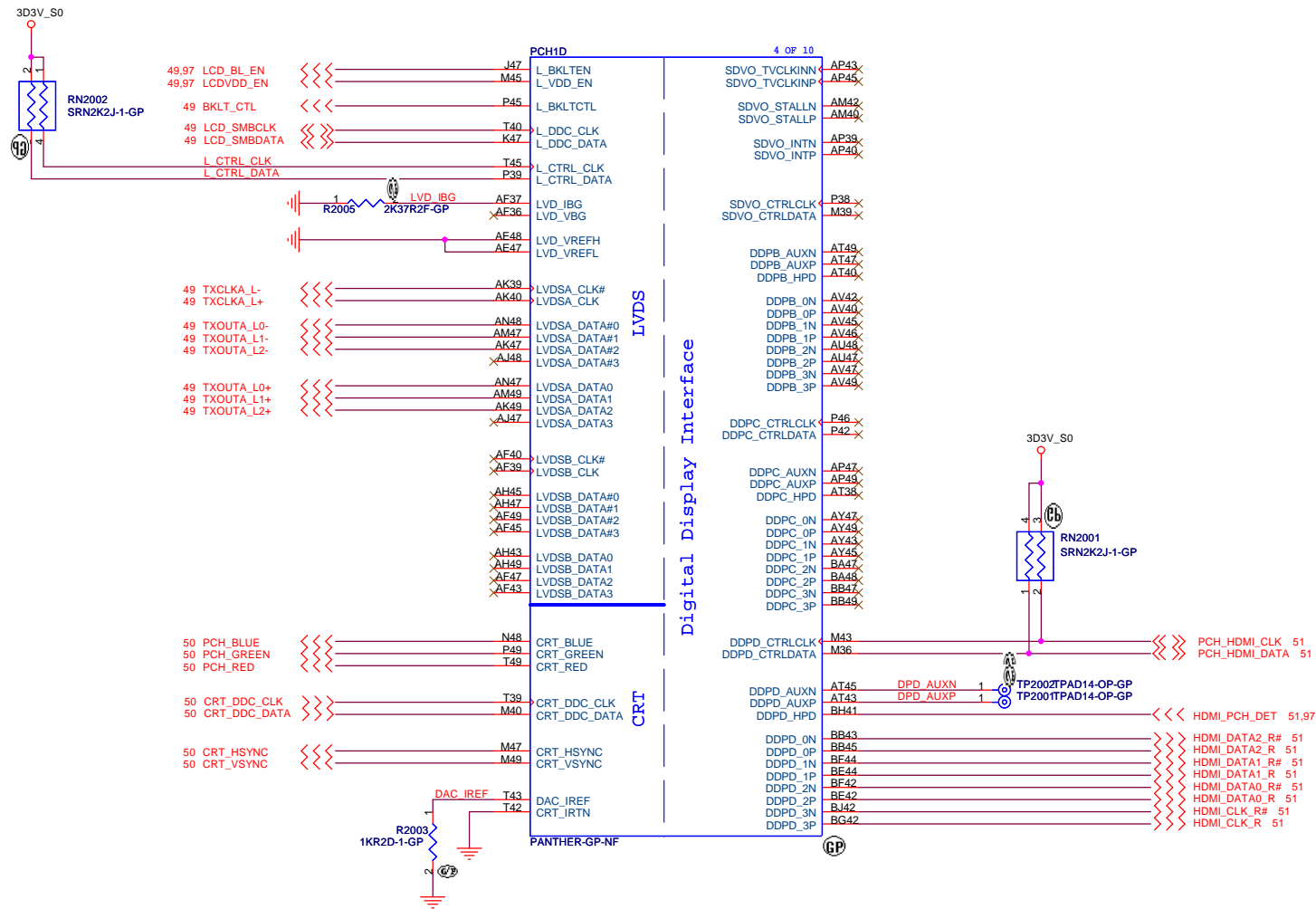
緯創資通 Wistron Corporation
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Title: **PCH(3/9) : DMI/FDI/PM**

Size: A3 Document Number: **2012 S-Series Richie 13.3** Rev: -1

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PCH(4/9)



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PCH(4/9) : LVDS/CRT/DDI	
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GPIO Table	
S 2012 Chief River	PCH GPIO 52
Richie U&D (13 inches)	1
Rocky U&D (14 inches)	1
Rocky U&D (15/17 inches)	0

Boot BIOS Strap		
GNT1#/GPIO51	SATA1GP#/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

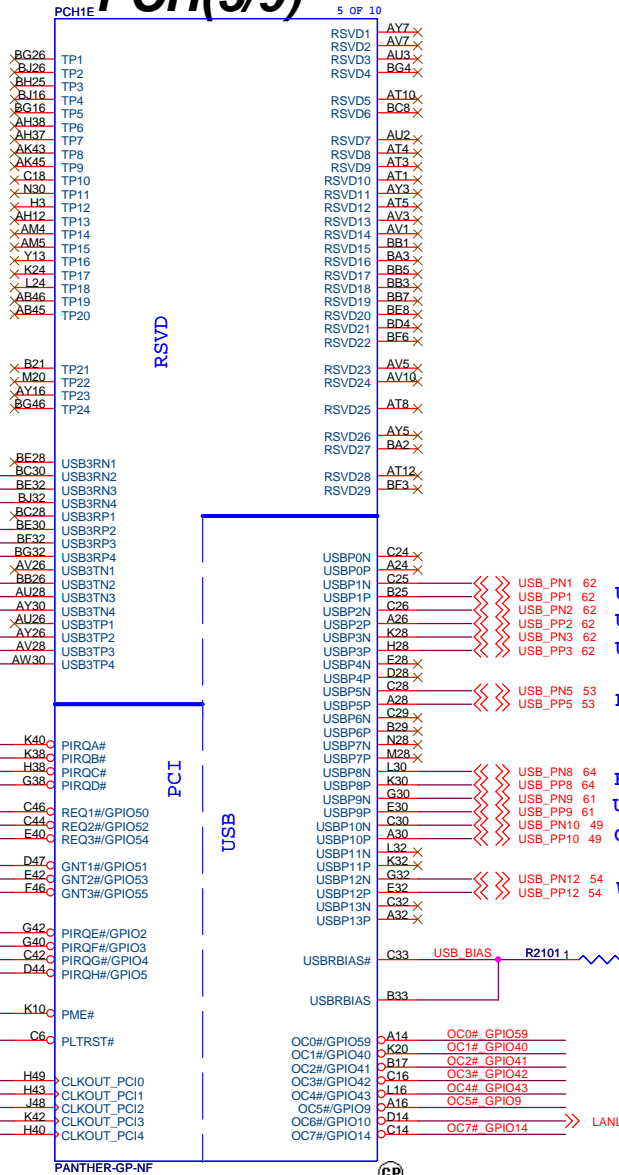
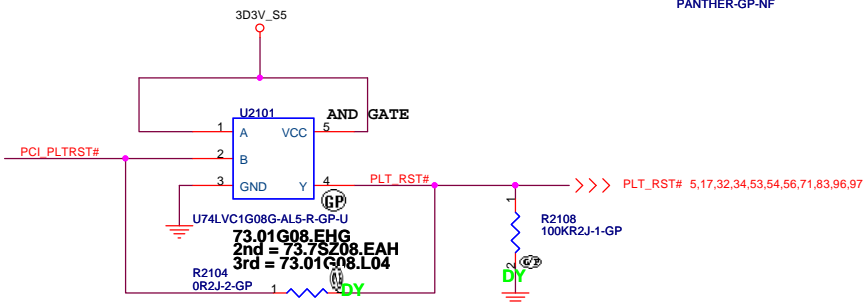
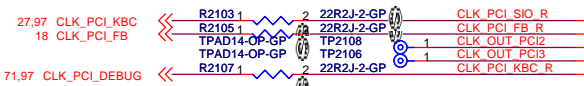
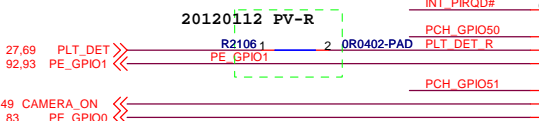
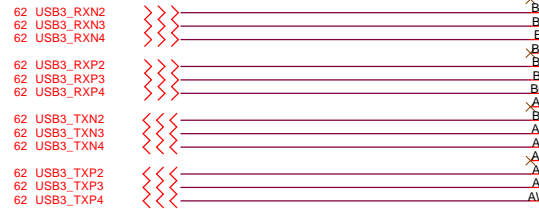
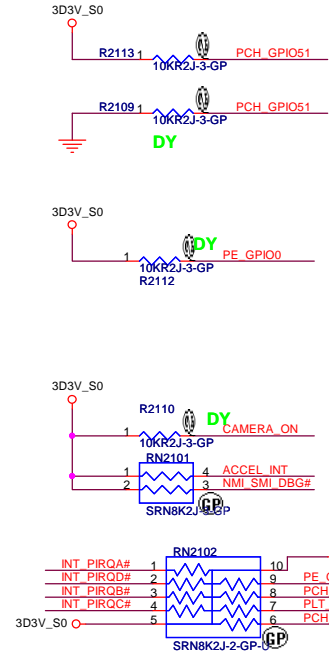
PCH(5/9)

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

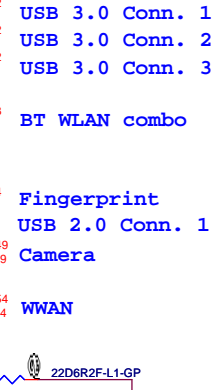
USB3.0 Table

Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3



USB2.0 Table

Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE



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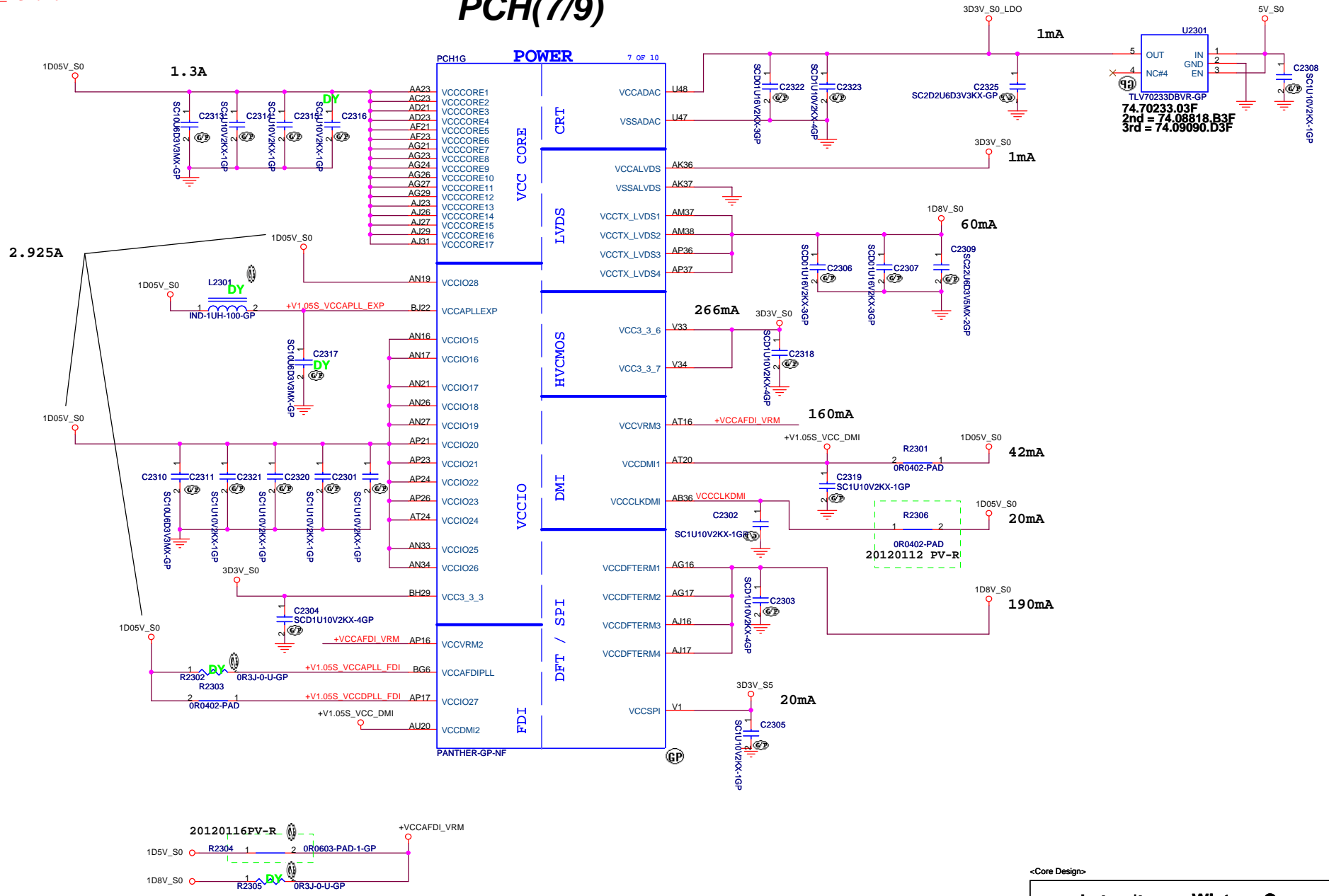
File: **PCH(5/9) : PCI/USB/NVM**

Size: A3 Document Number: **2012 S-Series Richie 13.3** Rev: -1

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VCC_PCH: 6A

PCH(7/9)



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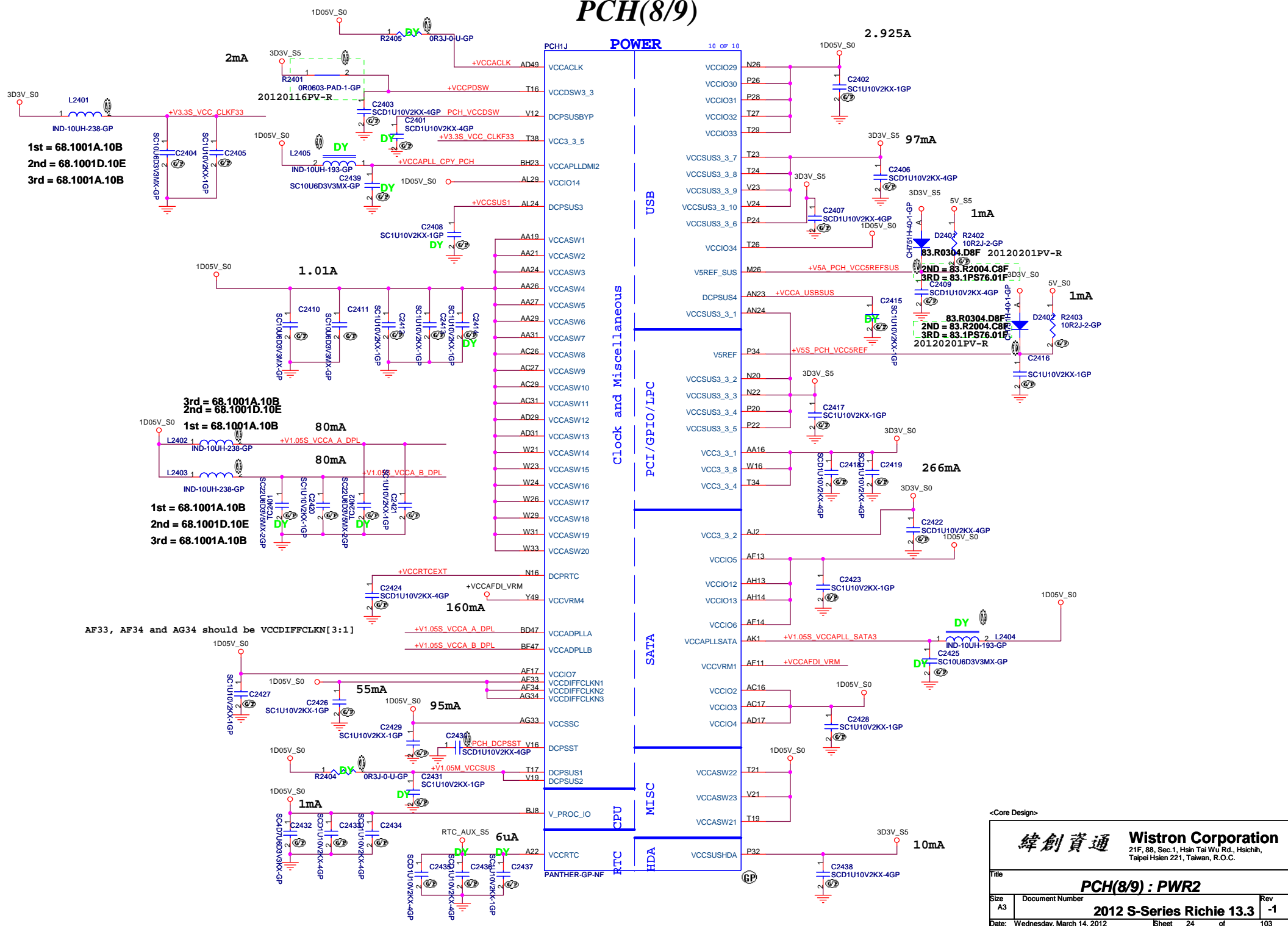
緯創資通 Wistron Corporation
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Title: **PCH(7/9) : PWR1**

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PCH(8/9)



1st = 68.1001A.10B
2nd = 68.1001D.10E
3rd = 68.1001A.10B

3rd = 68.1001A.10B
2nd = 68.1001D.10E

1st = 68.1001A.10B
2nd = 68.1001D.10E
3rd = 68.1001A.10B

AF33, AF34 and AG34 should be VCCDIFFCLKN[3:1]

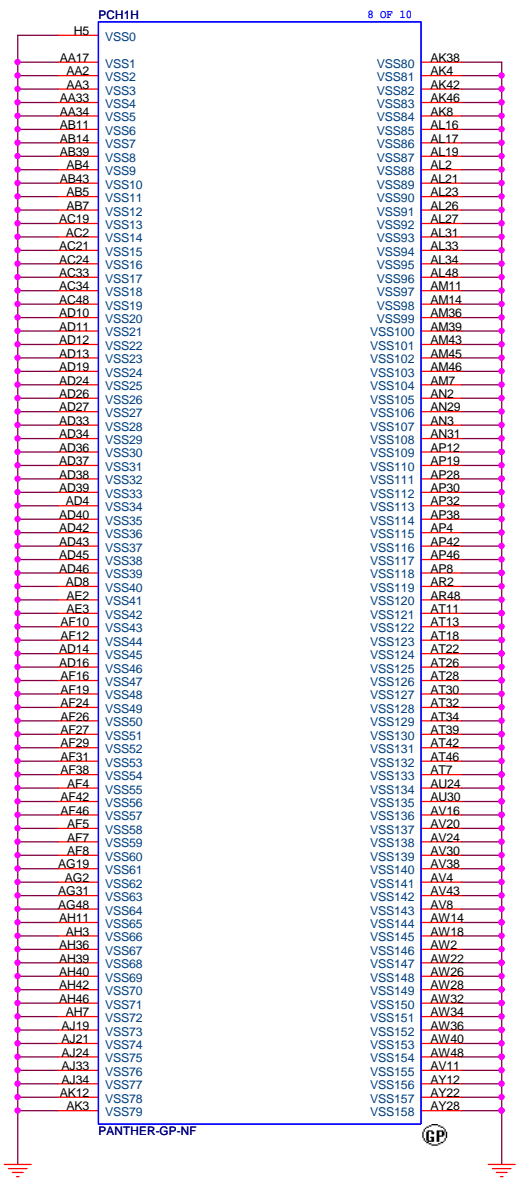
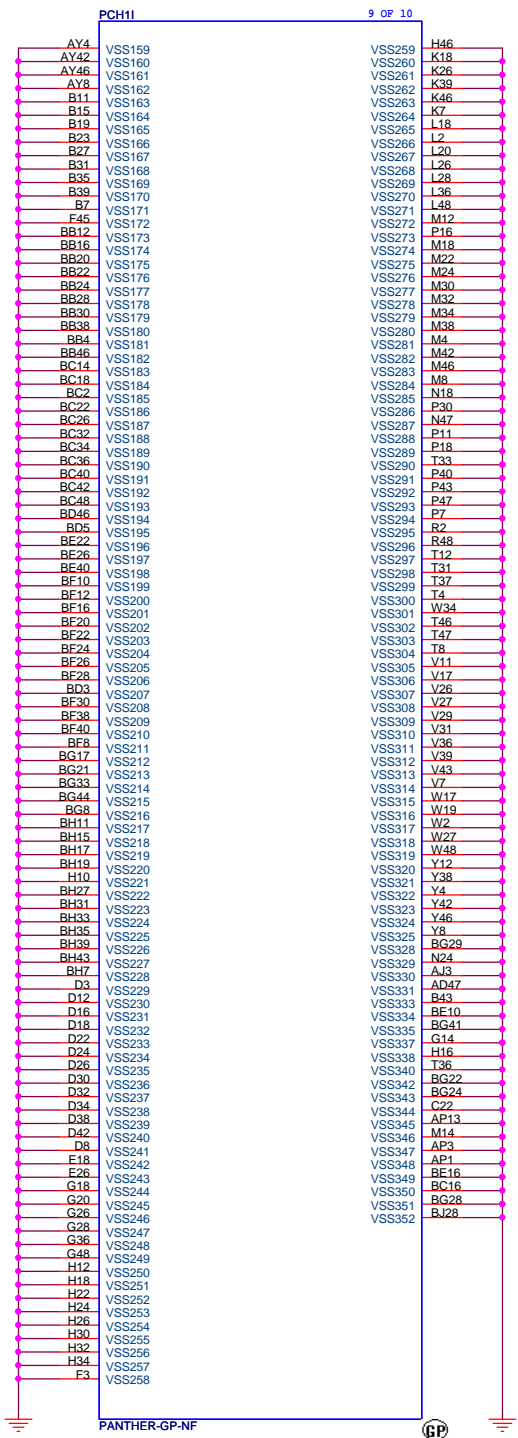
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Title: **PCH(8/9) : PWR2**

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PCH(9/9)



<Core Design>

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Title: **PCH(9/9) : GND**

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<Core Design>

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Title

PCH_XDP

Size
A3

Document Number

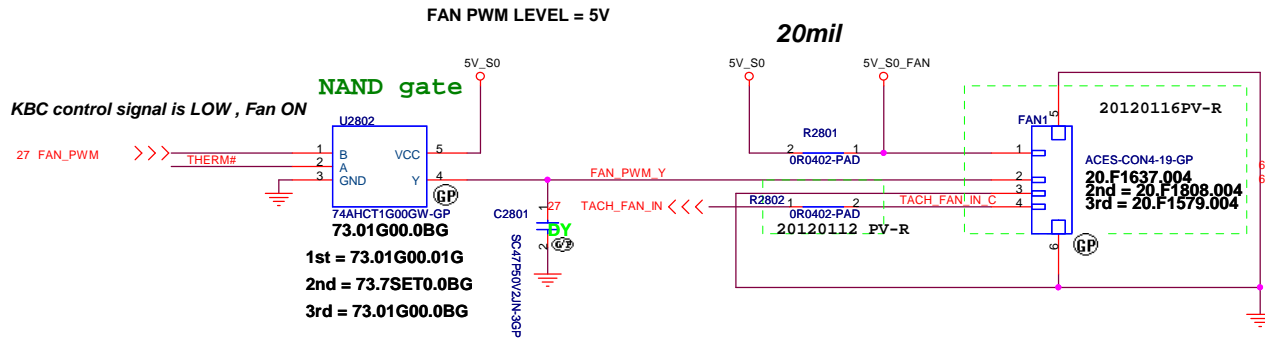
2012 S-Series Richie 13.3

Rev
-1

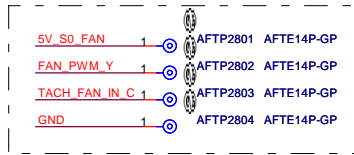
Date: Wednesday, March 14, 2012

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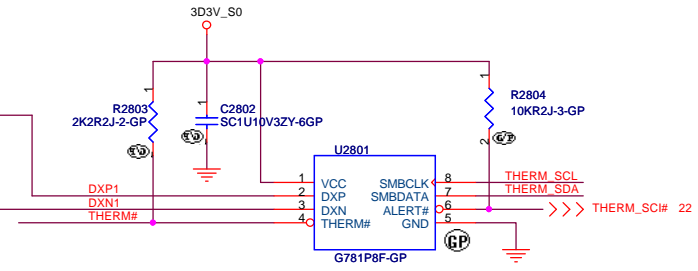
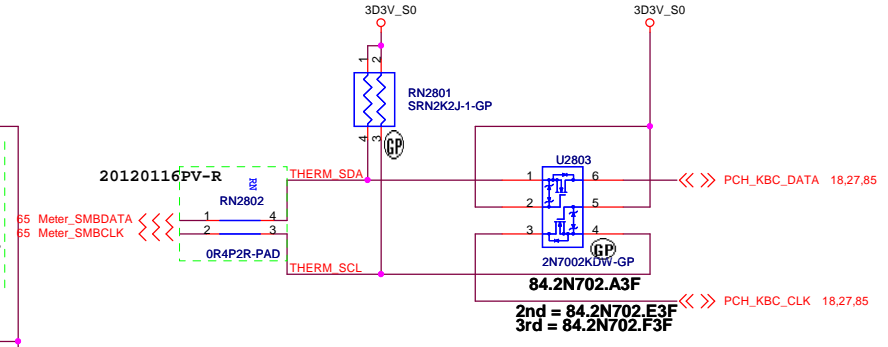
4 WIRE PWM Fan Control circuit



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

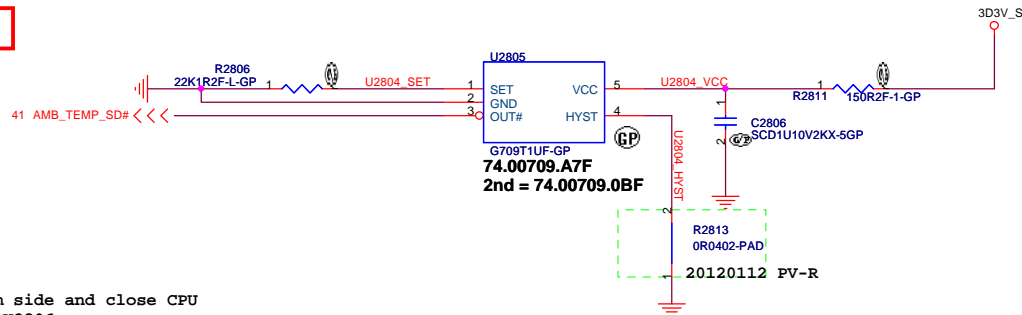


Thermal IC Control circuit



T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K

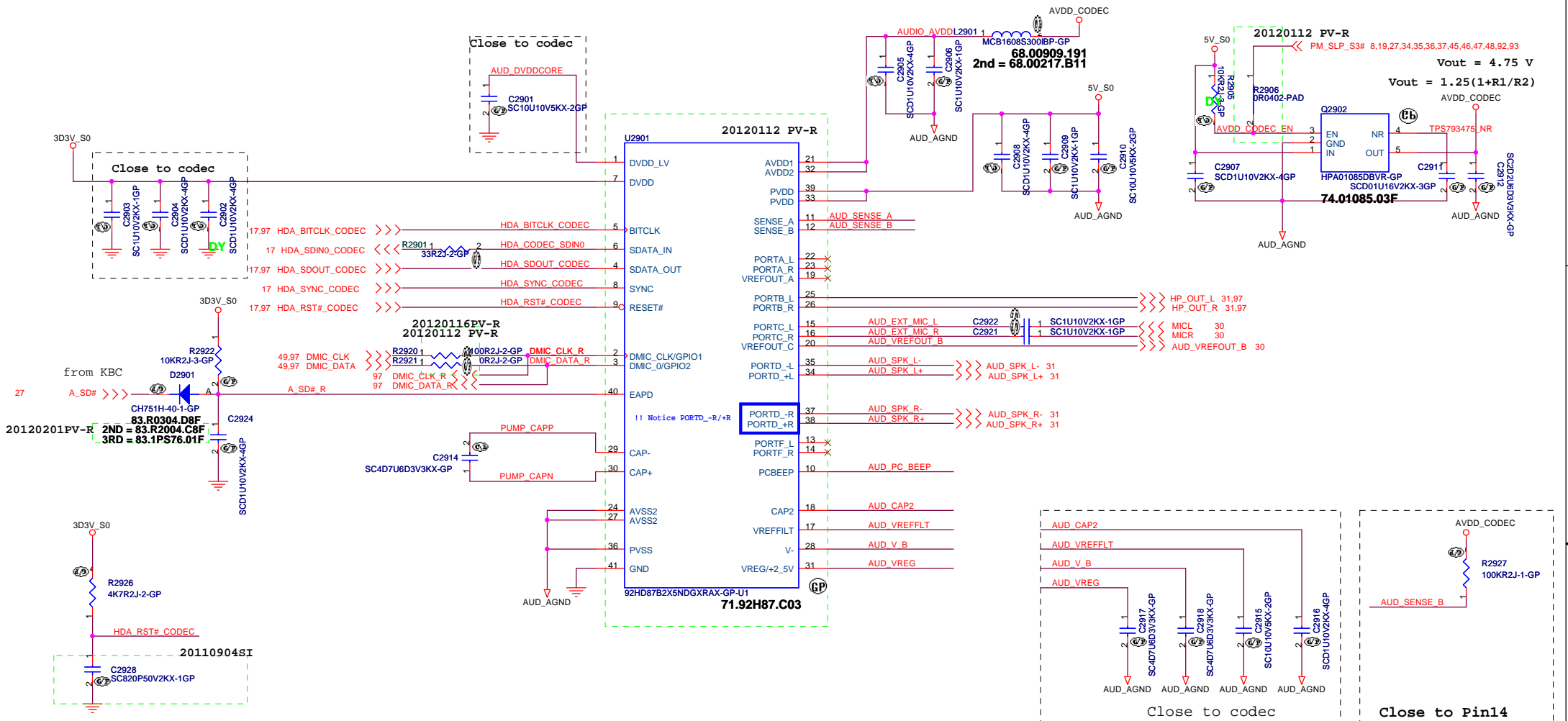


Layout: PUT U2805 Bottom side and close CPU
PUT R2806 Close U2806

<Core Design>

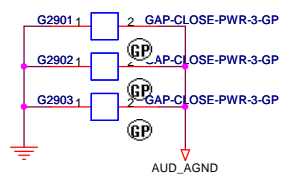
緯創資通 Wistron Corporation
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Title		
Thermal G781 / FAN		
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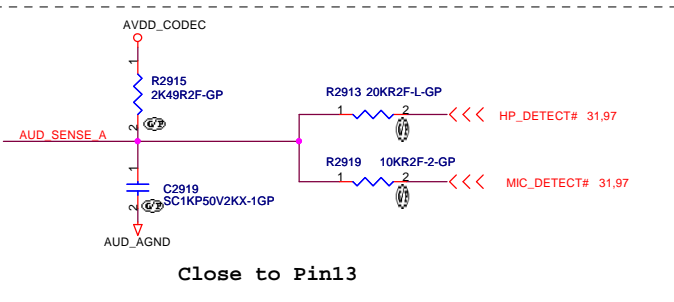
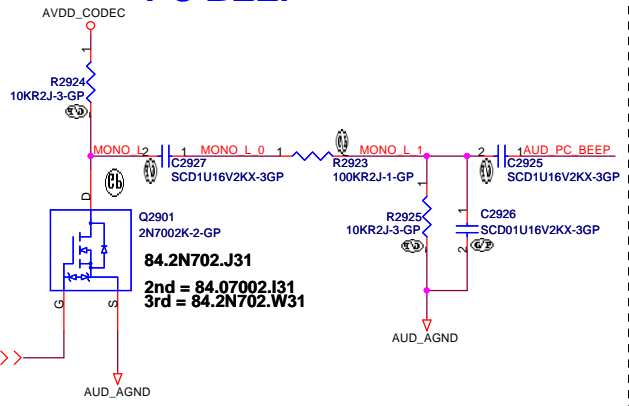
Digital GND & AUD_AGND

Tie Analog GND and Digital GND under codec by a single point



audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



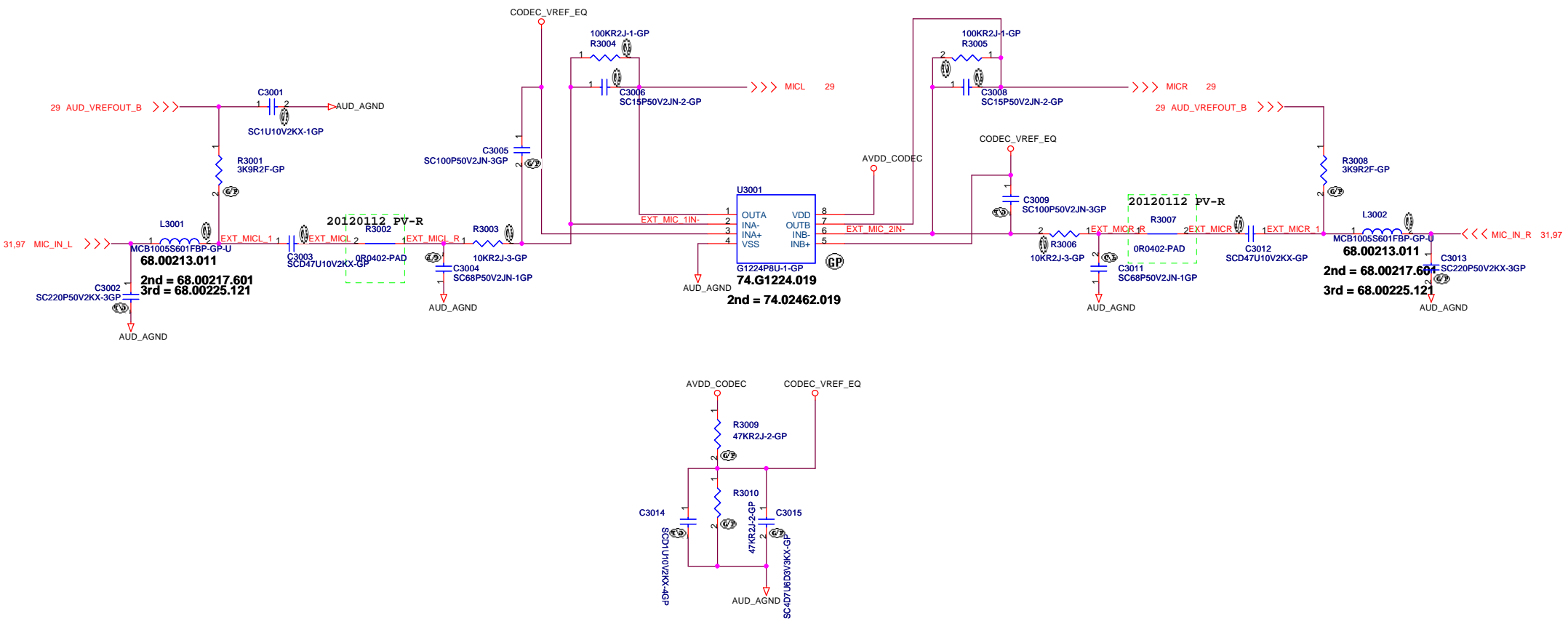
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Codec 92HD87B2X5**

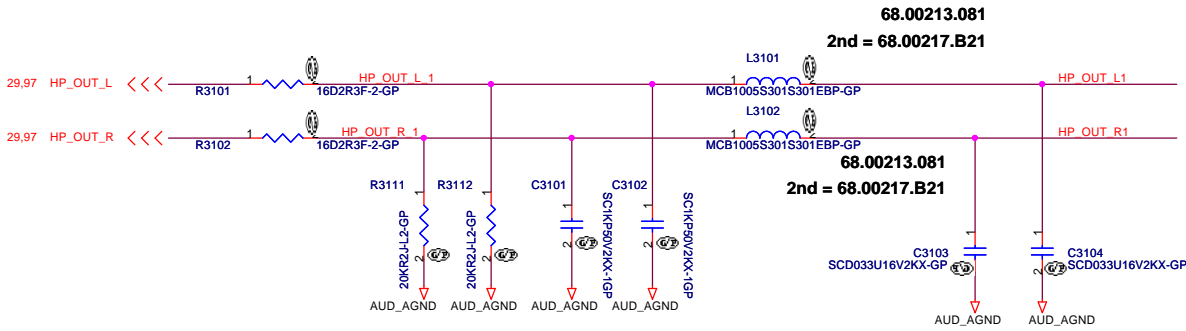
Size: A3 Document Number: **2012 S-Series Richie 13.3** Rev: -1

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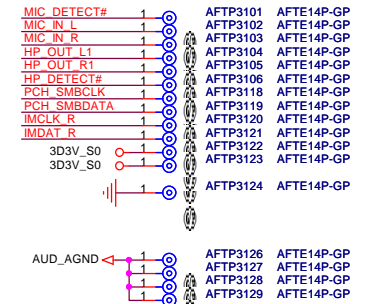
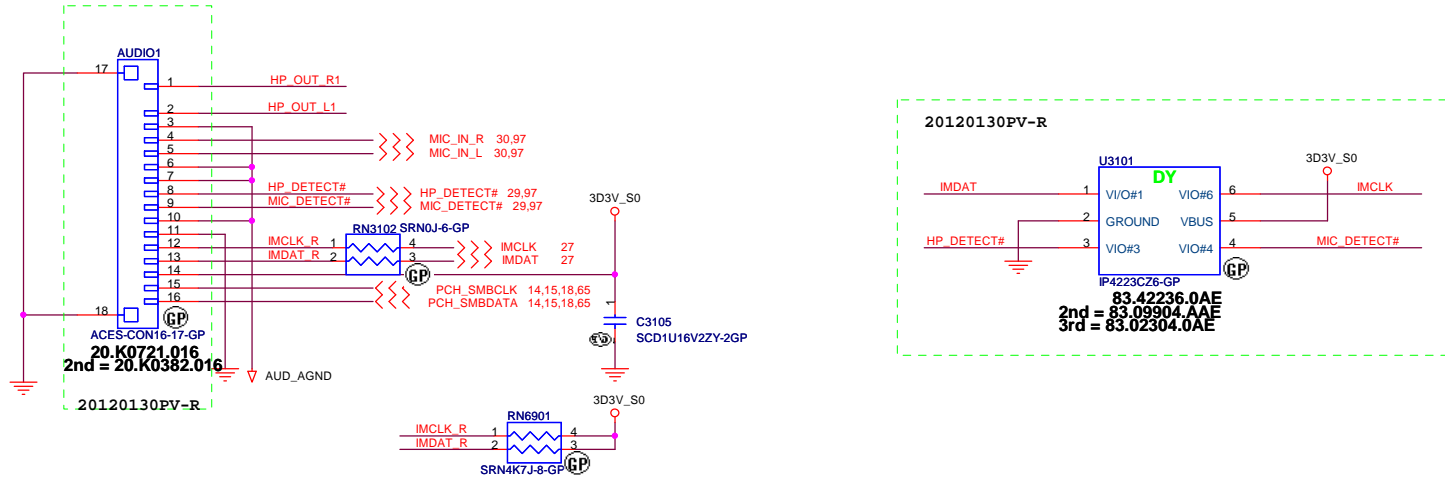
Pre-AMP. for External MIC



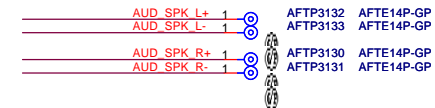
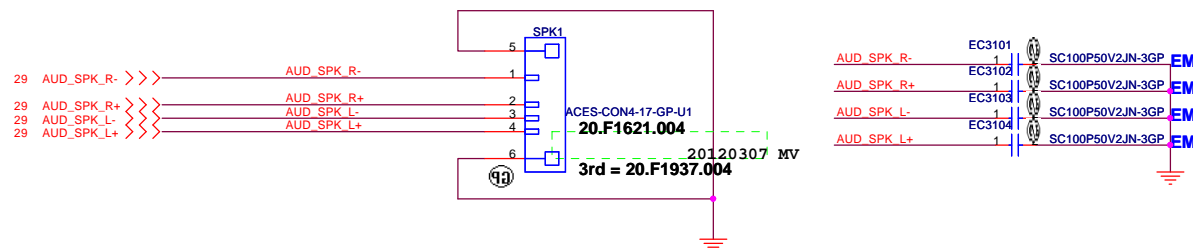
HeadPhone OUT



Audio Board + Touch Pad Connector



Speaker Connector



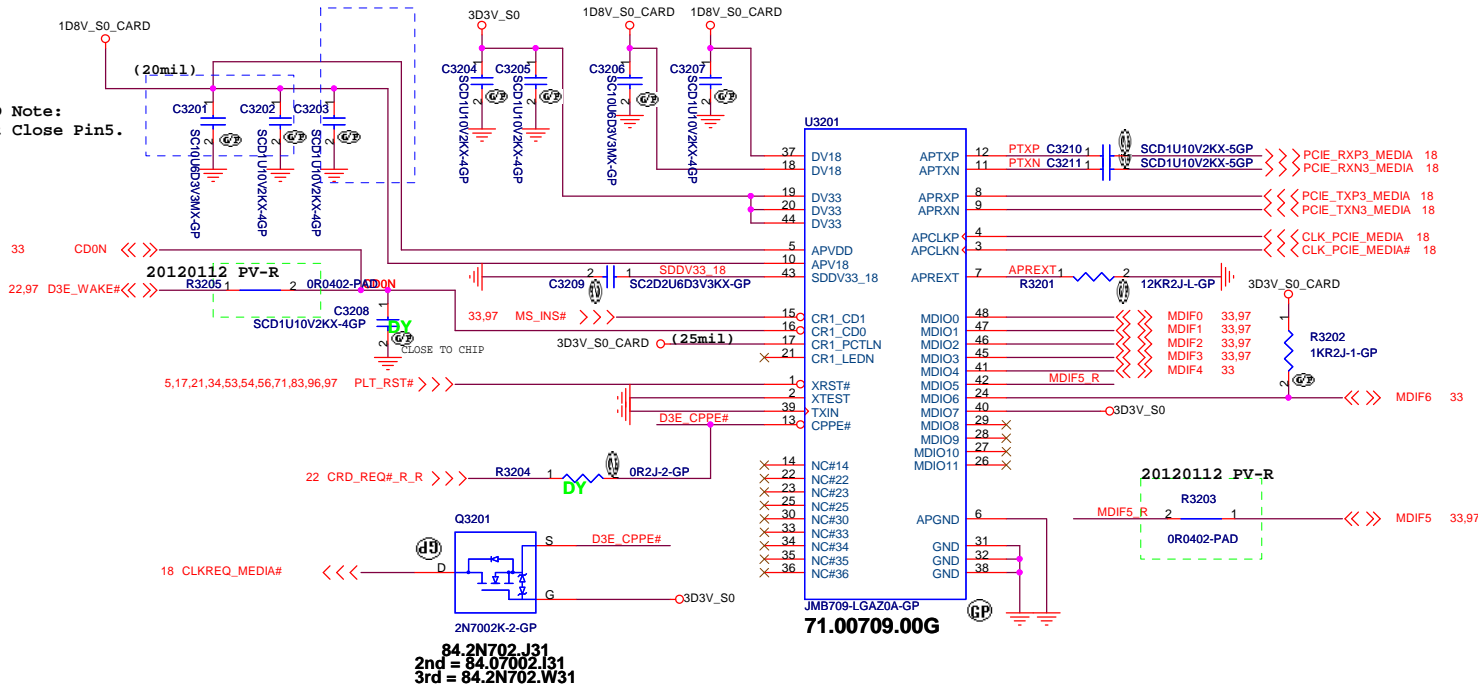
<Core Design>

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AUDIO Connector			
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CardReader JMicron JMB709

CAD Note:
Put Close Pin10

CAD Note:
Put Close Pin5.



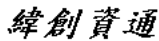
D3E Detection Table

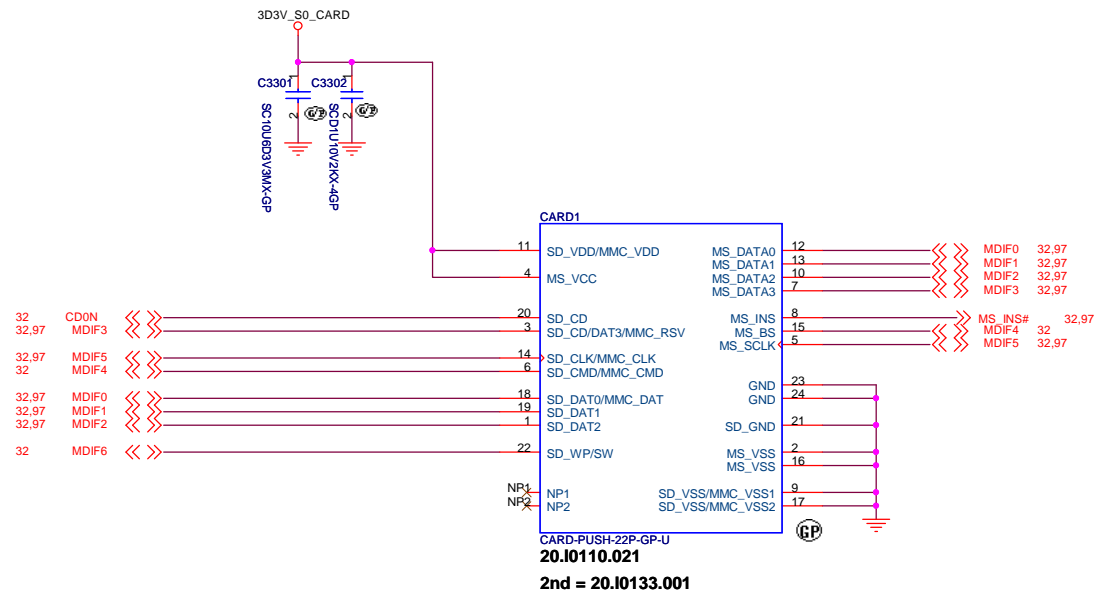
D3E_CPPE#	Status
H	D3E mode
L	Normal mode

CR1_CDxN Detection Table

CR1_CDxN	Card Type
1 0	(No Card)
H H	(No Card)
H L	SD Card/MMC
L H	MemoryStick
L L	XD Card

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Card Reader-JMB 709		
Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012		
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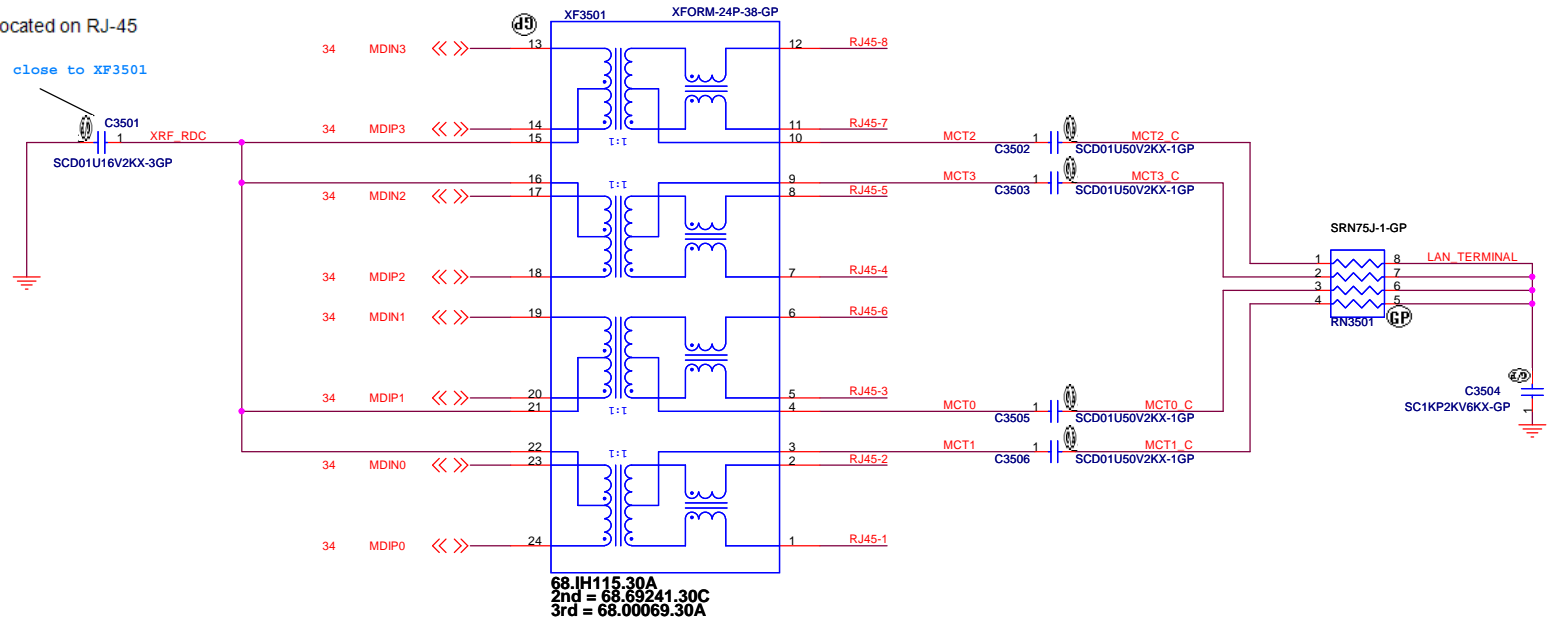
Pin Name	Default Mode	SD/MMC Card	MS Card
MDIO0	SD/MMC/MS	SD1_DAT0	MS1_DAT0
MDIO1		SD1_DAT1	MS1_DAT1
MDIO2		SD1_DAT2	MS1_DAT2
MDIO3		SD1_DAT3	MS1_DAT3
MDIO4		SD1_CMD	MS1_BS
MDIO5		SD1_CLK	MS1_CLK
MDIO6		SD1_WP	
MDIO7			
MDIO8		MMC_DAT4	MS1_DAT4
MDIO9		MMC_DAT5	MS1_DAT5
MDIO10		MMC_DAT6	MS1_DAT6
MDIO11		MMC_DAT7	MS1_DAT7
CR1_LEDN		SD1_LED#	MS1_LED#
CR1_PCTLN		SD1_PCTL#	MS1_PCTL#
CR1_CD0		SD1_CD#	
CR1_CD1			MS1_CD#

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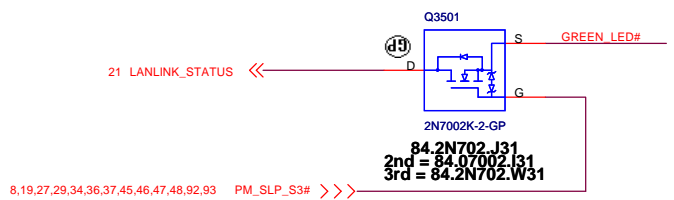
Title			
SD/MS/MMC CONNECTOR			
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White LED for connectivity and Amber LED for activity located on RJ-45 connector ↗



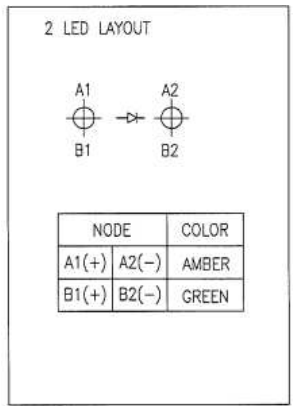
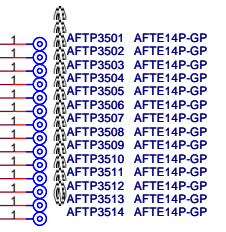
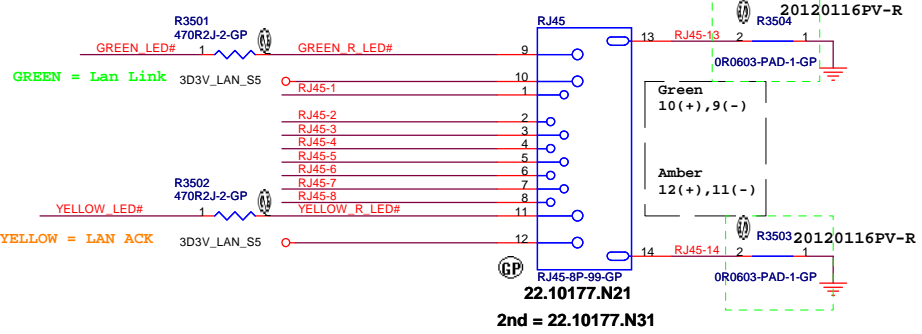
68.IH115.30A
2nd = 68.69241.30C
3rd = 68.00069.30A

RJ45 Connector



8,19,27,29,34,36,37,45,46,47,48,92,93 PM_SLP_S3# >>>

34,97 GREEN_LED# >>>
34,97 YELLOW_LED# >>>



- (1) route on bottom as differential pairs.
- (2) Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- (3) No vias, No 90 degree bends.
- (4) pairs must be equal lengths.
- (5) 6mil trace width, 12mil separation.
- (6) 36mil between pairs and any other trace.
- (7) Must not cross ground moat, except RJ-45 moat.

<Core Design>

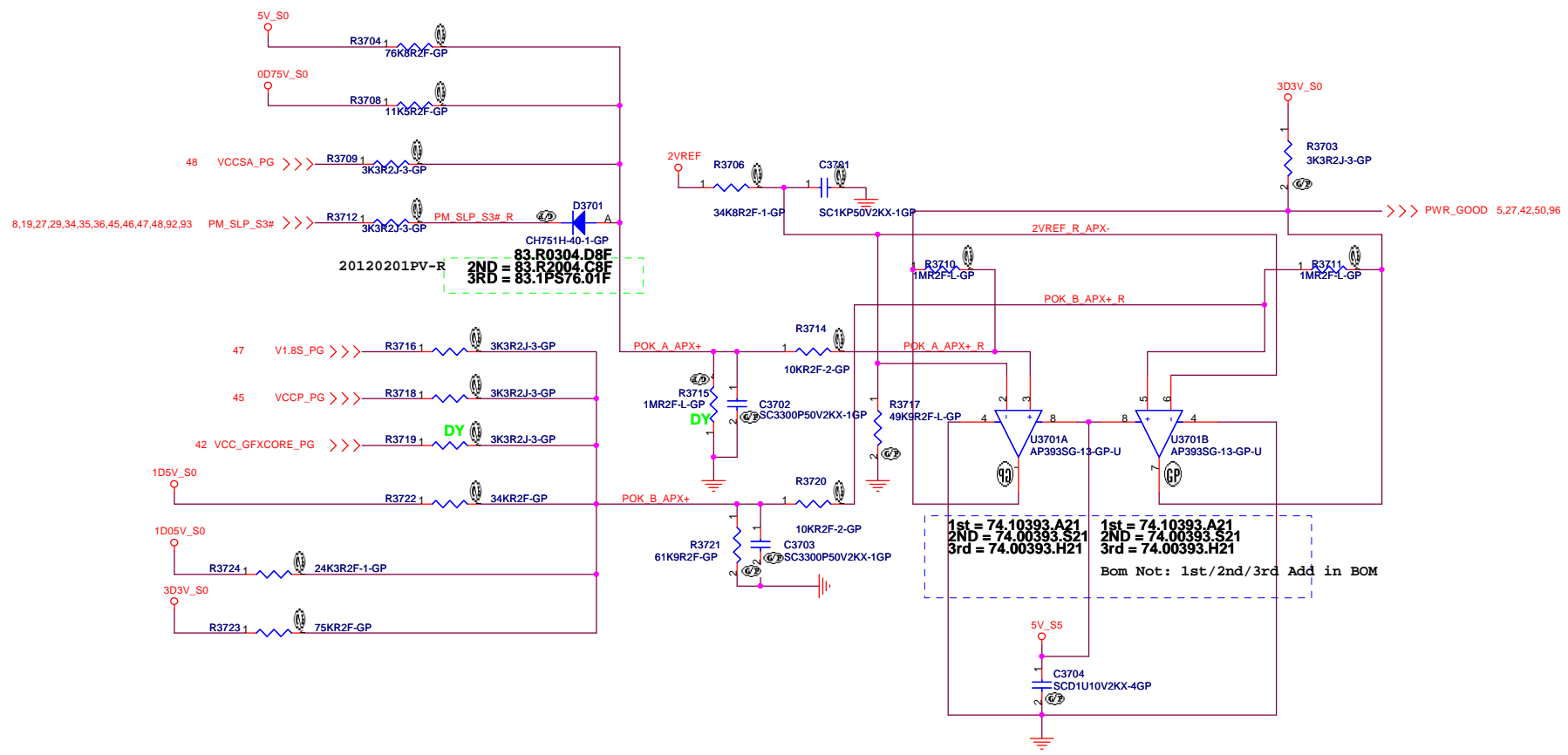
緯創資通 Wistron Corporation
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Title: **LAN RJ45**

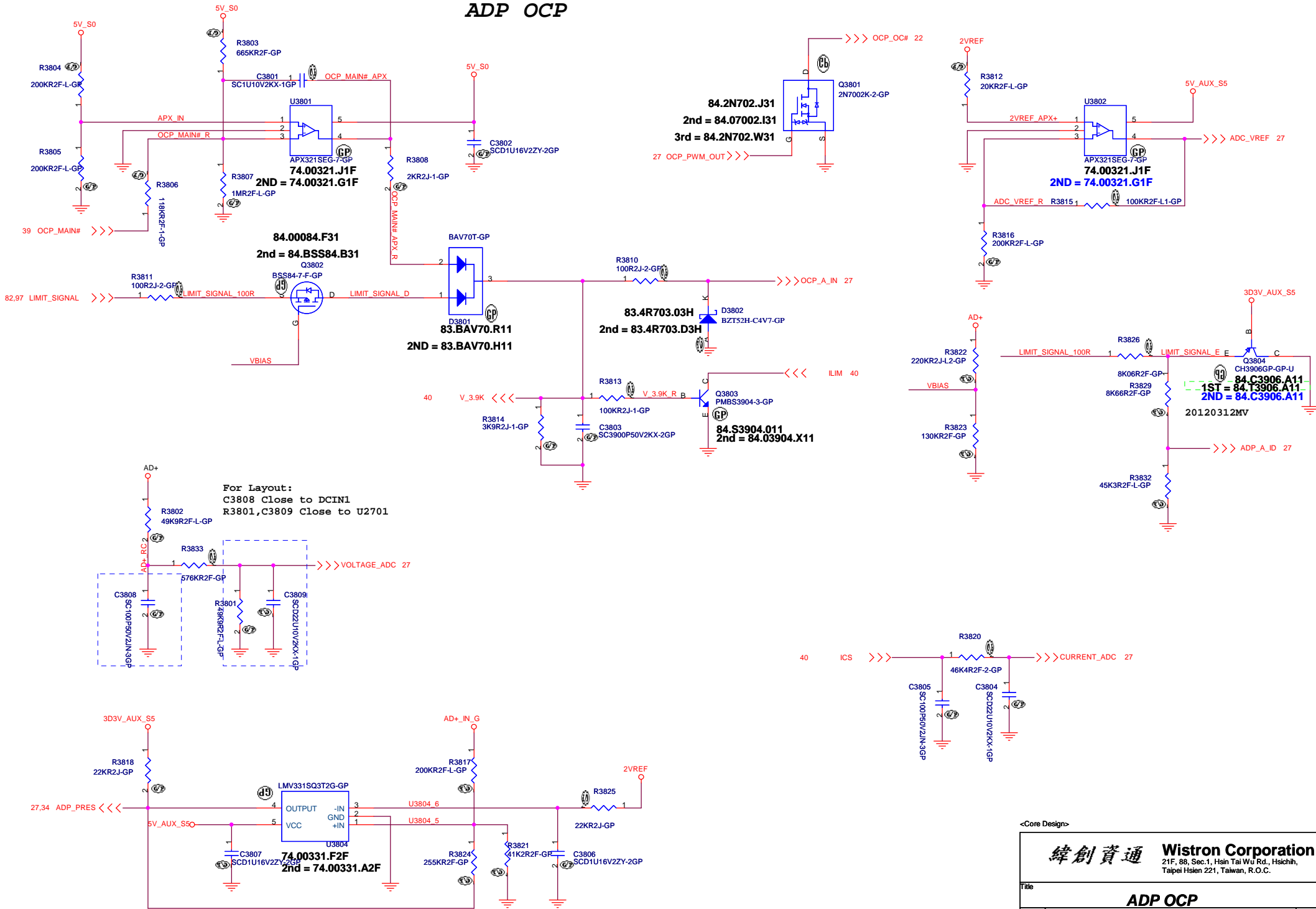
Size: A3 Document Number: **2012 S-Series Richie 13.3** Rev: -1

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POK

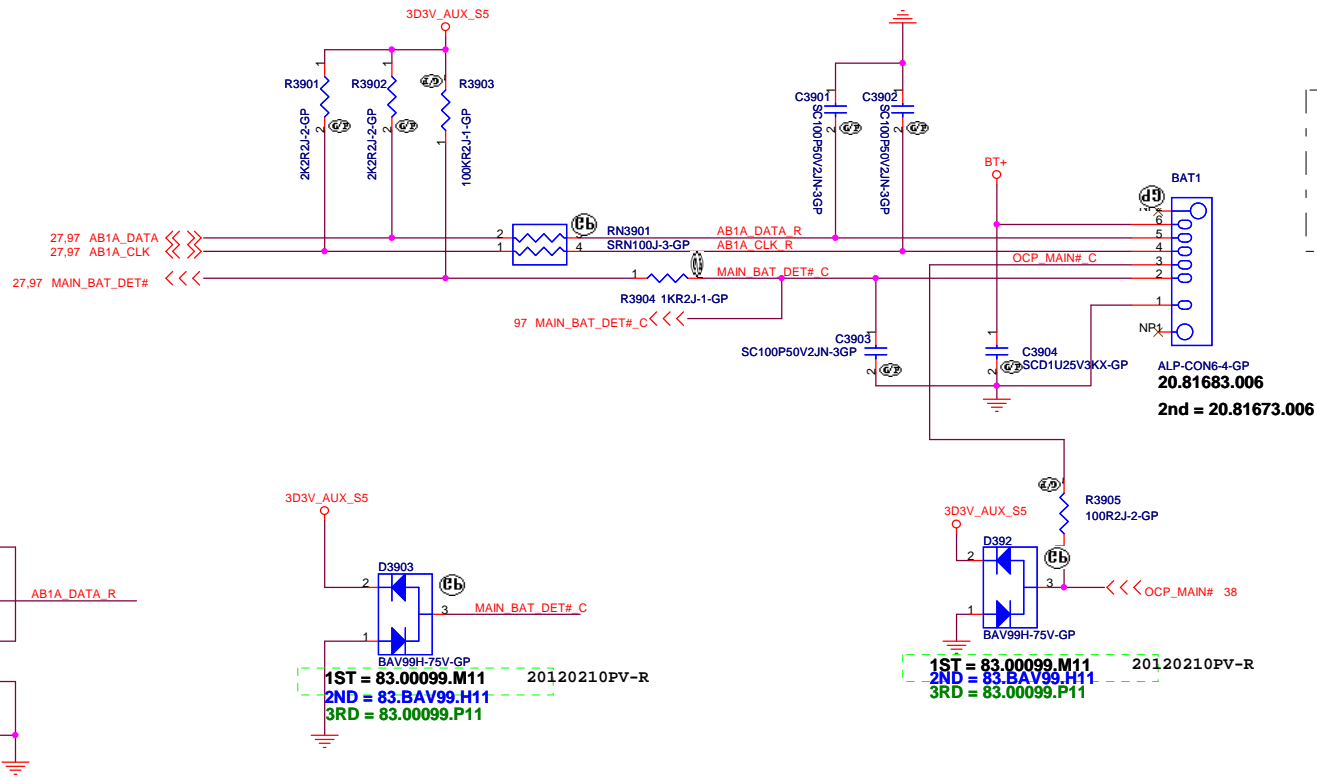


ADP OCP

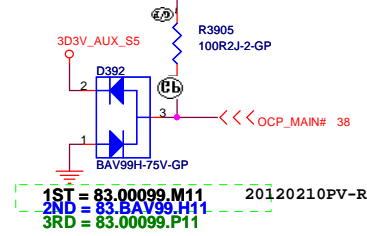
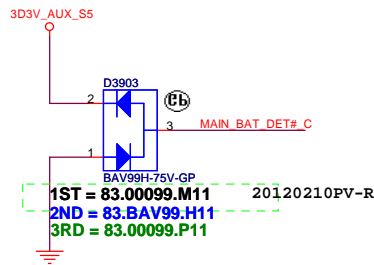
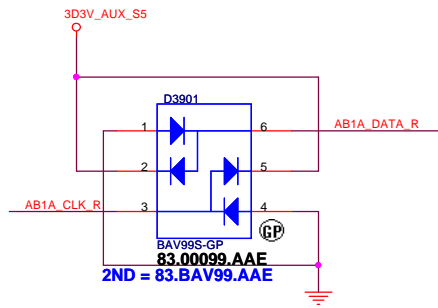


For Layout:
 C3808 Close to DCIN1
 R3801, C3809 Close to U2701

Battery Connector

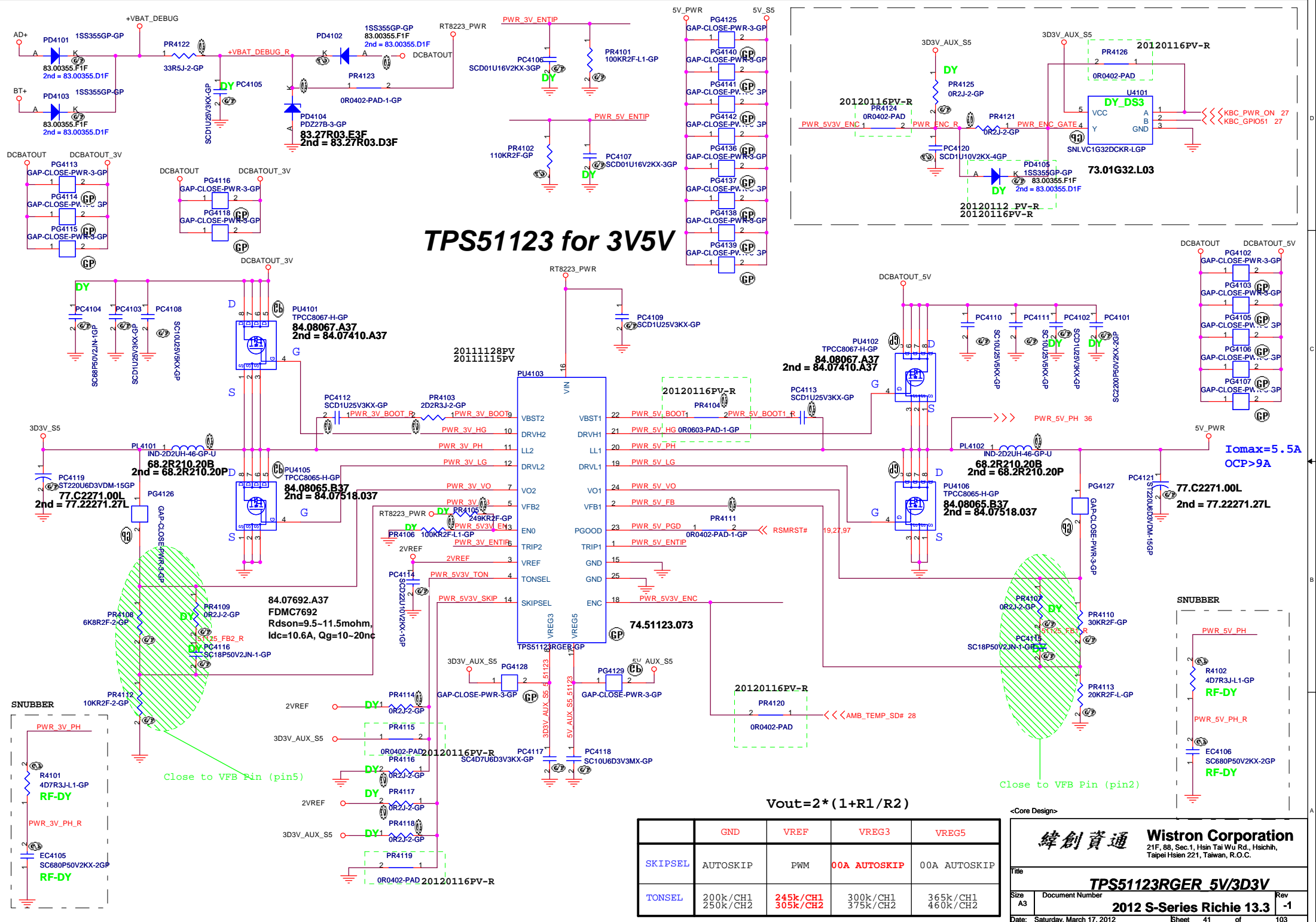


BT+	1	AFTP3901	AFTE14P-GP
BT+	1	AFTP3902	AFTE14P-GP
AB1A_DATA_R	1	AFTP3903	AFTE14P-GP
AB1A_CLK_R	1	AFTP3904	AFTE14P-GP
MAIN_BAT_DET#_C	1	AFTP3905	AFTE14P-GP
OCP_MAIN#_C	1	AFTP3906	AFTE14P-GP
GND	1	AFTP3907	AFTE14P-GP
GND	1	AFTP3908	AFTE14P-GP



<Core Design>

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BATT CONN	
Size A3	Document Number 2012 S-Series Richie 13.3
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TPS51123 for 3V5V

$$W_{out} = 2 * (1 + R1/R2)$$

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

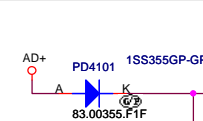
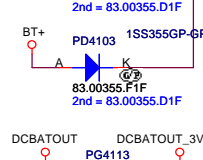
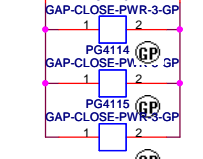
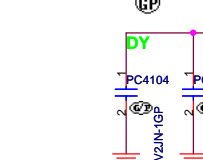
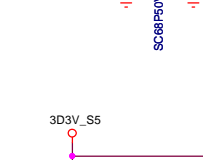
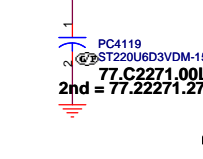
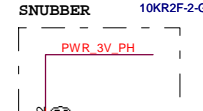
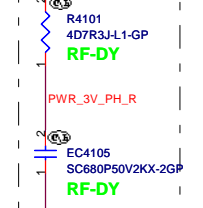
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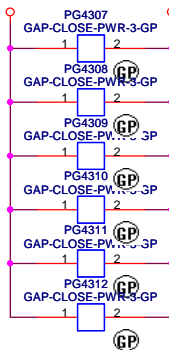
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Size A3 Document Number **2012 S-Series Richie 13.3** Rev -1

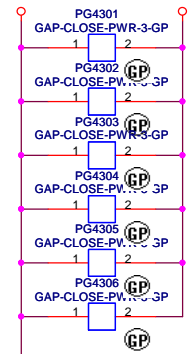
Date: Saturday, March 17, 2012 Sheet 41 of 103



DCBATOUT PWR_VCCCORE2_DCBATOUT



DCBATOUT PWR_VCCCORE1_DCBATOUT



Vcc_core
 Iccmax=53A
 Itdc=36A
 OCP>65A

- 42 PWR_VCORE_HG2
- 42 PWR_VCORE_SW2
- 42 PWR_VCORE_LG2

PU4303
 FDMS7698-GP
 84.07698.037
 2nd = 84.06414.037

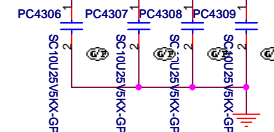
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 FDMS0302S-GP
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 2nd = 84.06512.037

PU4301
 FDMS7698-GP
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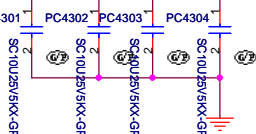
PU4302
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- 42 PWR_VCORE_HG1
- 42 PWR_VCORE_SW1
- 42 PWR_VCORE_LG1

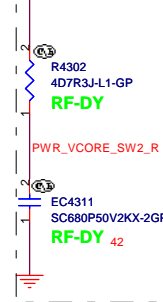
PWR_VCCCORE2_DCBATOUT



PWR_VCCCORE1_DCBATOUT



SNUBBER

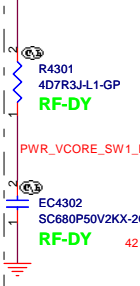


IND-D24UH-1-GP
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 2nd = 68.R2610.101

PT4304
 ST470UF2VDM-GP
 1st = 79.47719.2BL
 2nd = 77.24771.13L
 3rd = 79.47719.2BL

PT4305
 ST470UF2VDM-GP
 1st = 79.47719.2BL
 2nd = 77.24771.13L
 3rd = 79.47719.2BL

SNUBBER



IND-D24UH-1-GP
 68.R2410.201
 2nd = 68.R2610.101

PT4301
 ST470UF2VDM-GP
 1st = 79.47719.2BL
 2nd = 77.24771.13L
 3rd = 79.47719.2BL

PT4303
 ST470UF2VDM-GP
 1st = 79.47719.2BL
 2nd = 77.24771.13L
 3rd = 79.47719.2BL

PWR_VCORE_CSREF_R

PWR_VCORE_CSREF

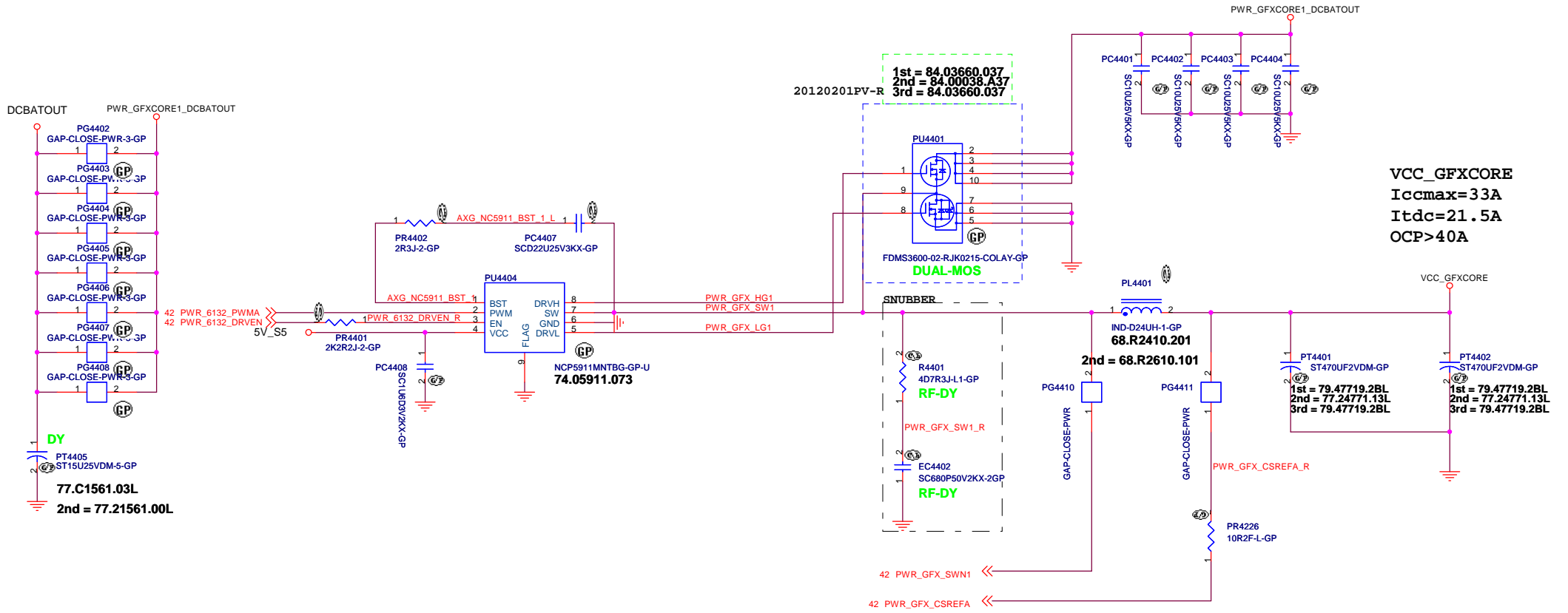
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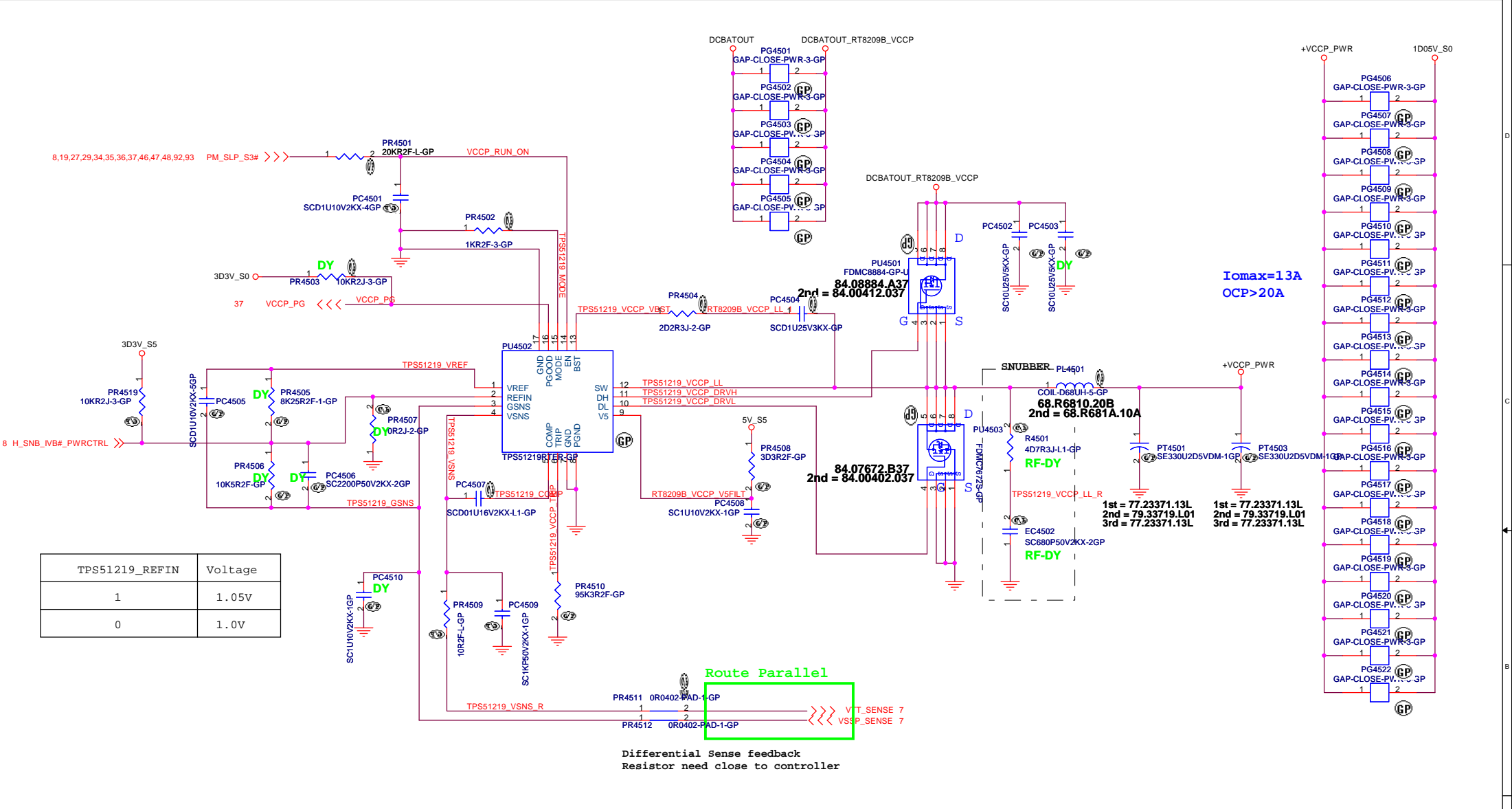
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Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
Date: Wednesday, March 14, 2012	Sheet: 43	of 103



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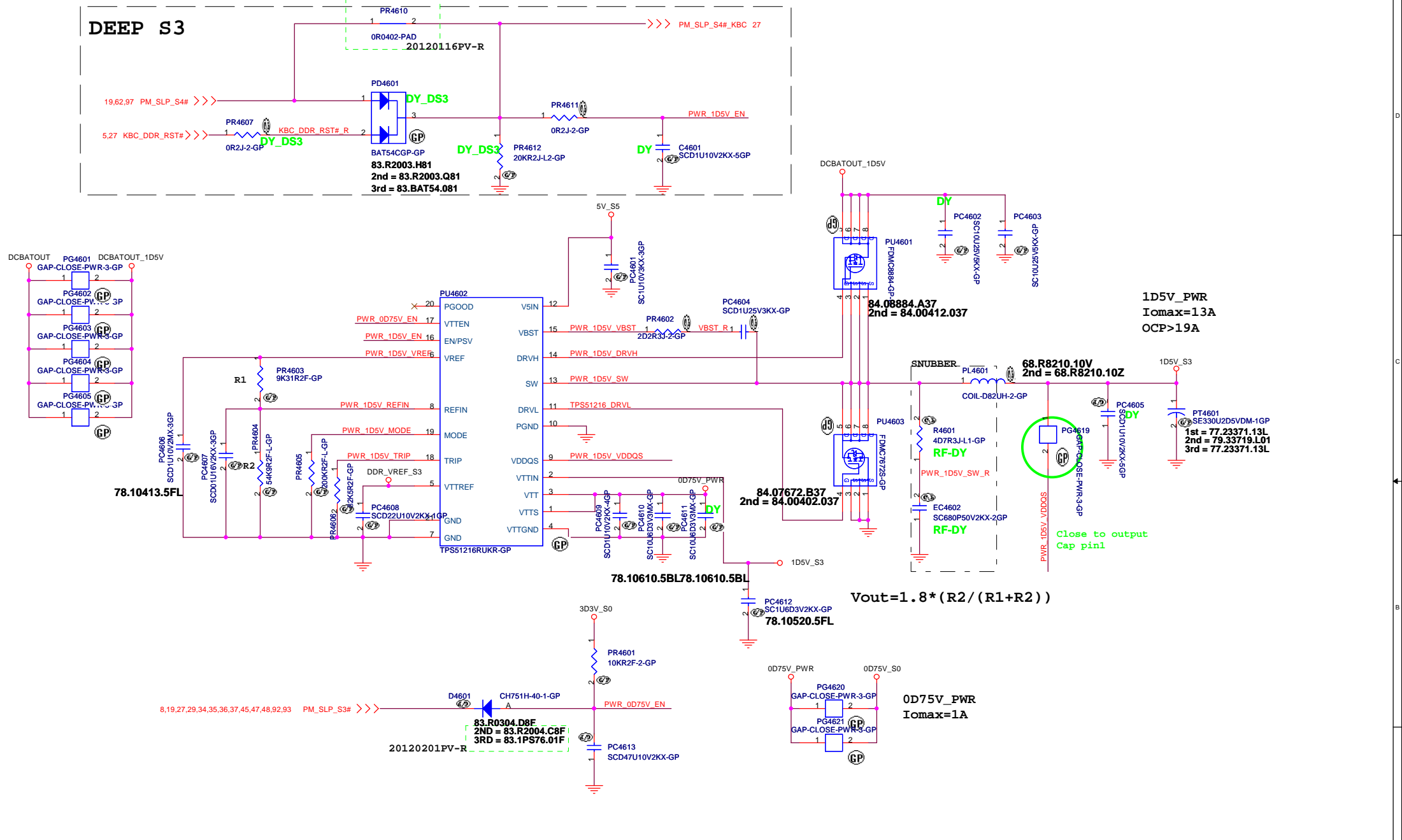
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
ISL95832 IMVP7-3/3	
Title	-1
Size A3	2012 S-Series Richie 13.3
Date: Monday, March 19, 2012	Sheet 44 of 103



Route Parallel

Differential Sense feedback
Resistor need close to controller

DEEP S3

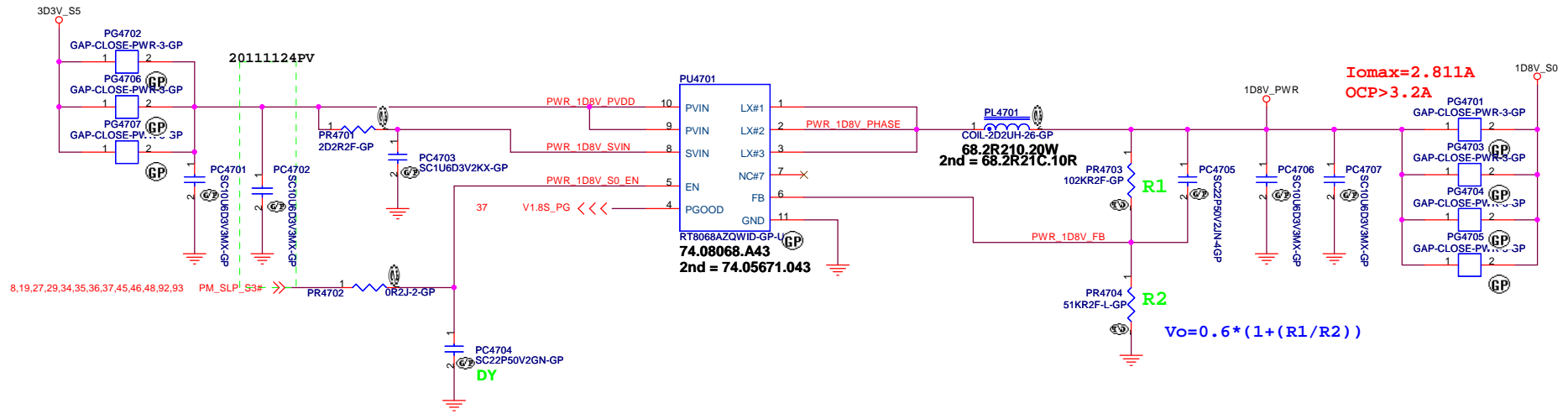


1D5V_PWR
I_{omax}=1.3A
OCP>19A

$$V_{out} = 1.8 * (R2 / (R1 + R2))$$

0D75V_PWR
I_{omax}=1A

RT8068A for 1D8V_S0

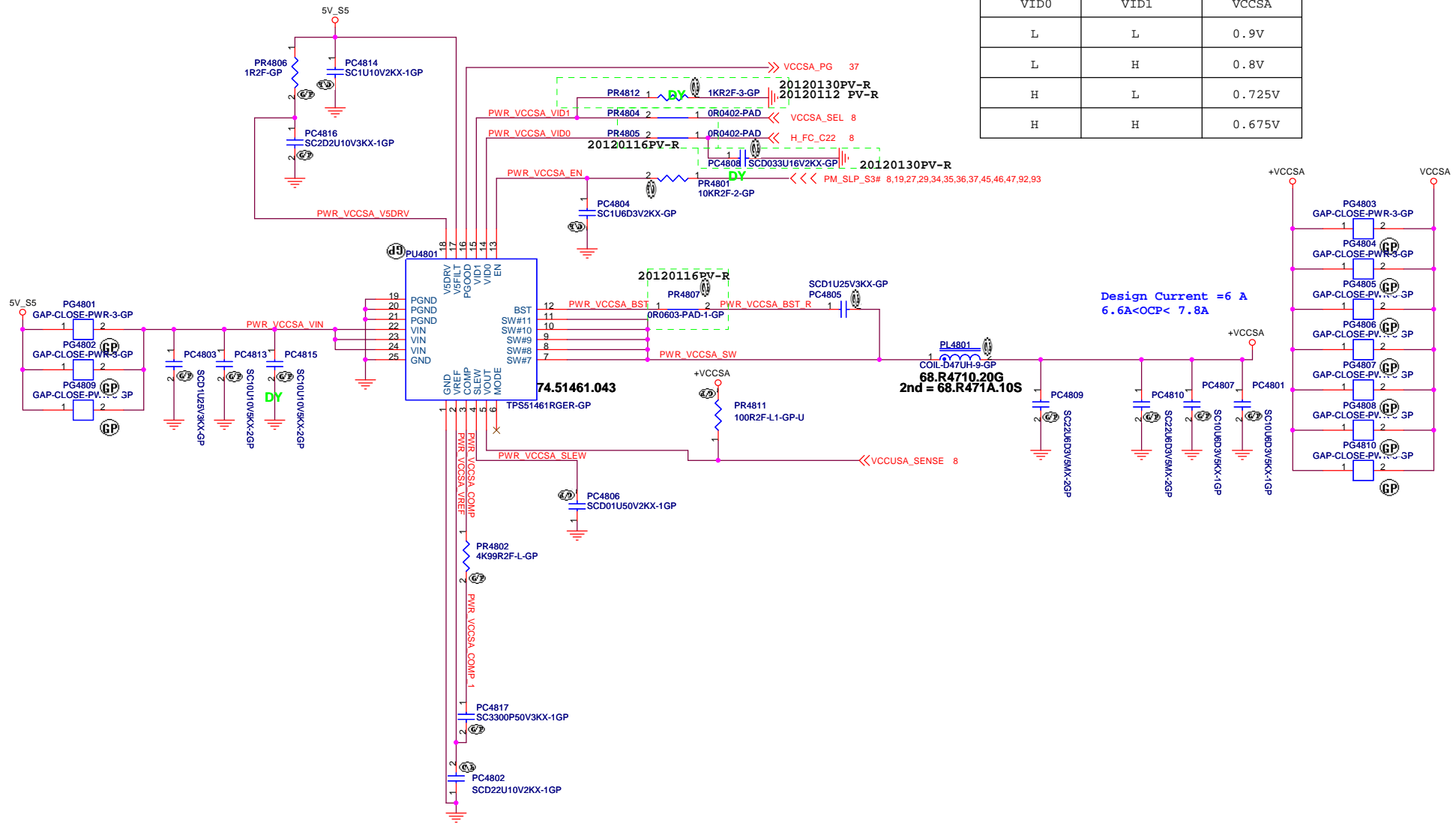


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 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
1D8V_S0	
Title 1D8V_S0	Document Number 2012 S-Series Richie 13.3
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TPS51461 for VCCSA

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



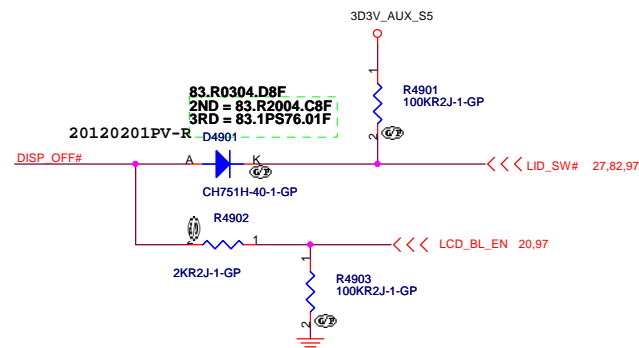
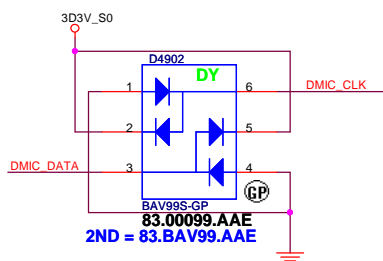
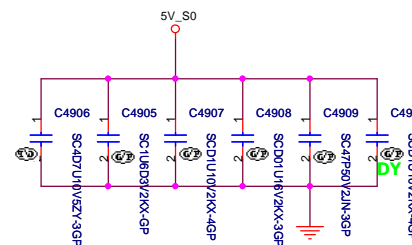
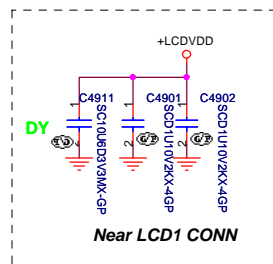
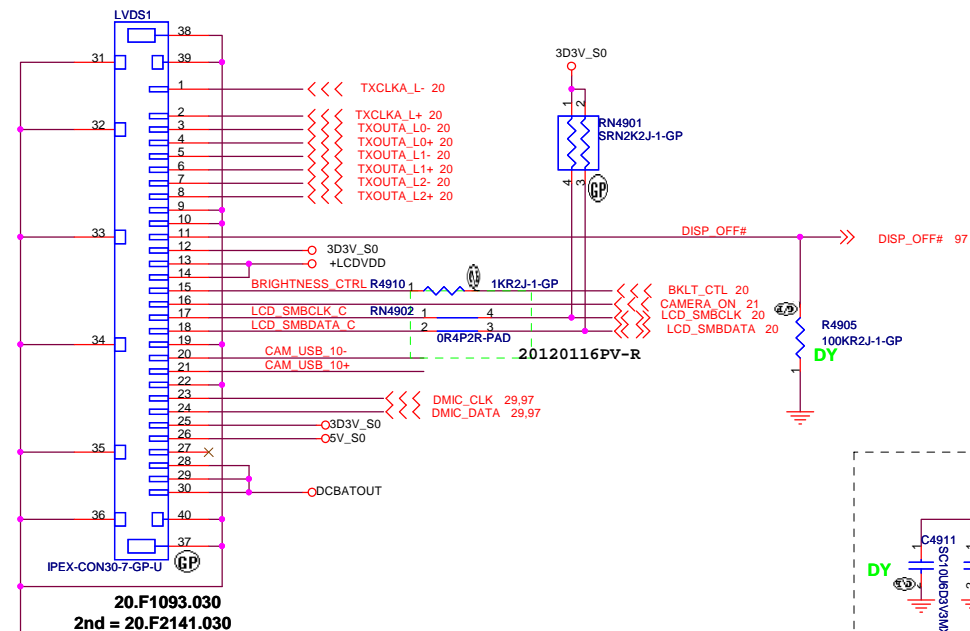
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 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
ISL95870A VCCSA		
Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1
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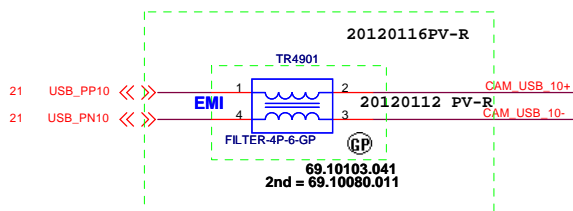
LCD Connector

CARMER PINDEFINE

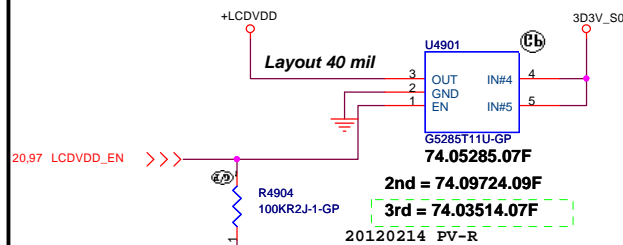
No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-



CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER

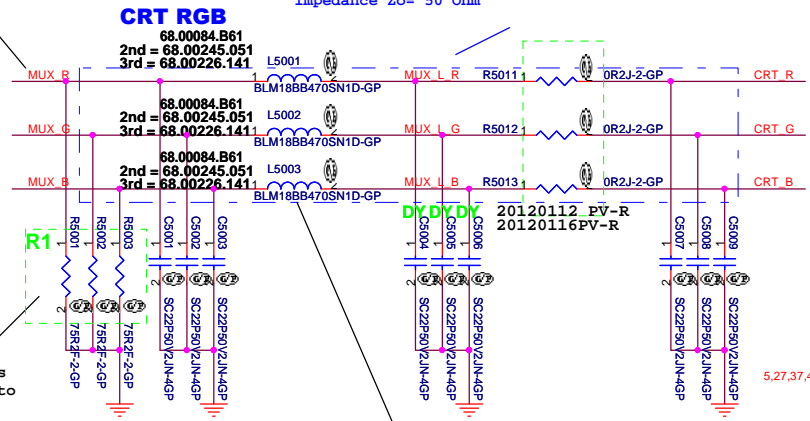
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Title		
LCD Connector		
Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1
Date:	Wednesday, March 14, 2012	Sheet 49 of 103

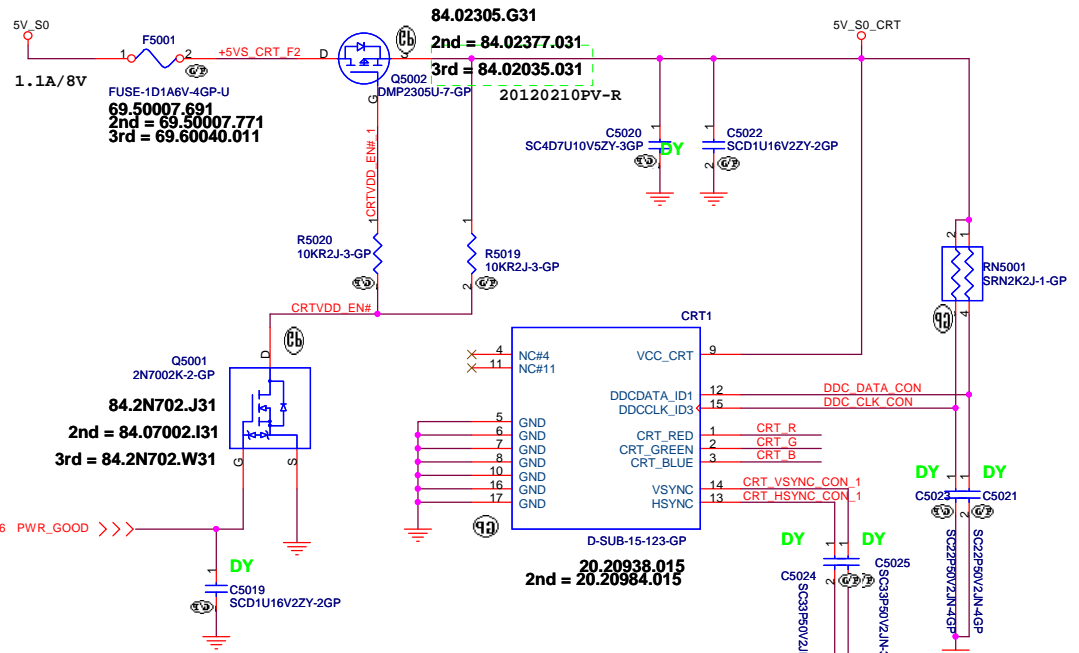
CRT Connector

CRT1
Transmission line characteristic impedance for RGB signals $Z_0 = 37.5 \text{ Ohm}$

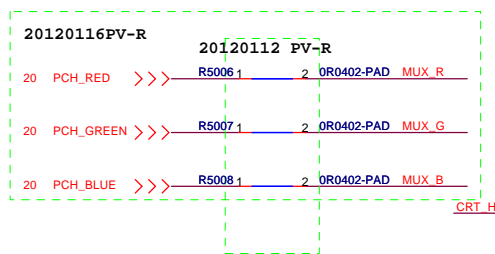
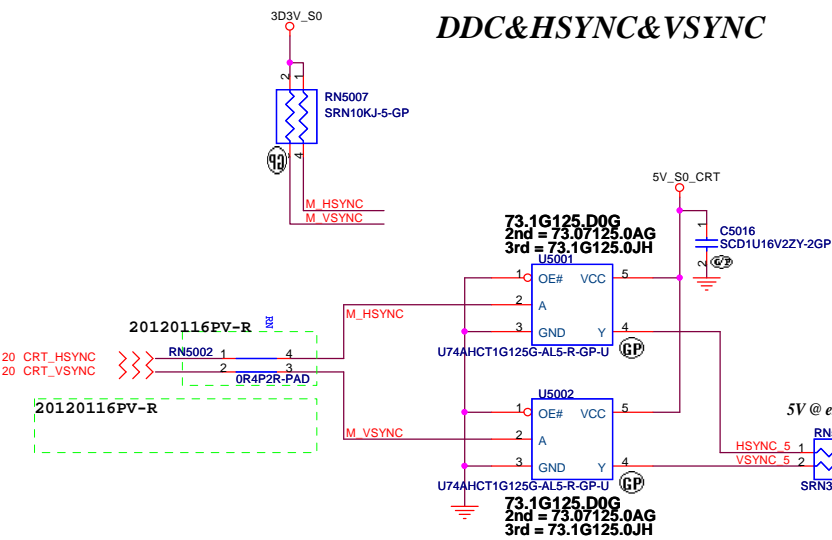


Place these resistors as the closest components to connector CRT1

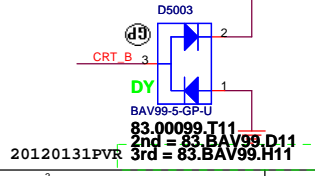
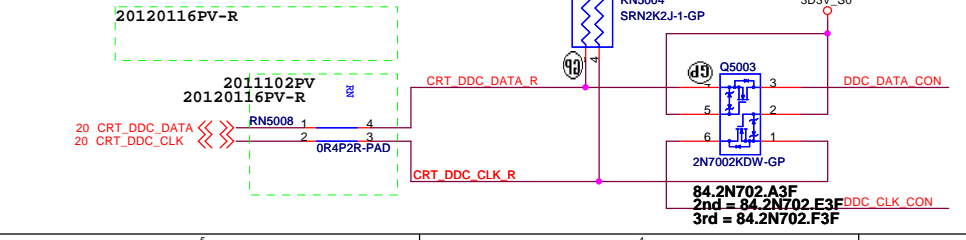
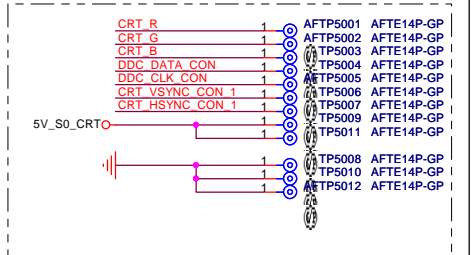
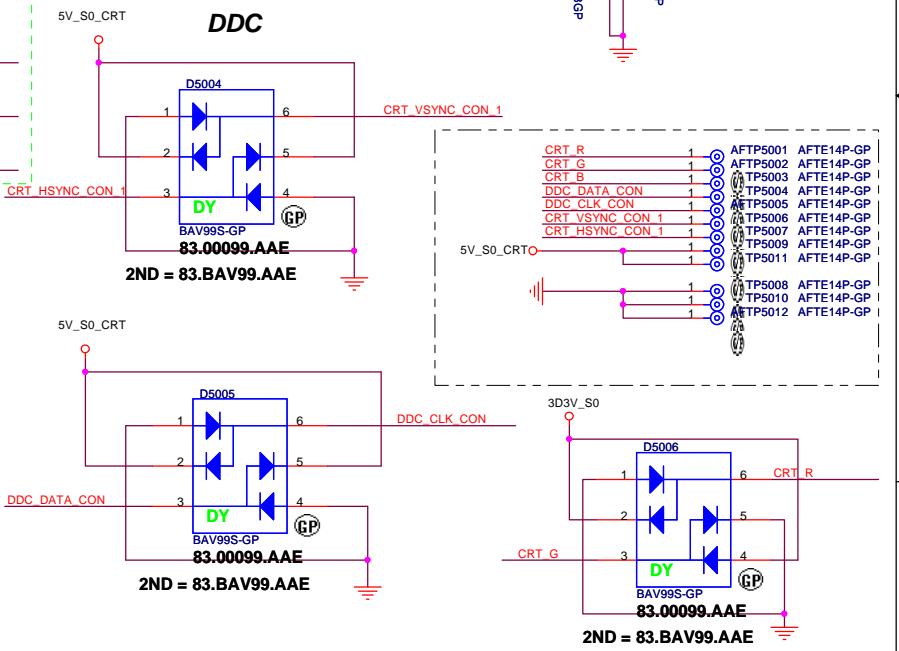
Transmission line characteristic impedance $Z_0 = 50 \text{ Ohm}$



DDC&HSYNC&VSYNC



DDC



<Core Design>

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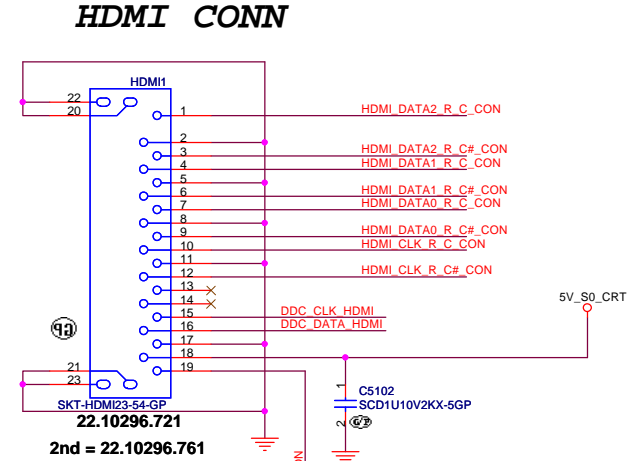
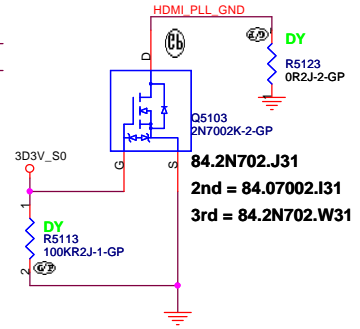
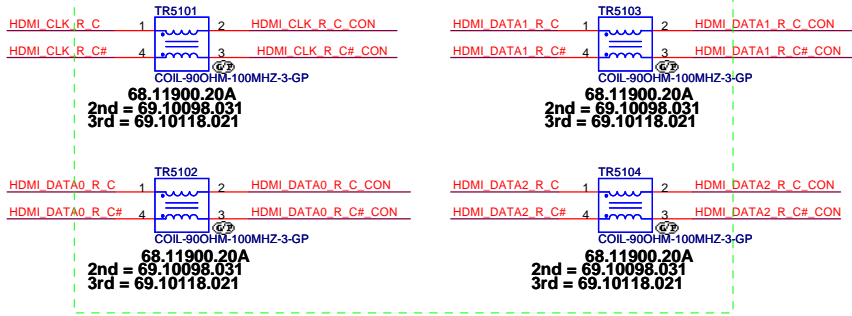
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Size A3	Document Number	Rev
		-1

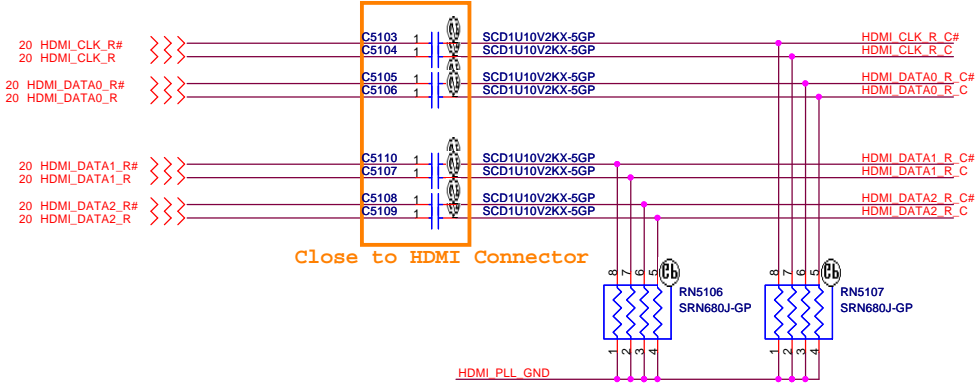
Date: Wednesday, March 14, 2012 Sheet 50 of 103

HDMI Connector

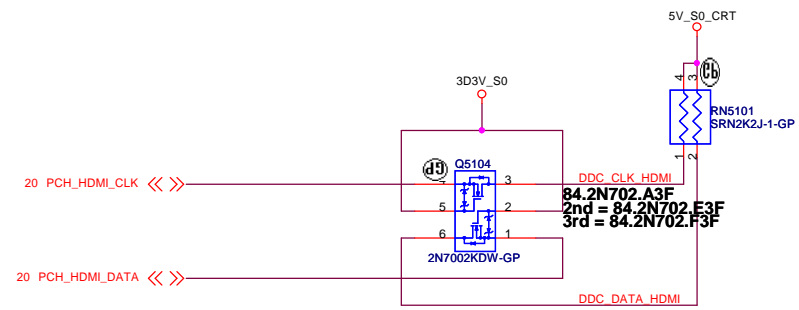
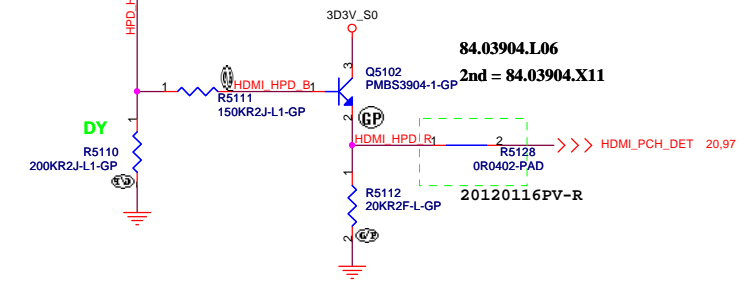
20120130PV-R



Close to PCH



Close to HDMI Connector



Routing Guidelines:

CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
 The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

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Title: **HDMI Level Shifter/Conn**
 Size A3 Document Number: **2012 S-Series Richie 13.3** Rev: **-1**
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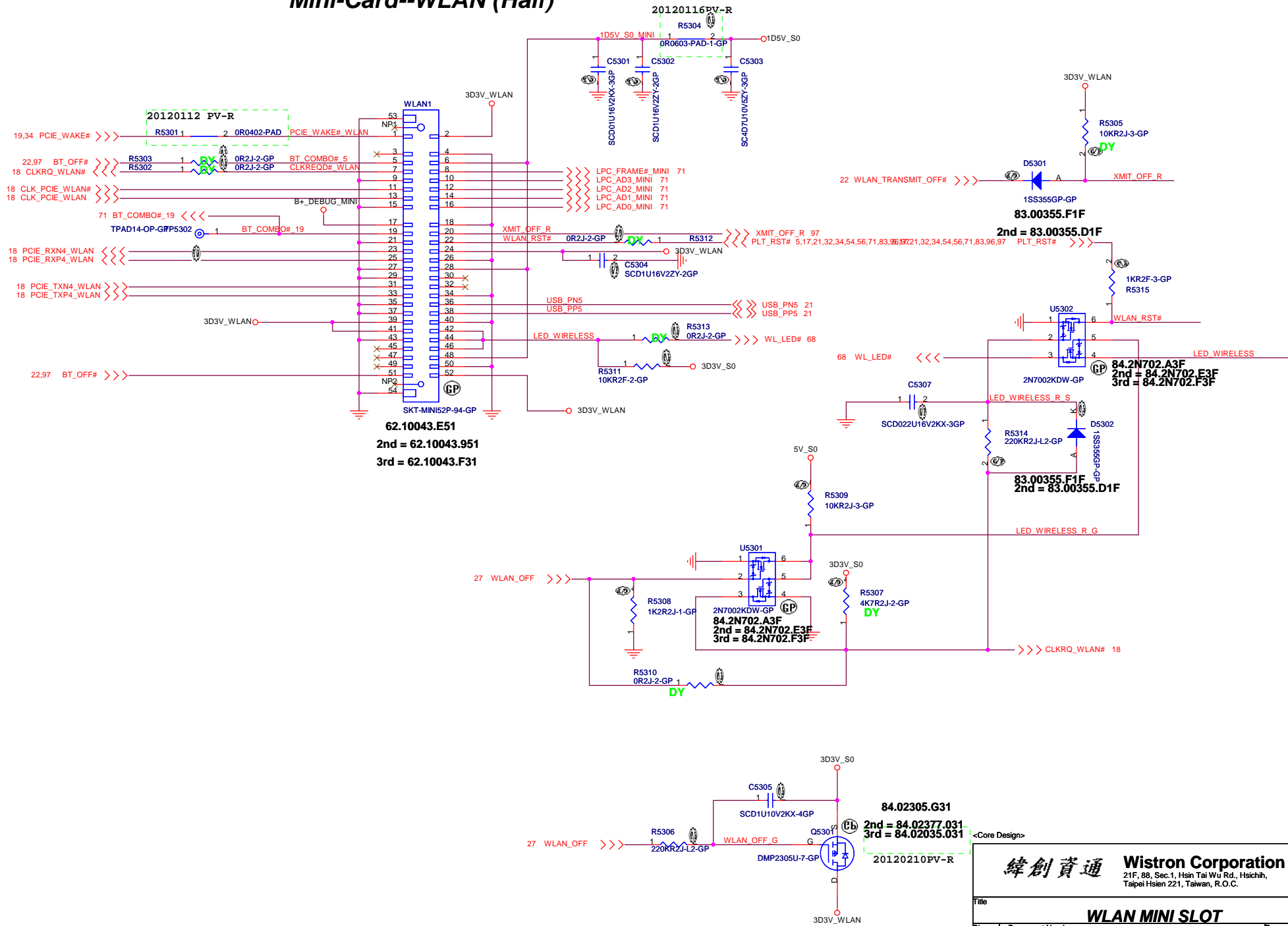
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<Core Design>

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number	Rev	
A3	2012 S-Series Richie 13.3	-1	
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WLAN Connector

Mini-Card--WLAN (Half)



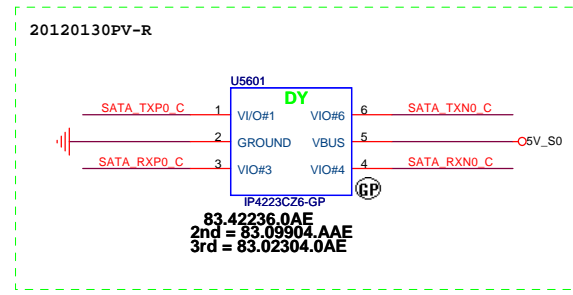
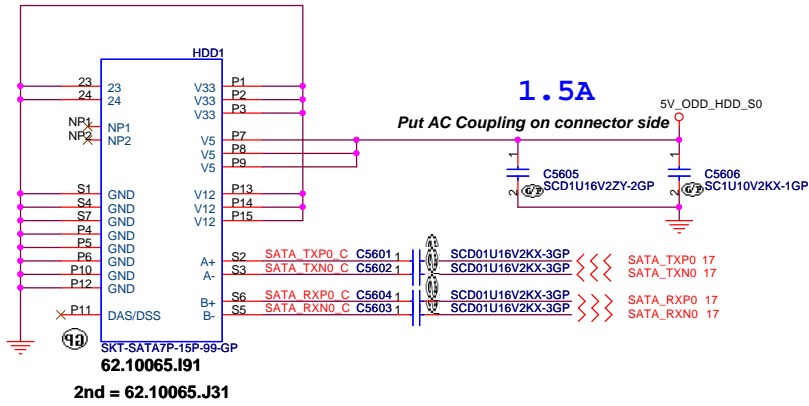
 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
WLAN MINI SLOT		
Title WLAN MINI SLOT	Document Number 2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012 Sheet 53 of 103		

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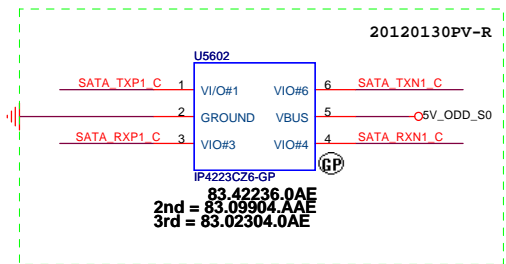
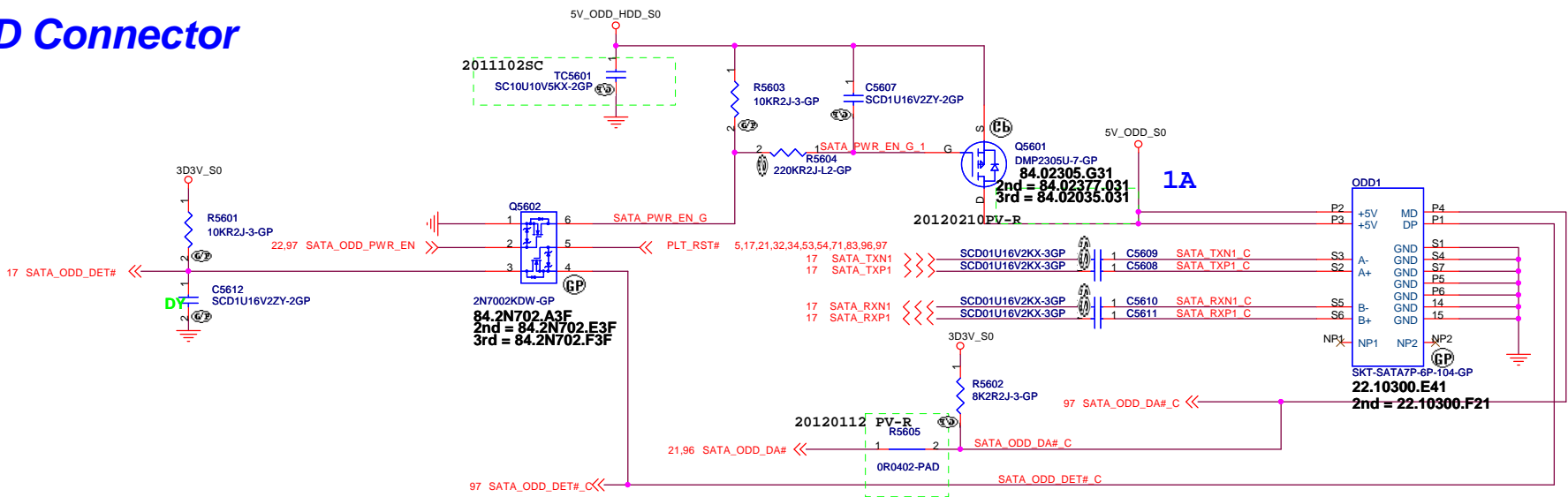
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緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012		Sheet 55 of 103

HDD Connector



ODD Connector



(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
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Date: Wednesday, March 14, 2012 Sheet 57 of 103

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
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Date: Wednesday, March 14, 2012 Sheet 58 of 103

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number

2012 S-Series Richie 13.3

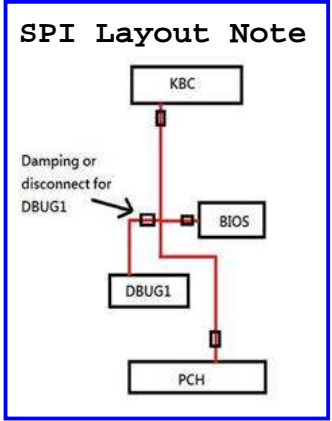
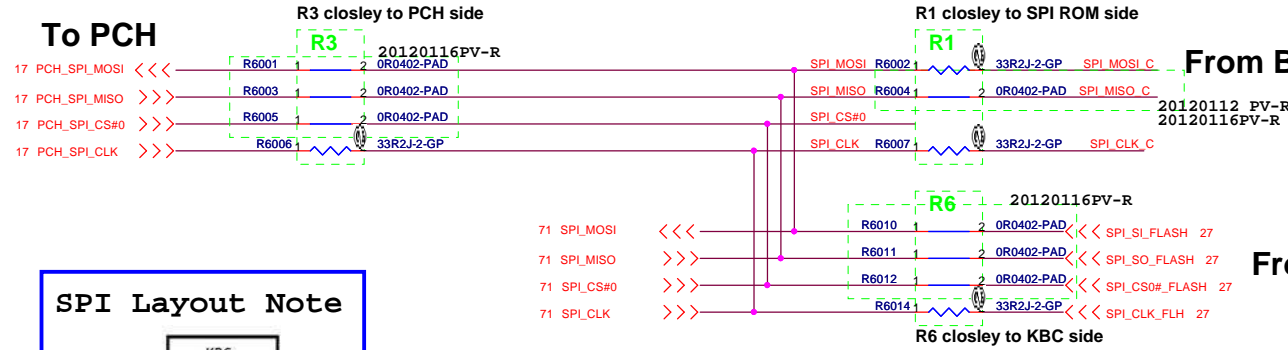
Rev

-1

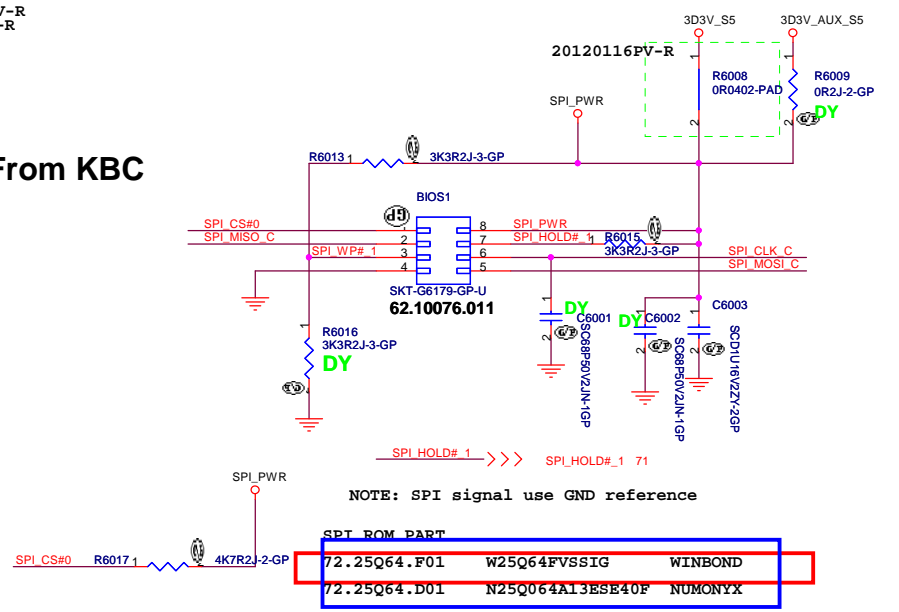
Date: Wednesday, March 14, 2012

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SSID = Flash.ROM

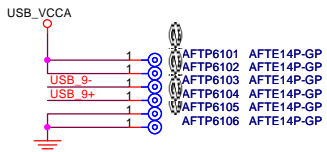
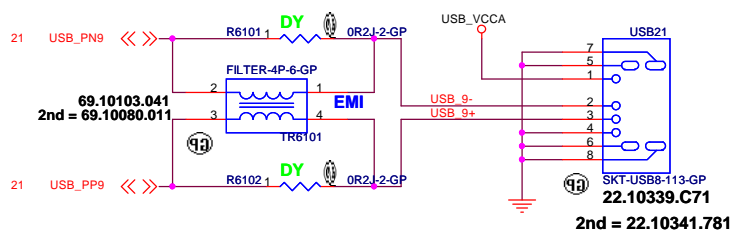


SYSTEM SPI ROM Socket

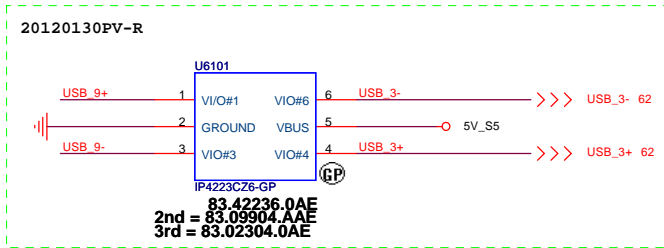
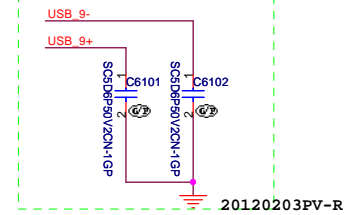


Right Side USB 2.0 Connector

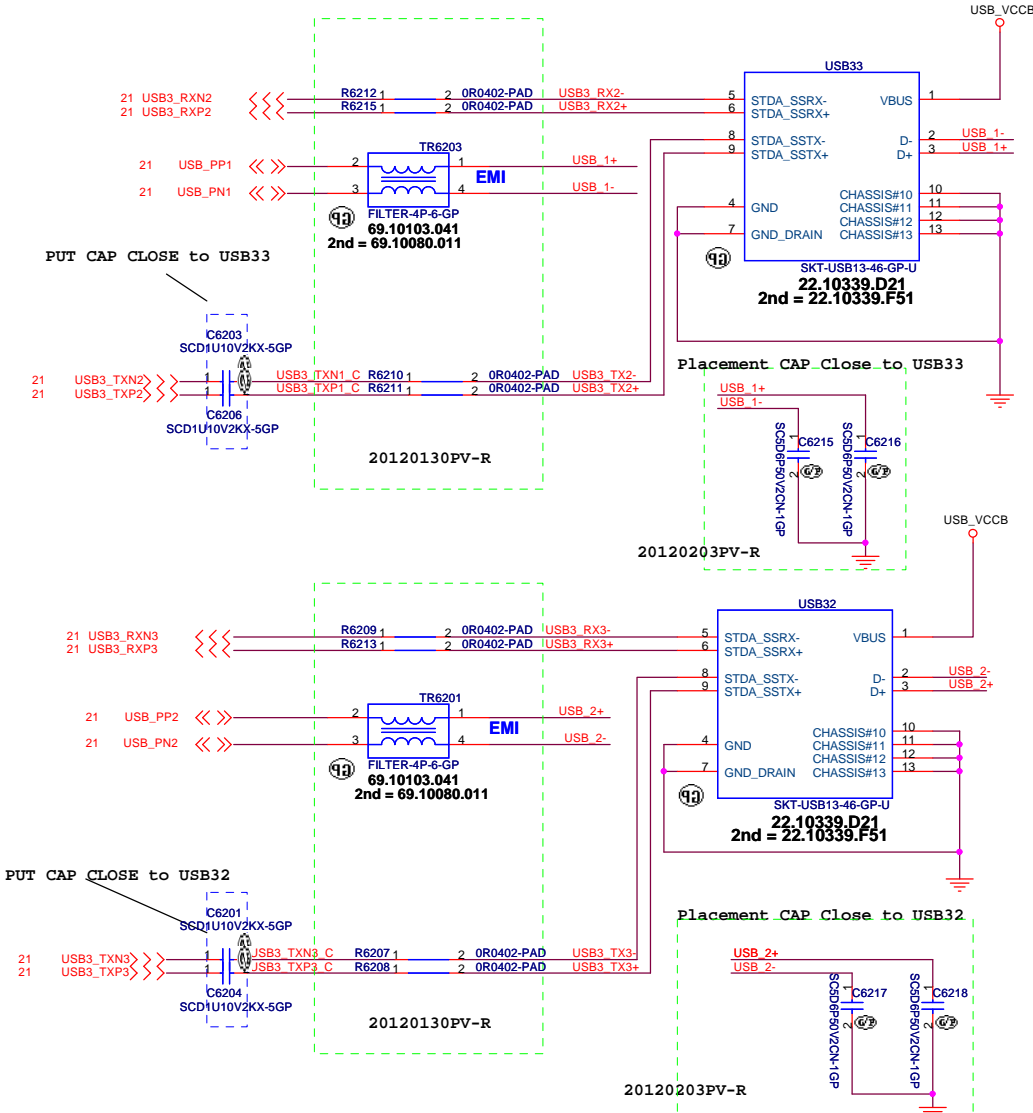
Right Side USB 2.0



For RF Placement CAP Close to USB21



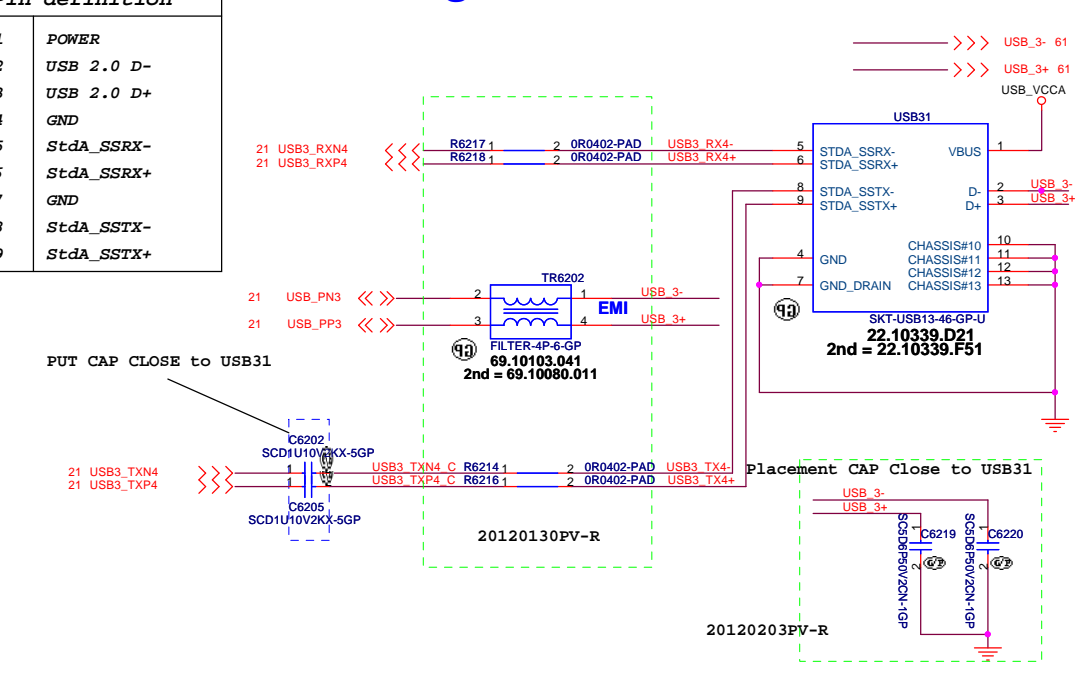
Left Side USB 3.0 Connector



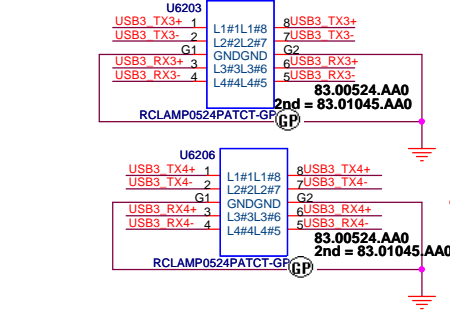
USB 3.0 Connector Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	Stda_SSRX-
6	Stda_SSRX+
7	GND
8	Stda_SSTX-
9	Stda_SSTX+

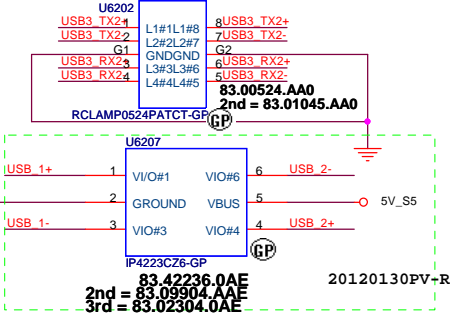
Right Side USB 3.0 Connector



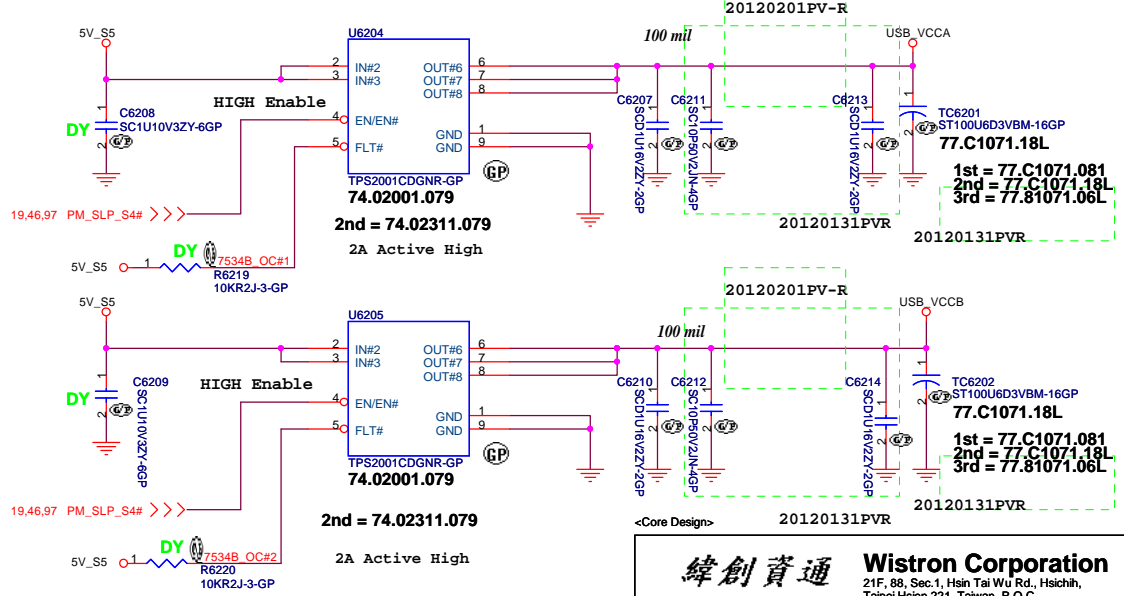
Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



USB POWER



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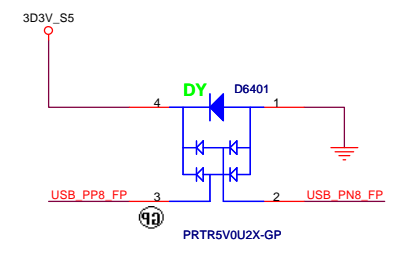
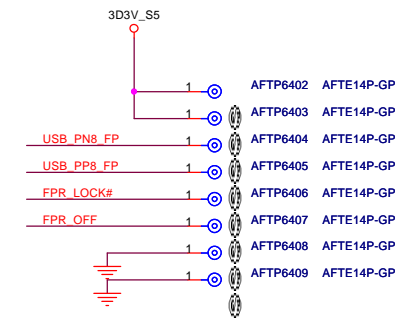
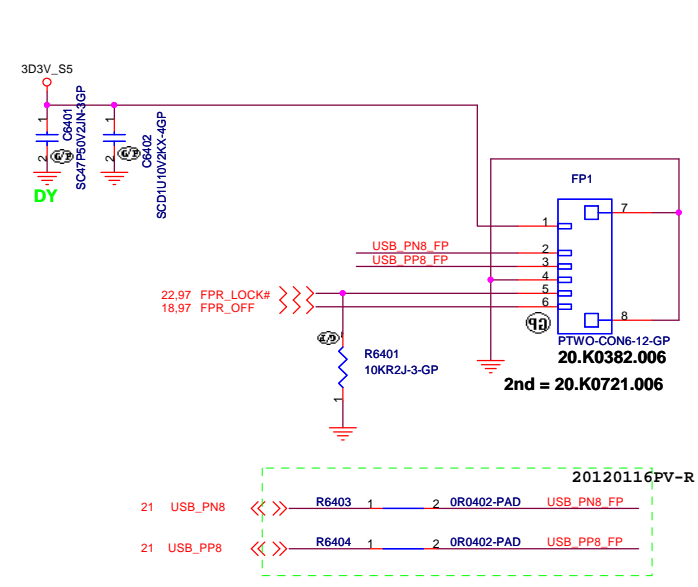
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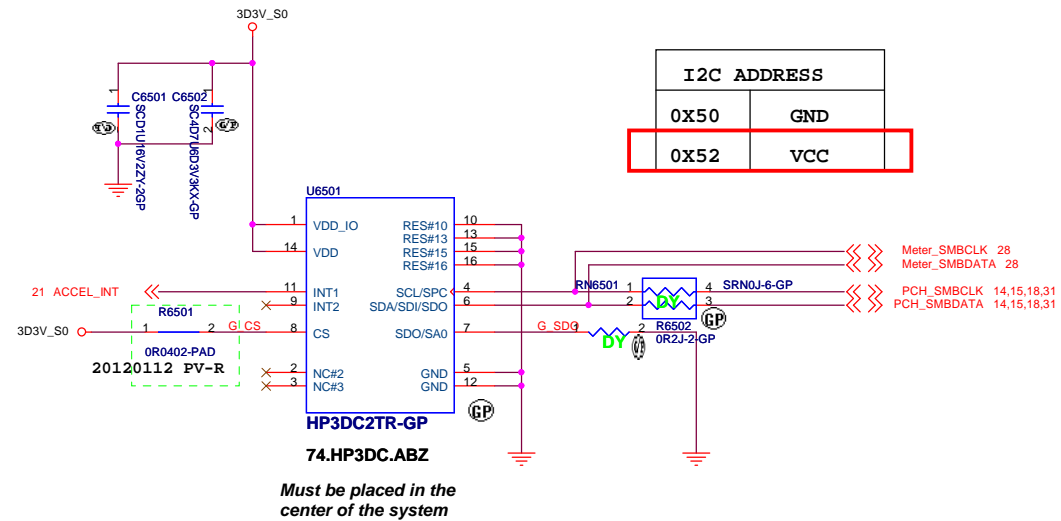
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Finger Printer Connector



ACCELEROMETER



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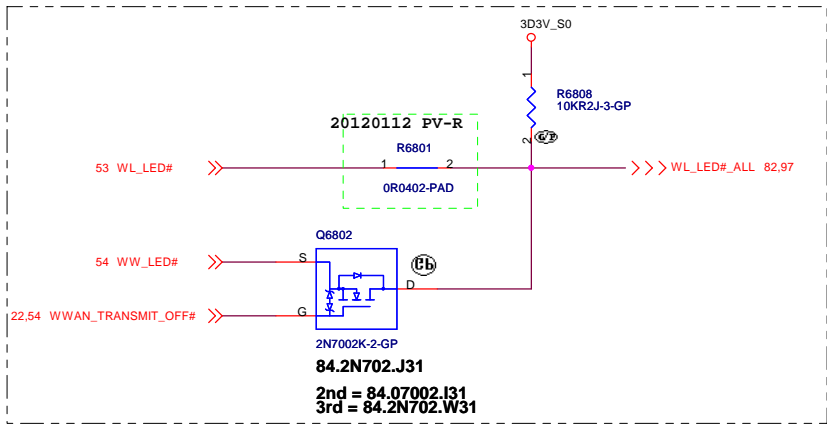
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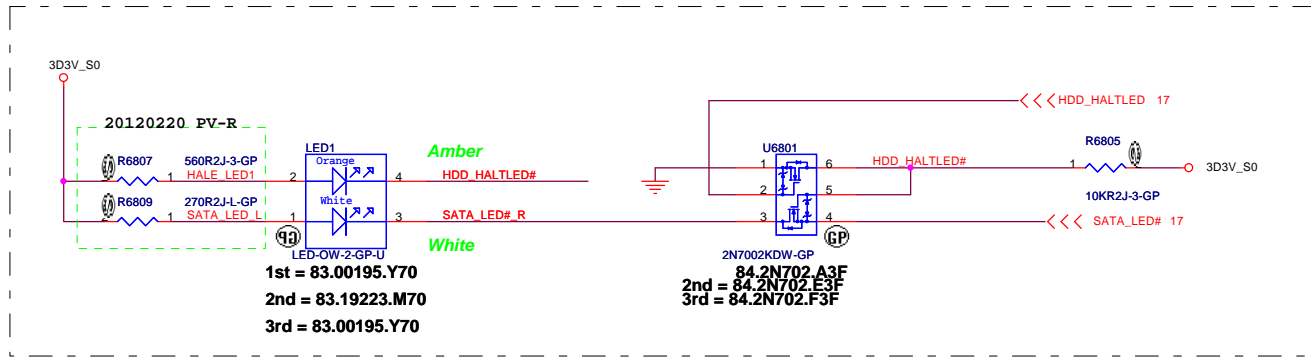
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Reserved		
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WLAN / WWAN POWER LED



HDD LED

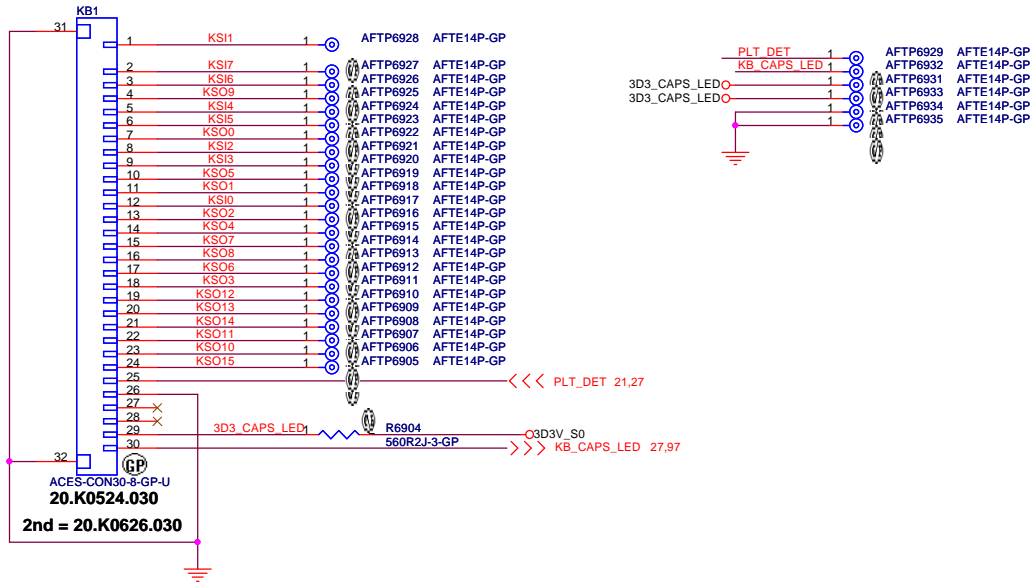


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LED Control			
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Keyboard Connector

<<< KS[0..7] 27.82,97
>>> KSO[0..15] 27.97



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Title		
Key Board/Touch Pad		
Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1
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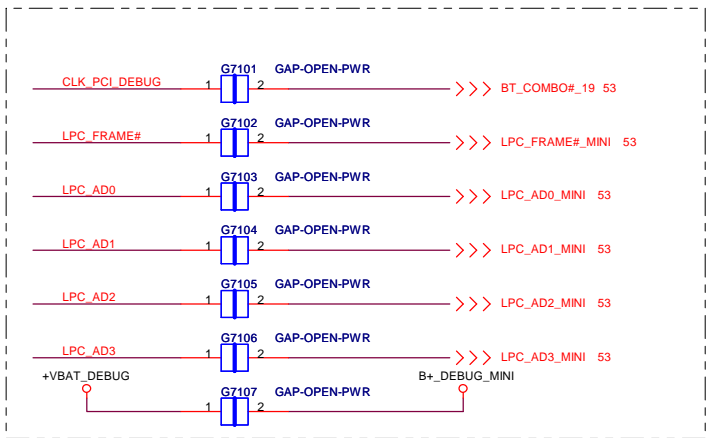
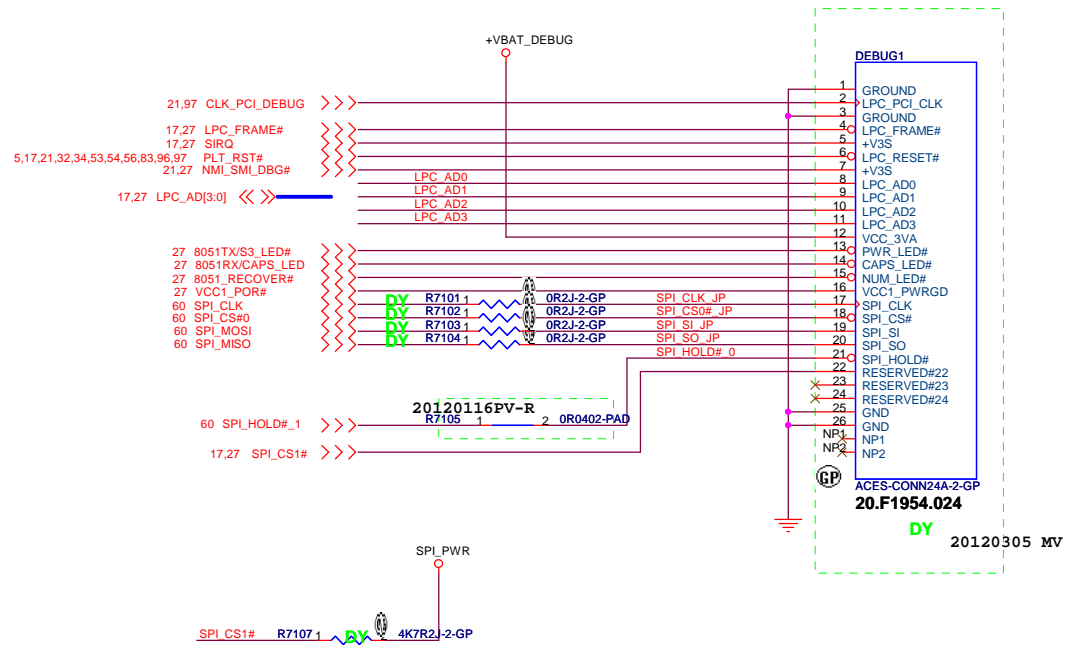
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24 PIN LPC DEBUG CONN.



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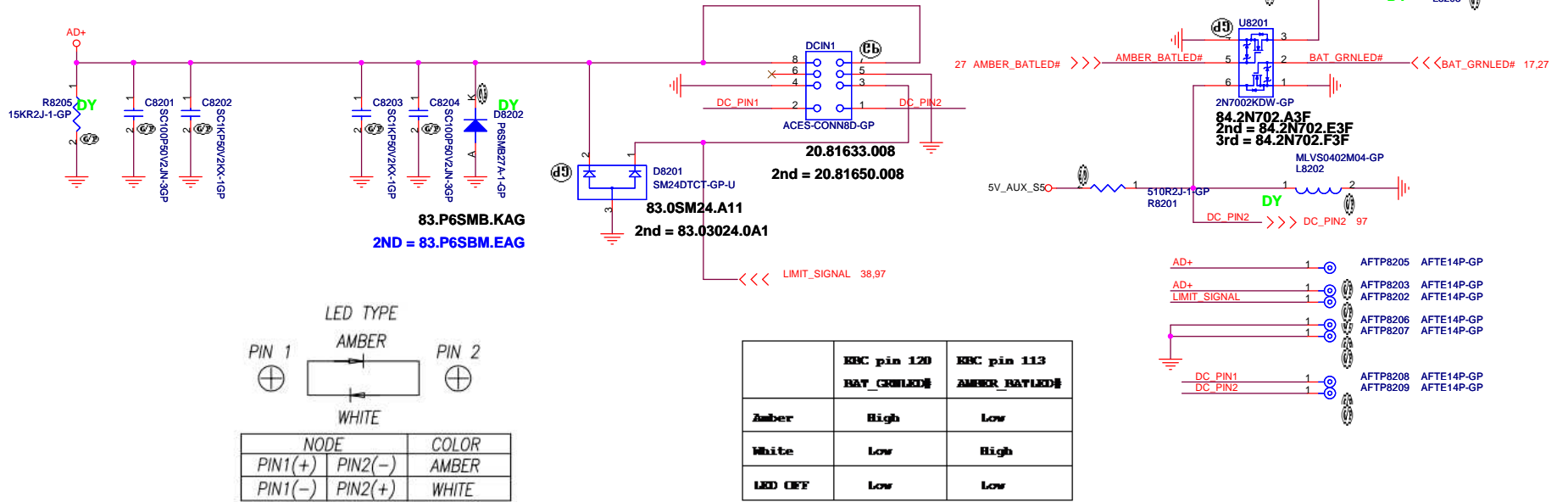
Rev

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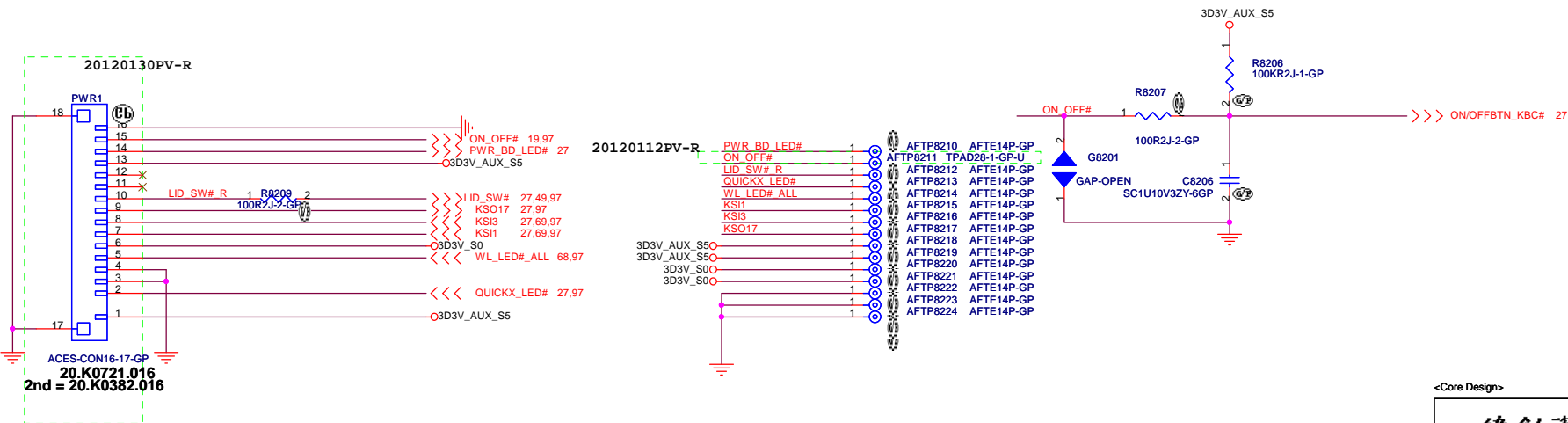
Date: Wednesday, March 14, 2012

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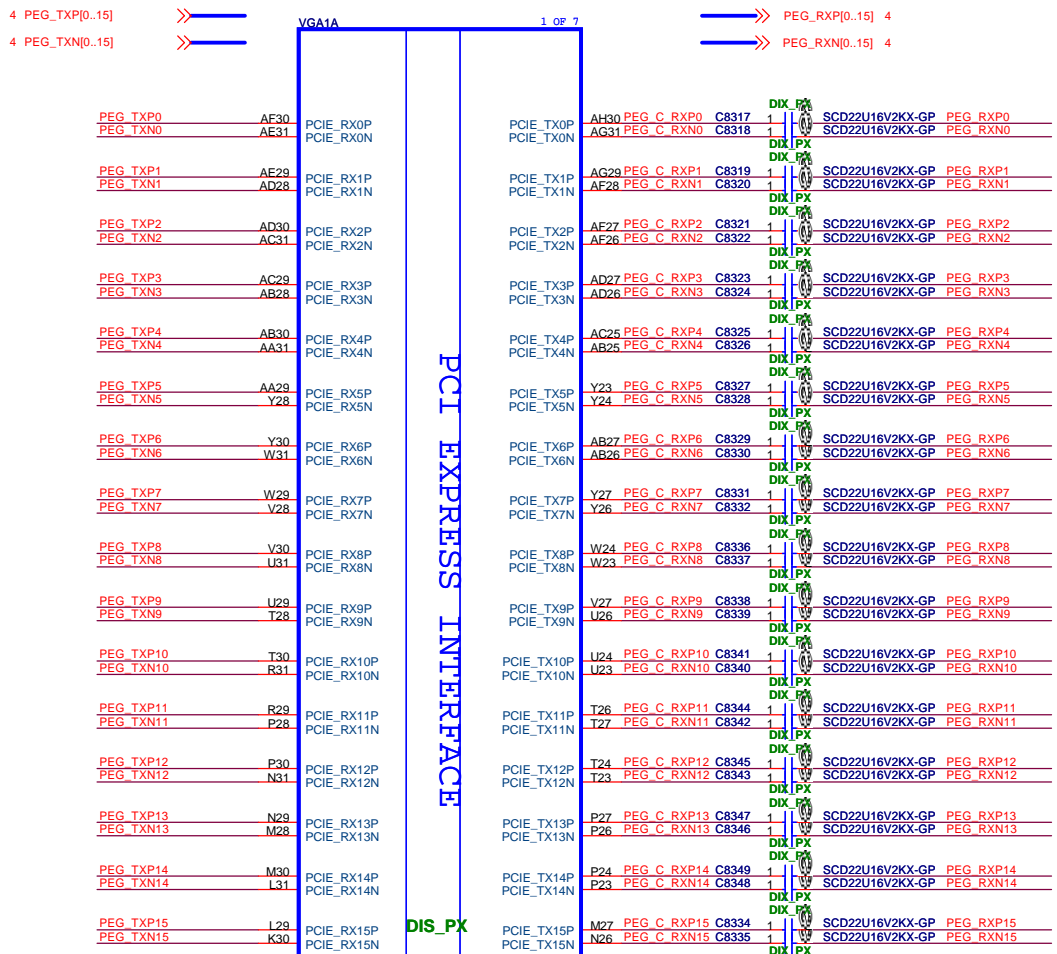
Adaptor in to generate DCBATOUT



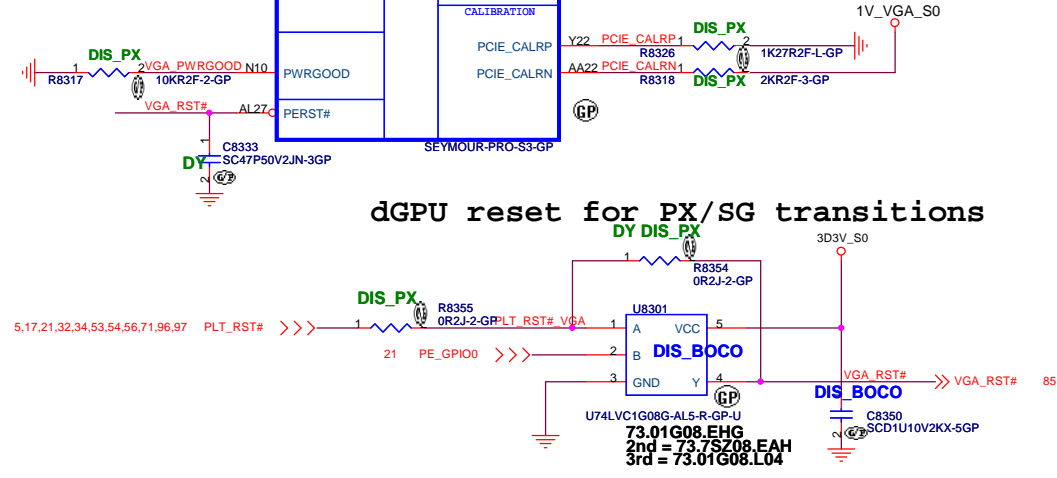
Power Button + Quick Lanch board



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dGPU reset for PX/SG transitions

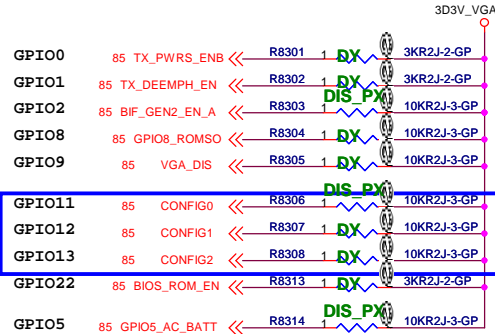


CONFIGURATION STRAPS

ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

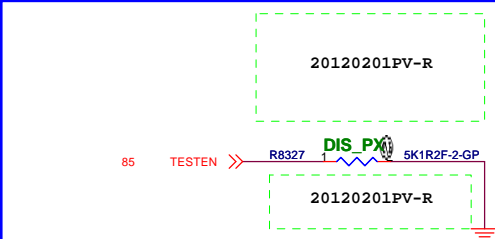
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERIC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSNC		X	1



GPIO_13	GPIO_12	GPIO_11	Memory Aperture Size
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1" (PU)	"1" (PU)	"0" (PD)
JTAG_TRST#	"0" (PD)	"1" (PU)	NC
JTAG_TCK	CLK	"1" (PU)	NC
JTAG_TMS	"1" (PU)	"1" (PU)	NC



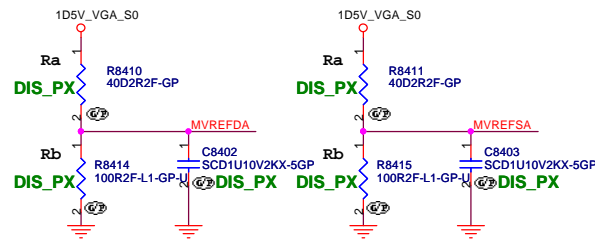
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Title: **GPU PCIE/STRAPPING(1/5)**

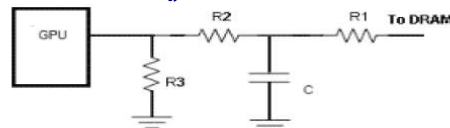
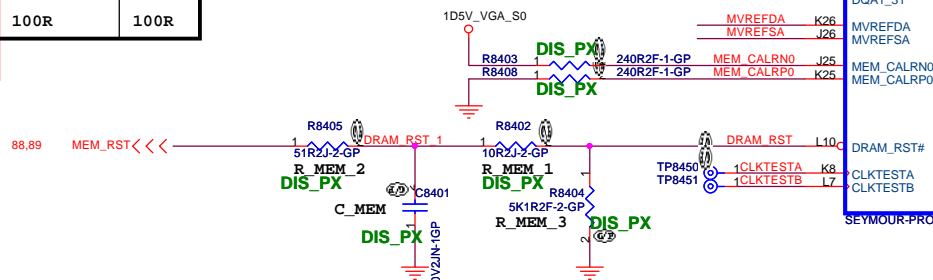
Size A3 Document Number **2012 S-Series Richie 13.3** Rev -1

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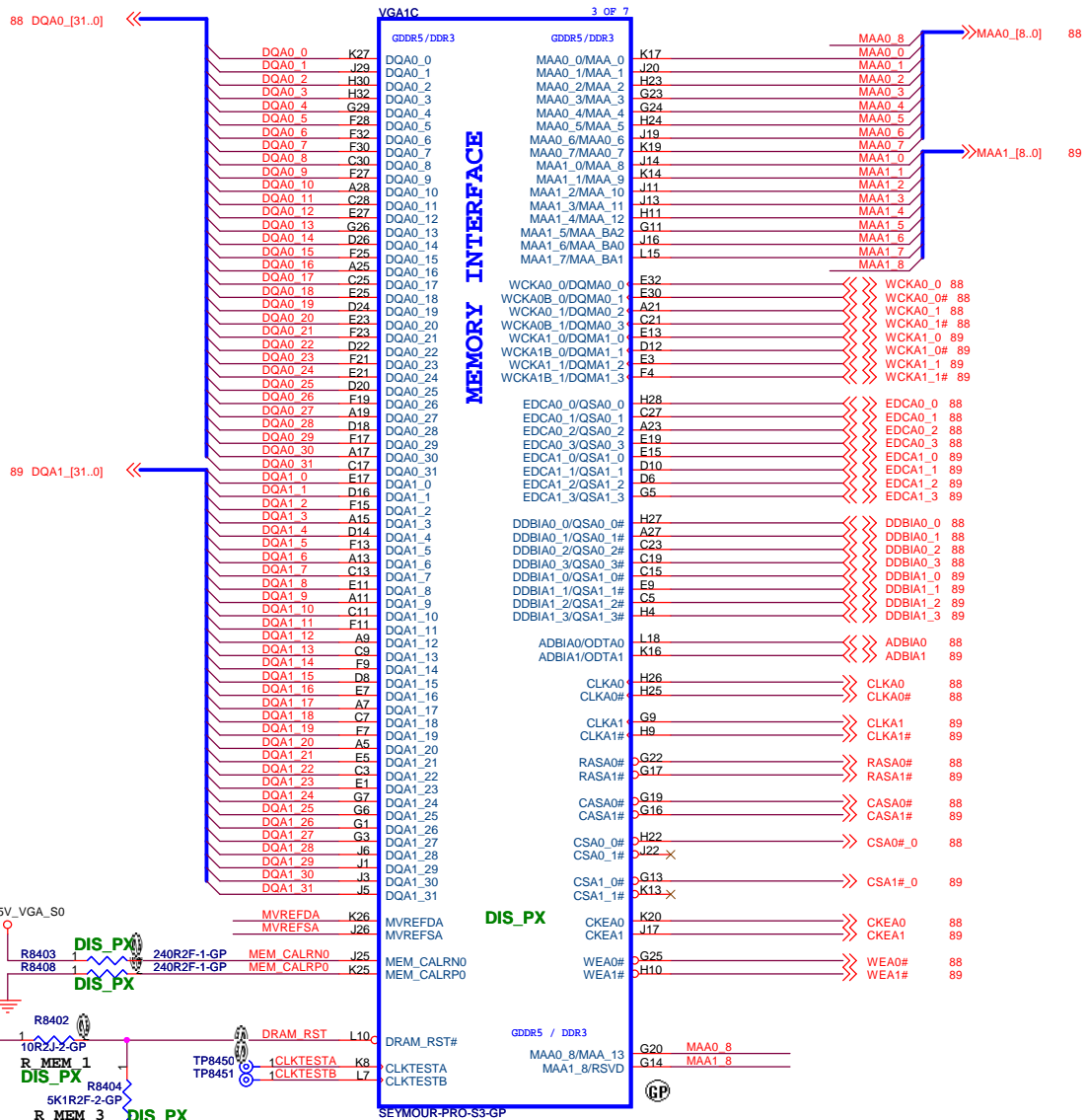


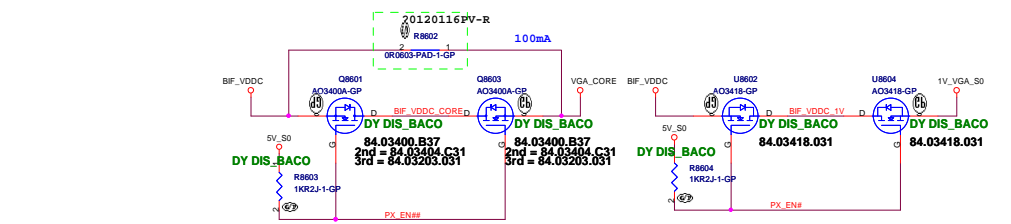
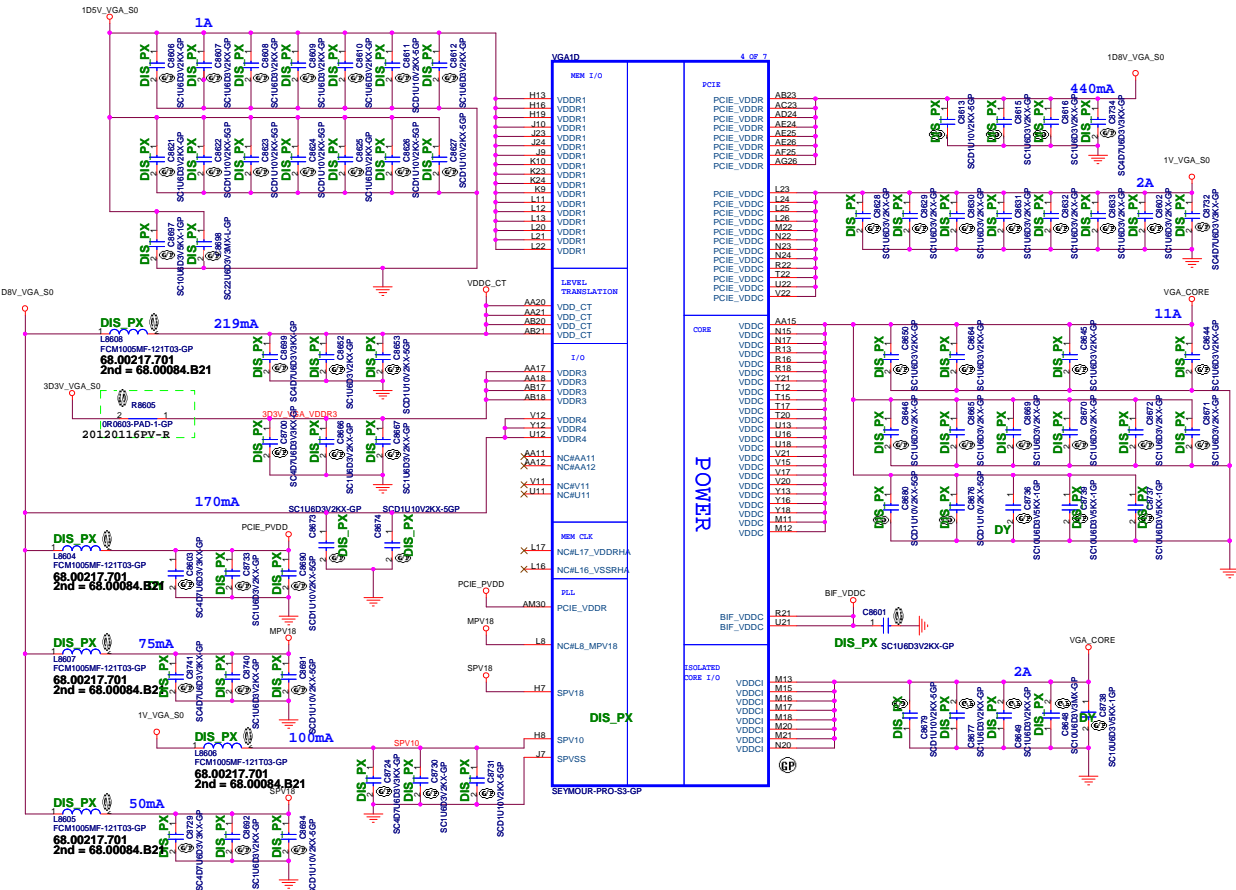
GDDR3/GDDR5 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

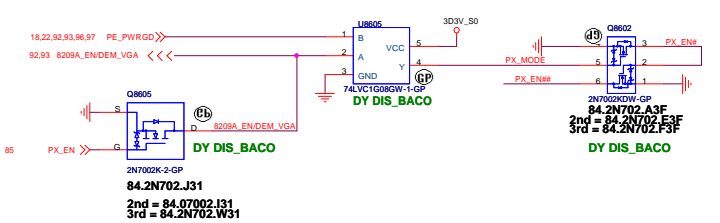


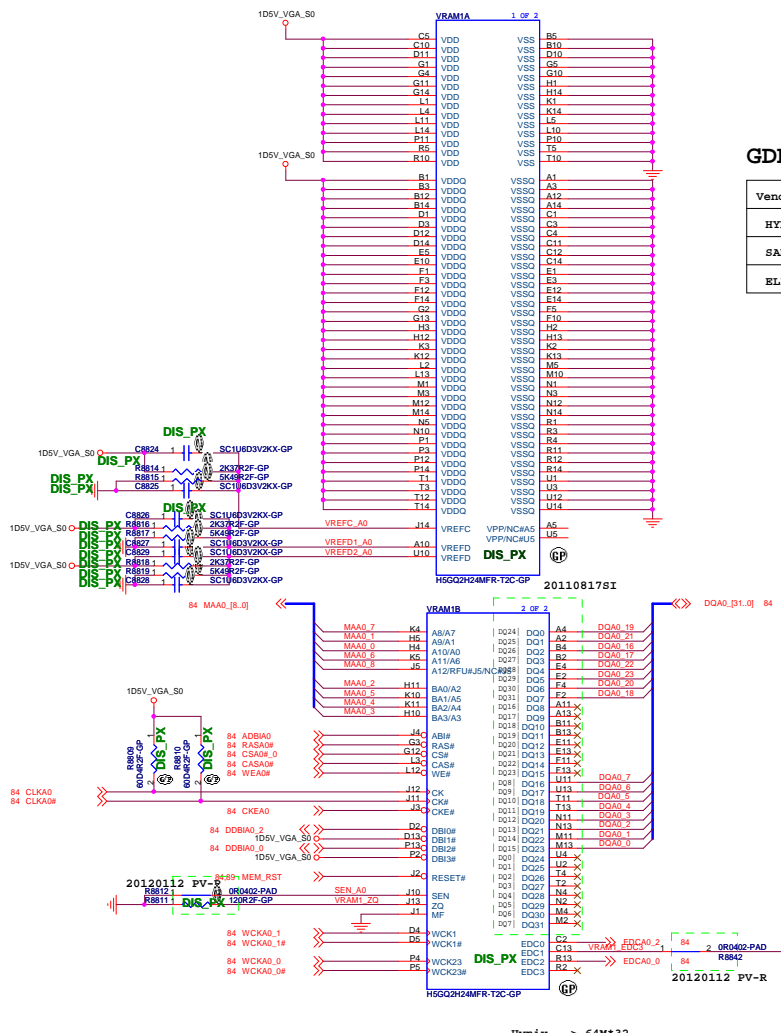


	PX_EN	S209A_EN/DEM_VGA	PX_MODE	PX_EN#	PX_EN#	BIF_VDDC
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
 PX_EN## = High, BIF_VDDC = VGA_CORE

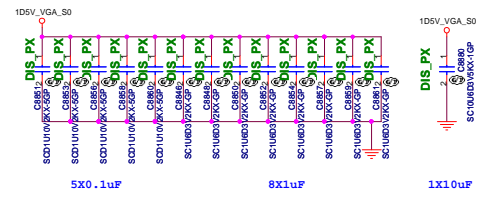
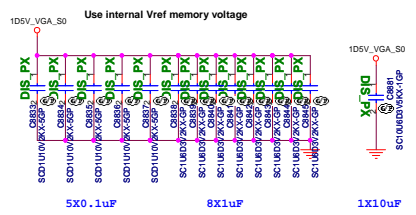
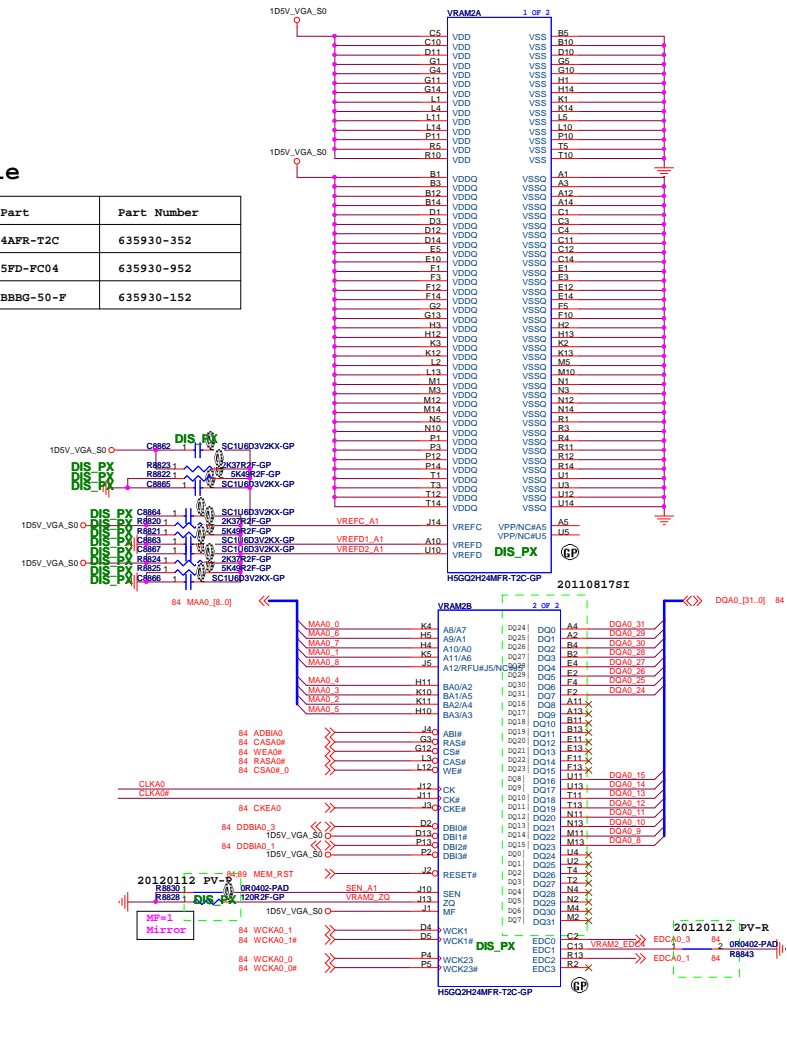
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

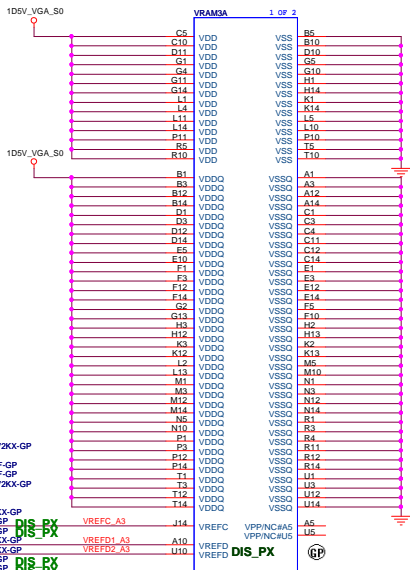




GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24AFR-T2C	635930-352
SAMSUNG	K4G20325FD-PC04	635930-952
ELPIDA	EDW1032BBG-50-F	635930-152

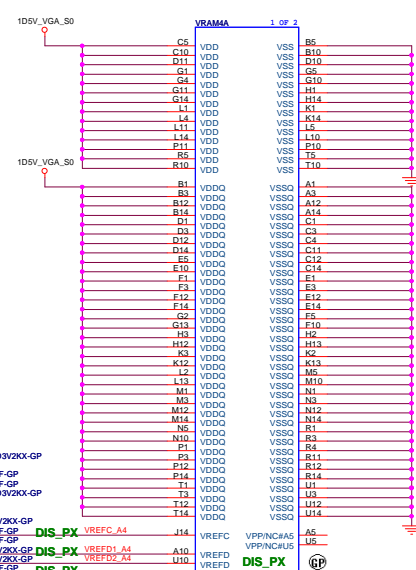




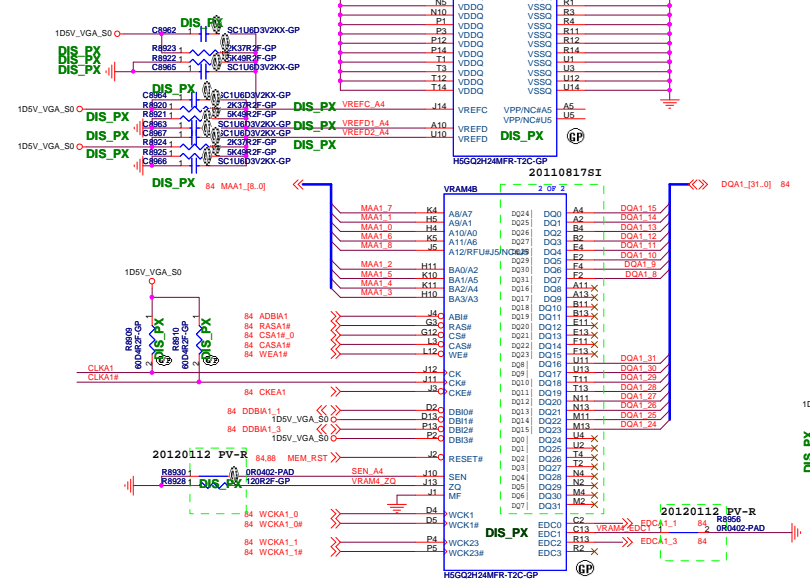
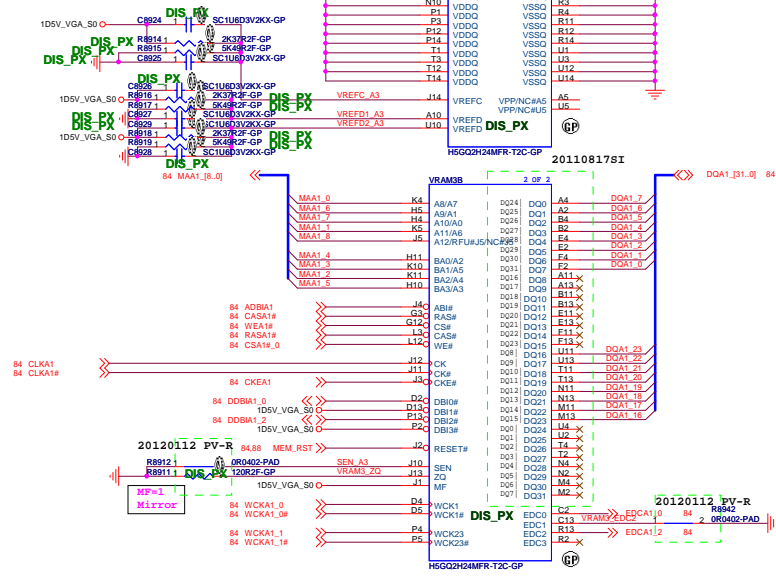
20100903 X01: Change VRAM1,VRAM2 to GDDR5.
 20100908 X01: Modify VRAM set name for Mirror Function.

GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24MFR-T2C	72.05224.00U
SAMSUNG	K4G20325FC-HC04	72.20325.00U



20100903 X01: Change VRAM1,VRAM2 to GDDR5.
 20100908 X01: Modify VRAM set name for Mirror Function.



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Title					
(Reserved) GPU-VRAM5,6 (3/4)					
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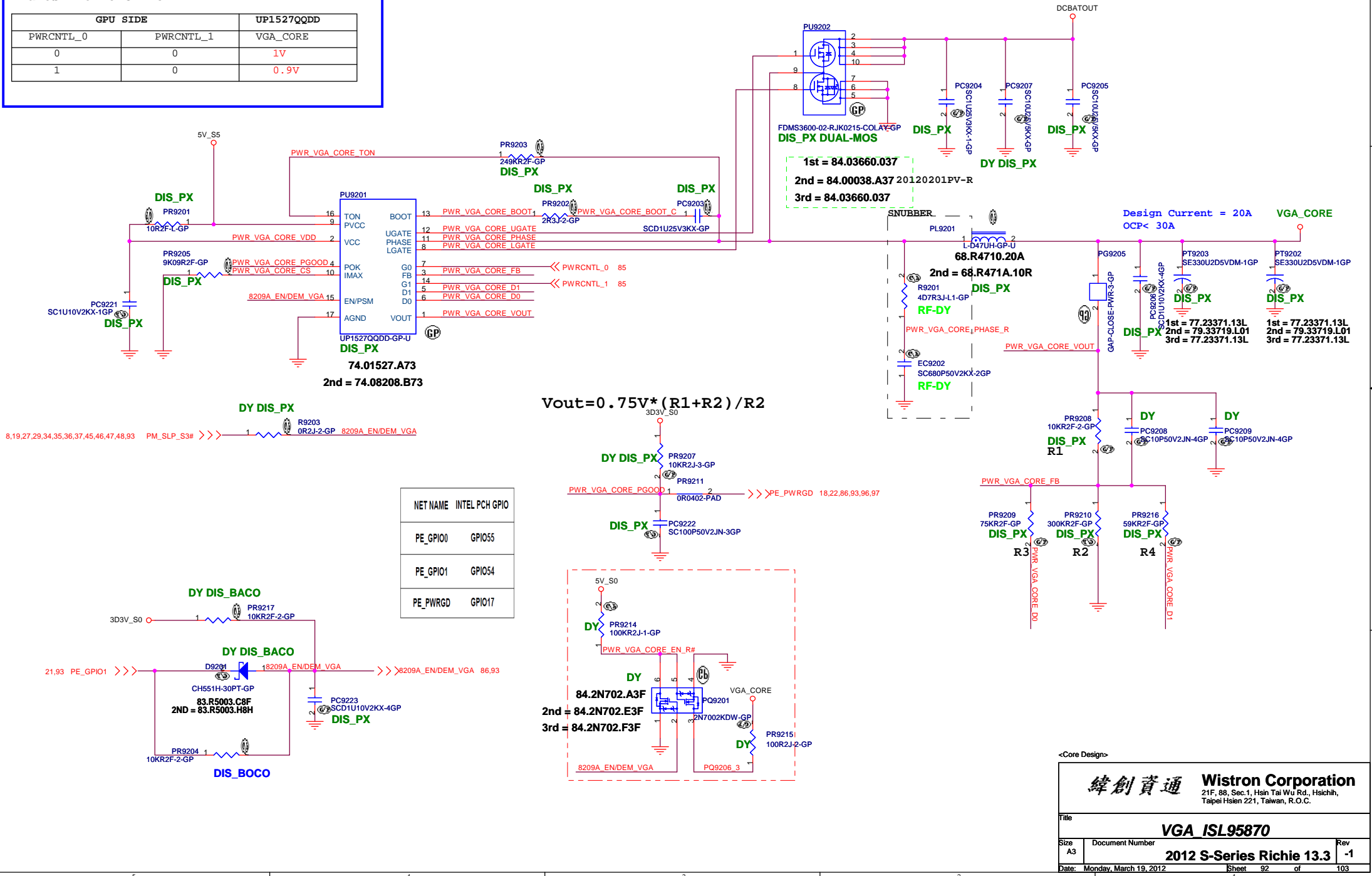
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Title					
(Reserved) GPU-VRAM7,8 (4/4)					
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+VGA_CORE

GPU Power ID Table

Thames Pro S3 GDDR5

GPU SIDE		UP1527QDD
PWRCNTL_0	PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V



$$V_{out} = 0.75V * (R1 + R2) / R2$$

NET NAME	INTEL PCH GPIO
PE_GPIO0	GPIO55
PE_GPIO1	GPIO54
PE_PWRGD	GPIO17

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Title: **VGA ISL95870**

Size: A3 Document Number: **2012 S-Series Richie 13.3** Rev: -1

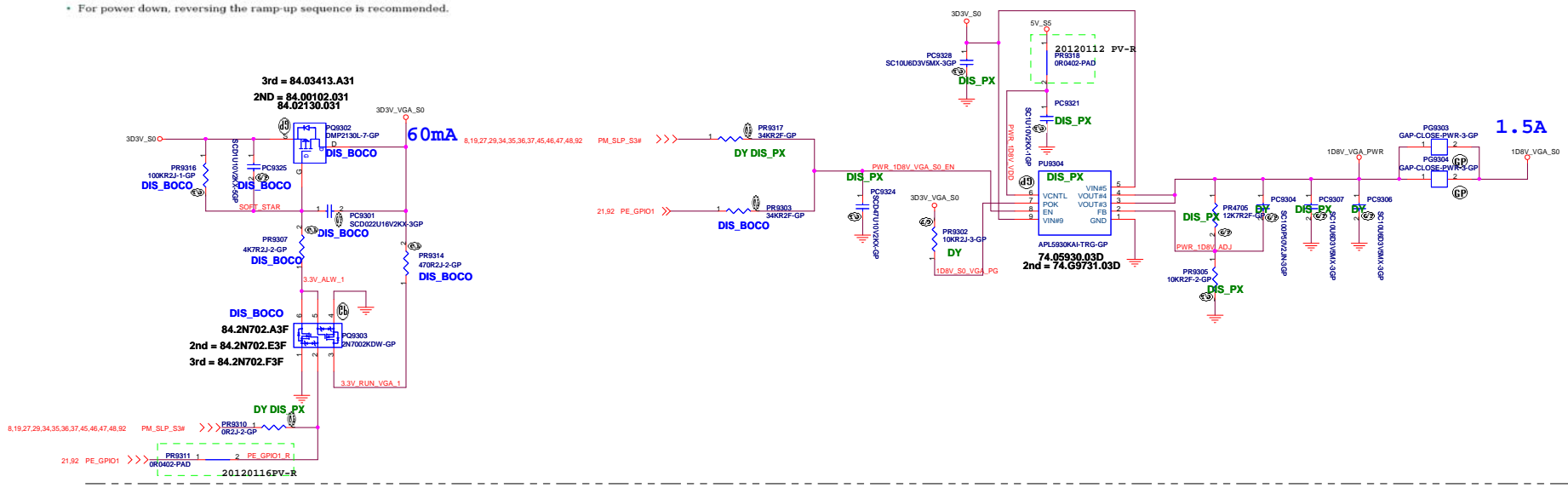
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5.3 Power-Up/Down Sequence

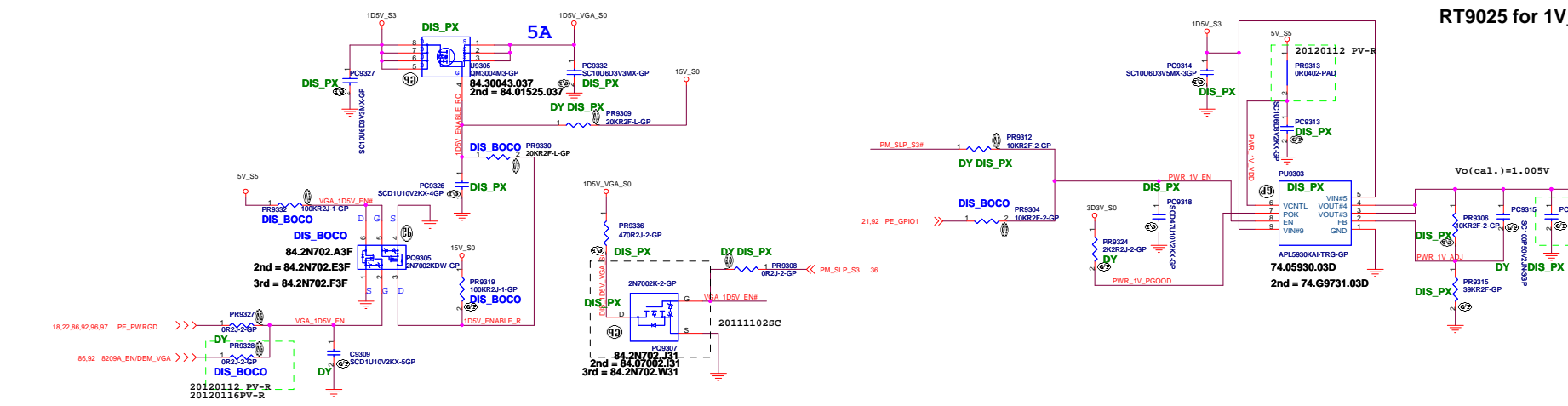
Seymour has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0



1D5V_VGA_S0



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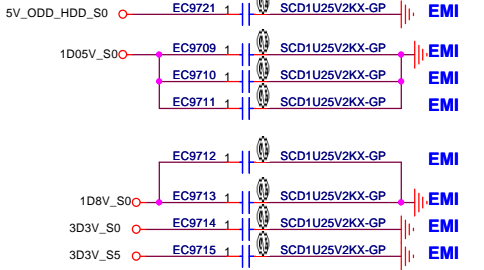
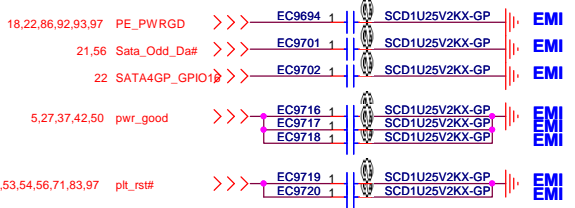
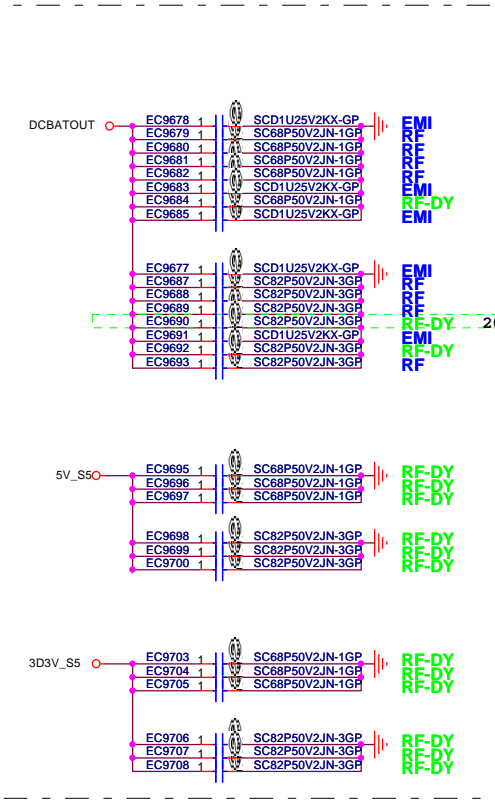
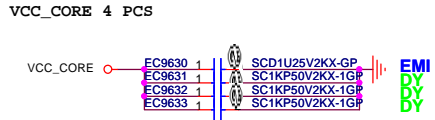
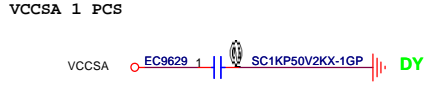
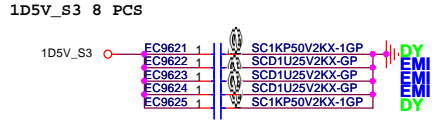
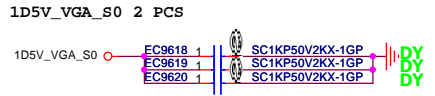
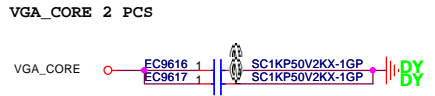
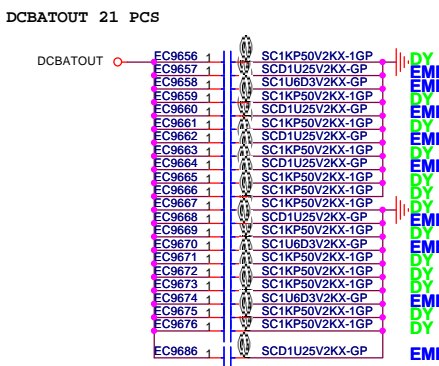
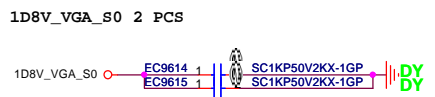
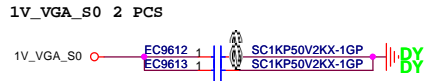
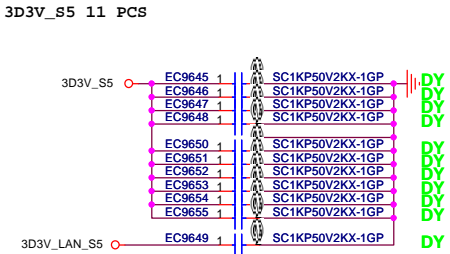
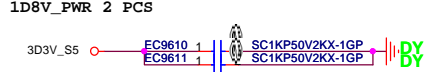
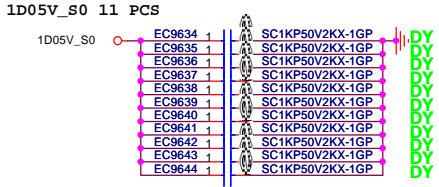
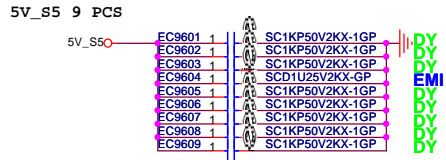
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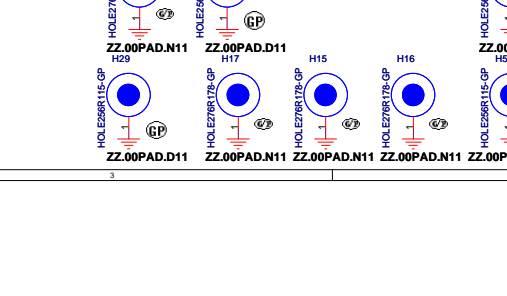
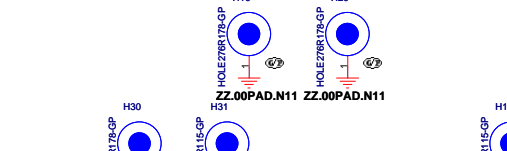
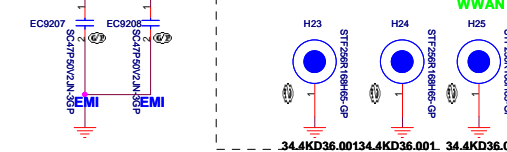
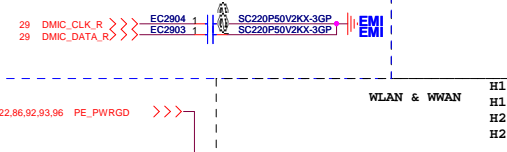
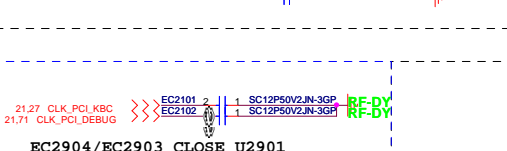
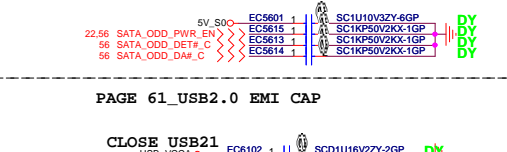
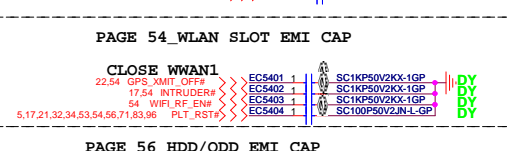
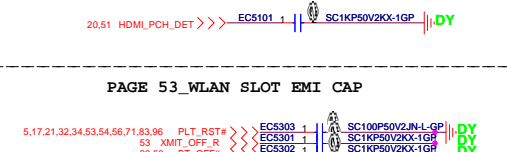
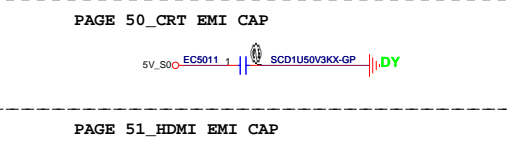
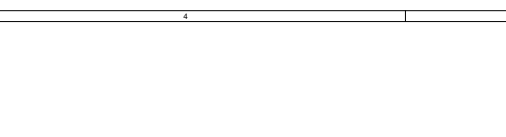
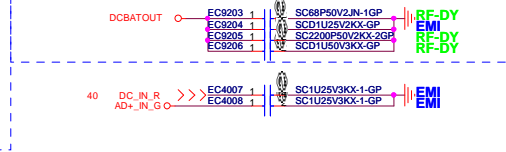
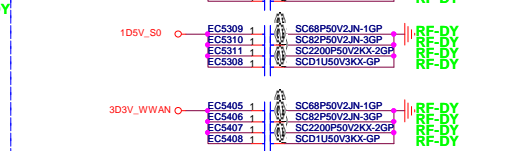
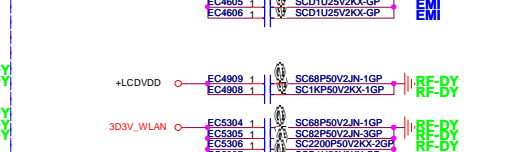
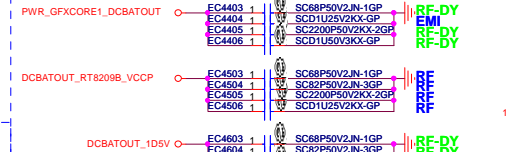
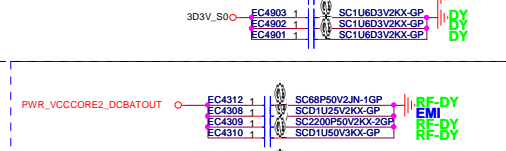
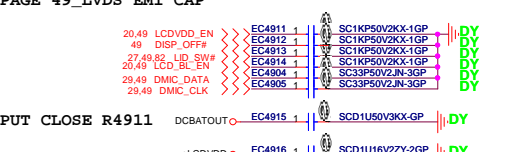
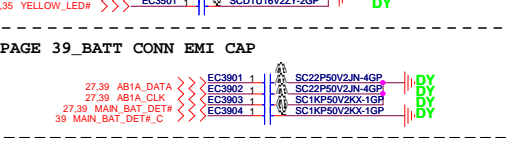
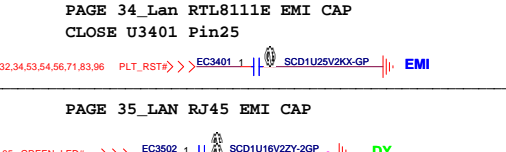
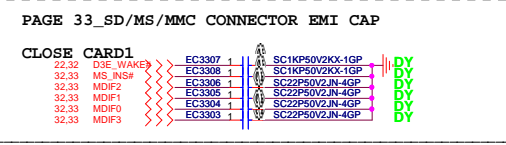
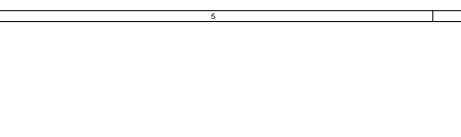
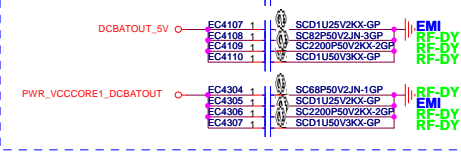
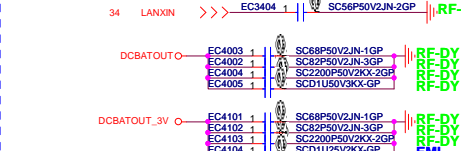
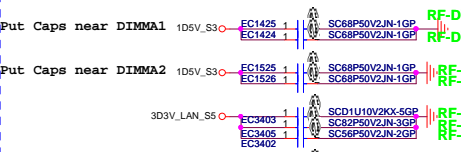
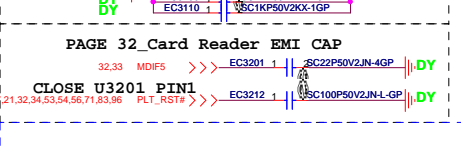
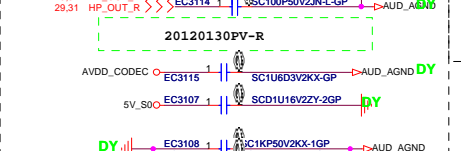
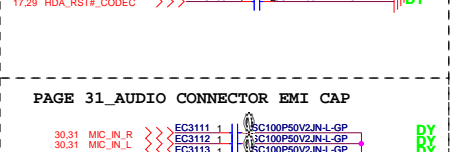
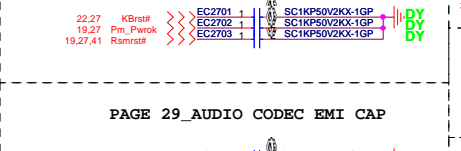
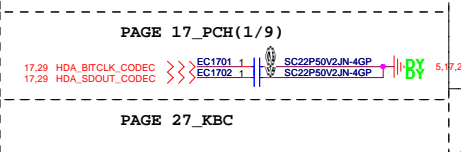
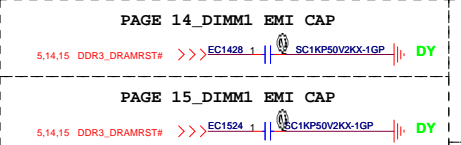
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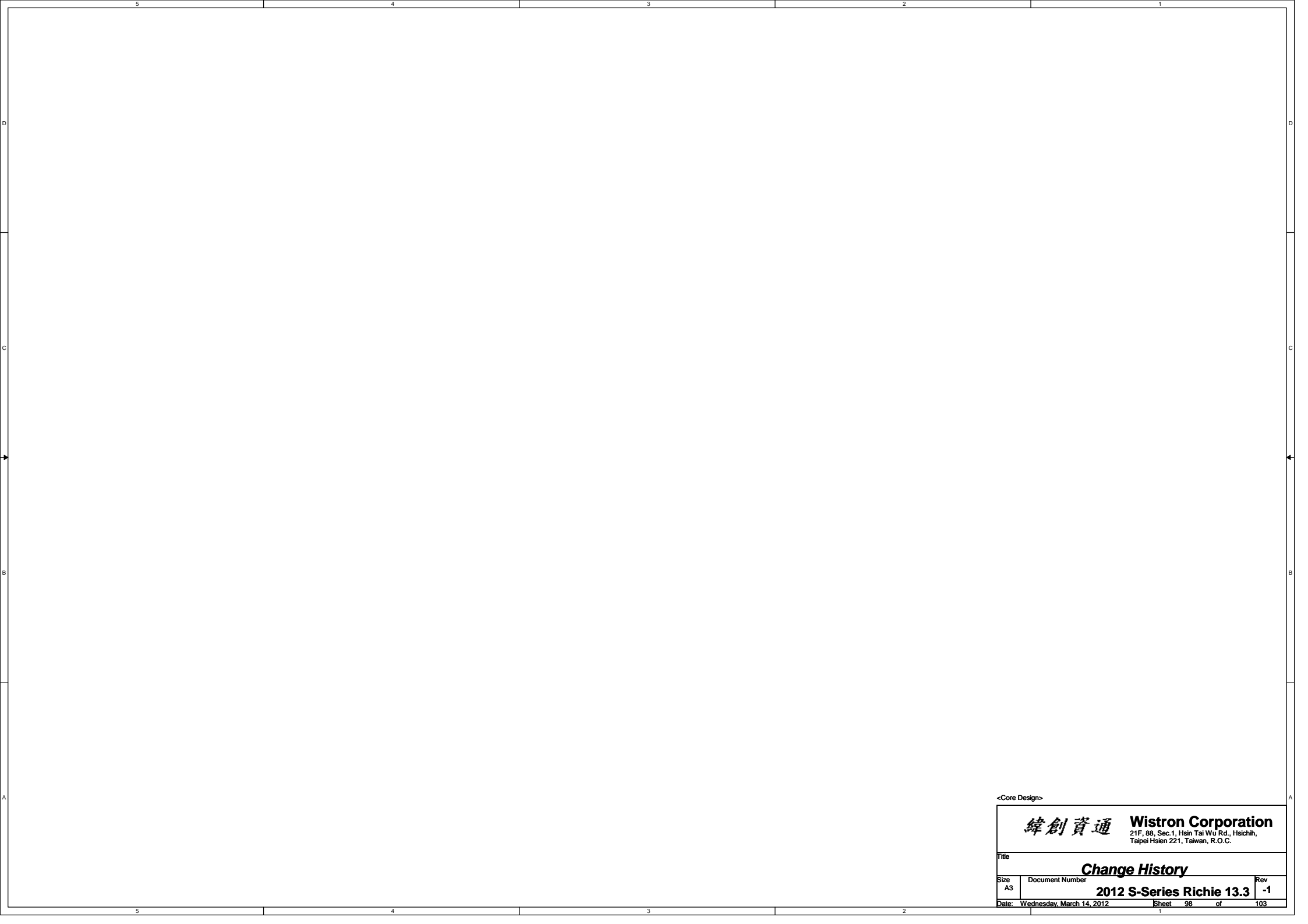
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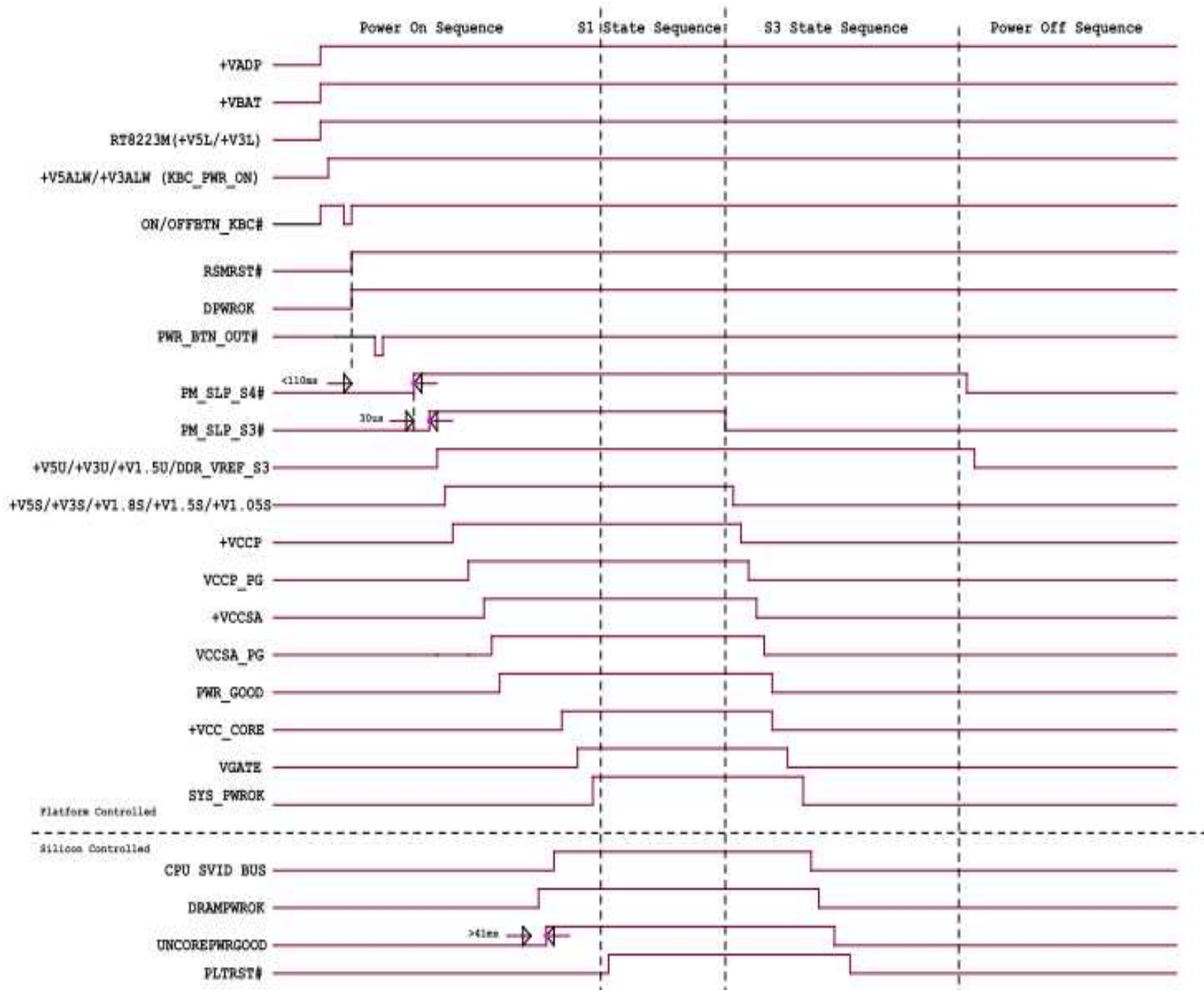
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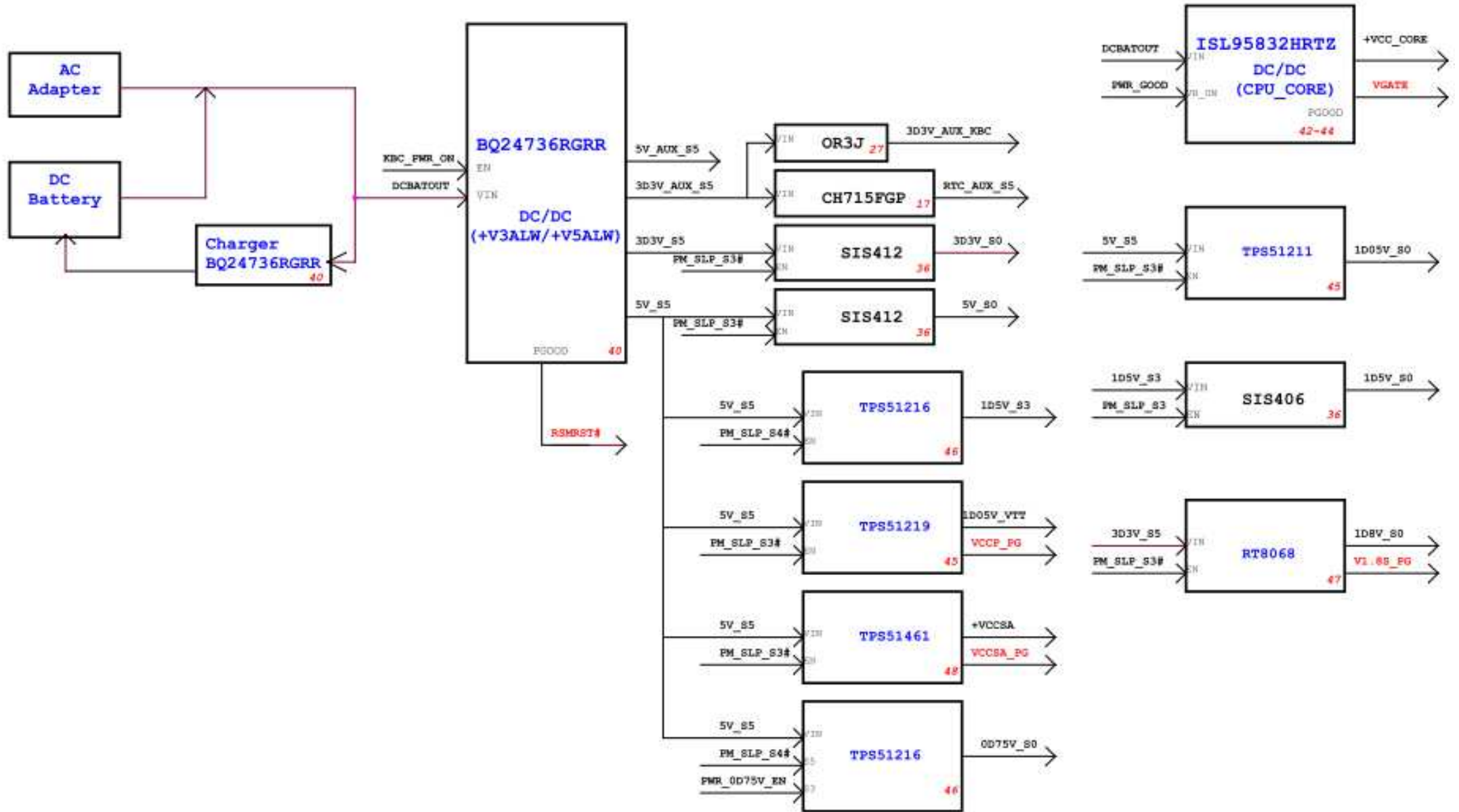
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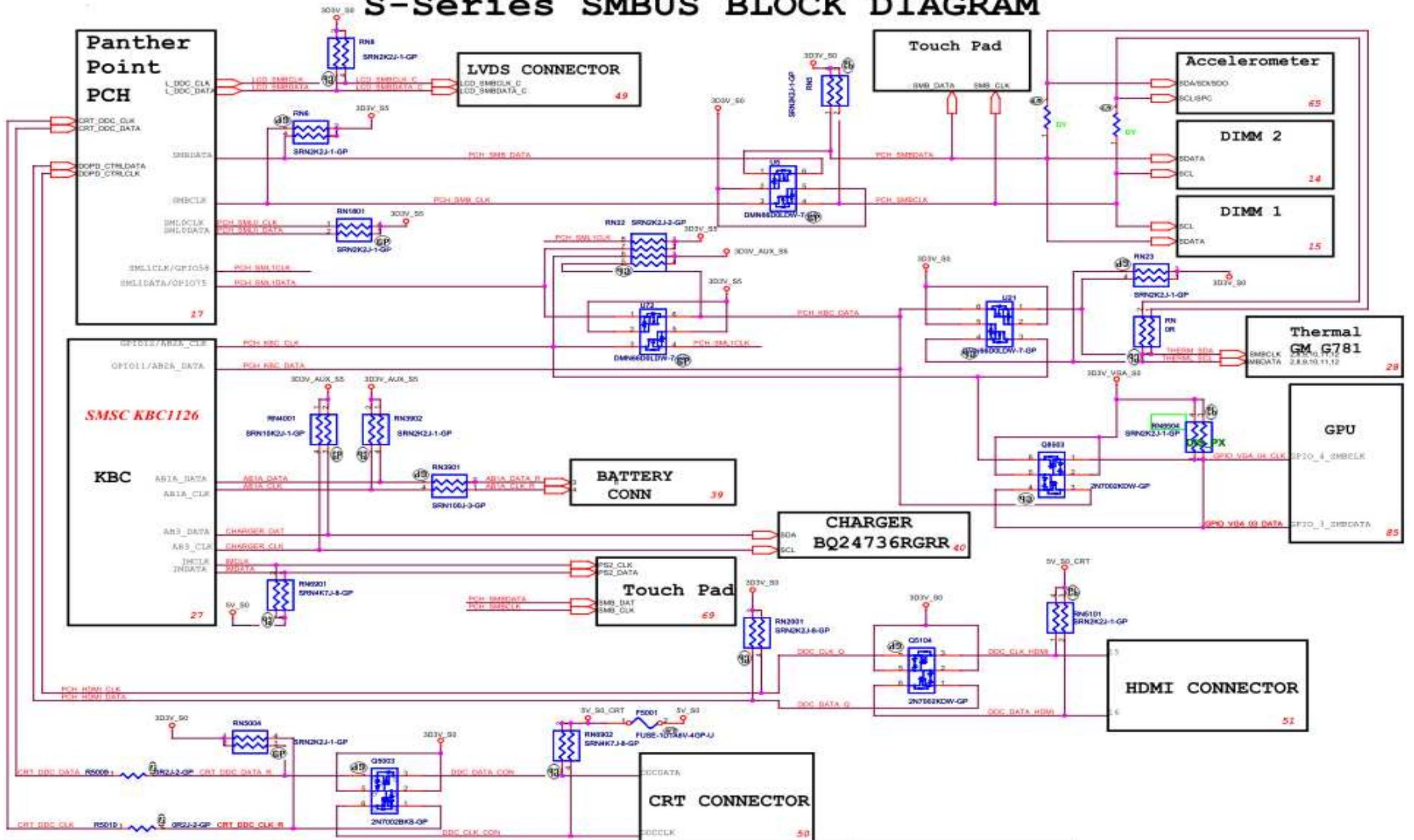
S-Series Power Sequence and Reset Signal Timing



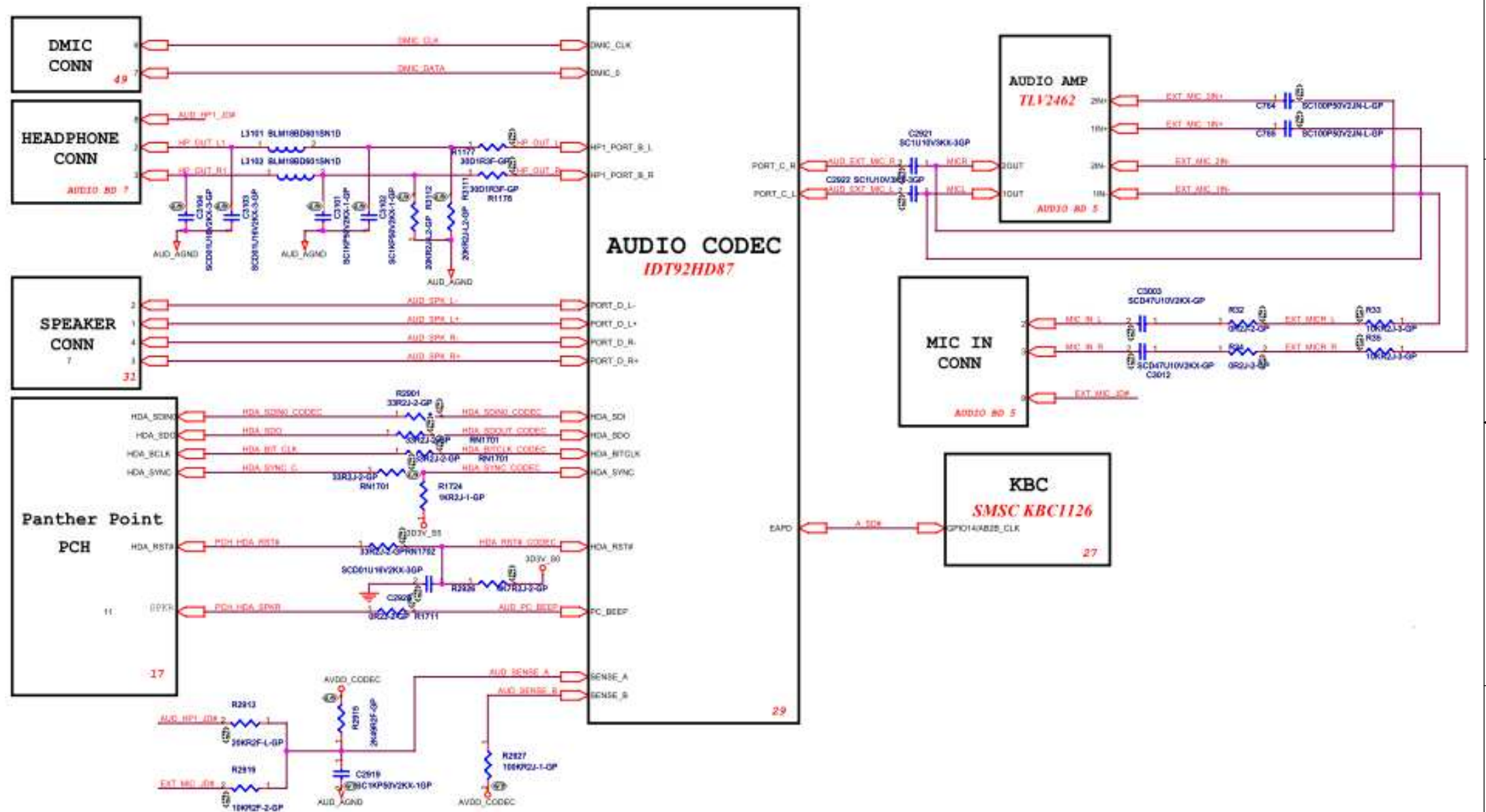
S-Series POWER BLOCK DIAGRAM



S-Series SMBUS BLOCK DIAGRAM



S-Series AUDIO BLOCK DIAGRAM



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