Compal Confidential

YOGA Gloria 14" & 15"
DIS M/B Schematics Document

Intel KabyLake U Processor with DDR4

N16S-GTR-S(940) (23x23mm)

2016-6-6

LA-D471P

REV :2.0

ZZZ BIUY2_PCB

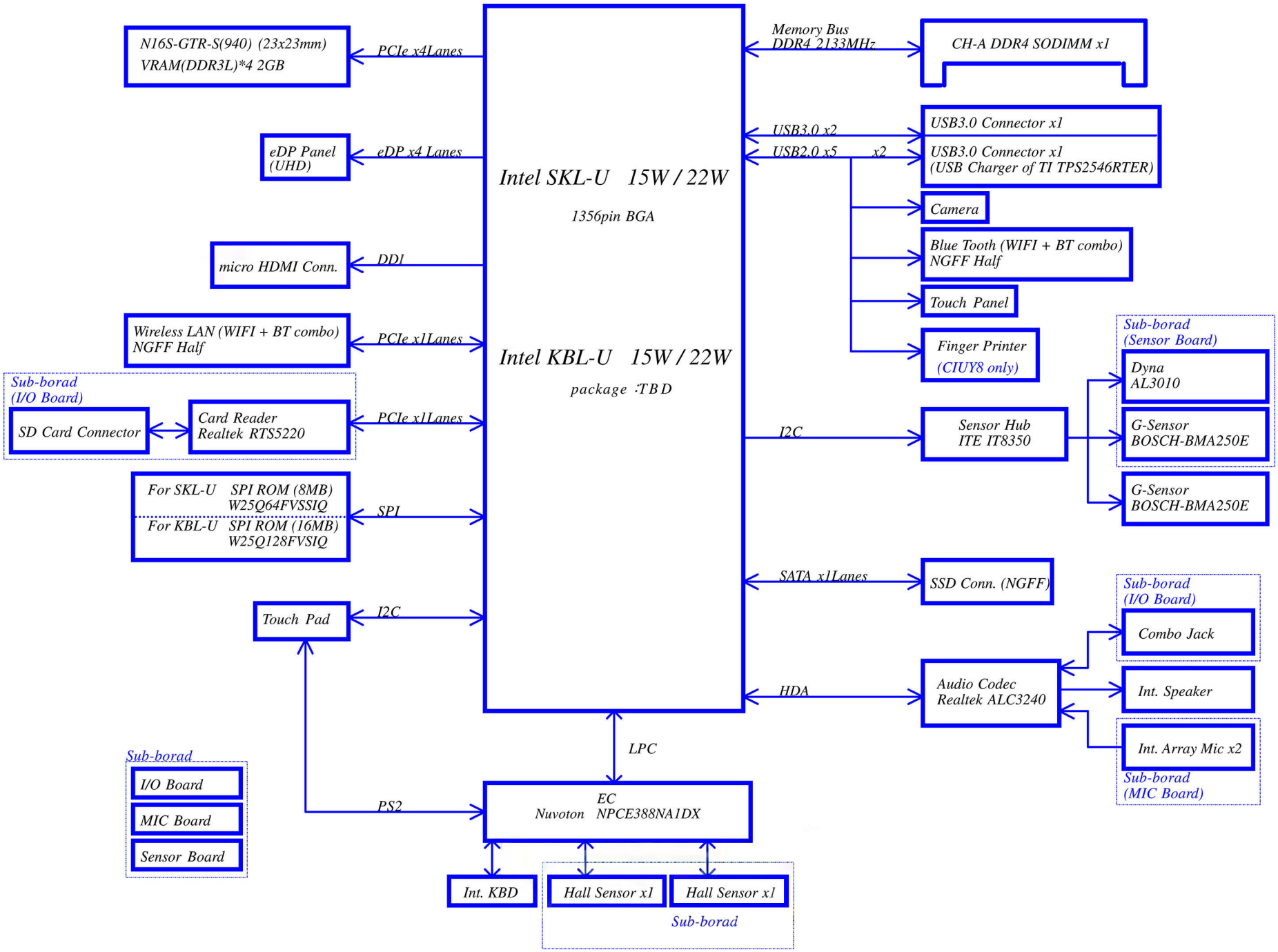
Part Number	Description
DAZ1JH00100	PCB BIUY2 LA-D471P LS-D471P/D472/D473 02

PCB@

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.			
Title: Cover Page			
Size: C	Document Number: LA-D471P		Rev: 2.0
Date: Thursday, October 20, 2016	Sheet 1 of 53		

YOGA Gloria 14" & 15"



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Voltage Rails

power plane / State	B+	+5VALW +3VALW +1.8VALW +1.0VALW	+1.2V +2.5V	+5VS +3VS +1.0VS_VCCOPC +VCCCORE +VCCGT +1.0V_VCCST +1.0VS_VCCIO +1.8VS +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
for 2+3E power	23E@
For Camera	CMOS@
For DIS	DIS@
For UMA	UMA@
For GPU GC6	GC6@
No GPU GC6	NOGC6@
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For Thermal sensor	EX_THM@
For RF	RF@
For EMI	EMI@
No EMI	@EMI@
For ESD	ESD@
No ESD	@ESD@
Connector	ME@
For Test Point	TP@
For PCB	PCB@
For Hynix Memory	H2G@
For Samsung Memory	S2G@
For Micron Memory	M2G@
For VARM X76	GM_X76@
For Finger Print (only 15)	FP@
for KBL platform	KB_L@
for SKL platform	SKL@
For 15" ESD_FP	@ESD_FP@
For UHD	UHD@

ZZZ1 @ BARCODE_8X8

ZZZ3 @ BARCODE_12X4

ZZZ2 @ BARCODE_20X4

ZZZ4 @ BARCODE_10X10

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h

EC SM Bus4 address

Device	Address
BMA250E	0001 100X 18h
AL3010	0001 110X 1Ch

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	SODIMM	Thermal Sensor	TP	PCH	G-SENSOR	L-SENSOR
SMB_EC_CK1 SMB_EC_DA1	NECP388 +3VALW	X	V +3VALW	V +19V_VIN	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	NECP388 +3VS	V +3VGS	X	X	X	V +3VS	X	V +3VS	X	X
SMB_EC_CK3 SMB_EC_DA3	NECP388 +3VS	X	X	X	X	X	X	V +3VS	X	X
SMB_EC_CK4 SMB_EC_DA4	NECP388 +3VS	X	X	X	X	X	X	X	V +3VS	V +3VS
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VS	X	X	X	V +3VS	X	V +3VS	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vinafix

USB 2.0 Port Table

Port	External USB Port
1	
2	USB2/3 MB(IO_Port2)
3	USB2/3 MB(IO_Port1)
4	
5	Camera
6	
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	
2	USB2/3 MB(IO_Port2)
3	USB2/3 MB(IO_Port1)
4	
5	
6	

SATA Port Table

Port	
0	SSD
1	

PCIE Port Table

Port	Lane	
1	1	
2	2	GPU
3	3	
4	4	
5		
6		NGFF WLAN+BT
7		
8		
9		CardReader
10		

Compal Electronics, Inc.

Title: Notes List

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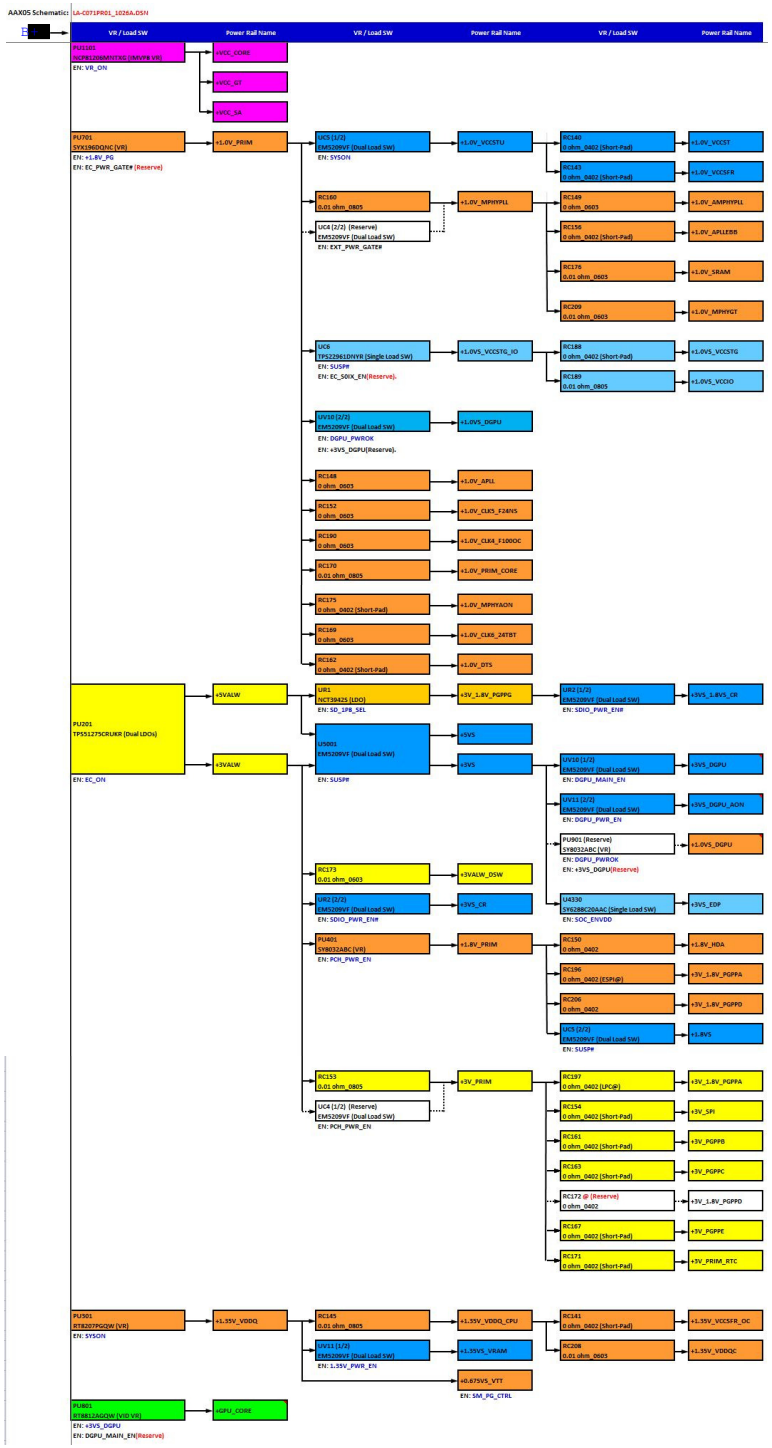
BIVS3/ VE3 -PowerMap_SKL-U22_DDR3L_Volume_NON CS]

AAX0S Schematics: LA-C071PR01_1026A.DSN



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Compal Electronics, Inc.

Title: Power MAP

Size	Document Number	Rev
		2.0

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[AAX05-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]

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Compal Electronics, Inc.

Title: **Power Sequence**

Size	Document Number	Rev
		2.0

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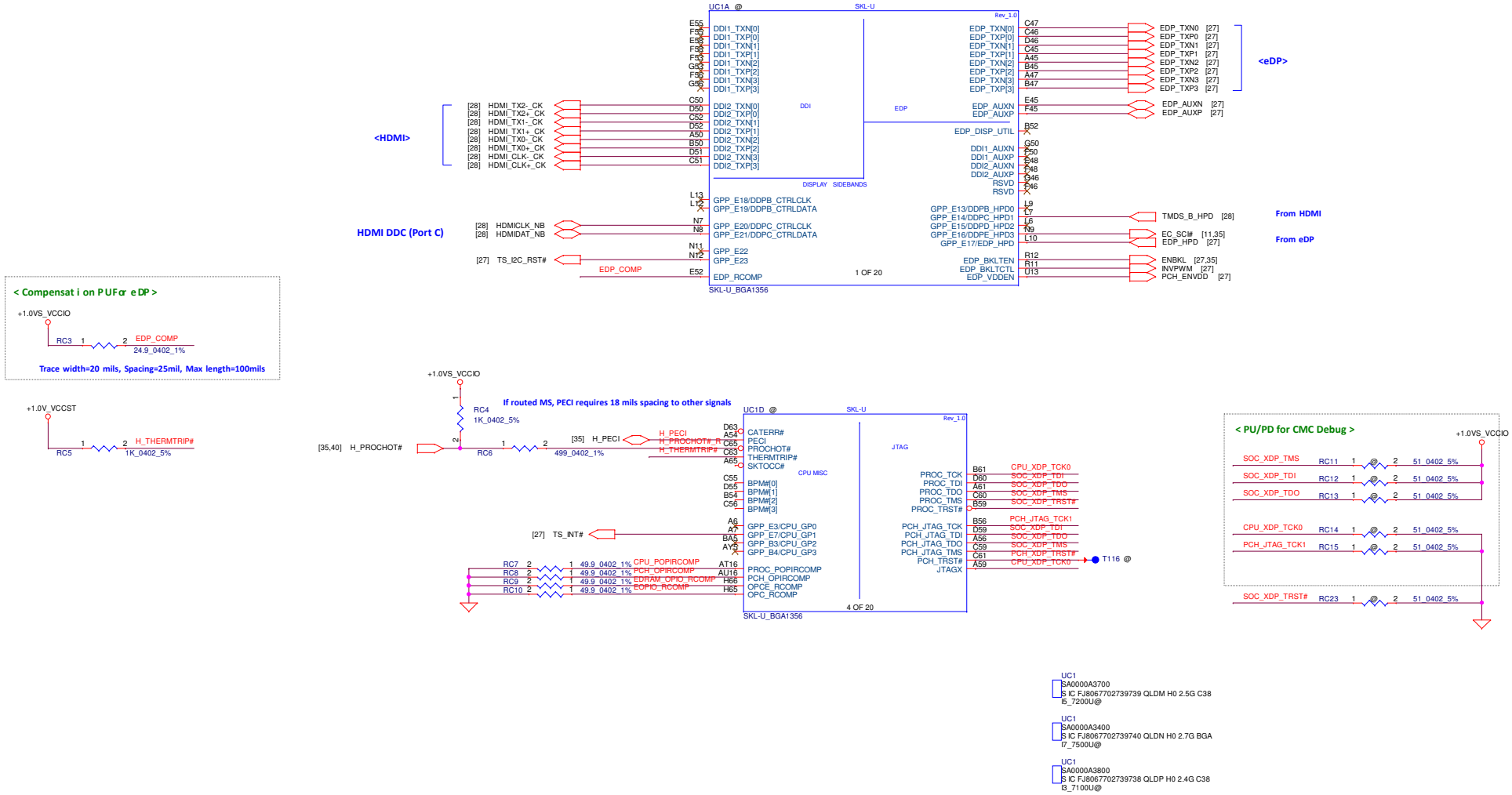

Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,EDP,MISC,CMC

Size	Document Number	Rev
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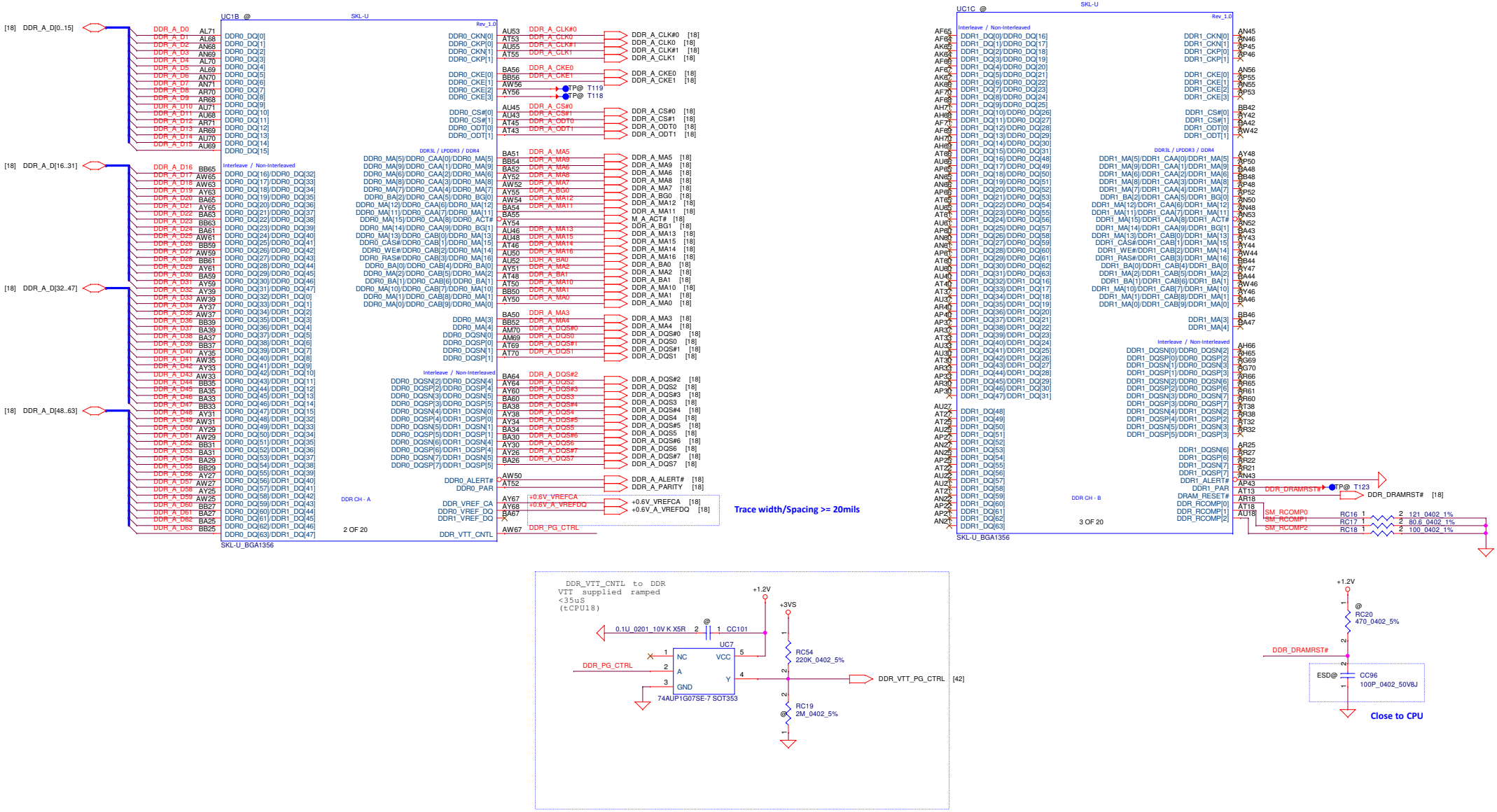
Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.			
Title	SKL-U(2/12)DDR3L		
Size	Document Number		Rev
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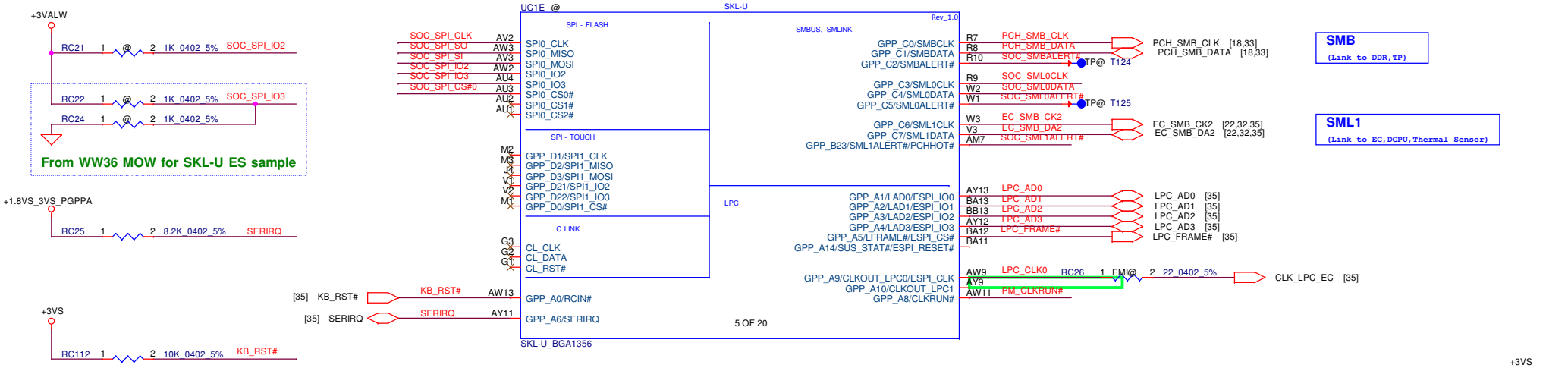
SML0ALERT# (Internal Pull Down):

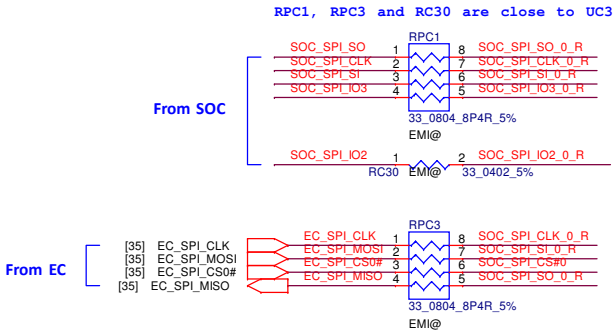
eSPI or LPC

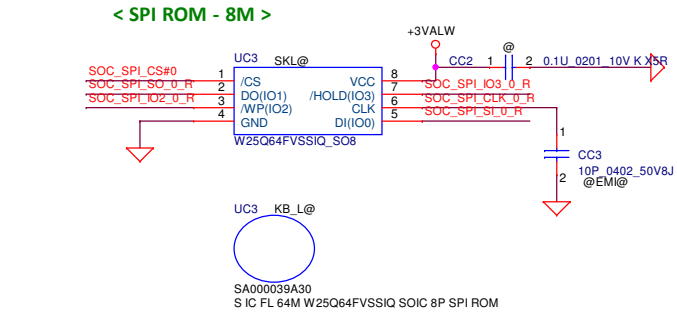
0 = LPC is selected for EC ==> Default

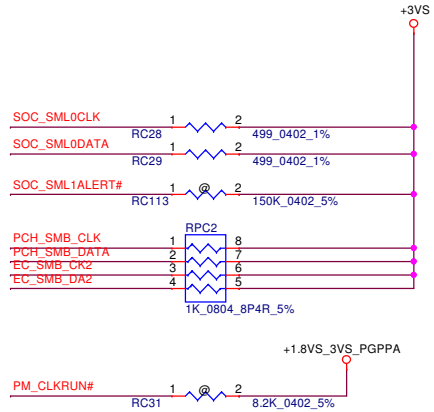
1 = eSPI is selected for EC



RPC1, RPC3 and RC30 are close to UC3







Follow 543016_SKL_U_Y_PDG_0_9

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,SMB,LPC,ESPI

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< HD AUDIO >

[29] HDA_BITCLK_AUDIO
[29] HDA_SYNC_AUDIO
[29] HDA_SDOUT_AUDIO

RPC4
1 2 3 4 8 7 6 5
HDA_BIT_CLK
HDA_SYNC
HDA_SDOUT
33_0804_8P4R_5%
EMI@

< To Enable ME Override >

[35] ME_EN — RC116 2 — 1 0_0402_5% — HDA_SDOUT

UC1G @ SKL-U Rev_1.0

AUDIO

HDA_SYNC BA22 HDA_SYNC/I2S0_SFRM
HDA_BIT_CLK AY22 HDA_BLK/I2S0_SCLK
HDA_SDOUT BB22 HDA_SDO/I2S0_TXD
[29] HDA_SDIN0 BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD

AK7 GPP_F1/I2S2_SFRM
AK6 GPP_F0/I2S2_SCLK
AK9 GPP_F2/I2S2_TXD
AK10 GPP_F3/I2S2_RXD

H5 GPP_D19/DMIC_CLK0
D7 GPP_D20/DMIC_DATA0

D8 GPP_D17/DMIC_CLK1
C8 GPP_D18/DMIC_DATA1

[29] HDA_SPKR HDA_SPKR AW5 GPP_B14/SPKR

SDIO / SDXC

GPP_G0/SD_CMD AB11
GPP_G1/SD_DATA0 AB13
GPP_G2/SD_DATA1 AB12
GPP_G3/SD_DATA2 W12
GPP_G4/SD_DATA3 W11
GPP_G5/SD_CD# W10
GPP_G6/SD_CLK W8
GPP_G7/SD_WP W7

GPP_A17/SD_PWR_EN#/ISH_GP7 BA9
GPP_A16/SD_1P8_SEL BB9

SD_RCOMP AB7 — 1 RC76 @ 2 200_0402_1%

GPP_F23 AF13

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SKL-U_BGA1356

+3VS

RC33 1 @ 2 2.2K_0402_5% HDA_SPKR

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

UC1I @ SKL-U Rev_1.0

CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C38 CSI2_DN1
D38 CSI2_DP1
C36 CSI2_DN2
D36 CSI2_DP2
A38 CSI2_DN3
B38 CSI2_DP3

C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 C32
CSI2_CLKP1 D32
CSI2_CLKN2 C29
CSI2_CLKP2 D29
CSI2_CLKN3 B26
CSI2_CLKP3 A26

CSI2_COMP E13 — 1 RC80 @ 2 100_0402_1%
GPP_D4/FLASHTRIG B7

EMMC

GPP_F13/EMMC_DATA0 AP2
GPP_F14/EMMC_DATA1 AP1
GPP_F15/EMMC_DATA2 AP3
GPP_F16/EMMC_DATA3 AN3
GPP_F17/EMMC_DATA4 AN1
GPP_F18/EMMC_DATA5 AN2
GPP_F19/EMMC_DATA6 AM4
GPP_F20/EMMC_DATA7 AM1

GPP_F21/EMMC_RCLK AM2
GPP_F22/EMMC_CLK AM3
GPP_F12/EMMC_CMD AP4

EMMC_RCOMP AT1 — 1 RC129 @ 2 200_0402_1%

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SKL-U_BGA1356

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

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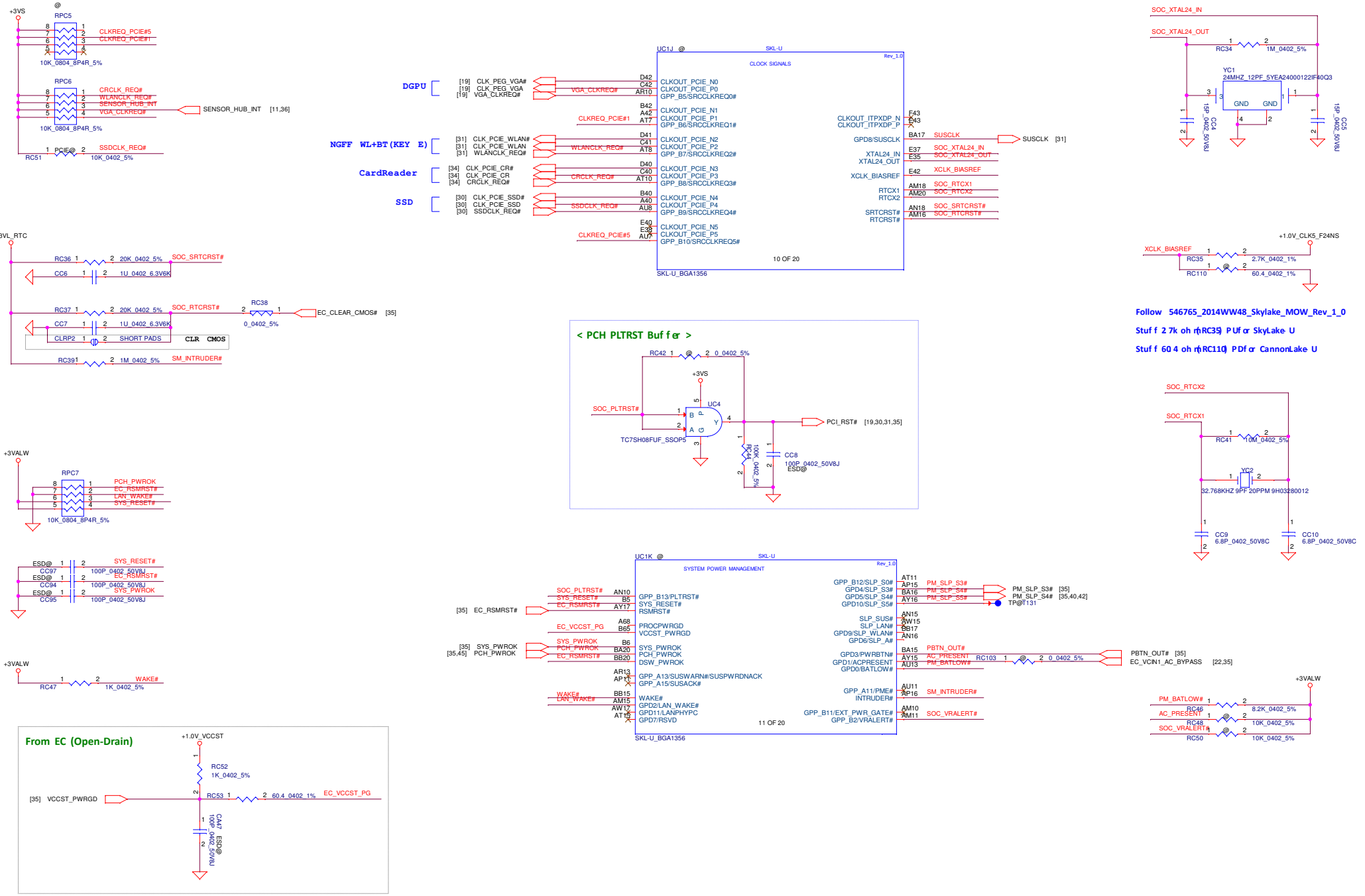

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,PM,GPIO

Size	Document Number	Rev
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GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

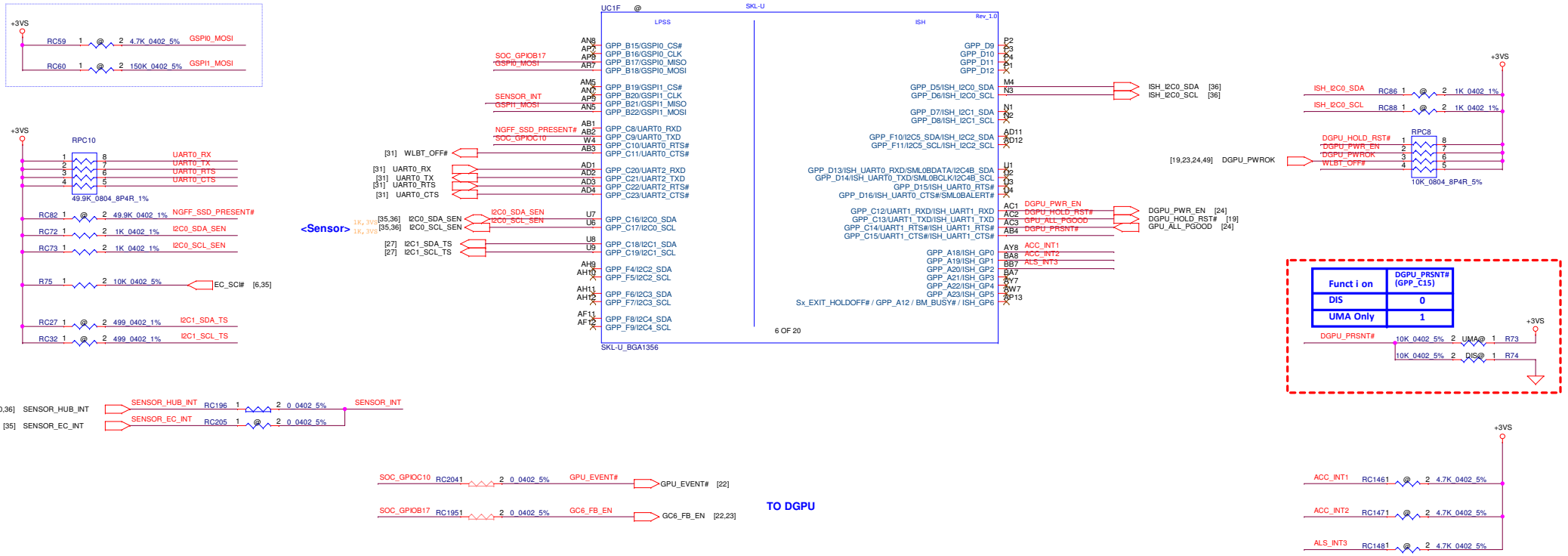
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i oni s usef ul when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode

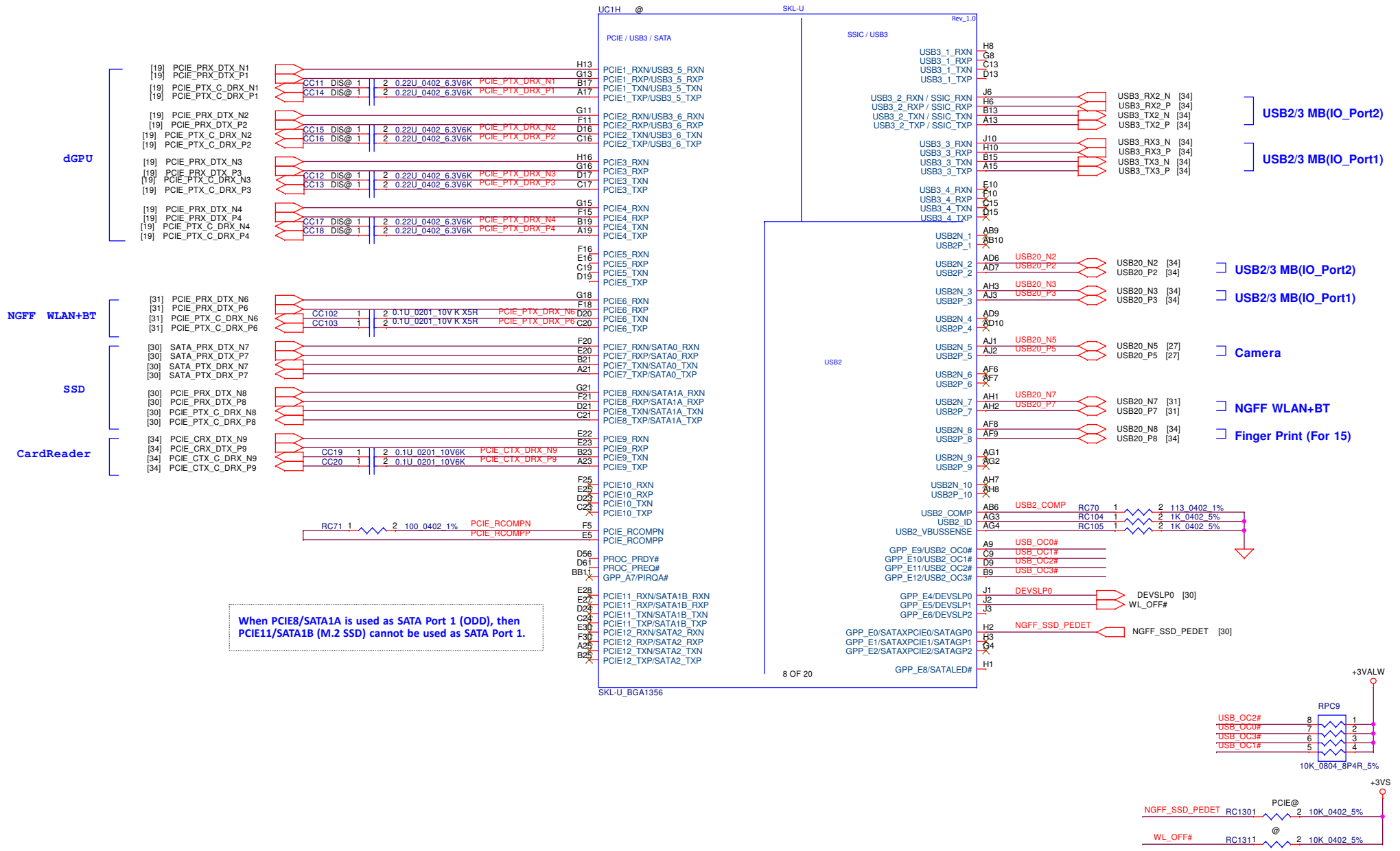


Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

Size	Document Number	Rev
Custom	LA-D471P	2.0

Date: Monday, June 06, 2016 Sheet 11 of 53



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.			
Title	SKL-U(7/12)PCIE,USB,SATA		
Size	Document Number		Rev
Custom	LA-D471P		2.0
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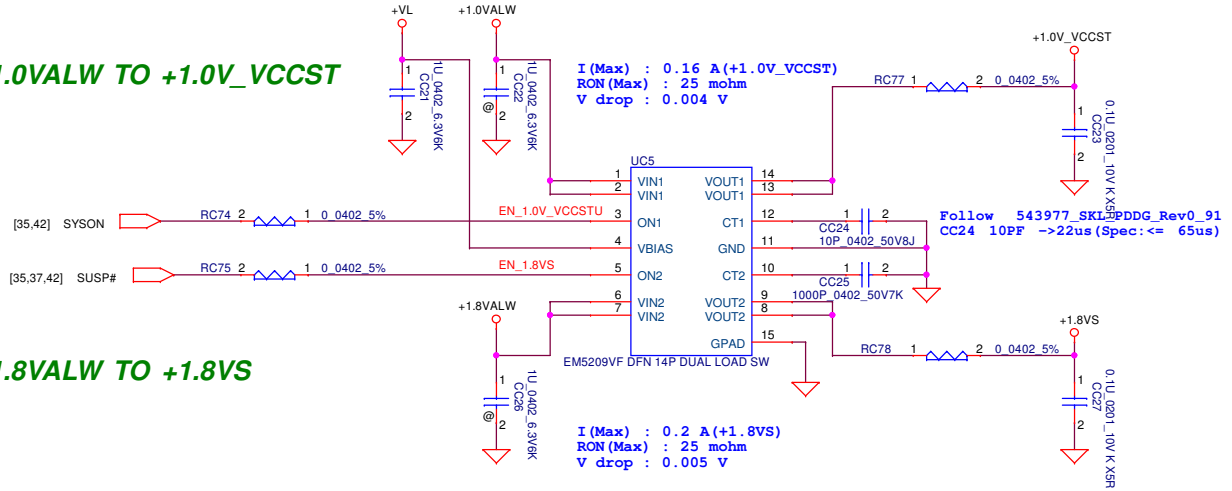
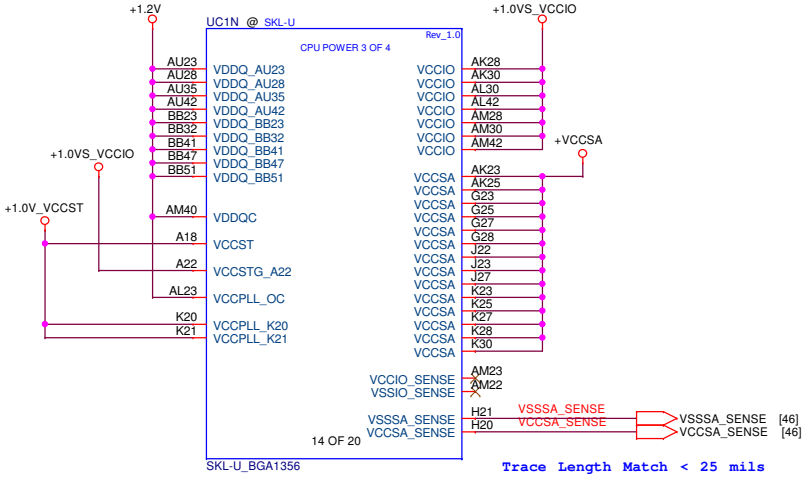
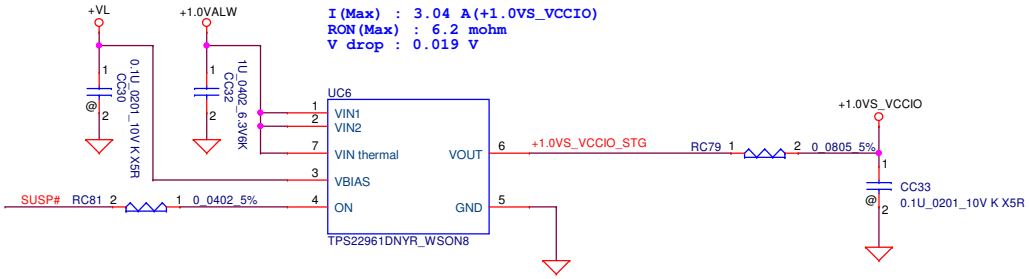
+1.0VALW TO +1.0V_VCCST

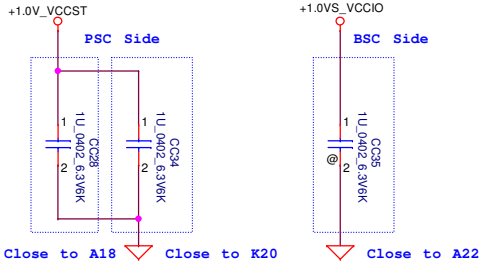


+1.8VALW TO +1.8VS

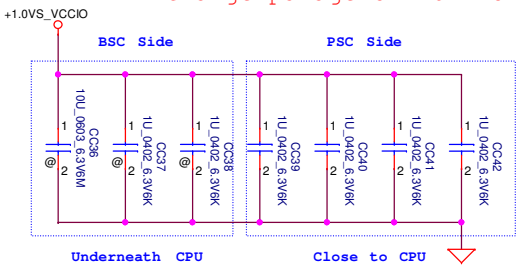


+1.0VALW TO +1.0VS_VCCIO

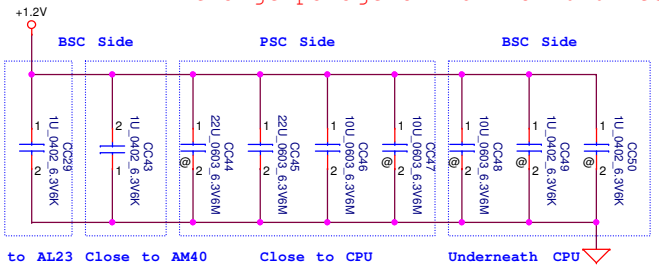




change pakage of 1U from 0201 to 0402



change pakage of 1U from 0201 to 0402



change pakage of 10U from 0402 to 0603

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: **SKL-U(8/12)Power**

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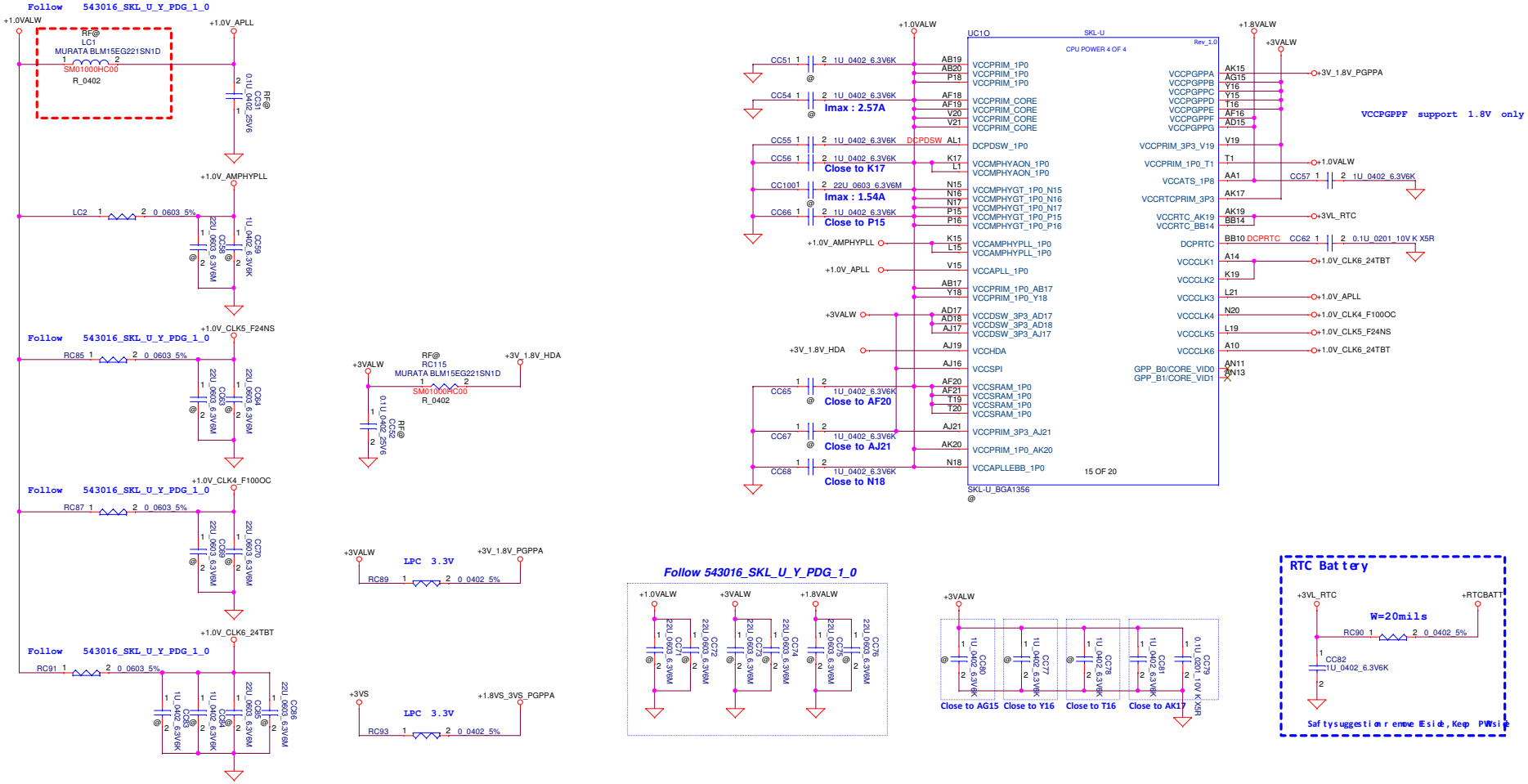
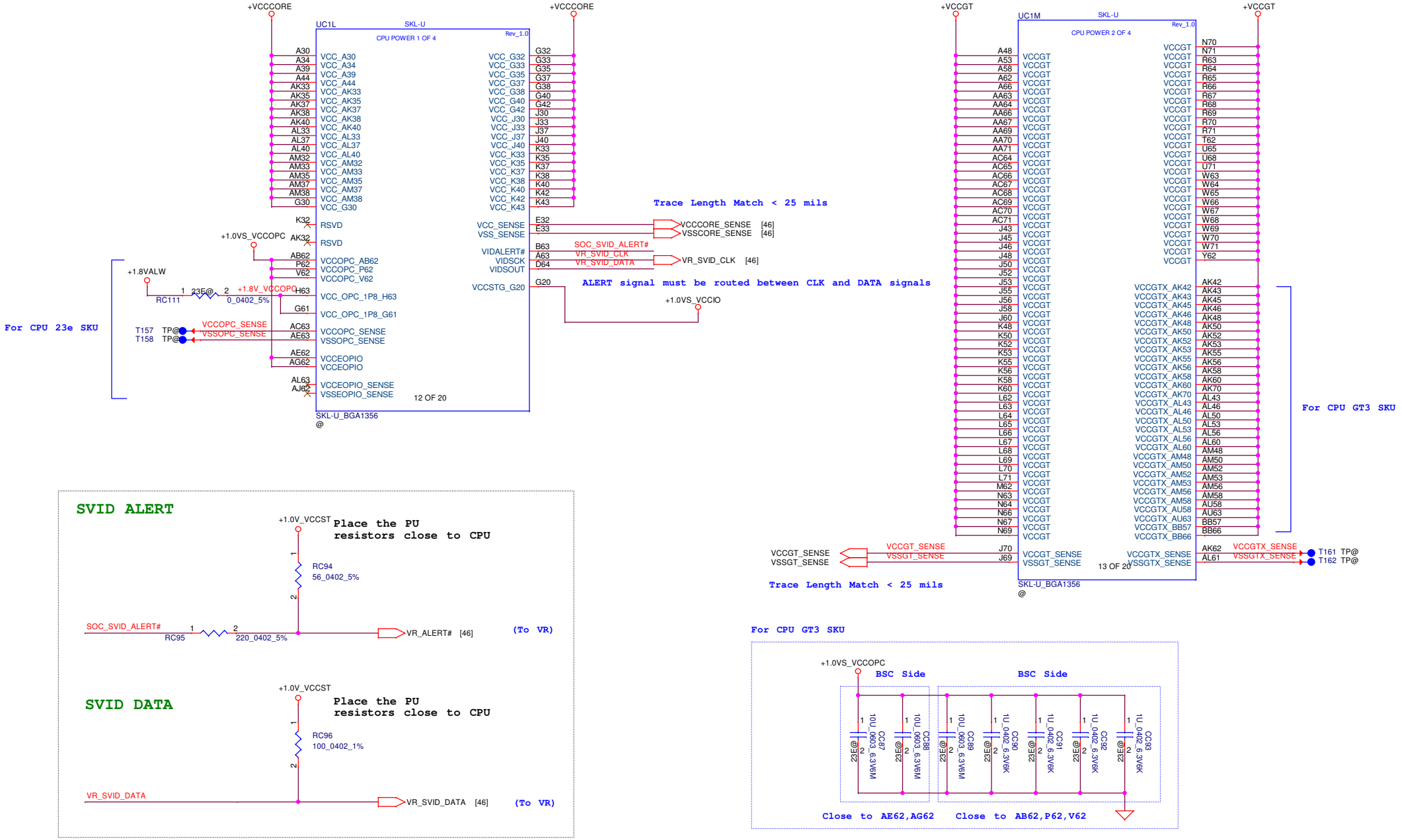


Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.			
Title	SKL-U(9/12)Power		
Size: Custom	Document Number: LA-D471P		Rev: 2.0
Date: Monday, June 06, 2016	Sheet 14 of 53		



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.			
Title	SKL-U(10/12)Power,SVID		
Size	Document Number		Rev
Custom	LA-D471P		2.0
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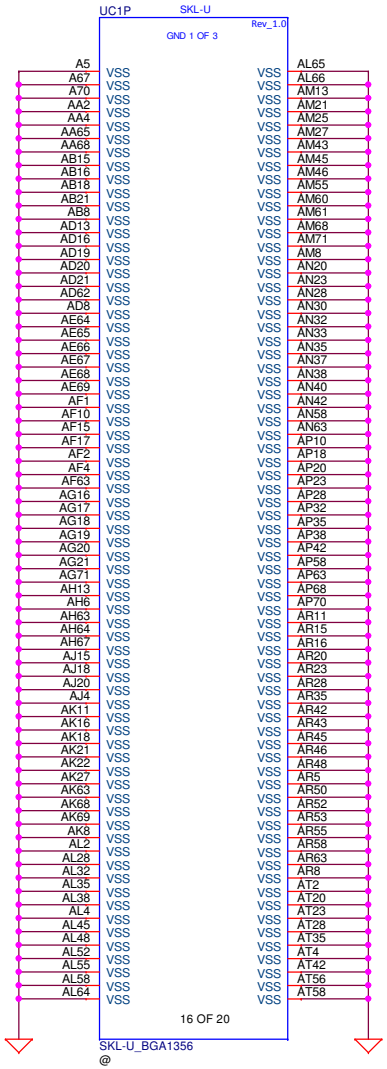
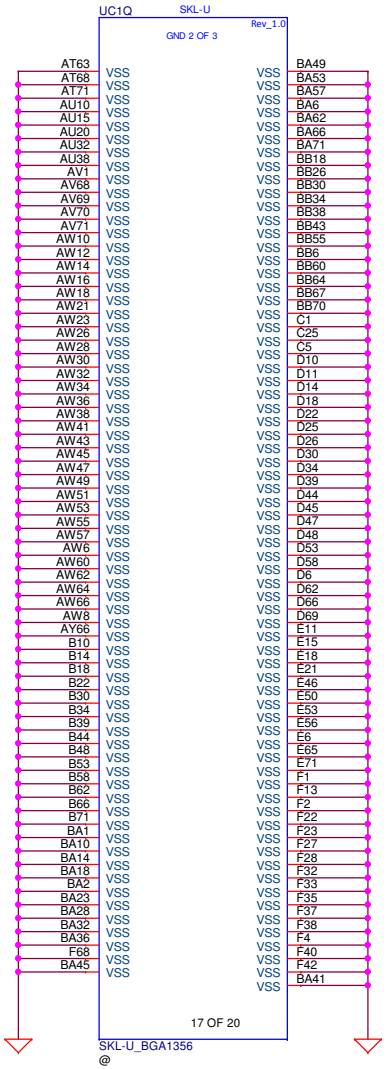
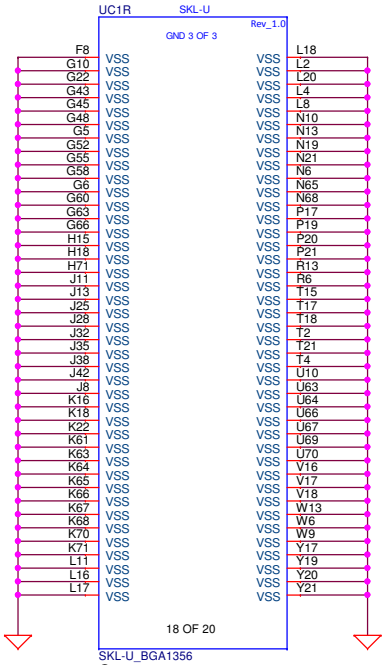






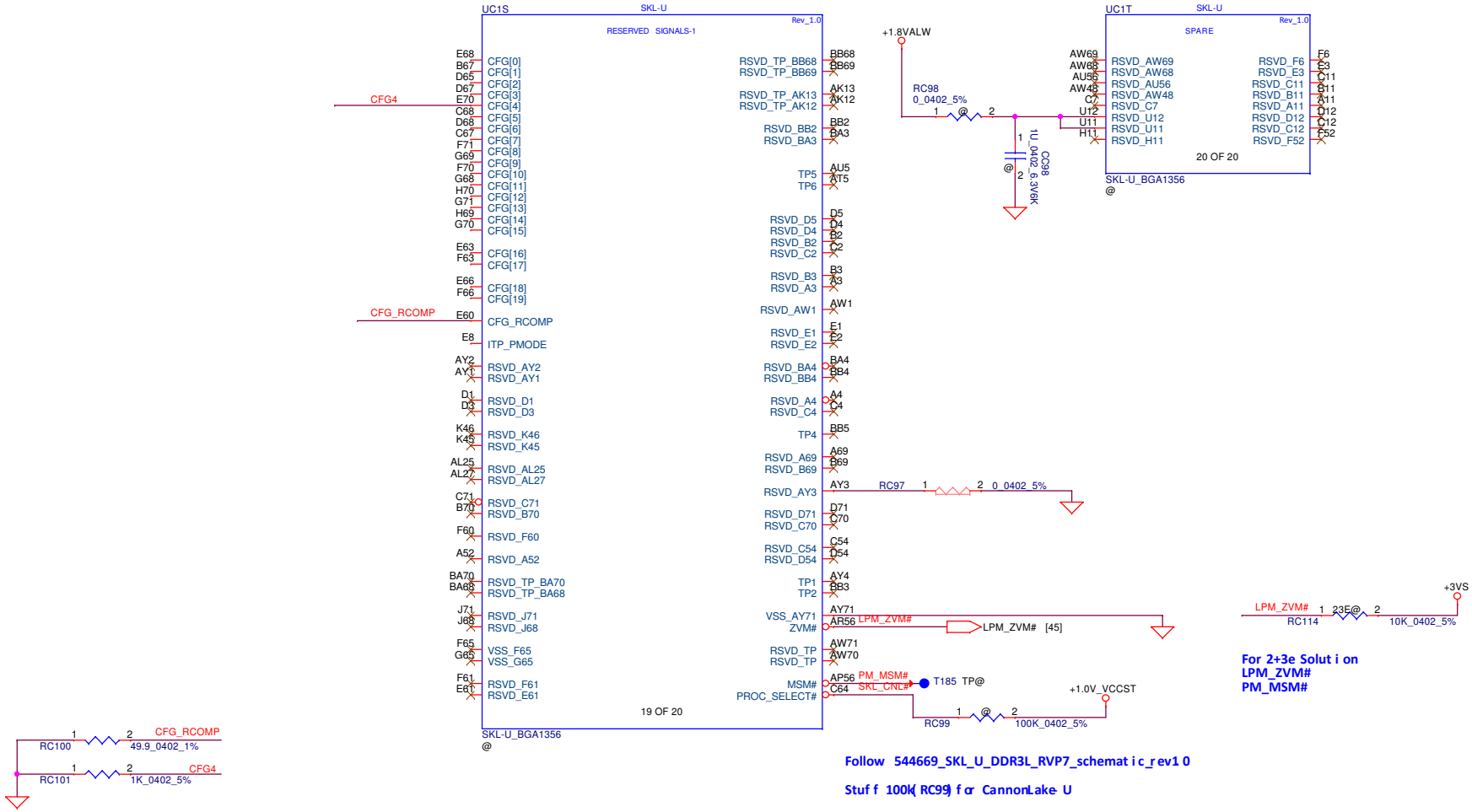
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size	Document Number	Rev
Custom	LA-D471P	2.0

Date: Monday, June 06, 2016 Sheet 16 of 53



For 2+3e Solution
LPM_ZVM#
PM_MSM#

Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1 0

Stuff 100K(RC99) for CannonLake- U

Un-stuff 100K(RC99) for SkyLake- U

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.		
Title: SKL-U(12/12)CFG,RSVD		
Size: Custom	Document Number: LA-D471P	Rev: 2.0
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[7] DDR_A_DQS#[0..7]
[7] DDR_A_D[0..63]
[7] DDR_A_DQS[0..7]

[7] DDR_A_MA[0..16]

[7] DDR_A_BA0
[7] DDR_A_BA1
[7] DDR_A_BG0
[7] DDR_A_BG1

[7] DDR_A_CLK0
[7] DDR_A_CLK#0
[7] DDR_A_CLK1
[7] DDR_A_CLK#1

[7] DDR_A_CKE0
[7] DDR_A_CKE1

[7] DDR_A_CS#0
[7] DDR_A_CS#1

[8,33] PCH_SMB_DATA
[8,33] PCH_SMB_CLK

[7] DDR_A_ODT0
[7] DDR_A_ODT1

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

+1.2V

CD01 1U_0402_6.3V6K
CD25 1U_0402_6.3V6K
CD05 1U_0402_6.3V6K
CD27 1U_0402_6.3V6K
CD08 1U_0402_6.3V6K
CD09 1U_0402_6.3V6K
CD17 1U_0402_6.3V6K
CD18 1U_0402_6.3V6K

4 as near side of the DIMM close to VDD pins

+1.2V

CD10 10U_0603_6.3V6M
CD11 10U_0603_6.3V6M
CD12 10U_0603_6.3V6M
CD13 10U_0603_6.3V6M
CD14 10U_0603_6.3V6M
CD19 10U_0603_6.3V6M
CD15 10U_0603_6.3V6M
CD16 10U_0603_6.3V6M
CD20 10U_0603_6.3V6M
CD95 330U_D3_2.5VY_R6M

Place these caps on the VTT plane close to DIMM

+0.6VS

CD30 1U_0402_6.3V6K
CD31 1U_0402_6.3V6K
CD32 1U_0402_6.3V6K
CD33 1U_0402_6.3V6K
CD22 10U_0603_6.3V6M
CD23 10U_0603_6.3V6M

+3VS

C2142 2.2U_0402_6.3V6M

+3VS_DIMM

CD28 0.1U_0201_10V K5R

close to DIMM

+2.5V

C2140 10U_0603_6.3V6M
CD29 1U_0402_6.3V6K

Reverse Type

2-3A to 1 DIMMs/channel

+1.2V

JDIMM1

DDR_A_D4	VSS1	VSS2	DDR_A_D1
DDR_A_D5	DQ5	DQ4	DDR_A_D0
	VSS3	VSS4	
	DQ1	DQ0	
DDR_A_DQS#0	VSS5	VSS6	
DDR_A_DQS0	DQS0_c	DM0_n/DBI0_n	
	DQS0_t	VSS7	
DDR_A_D2	VSS8	DQ6	DDR_A_D3
	DQ7	VSS9	DDR_A_D7
DDR_A_D6	VSS10	DQ2	
	DQ3	VSS11	DDR_A_D9
DDR_A_D8	VSS12	DQ12	
	DQ13	VSS13	DDR_A_D13
DDR_A_D12	VSS14	DQ8	
	DQ9	VSS15	DDR_A_DQS#1
	VSS16	DQS1_c	DDR_A_DQS1
	DM1_n/DBI_n	DQS1_t	
DDR_A_D11	VSS17	VSS18	DDR_A_D15
	DQ15	DQ14	
DDR_A_D10	VSS19	VSS20	DDR_A_D14
	DQ10	DQ11	
DDR_A_D21	VSS21	VSS22	DDR_A_D17
	DQ21	DQ20	
DDR_A_D20	VSS23	VSS24	DDR_A_D16
	DQ17	DQ16	
DDR_A_DQS#2	VSS25	VSS26	
DDR_A_DQS2	DQS2_c	DM2_n/DBI2_n	
	DQS2_t	VSS27	DDR_A_D23
	VSS28	DQ22	
DDR_A_D22	DQ23	VSS29	DDR_A_D19
	VSS30	DQ18	
DDR_A_D18	DQ19	VSS31	DDR_A_D28
	VSS32	DQ28	
DDR_A_D25	DQ29	VSS33	DDR_A_D29
	VSS34	DQ24	
DDR_A_D24	DQ25	VSS35	DDR_A_DQS#3
	VSS36	DQS3_c	DDR_A_DQS3
	DM3_n/DBI3_n	DQS3_t	
	VSS37	VSS38	DDR_A_D31
DDR_A_D30	DQ30	DQ31	
DDR_A_D26	VSS39	VSS40	DDR_A_D27
	DQ26	DQ27	
	VSS41	VSS42	
	CB5/NC	CB4/NC	
	VSS43	VSS44	
	CB1/NC	CB0/NC	
	VSS45	VSS46	
	DQS8_c	DM8_n/DBI_n/NC	
	DQS8_t	VSS47	
	VSS48	CB6/NC	
	CB2/NC	VSS49	
	VSS50	CB7/NC	
	CB3/NC	VSS51	
DDR_A_CKE0	VSS52	RESET_n	DDR_DRAMRST#_R
	CKE0	CKE1	DDR_A_CKE1
DDR_A_BG1	VDD1	VDD2	
DDR_A_BG0	BG1	ACT_n	M_A_ACT# [7]
	BG0	ALERT_n	DDR_A_ALERT# [7]
DDR_A_MA12	VDD3	VDD4	DDR_A_MA11
DDR_A_MA9	A12	A11	DDR_A_MA7
	A9	A7	
DDR_A_MA8	VDD5	VDD6	DDR_A_MA5
DDR_A_MA6	A8	A5	DDR_A_MA4
	A6	A4	
DDR_A_MA3	VDD7	VDD8	DDR_A_MA2
DDR_A_MA1	A3	A2	
	A1	EVENT_n/NF	
	VDD9	VDD10	
DDR_A_CLK0	CK0_t	CK1_t/NF	DDR_A_CLK1
DDR_A_CLK#0	CK0_c	CK1_c/NF	DDR_A_CLK#1
	VDD11	VDD12	
[7] DDR_A_PARITY	PARITY	A0	DDR_A_MA0
DDR_A_BA1	BA1	A10/AP	DDR_A_MA10
	VDD13	VDD14	
DDR_A_CS#0	CS0_n	BA0	DDR_A_BA0
DDR_A_MA14	WE_n/A14	RAS_n/A16	DDR_A_MA16
	VDD15	VDD16	
DDR_A_ODT0	ODT0	CAS_n/A15	DDR_A_MA15
DDR_A_CS#1	CS1_n	A13	DDR_A_MA13
	VDD17	VDD18	
DDR_A_ODT1	ODT1	C0/CS2_n/NC	
	VDD19	VREFCA	
	C1, CS3_n,NC	SA2	
	VSS53	VSS54	
DDR_A_D37	DQ37	DQ36	DDR_A_D34
DDR_A_D33	VSS55	VSS56	DDR_A_D32
	DQ33	DQ32	
DDR_A_DQS#4	VSS57	VSS58	
DDR_A_DQS4	DQS4_c	DM4_n/DBI4_n	
	DQS4_t	VSS59	
DDR_A_D38	VSS60	DQ39	DDR_A_D39
DDR_A_D35	DQ38	VSS61	DDR_A_D36
	VSS62	DQ35	
DDR_A_D44	DQ34	VSS63	DDR_A_D41
DDR_A_D45	VSS64	DQ45	
	DQ44	VSS65	DDR_A_D40
	VSS66	DQ41	
	DQ40	VSS67	DDR_A_DQS#5
	VSS68	DQS5_c	DDR_A_DQS5
DDR_A_D43	DM5_n/DBI5_n	DQS5_t	
	VSS69	VSS70	DDR_A_D47
DDR_A_D42	DQ46	DQ47	
DDR_A_D49	VSS71	VSS72	DDR_A_D46
DDR_A_D52	DQ42	DQ43	
	VSS73	VSS74	DDR_A_D48
	DQ52	DQ53	
	VSS75	VSS76	DDR_A_D53
DDR_A_DQS#6	DQ49	DQ48	
DDR_A_DQS6	VSS77	VSS78	
	DQS6_c	DM6_n/DBI6_n	
	DQS6_t	VSS79	
DDR_A_D55	VSS80	DQ54	DDR_A_D54
	DQ55	VSS81	DDR_A_D51
DDR_A_D50	VSS82	DQ50	
	DQ51	VSS83	DDR_A_D57
DDR_A_D59	VSS84	DQ60	
	DQ61	VSS85	DDR_A_D56
DDR_A_D58	VSS86	DQ57	
	DQ56	VSS87	DDR_A_DQS#7
	VSS88	DQS7_c	DDR_A_DQS7
	DM7_n/DBI7_n	DQS7_t	
	VSS89	VSS90	DDR_A_D63
DDR_A_D61	DQ62	DQ63	
DDR_A_D60	VSS91	VSS92	DDR_A_D62
	DQ58	DQ59	
PCH_SMB_CLK	VSS93	VSS94	PCH_SMB_DATA
+3VS_DIMM	SCL	SDA	DDR_A_SA0
	VDDSPD	SA0	
	VPP1	VTT	DDR_A_SA1
	VPP2	SA1	
	GND1	GND2	

DEREN_40-42261-26001RHF
LTC0D09C0D00
ME@

6/16 INTEL suggest

RD160 1 2 0_0402_1%
RD162 1 2 0_0402_1%

+1.2V

ESD@
CD34
100P_0201_25V8J

+DIMM_VREF_DQ

+2.5V

+0.6VS

[7] +0.6V_VREFCA
[7] +0.6V_A_VREFDQ

RD200 1 2 0_0402_5%
RD201 1 2 0_0402_5%

+0.6V_VREFCA_R

20mil

RD10 2_0402_1%

CD21 0.022U_0402_16V7K

RD12 24.9_0402_1%

+1.2V

RD194 1K_0402_1%
RD199 1K_0402_1%

+DIMM_VREF_DQ

+1.2V

RD43 470_0402_1%

DDR_DRAMRST#_R
RD45 1 2 0_0402_5%
DDR_DRAMRST# [7]

+3VS

RD109 10K_0402_5%
RD139 0_0402_5%

DDR_A_SA1

+3VS

RD108 10K_0402_5%
RD138 0_0402_5%

DDR_A_SA0

Interleaved Memory

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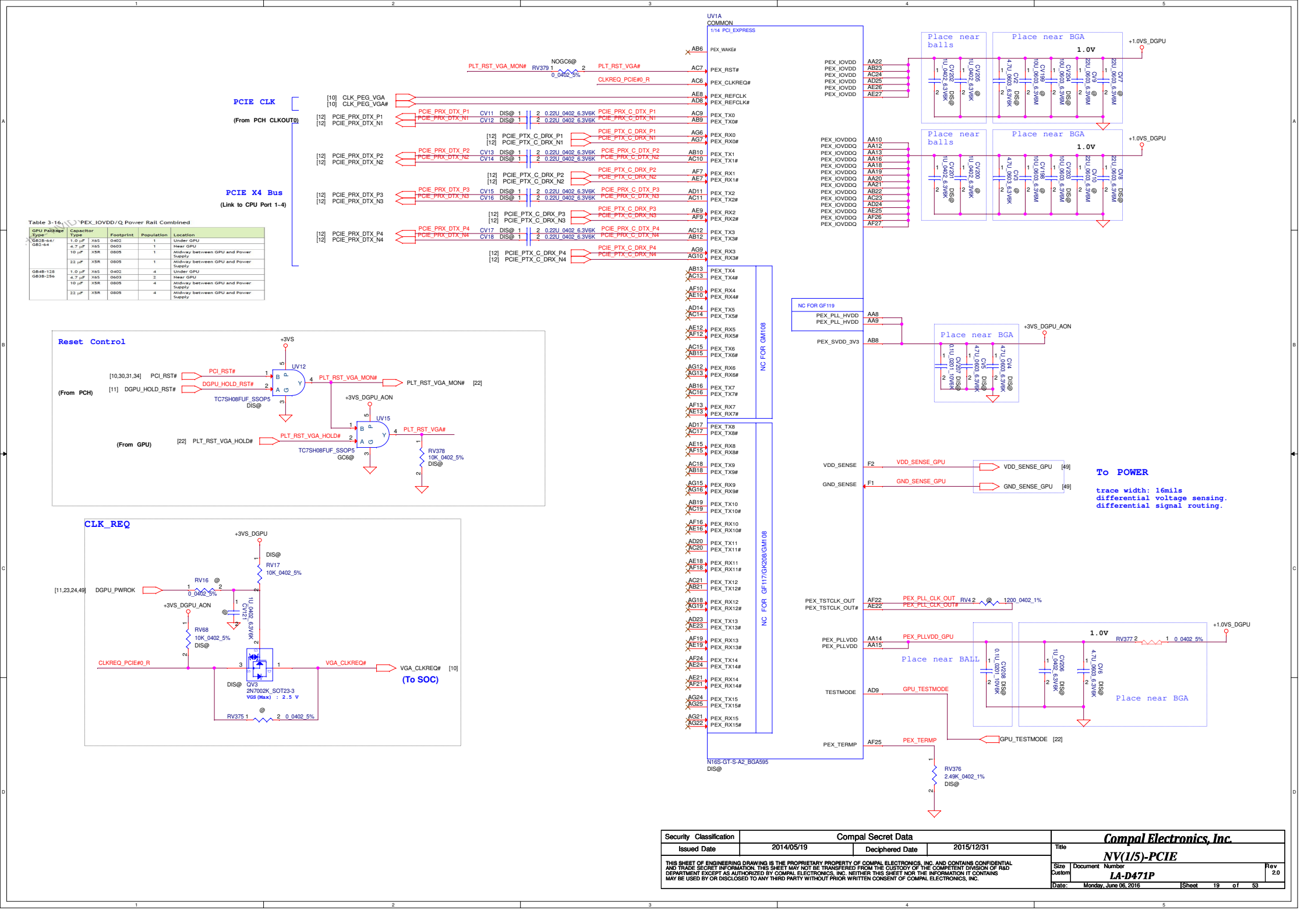

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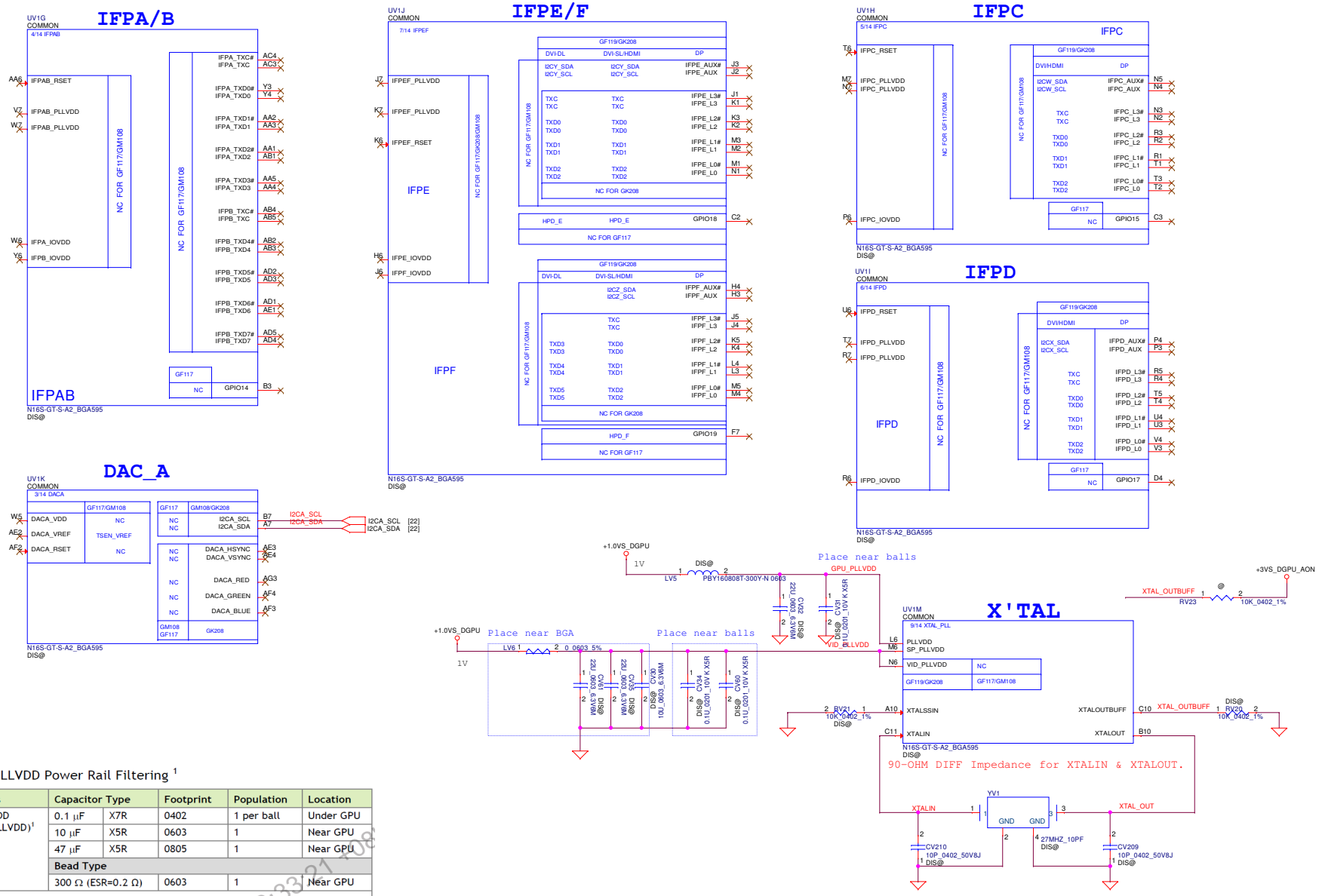

Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 μF	X7R	0402	1 per ball	Under GPU
		10 μF	X5R	0603	1	Near GPU
		47 μF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.

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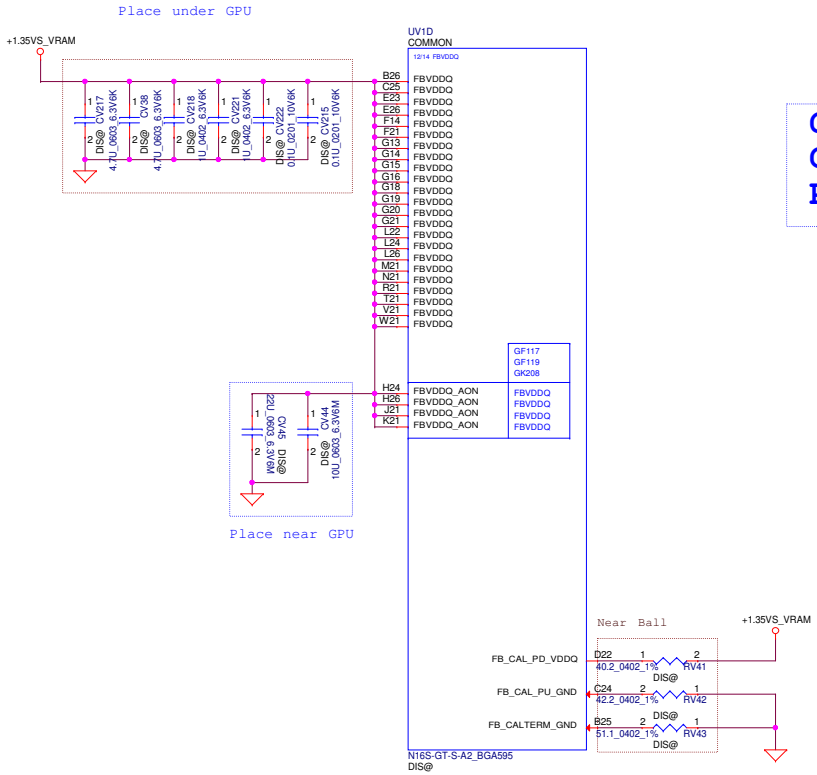
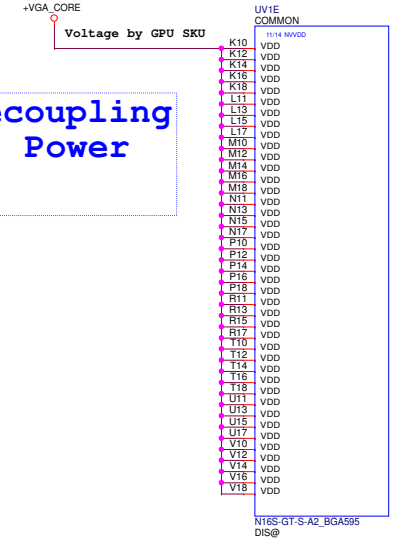
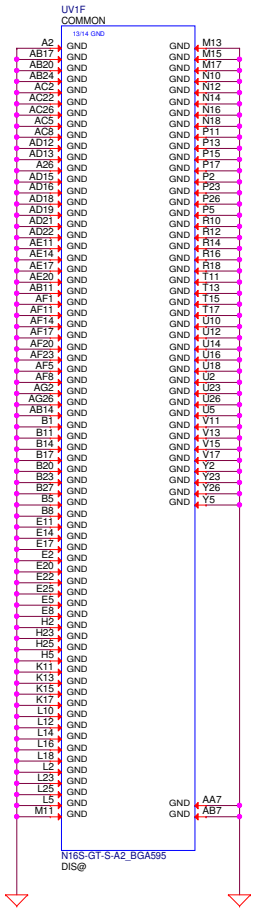
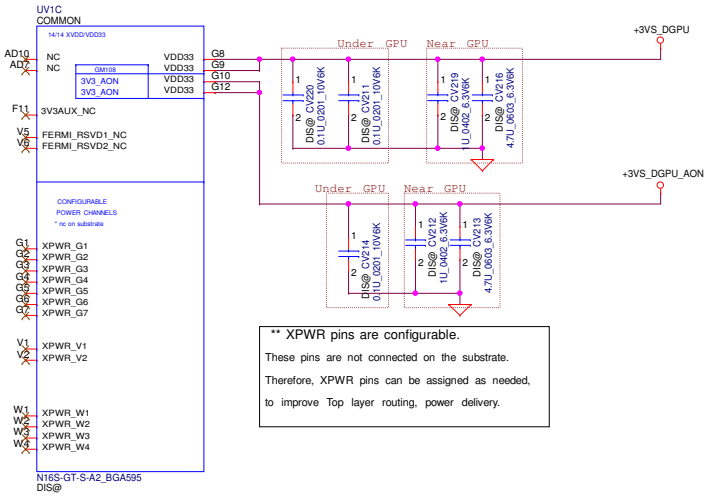
GPU_Decoupling CAPs @ Power Page









** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed,

to improve Top layer routing, power delivery.

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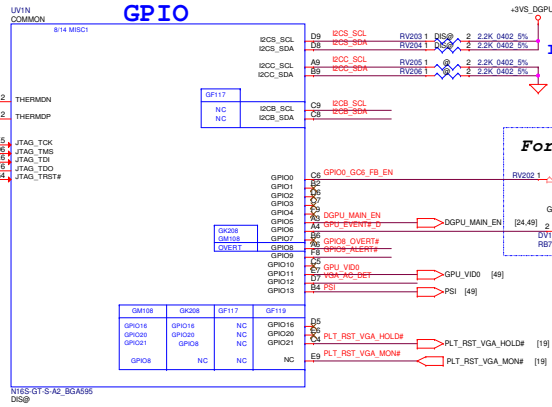
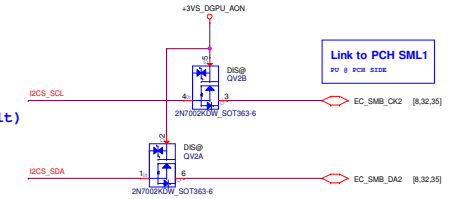
GPIO

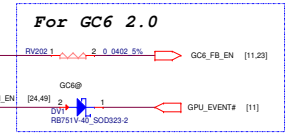
Internal Thermal Sensor

VGA_THERMDN and VGA_THERMDP:
1. 5mil track width and spacing
2. 5mil grounded gurad tracks width and spacing
3. ground referenced
4. Connect guard tracks to pin5

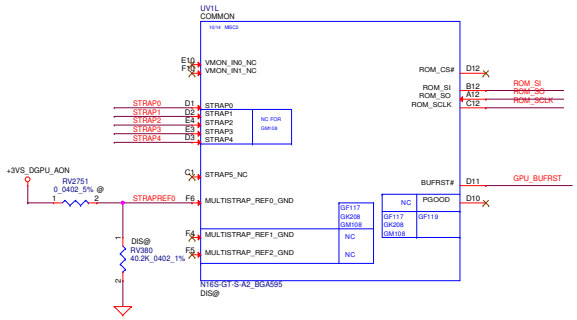


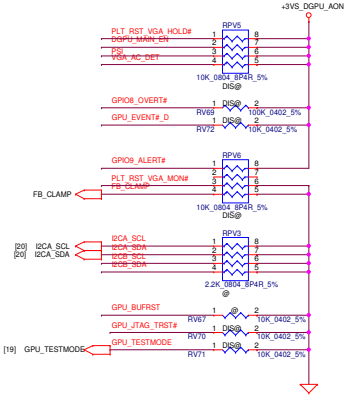
I2CS SMBUS: 0x96 and 0x9E(Default)

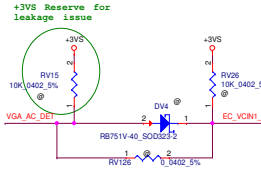


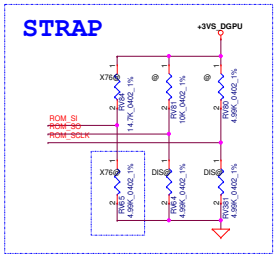


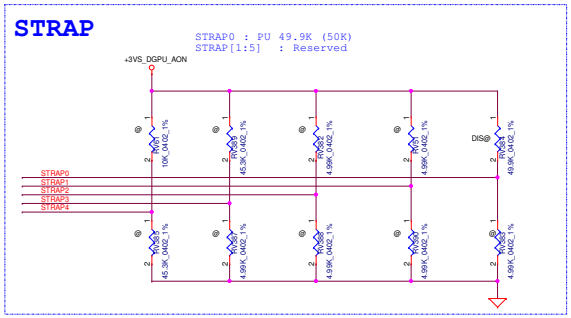
Item	N16P-GT	N16S-GT-B/S
Device ID	0X139A	0x1347
Package	GB4B-128	GB4B-128/GB2B-64
Internal P/N	GM107-750,28nm	GM108-755/655,28nm
ROM_SI	Refer to N16x_RAM_Straps table	Refer to N16x_RAM_Straps table
ROM_SO	0x0000, 4.99Kohm pull down	0x0000, 4.99Kohm pull down
ROM_SCLK	0x0 for Optimus, 4.99Kohm pull down	0x0 for Optimus, 4.99Kohm pull down
Strap0	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)
Strap1	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
Strap2		
Strap3		
Strap4		
Open_VRG SKU	B	B
NVVDD Boot Voltage	0.9V	0.9V











10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful I²CS Slave addresses can be used with SMB_ALT_ADDR strapping.

From EC

RAM_CFG[3:0] (ROM_SI)	BAX40
0x9 (PU 10K)	
0xA (PU 15K)	
0xB (PU 20K)	
0x3 (PD 20K)	
0x4 (PD 24.9K)	
0x5 (PD 30.1K)	
0x1 (PD 10K)	S2G
0x2 (PD 15K)	H2G
0x3 (PD 20K)	
0x4 (PD 24.9K)	
0x5 (PD 30.1K)	
0xF (PU 45.3K)	
0xE (PD 34.8K)	

Table 4. N16S-GM/-GT/-LP DDR3L Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC2G63FFR-11C	F-die	0x9	900	N/A	Production ready
				Micron	MT41J128M16JT-093G:K	K-die	0xA	900	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0xB	900	N/A	Production ready
		256Mx16	Single Rank or Single Rank Stuffing for Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x1	900	N/A	Post production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0x2	900	N/A	Post production ready
			Dual Rank	Hynix	H5TC4G63AFR-11C	A-die	0x3	900	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x4	900	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x5	900	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0xF	900	N/A	Post production ready
				Hynix	H5TC4G63CFR-N0C	C-die	0xE	900	N/A	Post production ready

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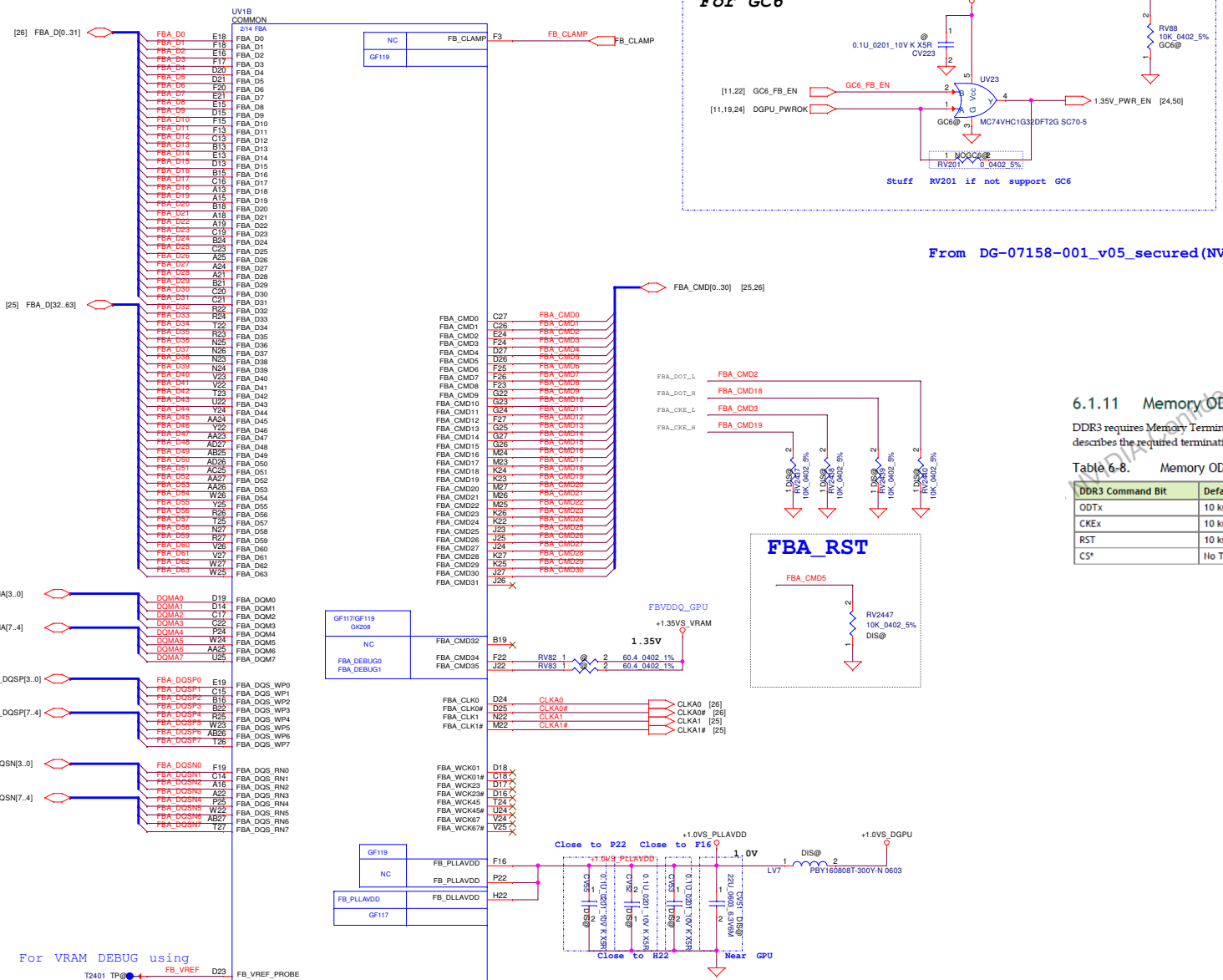

6.1.11 Memory ODTx, CKEx, and RST Termination

DDR3 requires Memory Termination on CKEx, ODTx, and Memory Reset (RST). Table 6-8 describes the required termination.

Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 kΩ
CKEx	10 kΩ
RST	10 kΩ
CS*	No Termination

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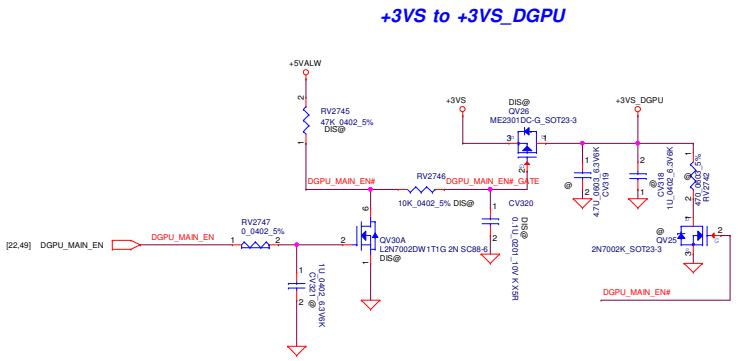
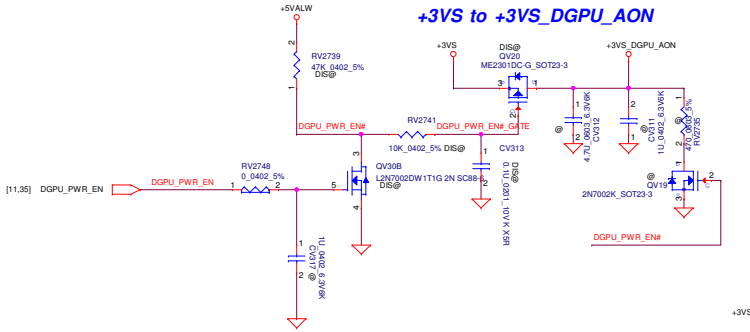
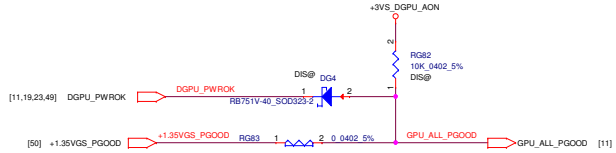
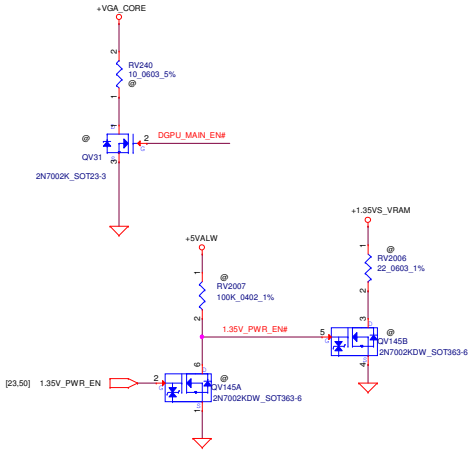








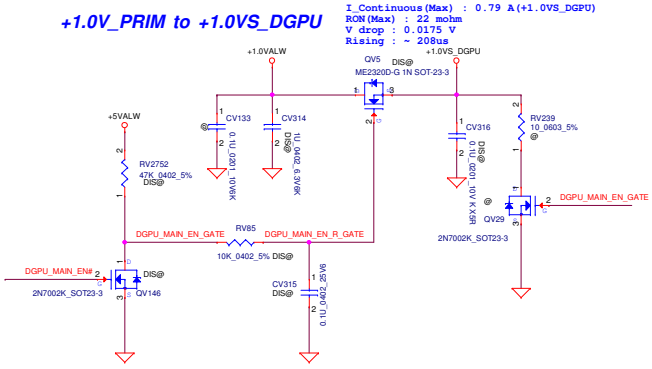


Table 5. EDP-Continuous [3]

Products	VRM Type	GPU Core	GPU FBIO		FB Total [1, 5]		1.05V Total [2]	3.3V Total
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GT	DDR3/L	26	1.37	1.33	2.32	2.12	0.79	0.06
N16S-GM	DDR3/L	20	1.37	1.31	2.32	2.05	0.79	0.06
N16S-LP	DDR3L	16	N/A	1.29	N/A	2.05	0.79	0.06

Only For N16S-GT(GB2B-64)

Table 3-15. PCI Express Power Rails Specification

GPU Package	Power Rails	Voltage	Transient Noise
GB2-64/ GB2B-64	PEX_IOVDD/Q and	1.05 V ± 30 mV or	100 mV pk-pk within 20 MHz (1.05V) or
	PEX_PLLVDD	1.0 V ± 15mV	70 mV pk-pk within 20 MHz (1.0V)

Table 3-7. Power Rail Specification for DDR3 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDDQ/FBVDD	1.5 V (DDR3) or 1.35V (DDR3L)
DC tolerance	± 3%
AC tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW

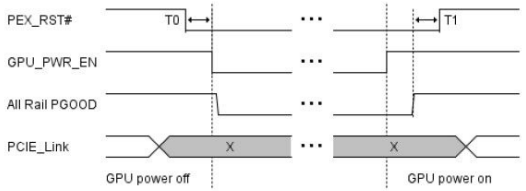
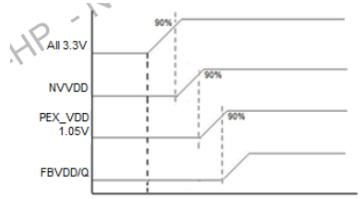


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

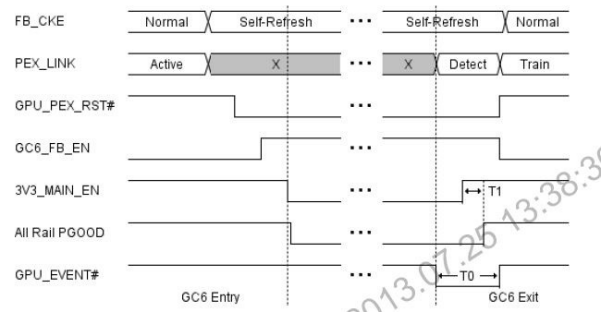


Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

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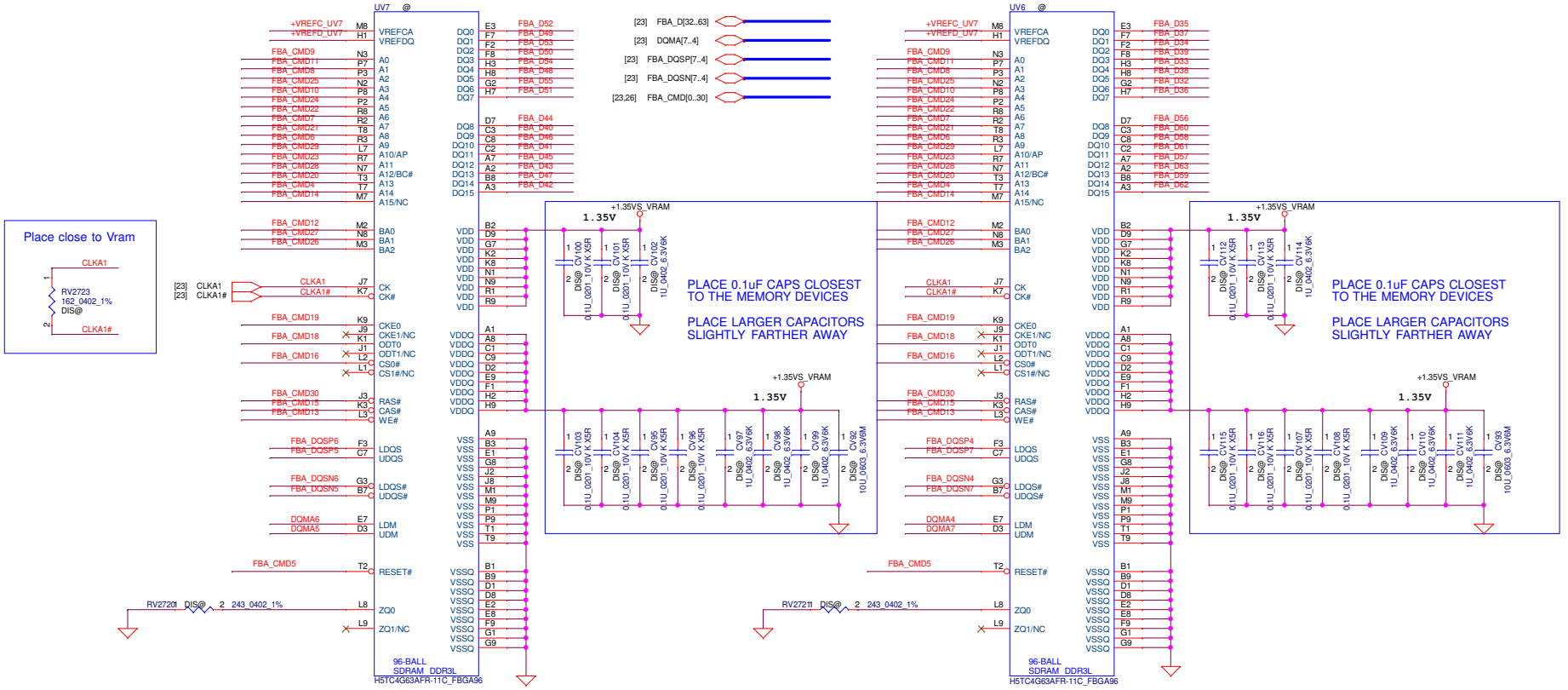
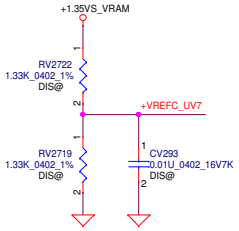
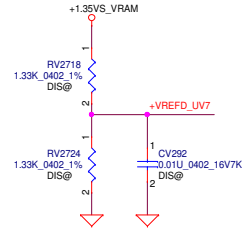
Memory Partition A - Upper 32 bits [64..32]







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Memory Partition A – Lower 32 bits [31..0]

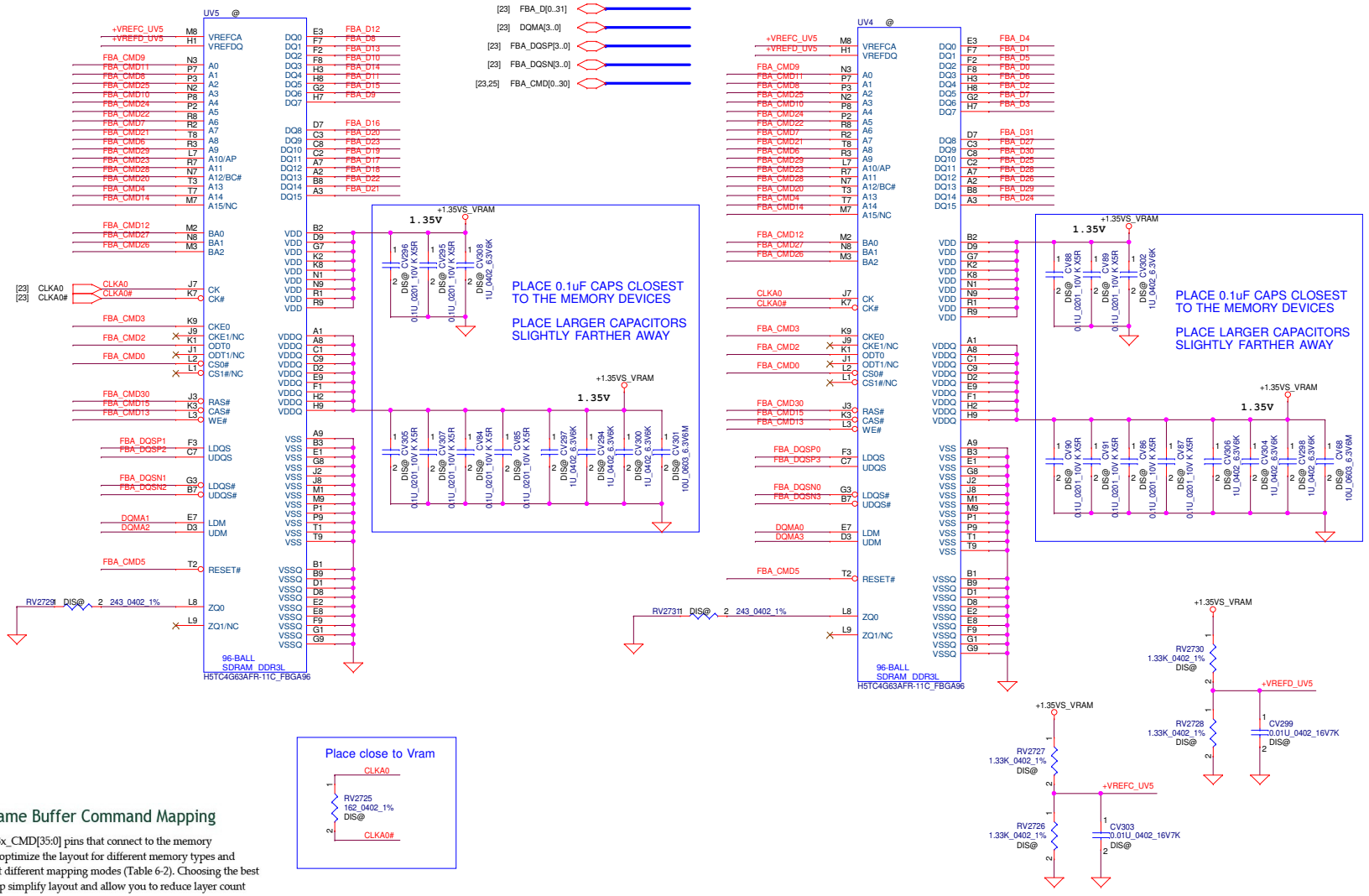
Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

Table 6-3. Mode D Command Mapping

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11



6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for N15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers[1]. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

Note: [1]Not including two additional layers for power planes.

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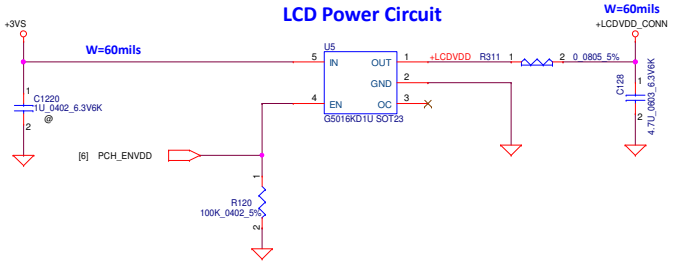
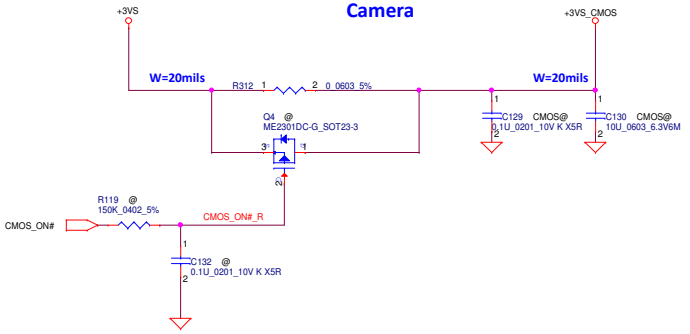
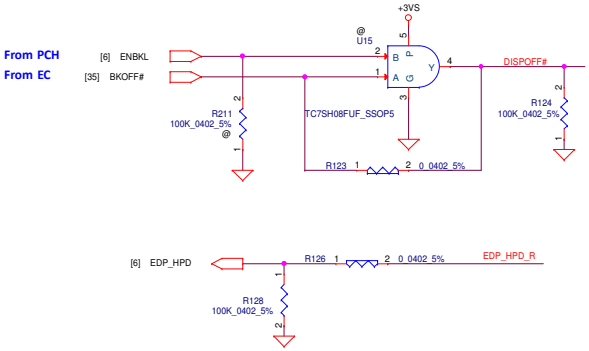
LCD Power Circuit



Camera





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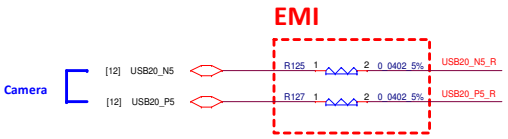
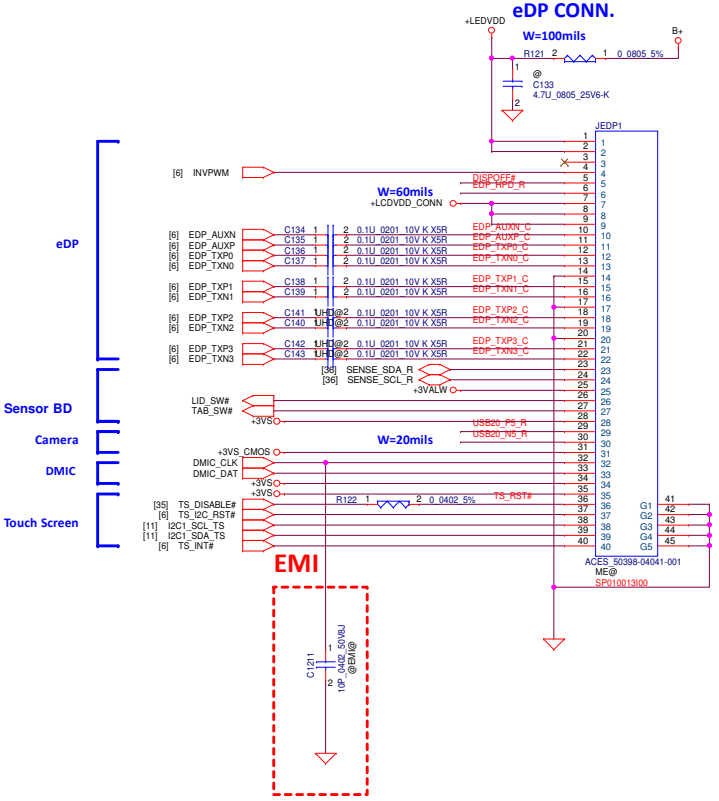


eDP CONN.



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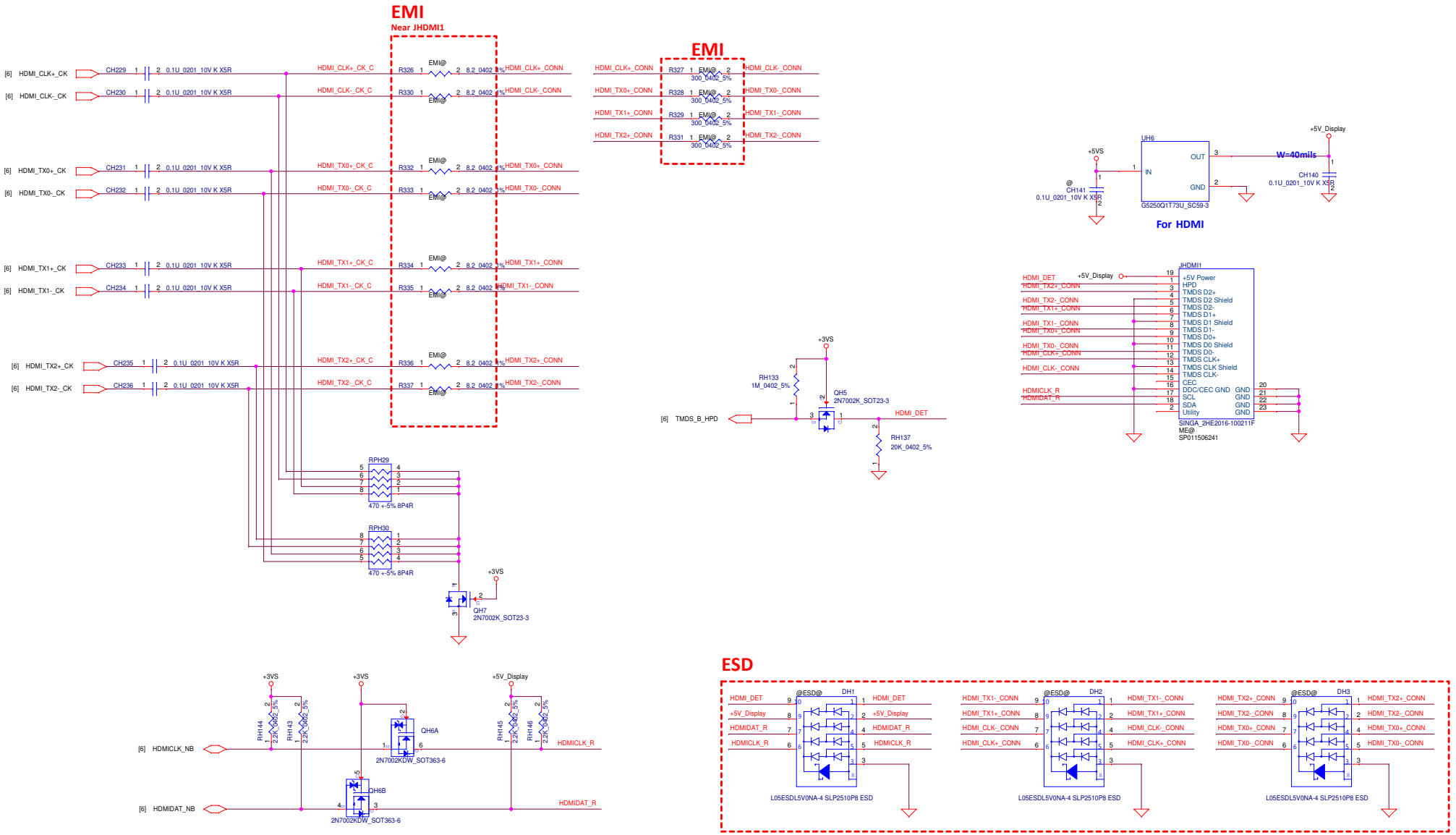

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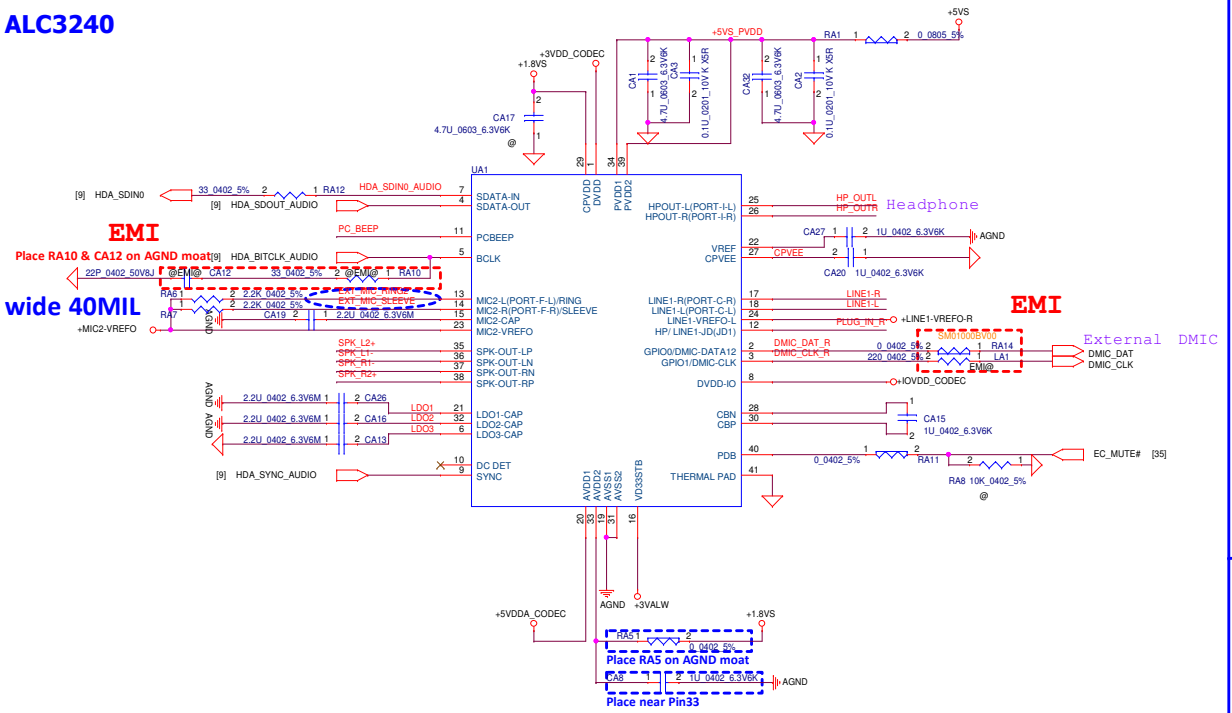
ALC3240



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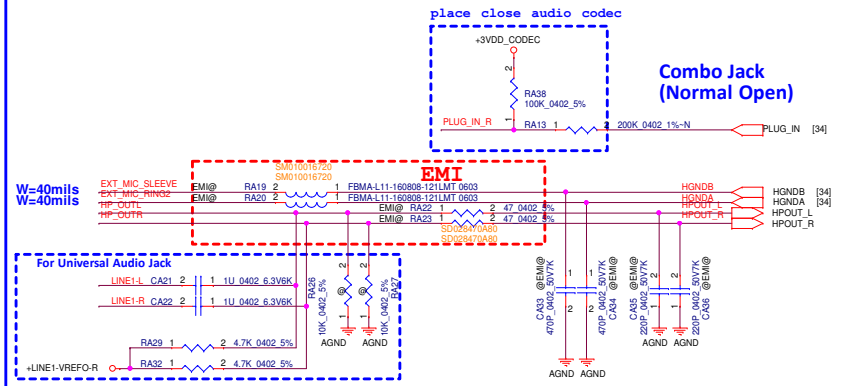

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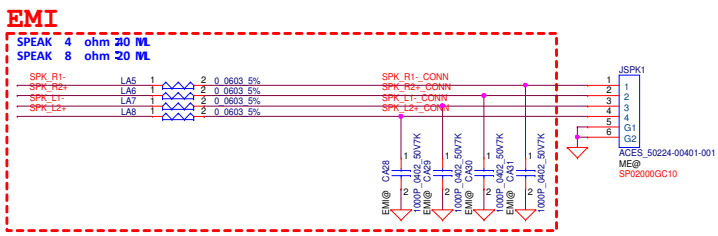
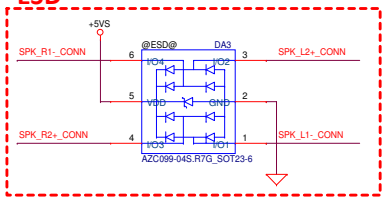


ESD protection needs to be placed near connector side



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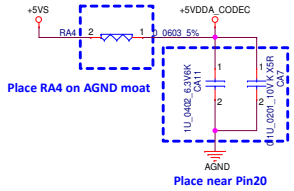


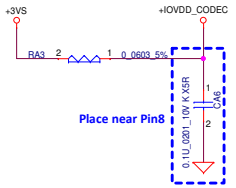
Each Platform Power Net Support List:

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

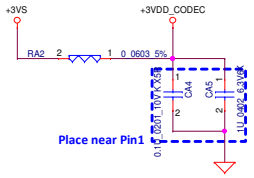
Each Platform HDA Link Voltage Support (Pin 8):

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

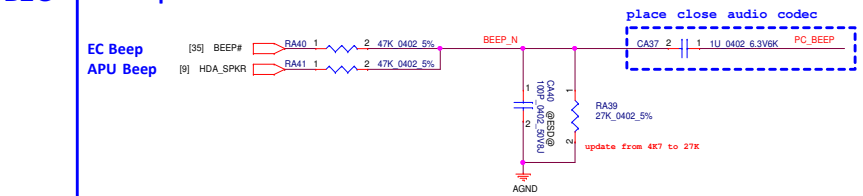
+3VS → +IOVDD_CODEC



+3VS → +3VDD_CODEC



PC Beep



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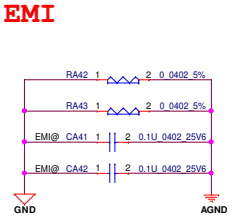

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Compal Electronics, Inc.	
Title	HD Audio Codec_ALC3240
Size C	Document Number LA-D471P
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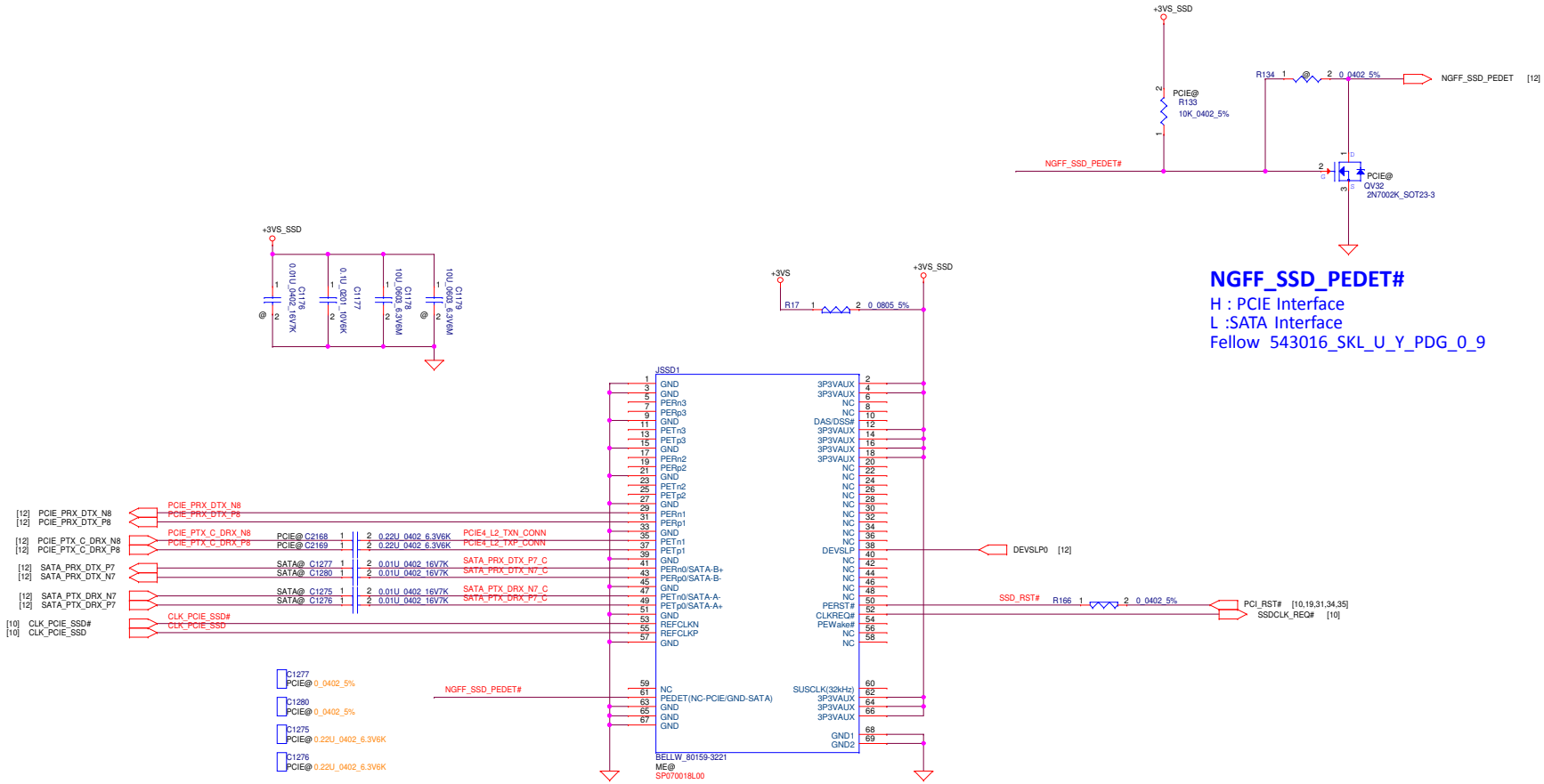
SSD



NGFF_SSD_PEDET#

H : PCIE Interface

L :SATA Interface

Fellow 543016_SKL_U_Y_PDG_0_9

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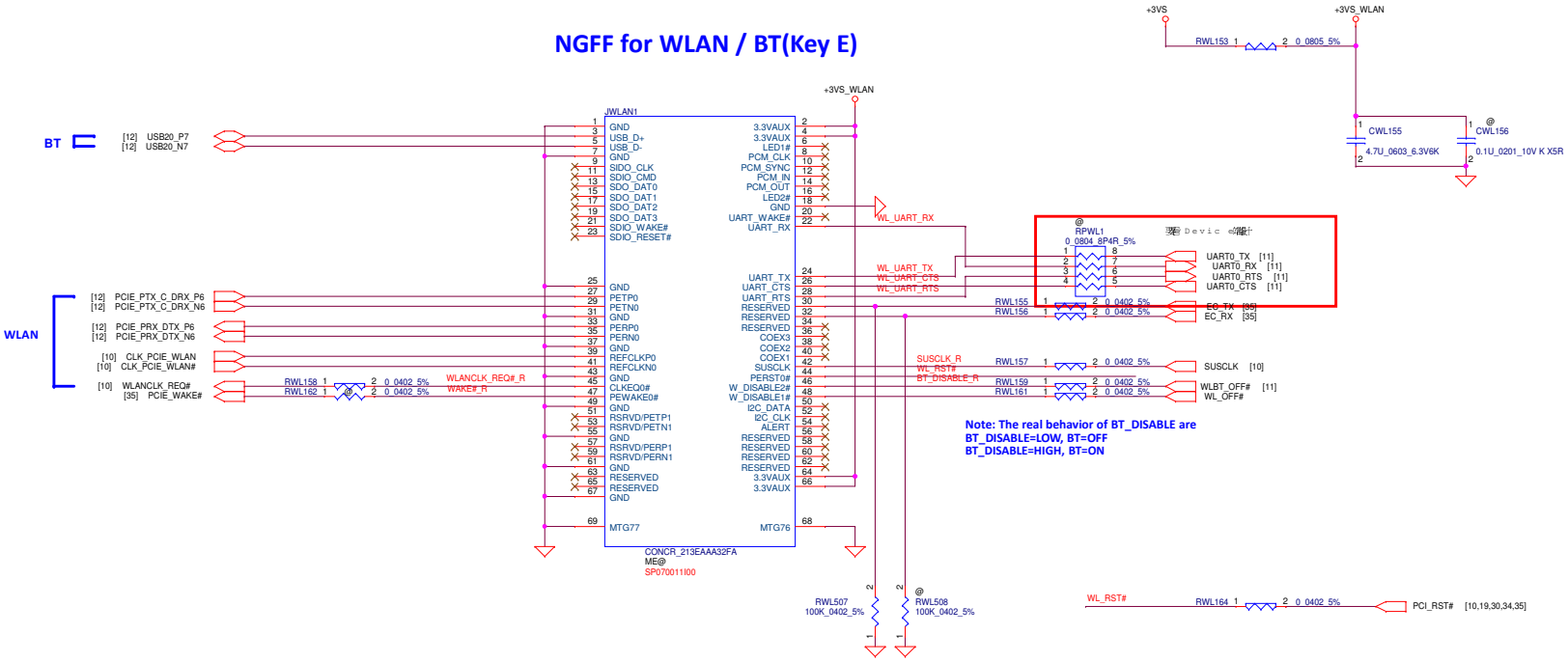
NGFF for WLAN / BT(Key E)



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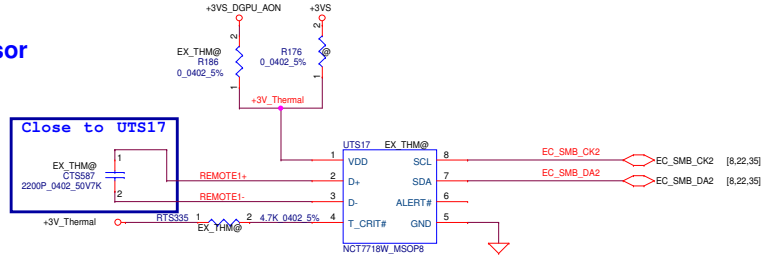
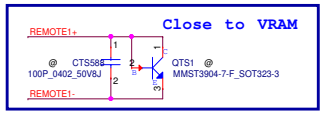
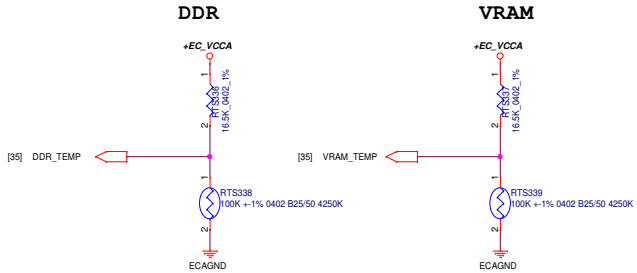
Thermal Sensor

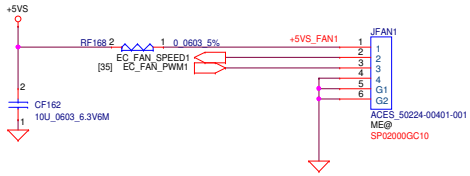


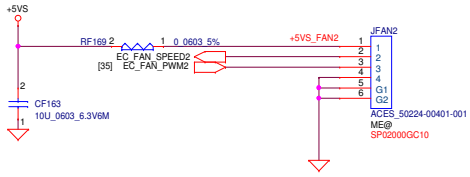
SMB Address: 1001100x

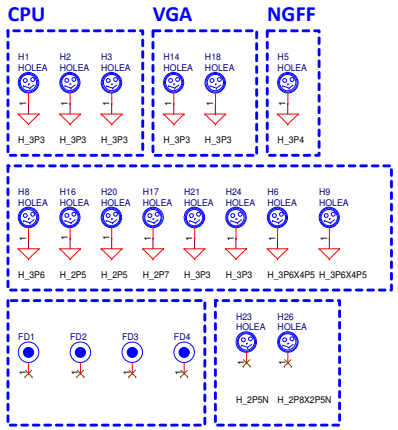
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

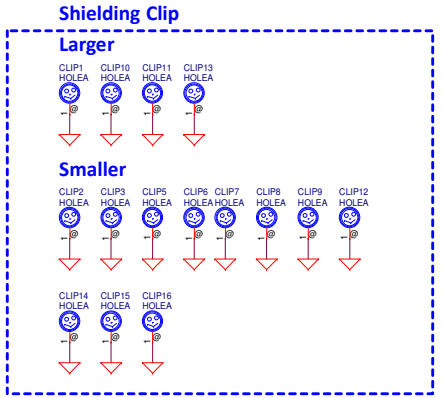












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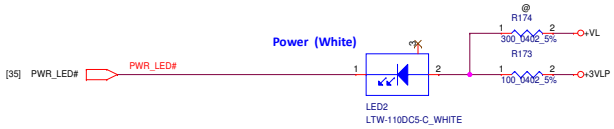
Power But t on LE D



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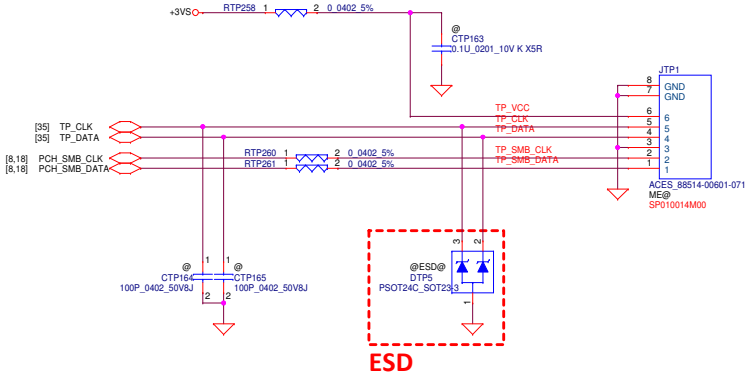

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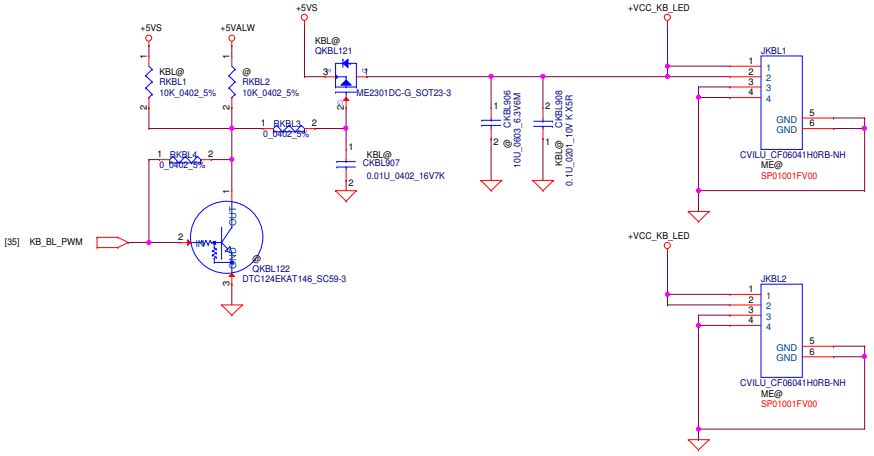
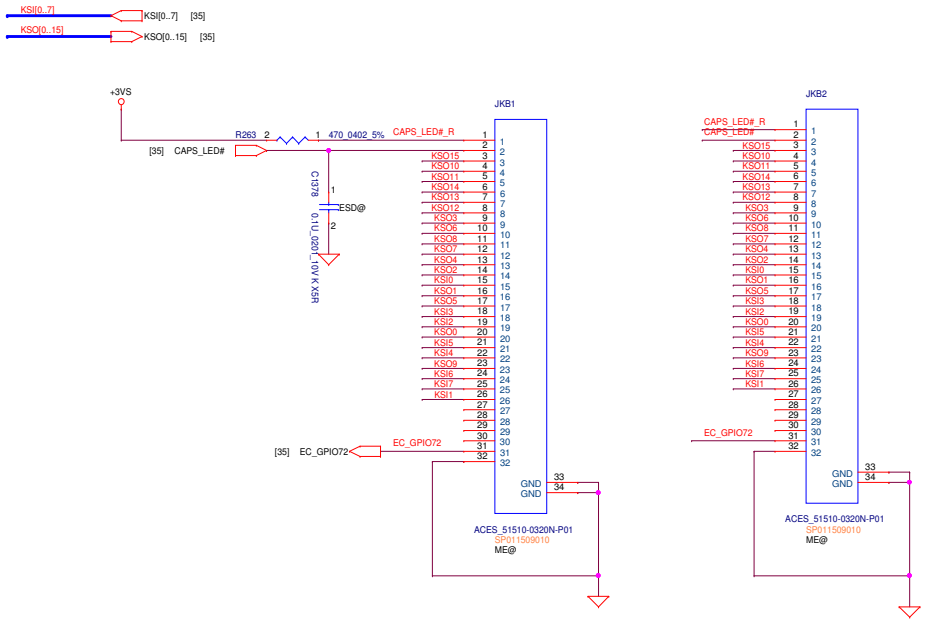


Keyboard



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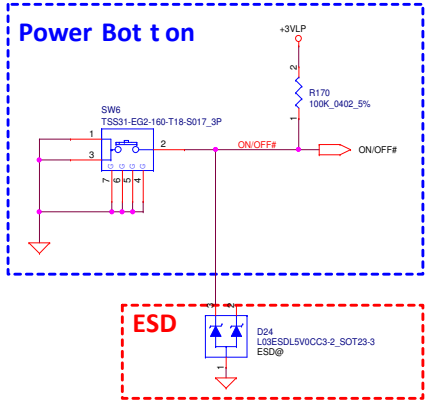

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Compal Electronics, Inc.			
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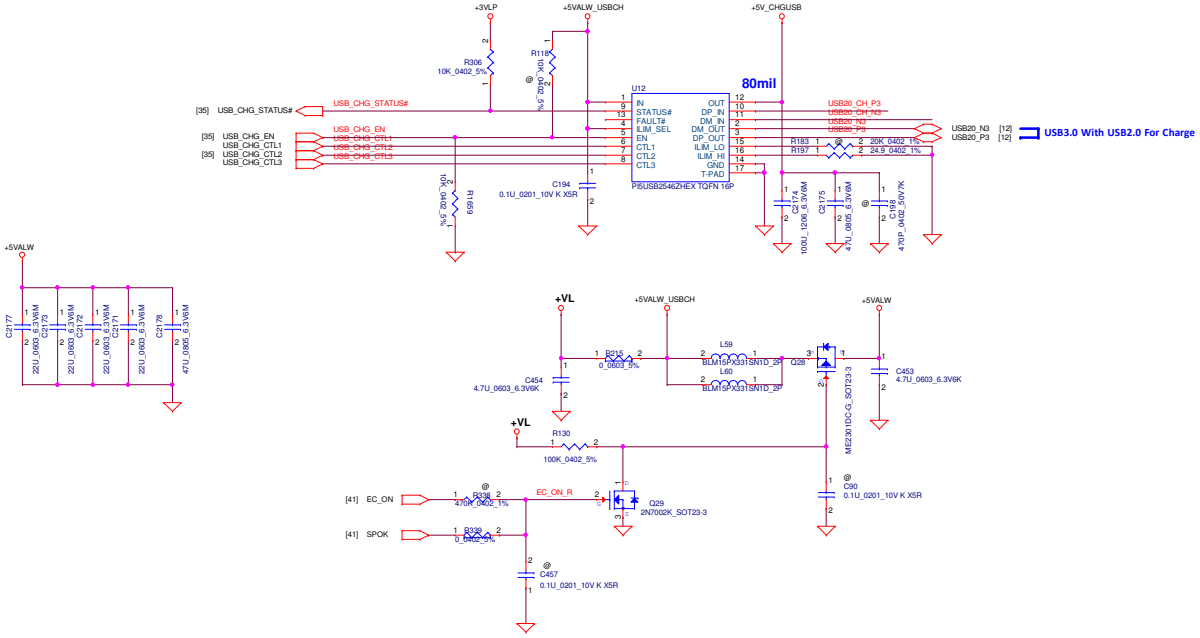
USB Charge



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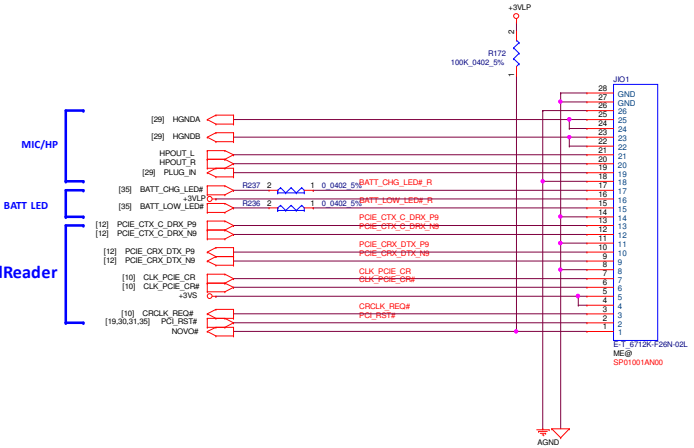

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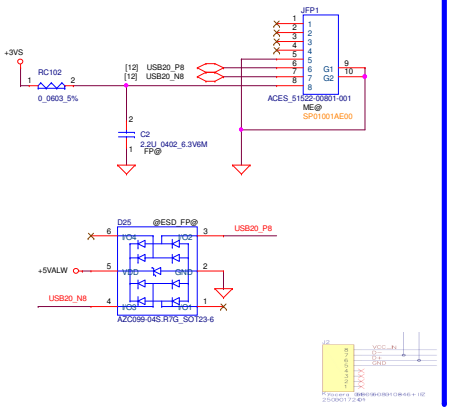

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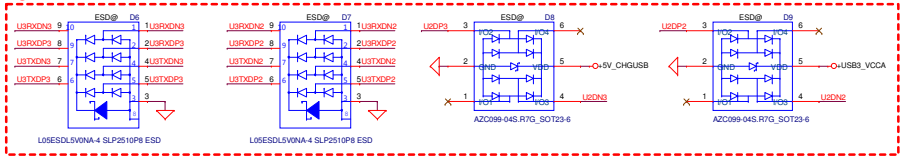
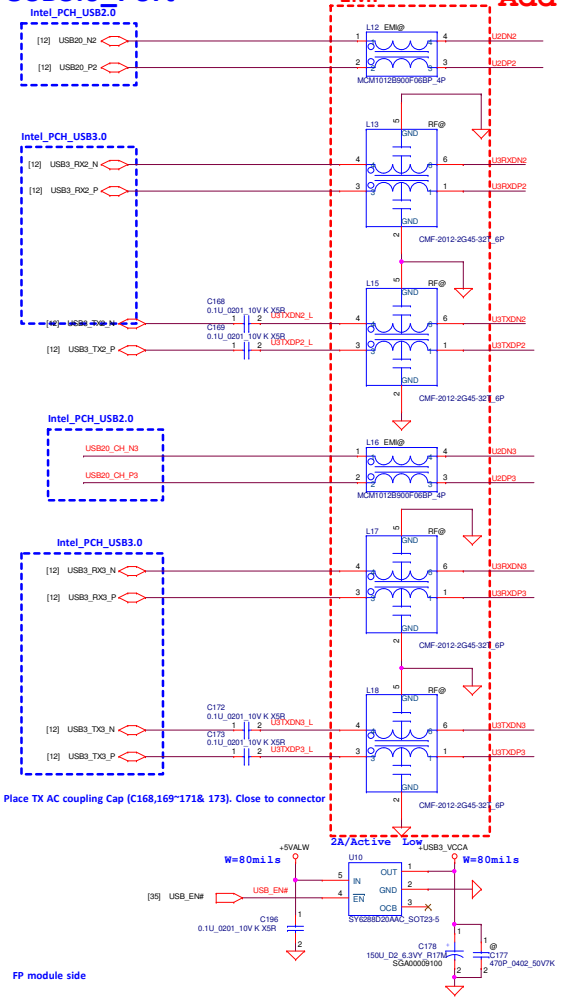
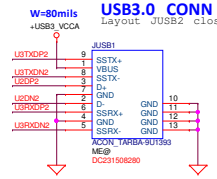


USB3.0_Port



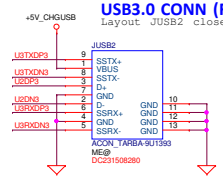
USB3.0 CONN

Layout JUSB2 close HDMI



USB3.0 CONN (For Charge)

Layout JUSB2 close EDP



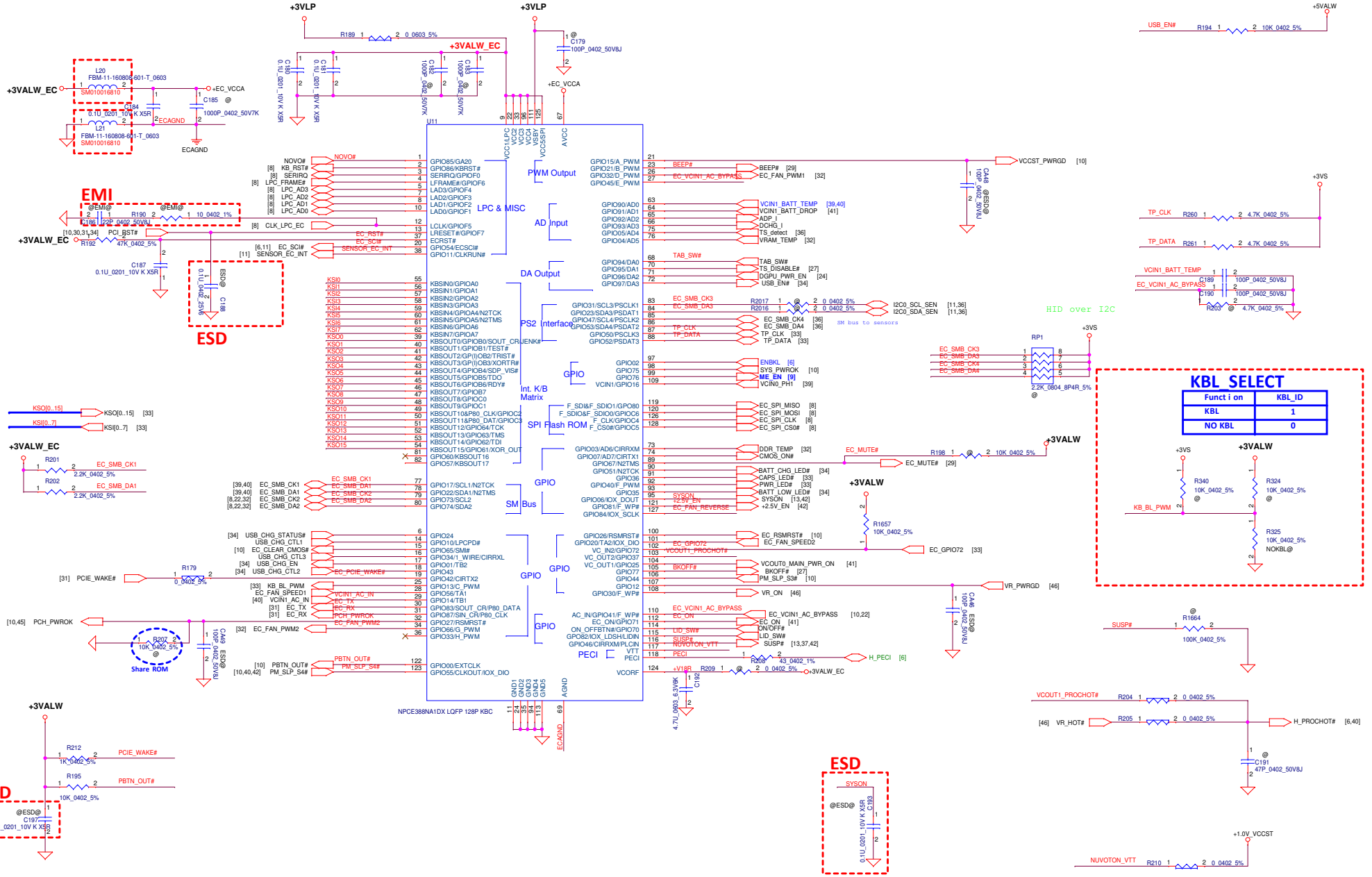
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: USB2 / USB3 / FP / IO Board

Size: Custom | Document Number: LA-D471P | Rev: 2.0

Date: Monday, June 06, 2016 | Sheet 34 of 53



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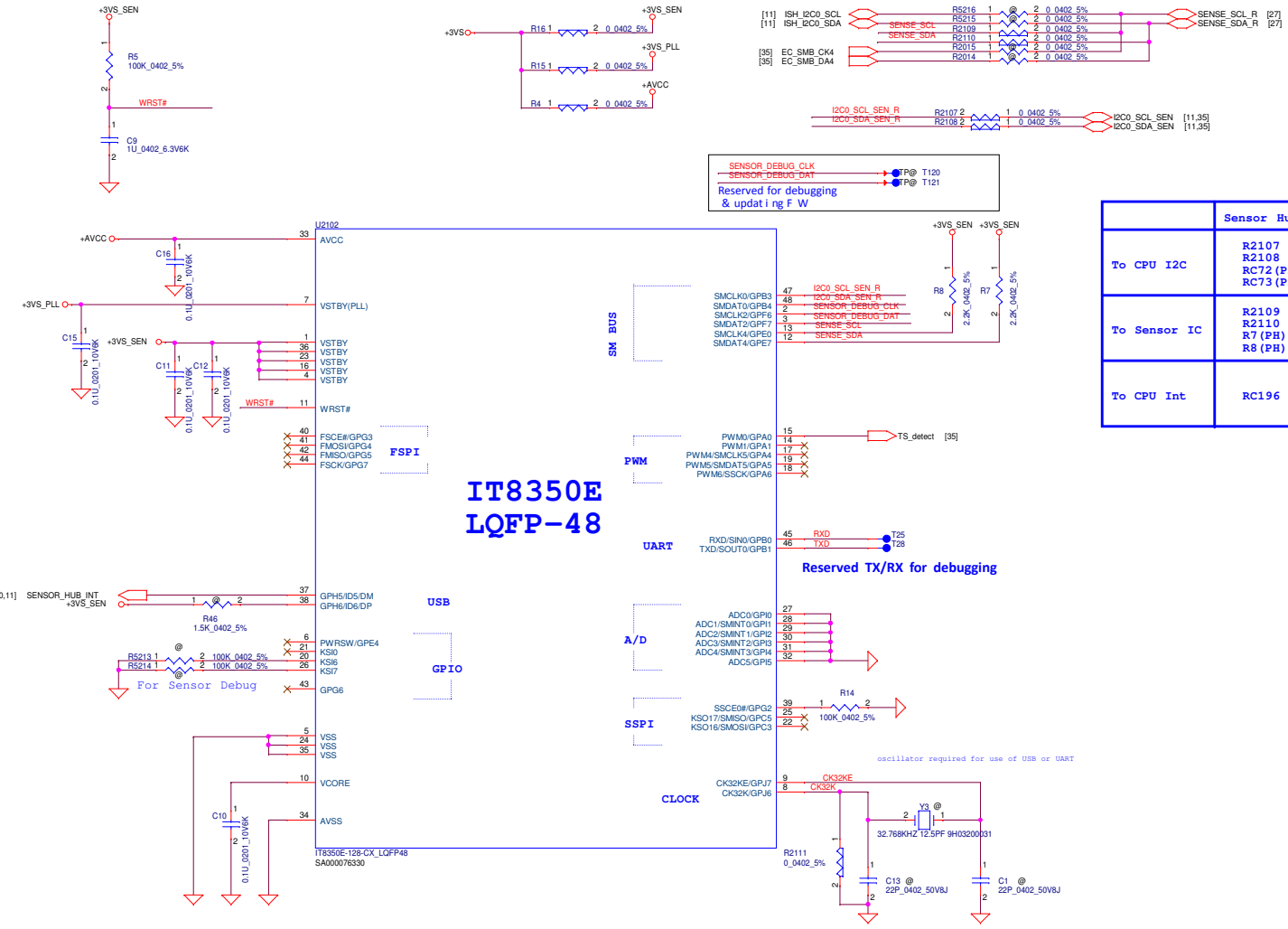
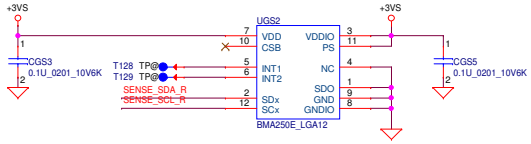
Sensor Hub



	Sensor Hub	EC	Intel Sensor Hub
To CPU I2C	R2107 R2108 RC72(PH) RC73(PH)	R2016 R2017 RP1(PH)	NC
To Sensor IC	R2109 R2110 R7(PH) R8(PH)	R2014 R2015 RP1(PH)	R5215 R5216 RC86(PH) RC88(PH)
To CPU Int	RC196	RC205	Test Point

G-Sensor x1



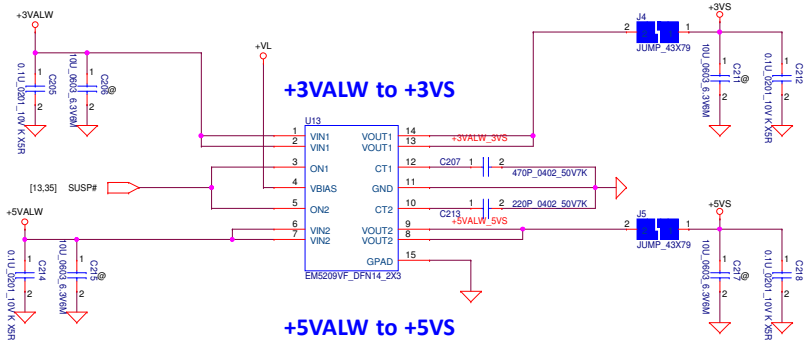
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

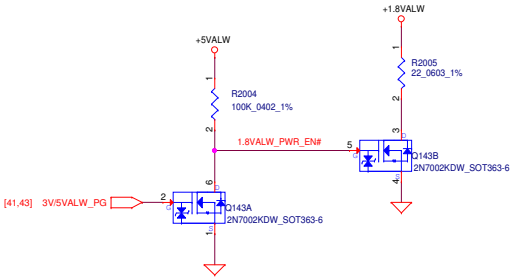
Title: LAN_RTL8111H / RTL8107E

Size	Document Number	Rev
C	LA-D471P	2.0

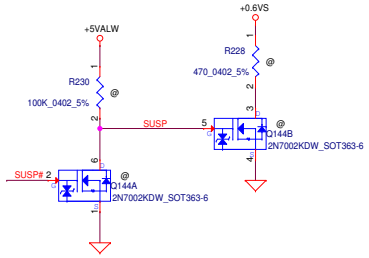
Date: Monday, June 06, 2016 | Sheet 36 of 53



For +1.8VALW Discharge



For +0.6VS Discharge



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: DC to DC

Size	Document Number	Rev
C	LA-D471P	2.0

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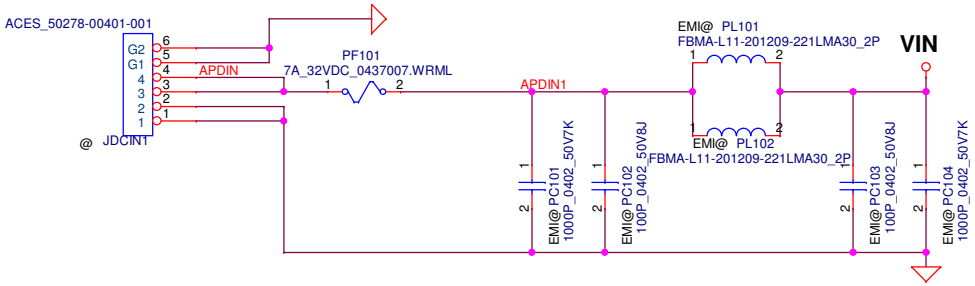
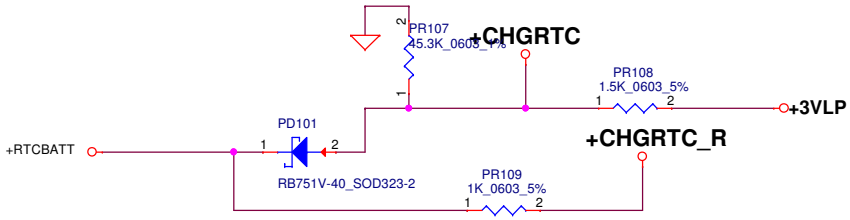


ADP_ID

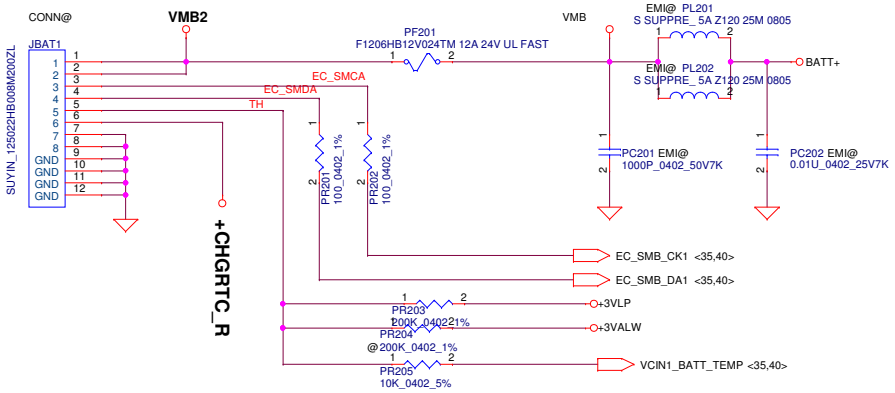
AC Adapter	65W	45W
R(ohm)	287	118
ADP_ID(V)	0.913	0.448
Detection voltage	0.693~1.134	0.234~0.663



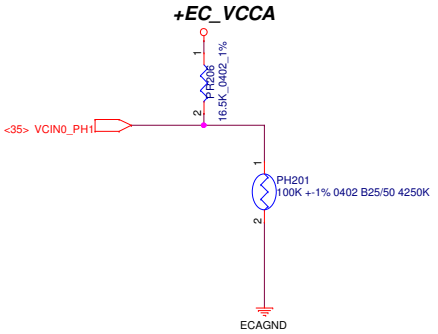
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Title: **PWR- DCIN / Vin Detector**

Size: B	Document Number	Rev: 2.0
Date: Monday, June 06, 2016	Sheet 38 of 53	



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



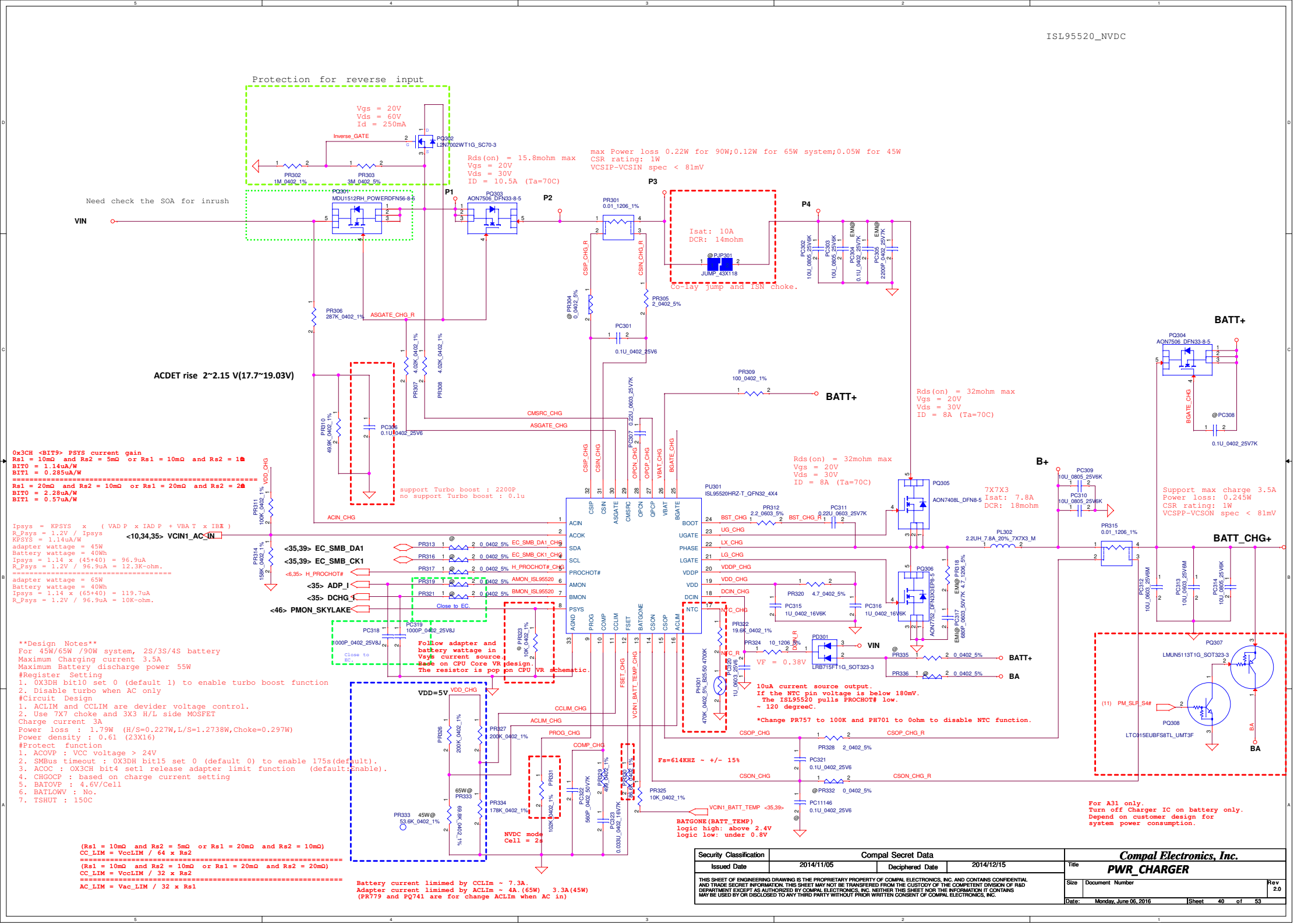
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	SKL	2.0

Date: Monday, June 06, 2016 Sheet 39 of 53



Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

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Compal Electronics, Inc.

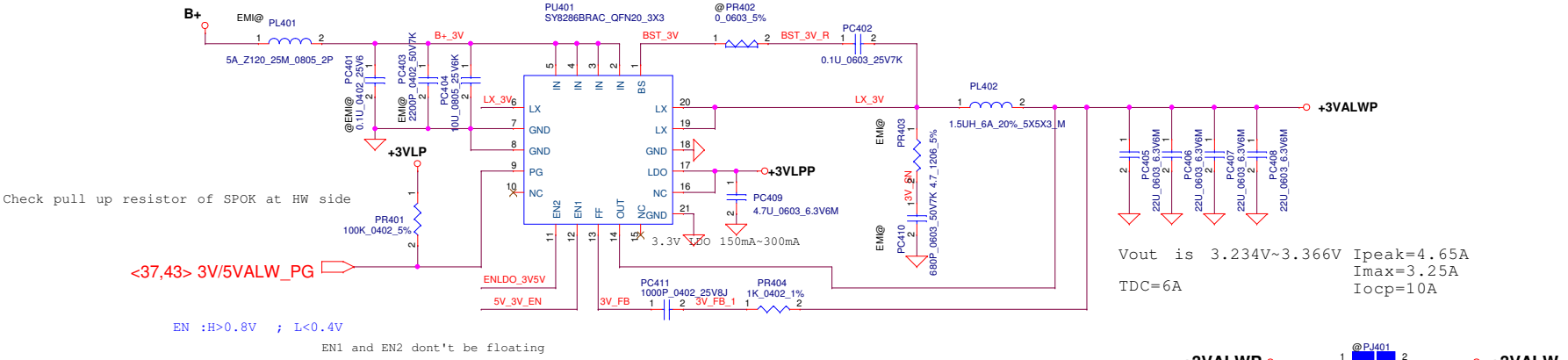
Title: **PWR_CHARGER**

Size	Document Number	Rev
		2.0

Date: Monday, June 06, 2016 Sheet 40 of 53

Module model information

SY8286B_V1.mdd

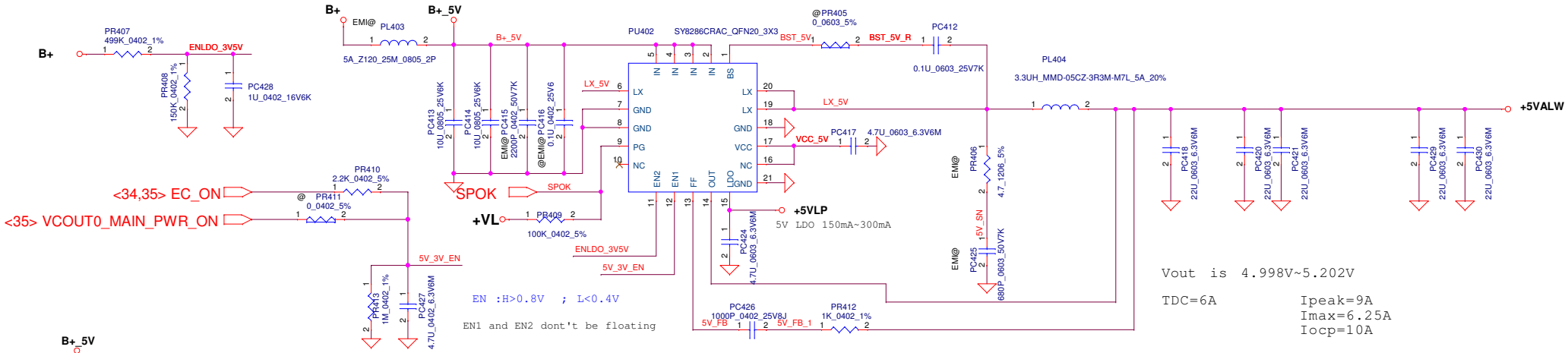


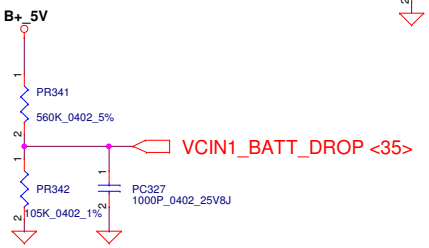
+3VALWP — @PJ401 JUMP_43X118 — +3VALW

+3VLPP — @PJP402 JUMP_43X39 — +3VLP

Module model information

SY8286C_V1.mdd





+5VLP — @PJP404 JUMP_43X39 — +VL

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: PWR- 3VALW/5VALW-SY8286B&C

Size	Document Number	Rev
Custom		2.0

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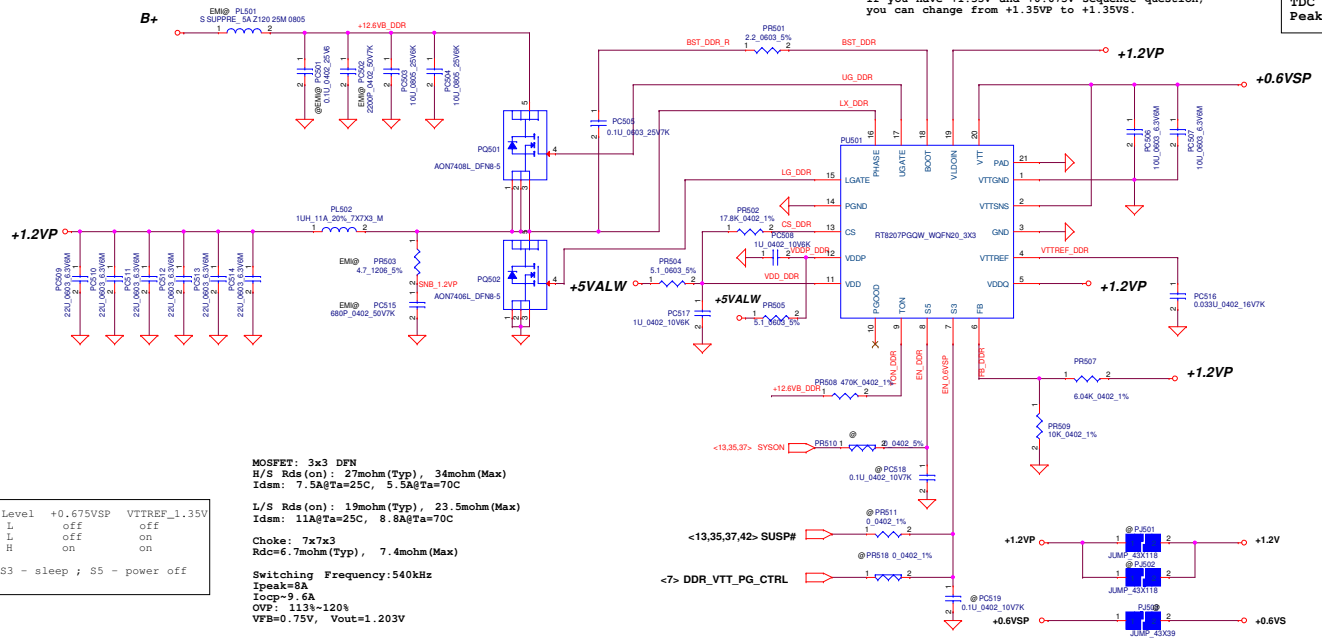
Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 19mohm(Typ), 23.5mohm(Max)
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

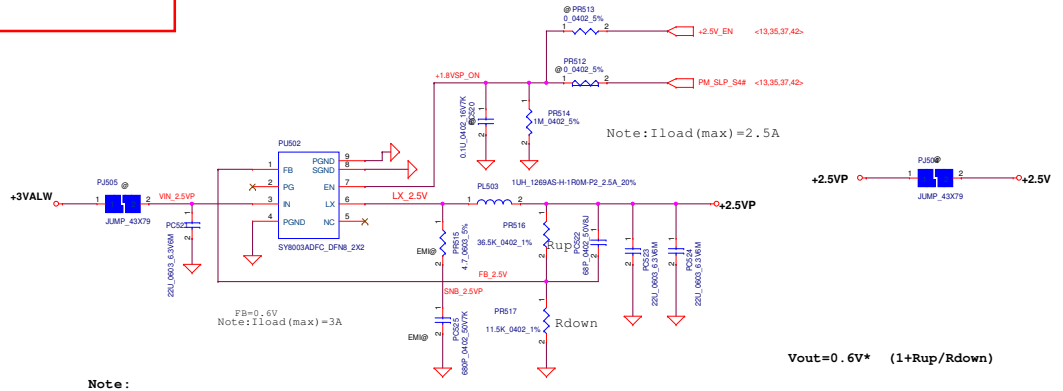
Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp=9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.203V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Module model information
SY8003A_V1.mdd



Vout=0.6V* (1+Rup/Rdown)

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: +1.2VP/+0.6VSP/+2.5VP

Size	Document Number	Rev
Custom	LA-D471P	2.0

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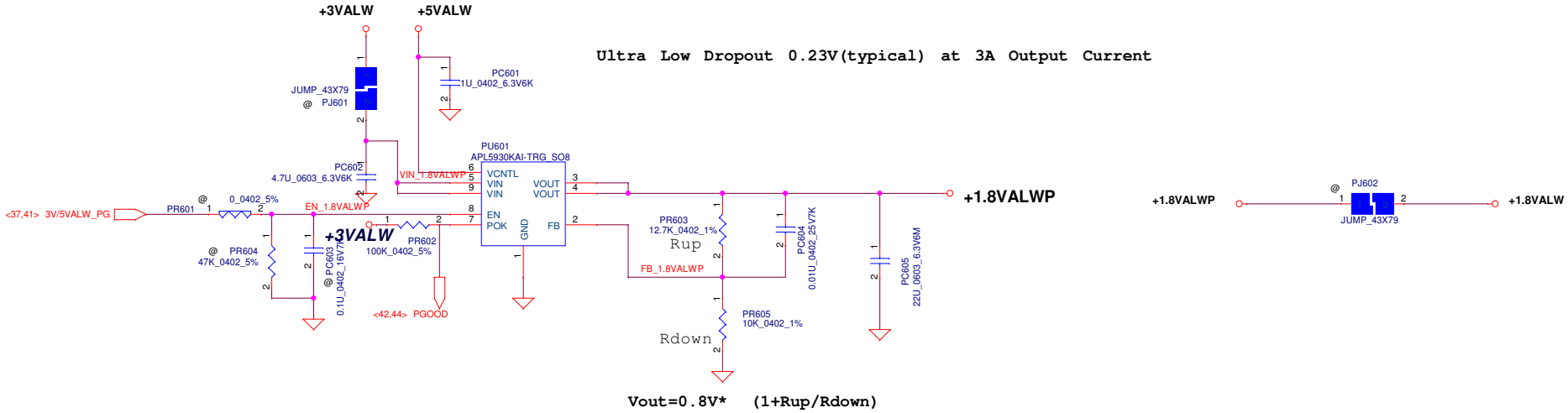
Module model information

APL5930_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: +1.8V_PRIM

Size: Custom | Document Number | Rev: 2.0

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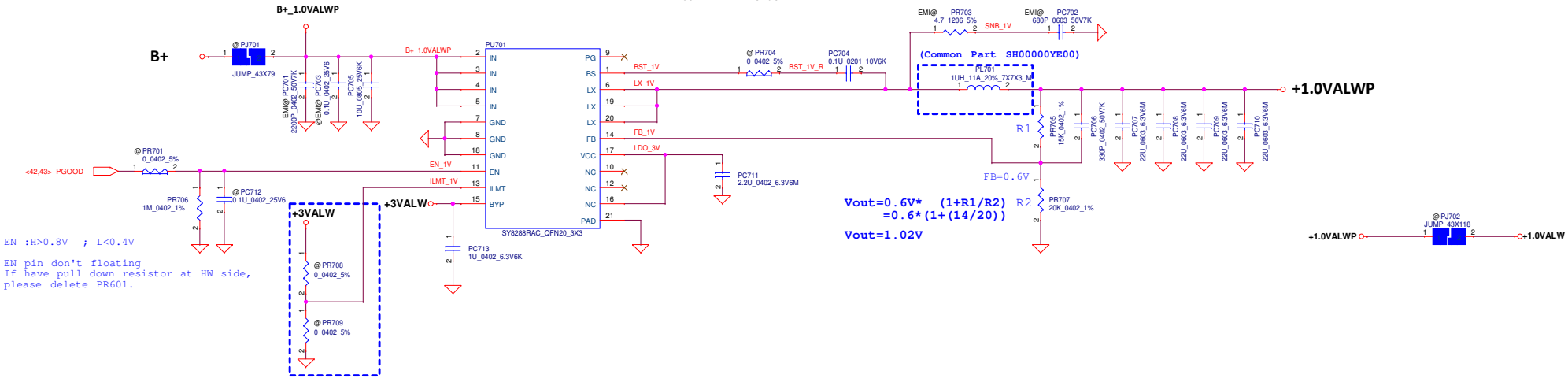
Module model information

SY8288_V1.mdd

Confirm HW side



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: +1.0VS

Size	Document Number	Rev
C	Z_SKL	2.0

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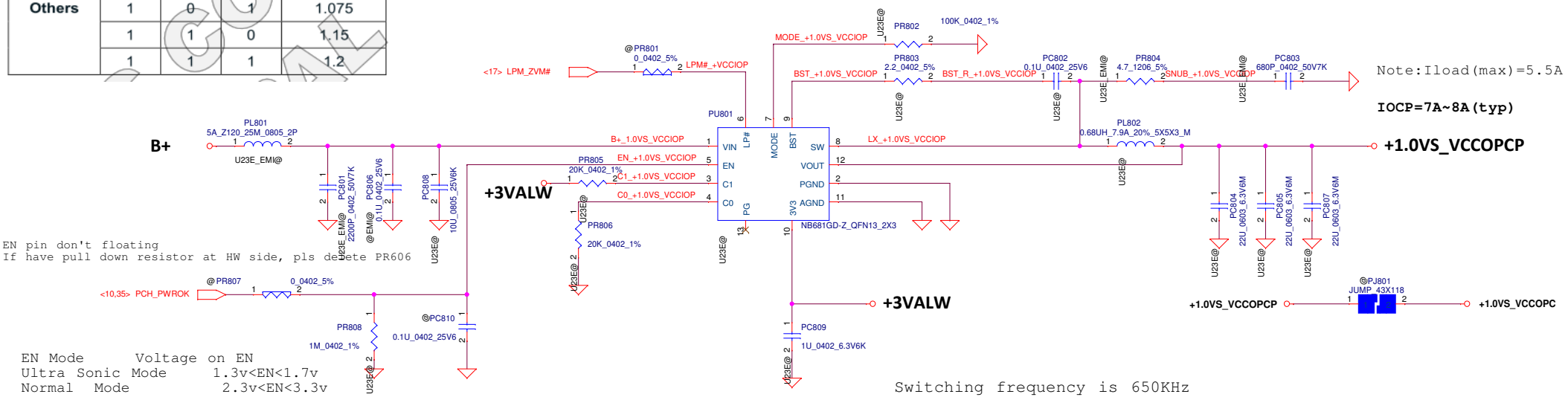
Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

Module model information

NB681_V1.mdd



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Title: +1.0VS_VCCOPC

Size: Custom | Document Number | Rev: 2.0

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CPU CORE

Due to U23e VCC_GT and GTX merged current spec is TBD in PDDG.
Please confirm FAE the setting of PRI23, PRI39 PRI63 for U23e GT and GTX merged.

Module model information

NCP81208_U2223E_COLAY_V1A.mdd for IC portion

NCP81208_U2223E_COLAY_V1B.mdd for SW portion

Copy the schematic to new page,
the co-lay location maybe changed.

PRI2, PRI8 place near CPU side.
If the resisters are at HW side and POP. PRI2, PRI8 can be canceled.

PRI11, PRI16 place near CPU side.
If the resisters are at HW side and POP. PRI11, PRI16 can be canceled.

RIOUT@GT:
U23e = 22.1K PRI23
U22 = 25.5K PRI23
U23E@ PRI23 22.1K_0402_1%

RPH@GT:
U23e = 130K PRI30,PRI38
U22 =84.5K PRI30,PRI38(De-pop)
U23E@ PRI30 130K_0603_1%
U23E@ PRI38 130K_0603_1%

For U22:
PRI43=De-pop
For U23e:
PRI43,PRI38=Pop

For U22:
PRI47=2K, PRI54=De-pop
For U23e:
PRI47,PRI54=2K

For U22:
PCI23=De-pop
For U23e:
PCI23=0.1u

U22 OCP@GT= 40A
RLIM@GT=12.4K --->PRI39
U23e OCP@GT= 62A
RLIM@GT=12.4K --->PRI39

RLIM= IoutLIMIT * Load line/10

U22 IccMAX@GT= 31A
RIccMAX2ph= 48.7K --->PRI63
U23e IccMAX@GT= 56A
RIccMAX2ph= 87.6k --->PRI63

RIccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127

U22 Iout@GT= 31A
RIOUT@GT=25.5K --->PRI23
U23e Iout@GT= 56A
RIOUT@GT=22.1K --->PRI23

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

U22 Load line@GT= 3.1m
RPH@GT=84.5K --->PRI30,PRI38
U23e Load line@GT= 2m
RPH@VGT=130K --->PRI30,PRI38

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

NCP81208 Operating Frequency Rosc=24K
I/A and GT are 450KHz and SA is 450KHz

RIccMAX2ph:
For U22:
PRI63=48.7K
For U23e:
PRI63=100K
PRI63 U23E@ 100K_0402_1%

VBOOT:
22.1K for debuge setting.

PSYS:
Please confirm charger pull low resistance.
Charger side should be unpop.

IccMAX@SA= 5A
RIccMAX@SA= 15.8K --->PRI65

RIccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K --->PRI14

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=24K --->PRI5

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.78K --->PRI4

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IMVP8_EN
Upper Threshold > 0.8V
Lower Threshold < 0.3V

confirm with power sequence,
it need behind +5VS.

PRI26 and PRI33 pull high resistor are pop at the end of VR SVID.
Other VR is unpop.

U22 Load line@VCORE= 2.35m
RDRPSP@VCORE=2.1K --->PRI56
U23e Load line@VCORE= 2.1m
RDRPSP@VCORE=1.87K --->PRI56

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 28A
RIccMAX@VCORE= 87.6K --->PRI64

RIccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=64.9K --->PRI42

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@VCORE= 35A
RLIMSP@VCORE=33.4K --->PRI53

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

For U22:
PRI115=2.1K
For U23e:
PRI115=1.87K

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

PRI51, PRI58 place near CPU side.
If the resisters are at HW side and POP. PRI51, PRI58 can be canceled.

Title	NCP81208
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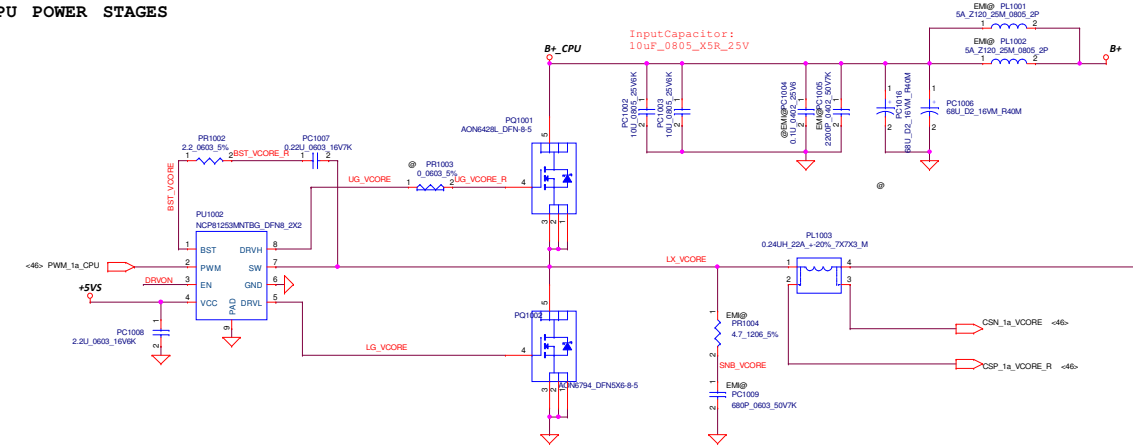
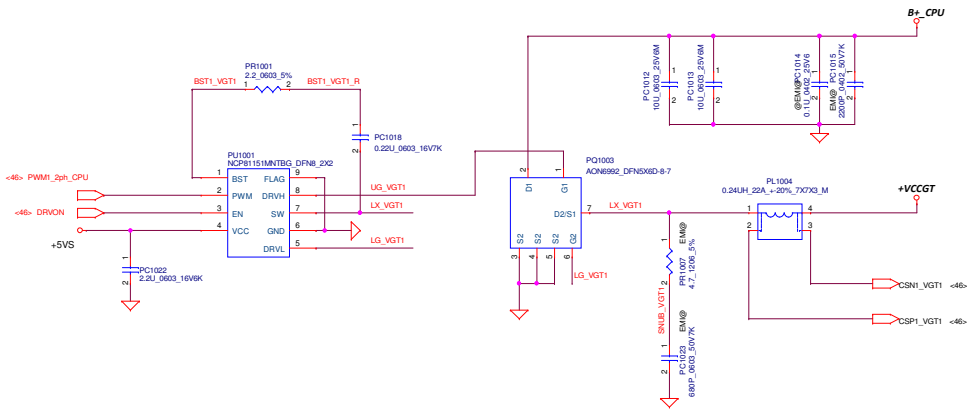
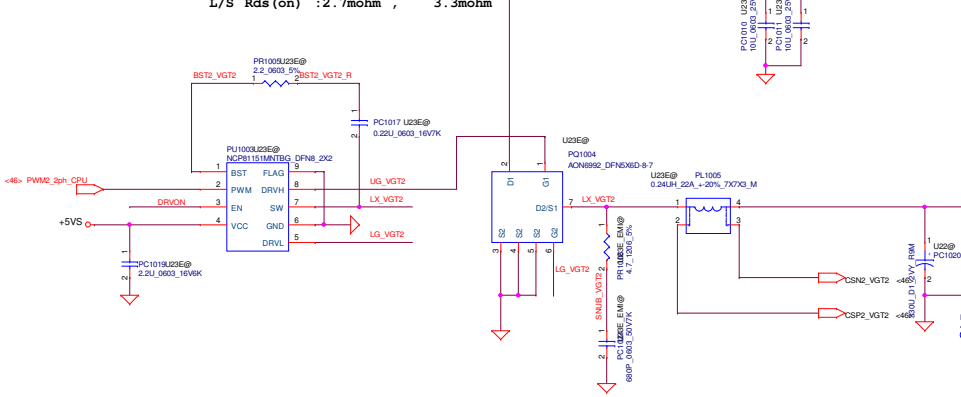
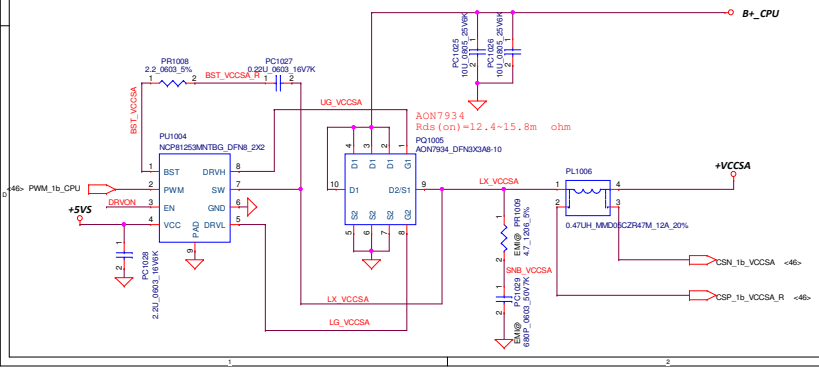
CPU POWER STAGES









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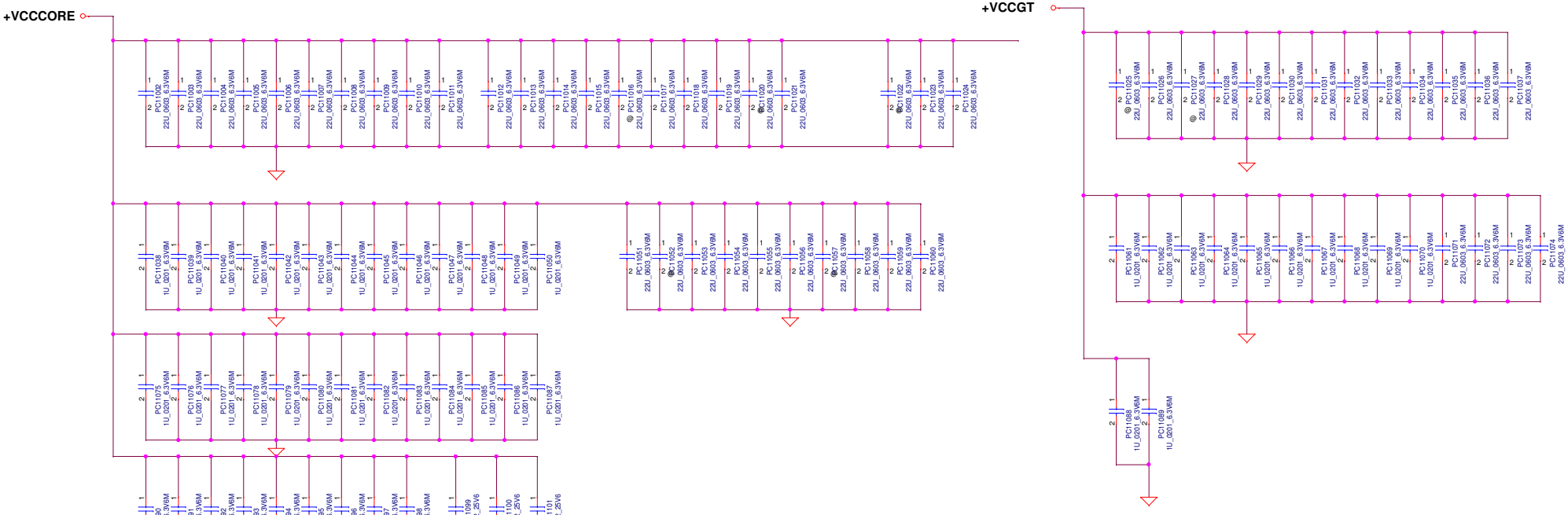
Issued Date	2015/07/27	Deciphered Date	2016/07/27

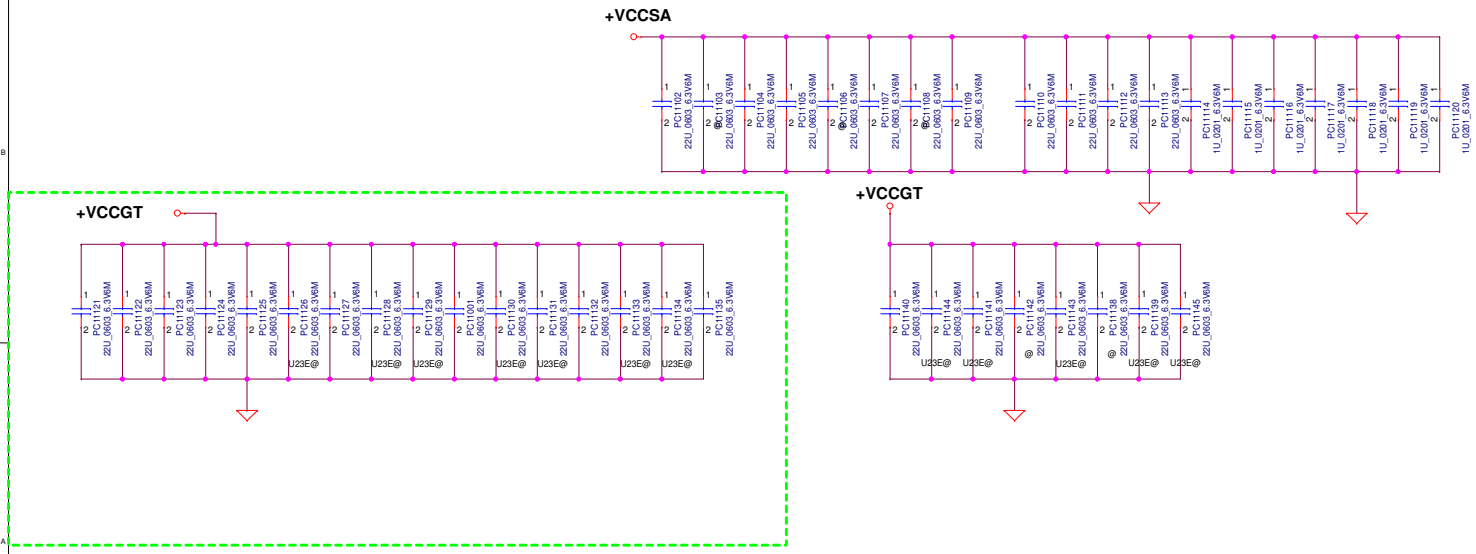
Compal Electronics, Inc.			
Title	PWR-PROCESSOR DECOUPLING		
Size Custom	Document Number		Rev 2.0
Date: Monday, June 06, 2016		Sheet 47 of 53	

VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 28 pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 29 pcs +1U_0201*12 pcs



VCC_SA Place on CPU Back Side @ V09
22U_0603 * 9 (4 CPU back+8 outside)pcs + 1U_0201*7



Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.

Title: PWR-PROCESSOR_DECOUPLING

Size	Document Number	Rev
C		2.0

Date: Monday, June 06, 2016 | Sheet 48 of 53

PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

unmount PRV5 for 2 phase select

Pull high at HW side.(20150831)

PR1214: OCP setting from 50A to 25A

H/L side Rds(on): 12.2mohm(Typ), 15mohm(Max)
Idsm: 11A@Ta=25C, 14A@Ta=70C

CHOKE:0.36uH, DCR 1.4m ohm, L/2 over 36A

FSW = 245.55KHz
Iripple = 12.74A
OCP = 50A
OVP=Vout*(145%~155%)

+VGA_CORE Under GPU Core GB4-128 package

+VGA_CORE Near GPU Core

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Issued Date	2014/12/31	Deciphered Date	2016/12/31

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Title: NVIDIA VGA_CORE

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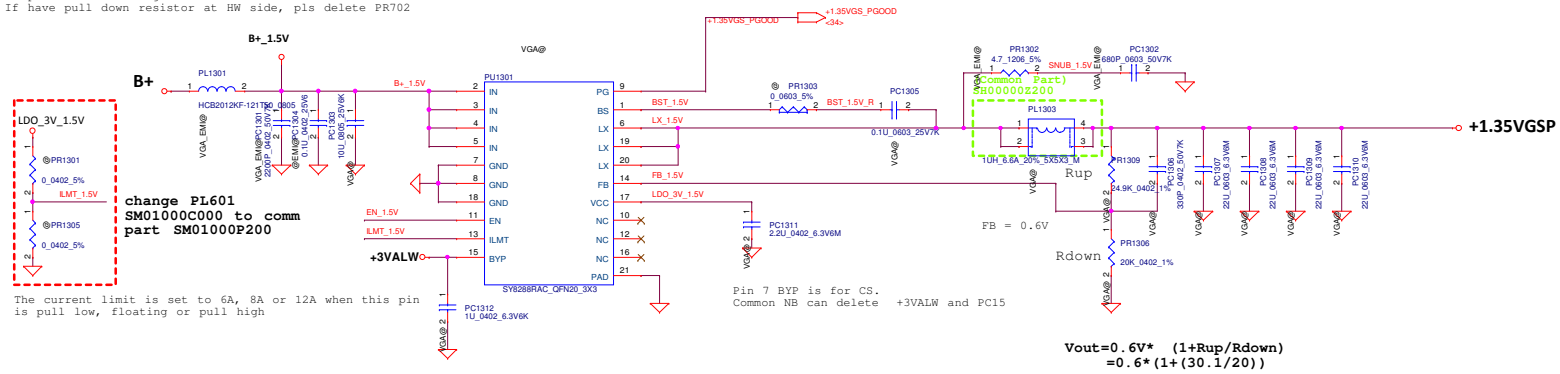
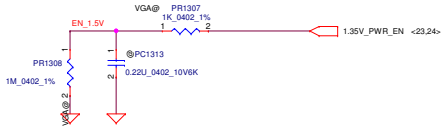
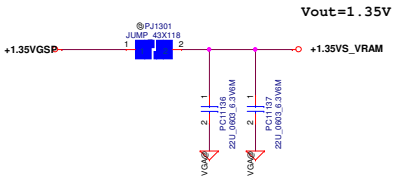
EN pin don't floating
If have pull down resistor at HW side, pls delete PR702







Security Classification	Compal Secret Data		
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Compal Electronics, Inc.			
Title	PWR-CPU_CORE/CPU_CORE_NB		
Size	Document Number		Rev
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	request by HW	P49	change PR1206 to 0 ohm	2015/11/10	SIV
2	request by HW	P50	change PR1307 to 1K ohm	2015/11/10	SIV
3	avoid 1V0 voltage drop	P44	change PR705 to 15K ohm	2015/11/10	SIV
4	adjust charge current limit	P40	change PR334 to 178K ohm	2015/11/10	SIV
6	reduce 5v ripple voltage	P41	add PC423 on schematic	2015/11/10	SIV
7	adjust component bom structure of U23E	P47	PQ1004->U23E@,PC1020->U23E@,PC1021->POP	2015/11/10	SIV
8	adjust DDR over current protect value	P42	change PR502 to 17.8K ohm	2015/11/10	SIV
9	request by part count	P40,42-45	PR319,PR321,PR510,PR601,PR701,PR807 change to 0 ohm short pad	2015/11/10	SIV
10 11	optimize cpu transient	P47/48	change below value: PCI18->680P,PRI23->26.7K ohm,PRI14->64.9K ohm, PRI42 ->59K ohm,PCI21->2200P,PRI49->649 ohm change pop and up pop CPU OUTPUT CAP location: PC11138,PC11140,PC11142,PC11143->POP PC11126,PC11128,PC11129,PC11133->U23E@	2015/11/10	SIV
12	request by EMI	P40	PC317,PR318,PC304->POP change PR312 to 2.2 ohm	2015/11/10	SIV
13	request by RF	P40-50	PR318,PR403,PR406,PR503,PR515,PR703,PR804,PR1004,PR1007,PR1006, PR1009,PR1213,PR1224,PR1302 ->POP PC317,PC410,PC425,PC515,PC525,PC702,PC803,PC1009,PC1023PC1024, PC1029,PC1215,PC1218,PC1302->POP	2015/11/10	SIV
14	reduce power consumption	P40	Del PR335,Add:PR336,PQ307,PQ308	2015/11/13	SIV
15	charger ac in detect	P40	change PC306 to 0.1uA	2015/11/16	SIV
16	reduce Aucostic noise	P40,47,49	Change 10u_0805(SE00000QK00) to 10u_0603(SE00000X200)	2015/12/05	SIT
17	When battery connector first touch positive pin can't power on	P41	Reserve PC428 and change PR409 to 100K pull high +VL	2015/12/14	SIT
18	reduce Aucostic noise	P47	change PC1006 from 33u to 68u, del PC1016	2015/12/18	SIT
19	request by EMI	P38	change PL102 and PL102 PN to SM010014520	2015/12/23	SIT
20	reduce ripple current	P41	change PC419,PC422,PC423 from 22u 0603 to 47u 0805 change PL404 from 1.5uH to 3.3uH	2016/01/19	SVT
21	solve ISL95521 didn't protect function (dc prochot)	P41	change PU301 from ISL95521 to ISL95520 change PR306 from 392K to 287K	2016/01/19	SVT
22	resive PC1016 for acustic noise	P47	resive PC1016 for acustic noise	2016/04/21	CIUY7-SIT
23	Modify PRI53,PRI64,PRI42 for cpu transient test	P46	PRI53 form 33.2k to 30.3k PRI42 form 59k to 56.2k PRI64 form 90.9k to 100k	2016/04/21	CIUY7-SIT
24	change for cost priority change AOS to main source on PQ1001 and PQ1002	P46	PQ1001 from SB00000S800 to SB00000JZ00 PQ1002 from SB00000SD00 to SB000017Q00	2016/06/03	CIUY7-SVT

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Title: PIR (PWR)			
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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For camera power control	27	Add Q4,R119,C132	2015/11/06	SDV=>SIV
2	For ME requestment	33	Swap JKBL1/JKBL2 symbol	2015/11/06	SDV=>SIV
3	For KB matrix design change	33 35	Add EC_GPIO72	2015/11/06	SDV=>SIV
4	For VGA sequence control	11	Change UC1.AC3 pin define to GPU_ALL_PGOOD	2015/11/06	SDV=>SIV
5	For ME requestment	32	H6,H9 change to H_3P6X4P5 Delete H7	2015/12/21	SIV=>SIT
6	Removing useless pull-high resistor	18	removing RD43 for DDR_DRAMRST#	2015/12/21	SIV=>SIT
7	For ME requestment	32	CLIP13 change to Larger size	2015/12/21	SIV=>SIT
8	For EC requestment	32	Change R1657 pull high to +3VS	2015/12/21	SIV=>SIT
10	Reserve cap for USB charger	32	Reserver C2171,C2172,C2173,C2177,C2178	2015/02/18	SIT=>SVT
11	Add USB3.0 CMC for RF requestment	32	Add L13,L15,L17,L18		
12	For Cable Shift Issue	27	JEDP1.3 from GND change to NC	2016/4/6	SIV=>SIT
13	Add USB 2.0 for FP	12 34	Add FP schematic & FP@	2016/4/6	SIV=>SIT
14	Add TS_detect function for EC	35 36	connect U11.75 to U2102.15	2016/4/7	SIV=>SIT

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Title: PIR (HW)

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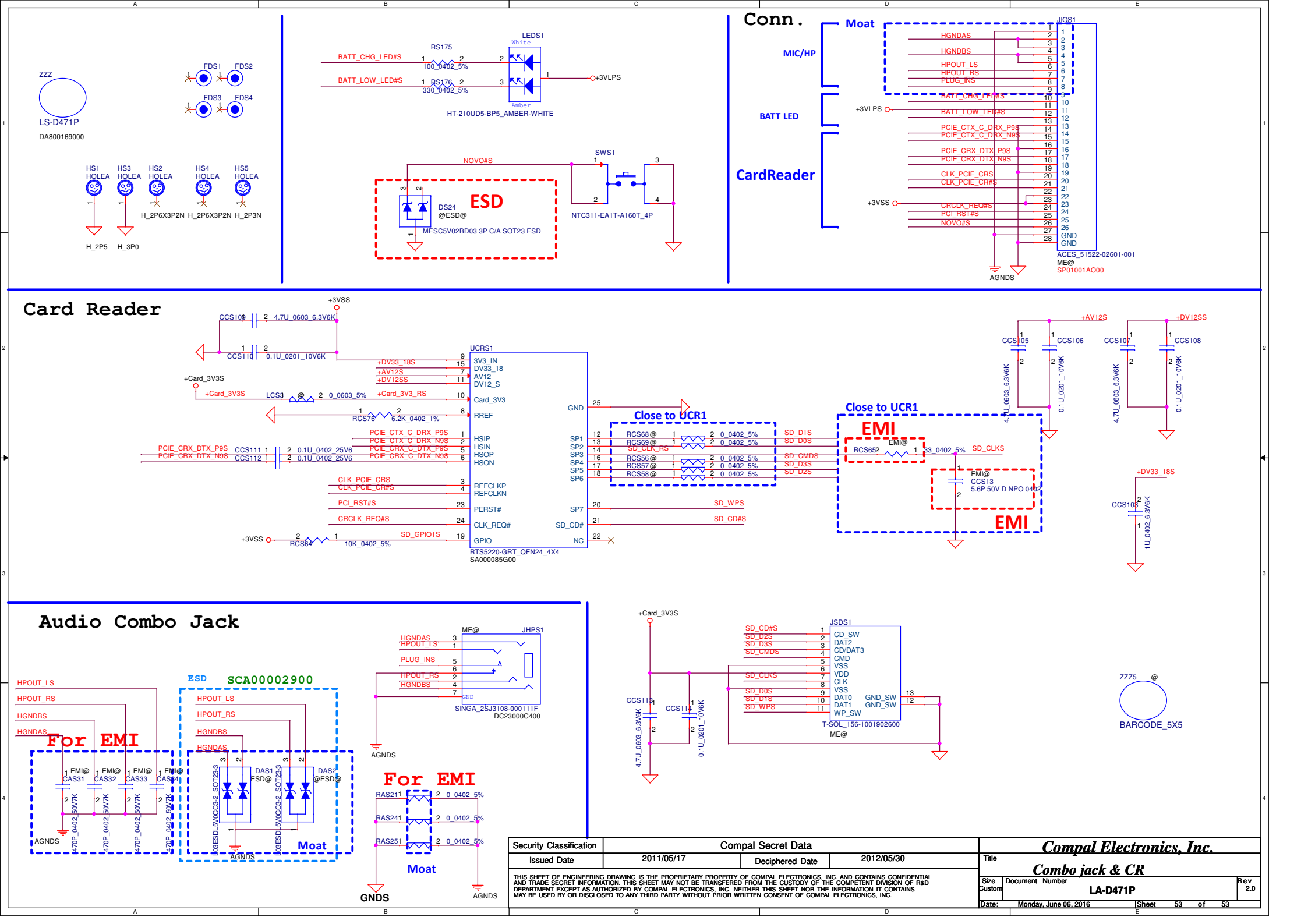

Security Classification	Compal Secret Data		
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Title: **Combo jack & CR**

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