

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.0	07'06'22	36	ICH8-M(GND) 5/5	1.0	07'06'22
02	Block Diagram	1.0	07'06'22	37	SATA HDD/CD-ROM	1.0	07'06'22
03	Merom(HOST BUS) 1/3	1.0	07'06'22	38	EC+KBC	1.0	07'06'22
04	Merom(HOST BUS) 2/3	1.0	07'06'22	39	Flash ROM/XBUS	1.0	07'06'22
05	Merom(Power/Gnd) 3/3	1.0	07'06'22	40	Mini-PCIE Card	1.0	07'06'22
06	CLOCK GEN	1.0	07'06'22	41	Bluetooth/CAM/OIDE	1.0	07'06'22
07	Crestline (HOST) 1/7	1.0	07'06'22	42	EXPRESS	1.0	07'06'22
08	Crestline (DMI) 2/7	1.0	07'06'22	43	BTB to Audio/MDC	1.0	07'06'22
09	Crestline (GRAPHIC) 3/7	1.0	07'06'22	44	FAN/Thermal-Sensor	1.0	07'06'22
10	Crestline (DDRII) 4/7	1.0	07'06'22	45	PCI (PCI BUS)	1.0	07'06'22
11	Crestline (POWER,VCC) 5/7	1.0	07'06'22	46	PCI (i.LINK)	1.0	07'06'22
12	Crestline (VCC CORE) 6/7	1.0	07'06'22	47	PCI (SD/MS-DUO)	1.0	07'06'22
13	Crestline (VSS) 7/7	1.0	07'06'22	48	USB2.0	1.0	07'06'22
14	DDRII(SO-DIMM_0) 1/3	1.0	07'06'22	49	LAN (88E8036)	1.0	07'06'22
15	DDRII(SO-DIMM_1) 2/3	1.0	07'06'22	50	Power Design Diagram	1.0	07'06'22
16	DDRII(Termination) 3/3	1.0	07'06'22	51	DCIN&Charger	1.0	07'06'22
17	VGA(PCI-E)	1.0	07'06'22	52	SYS Power (+3_3V/+5V)	1.0	07'06'22
18	VGA(STRAP)	1.0	07'06'22	53	SYS Power(+1_5V/+1_05V)	1.0	07'06'22
19	VGA(GDDR)#	1.0	07'06'22	54	DDR2 Power(+1_8V/+0_9V)	1.0	07'06'22
20	VGA(MULTIUSE)	1.0	07'06'22	55	CPU_Vcore---ISL6262A	1.0	07'06'22
21	VGA(LVDS/VDAC)	1.0	07'06'22	56	Others power plane	1.0	07'06'22
22	VRAM(GDDR)# 1/2	1.0	07'06'22	57	OVP protection	1.0	07'06'22
23	VRAM(GDDR)# 2/2	1.0	07'06'22	58	VGA POWER(+1_1V/ +1_2V)	1.0	07'06'22
24	VGA(POWER) 1/3	1.0	07'06'22	59	GMCH power	1.0	07'06'22
25	VGA(POWER) 2/3	1.0	07'06'22	60	HOLE	1.0	07'06'22
26	VGA(POWER) 3/3	1.0	07'06'22	61	EC+KBC(3925)	1.0	07'06'22
27	VRAM(BYPASS) 1/2	1.0	07'06'22	62	HDMI	1.0	07'06'22
28	VRAM(BYPASS) 2/2	1.0	07'06'22	63	ROBSON B to B Connector.	1.0	07'06'22
29	TVIN and OUT/Semi-PnP#	1.0	07'06'22	64	LED/Touch/Lid	1.0	07'06'22
30	CRT	1.0	07'06'22	65	History (1)	1.0	07'06'22
31	LVDS	1.0	07'06'22	66	History (2)	1.0	07'06'22
32	ICH8-M(PCI/USB) 1/5	1.0	07'06'22	67			
33	ICH8-M(LPC, IDE, SATA) 2/5	1.0	07'06'22	68			
34	ICH8-M(GPIO) 3/5	1.0	07'06'22	69			
35	ICH8-M(POWER) 4/5	1.0	07'06'22	70			

BOM configuration		
SKU	Stuff	No stuff
NB8M-256MB-Samsung	NV_,NVNB8M_,NV128bit_,NV16M_,NVH/S_,NVQ/S_	NC_* ,NVNB8P_,NV64bit_,NV8M_,NVQ_,NVH_
NB8M-256MB-Qimonda	NV_,NVNB8M_,NV128bit_,NV16M_,NVQ_,NVQ/S_	/NC_* ,NVNB8P_,NV64bit_,NV8M_,NVH/S_,NVH_
NB8M-256MB-Hynix	NV_,NVNB8M_,NV128bit_,NV16M_,NVH/S_,NVH_	NC_* ,NVNB8P_,NV64bit_,NV8M_,NVQ_,NVQ/S_
NB8M-128MB-Samsung	NV_,NVNB8M_,NV64bit_,NV16M_,NVH/S_,NVQ/S_	NC_* ,NVNB8P_,NV128bit_,NV8M_,NVQ_,NVH_
NB8M-128MB-Qimonda	NV_,NVNB8M_,NV64bit_,NV16M_,NVQ_,NVQ/S_	NC_* ,NVNB8P_,NV128bit_,NV8M_,NVH/S_,NVH_
NB8M-128MB-Hynix	NV_,NVNB8M_,NV64bit_,NV16M_,NVH/S_,NVH_	NC_* ,NVNB8P_,NV128bit_,NV8M_,NVQ_,NVQ/S_
NB8M-64MB-Hynix	NV_,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVH_	NC_* ,NVNB8P_,NV128bit_,NV16M_,NVQ/S_,NVQ_
NB8M-64MB-Samsung	NV_,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVQ/S_	NC_* ,NVNB8P_,NV128bit_,NV16M_,NVQ_,NVH_
NB8P-256MB-Samsung	NV_,NVNB8P_,NV128bit_,NV16M_,NVH/S_,NVQ/S_	NC_* ,NVNB8M_,NV64bit_,NV8M_,NVQ_,NVH_
NB8P-256MB-Qimonda	NV_,NVNB8P_,NV128bit_,NV16M_,NVQ_,NVQ/S_	NC_* ,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVH_
NB8P-256MB-Hynix	NV_,NVNB8P_,NV128bit_,NV16M_,NVH/S_,NVH_	NC_* ,NVNB8M_,NV64bit_,NV8M_,NVQ_,NVQ/S_
GM965/GL960	CA_	No CA_>

Project Code & Schematics Subject: MS91 Main Board

PCB P/N:
 1P-0076100-8010 (FUBAI)
 1P-0076500-8010 (HANNSTAR)
 1P-0076200-8010 (NAN YA)

The "NC_*" include "NC_CA_"and "NC_NV*", the are prefix which comes from MS90 schematic,it means NC also, but if the component is needed again, "NC_CA_" is only for Low module only and "NC_NV*" only for HH/H/M module only.the rule is help to remind this.

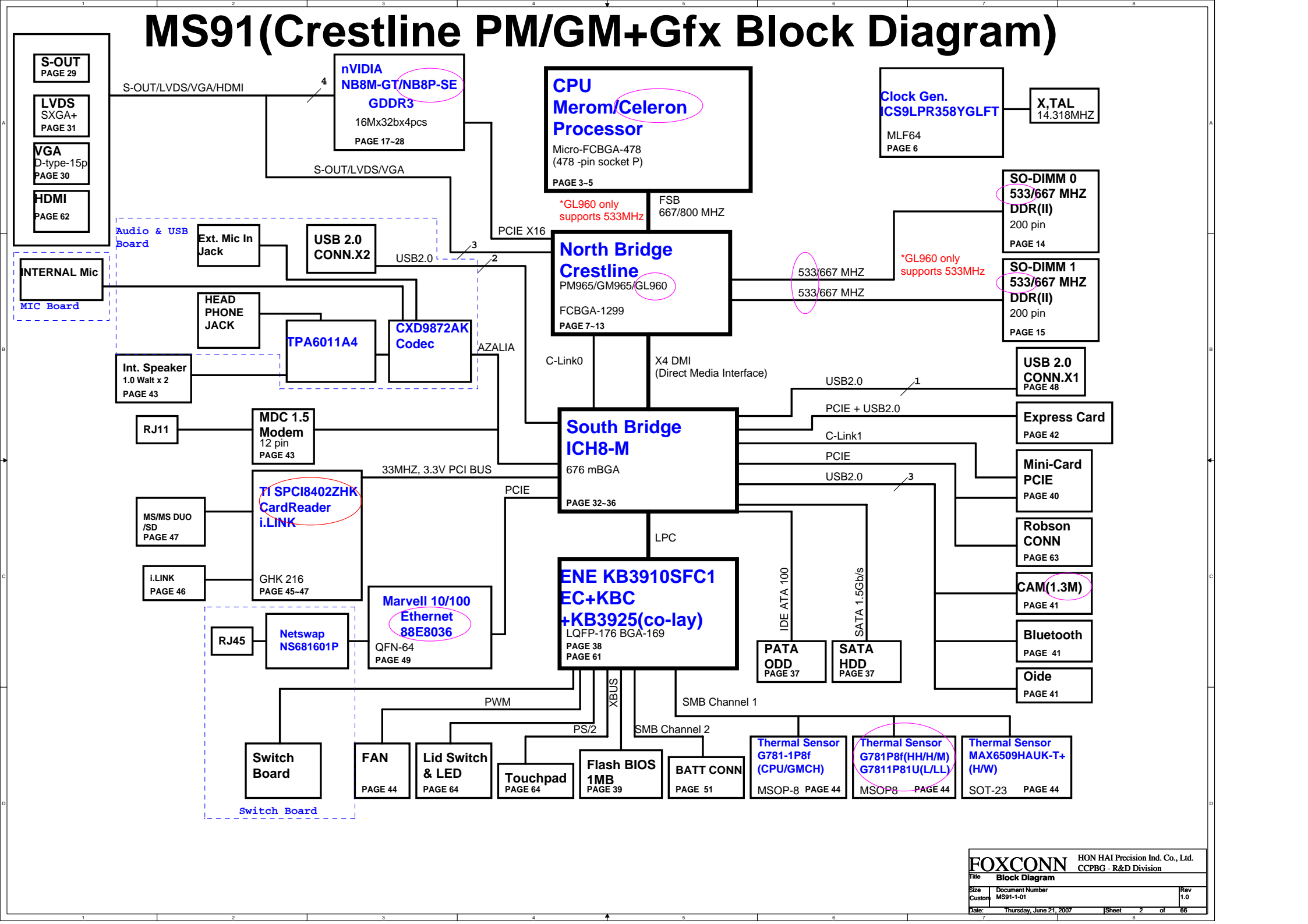
P. Leader	Check by	Design by

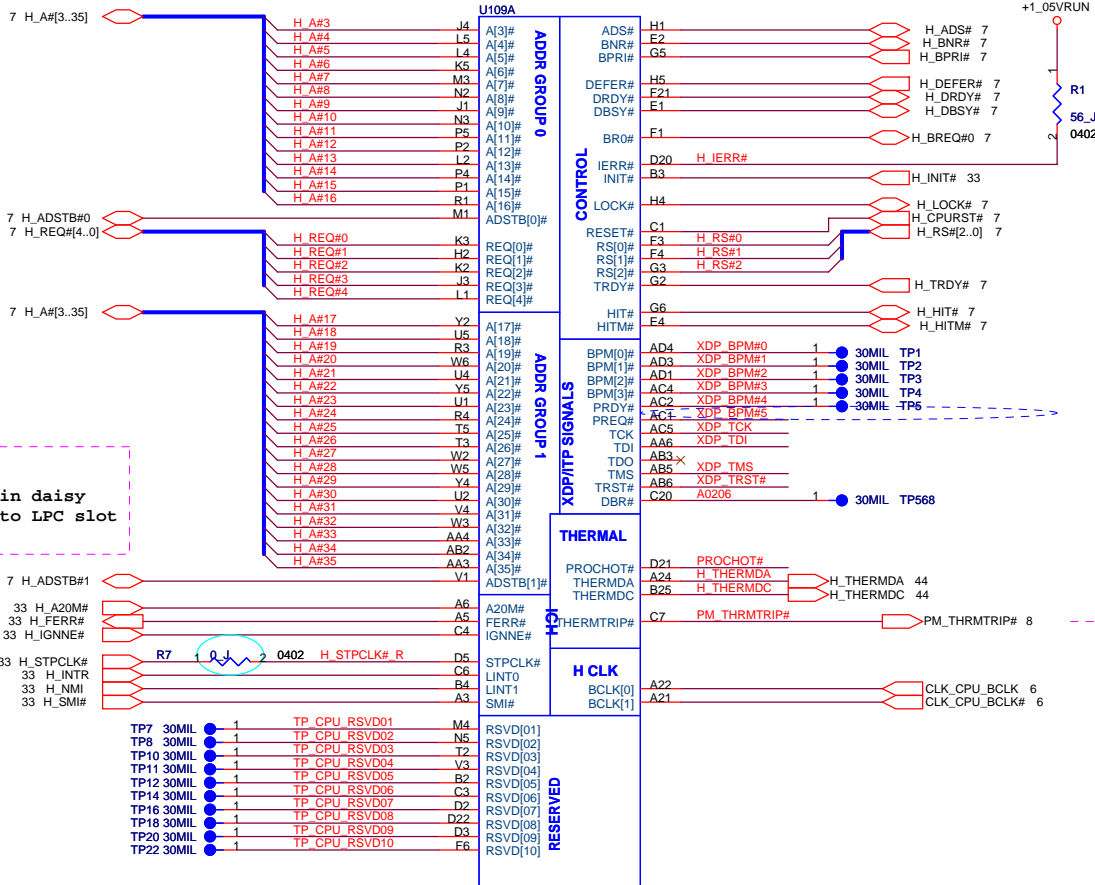
Dropped the NB8P-SE/128MB and NB8P-SE/64M for MOR request

"no CA_" means all of other prefix including the "NC_" prefix.

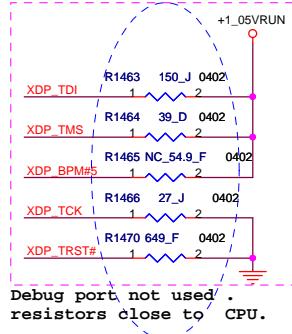
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Index Page		
Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 1	of 66

MS91 (Crestline PM/GM+Gfx Block Diagram)

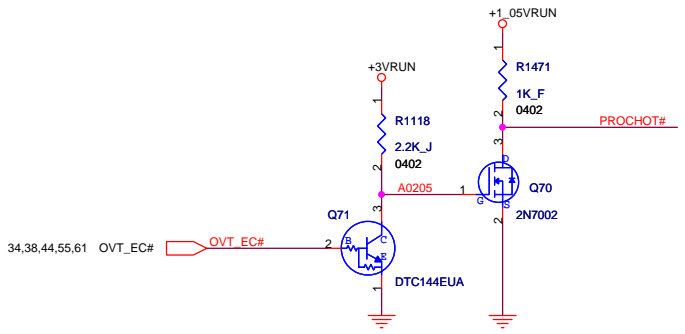




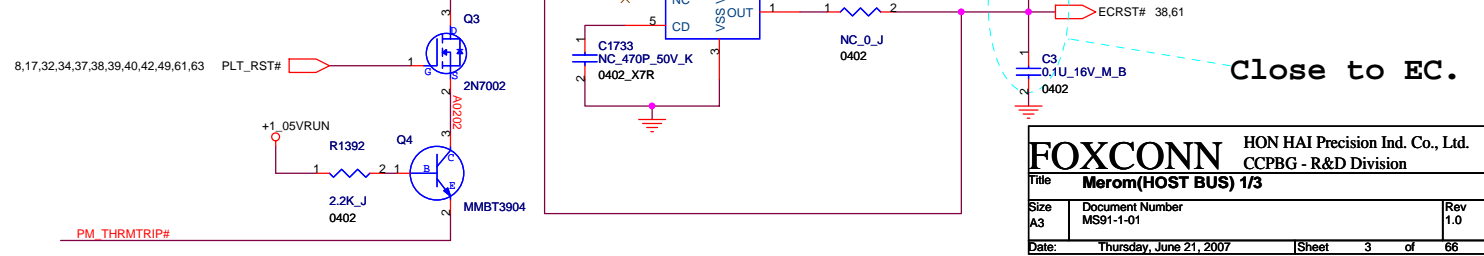
Layout note:
no stub on H_STPCLK TP.
H_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.



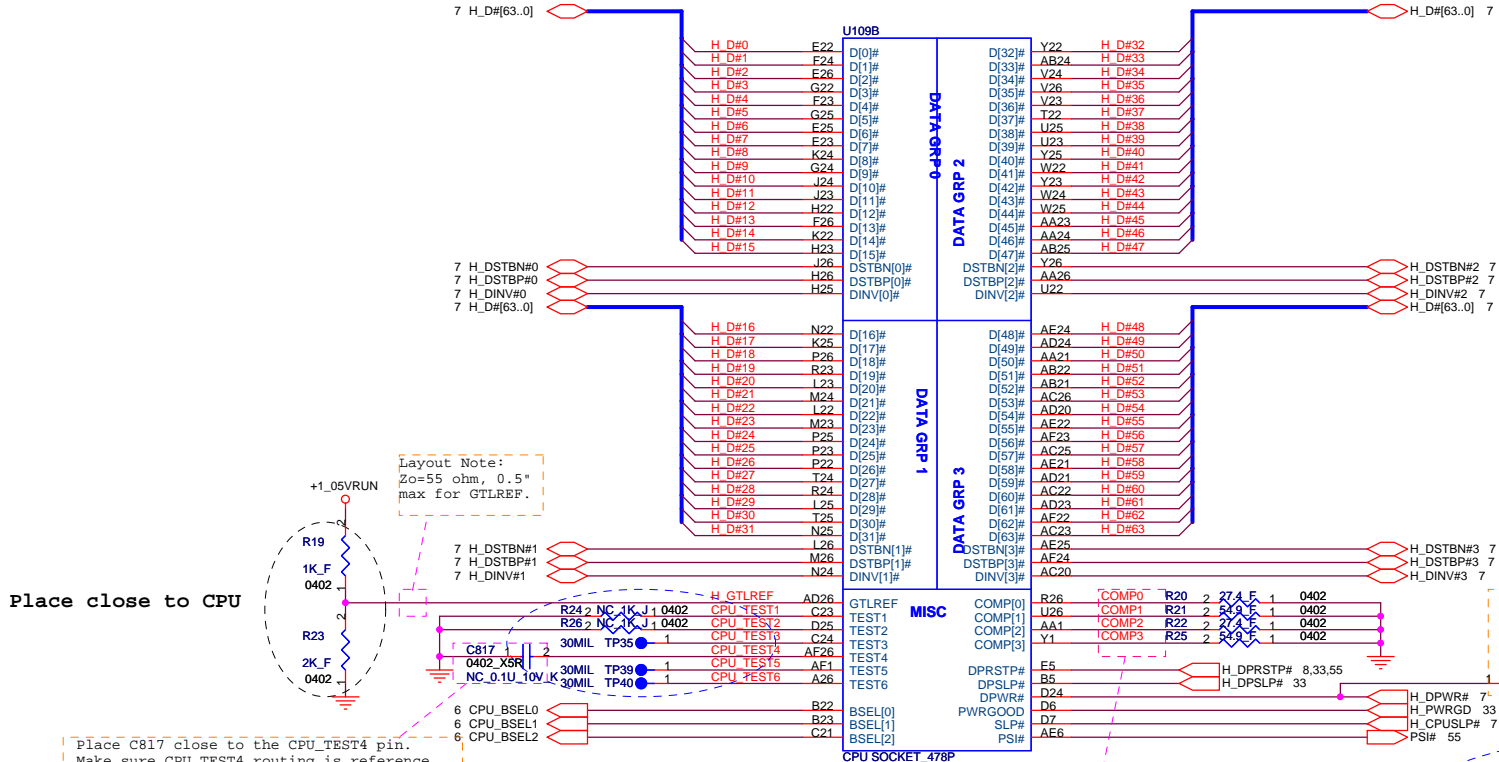
PM_THRMTRIP# should connect to ICH8-M and GMCH without T-ing (No stub)



CPU SOCKET_478P
FOX_PZ4782A-274M-01



ICH8M's GPIO12: VIL----> -0.5V ~ 0.8V
VIH----> 2.0V ~ 3.3+0.5V
MEROM's PROCHOT#: VIL----> -0.1V ~ 0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1



Layout Note:
 $Z_0=55$ ohm, 0.5" max for GTLREF.

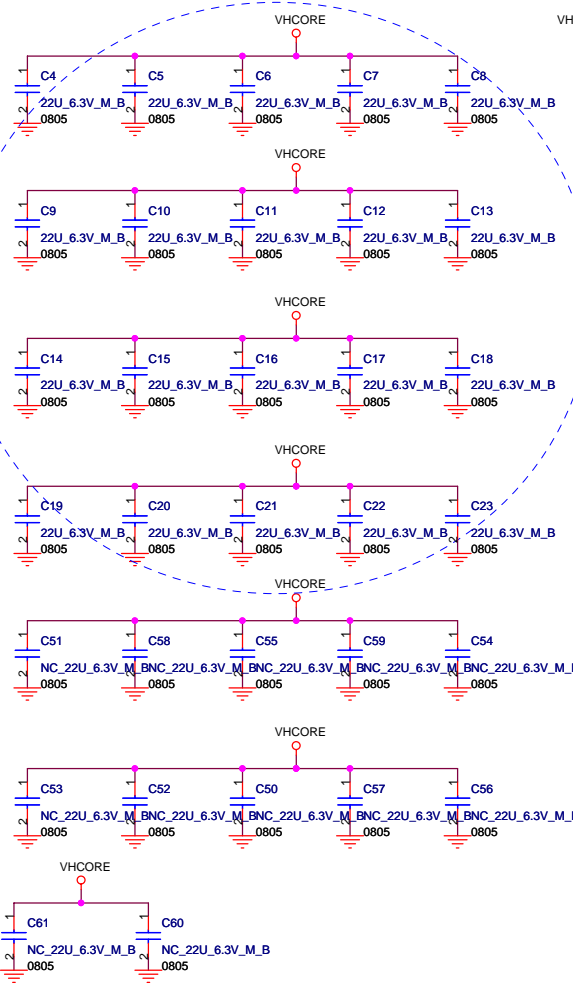
Place close to CPU

Place C817 close to the CPU_TEST4 pin.
 Make sure CPU_TEST4 routing is reference to GND and away from other noisy signals.

Layout Note:
 Comp0,2 connect with $Z_0=27.4$ ohm, make trace length shorter then 0.5".
 Comp1,3 connect with $Z_0=55$ ohm, make trace length shorter then 0.5".

IMVP6 (ISL6262ACRZ-T)
 cpu PSI# <-> ISL6262ACRZ-T PSI#
 ISL6262ACRZ-T: VIHmin=0.315V
 VILmax=0.735V
 (ref. IMVP-6 NO:18904)

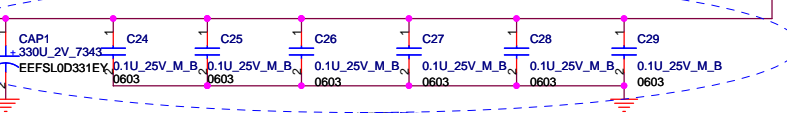
Layout:
 Connect test point with no stub



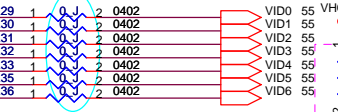
U109C

A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	B13
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	G21
E12	VCC[036]	VCCP[02]	V6
E13	VCC[037]	VCCP[03]	K6
E15	VCC[038]	VCCP[04]	IM6
E17	VCC[039]	VCCP[05]	J21
E18	VCC[040]	VCCP[06]	K21
E20	VCC[041]	VCCP[07]	M21
F7	VCC[042]	VCCP[08]	N21
F10	VCC[043]	VCCP[09]	R21
F12	VCC[044]	VCCP[10]	R6
F14	VCC[045]	VCCP[11]	T21
F15	VCC[046]	VCCP[12]	T6
F17	VCC[047]	VCCP[13]	V21
F18	VCC[048]	VCCP[14]	W21
F20	VCC[049]	VCCP[15]	
F22	VCC[050]	VCCP[16]	
AA7	VCC[051]	VCC[051]	B26
AA9	VCC[052]	VCC[052]	C26
AA10	VCC[053]	VCC[053]	
AA12	VCC[054]	VCC[054]	
AA13	VCC[055]	VCC[055]	
AA15	VCC[056]	VCC[056]	
AA17	VCC[057]	VCC[057]	
AA18	VCC[058]	VCC[058]	
AA20	VCC[059]	VCC[059]	
AB9	VCC[060]	VCC[060]	
AC10	VCC[061]	VCC[061]	
AB10	VCC[062]	VCC[062]	
AB12	VCC[063]	VCC[063]	
AB14	VCC[064]	VCC[064]	
AB15	VCC[065]	VCC[065]	
AB17	VCC[066]	VCC[066]	
AB18	VCC[067]	VCC[067]	

CPU_VCCA----->120mA
 CPU_VCCP----->2.5A
 CPU_VCC----->36A



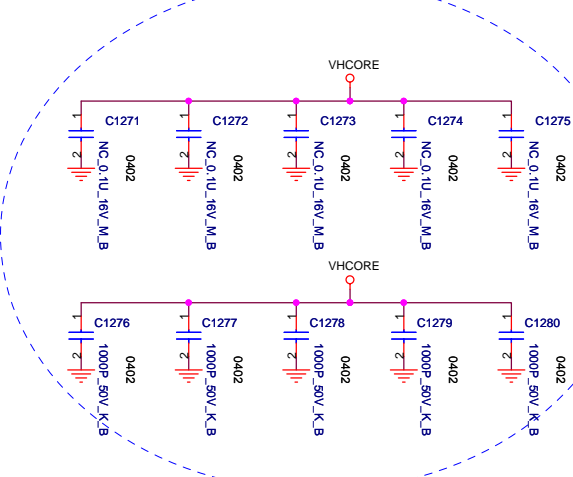
LAYOUT-NOTE:
Place 0.01uF
near PIN B26



VCCSENSE
 VSSSENSE
 Same Length

Layout Note: Route
 VCCSENSE & VSSSENSE
 traces at 27.4 Ohms with
 50 mil spacing. Place PU
 and PD within 1 inch of
 CPU.
 width=18 mil
 spacing=7 mil

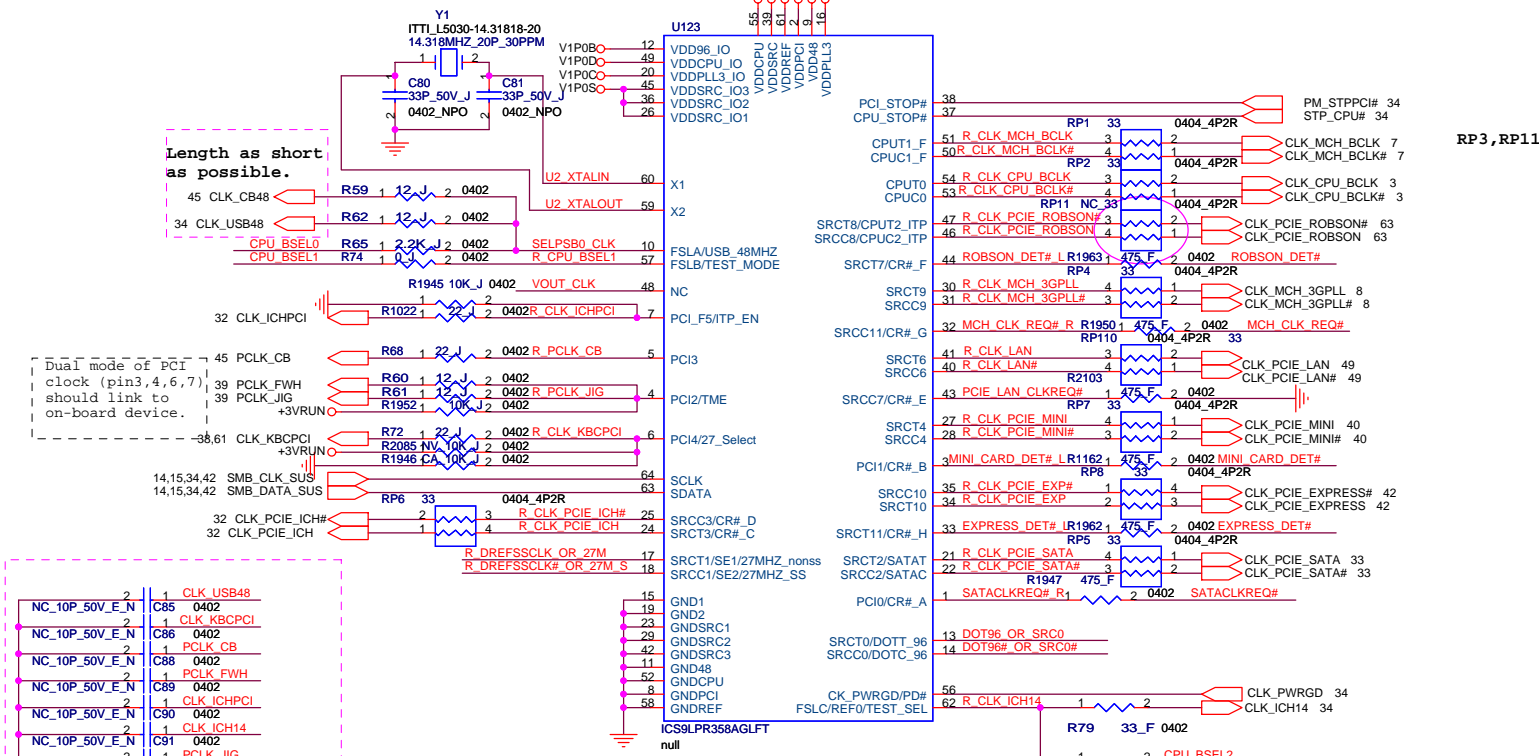
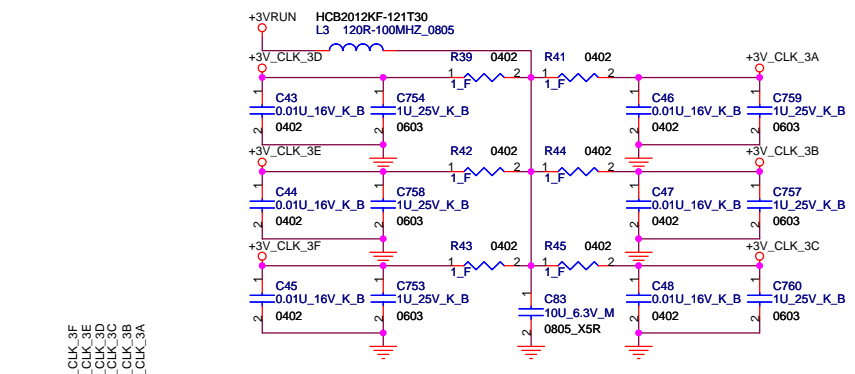
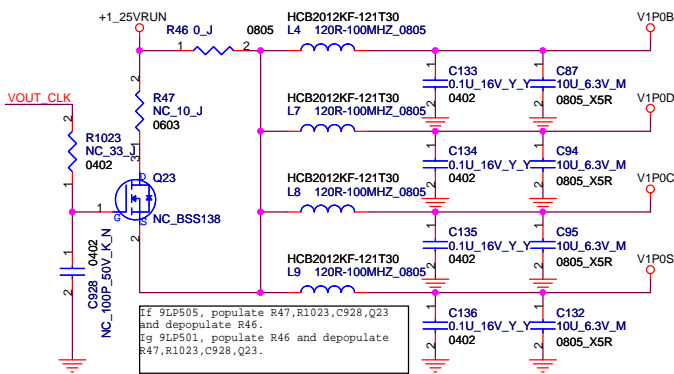
- TP890 tpc40t_50 1 H_VID0
- TP891 tpc40t_50 1 H_VID1
- TP892 tpc40t_50 1 H_VID2
- TP893 tpc40t_50 1 H_VID3
- TP894 tpc40t_50 1 H_VID4
- TP895 tpc40t_50 1 H_VID5
- TP896 tpc40t_50 1 H_VID6



U109D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C2	VSS[023]	VSS[104]	Y3
C22	VSS[024]	VSS[105]	Y6
C2	VSS[025]	VSS[106]	Y21
D1	VSS[026]	VSS[107]	Y24
D4	VSS[027]	VSS[108]	AA2
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D16	VSS[031]	VSS[112]	AA14
D18	VSS[032]	VSS[113]	AA16
D23	VSS[033]	VSS[114]	AA19
D26	VSS[034]	VSS[115]	AA22
E3	VSS[035]	VSS[116]	AA25
E6	VSS[036]	VSS[117]	AB1
E8	VSS[037]	VSS[118]	AB4
E11	VSS[038]	VSS[119]	AB8
E14	VSS[039]	VSS[120]	AB11
E16	VSS[040]	VSS[121]	AB13
E19	VSS[041]	VSS[122]	AB16
E21	VSS[042]	VSS[123]	AB19
E24	VSS[043]	VSS[124]	AB22
F5	VSS[044]	VSS[125]	AB25
F8	VSS[045]	VSS[126]	AC3
F11	VSS[046]	VSS[127]	AC6
F13	VSS[047]	VSS[128]	AC8
F16	VSS[048]	VSS[129]	AC11
F19	VSS[049]	VSS[130]	AC14
F2	VSS[050]	VSS[131]	AC16
F22	VSS[051]	VSS[132]	AC19
F25	VSS[052]	VSS[133]	AC21
G4	VSS[053]	VSS[134]	AC24
G1	VSS[054]	VSS[135]	AD2
G23	VSS[055]	VSS[136]	AD5
G26	VSS[056]	VSS[137]	AD8
H3	VSS[057]	VSS[138]	AD11
H6	VSS[058]	VSS[139]	AD13
H21	VSS[059]	VSS[140]	AD16
H24	VSS[060]	VSS[141]	AD19
J2	VSS[061]	VSS[142]	AD22
J5	VSS[062]	VSS[143]	AD25
J22	VSS[063]	VSS[144]	AE1
J25	VSS[064]	VSS[145]	AE4
K1	VSS[065]	VSS[146]	AE8
K4	VSS[066]	VSS[147]	AE11
K23	VSS[067]	VSS[148]	AE14
K26	VSS[068]	VSS[149]	AE16
L3	VSS[069]	VSS[150]	AE19
L6	VSS[070]	VSS[151]	AE23
L21	VSS[071]	VSS[152]	AE26
L24	VSS[072]	VSS[153]	A2
M2	VSS[073]	VSS[154]	AF6
M5	VSS[074]	VSS[155]	AF8
M22	VSS[075]	VSS[156]	AF11
M25	VSS[076]	VSS[157]	AF13
N1	VSS[077]	VSS[158]	AF16
N4	VSS[078]	VSS[159]	AF19
N23	VSS[079]	VSS[160]	AF21
N26	VSS[080]	VSS[161]	A25
P3	VSS[081]	VSS[162]	AF25

CPU SOCKET_478P
 FOX_PZ4782A-274M-01

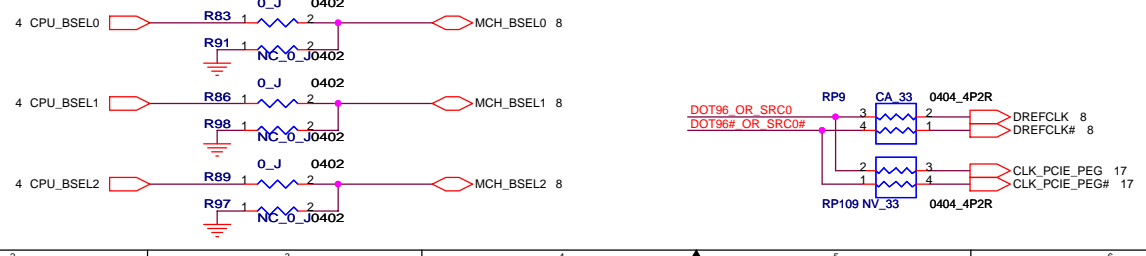


close to clk gen (For EMI)

NC_10P_50V_E_N	C85	0402	1	CLK_USB48
NC_10P_50V_E_N	C86	0402	1	CLK_KBCPCI
NC_10P_50V_E_N	C87	0402	1	PCLK_CB
NC_10P_50V_E_N	C88	0402	1	PCLK_FWH
NC_10P_50V_E_N	C89	0402	1	CLK_ICHPCI
NC_10P_50V_E_N	C90	0402	1	CLK_ICH14
NC_10P_50V_E_N	C91	0402	1	PCLK_JIG
NC_10P_50V_E_N	C92	0402	1	PCLK_JIG

FSB Frequency Table:

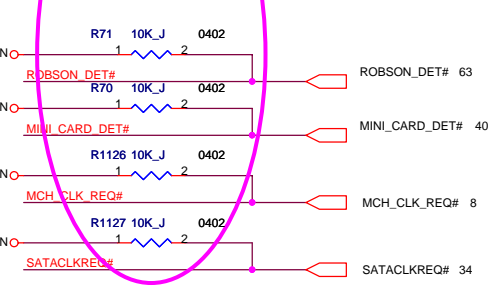
FSLC	FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33



RP3,RP11 close to CLK GEN.

Check CLKREQ with internal pull-up resistor or not. Default stuff Pull-up Resistor.

Delete(for docking)

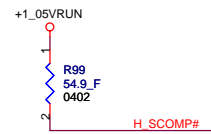
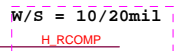
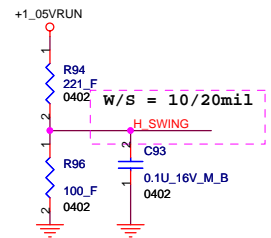


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

File: **CLOCK GEN**

Size A3	Document Number MS91-1-01	Rev 1.0
---------	---------------------------	---------

Date: Thursday, June 21, 2007 Sheet 6 of 66



4 H_D#[63..0] H_D#[63..0]

H_D#0	E2	H_D#0
H_D#1	G2	H_D#1
H_D#2	G7	H_D#2
H_D#3	M6	H_D#3
H_D#4	H7	H_D#4
H_D#5	H3	H_D#5
H_D#6	G4	H_D#6
H_D#7	F3	H_D#7
H_D#8	N8	H_D#8
H_D#9	H2	H_D#9
H_D#10	M10	H_D#10
H_D#11	N12	H_D#11
H_D#12	N9	H_D#12
H_D#13	H5	H_D#13
H_D#14	P13	H_D#14
H_D#15	K9	H_D#15
H_D#16	M2	H_D#16
H_D#17	W10	H_D#17
H_D#18	Y8	H_D#18
H_D#19	V4	H_D#19
H_D#20	M3	H_D#20
H_D#21	J1	H_D#21
H_D#22	N5	H_D#22
H_D#23	N3	H_D#23
H_D#24	W6	H_D#24
H_D#25	W9	H_D#25
H_D#26	N2	H_D#26
H_D#27	Y7	H_D#27
H_D#28	Y9	H_D#28
H_D#29	P4	H_D#29
H_D#30	W3	H_D#30
H_D#31	N1	H_D#31
H_D#32	AD12	H_D#32
H_D#33	AE3	H_D#33
H_D#34	AD9	H_D#34
H_D#35	AC9	H_D#35
H_D#36	AC7	H_D#36
H_D#37	AC14	H_D#37
H_D#38	AD11	H_D#38
H_D#39	AC11	H_D#39
H_D#40	AB2	H_D#40
H_D#41	AD7	H_D#41
H_D#42	AB1	H_D#42
H_D#43	Y3	H_D#43
H_D#44	AC6	H_D#44
H_D#45	AE2	H_D#45
H_D#46	AC5	H_D#46
H_D#47	AG3	H_D#47
H_D#48	AJ9	H_D#48
H_D#49	AH8	H_D#49
H_D#50	AI4	H_D#50
H_D#51	AE9	H_D#51
H_D#52	AE11	H_D#52
H_D#53	AH12	H_D#53
H_D#54	AJ5	H_D#54
H_D#55	AH5	H_D#55
H_D#56	AJ6	H_D#56
H_D#57	AE7	H_D#57
H_D#58	AJ7	H_D#58
H_D#59	AJ2	H_D#59
H_D#60	AE5	H_D#60
H_D#61	AJ3	H_D#61
H_D#62	AH2	H_D#62
H_D#63	AH13	H_D#63

U112A

HOST

H_A#3	J13	H_A#3
H_A#4	B11	H_A#4
H_A#5	C11	H_A#5
H_A#6	M11	H_A#6
H_A#7	C15	H_A#7
H_A#8	F16	H_A#8
H_A#9	L13	H_A#9
H_A#10	G17	H_A#10
H_A#11	C14	H_A#11
H_A#12	K16	H_A#12
H_A#13	B13	H_A#13
H_A#14	L16	H_A#14
H_A#15	J17	H_A#15
H_A#16	B14	H_A#16
H_A#17	K19	H_A#17
H_A#18	P15	H_A#18
H_A#19	R17	H_A#19
H_A#20	B16	H_A#20
H_A#21	L19	H_A#21
H_A#22	D17	H_A#22
H_A#23	M17	H_A#23
H_A#24	N16	H_A#24
H_A#25	J19	H_A#25
H_A#26	B18	H_A#26
H_A#27	E19	H_A#27
H_A#28	B17	H_A#28
H_A#29	B15	H_A#29
H_A#30	E17	H_A#30
H_A#31	C18	H_A#31
H_A#32	A18	H_A#32
H_A#33	B19	H_A#33
H_A#34	N19	H_A#34
H_A#35		

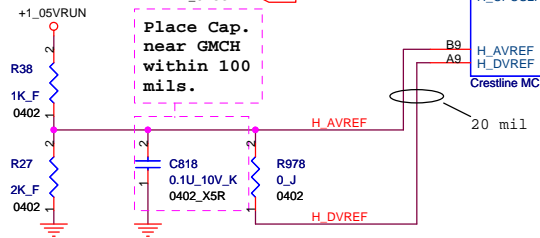
H_A#[3..35] 3

H_ADS#	G12	H_ADS# 3
H_ADSTB#0	H17	H_ADSTB#0 3
H_ADSTB#1	G20	H_ADSTB#1 3
H_BNR#	C8	H_BNR# 3
H_BPRI#	E12	H_BPRI# 3
H_BREQ#	D6	H_BREQ# 3
H_DEFER#	C10	H_DEFER# 3
H_DBSY#	AM5	H_DBSY# 3
HPLL_CLK	AM7	CLK_MCH_BCLK# 6
HPLL_CLK#	J8	CLK_MCH_BCLK# 6
H_DPWR#	KZ	H_DPWR# 4
H_DRDY#	E4	H_DRDY# 3
H_HIT#	C6	H_HIT# 3
H_HITM#	G10	H_HITM# 3
H_LOCK#	B7	H_LOCK# 3
H_TRDY#		H_TRDY# 3

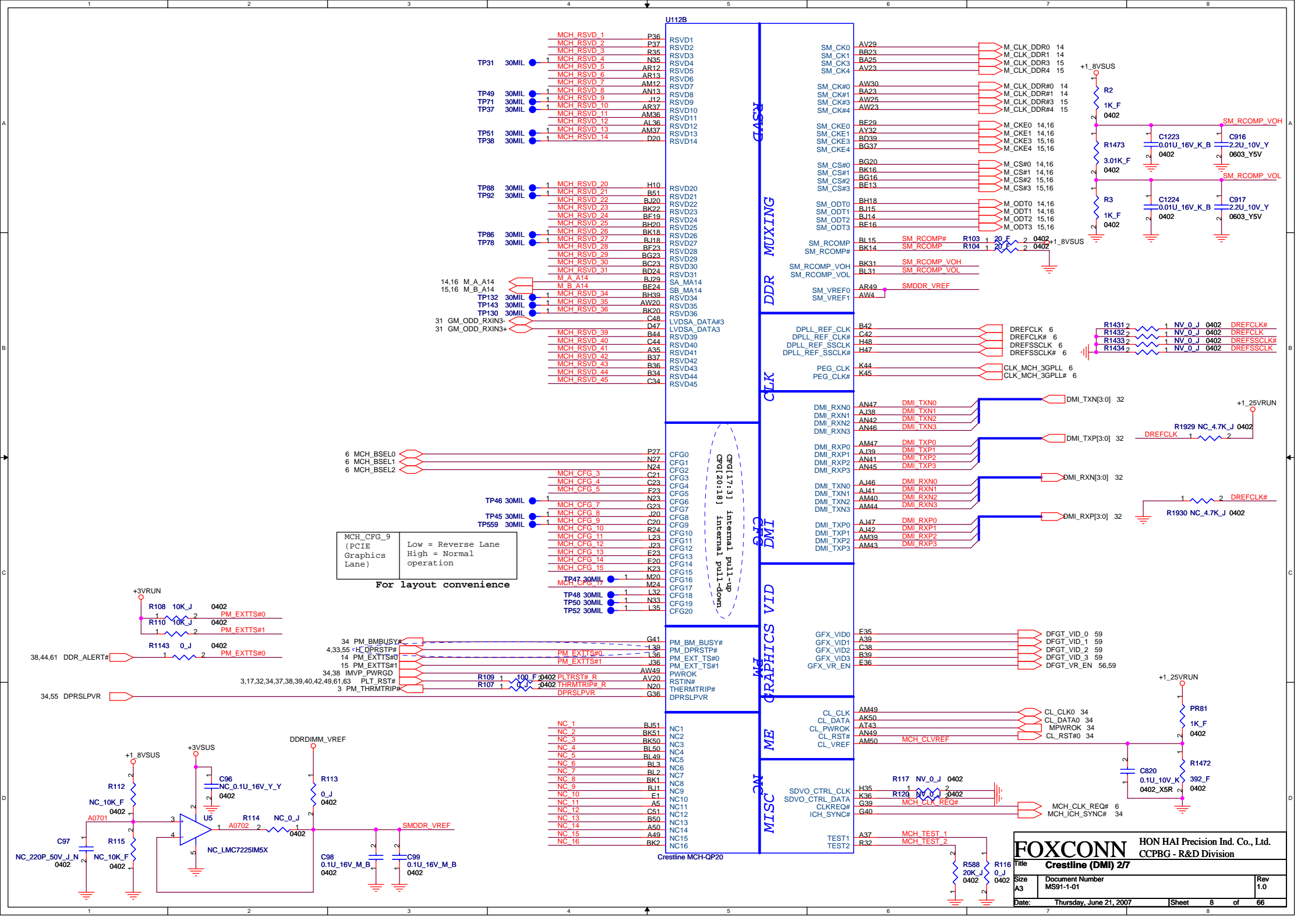
H_DIN#0	K5	H_DIN#0
H_DIN#1	L2	H_DIN#1
H_DIN#2	AD13	H_DIN#2
H_DIN#3	AE13	H_DIN#3
H_DSTBN#0	MZ	H_DSTBN#0
H_DSTBN#1	K3	H_DSTBN#1
H_DSTBN#2	AD2	H_DSTBN#2
H_DSTBN#3	AH11	H_DSTBN#3
H_DSTBP#0	L7	H_DSTBP#0
H_DSTBP#1	K2	H_DSTBP#1
H_DSTBP#2	AC2	H_DSTBP#2
H_DSTBP#3	AJ10	H_DSTBP#3
H_REQ#0	M14	H_REQ#0
H_REQ#1	E13	H_REQ#1
H_REQ#2	A11	H_REQ#2
H_REQ#3	H13	H_REQ#3
H_REQ#4	B12	H_REQ#4
H_RS#0	E12	H_RS#0
H_RS#1	D7	H_RS#1
H_RS#2	D8	H_RS#2

H_DIN#[3..0] 4
H_DSTBN#[3..0] 4
H_DSTBP#[3..0] 4
H_REQ#[4..0] 3
H_RS#[2..0] 3

H_SWING	B3	H_SWING
H_RCOMP	C2	H_RCOMP
H_SCOMP	W1	H_SCOMP
H_SCOMP#	W2	H_SCOMP#
H_CPURST#	B6	H_CPURST#
H_CPUSLP#	E5	H_CPUSLP#



Crestline MCH-QP20



U112B

- MCH_RSVD_1 P36
- MCH_RSVD_2 P37
- MCH_RSVD_3 R35
- MCH_RSVD_4 N35
- MCH_RSVD_5 AR12
- MCH_RSVD_6 AR13
- MCH_RSVD_7 AM12
- MCH_RSVD_8 AN13
- MCH_RSVD_9 J12
- MCH_RSVD_10 AR37
- MCH_RSVD_11 AM36
- MCH_RSVD_12 AL36
- MCH_RSVD_13 AM37
- MCH_RSVD_14 D20
- MCH_RSVD_20 H10
- MCH_RSVD_21 B51
- MCH_RSVD_22 BJ20
- MCH_RSVD_23 BK22
- MCH_RSVD_24 BF19
- MCH_RSVD_25 BH20
- MCH_RSVD_26 BK18
- MCH_RSVD_27 EL18
- MCH_RSVD_28 BF23
- MCH_RSVD_29 BG23
- MCH_RSVD_30 BC23
- MCH_RSVD_31 BD24
- MCH_RSVD_32 BJ29
- MCH_RSVD_33 BF24
- MCH_RSVD_34 BH39
- MCH_RSVD_35 AW20
- MCH_RSVD_36 BK20
- MCH_RSVD_37 C48
- MCH_RSVD_39 D47
- MCH_RSVD_40 B44
- MCH_RSVD_41 A35
- MCH_RSVD_42 B37
- MCH_RSVD_43 B36
- MCH_RSVD_44 B34
- MCH_RSVD_45 C34
- MCH_CFG_3 C21
- MCH_CFG_4 C23
- MCH_CFG_5 F23
- MCH_CFG_7 G23
- MCH_CFG_8 J20
- MCH_CFG_9 C20
- MCH_CFG_10 R24
- MCH_CFG_11 L23
- MCH_CFG_12 J23
- MCH_CFG_13 E23
- MCH_CFG_14 E20
- MCH_CFG_15 K23
- M20
- M24
- L32
- N32
- L35
- RSVD1
- RSVD2
- RSVD3
- RSVD4
- RSVD5
- RSVD6
- RSVD7
- RSVD8
- RSVD9
- RSVD10
- RSVD11
- RSVD12
- RSVD13
- RSVD14
- RSVD20
- RSVD21
- RSVD22
- RSVD23
- RSVD24
- RSVD25
- RSVD26
- RSVD27
- RSVD28
- RSVD29
- RSVD30
- RSVD31
- RSVD32
- RSVD33
- RSVD34
- RSVD35
- RSVD36
- LVDSA_DATA#3
- LVDSA_DATA3
- RSVD39
- RSVD40
- RSVD41
- RSVD42
- RSVD43
- RSVD44
- RSVD45
- CFG0
- CFG1
- CFG2
- CFG3
- CFG4
- CFG5
- CFG6
- CFG7
- CFG8
- CFG9
- CFG10
- CFG11
- CFG12
- CFG13
- CFG14
- CFG15
- CFG16
- CFG17
- CFG18
- CFG19
- CFG20
- SA_MA14
- SB_MA14
- RSVD39
- RSVD40
- RSVD41
- RSVD42
- RSVD43
- RSVD44
- RSVD45
- CFG17-31 internal pull-up
- CFG20-31 internal pull-down

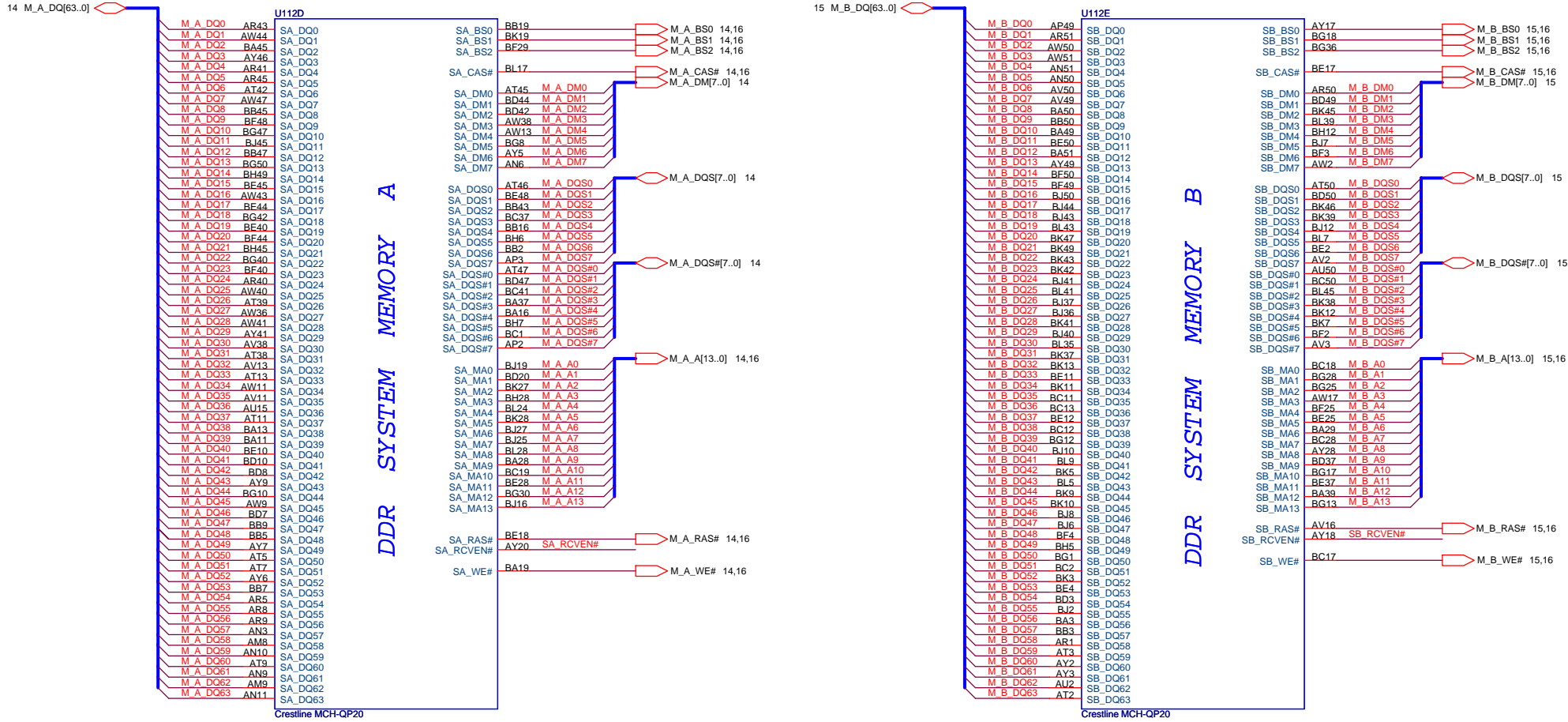
MCH_CFG_9 (PCIE Graphics Lane)
 Low = Reverse Lane
 High = Normal operation

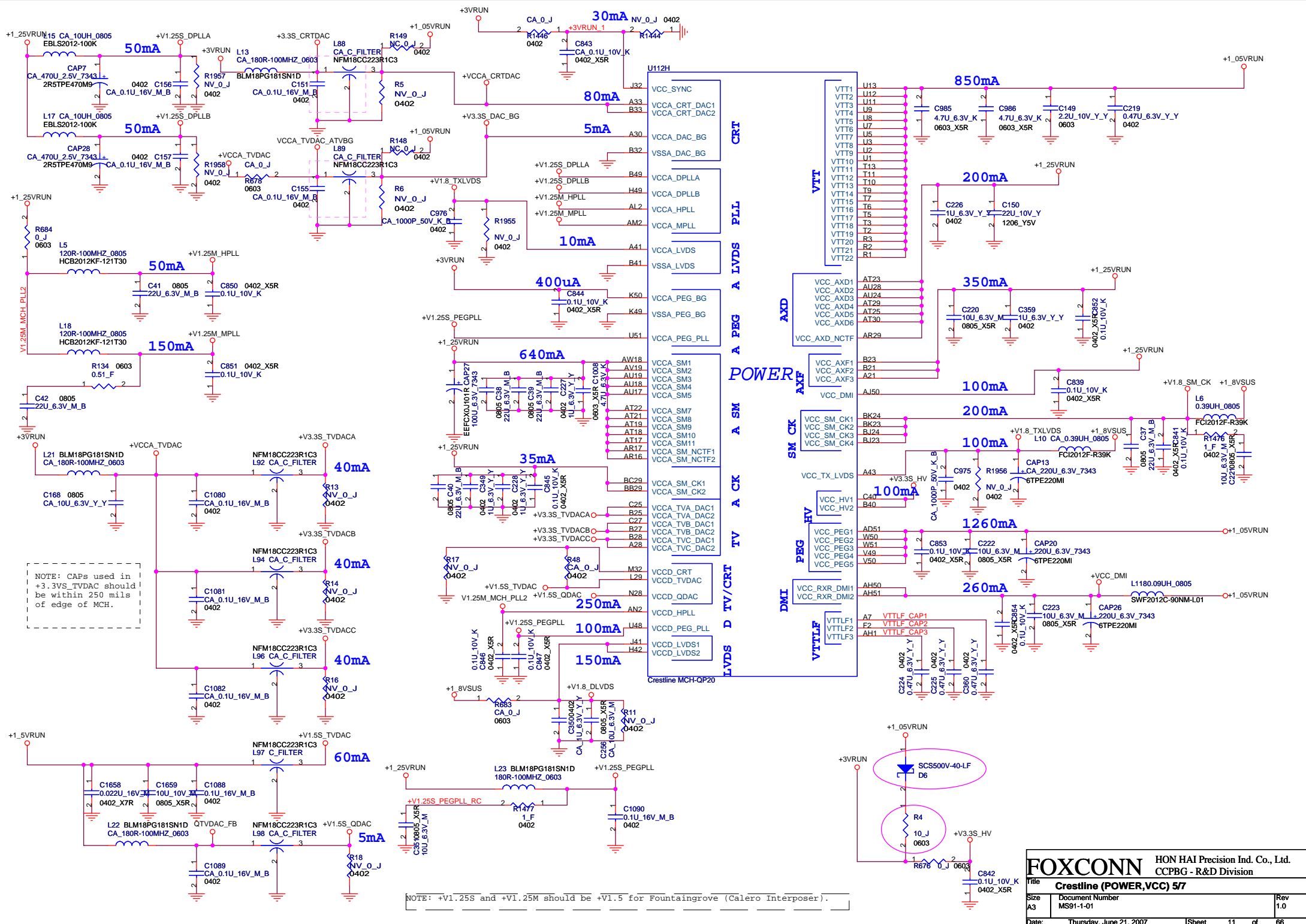
For layout convenience

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Crestline (DMI) 2/7

Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 8	of 66





NOTE: CAPs used in +3.3VS_TVDAC should be within 250 mils of edge of MCH.

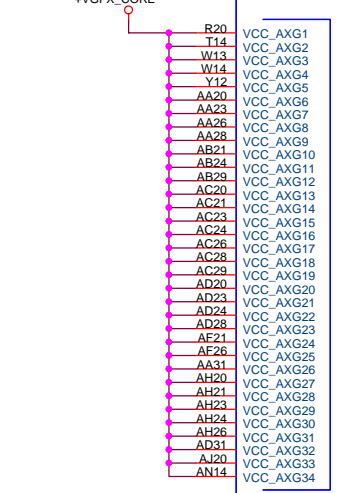
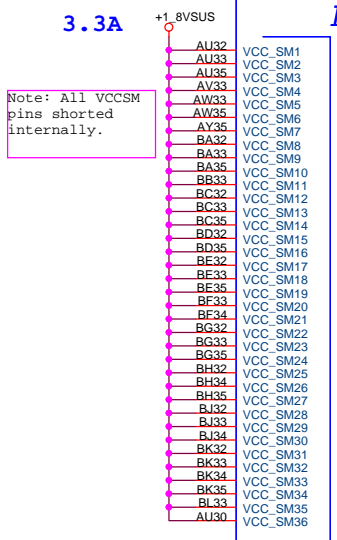
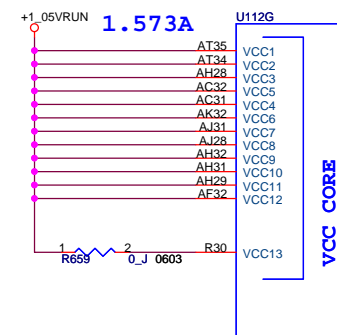
NOTE: +V1.25S and +V1.25M should be +V1.5 for Fountaingrove (Calero Interposer).

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

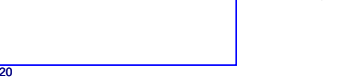
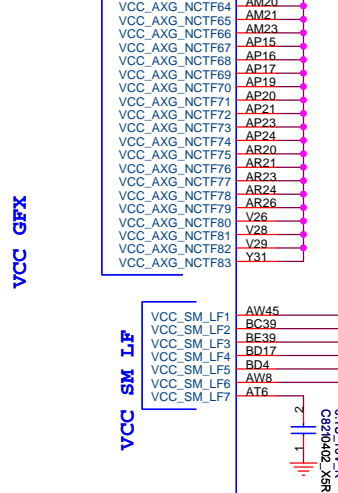
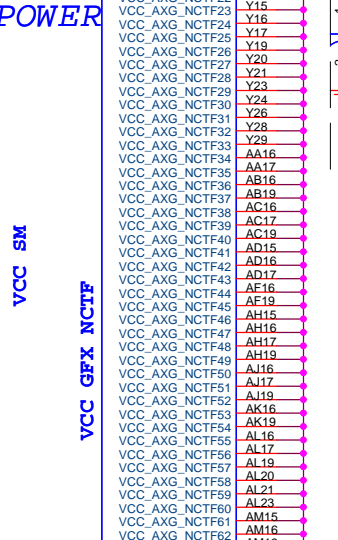
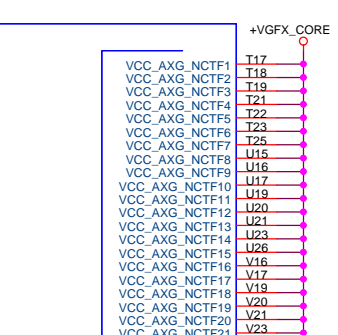
Title: **Crestline (POWER,VCC) 57**

Size	Document Number	Rev
A3	MS91-1-01	1.0

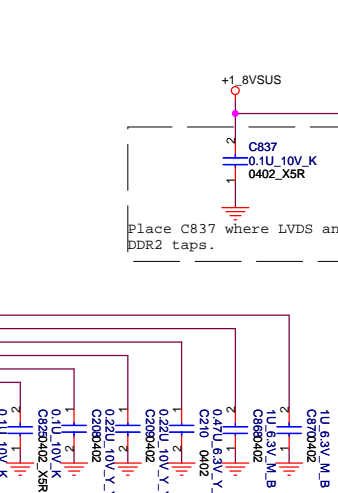
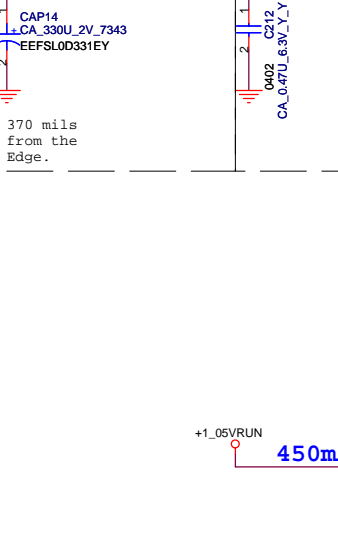
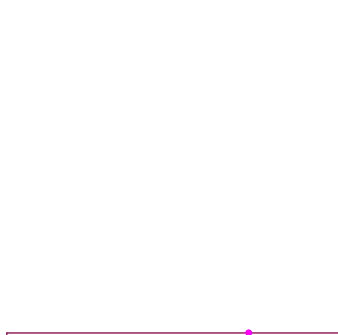
Date: Thursday, June 21, 2007 Sheet 11 of 66



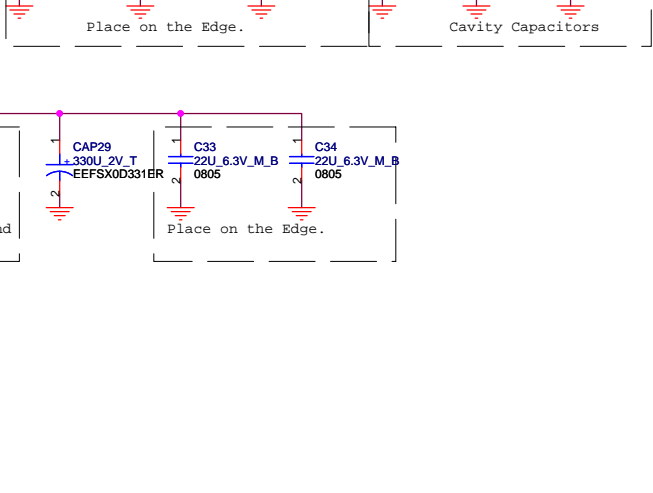
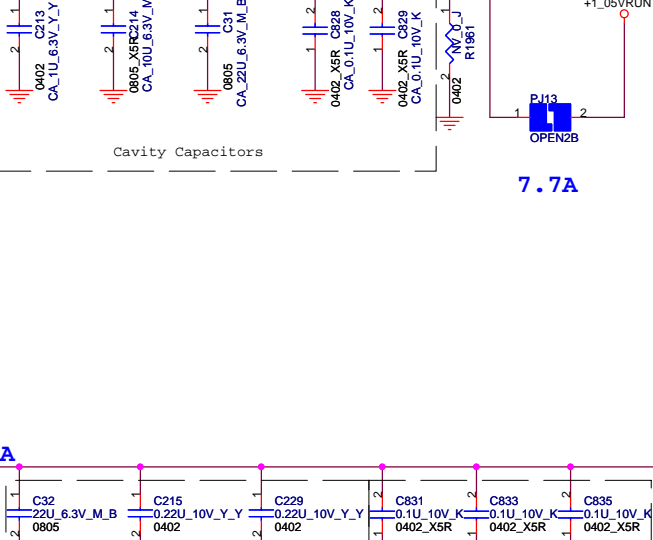
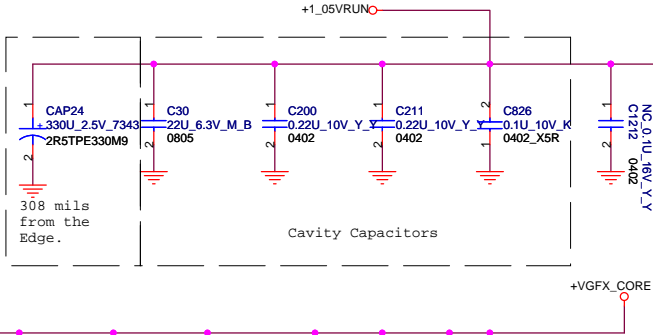
Crestline MCH-QP20



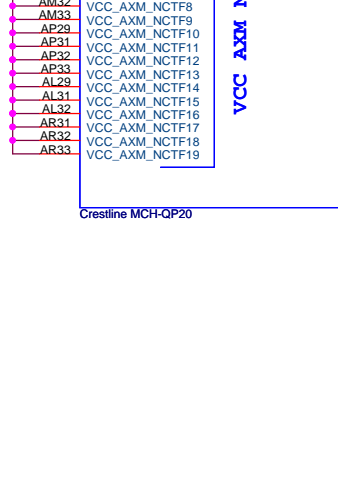
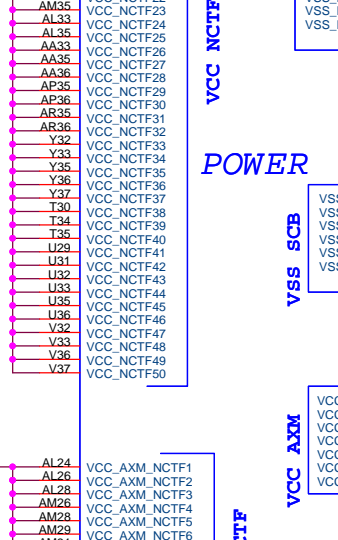
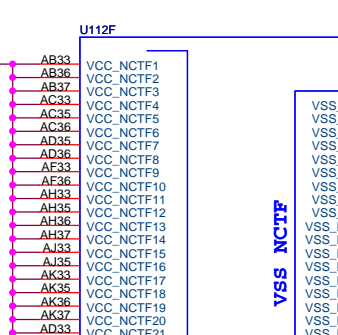
Crestline MCH-QP20



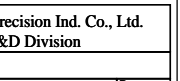
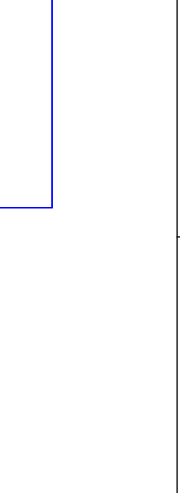
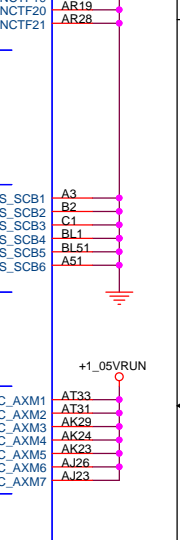
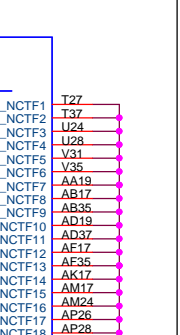
Crestline MCH-QP20



Crestline MCH-QP20



Crestline MCH-QP20



Crestline MCH-QP20

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Crestline (VCC CORE) 67			
Size A3	Document Number MS91-1-01	Rev 1.0	
Date: Thursday, June 21, 2007	Sheet 12	of 66	

U112I		U112J	
A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B43
AD26	VSS21	VSS120	B46
AD29	VSS22	VSS121	B5
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BH11
AN53	VSS72	VSS171	BH13
AN5	VSS73	VSS172	BH38
AN7	VSS74	VSS173	BH4
AP4	VSS75	VSS174	BH42
AP48	VSS76	VSS175	BH46
AP90	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C38
AW16	VSS99	VSS198	C41

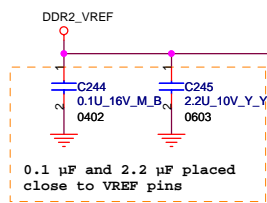
VSS

VSS

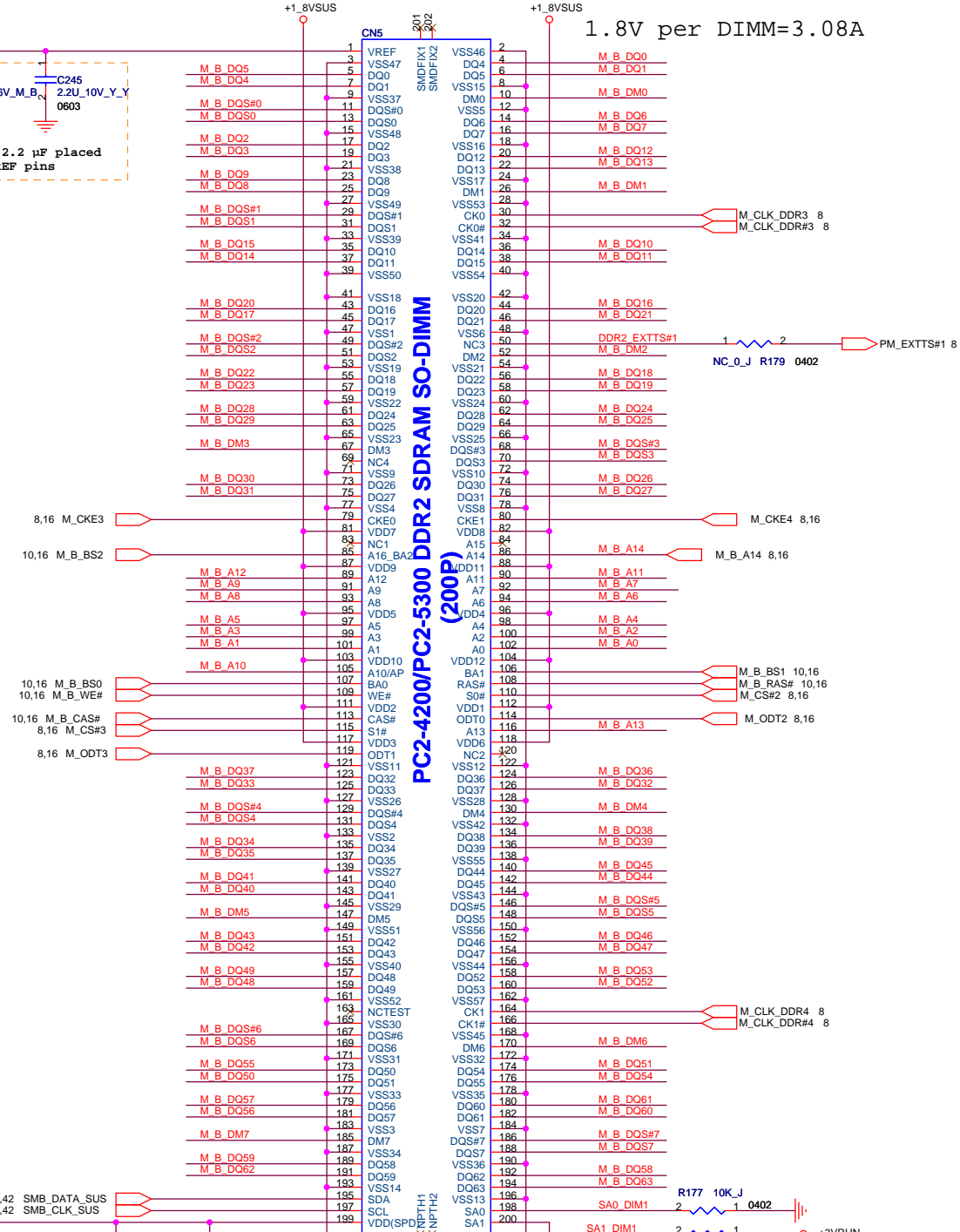
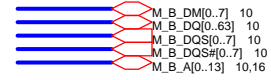
U112J		W11	
C46	VSS199	VSS287	W39
C50	VSS200	VSS288	W43
C7	VSS201	VSS289	W47
D13	VSS202	VSS290	W5
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	Y17
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y41
D45	VSS207	VSS295	Y45
D49	VSS208	VSS296	Y49
E10	VSS209	VSS297	Y5
E16	VSS210	VSS298	Y50
E24	VSS211	VSS299	Y11
E28	VSS212	VSS300	P29
E32	VSS213	VSS301	T29
E47	VSS214	VSS302	T31
F19	VSS215	VSS303	T33
F36	VSS216	VSS304	R28
F4	VSS217	VSS305	
F40	VSS218		
F50	VSS219		
G1	VSS220		
G13	VSS221	VSS306	AA32
G16	VSS222	VSS307	AB32
G19	VSS223	VSS308	AD32
G24	VSS224	VSS309	AF28
G28	VSS225	VSS310	AT27
G29	VSS226	VSS311	AV25
G33	VSS227	VSS312	H50
G42	VSS228		
G45	VSS229		
G48	VSS230		
G8	VSS231		
H24	VSS232		
H28	VSS233		
H4	VSS234		
H45	VSS235		
J11	VSS236		
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline MCH-QP20

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Crestline (VSS) 7/7		CCPBG - R&D Division	
Title			
Size	Document Number	Rev	
A3	MS91-1-01	1.0	
Date:	Thursday, June 21, 2007	Sheet	13 of 66



1.8V per DIMM=3.08A

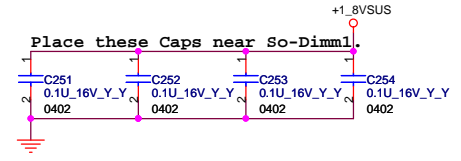
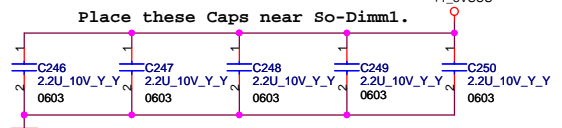


PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

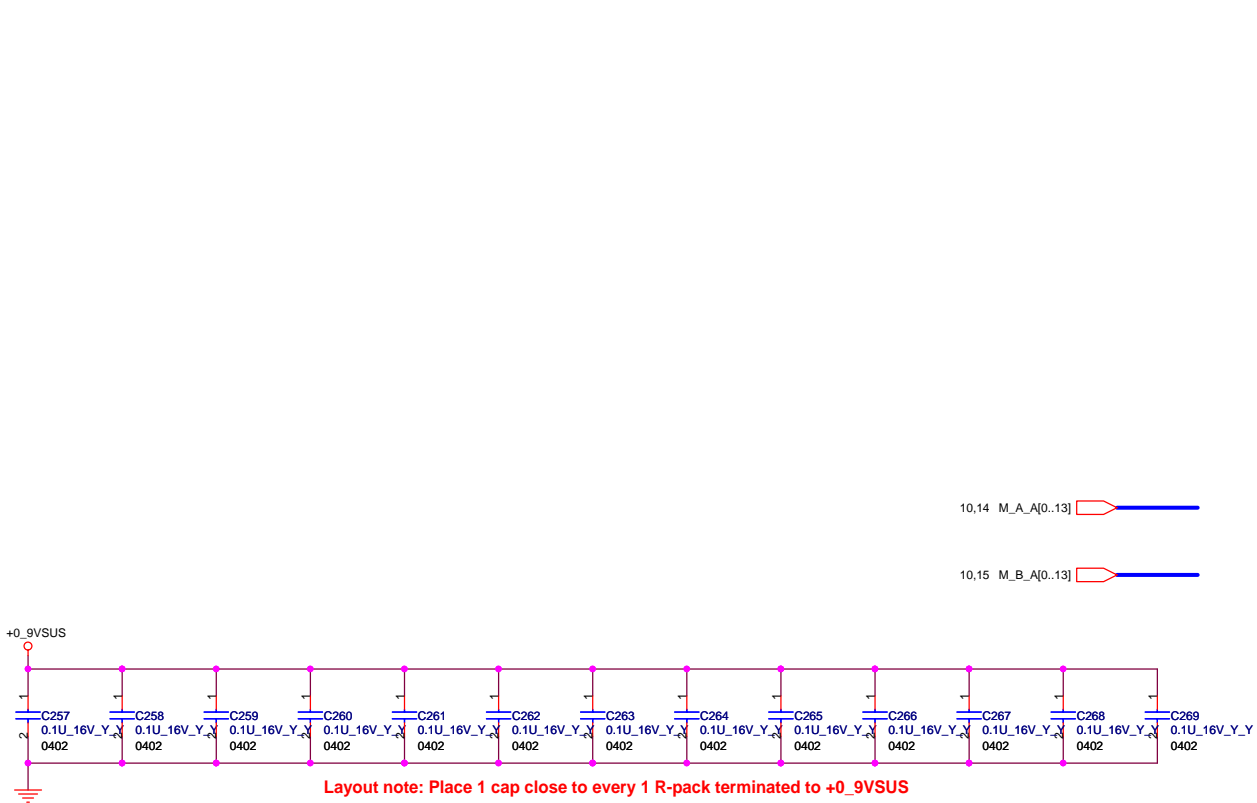
DIMM_1

SMBus Address: A4(W)/A5(R)

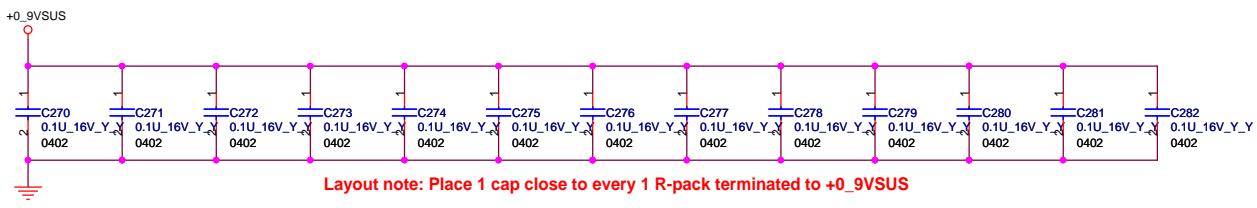
DIMM_1 is placed farther from the GMCH than DIMM_0



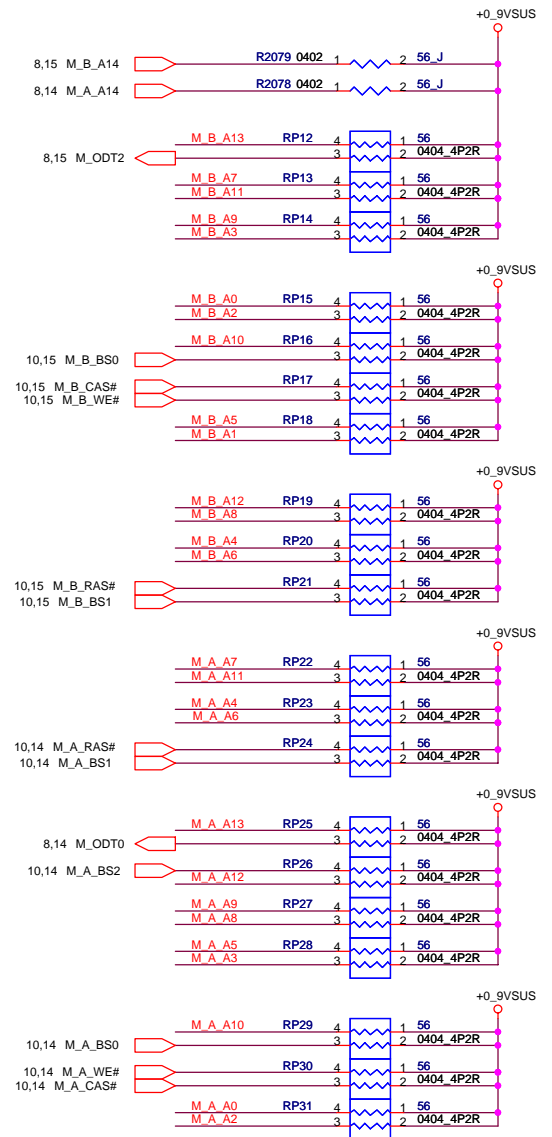
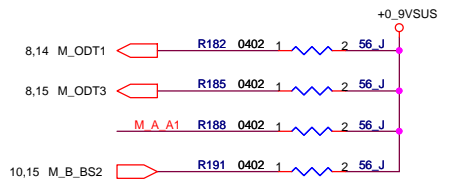
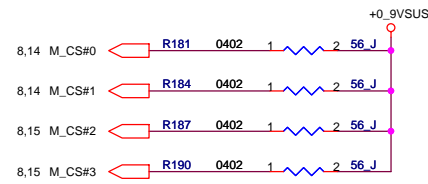
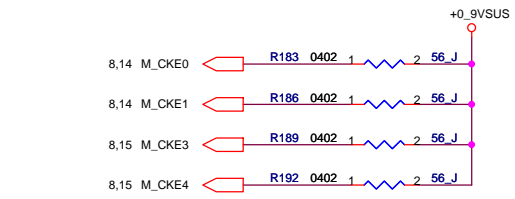
FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: DDR(I)SO-DIMM_1			
Size A3	Document Number: MS91-1-01	Rev 1.0	
Date: Thursday, June 21, 2007	Sheet 15	of 66	

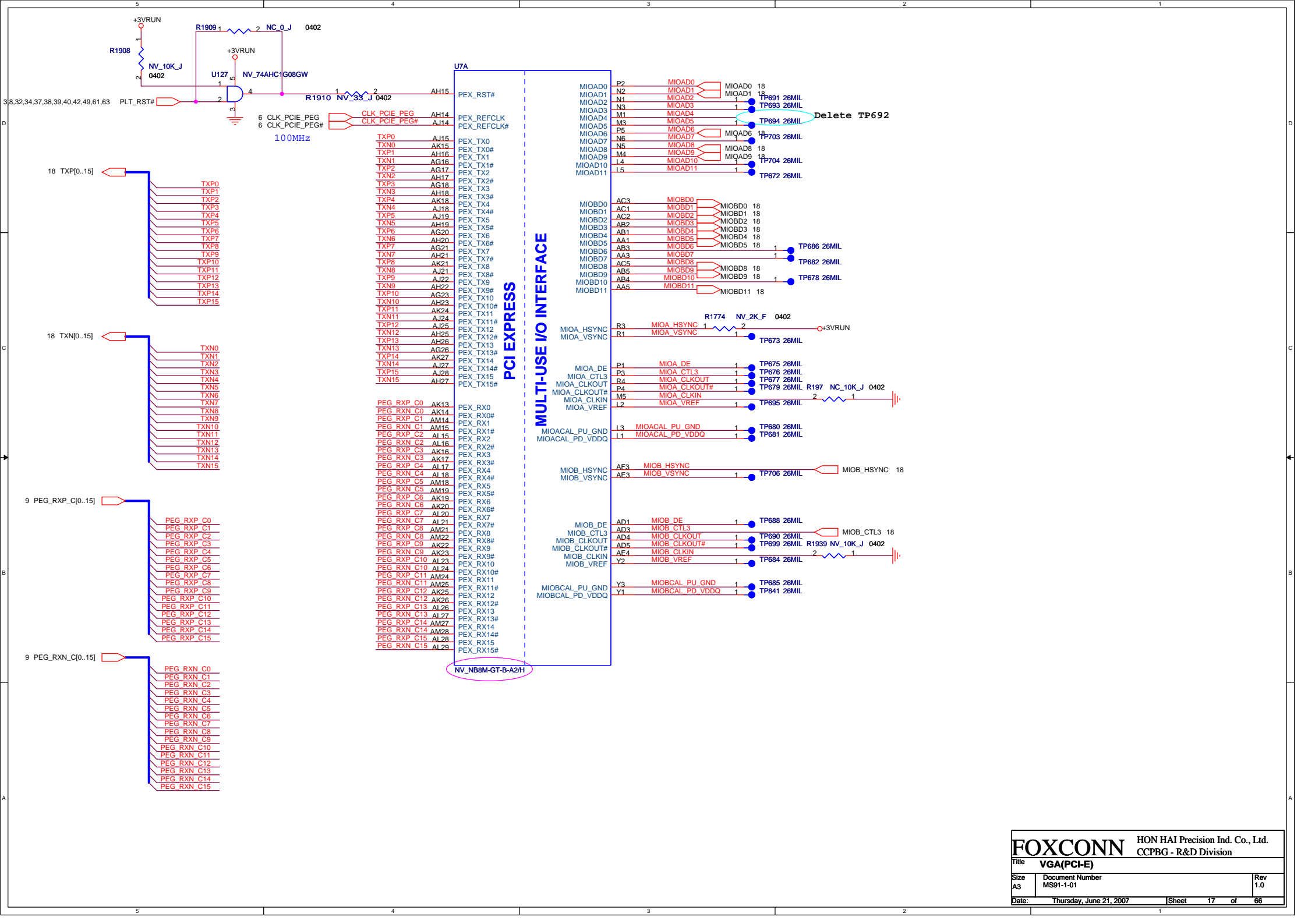


Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9VSUS



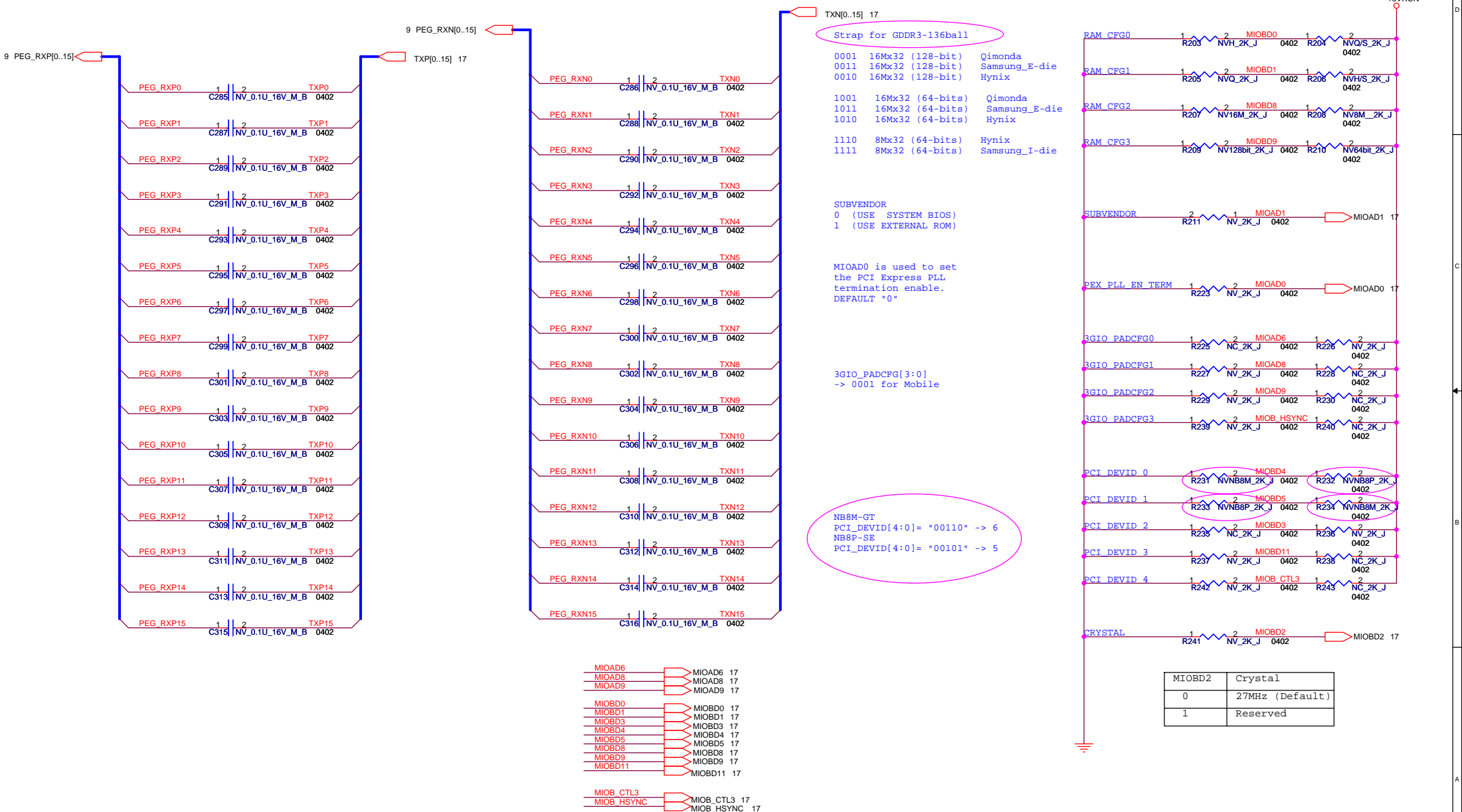
Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9VSUS



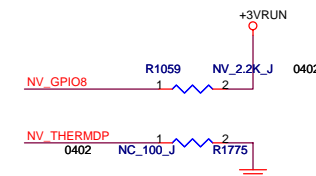
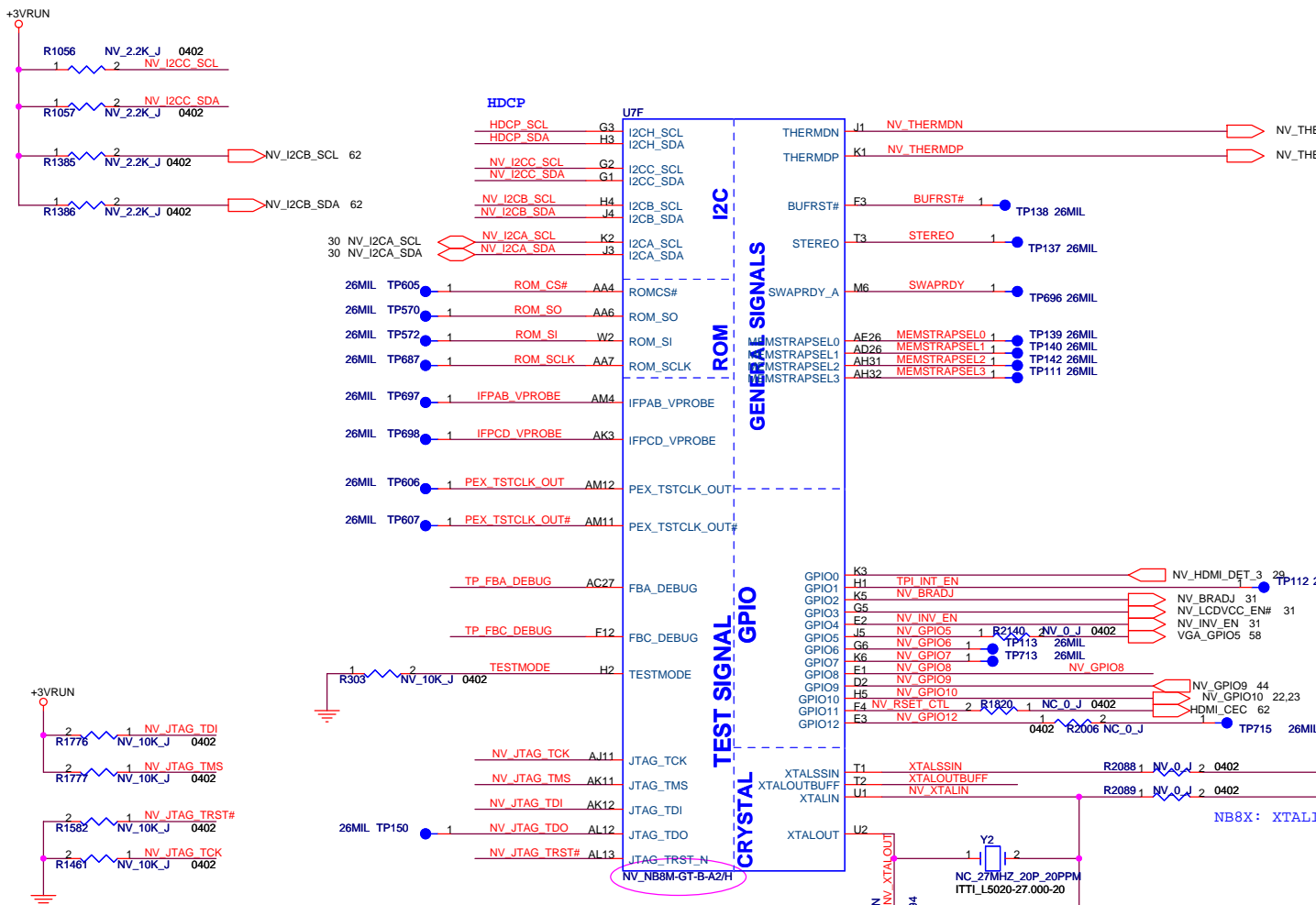


SKU	HH			H			M	
Vendor	Hynix	Qimonda	Samsung	Qimonda	Samsung	Hynix	Samsung	Hynix
Vendor PN	HY5RS123235BFP-14	HYB18H512321BF-14	K4J52324QE-BC14	HYB18H512321BF-14	K4J52324QE-BC14	HY5RS123235BFP-14	K4J55323QI-BC14	HY5RS573225BFP-14
H.H PN	13-HY5RS12-3001	13-HYB18H5-3003	13-K4J5232-3001	13-HYB18H5-3003	13-K4J5232-3001	13-HY5RS12-3001	13-K4J5532-3003	13-HY5RS57-3003
Configuration	NB8X with 4pcs (16Mx32) GDDR3			NB8M-GT with 2pcs (16Mx32) GDDR3			NB8M-GT with 2pcs (8Mx32) GDDR3	
LOCATION	Stuff U11,U12,U13,U14			Stuff U11,U12; No stuff U13,U14			Stuff U11,U12; No stuff U13,U14	

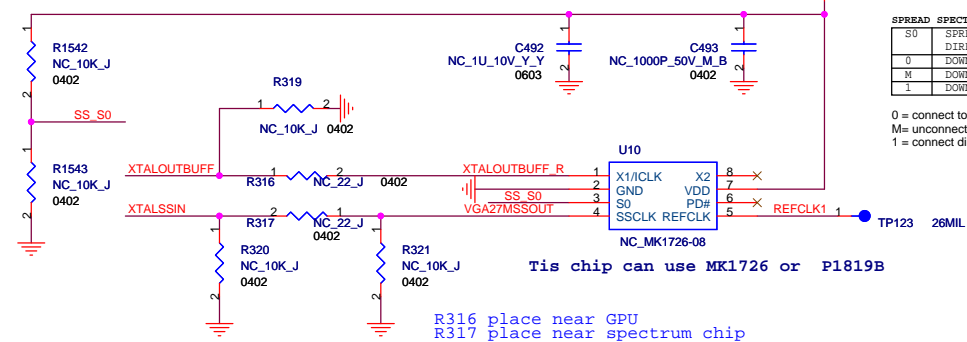
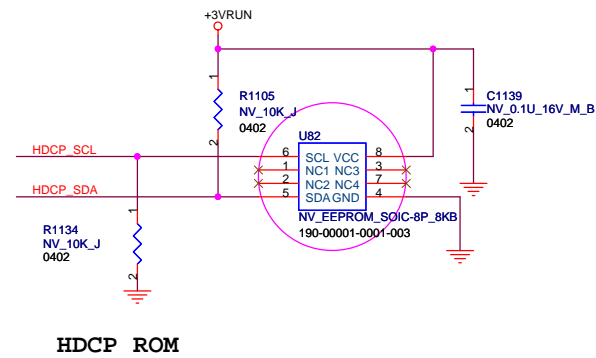
FAB: TV Mode Strap no use, remove.
(MIOAD7, MIOAD10, MIOBD6)



MIOBD2	Crystal
0	27MHz (Default)
1	Reserved



	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	HDMI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) Active High
GPIO3	O	No	Panel Power Enable Active Low
GPIO4	O	Yes	Panel Backlight On/Off Active High
GPIO5	O	Yes	NV_VDD VID0
GPIO6	O	Yes	NV_VDD VID1
GPIO7	O	Yes	FBVDD VID0
GPIO8	OD	No	THERM Active Low
GPIO9	OD	No	ALERT Active Low
GPIO10	O	No	TMDS LINK SELECT
GPIO11	O	No(Low)	CEC no function yet
GPIO12	I	--	AC/BATT#



SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

SPREAD SPECTRUM SETTING FOR P1819B

SRS	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

0 = connect to GND
M = unconnected
1 = connect directly to VDD

nVidia support Down -1.25%

Tis chip can use MK1726 or P1819B

R316 place near GPU
R317 place near spectrum chip

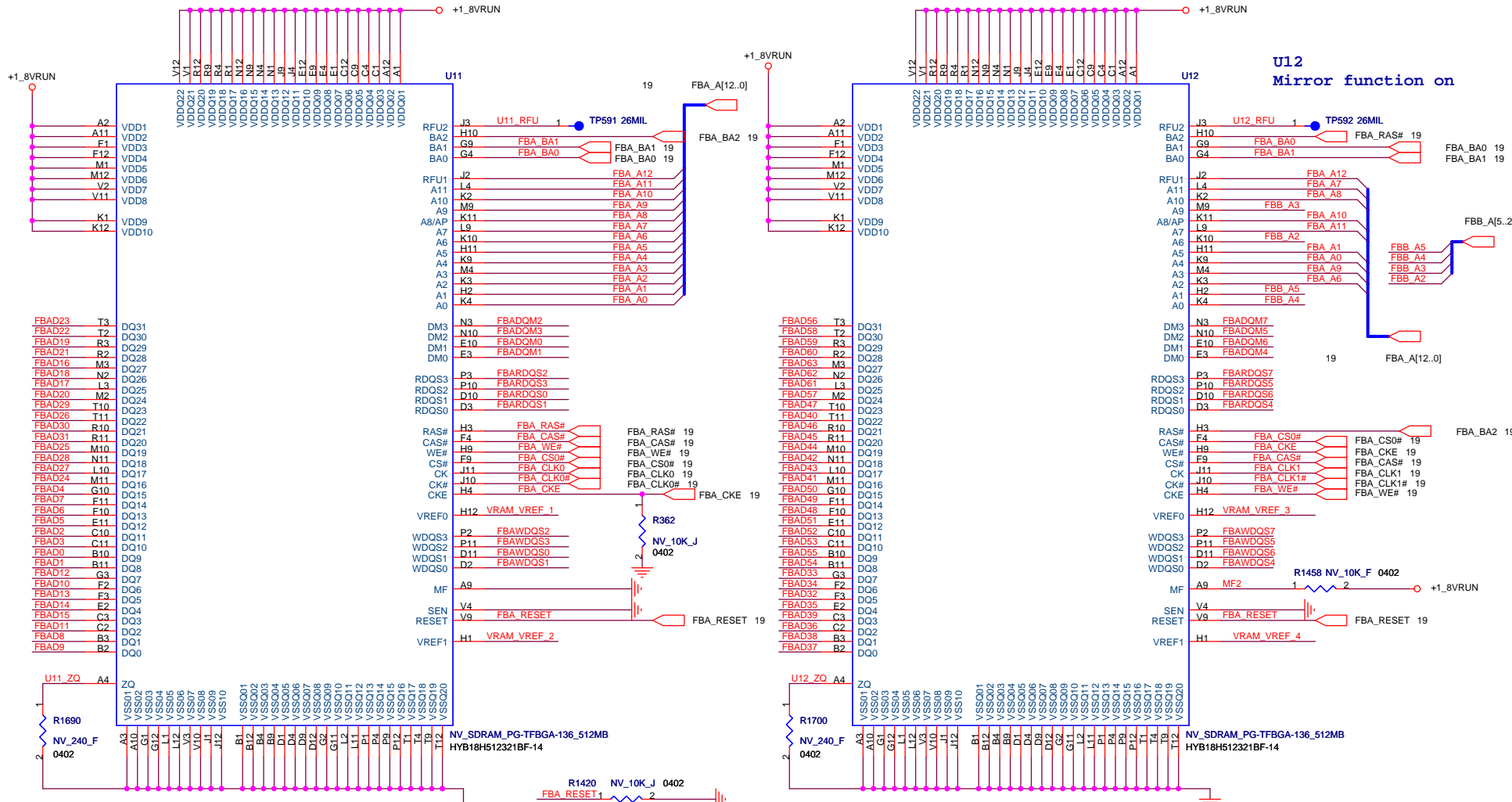
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **VGA(MULTIUSE)**

Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 20	of 66



DACA	VGA-CRF	I2CA	DACB	S-VIDEO
DACA-RED	R	AL10	DACB-RED	C
DACA-GREEN	G	AG13	DACB-GREEN	Y
DACA-BLUE	B	AM10	DACB-BLUE	
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCLK	SDA		
	VGA-DDDATA			

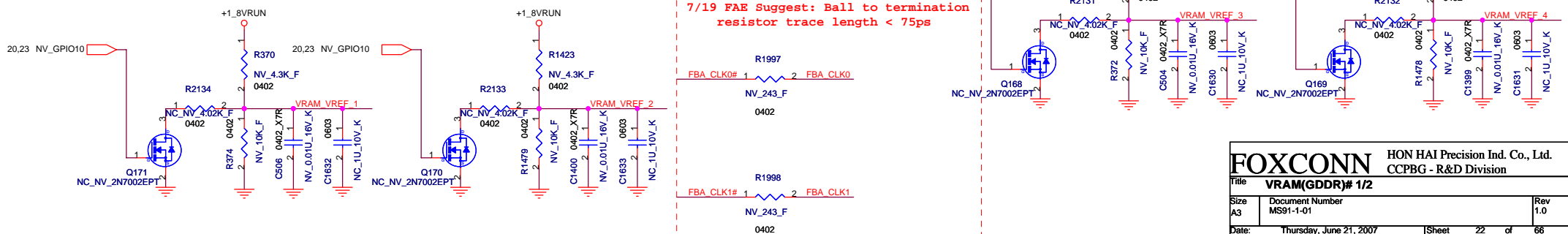


- FBAD[0:63] 19
- FBADQM[7:0] 19
- FBARDQS[7:0] 19
- FBAWDQS[7:0] 19

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

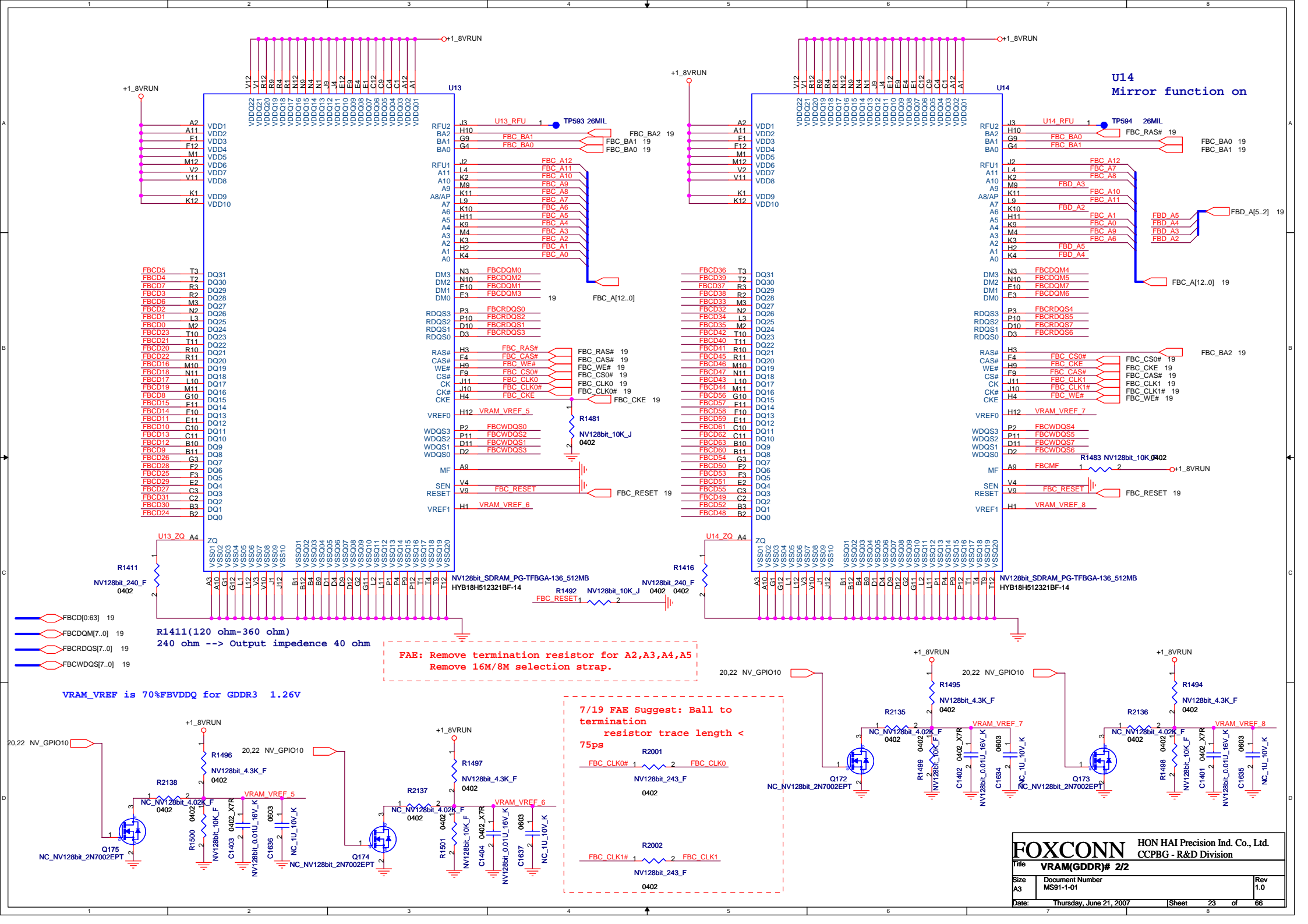
FAE: Remove termination resistor for A2,A3,A4,A5
Remove 16M/8M selection strap.

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps



U12 Mirror function on

FOXCONN			HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title VRAM(GDDR)# 1/2					
Size	Document Number				Rev
A3	MS91-1-01				1.0
Date:	Thursday, June 21, 2007	Sheet	22	of	66



U14 Mirror function on

- FBCD5 T3 DQ31
- FBCD4 T2 DQ30
- FBCD7 R3 DQ29
- FBCD3 R2 DQ28
- FBCD6 M3 DQ27
- FBCD2 N2 DQ26
- FBCD1 L3 DQ25
- FBCD9 M2 DQ24
- FBCD23 T10 DQ23
- FBCD21 T11 DQ22
- FBCD20 R10 DQ21
- FBCD22 R11 DQ20
- FBCD16 M10 DQ19
- FBCD18 N11 DQ18
- FBCD17 L10 DQ17
- FBCD19 M11 DQ16
- FBCD8 G10 DQ15
- FBCD15 E11 DQ14
- FBCD14 F10 DQ13
- FBCD11 E11 DQ12
- FBCD10 C10 DQ11
- FBCD13 B10 DQ10
- FBCD12 B10 DQ09
- FBCD9 B11 DQ08
- FBCD26 G3 DQ07
- FBCD28 F2 DQ06
- FBCD25 F3 DQ05
- FBCD29 E2 DQ04
- FBCD27 C3 DQ03
- FBCD31 C2 DQ02
- FBCD30 B3 DQ01
- FBCD24 B2 DQ00

- FBCD[0:63] 19
- FBCDQM[7:0] 19
- FBCRDQS[7:0] 19
- FBCWDQS[7:0] 19

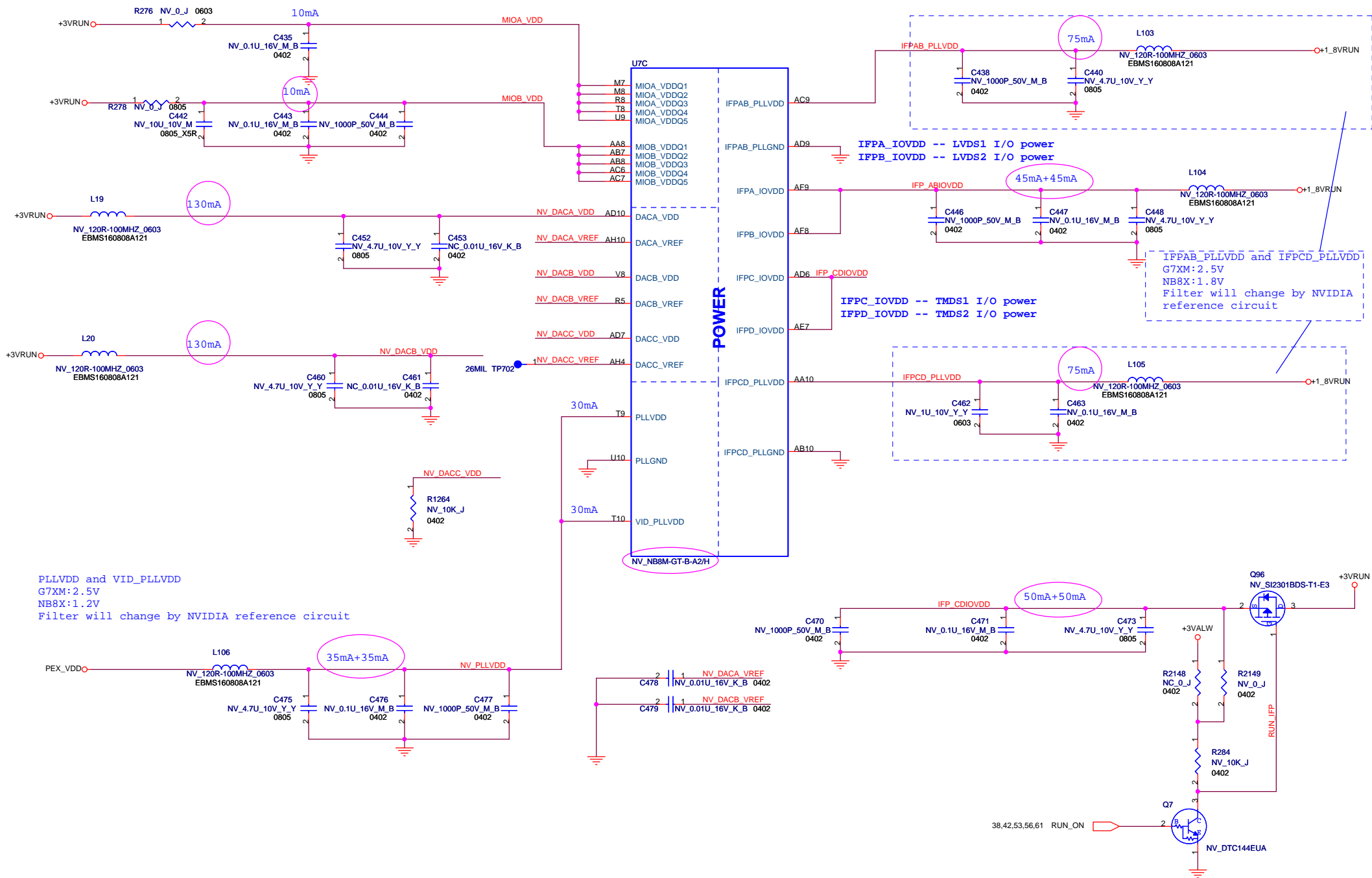
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

**FAE: Remove termination resistor for A2,A3,A4,A5
Remove 16M/8M selection strap.**

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

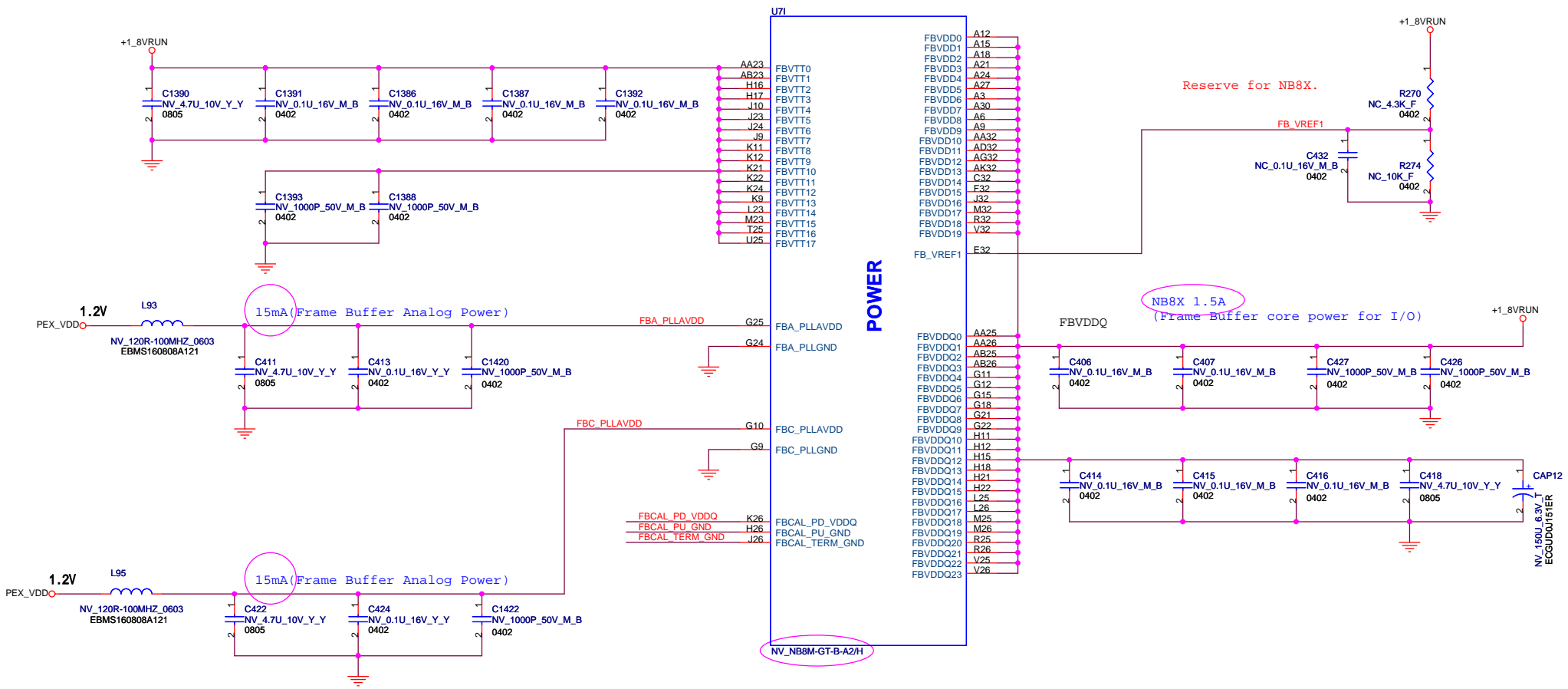
FBC CLK0# 1 2 FBC CLK0

FBC CLK1# 1 2 FBC CLK1



PLLVDD and VID_PLLVDD
 G7XM:2.5V
 NB8X:1.2V
 Filter will change by NVIDIA reference circuit

IFPAB_PLLVDD and IFPCD_PLLVDD
 G7XM:2.5V
 NB8X:1.8V
 Filter will change by NVIDIA reference circuit



U71

FBVTT0
FBVTT1
FBVTT2
FBVTT3
FBVTT4
FBVTT5
FBVTT6
FBVTT7
FBVTT8
FBVTT9
FBVTT10
FBVTT11
FBVTT12
FBVTT13
FBVTT14
FBVTT15
FBVTT16
FBVTT17

FBVDD0
FBVDD1
FBVDD2
FBVDD3
FBVDD4
FBVDD5
FBVDD6
FBVDD7
FBVDD8
FBVDD9
FBVDD10
FBVDD11
FBVDD12
FBVDD13
FBVDD14
FBVDD15
FBVDD16
FBVDD17
FBVDD18
FBVDD19

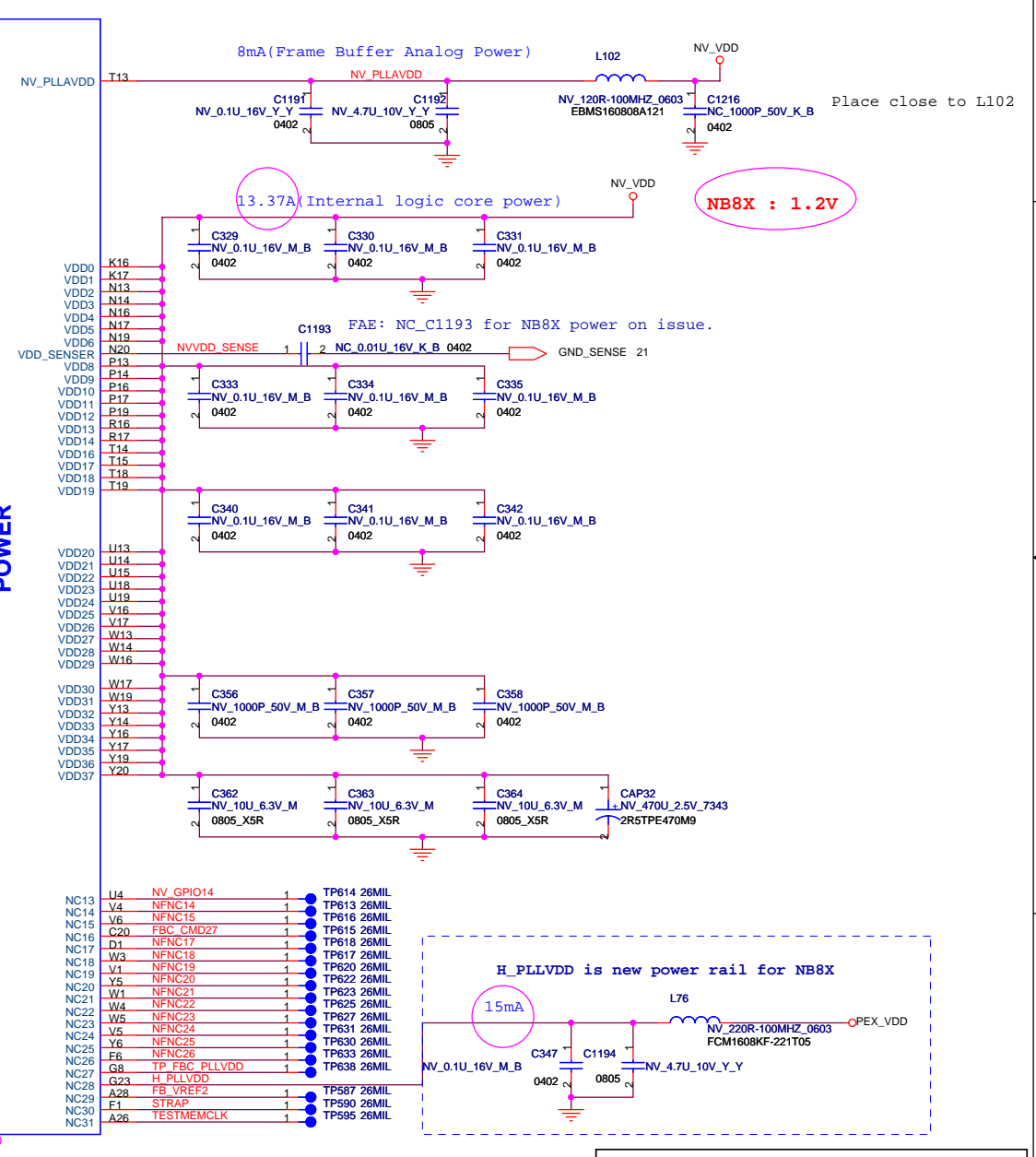
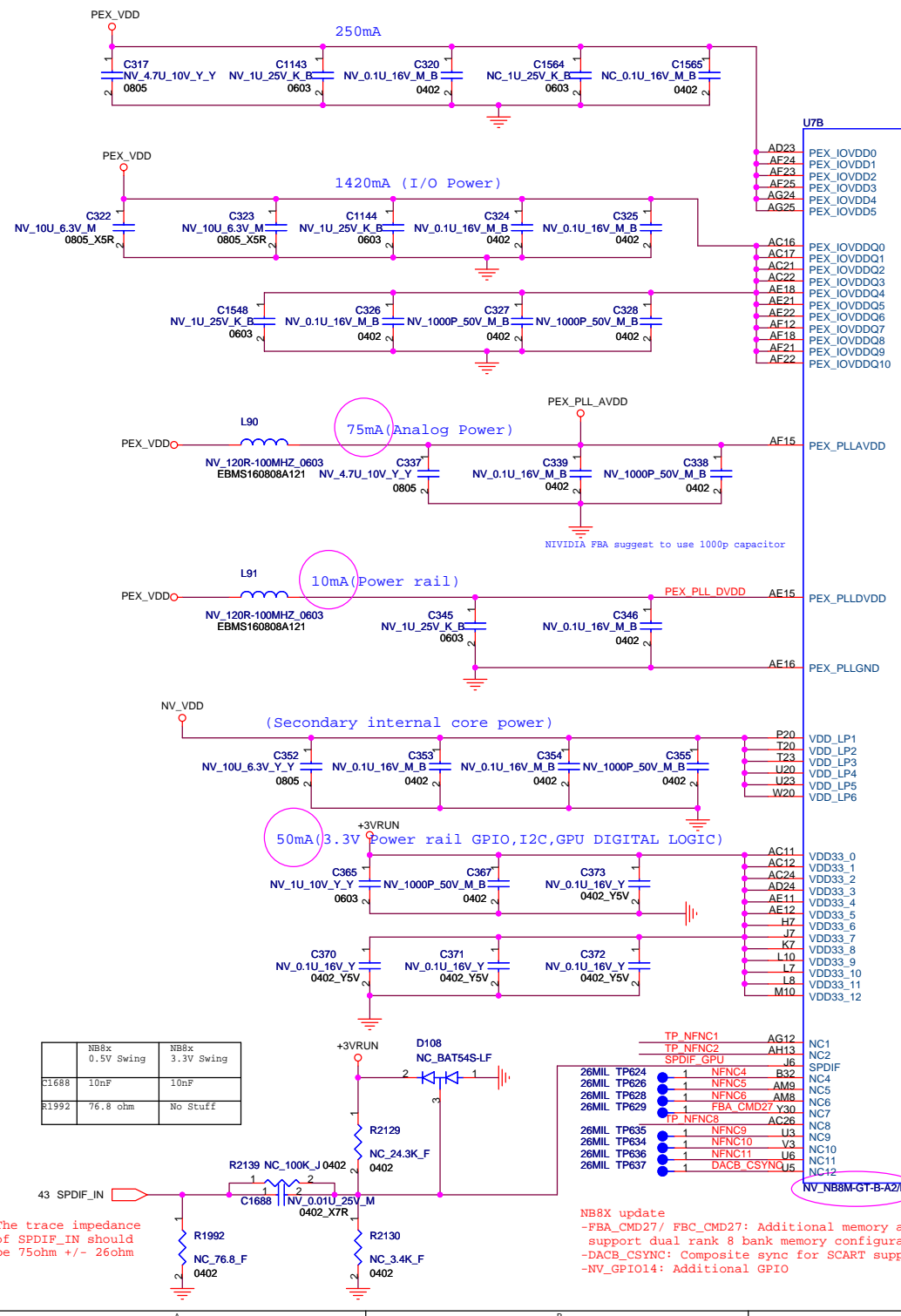
FBVDDQ0
FBVDDQ1
FBVDDQ2
FBVDDQ3
FBVDDQ4
FBVDDQ5
FBVDDQ6
FBVDDQ7
FBVDDQ8
FBVDDQ9
FBVDDQ10
FBVDDQ11
FBVDDQ12
FBVDDQ13
FBVDDQ14
FBVDDQ15
FBVDDQ16
FBVDDQ17
FBVDDQ18
FBVDDQ19
FBVDDQ20
FBVDDQ21
FBVDDQ22
FBVDDQ23

FBA_PLLAVDD
FBA_PLLGND
FBC_PLLAVDD
FBC_PLLGND
FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND

POWER

NV_NB8M-GT-B-A2/H

	GDDR3/BGA1.36
FBCAL_PD_VDDQ	45.3 ohm
FBCAL_PU_GND	24.9 ohm
FBCAL_TERM_GND	40.2 ohm

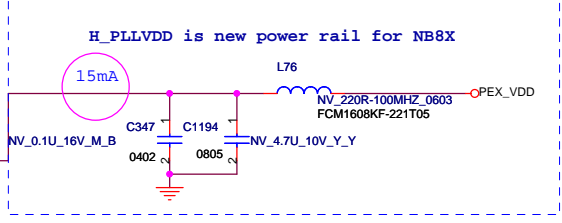


	NB8x 0.5V Swing	NB8x 3.3V Swing
C1688	10nF	10nF
R1992	76.8 ohm	No Stuff

- TP NFNC1 AG12
- TP NFNC2 AH13
- TP NFNC3 SPDIF_GPU
- TP NFNC4 B32
- TP NFNC5 AM3
- TP NFNC6 AM8
- TP NFNC7 FBA_CMD27 Y30
- TP NFNC8 AC26
- TP NFNC9 U3
- TP NFNC10 V3
- TP NFNC11 U8
- TP DACB_CSQNCJ5

The trace impedance of SPDIF_IN should be 75ohm +/- 26ohm

NB8X update
 -FBA_CMD27/ FBC_CMD27: Additional memory address bit to support dual rank 8 bank memory configuration.
 -DACB_CSQNC: Composite sync for SCART support
 -NV_GPIO14: Additional GPIO

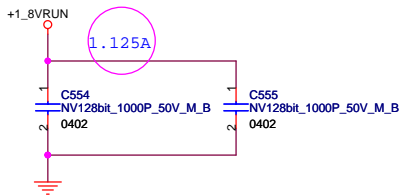
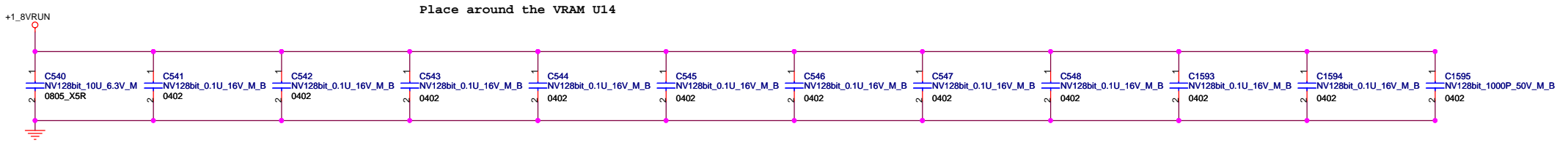
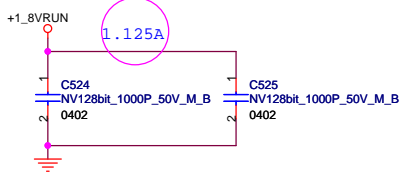
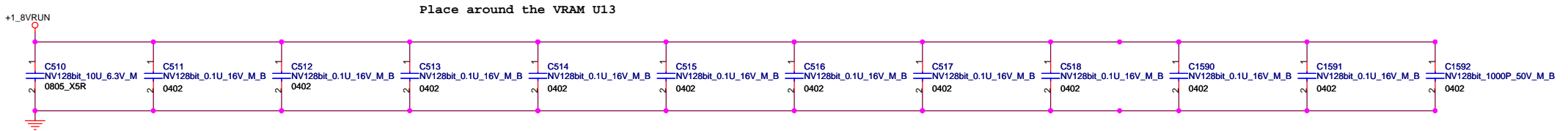


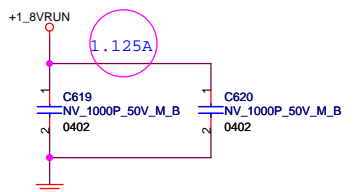
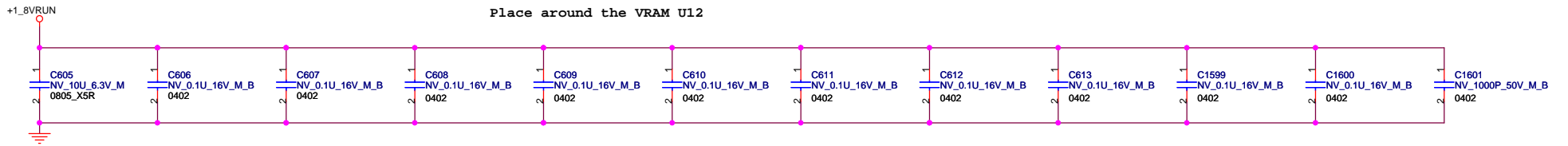
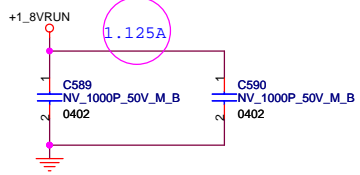
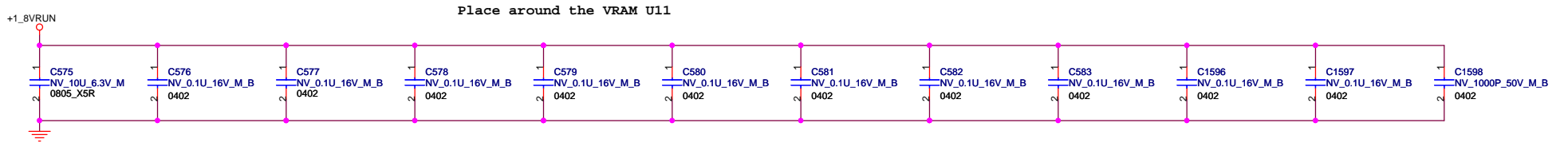
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **VGA(POWER) 3/3**

Size A3	Document Number MS91-1-01	Rev 1.0
---------	---------------------------	---------

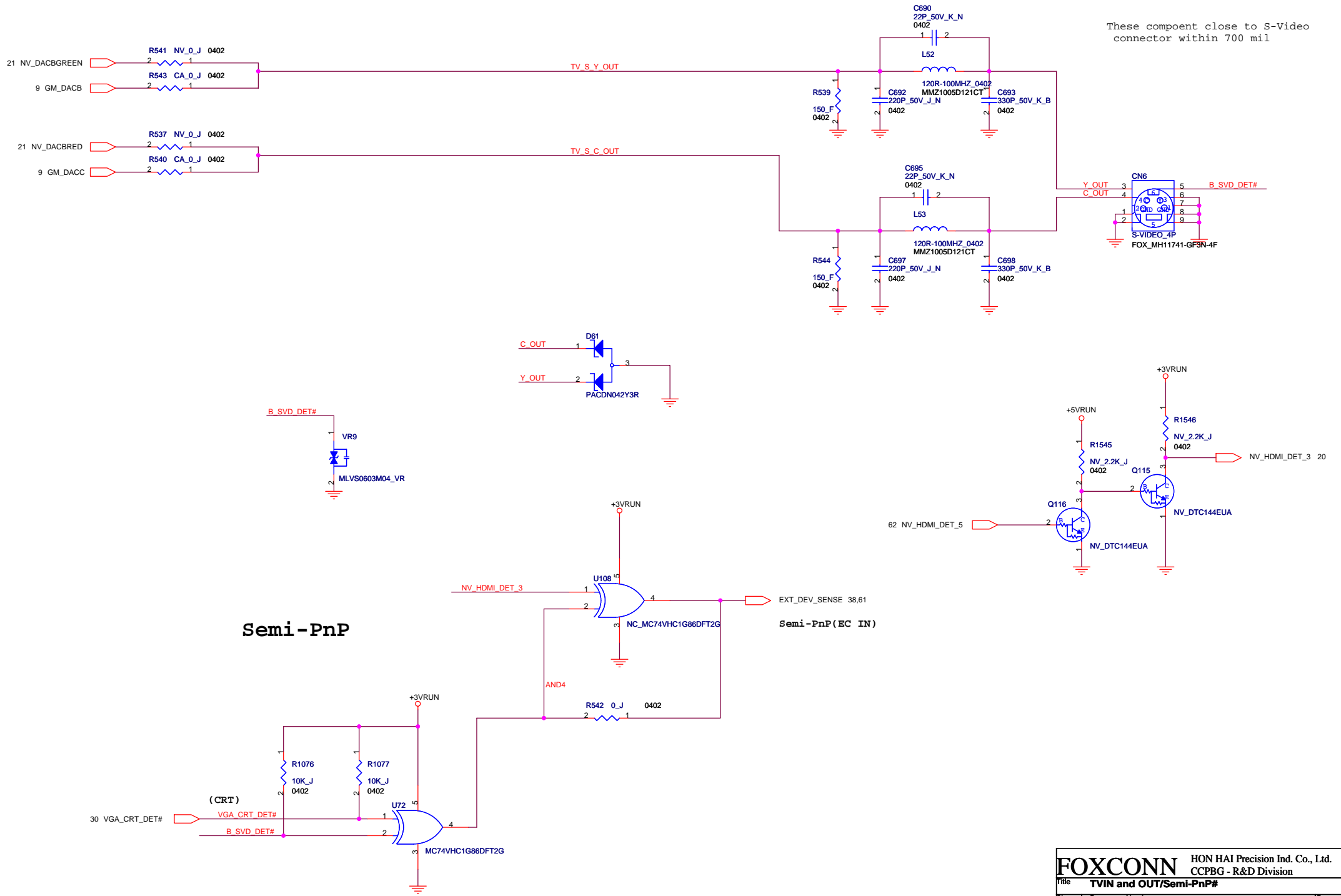
Date: Thursday, June 21, 2007 Sheet 26 of 66





S-VIDEO

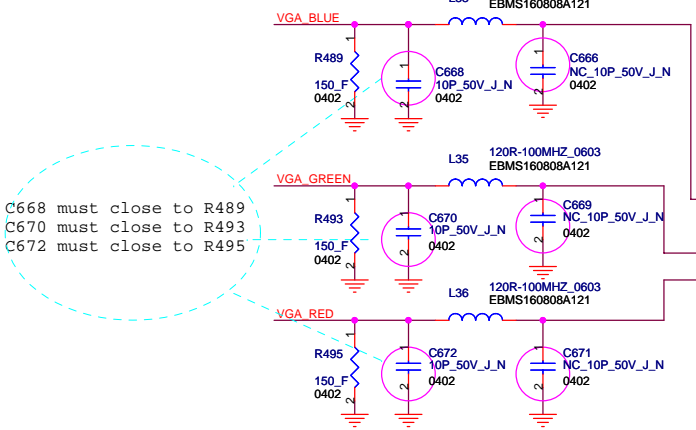
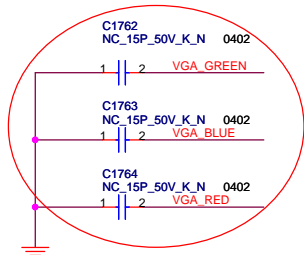
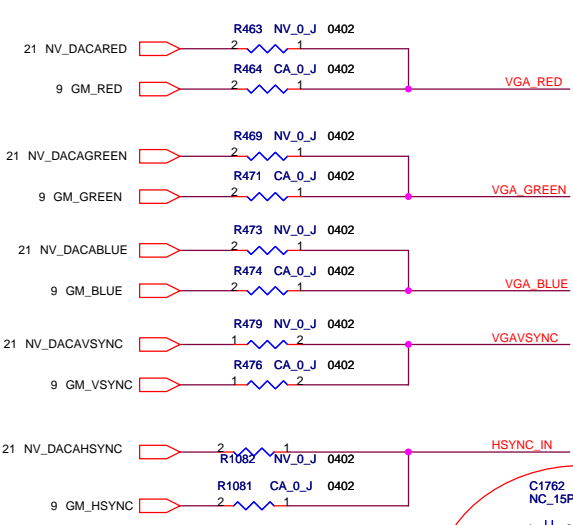
These components close to S-Video connector within 700 mil



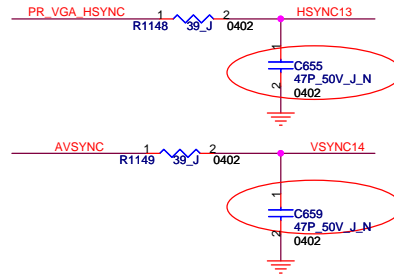
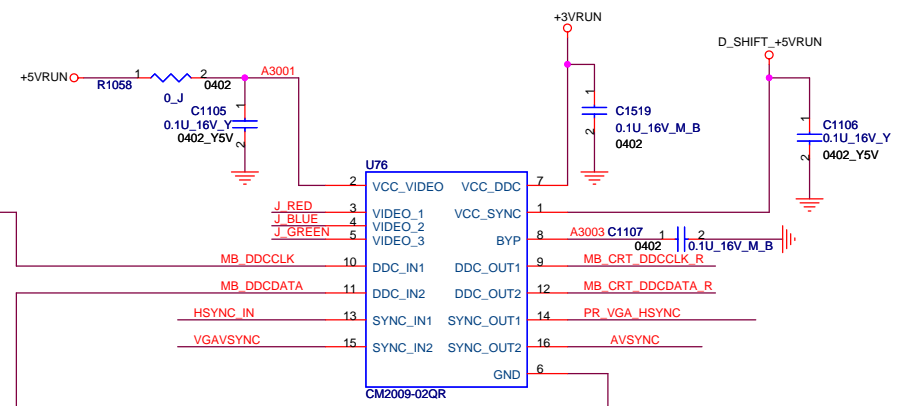
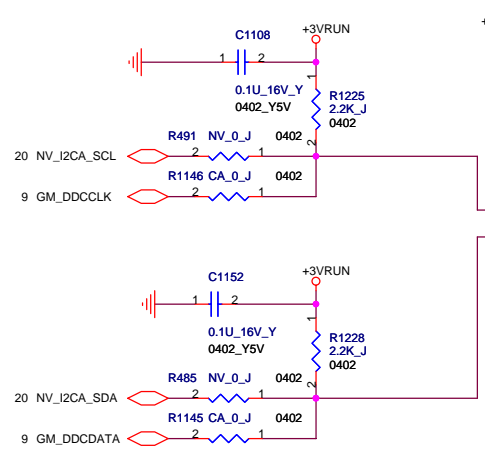
Semi-PnP

Semi-PnP (EC IN)

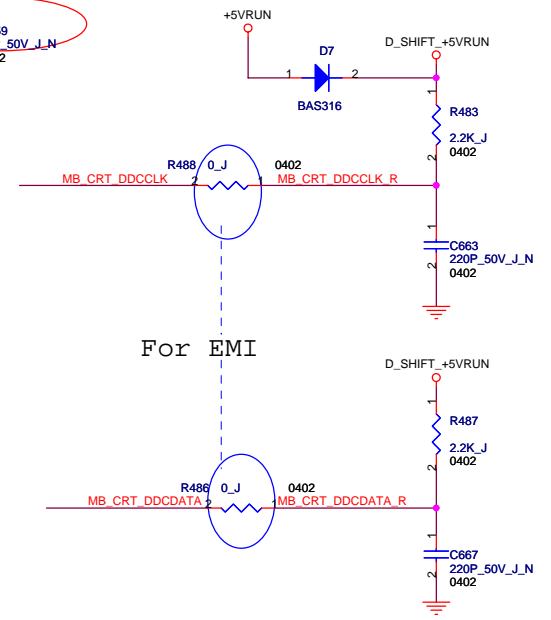
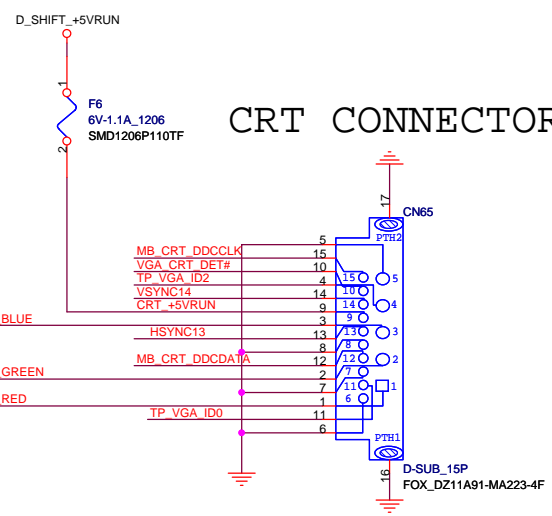
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title TVIN and OUT/Semi-PnP#		
Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 29	of 66



C668 must close to R489
 C670 must close to R493
 C672 must close to R495



CRT CONNECTOR



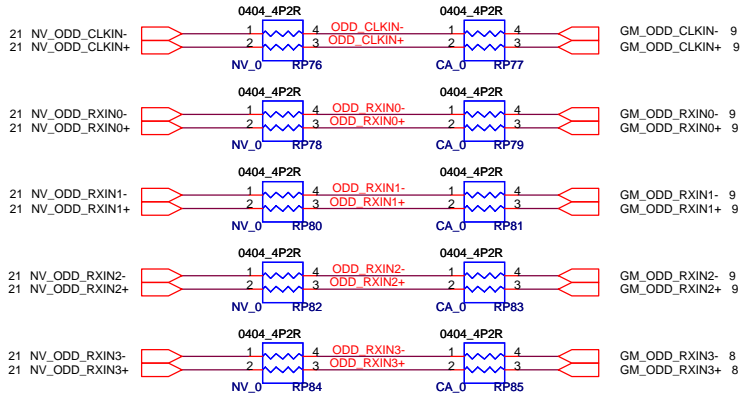
FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title CRT		
Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 30	of 66

LVDS

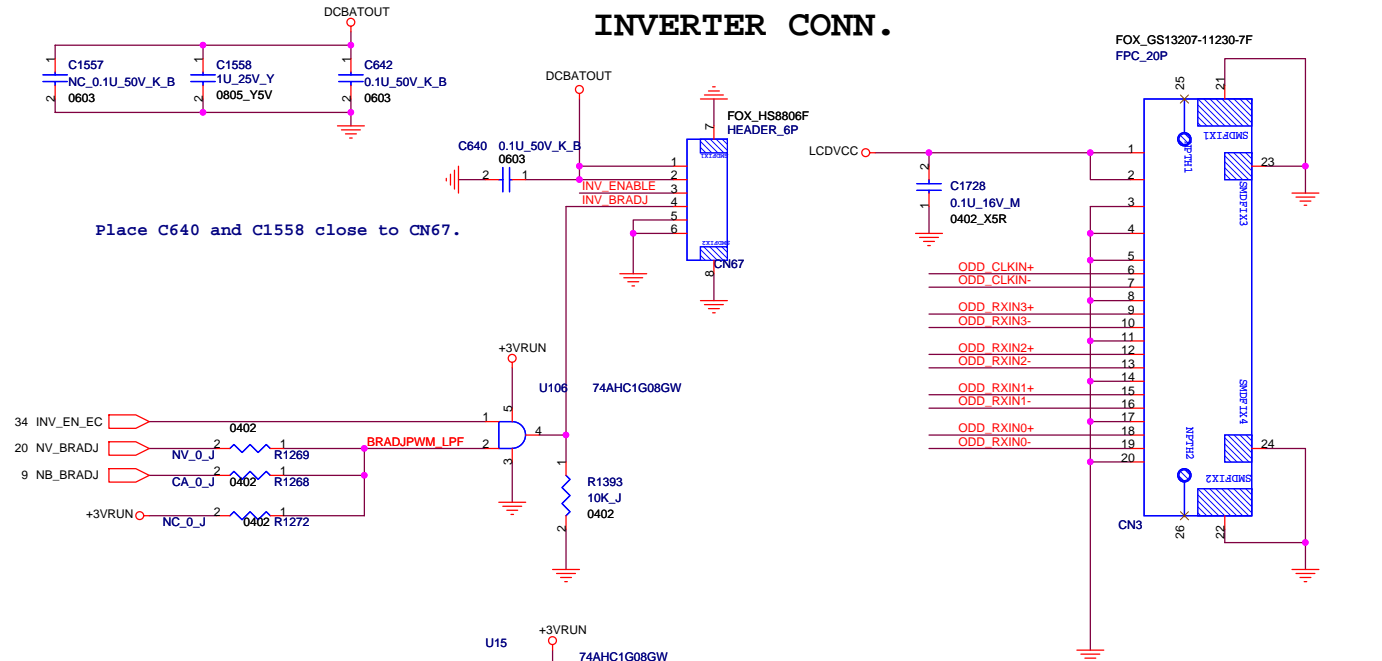
Group1, Group2 should be close

Group1

Group2



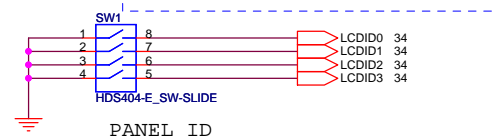
INVERTER CONN.



Place C640 and C1558 close to CN67.

LVDS CONNECTOR

EVT use 30pin
DVT modify to 20pin



Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vender	Samsung (2 lamp)	CPT (1 lamp)	AUO (2 lamp)	AUO (1 lamp)
Device Name	LTN154XB-L01	CLAA154WA05AN	B154EW07	QD15TL07
PanelID [2_0]	001	101	010	100

LCDID3 is for InstantOn switch
Enable: 0
Disable: 1

R459 close to R458.

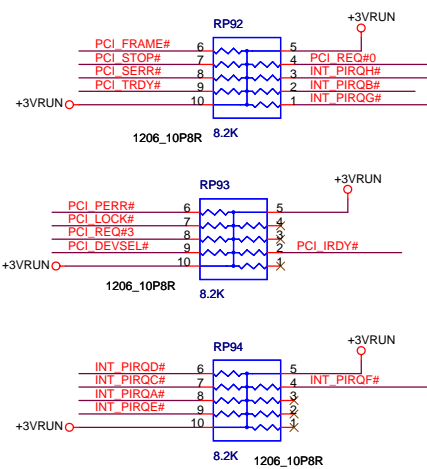
DISCHARGE
The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

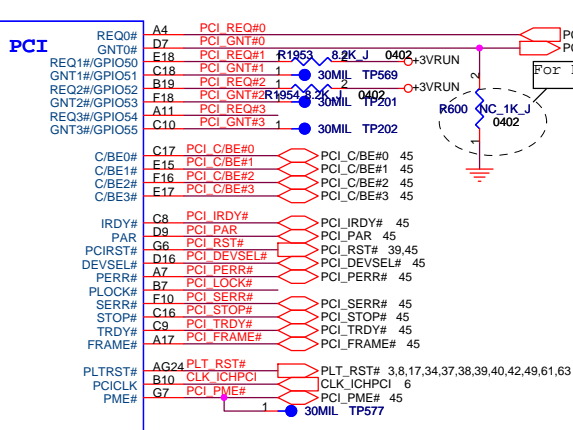
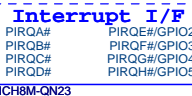
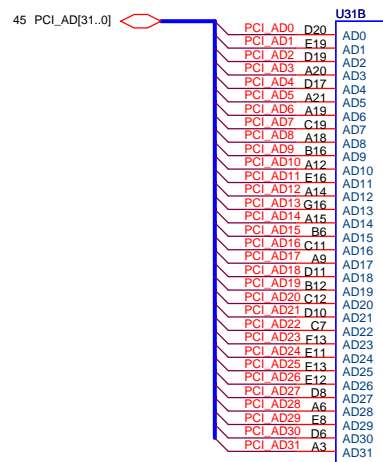
Title: **LVDS**

Size A3	Document Number MS91-1-01	Rev 1.0
---------	---------------------------	---------

Date: Thursday, June 21, 2007 Sheet 31 of 66



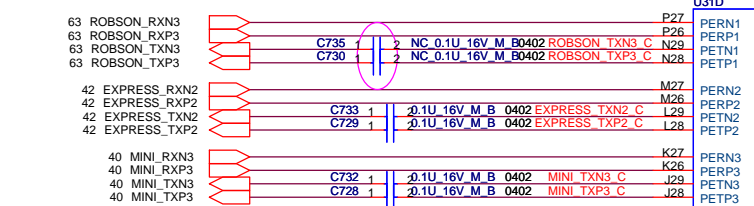
PCI Pullups



For Boot BIOS Selection.

Strap for Boot-BIOS

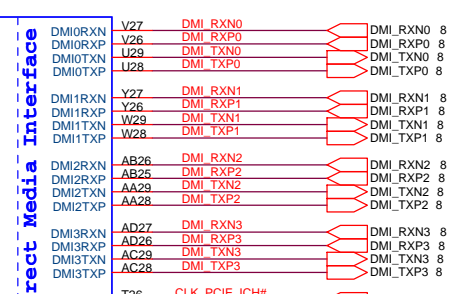
	GNT#	SPI_CS1#
IPC(Default)	Hi	Hi
PCI	Hi	Low
SPI	Low	Hi



Delete signal For Docking Connector

Place within 500 mils of ICH

PCI-Express



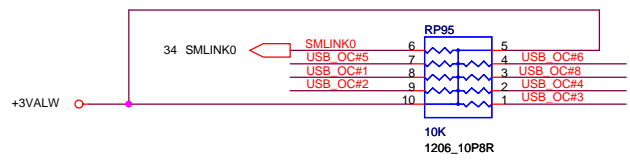
SPI

USB

ICH8M-QN23

For Boot BIOS Selection.

Place within 500 mils of ICH and don't routing next to high speed signals

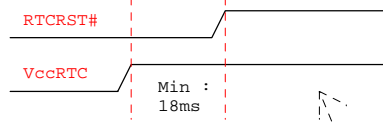


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

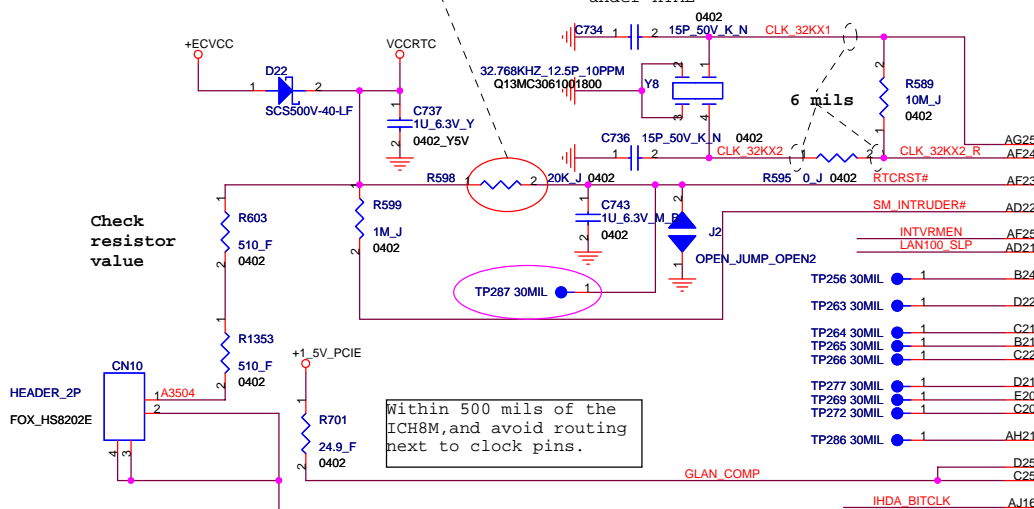
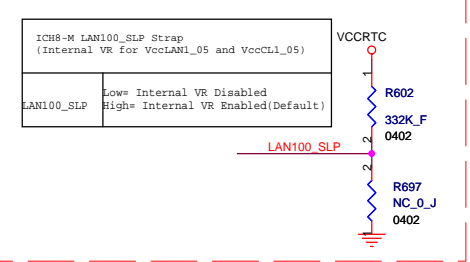
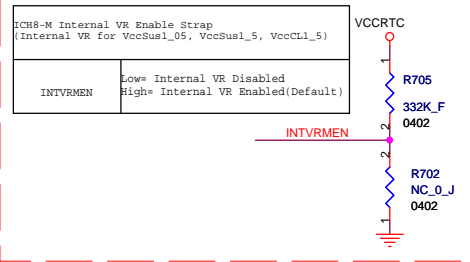
Title: **ICH8-M (PCI/DMI/USB/PCIE) 1/5**

Size A3 Document Number MS91-1-01 Rev 1.0

Date: Thursday, June 21, 2007 Sheet 32 of 66

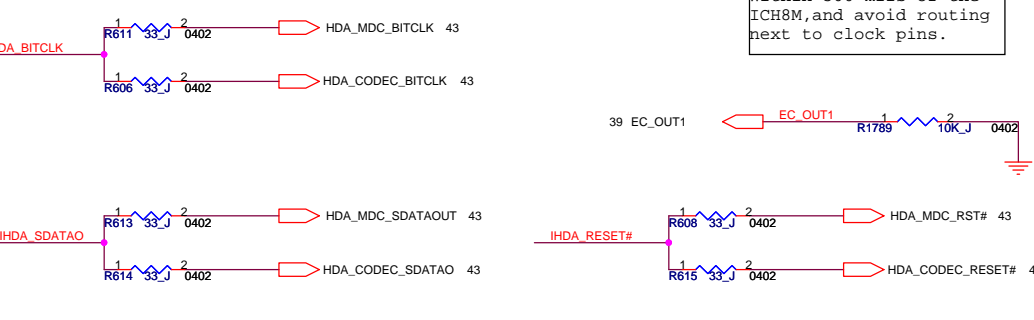
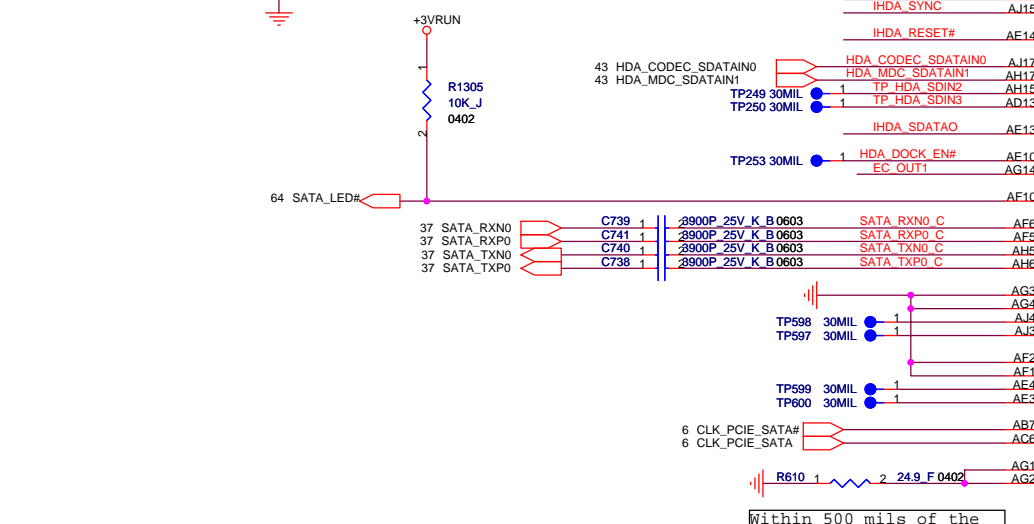
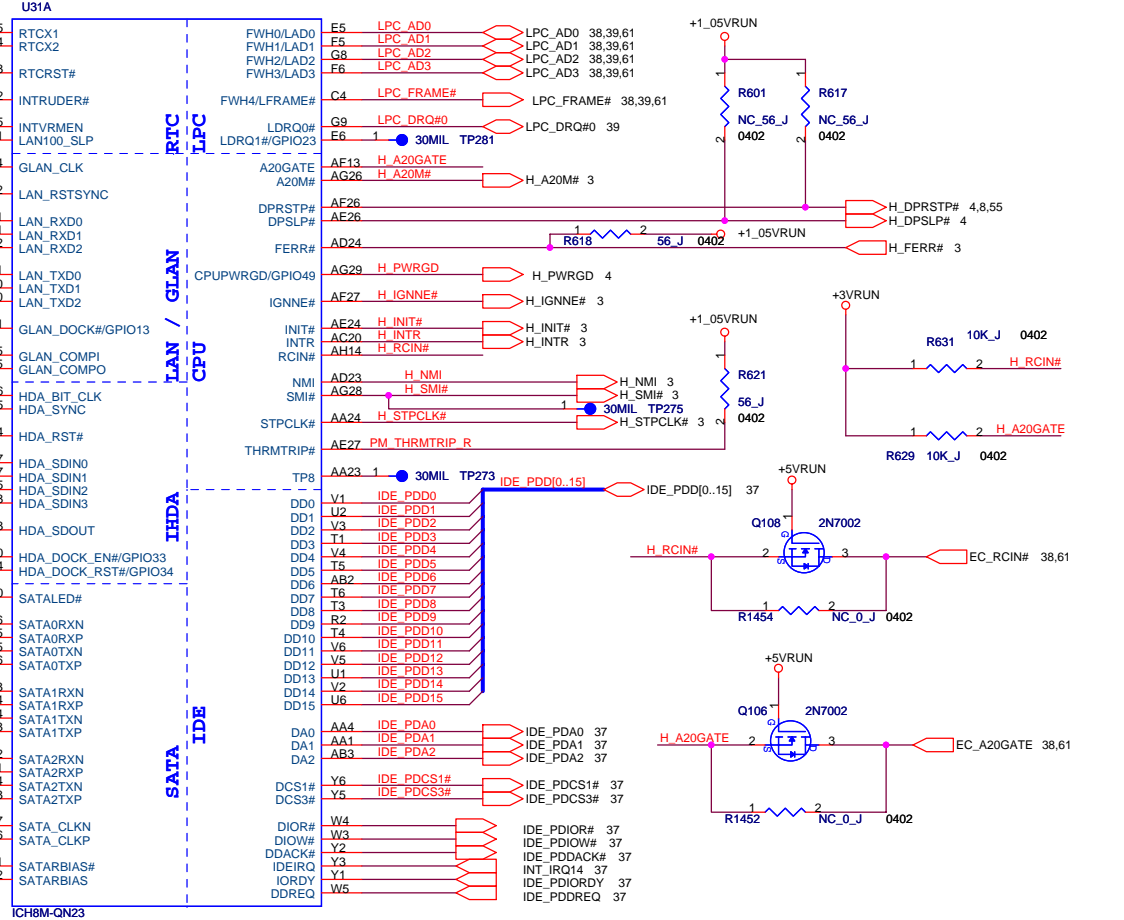


The traces inside this block should be wider. No digital signals routed under XTAL



Check resistor value

Within 500 mils of the ICH8M, and avoid routing next to clock pins.



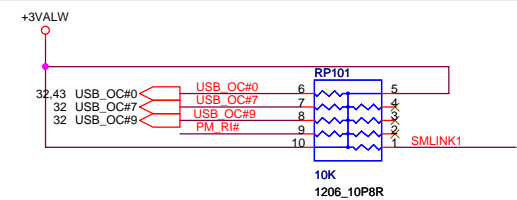
Within 500 mils of the ICH8M, and avoid routing next to clock pins.

FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

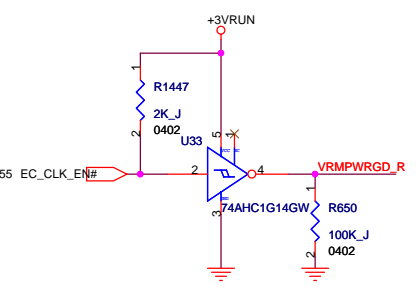
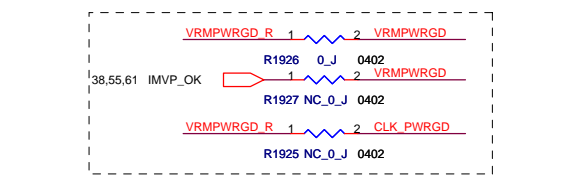
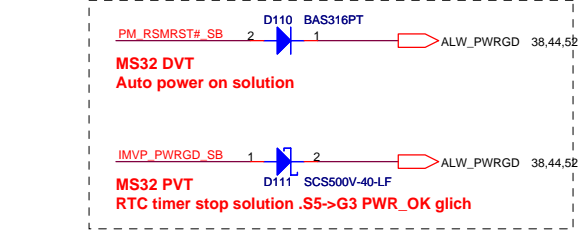
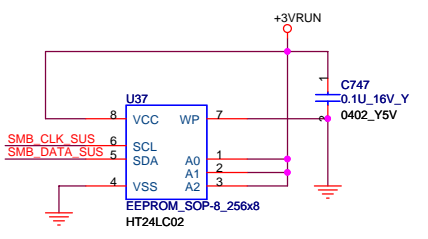
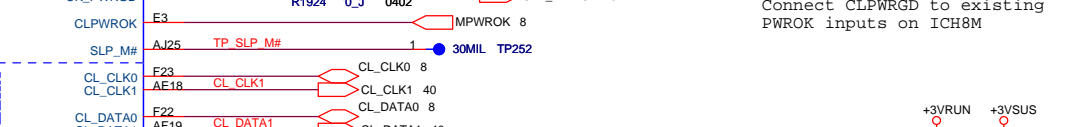
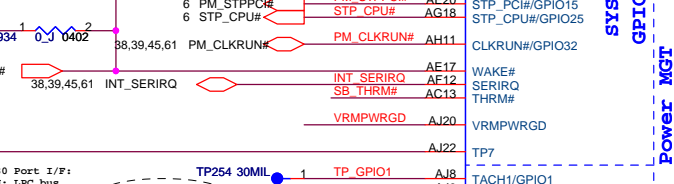
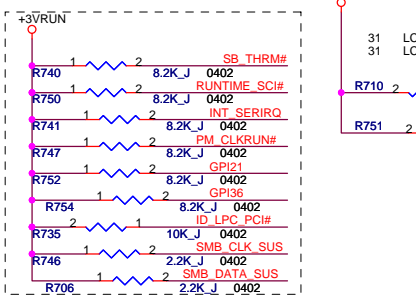
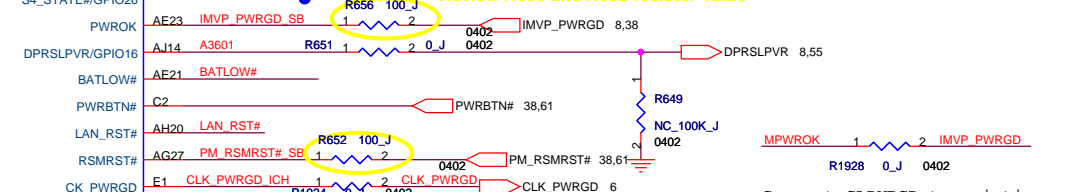
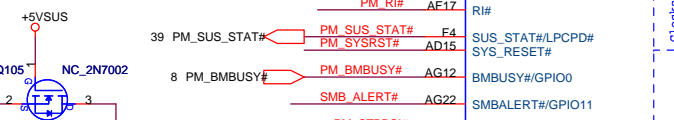
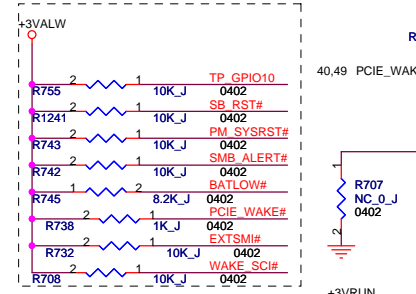
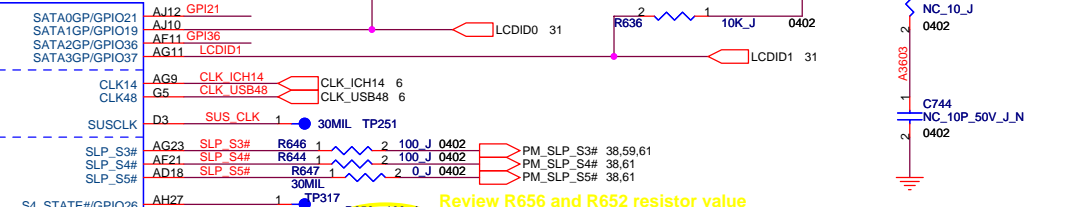
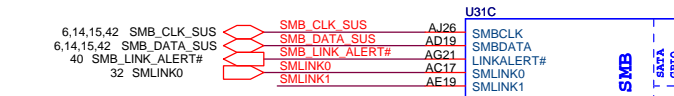
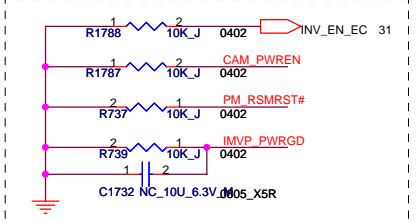
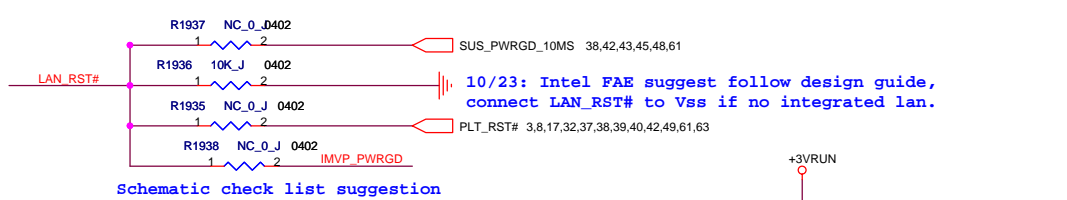
Title: **ICH8-M (LPC,IDE,SATA) 2/5**

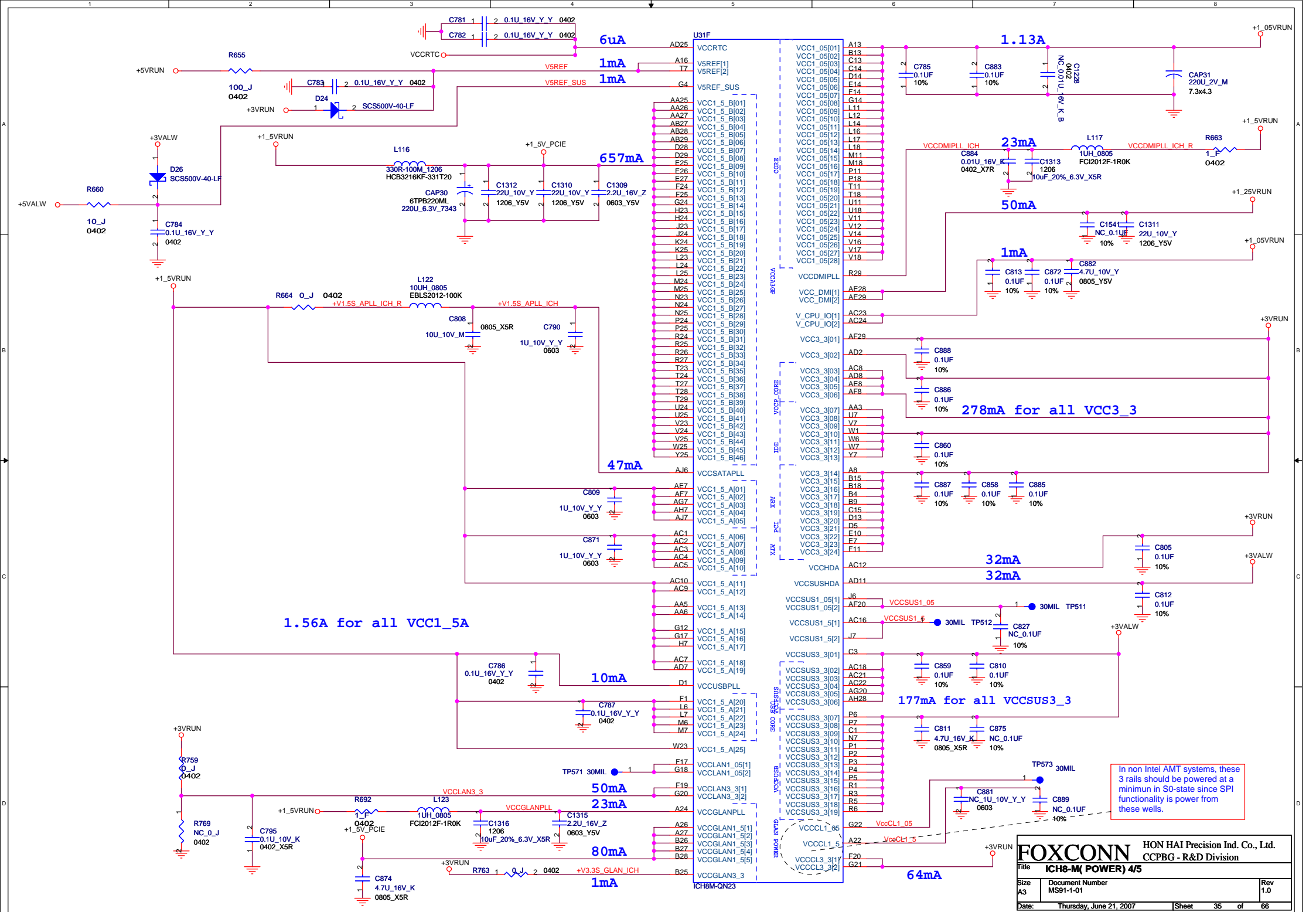
Size A3	Document Number MS91-1-01	Rev 1.0
---------	---------------------------	---------

Date: Thursday, June 21, 2007 | Sheet 33 of 66



Stuff for No-reboot
Low=Default
High=No-reboot





1.56A for all VCC1_5A

47mA

657mA

6uA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

1mA

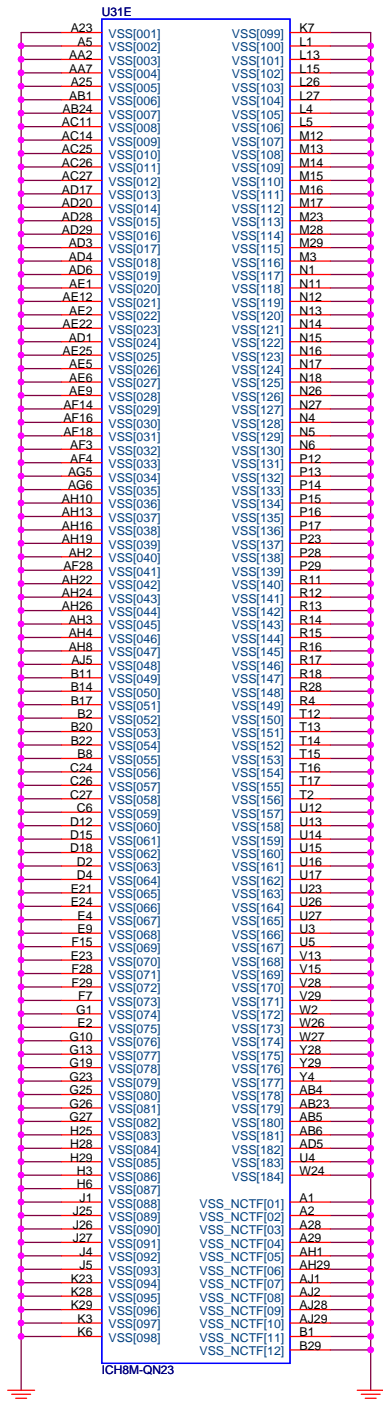
1mA

1mA

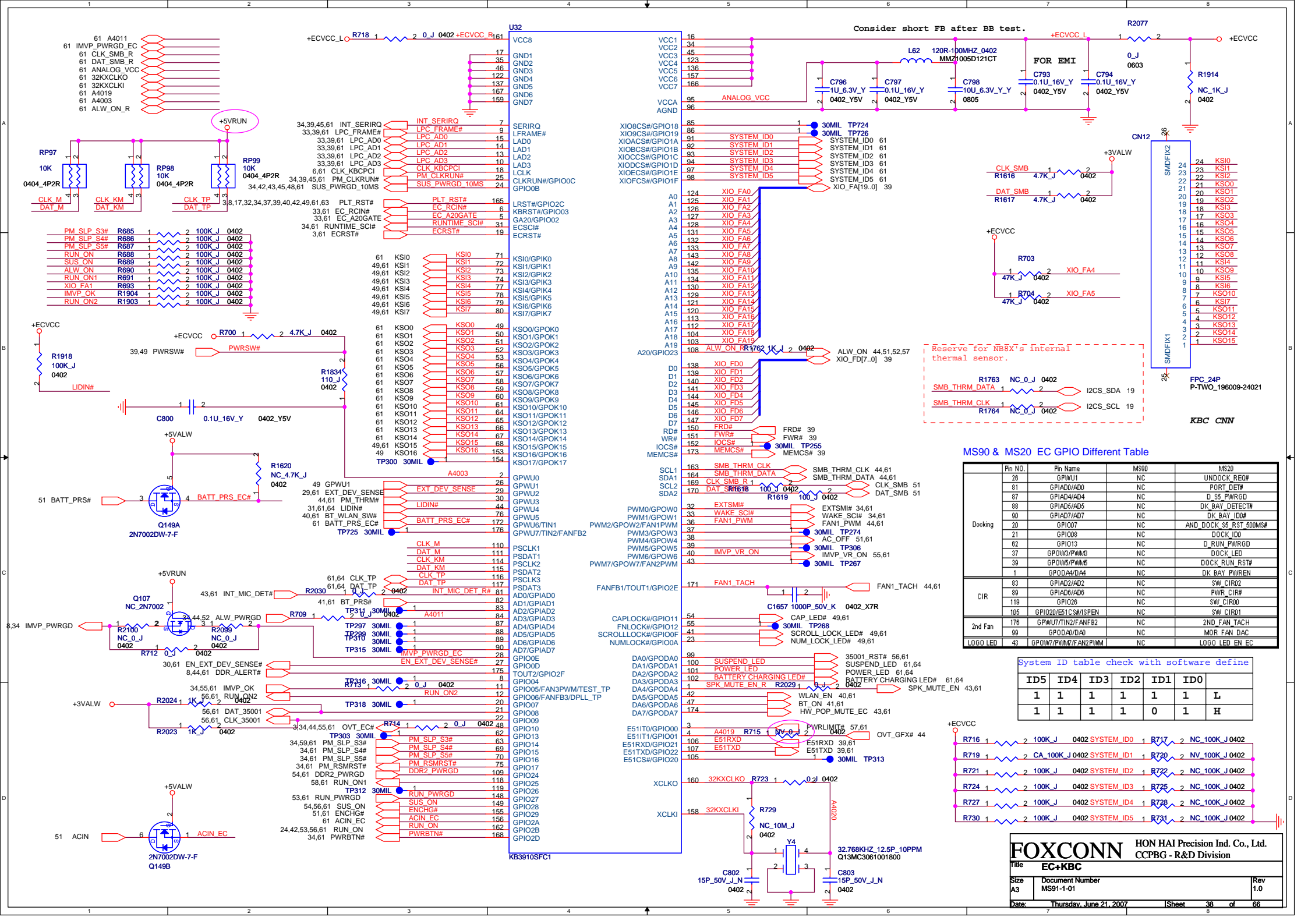
1mA

1mA

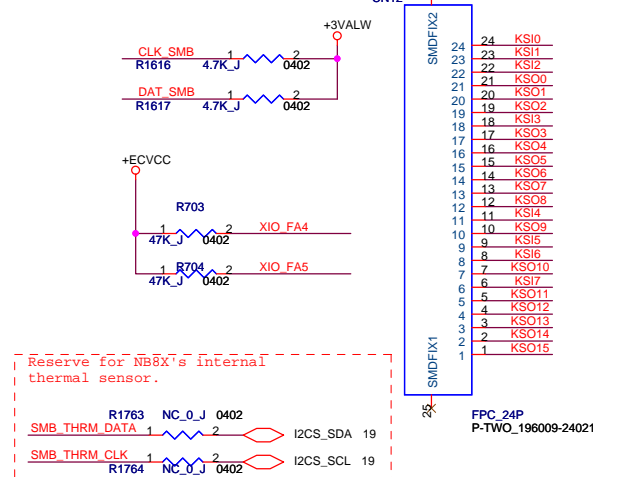
1mA



FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title ICH8-M(GND) 5/5			
Size A3	Document Number MS91-1-01	Rev 1.0	
Date:	Thursday, June 21, 2007	Sheet	36 of 66



Consider short FB after BB test.

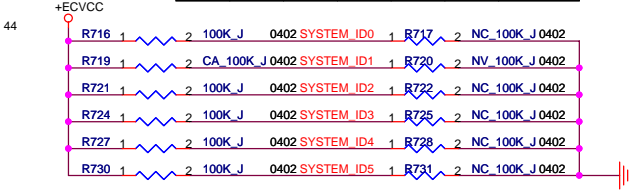


MS90 & MS20 EC GPIO Different Table

Pin NO.	Pin Name	MS90	MS20
26	GPWU1	NC	UNDOCK_REQ#
81	GPIOAD0/AD0	NC	PORT_DET#
87	GPIOAD4/AD4	NC	D_85_PWRGD
88	GPIOAD6/AD6	NC	DK_BAY_DETECT#
90	GPIOAD7/AD7	NC	DK_BAY_ID0#
20	GPIO07	NC	AND_DOCK_S5_RST_600MS#
21	GPIO08	NC	DOCK_ID0
62	GPIO13	NC	D_RUN_PWRGD
37	GPIOW3/PWM3	NC	DOCK_LED
39	GPIOW5/PWM5	NC	DOCK_RUN_RST#
1	GP0D4/AD4	NC	DK_BAY_PWREN
83	GPIOAD2/AD2	NC	SW_CIR02
89	GPIOAD6/AD6	NC	PWR_CIR0
119	GPIO26	NC	SW_CIR00
105	GPIO20/ES1CS#/ISPEN	NC	SW_CIR01
176	GPWU7/TIN2/FANFB2	NC	2ND_FAN_TACH
99	GP0D4/AD4	NC	MOR_FAN_DAC
43	GP0W7/PWM7/FAN2/PWM	NC	LOGO_LED_EN_EC

System ID table check with software define

ID5	ID4	ID3	ID2	ID1	ID0	
1	1	1	1	1	1	L
1	1	1	1	0	1	H

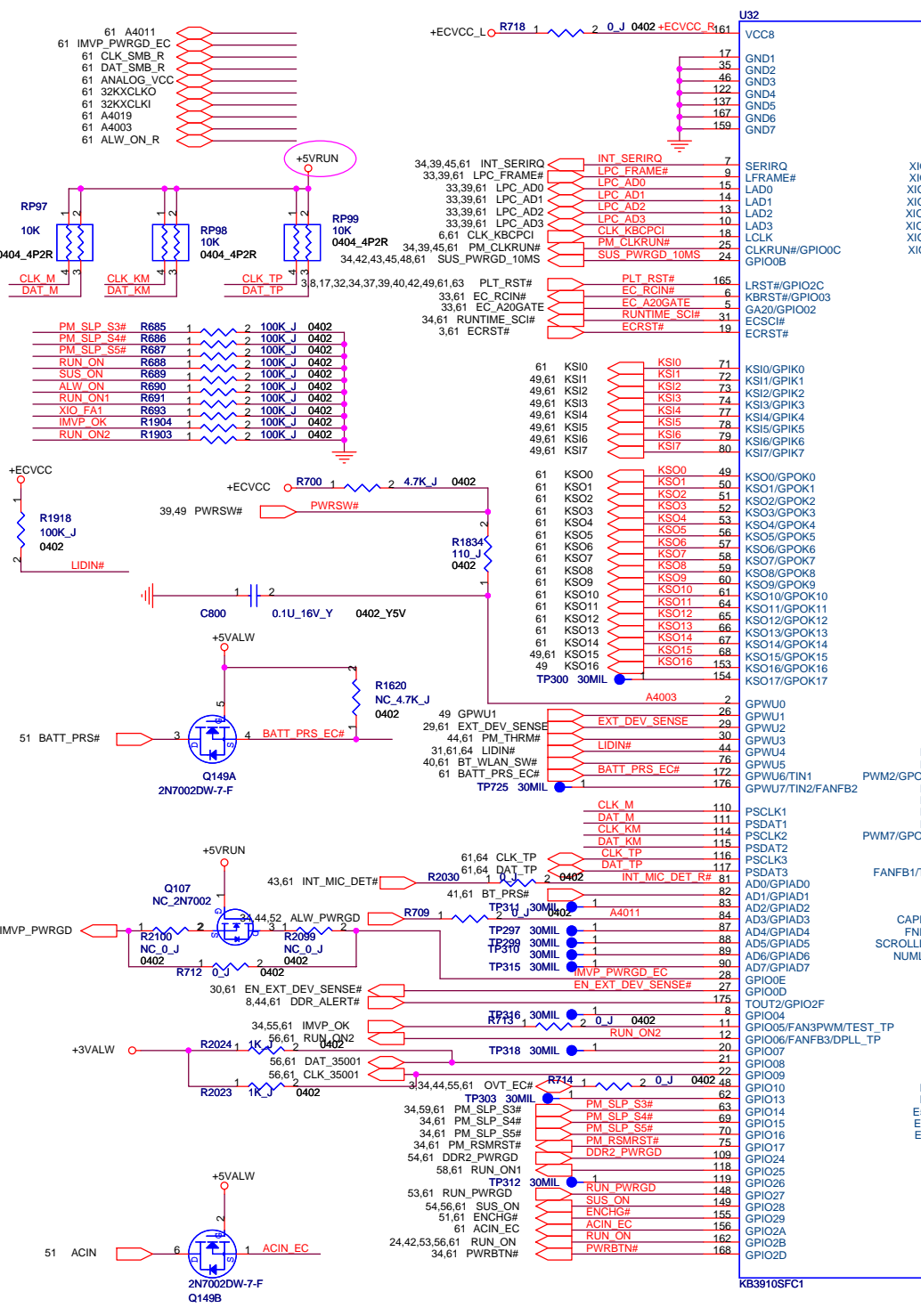
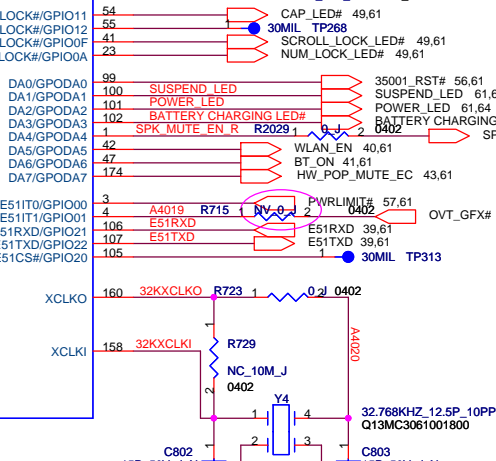
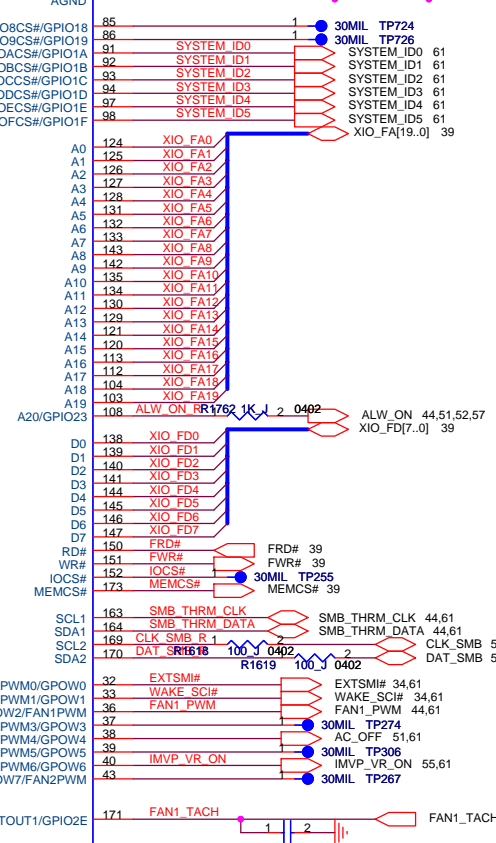


FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

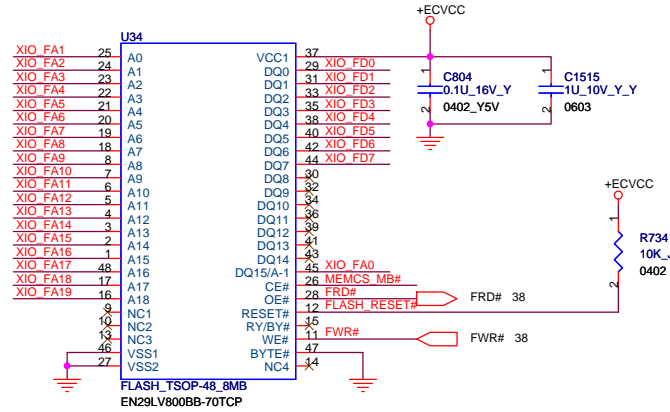
Title: **EC+KBC**

Size A3	Document Number MS91-1-01	Rev 1.0
---------	---------------------------	---------

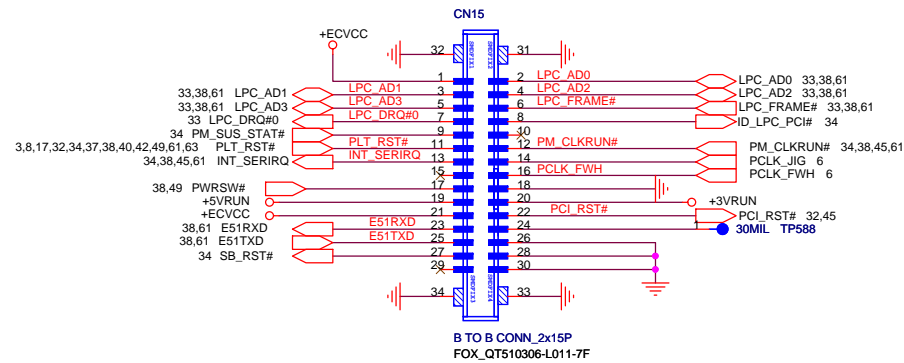
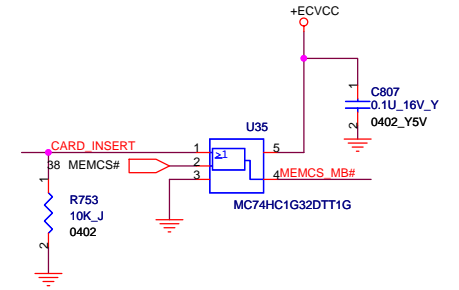
Date: Thursday, June 21, 2007 Sheet 38 of 66



38 XIO_FA[19..0]
38 XIO_FD[7..0]

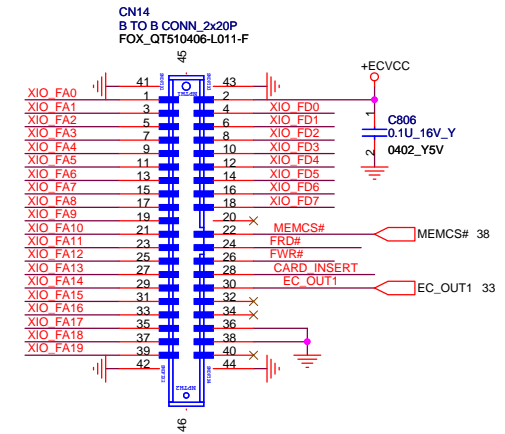


FLASH BIOS



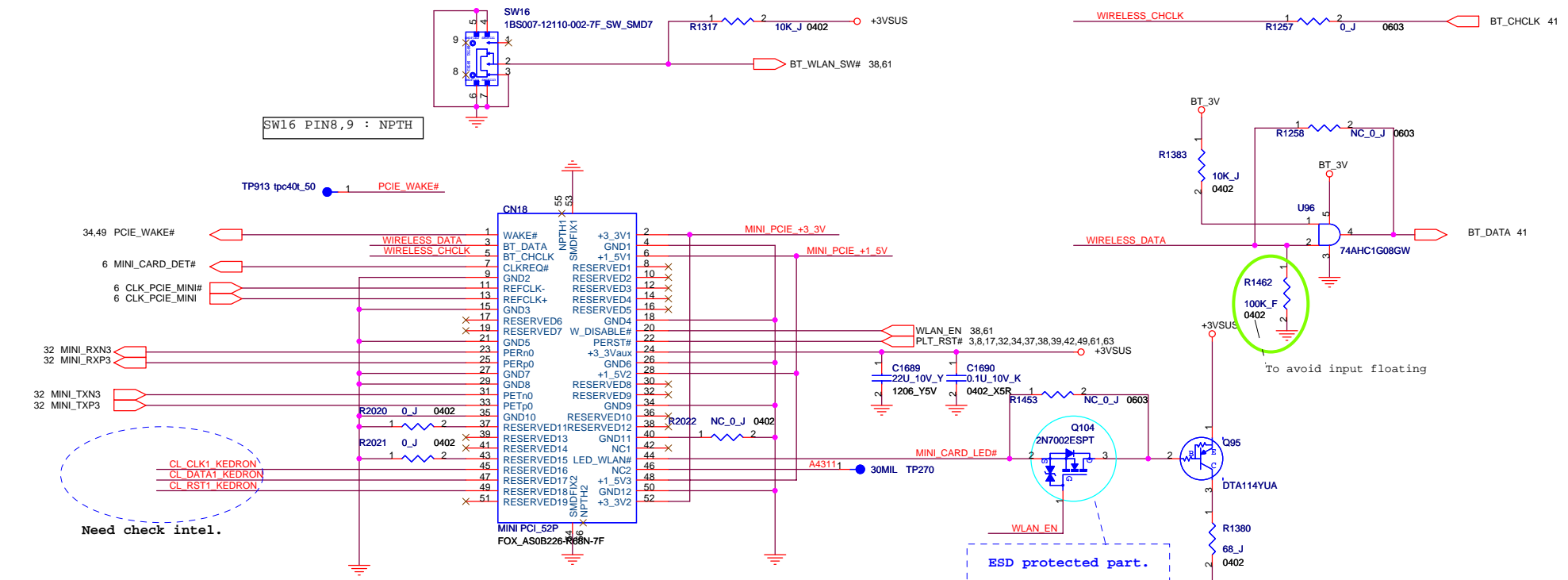
JIG-120

Pin 18 of JIG-120 is useless in debug board, so we let pin 18 NC.



X-BUS

WLAN Switch



SW16 PIN8,9 : NPTH

To avoid input floating

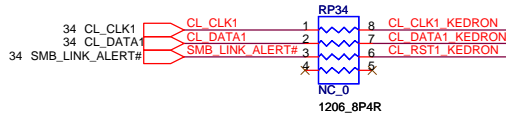
ESD protected part.

LED IF SPEC:
20mA (TYP) , 30mA (MAX)

Green

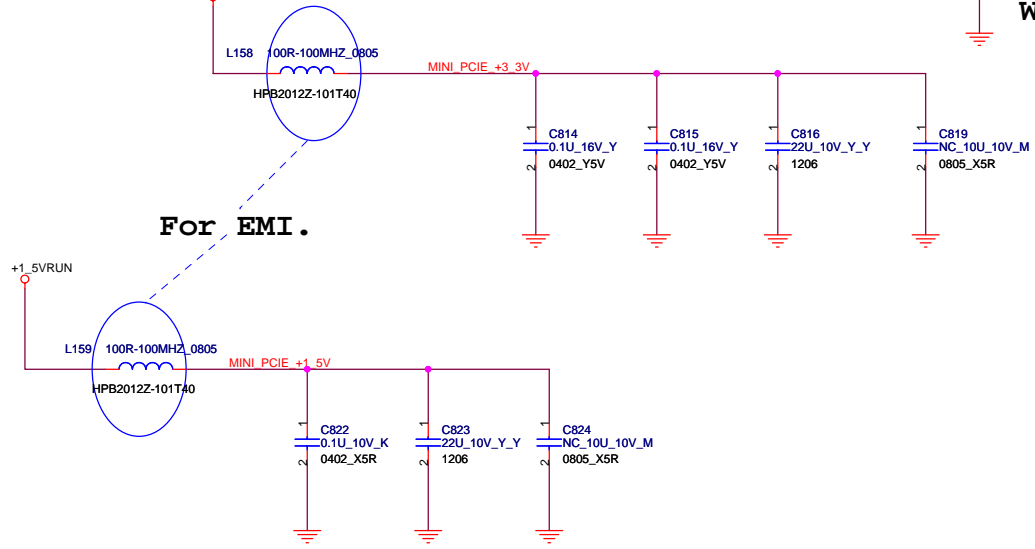
WLAN LED.

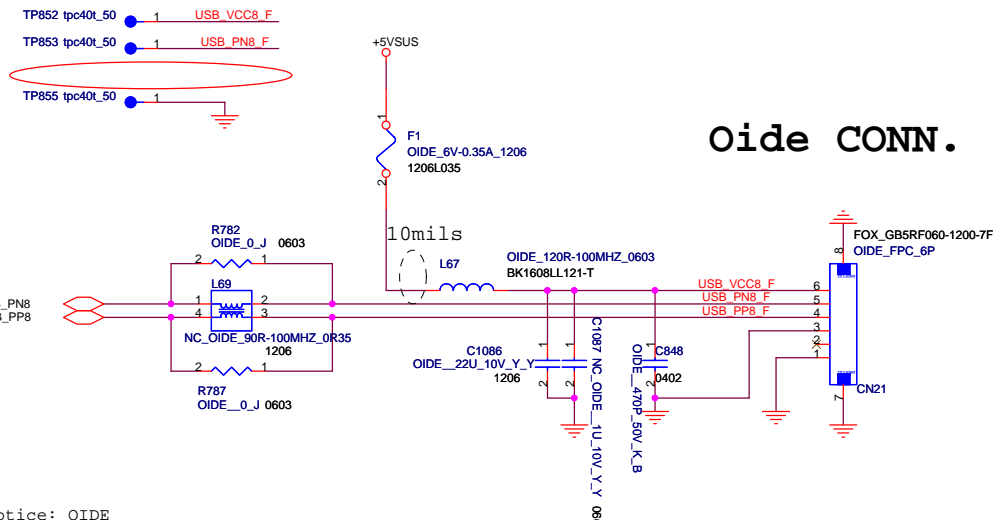
Mini Card. WLAN



+1_5V=>0.5A
+3_3VAux=>0.33A
+3_3V=>1A

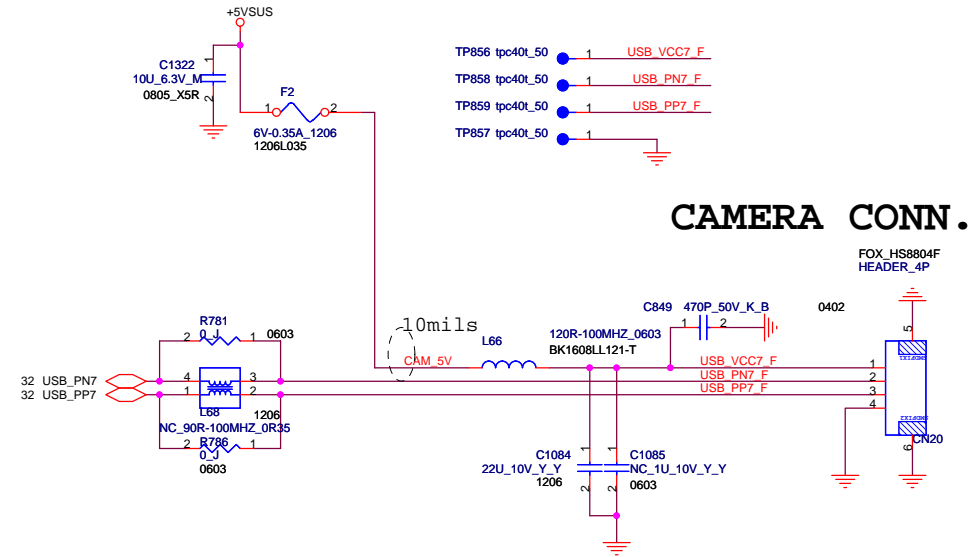
For EMI.



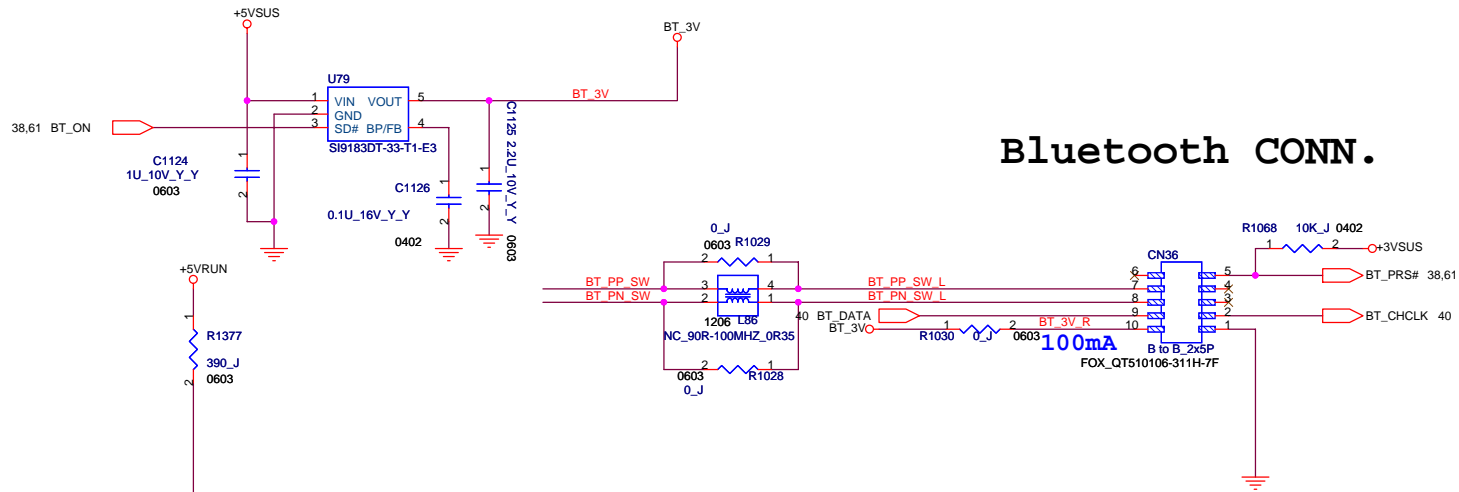


BOM Notice: OIDE_

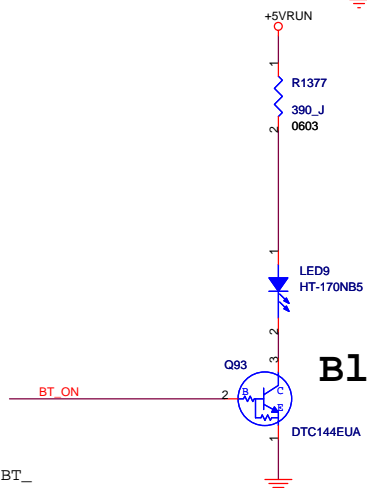
W/ Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	stuff
W/O Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	no stuff



Bluetooth CONN.

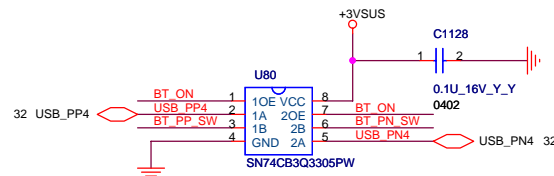


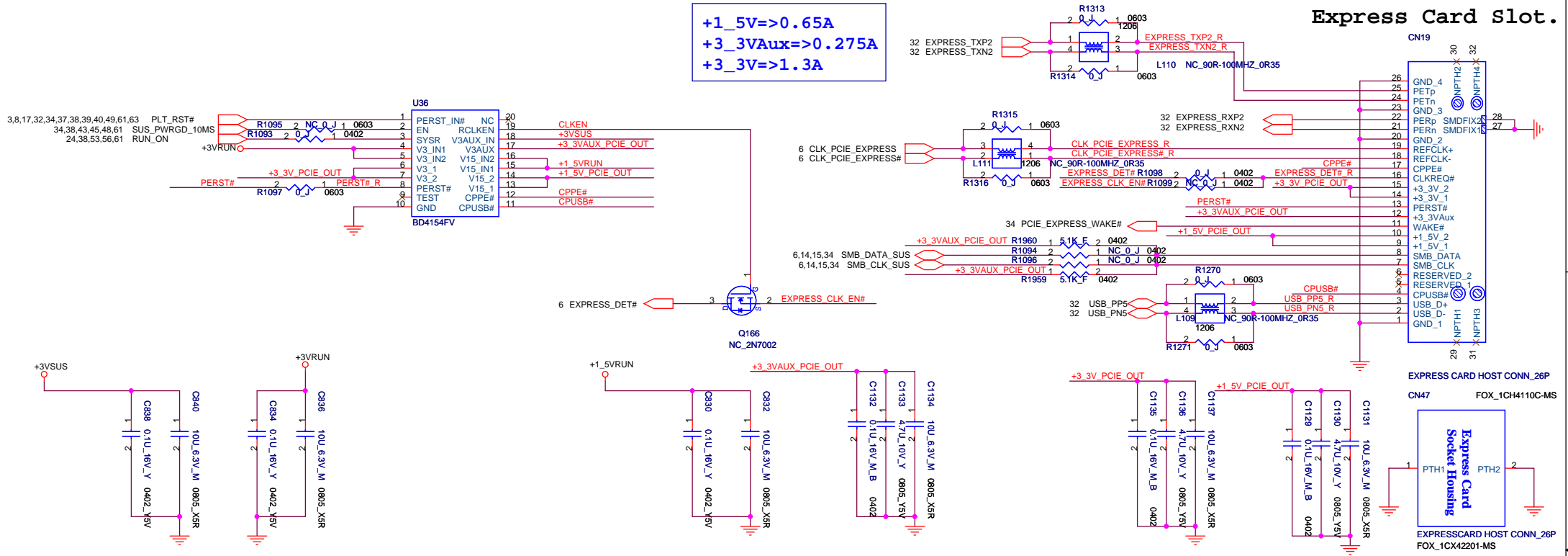
Bluetooth LED.



BOM Notice: BT_

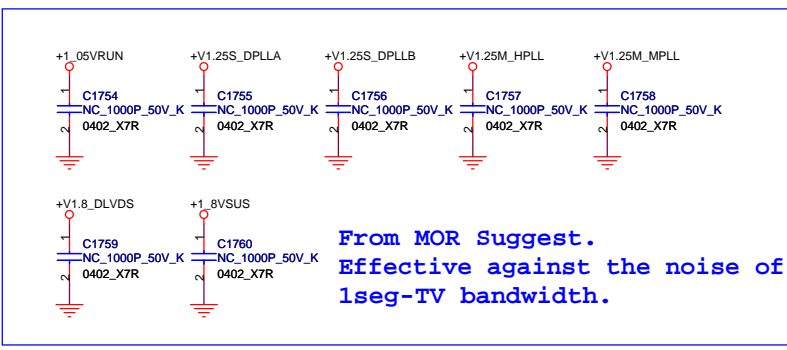
W/ BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	stuff
W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff



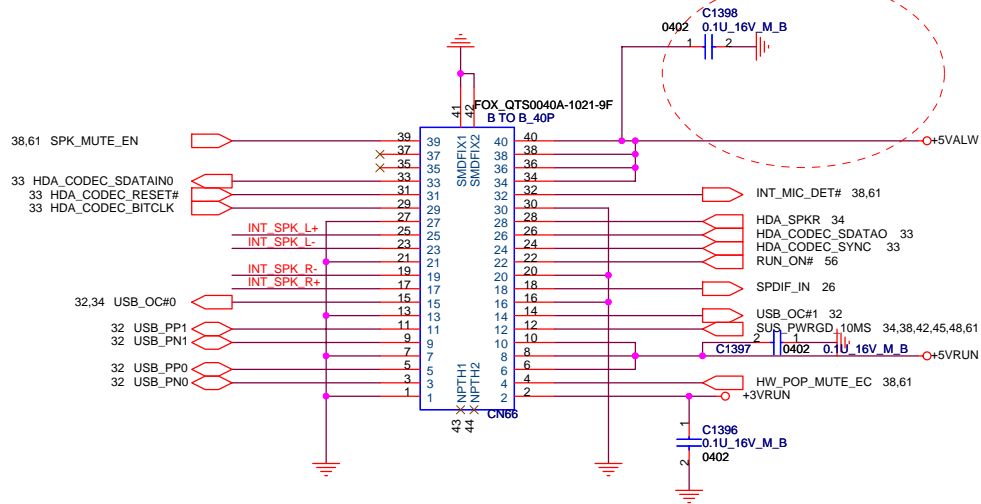


Express Card Slot.

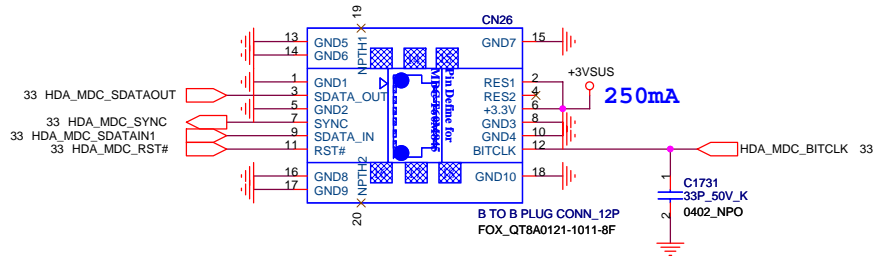
Express Card Housing.



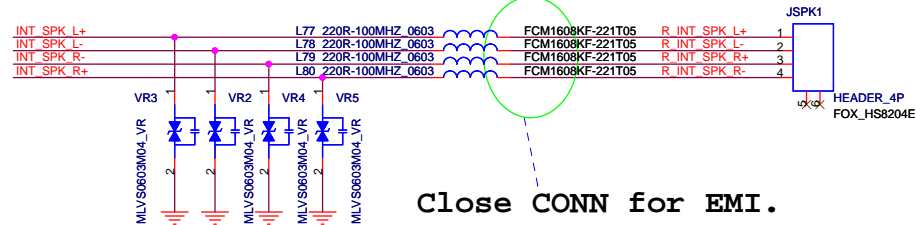
Audio & USB Board CONN.



MDC CONN.



INTERNAL SPEAKER



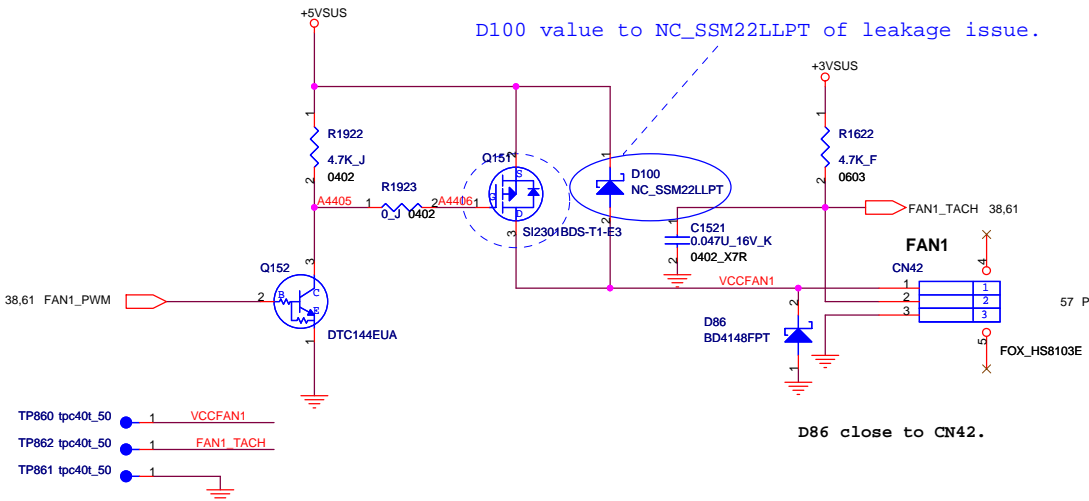
Close CONN for EMI.

- TP863 tpc40t_50 1 R_INT_SPK L+
- TP864 tpc40t_50 1 R_INT_SPK L-
- TP866 tpc40t_50 1 R_INT_SPK R+
- TP865 tpc40t_50 1 R_INT_SPK R-

0331: Add diode for inverse current and change pull-high resistor from 10K to 4.7K.

0331: Change C1521 from Y5V to X7R.

D100 value to NC_SSM22LLPT of leakage issue.

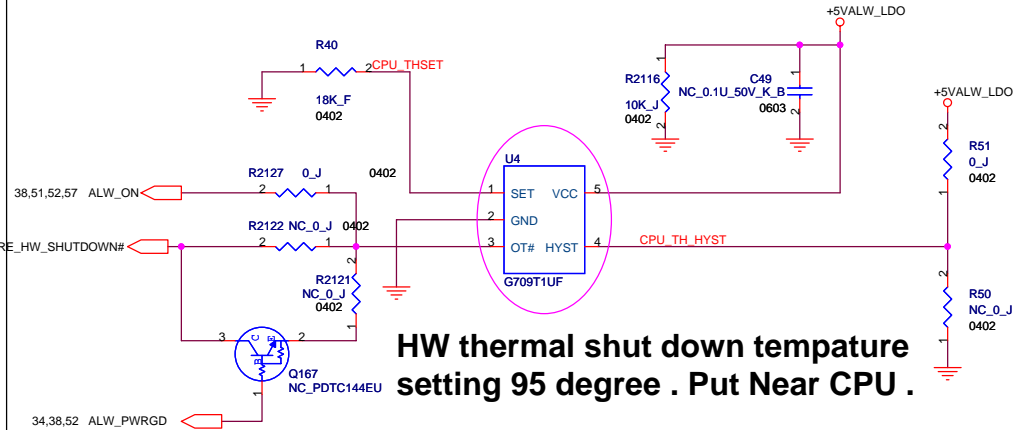


- TP860 tpc40t_50 1 VCCFAN1
- TP862 tpc40t_50 1 FAN1_TACH
- TP861 tpc40t_50 1

D86 close to CN42.

FAN

HW THERMAL PROTECTION

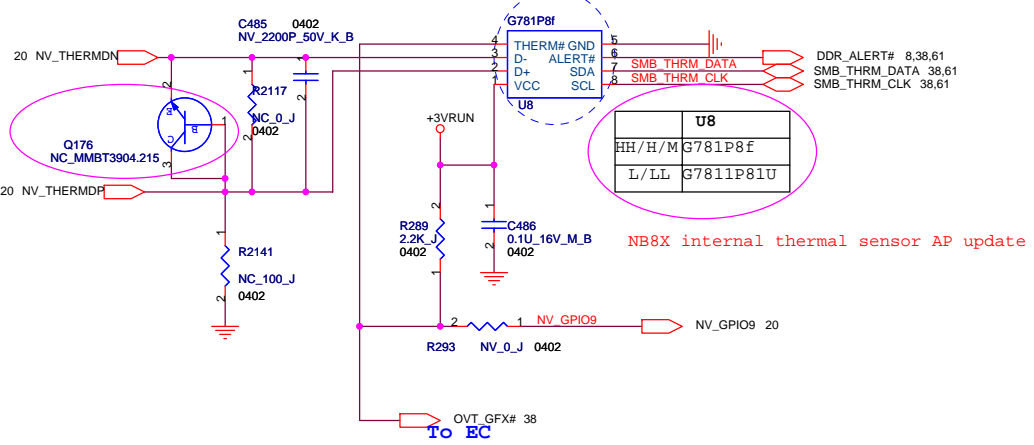


HW thermal shut down temperature setting 95 degree . Put Near CPU .

Delete VGA Thermal-Sensor

Delete local DDR2 themarl sensor.

SM bus Address :
1001100 (EC)
For G781P8f



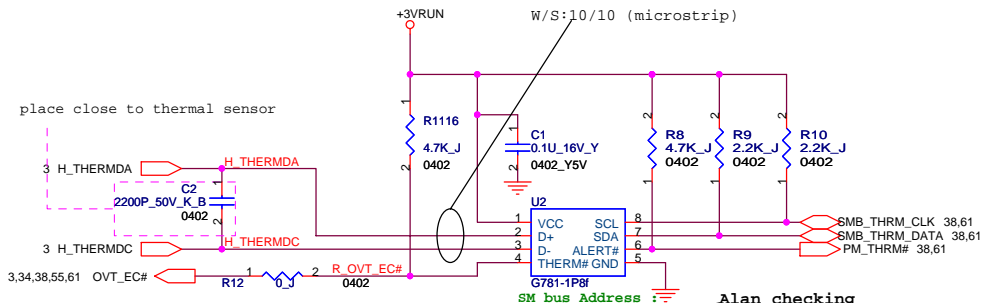
U8	
HH/H/M	G781P8f
L/LL	G7811P81U

NB8X internal thermal sensor AP update

Close to U7

- TP914 tpc40t_50 1 H_THERMDA
- TP915 tpc40t_50 1 H_THERMDC

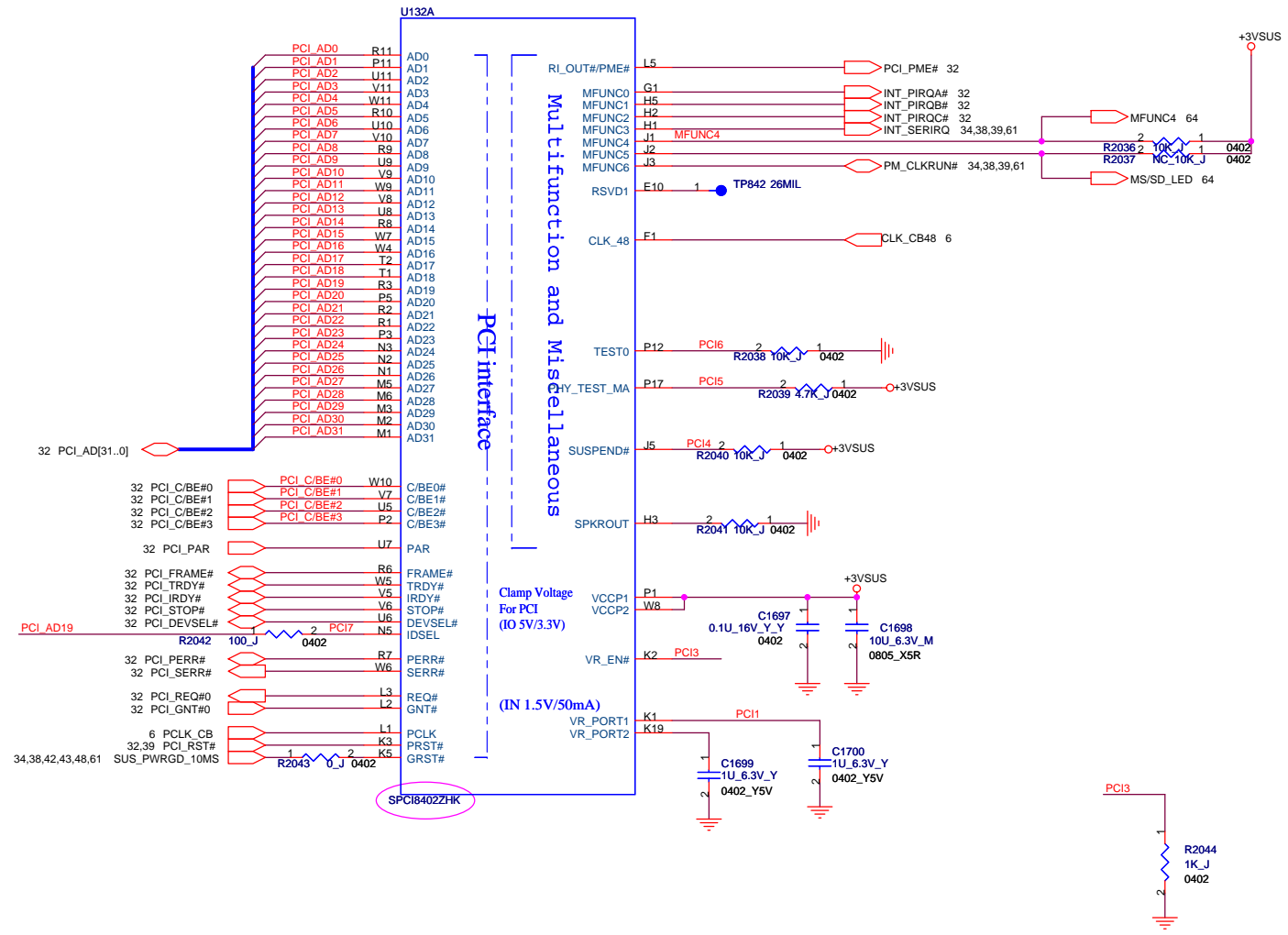
CPU Thermal-Sensor

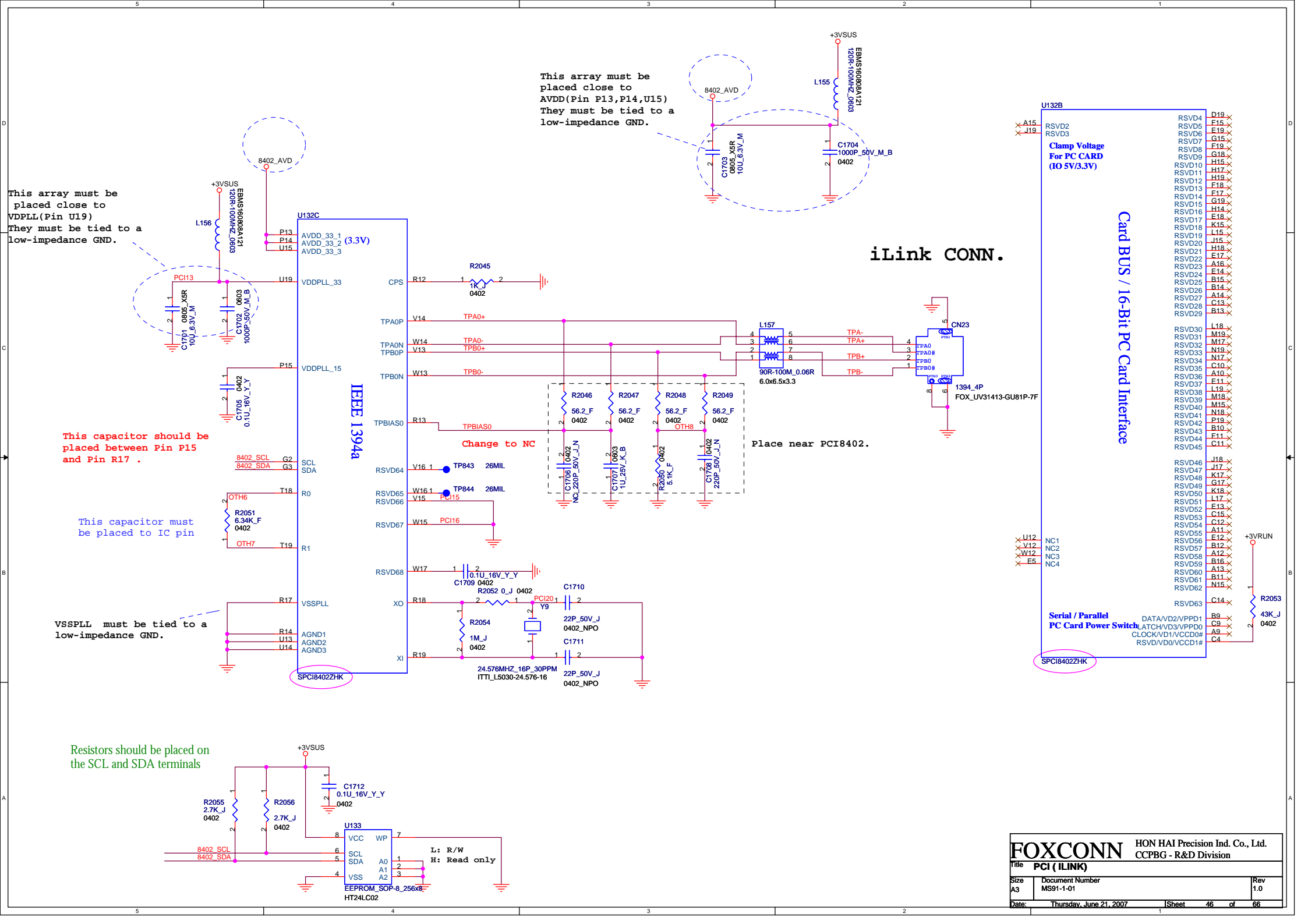


SM bus Address : 1001101 = 9A

Place Thermal-Sensor near CPU & GMCH.

Close to U109





This array must be placed close to AVDD (Pin P13,P14,U15) They must be tied to a low-impedance GND.

This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.

Resistors should be placed on the SCL and SDA terminals

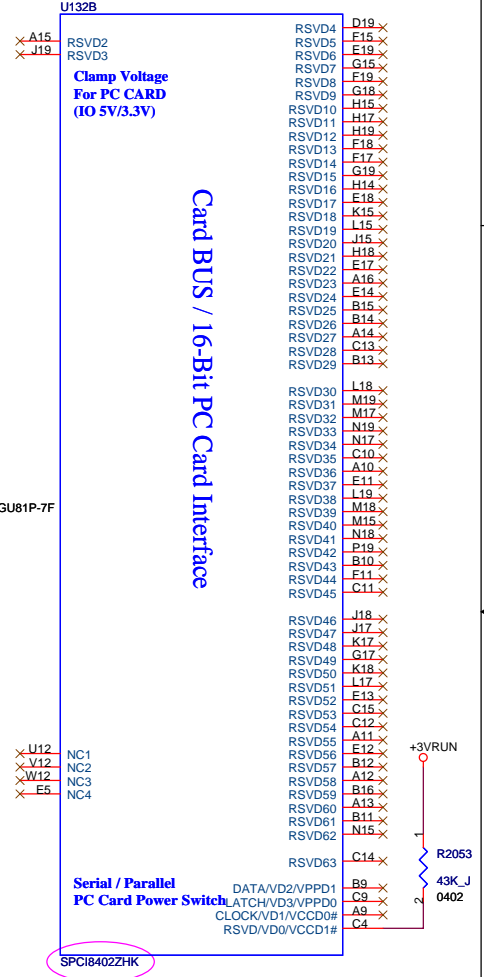
Place near PCI8402.

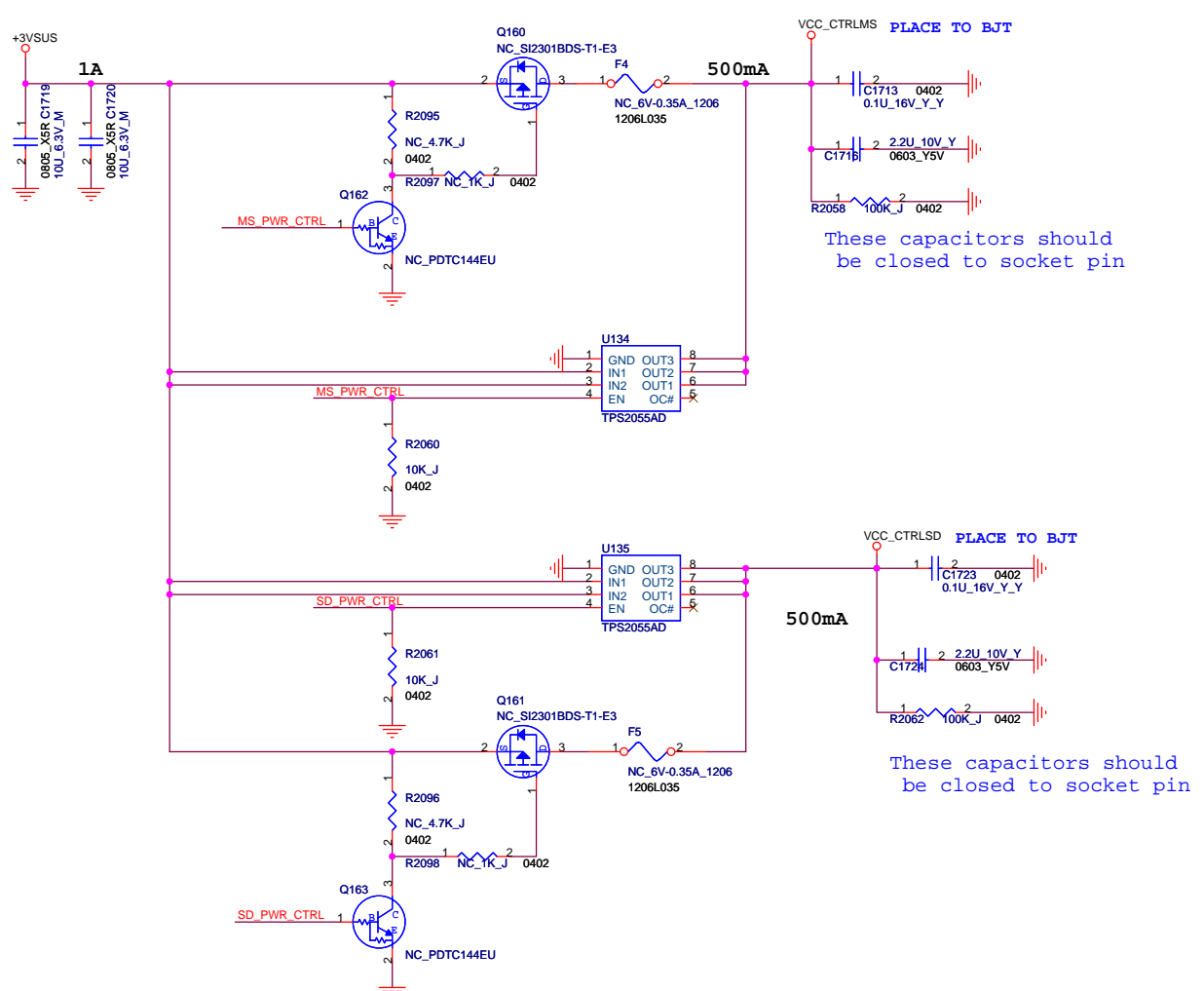
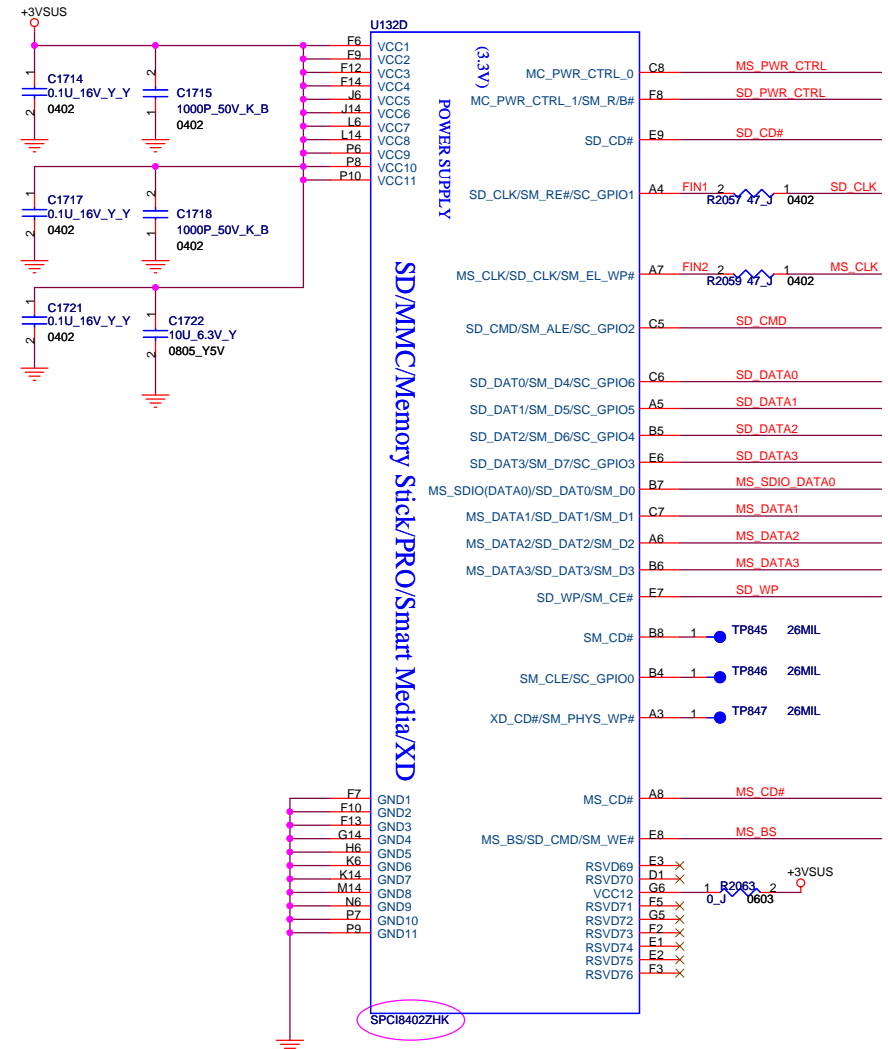
iLink CONN.

Clamp Voltage For PC CARD (IO 5V/3.3V)

Card BUS / 16-Bit PC Card Interface

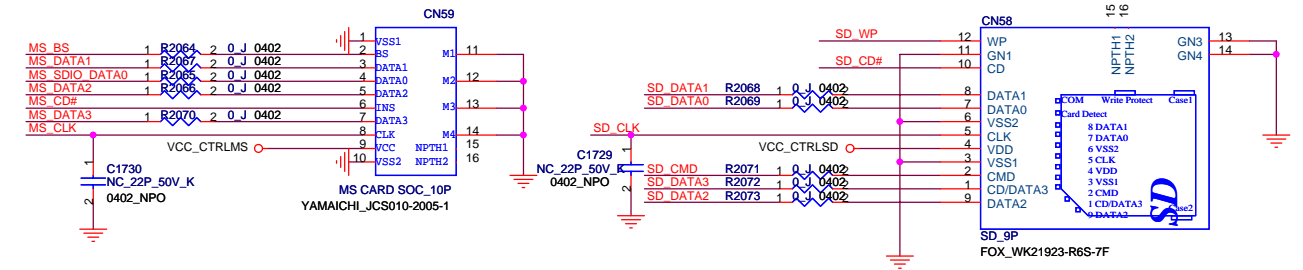
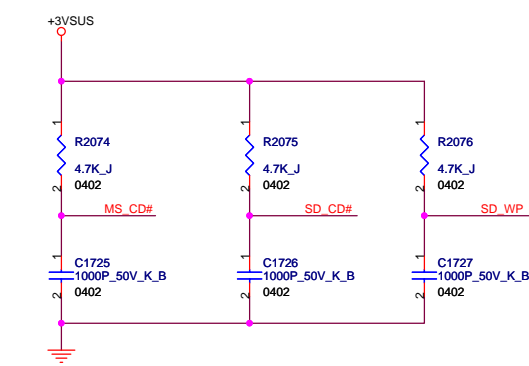
Serial / Parallel PC Card Power Switch



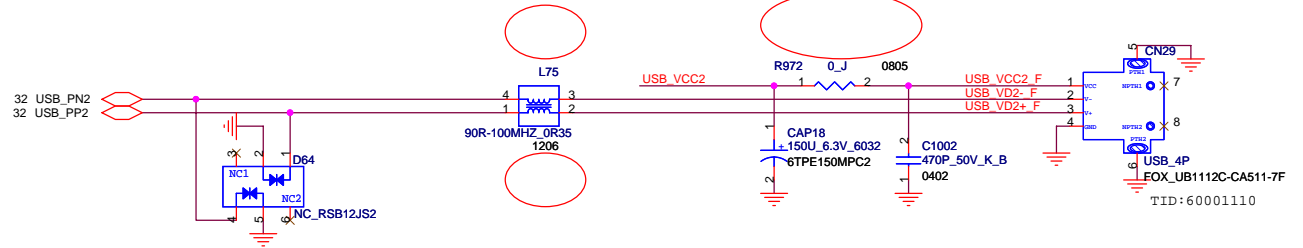
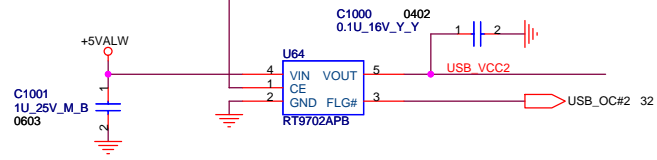


MS STD/DUO CONN.

SD CONN.



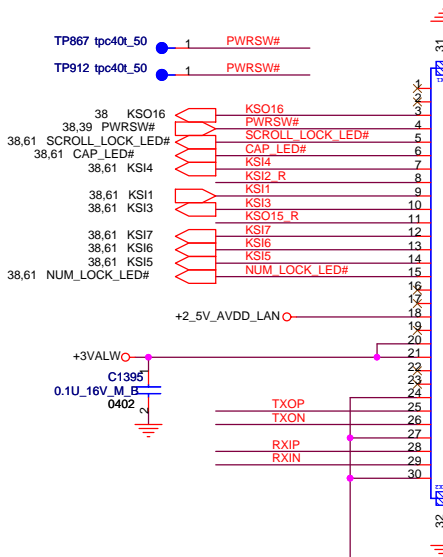
34,38,42,43,45,61 SUS_PWRGD_10MS



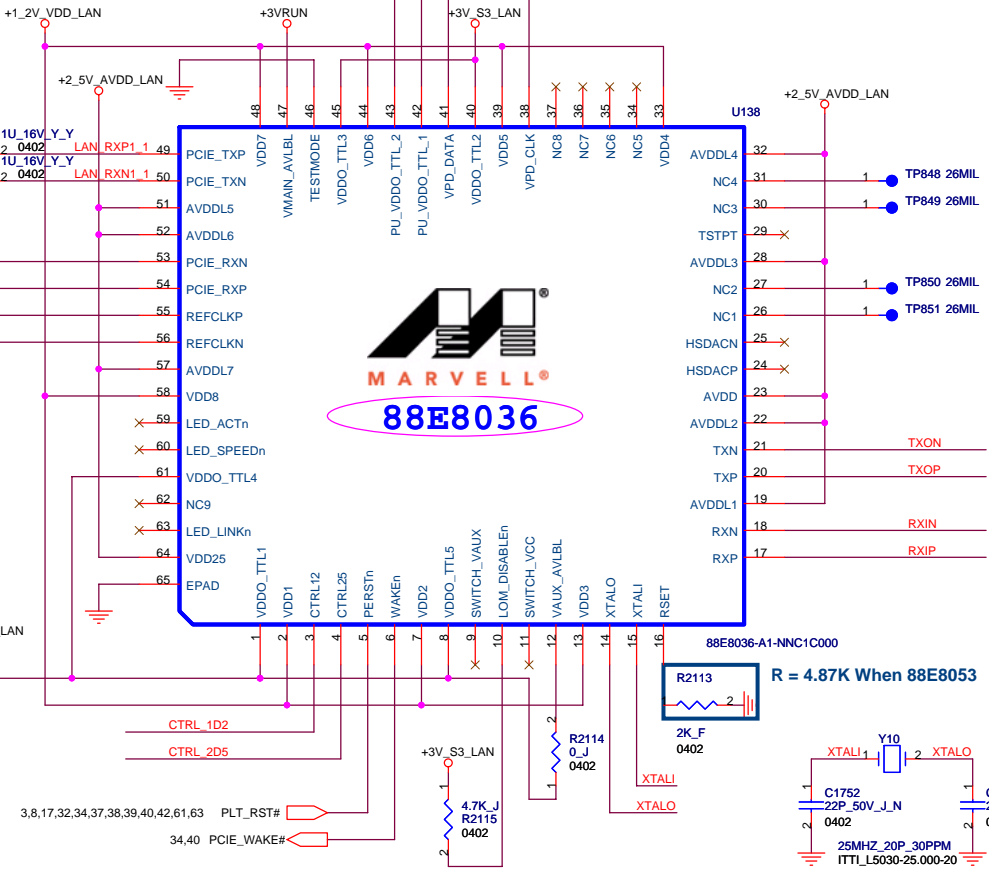
USB CONN.

TID: 60001110

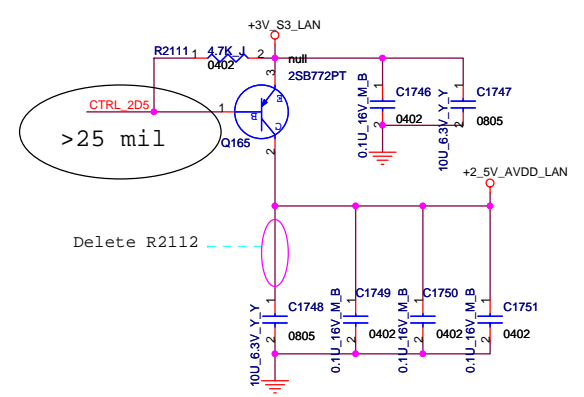
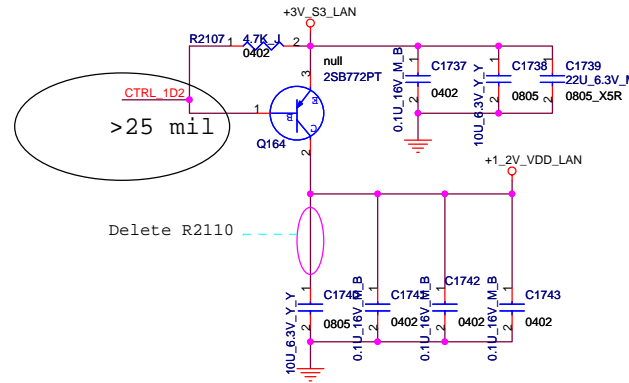
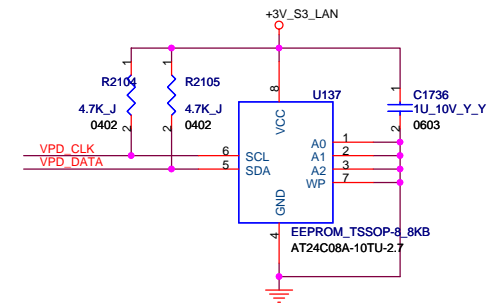
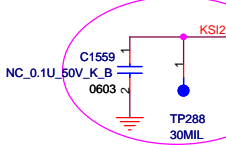
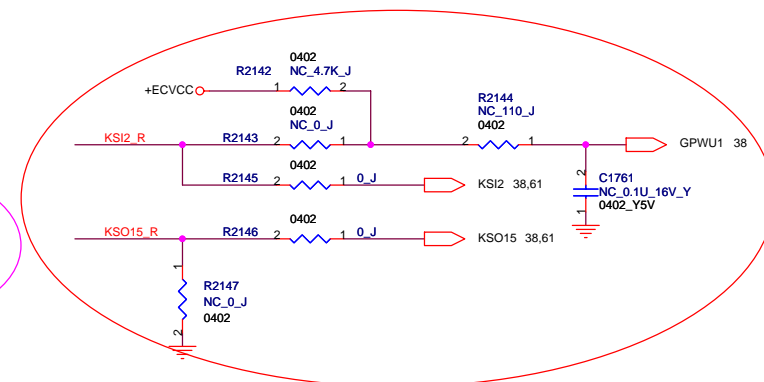
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title USB2.0		CCPBG - R&D Division	
Size A3	Document Number MS91-1-01	Rev 1.0	
Date: Thursday, June 21, 2007	Sheet 48 of 66		

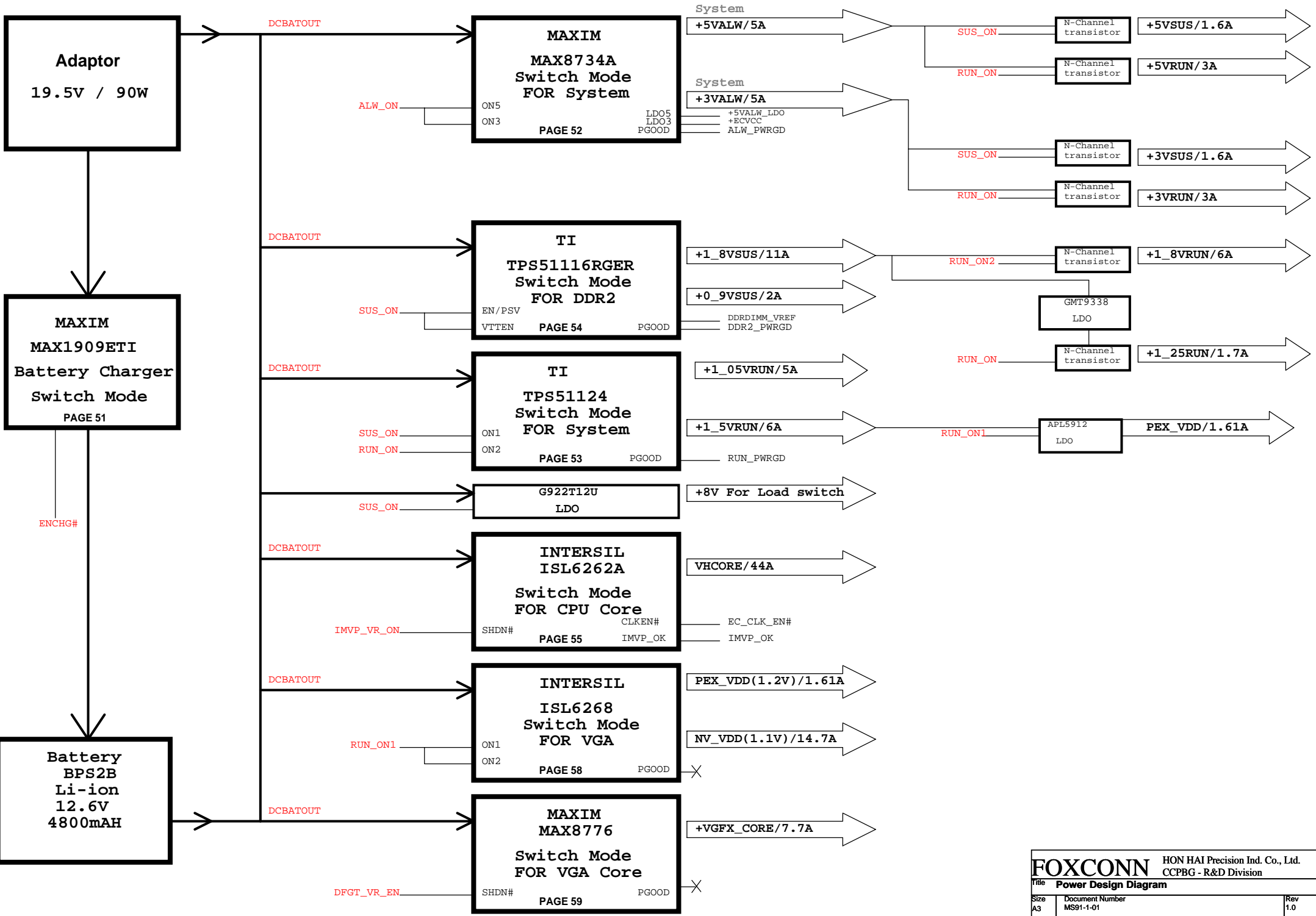
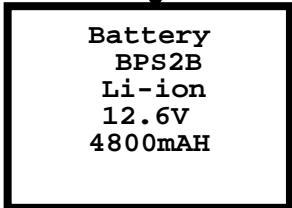
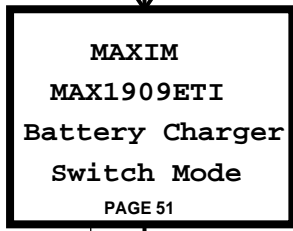
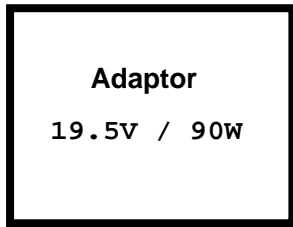


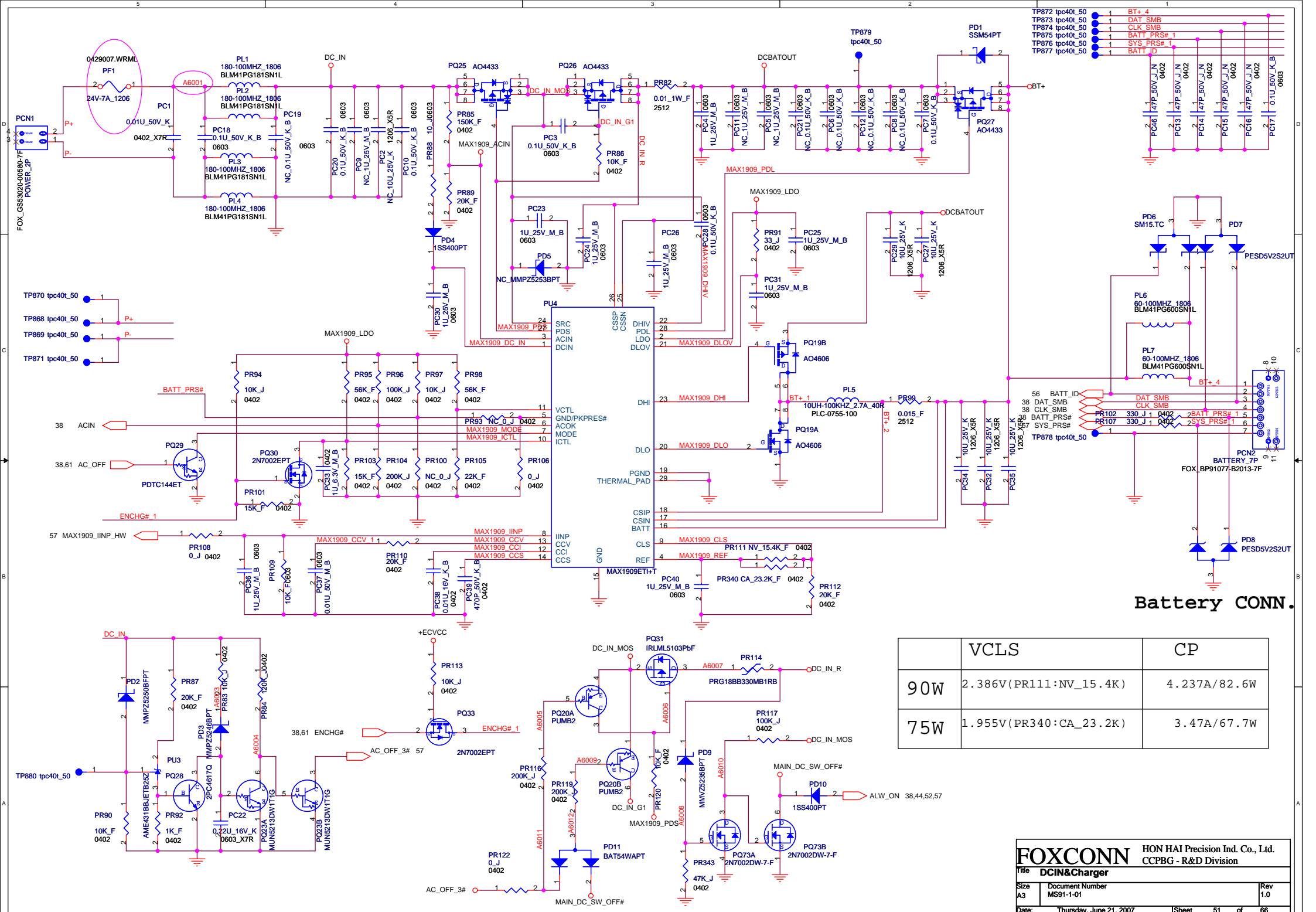
Switch Board CONN.



R2113 R = 4.87K When 88E8036







- TP872 tpc40t_50
- TP873 tpc40t_50
- TP874 tpc40t_50
- TP875 tpc40t_50
- TP876 tpc40t_50
- TP877 tpc40t_50
- BT+ 4
- DAT SMB
- CLK SMB
- BATT_PRS# 1
- SYS_PRS# 1
- BATT_ID

Battery CONN.

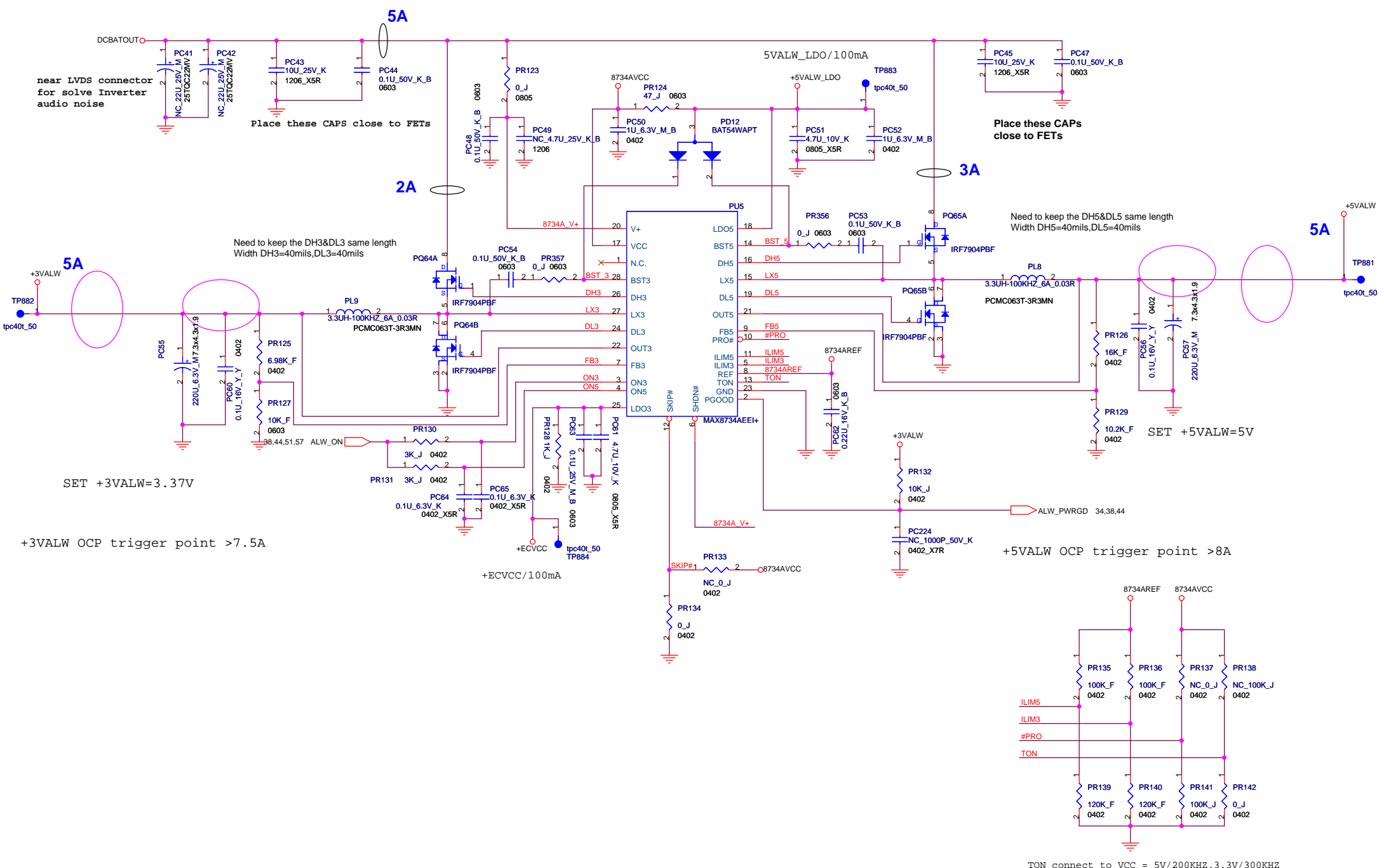
	VCLS	CP
90W	2.386V (PR111:NV_15.4K)	4.237A/82.6W
75W	1.955V (PR340:CA_23.2K)	3.47A/67.7W

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **DCIN&Charger**

Size: A3 | Document Number: MS91-1-01 | Rev: 1.0

Date: Thursday, June 21, 2007 | Sheet: 51 of 66



near LVDS connector
for solve Inverter
audio noise

Place these CAPS close to FETs

Place these CAPS
close to FETs

Need to keep the DH3&DL3 same length
Width DH3=40mils,DL3=40mils

Need to keep the DH5&DL5 same length
Width DH5=40mils,DL5=40mils

SET +3VALW=3.37V

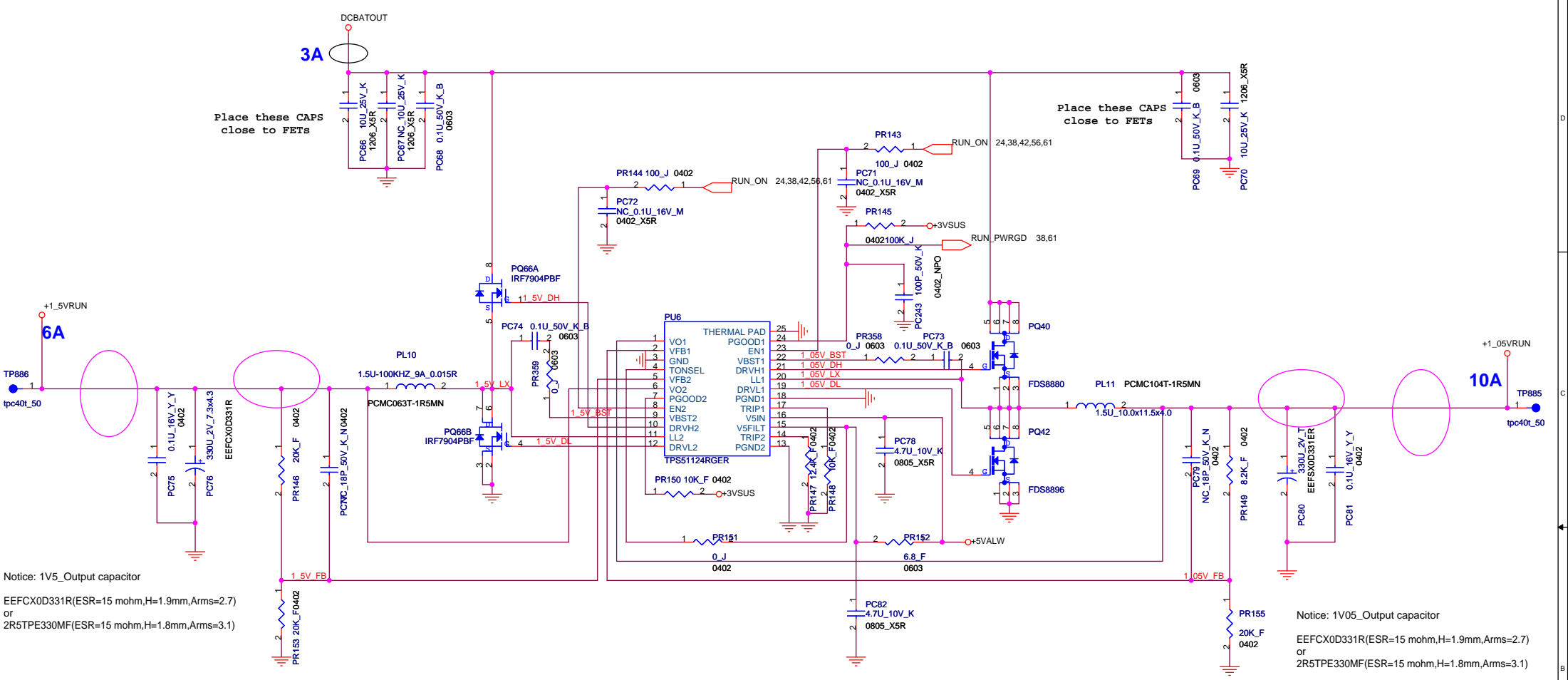
+3VALW OCP trigger point >7.5A

+ECVCC/100mA

+5VALW OCP trigger point >8A

TON connect to VCC = 5V/200KHZ, 3.3V/300KHZ

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
		Title SYS Power (+3.3V/+5V)
Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 52	of 66

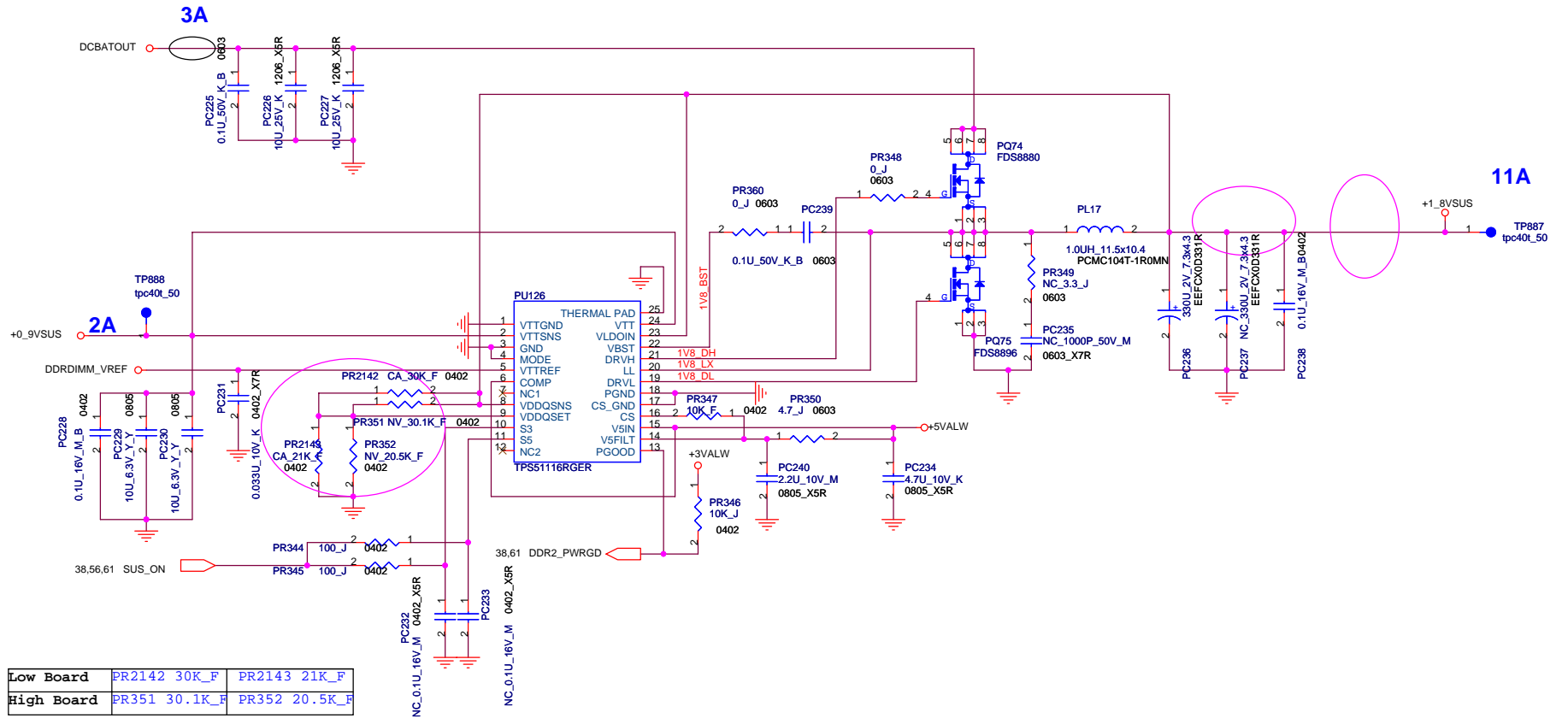


Notice: 1V5_Output capacitor
 EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7)
 or
 2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1)

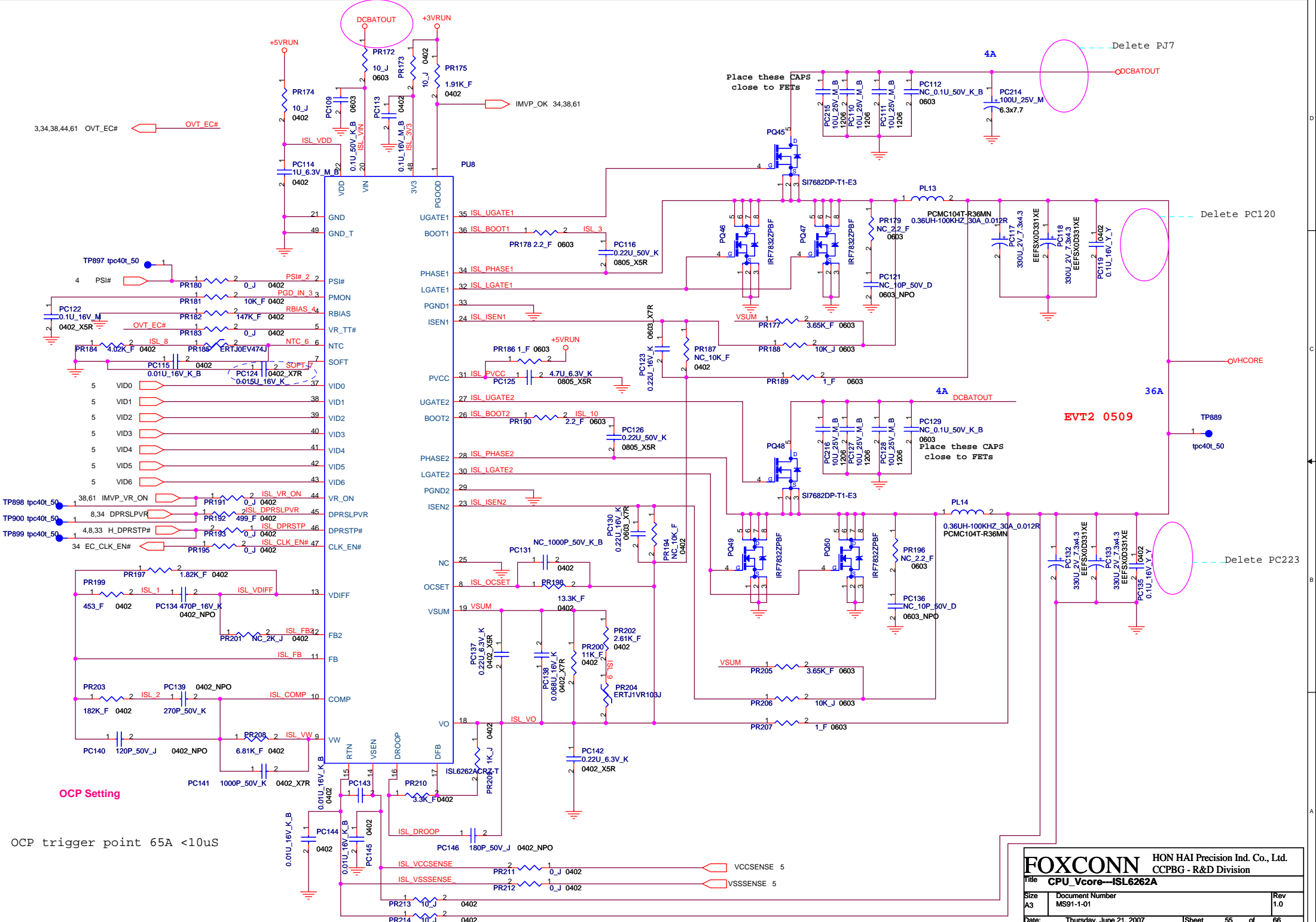
Notice: 1V05_Output capacitor
 EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7)
 or
 2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1)

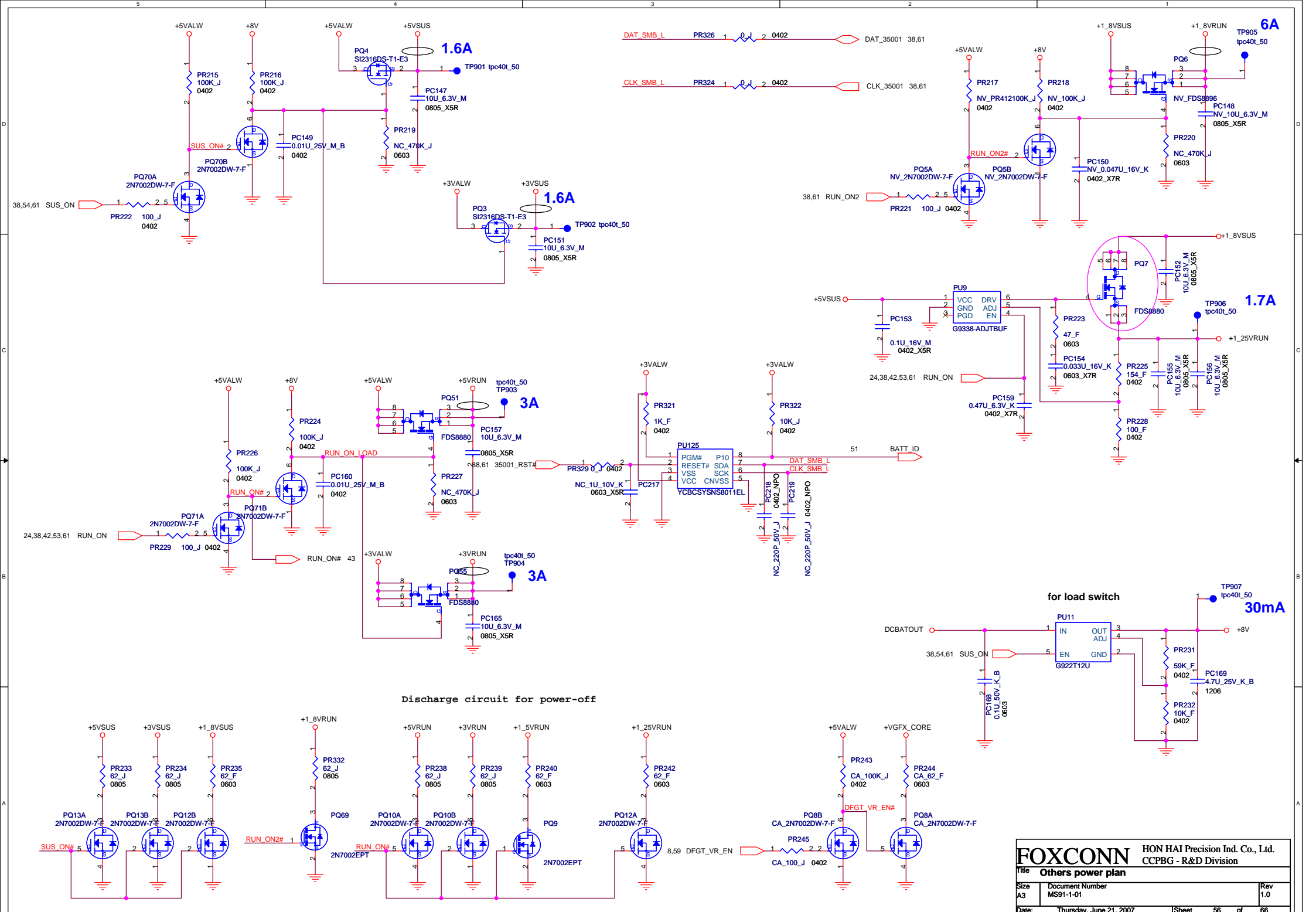
Setting +1_5VRUN OCP trigger point to 10.6A

Setting +1_05VRUN OCP trigger point to 14.2A

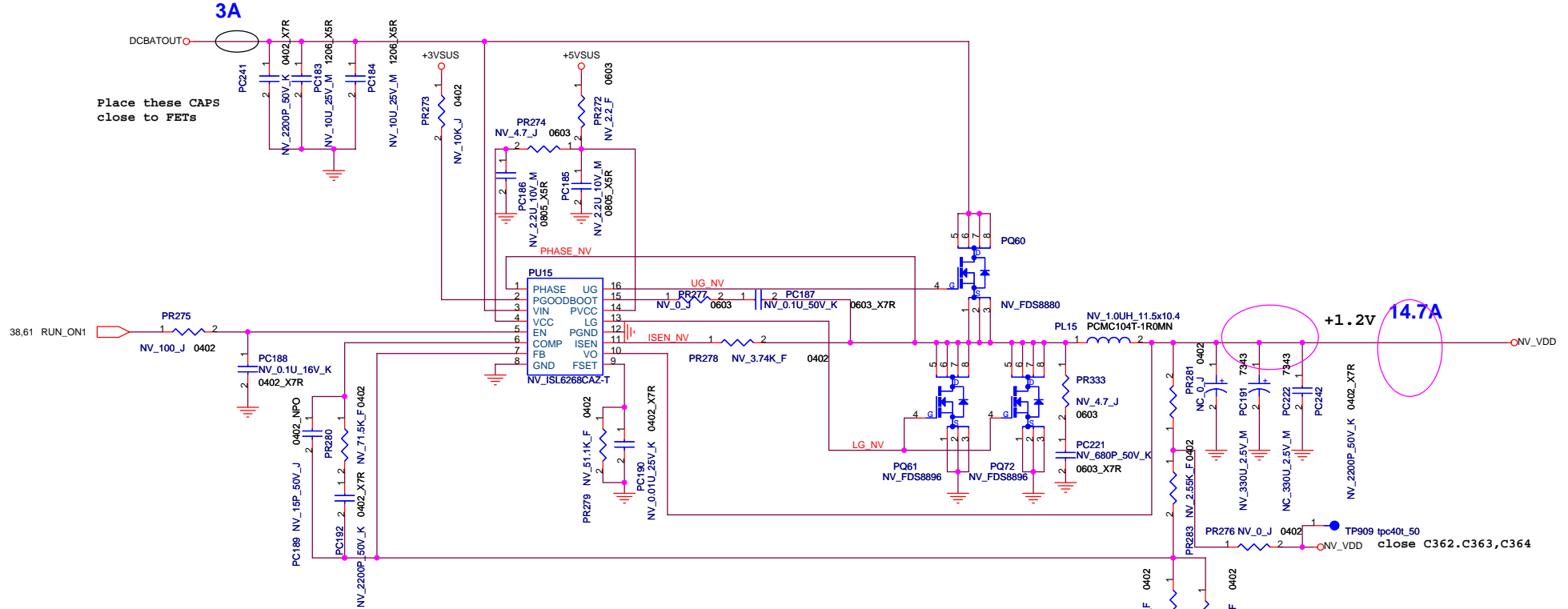


Setting +1_8VSUS OCP trigger point to 16A

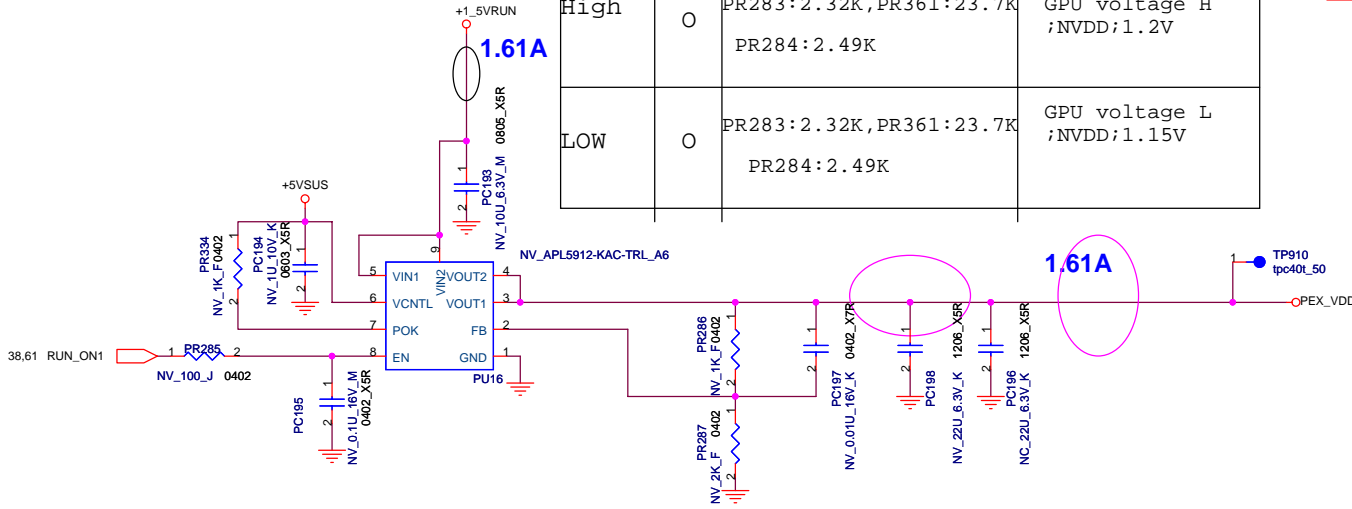


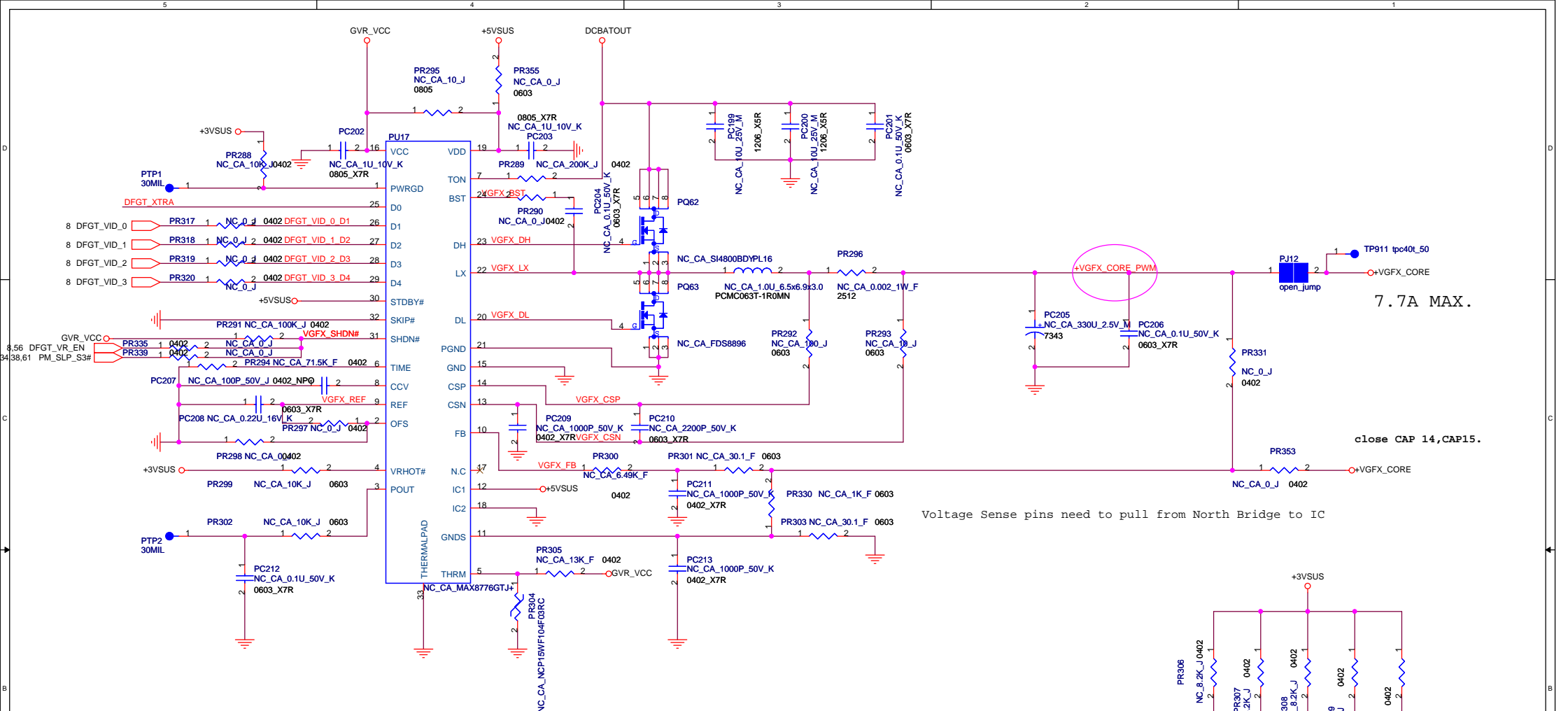


+VGA_CORE Ilimit =22.8A~27.38A



VGA_GPIO5	I/O		GPIO TABLE
High	O	PR283:2.32K, PR361:23.7K PR284:2.49K	GPU voltage H ;NVDD;1.2V
LOW	O	PR283:2.32K, PR361:23.7K PR284:2.49K	GPU voltage L ;NVDD;1.15V



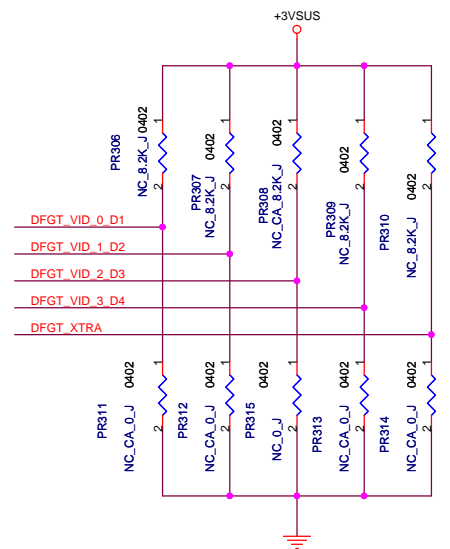


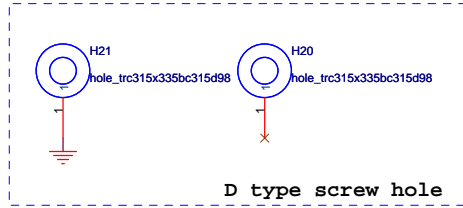
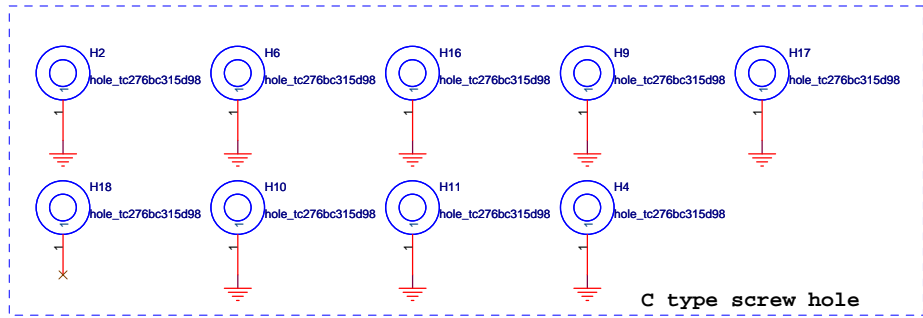
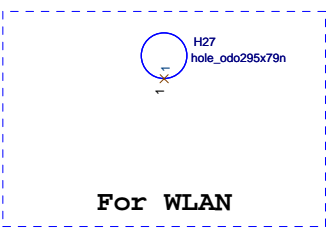
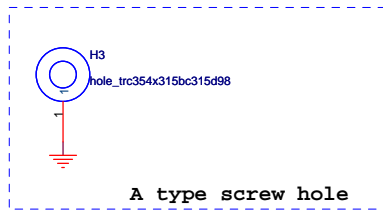
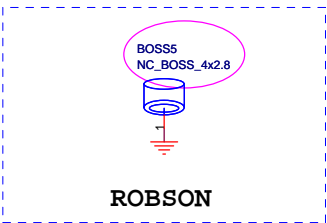
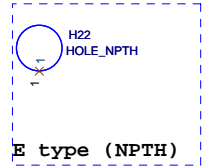
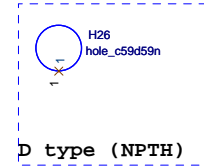
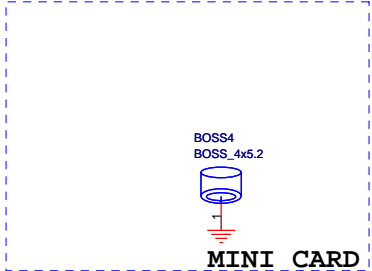
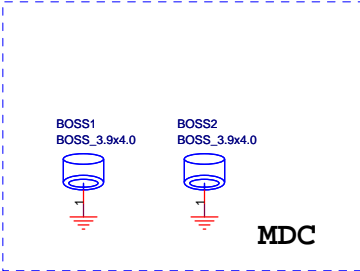
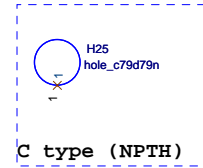
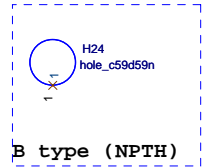
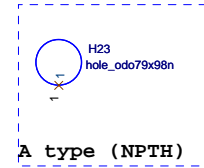
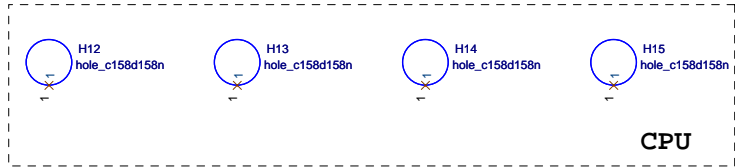
7.7A MAX.

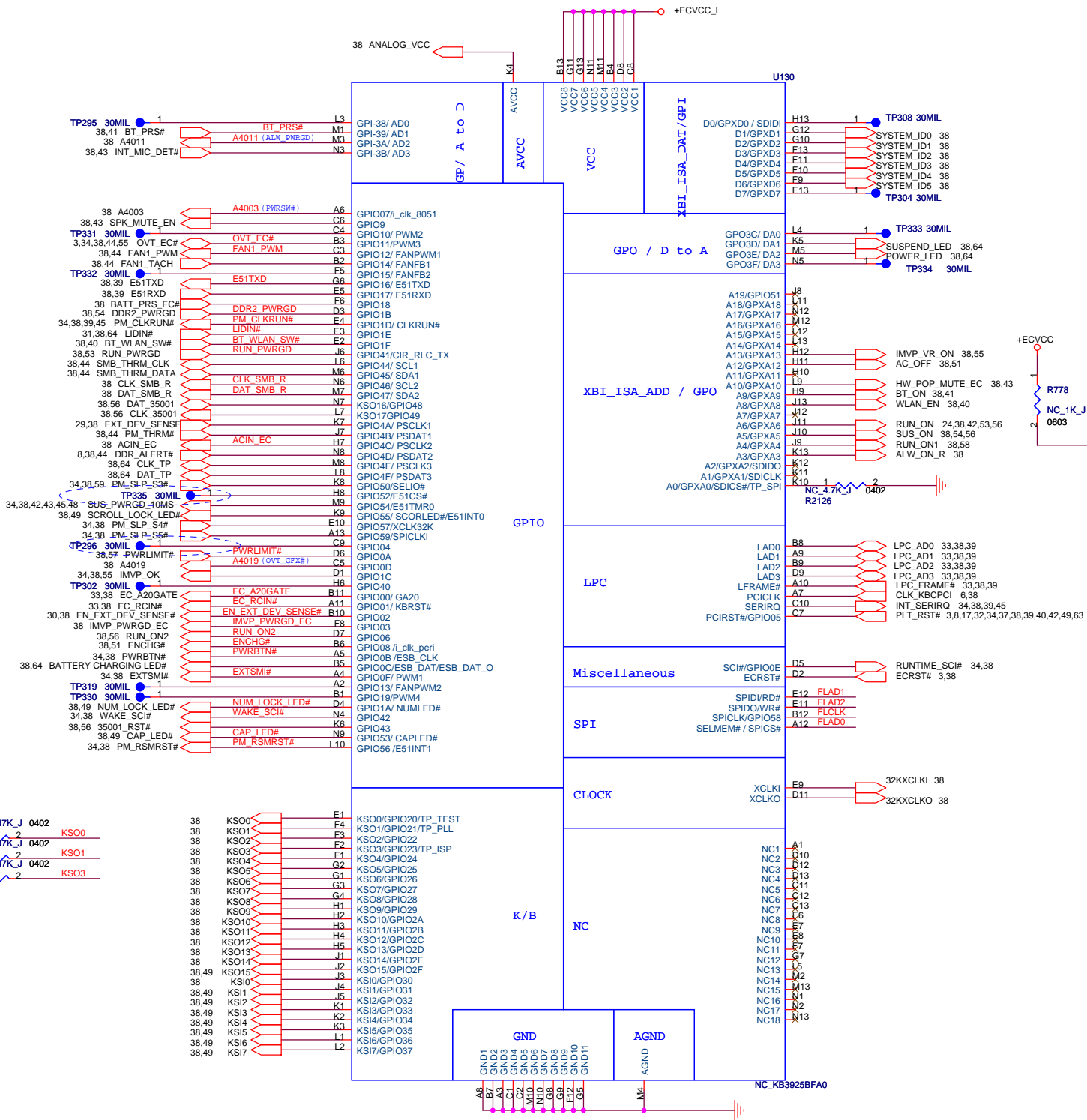
close CAP 14,CAP15.

Voltage Sense pins need to pull from North Bridge to IC

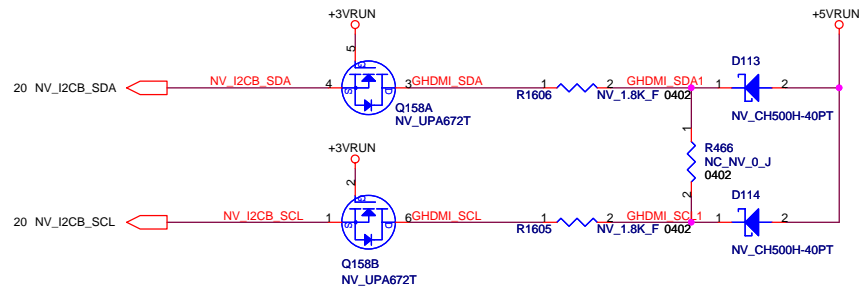
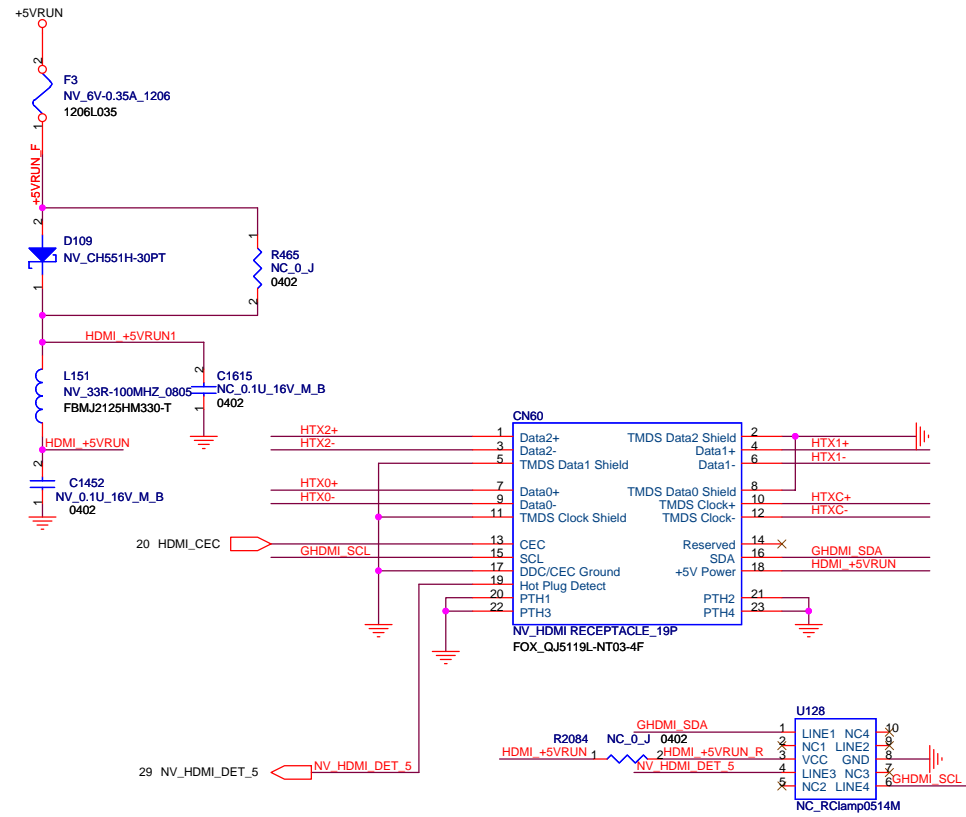
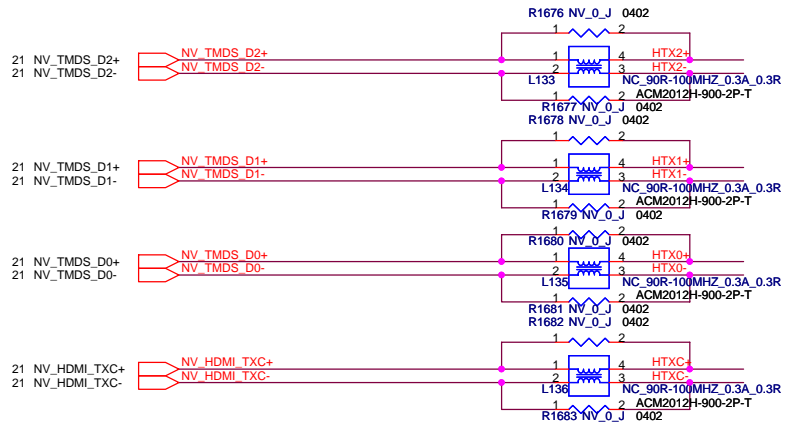
	GMCH W/O	GMCH W				
	PR355	no stuff	PR355	stuff	PR311	no stuff
	PR291	no stuff	PR335	stuff	PR312	no stuff
	PJ12	no stuff	PJ12	stuff	PR308	no stuff
					PR313	no stuff



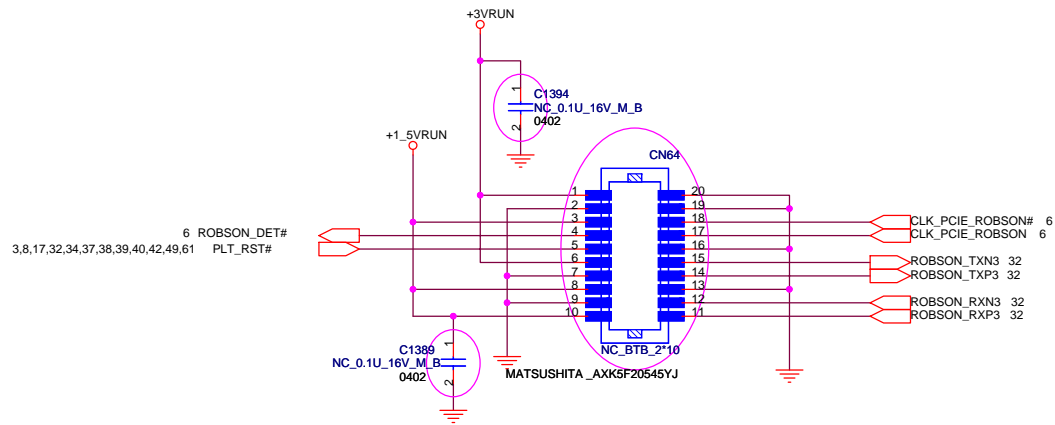




FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title EC+KBC(3925)			
Size A3	Document Number MS91-1-01	Rev 1.0	
Date: Thursday, June 21, 2007	Sheet 61	of 66	



ROBSON Board CONN



C1389,C1394 close to CN64.

MS91 DVT

(2007/04/04)

P.51 Move PF1 close to the PCN1 for MS1X burn out issue.
P.52,53,54,55,58 Add PJ1,PJ2,PJ3,PJ4,PJ5,PJ9,PJ11 for DVT debug.
P.54 Add PR2142, PR2143, change PR352 value 20.5K_F to NV_20.5K_F, PR351 value 30.1K_F to NV_30.1K_F. Because H version and L version need different voltage level.

P.6,32,63 Change RP11 value NC_33 to 33,
C1394 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
C1389 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
C735 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
C730 value NC_0.1U_16V_M_B to 0.1U_16V_M_B,
CN64 value NC_BT_B_2*10 to BTB_2*10,
for robson function need.

(2007/04/06)

p.2 Block diagram update for MS91 feature spec.
P.49 Change U138 from MARVELL 88E8036 to MARVELL 88E8039 for MS91 feature spec.
P.18 Add two Hynix type: 16Mx32 (128-bit) and 16Mx32 (64-bit) for backup solution.
P.18 Change PCI device ID: Change
R231 value NV_2K_J to NVNB8M_2K_J,
R232 value NC_2K_J to NVNB8P_2K_J,
R233 value NC_2K_J to NVNB8P_2K_J,
R234 value NV_2K_J to NVNB8M_2K_J.

(2007/04/09)

p.51 Move the net A6001 close to PF1 for moved PF1.
p.30 Change C666 10P_50V_J_N to NC_10P_50V_J_N,
C669 10P_50V_J_N to NC_10P_50V_J_N,
C671 10P_50V_J_N to NC_10P_50V_J_N for EMI request.
p.30 Add C668,C670,C672 for EMI request.
p.31 Add R459 for nVidia suggest.

(2007/04/11)

p.49 Delete R2110,R2112 for Marvell suggest.
p.38 Change touch pad power from +5VSUS to +5VRUN for design mistake.
p.55 Delete PC120 PC223 for save layout space.

(2007/04/12)

P.1 Add MS91 BOM configuration.
P.60 Change BOSS5 value NC_BOSS_4x2.8 to BOSS_4x2.8 for lock robson.

(2007/04/13)

P.52 Add net name +3VALW_PWM and +5VALW_PWM because add PJ2 and PJ1.
P.53 Add net name +1_5VRUN_PWM and +1_05VRUN_PWM because add PJ4 and PJ3.
P.54 Add net name +1_8VSUS_PWM because add PJ5.
P.55 Delete PJ7 and change DCBATOUT+ to DCBATOUT for save layout space.
P.58 Add net name NV_VDD_PWM and PEX_VDD+ because add PJ9 and PJ11.
P.59 Add net name +VGF_X_CORE_PWM because add PJ12.

(2007/04/16)

P.1 Dropped the NB8P-SE/128MB and NB8P-SE/64M for MOR request.
P.18 Delete two Hynix type: 16Mx32 (128-bit) and 16Mx32 (64-bit) for needless to backup solution.

(2007/04/17)

P.44 Add U8 solution for H/L has different thermal sensor.
Change Q176 value from CA_MMBT3904.215 to NC_MMBT3904.215 for new solution.
P.44 Delete C62,U139,R2031,R2032,R73 for delete VGA thermal sensor.
P.24 Change MIOB_VDD current from 900mA to 10mA.
NV_DACA_VDD from 135mA to 130mA.
NV_DACB_VDD from 200mA to 130mA.
NV_PLLVDD from 60mA to 35mA+35mA.
IFP_CDI0VDD from 150mA+150mA to 50mA+50mA.
IFPCD_PLLVDD from 35mA to 75mA.
IFP_ABIOVDD from 130mA+130mA to 45mA+45mA.
IFPAB_PLLVDD from 35mA to 75mA for power budget spec.

P.25 P.26 Change FBA_PLLAVDD from 30mA to 15mA.
FBC_PLLAVDD from 30mA to 15mA.
Change NB8M-GT xx mA to NB8X 1.5A.
PEX_PLL_AVDD from 100mA to 75mA.
PEX_PLL_DVDD from 20mA to 10mA.
VDD33 from 110mA to 50mA.
NV_VDD from 16.25A to 13.37A.
change NB8M-GT : 1.1V(TBD) to NB8X : 1.2V for power budget spec.
Add H_PLLVDD power budget spec 15mA.

P.27,P.28 Add +1_8VRUN power budget spec 1.125A.
change +1_8VRUN from 1.2A to 1.125A for power budget spec.
P.1 Update the PCB P/N.

(2007/04/17)

P.17,P.19,P.20,P.21,P.22,P.23,P.24,P.25,P.26 Change U7A,U7D,U7E,U7F,U7H,U7G,U7C,U7I value from NB8M-GT-B-A2/H to NV_NB8M-GT-B-A2/H.
P.20 Change U82 to NV_ for low board needless it.

(2007/04/23)

P.56 PQ7 Change from SI4800BDY to FDS8880 because the +1_25VRUN load increase.
P.33 Add TP287 for test the RTCRST#.
P.49 Add C1559,TP288 for stable AV mode start.

(2007/04/24)

P.38 Change R715 to NV_ for low board needless it.

(2007/04/24)

P.44 Change U4 from MAX6509HAUK-T+ to G709T1UF for PUR request.

(2007/04/27)

P.44,45,46 Change U132 from 12-PC18402-0000 to 12-SPC1840-0000 for PUR suggest.

(2007/05/07)

P.11 Change D6,R4 from CA_ to stuff all the SKU for Intel suggest.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title History (1)			
Size A3	Document Number MS91-1-01	Rev 1.0	
Date	Thursday, June 21, 2007	Sheet	65 of 66

MS91 PVT

(2007/05/30)

P.43 Add Polyswitch (F7) and resistor (R2142)_NC co-layout on USB power input of M/B for TUV

P.48 Add Polyswitch (F8) and change resistor R972 from stuff to NC co-layout on USB power input of M/B for TUV

(2007/06/01)

P.6,32,60,63 Change RP11 value 33 to NC_33,
C1394 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
C1389 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
C735 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
C730 value 0.1U_16V_M_B to NC_0.1U_16V_M_B,
CN64 value BTB_2*10 to NC_BTB_2*10,
Change BOSS5 value BOSS_4x2.8 to NC_BOSS_4x2.8 for lock robson.
for robson function Disable.

(2007/06/05)

P.52,53,54,55,58 Del PJ1,PJ2,PJ3,PJ4,PJ5,PJ9,PJ11 for PVT stage.

P.52 Del net name +3VALW_PWM and +5VALW_PWM becuase del PJ2 and PJ1.

P.53 Del net name +1_5VRUN_PWM and +1_05VRUN_PWM becuase del PJ4 and PJ3.

P.54 Del net name +1_8VSUS_PWM becuase del PJ5.

P.58 Del net name NV_VDD_PWM and PEX_VDD+ becuase del PJ9 and PJ11.

P.43 Change C1398 Pin 1 net name from +5VALW to +5V_USB0_1.

P.48 Del co-layout resistor R971,R973 for level 6 suggest.

P.41 Del TP854 for level 6 suggest.

(2007/06/07)

P.43 Del Polyswitch (F7) and resistor (R2142)_NC on USB power input of M/B for MOR suggest.

P.48 Del Polyswitch (F8) and change resistor R972 from NC to stuff on USB power input of M/B for MOR suggest.

(2007/06/08)

P.1,18 Add three BOM on BOM configuration for Hynix VRAM.

P.38,49 Add option circuit for keyboard auto power on issue.

1> Del TP294

2> Add R2142(NC),R2143(NC),R2144(NC),R2145,R2146,R2147(NC).

P.37 CN32 change from 2N-0050004-FKG0 to 2N-0050006-FKG0 for level 6 suggest.

(2007/06/12)

P.24 Add R2148,R2149 for HDMI leakage issue.

P.30 R/G/B add C1762(NC),C1763(NC),C1764(NC) for EMI suggest.

(2007/06/20)

P.49 LAN controller U138 change from 88E8039 to 88E8036 for EMI fail issue.

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
History (2)			
Title	Document Number		Rev
A3	MS91-1-01		1.0
Date:	Thursday, June 21, 2007	Sheet	66 of 66