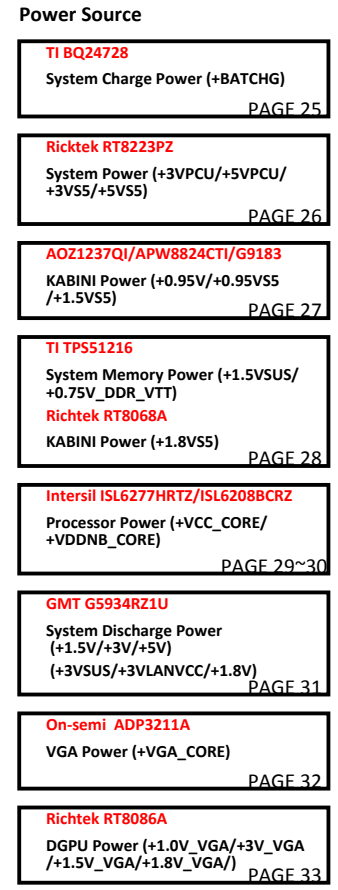
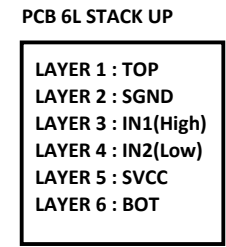
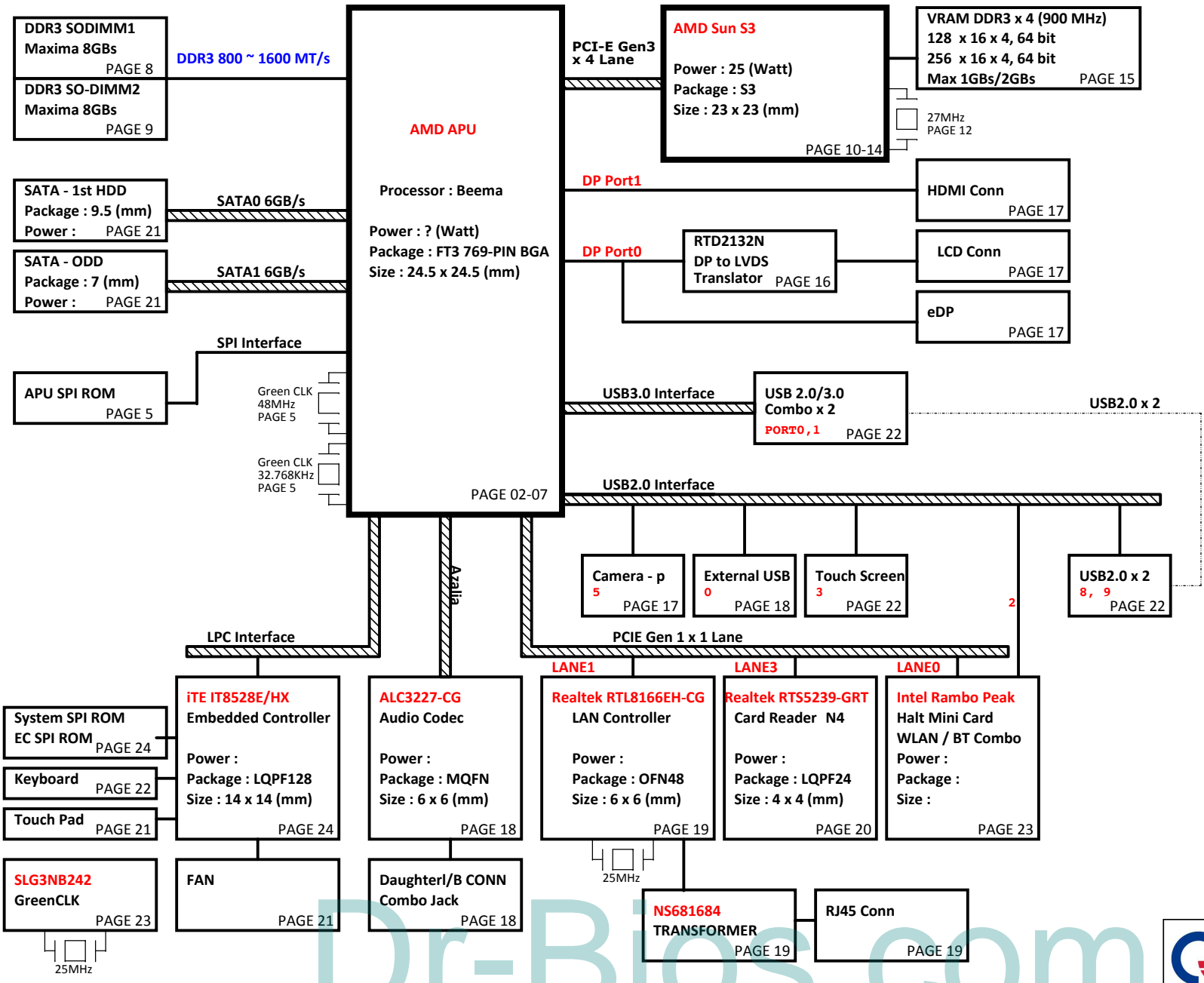


Lean G_AMD Beema DIS/UMA (14"/15.6")

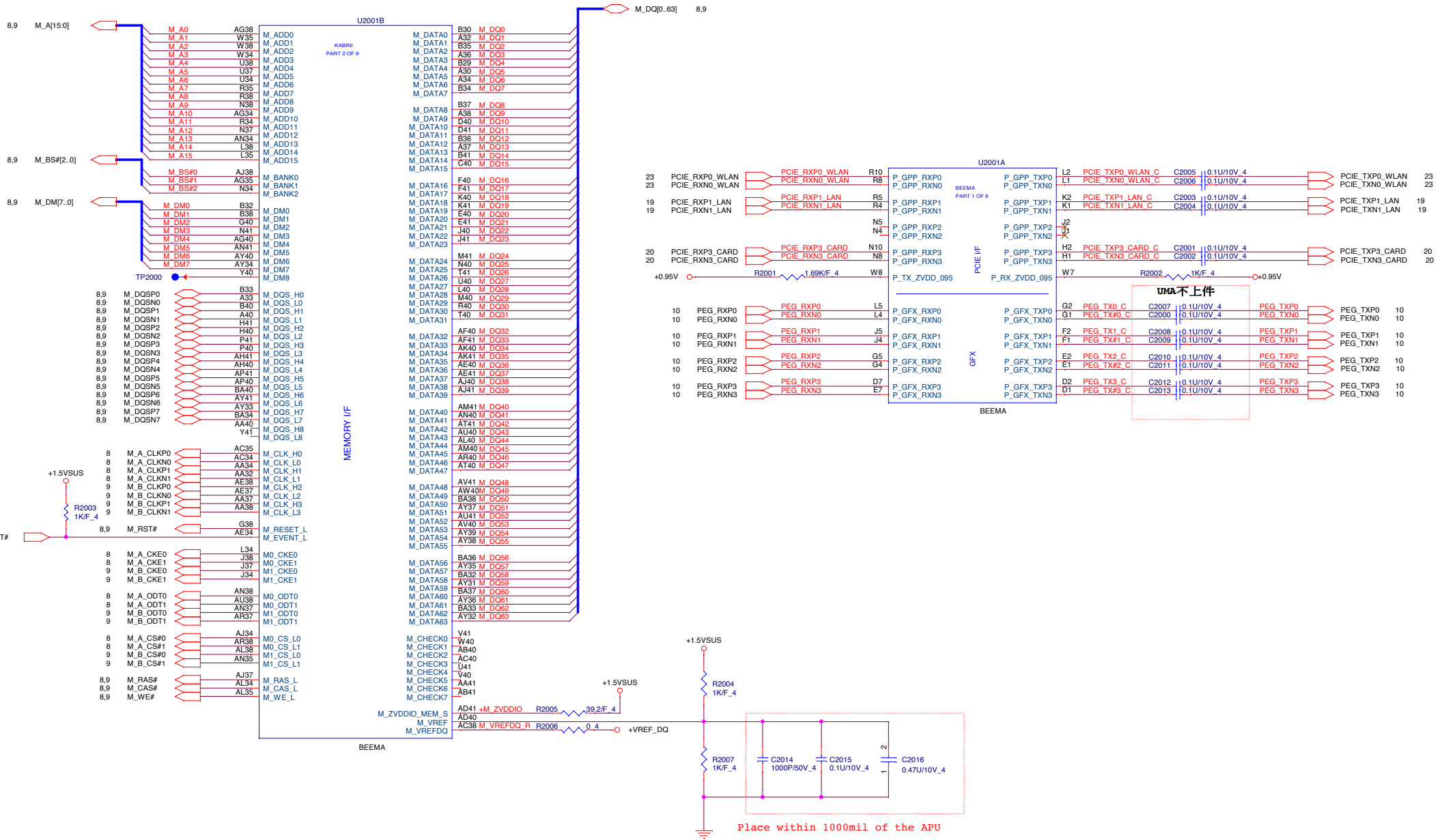
Ultra/Slim




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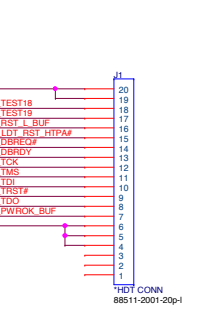
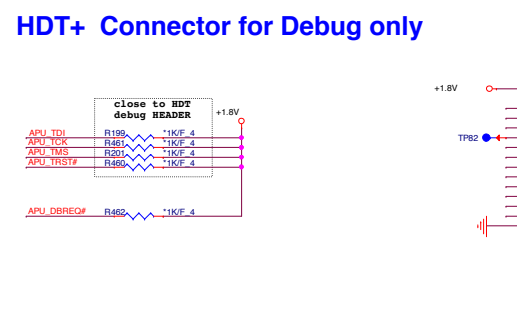
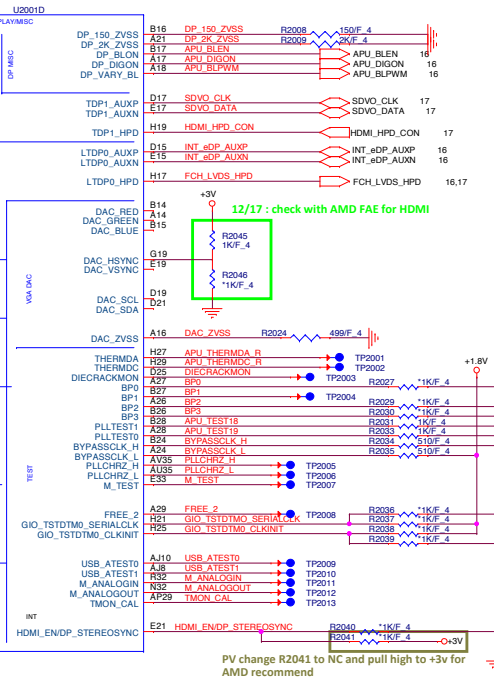
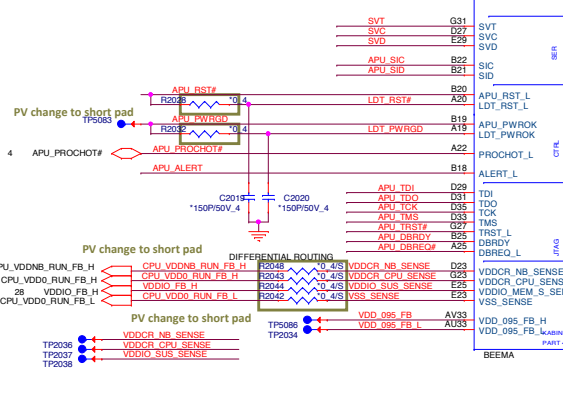
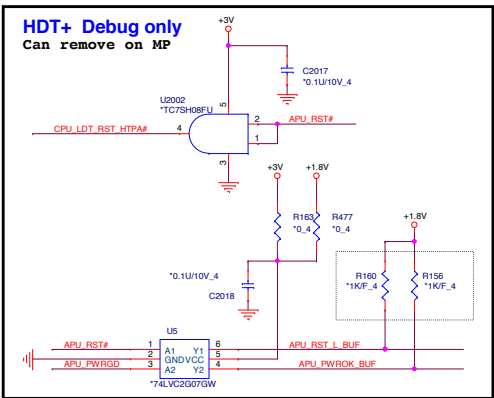
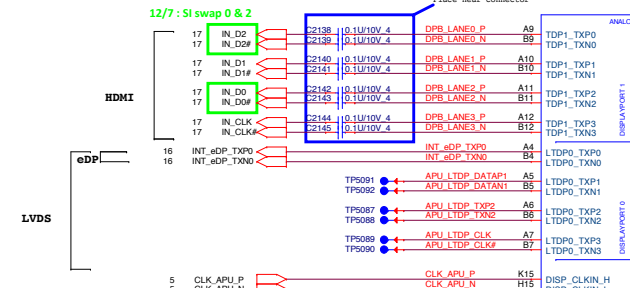
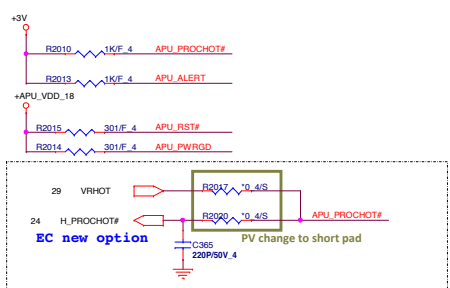
PROJECT :U99
Quanta Computer Inc.

Size A3	Document Number	Rev 1A
Block Diagram(for HP)		
Date: Monday, May 19, 2014	Sheet	1 of 33

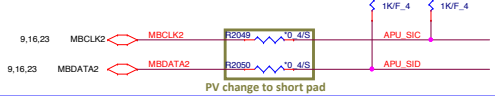


6,8,9,28,31,33 +1.5VSUS
 8,9 +VREF_DQ
 5,6,27 +0.95V

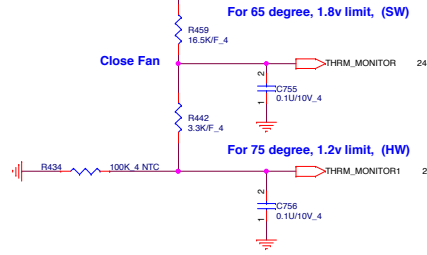
 PROJECT :U99 Quanta Computer Inc.		
Size	Document Number	Rev
	MEM/PCIE (1/6)	1A
Date:	Monday, May 19, 2014	Sheet 2 of 33



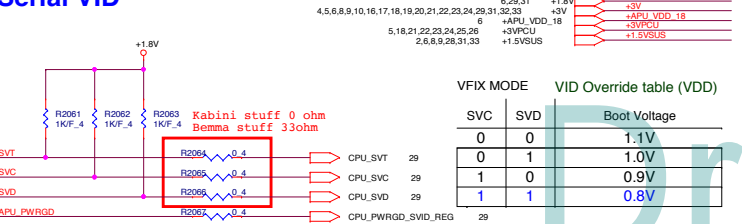
Thermal Sensor



IO Thrm Protect



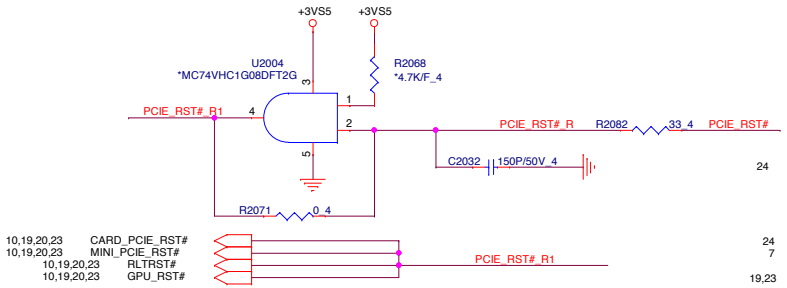
Serial VID



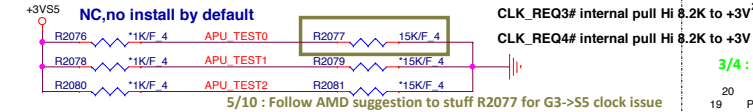
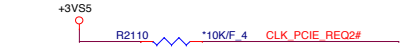
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

PROJECT :U99
Quanta Computer Inc.



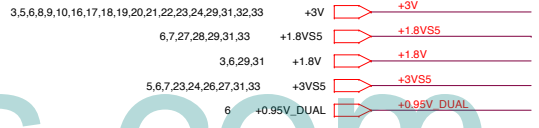
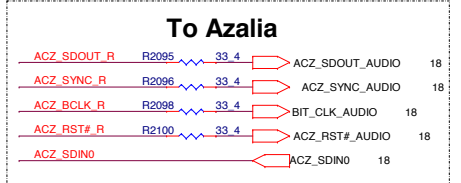
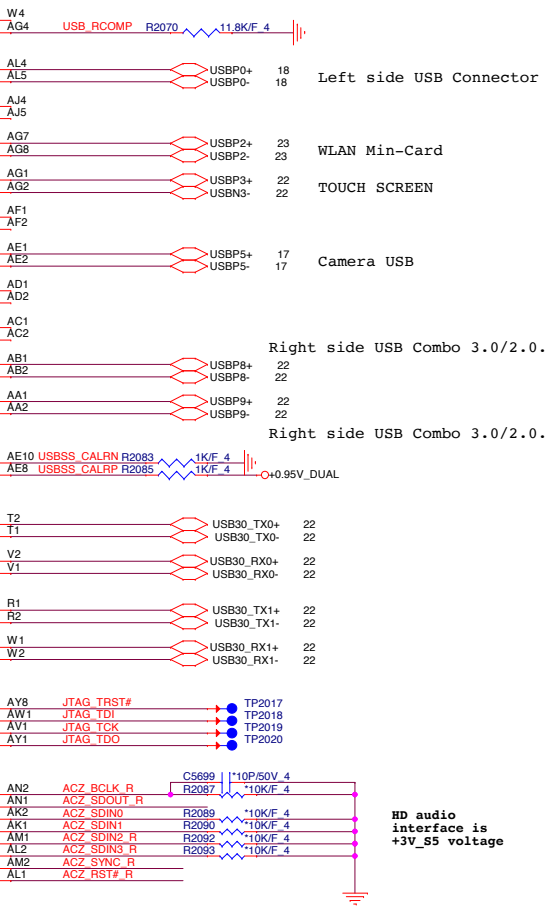
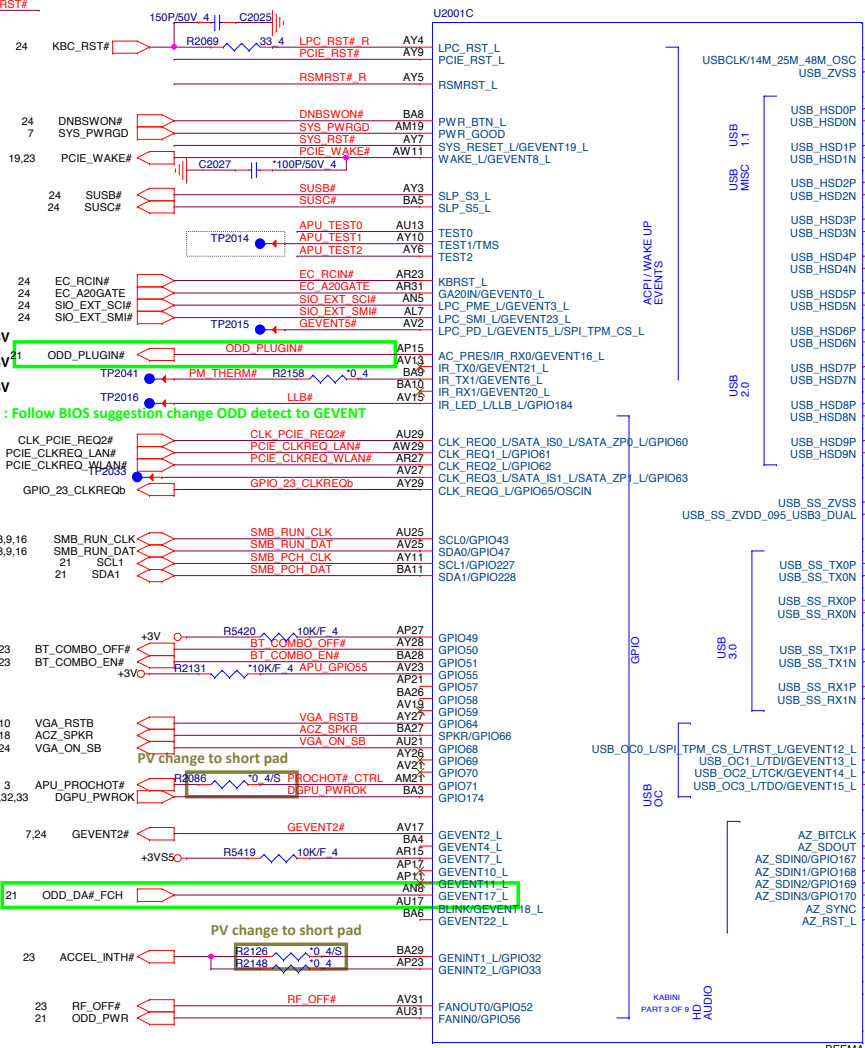
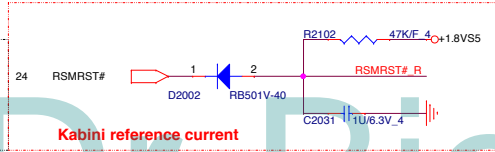
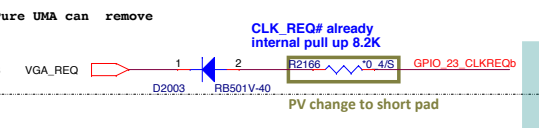
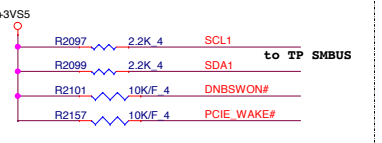
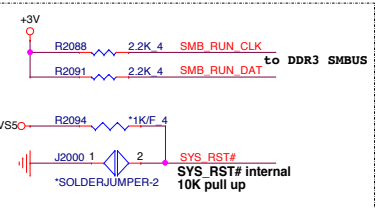


10,19,20,23 CARD_PCIE_RST#
10,19,20,23 MINI_PCIE_RST#
10,19,20,23 RLTRST#
10,19,20,23 GPU_RST#



5/10 : Follow AMD suggestion to stuff R2077 for G3->S5 clock issue

TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted. FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



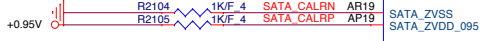
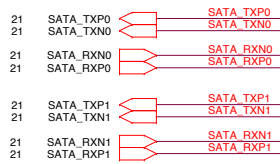
PROJECT :U99
Quanta Computer Inc.

Size Document Number
GPIO/USB/AZ (3/6)

Date: Monday, May 19, 2014 Sheet 4 of 33

SATA HDD

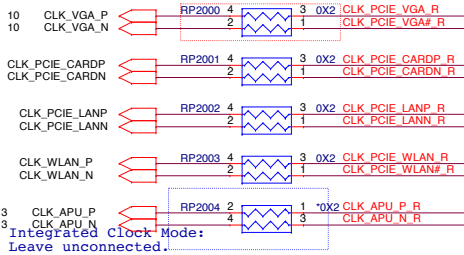
SATA ODD



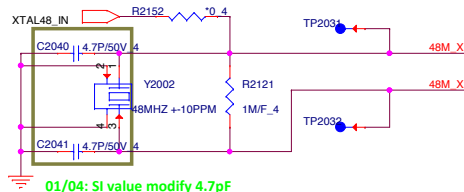
Use with external clock generator only
 TP2039 ← AY12
 TP2040 ← BA12

Integrated Clock Mode:
 Leave unconnected.

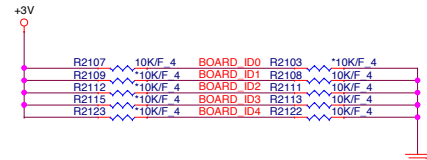
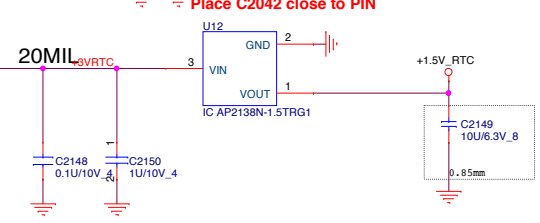
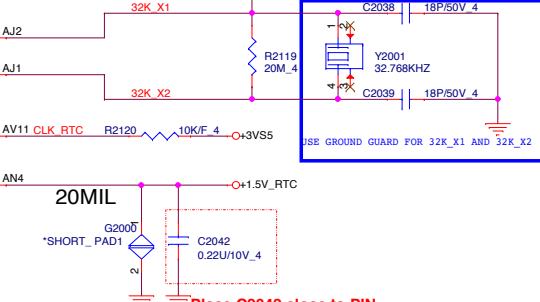
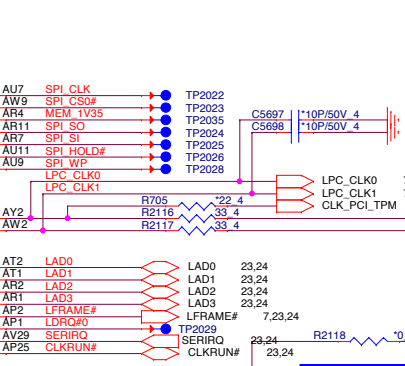
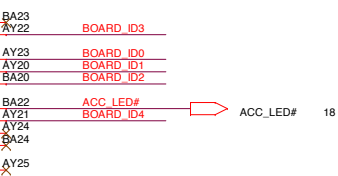
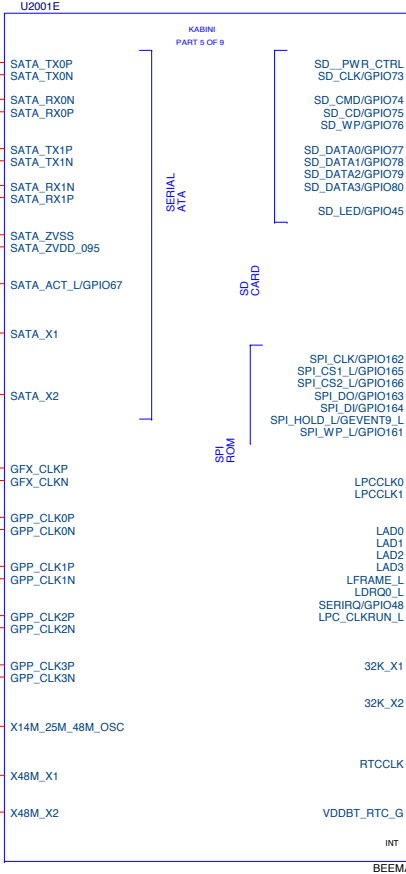
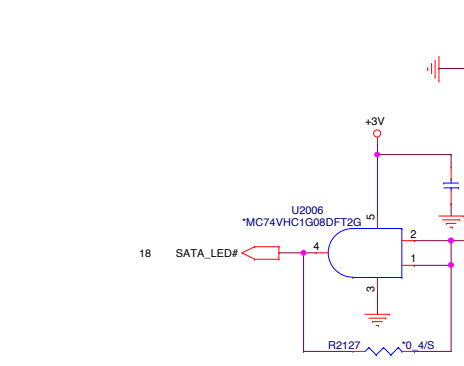
UMA不上件



Integrated Clock Mode: Leave unconnected.



01/04: SI value modify 4.7pF



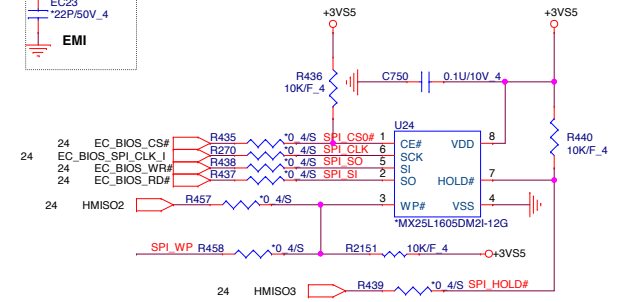
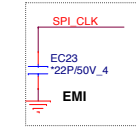
BOARD ID SETTING

Model	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4
14" UMA	0	0	0	0	0
15" UMA	0	1	0	0	0
14" DIS	1	0	0	0	0
15" DIS	1	1	0	0	0

APU SPI ROM

Replace to MX25L6436E

Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023

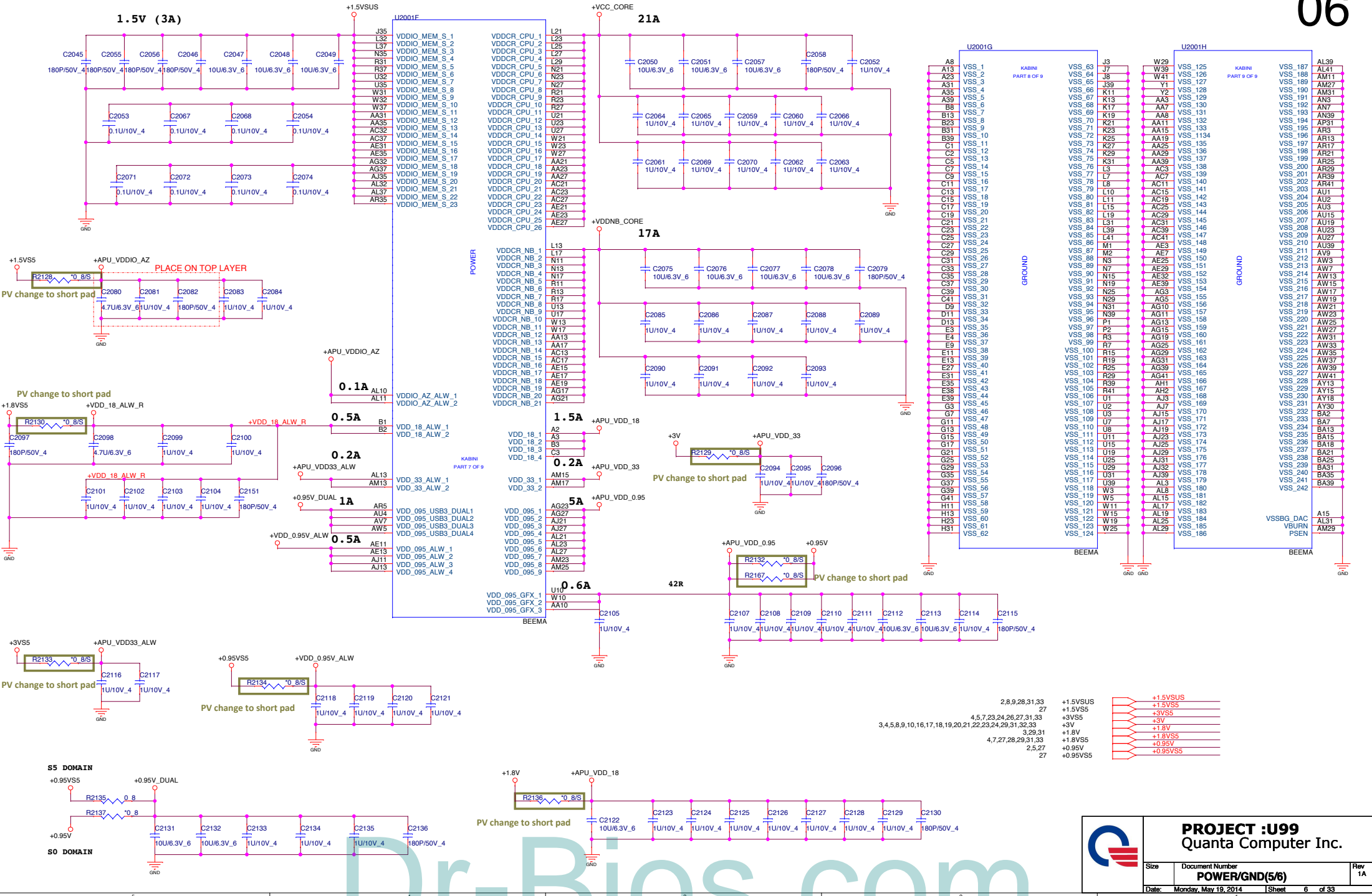


un-mount

PROJECT :U99
 Quanta Computer Inc.

Size	Document Number	Rev
	SATA/CLK (4/6)	1A
Date:	Monday, May 19, 2014	Sheet 5 of 33

PV change to 5.6P for vender's suggestion

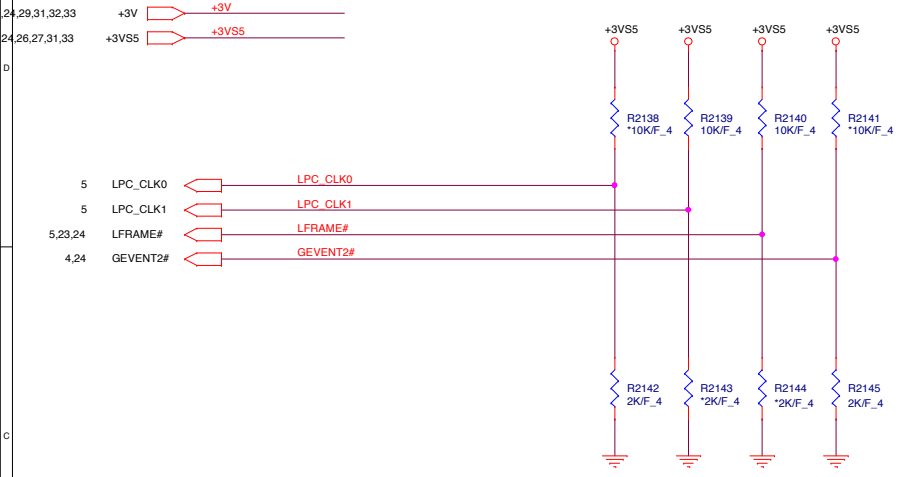


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STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

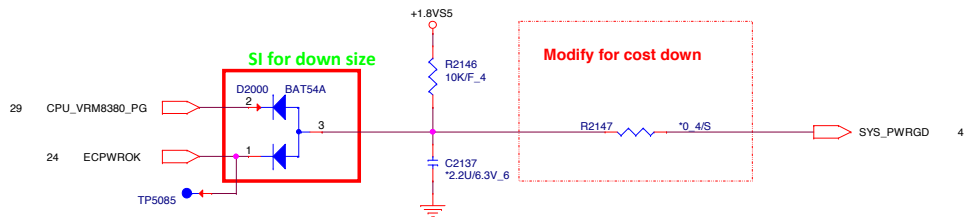
DEBUG STRAPS



REQUIRED STRAPS

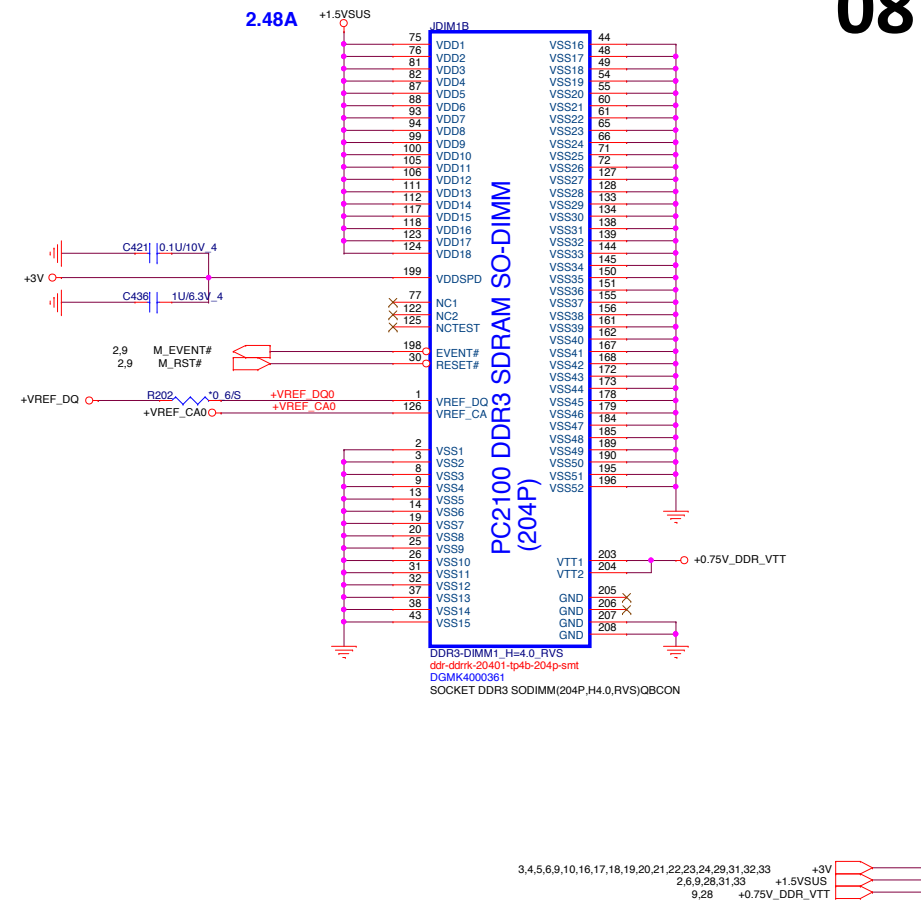
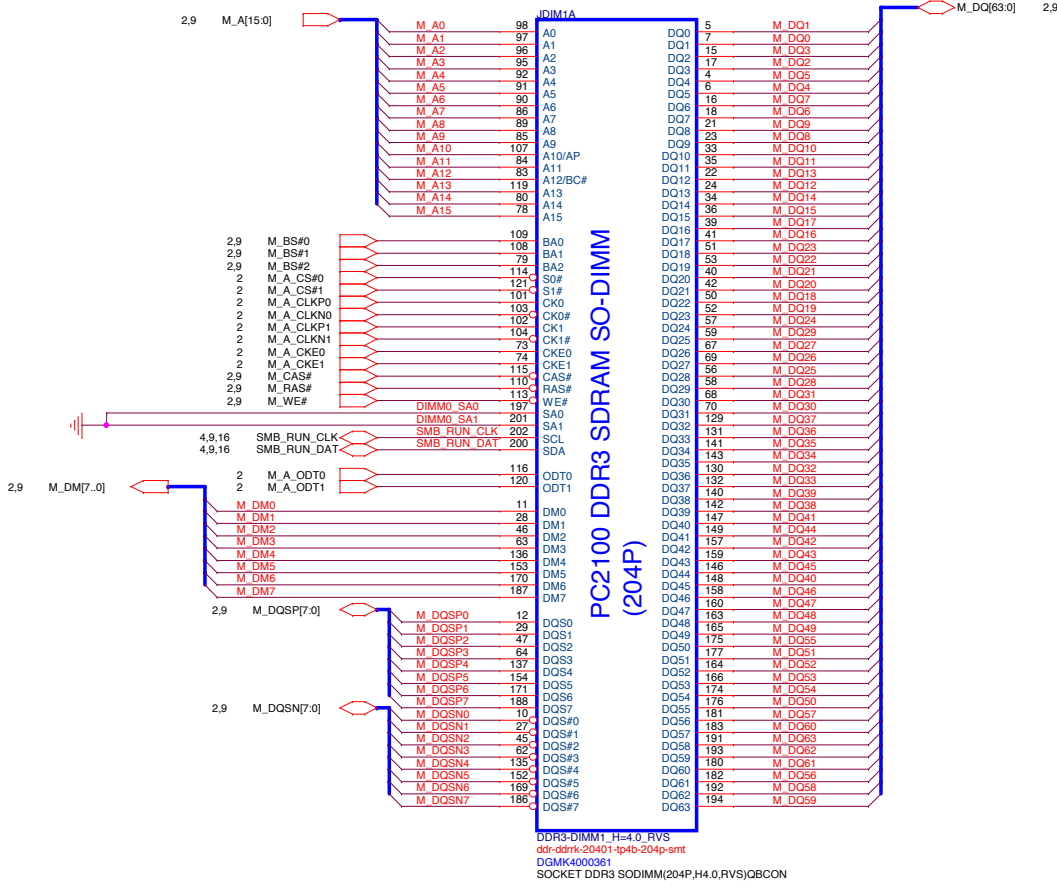
				LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH				BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW				BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

SYS_PWRGD

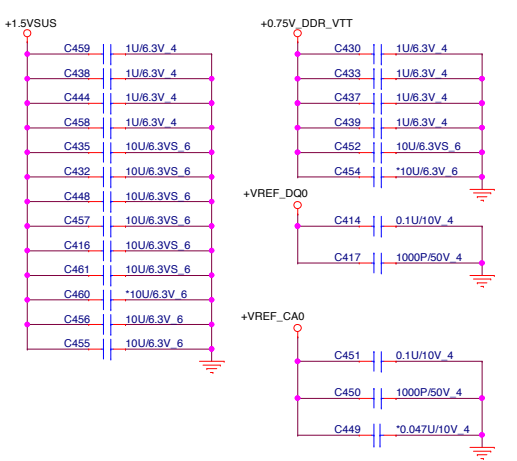


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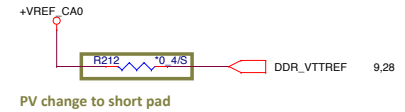
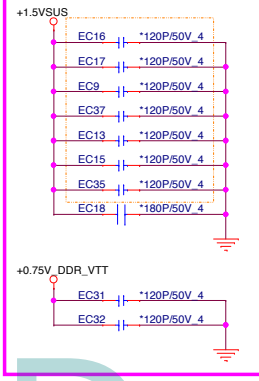
	PROJECT :U99 Quanta Computer Inc.		
	Size	Document Number	Rev
	STRAP (6/6)		1A
Date: Monday, May 19, 2014		Sheet 7 of 33	



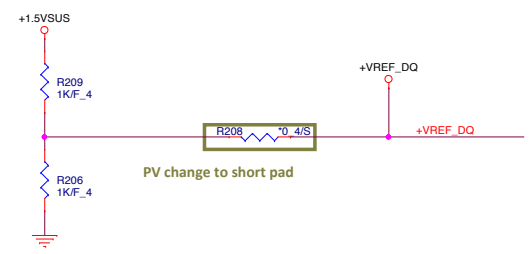
Place these Caps near So-Dimm0.



For EMI RESERVE

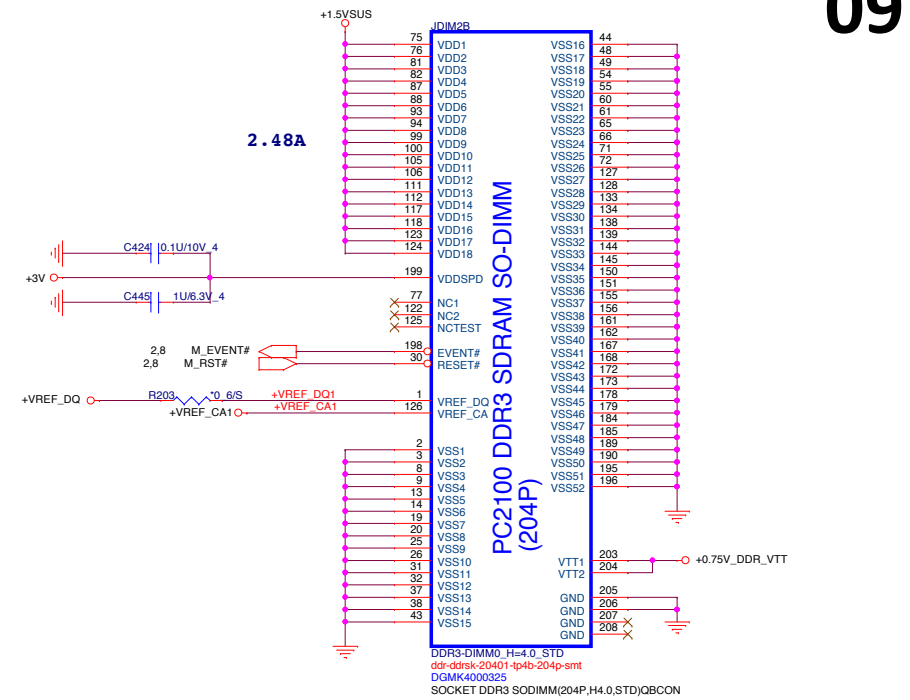
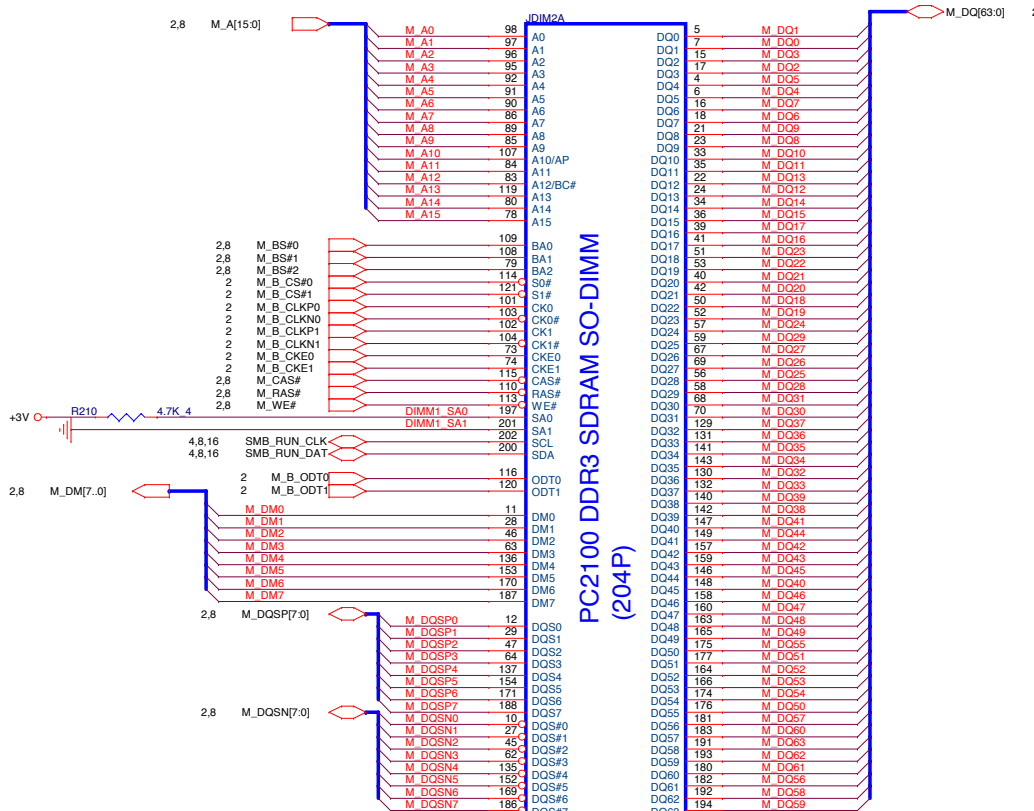


Reserved for AMD suggest



PROJECT :U99
 Quanta Computer Inc.

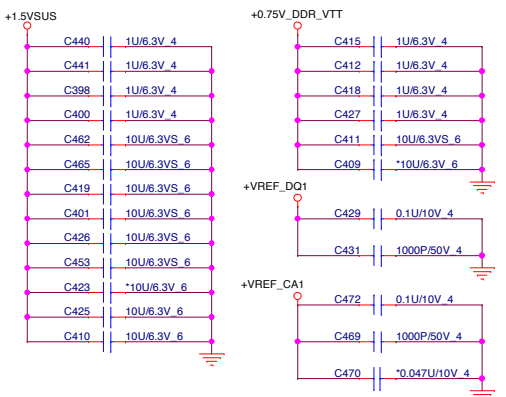
Size Custom	Document Number System Memory 1/2 (5.2H)	Rev 1A
Date: Monday, May 19, 2014	Sheet 8 of	33



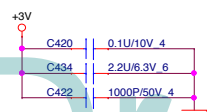
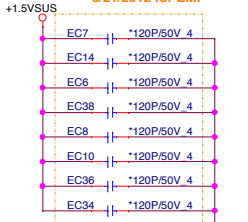
DDR3-DIMM0_H=4.0_STD
 ddr-ddrsk-20401-tp4b-204p-smt
 DGMK4000325
 SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCON

3,4,5,6,8,10,16,17,18,19,20,21,22,23,24,29,31,32,33 +3V
 2,6,8,28,31,33 +1.5VSUS
 8,28 +0.75V_DDR_VTT

Place these Caps near So-Dimm1.

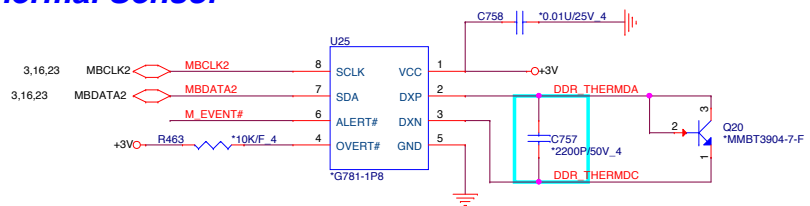


For EMI RESERVE
 6/21/2012 for EMI



Local Thermal Sensor

DDR3 Thermal Sensor

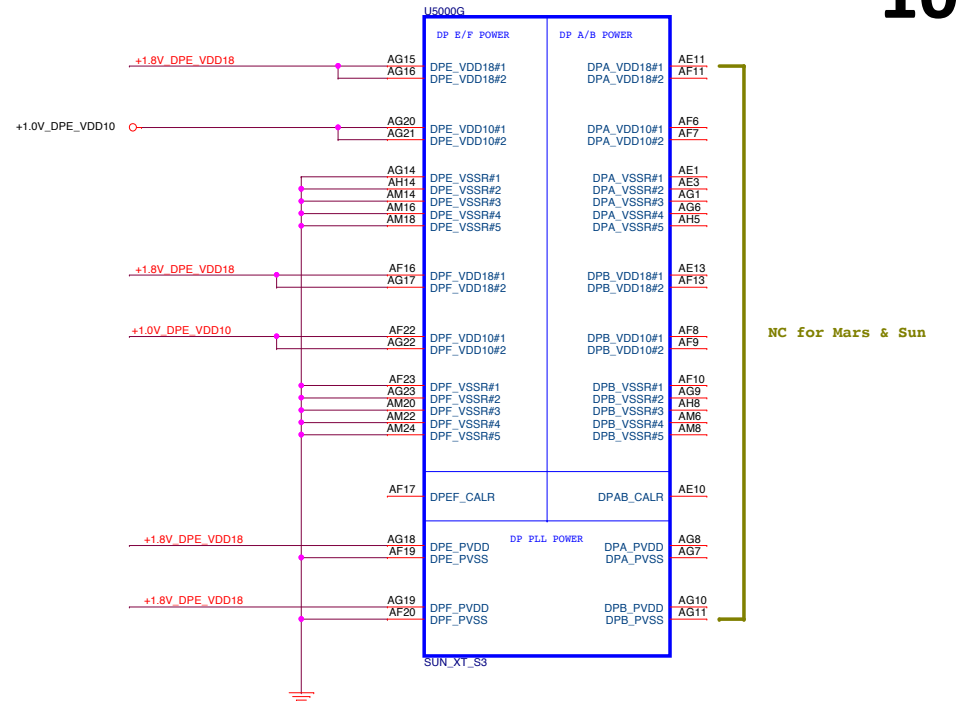
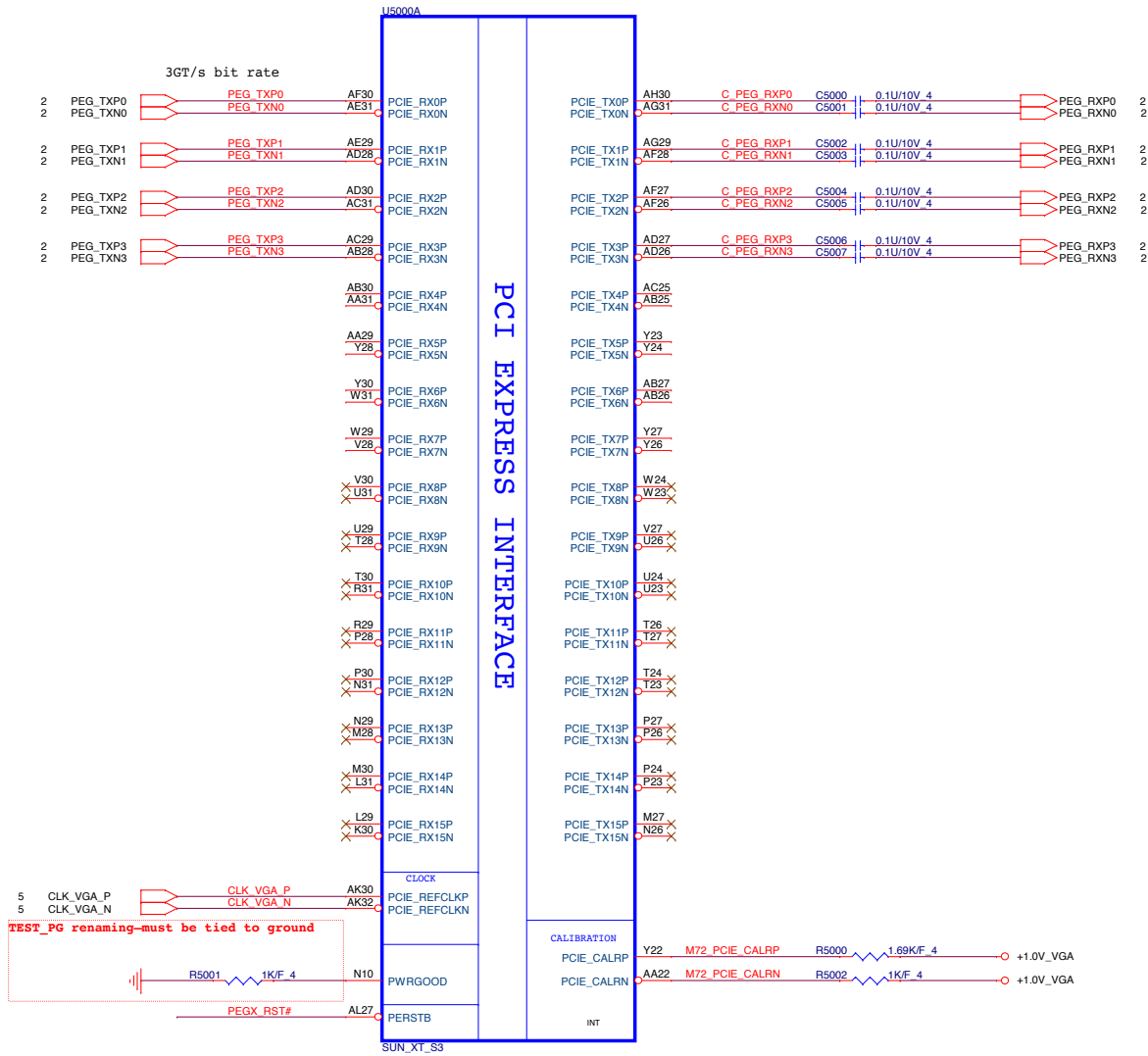


If use internal thermal IC, C9007 use 0ohm.

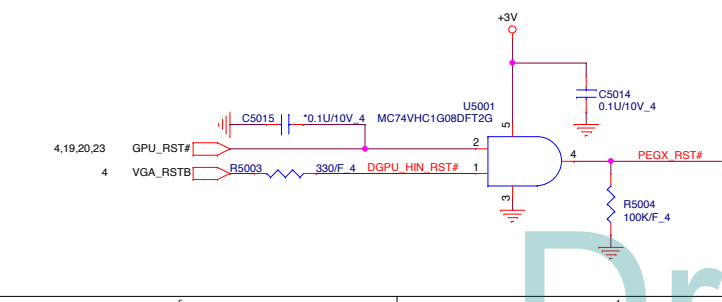
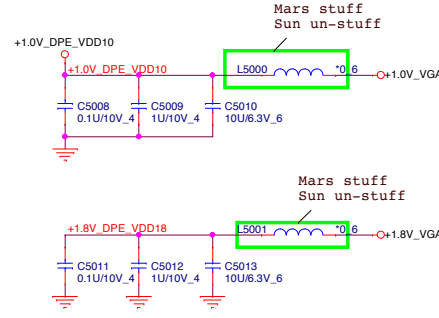
Main:AL000781039 G781-1P8(9Ah)
 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
 2nd:AL000431014 TMP431ADGKR(98h)

<p>PROJECT :U99 Quanta Computer Inc.</p>		
Size Custom	Document Number System Memory 2/2 (9.2H)	Rev 1A
Date: Monday, May 19, 2014	Sheet 9	of 33



NC for Mars & Sun



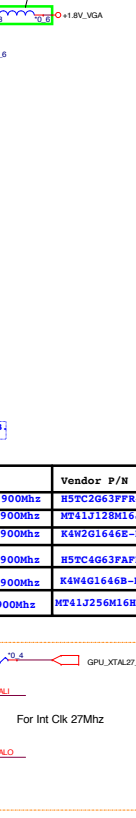
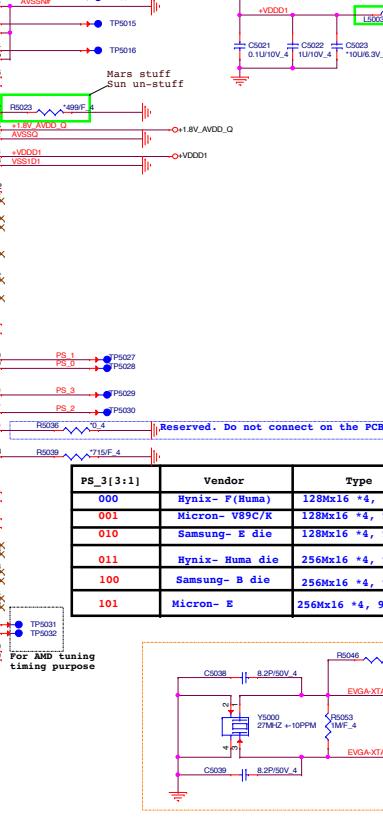
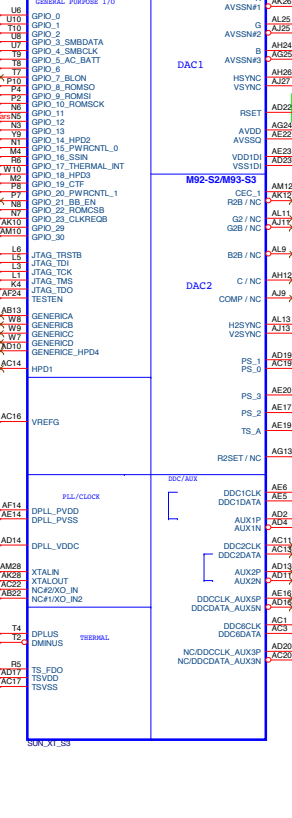
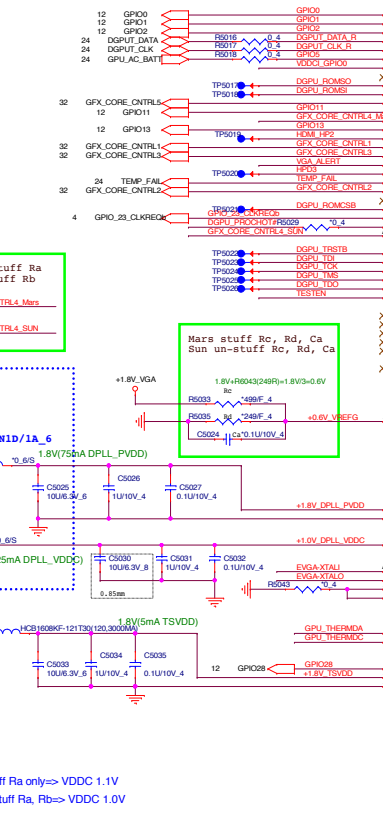
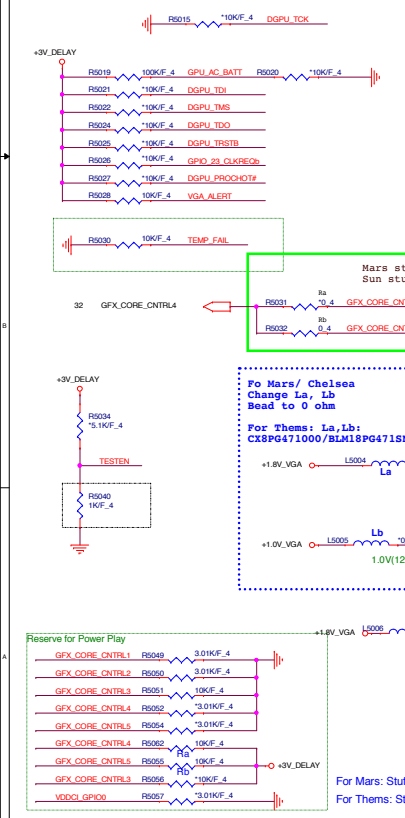
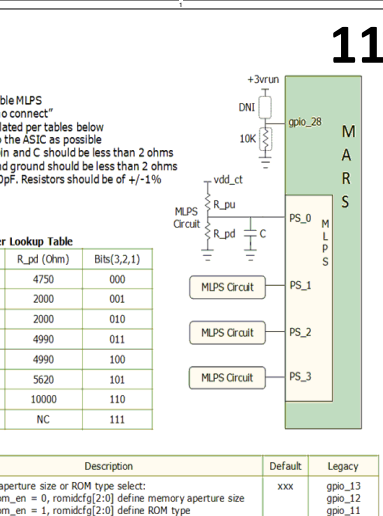
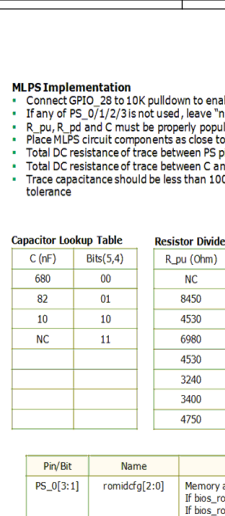
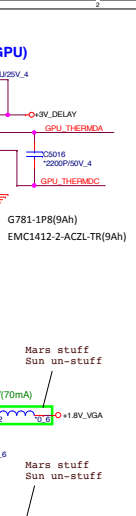
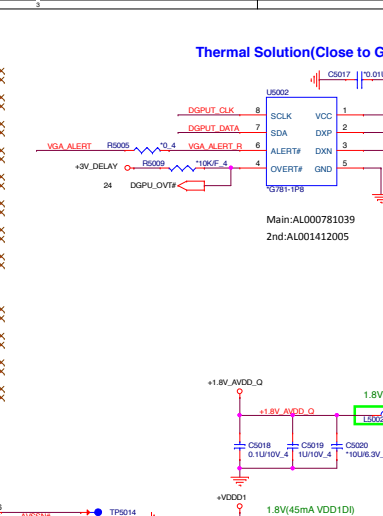
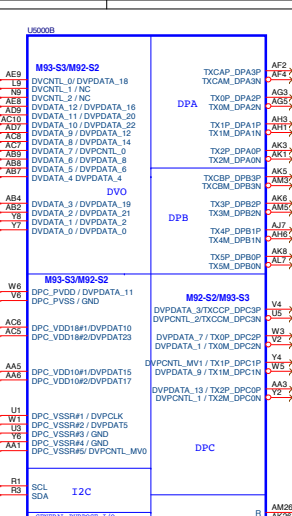
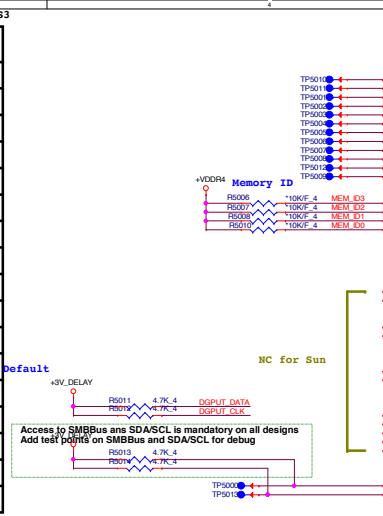
+1.0V_VGA 11:13,33
+1.8V_VGA 11:13,23,33

PROJECT :U99
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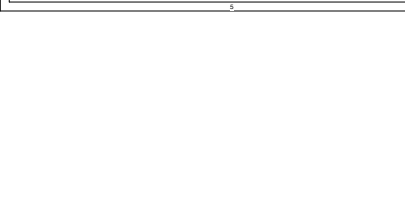
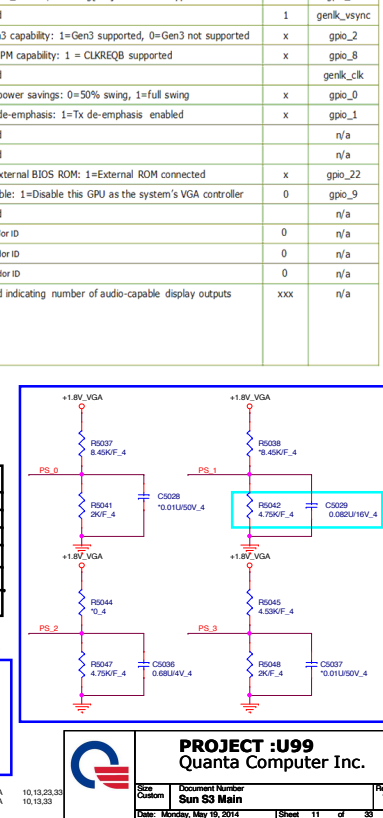
Size Custom	Document Number Sun S3 PCIe Interface	Rev 1A
Date: Monday, May 19, 2014		Sheet 10 of 33

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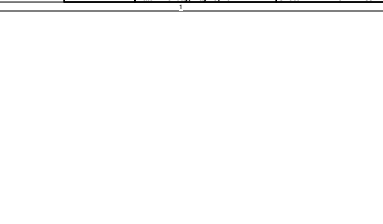
GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT FS
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	1	0	0.975V
1	0	1	1	1	0.950V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

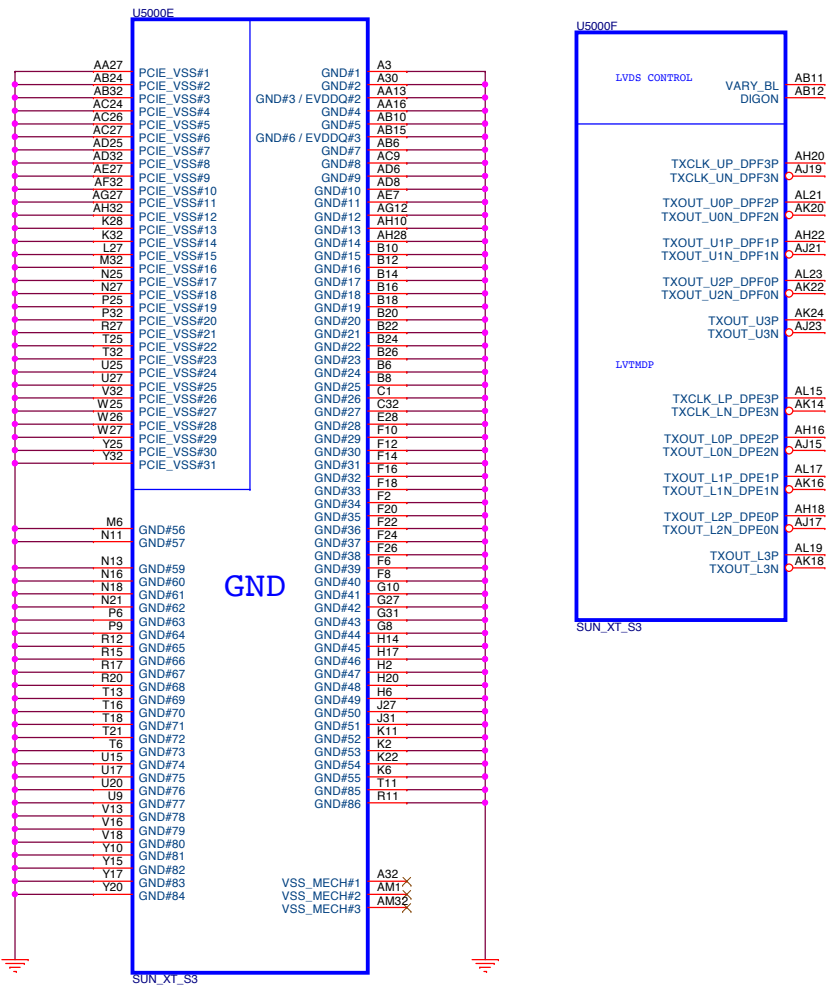


Pin/Bt	Name	Description	Default	Legacy
PS_0[3:1]	romidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidfg[2:0] define memory aperture size If bios_rom_en = 1, romidfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwrsv_erb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_3[0]	aud_port_cp[0]			



PS_3[3:1]	Vendor	Type	Vendor P/N	R5045	R5048
000	Hynix - F(Ruma)	128Mx16 *4, 900Mhz	H57C2G63PFR-11C	NC	4.75K
001	Micron - V89C/R	128Mx16 *4, 900Mhz	MT41J128M16JF-093G:K	8.45K	2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4W2G1646B-BC1A	4.53K	2K
011	Hynix - Huma die	256Mx16 *4, 900Mhz	H57C4G63FAFR-11C	6.98K	4.99K
100	Samsung- E die	256Mx16 *4, 900Mhz	K4W4G1646B-BC1A	4.53K	4.99K
101	Micron - E	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K	5.62K





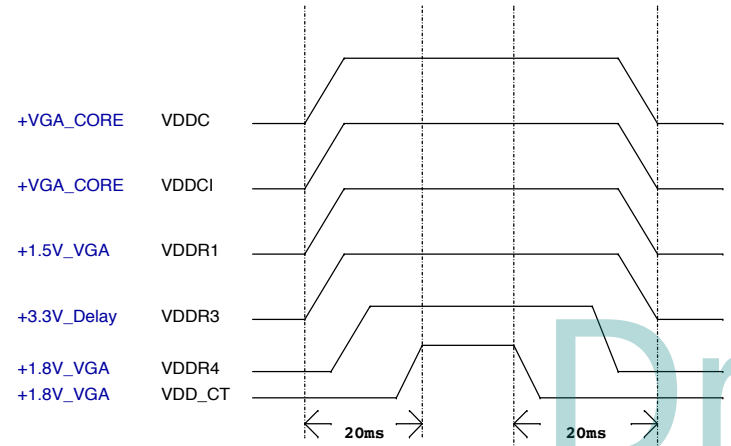
CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	RESERVED	X
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

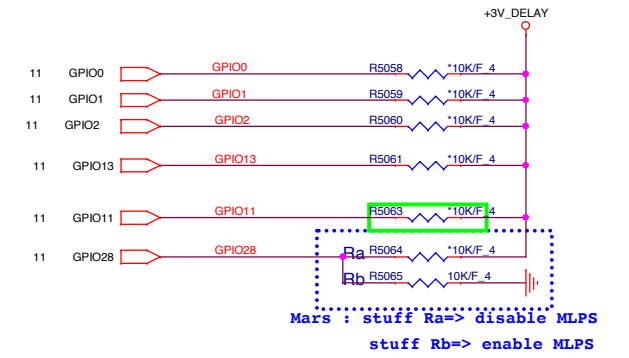
Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

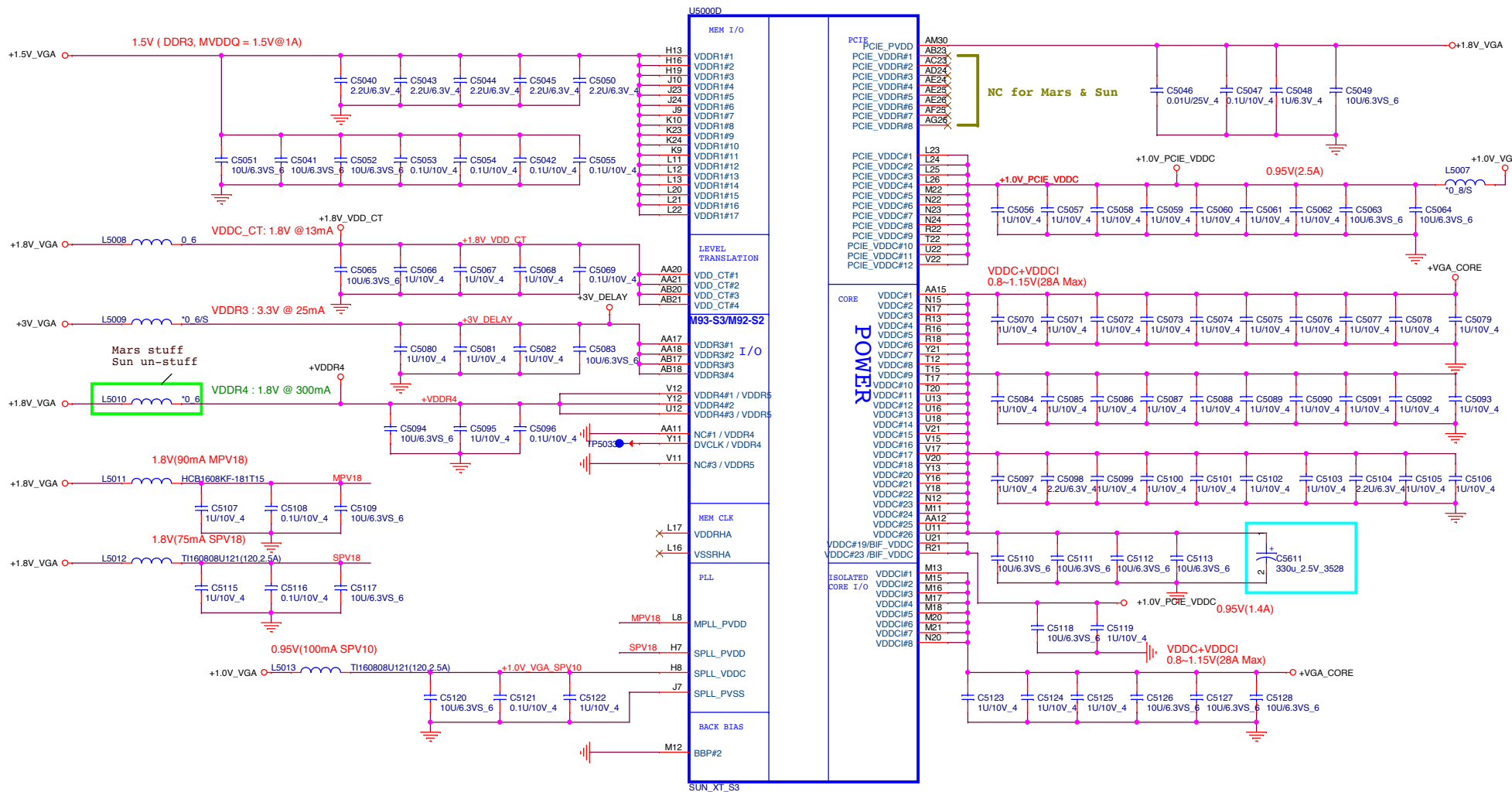
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



Mars : stuff Ra=> disable MLPS
stuff Rb=> enable MLPS

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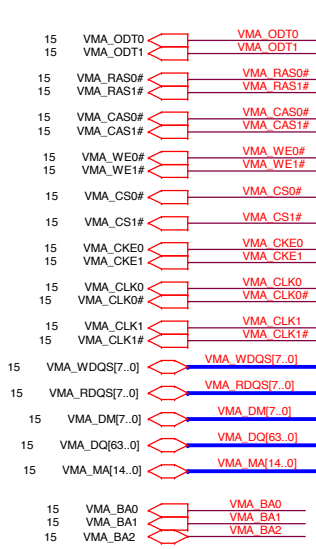
Size Custom Document Number Sun S3 GND / LVDS/ Straps Rev 1A
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+1.5V_VGA	14,15,33
+1.8V_VGA	10,11,23,33
+1.0V_VGA	10,11,33
+VGA_CORE	32,33
+3V	3,4,5,6,8,9,10,16,17,18,19,20,21,22,23,24,29,31,32,33
+5V	17,18,21,22,31

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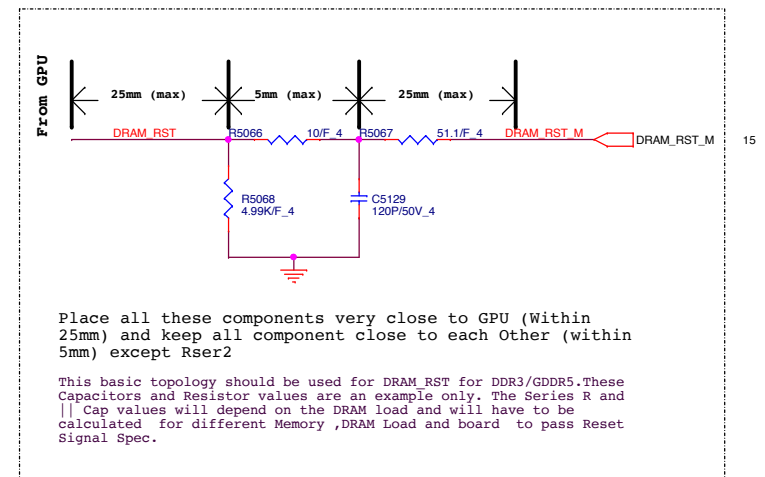
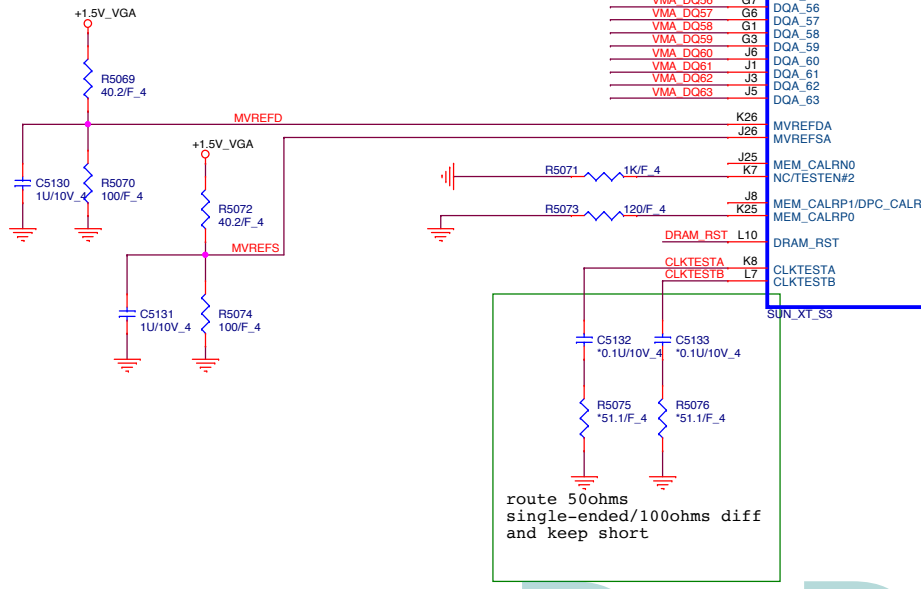
Size Custom	Document Number SUN S3 Power_and_NC	Rev 1A
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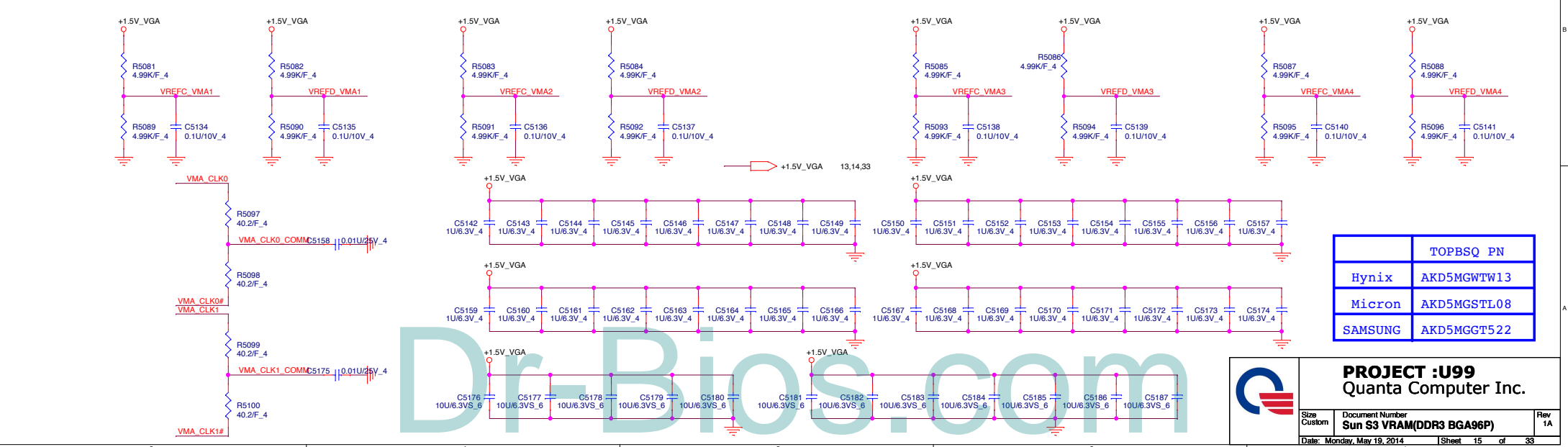
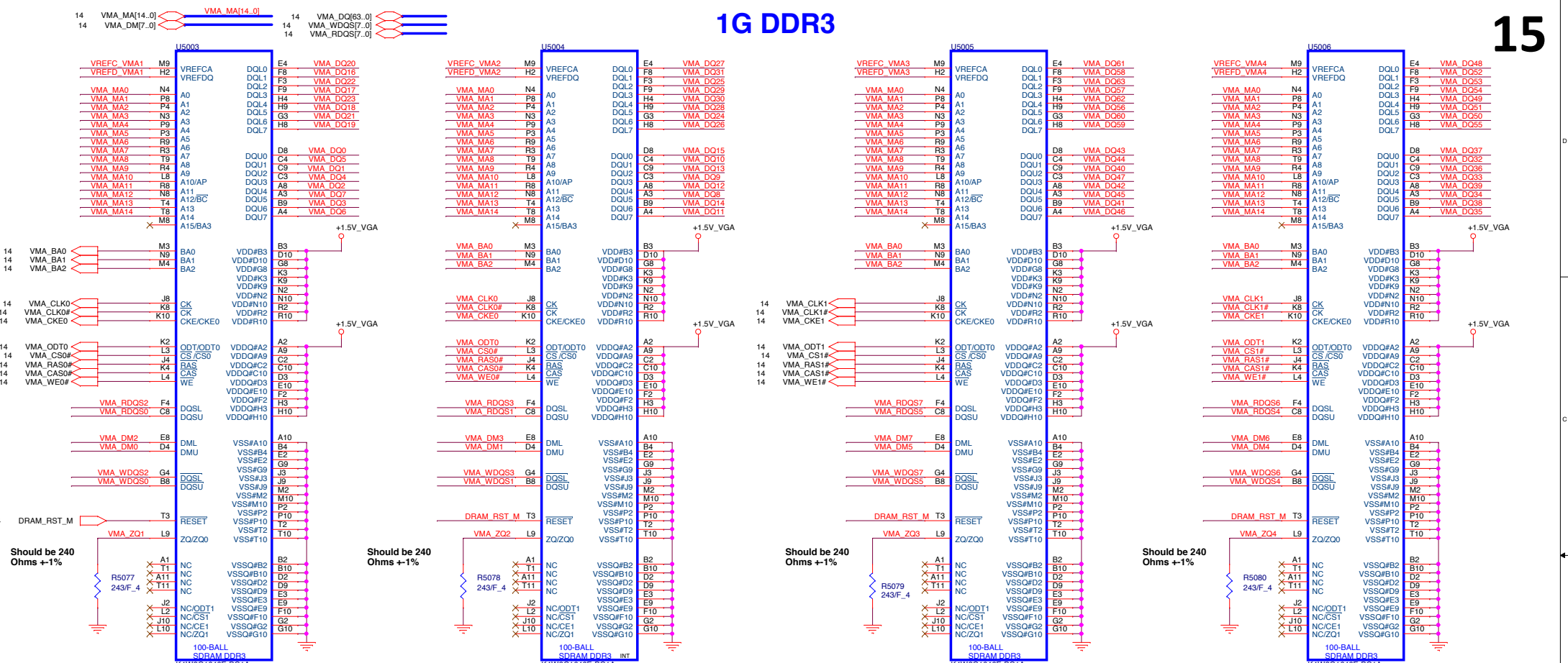
support 1Gbit
VRAM (64M x 16)

U5000C		MEMORY INTERFACE	
VMA_DQ0	K27	DOA_0	
VMA_DQ1	J29	DOA_1	
VMA_DQ2	H30	DOA_2	
VMA_DQ3	H32	DOA_3	
VMA_DQ4	G29	DOA_4	
VMA_DQ5	F28	DOA_5	
VMA_DQ6	F32	DOA_6	
VMA_DQ7	F30	DOA_7	
VMA_DQ8	C30	DOA_8	
VMA_DQ9	F27	DOA_9	
VMA_DQ10	A28	DOA_10	
VMA_DQ11	C28	DOA_11	
VMA_DQ12	E27	DOA_12	
VMA_DQ13	G26	DOA_13	
VMA_DQ14	D26	DOA_14	
VMA_DQ15	F25	DOA_15	
VMA_DQ16	A25	DOA_16	
VMA_DQ17	C25	DOA_17	
VMA_DQ18	E25	DOA_18	
VMA_DQ19	D24	DOA_19	
VMA_DQ20	E23	DOA_20	
VMA_DQ21	F23	DOA_21	
VMA_DQ22	D22	DOA_22	
VMA_DQ23	F21	DOA_23	
VMA_DQ24	E21	DOA_24	
VMA_DQ25	D20	DOA_25	
VMA_DQ26	F19	DOA_26	
VMA_DQ27	A19	DOA_27	
VMA_DQ28	D18	DOA_28	
VMA_DQ29	F17	DOA_29	
VMA_DQ30	A17	DOA_30	
VMA_DQ31	C17	DOA_31	
VMA_DQ32	E17	DOA_32	
VMA_DQ33	D16	DOA_33	
VMA_DQ34	F15	DOA_34	
VMA_DQ35	A15	DOA_35	
VMA_DQ36	D14	DOA_36	
VMA_DQ37	F13	DOA_37	
VMA_DQ38	A13	DOA_38	
VMA_DQ39	C13	DOA_39	
VMA_DQ40	E11	DOA_40	
VMA_DQ41	A11	DOA_41	
VMA_DQ42	C11	DOA_42	
VMA_DQ43	F11	DOA_43	
VMA_DQ44	A9	DOA_44	
VMA_DQ45	C9	DOA_45	
VMA_DQ46	F9	DOA_46	
VMA_DQ47	D8	DOA_47	
VMA_DQ48	E7	DOA_48	
VMA_DQ49	A7	DOA_49	
VMA_DQ50	C7	DOA_50	
VMA_DQ51	F7	DOA_51	
VMA_DQ52	A5	DOA_52	
VMA_DQ53	C5	DOA_53	
VMA_DQ54	E5	DOA_54	
VMA_DQ55	A1	DOA_55	
VMA_DQ56	G7	DOA_56	
VMA_DQ57	G6	DOA_57	
VMA_DQ58	G1	DOA_58	
VMA_DQ59	G3	DOA_59	
VMA_DQ60	J6	DOA_60	
VMA_DQ61	J1	DOA_61	
VMA_DQ62	J3	DOA_62	
VMA_DQ63	J5	DOA_63	
MVREFDA	K26	MEM_CALRNO	K7
MVREFSA	J26	NCTESTEN#2	K7
MEM_CALRP0	J8	MEM_CALRP1/DPC_CALR	K25
MEM_CALRP0	K25	DRAM_RST	L10
CLKTESTA	K8	CLKTESTA	L7
CLKTESTB	L7	CLKTESTB	L7

MAA_0	K17	VMA_MA0	
MAA_1	J20	VMA_MA1	
MAA_2	H23	VMA_MA2	
MAA_3	G23	VMA_MA3	
MAA_4	G24	VMA_MA4	
MAA_5	H24	VMA_MA5	
MAA_6	J19	VMA_MA6	
MAA_7	K19	VMA_MA7	
MAA_8	J14	VMA_MA8	
MAA_9	K14	VMA_MA9	
MAA_10	J11	VMA_MA10	
MAA_11	J13	VMA_MA11	
MAA_12	H11	VMA_MA12	
MAA_13/BA2	G11	VMA_BA2	
MAA_14/BA0	J16	VMA_BA0	
MAA_15/BA1	L15	VMA_BA1	
DQMA_0	E32	VMA_DM0	
DQMA_1	E30	VMA_DM1	
DQMA_2	A21	VMA_DM2	
DQMA_3	C21	VMA_DM3	
DQMA_4	E13	VMA_DM4	
DQMA_5	D12	VMA_DM5	
DQMA_6	E3	VMA_DM6	
DQMA_7	F4	VMA_DM7	
RDQSA_0	H28	VMA_RDQSA0	
RDQSA_1	C27	VMA_RDQSA1	
RDQSA_2	A23	VMA_RDQSA2	
RDQSA_3	E19	VMA_RDQSA3	
RDQSA_4	E15	VMA_RDQSA4	
RDQSA_5	D10	VMA_RDQSA5	
RDQSA_6	D6	VMA_RDQSA6	
RDQSA_7	G5	VMA_RDQSA7	
WDQSA_0	H27	VMA_WDQSA0	
WDQSA_1	A27	VMA_WDQSA1	
WDQSA_2	C23	VMA_WDQSA2	
WDQSA_3	C19	VMA_WDQSA3	
WDQSA_4	C15	VMA_WDQSA4	
WDQSA_5	E9	VMA_WDQSA5	
WDQSA_6	C5	VMA_WDQSA6	
WDQSA_7	H4	VMA_WDQSA7	
ODTA0	L18	VMA_ODT0	
ODTA1	K16	VMA_ODT1	
CLKA0	H26	VMA_CLK0	
CLKA0B	H25	VMA_CLK0#	
CLKA1	G9	VMA_CLK1	
CLKA1B	H9	VMA_CLK1#	
RASA0B	G22	VMA_RAS0#	
RASA1B	G17	VMA_RAS1#	
CASA0B	G19	VMA_CAS0#	
CASA1B	G16	VMA_CAS1#	
CSA0B_0	H22	VMA_CS0#	
CSA0B_1	J22		
CSA1B_0	G13	VMA_CS1#	
CSA1B_1	K13		
CKEA0	K20	VMA_CKE0	
CKEA1	J17	VMA_CKE1	
WEA0B	G25	VMA_WE0#	
WEA1B	H10	VMA_WE1#	
PX_EN	AB16	PX_EN	TP5034
RSVD#2	G14	VMA_MA12	
RSVD#3	G20	VMA_MA13	



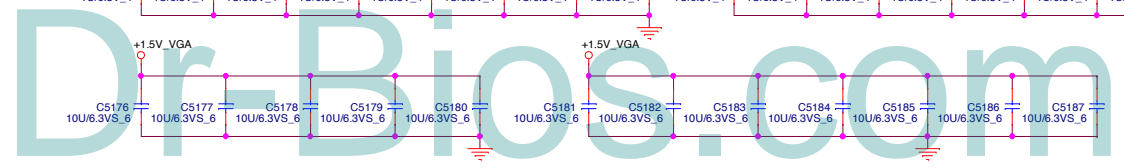
1G DDR3



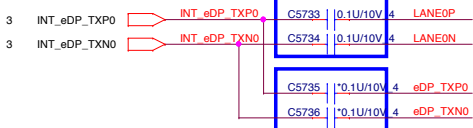
TOPBQ PN
Hynix AKD5MGWTW13
Micron AKD5MGSTL08
SAMSUNG AKD5MGST522

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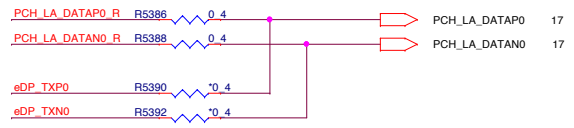


for Bemma LVDS need stuff 0.1u cap ; need change 0.1u on next stage



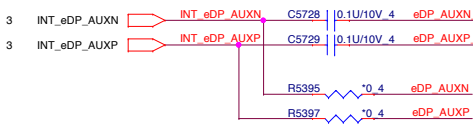
Bemba to LVDS Converter

From LVDS Converter



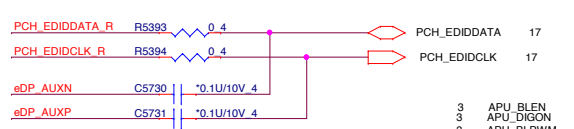
to Bemba eDP

from Bemba eDP



Bemba to LVDS Converter

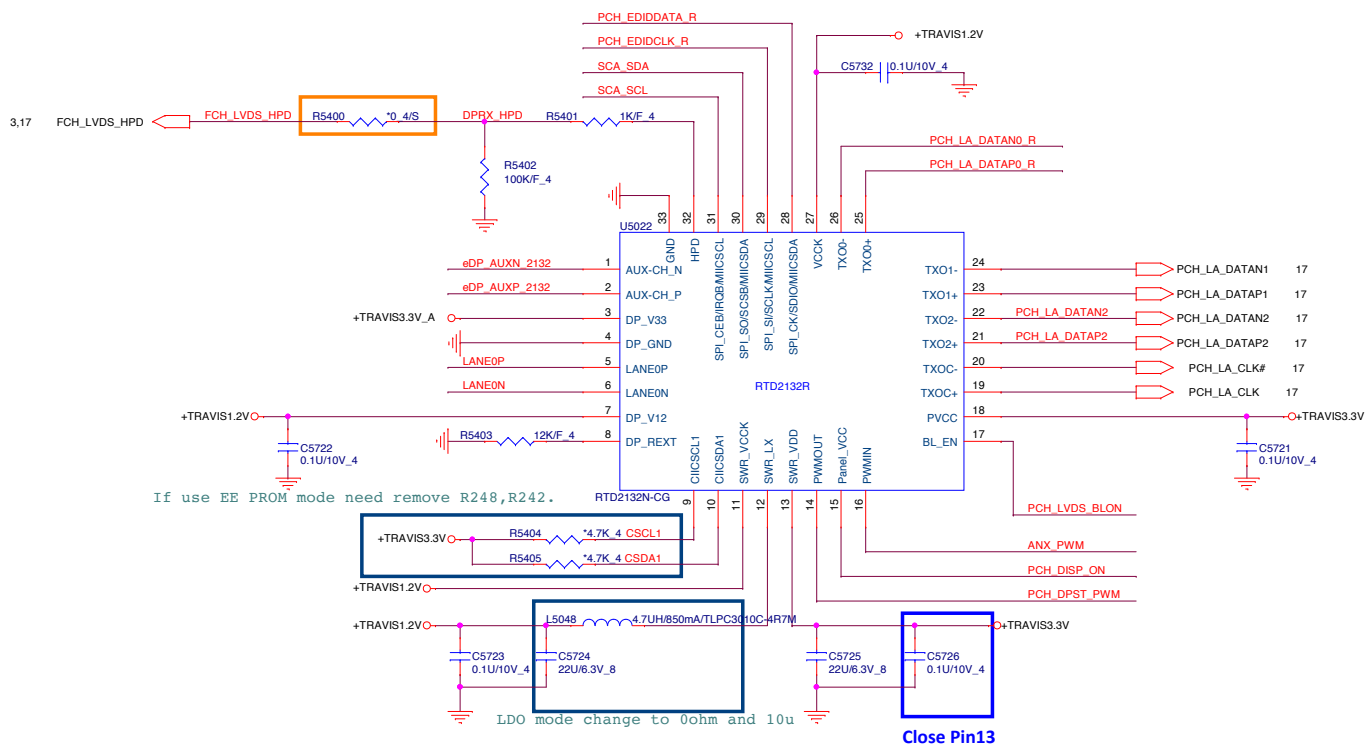
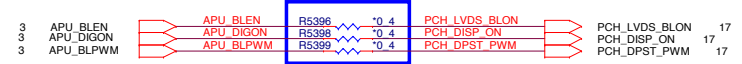
From LVDS Converter



to Bemba eDP

from Bemba eDP

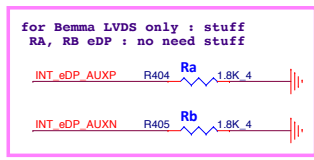
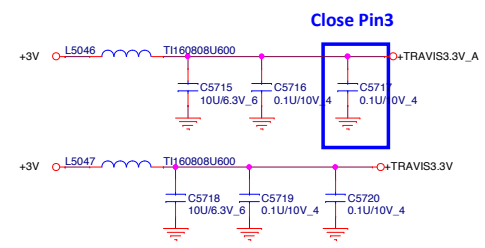
for Bemma eDP : stuff R5396 / R5398 / R5399
for Bemma LVDS : Don't stuff R5396 / R5398 / R5399



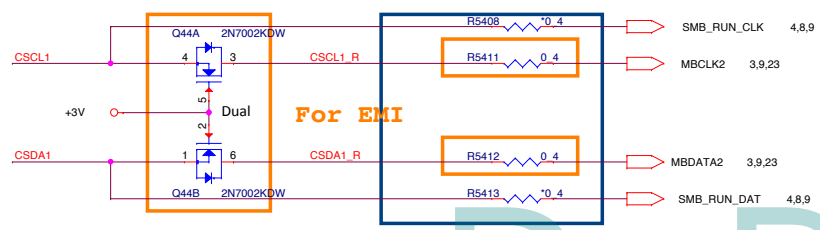
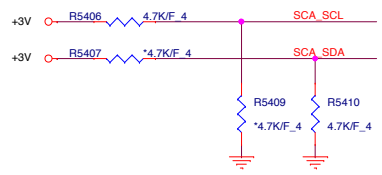
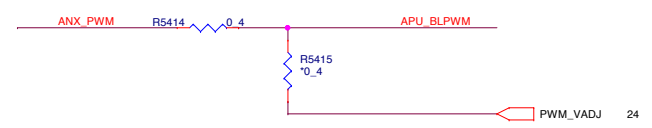
If use EE PROM mode need remove R248,R242.

LDO mode change to 0ohm and 10u

Close Pin13



for Bemma LVDS only : stuff RA, RB eDP : no need stuff



For EMI

EE PROM EC OPTION R5408, R5413 R5411, R5412

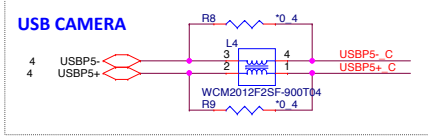
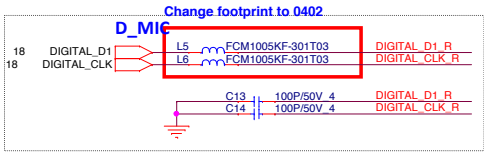
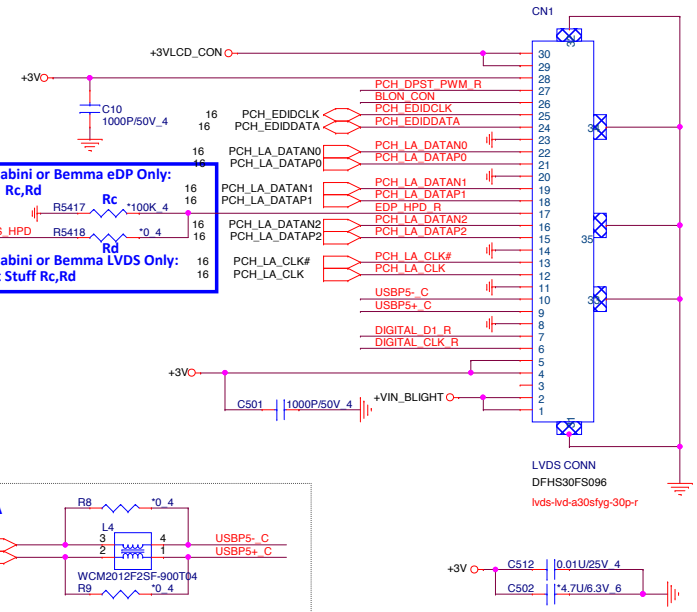
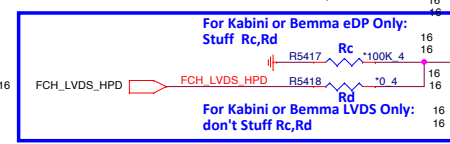
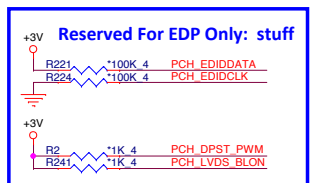
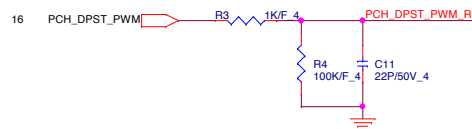
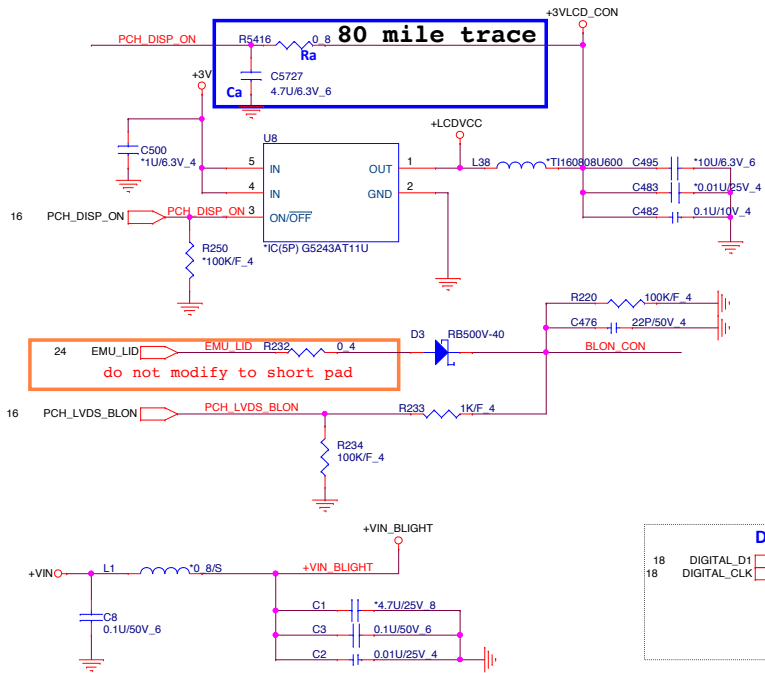
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

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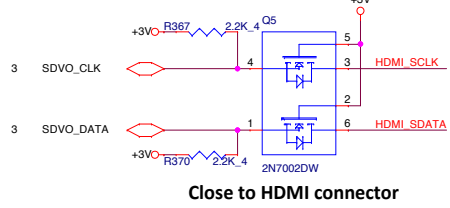
LVDS Conn.

for Bemma eDP : don't stuff Ra / Ca ;
for Bemma LVDS : stuff Ra / Ca



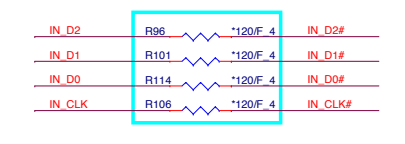
HDMI Conn.

HDMI SMBus Isolation

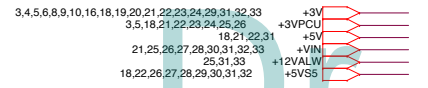
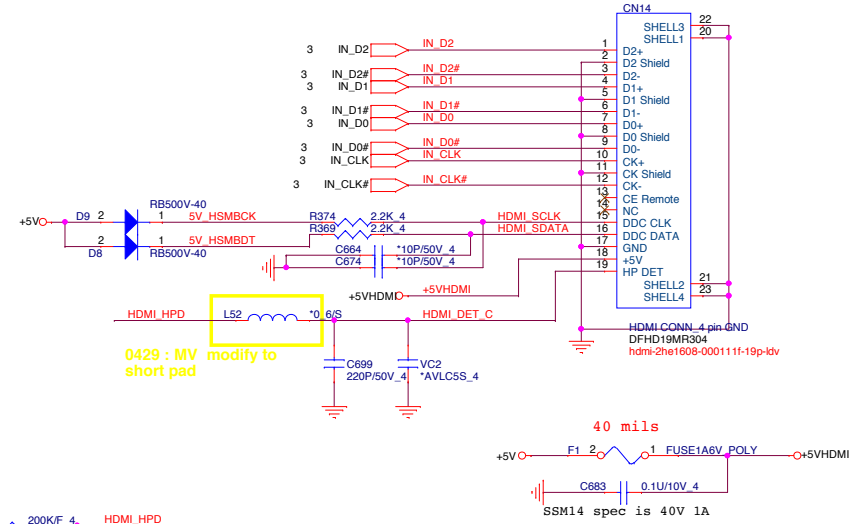
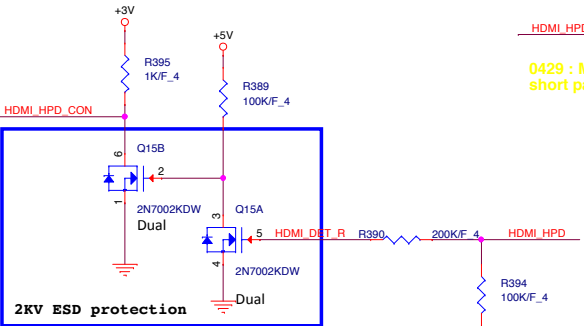


Close to HDMI connector

EMI Solution



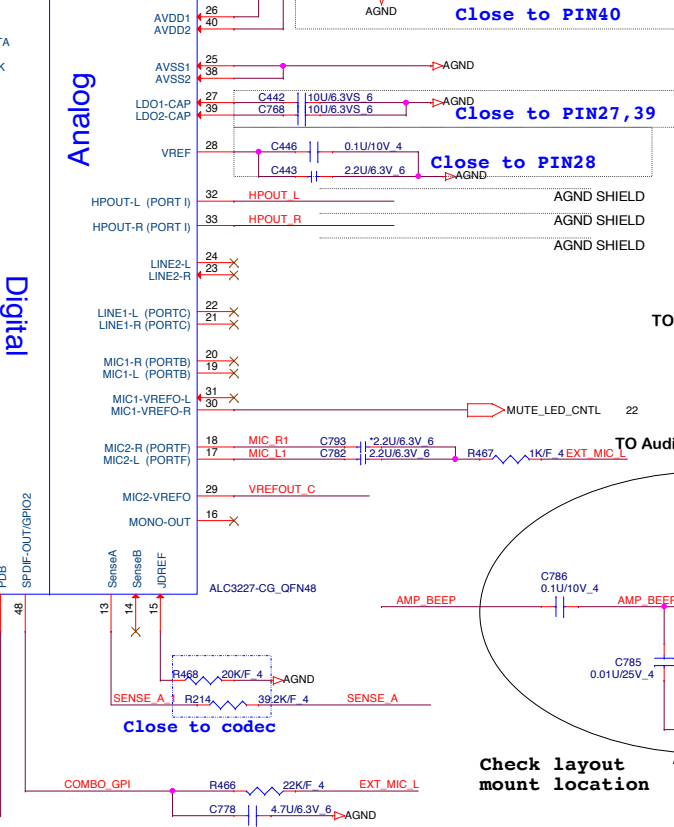
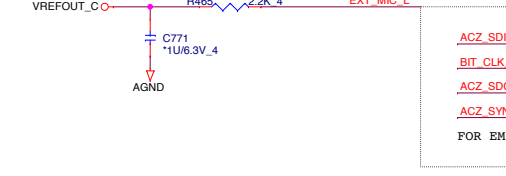
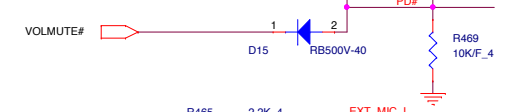
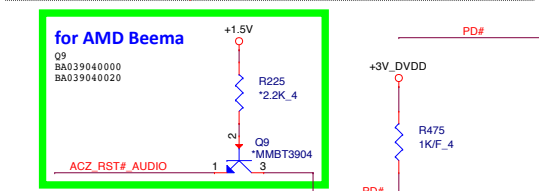
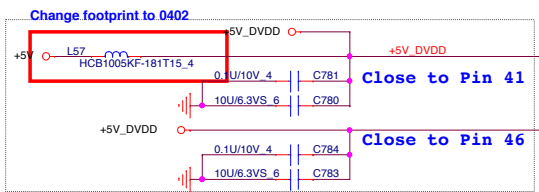
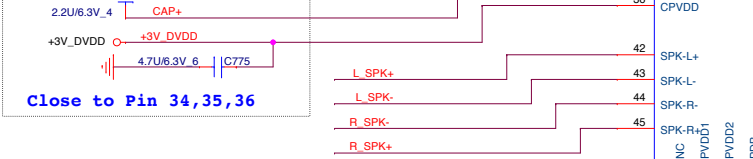
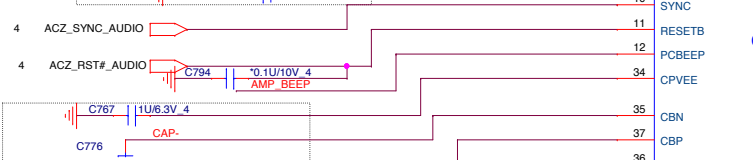
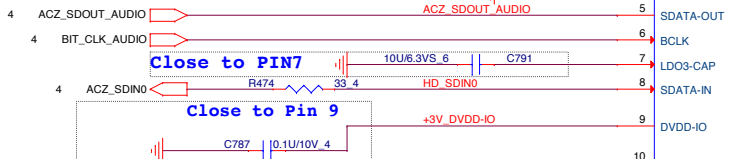
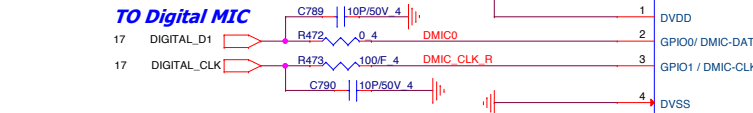
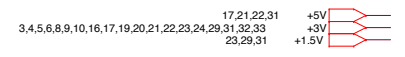
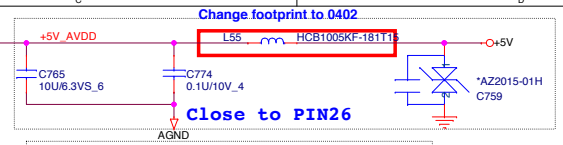
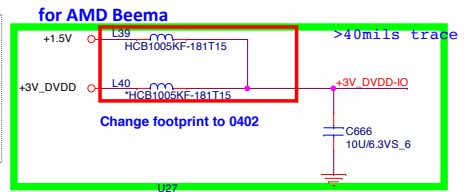
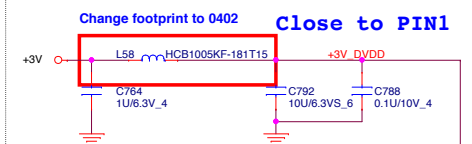
HDMI HPD SENSE



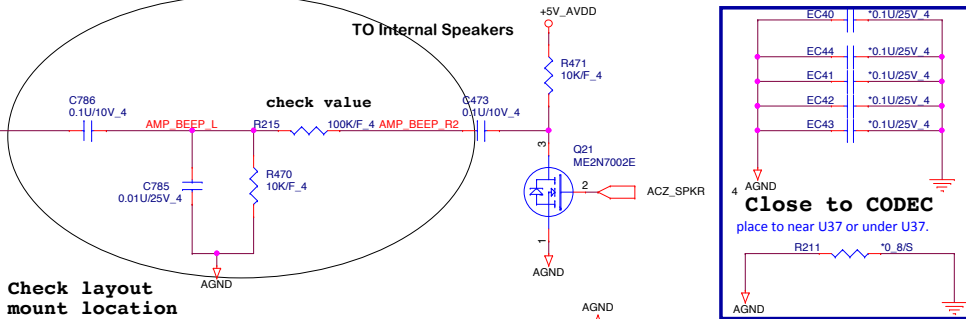
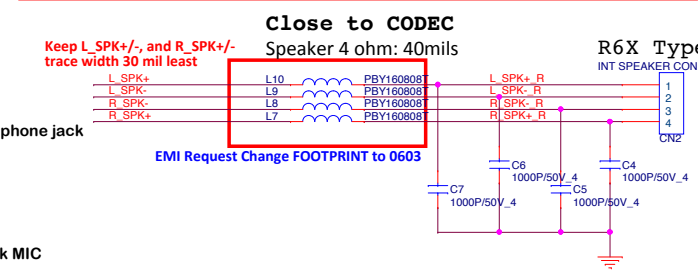
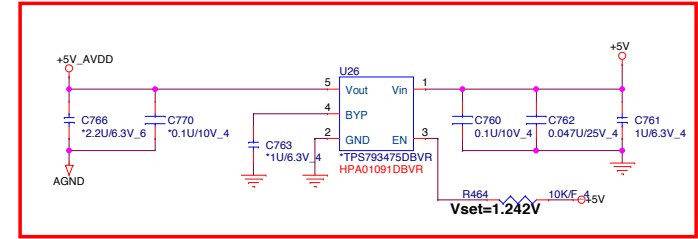
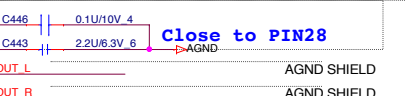
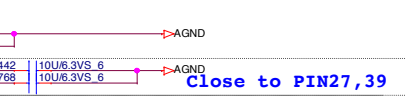
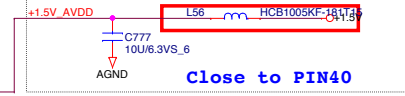
PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number LCD Connector (LVDS)	Rev 3A
Date: Monday, May 19, 2014		
Sheet 17 of 33		

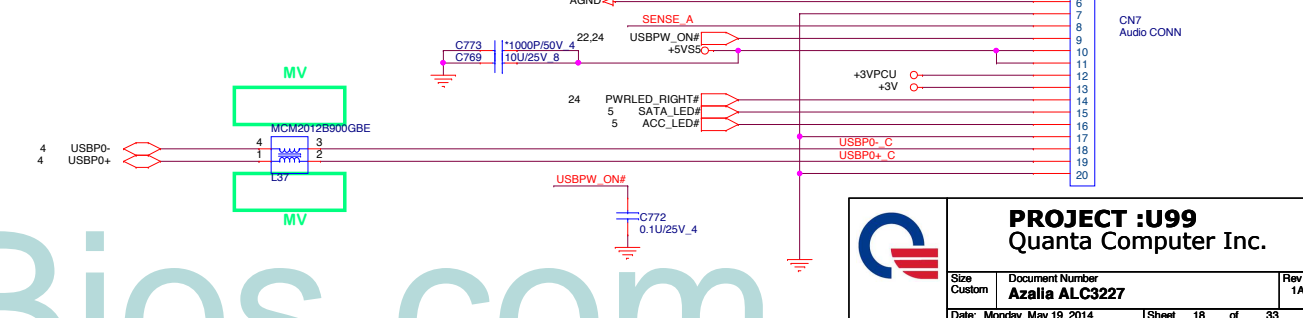
DI-Bios.com



Digital



USB 2.0 AND AUDIO COMBO JACK



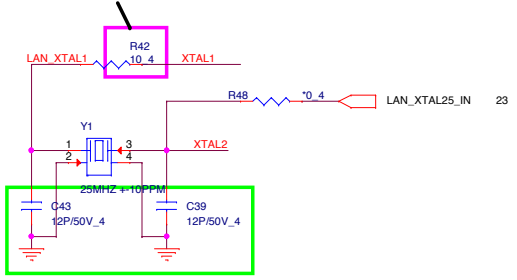
ACZ_SDINO	EC39	*33P/50V_4
BIT_CLK_AUDIO	EC11	*33P/50V_4
ACZ_SDOUT_AUDIO	EC33	*10P/50V_4
ACZ_SYNC_AUDIO	EC12	*10P/50V_4

FOR EMI

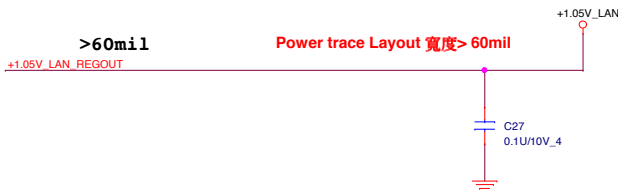
PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number Azalia ALC3227	Rev 1A
Date: Monday, May 19, 2014	Sheet 18 of 33	

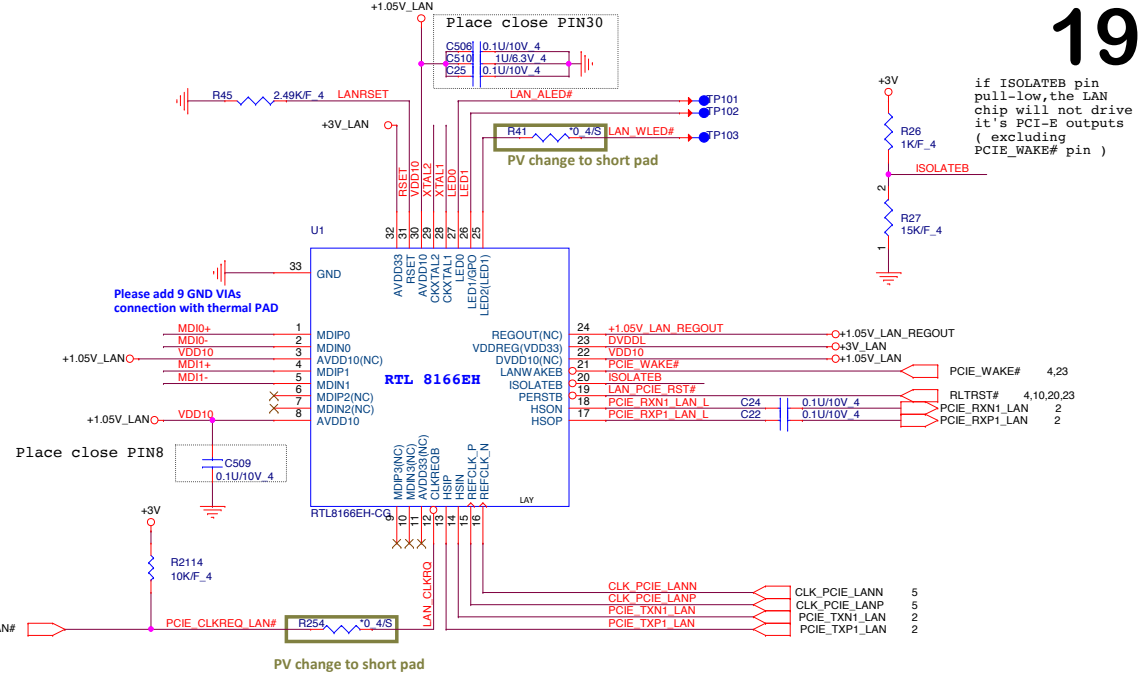
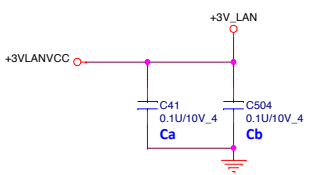
For EMI 0 - 22 ohm



SI change to 12p



Place close PIN23 and PIN32



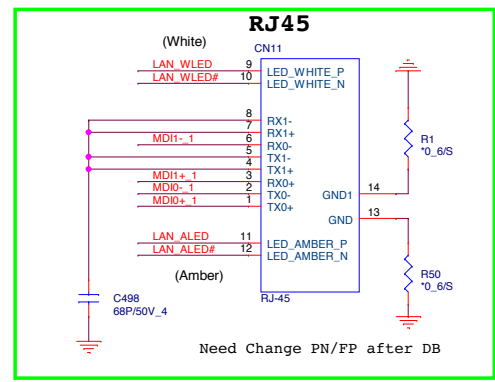
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCI_E_WAKE# pin)

Please add 9 GND VIAS connection with thermal PAD

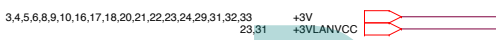
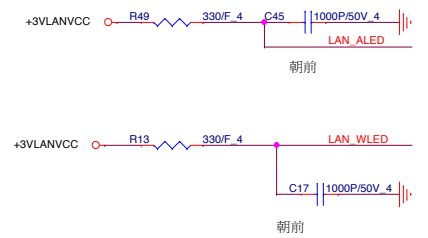
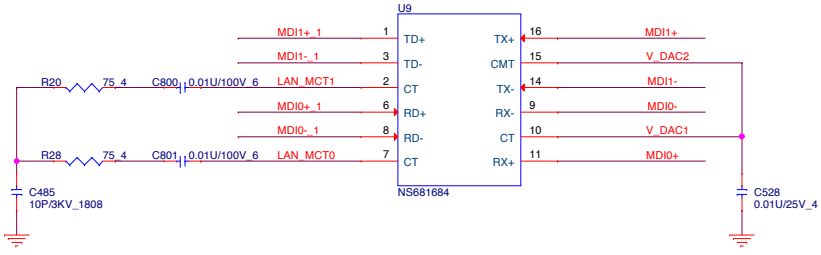
Place close PIN8

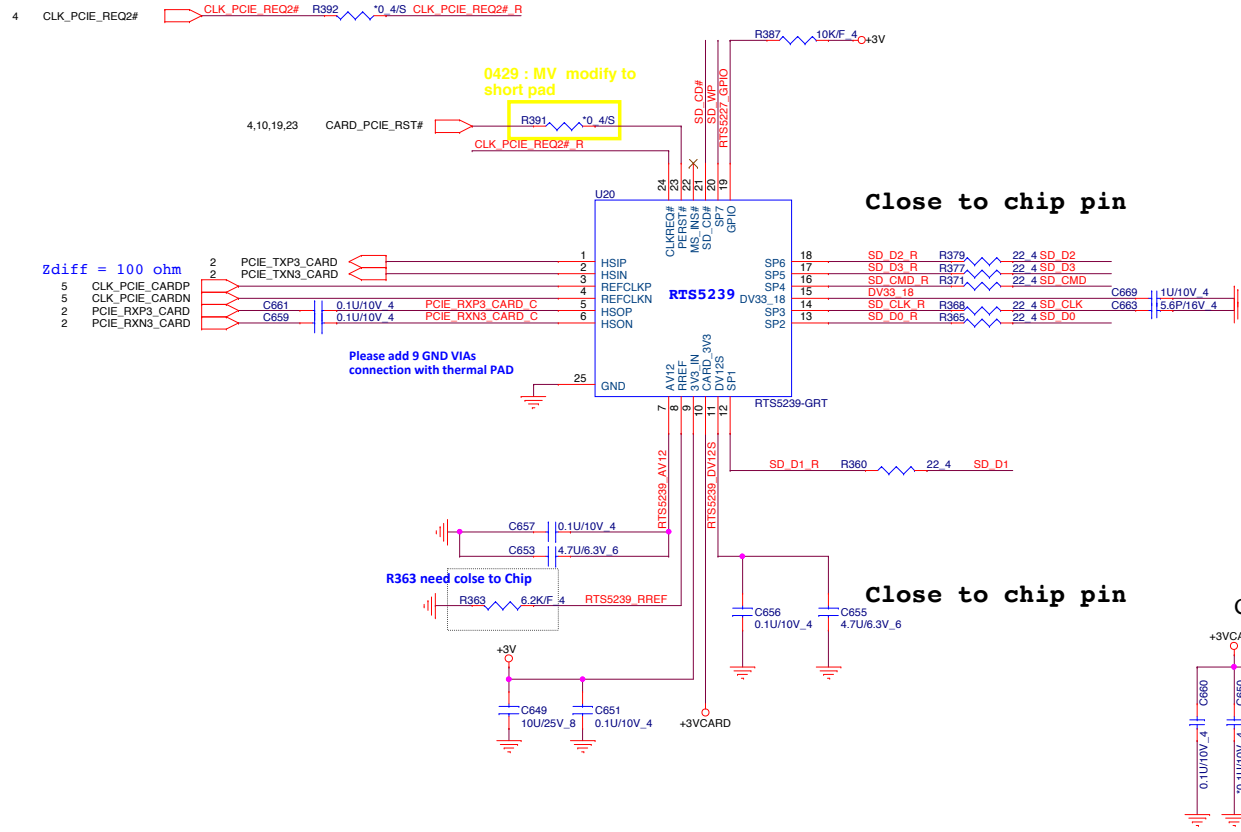
PV change to short pad

LAN conn



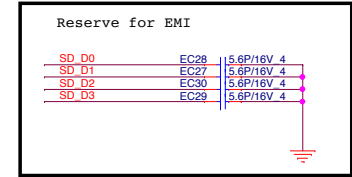
Need Change PN/FP after DB



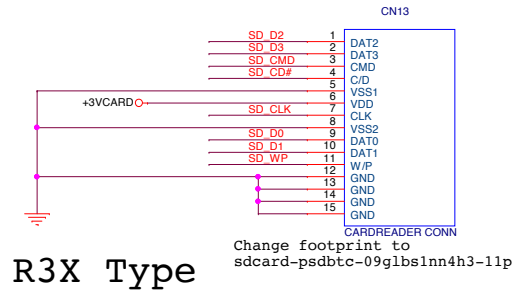


SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin



SD / MMC CARD READER

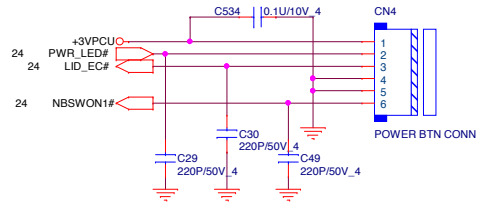


R3X Type

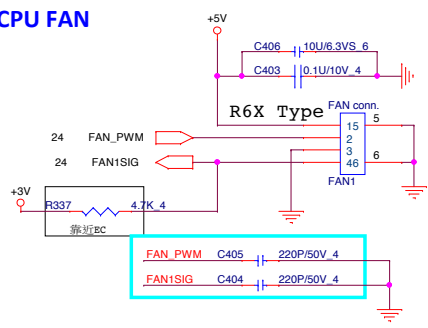
Change footprint to sdcard-psbttc-09glbs1nn4h3-11p

Power Button Connector

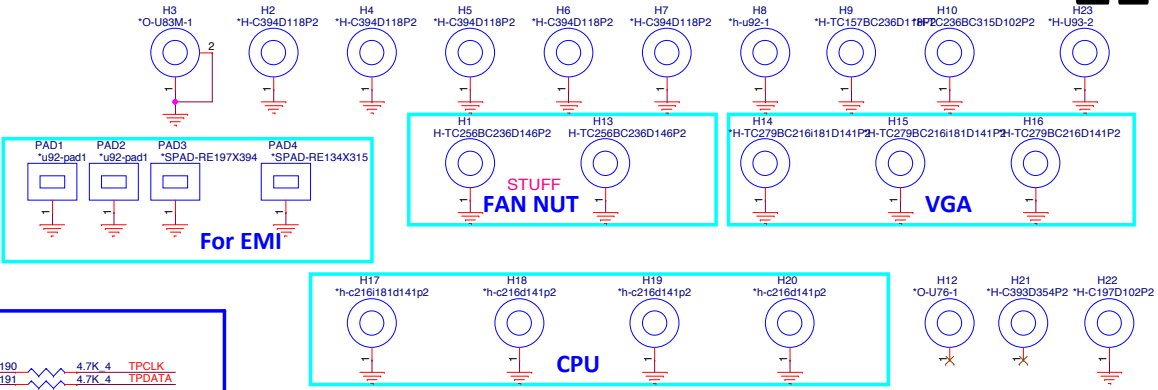
Pin1 : +3VPCU(LIDSWITCH PWR)
 Pin2 : POWER LED
 Pin3 : LIDSWITCH
 Pin4 : GND
 Pin5 : GND
 Pin6 : POWERON#



CPU FAN

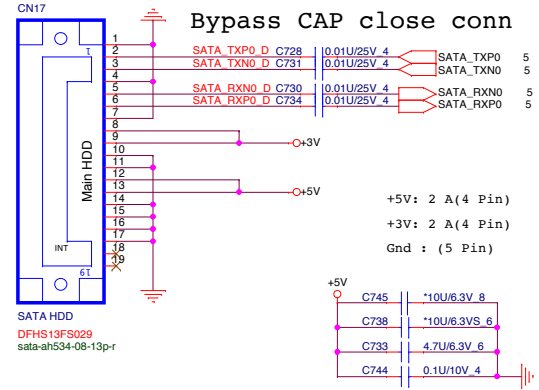


Hole

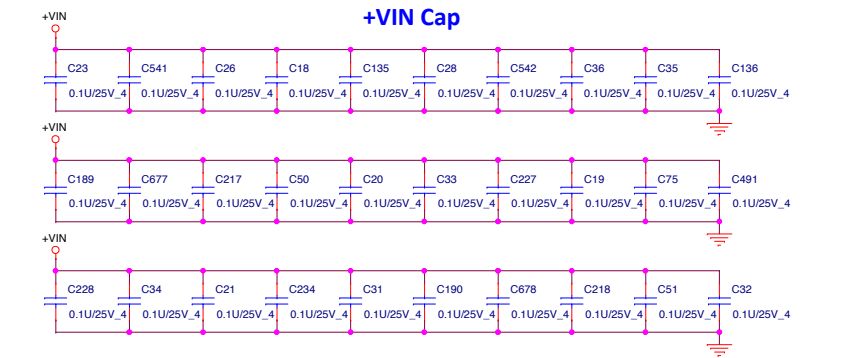
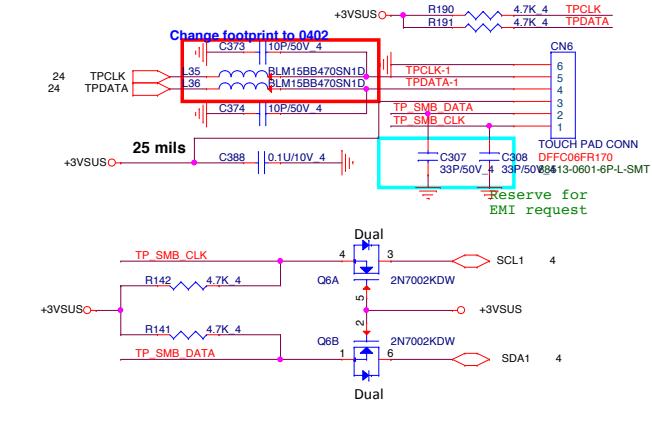


SATA HDD Connector(Cable type)

Bypass CAP close conn

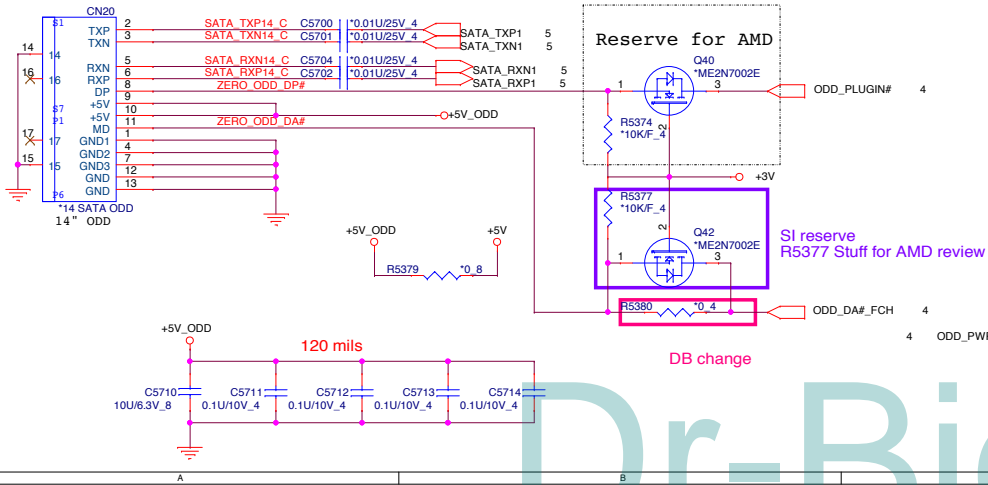


Touch Pad



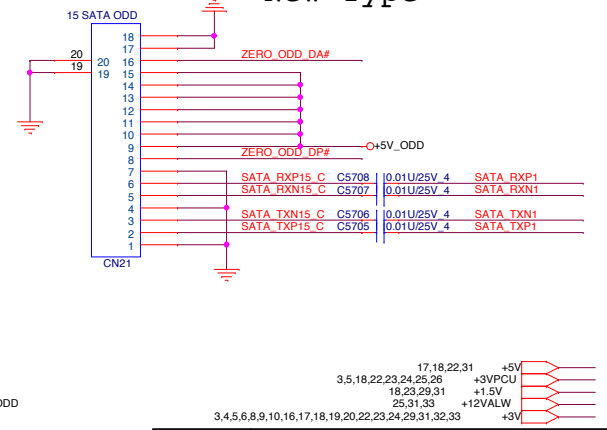
SATA ODD CONNECTOR

14" SATA ODD Bypass CAP close conn



15" SATA ODD

New Type

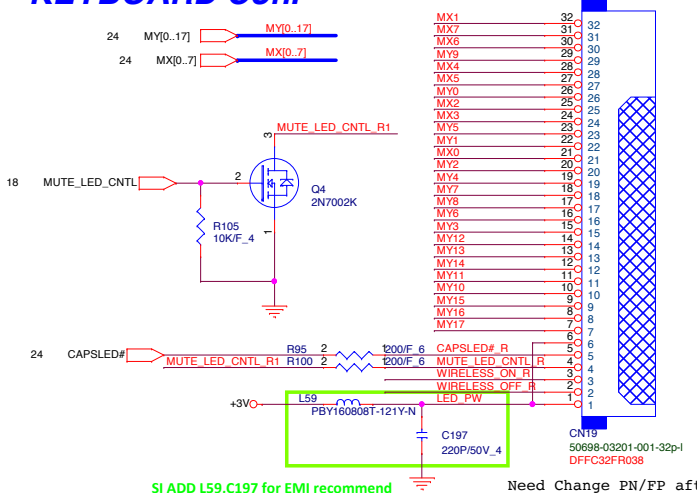


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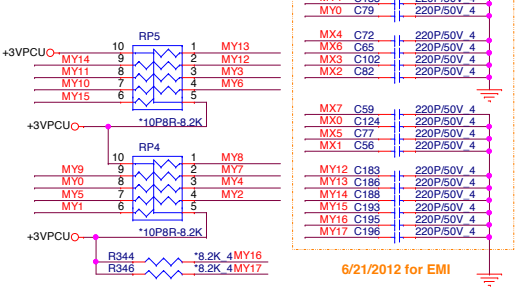
PROJECT :U99
 Quanta Computer Inc.

Size Custom	Document Number SATA HDD/ODD/MSATA CONN	Rev 1A
Date: Monday, May 19, 2014	Sheet 21 of	33

KEYBOARD Con.

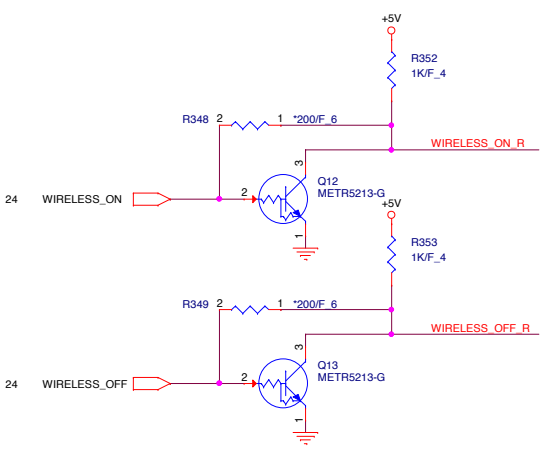


KEYBOARD PULL-UP



MY5	C106	220P/50V_4
MY6	C157	220P/50V_4
MY3	C179	220P/50V_4
MY7	C143	220P/50V_4
MY8	C153	220P/50V_4
MY9	C69	220P/50V_4
MY10	C192	220P/50V_4
MY11	C191	220P/50V_4
MY1	C119	220P/50V_4
MY2	C130	220P/50V_4
MY4	C133	220P/50V_4
MY0	C79	220P/50V_4
MX4	C72	220P/50V_4
MX6	C65	220P/50V_4
MX3	C102	220P/50V_4
MX2	C82	220P/50V_4
MX7	C59	220P/50V_4
MX0	C124	220P/50V_4
MX5	C77	220P/50V_4
MX1	C56	220P/50V_4
MY12	C183	220P/50V_4
MY13	C186	220P/50V_4
MY14	C188	220P/50V_4
MY15	C193	220P/50V_4
MY16	C195	220P/50V_4
MY17	C196	220P/50V_4

6/21/2012 for EMI

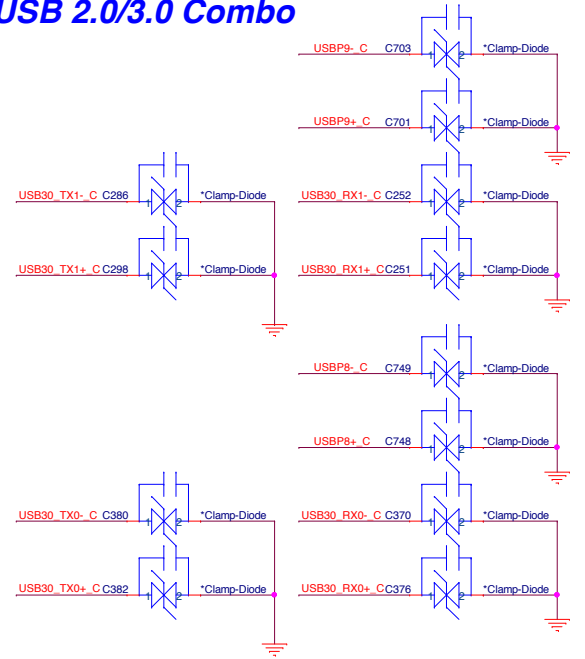


SI ADD L59,C197 for EMI recommend

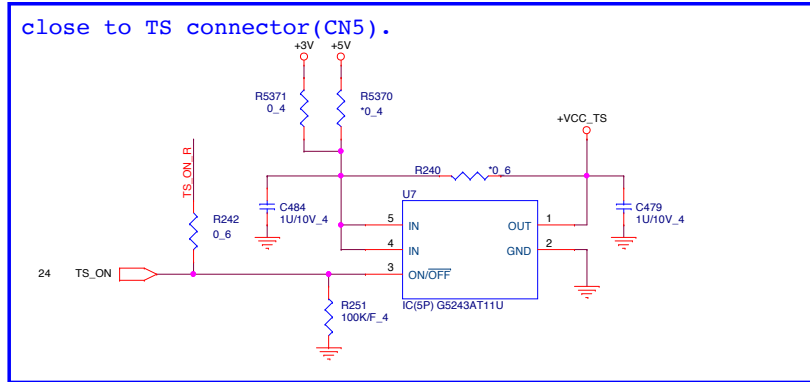
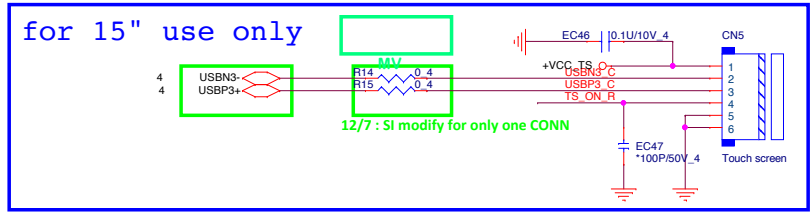
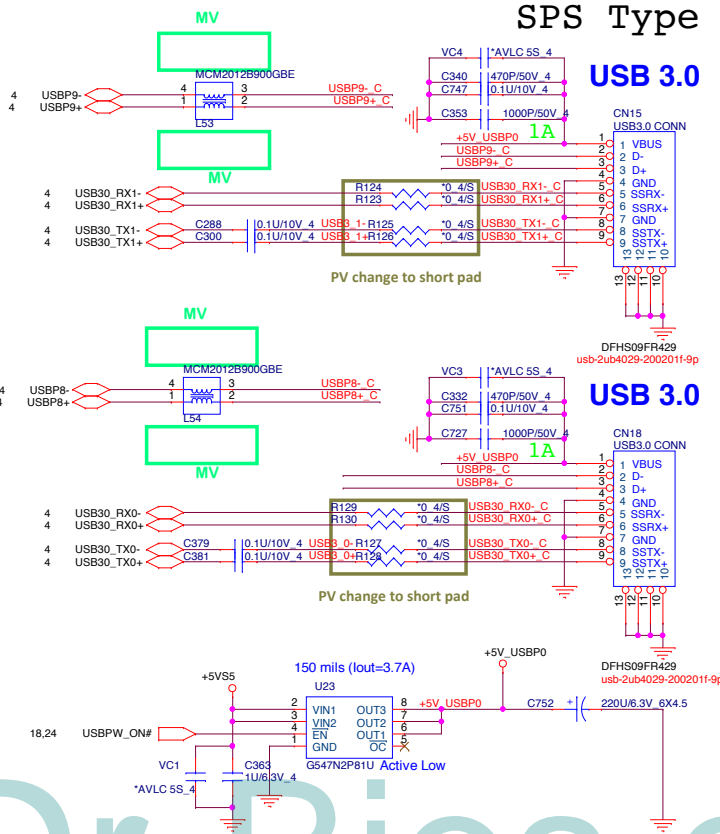
Need Change PN/FP after DB

NM9 Type

USB 2.0/3.0 Combo



SPS Type



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PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	USB 3.0/KB/Green CLK	
Date: Monday, May 19, 2014	Sheet 22of	33

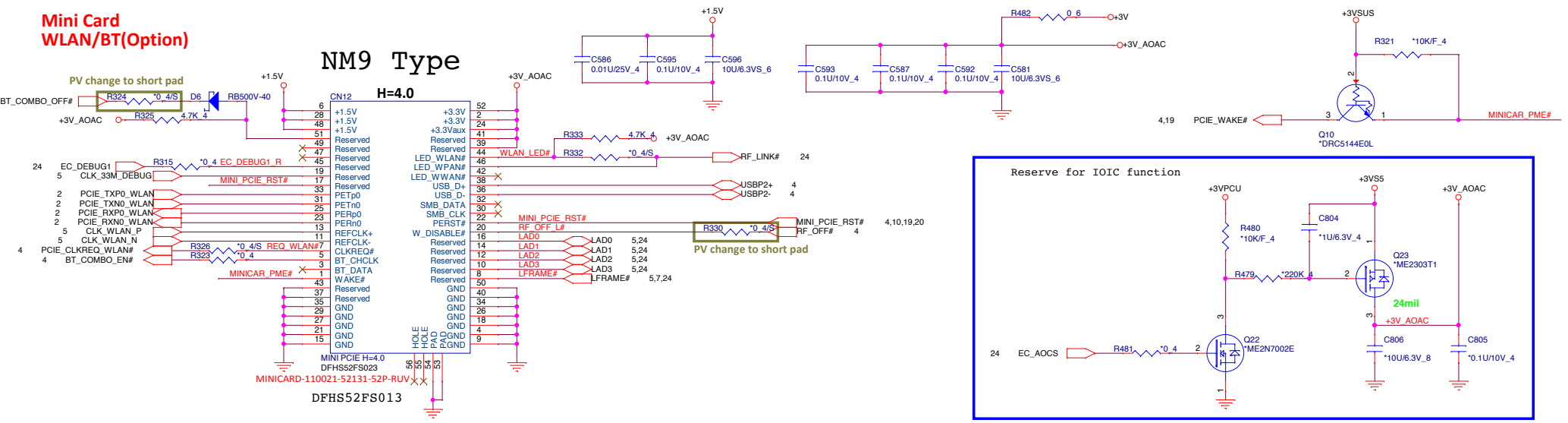
18.26.27.28.29.30.31.32
3.5,18.21,23,24,25,26

+5VS5

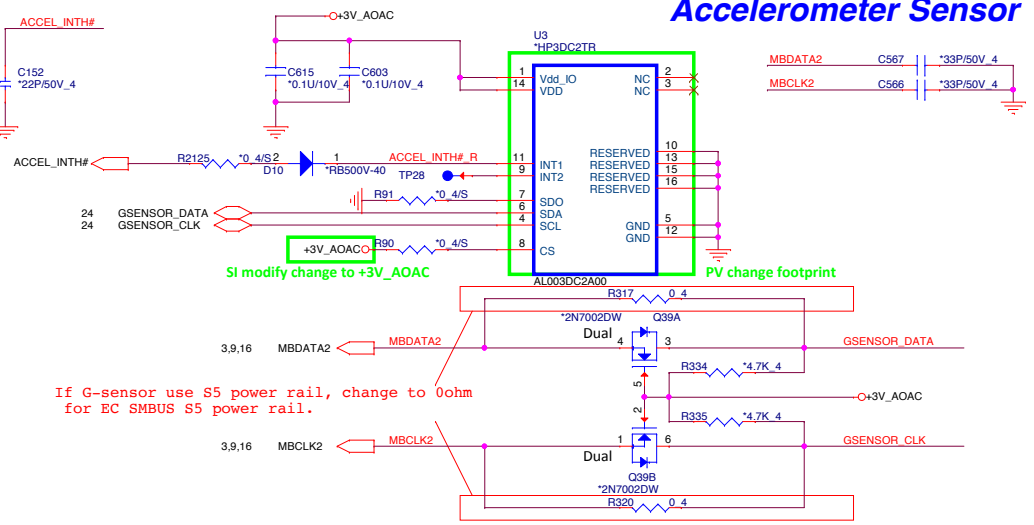
+3VPCU

Mini Card WLAN/BT(Optional)

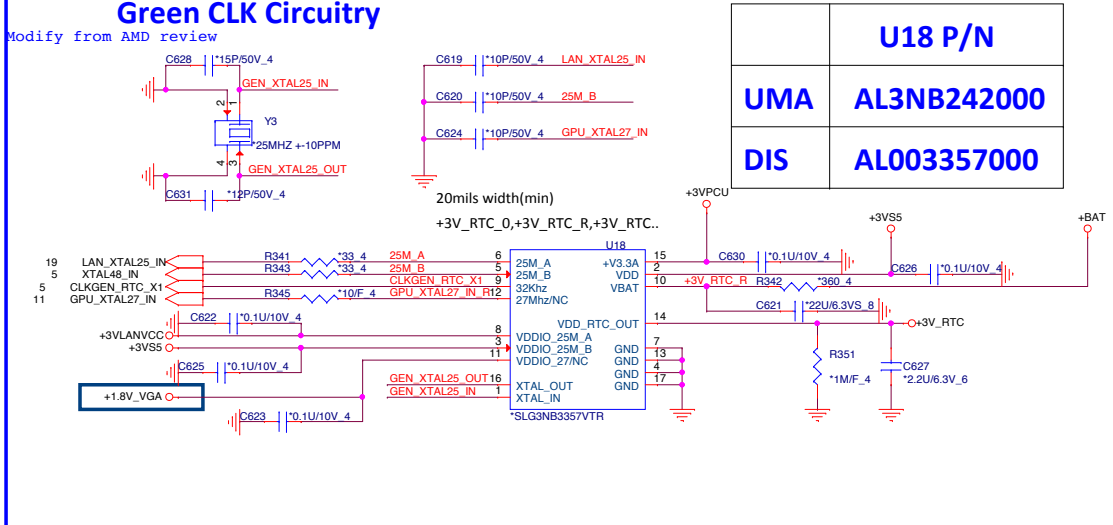
NM9 Type



Accelerometer Sensor

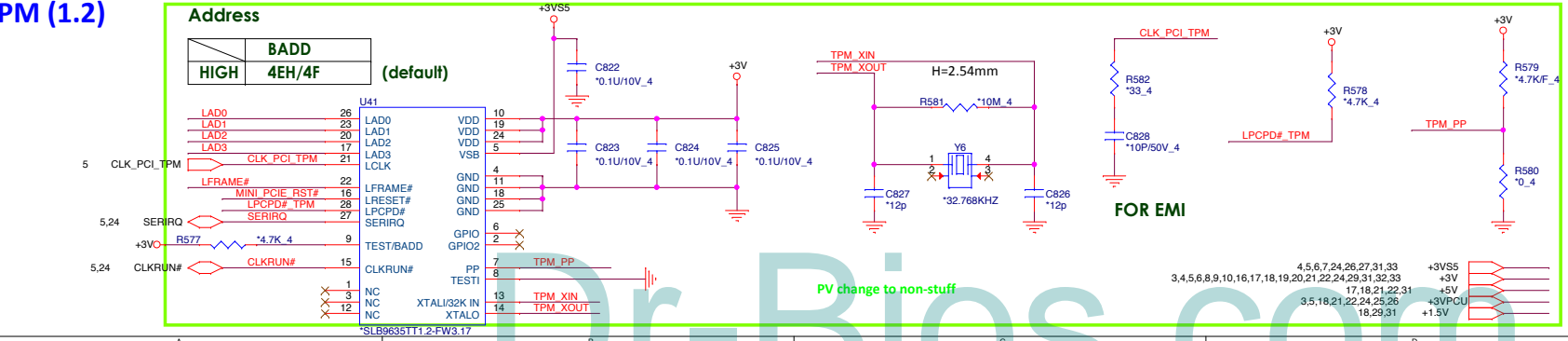


Green CLK Circuitry



U18 P/N	
UMA	AL3NB242000
DIS	AL003357000

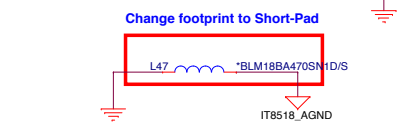
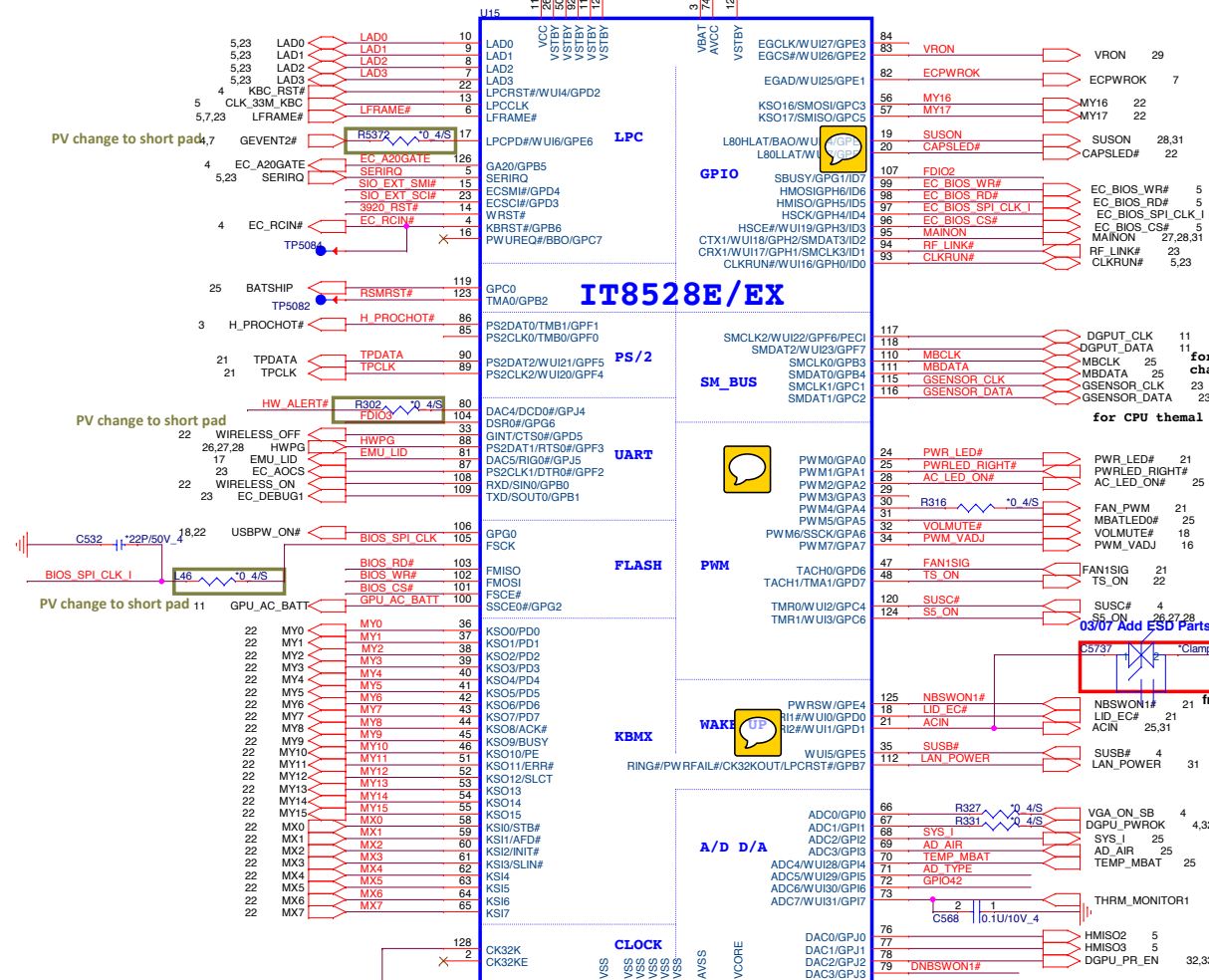
TPM (1.2)



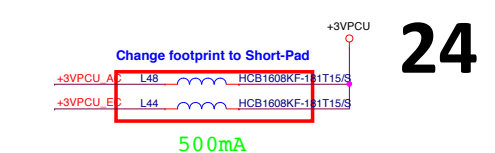
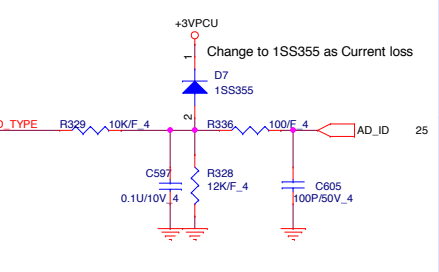
PROJECT :U99 Quanta Computer Inc.			
Size Custom	Document Number MINI-PCIE/LED	Rev 1A	
Date: Monday, May 19, 2014	Sheet 23of	33	

3,4,5,6,8,9,10,16,17,18,19,20,21,22,23,29,31,32,33
3,5,18,21,22,23,25,26

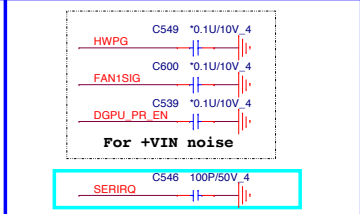
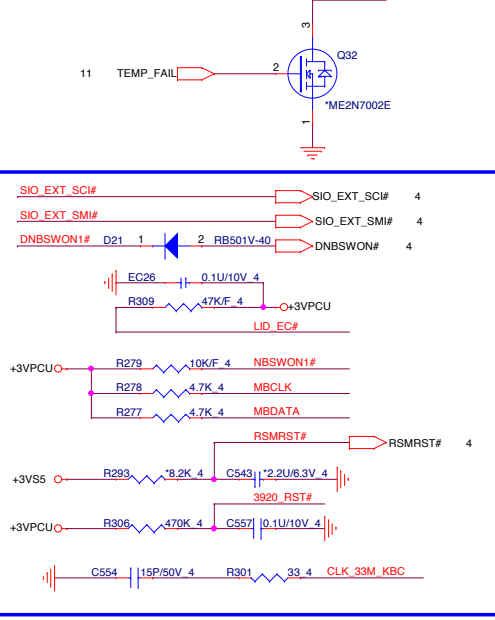
ITE pin 100, 104, 106 default can not pull up to +3VPCU it will cause chip into test mode



Smart adapter Type check

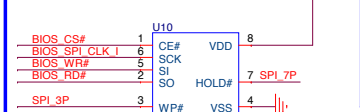


DGPU Thermal protect

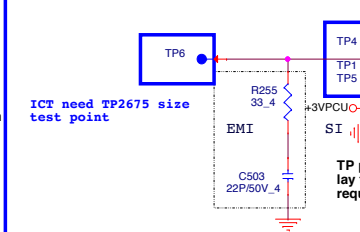


Vender	Size	P/N
AIT	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WND	4M	AKE39FN0N01
Socket		DFHS08FS023

4M SPI EC ROM



128K byte SPI EC ROM



Adapter select

Hi ==> A6-5200 25W CPU + DIS
Low ==>UMA/DIS/SG

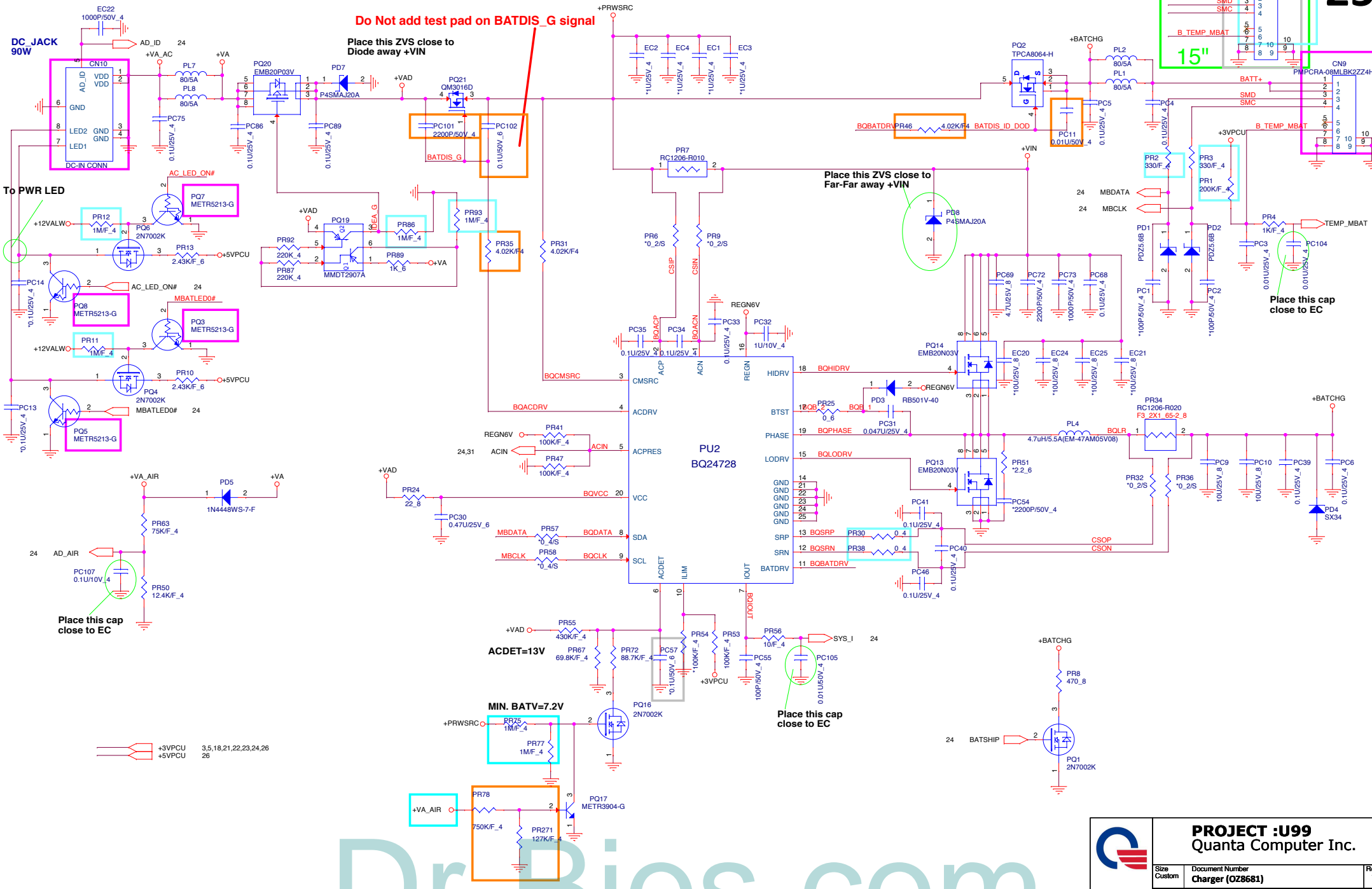
Platform model	GPIO42	adapter
A6 25W CPU + DIS	High	90W
DIS/SG/UMA	Low	65W


PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number EC (IT8528E)/ROM	Rev 1A
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Date: Monday, May 19, 2014 | Sheet 24 of 33

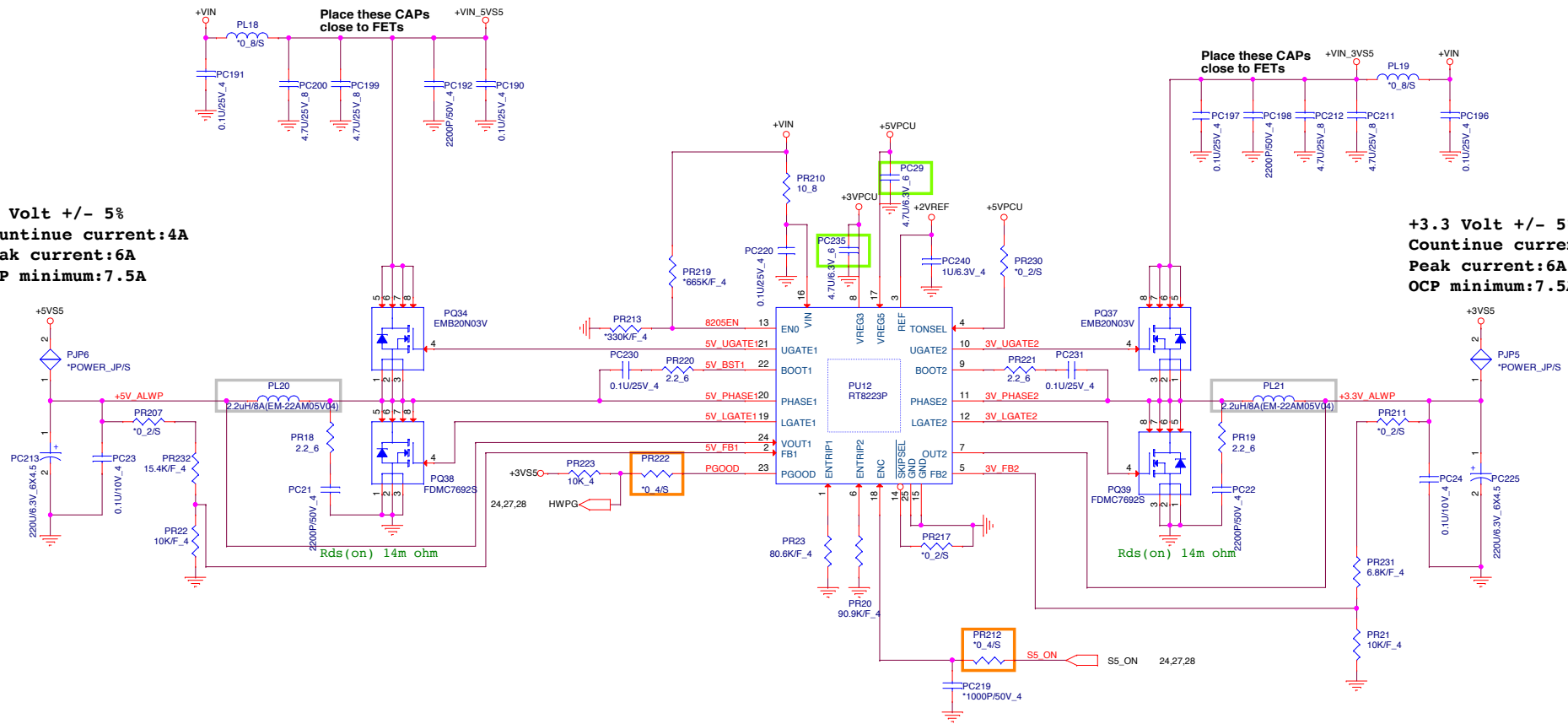
ADD VGA TEMP_FAIL function is active Hi




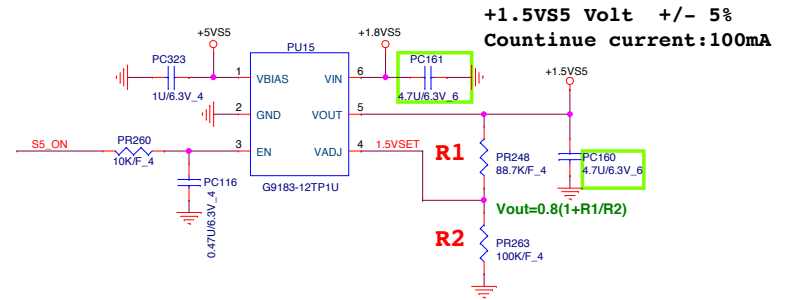
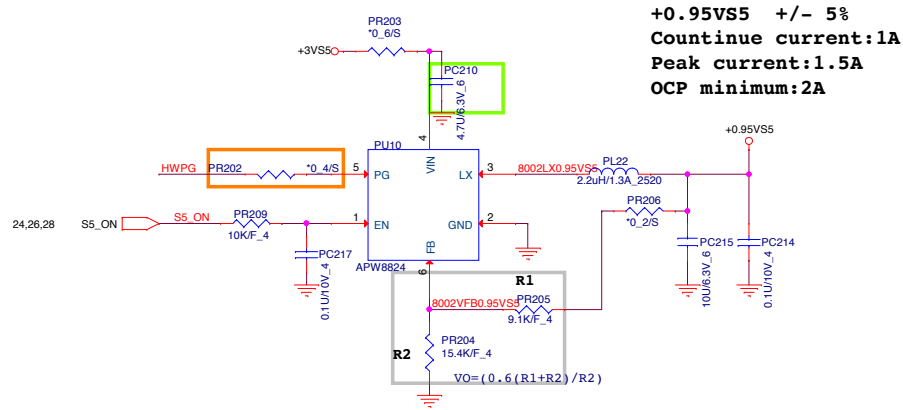
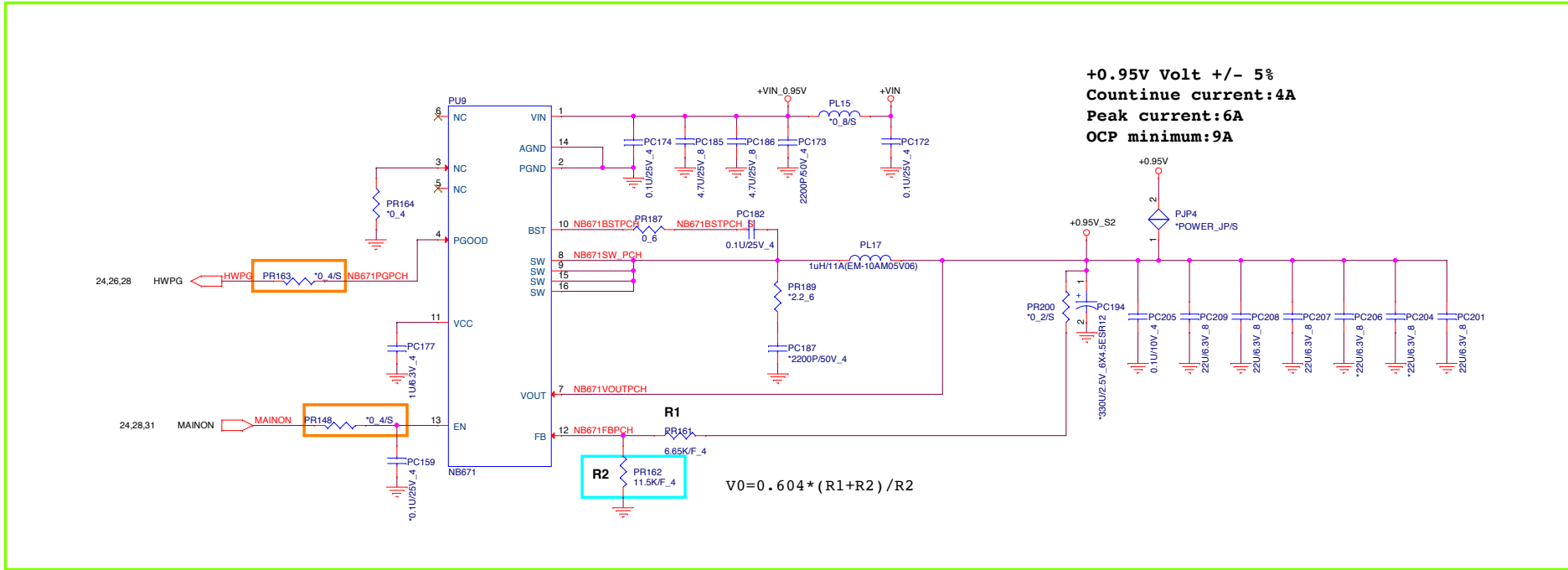
 PROJECT :U99 Quanta Computer Inc.		
Size Custom	Document Number Charger (028681)	Rev 1A
Date: Monday, May 19, 2014	Sheet 25 of 33	

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

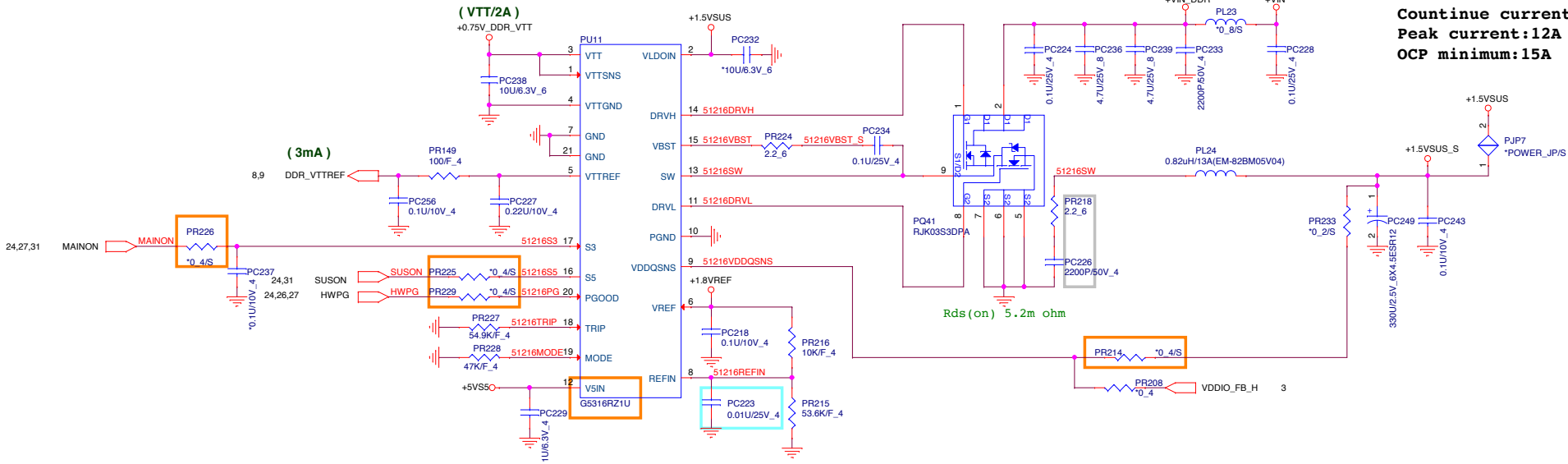


 PROJECT :U99 Quanta Computer Inc.			Size	Document Number	Rev
			Custom	3/5VPCU(RT8223P)	1A
Date:	Monday, May 19, 2014	Sheet	26	of	33

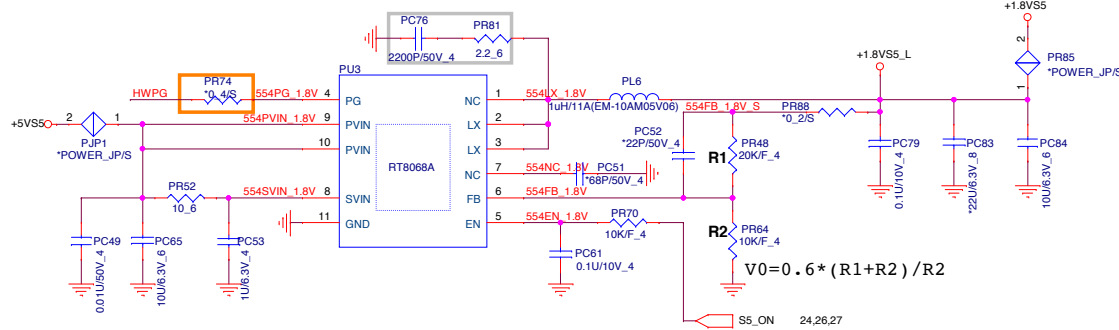


+1.5VSUS 2.6,8,9,31,33

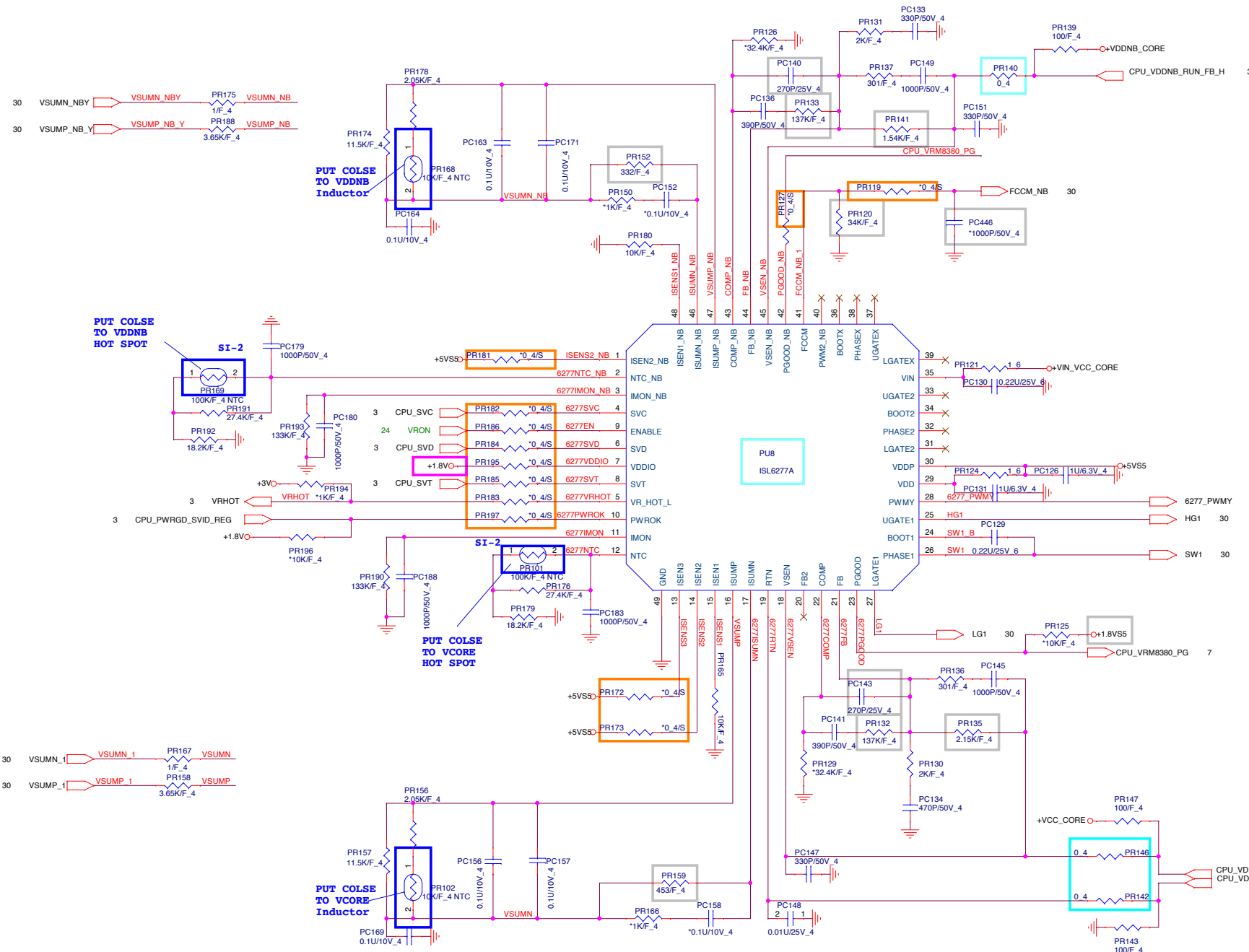
+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCp minimum:15A



1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCp minimum:4A



PROJECT :U99 Quanta Computer Inc.		
Size Custom	Document Number DDR3 (TP551216)	Rev 1A
Date: Monday, May 19, 2014	Sheet 26 of 33	



PUT COLSE TO VDDNB Inductor

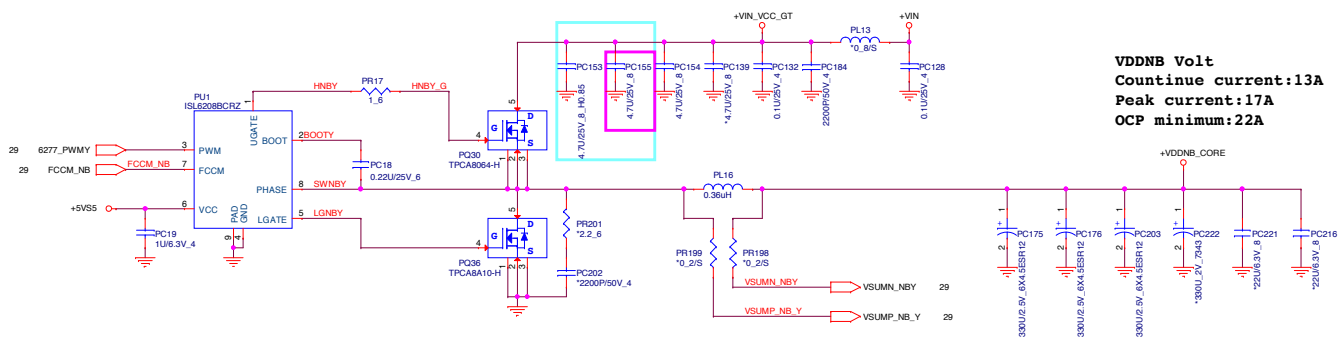
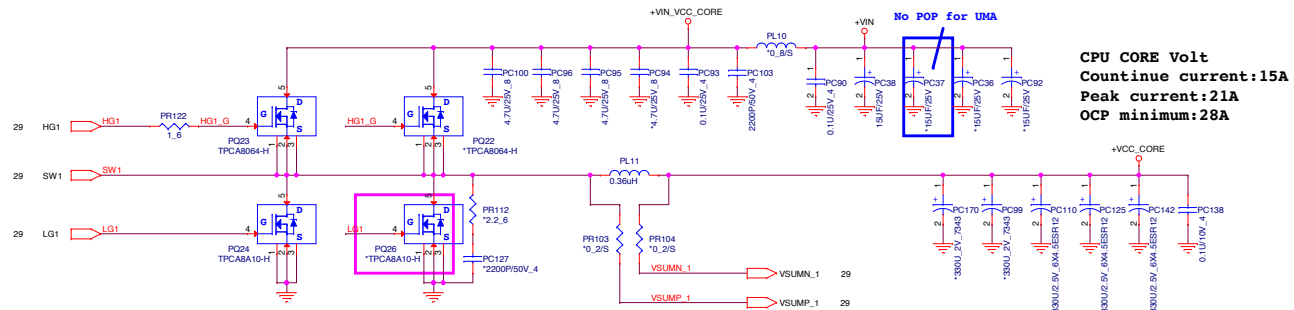
PUT COLSE TO VDDNB HOT SPOT

PUT COLSE TO VCORE HOT SPOT

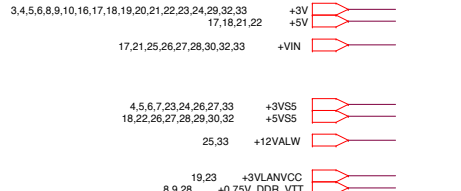
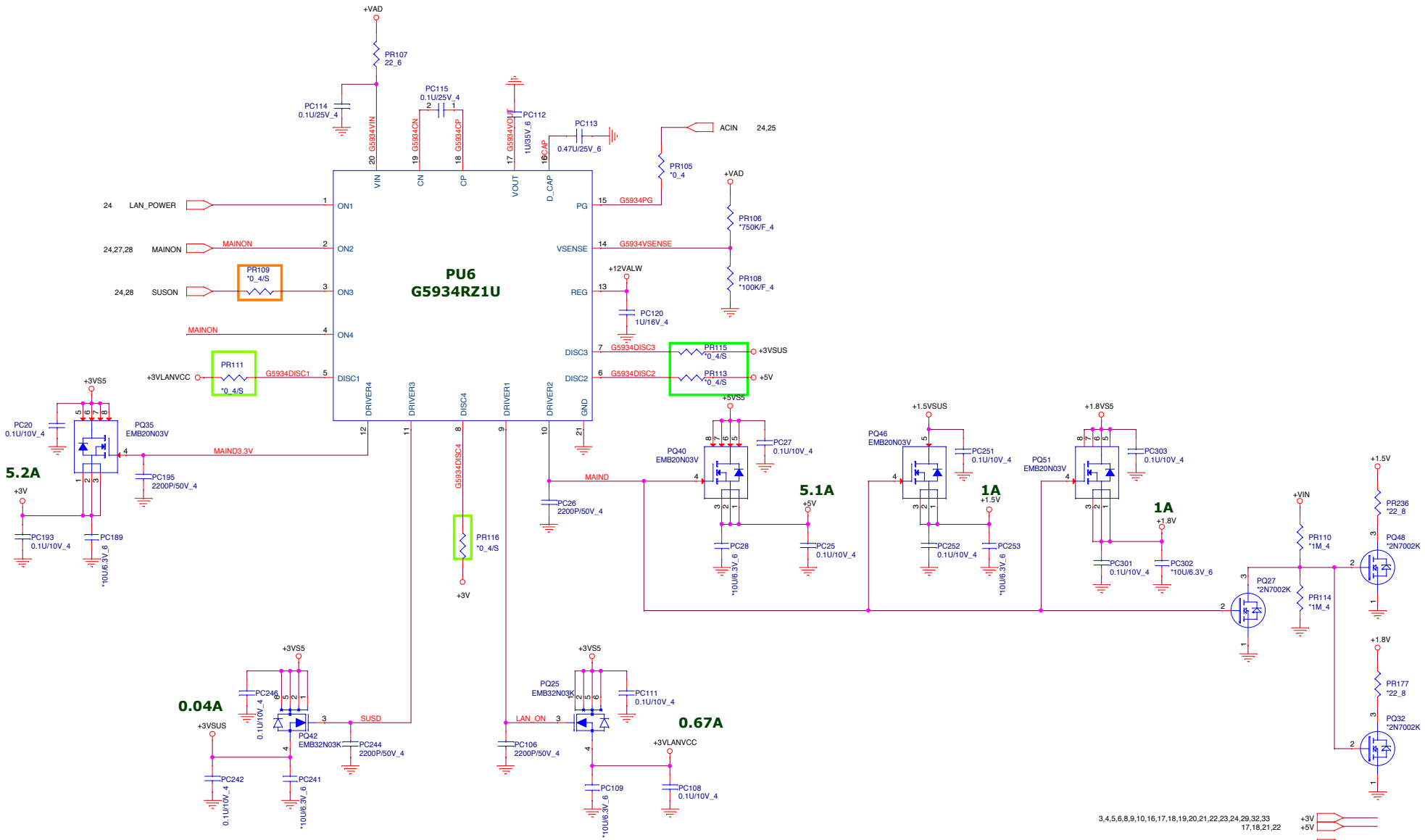
PUT COLSE TO VCORE Inductor

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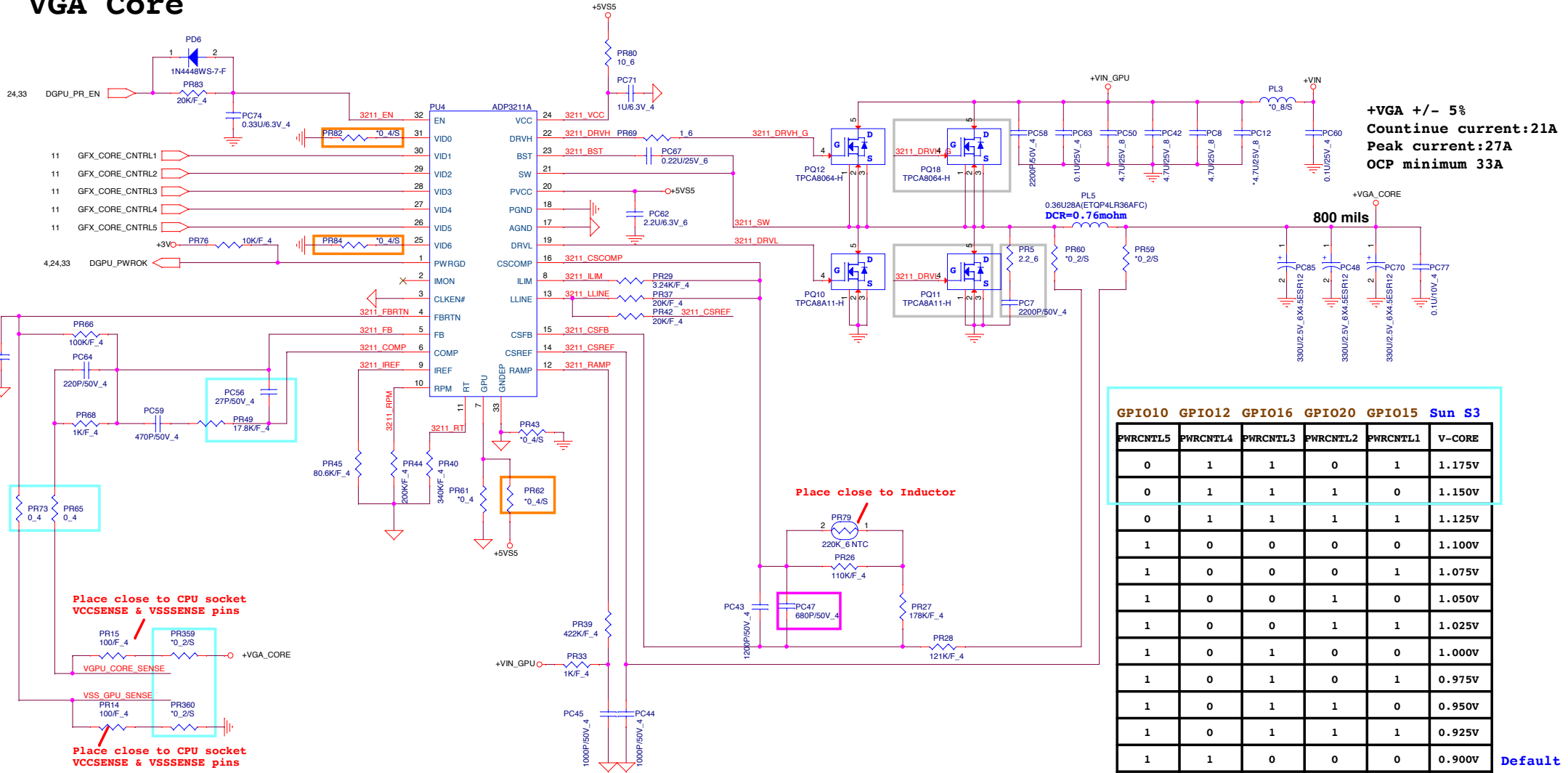
		PROJECT :U99 Quanta Computer Inc.	
Size Custom	Document Number ISL6277	Rev 1A	
Date: Monday, May 19, 2014		Sheet 29 of 33	



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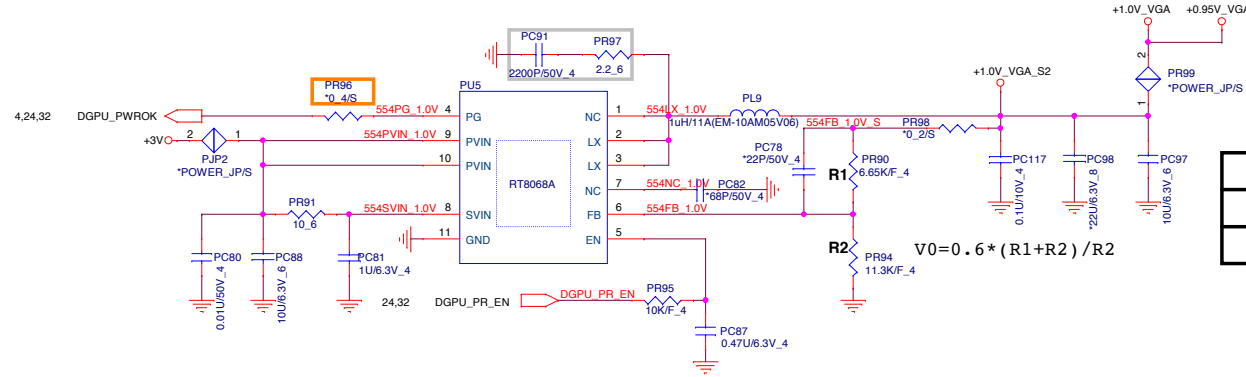
VGA Core



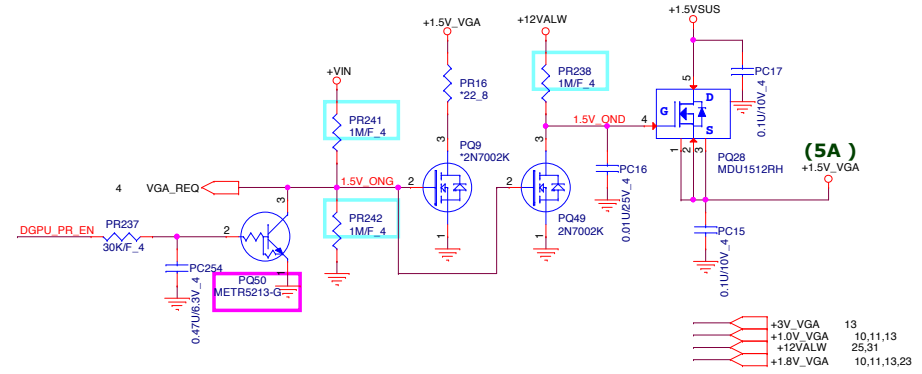
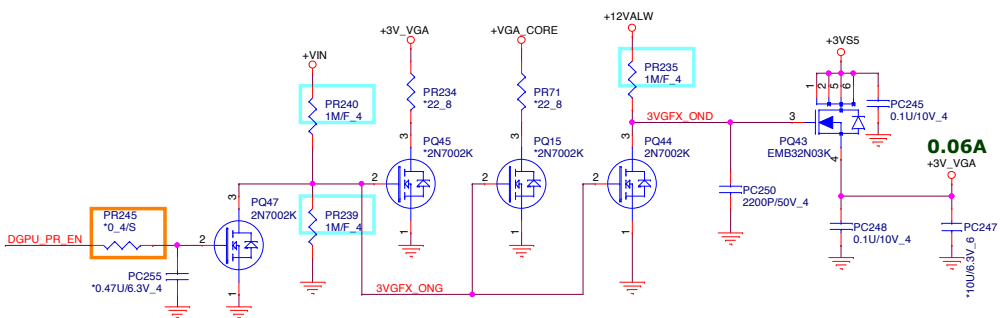
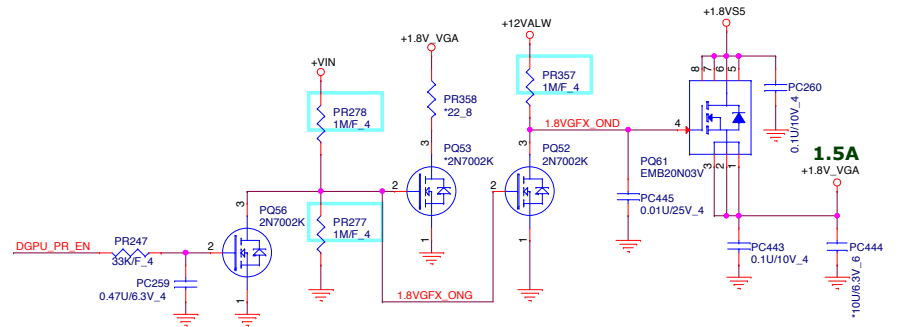
PROJECT :U99
Quanta Computer Inc.

Size Custom	Document Number +VGCORE NCP3218G)	Rev 1A
Date: Monday, May 19, 2014	Sheet 32 of 33	

+0.95V +/- 3%
Continue current:2A
Peak current:3A
OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V



- +3V_VGA 13
- +1.0V_VGA 10,11,13
- +12VALW 25,31
- +1.8V_VGA 10,11,13,23

<p>PROJECT :U99 Quanta Computer Inc.</p>		
Date: Monday, May 19, 2014	Sheet 33	of 33