

Compal confidential

Liverpool 10AR/10ARG

KSWAE LA-4971P Schematics Document

Mobile AMD S1G2 S1G3/
RS780MN & RS780MC & RX781 & RS880 /
SB700 & SB710

2009-02-09 Rev. 0.3

Security Classification	Compal Secret Data	Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25
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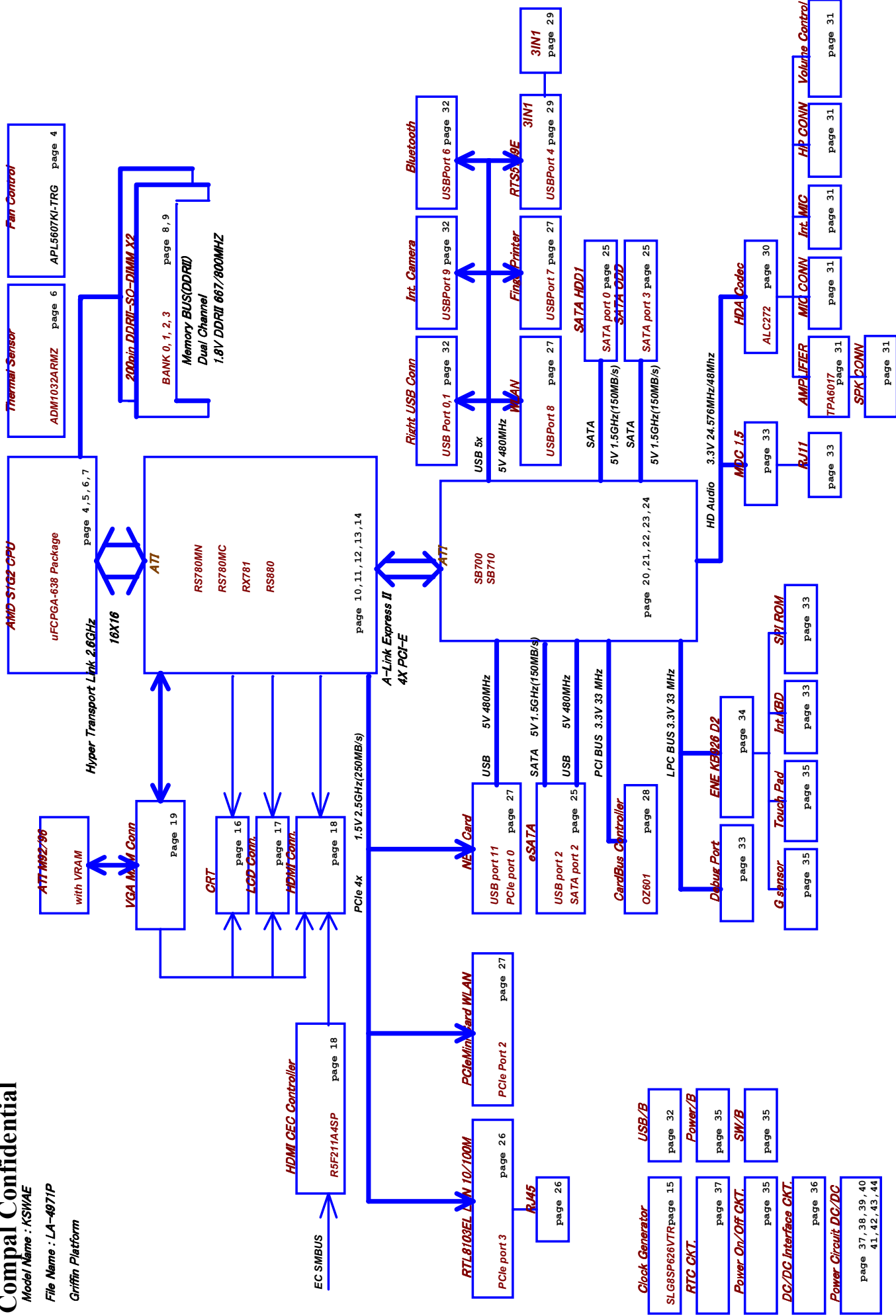
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Cover Sheet

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Model Name : KSWAE

File Name : LA-4971P

Griffin Platform



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Voltage Rails

O : ON
X : OFF

power plane	+B +3VL +5VL +RRCVCC	+5VALW +3VALW +1.2VALW +3V_IAN	+1.8V +0.9V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
state				
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : Digital Ground

 : Analog Ground

@ : just reserve , no build

DEBUG@ : reserve for debug.

 Layout Notes

UMA@: means for RS780M.

BTO (Build-To-Order) Option Table

Function	Express card / PCMCIA (E/A)	BLUE TOOTH (B)	RJ11 (R)	SSD (S)	SATA ODD	WIFI (H)	G- sensor
Description							
Explain		16"	17"	Half - size	First	Second	RTS5159
BTO	EXPCARD@/PCMCIA@	BT@	MDC@	SSD@	16inch@	WLAN@	WIMAX@ G@ + G_1st@ G@ + G_2nd@

Function	FingerPrinter (F)	CAMERA & MIC (X)	HDMI (Y)	DC-IN
Description				
Explain		CAMERA MIC	AMD(UMA) ATI VGA/B COMMON	Cost down
BTO	FP@	CAM@ MIC@ IHDMI@	HDMI@	H@

SMBUS Control Table

SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD	MXM Thermal Sensor
EC_SMB_CK1											
EC_SMB_DA1		V	V								
EC_SMB_CK2				V							V
EC_SMB_DA2											
I2C_CLK											
I2C_DATA								V			
DDC_CLK0									V		
DDC_DATA0										V	
DDC_CLK1											
DDC_DATA1											
SCL0										V	
SDA0											
SCL1										V	
SDA1											
SCL2											
SDA2											
SCL3											
SDA3											

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM0	A0	10100000
DDR SO-DIMM1	A4	10100100
CLOCK GENERATOR (EXT)	D2	11010010

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001011X b
HDMI-CEC	34H	0011010X b
EC KB926D2		

EC SM Bus2 address

Device	HEX	Address
AD1032-1 CPU	98H	1001100X b
AD1032-2 VGA	9AH	1001101X b
EC KB926D2		
ExL VGA/B		
CS/B		

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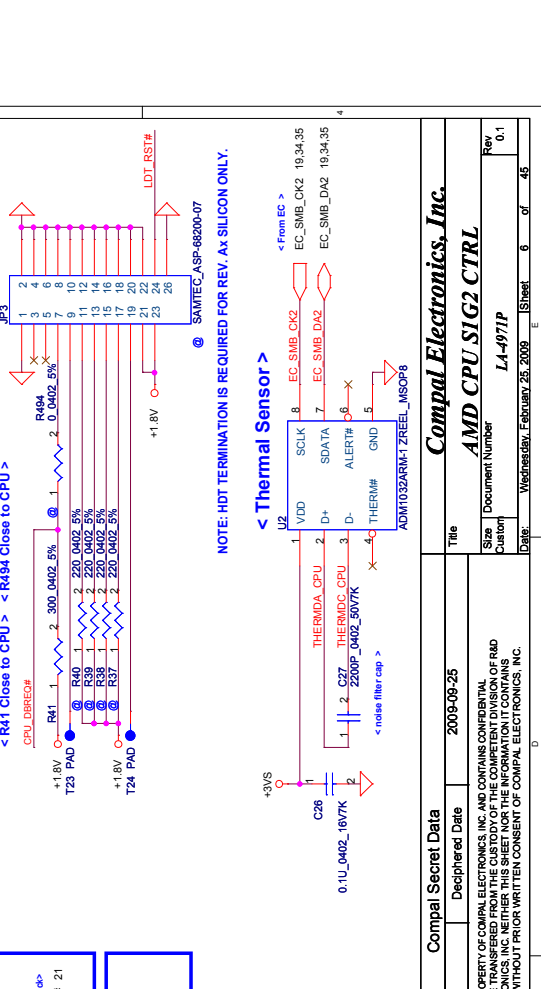
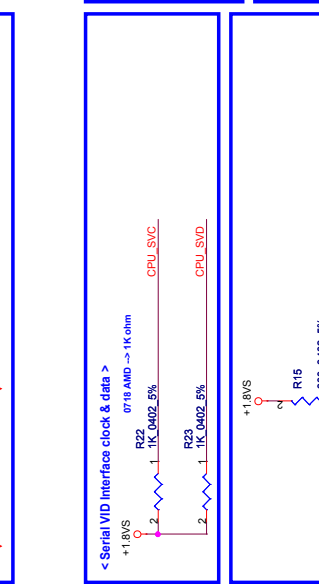
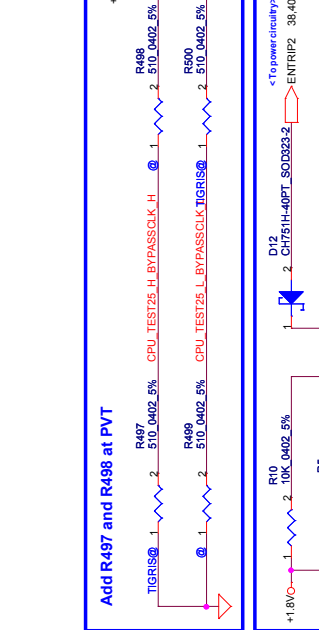
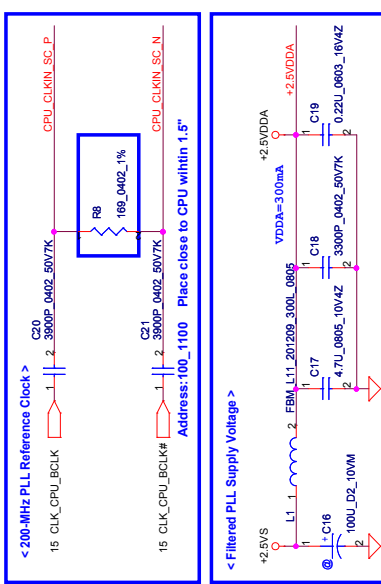
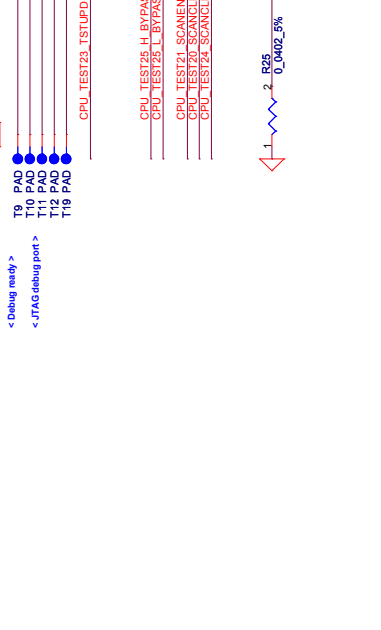
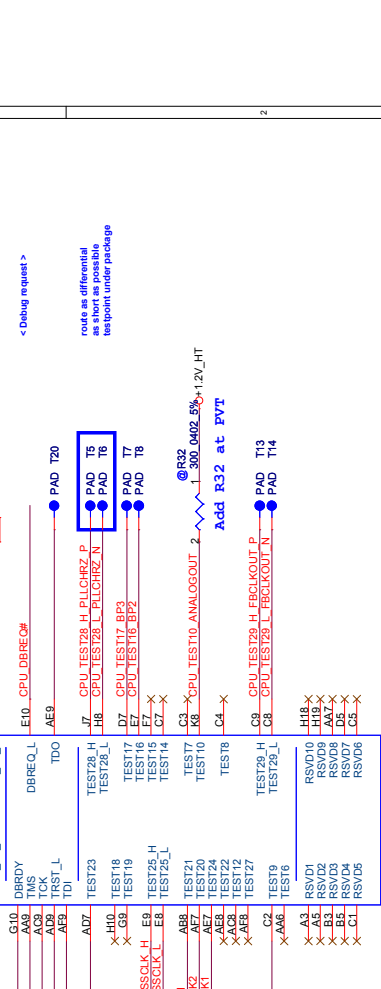
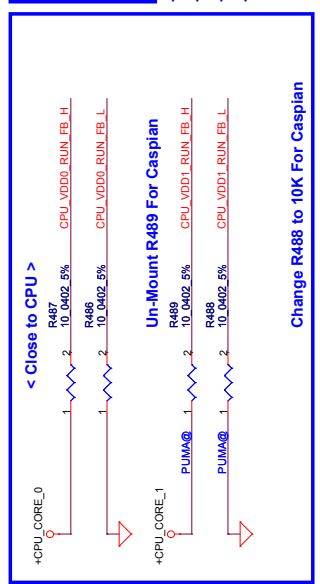
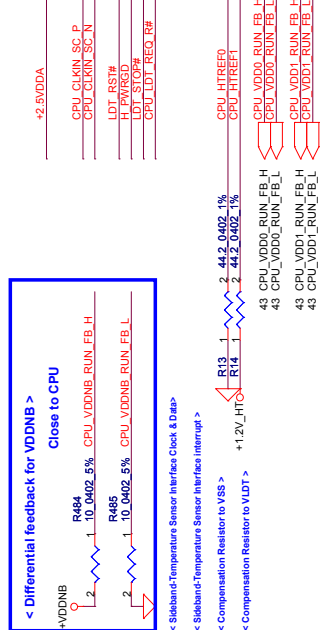
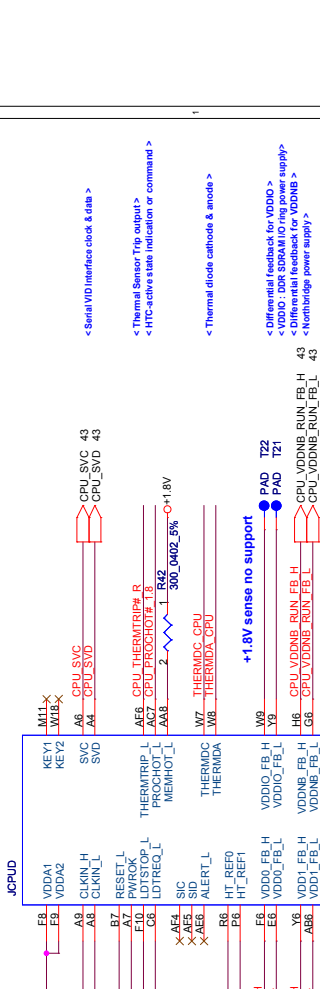
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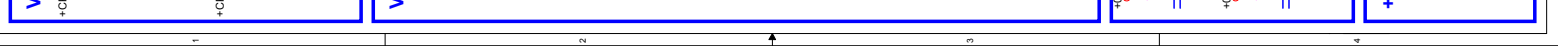
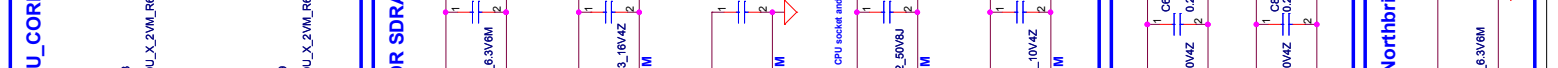
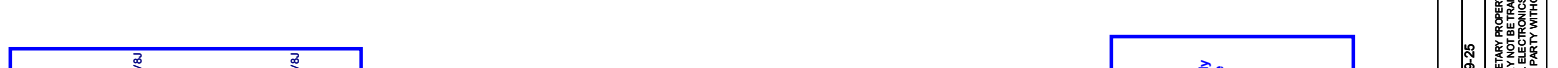
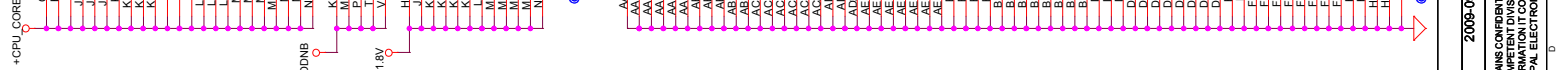
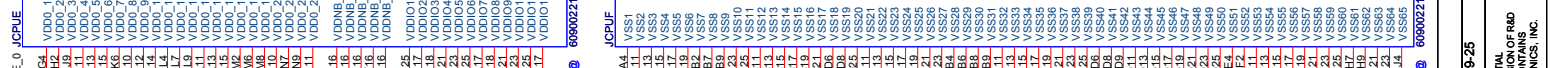
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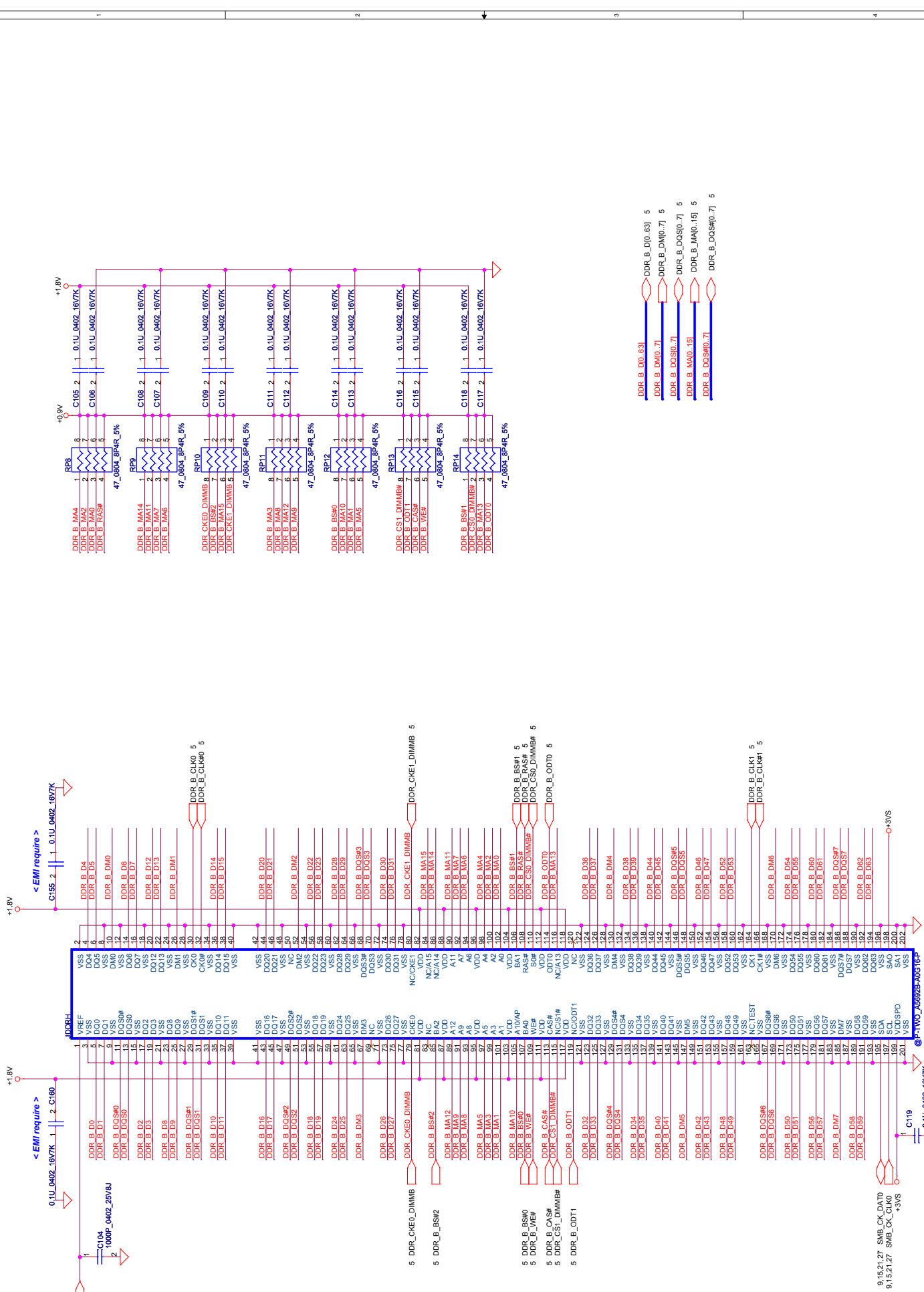
Notes List

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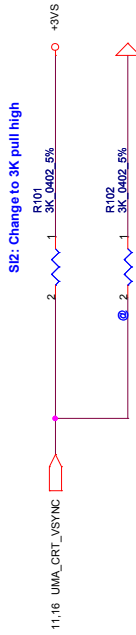


- DDR_B_D0(63) 5
- DDR_B_DM0(7) 5
- DDR_B_DOS0(7) 5
- DDR_B_MA0(15) 5
- DDR_B_DOS0(7) 5

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				Compal Secret Data	
				DDRII SO-DIMM 0	
				Size Document Number	
				L4-4971P	
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< RS780 DFT_GPIO5 mux at CRT_VSYNC pull High to 3K >

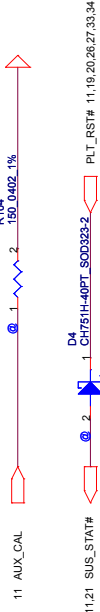


< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED >
 Enables the Test Debug Bus using GPIO.
 1 : Enable (RX780, RS780)
 0 : Disable (RX780, RS780)
 PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780-->VSYNC#

< RS780 use register to control PCIe configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >
 These pin straps are used to configure PCIe GPP mode.
 000 : 00001
 001 : 00010
 010 : 01011
 011 : 00100
 100 : 01010
 101 : 01100
 111 : 01011

< RS780 DFT_GPIO1 >



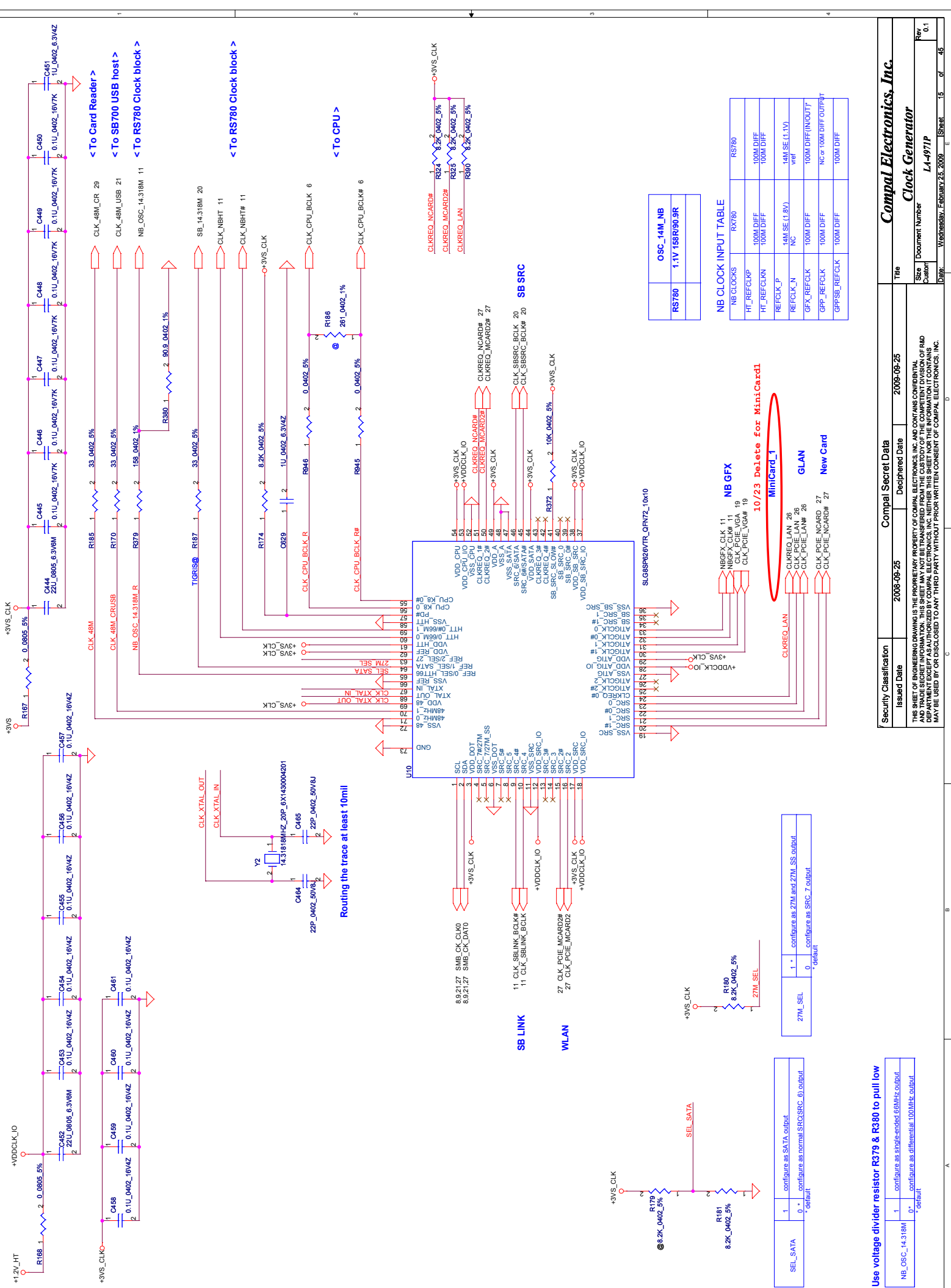
< DFT_GPIO1 : LOAD_EEPROM_STRAPS >
 Selects Loading of STRAPS from EPROM
 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

< RS780 use HSYNC to enable SIDE PORT (internal pull high) >



< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLED >
 RX780: Enables the Test Debug Bus using PCIe bus
 1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable
 RS780: Enables Side port memory (RS780 use HSYNC#)
 1 : Disable (RS780)
 0 : Enable (RS780)

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Title	RS780M&RX781 STRAPS		
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Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 6MHz output
0*	0*	configure as differential 100MHz output
* default		

SEL_SATA	1	configure as SATA output
0*	0*	configure as normal SRC(SRC.B) output
* default		

27M_SEL	1*	configure as 27M and 27M_SS output
0*	0*	default

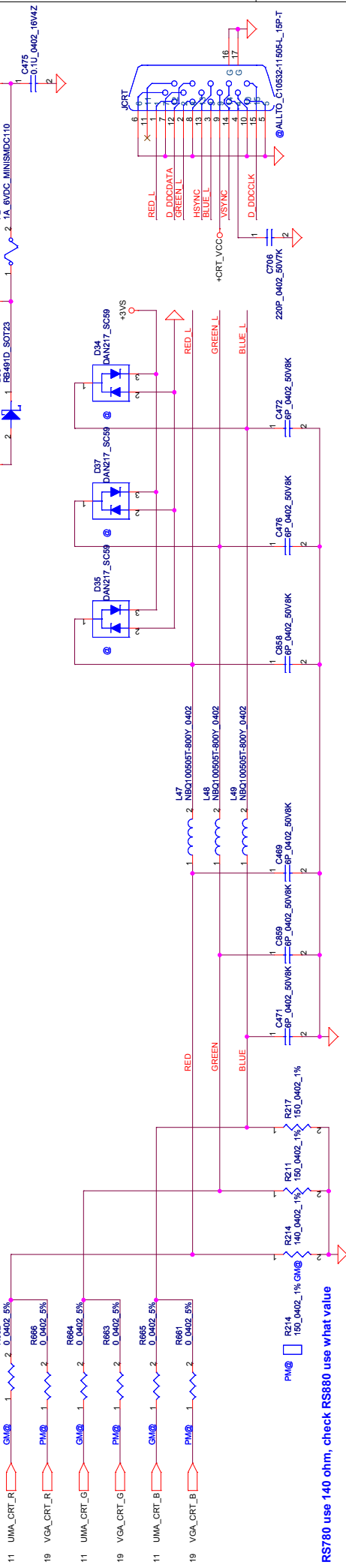
OSC_14M_NB

RS780	1-1V 158R/90.9R
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NB CLOCK INPUT TABLE

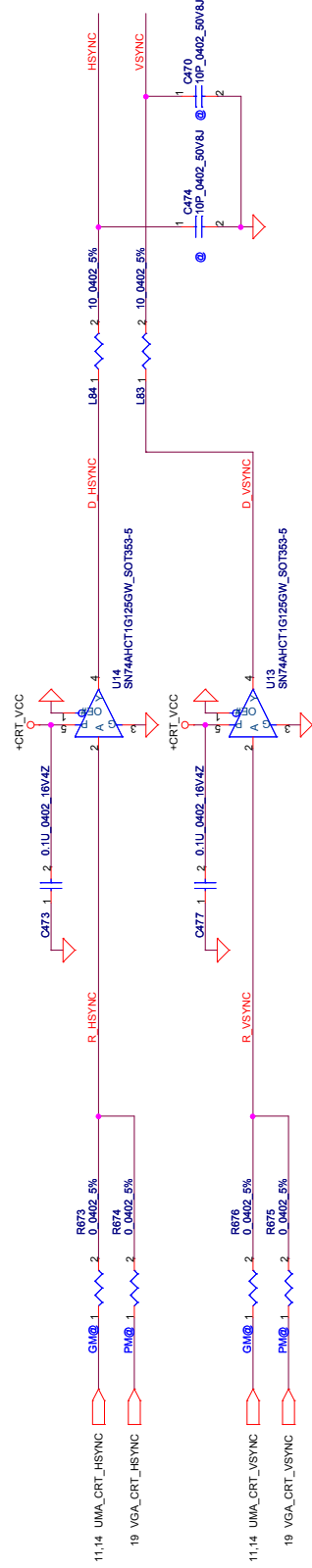
NB CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.8V)
REFCLK_N	NC
GPX_REFCLK	100M DIFF
GPX_REFCLK	100M DIFF
GPFSB_REFCLK	100M DIFF

< CRT CONNECTOR >

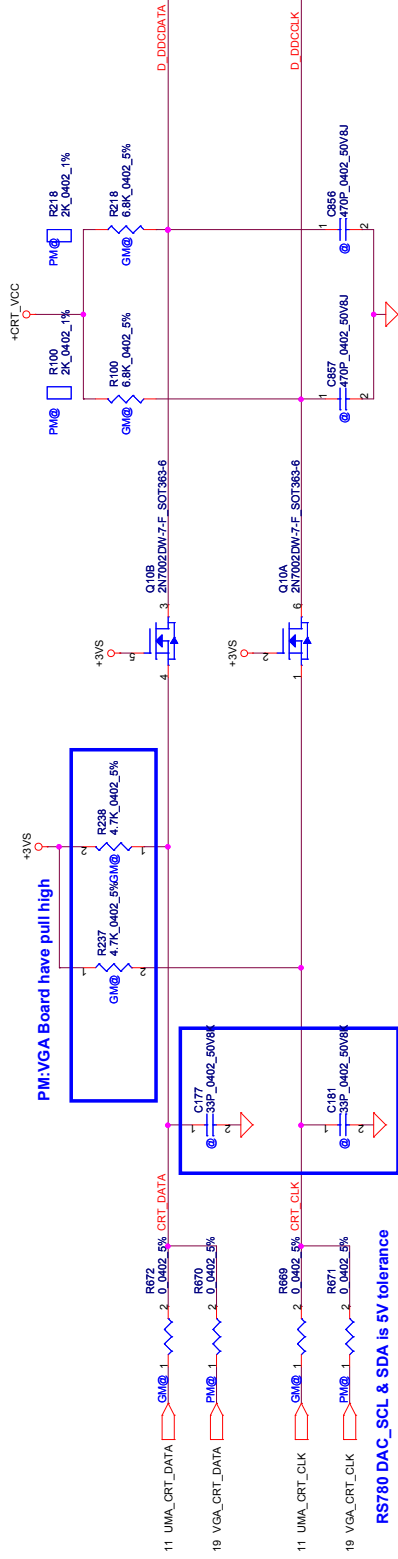


RS780 use 140 ohm, check RS880 use what value

< SYNC SIGNAL >



< Display Data Channel >



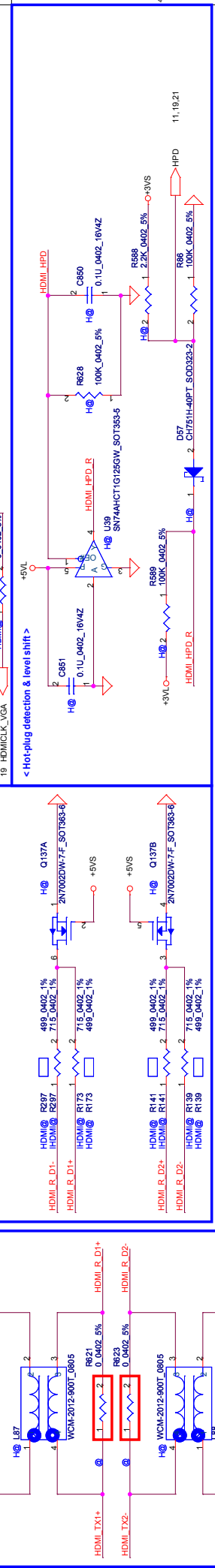
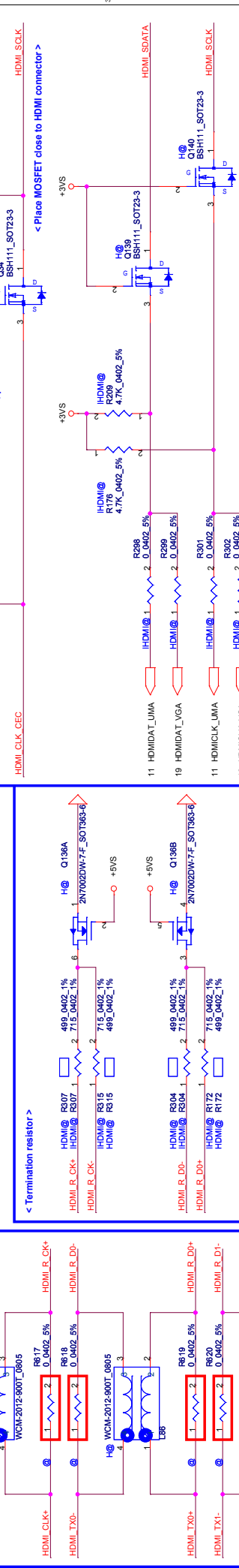
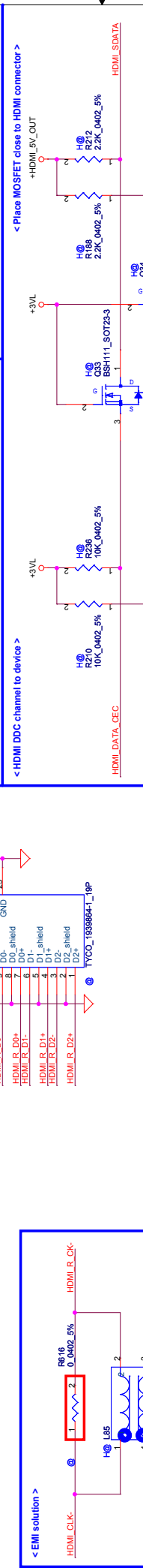
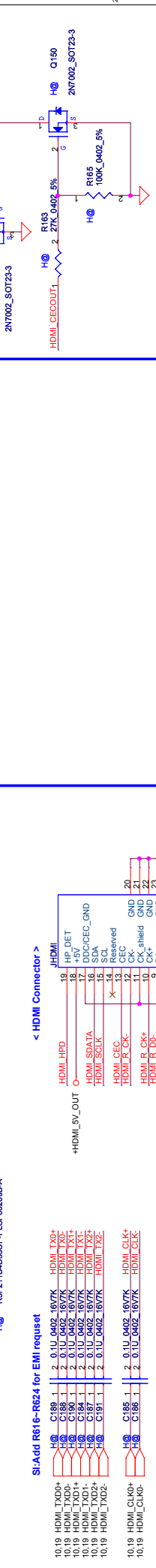
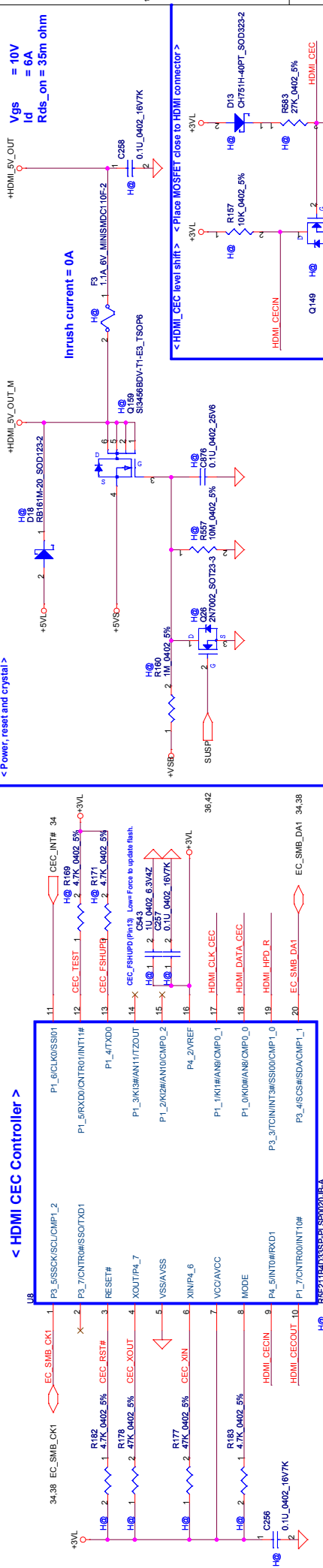
PM:VGA Board have pull high

RS780 DAC_SCL & SDA is 5V tolerance

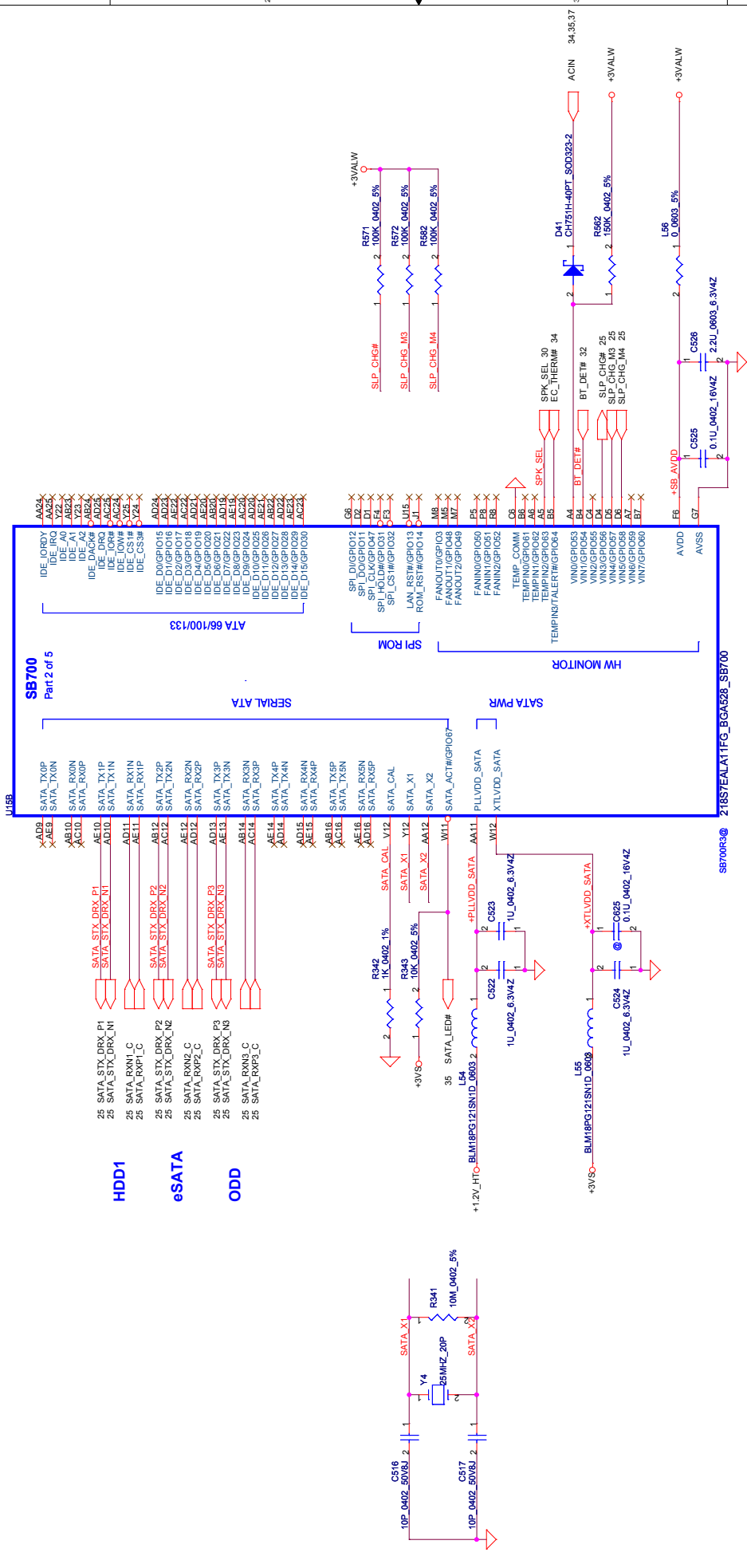
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CRU/TV-OUT Connector



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<p>Compal Electronics, Inc. HDMI/CEC</p>				



SB700
Part 2 of 5

ATA 68/100/133

SPI ROM

HW MONITOR

SATA PWR

SERIAL ATA

IDE_IORX

IDE_IRO

IDE_A0

IDE_A1

IDE_A2

IDE_A3

IDE_A4

IDE_A5

IDE_A6

IDE_A7

IDE_A8

IDE_A9

IDE_A10

IDE_A11

IDE_IORX

IDE_IRO

IDE_A0

IDE_A1

IDE_A2

IDE_A3

IDE_A4

IDE_A5

IDE_A6

IDE_A7

IDE_A8

IDE_A9

IDE_A10

IDE_A11

IDE_A12

IDE_IORX

IDE_IRO

IDE_A0

IDE_A1

IDE_A2

IDE_A3

IDE_A4

IDE_A5

IDE_A6

IDE_A7

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IDE_A9

IDE_A10

IDE_A11

IDE_A12

IDE_IORX

IDE_IRO

IDE_A0

IDE_A1

IDE_A2

IDE_A3

IDE_A4

IDE_A5

IDE_A6

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IDE_A12

IDE_IORX

IDE_IRO

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IDE_A2

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IDE_A4

IDE_A5

IDE_A6

IDE_A7

IDE_A8

IDE_A9

IDE_A10

IDE_A11

IDE_A12

IDE_IORX

IDE_IRO

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IDE_IORX

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IDE_IORX

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IDE_IORX

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IDE_A11

IDE_A12

IDE_IORX

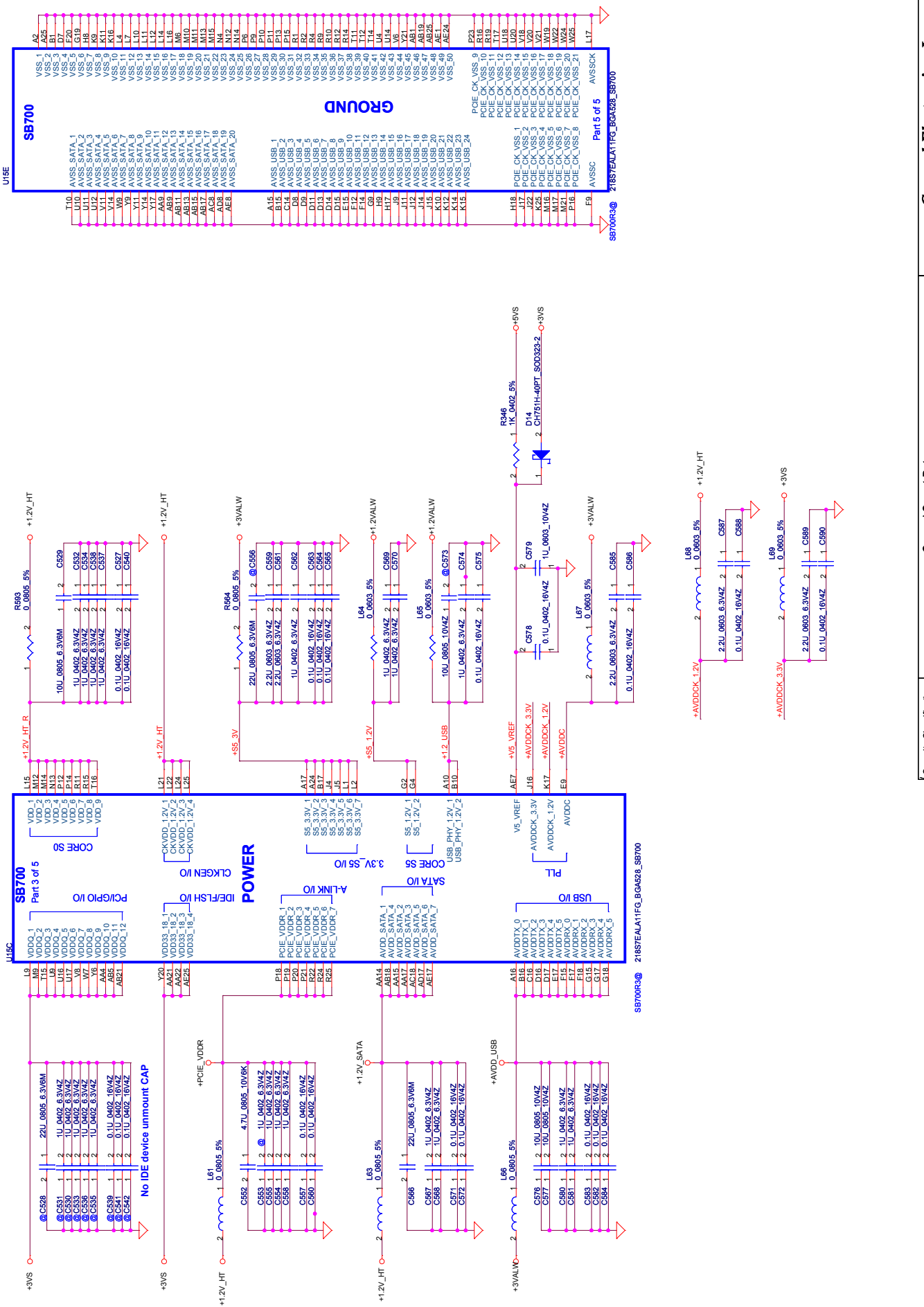
IDE_IRO

IDE_A0

IDE_A1

IDE_A2

IDE_A3



SB700
Part 3 of 5

POWER

A-LINK I/O

SATA I/O

USB I/O

AVSS

AVDD

AVSS

AVDD

AVSS

AVDD

AVSS

AVDD

AVSS

AVDD

AVSS

SB700
Part 5 of 5

GROUND

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

AVSS

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SB700 Power/GND

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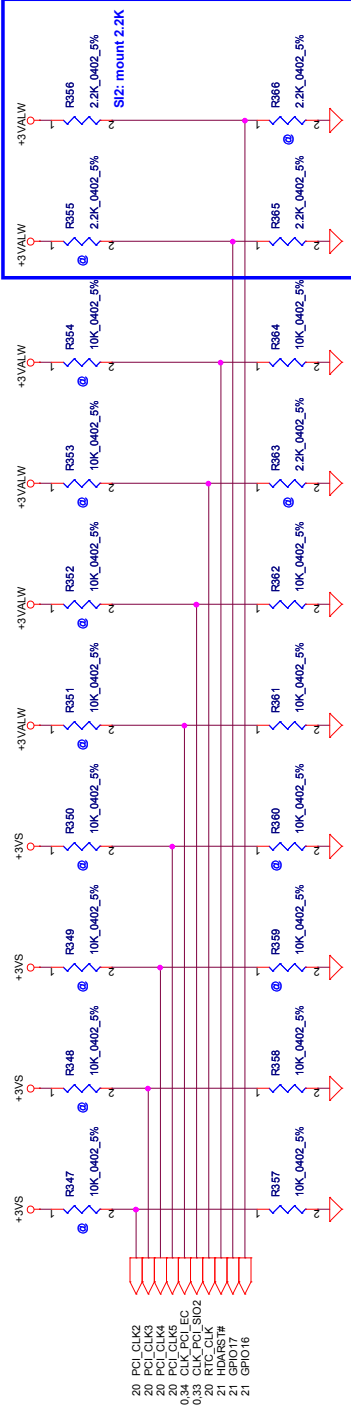
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK_AZ_RST_CD#	GP17	GP16
PULL HIGH	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC	Internal pull up	Reserved
PULL LOW	IGNORE DEBUG STRAPS			DISABLE PCI MEM BOOT	CLKGEN DISABLED	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	H.I = Reserved H.L = SPI ROM	L.H = LPC ROM (Default) L.L = FWH ROM

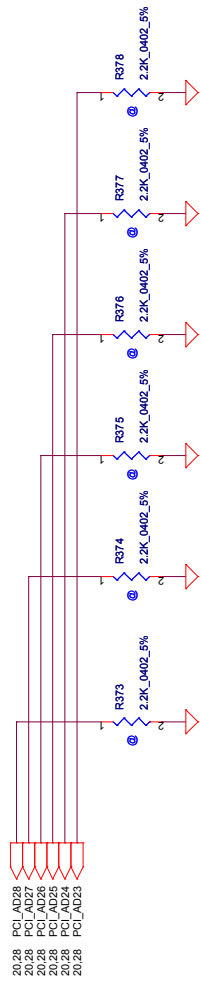


Need to confirm if SB SPI ROM will mount

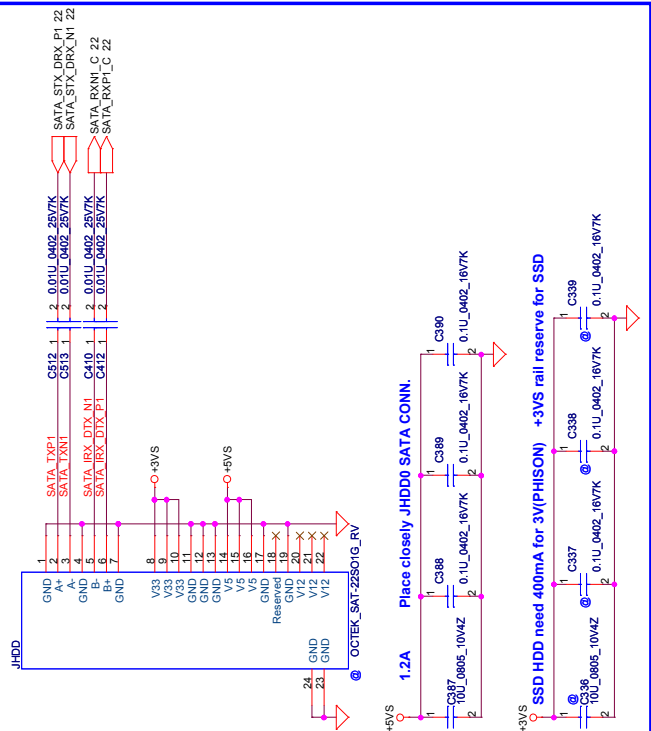
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:33]

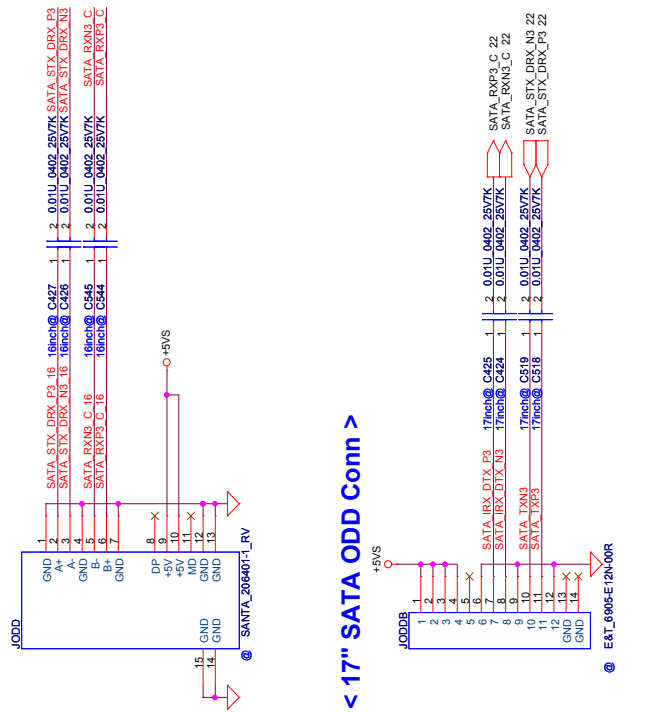
PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT POE STRAPS	RESERVED
PULL LOW	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM POE STRAPS	



< SATA HDD1 Conn >



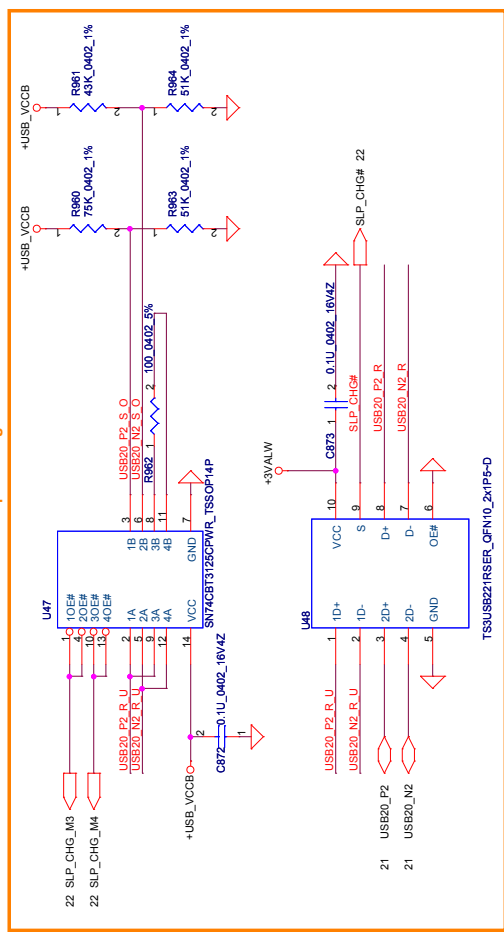
< 16" SATA ODD Conn >



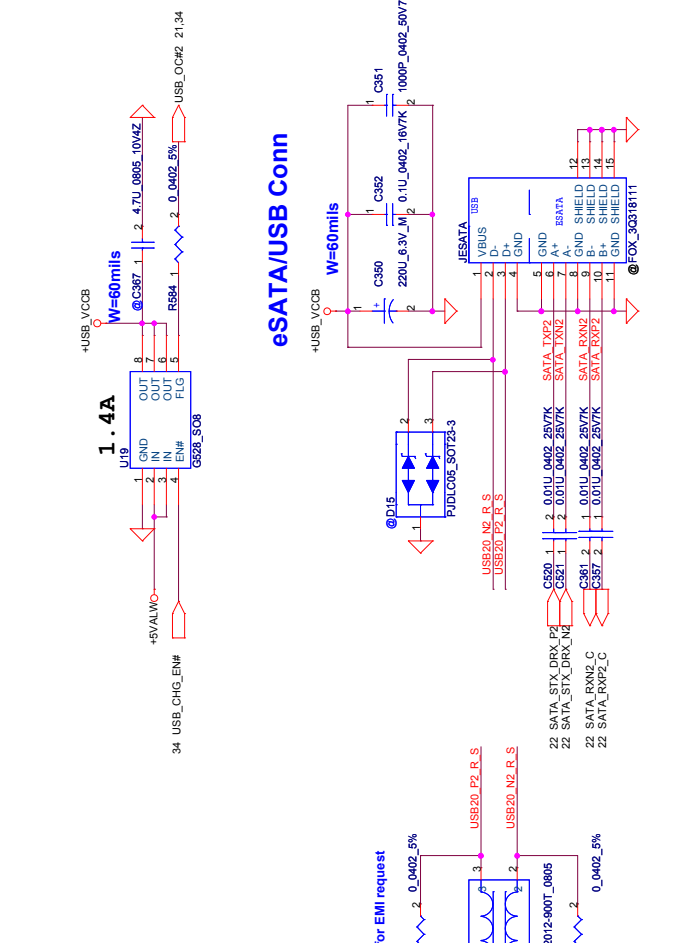
< 17" SATA ODD Conn >



< eSATA/USB >



< eSATA/USB Conn



Mode	SIP_CHG_M3	SIP_CHG_M4	FUNCTION
3	HIGH	LOW	D=1D
4	LOW	HIGH	D=2D

SIP_CHG#	FUNCTION
LOW	D=1D
HIGH	D=2D

Security Classification: 2008-09-25
 Issued Date: 2008-09-25
 Deciphered Date: 2009-09-25
 Title: SATA HDD/ODD/ESATA USB
 Size: L4-4971P
 Customer: Compal Electronics, Inc.
 Date: Wednesday, February 25, 2009 25 of 49

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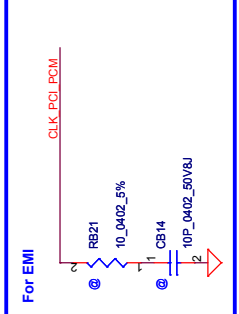
22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

+3VS

RB22 2 33K 0402 5% CLKRUN#

RB23 2 33K 0402 5% SERIRQ

RB24 2 33K 0402 5% PCI_PIRQA#



NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.

IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

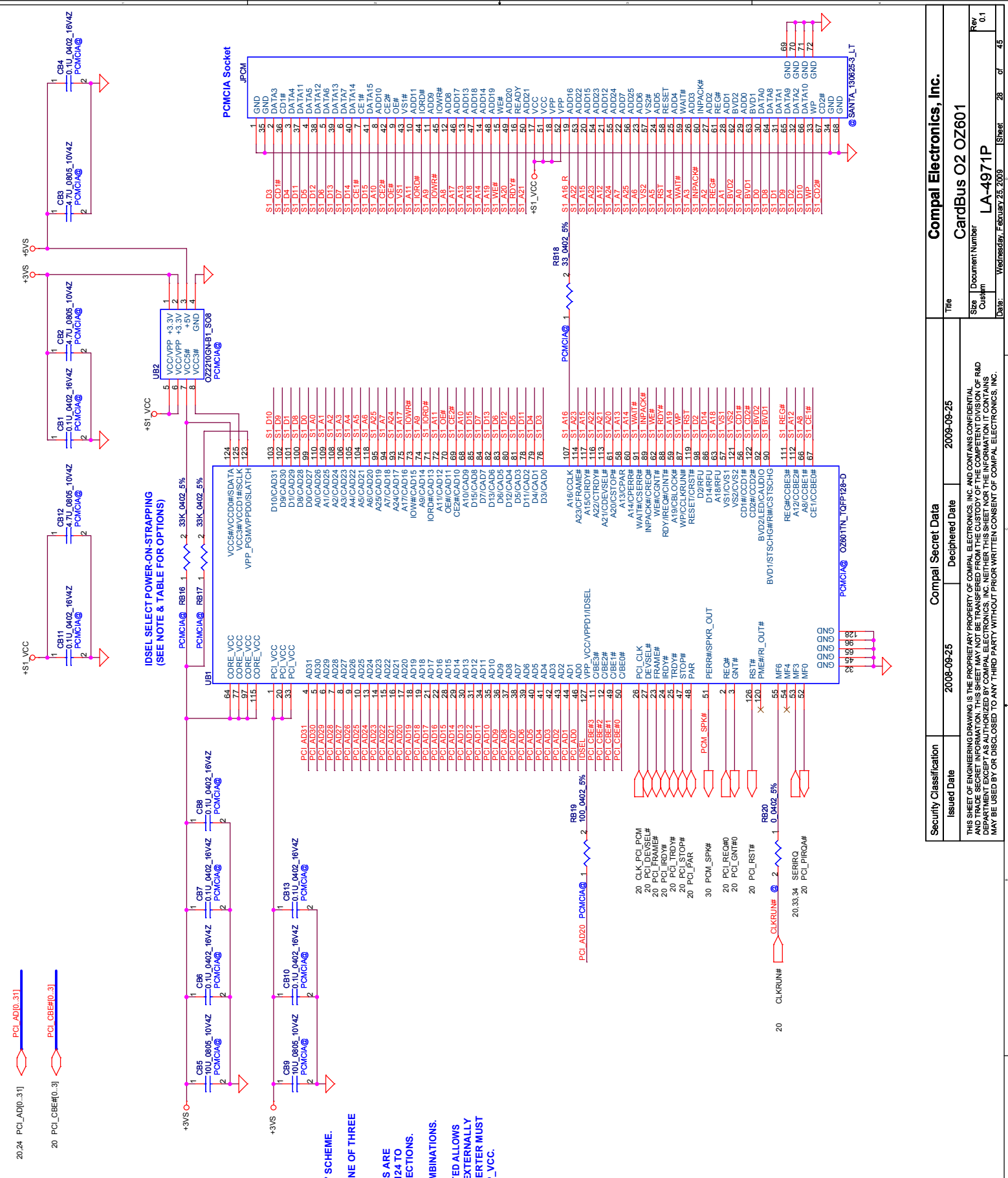
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.

THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCCS#	VPP_PGM	IDSEL SELECT
(124)	DOWN	AD18
	DOWN	AD20
	UP	AD25
	UP	PIN 127 ball F4

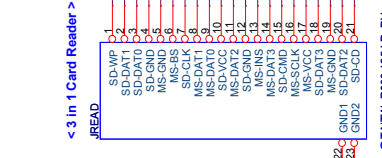
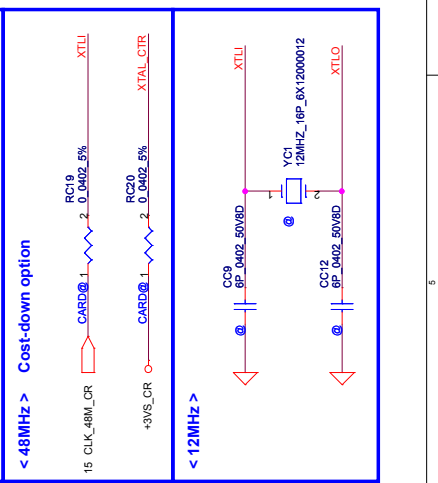
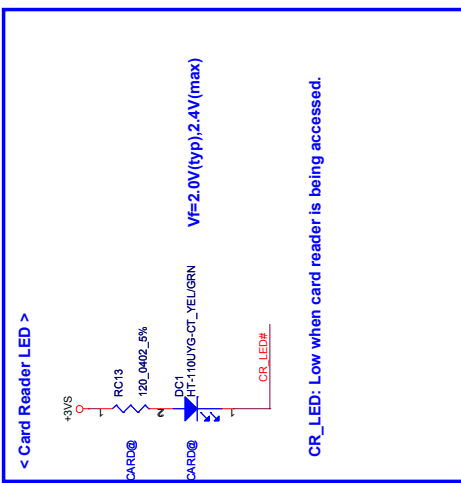
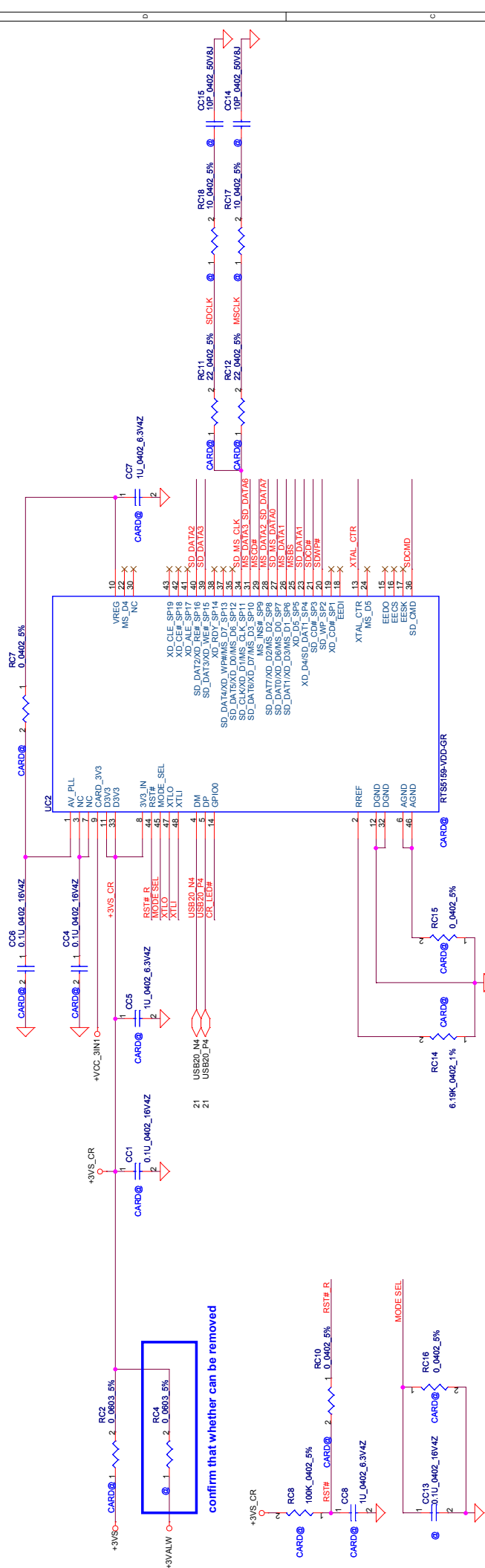
must check IDSEL, PCI_PIRQA#,



IDSEL SELECT POWER-ON-STRAPPING (SEE NOTE & TABLE FOR OPTIONS)

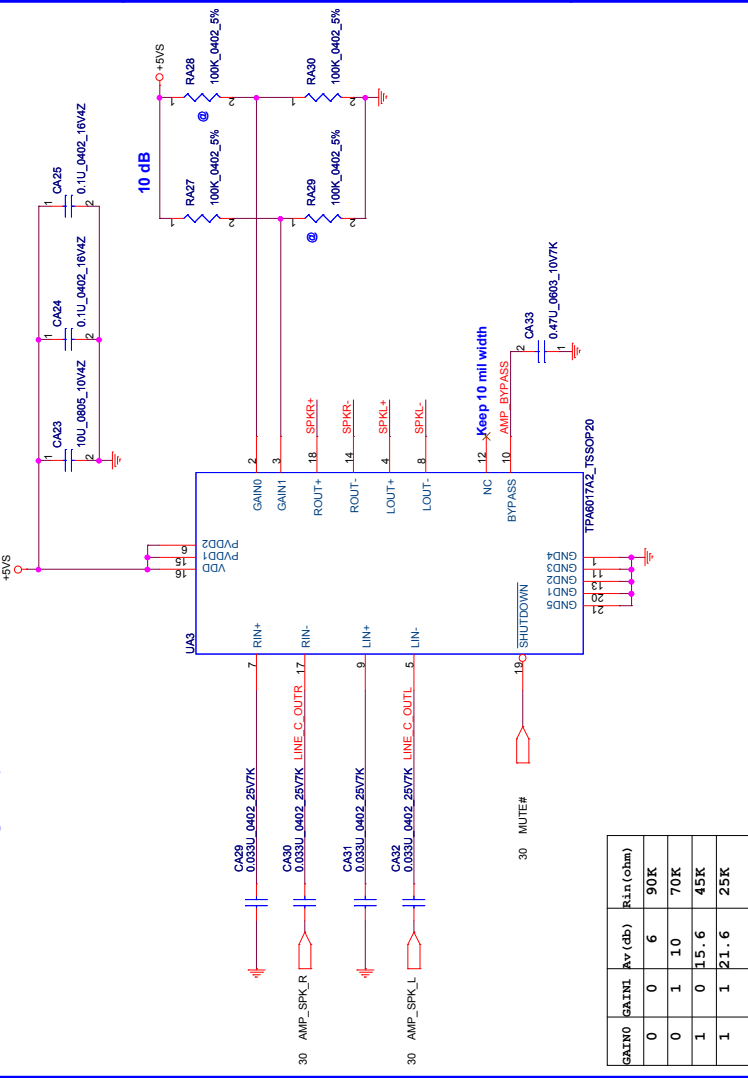
103	S1 D10
104	S1 D9
105	S1 D8
106	S1 D7
107	S1 D6
108	S1 D5
109	S1 D4
110	S1 D3
111	S1 D2
112	S1 D1
113	S1 D0
114	S1 A16
115	S1 A15
116	S1 A14
117	S1 A13
118	S1 A12
119	S1 A11
120	S1 A10
121	S1 A9
122	S1 A8
123	S1 A7
124	S1 A6
125	S1 A5
126	S1 A4
127	S1 A3
128	S1 A2
129	S1 A1
130	S1 A0
131	S1 V17
132	S1 V16
133	S1 V15
134	S1 V14
135	S1 V13
136	S1 V12
137	S1 V11
138	S1 V10
139	S1 V9
140	S1 V8
141	S1 V7
142	S1 V6
143	S1 V5
144	S1 V4
145	S1 V3
146	S1 V2
147	S1 V1
148	S1 V0
149	S1 VPP
150	S1 VCC5#
151	S1 VCC4#
152	S1 VCC3#
153	S1 VCC2#
154	S1 VCC1#
155	S1 VCC#
156	S1 GND
157	S1 GND
158	S1 GND
159	S1 GND
160	S1 GND
161	S1 GND
162	S1 GND
163	S1 GND
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297	S1 GND
298	S1 GND
299	S1 GND
300	S1 GND

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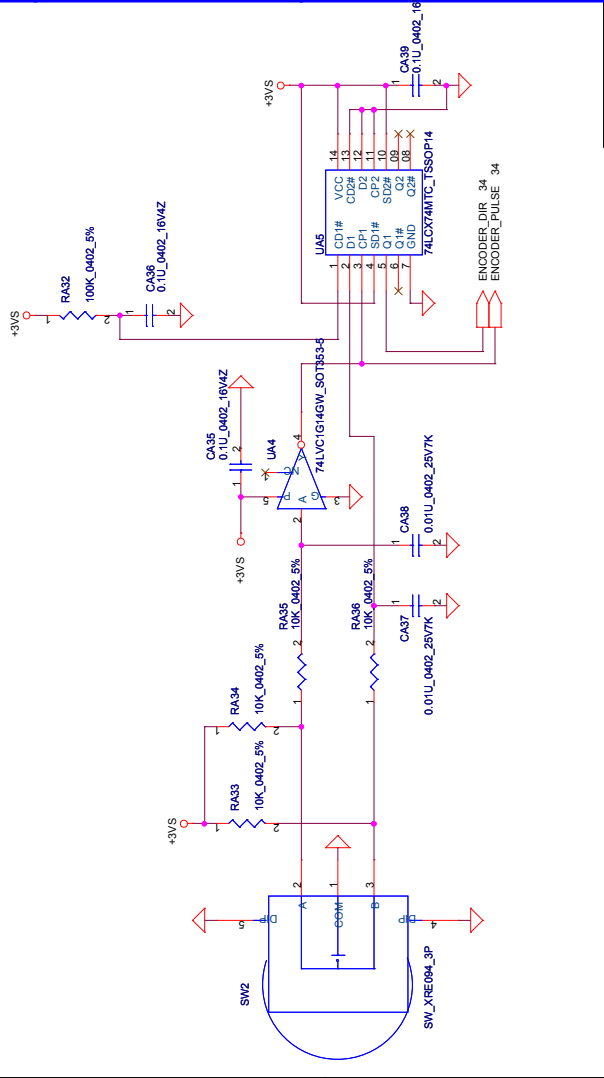


R	C	USB	AUTO	DE-LINK	MS	FORMATTER	Description
0	NC	YES	YES	YES	YES	YES	Recommended
NC	47P	YES	YES	YES	YES	YES	Compatible with RTS5158E
NC	680P	YES	YES	YES	YES	YES	LED ON
10K	180P	YES	YES	YES	YES	YES	LED ON
10K	680P	YES	YES	YES	YES	YES	LED ON

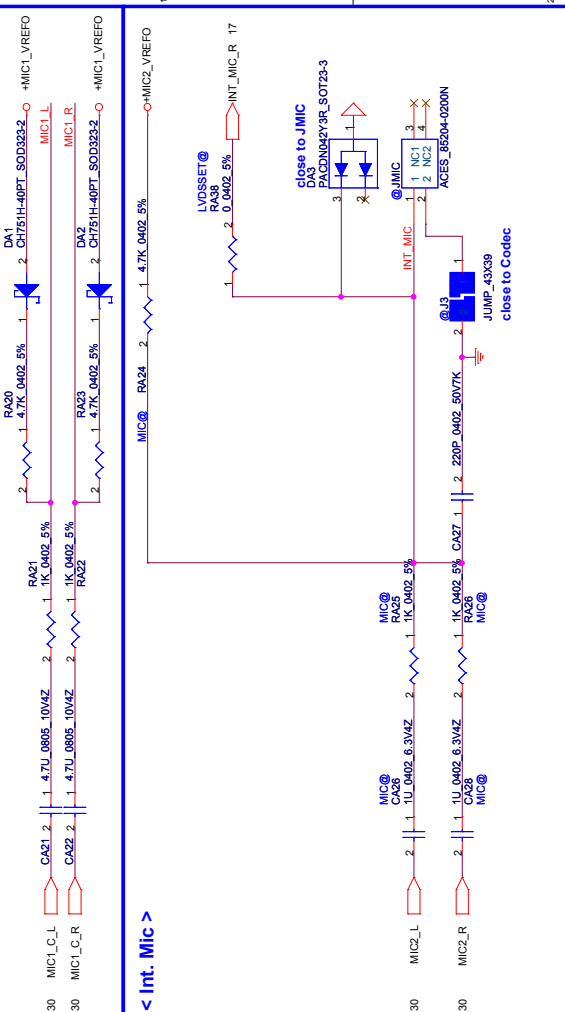
< TPA6017 Medium Range Amplifier >



< Volume Control >

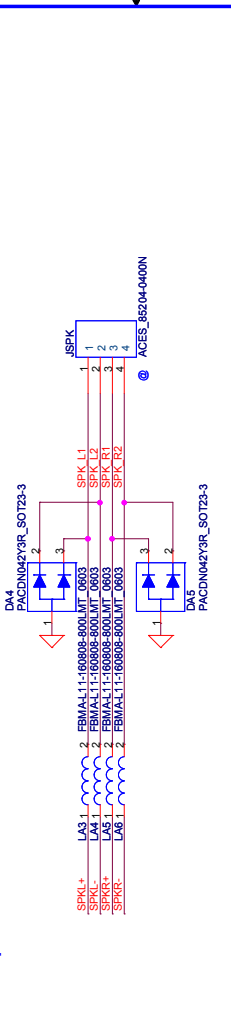


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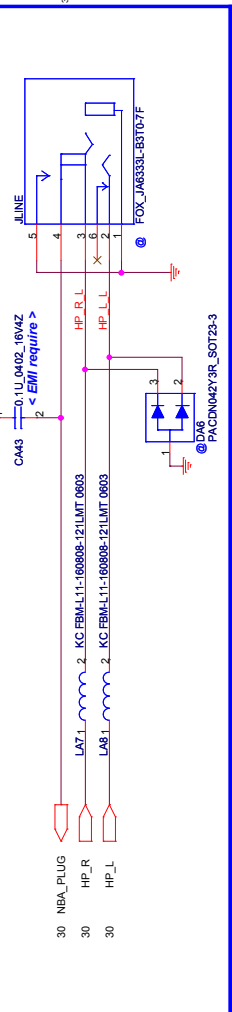


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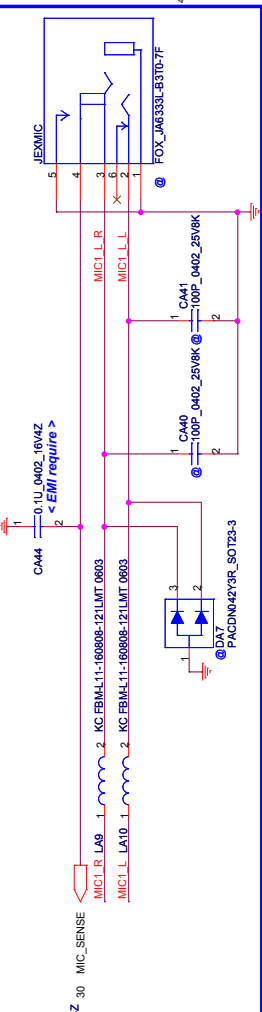
< Speaker Connector >



< HeadPhone JACK >



< Ext. MIC/LINE IN JACK >



Security Classification	2008-09-25	Deciphered Date	2009-09-25
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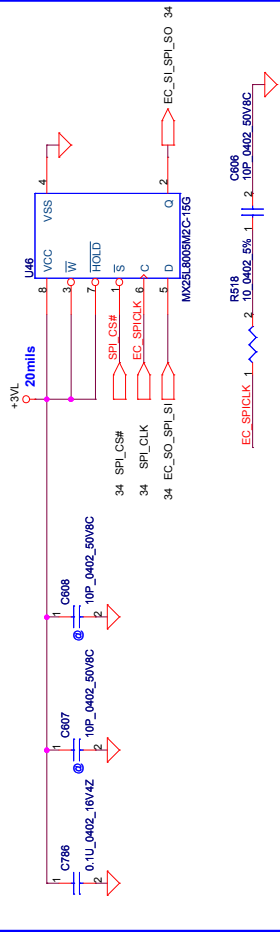
Compal Secret Data

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Title	AMP/Audio Jack/HP/SPEAKER/VR
Size	Document Number
Rev	LA-4971P
Date	Wednesday, February 25, 2009
Sheet	31 of 45

Compal Electronics, Inc.

< MDC 1.5 Conn >

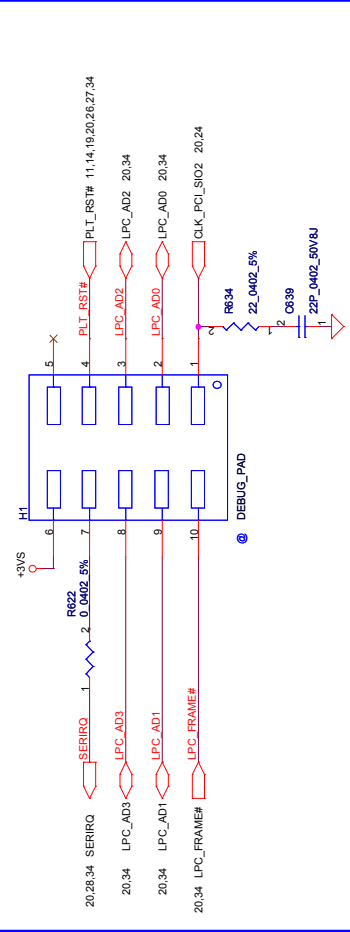


21 HDA_SDOOUT_MDC
21 HDA_SYNC_MDC
21 HDA_SDINT_MDC
21 HDA_RST#_MDC

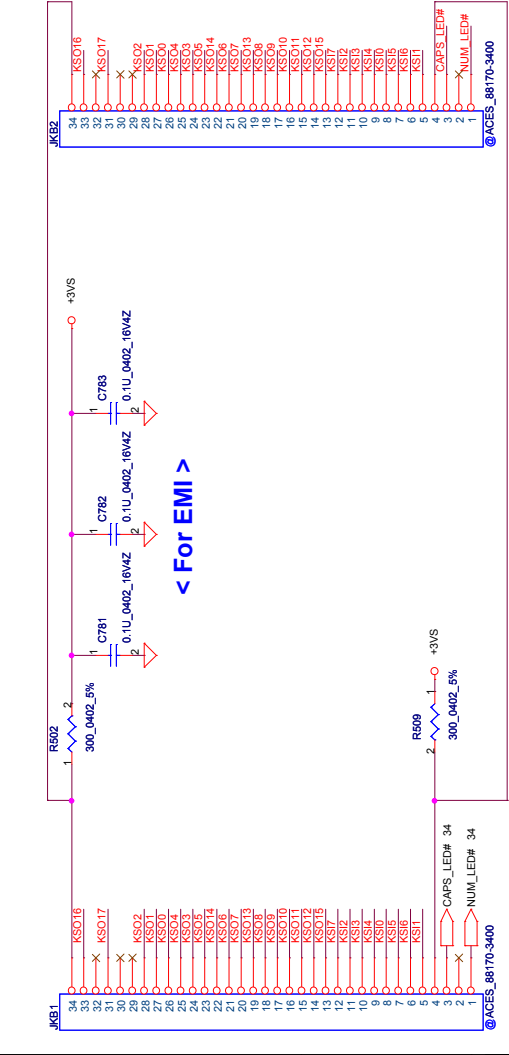
RES0
RES1 3.3V
GND1
GND2
GND3
GND4
GND5
GND6
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< LPC Debug Port >

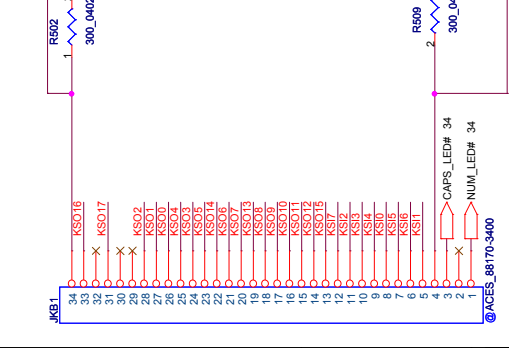
Please place the PAD under DDR DIMM.



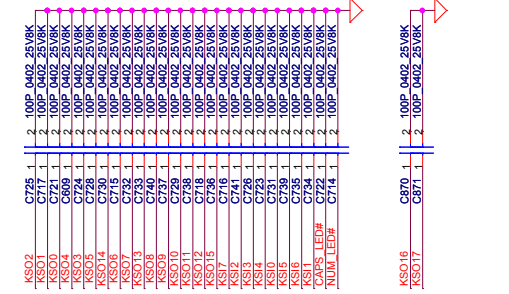
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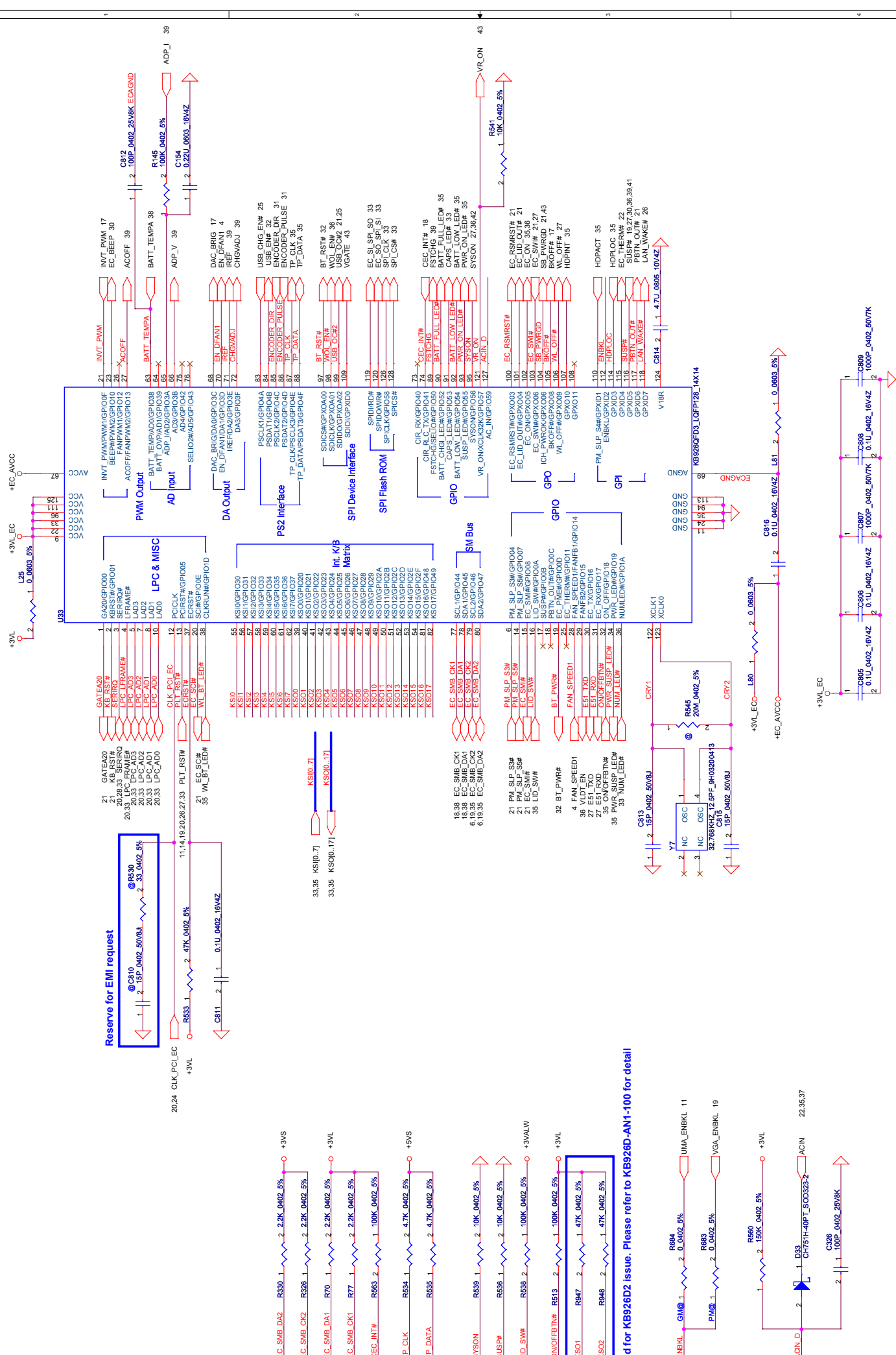


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< For EMI >





Reserve for EMI request

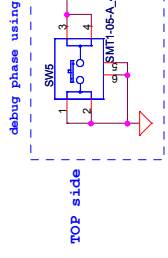
Add for KB926D2 issue. Please refer to KB926D-AN1-100 for detail

Security Classification	2008-09-25	Deciphered Date	2009-09-25
Issued Date	2008-09-25		
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<p>ENE KB926C</p>			
<p>LA-4971P</p>			
Size	Document Number	Rev	0.1
Customer	Wednesday, February 25, 2009		Sheet 34 of 48

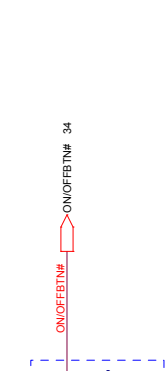
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Compal Electronics, Inc.
ENE KB926C
 LA-4971P
 Wednesday, February 25, 2009
 Sheet 34 of 48

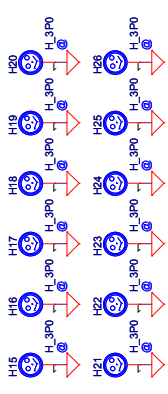
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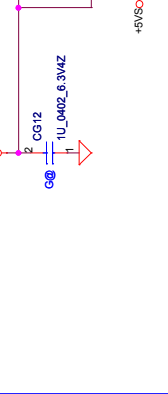
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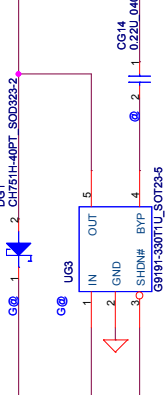
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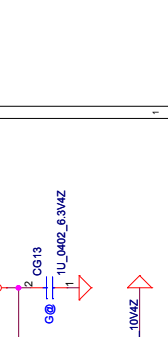
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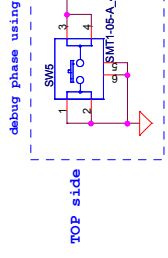
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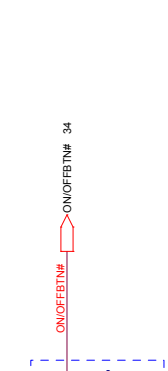
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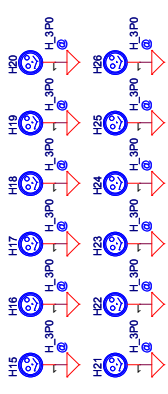
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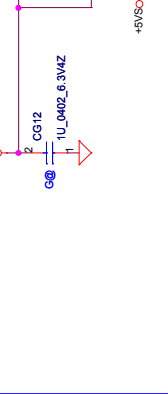
< Touch/B Connector >



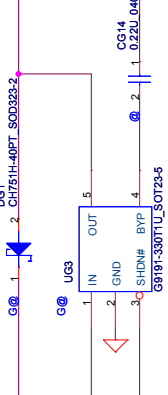
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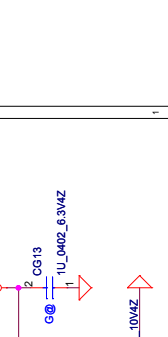
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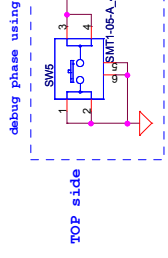
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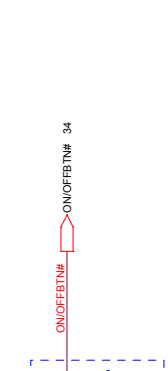
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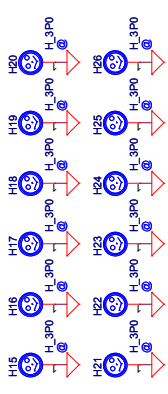
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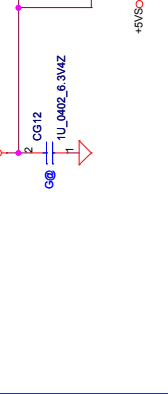
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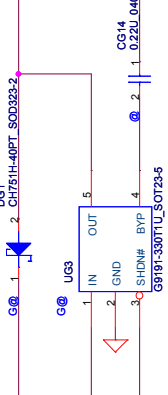
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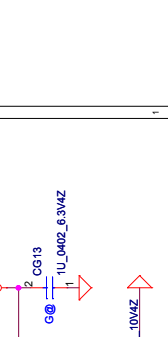
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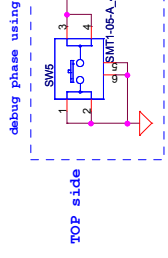
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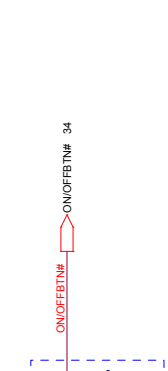
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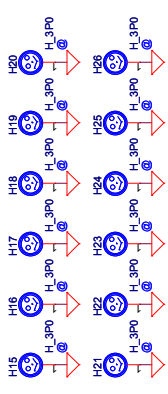
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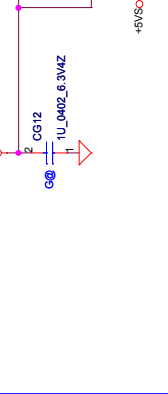
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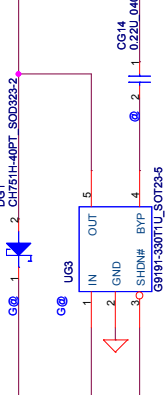
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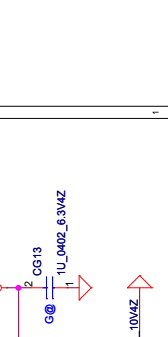
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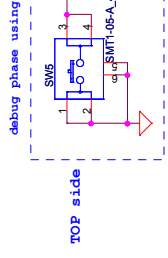
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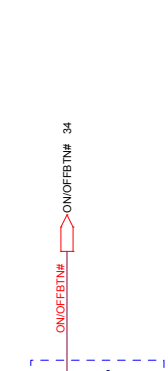
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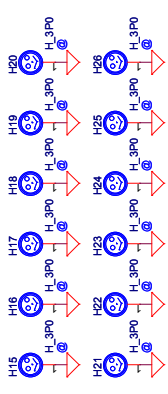
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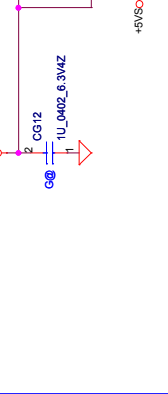
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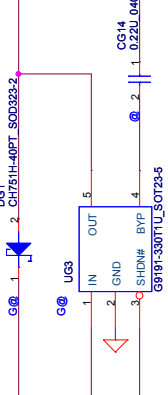
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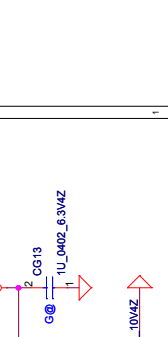
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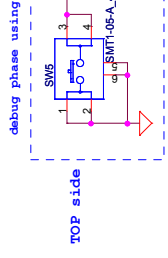
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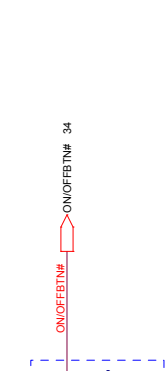
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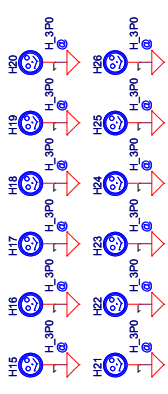
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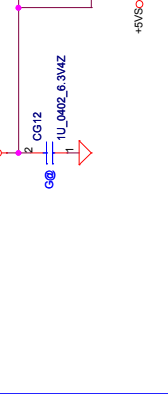
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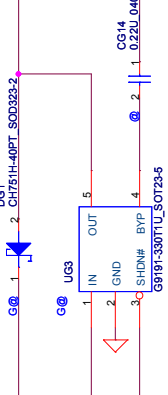
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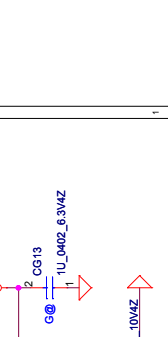
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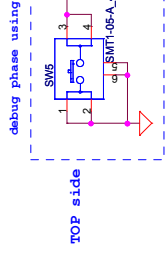
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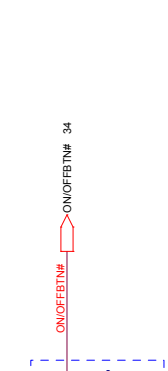
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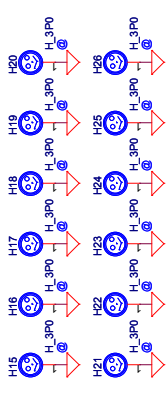
< Remove WIMAX LED control circuit >



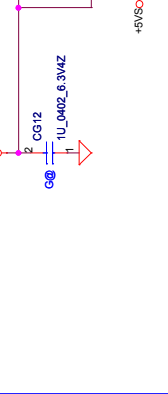
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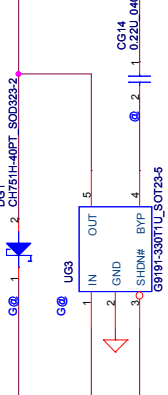
< HDD LED >



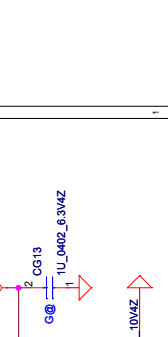
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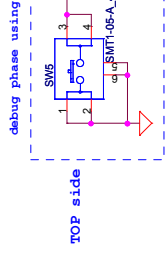
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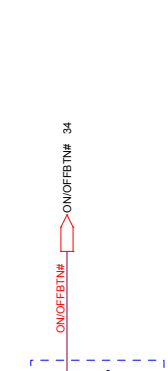
< BATT CHARGE/FULL LED >



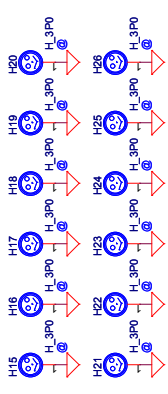
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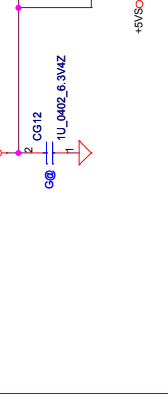
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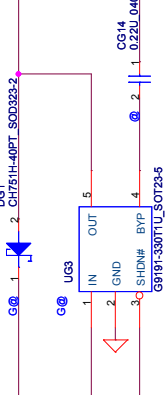
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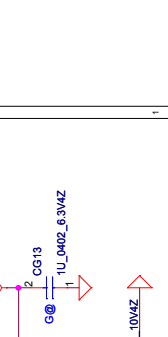
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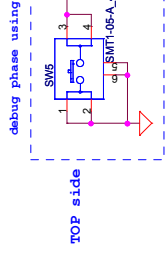
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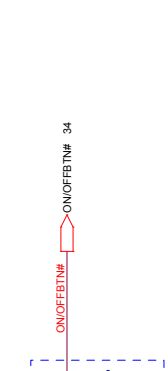
< Lid Switch >



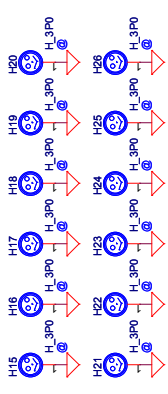
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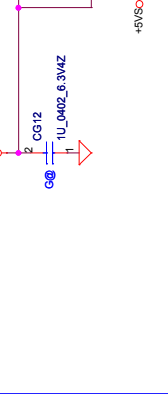
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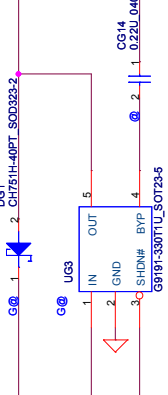
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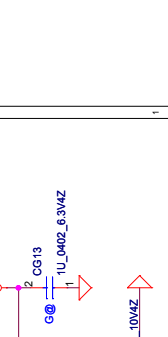
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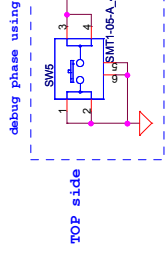
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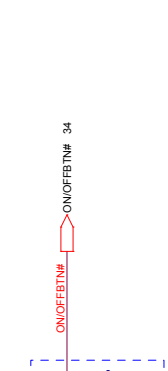
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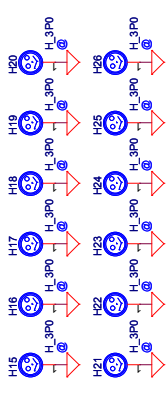
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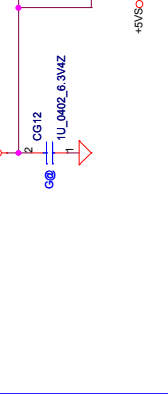
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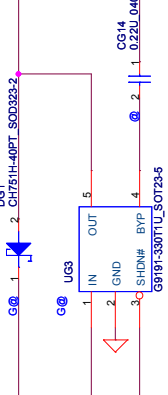
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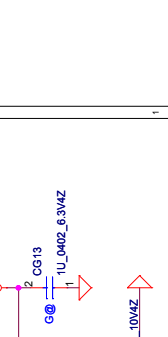
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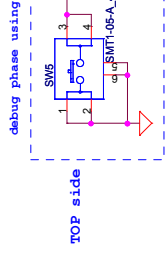
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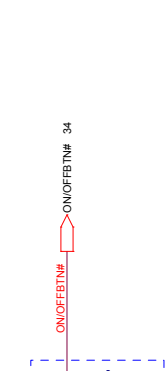
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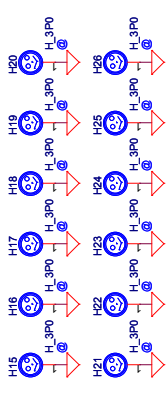
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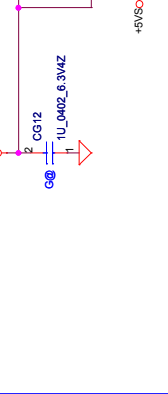
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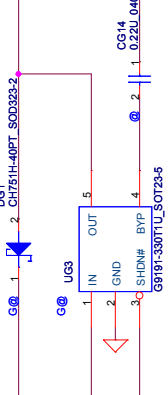
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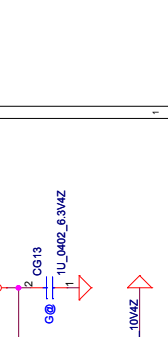
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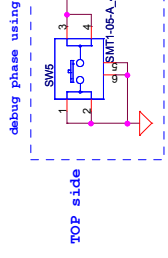
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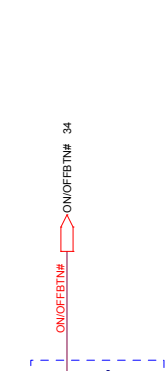
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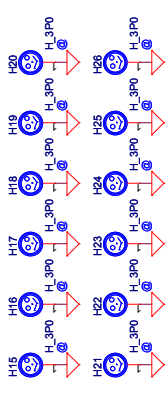
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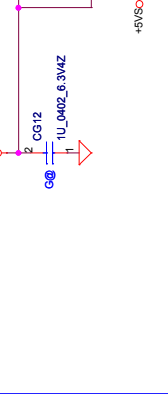
< Touch/B Connector >



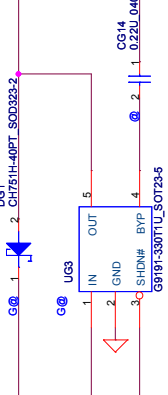
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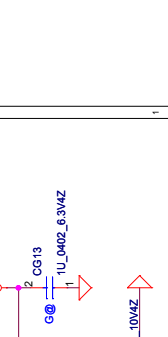
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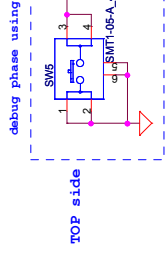
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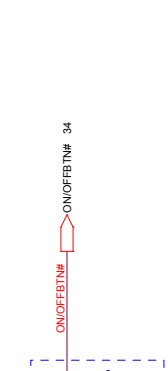
< Lid Switch >



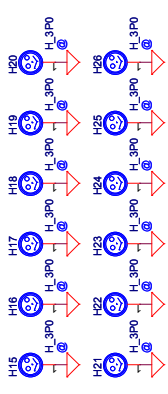
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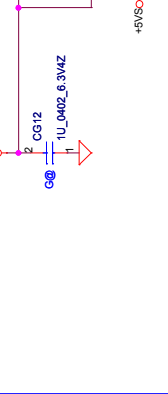
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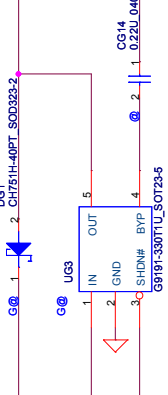
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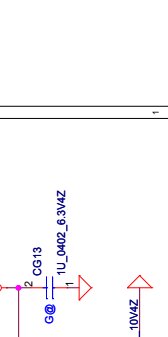
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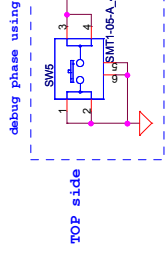
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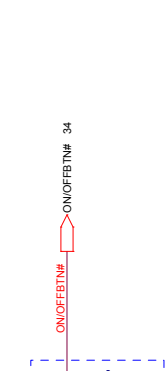
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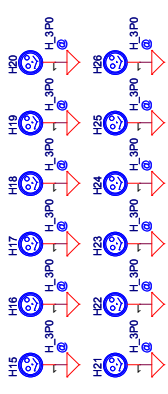
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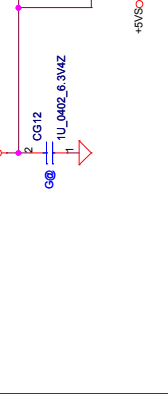
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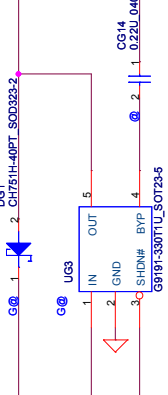
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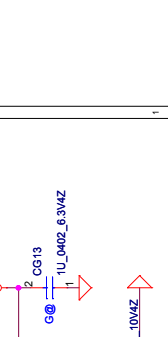
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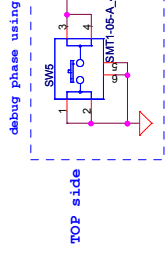
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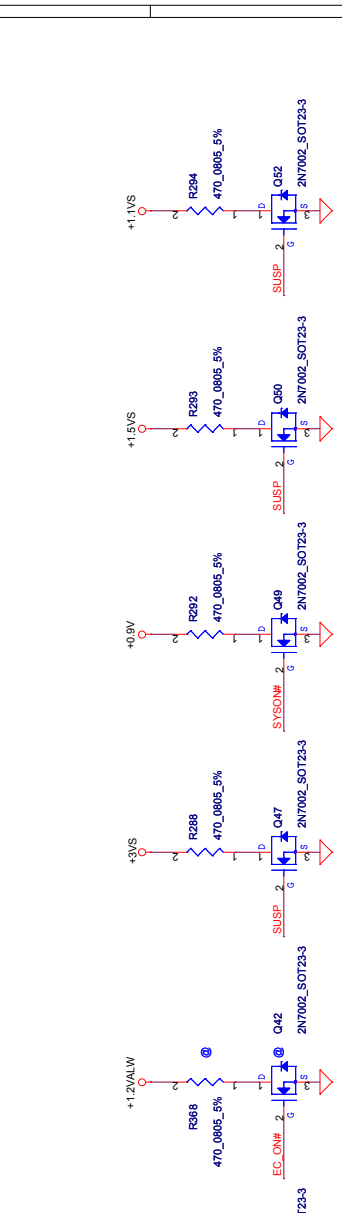
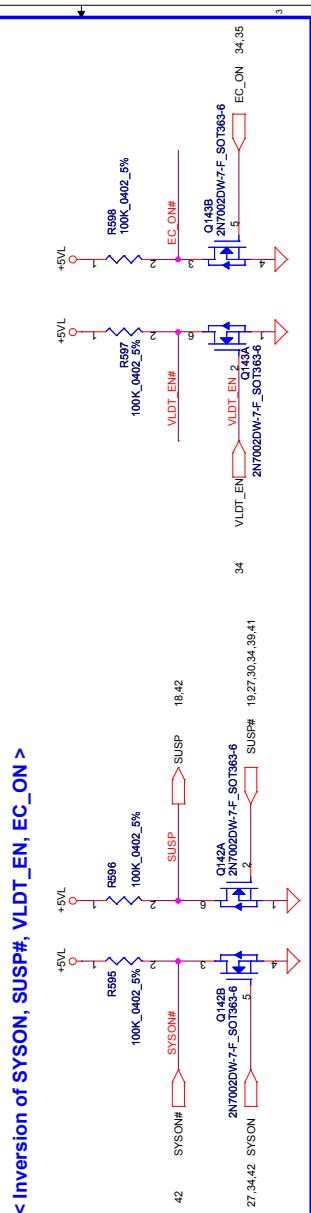
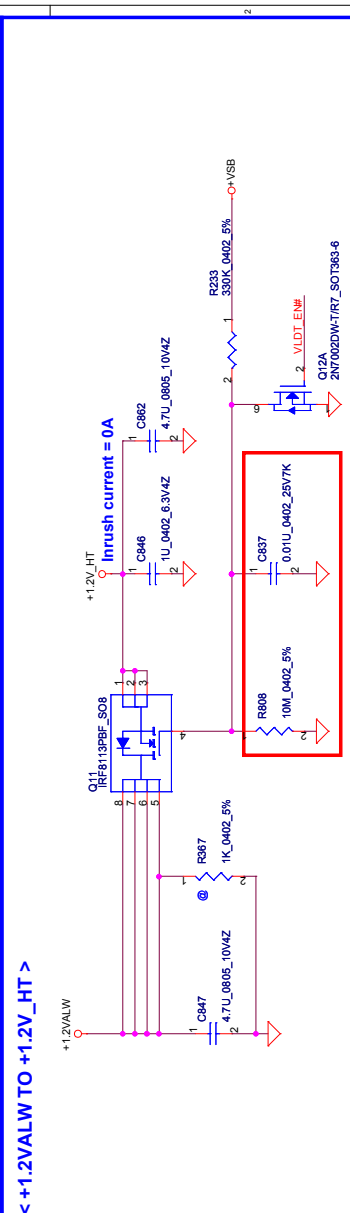
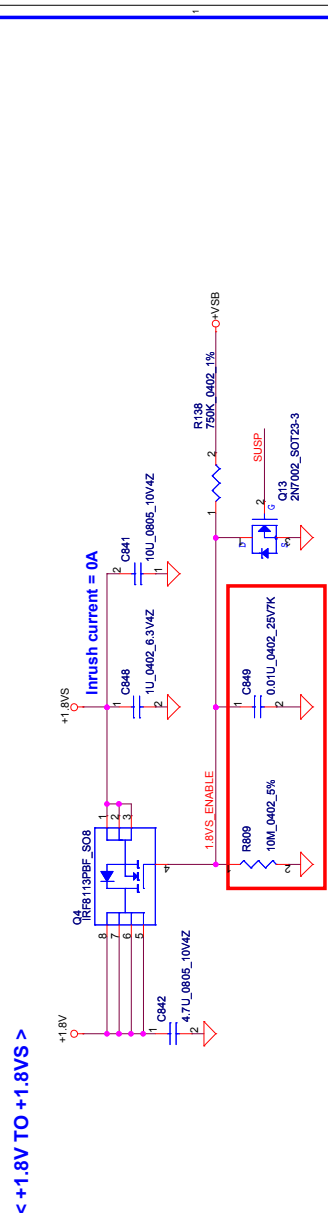
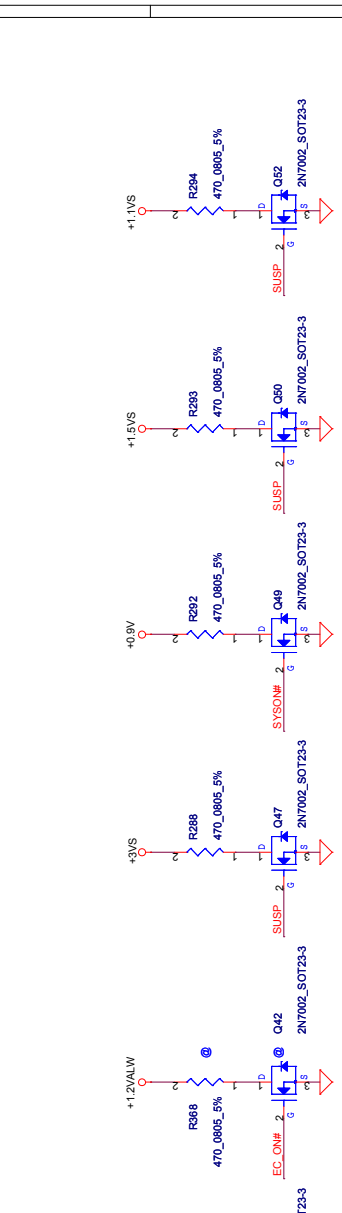
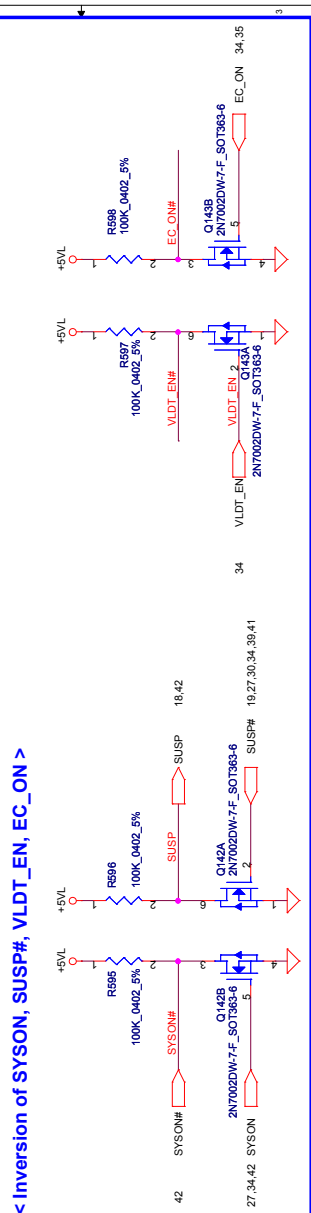
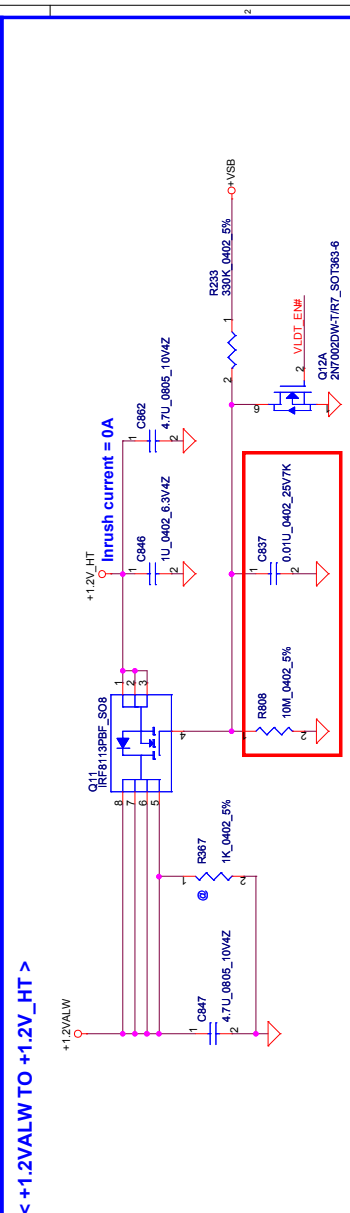
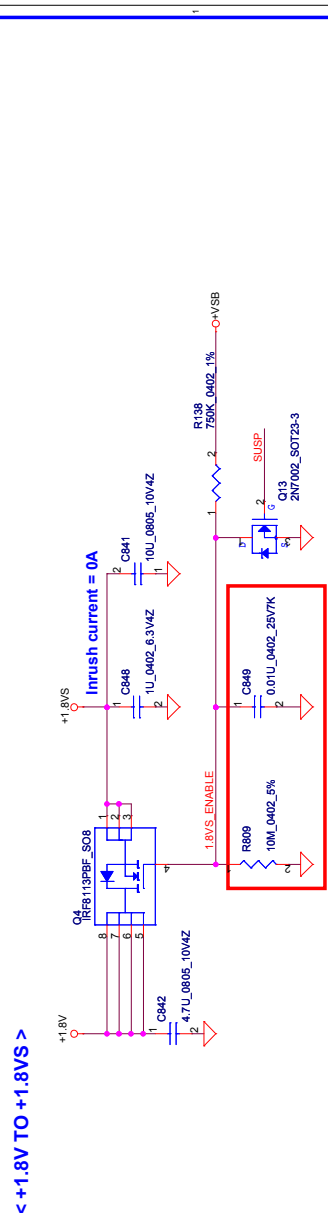
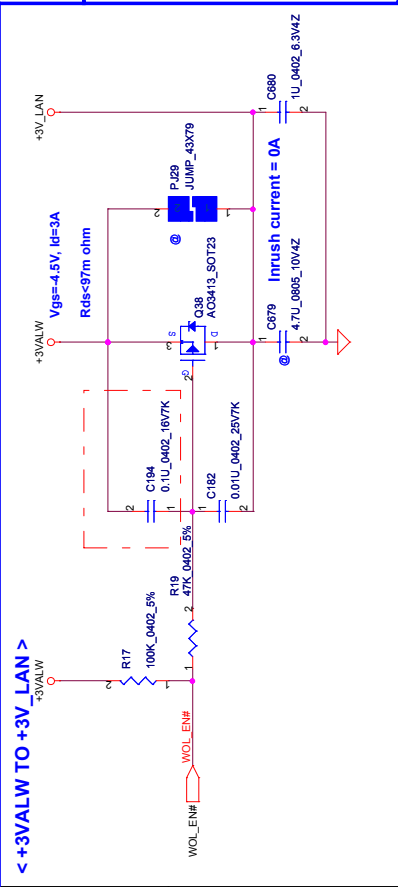
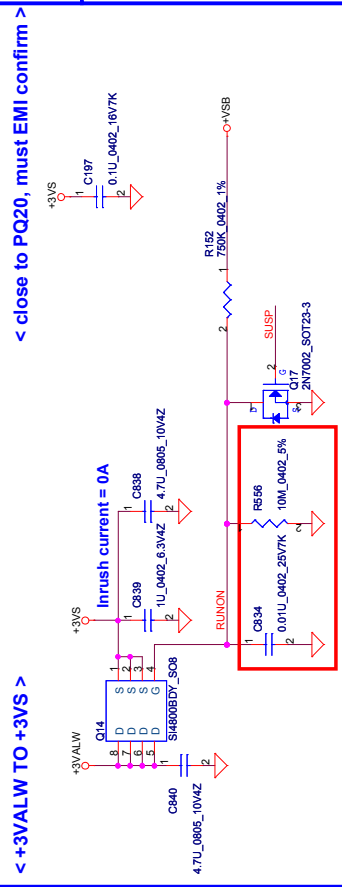
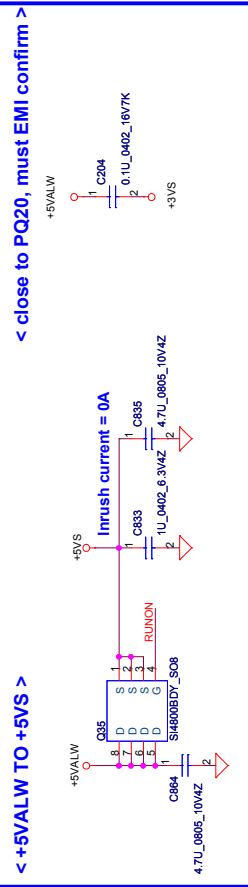


< Lid Switch >



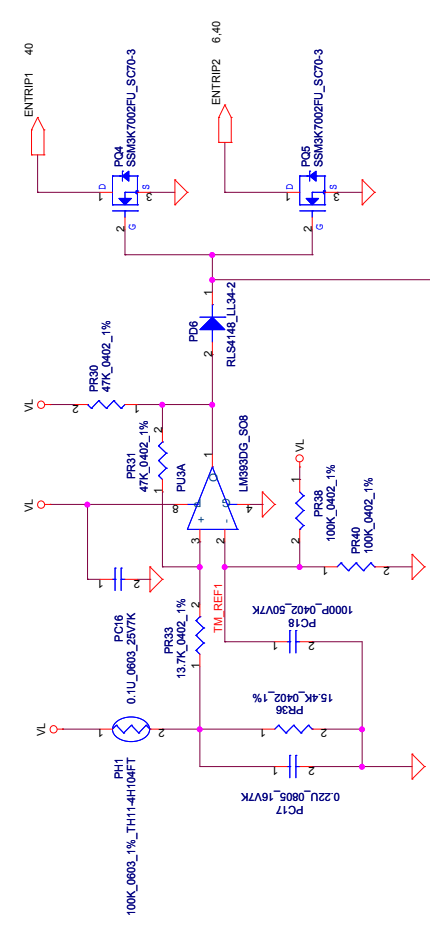
< Remove WIMAX LED control circuit >



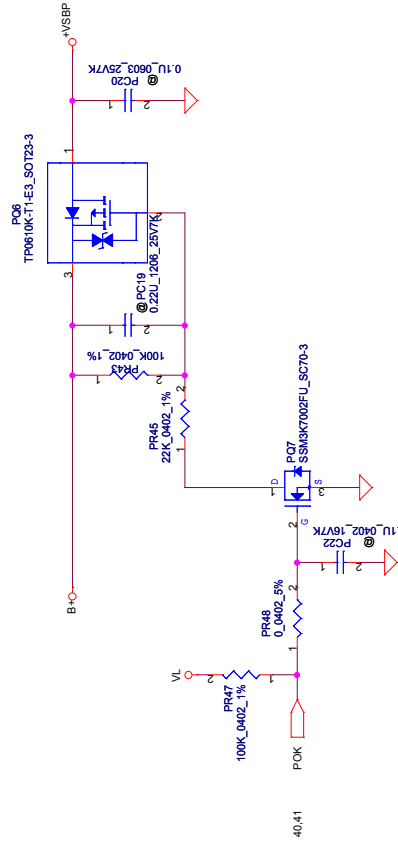
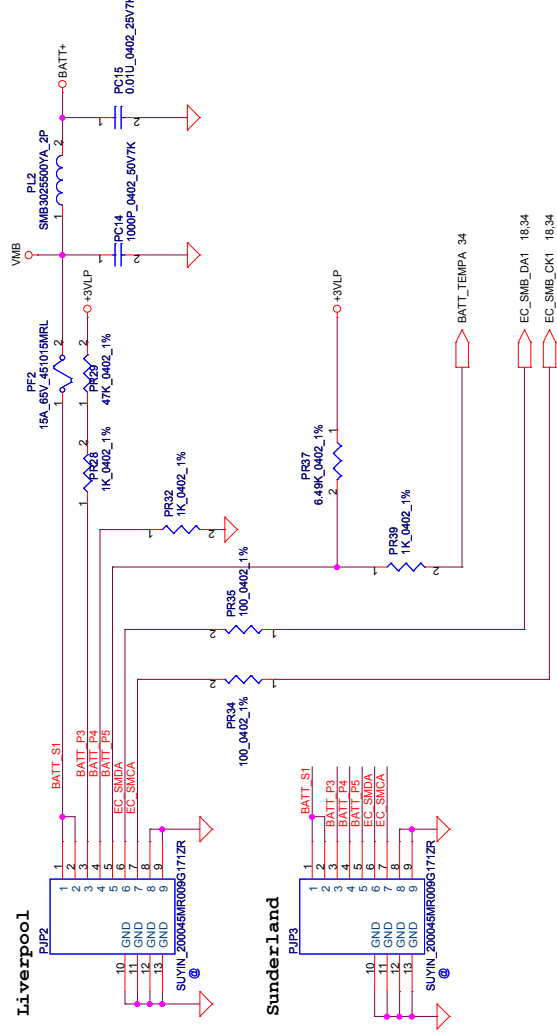
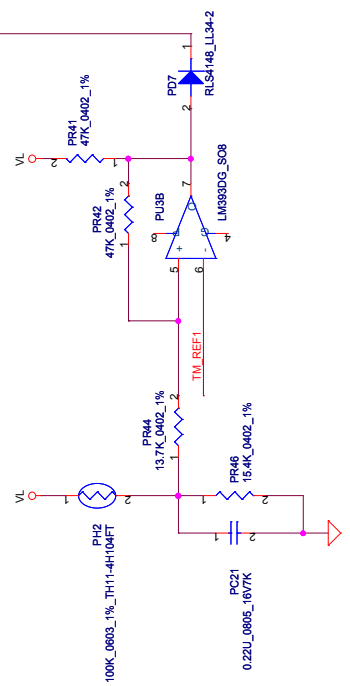


Security Classification	2008-09-25	Deciphered Date	2009-09-25
Issued Date	Title		
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Rev	0.1	Doc Number	L4-4971P
Date	Wednesday, February 25, 2009	Sheet	35 of 49

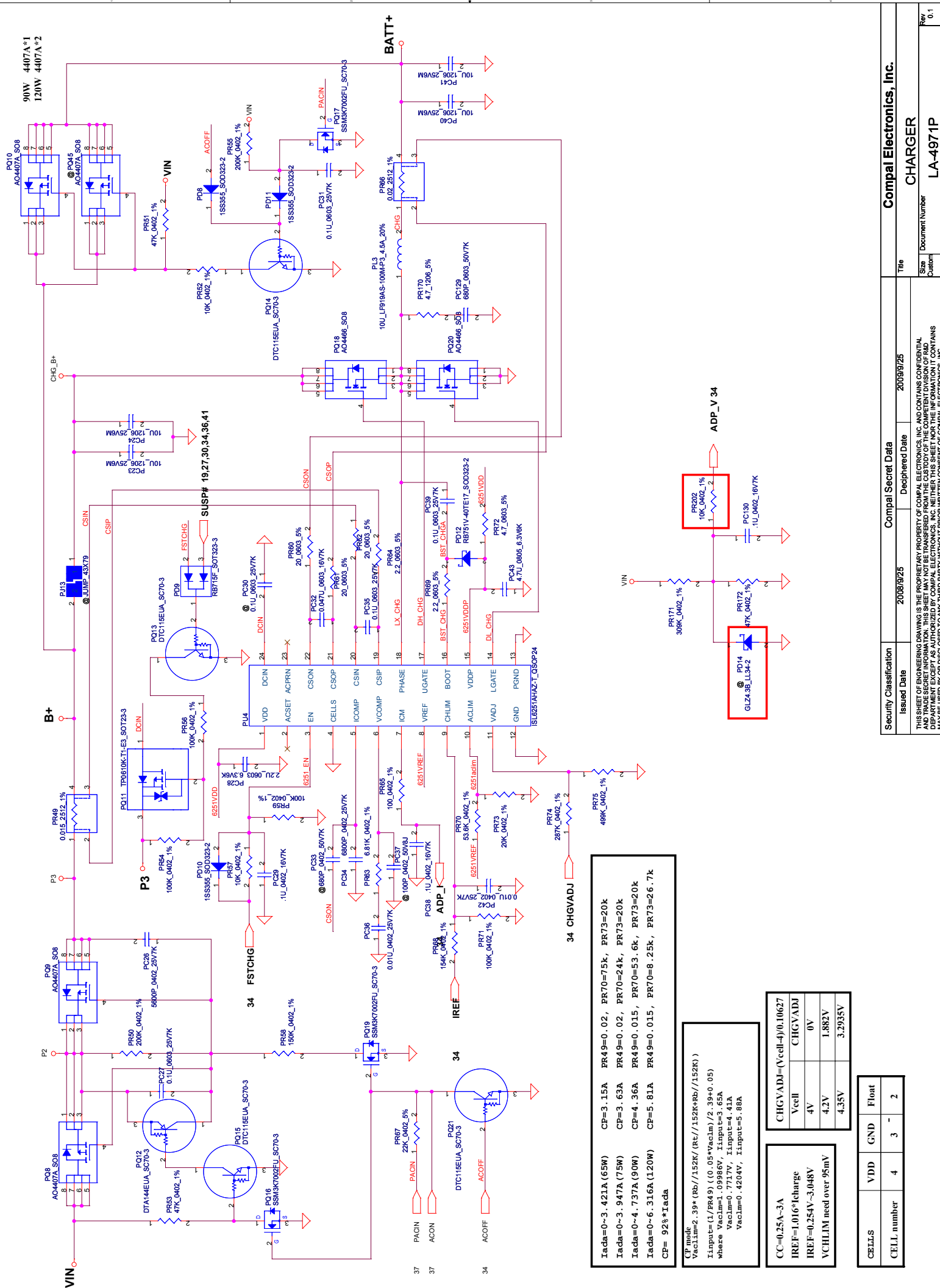
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 92 degree C
 Recovery at 56 degree C



Security Classification	2008/9/25	Compal Secret Data	2008/9/25	Dispersed Date	2008/9/25	Title	Compal Electronics, Inc.	
Issued Date	2008/9/25	Dispersed Date	2008/9/25	Dispersed Date	2008/9/25	Document Number	BATTERY CONN / OTP	
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							Size	L.A-4971P
							Date:	Wednesday, February 25, 2009
							Sheet	38 of 46



I_{ada}=0-3.421A (65W) CP=3.15A PR49=0.02, PR70=75k, PR73=20k
I_{ada}=0-3.947A (75W) CP=3.63A PR49=0.02, PR70=24k, PR73=20k
I_{ada}=0-4.737A (90W) CP=4.36A PR49=0.015, PR70=53.6k, PR73=20k
I_{ada}=0-6.316A (120W) CP=5.81A PR49=0.015, PR70=8.25k, PR73=26.7k
CP= 92% *I_{ada}

CP mode
 Vac_{lim}=2.39*(Rb/152k)/(Rt/152k+Rb/152k)
 I_{in}=(1/PR49)*(0.05*Vac_{lim})/2.39+0.05
 where Vac_{lim}=1.09986V, I_{in}=3.65A
 Vac_{lim}=0.7717V, I_{in}=4.41A
 Vac_{lim}=0.4204V, I_{in}=5.88A

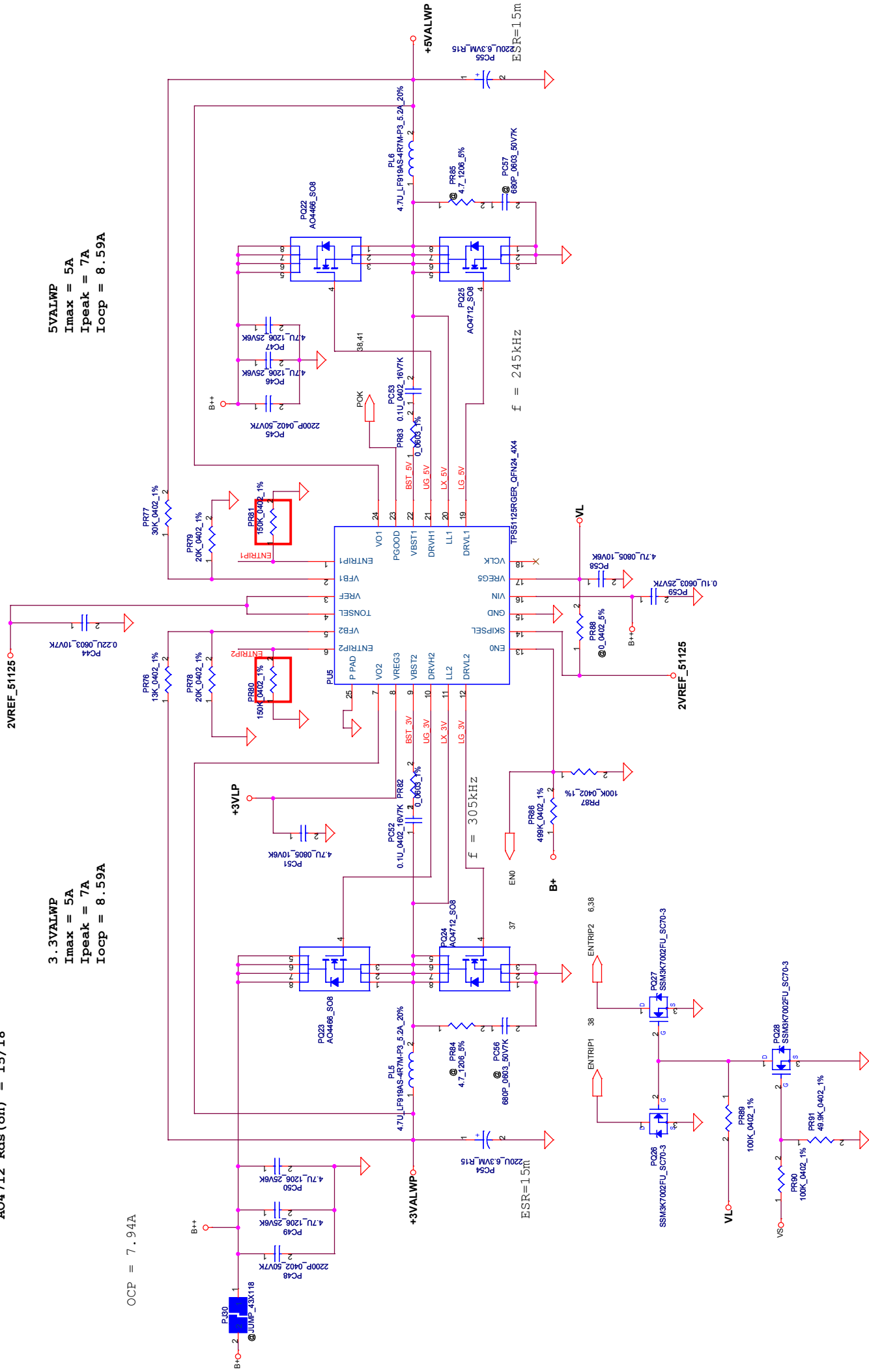
CC=0.25A-3A	CHGVADJ=(V _{cell} -0)/0.10627
IREF=1.016*Icharge	V _{cell} CHGVADJ
IREF=0.254V-3.048V	4V 0V
VCHLIM need over 95mV	4.2V 1.882V
	4.35V 3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

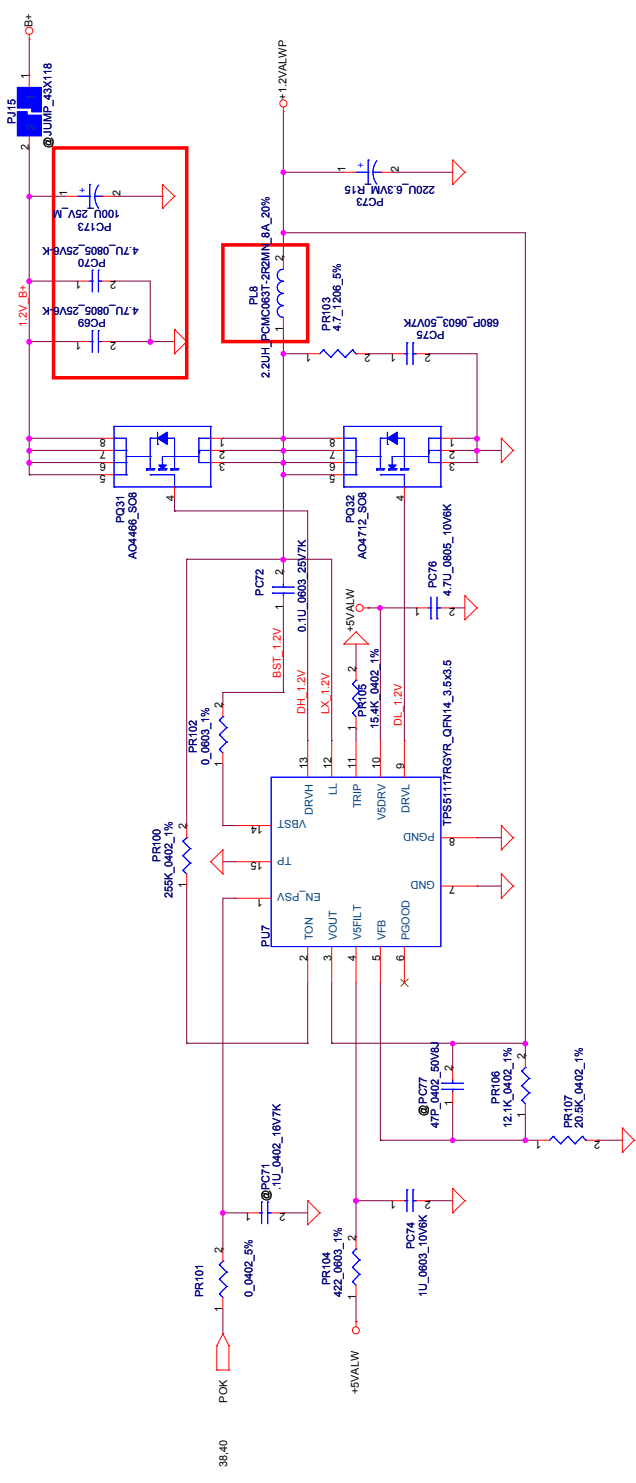
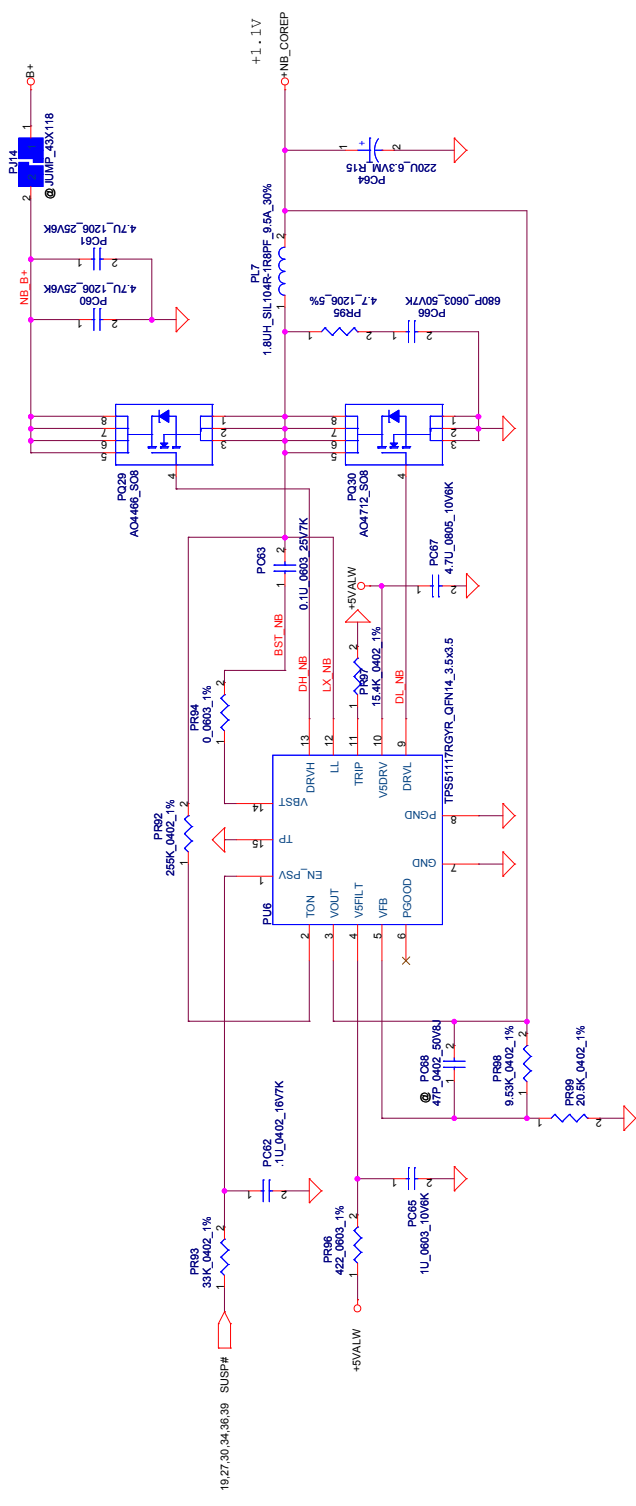
3.3VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A

5VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A

OCP = 7.94A

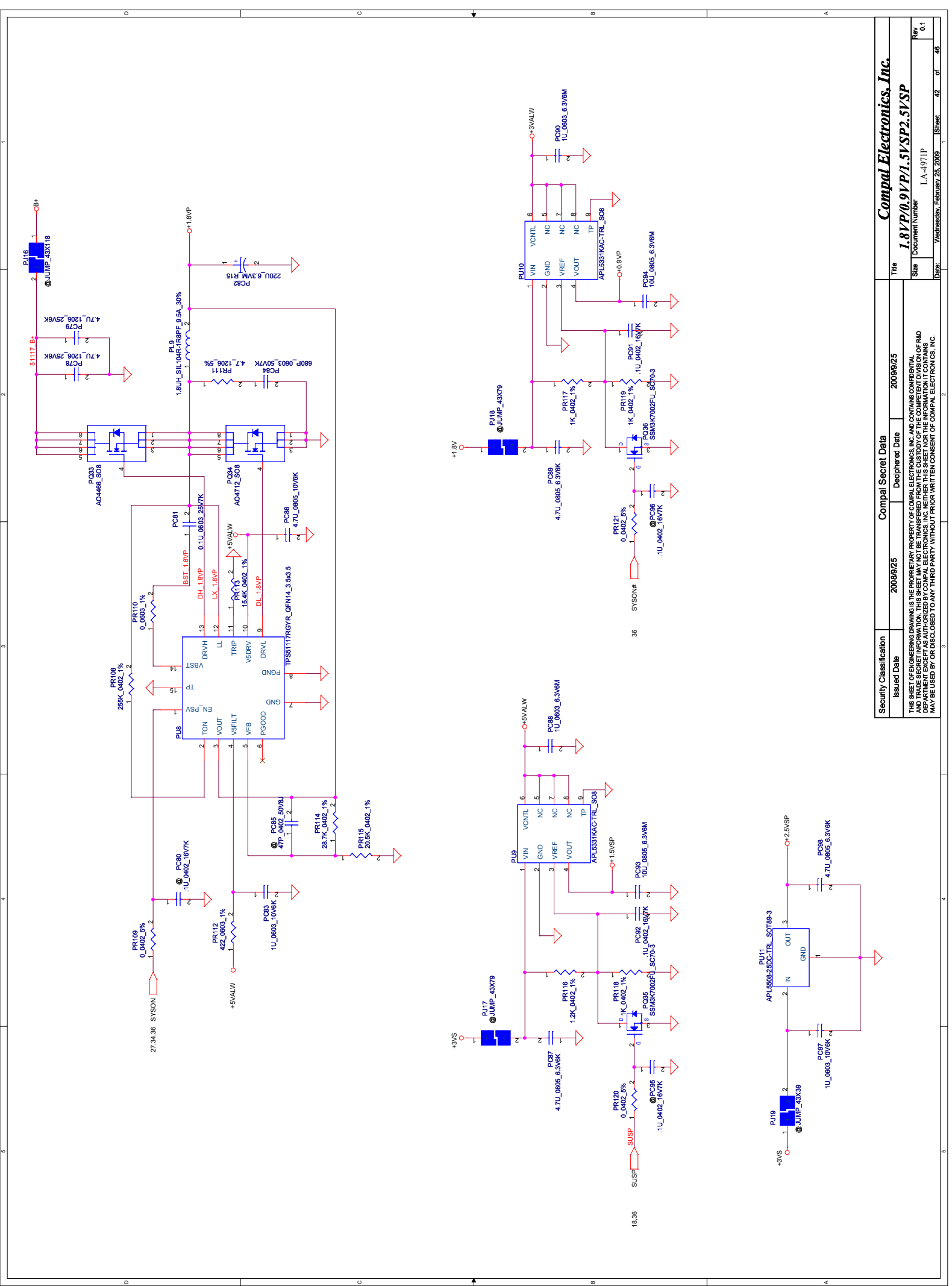


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Title	3VALWP/5VALWP		
Size	Document Number	L.A-4971P	
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Issued Date	2008/5/25	Deciphered Date	2009/9/25
Title			
NB COREP/1.2VALLWP			
Size	Document Number	1.A-4971P	Rev
0.1			0.1
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Title	1.8VP/0.9VP/1.5VSP2.5VSP		
Size	Document Number 1.A-4971P		
Rev	0.1		
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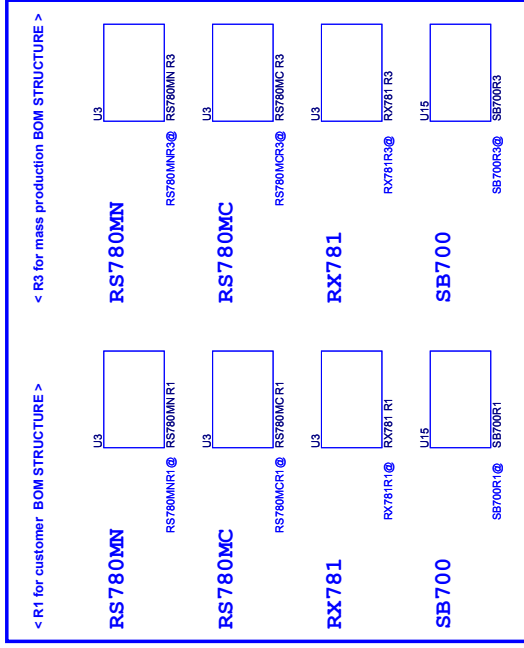
Version Change List (P. I. R. List) for Circuit

Item Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	2008/11/29	→ change SLP_CHG to SLP_CHG#			57. 2009/02/09 → change UG1's Value from TIS555AL3TR to TSH85TR	
2.	2008/12/29	→ change HDMI_SCLK and HDMI_SDATA path circuit (add two MOSFETs)			58. 2009/02/09 → change UL3's P/N to SP050005V00	
3.	2008/12/29	→ connect HDPINT to pin 107 of EC, HDPACT to pin 110 of EC			59. 2009/02/09 → change R489 & R488 BOM structure	
4.	2008/12/29	→ Change 2nd source of G-sensor to new part			60. 2009/02/09 → change R142 from 300 ohm to 150 ohm	
5.	2008/12/29	→ Change +3VALW to +3V_LAN soft-start circuit (R=4.7K ohm, C=0.1uF)			61. 2009/02/09 → change R143 from 1M ohm to 100K ohm	
6.	2008/12/29	→ Change +BT_VCC circuit (change BT_PWR from high active to low active in pin19 of EC)			62. 2009/02/09 → change JREAD footprint to TAITW_R009-125-LR_21P_RV-T	
7.	2008/12/29	→ Change +LCD_VDD circuit (change +3VALW to +3VS(R143) and add 0.1uF cap to +3VS)			63. 2009/02/09 → change C867 from 0.1u_0603 to 680pF_0402	
8.	2008/12/29	→ add pull-down resistor R146 to BKOFF# to prevent backlight flash when power down			64. 2009/02/09 → change +HDMI_5V_OUT circuit, add D18, R160, Q26, R557, C876 and change power	
9.	2008/12/29	→ connect SHDN# of UG3 to +5VS and remove EC_HDPPD			65. 2009/02/11 → change UG1 P/N to SA000039900	
10.	2008/12/29	→ connect PD of UG1 to GND and remove EC_HDPPD			66. 2009/02/12 → change CV2 to C706	
11.	2008/12/29	→ Let OG-DET of UG4 float			67. 2009/02/12 → change PCMCIA connector	
12.	2008/12/29	→ connect SLEEP# to +3VS_HDP and remove EC_HDPPD			68. 2009/02/12 → remove WIMAX LED control circuit	
13.	2008/12/29	→ Connect G-SELECT to GND			69. 2009/02/17 → remove Audio codec digital GND to analog GND net	
14.	2008/12/29	→ Connect pin10 of UG2 to GND and remove HDPPD			70. 2009/02/17 → add NPTH Hole H41, H42	
15.	2008/12/29	→ Add HDPLOC to pin14 of UG2			71. 2009/02/17 → change JTOUCH footprint	
16.	2008/12/29	→ Change pin99 of EC from EC_HDPPD to USB_OC#2 and remove EC_HDPPD			72. 2009/02/17 → add CA12	
17.	2008/12/29	→ Change pin107 of EC to HDPINT			73. 2009/02/17 → change Int MIC ground to AGND between CA27 and J3	
18.	2008/12/29	→ Change pin110 of EC to HDPACT			74. 2009/02/17 → add JPOWER1 for co-lay	
19.	2008/12/29	→ Change pin114 of EC from USB_OC#2 to HDPLOC			75. 2009/02/17 → change NEWCARD power switch (UN1) to TI SA00001SL20	
20.	2008/12/29	→ add R689			76. 2009/02/17 → add CA45, CA46, CA47, CA48, CA49, CA50, CA51, CA52, CA53	
21.	2009/01/13	→ change the footprint of L47, L48 and L49 to R_0402			77. 2009/02/17 → replace RA12, RA13, RA14 with CA54, CA55, CA56 and add CA57	
22.	2009/01/19	→ add differential clock name CLK_CPU_BCLK_R & CLK_CPU_BCLK_R#			78. 2009/02/23 → change R70, R77 from 4.7K to 2.2K	
23.	2009/01/19	→ change 3 in 1 card reader connector to push-pull type			79. 2009/02/23 → change R178 from 4.7K to 47K	
24.	2009/01/19	→ change the pin158 of MXM connector from GND to NC			80. 2009/02/28 → change SPI ROM from SST to MXIC	
25.	2009/01/19	→ add BOM structure of C1, C2 and C7 for Tigris				
26.	2009/01/19	→ add R486, R487, R488, R489 & R27 for Tigris				
27.	2009/01/19	→ add R497, R498, R499, R500 for Tigris				
28.	2009/01/19	→ add R29, R31 & R32 for Tigris				
29.	2009/01/19	→ add C54 for Tigris				
30.	2009/01/19	→ add R187 for Tigris				
31.	2009/01/19	→ change RL2 from 10Kohm to 1Kohm suggested by vendor				
32.	2009/01/19	→ change CL14 from 0.1uF to 1uF suggested by vendor				
33.	2009/01/19	→ change RL4 from 100Kohm to 10Kohm suggested by vendor				
34.	2009/01/19	→ remove kill switch and add R87				
35.	2009/01/21	→ add card reader BTO				
36.	2009/01/21	→ change Q33, Q34, Q139 & Q140 symbol				
37.	2009/01/22	→ add +1.8V to CPU_VDD1_RUN_FB_L for Tigris platform (add PR173 10K unmount)				
38.	2009/01/22	→ add jump PJ20, PJ21 to connect +CPU_CORE_0 and +CPU_CORE_1 for Tigris platform (add PJ20, PJ21)				
39.	2009/01/22	→ remove PR148, PR153, PR154, PR158, HW already reserves these components				
40.	2009/01/22	→ PU1 VCC issue, VCC later than input signals results in output pin drop (connect N1 to PU1 VCC)				
41.	2009/02/02	→ add C182, C195, C196 for soft-start, change R441 to 47K ohm, change R19 to 47K ohm, change R140 to 47K ohm				
42.	2009/02/02	→ change BT_PWR from +5VS to +3VS(R432)				
43.	2009/02/02	→ remove kill SW component, delete KILL_SW# on EC, connect WL_OFF# to JWLAN pin20 directly.				
44.	2009/02/02	→ change +HDMI_5V_OUT circuit				
45.	2009/02/03	→ change DA3-DA7 to SCA00000G00				
46.	2009/02/03	→ change JREAD from TAITW_R009-135-LR_21P_RV-T to TAITW_R009-125-LR_RV				
47.	2009/02/03	→ add J3 in Int-MIC				
48.	2009/02/04	→ change USB port of New card from port11 to ports				
49.	2009/02/04	→ modify HDMI_CEC power & related circuit.				
50.	2009/02/05	→ add 3PCS Cap.=0.1uF_0402 (PC136 to PC138) on B+				
51.	2009/02/05	→ add snubber circuit : PR155, PR141, PR111, PR103, PR95, PR170; PC119, PC113, PC84, PC75, PC66, PC129				
52.	2009/02/05	→ change PR74 to 287K, PR75 to 499K				
53.	2009/02/05	→ add C197 on +3VS and close to PQ20 (Place EMI confirm)				
54.	2009/02/05	→ add C204 between +3VS with +5VALW and close to PQ20 (Place EMI confirm)				
55.	2009/02/05	→ add D76, R966, R965 on LPC_FRAME#				
56.	2009/02/09	→ change UG3				

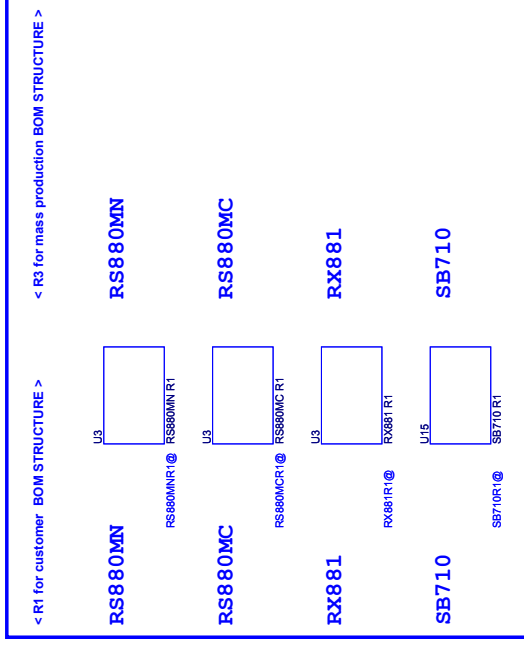
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<p>Compel Electronics, Inc. List History</p>				Size	0.1
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HW4 Product Improvement Record (P.I.R.)

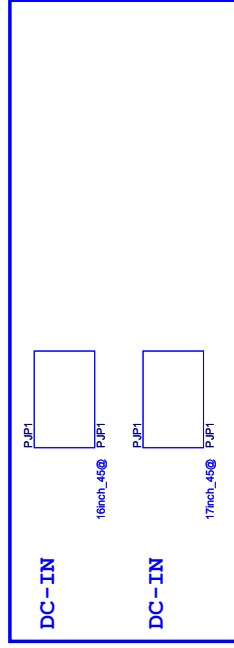
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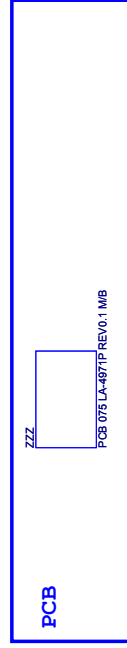
< Tigris >



< DC Jack >



< PCB >



Use MEMO : change UG1 R5F211B4D31SP (SA000037Y60) to R5F211B4D34SP (SA00003A600)

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