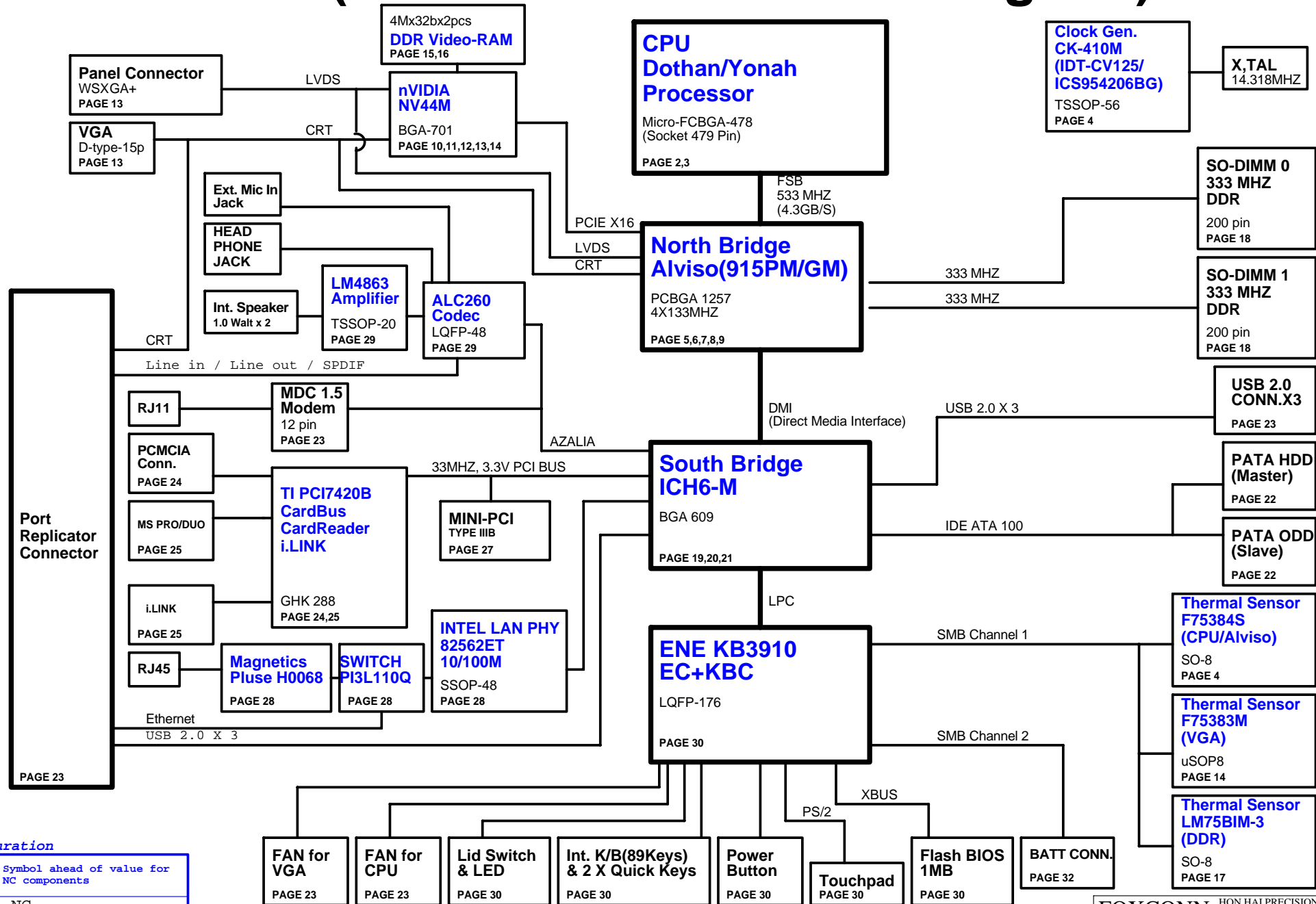
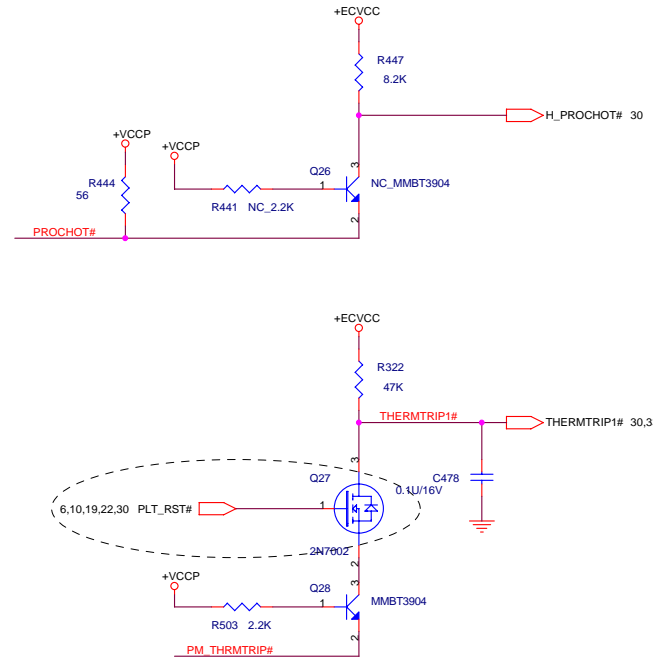
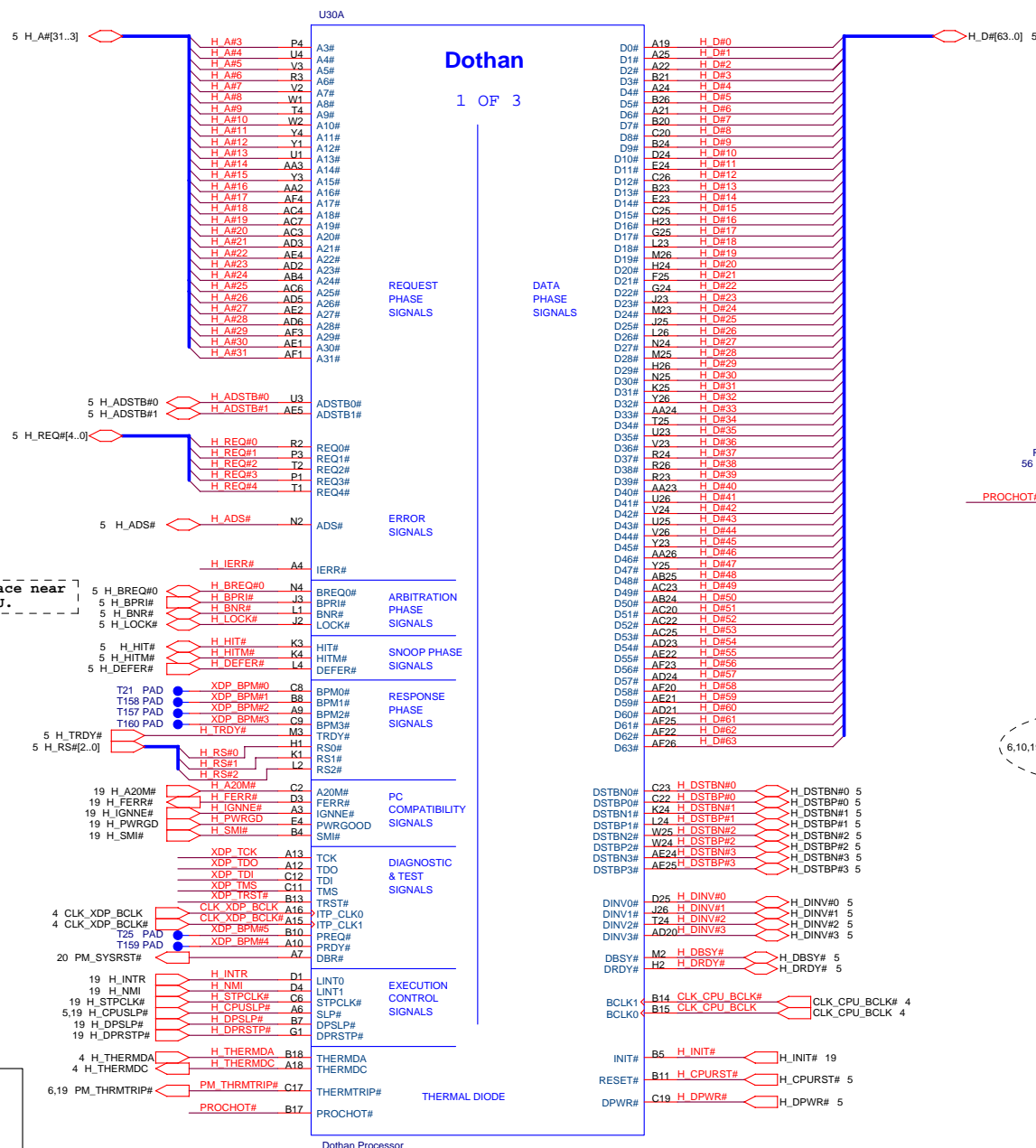


MS01(915PM/GM+Gfx Block Diagram)



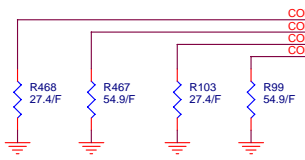
BOM configuration

	Symbol ahead of value for NC components
BOTH	NC_
915GM + NV44M	AL_
915GM	NV_

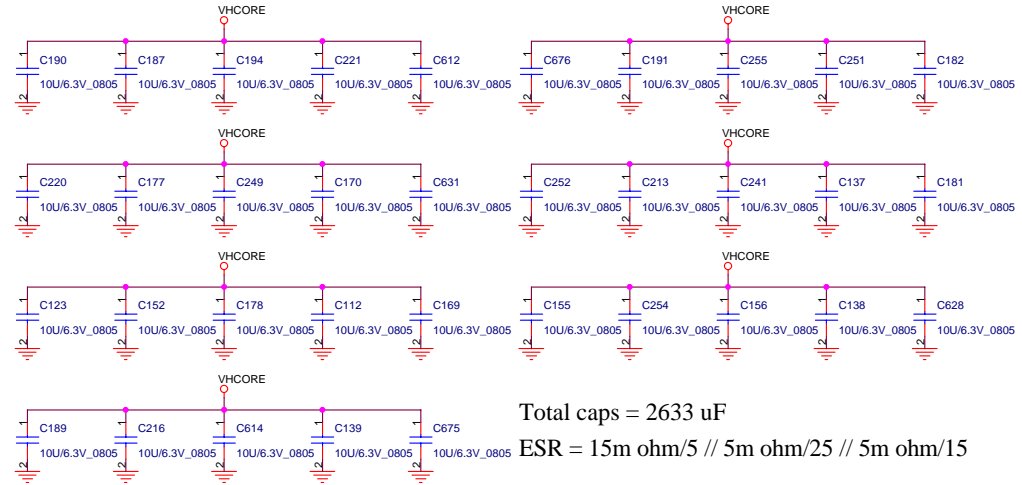
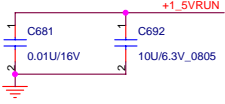
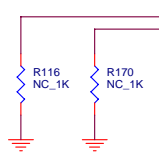


Place near CPU.

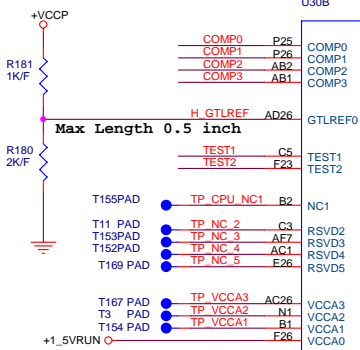
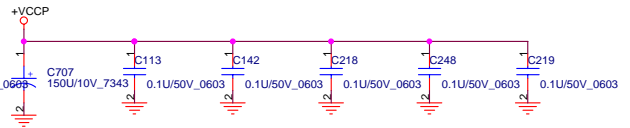
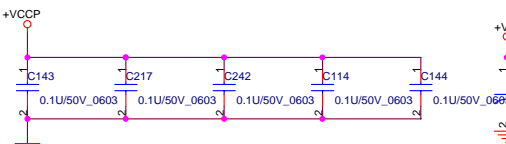
PM_THRMTRIP# should connect to ICH6-M and ALVISO without T-ing (No stub)



Place pull-down resistors within 0.5" of COMP pins

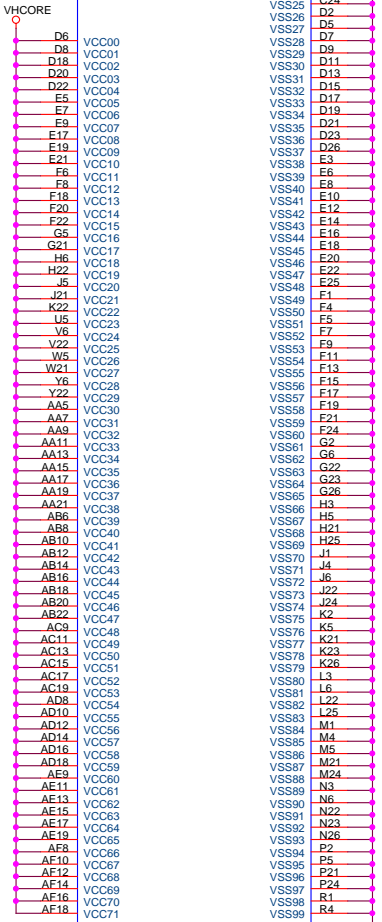


Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15

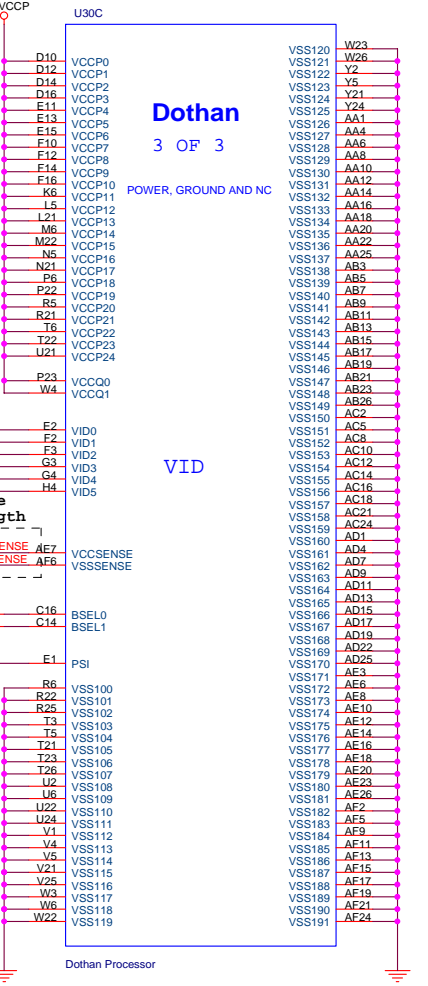
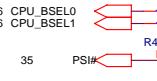
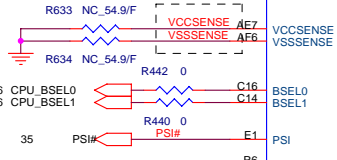


Dothan
2 OF 3

POWER, GROUND, RESERVED SIGNALS



Same Length



Dothan
3 OF 3

POWER, GROUND AND NC

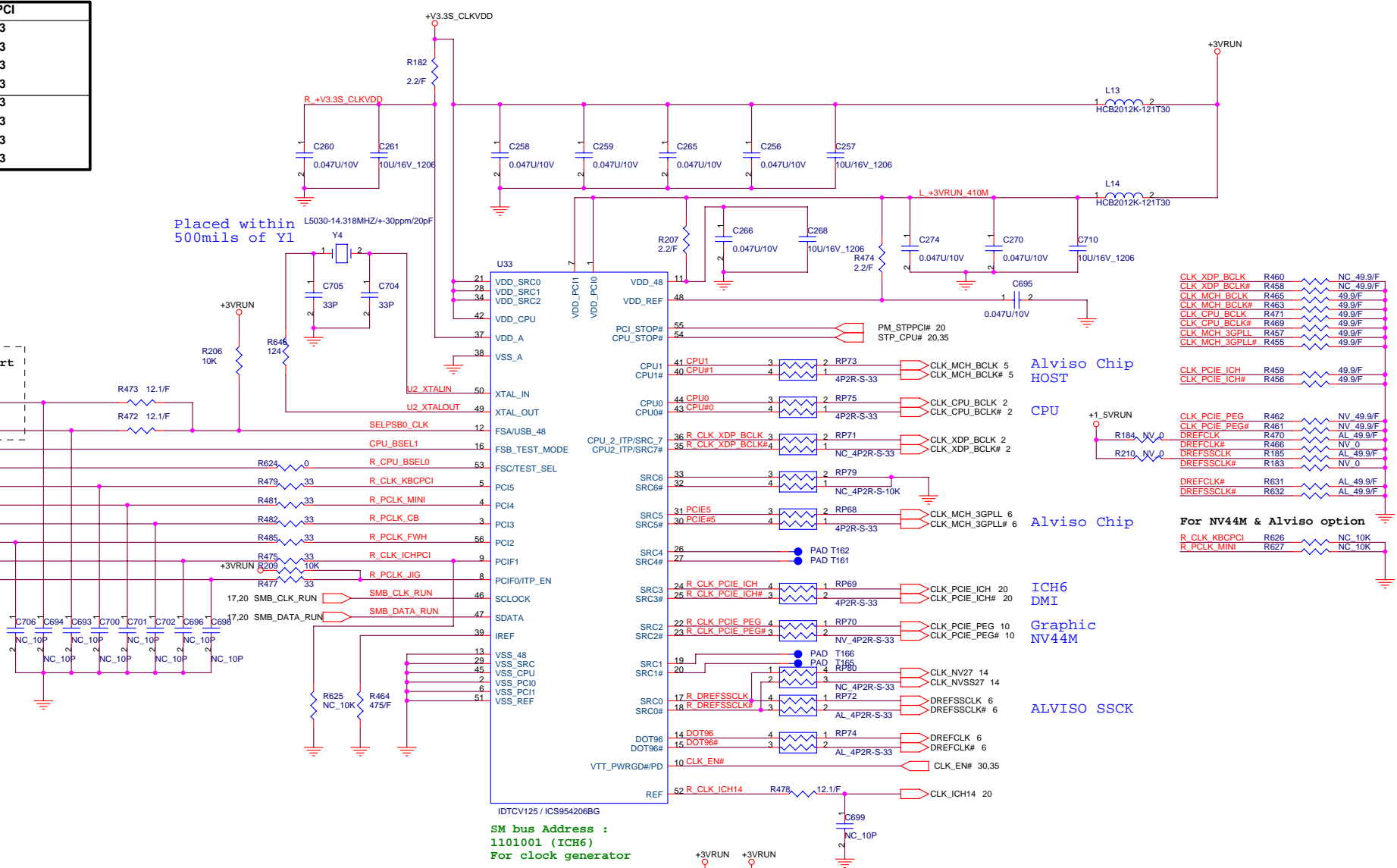
VID

Dothan Processor

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Length as short as possible.

Placed within 500mils of Y1



SM bus Address :
1101001 (ICH6)
For clock generator

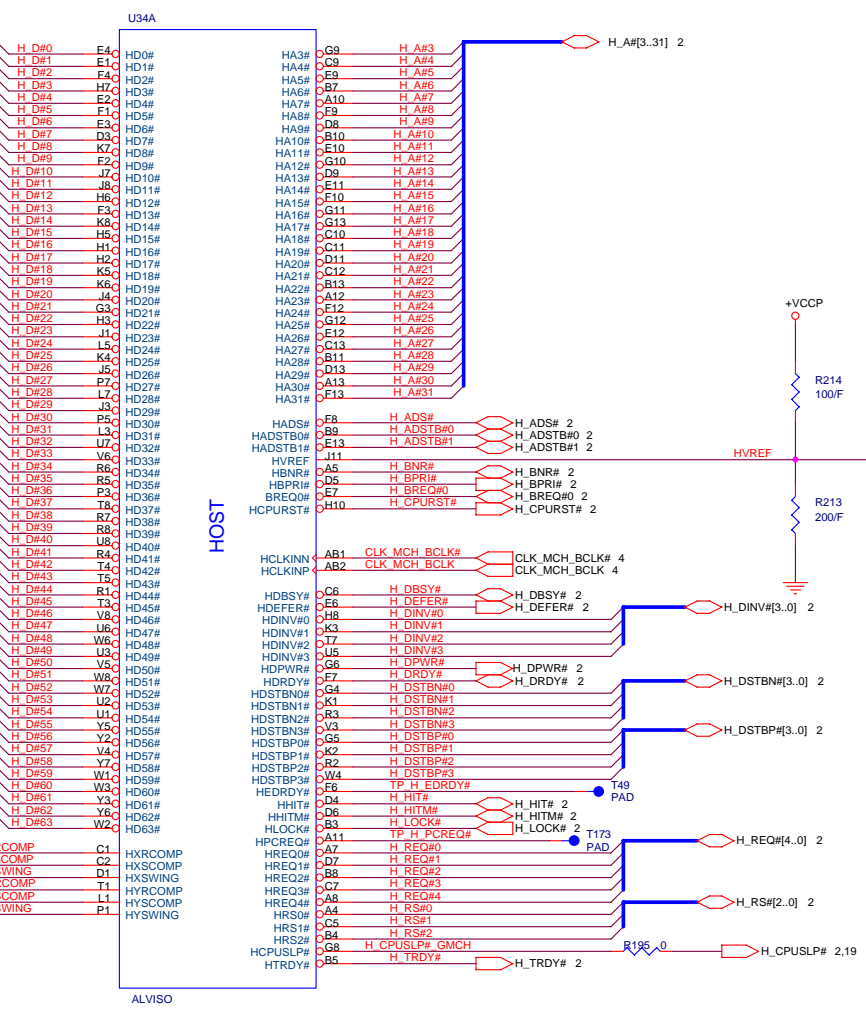
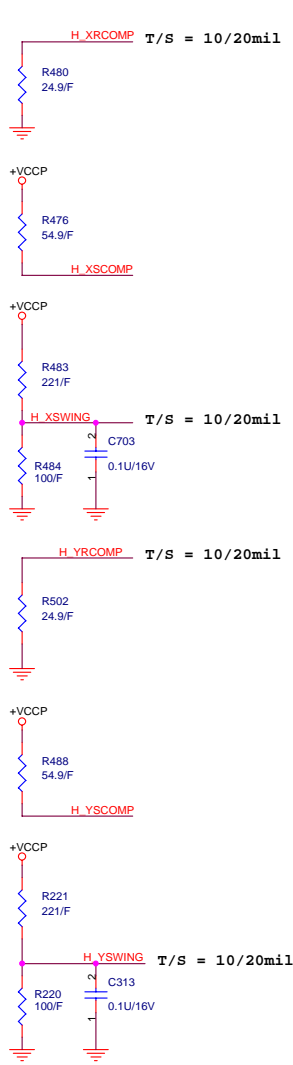
SM bus Address :
1001101 (EC)
For F75384S

Place Thermal-Sensor near CPU & GMCH.

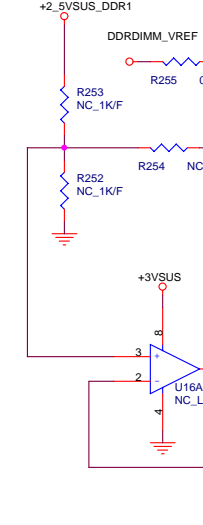
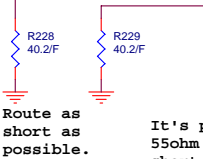
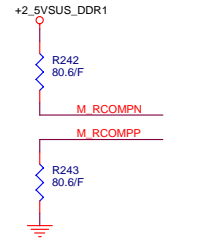
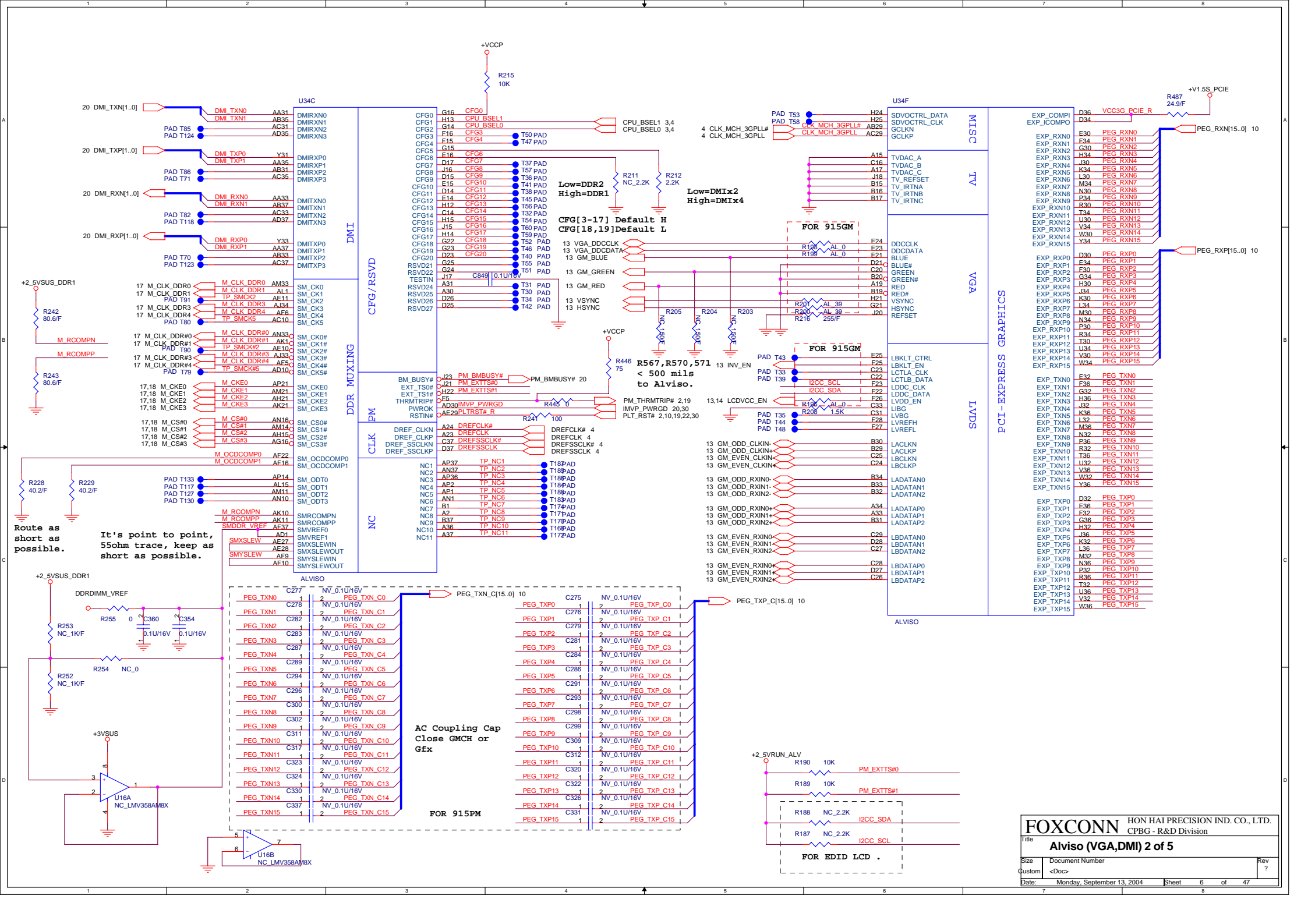
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File: **CLOCK_GEN(CK-410M)**

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Place Cap. near GMCH within 100 mils.

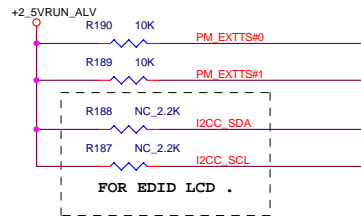


Route as short as possible.
It's point to point, 55ohm trace, keep as short as possible.

ALVISO

PEG_TXN0	C277	NV_0.1U/16V	PEG_TXN_C0	C275	NV_0.1U/16V	PEG_TXP_C0
PEG_TXN1	C278	NV_0.1U/16V	PEG_TXN_C1	C276	NV_0.1U/16V	PEG_TXP_C1
PEG_TXN2	C282	NV_0.1U/16V	PEG_TXN_C2	C279	NV_0.1U/16V	PEG_TXP_C2
PEG_TXN3	C283	NV_0.1U/16V	PEG_TXN_C3	C281	NV_0.1U/16V	PEG_TXP_C3
PEG_TXN4	C287	NV_0.1U/16V	PEG_TXN_C4	C284	NV_0.1U/16V	PEG_TXP_C4
PEG_TXN5	C289	NV_0.1U/16V	PEG_TXN_C5	C286	NV_0.1U/16V	PEG_TXP_C5
PEG_TXN6	C294	NV_0.1U/16V	PEG_TXN_C6	C291	NV_0.1U/16V	PEG_TXP_C6
PEG_TXN7	C296	NV_0.1U/16V	PEG_TXN_C7	C293	NV_0.1U/16V	PEG_TXP_C7
PEG_TXN8	C300	NV_0.1U/16V	PEG_TXN_C8	C298	NV_0.1U/16V	PEG_TXP_C8
PEG_TXN9	C302	NV_0.1U/16V	PEG_TXN_C9	C299	NV_0.1U/16V	PEG_TXP_C9
PEG_TXN10	C311	NV_0.1U/16V	PEG_TXN_C10	C309	NV_0.1U/16V	PEG_TXP_C10
PEG_TXN11	C317	NV_0.1U/16V	PEG_TXN_C11	C312	NV_0.1U/16V	PEG_TXP_C11
PEG_TXN12	C323	NV_0.1U/16V	PEG_TXN_C12	C320	NV_0.1U/16V	PEG_TXP_C12
PEG_TXN13	C324	NV_0.1U/16V	PEG_TXN_C13	C322	NV_0.1U/16V	PEG_TXP_C13
PEG_TXN14	C330	NV_0.1U/16V	PEG_TXN_C14	C326	NV_0.1U/16V	PEG_TXP_C14
PEG_TXN15	C337	NV_0.1U/16V	PEG_TXN_C15	C331	NV_0.1U/16V	PEG_TXP_C15

FOR 915PM



17 M_A_DQ[63..0]

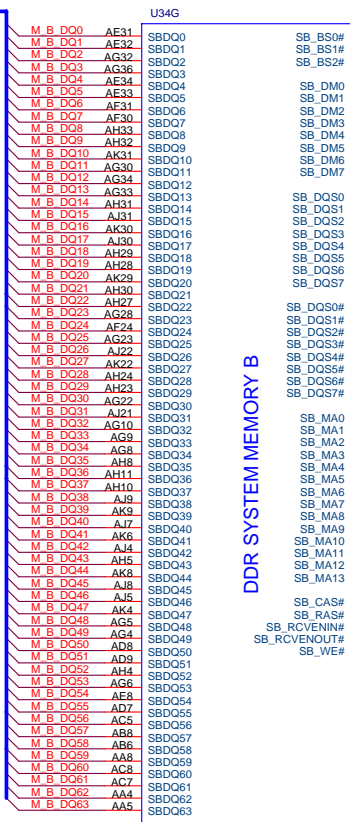


U34B

DDR SYSTEM MEMORY A

ALVISO

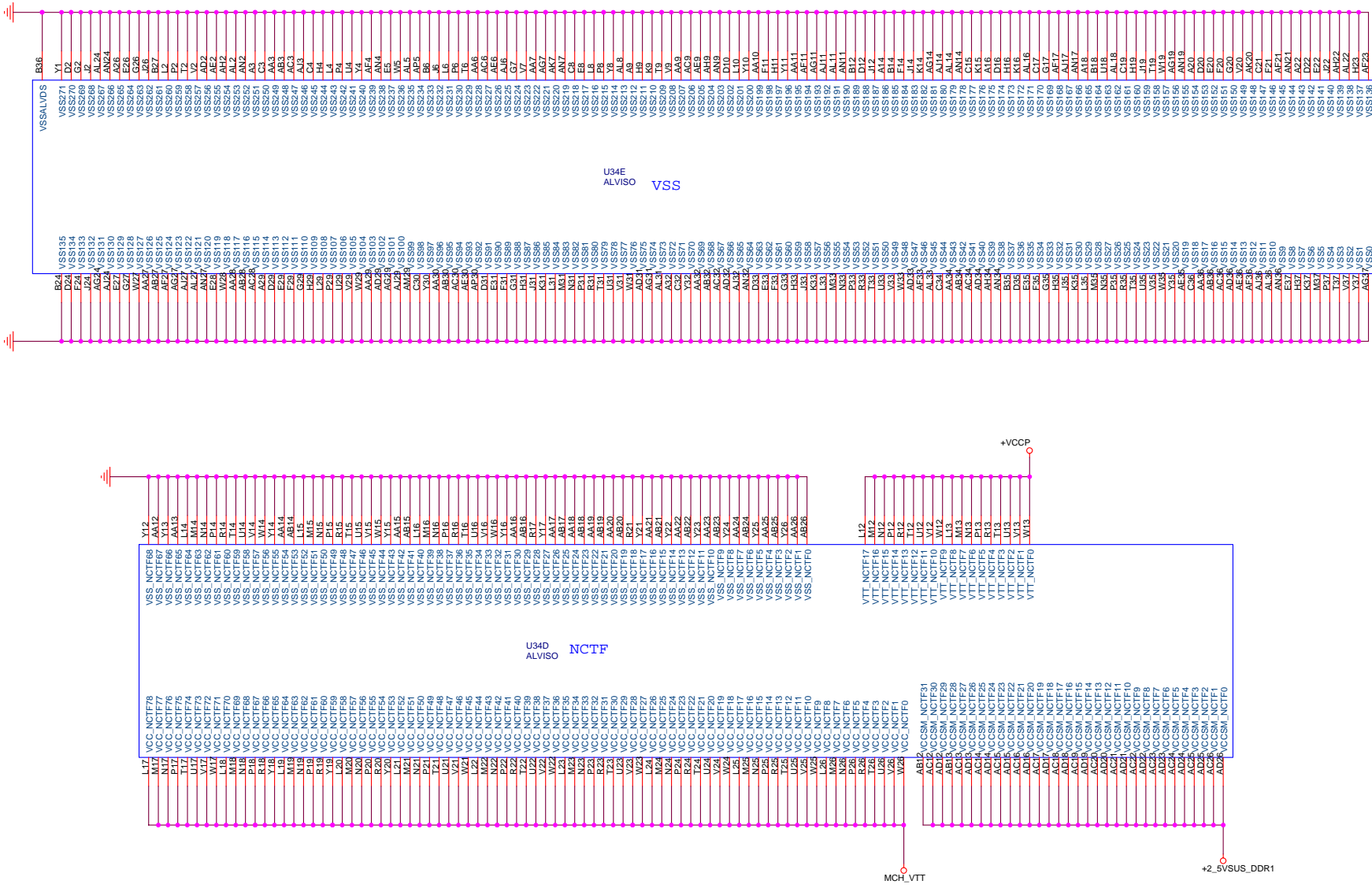
17 M_B_DQ[63..0]

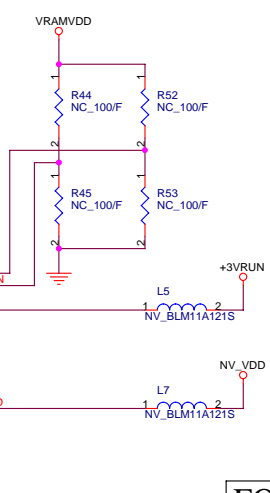
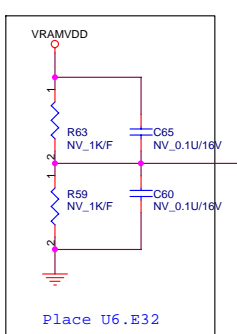
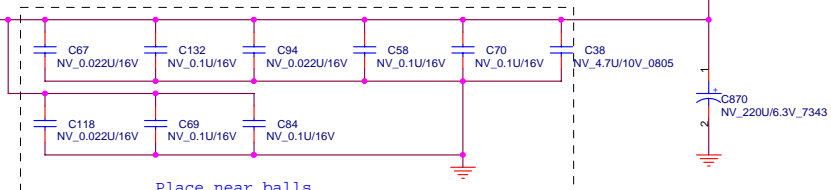
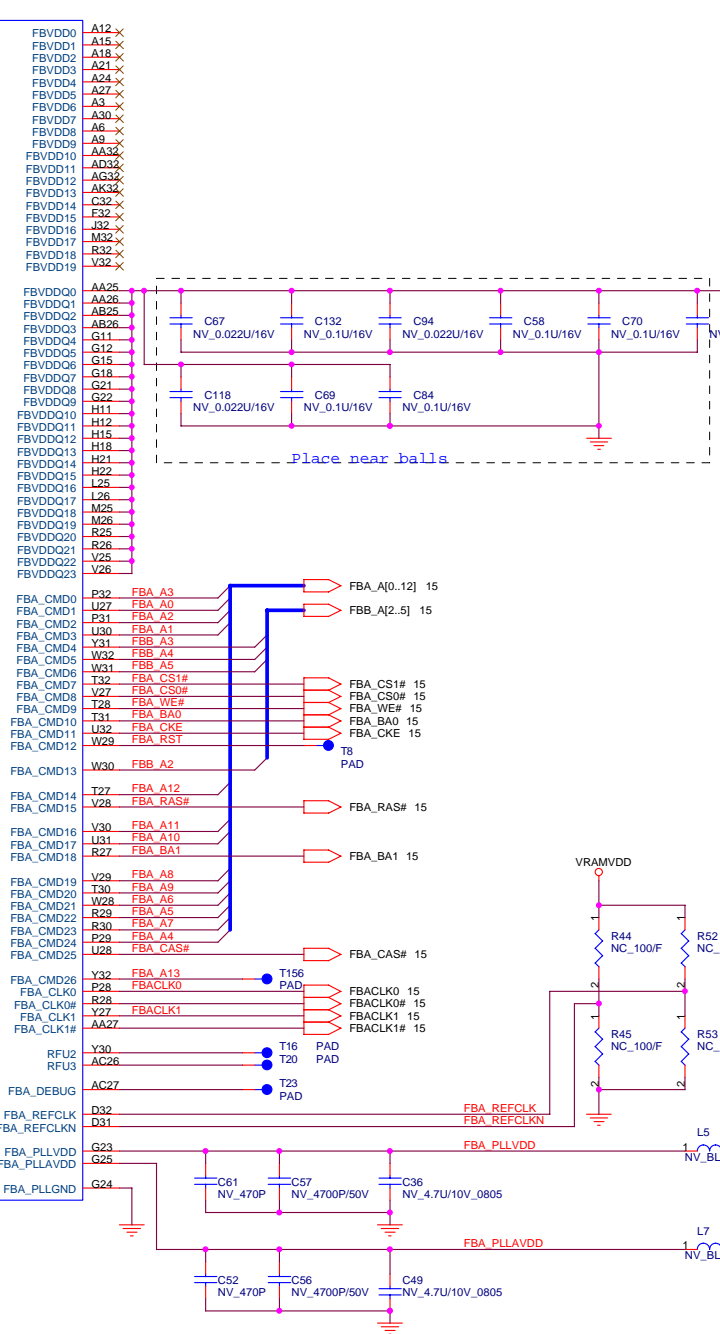
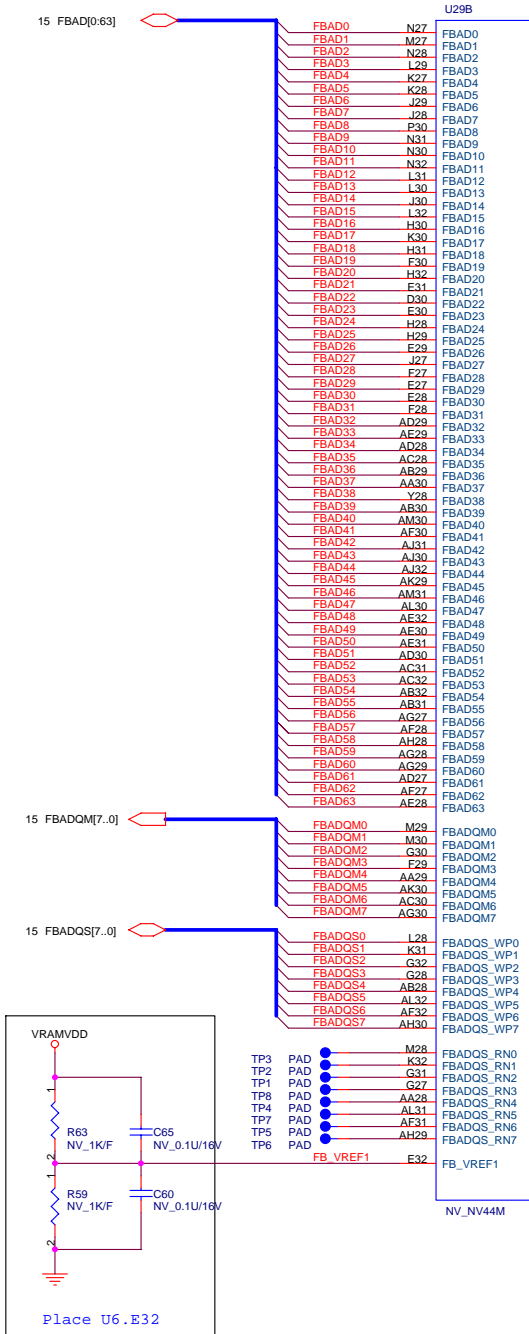
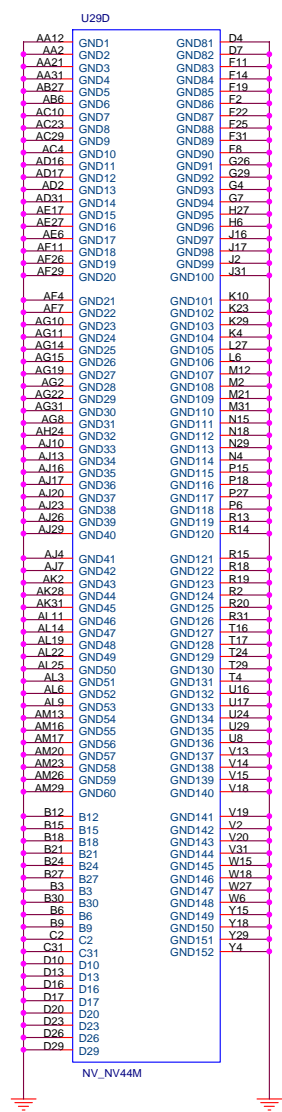


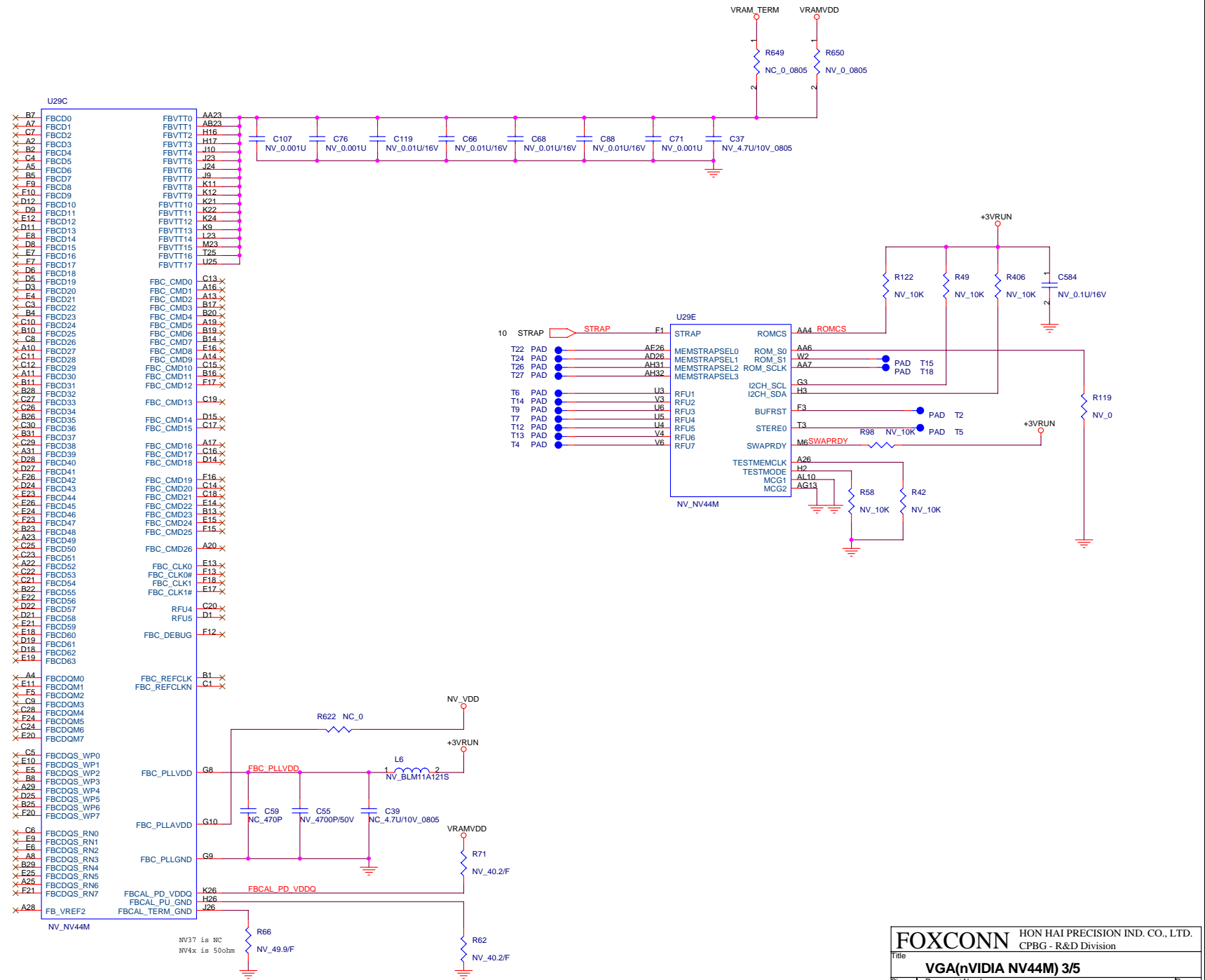
U34G

DDR SYSTEM MEMORY B

ALVISO



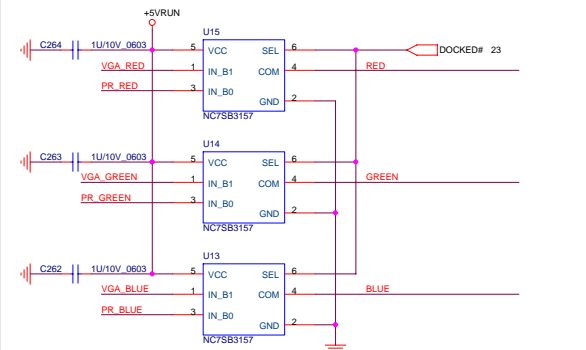
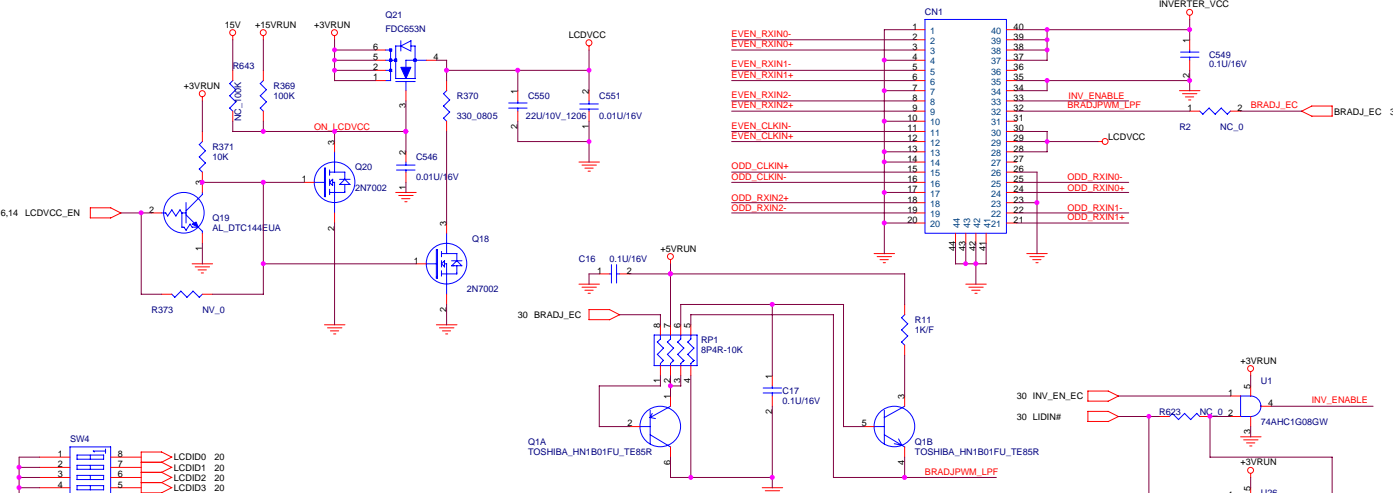




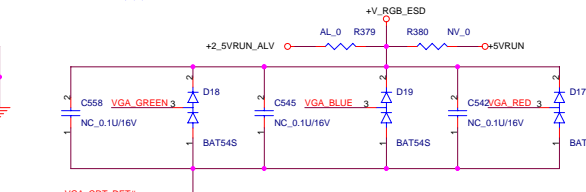
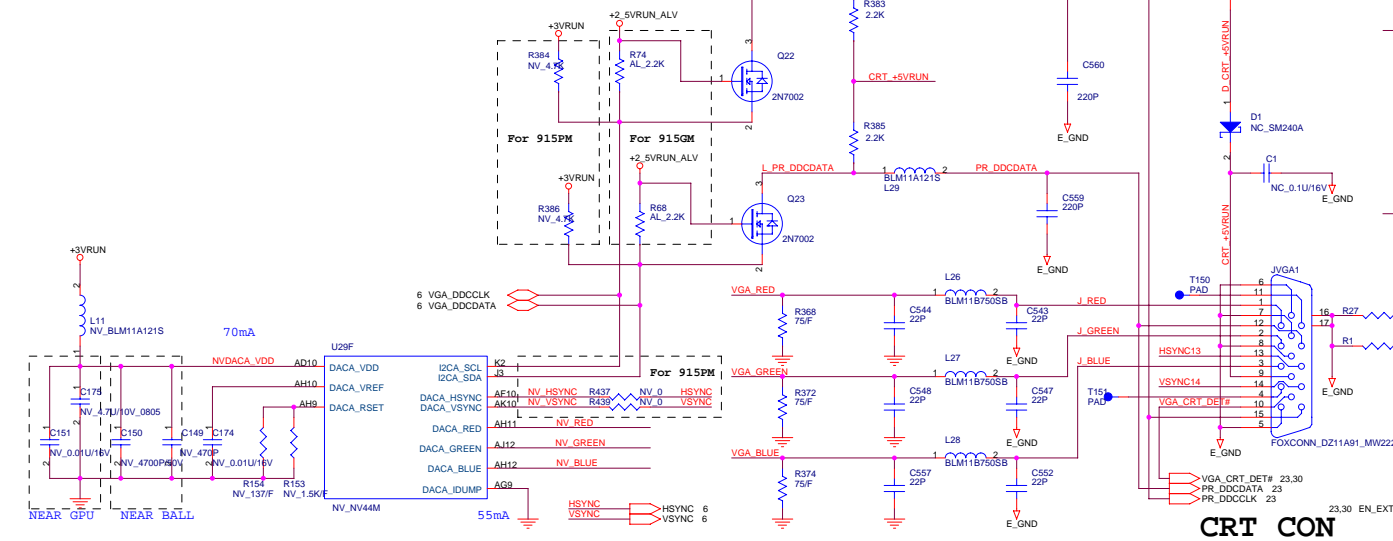
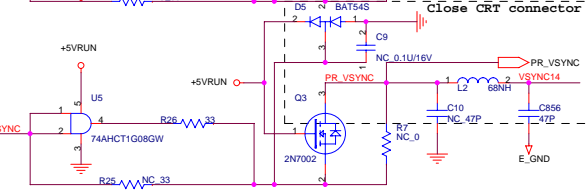
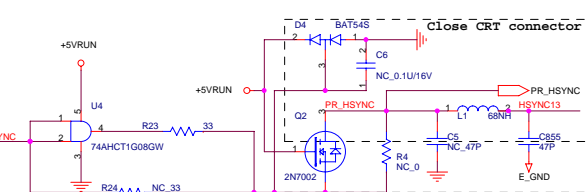
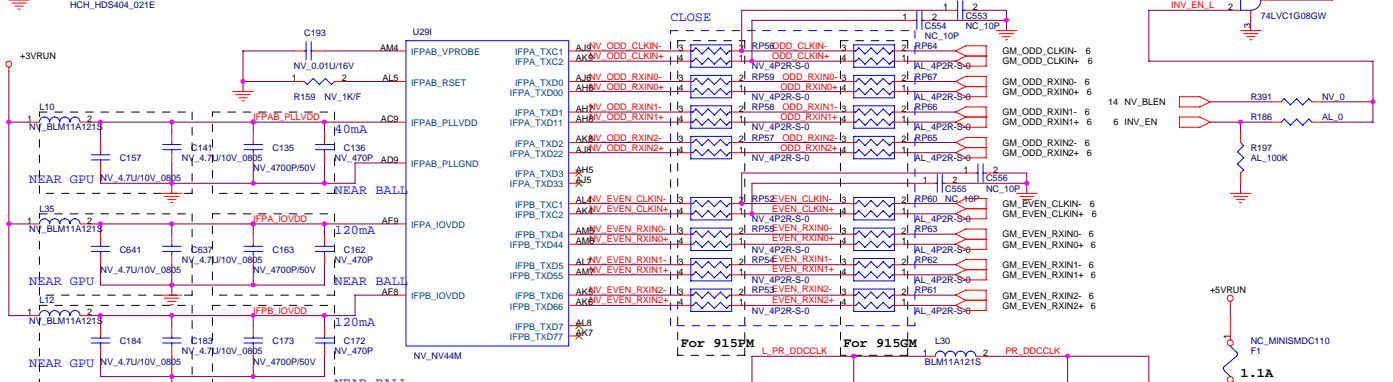
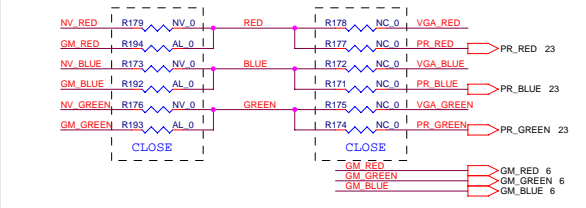
LVDS CONNECTOR

FOXCONN_GS12401_1011

H : NOTEBOOK
L : PORT REPLICATOR



RGB ANALOG SWITCH

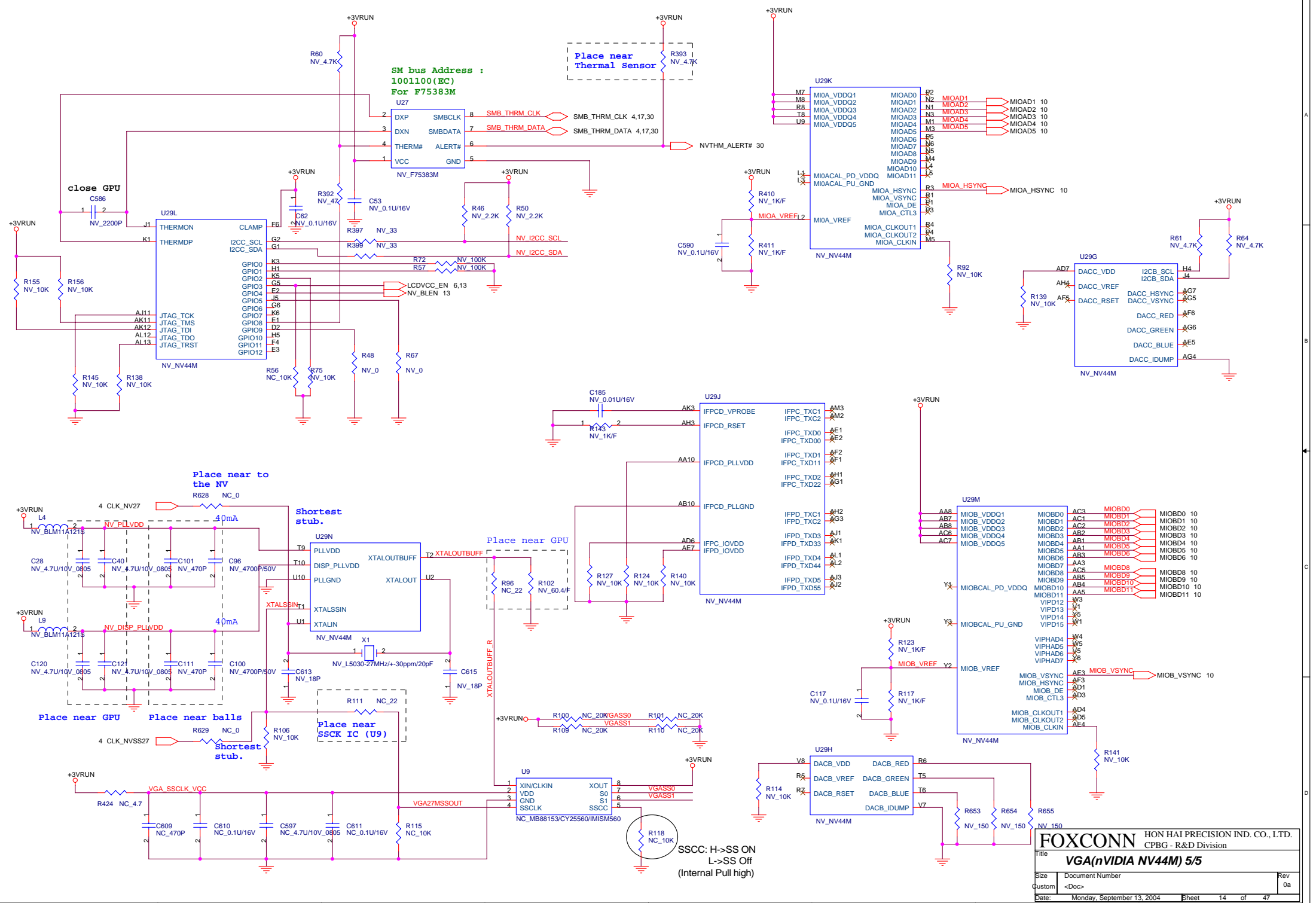


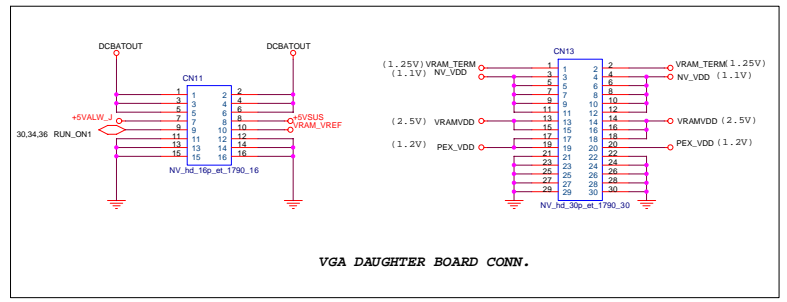
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CPBG - R&D Division
VGA(nVIDIA NV44M) 4/5

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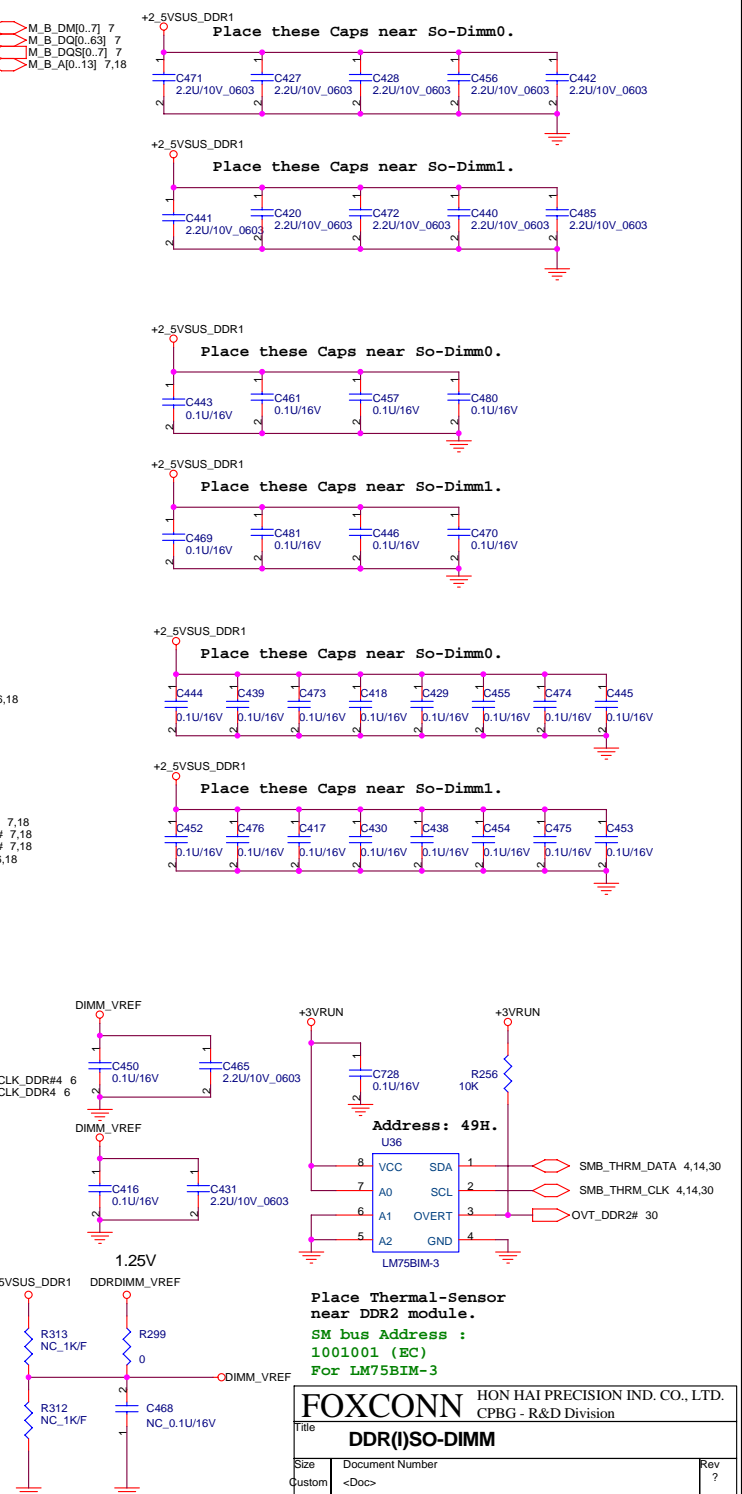
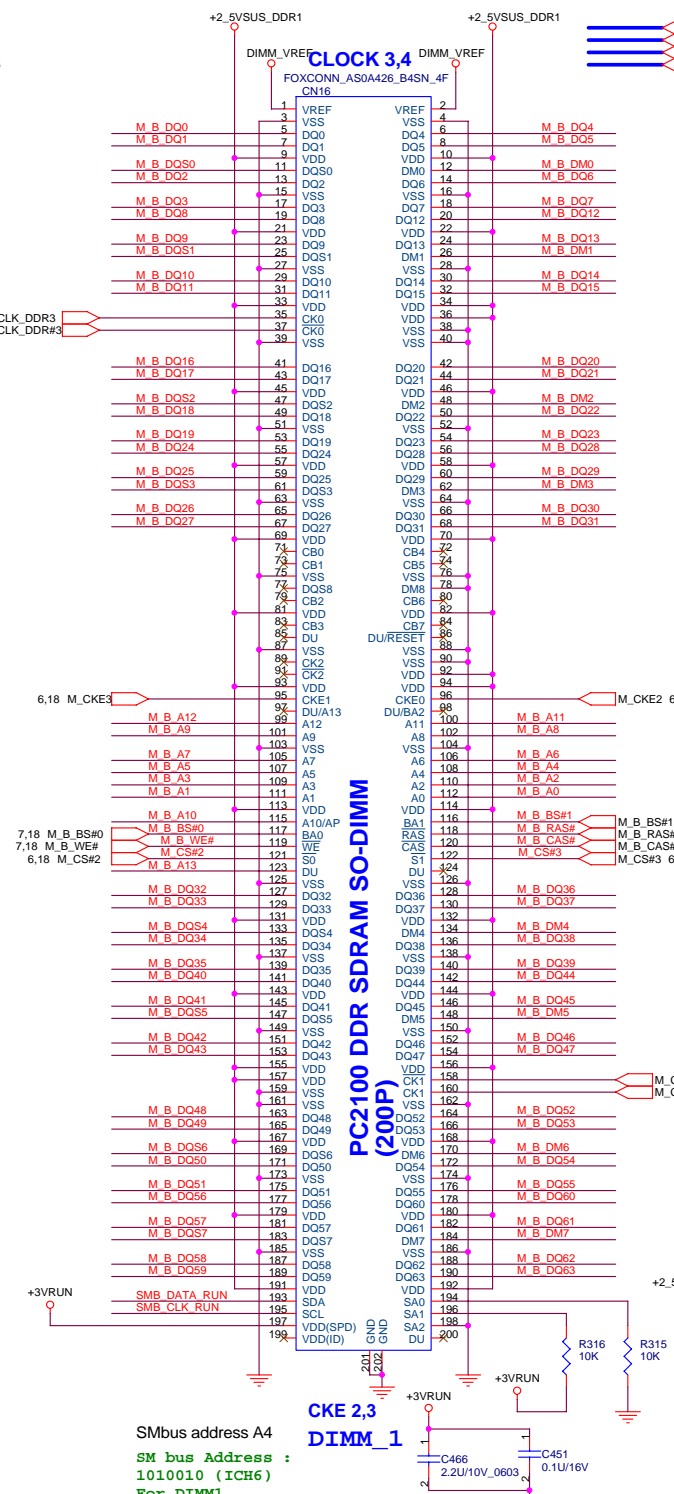
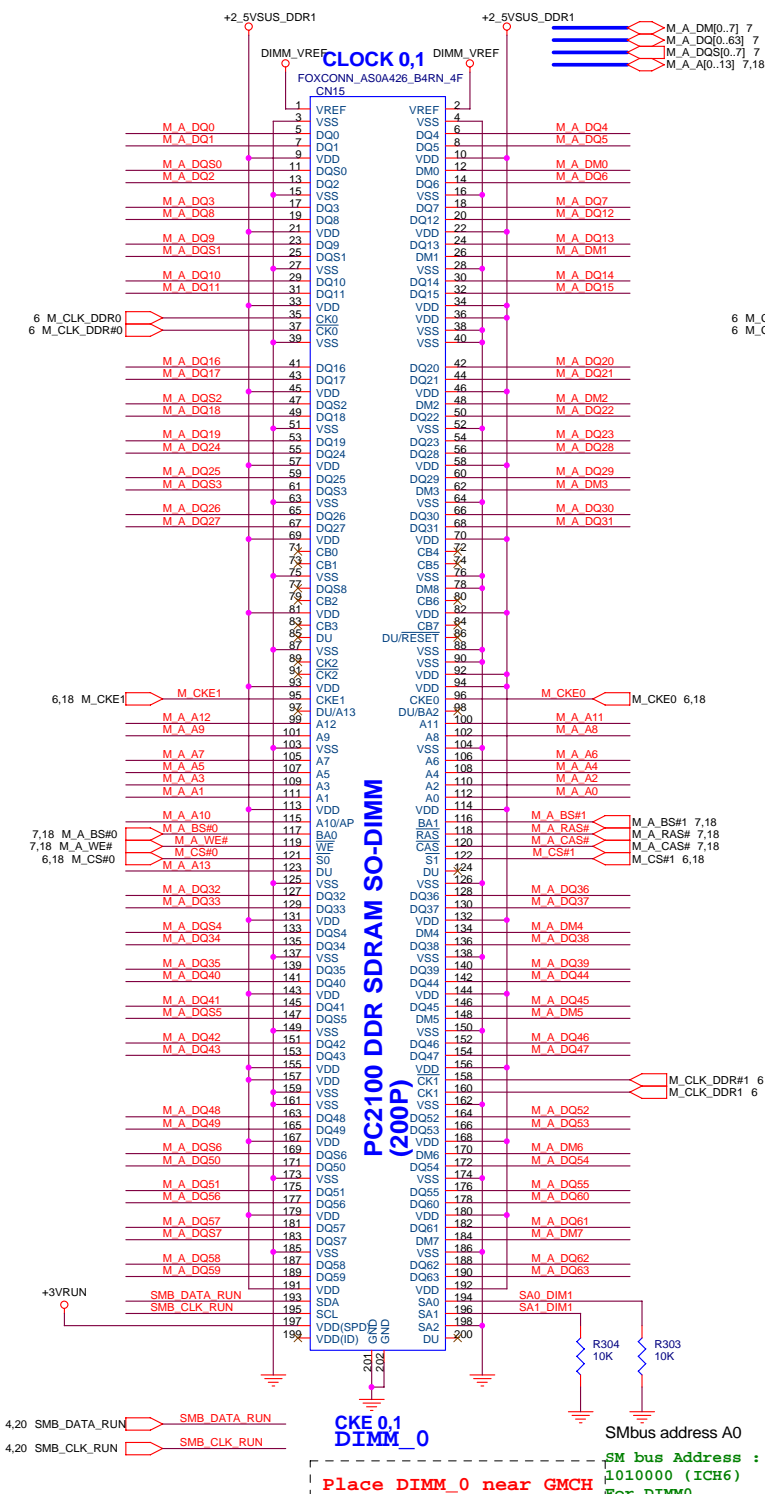
CRT CON

R235, R237, R241 L30, L32, L33
<1000 mils to JVG1. <500mils to JVG1A.



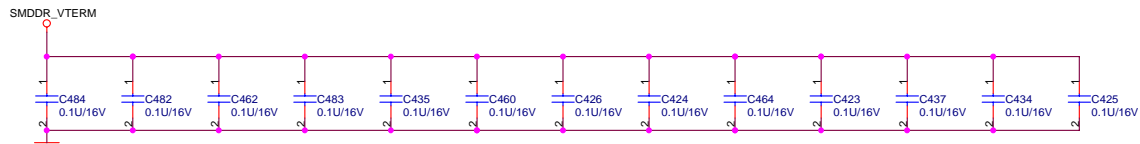


VGA DAUGHTER BOARD CONN.

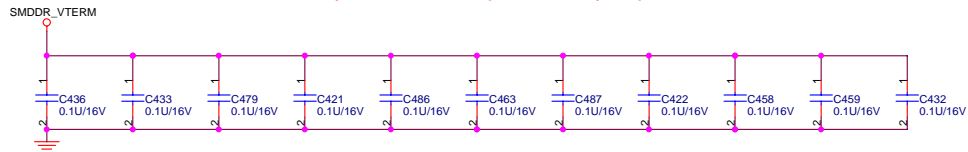


M_A_A[0..13] 7,17

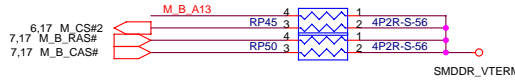
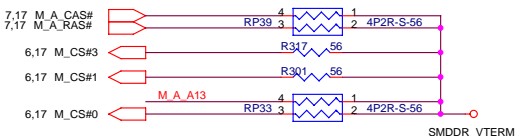
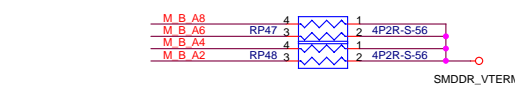
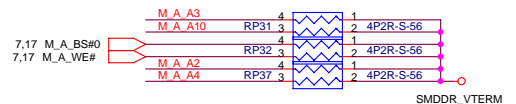
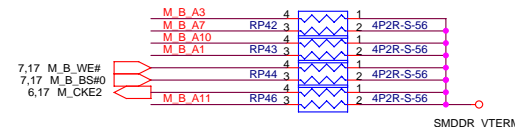
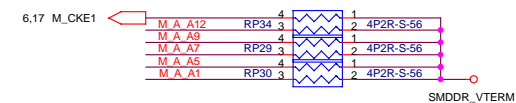
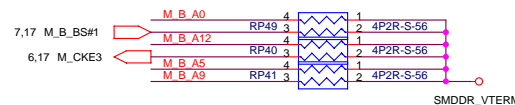
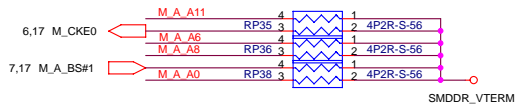
M_B_A[0..13] 7,17

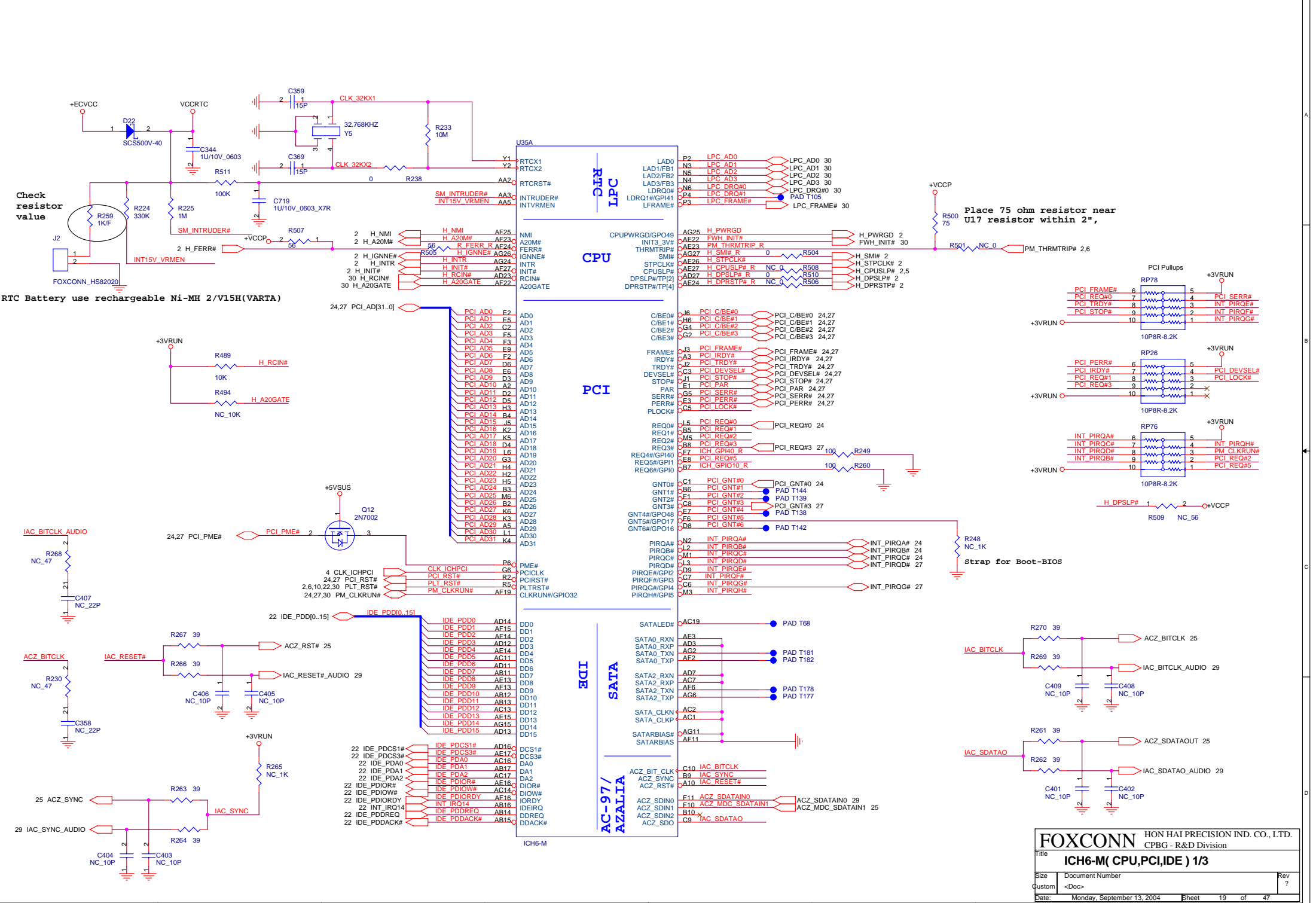


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

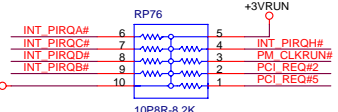
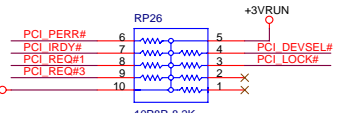
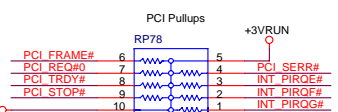




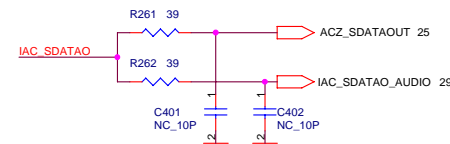
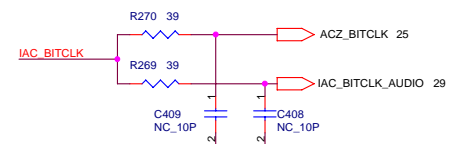
Check resistor value

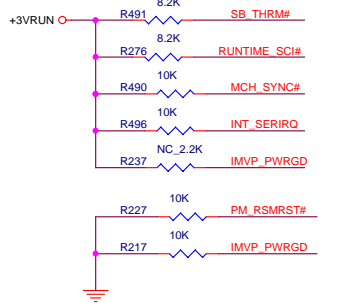
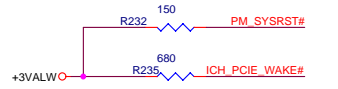
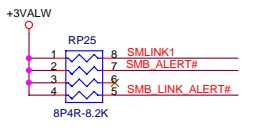
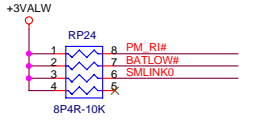
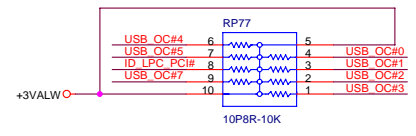
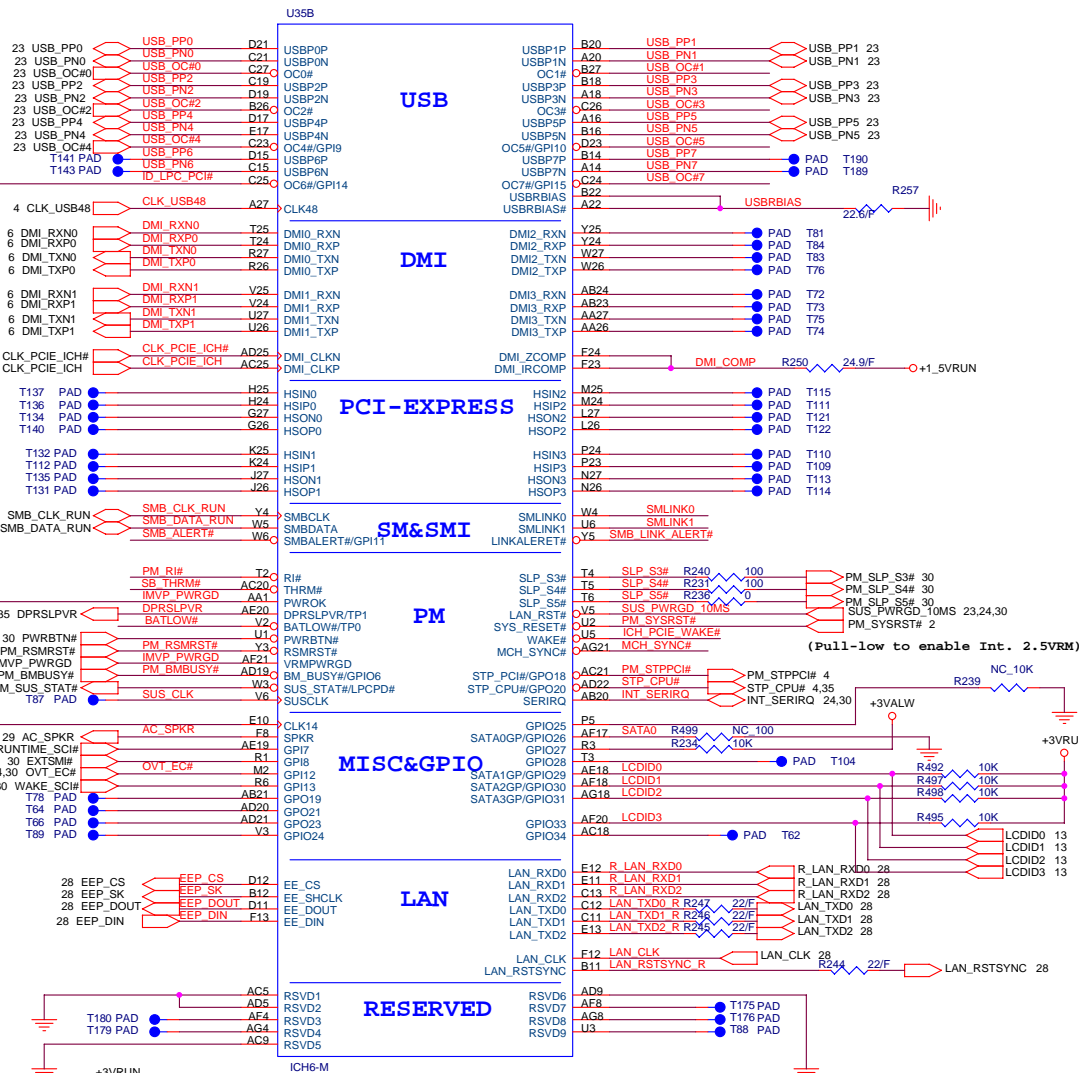
RTC Battery use rechargeable Ni-MH 2/V15H(VARTA)

Place 75 ohm resistor near U17 resistor within 2",



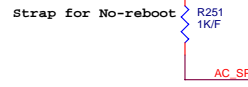
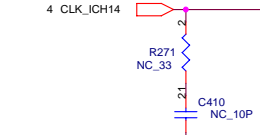
Strap for Boot-BIOS



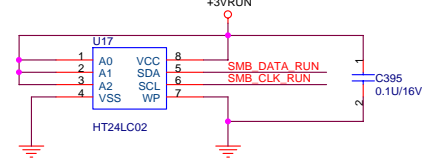


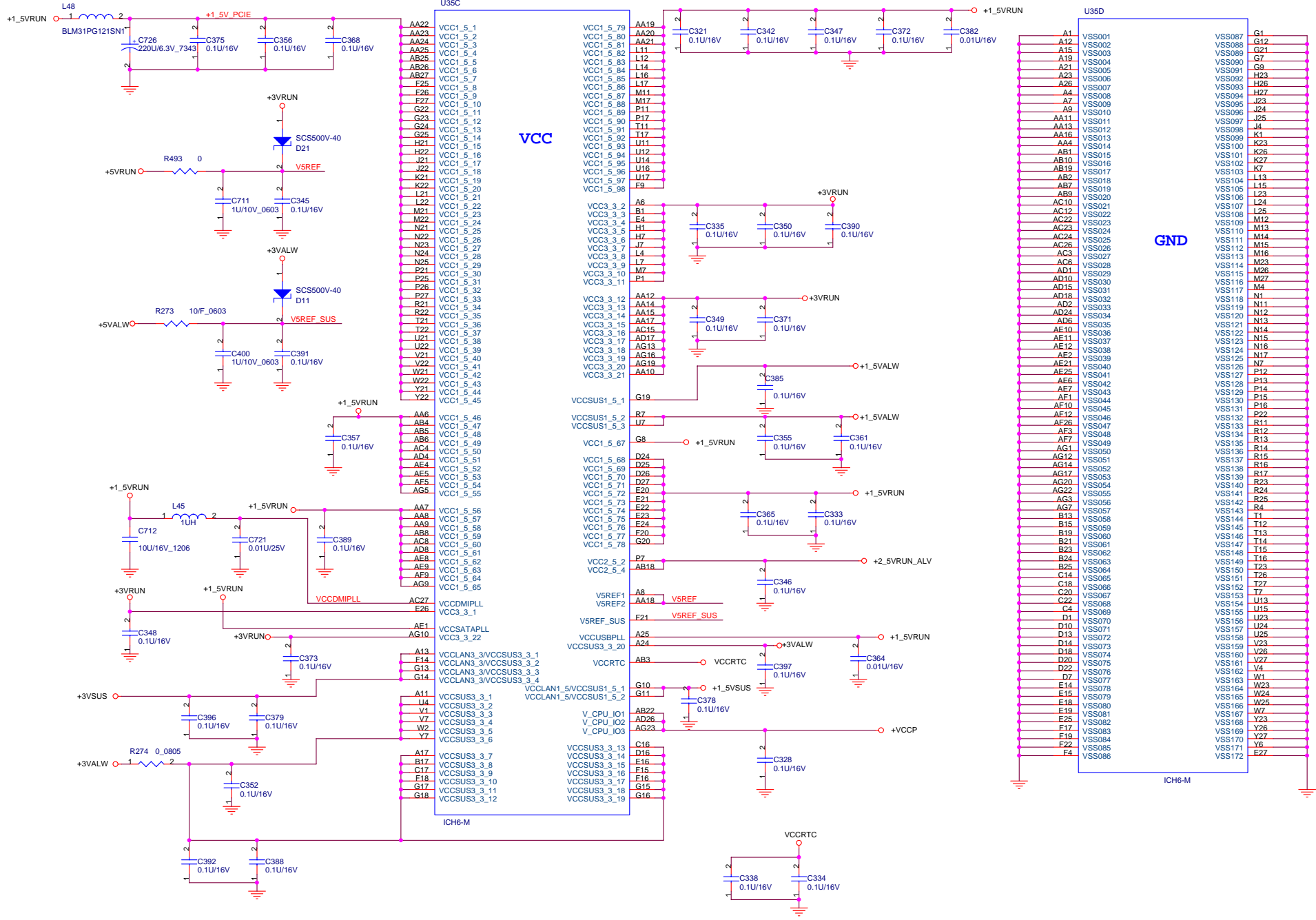
30 ID_LPC_PCIF#
80 Port I/F:
H: LCP bus
L: PCI bus

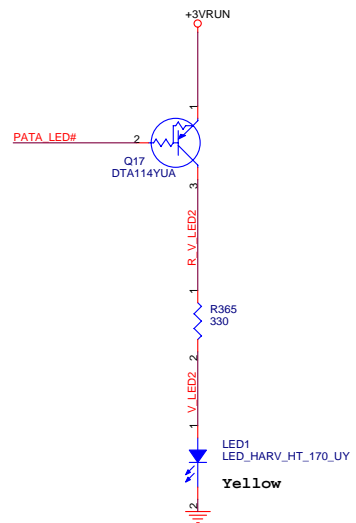
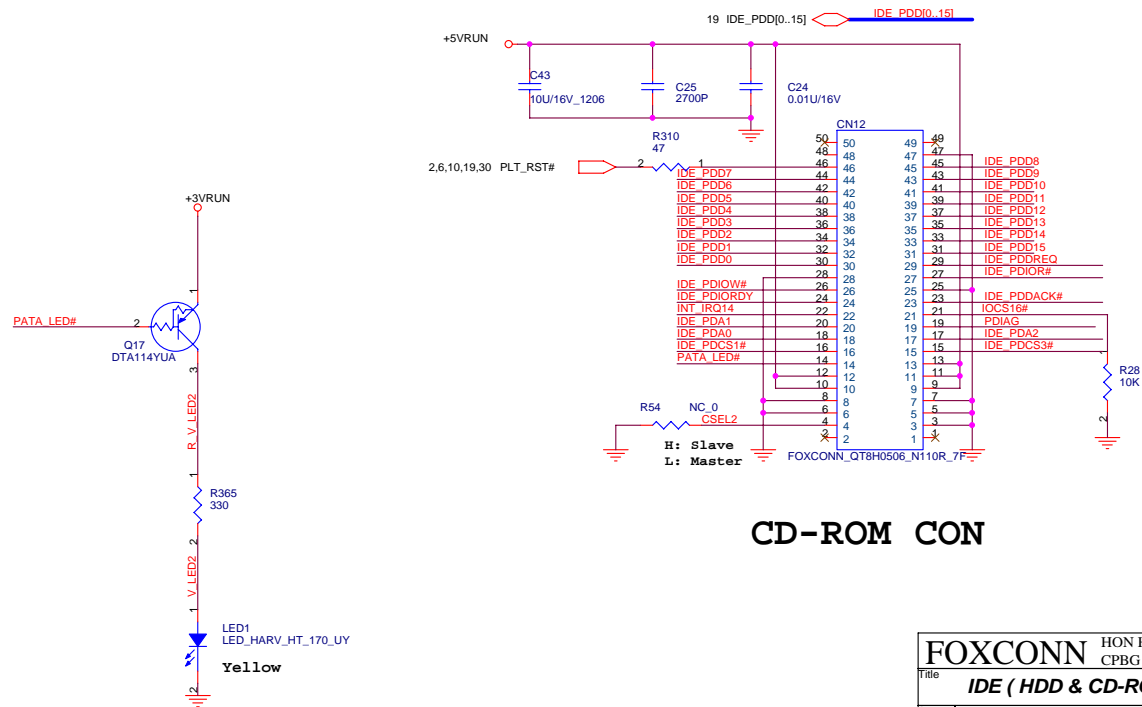
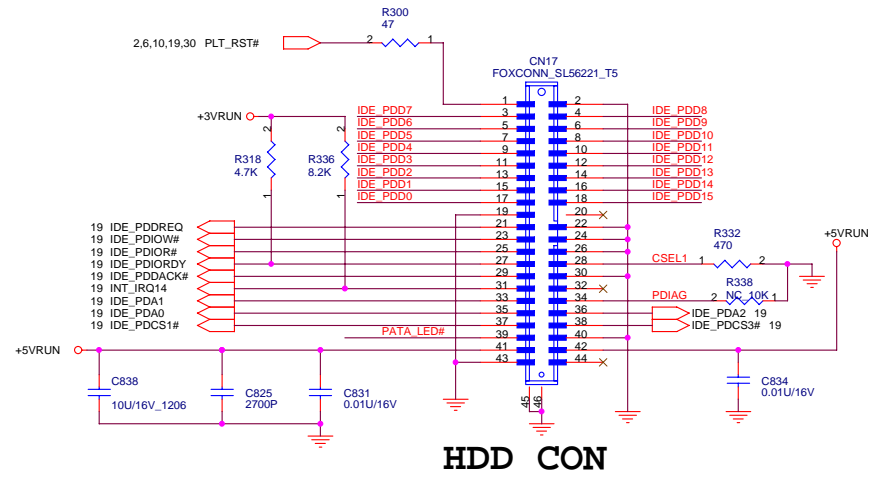
6.30 IMVP_PWRGD
35 DPRSLPVR
30 PWRBTN#
30 PM_RSMRST#
6.30 IMVP_PWRGD
6 PM_BMBUSY#
30 PM_SUS_STAT#



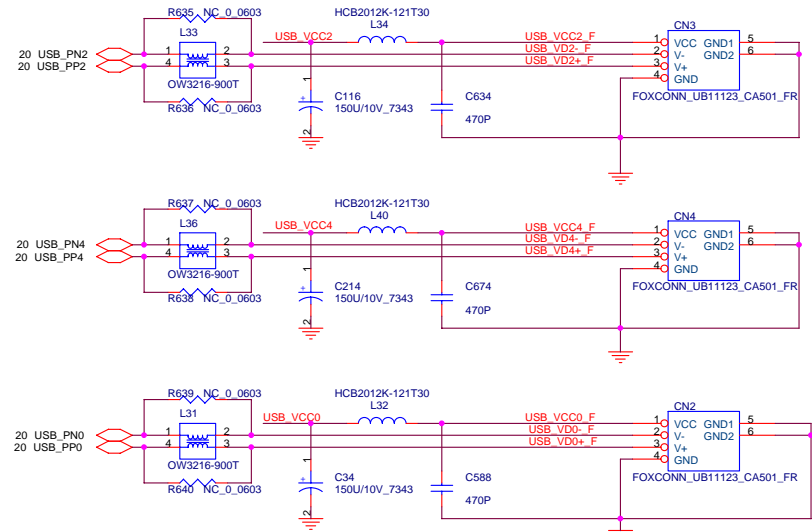
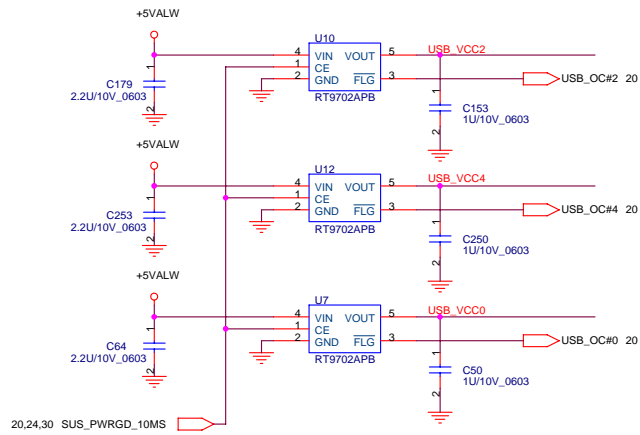
Adds .AEH



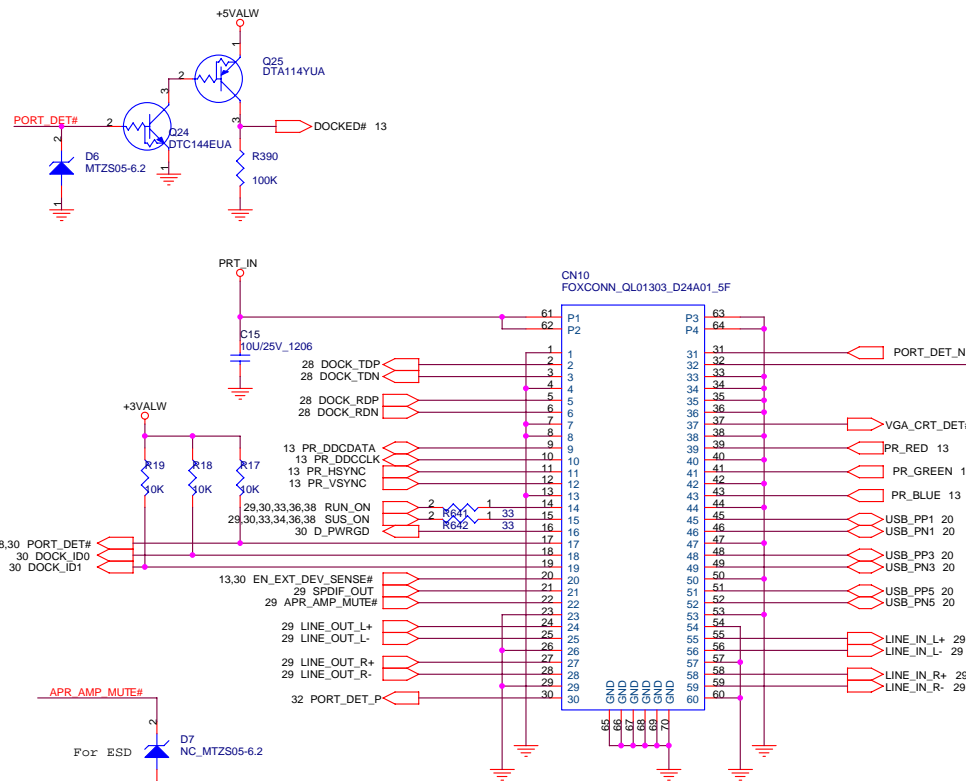




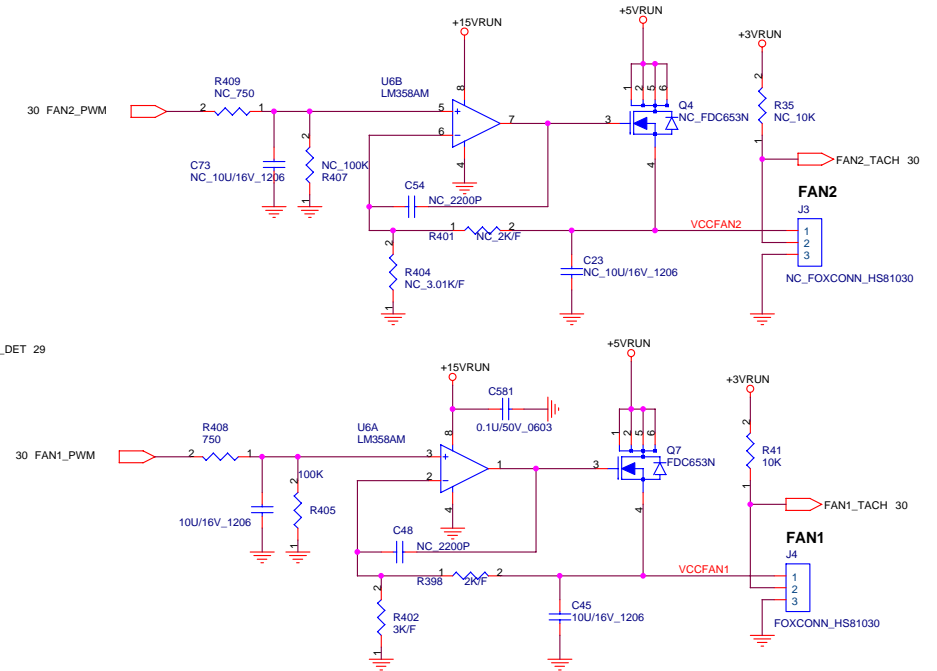
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CPBG - R&D Division	
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Date:	Monday, September 13, 2004
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Rev	?



USB2.0 X 3

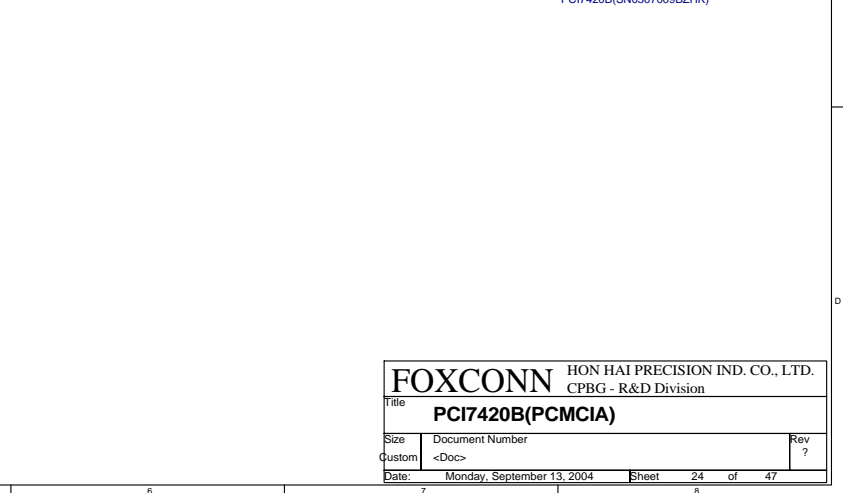
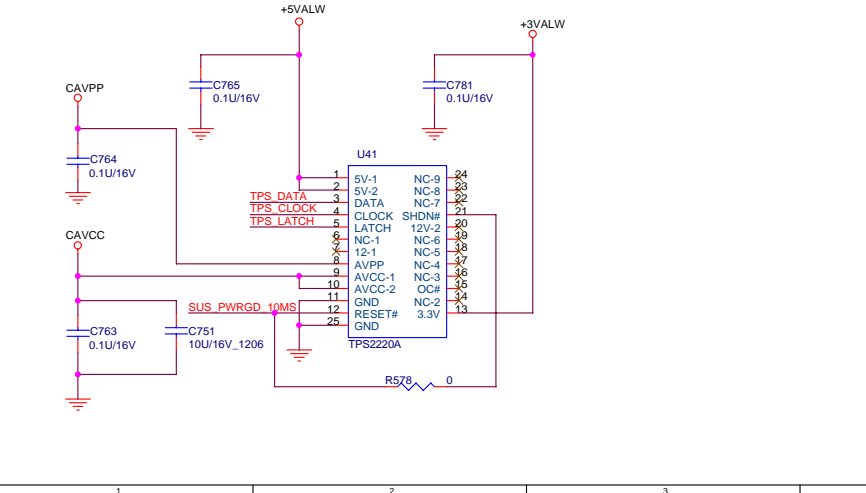
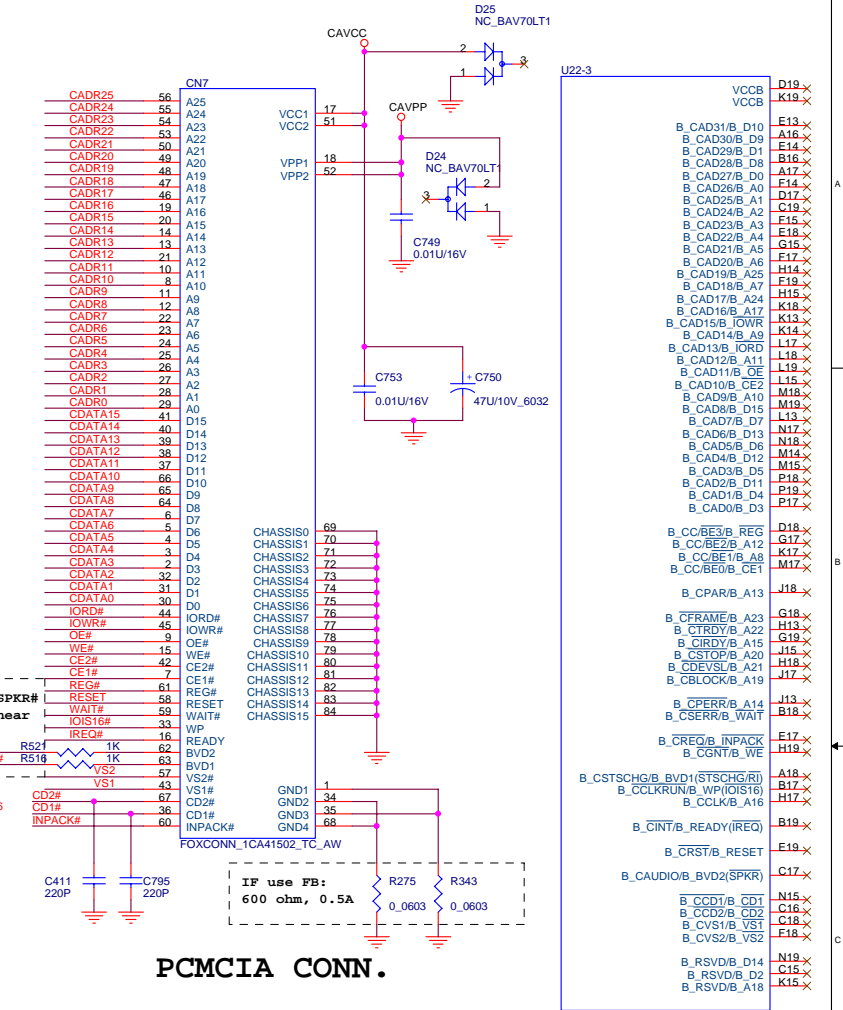
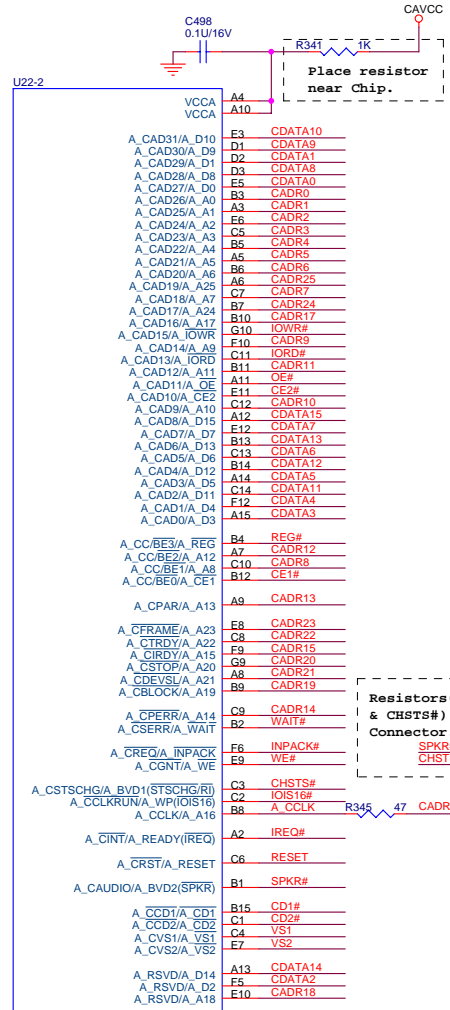
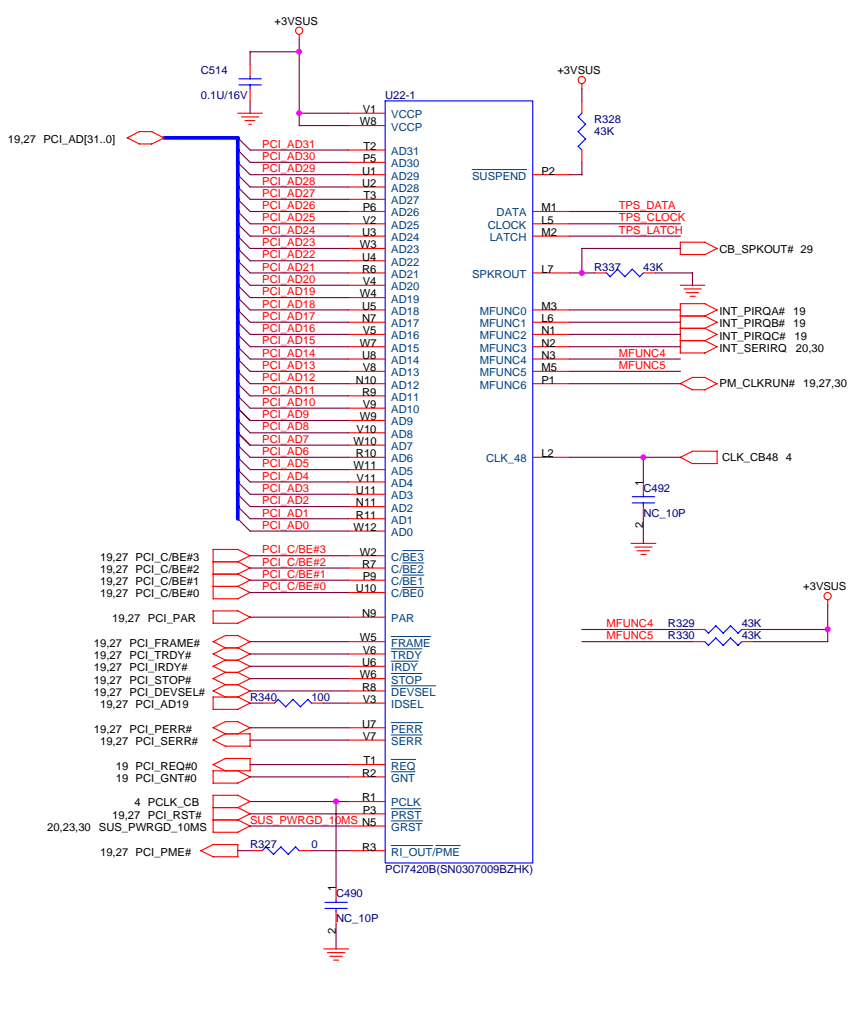


Replicator Port

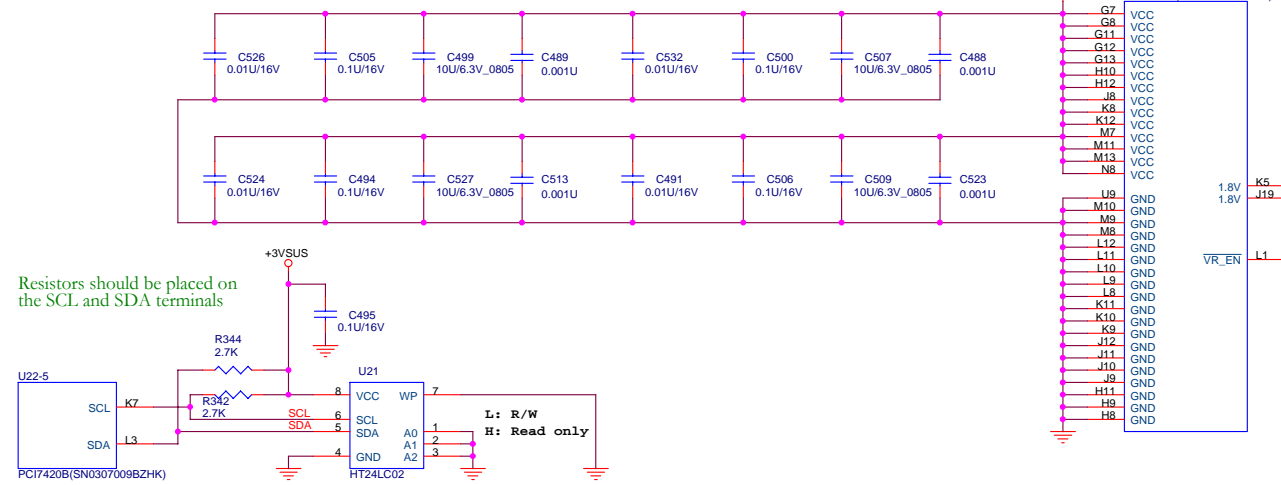
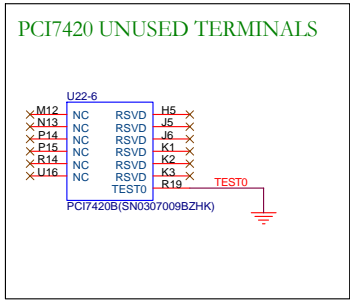
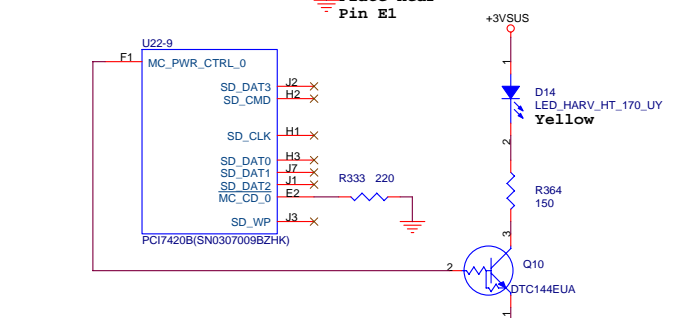
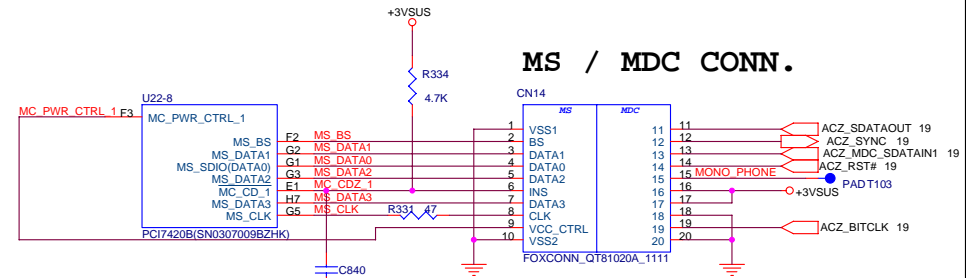
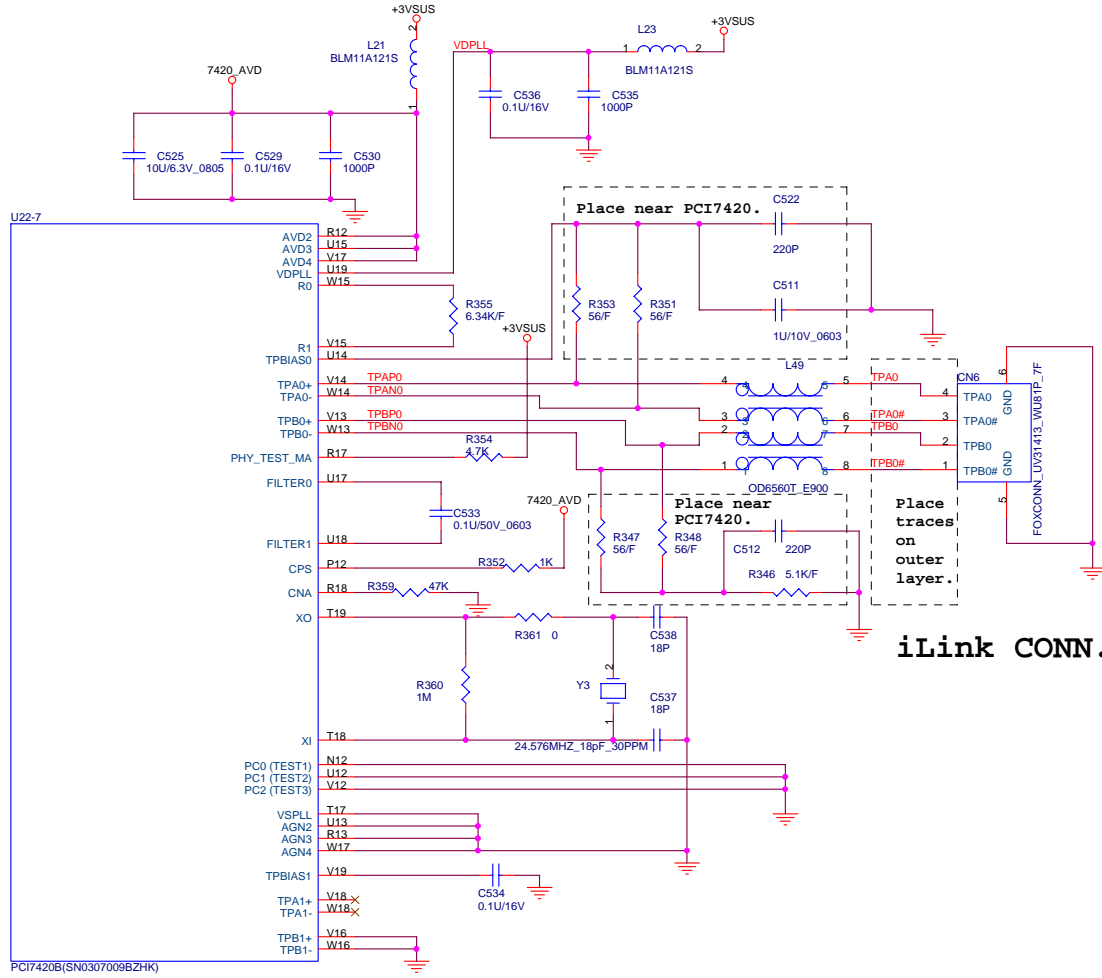


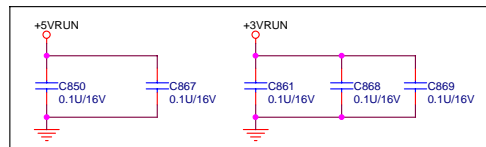
FAN

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USB2.0/MDC/FAN/DOCKING Connector			
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PCMCIA CONN.





For EMI .



Near RP51 ,
for EMI .



Near R607 ,
for EMI .



Near Q7 ,
for EMI .



Near Q4 ,
for EMI .



Near U37 ,
for EMI .



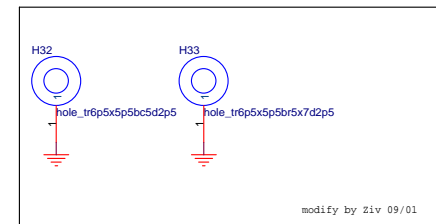
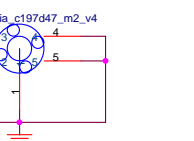
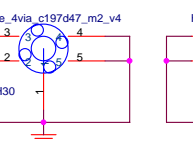
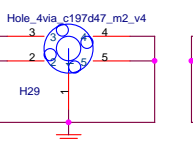
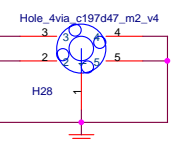
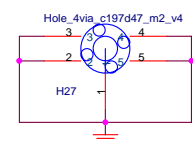
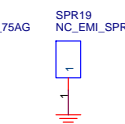
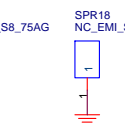
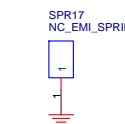
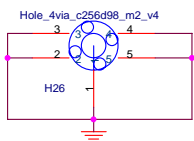
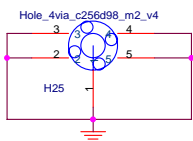
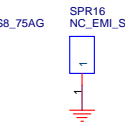
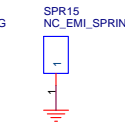
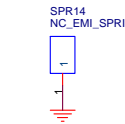
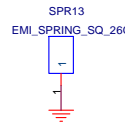
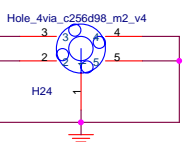
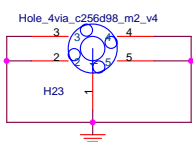
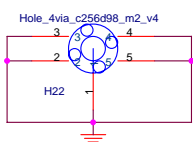
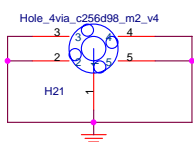
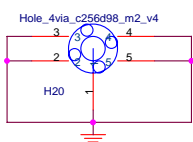
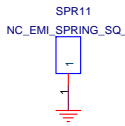
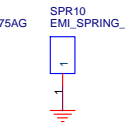
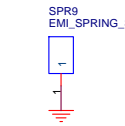
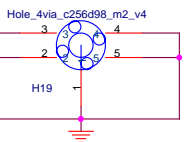
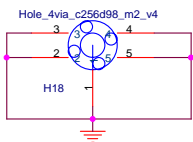
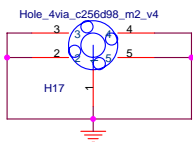
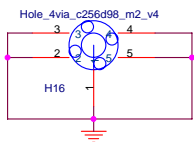
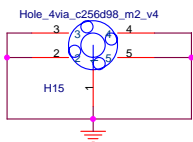
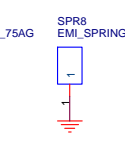
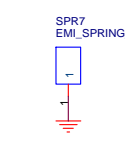
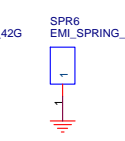
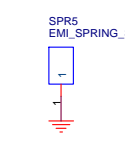
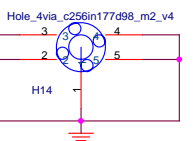
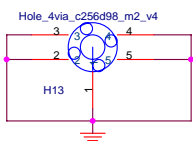
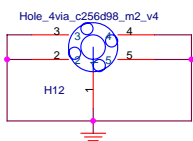
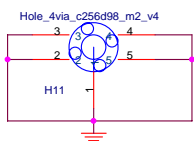
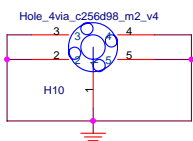
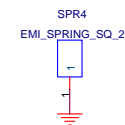
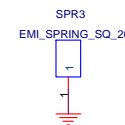
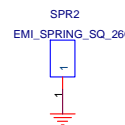
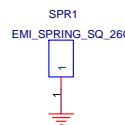
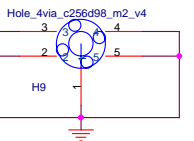
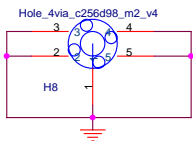
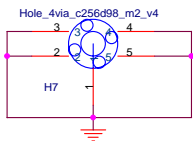
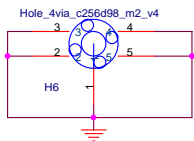
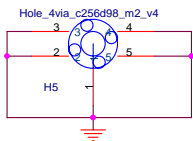
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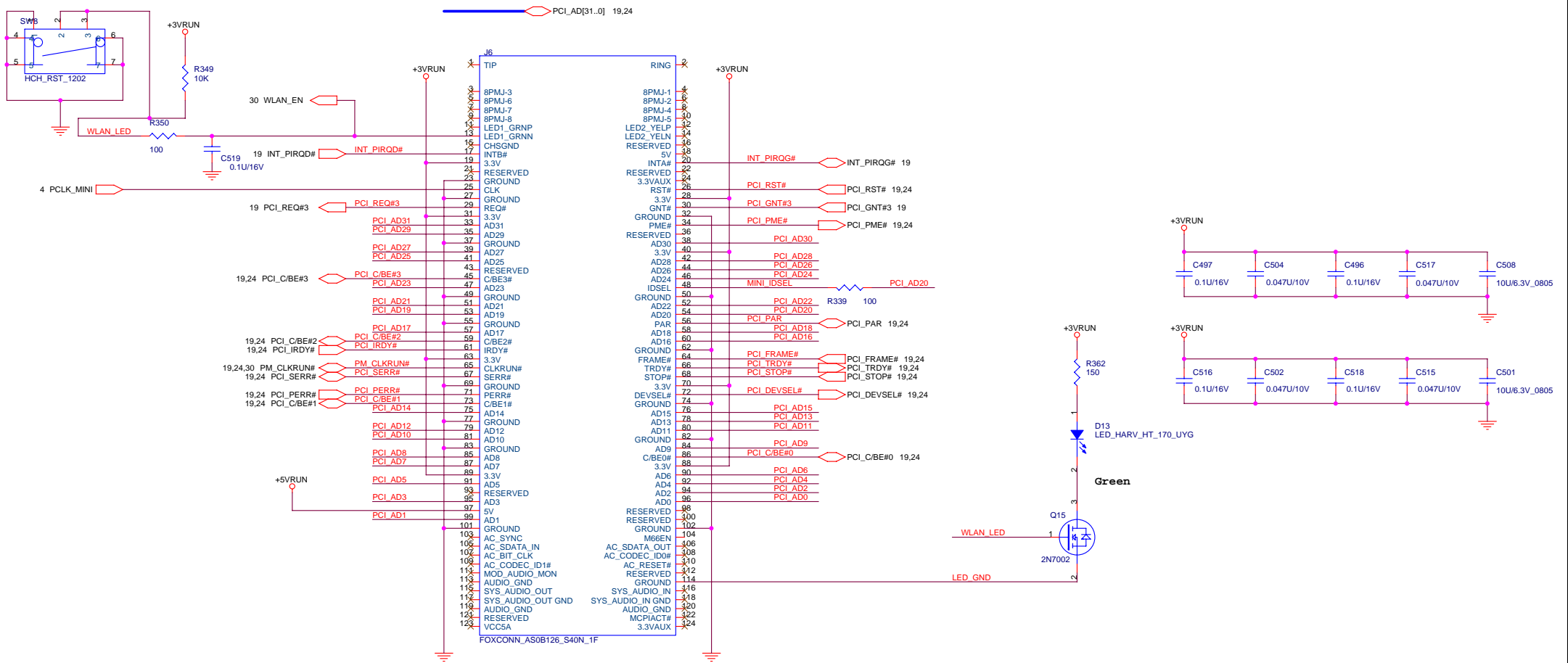


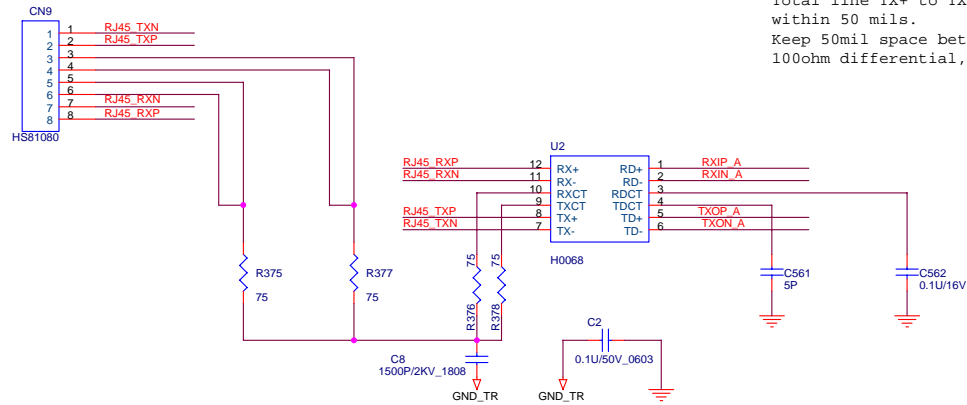
Near Q4 ,
for EMI .



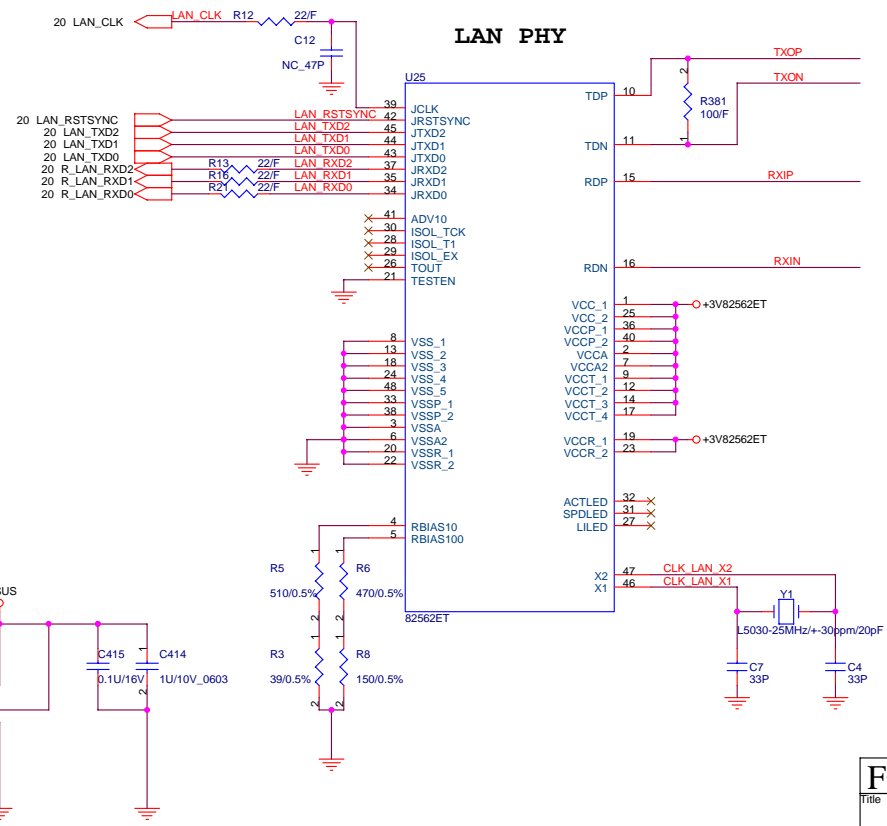
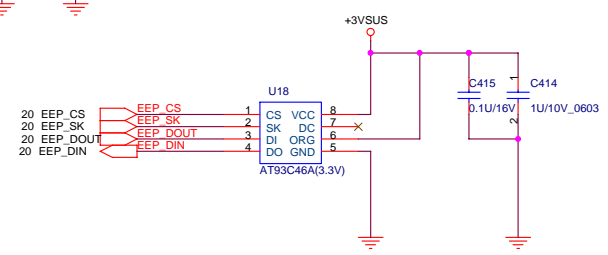
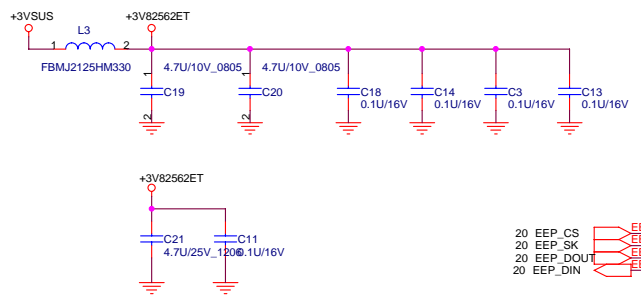
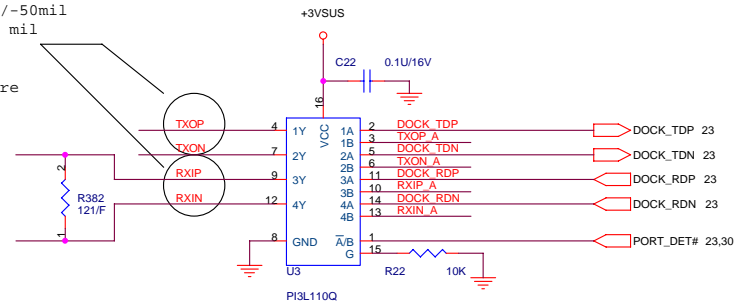
Near D8 ,
for EMI .

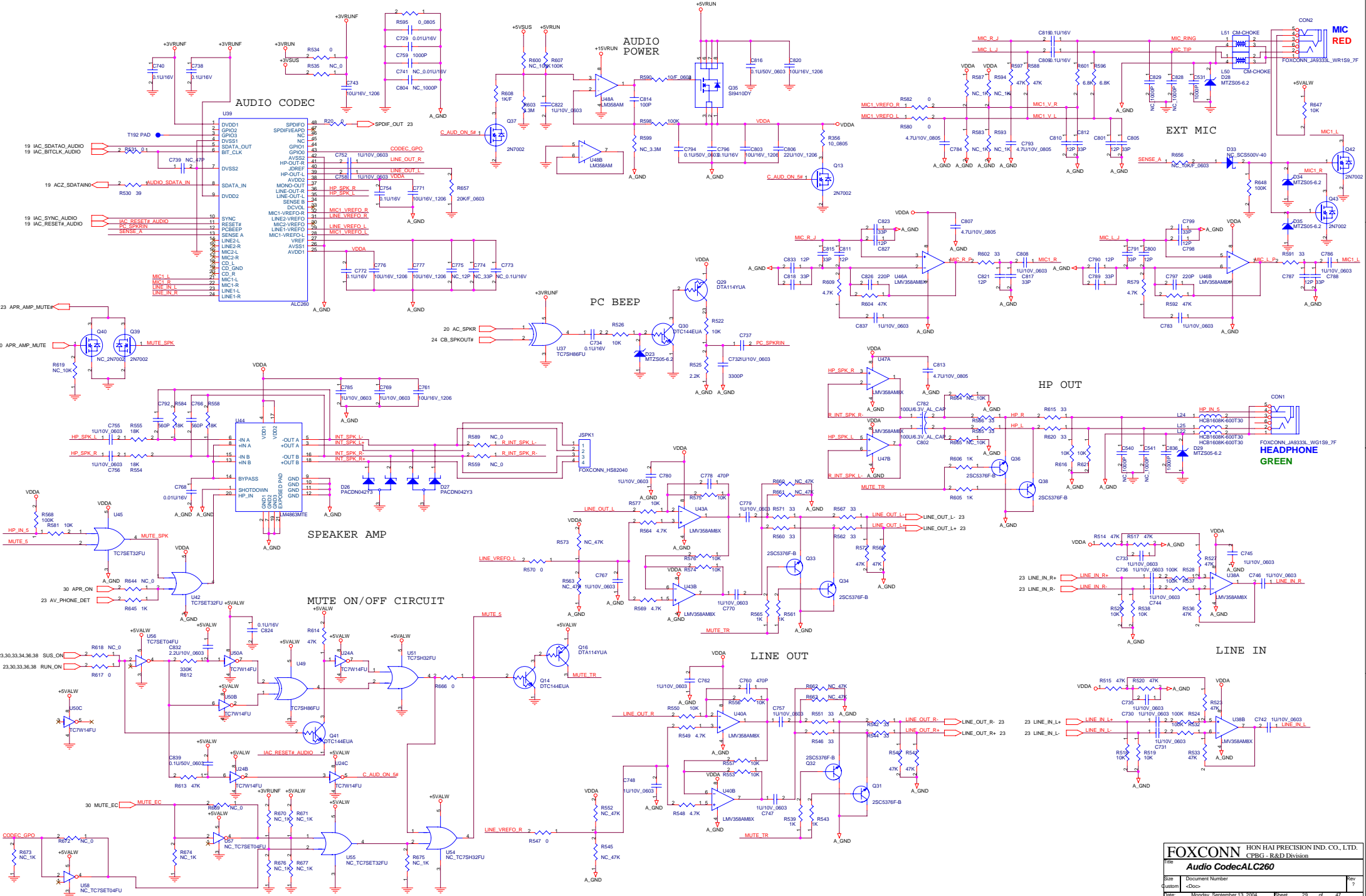


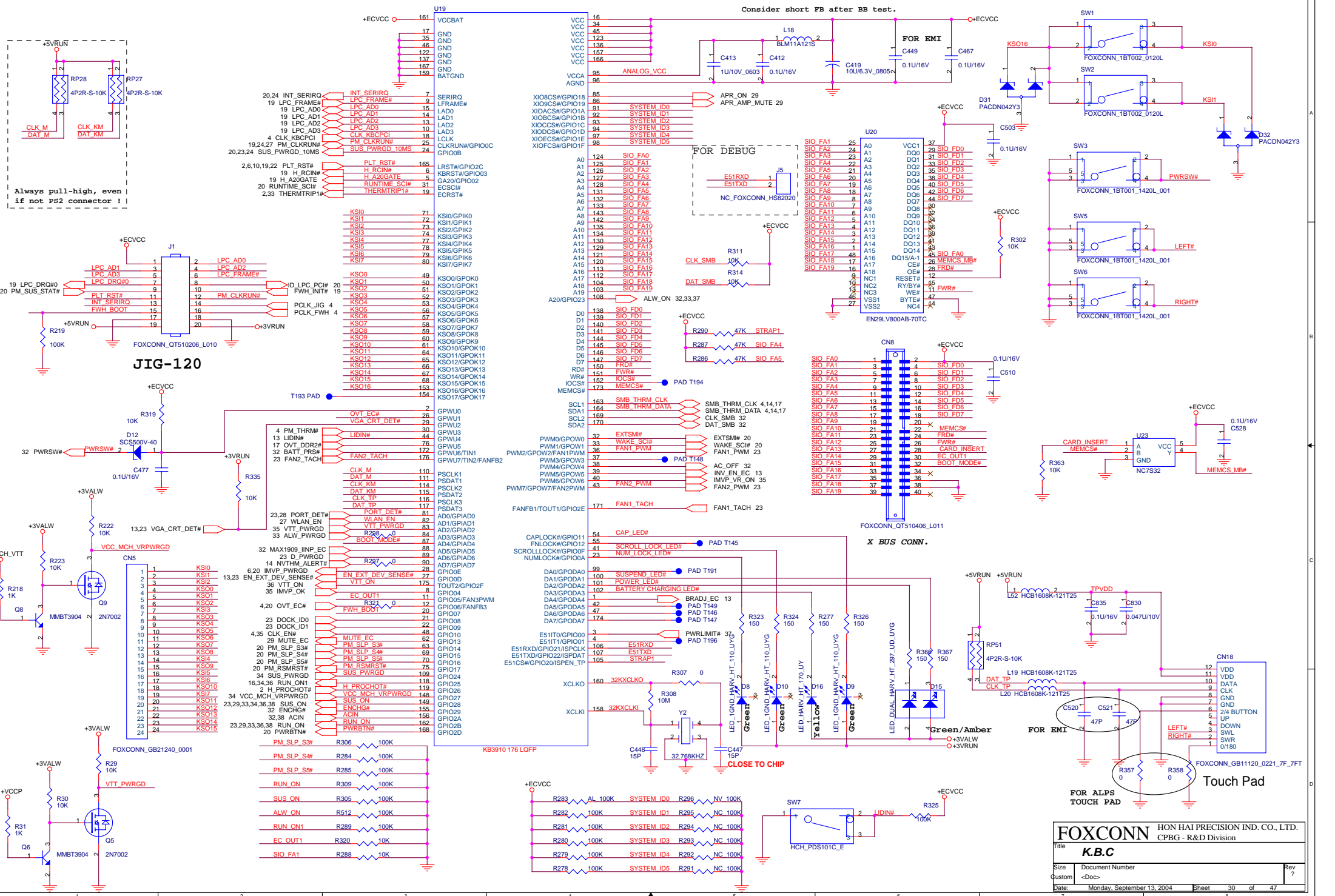




Match trace length
 LAYOUT NOTES:
 Match total length of chip side Rx and Tx pair traces +/-50mil
 Match length of cable side Rx and Tx pair traces +/- 50 mil
 Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
 Keep 50mil space between pairs and other traces.Pairs are 100ohm differential,







Always pull-high, even if not PS2 connector!

JIG-120

Consider short FB after BB test.

FOR EMI

FOR DEBUG

CLOSE TO CHIP

FOR EMI

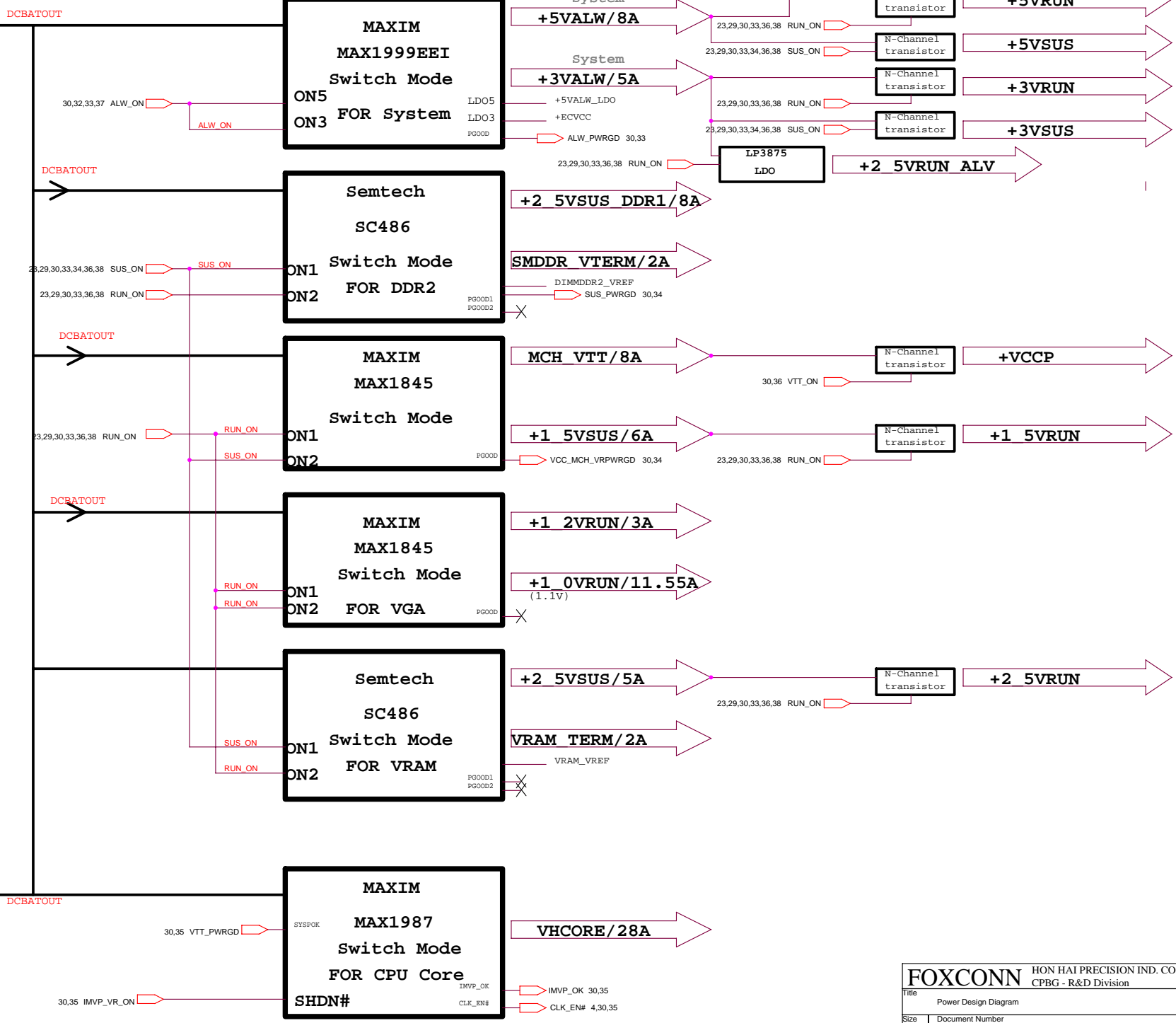
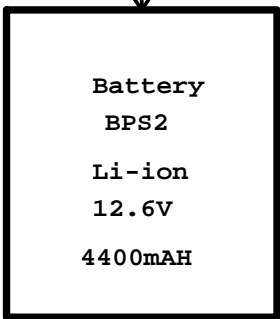
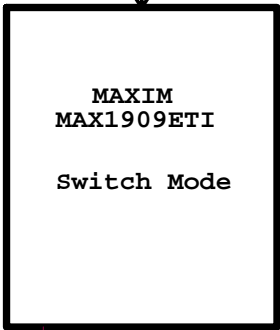
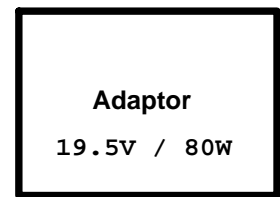
FOR ALPS TOUCH PAD

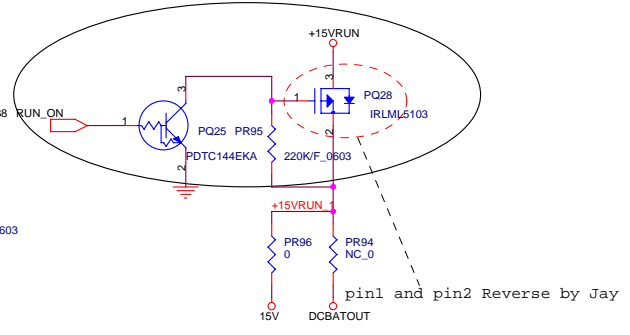
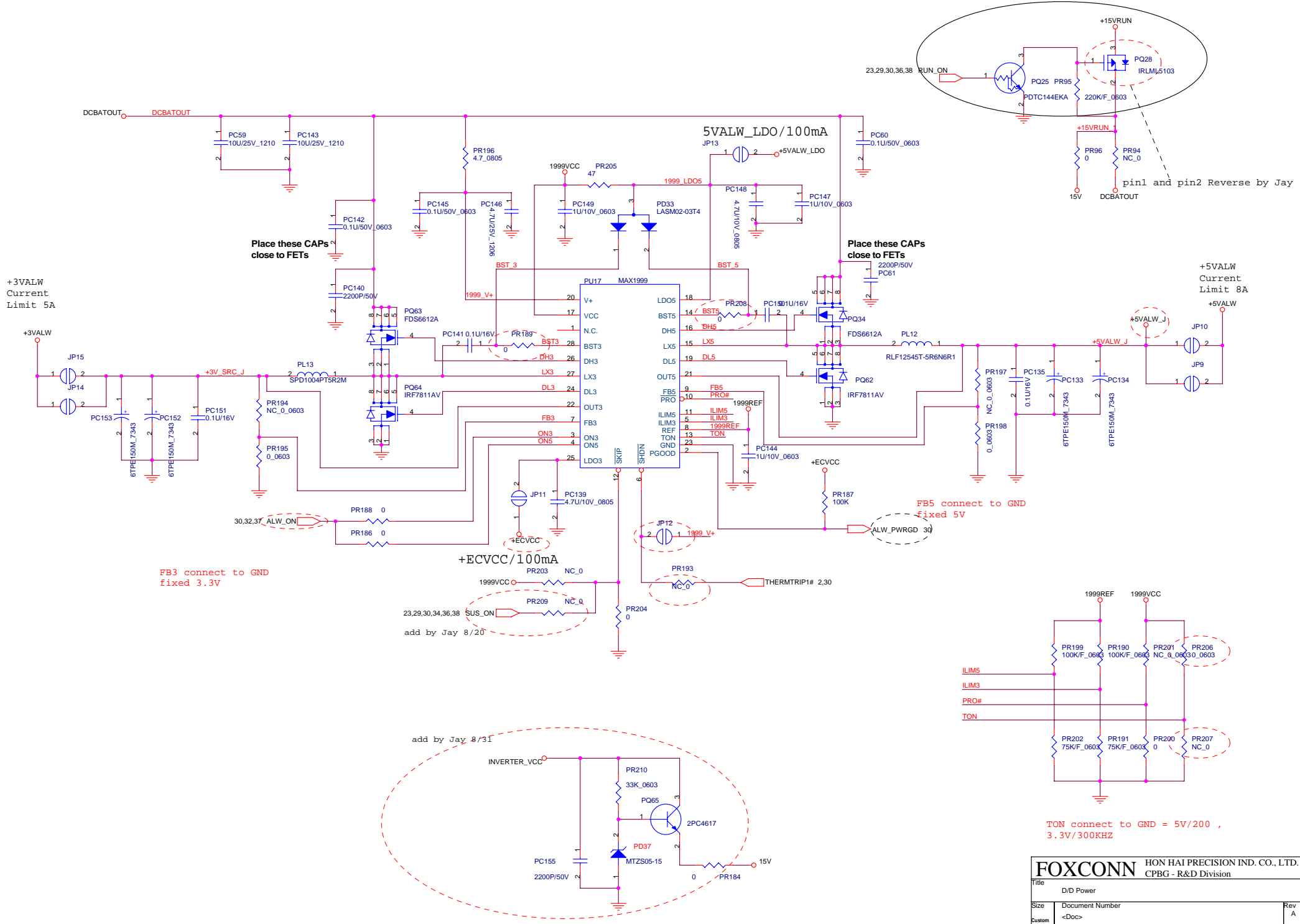
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

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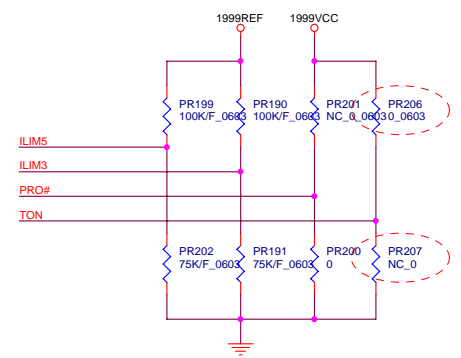


FB3 connect to GND fixed 3.3V

FB5 connect to GND fixed 5V

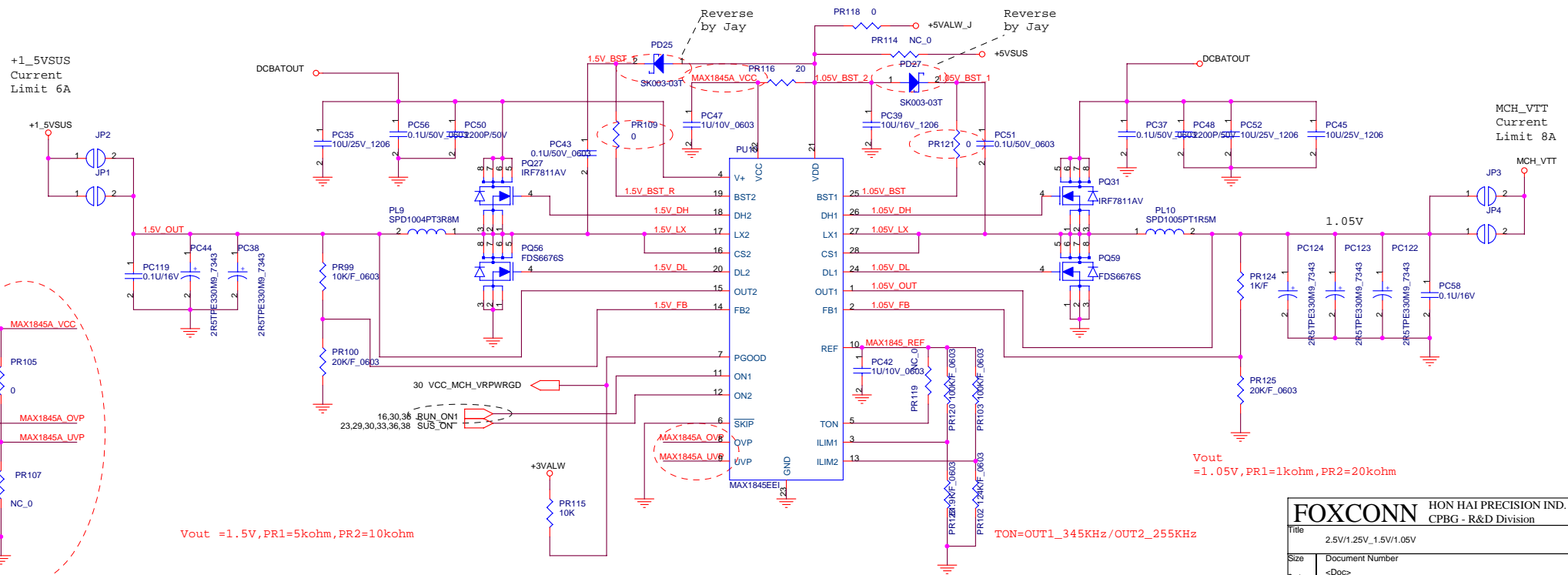
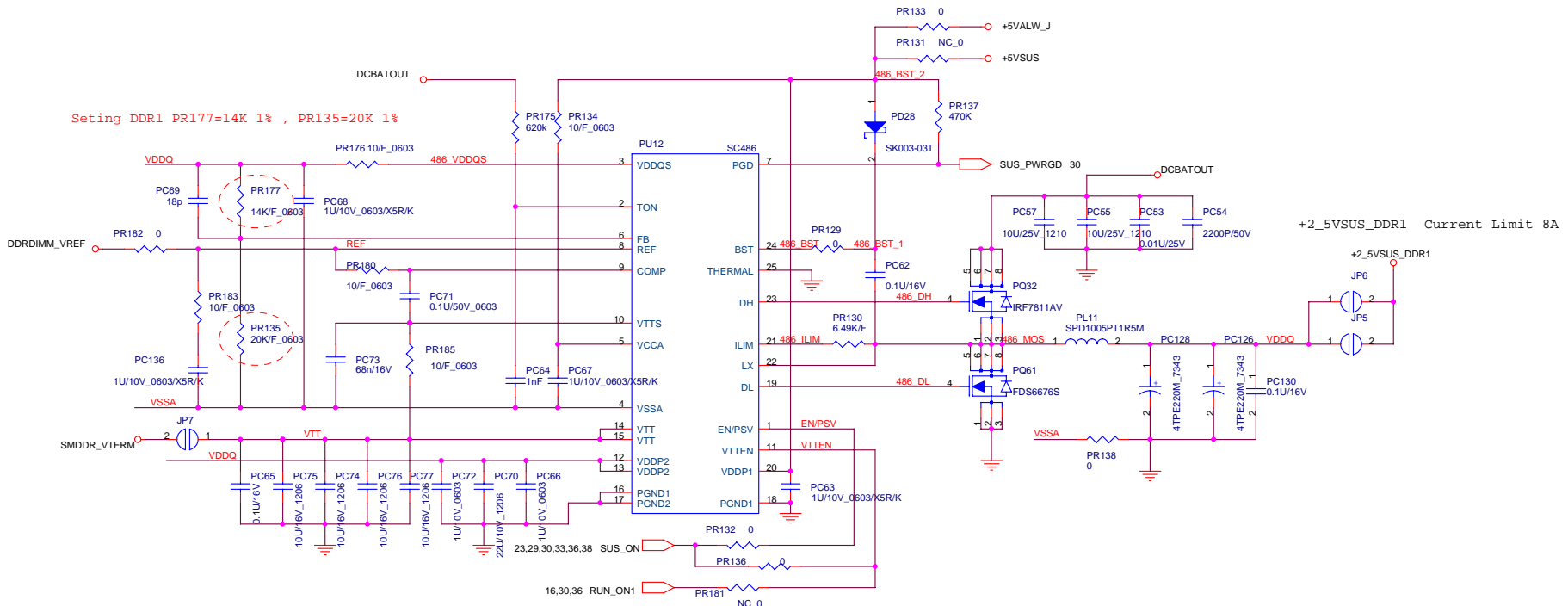
add by Jay 8/31

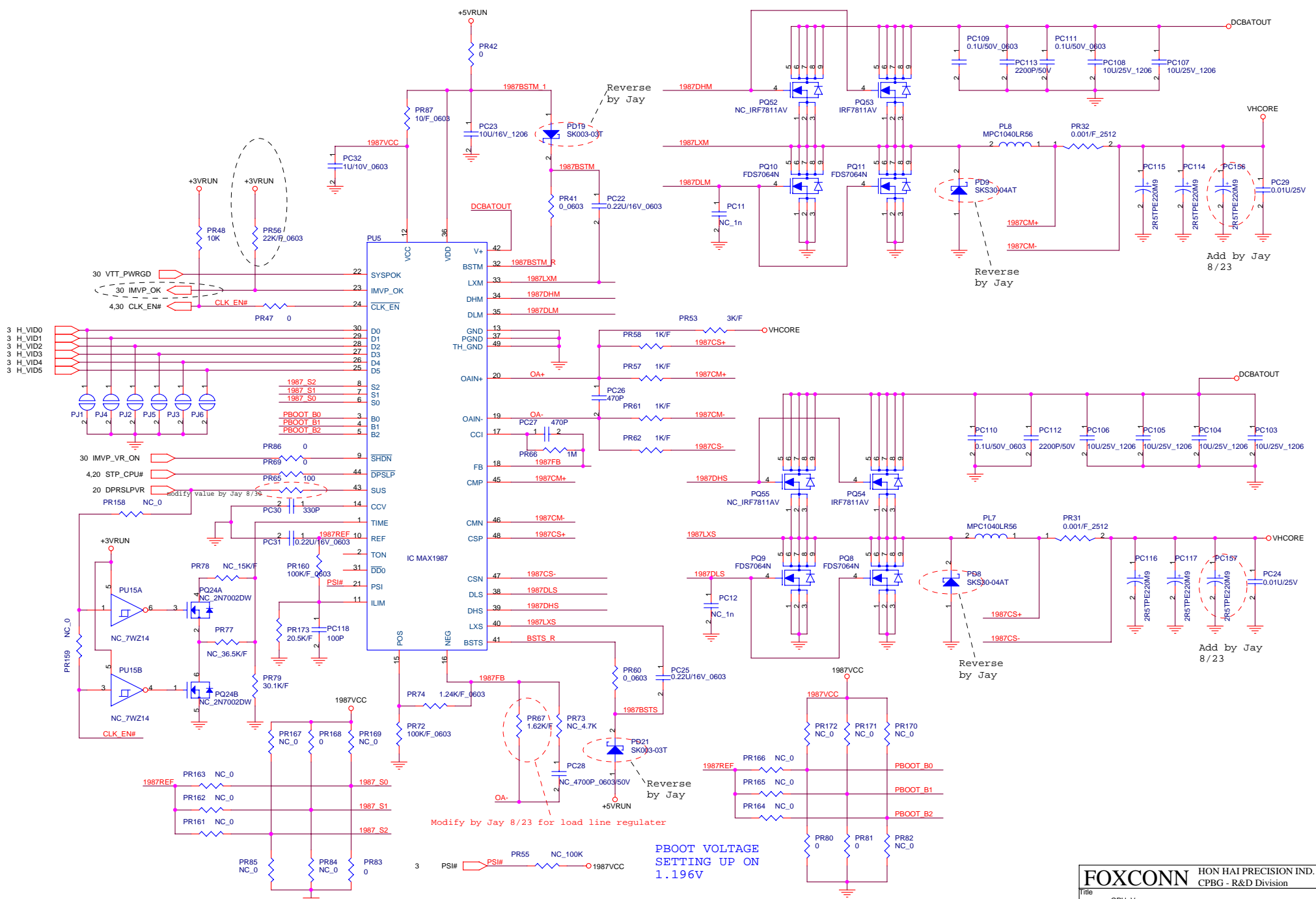
add by Jay 8/20



TON connect to GND = 5V/200, 3.3V/300KHZ

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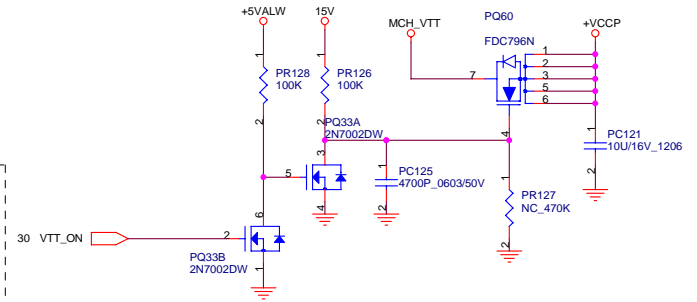
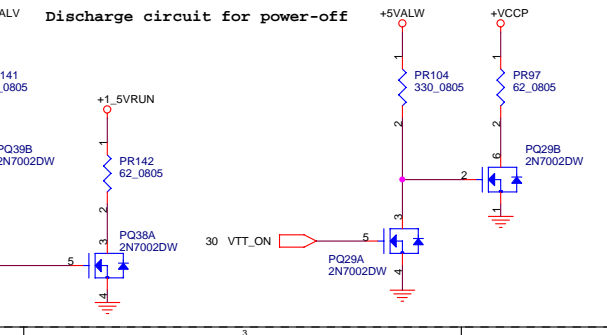
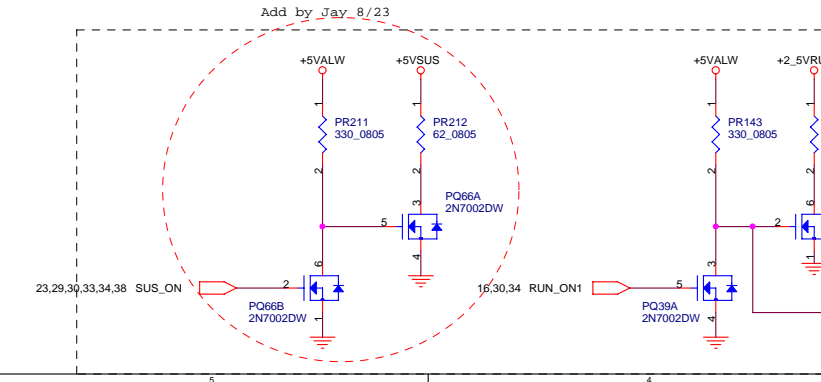
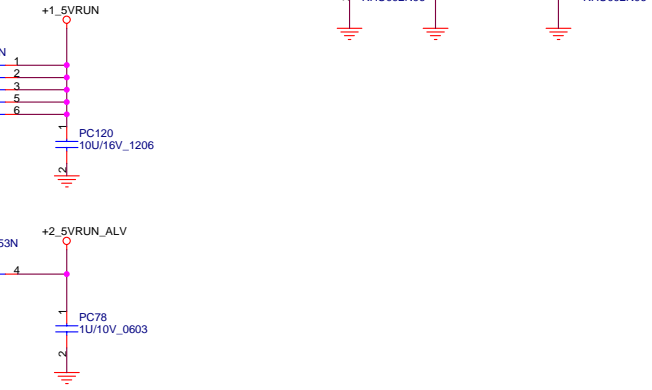
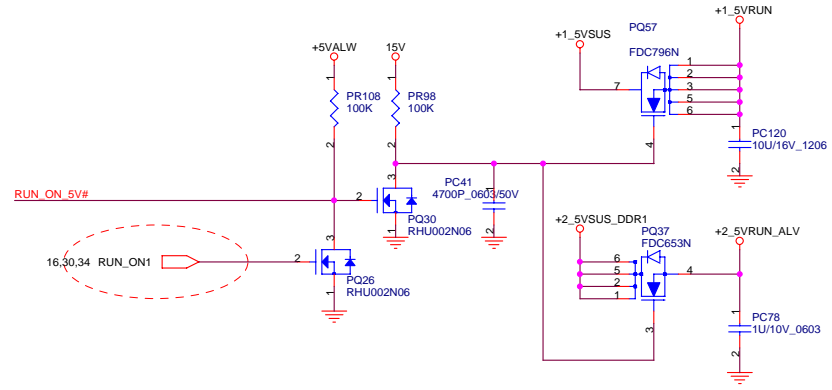
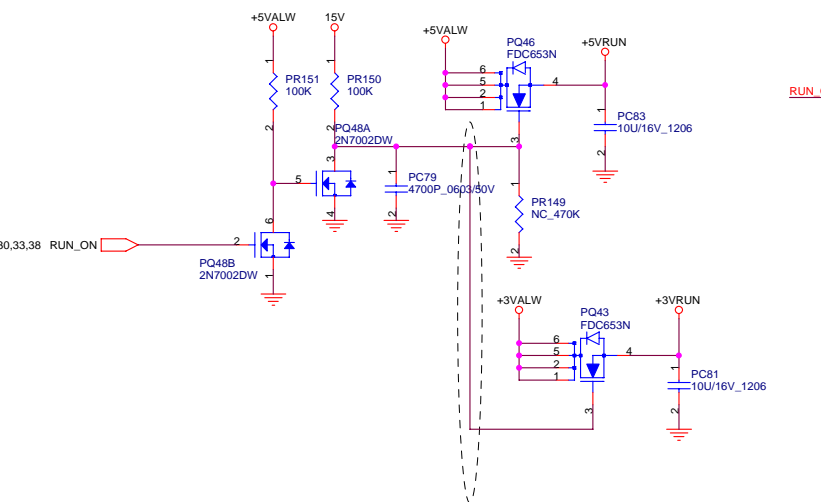
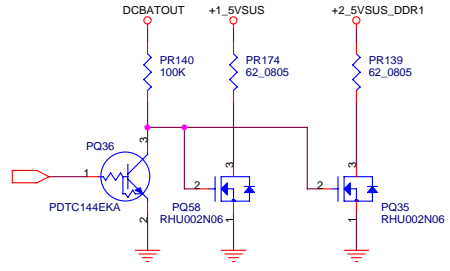
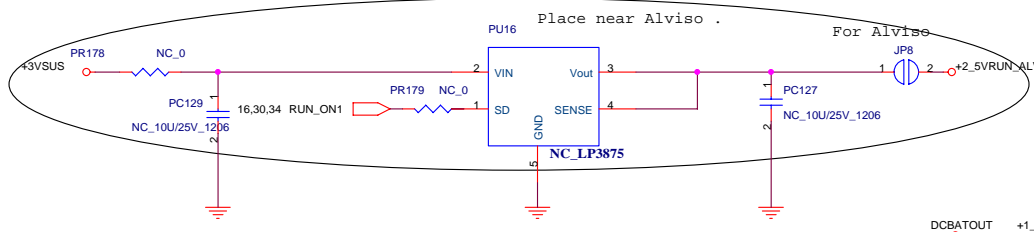
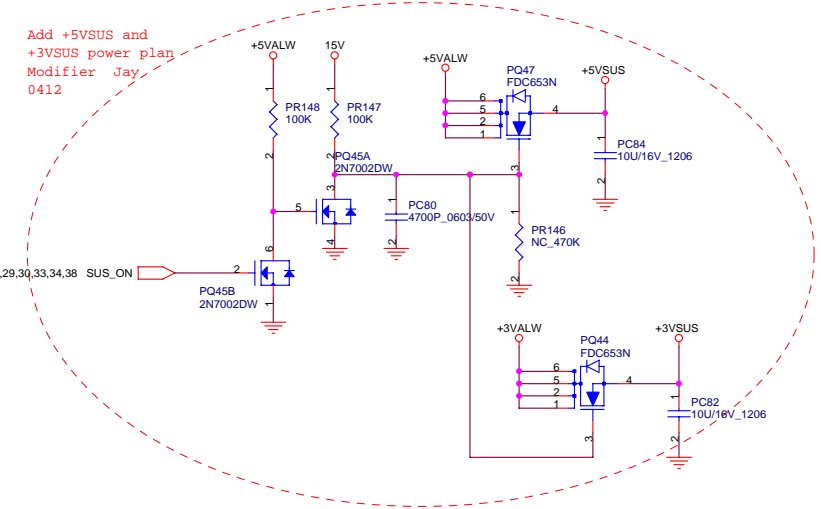


The C4 mode voltage is 0.748V TON = 300KHZ

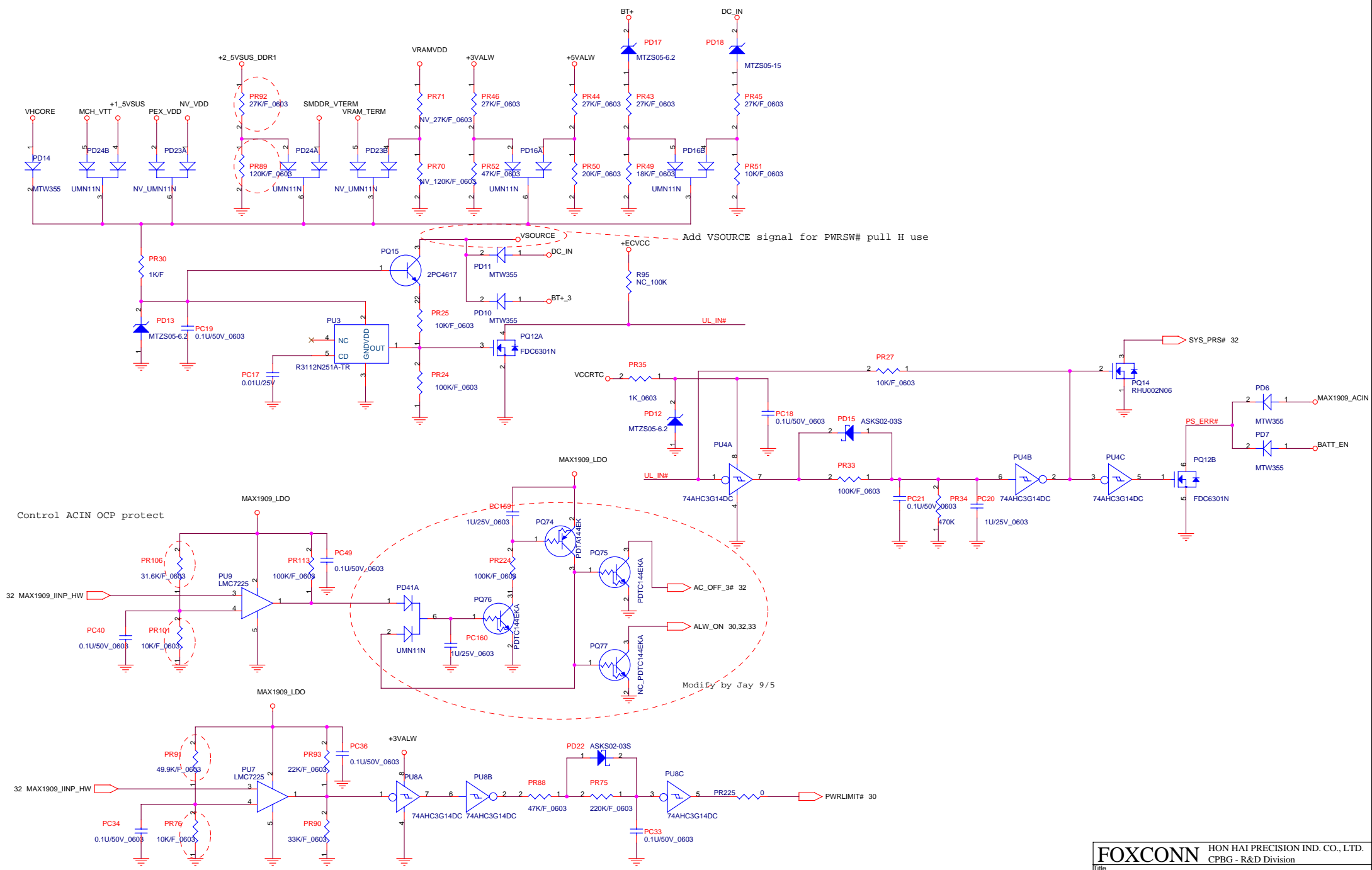
PBOOT VOLTAGE
SETTING UP ON
1.196V

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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Add +5VSUS and +3VSUS power plan Modifier Jay 0412



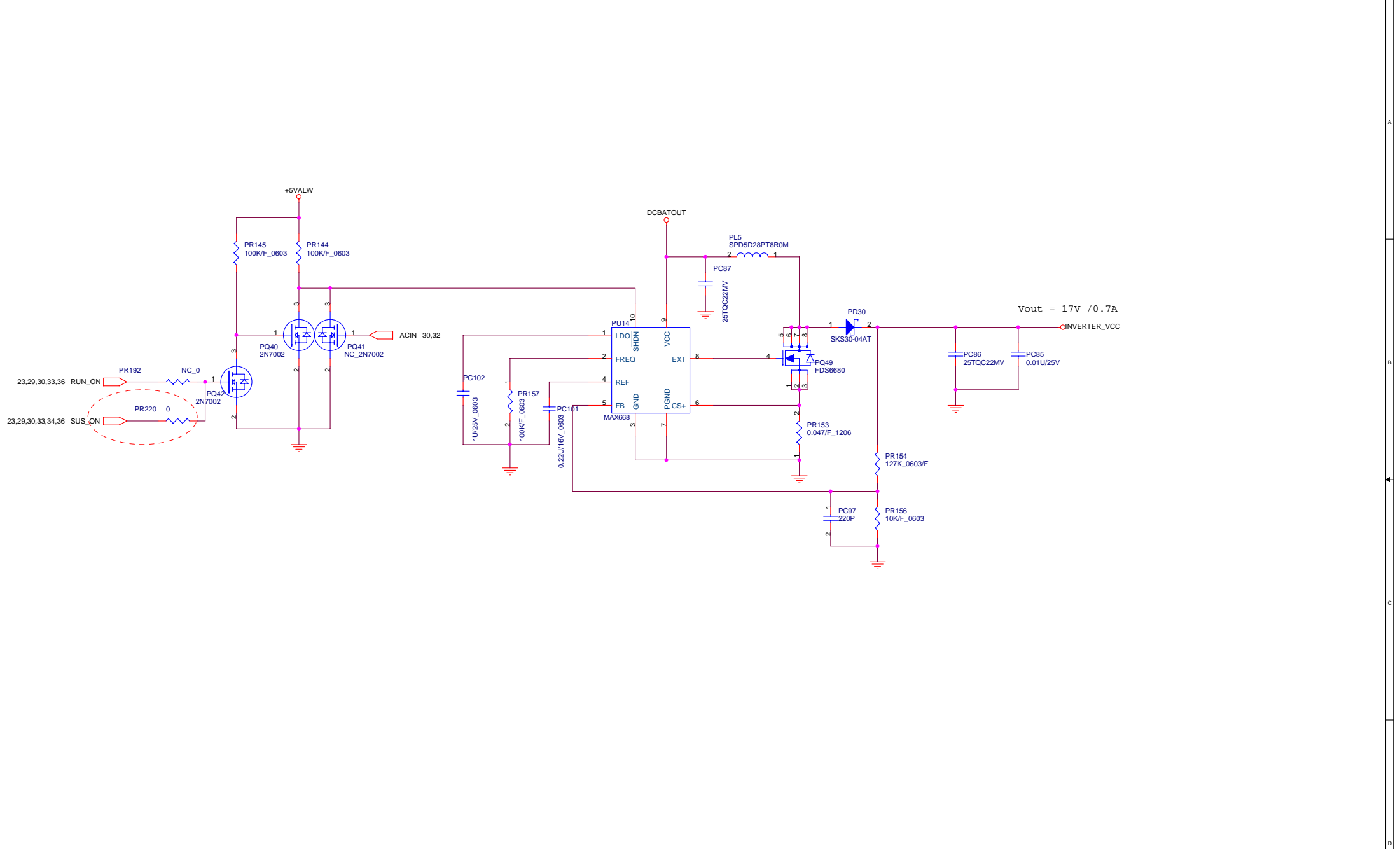
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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Control ACIN OCP protect

Modify by Jay 9/5

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HISTORY

REV 0.A: (2004/04/30)

P25: Add Label: TPAP0/N0, TPBP0/0. (Net_name change: N26323439 -> TPAP0, N26323537 -> TPAN0, N26323466 -> TPBP0, N26323428 -> TPBN0.
 P28: Add 4 resistors(R962 - R965, 0 ohm) between U23 pin1/2/5/6 and PR_MDI1+/-, PR_MDI0+/-.

(2004/05/03)

P11: R563/R564(Size 0603) changed to 0805 Size.
 P12: R565(Size 0603) changed to 0805 Size.
 P15: R612/R613(Size 0603) changed to 0805 Size.
 P22: Add R967(Size 0805)
 P23: Change R420-R423 connection from PR_MDI0/1+/- to MDIO/1+/-.
 P28: Change R420-R423 connection from PR_MDI0/1+/- to MDIO/1+/-.
 P29: R517(Size 0402) changed to 0805 Size.
 P29: D31 swap pin1 and pin2.

EVT board start .

(2004/05/12)

P35: Change VGA power solution for +2_5VRUN & delete VRAM_TERM (1.25V) for GDDR use 1.8V & 0.9V .
 P4: Remove Spread Spectrum IC (U3) & accessories for VGA LVDS , and Use IDT CV125 for U2 instead .
 P22: Remove CN5 & accessories for using SATA HDD .
 P28: Remove CN27 & CN16 for RJ11 is outside of MB .
 P28: Remove CON1 & CN25 & R968 for RJ45 is out of MB ; Change the LAN solution to Marvell 88E8036 .
 P30: Remove PS/2 function on MB , CN23 , L75 , C954 , RP92 , RP93 removed .
 P30: XBUS (CN22) connector & it's accessories removed for EVT board .
 Survey all connectors for correct type for EVT board .

(2004/05/14)

P35: Remain VGA power solution for +2_5VRUN on Alviso and add nVIDIA VGA power solution back (2.5V & 1.25V) for placement on power daughter board .
 P30: Add XBUS (CN22) connector & it's accessories back for it's for RMA .
 P.22 Remove C559-C561 , C920-C922 per no need for PATA HDD .

(2004/05/18)

P.13 Depopulate R229 & R233 for default 915PM
 P.35 Remove CN26 & CN27 for VGA power , and wait for new connector .
 Add Line-in / Line-out / SPDIF / POWER pin / and detect pins for Port Replicator
 P.22 Apply Marvell SATA to PATA for HDD.
 P.28 Add 078,079,R987 for PR mute circuits
 P.23 & P.28 Modify CN24 & CN25 for LAN use 8-pin CONN .
 P.28 Change LAN solution to RTL8101L .
 Use LDO for Alviso 2.5 V , +2_5VRUN_ALV , for nVIDIA use power daughter board .

(2004/05/19)

P.32 Change DC_IN connector to molex_53259_0220
 P.30 U34 change flash socket to flash IC : EN29LV800 footprint TSSOP_48P_20_787X472 .
 P.30 Remove CN22 , C953 , R700 , U41 , C952 , for no place for XBUS connector .

(2004/05/20)

P.13 Correct CN1 footprint to FOXCONN_QTSONNNA_0001 .
 P.22 Remove LED1 R631 Q47 because the QDD LED is not necessary on EVT board .
 P.13 Depopulate R576, R580, R584 for default is 915PM .
 P.29 Change SPK1 to 2-pin CONN. * 2 , FOXCONN_HS82020 , SPK1 & SPK2 .
 P.30 Change the footprint of SW8 to HCH_CLS_020A .
 P.27 Change the footprint of SW1 to HCH_RST_1202 .
 P.25 Change CN20 footprint to molex_52465_1091 for MS CONN. and remove R402,R404,R719-R722,C1101,C846,C1102 , because they are on the MS daughter board .

(2004/05/21)

P.04 Add RP97 to 33 ohm resistor.

(2004/05/24)

P.04 Add C1151-C1153 , NC , for EMI reserved circuits .
 P.13 Add C1154-C1157 , NC , for EMI reserved circuits .
 P.23 Add C1158-C1163 , NC , for EMI reserved circuits .
 P.29 Add R988 , for EMI reserved circuits .
 P.39 Add D38-D41 , for ESD protect circuits .

(2004/05/27)

P.13 Depopulate R585 , R587-R591 , R593 , R594 , R596-R603 for default using 915PM + NV .
 P.13 Change L30 , L32 , L33 to BLM11B750SB for 0603 package .
 P.23 & 30 Add R989-R994 , C1164-C1167 , Q80 , J6 for 2nd FAN .

(2004/05/28)

P.22 Change the footprint of HDD connector , CN5 , to SL56221-T4 .
 P.22 Add C1168 & L90 for 88SA8040 / Si13811 option
 P.30 Connect ID_LPC_PCI# to pin 8 of J5 , & remove T260 for debug output to 80 port selecting option by JIG-120 plug .
 P.22 Connect CSSEL2 to GND by R995 for CD-ROM is Master by default
 P.22 Delete SW18 & SW19 for layout require ; add R996 -R1001 to replace SW18 & SW19 .
 P.20 & 28 Change LAN solution to Intel 82562ET
 P.23 Remove CN25 for LAN 82562ET near Port Replicator .
 P.23 Change footprint of CN12 to FOXCONN_UV31413_Z6_TR
 P.23 Add CN23 , 24 for VGA power board , footprint : FOXCONN_QT600706_2101 .

(2004/05/29)

P.30 & 38 For Power limit circuits , remove T264 , add PU17 , PU18 , PC185-187 , PD38 , PD38 , PR697-PR702 .

(2004/05/31)

P.14 Change U11 to MAX6647 , and footprint to USOP_8P_26_118X193 for different SMBUS address from MAX6657 .
 P.14 Change U70 footprint to QSOP_16P_25_193X236 ; U72 to SSOP_48P_25_624X405 .
 P.25 Change CN20 footprint to FOXCONN_QT800101_1210S for MS connector .
 P.22 Correct CN5 footprint to SL56221-T3
 P.14 Correct U11 footprint to USOP_8P_26_118X193 .

(2004/06/1)DCDC modify

Reverse Pd11,12,13,14,15,16,17,18,19,20,21,22,23 pin define
 Change PC73,PC162 value from 47p to 0.1u/10v
 Remove PD9,PD10,PC37 and the 15V net change to DCBATOUT
 Reverse P082 pin1 and pin2
 Move PR65 to PR176,PR191 to PR192,PR79 to PR181,PR175 to PR174
 Change PL6 value from NC125RT-B4R7M to RLF12545T-5R6N6R1
 Add power limit circuit on P.38

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(2004/06/1)

P.30 Change CN34 from BIOS flash to BIOS socket , footprint : EN29LV800AB-70TC .
 P.13 Change LVDS option resistors from single chip to resistors arrays ; remove R206,R207,R209-R212,R214-R219,R221,R222,R224,R225,R585,R587-R591,R593,R594,R596-R603 ; add RP98-RP113 , and depopulate the odd reference .
 P.10 Remove R703 & R704 for default NV4X family
 For better power plane , remove the unnecessary resistors : R526-R528,R624-R627,R629,R630,R726,R740,R741,R865-R874,R884-R886,R888,R889,R899,R900,R967 .
 P.28 Change the package , from C0603 to C0402 : C1172,C1169,C1179-C1184,C1189,C1190 .
 P.28 Change the package from C1210 to C1206 : C1142 .
 P.13 Change CN1 footprint to , FOXCONN_GS12401_1011 ; and rearrange pin assignment for it .
 P.28 LAN change list :
 +3VALW to +3VSUS ;
 U72 : pin 28,29,30,41 open ; pin 21 connect to GND ; remove Q81 , R1028 .
 Delete R1029,R1030 ; add R1033-R1036 .
 Change R1025 to 100 ohm .
 Delete R1026,1027,C1177 , add R1037 .
 Delete R1019-R1022,C1174,1175,R1002-R1004,R1016,R1023,R1005-R1007,R1012 .
 Follow Intel reference design : del R1008-R1011,C1190 ; change R1014,R1015 to 75 ohm , C1178 & C1179 to 4.7U .
 Follow check list Rev:1.6 : Change C1173 to 1500P .
 P.19 & 27 Change Wireless LAN IRQ routing to INT_PIRQ# per MOR request .

(2004/06/2)

P.22 Change the footprint of HDD connector , CN5 , to SL56221_T6 .

(2004/06/3)

P.6 Place R567,R570,R571 to close Alviso , and depopulate them for default is NVIDIA VGA , refer to REF NO. 15680 Figure 96 & NVIDIA layout guide DG-00969-001_v05.pdf , change R235,R237,R241 to 75/F by default is NV .
 P.13 Add R198-R1041 , C1190-1094 for Alviso CRT ESD protection recommendation , REF NO.15680 Figure 96 & 97 ; and add option for NVIDIA & Alviso graphics .
 P.28 Base on Intel Alviso Checklist rev1.601.doc, change R1037 to 121 ohm 1%
 P.25 Change CN20 footprint to FOXCONN_OT810200_1100 , 20 pins , and connect MDC signals on the connector ; remove CN10 for it's on the MS/MDC daughter board .
 P.30 Add CN25 , C1195 for X bus CONN footprint FOXCONN_OT510406_L011
 P.30 Change footprint of CON2 to FOXCONN_JA933L_WG1S9 , CON3 to FOXCONN_JA933L_WR1S9 .
 P.16 Add CN26 and CN27 for VGA power daughter board .

(2004/06/3)DCDC modify

P.32 Add DIAG process require If AC_OFF is low level, system power source comes from AC-adaptor. If AC_OFF is high level, system power source comes from battery.
 Change DDR2 solution to Sentech SC486
 Del 1.0V and 1.2V , 2.5V & 1.25V , move to daughter board

(2004/06/4)

Change footprint for smaller PCB pad for layout space : c0603 to c0603_mor ; c0805 to c0805_mor ; c1206 to c1206_mor ; c1210 to c1210_mor ; r0603 to r0603_mor ; r0805 to r0805_mor ; r1206 to r1206_mor .
 P.23 Remove C1164 , and correct VCCFAN1 to FAN2 CONN. to VCCFAN2 .

(2004/06/7)

P.13 Correct the net name on two side of L28 & L29 .

(2004/06/7)[DDR II --> DDR] modify

Modify +1_8VSUS to +2_5VSUS_DDR1
 P.34 Change PR712 , PR717 value for DDR +2_5VSUS (When change to DDR2_PR712= 5.23kohm , PR717=23kohm) ; Add pin 25 on SC486 (PU19.25) for thermal pin .
 P.37 Add PR726 & PR727 to modify the OVP for +2_5VSUS_DDR1 from +1_8VSUS .
 P.10 Depopulate R87 for default is DDR .
 P.17 Change DDR II connectors to DDR connector , and add T306-T321 .
 P.6 For reserved circuits for SMDDR_VREF , remove C99 and Link C98 to Alviso pin AF37 & AD1 ; depopulate R127,R129,R939 and add R1045 to link SMDDR_VREF to DDRDIMM_VREF ; Delete C918 . So that we can use Vref from SC486 .

(2004/06/8)

P.29 Change Q58.2,R790.2,C998.2,U47.4,U47.5 connection to digital GND from AGND ; and link U47.6 & U47.7 .
 P.3 Modify the block diagram : FAN for VGA ; LAN ; add LAN switch ; 400/533 MHz DDR(II) to 333 MHz DDR ; 3 thermal sensor for CPU/NB,VGA & DDR .
 P.29 Swap D30.1 & D30.2 for layout .
 P.29 NC Q87 & R987 per MOR/Nishio request , no need EC control .
 P.29 MUTE_5(R861.&R830.1) change to MUTE_TR per MOR/Nishio request for transistor need enough current to operate .
 P.3 Remove R22 & R23 , fix on +1_SVRUN , per 6/5 Doi san : MS01 don't need to work with Dothan A-x step. This reserve CPU VCCA 1.8V connection is no longer need .

(2004/06/9)

Add C1196,C1197,C1198 & R1042 for EMI requested .

(2004/06/10)

P.22 Remove SATA bridge for MOR request , and use master PATA HDD , slave PATA CD-ROM , add R1043 .
 P.19 Remove C511-C514 for no more SATA needed , and add TP : T302-T305 .
 P.36 Change the output of PQ59 from +2_5VRUN to +2_5VRUN_ALV .
 P.30 Correct the CN21 pin NO. from 28 to 24 .
 P.29 Add R1044 for pull high of APR_AMP_MUTE# .
 P.29 Correct *Q78 to Q78 .
 P.23 Change the position of C1158-C1163 location to near USB connector .
 P.21 Change U17/G8 net name to +1_SVRUN .
 P.29 Change D30.3,D31.3,C993.2,C994.2,C995.2,D27.1,C1043.2,C1044.2,C1045.2,D29.1 connect from DGND to A_GND by EMI suggestion .
 P.23 Change CN11.23,CN11.26,CN11.29,CN11.54,CN11.57,CN11.60 from AGND to GND for no AGND guard will be routed to PR by Ziv discussed with Nishio san .
 P.23 Remove C1158-C1163 per MOR/Baki san requested .
 P.23 Del R1044 per Nishio san mail : the Resistor will be added on PR .
 Change L13,L14,L18,L24,L25,L27-L29,L31,L34,L35,L59,L69,L82,L85,L86 from BC-120-OHM to BLM11A121S , footprint R0603_MOR ; L14 & L70 need to check the current over 200mA Bead .
 P.29 Change D30.3,D31.3,C993.2,C994.2,C995.2,D27.1,C1043.2,C1044.2,C1045.2,D29.1 connect from A_GND to GND by Nishio san suggestion .

(2004/06/11)

P.30 Add U74,R1046,C1199 for the XBUS switching . Change U34.26 to MEMCS_MB# .
 Change SW9.10,14,15,16 footprint from FOXCONN_1BT002-01200 to FOXCONN_1BT002_01200 .
 P.32 Change PCON2 footprint from FOXCONN_BP34063-P4211 to FOXCONN_BP34063_P4211 .
 P.4 & P.28 Change Y5 & Y7 to 14.318MHz/20pF/+30PPM & 25MHz/20pF/+30PPM , footprint : CRYSTAL_2P_150_197X126 .

Check & modify per MOR recommendation document : MS01_EVT_20040604B_a-doi.pdf

P.2 C878 is not necessary , remove it .
 P.2 Delete R13(0ohm) and short H_STPCLK# to U1.C6 pin.
 P.3 R22 & R23 deleted on (2004/06/8)
 P.4 Delete Pull-Up, Pull-Down options for CPU_BSEL1,0 and SELPSB0_CLK. - Delete R34-R38 . The option will be dependent on B-step,CPU .
 P.4 C860 and C861 have no meaning,Delete them.(If high frequency bypass capacitor are required, it should be being inside of the inductor.)
 P.4 This note "For 915GM" should include not only RF7 but also RF97,RF6 , R547 and R548 is only for NV43M(915PM).
 P.6 Delete R81 and R83 connect CPU_BSEL1,0 to Alviso B15/G14 directly.
 P.6 Delete C984 and add T322 .This is only for backup.
 P.6 By design guide 17.4.2 GMCH Miscellaneous signals, SDVOCTRL_DATA can be left N.C . Delete R552 and add T323
 P.6 Q42 can make BRADJPWM as N.C. So R101(0ohm) is not need. Short it . Also , delete R102 and short it . Depopulate R553 R554 , R106 for default is 915PM & NV43M
 P.6 R943 is same connection as R33.R943 is same connection as R674,So, Delete R942 and R943 and change the resistor value of R942 and R943 for 915PM or 915GM/915GML .
 Change R33 & R674 to 0 ohm depopulate R32 & R673 for default is NV43M
 P.6 MS01 will not use 1.5V for Alviso VCC. Delete R523 and make CPG18 TP. Add T324 .
 P.6 I wonder if LDDC_CLK and LDDC_DATA should be N.C. when these are not used. Please check design guide 17.4.2 GMCH Miscellaneous signals.
 Alan , Change " For 915 GM " to "For EDID LCD PANEL "

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HISTORY

(2004/06/11)

Check & modify per MOR recommendation document : MS01_EVT_20040604B_a-doi.pdf ~ CONTINUED .

- P.13 Add name to these NV's LVDS signals to easily to check the trace length in allegro data.
- P.13 & P.6 What is the purpose of these R608-R611(0ohm)(VGA_DPCCLK/DATA and NV_HSYNC/NV_VSYNC) resistors? System with 915 PM will never mount NV46M. It seems redundant. If the purpose is to reduce the brunch of signals in artwork, you should pay attention for the placement. Alan ,Delete R608 & R609 ; depopulate R90 & R91 for default is NV43M
- P.13 Min Vin of U35,U36,U37 (NC7S8B357) is 0.7VCC. PORT_DPTH is 3.3V, lower than the spec. ; Alan ,Delete R566 and add D42,R1047,Q82,Q81 for the voltage level shift on DOCKED# link to U35.1,U36.1,U37.1 .
- P.13 R1039(0ohm) could never use. Delete +3VRUN connection and R1039 and short R1038.As for 915GM, you could never bypass the buffer for HSYNC/VSHNC because 915GM signal level is 2.5V level shift is always required. So the voltage of PR_HSYNC/VSYNC are 5V.As for 915PM, nVidia reference circuit use 5V for EDS diode power. Alan Delete R1039 and R1038 .
- P.14 D33 and D3 are owing same function. If you connect here, D33 can be omitted, Alan delete D33 .
- P.14 What is the purpose of this resistor R257(0ohm)? It seems not need, Alan delete R257 .
- P.20 To support wake from S3 with LAN, LAN_RST# must be released(High) in the S3 state. And this signal is input of ICH6-M. Alan delete R621 & T229 and change connection to U32.1 GPIO .
- P.20 Signal Direction is wrong. EP_DIN is input of ICH6-M. Alan correct it .
- P.21 U17.G8 +1.5V_ICH is wrong, change net name to +1.5VRUN .
- P.21 To support wake from S3 with LAN, this power source must be supplied even in the S3 state. U17.G10, U17.G11 change connection to +1.5VSUS .
- P.21 To support wake from S3 with LAN, this power source must be supplied even in the S3 state. U17.A13, U17.F14 , U17.G13,U17.G14 change connection to +3VSUS .
- P.28 R1031 can be deleted. Connect U73 6pin ORG to +3VSUS directly.
- P.28 Connection of EEP_DIN and EEP_DOUT is wrong. Signal direction of pin4 is also wrong,U73 DO is output.ICH6-M has internal pull-down for EEP_CS while LAN_RST# is Low. So Pull-Down R1032 seems needless. Alan modify and delete R1032 .

Check & modify per MOR recommendation document : MS01_EVT_20040604B_a-doi.pdf ~ END .

- P.13 Change C294-C296,C298,C300,C306,C285,C289 & JVGAI.5-8 from GND to E_GND .
- P.23 Remove C582-C588 , for these not necessary
- P.37 PR726 & PR727 ,change footprint to R0603_MOR .
- P.17 Swap CN2 & CN3 for DDR A channel & B channel ; for channel A should be closer to Alviso .
- P.29 Change C1061 from A_GND to GND by Ziv
- P.6 & P.20 Delete DMI bus signals Port 2 & Port 3 , for DMI X 2 only need Port 0 & Port 1 . Add T325-T340 .
- Remove +2_VSUS power on board change net of CN27.3 & CN27.4 net to +2_V5VRUN ; Delete CN26.17 net ; Delete PQ65,PC173 ; Change OVP net +2_V5VSUS on PR673 to +2_V5VRUN .
- P.13 Change DACA_HSYNC pin NO. to AF10 DACA_VSYNC pin NO. to AK10 on U6F to fix CRT issue on NVidia chip .
- P.13 Change U17.A24 from +3VALW_ICH to +3VALW .
- P.6 & P.22 Remove net : CLK_PCIE_SATA & CLK_PCIE_SATA# and SATA_LED# , remove RP4,R30,R31,R742 ; disconnect SATA_LED# on CN6.14 . Add T341-T345 .
- P.29 The two arrows of IAC_BITCLK_AUDIO and IAC_RESET#_AUDIO , modify them
- Remove M_ODT0-3 , M_A_BS#2 & M_A_BS#2 , Add T346-T351 . Delete R299,R300,C475,C476,RP67,R303 per DDR1 can be NC - Doi san informed .

BB board rework implement , file name : rework_notice_040529.doc

- Rework number 1**
- A.Remove R576,R580,R584 --> already done .
- B.Remove R53,RP7,R32,R33 --> Depopulate RP7,RP97,R32 and change R33 to 0 ohm for NV
- C.Remove U3,R46,R61,R66,R673,R674,C69,E72 --> EVT removed SSCR MK1493-05G ,and R673,R674 have been rearranged .
- D.R588,R589,R590,R591,R593,R594,R596,R597,R598,R599,R600,R601,R602,R603 --> LVDS option R rearranged .
- E.Remove R563 --> will remove in MEP circuits remove part .
- F.Remove R229,R233 --> Already Removed
- G.Remove R553,R554,R91,R106,R101,R90,R102,R98,R99,C785,L69,C786 Short C143 -- > C143 mount 0 ohm for default is NV . 915PM: R133 NC, C143 OR ; 915GM: R133 OR ,C143 mount 0.1U/16V .

Rework number 2 Should be checked when using 915GM ; conflicts with NV had been checked .

Rework number 3 P.30 Remove Q51 , add R1048 & Q83 for no VHCORE issue .

Rework number 4-6 EVT different from BB .

Rework number 7 C173 Already existed .

Rework number 8 Material issue .

Rework number 9 Material issue use the value on schematics instead of the rework parts , 3904 .

Rework number 10-11 EVT different from BB .

Rework number 12 Connect U3 pin9# to +5VRUN .

Rework number 13 EVT different from BB .

Rework number 14 P.29 Delete U54,U55 , Add U75 and rearrange U56 & U75 A,B,C link .

Rework number 15-16 Material issue .

(2004/06/14)

- P.17 Connect to CN3 M_A_A13 and M_B_A13 to CN2 per DDR1 can't be NC (20040614 added in history) .
- P.21 Correct net +3VALW_ICH on C577-2 & C558.2 to +3VALW for no more +3VALW_ICH net
- P.32 To reduce +EVCVCC routing to BATT_CONN. Change the ESD protector to PACDN042Y3 (20KV contact) . Delete D38 -D41 , Add D43 & D44 .
- P.17 Correct the M_CS#1 connected to CN2.122 to M_CS#3
- P.29 Change LM358AM to LMV358AM8X for U47,U48,U49,U51,U53,U59 and change VCC of U47 to +5VRUN from +15VRUN ,others remain VDDA for VCC on pin 8 .

(2004/06/15)From MOR - Doi san , file name : SchematicsComment20040611.xls

- P2. Delete R928 and Q72 .
- P3. "27.4/F" means "27 ohm @1% .
- P6. Change direction of CPU_BSEL0_1 .
- P.13 Connect the signal between R227 and R232 to D3.2pin .
- P.21 I measured the power consumption of ICH6-M. If VCCSUS1_5 is made by ICH6-M internal VR, Power consumption of ICH6-M in S0 state increased more than 150mW. So please consider if it is possible to provide +1_5VALW from external power source? (for DVT) --> list in issue tracker .
- P.22 Depopulate R995 for CD-ROM slave .
- P.28 Modify the signal direction of U73 .
- P.31 Delete +1_8VRUN in power diagram .
- ITEM 11 ~ 16 (regarding DDR1 signals) modified OK .
- P.13 Add L92 and change C278 to 0.1uF for Low Pass Filter for inverter need DC to control brightness.
- P.30 P.4 Change the JIG-120 pin assignment, add two signals "PCLK_FWH" & "FWH_BOOT" for FWH debug ; Remove T220 and change INV_EN_EC to U32.30 and reserve U32.20 for FWH_BOOT ; Add R1049 & C1200 for PCLK_FWH .
- P.13 Hsync is AF10 not AF1, Vsync is AK10 not AK1 ; modified OK .

(2004/06/15)

- P.25 Remove C1099,Q75,R944,Q76 and place them on MS daughter board , Connect CN20.10 to U21-8.F3 , Change CN20.17 net from GND to +3VSUS ; For simple power trace on M/B .
- P.30 Remove T263
- P.29 Add R1050 & R1051 for reserved circuits for save U49 component when U50 gain is 1.
- P.18 Change U5 footprint from FOXCONN_OT016-L010 to FOXCONN_OT51206-L010
- P.18 Swap the terminator of DDR1 per Layout request , file name : c720004-0615swap.zip ; delete RP80 , add R1052 .

(2004/06/16)

- P.16 Change CN26 pin define per VGA dauhter board change .
- P.27 Change U3 footprint from FOXCONN_AS0A226-S4 to FOXCONN_AS0A226-S4 , and correct the value to FOXCONN_AS0A226-S4 as well .
- P.11 Remove R563& C210-C211,C213-C215,C217,C221,C222,C229 and NVFBVDD net for no MEP circuits needed on MS01 . informed by Scott .
- P.15 Remove terminal resistors RP9-RP24 , RP29-RP34 for no need to reserve these resistors for VGA DDR over 300 MHz . informed by Scott .
- P.37 Correct PQ80 pin define and add R1053 for reserved circuits by Jay .
- P.30 & P.20 & P.23 & P.24 Change the enable signal to DEV_EN from EC , by connecting DEV_EC to U32.24,U44.1,U45.1,U46.1,U21.N5,U22.12,U17.V5 ; delete T215 add T352 .
- P.34 Add SUS_PWRGD net on SC486 to system.
- P.32 Change PCON1 footprint to JMT_A3963XR2_2P .
- P.29 R1050 & R1051 default is NC
- P.29 Change U47 to LMV358AM & power from +15VRUN for driving Q57 .
- P.20 & P.28 Add R1054-R1060 for Ethernet series resistors for MOR requested on EMI solution .

(2004/06/18)

- P.10 Add R1061 per NVIDIA recommended 6A for NV_VDD .
- P.15 & P.16 rearrange the net bus for VDDR
- P.37 Correct the footprint of PQ80 to SOT363 per layout inform
- P.34 Correct the net link of VTEN & EN/PSV for +2_VSUS_DDR1 should be controlled by SUS_ON for DDR & SMDDR_VTERM controlled by RUN_ON (SUS_ON reserved) for DDR terminal .

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HISTORY

(2004/06/18)

- P.33 Populate PR704 for default +15VRUN from DCBATOUT.
- P.25 Add R1062 near PCI7420 on MS_CLK net per MOR / Baki-san requested for reserved circuits on debugging MS function .
- P.34 PR 712 no 5% component , Leon prepare BOM for 1% , change the PR712 value to 40k2/F .
- P.20 Correct the direction of LAN TX & RX signals
- P.04 Correct the value of clock from IDTVCV125 / ICS954201BG to IDTVCV125 / ICS954206BG , for ICS954206BG has SCK function , ICS954201BG not .
- P.34 Change PCI92 & PCI93 footprint from C0603_MOR to C0805_MOR and value from 4.7u to 4.7u_0805
- P.14 Change connection of GPIO8 and MAX6647 ; change link from "R258.2 to U11.6" by "R258.2 to U11.4" ; for BIOS team recommend that can be controlled separately .
- P.28 Remove R1032 for ICH6-M has internal pull-down for EEP_CS while LAN_RST# is Low ; this should be removed on (2004/06/11) , but missed .
- P.34 Correct PC208 footprint to CI206_MOR
- P.14 Change X1 footprint to CRYSTAL_2P_150_197X126 ; X1 value change to L5030-27MHz/+-30ppm/20pF .
- P.04 Change Y5 value to L5030-14.318MHz/+-30ppm/20pF ; Y7 to L5030-25MHz/+-30ppm/20pF per correct BOM .
- P.30 Change KB_CONN. to FOXCONN GB21024_0001 per mechanical change .
- P.25 Remove R537 for this R should near MDC card on MS daughter board .

(2004/06/18) 20040617 - Doi-san mail title : RE: [MS01] Release EVT M/B schematics 6/16 .

Correct page 31 power diagram, MAX1987 IMVP_OK output signal name isn't IMVP_PWRGD, It is IMVP_OK

- P.20 Remove 077 for no need . BB reserved this for leakage reserved circuits , and test OK , no leakage from ICH6-M when S3 . informed by Dick .
- P.30 Add R1063 for FWH_BOOT per MOR / Doi-san request
- P.30 remove net : PR_CRT_DET# and replace with VGA_CRT_DET# ; delete U63,R894 . For PR VGA and MB VGA_CONN. can't plug at the same time .
- P.28 Do you decided not to delete R1032?(In the change history, this register had been deleted.) ; Alan , sorry ! I missed this, remove R1032 .
- P.32 For AC in issue, delete PR14, add PR730 , change PR7 value to 100K_0603 , and PR7 pull high change to MAX1909_LDO. by Jay .
- P.19 ECDC can't be powered off when battery only issue , Add P098, P087, PR728, PR729 to stop the reverse current. PUL1 is needed to stop the current from BT+ to DCBATOUT when battery only . by Jay .
- P.19 We will not use ICH6-M THRMTRIP# function. So let's delete R318 and shortit.Additionally R755's "*" is far from the parts, it is not easy to see the schematics. Please move "*" to right side of resistor. (You should not delete R315. It is still need.)
- P.18 When system memory is changed from DDR2 to DDR1, some signal termination reduced. So capacitor for DDR_VTERM also can be reduced. Alan : but the Alviso_Checklist_rev1_501.doc recommended 64 Capacitors for DDR . Please provide instructions of this
- P.30 In R1909 list, LEDs in page6 and resistance have changed. Please modify the schematics also. Rework in the ms01_system_rework_notice_040616.doc
- In Sonoma Platform Message of the Week WW23 and WW24, intel recommend to change the connection of CPUSLP# from ICH to Alviso.SO, please change the mount of R76 (Alviso) and R320 (ICH) from EVT. This change also need BIOS support. Please check the MOW and talk with your BIOS team too. Alan change the mounting of R320 to NC , and mount R76 .

(2004/06/18) BB board rework implement , file name : ms01_system_rework_notice_040616.doc

- Rework number 16**
Remove R142,R145,R148,R177-R180,R559,R561 Solder R140 / 10K_0402 fro Strapping erroron NVIDIA chip . Alan modified shcematics OK .
- Rework number 17**
Q75 is removed on MB schematics and will be modified on MS daughter board , reference is Q1 .
- Rework number 18**
Change LED power from +5RUN to +3RUN ; Change current-limited resistors from 330 ohm to 150 ohm . For D14,D15,D17 LED slightly light when LED off .
- Rework number 19**
Change LED power from +5ALW to +3ALW ; Change current-limited resistors from 330 ohm to 150 ohm . For D16,D20 LED slightly light when LED off .
- Rework number 20**
Rework issue .
- Rework number 21**
Already done on 20040616 and net name updated to SUS_PWRGD_2MS on 20040618 .
- Rework number 22**
Already done on 20040601 .

(2004/06/18)

- P.03 Remove C879-C900 for it's not necessary .
- Change the connection of U65.8 to +3VSUS and U65.6 & U65.7 short for the component recommend this . informed by David .
- Change the pin for MMBT3904 , Q2,Q38,Q85 , edit part to swap pin 1 & pin 2 . For the database is wrong , 3906 (Q75 on BB board) is the same thing
- Change name from DRV_EN to SUS_PWRGD_2MS for more clear on the net meaning -- EC turn this signal on for 2 ms later than SUS_PWRGD . informed by David requested by MOR / Doi-san .
- P.29 correct U50.L, shutdown should be high level . informed by Tim and check SPEC. OK .
- P.25 Fill the net name in the ILink symbol (CN12) .

(2004/06/24) Power

- P.32 Move PUL_P03,PR3 to charger output side to stop the reverse current by Jay .
- P.37 Add VSOURCE signal for PWRSW# pull H use on PD31.2 .
- P.32 Delete net "1909_CSIP" that is conflicting with "BT+_2";delete net "1909_CSIN","1909_BATT","BT+_3" that are conflicting with "BT+" .

(2004/06/24)

- P.30 Change J4 to 4-pin CONN.and add +5VRUN_GND net for debug board use .
- P.30 Modify the pin assignment for Elantech and ALPS touch pad ; Add R1064 & R1065 for ALPS touch pad reserved circuits .
- P.11 FBVD net for NV chip add "X1" on NC pins
- P.20 change net of IMVP_PWRGD for PWR0K should pull low ; no mount R525 for default IMVP_PWRGD pull low to GND . This net is output from EC .
- P.06 Change R100 from 255/F to 256/F per RDDP_REF 15680 & REF14511 is 256/F while Intel CRB Ver.1.501 is 255/F .
- P.30 Add R1066-R1068,Q85,Q84 for The VCC_MCH_VRPWRGD isn't correct for our original design on BB. informed fy David
- Change SUS_PWRGD_2MS to SUS_PWRGD_10MS for LAN_RST# must be asserted for at least 10 ms after the resume power is valid . (From ICH6 EDS REF.15851)
- P.18 Change R118 and delete R301,R302,R304-R310 , R1052 ; rearrange the DDR1 control terminator ; delete C504,C505,C506 for the pull high resistor array need 1 capacitor each .
- P.29 Add R1069 for reserved circuit connect from pin 43 of U29 to pin 1 of Q65 for ACL 260 codec .
- P.30 Swap RP92 & RP93 for layout request .
- P.15 Add RP9-RP24 & RP29-RP34 back for Igarashi-san request .
- P.36 change the Discharge circuit for power-off PR669.1 change connection to +2.5VRUN_ALV .
- Modify per David file : Issue List BB HW_06182004b.xls ; Change R352 from 100 to 0 for power level ; Correct the pin of Q60,Q65,Q66 by exchanging pin1 & pin2 .
- P.19 Delete T302,T303,T99,T100,T344,T345,R327 and connect the pins of ICH6 to GND directly & Delete C546 , connect to +1.5VRUN directly ; to disable SATA function .
- P.16 Change CN27 back to MOLEX 22_01_7085 and rearrange the pin define . For we don't need so many GND on CONN. power daughter & MB have 3 screw hole for strong GND
- P.14 Change the SCK IC to CY22560/SW560 and NC the accessories : U12,R713,R267,R268,R271,C321-C324,R272,R269 and add R1070-R1073 for NC , reserved for SCK circuits .
- P.25 Change R1062 to 0 ohm , that's it should be . For just a reserved circuits for MS board debugging .

(2004/06/25)Power

- P.34 Change net of PD41.2 to 486_BST_1 from 486_BST_2 , change PL16.2 net to VDDQ ; Add PC215 . By Jay .

(2004/06/25)

- P.32 Correct PC0N1 footprint to JMT A3963WR2.2P
- P.06 Change U65 value to *LMV358AM8X for power level 3.3V .
- P.01 Correct the Block diagram for NV43M-L , ALC260 , PATA HDD (Master) , PATA ODD (Slave) .
- Add description of SM bus address (KBC3910) for 3 thermal sensors (LM75BIM-3,MAX6647,MAX6657) , Smart Battery ; and SM bus address (ICH6-M) for clock generator, DIMM0 & DIMM1 .
- P.13 Remove R569 for there is a pull-down R937 and BB tried Ok for both NVIDIA & Alviso without R569 .
- P.13 Mount R709 , NC R569 , R9 for NV4X no need to reverse , but 915GM need .
- P.13 Mount Q8,Q9 , NC R213,R223 for current leakage bug in BB
- P.13 Change pin define of CN1 (LCD connector) for ME need to rotate 180 degree .
- Change R634 & R759 for balance LED light on MS01 .
- P.29 Delete R1069 and short the net "Codec_GPO" to U29.43 ; delete "Codec_GPO" to U29.2 for ALC260 only for MS01 .
- P.29 Change net name "C_AUD_ON_5" to "C_AUD_ON_5H" for it's low enable now
- P.35 Change PR166 to 10K and PR667 to 22K for voltage level to low (1V) on BB board .
- P.22 FOXCONN QT8H0506_M110R pin14 should connect toPATA_LED# by MOR / Ogasawara-san request .
- P.25 Change R1062 from 0 ohm to 47 ohm by MOR / Ogasawara-san request .
- P.25 Add 4.7k pull-up (R1074) to +3VSUS from U21 E1 pin (MC_CDZ_1) .
- P.25 Delete R384 and connect to GND
- P.10 Remove net "MSTRAPSEL[3:0]" and delete R139,R142,R145,R148 for these are for MEP NV chip ; Add T353-T356 .
- P.10 NC R560 & R562 for they are for NV370 .
- P.15 Remove net "MIOAD[5:2]" for we use VGA call back for the panel ID, The USER0-USER3 can be keep NC ; Add T357-t360. by Scott .
- Rearrange strap pin for NV43M-L A02 version ; add T361 .

(2004/06/28)

- P.24 & P.25 Change U21 value to PCI7420B(SN0307009BZHk) for correct vendor P/N .
- P.38 Add step up circuits for inverter if battery voltage lower than 10V . By Jay .
- P.13 Change CN1_38,CN1_39,CN1_40 net to INVERTER_VCC per step up circuits for inverter .
- P.25 Swap CN12 pin define for old pin define is wrong referring to ILink interface SPEC.
- P.13 Rearrange the pin define of CN1(LVDS_CONN.) , for layout and INVERTER_VCC need 1.2A current .

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(2004/06/28)

- P.38 Change PQ90.1 net to RUN_ON for step-up control
- P.15 Swap for layout need file name : e0720.004a.swap0625-new.txt
- P.06 Add C1201 for SMDR_VREF have two pins separately on Alviso .
- P.01 Correct block diagram for CRT & LVDS also from Alviso .
- Change 10U/10V_3216 to 10U/10V_1206 18pcs . C542,C603,C755,C756,C772,C773,C781,C915,C991,C996,C1006,C1036,C779,C563,C194,C819,C184,C183 .
- P.29 correct U23 pin define for ALC260
- P.14 U6.L2 & U6.Y2 should be different net , so change U6.L2 net from "MIOB_VREF" to "MIOA_VREF" .
- P.13 R573 NC .
- P.37 Rearrange PD28 & PD29 for PD28 NC on Alviso Graphic board .
- P.08 Add R1075 for simple BOM control
- P.29 Delete U52 and add U76 & U77 for TTL circuits on MUTE_5 .

Separate BOM by adding a symbol ahead of value ; "*" for components both NC , "@" for NC components on 915GM+NVIDIA VGA , "\$" for NC components on 915GM graphics ; Add a table on P.1 .

(2004/06/29)

- P.21 Add R1076 for ICH6 to measure the current of VCCSUS3_3 when converting VCCSUS1_5 .
- P.32 Add R1077-R1080 for Tim recommended , BB destroyed KBC 2 pcs when Battery in .
- P.29 Delete JSPK1 & JSPK2 and add JSPK3 for changing 2 pcs of 2-pin speakers to 1 pc of 4-pin speaker connector .

(2004/06/30)

- P.10 & P.14 Delete T357-T361 , add R1081-R1092 for NVIDIA chip strap and rearrange the configuration for NV43M , A01 .
- P.14 Change R260 to "\$10K" , and add "R1093" for "\$60.4/P" .
- P.23 Change CN11 footprint to FOXCONN_QL01303_D24A01_5F .
- P.16 Rearrange CN27 pin assignment for +1.0VRUN need 11.55A .
- P.10 Add R1094,R1095,R1096 for +1.0VRUN need 11.55A
- P.17 Add R1078 and net "DIMM_VREF" for DIMM_VREF replacing "DDRDIMM_VREF" on DIMM1 DIMM2 and C477-C480 . Requested by MOR / Doi-san .
- P.23 Add R108 and R755 and connect OVP_EC# to ICH6-M GP112,"ID_LPC_PCI#" to GP114 for THROTTLING FUNCTION discussion . requested by MOR / Doi-san .
- P.38 Change PL17 to CDRH5D28_8R2 . by Jay
- P.35 Change PQ32,PQ33,PQ36,PQ37 to IRF7811AV ; change PQ34,PQ35,PQ38,PQ39 to FDS7064N .by Jay .
- P.34 Correct PC194 value to 0.1U/16V
- Correct PD18,PD19,PD24 footprint to DIODE_2P_152_191X102 .
- P.32 Correct PR20 value to 75K/F 0603
- P.37 Correct PU18 footprint to US8_8P_20_79X122 .
- P.26 Add Screw hole H22-H45
- P.38 Change PC216-PC219 to 25TQC22MV . by Jay
- P.26 Change H26 to HOLE_C87D87N and disconnect pin 1, and add H46 .
- P.38 Change PC220 footprint to C0402 .

(2004/07/01)

- For BOM simplification , change PR94,PR708,PR711,PR716,PR788 to 10R
- P.32 Rearrange the R1077-R1080 for BB recommendation to prevent KBC destroyed when plug Battery .
- P.29 Change C998 to 1U/10V_0603 and footprint to C0603_MOR .
- P.29 Change U76 & U77 to TC7SE32PU for "power down protection function"
- P.26 Change H7 footprint to HOLE_C157D39 , delete H19,H22,H1,H15,H14,H4,H18,H20,H11,H5,H13,H2,H12,H10,H3,H17,H6,H21 for screw holes .
- P.29 Swap D31 pin 1 & pin 2 for layout .
- P.08 Delete PWM control from NVIDIA chip & Alviso chip and add bright control circuit from MOR / Igarashi-san requested : Delete R897,R714,R470,R573,Q42 . Add C1202,C1203,Q86,RP119,R1098 .
- P.10 & P.30 Delete T352 and add R1099 for net "BRADT_EC" connection for EC to control inverter brightness , this is reserved for testing in EVT .
- P.17 delete R559 - R562 per NV37 reserved circuits is not needed .
- P.06 Add T357 .
- P.17 Correct R1097 location for better DIMM_VREF connection .
- P.18 Delete RP116 and add C1204, R1100,R1101 for separating Resistor Pack to two resistors for layout .

(2004/07/02)

- P.13 Correct Q86 footprint to MOS_6P_26_79X83 .
- P.13 Rearrange D1 & D2 connection for ESD to prevent leakage from CRT when S3 .
- P.16 Rearrange CN27 pin define for reserving 1 pin for GND .
- P.29 Change U50.9-U50.12 net to "GND" FOR LM4863MTE.
- P.06 Change R567,R570,R571 to NC for default CRT impedance control for NVIDIA . Because Port Replicator mount 75 ohm .

(2004/07/02) POWER

- P.37 Add control ACIN_OCP protect, add PR741,PR744-pr748,PU21,PU22,PD43,PC224-PC226 .
- P.32 Delete PU13 , add PR742,PR743
- P.38 PR734 change to 0.047/F 1206, delete PC218, PC219 .
- P.36 Change PR688-PR672 from 100K to 47_0805 .
- P.33 & P.34 Delete JP30,JP18 & JP26
- P.33 Change PC188-PC191 to 10UF_25_1210 .

(2004/07/05)

- P.29 Change C1063 to 2.2U/10V_0603, Add Q87 & R1102 for pop noise solution from BB. by Tim .
- P.28 Swap LAN signals on CN22 for layout smoothly . By MOR / Tajiri - san request .
- P.32 Swap PC0N2 for correct pin define .
- P.10 Add C173 for missing component .

Separate BOM by adding a symbol ahead of value ; "NC_" for components both NC , "AL_" for NC components on 915GM+NVIDIA VGA , "NV_" for NC components on 915GM graphics ; modify the table on P.1 .

- P.34 Change PR708.2 net , 486 VDDQS should not link to it . by Jay .
- P.29 Correct U50.9-U50.12 net to "A_GND" FOR LM4863MTE.

(2004/07/06)

- P.29 Correct JSPK3 to HS82040 .
- P.25 Correct CN12 pin define for SPEC. change .
- P.16 CN26 pin 7,8,13,14 connect to GND . by Igarashi - san request .
- P.25 Correct pin name of CN12
- P.15 & P.16 Add R1109-R1114 & C1205-C1208 for NVIDIA recommendation for VRAM_VREF .
- P.13 Change C289 to L26.1 & C285 to L23.1 for Port Replicator use same "C" .
- P.13 & P.30 Delete L92 & C278 , Add T358 for Bright control change circuits from MOR / Igarashi-san request .
- P.22 Change CN6 value & footprint to FOXCONN_QT8H0506_N110R_F for different Z-HIGH connector . (Layout pad not changed .)
- P.32 Change PC0N2 value & footprint to FOXCONN_BP34063_C6201_7F for different Z-HIGH connector . (Layout pad not changed .)

(2004/07/07)

- P.29 Change R1102 to 0805 package for power capacity .
- P.17 Add C1209-1224 for DDR . by MOR / Doi-san request .
- P.04 Change R544,R549,R550 to 2.2/F for IDT recommendation .
- P.34 PC192 & PC193 change to 4.7U_1210.
- Add R1115-R1117 , Delete C1078,T191 and NC R937 , R568 always mount for strap pin by MOR / Igarashi-san inform from NVIDIA / JAPAN.

(2004/07/08)

Rename the reference .

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HISTORY

DVT board start .

(2004/08/09)
Change NV43M value to NV44M.

(2004/08/11)
EVT board rework implement , file name : MS01_Rework_Notice_EVT_20040811 Rev.1.3.doc

- Rework number 0**
P.06 Change R216 value to 255/F, from 256/F.
P.08 Change L46 value to 1UH, from 91NH.
P.13 Change R370 value to 330_0805, from 47_0805.
P.36 Change PR104 value to 330_0805, from 47_0805.
P.34 Change PR143 value to 330_0805, from 47_0805.
P.34 Change PR97 value to 62_0805, from 47_0805.
P.36 Change PR141 value to 62_0805, from 47_0805.
P.36 Change PR142 value to 62_0805, from 47_0805.
P.36 Change PR174 value to 62_0805, from 47_0805.
P.36 Change PR139 value to 62_0805, from 47_0805.
P.32 Change PR12 value to 33.3, from 33.3/f_0603.
P.32 Change PR22 value to 56K, from 59K_0603.
P.32 Change PR23 value to 56K, from 54.9K_0603.
P.32 Change PR17 value to 15K, from 14.7K_0603.
P.32 Change PR18 value to 22K, from 22.6K_0603.
P.32 Change PR63 value to 75K/F, from 76.2K/F_0603.
P.34 Change PC53 value to 0.01U/25V, from 0.1U/16V.
P.38 Change PC85 value to 0.01U/25V, from 0.1U/16V.
P.35 Change PC30 value to 330P, from 270P.
P.08 Change C398 value to 220U/6.3V, from 330U/6.3_7343.
P.08 Change L48 value to 0.47UH, from 0.5UH.
P.30 Change R283 value to AL_100K , from 100K .
P.30 Change R296 value to NV_100K, from NC_100K.
P.04 Change R466 value to NV_0, from 0.
P.04 Change R183 value to NV_0, from 0.
P.33 Change PC146 value to 4.7u/25V from 4.7u/35V .
P.28 Change C21 value to 4.7u/25V from 4.7u/10V.
P.34 Change PC55 value to 10u/25V from 4.7U_1210.
P.34 Change PC57 value to 10u/25V from 4.7U_1210.
P.32 Change R14 value to 100 from 330.
P.32 Change R15 value to 100 from 330.
P.30 Change R311 value to 10K from 4.7K.
P.30 Change R314 value to 10K from 4.7K.
P.34 Change PC76 value to 10uF/25V 1206 X5R from dummy.
P.34 Change PC77 value to 10uF/25V 1206 X5R from dummy.
P.32 Change PR177 value to 14K ohm 0402 1% from 40K.
P.32 Change PR135 value to 20K ohm 0402 1% from 10K.
P.34 Change PC71 value to 0.1uF/16V 0402 X5R from dummy.
P.34 Change PR185 value to 10 ohm 0402 1% from dummy.
P.34 Change PC69 value to 18PF 0402 X5R from 100P.
P.34 Change PR130 value to 6.49K ohm 0402 1% from 10K.
P.34 Change PR136 value to 0 ohm 0402 1% from dummy.
P.34 Change PR181 value to dummy from 0 ohm 0402 1%.
P.33 Change PR96 value to 0 ohm 0402 1% from dummy.
P.36 Correct the pin define for PQ29,33,PQ38,PQ39,PQ45,PQ48 .
P.37 Correct the footprint for PQ12 , it should be SSOT6 .
P.32 Change PR30 value to 3K 0402 1% from 6.49K.
P.37 Change PR13 value to 24K 0402 1% from 61.9K.
P.35 Change PR31 value to 10 ohm 0402 1% from dummy.
P.35 Change PC27 value to 0.1uF/16V 0402 X5R from dummy.
P.37 Link the pin 8 of PUL1 to +ECVCC , no link to +3VALW .

- Rework number 1**
P.13 NC U13,U14,U15 ; Add R171,R172,R174,R175,R177,R178 with 0 ohm .
Rework number 2
P.13 Pin 4 of SW7 Link to GND ; modify the symbol .
Rework number 3
Done on Rework 0 .
Rework number 4
Done on Rework 0 .
Rework number 5
No need to modify schematics .
Rework number 6
No need to modify schematics .
Rework number 7
PR29 & PR6 is on VGA Power board ; R451 not changed yet , need to verify .
Rework number 8
No need to modify schematics .
Rework number 9
No need to modify schematics .

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(2004/08/11)

For collecting similar together :
P.37 Change PC17 to 0.01u/25V_0402
P.35 Change PC24 to 0.01u/25V_0402
P.03 Change C681 to 0.01u/16V_0402
P.32 Change PC14 to 0.01u/50V_0603
P.33 Change PC141, PC150 to 0.1u/16V_0402
P.25 Change C533 to 0.1u/50V_0603
P.34 Change PC71 to 0.1u/50V_0603

Change ALL 0.1u_0603 to 0.1u/50v_0603

P.32 Change PC2 to NC_0.1u/50v_0603
P.35 Change PR74 to 1.24K/F_0603
P.34 Change PR185 to 10/F_0603
P.34 Change PR103, PR120 to 100K/F_0603
P.35 Change PR72, PR160 to 100K/F_0603
P.32 Change PR1, PR21, PR13, PR59, PR68 to 100K/F_0603
P.33 Change PR190, PR199 to 100K/F_0603
P.37 Change PR24, PR33 to 100K/F_0603
P.38 Change PR157 to 100K/F_0603

P.33 Change PC152, PC153, PC133, PC134 to 150u/6.3V_7343
P.32 Change PR14,15,22,23,17,18 to 100K/F_0603
P.08 Change PR24,25,30,43,44,45,46,49~52,53,70,71,75,76,88~93,101,106,110,113,117,122 to 100K/F_0603 .
P.34 Change PR99 to 10K/F_0603
P.32 Change PR16 & PR27 to 10K/F_0603 .
P.34 Change PR134,176,180,183 to 10/F_0603
P.21 Change R273 to 10/F_0603
P.29 Change R590 to 10/F_0603
P.35 Change PR87 to 10/F_0603
P.08 Change R486 to AL_10/F_0603
P.34 Change PR102,123 to 0603

Change R11,371,259,251,608,PR124 to 1% .

P.32 Change PC90 to 1U/25V_0603
P.02 Change R420 to 1%
P.32 Change PR11 to 1%
P.34 Change PR135,100,125 to 0603.
P.32 Change PR19,20,7 to 1%

P.28 Change R12 to 1%
P.33 Change PR95 to 1%_0603
P.33 Change PC140,61 to 0402
P.35 Change PR56 to 1%_0603
P.34 Change PC70 to 10V_1206
P.23 Change R398,401 to 1%
P.32 Change PR12 to 33_0402
P.23 Change R402,404 to 1%

P.37 Change PR34 to 0402
P.34 Change PR137 to 0402
P.32 Change PC15 to 0402
P.08 Change C677,697,714,715 to 470u/2.5V_7343
P.33 Change PR191,202 to 1%_0603
P.32 Change PR5 1%_0603

Change LED :
D14,D16,LED1 to HSMY-C170 .

P.30 Change J5 to NC_FOXCONN_HS82020

Change C683 value to AL_22000P_0805_3P , but BOM no change .

P.10 Change R157 to 0 ohm, from NC_0
P.12 Add R622 NC_0 to NVVDD
P.12 Change R71,62 to 40/F
P.13 Add R623
P.13 Change U26,R391,186,197 to NC_0 ohm
P.14 Change U9 to NC_MB88153/CY25560/IMISM560
P.23 Change U7,U10,U12 to RT9702APB for Lead free part .

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HISTORY

(2004/06/18) Doi san requested for clock measurement reserver circuits , file name : CLK.pdf .

P.04 Add R624 for value = "0" ; R625 for value = "NC_10K" ; RP80 for value = "NC_4P2R-S-33" ; R626,R627 for value = "NC_10K" ; RP79 for value = "NC_4P2R-S-10K" ; swap net "PCLK_JIG/R_PCLK_JIG" to "CLK_ICHPCI" ; Del T164 & T163 .
 P.14 Add R628 & R629, value = "NC_0" .

(2004/08/18) Intel check MS01 schematics , file name : Sony_Foxconn_MS01 schematic review.pdf .

P.02 NC R438 for no ITP ;NC R436 for H_CPURST# no need to pull high .
 P.03 Del T17 & T19 , add R633 & r634 for 54.9/F .
 P.04 NC R458,R460,R71 , add C841 value = "10U/6.3V_0805"
 P.08 Del C969 & C271 ;
 P.08 C280 is not necessary in CRB 1,601 and lviso check list 1.601 , NC C280 .
 P.08 Add C842 calue = "10U/6.3V_0805" .

(2004/08/18)

P.19 Change R511 to 100K & C719 to 1U/10V_0603 for Doi san requested on 8/12 .
 P.28 Change C4/C7 from 22pf to 33pf for Y1 clock precision .
 P.25 Change C537/C538 from 12pf to 18pf for Y3 clock precision .
 P.19 NC R506 value = "NC_0" .
 P.20 Link pin AC5 , AD5 , AC9 , AD9 of ICH6m to GND to disable SATA[3,1] ; del T63,T65,T67,T69 .
 P.02 Change R135 value = "39" for RDDP rev1.5 .
 P.08 Add R630 value = "NV_0" , R191 value = "0" , Del R202 ; for disabling CRT .
 P.25 Add C840 value = "1000P" for MS , it's more effectiv than near MS connector .
 P.04 Change value of R466 & R183 from "0" to "NV_0" for HIGH ; add R631 & R632 value = "AL_49.9/F" for LOW .
 P.30 Change net name "TEST1" to "TEST1_EC" to avoid conflict with "TEST1" on P.3 .
 P.08 Add C842 calue = "10U/6.3V_0805"
 P.30 Change R283 value to AL_100K & R296 value to "NV_100K" for system ID identification .
 P.04 Change U32 to F75383S for CPU & NB thermal sensor ; change R448 & R454 to 4.7K , C655 to 0.1U/16V per recommended schematics .
 P.14 Change U27 to NV_F75383M for NVIDIA thermal sensor ; Delete R55 ,change R60 & R393 to NV_4.7K , C53 to NV_0.1U/16V per recommended schematics ; Change net "MAX6647_VDD" to "U27_VDD" .
 P.30 Change R321 to 0 ohm and connect from OVT_EC# to pin 12 (GPIO06) of EC for thermal throttling control method .

(2004/08/20)

P.34 Change PC136 to 1U/10V_0603
 P.25 Change R352 to 390K ohm , for TI suggest .

(2004/08/26)

P.08 Change D20 to SCS500V-40 .
 P.08 Change R486 to 10/F_0603
 P.08 Change C842 to AL_10U/6.3V_0805 .
 P.04 Change R633 & R634 to NC_54.9/F .

For Power Change

P.36 Add P066 to 2N7002DW. Add PR211, PR212
 P.35 Change PR67 to 1.62K/F. Add PC156. PC157 to 2R5TPE220M9
 P.34 Change PC128, PC152 to 4TPE220M_7343. Change PC122, PC123, PC124 , PC44 & PC38 to 2R5TPE330M9_7343
 P.33 Change PC133, PC134, PC152 & PC153 to 6TPE150M_7343
 P.34 Change PR177 to 14K/F_0603
 P.38 Change PR153 to 0.047/F_1206
 P.36 Change P044 & P047 to PDC653N
 P.36 Change P057 to PDC796N
 P.32 Change PD4 & PD5 to DIODE_2P_51_63X31(Change footprinter)
 P.32 Change PD15 & PD22 & PD26 to DIODE_2P_51_63X31(Change footprinter)

(2004/08/28) MOR suggested on MS01 schematics .

P.04 Remove the leader rectangles , and change the values of R461 , R462 to "NV_49.9/F"
 P.10 Delete R388,389,387,33,32,34,65,451, and change net "NV_VDD33" to "+3VRUN" ; "+1_2VRUN" to "PEX_VDD" ; "+1_0VRUN" to "NV_VDD" , for no need current measuring R .
 P.13 Change R371 to "10K" for NVIDIA Design guide .
 P.13 U26 mount , R623 "NC_0" , R391 "NV_0" , R186 "AL_0" , R197 "AL_100K" .
 P.13 D1 & F1 NC for no +5VRUN needed on pin9 of VGA connector .
 P.15 Delete R452,R38, & change net "+2_5VRUN" to "VRAMVDD" ; delete R37 & change net "NVFBVDDQ" to "VRAMVDD" ; delete R36 & change net "NVFBVTT" to "VRAM_TERM" ; delete R429 & change net "FBVTT" to "VRAN_TERM" , for no need current measuring R .
 P.19 Change C359 & C369 to "15P" for CLK accuracy .
 P.23 Add R635~R640 with "NC_0" for USB signals .
 P.23 Add R641 & R642 value "33" series with SUS_ON & RUN_ON for noise concern on Port Replicator .
 P.29 Mount Q40 & R619 for mute on Port Replicator .
 P.30 Change C447 & C448 to "15P" for CLK accuracy .
 P.30 Add D31 & D32 with "PACDN042Y3" for ESD concern .

(2004/08/29)

P.14 Delete R97 , R128 and short it for no need current measuring R .
 P.13 Change U13~U15 to mount "NC7SB3157" and R178,177,171,172,175,174 to "NC_0" for SI tested need analog switch for Port Replicator .
 P.08 Delete R191 for it's not needed
 P.11 Delete T61 and add C849 for "0.1U/16V" for intel suggestion "OHLONE/GUADALUPE CRB BOARD REWORK #15"
 P.08 Delete R226 for no need current measuring R .
EMI solutions :
 Add C850-C854 & C857-C859 "0.1U/16V" ; Add C855 , C856 "47P" and C5 , C10 "NC_47P" and change GND connection on HSYNC13 & VSYNC14 .
 P.23 CN10 pin 65~70 connect to GND .

for using common components and material lead time issue , change some value of components .
 Change "NV_40/F" to "NV_40.2/F" for R71,62 .

For Power Change 8/29

P.32 change PR16 to 4.99K/F_0603
 P.32 change PR8 to 21.5K/F_0603
 P.36 change P046 source from +5VSUS to +5VALW
 P.36 change P043 source from +3VSUS to +3VALW
 P.13 Add R643 "NC_100K" for reserved circuits .

(2004/08/30)

P.23 NC FAN 2 & it's accessories : R409,C73,R407,R404,R401,C23,Q4,R35,J3 .
 P.16 Remove two VGA memory :
 delete :
 C27,29,30,32,33,41,42,44,47,77,79,85,87,92,103,104,105,124~128,140,154,164,165,171,180,188,192,222,239,240,243~247,564,589,594,598,617,620,623,624,626,630,633,638,640,642,646,647,654,658,659,664,666,667,671,673 ;
 R51,69,81,152,160,T10,T29,U8,U11 ; and delete NC parts :C592,602,605,606,621 ; R70,80,162,167 .
 P.26 Screw hole change .

Change connector footprint & value for ME modify :
 JVGAI,CN16,CN15,CON1,CON2,CN17,J6,U30,CN12,CN6,PCON2,SW1,SW2,SW3,SW5,SW6,SW4,JSPK1,CN5,CN11,CN14,J2 footprint & value changed , footprint is the same with the value of the corresponding component .
 P.30 Change SW7 to a 3-pin connector for ME modify .

For Power Change 8/30

P.35 change PR65 to 100ohm
 P.36 PU6 change RUN_ON to RUN_ON_1
 P.32 Change P01,P04,PQ05,PQ51 value from "SI4835DY" to "SI4835BDY"

(2004/08/30)

P.16 CN11 and CN13 change connector : hd_16p_et_1790_16 for CN11 , hd_30p_et_1790_30 for CN13 .

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HISTORY

(2004/09/01) Nishio san requested add signal AV_PHONE_DET to mute system speaker when haedphone plug in AV port replicator

P.23 Add signal AV_PHONE_DET at Pin 32 of Replicator connector (CN10)
P.29 Add R644 & R645 for Control mute function by AV_PHONE_DET signal or APR_ON signal.

(2004/09/02)

P.23 R635,R636,R637,R638,R639,R640 change footprint to compatible common choke pad for layout easy
P.26 Add EMI spring pad SPR1 ~ SPR10
P.32 PCON2 change component for meet Lead Free requirement
P.04 Add R646 to keep drive level keep under 500 uW

(2004/09/03)

P.29 Change C782,C802 material from POSCAP to aluminium electrical capacitor 100u/6.3V.
P.26 Add C867 , C868 , C869 0.1u F for EMI request

(2004/09/04)

P.08 Add C871 to 150U/6.3V_7343 for CRT noise .
P.11 Add C870 to 220U/6.3V_7343 for ripple noise .
Change +15VRUN to +17VRUN

(2004/09/05)

P.08 Add C872 & C873 to NC_470U/2.5V_7343
P.29 Add Q42 & Q43 to 2N7002;Add R647 to 10K; Add R648 to 1K .

(2004/09/06)

P.28 Change U3 to PI3L110Q for a better Ron value , requested from David san .
P.11 Change C870 to NV_220U/6.3V_7343 .
P.16 CN11 & CN13 are "NV" option ; NV_hd_16p_et_1790_16 for CN11 , NV_hd_30p_et_1790_30 for CN13 .
P.30 Delete T195 and change connect PWRLIMIT# to pin 3 of EC ,MAX1909_T1NE_EC to pin 88 of EC for power request .
P.04 Swap EP80 for layout request .
Combine power circuits p.31-p.38 .
P.08 Add C871 to "AL_150U/10V_7343" for combining BOM .

(2004/09/07)

P.30 Change touch pad to ALPS ,R357,R358 value ="0" ; change CN18 pin define for ME changing touch pad position .
P.12 Add R649 "NC_0_0805" & R650 "NV_0_0805" for FBVTT voltage option for NVIDIA recommendation link to FBVDDQ .
P.16 Modify CN13 pin define for Layout .
P.15 Add R651 & R652 "NC_0" for PBA CSI# on NVIDIA DDR option .
P.15 Add R653 ,R654 ,R655 value "NV_150" for NVIDIA recommendation .
P.16 Change R61 & R64 to "NV_4.7K" for NVIDIA recommendation .
P.10 FOR 4Mx32 memory setting :

Change R78 value from "NC_2K" to "NV_2K" .
Change R422 value from "NV_10K" to "NC_10K" .
Change R412 value from "NC_2K" to "NV_2K" .
Change R73 value from "NV_10K" to "NC_10K" .
Change R425 value from "NC_2K" to "NV_2K" .
Change R104 value from "NV_10K" to "NC_10K" .
Change R416 value from "NC_2K" to "NV_2K" .
Change R414 value from "NV_10K" to "NC_10K" .
FOR PCI_DEVID setting :
Change R90 value from "NC_2K" to "NV_2K" .
Change R423 value from "NV_10K" to "NC_10K" .
Change R435 value from "NV_10K" to "NV_2K" .
Change R431 value from "NV_10K" to "NV_2K" .
Change R433 value from "NV_10K" to "NV_2K" .
Change R421 value from "NV_10K" to "NV_2K" .
Change R430,R432,R434 value from "NC_10K" to "NC_2K" .

(2004/09/08)

P.29 Change R648 to 100K for 1K pull down to GND too strong , pin 1 of Q42 can't be high .
P.21 Change L48 to BLM31PG121SN1 for +1.5V_PCIE voltage drop issue .
P.26 Delete H1 ~ H4 for changing to Non_PTH screw holes .
P.08 Change C871 to "AL_150U/10V_7343" for MS01_L CRT noise issue .
P.19 Add C874 value = "NC_470U/2.5V_7343" reserved CAP for 3D hang up issue .
P.29 Add R657 "20K/F_0603" link from U39_40 to GND R656 "20K/F_0603" link net "SENSE_A" from Q42.1 to U39.13. For MIC jack sense .
P.25 Change R352 to from "390K" to "1K" following TI datasheet .
P.29 Change C782 & C802 value to "100U/6.3V_AL_CAP" .
P.29 Change D6 ,D23 ,D28 ,D29 to "MTZS05-6.2" for correct zener diode ESD protection .
P.30 Change D15 to HT_297 UD_UYG ; LED1,D14,D16 to "HT_170_UYG" ; D8 ,D9 ,D10 to "HT_110_UYG" ; D13 to "HT_170_UYG" .

(2004/09/08) Nishio san requested to modify , file name : MS01 Audio0906.jpg .

P.29 R619 and Q40 NC .
P.29 R645 change from "0" to "1K" .
P.29 R611 & R610 change from "NC_0" to "0" .
P.29 Add R658-R663 "NC_47K" , U52 "TC7SH32FU" , R664,R665 "NC_10K" .

(2004/09/08) Nishio san requested to modify , file name : MS01 Mute.jpg .

P.29 Add R666 "0" ; R669,R672 "NC_0" ; R670,R671,R673,R674,R675,R676,R677 "NC_1K" ; U53 "NC_TC7W14FU" ; U54,U55 "NC_TC7SH32FU" for reserved MUTE circuit .

(2004/09/09)

P.29 Change net "SENSE_A" to "SENSE_A" to meet orcad rule .
Combine Power Circuit from Jay . P.31-p.38
Change net "17V" to "15V" ; "+15VRUN" to "+17VRUN" for power circuit change .
P.34 Disconnect net "VSSA" & "GND" by Jay .
P.29 Delete U53,U52,R611,610,667,668 ; Add U56 "TC7SET04FU",U57,U58 "NC_TC7SET04FU" , change U55 to "NC_TC7SET32FU" ; add D33 "NC_SCS500V-40" and change R656 to "NC_10K" for "SENSE_A" net ; Add D34 , D35 "MTZS05-6.2" for ESD concern ; Nishio san requested .
P.23 Change D7 to "NC_MTZS05-6.2" , for correct zener diode .
P.23 Add D36 "NC_MTZS05-6.2" for Nishio san requested .

(2004/09/10)

P.29 Change R656 value to "NC_10K/F_0603"
P.10 Change components value : R136,R133,R130,R125 to "NV_2K" ; change R132,R137,R129 to "NC_2K" ; change R93 to "NC_10K" .
P.16 Change NV_VDD voltage description from 1.2V to 1.1V for NVIDIA recommendation
P.30 Change value : D15 to "LED_DUAL_HARV_HT_297_UD_UYG" ; LED1,D14,D16 to "LED_HARV_HT_170_UYG" ; D8,D9,D10 to "LED_1GND_HARV_HT_110_UYG" ; D13 to "LED_HARV_HT_170_UYG" .
P.32 PR222 Change to 100K/F_0603 , by Jay .
P.32 PR28 "NC_0" , PR223 "0" , by Jay .

(2004/09/13)

P.26 Change H14 to "ho_c256in177d98_m2_v4" for Layout .
P.26 Delete SPR12 for not needed .
P.37 Change PR30 to 1K/F for combining BOM .
P.32 PCON1 add GND pin(7,8pin)
P.30 SW3,SW5,SW6 modify pin assignment due to change parts

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