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P. Leader	Check by	Design by

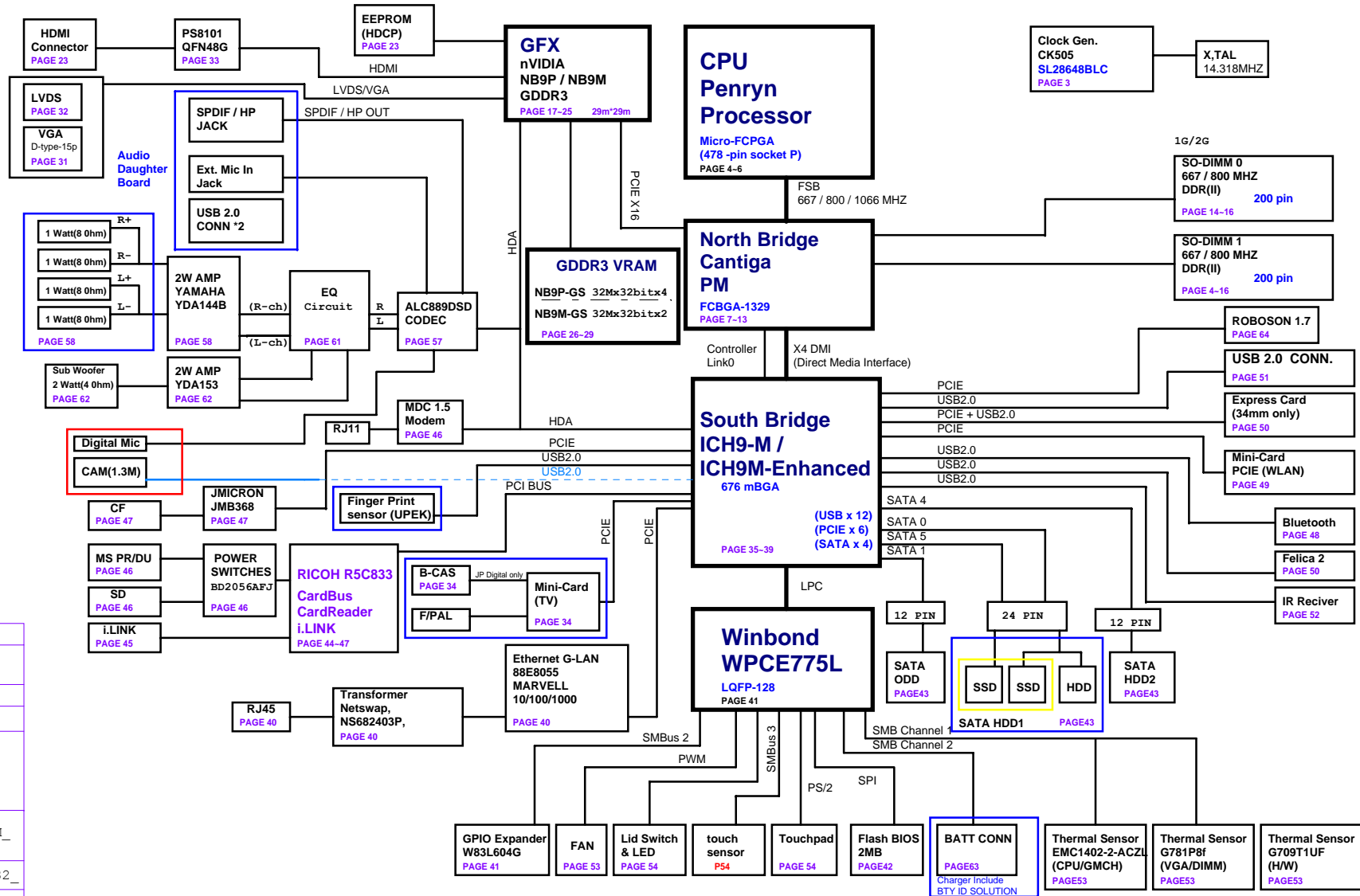
DVT to PVT

Project Code & Schematics Subject: M780 EVT Main Board

PCB P/N: FUBAI 1P-0086102-8010

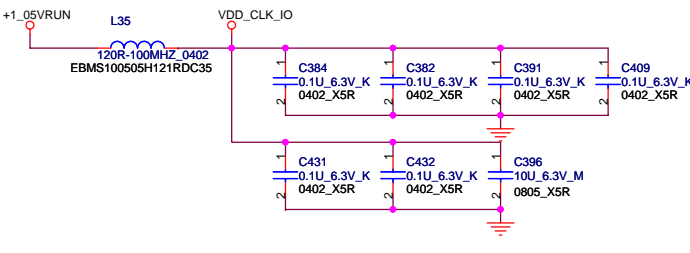
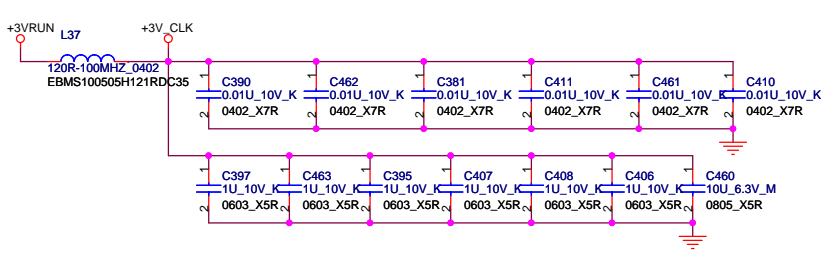
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
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M780 Montevina Block Diagram

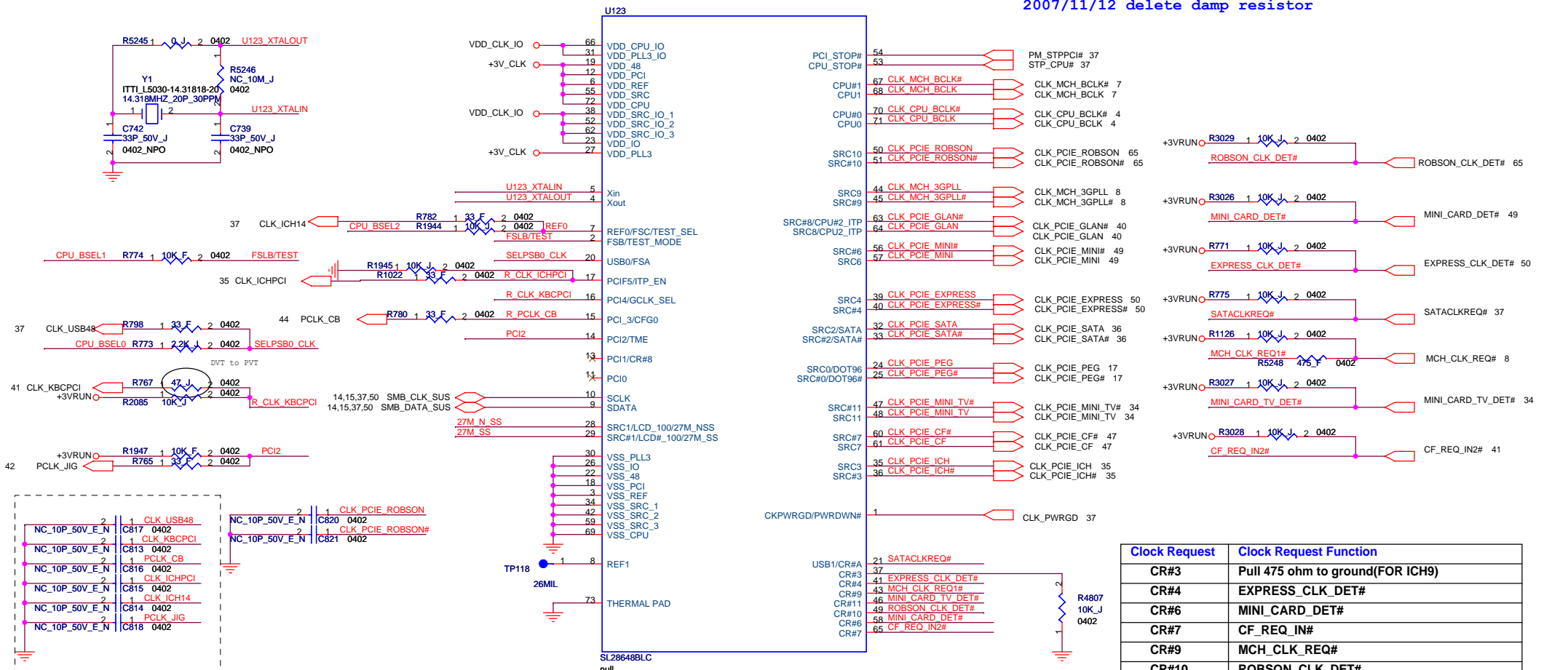


TI CHARGER	
BQ24751 P.63	
INPUTS	OUTPUTS
DC_IN	BT+ DCBATOUT
SYSTEM DC/DC	
ISL6236IRZA-T P.64	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +15V_ALW
SYSTEM DC/DC	
SC411 P.65	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VM
SYSTEM DC/DC	
ISL6269A P.66	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSDS
SYSTEM DC/DC	
G2998 P.66	
INPUTS	OUTPUTS
DCBATOUT	+0_9VRUN
CPU DC/DC	
ISL6266A P.67	
INPUTS	OUTPUTS
DCBATOUT	VHCORE
SYSTEM DC/DC	
APL5913 P.70	
INPUTS	OUTPUTS
+1_5VRUN	APL5913
SYSTEM DC/DC	
SC411 P.70	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD

M780 BOM configuration	
unstuff	NC_
NB9P-GS + NB9M-GS	NV_
for L model	NV9L_
for M model	NV9M_
B-CAS Card, Felica module for J SKU stuff	LNC_
Roboson,TV Tuner, I.R. Receiver, CF Card Slot unstuff for L Model	
for H M model	NV9HM_
for L model 32Mx32 GDDR3	NV9L32_
for H model	NV9H_
for Qimonda VRAM	NV9QI_
for Samsung VRAM	NV9SAM_



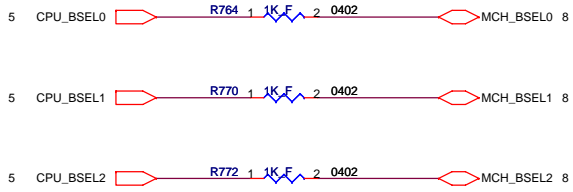
2007/11/12 delete damp resistor



FSB Frequency Table:

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

close to clk gen (For EMI)



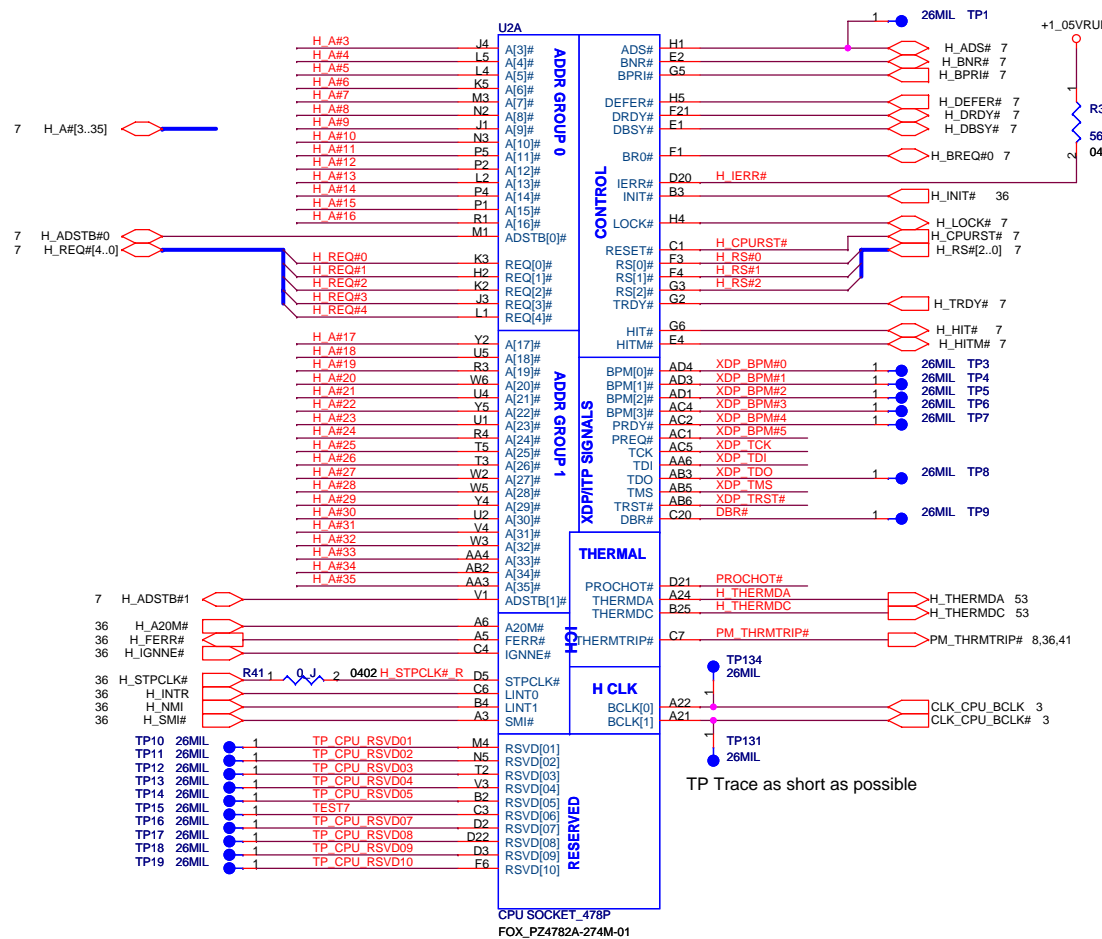
Clock Request	Clock Request Function
CR#3	Pull 475 ohm to ground(FOR ICH9)
CR#4	EXPRESS_CLK_DET#
CR#6	MINI_CARD_DET#
CR#7	CF_REQ_IN#
CR#9	MCH_CLK_REQ#
CR#10	ROBSON_CLK_DET#
CR#11	MINI_CARD_TV_DET#
CR#A	SATACLKREQ#

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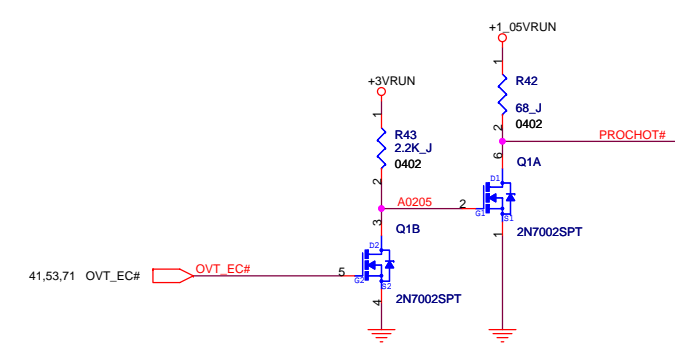
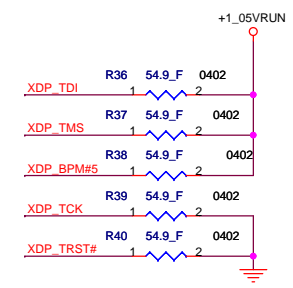
Title: **CLOCK GEN (SL28648LFXC)**

Size: A3 Document Number: **M780(MBX-194)** Rev: **0.1**

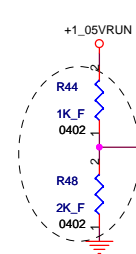
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H_CPURST# 1 26MIL TP2
as Close as possible to Pin out trace

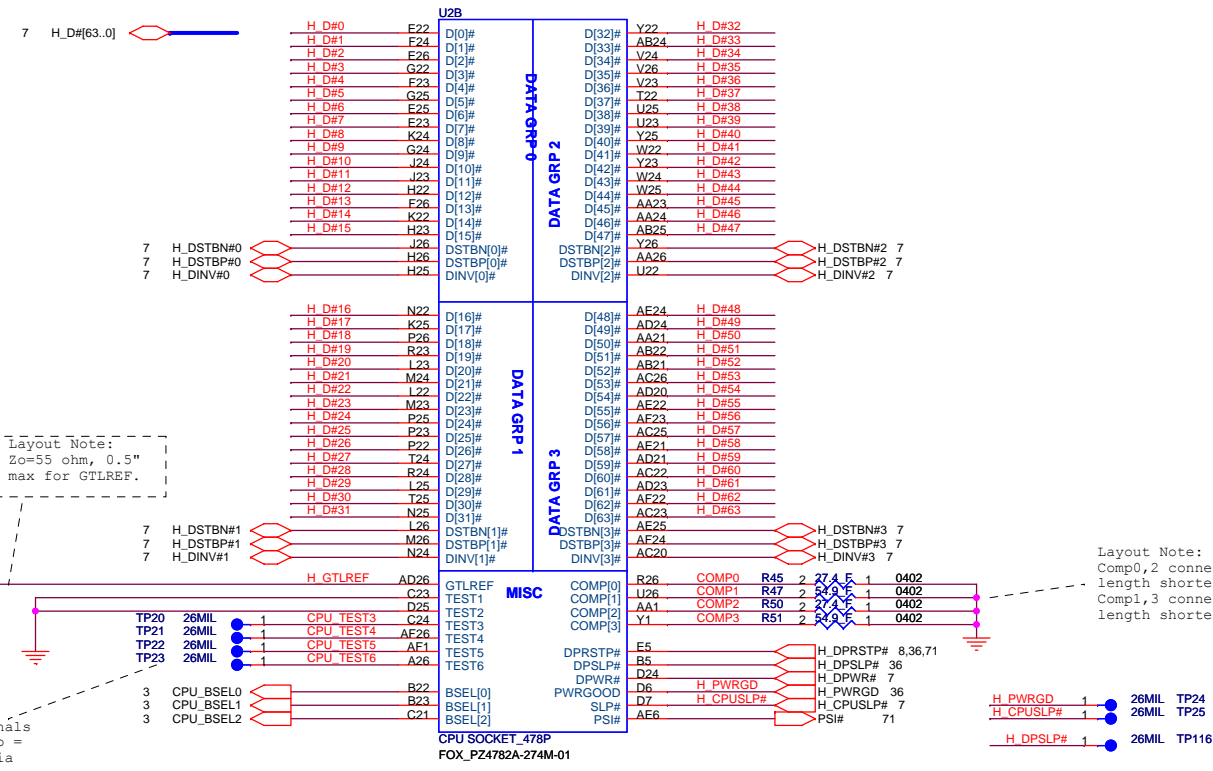


Place close to CPU



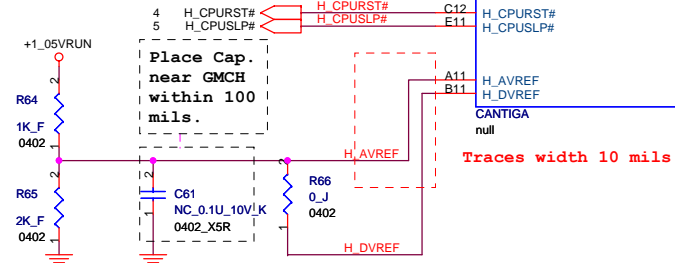
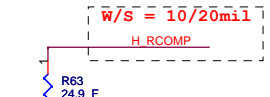
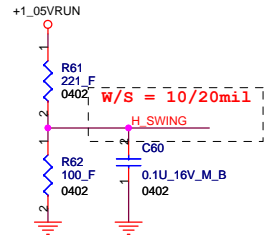
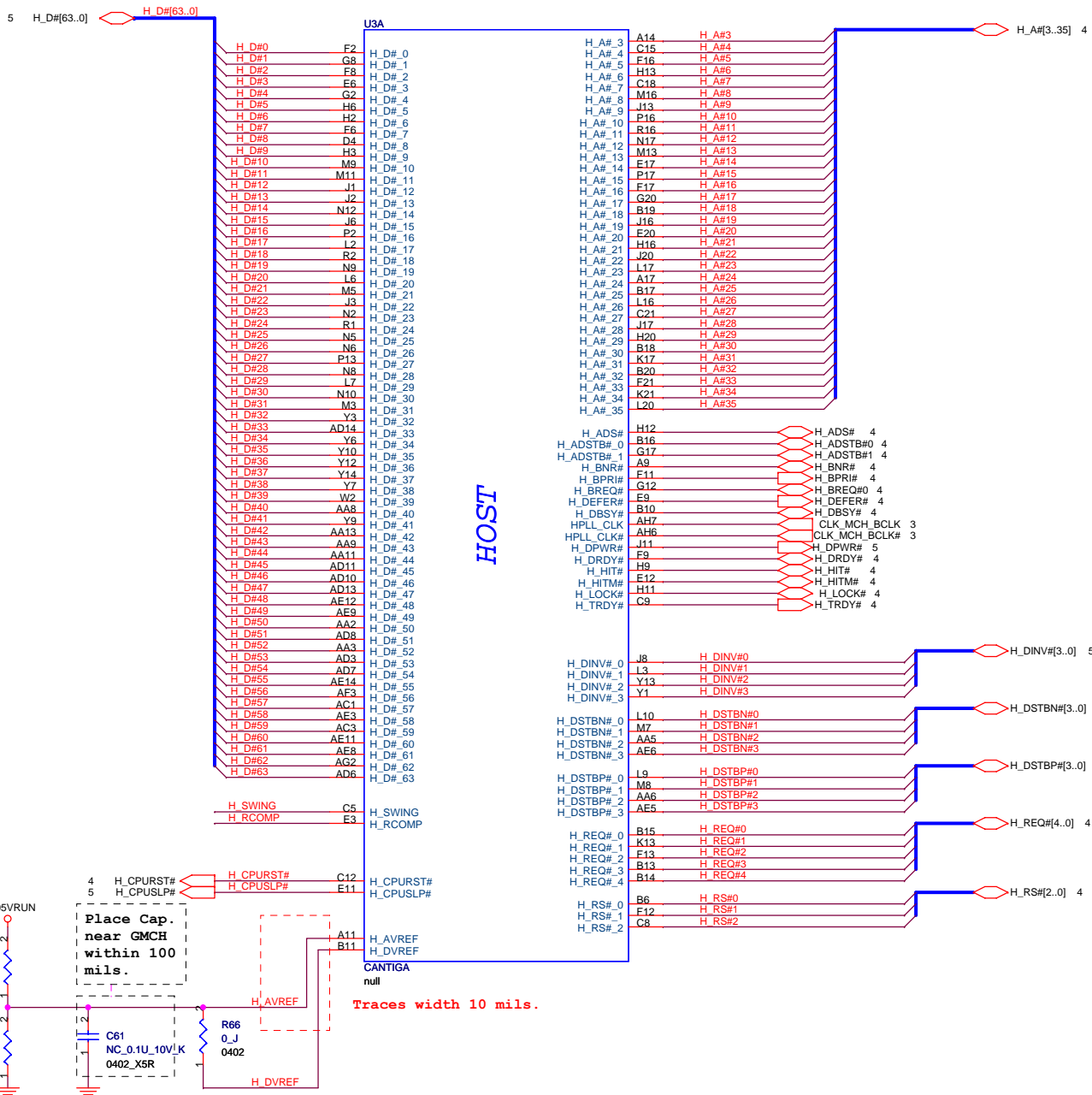
Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

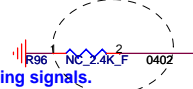


Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Width=19mil(MS)
Comp1,3 connect with Zo=55 ohm, make trace length shorter than 0.5". Width=5mil(MS)

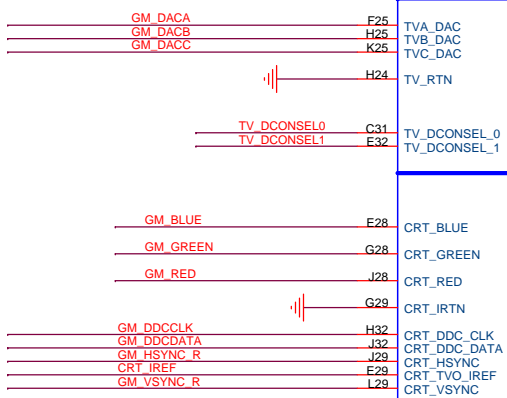
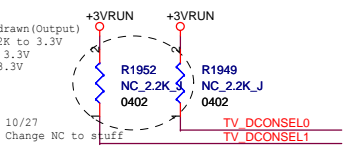
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title Penryn (HOST BUS) 2/3			
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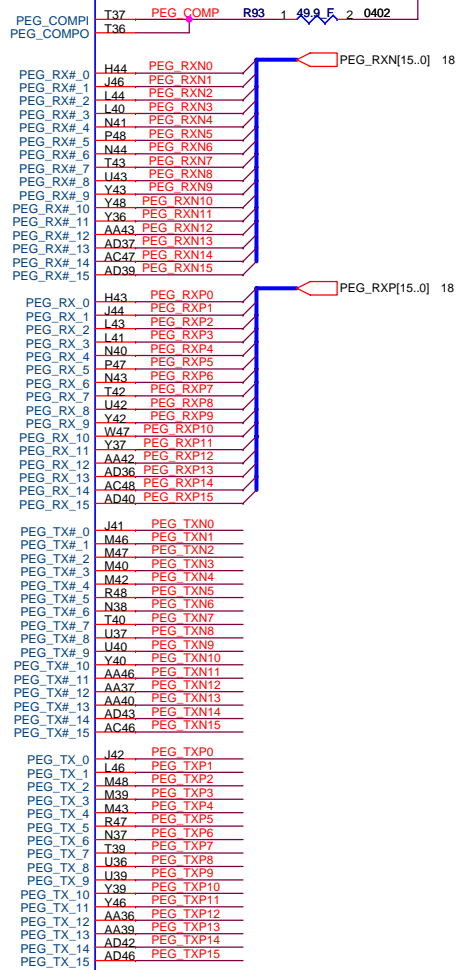
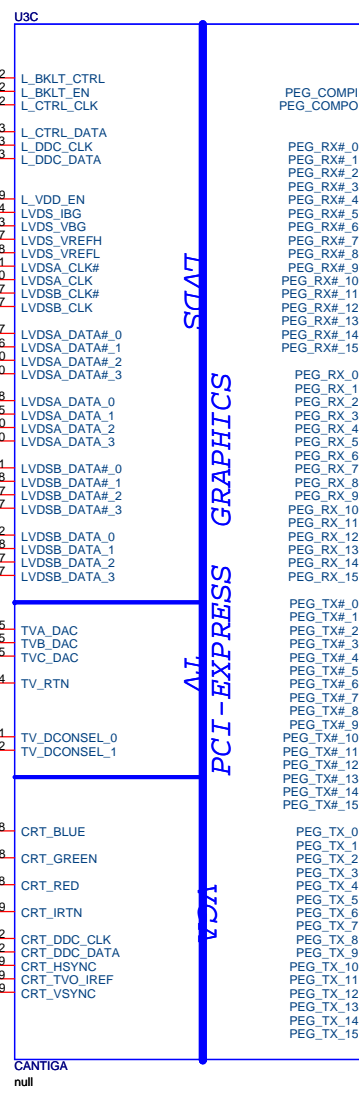
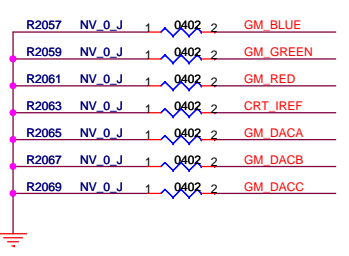
20 mils away from toggling signals.



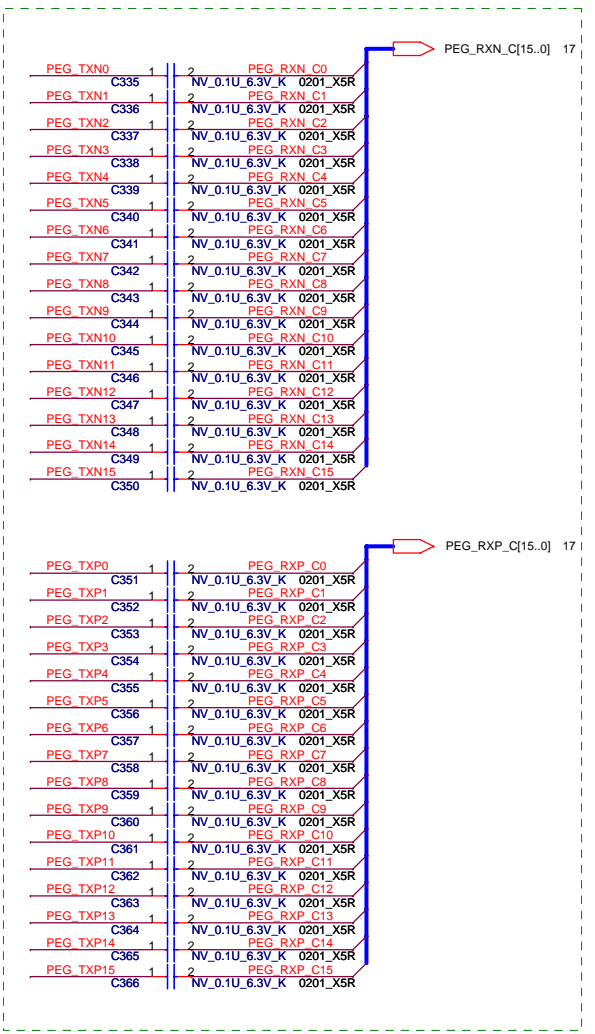
TYPE is open drawn(Output)
Check list 2.2K to 3.3V
MS90 2.2K to 3.3V
CRB 2.2K to 3.3V



External Graphics (GMCH CRT/TVOUT Disable)



214. (Page 9) 07/11/28 Change PCIE Capacitor size from 0402 to 0201



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Title: **Cantiga (GRAPHIC) 3/7**

Size: Document Number
Custom: **M780(MBX-194)** Rev: **0.1**

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14 M_A_DQ[63..0]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AM38	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AU40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AU44	SA_DQ_14
M A DQ15	AU42	SA_DQ_15
M A DQ16	AV39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BD43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BB41	SA_DQ_22
M A DQ23	BC40	SA_DQ_23
M A DQ24	AY37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AY37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BB38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	AW36	SA_DQ_31
M A DQ32	BD13	SA_DQ_32
M A DQ33	AU11	SA_DQ_33
M A DQ34	BC11	SA_DQ_34
M A DQ35	BA12	SA_DQ_35
M A DQ36	AU13	SA_DQ_36
M A DQ37	AV13	SA_DQ_37
M A DQ38	BD12	SA_DQ_38
M A DQ39	BC12	SA_DQ_39
M A DQ40	BB9	SA_DQ_40
M A DQ41	BA9	SA_DQ_41
M A DQ42	AU10	SA_DQ_42
M A DQ43	AV9	SA_DQ_43
M A DQ44	BA11	SA_DQ_44
M A DQ45	BD9	SA_DQ_45
M A DQ46	AV8	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AU5	SA_DQ_52
M A DQ53	AU6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AN12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

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DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	14,16
SA_BS_1	BG18	M_A_BS1	14,16
SA_BS_2	AT25	M_A_BS2	14,16
SA_RAS#	BB20	M_A_RAS#	14,16
SA_CAS#	BD20	M_A_CAS#	14,16
SA_WE#	AY20	M_A_WE#	14,16
SA_DM_0	AM37	M_A_DM0	14
SA_DM_1	AT141	M_A_DM1	14
SA_DM_2	AY41	M_A_DM2	14
SA_DM_3	AU39	M_A_DM3	14
SA_DM_4	BB12	M_A_DM4	14
SA_DM_5	AY6	M_A_DM5	14
SA_DM_6	AT7	M_A_DM6	14
SA_DM_7	AJ5	M_A_DM7	14
SA_DQS_0	AJ44	M_A_DQS0	14
SA_DQS_1	AT144	M_A_DQS1	14
SA_DQS_2	BA43	M_A_DQS2	14
SA_DQS_3	BC37	M_A_DQS3	14
SA_DQS_4	AW12	M_A_DQS4	14
SA_DQS_5	BC8	M_A_DQS5	14
SA_DQS_6	AU8	M_A_DQS6	14
SA_DQS_7	AM7	M_A_DQS7	14
SA_DQS#_0	AJ43	M_A_DQS#0	14
SA_DQS#_1	AT143	M_A_DQS#1	14
SA_DQS#_2	BA44	M_A_DQS#2	14
SA_DQS#_3	BD37	M_A_DQS#3	14
SA_DQS#_4	AY12	M_A_DQS#4	14
SA_DQS#_5	BD8	M_A_DQS#5	14
SA_DQS#_6	AU9	M_A_DQS#6	14
SA_DQS#_7	AM8	M_A_DQS#7	14
SA_MA_0	BA21	M_A_A0	14,16
SA_MA_1	BC24	M_A_A1	14,16
SA_MA_2	BC24	M_A_A2	14,16
SA_MA_3	BH24	M_A_A3	14,16
SA_MA_4	BG25	M_A_A4	14,16
SA_MA_5	BA24	M_A_A5	14,16
SA_MA_6	BD24	M_A_A6	14,16
SA_MA_7	BG27	M_A_A7	14,16
SA_MA_8	BF25	M_A_A8	14,16
SA_MA_9	AW24	M_A_A9	14,16
SA_MA_10	BC21	M_A_A10	14,16
SA_MA_11	BG26	M_A_A11	14,16
SA_MA_12	BH26	M_A_A12	14,16
SA_MA_13	BH17	M_A_A13	14,16
SA_MA_14	AY25	M_A_A14	14,16

15 M_B_DQ[63..0]

M B DQ0	AK47	SB_DQ_0
M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ48	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AJ47	SB_DQ_8
M B DQ9	AU46	SB_DQ_9
M B DQ10	BA48	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT147	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	BA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BG43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BF45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BG38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG39	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BF11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BC7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AY3	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AU3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AH1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

CANTIGA
null

DDR SYSTEM MEMORY B

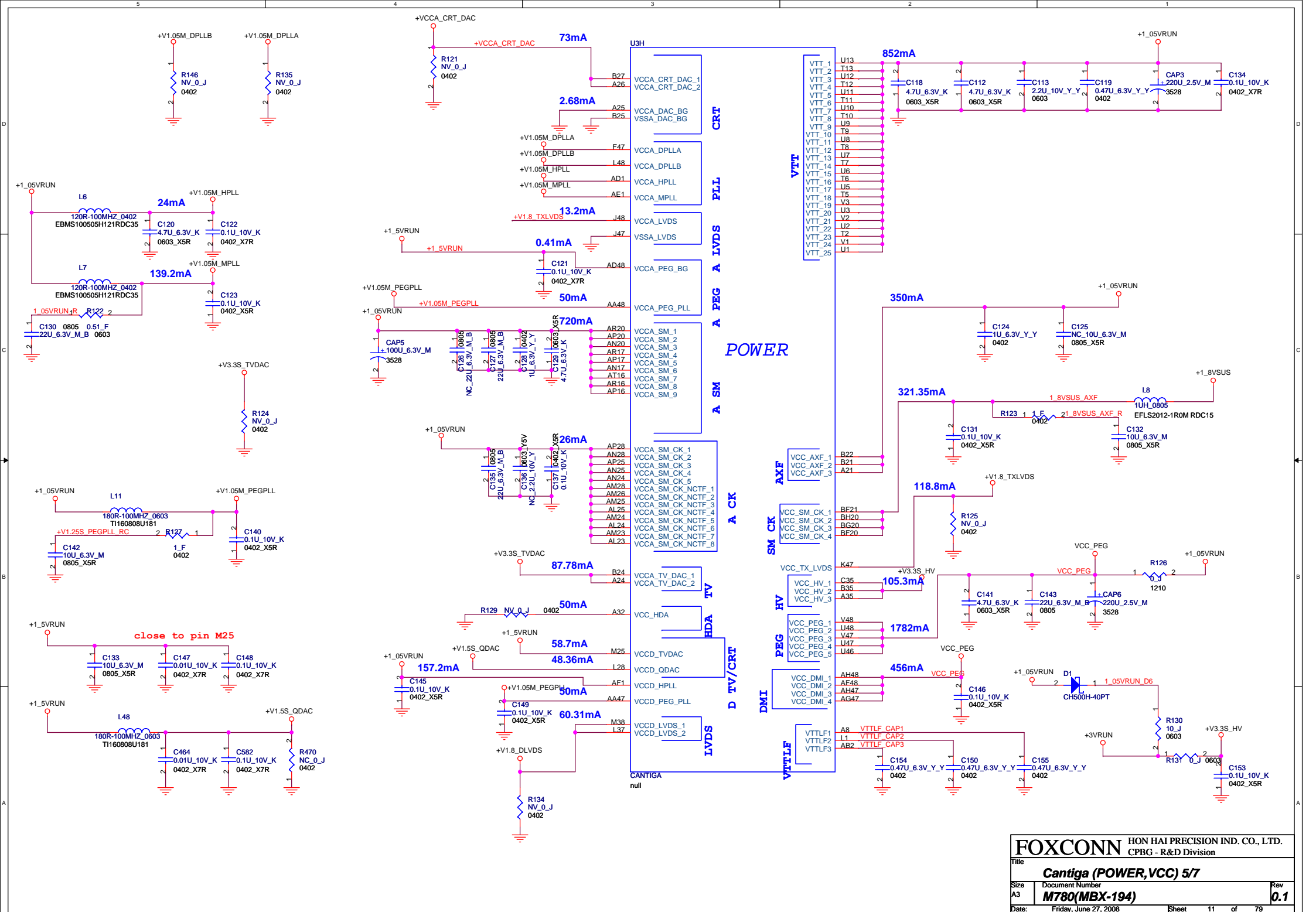
SB_BS_0	BC16	M_B_BS0	15,16
SB_BS_1	BB17	M_B_BS1	15,16
SB_BS_2	BB33	M_B_BS2	15,16
SB_RAS#	AU17	M_B_RAS#	15,16
SB_CAS#	BG16	M_B_CAS#	15,16
SB_WE#	BF14	M_B_WE#	15,16
SB_DM_0	AM47	M_B_DM0	15
SB_DM_1	AY47	M_B_DM1	15
SB_DM_2	BD40	M_B_DM2	15
SB_DM_3	BF35	M_B_DM3	15
SB_DM_4	BG11	M_B_DM4	15
SB_DM_5	BA3	M_B_DM5	15
SB_DM_6	AP1	M_B_DM6	15
SB_DM_7	AK2	M_B_DM7	15
SB_DQS_0	AJ47	M_B_DQS0	15
SB_DQS_1	AV48	M_B_DQS1	15
SB_DQS_2	BG41	M_B_DQS2	15
SB_DQS_3	BG37	M_B_DQS3	15
SB_DQS_4	BH9	M_B_DQS4	15
SB_DQS_5	BB2	M_B_DQS5	15
SB_DQS_6	AU1	M_B_DQS6	15
SB_DQS_7	AN6	M_B_DQS7	15
SB_DQS#_0	AL46	M_B_DQS#0	15
SB_DQS#_1	AV47	M_B_DQS#1	15
SB_DQS#_2	BH41	M_B_DQS#2	15
SB_DQS#_3	BH37	M_B_DQS#3	15
SB_DQS#_4	BG9	M_B_DQS#4	15
SB_DQS#_5	BC2	M_B_DQS#5	15
SB_DQS#_6	AT2	M_B_DQS#6	15
SB_DQS#_7	AN5	M_B_DQS#7	15
SB_MA_0	AV17	M_B_A0	15,16
SB_MA_1	BA25	M_B_A1	15,16
SB_MA_2	BC25	M_B_A2	15,16
SB_MA_3	AU25	M_B_A3	15,16
SB_MA_4	AW25	M_B_A4	15,16
SB_MA_5	BB28	M_B_A5	15,16
SB_MA_6	AU28	M_B_A6	15,16
SB_MA_7	AV28	M_B_A7	15,16
SB_MA_8	AT33	M_B_A8	15,16
SB_MA_9	BD33	M_B_A9	15,16
SB_MA_10	BB16	M_B_A10	15,16
SB_MA_11	AW33	M_B_A11	15,16
SB_MA_12	AY33	M_B_A12	15,16
SB_MA_13	BH15	M_B_A13	15,16
SB_MA_14	AU33	M_B_A14	15,16

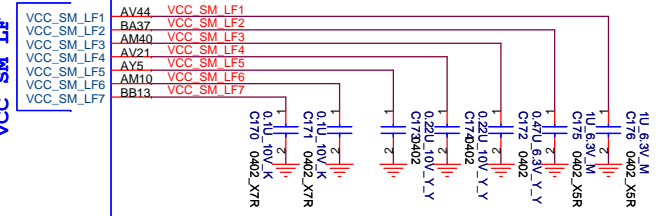
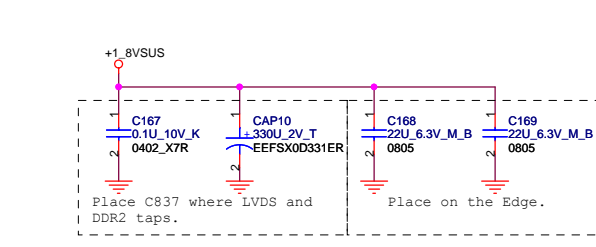
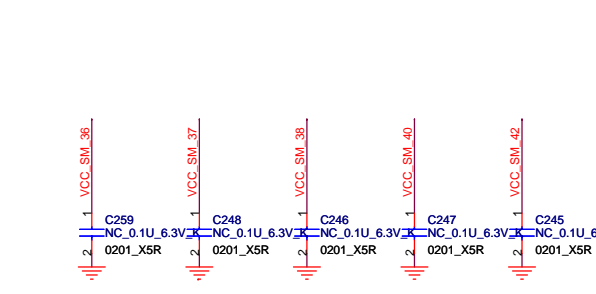
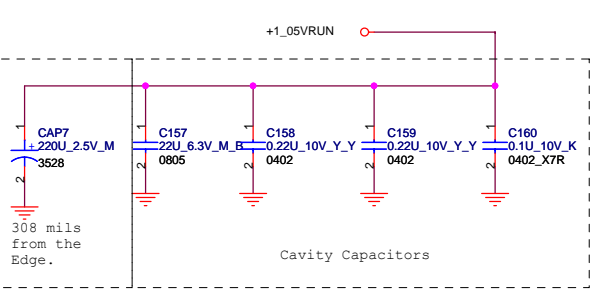
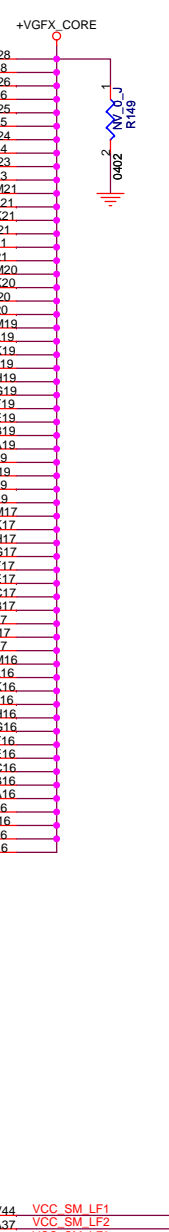
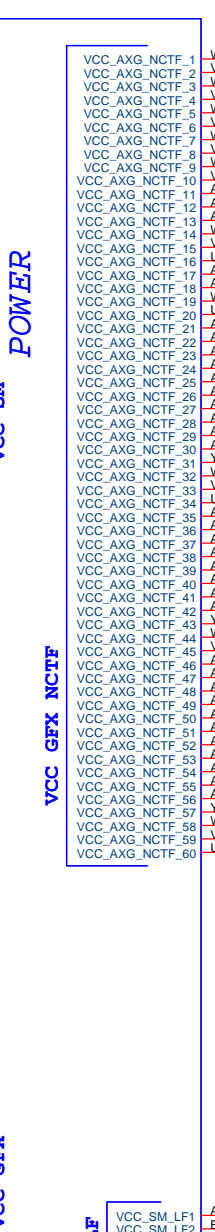
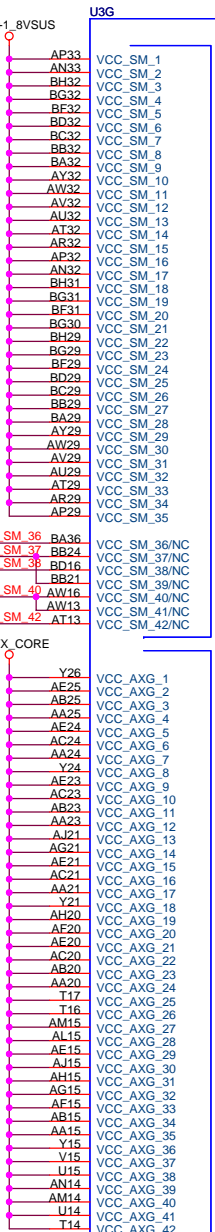
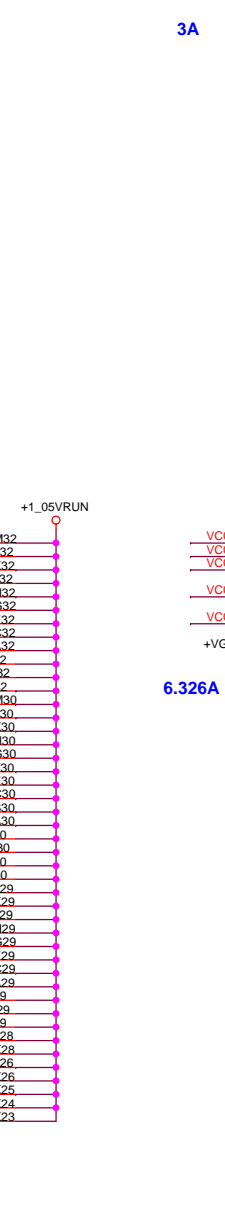
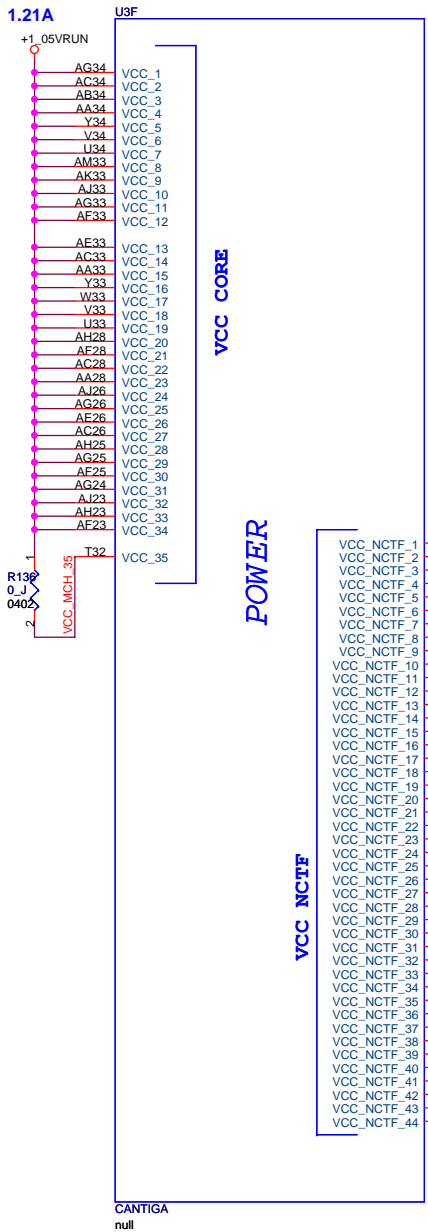
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Title: **Cantiga (DDRII) 4/7**

Size: A3 Document Number: **M780(MBX-194)** Rev: **0.1**

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Title: **Cantiga (VCC CORE) 6/7**

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U3I		
ALJ48	VSS_1	VSS_100
AR48	VSS_2	VSS_101
AL48	VSS_3	VSS_102
BB47	VSS_4	VSS_103
AW47	VSS_5	VSS_104
AL47	VSS_6	VSS_105
AF47	VSS_7	VSS_106
AD47	VSS_8	VSS_107
AB47	VSS_9	VSS_108
Y47	VSS_10	VSS_109
T47	VSS_11	VSS_110
L47	VSS_12	VSS_111
G47	VSS_13	VSS_112
BD46	VSS_14	VSS_113
BA46	VSS_15	VSS_114
AY46	VSS_16	VSS_115
AV46	VSS_17	VSS_116
AR46	VSS_18	VSS_117
AM46	VSS_19	VSS_118
V46	VSS_20	VSS_119
R46	VSS_21	VSS_120
P46	VSS_22	VSS_121
H46	VSS_23	VSS_122
F46	VSS_24	VSS_123
BF44	VSS_25	VSS_124
AH44	VSS_26	VSS_125
AD44	VSS_27	VSS_126
AA44	VSS_28	VSS_127
Y44	VSS_29	VSS_128
U44	VSS_30	VSS_129
T44	VSS_31	VSS_130
M44	VSS_32	VSS_131
F44	VSS_33	VSS_132
BC43	VSS_34	VSS_133
AV43	VSS_35	VSS_134
AU43	VSS_36	VSS_135
AM43	VSS_37	VSS_136
J43	VSS_38	VSS_137
C43	VSS_39	VSS_138
BG42	VSS_40	VSS_139
AY42	VSS_41	VSS_140
AT42	VSS_42	VSS_141
AN42	VSS_43	VSS_142
AJ42	VSS_44	VSS_143
AE42	VSS_45	VSS_144
N42	VSS_46	VSS_145
L42	VSS_47	VSS_146
BD41	VSS_48	VSS_147
AU41	VSS_49	VSS_148
AM41	VSS_50	VSS_149
AH41	VSS_51	VSS_150
AD41	VSS_52	VSS_151
AA41	VSS_53	VSS_152
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U41	VSS_55	VSS_154
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M41	VSS_57	VSS_156
G41	VSS_58	VSS_157
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AE39	VSS_69	VSS_168
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B39	VSS_72	VSS_171
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BC38	VSS_74	VSS_173
BA38	VSS_75	VSS_174
AU38	VSS_76	VSS_175
AH38	VSS_77	VSS_176
AD38	VSS_78	VSS_177
AA38	VSS_79	VSS_178
Y38	VSS_80	VSS_179
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C38	VSS_85	VSS_184
BF37	VSS_86	VSS_185
BB37	VSS_87	VSS_186
AV37	VSS_88	VSS_187
AM37	VSS_89	VSS_188
AJ37	VSS_90	VSS_189
AE37	VSS_91	VSS_190
N37	VSS_92	VSS_191
L37	VSS_93	VSS_192
B37	VSS_94	VSS_193
BH36	VSS_95	VSS_194
BC36	VSS_96	VSS_195
BA36	VSS_97	VSS_196
AU36	VSS_98	VSS_197
AH36	VSS_99	VSS_198
AD36		VSS_199

VSS

CANTIGA null

U3J		
BG21	VSS_199	VSS_297
L12	VSS_200	VSS_298
AW21	VSS_201	VSS_299
AU21	VSS_202	VSS_300
AP21	VSS_203	VSS_301
AN21	VSS_204	VSS_302
F36	VSS_205	VSS_303
AE21	VSS_206	VSS_304
AB21	VSS_207	VSS_305
R21	VSS_208	VSS_306
M21	VSS_209	VSS_307
J21	VSS_210	VSS_308
G21	VSS_211	VSS_309
BC20	VSS_212	VSS_310
BA20	VSS_213	VSS_311
AW20	VSS_214	VSS_312
AT20	VSS_215	VSS_313
AJ20	VSS_216	VSS_314
AG20	VSS_217	VSS_315
Y20	VSS_218	VSS_316
N20	VSS_219	VSS_317
K20	VSS_220	VSS_318
F20	VSS_221	VSS_319
C20	VSS_222	VSS_320
A20	VSS_223	VSS_321
BG19	VSS_224	VSS_322
AL33	VSS_225	VSS_323
AH33	VSS_226	VSS_324
AB33	VSS_227	VSS_325
P33	VSS_228	
L33	VSS_229	VSS_327
H33	VSS_230	VSS_328
N32	VSS_231	VSS_329
K32	VSS_232	VSS_330
F32	VSS_233	VSS_331
C32	VSS_234	VSS_332
A31	VSS_235	VSS_333
AN29		VSS_334
T29	VSS_237	VSS_335
N29	VSS_238	VSS_336
K29	VSS_239	VSS_337
H29	VSS_240	VSS_338
F29	VSS_241	VSS_339
A29	VSS_242	VSS_340
BG28	VSS_243	VSS_341
BD28	VSS_244	VSS_342
BA28	VSS_245	VSS_343
W15	VSS_246	VSS_344
A15	VSS_247	VSS_345
BG14	VSS_248	VSS_346
AA14	VSS_249	VSS_347
C14	VSS_250	VSS_348
BG13	VSS_251	VSS_349
BC13	VSS_252	VSS_350
BA13		VSS_351
		VSS_352
		VSS_353
		VSS_354
AN13	VSS_255	
AJ13	VSS_256	
AE13	VSS_257	
F26	VSS_258	
C28	VSS_259	
N13	VSS_260	
L13	VSS_261	
G13	VSS_262	
E13	VSS_263	
BF12	VSS_264	
AV12	VSS_265	
C26	VSS_266	
AM12	VSS_267	
AA12	VSS_268	
J12	VSS_269	
A12	VSS_270	
BD11	VSS_271	
BB11	VSS_272	
AY11	VSS_273	
AN11	VSS_274	
AH11	VSS_275	
	VSS_276	
Y11	VSS_277	
N11	VSS_278	
G11	VSS_279	
C11	VSS_280	
E11	VSS_281	
BF10	VSS_282	
AV10	VSS_283	
AT10	VSS_284	
AJ10	VSS_285	
AF10	VSS_286	
AA10	VSS_287	
M10	VSS_288	
BF9	VSS_289	
BC9	VSS_290	
L24	VSS_291	
AM9	VSS_292	
J24	VSS_293	
AG24	VSS_294	
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BH8	VSS_296	
BB8	VSS_297	
AV8	VSS_298	
AT8	VSS_299	
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		VSS_NCTF_2
		VSS_NCTF_3
		VSS_NCTF_4
		VSS_NCTF_5
		VSS_NCTF_6
		VSS_NCTF_7
		VSS_NCTF_8
		VSS_NCTF_9
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		VSS_SCB_2
		VSS_SCB_3
		VSS_SCB_4
		VSS_SCB_5
		VSS_SCB_1
		VSS_SCB_2
		VSS_SCB_3
		VSS_SCB_4
		VSS_SCB_5
		NC_26
		NC_27
		NC_28
		NC_29
		NC_30
		NC_31
		NC_32
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		NC_34
		NC_35
		NC_36
		NC_37
		NC_38
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		NC_41
		NC_42

VSS

VSS NCTF

VSS SCB

NC

CANTIGA null

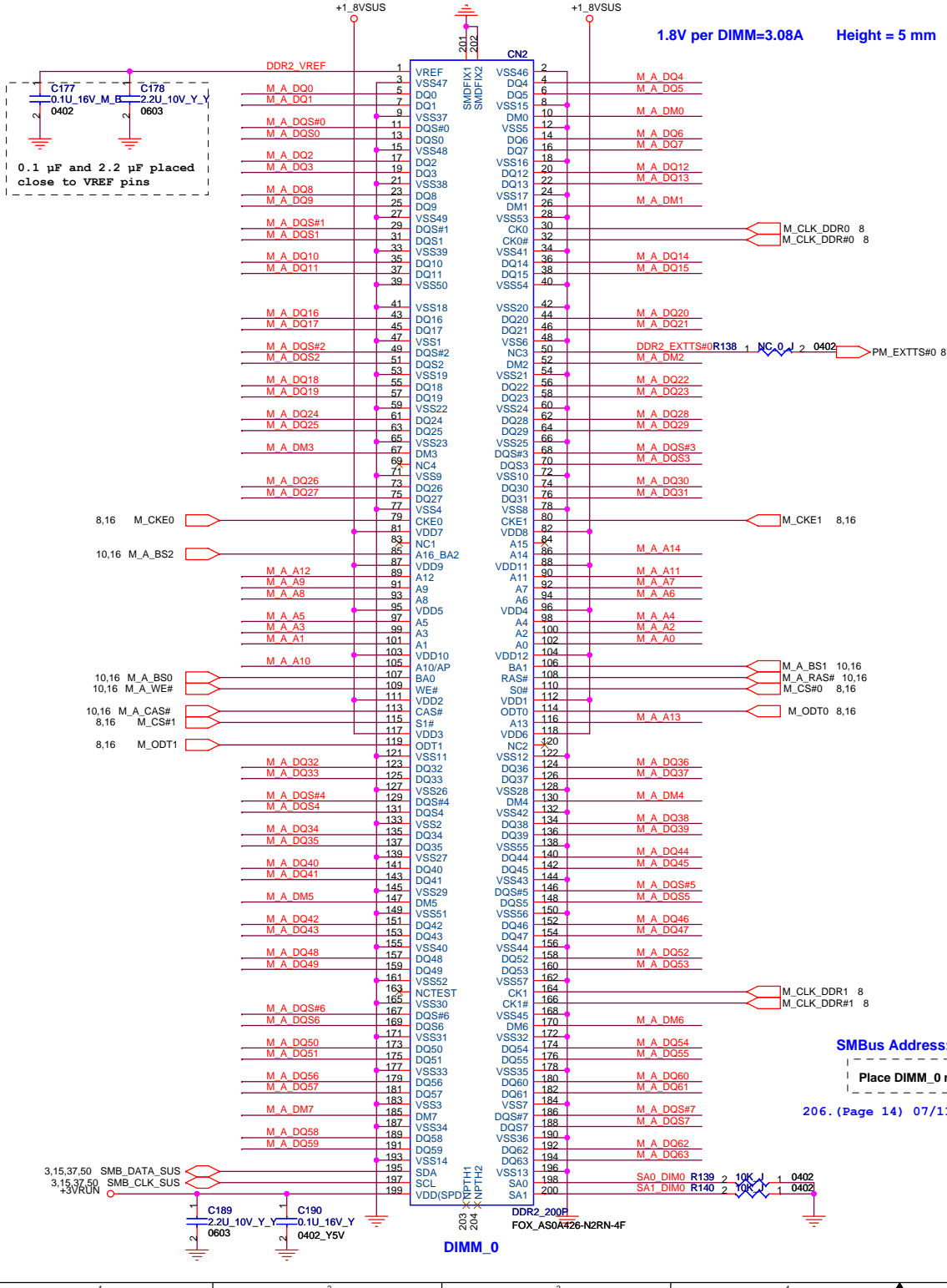
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U28	26MIL	TP97
U25	26MIL	TP98
U29	26MIL	TP99
AF32	26MIL	TP100
AB32	26MIL	TP101
V32	26MIL	TP102
AJ30	26MIL	TP103
AM29	26MIL	TP104
AE29	26MIL	TP105
AB29	26MIL	TP106
U26	26MIL	TP107
AC2	26MIL	TP108
U23	26MIL	TP109
AL20	26MIL	TP110
U20	26MIL	TP111
AC19	26MIL	TP112
AL17		
AJ17		
AA17		
U17		
BH48		
BH1		
A48		
C1		
A3		
E1		
D2		
C3		
B4		
A5		
A6		
A43		
A44		
B45		
C46		
D47		
B47		
E48		
F48		
E48		
C48		
B48		

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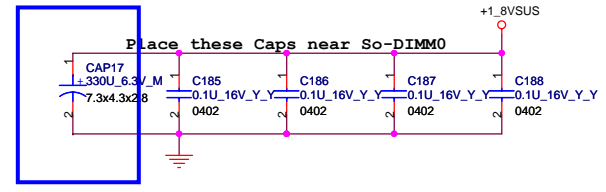
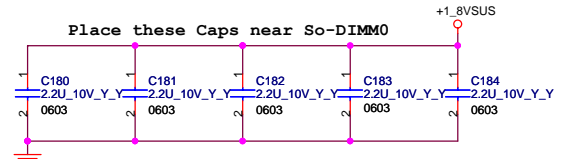
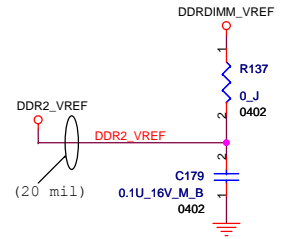
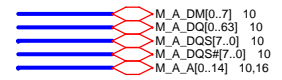
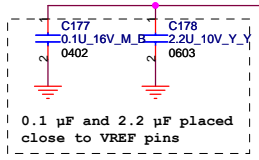
Title: **Cantiga (VSS) 7/7**

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1.8V per DIMM=3.08A Height = 5 mm

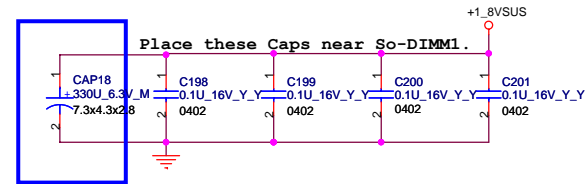
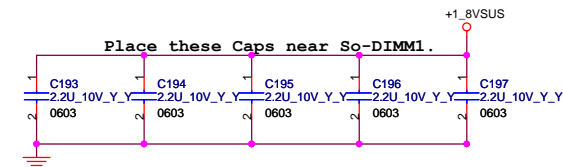
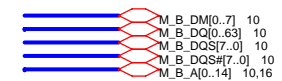
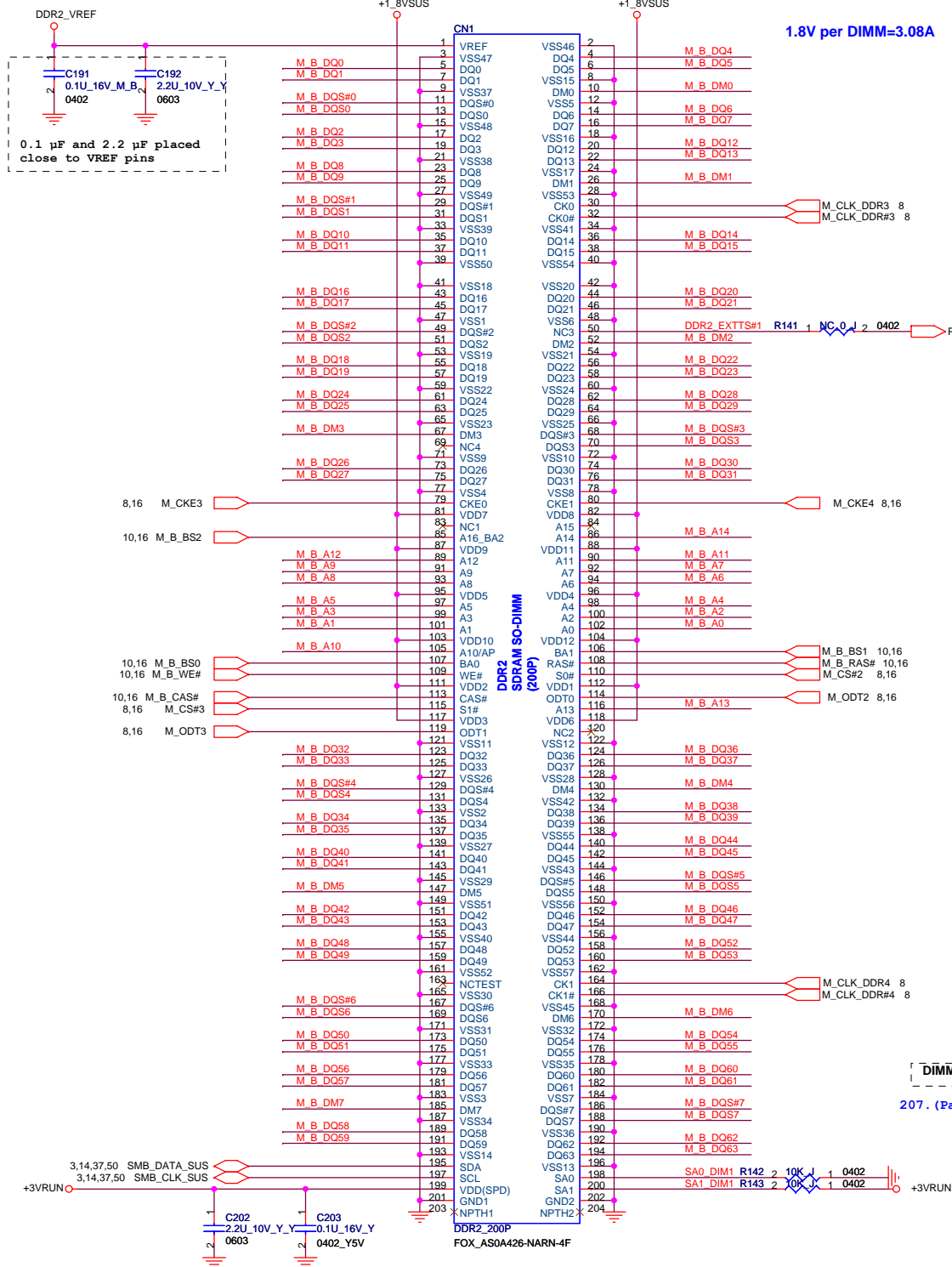


SMBus Address: A0H(W)/A1H(R)

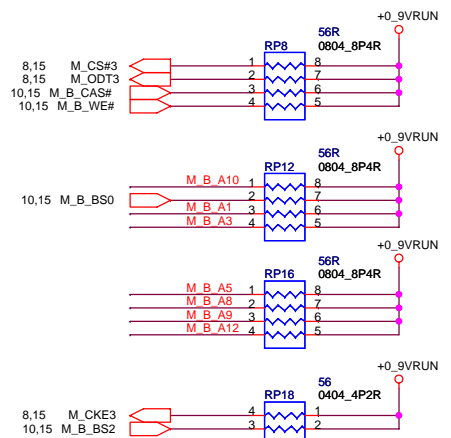
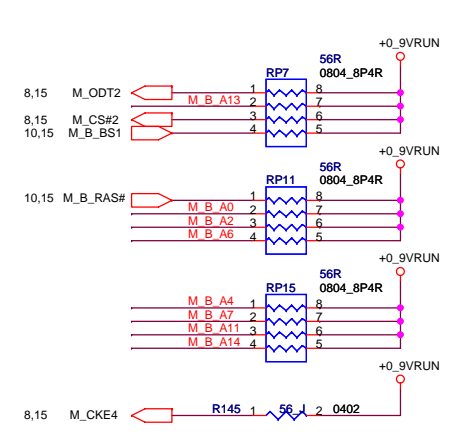
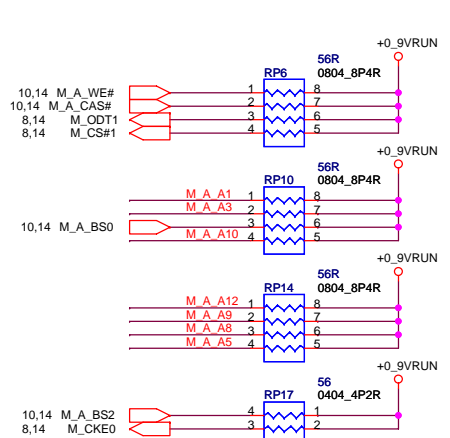
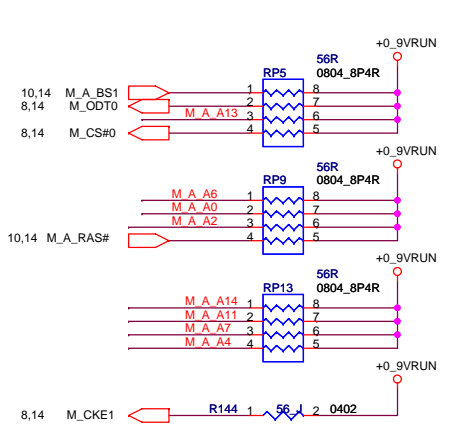
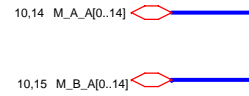
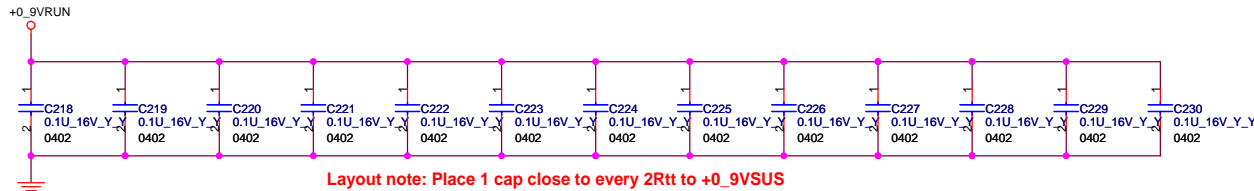
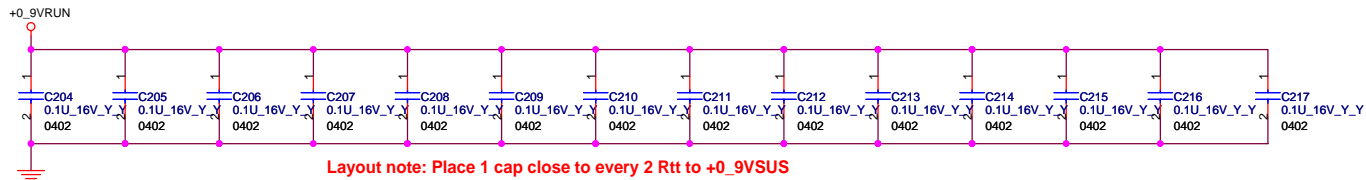
Place DIMM_0 near GMCH

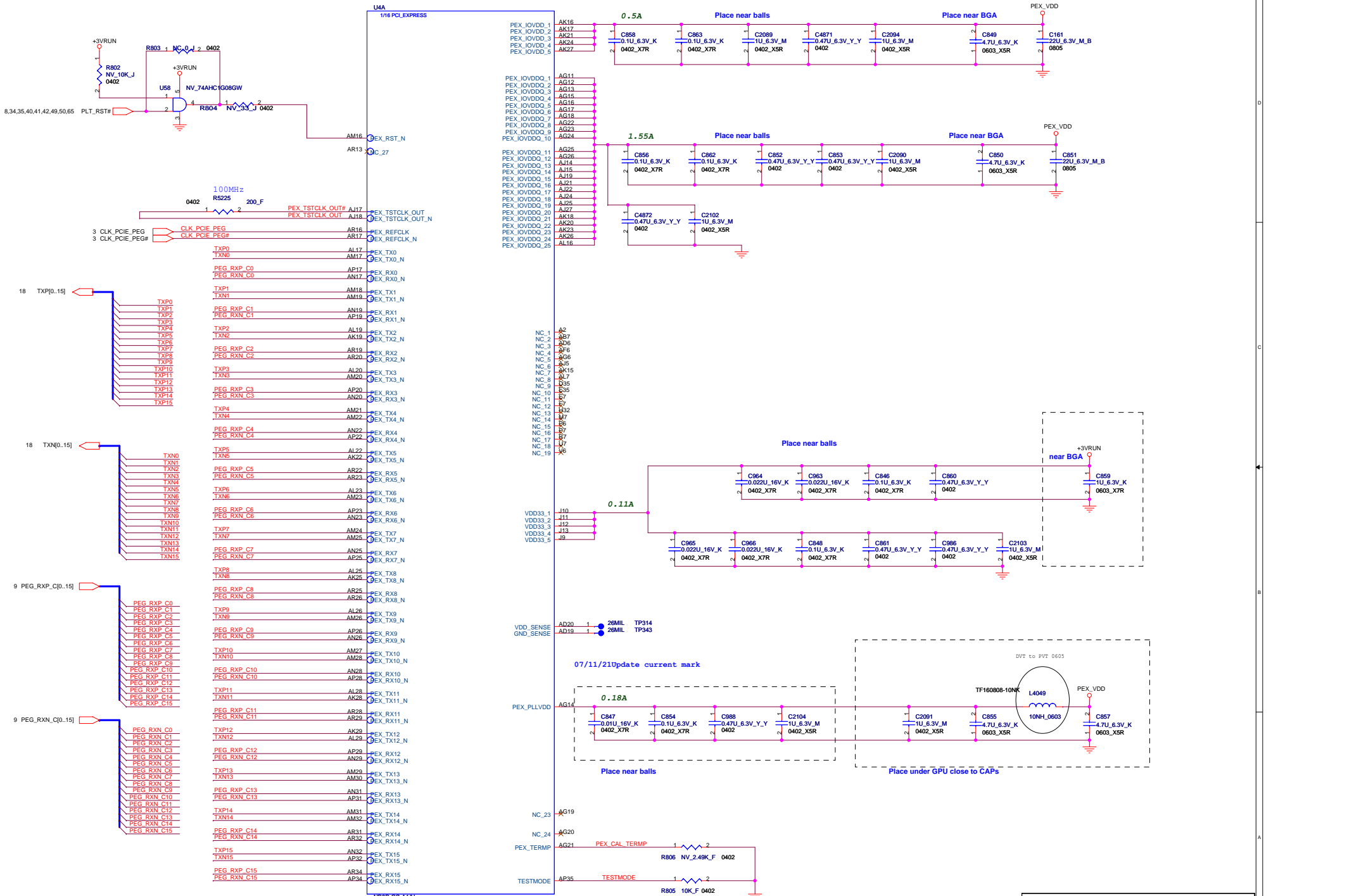
206. (Page 14) 07/11/27 change DDR2 CONN(CN1) from FOX_AS0A426-N5SN-7F to FOX_AS0A426_MN2RN_7F

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title DDR(II)SO-DIMM_0			
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Title		DDR(II)SO-DIMM_1	
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XCLK_277	
0 (Reserved)	
1 (27M Hz)	
NB9X TVMODE[2:0]	
000	
SUB_VENDOR	
0 (No vedio BIOS ROM)	ROM_SI (XXXX)
1 (BIOS ROM is present)	
SLOT_CLK_CFG	
0 (GPU and MCH not share a common reference clk)	ROM_SO (1000)
1 (GPU and MCH share a common reference clk)	
PEX_PLL_EN_TERM	
0 (Disable)	ROM_SCLK (0010)
1 (Enable)	
USER[3:0]	
1000	STRAP0 (1111)
NB9X 3GIO_PADCFG[3:0]	
0001	STRAP1 (0001)
NB9X PCI_DEVID[4:0]	
NB9P-GS X1001	STRAP2 (1001)
NB9M-GS X1001	

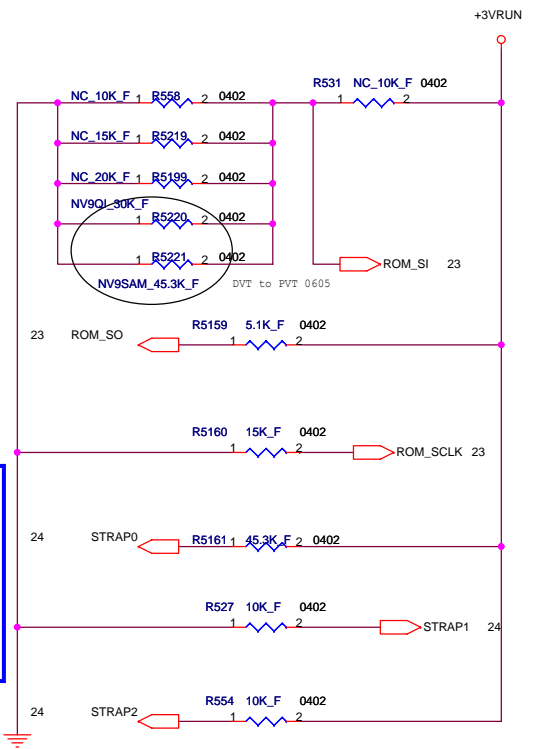
<< ROM_SI Setting condition >>

H Model
=> 32Mx32bx4 - 0101 Qimonda - 30K pull Low

M Model
=> 32Mx32bx4 - 0101(Qimonda) - 30K pul Low

L Model
=> 32Mx32bx2 - 0101 Qimonda - 30K pull Low

0100	64-bit Reserved
0101	32Mx32 GDDR3 - 136 ball - monolithic 64-bit Qimonda
0110	32Mx32 GDDR3 - 136 ball - monolithic 64-bit Hynix
0111	32Mx32 GDDR3 - 136 ball - monolithic 64-bit Samsung
0000	64-bit Reserved
0001	16Mx32 GDDR3 - 136 ball 64-bit Qimonda
0010	16Mx32 GDDR3 - 136 ball 64-bit Hynix
0011	16Mx32 GDDR3 - 136 ball 64-bit Samsung



Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

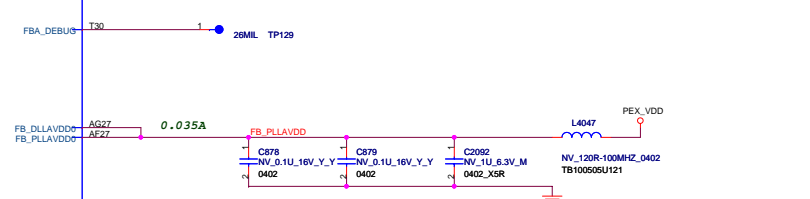
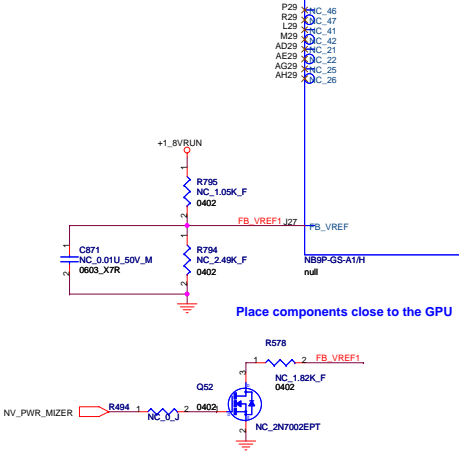
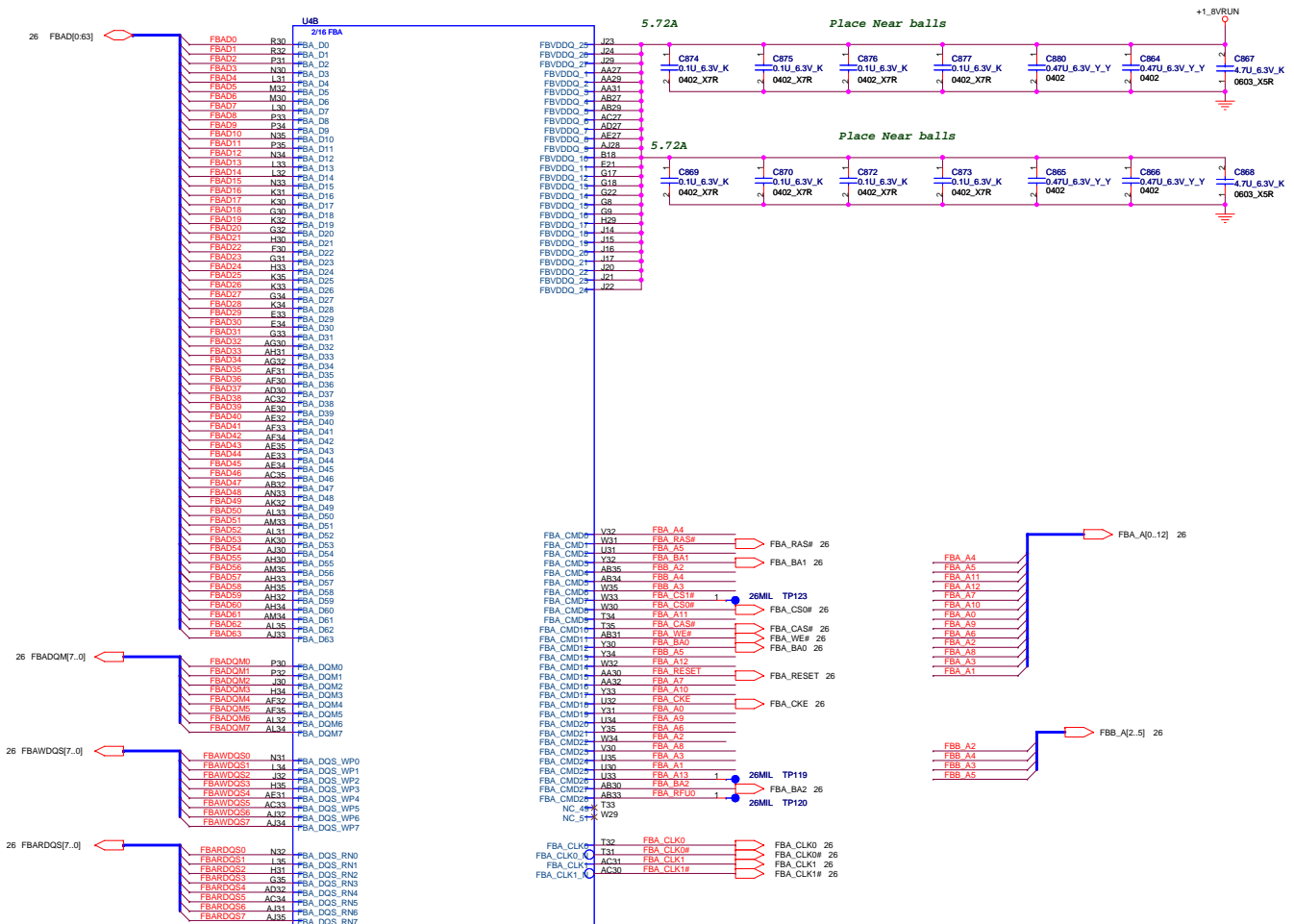
Refer to <GB1 Family Design Guide DG-03276-001_v01_secured>

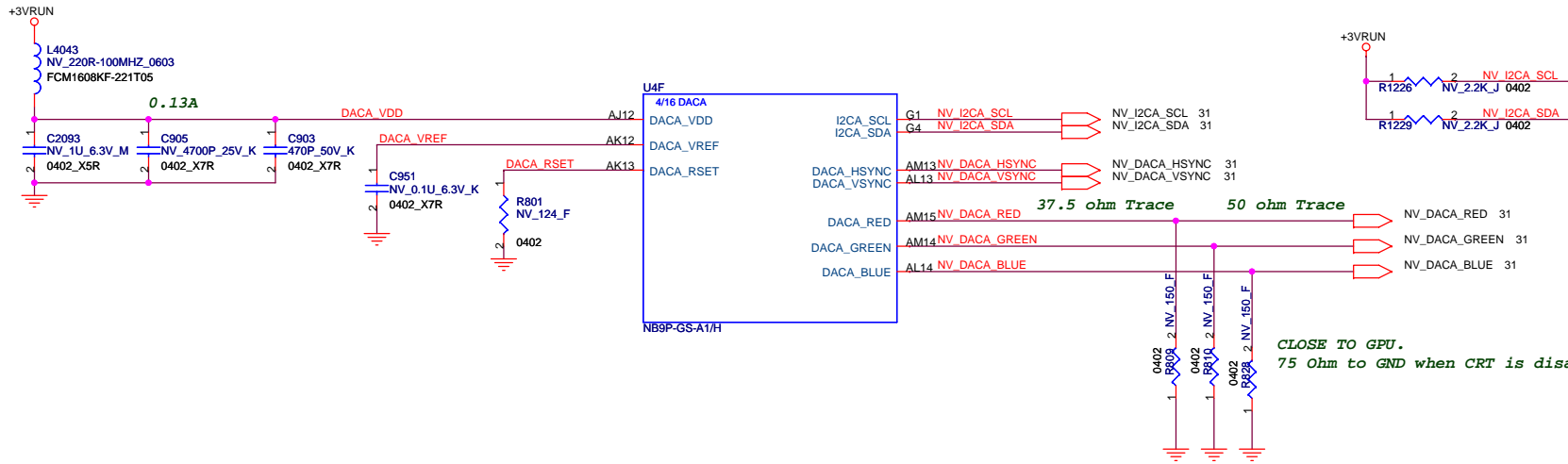
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Title: **VGA (PCI-EXPRESS/STRAP) 2 OF 9**

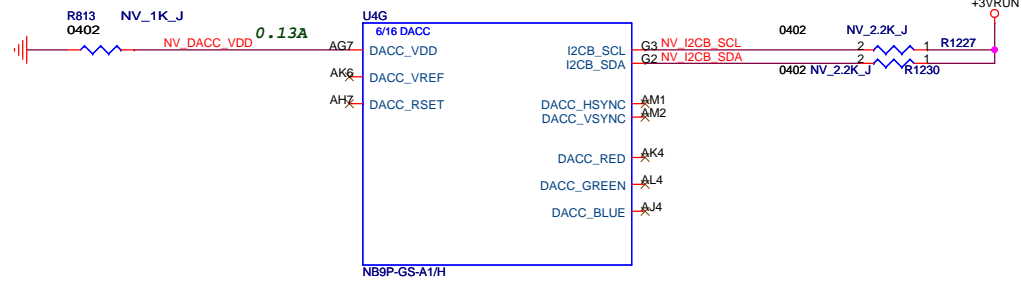
Size: Document Number **M780(MBX-194)** Rev **0.1**

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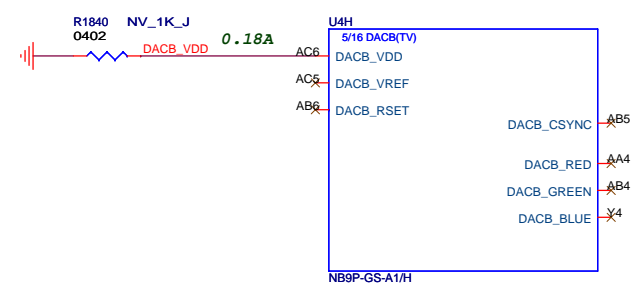


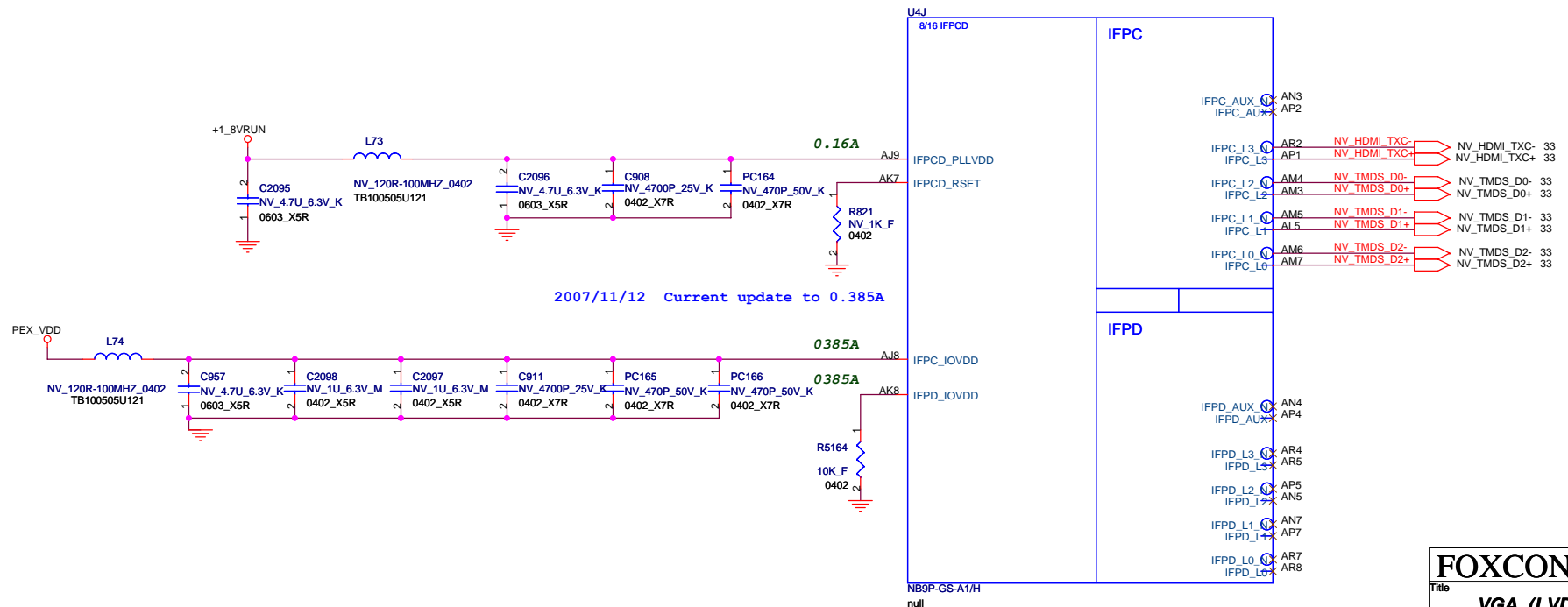
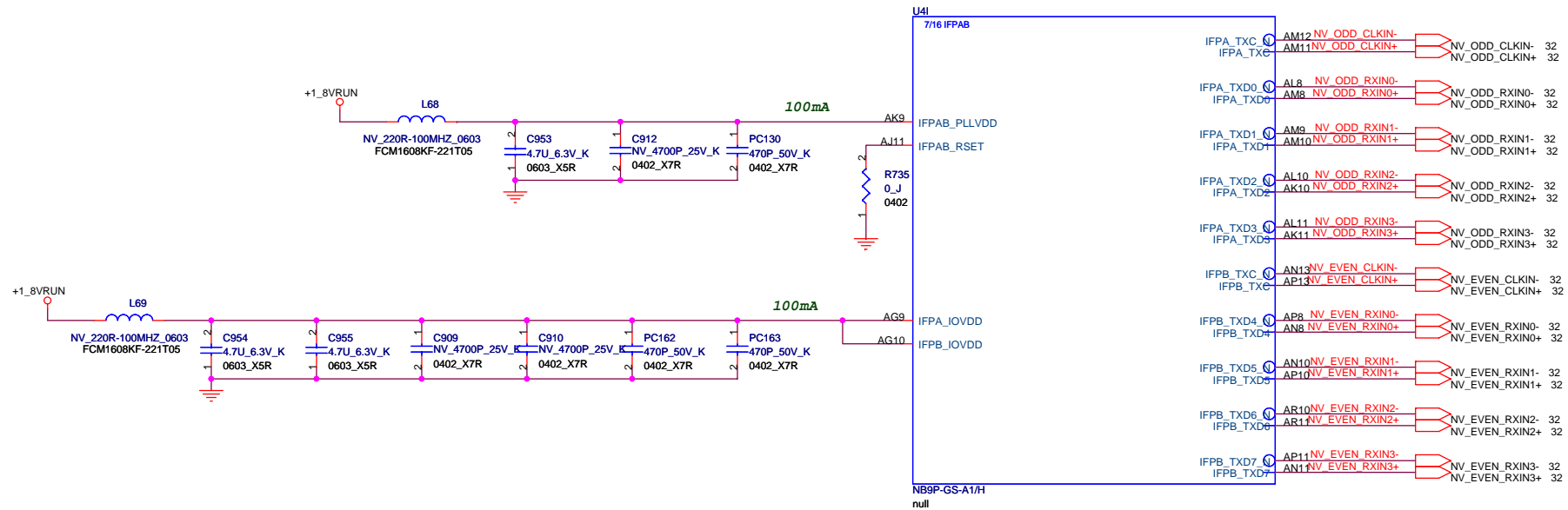


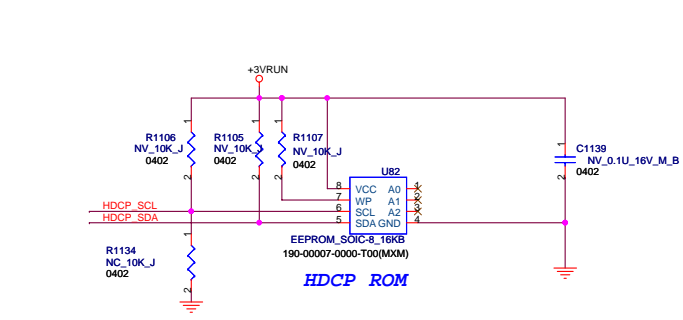
CLOSE TO GPU.
75 Ohm to GND when CRT is disabled.



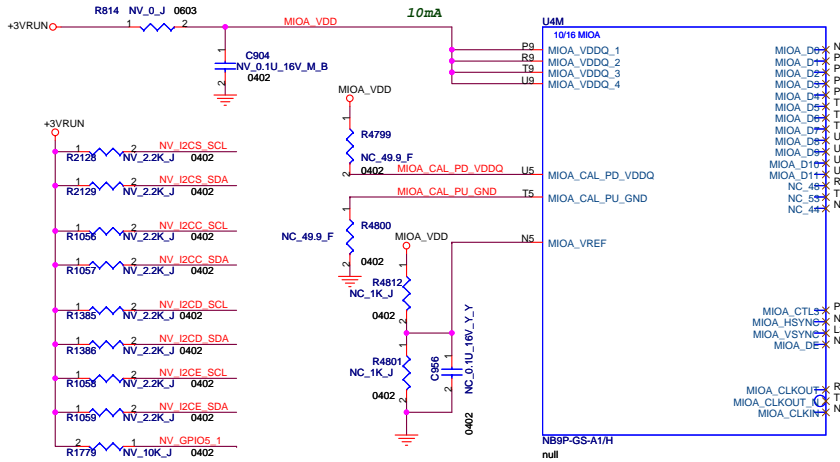
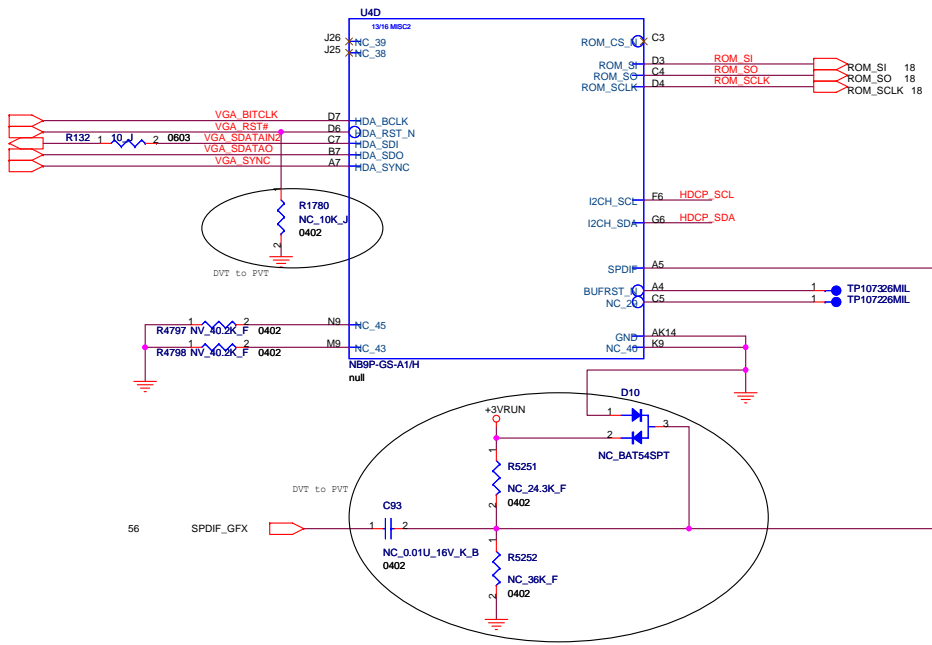
DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCLK	SCD
	VGA-DDCCLK	SdA



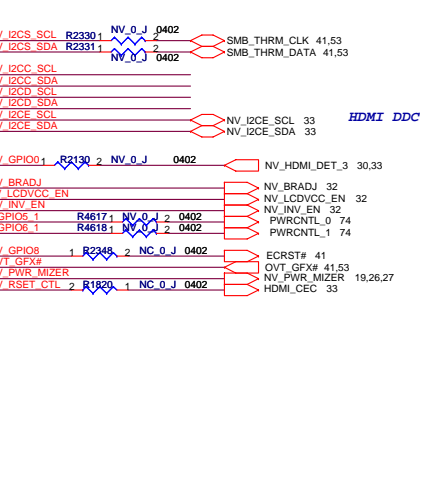
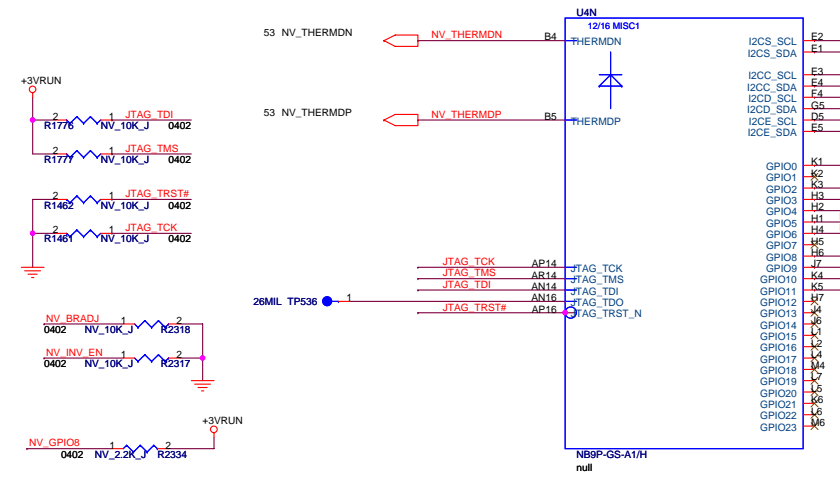




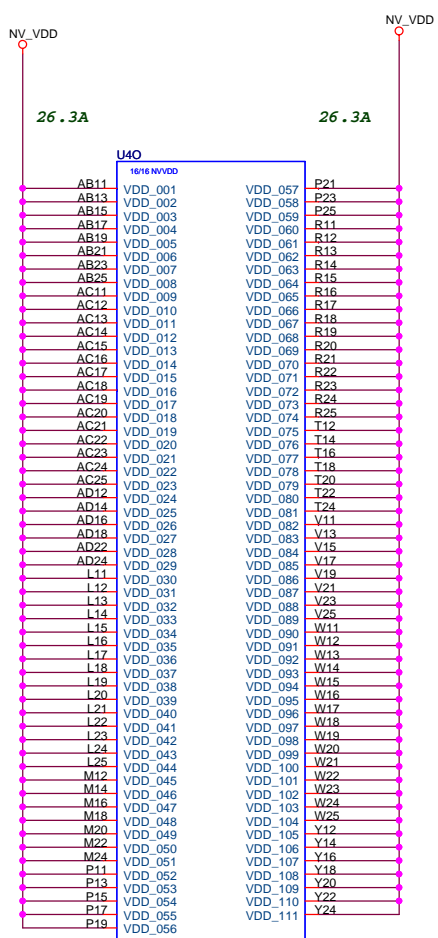
- 36 VGA_BITCLK
- 36 VGA_RST#
- 36 VGA_SDATAIN1
- 36 VGA_SDATAO
- 36 VGA_SYNC



GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes	HDMI Hot Plug Detect 0 (HPD0)	Active High
GPIO1	I	Yes		
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power(LCD0_VDD)	Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	Active High
GPIO5	O	Yes	FOR NVDD 0.9V-1.17V	Active High
GPIO6	O	No	reserve for NVDD adjust.	
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	Active Low
GPIO10	O	No	Memory Vref switch(MEM_VREF)	Active High
GPIO11	I/O	No	HDMI CEC Function Backup	

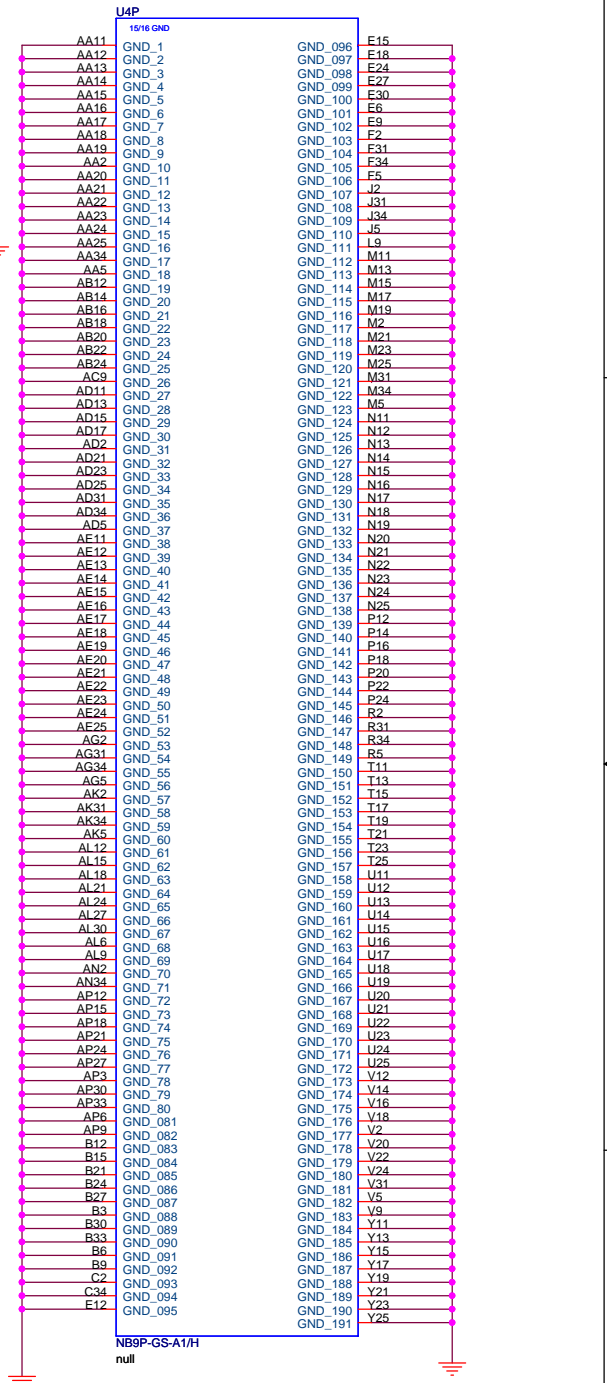
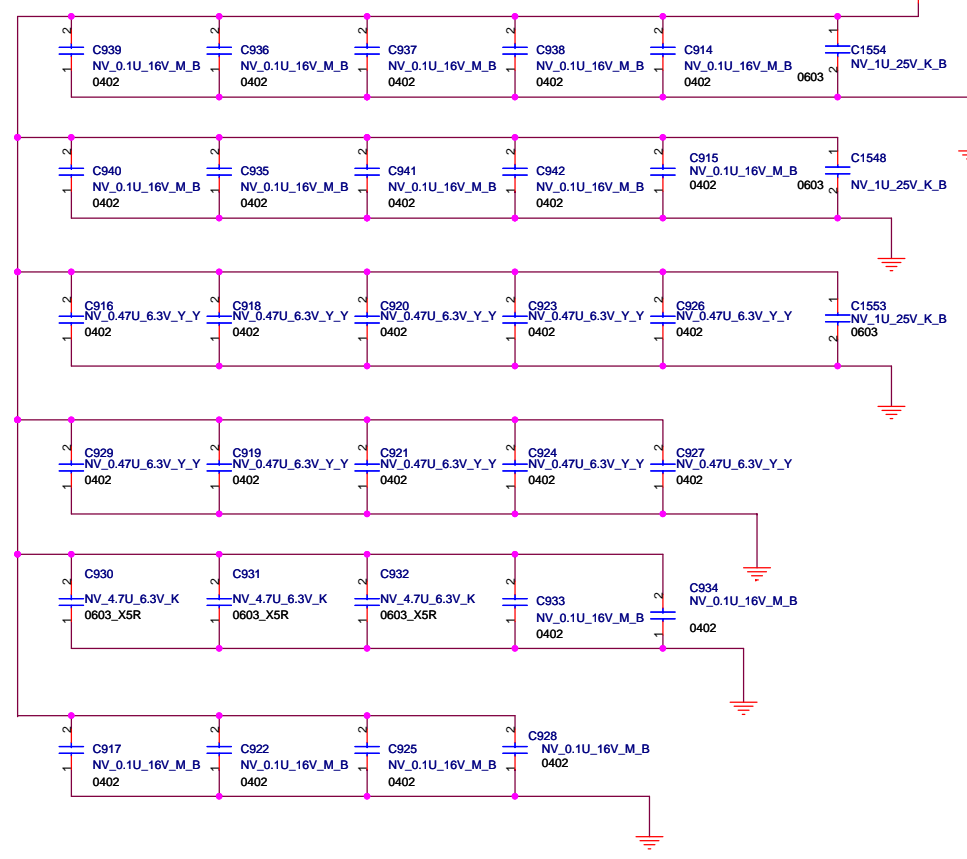


SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(All Other I2C_Compatibal Bus Signals)
I2CD_SCL I2CD_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CE_SCL I2CE_SDA	I/O	Notebook DVI I2C_Compatibal Bus Signals
I2CS_SCL I2CS_SDA	I/O	For VGA thermal I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor



PLACE NEAR BALLS

NEAR BGA

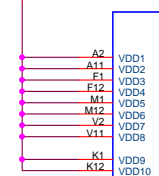
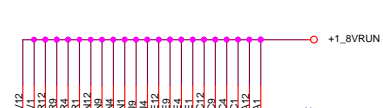
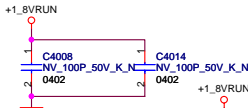
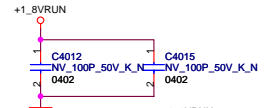


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Title: **VGA(POWER/GROUND) 9/9**

Size: Document Number
A3: **M780(MBX-194)** Rev: **0.1**

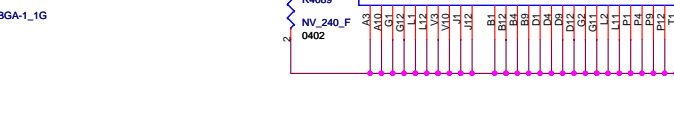
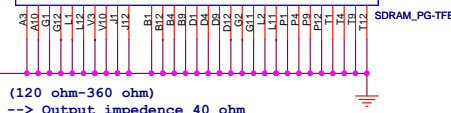
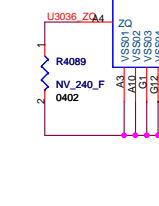
Date: Friday, June 13, 2008 Sheet 25 of 79



MIRROR TABLE

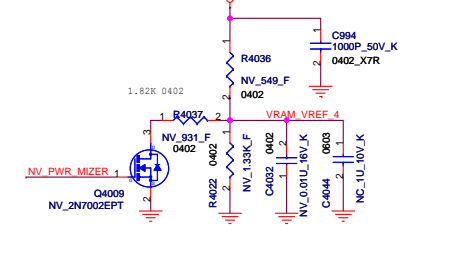
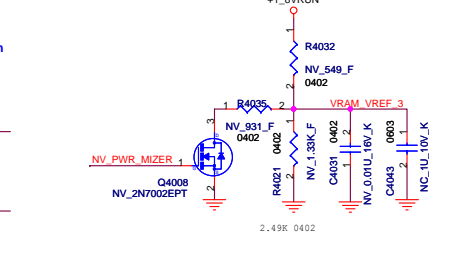
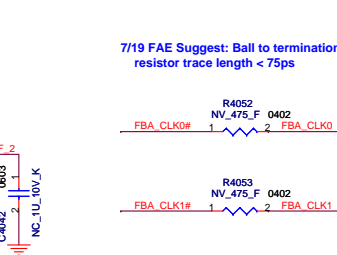
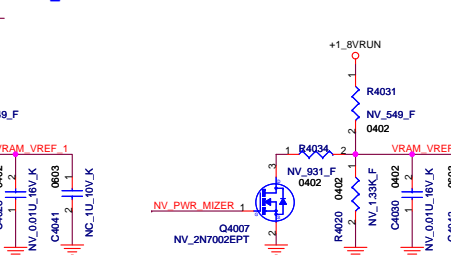
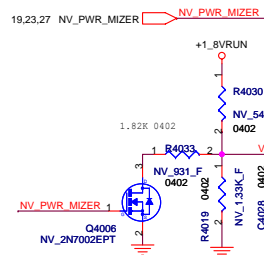
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H3	H10	RAS#	RAS#
F4	F9	CAS#	CAS#
H9	H4	WE#	WE#
F9	F4	CS#	CS#
H4	H9	CKE	CKE
K4	K9	A0	A0
H2	H1	A1	A1
K3	K10	A2	A2
M4	M9	A3	A3
K9	K4	A4	A4
H11	H2	A5	A5
K10	K3	A6	A6
L9	L4	A7	A7
K2	K2	A8	A8
M9	M4	A9	A9
K1	K11	A10	A10
L4	L9	A11	A11
G4	G9	BA0	BA0
G9	G4	BA1	BA1
H10	H3	BA2	BA2

FBAD8	T3	DQ31
FBAD9	T2	DQ30
FBAD11	R3	DQ29
FBAD10	R2	DQ28
FBAD15	M3	DQ27
FBAD12	N2	DQ26
FBAD14	L3	DQ25
FBAD13	M2	DQ24
FBAD1	T10	DQ24
FBAD0	T11	DQ22
FBAD2	R10	DQ23
FBAD3	R11	DQ21
FBAD5	M10	DQ19
FBAD6	N11	DQ18
FBAD7	M11	DQ17
FBAD4	M11	DQ17
FBAD17	G10	DQ15
FBAD21	F11	DQ16
FBAD16	F10	DQ14
FBAD19	E11	DQ12
FBAD20	R10	DQ11
FBAD18	C11	DQ10
FBAD23	B10	DQ10
FBAD22	B11	DQ8
FBAD25	G3	DQ8
FBAD26	F2	DQ7
FBAD28	F3	DQ5
FBAD24	E2	DQ4
FBAD29	C3	DQ4
FBAD31	C2	DQ3
FBAD30	B3	DQ1
FBAD27	B2	DQ0



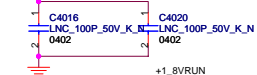
VREF	
H	50%
L	70%

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V



7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

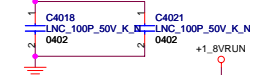
+1.8VRUN



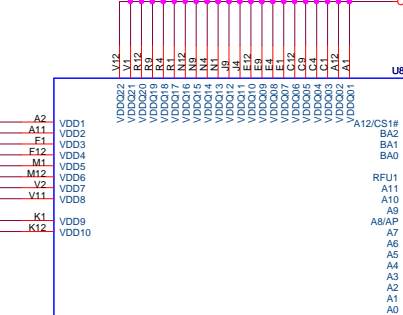
+1.8VRUN



+1.8VRUN



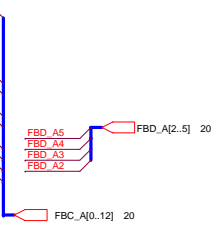
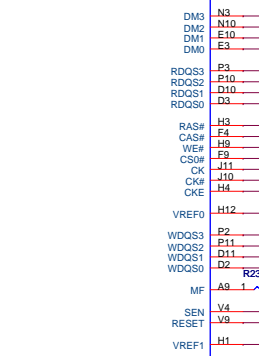
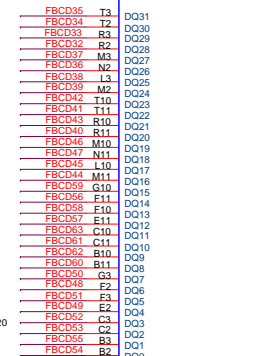
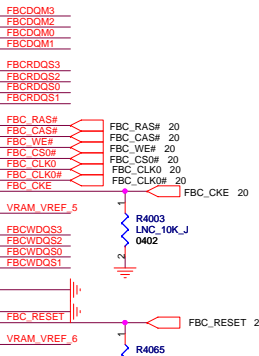
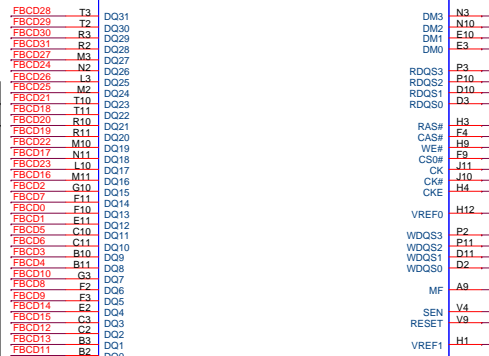
+1.8VRUN



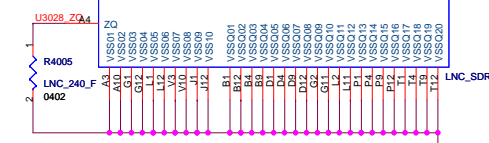
+1.8VRUN

MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F4	F9	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H5	BA2



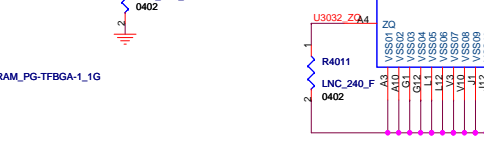
	0..30	32..63
CMD0	A4	RAS#
CMD1	A5	CAS#
CMD2	A5	CAS#
CMD3	BA1	BA1
CMD4	A2	A2
CMD5	A4	A4
CMD6	A4	A4
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13	A5	A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	A2
CMD23	A8	A8
CMD24	A3	A3
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2



R6,R15 (120 ohm-360 ohm) 240 ohm --> Output impedance 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

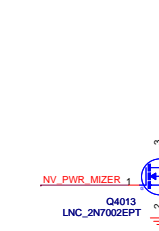
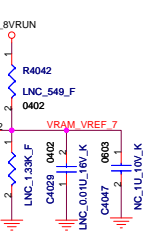
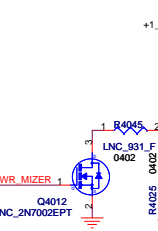
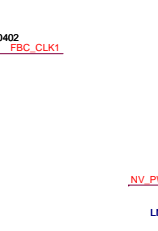
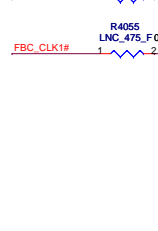
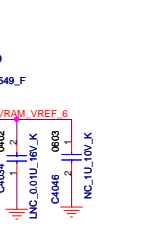
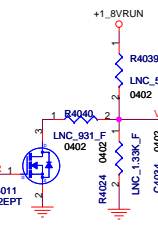
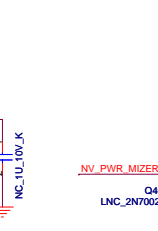
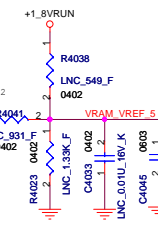
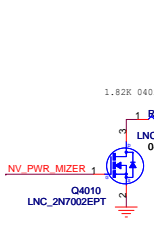
19.23.26 NV_PWR_MIZER



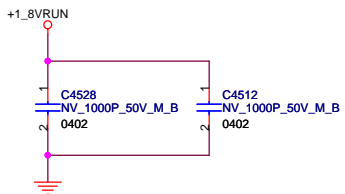
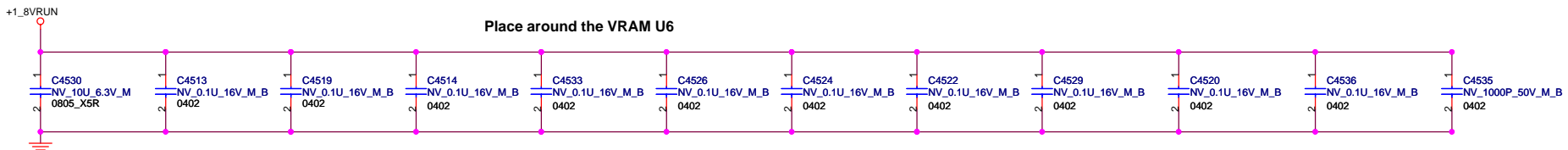
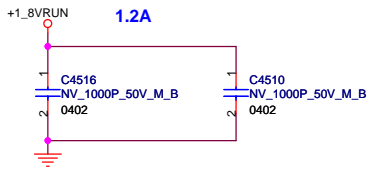
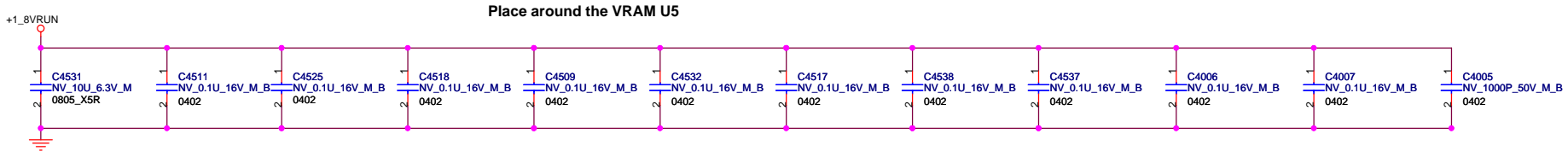
R6,R15 (120 ohm-360 ohm) 240 ohm --> Output impedance 40 ohm

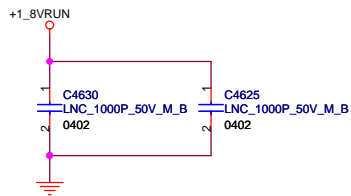
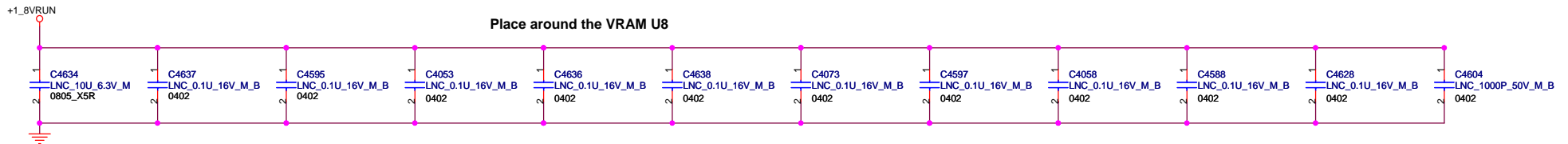
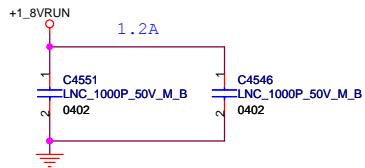
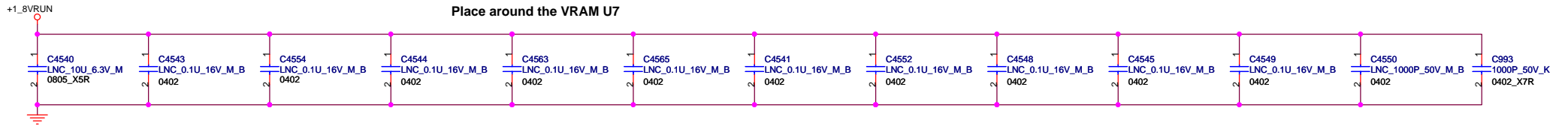
VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

19.23.26 NV_PWR_MIZER

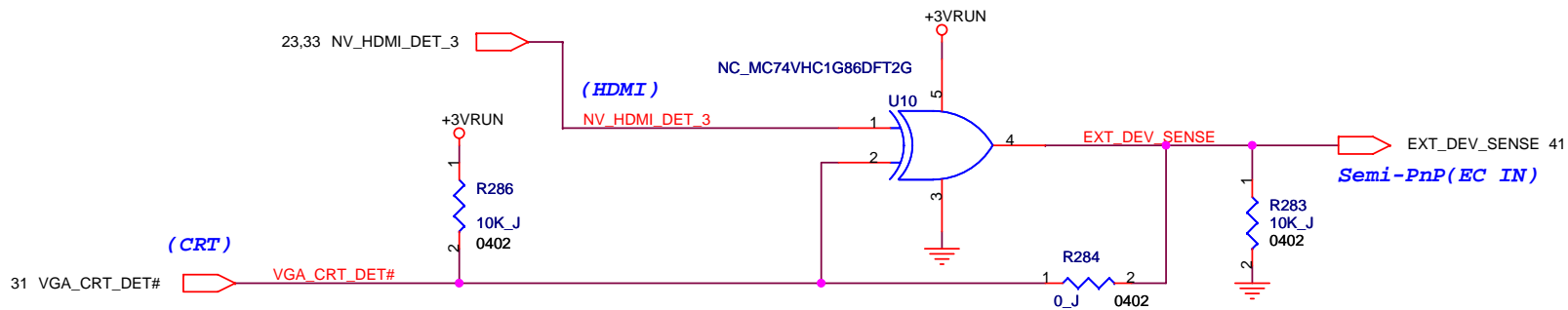


		VREF	
NV_PWR_MIZER	H	50%	
	L	70%	

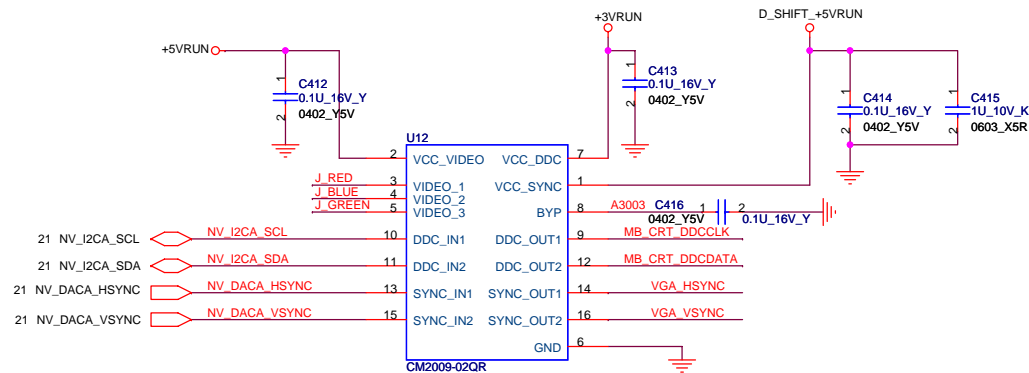
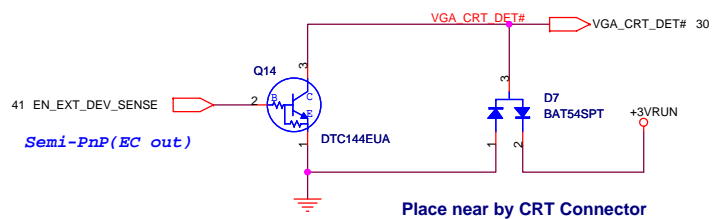




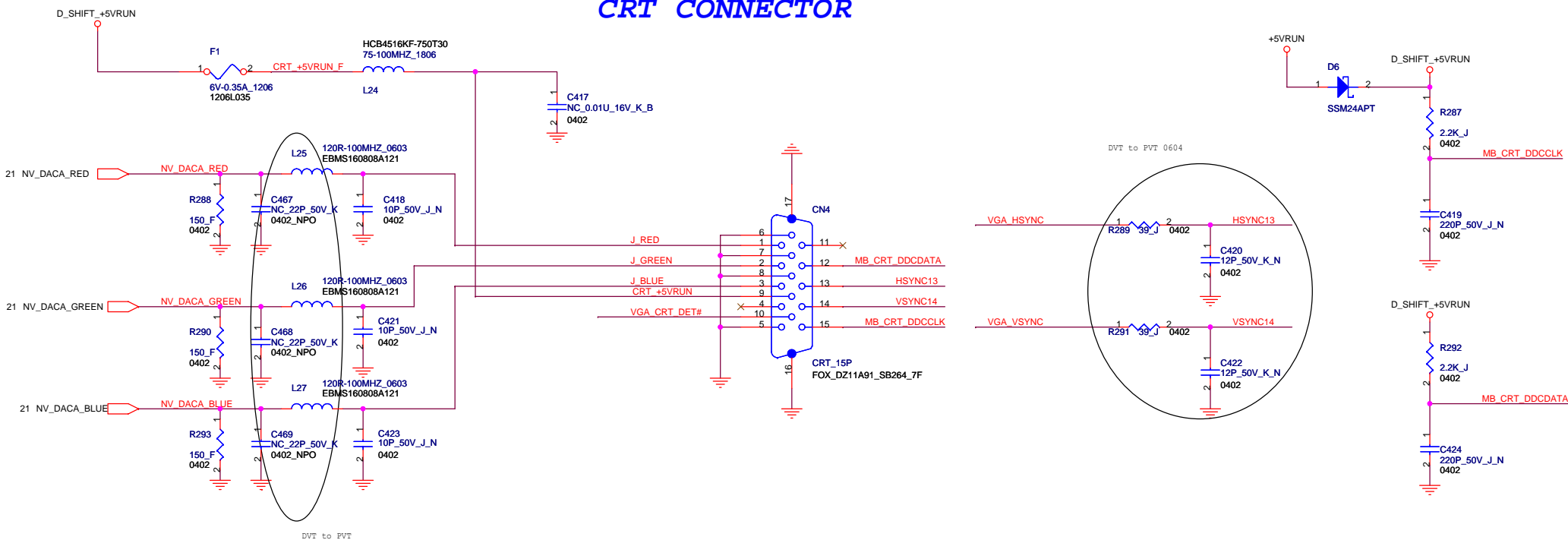
Semi-PnP Circuit



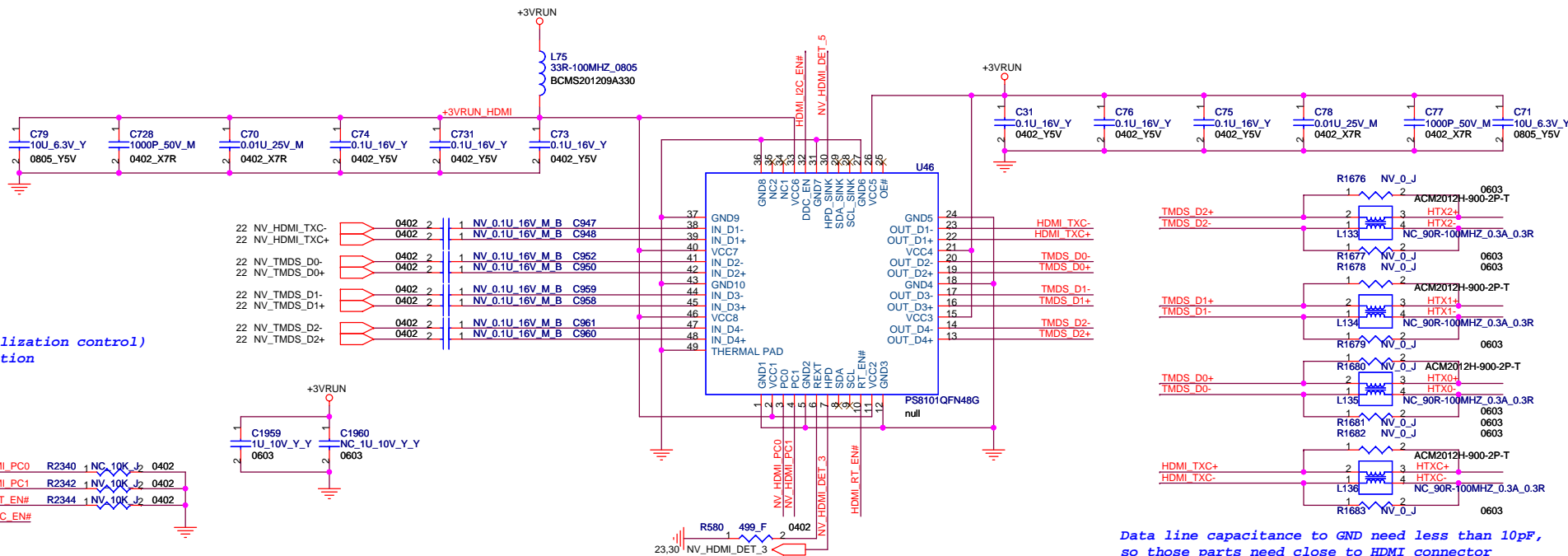
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		CPBG - R&D Division	
Title			
Semi-PnP			
Size	Document Number		Rev
Custom	M780(MBX-194)		0.1
Date:	Friday, June 13, 2008	Sheet	30 of 79



CRT CONNECTOR

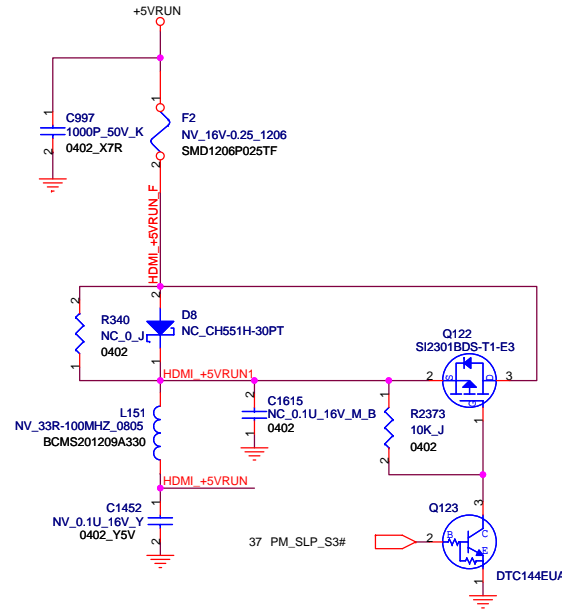
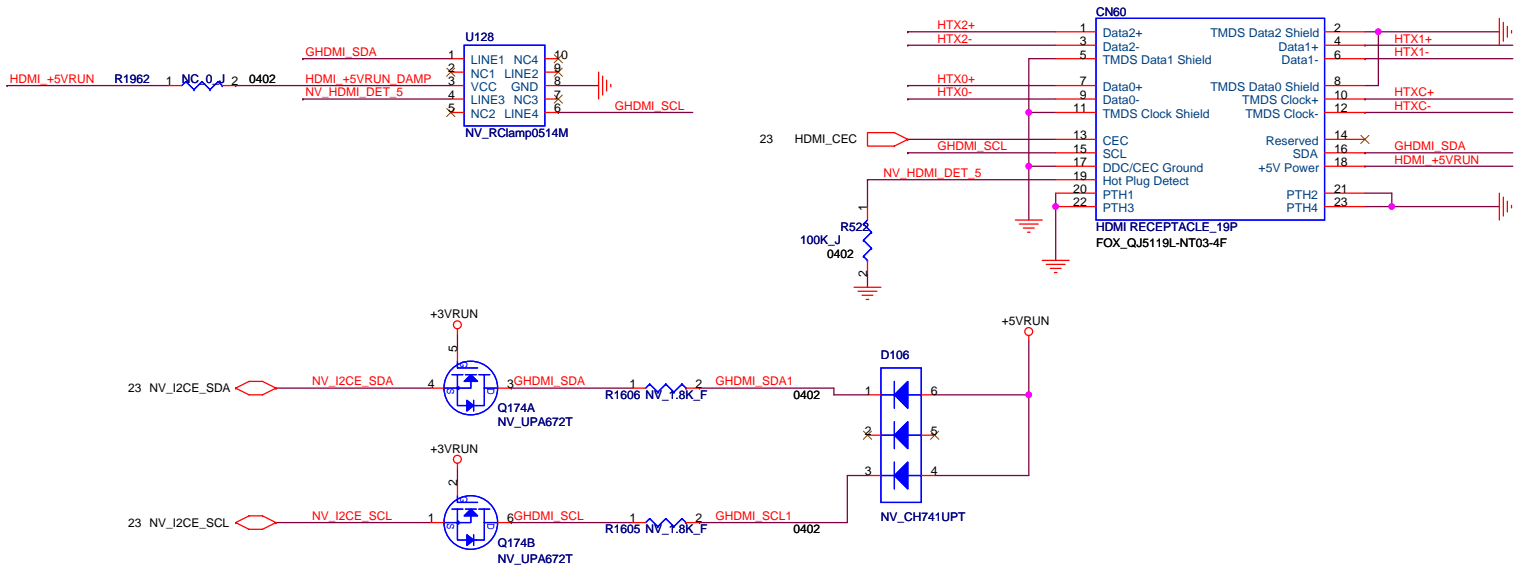


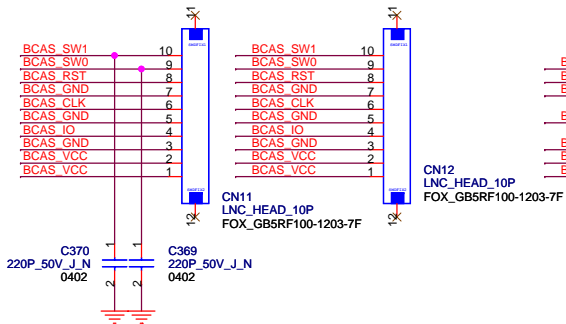
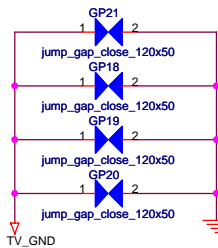
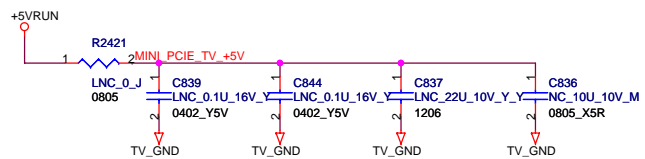
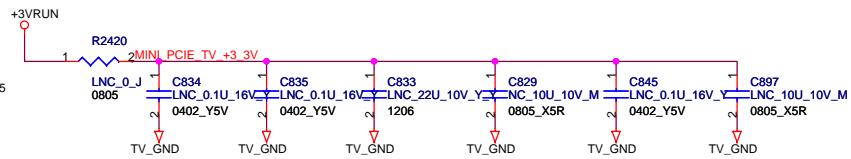
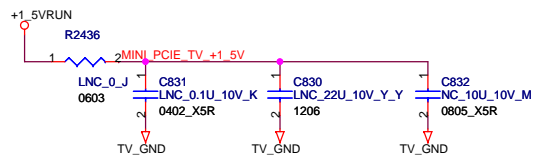
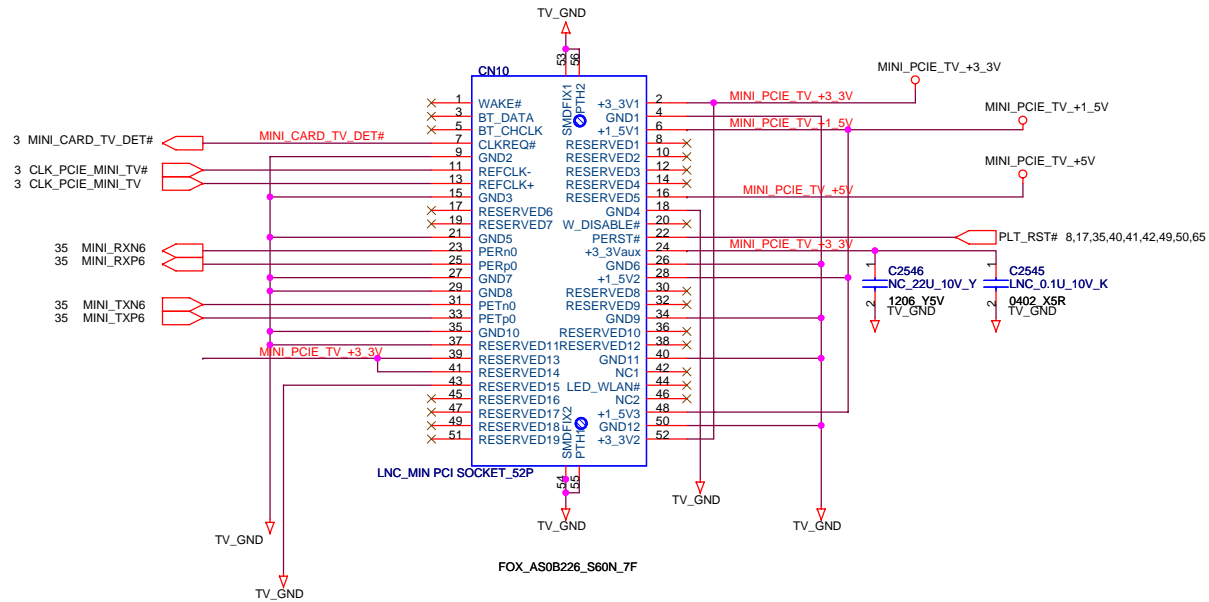
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Title CRT		
Size A3	Document Number M780(MBX-194)	Rev 0.1
Date: Thursday, June 26, 2008	Sheet 31	of 79



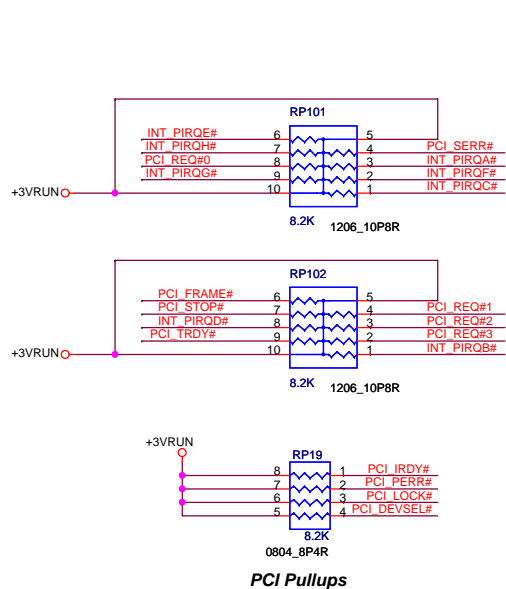
Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

HDMI CONNECTOR

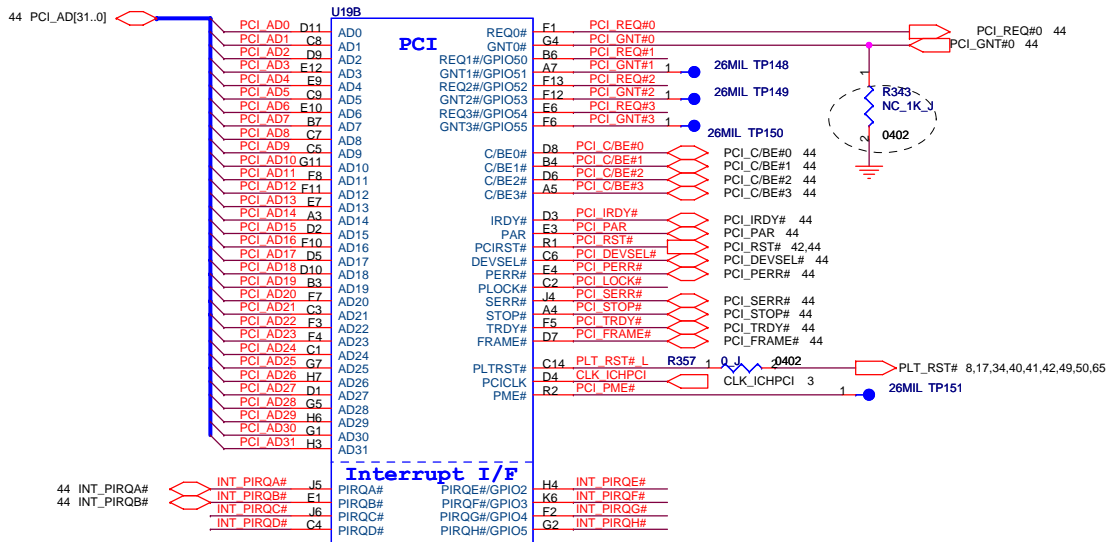




BCAS_SW1	1	TP141	tpc40t_50
BCAS_SW0	1	TP142	tpc40t_50
BCAS_RST	1	TP143	tpc40t_50
BCAS_CLK	1	TP144	tpc40t_50
BCAS_IO	1	TP145	tpc40t_50
BCAS_GND	1	TP146	tpc40t_50
BCAS_VCC	1	TP147	tpc40t_50

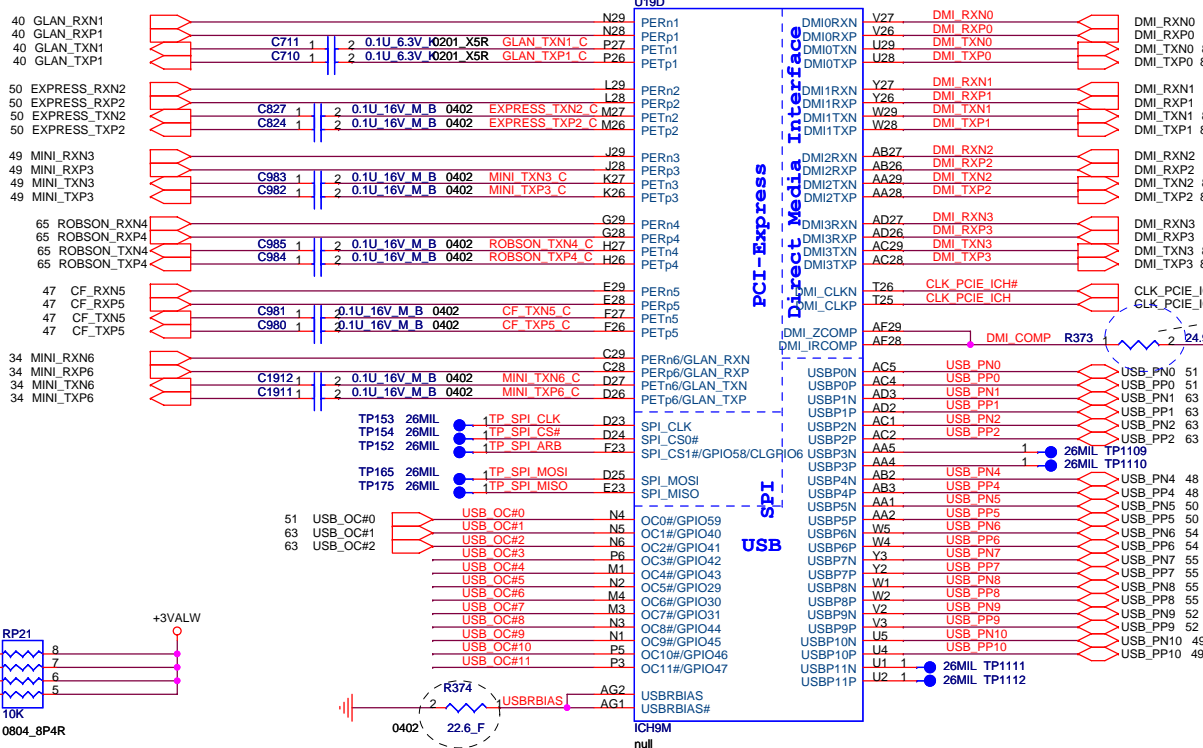


PCI Pullups



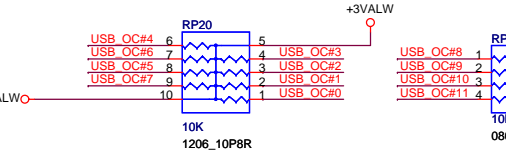
Strap for Boot-BIOS

	GNT0#	SPI_CS1#
LPC(Default)	H1	H1
PCI	H1	LOW
SPI	LOW	H1

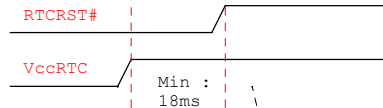


Place within 500 mils of ICH

- USB Port0 -- USB Port0
- USB Port1 -- USB Port1
- USB Port2 -- USB Port2
- USB Port3 -- X
- USB Port4 -- Bluetooth
- USB Port5 -- Express Card
- USB Port6 -- Finger print (BottomBoard)
- USB Port7 -- Camera
- USB Port8 -- OIDE
- USB Port9 -- CIR
- USB Port10 --WIMAX
- USB Port11 -- X

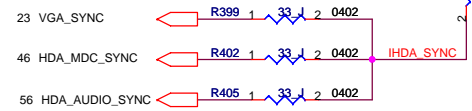
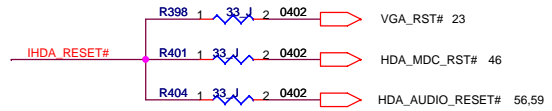
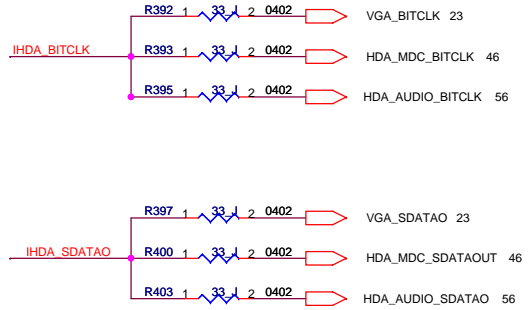
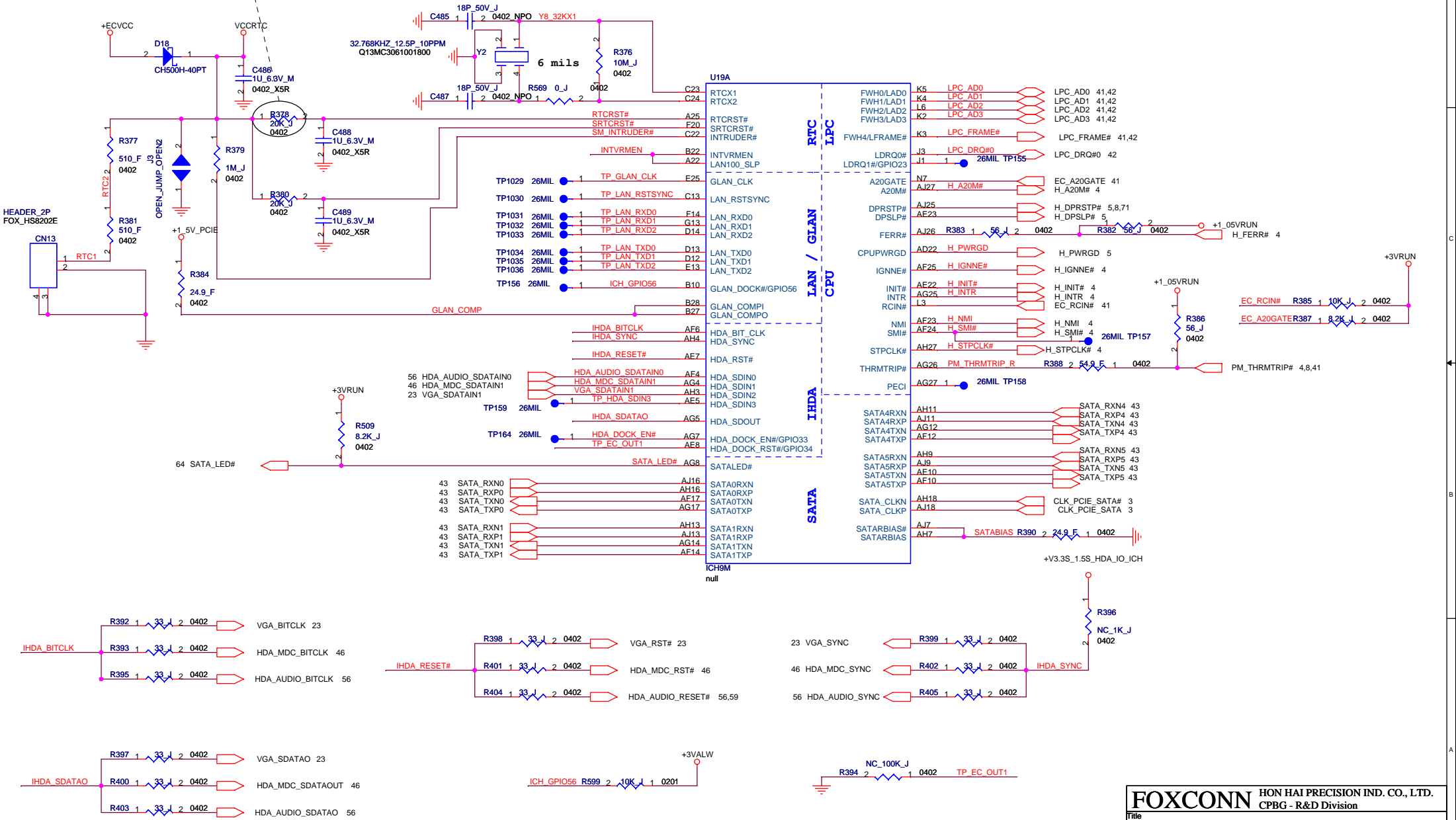
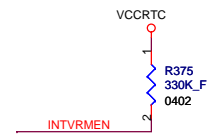


Place within 500 mils of ICH and don't routing next to high speed signals



The traces inside this block should be wider.

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCLL1_5, VccLAN1_05 and VccCLL1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)



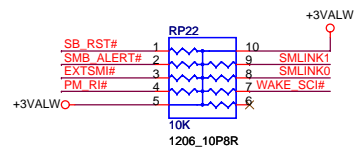
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **ICH9-M (LPC,IDE,SATA) 2/5**

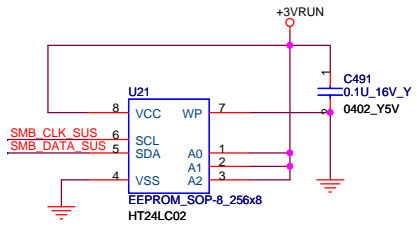
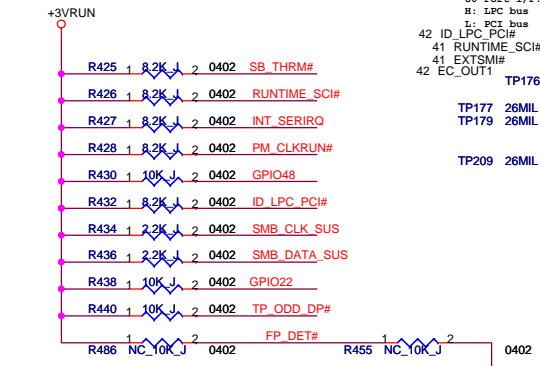
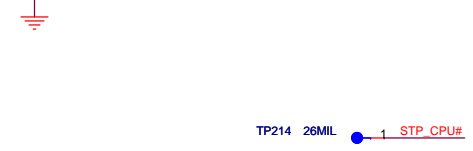
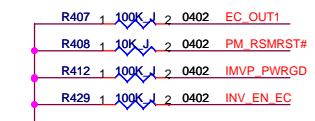
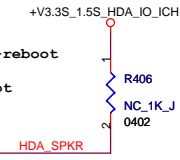
Size: Document Number
A3: **M780(MBX-194)**

Date: Friday, June 13, 2008 Sheet 36 of 79

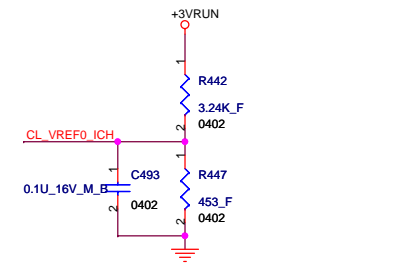
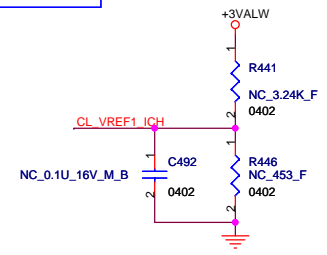
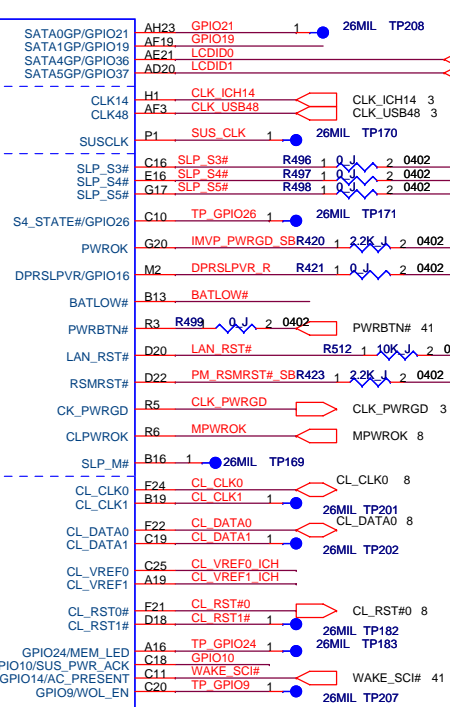
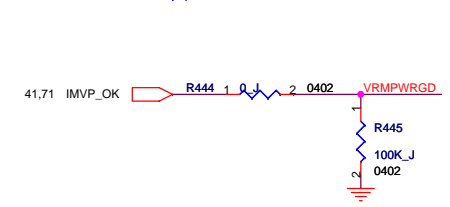
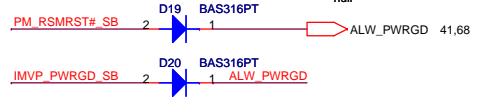
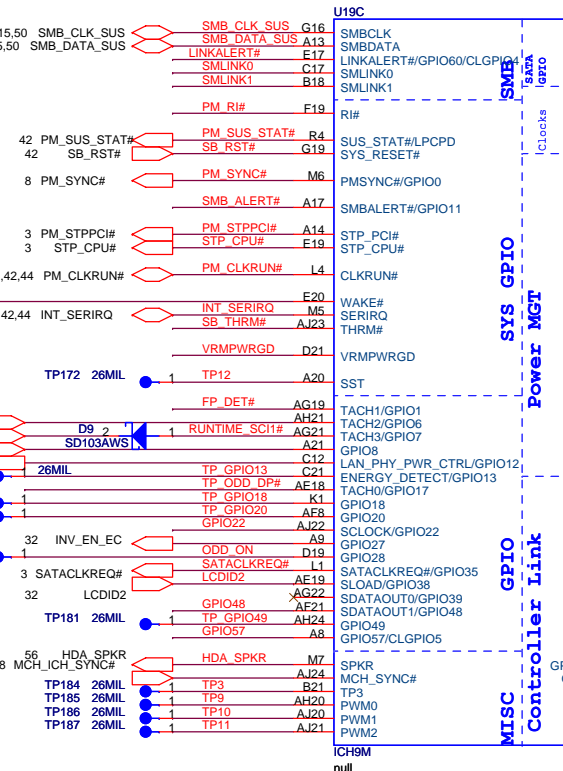
Rev: **0.1**



Stuff for No-reboot
Low=Default
High=No-reboot



SMBus Address: AEH

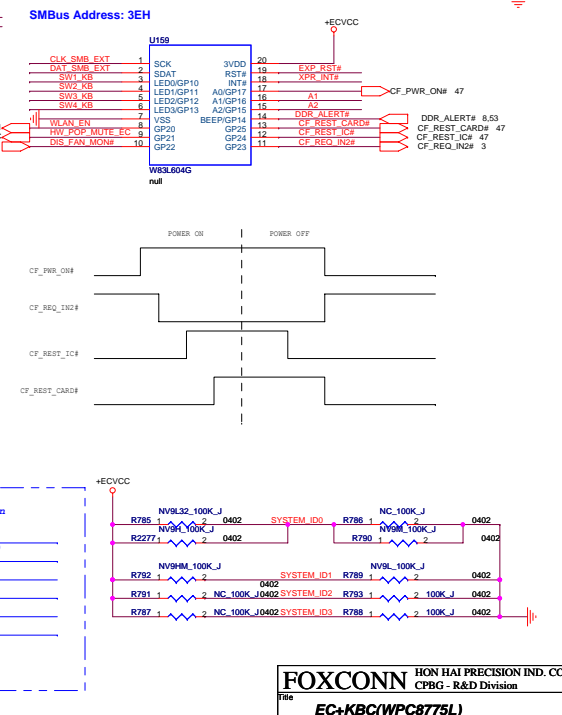
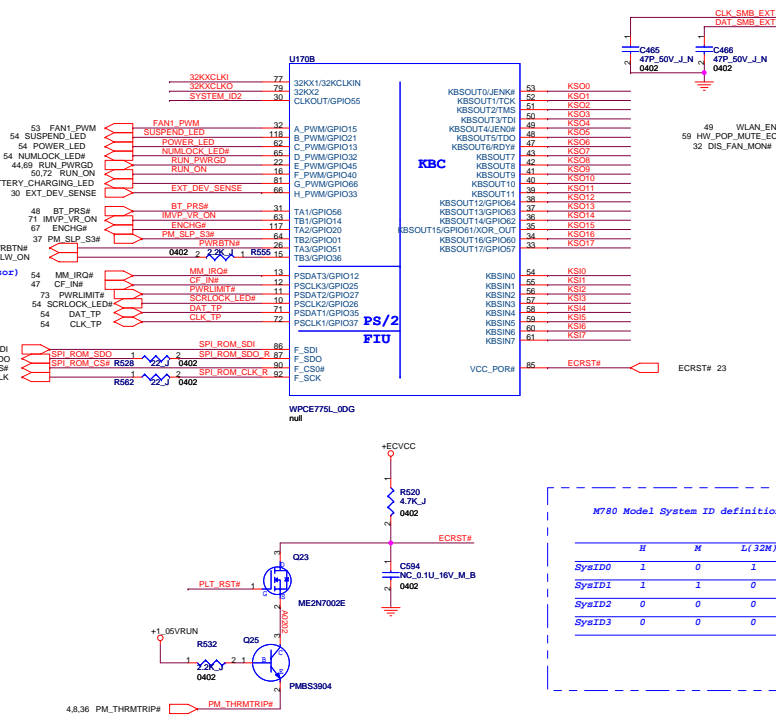
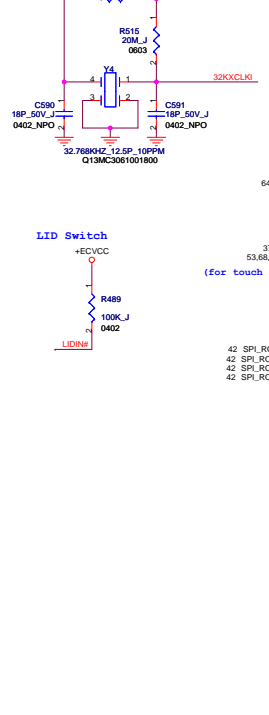
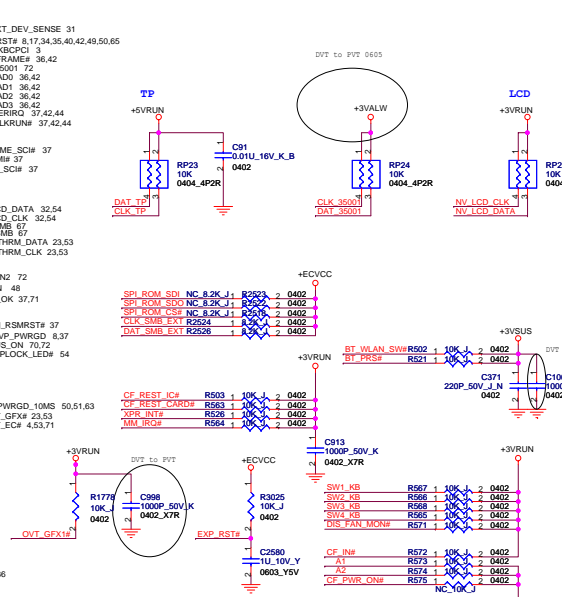
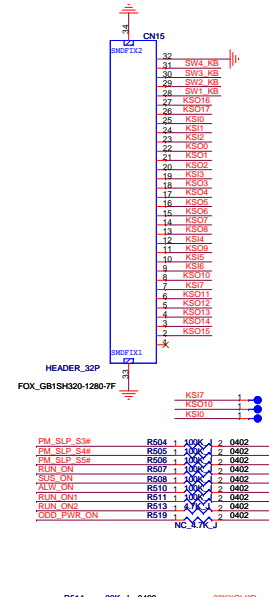
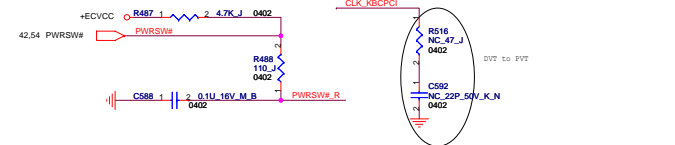
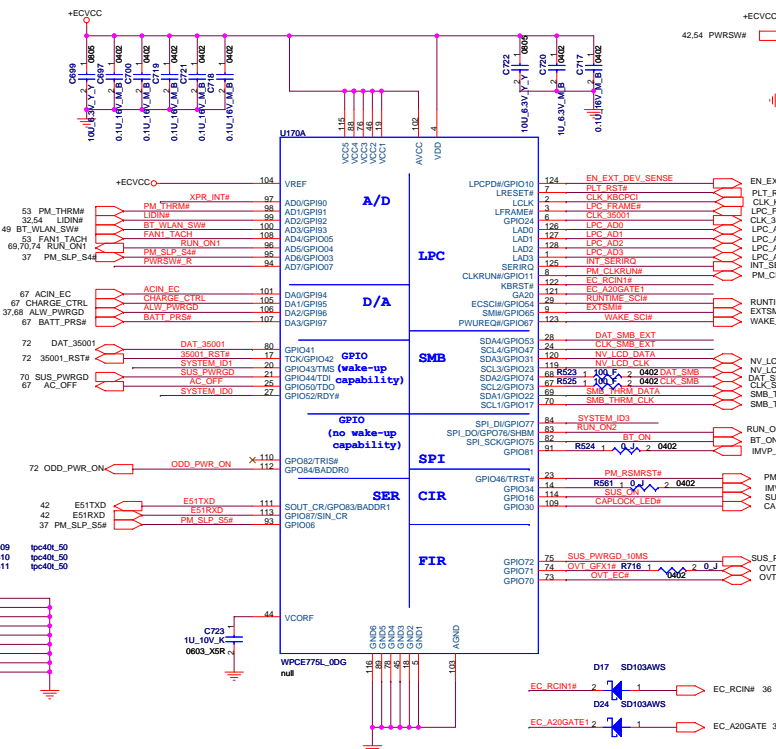
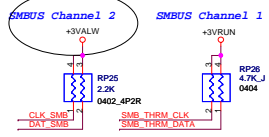


Change to 0402

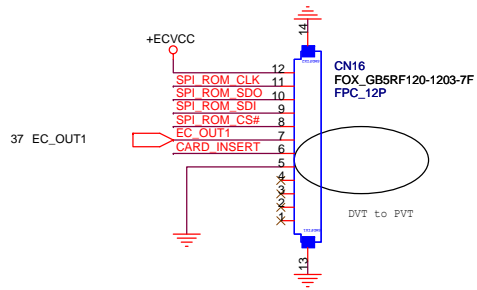
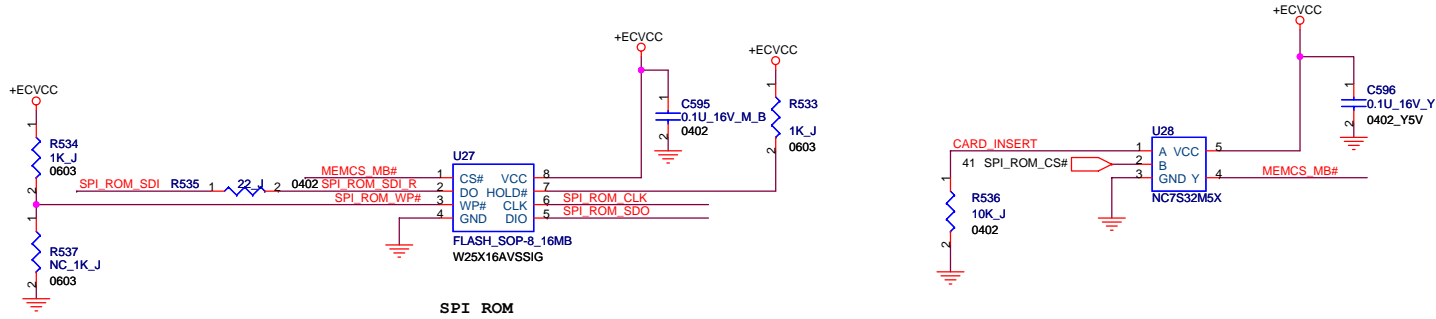
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AA26	VSS6	VSS126	H5
AA27	VSS7	VSS127	J23
AA3	VSS8	VSS128	J26
AA6	VSS9	VSS129	J27
AB1	VSS10	VSS16	AC22
AA23	VSS5	VSS130	K28
AB28	VSS11	VSS131	K29
AB29	VSS12	VSS132	L13
AB4	VSS13	VSS133	L15
AB5	VSS14	VSS134	L2
AC17	VSS15	VSS135	L26
AC26	VSS17	VSS136	L27
AC27	VSS18	VSS137	L5
AC3	VSS19	VSS138	L7
AD1	VSS20	VSS139	M12
AD10	VSS21	VSS140	M13
AD12	VSS22	VSS141	M14
AD13	VSS23	VSS142	M15
AD14	VSS24	VSS143	M16
AD17	VSS25	VSS144	M17
AD18	VSS26	VSS145	M23
AD21	VSS27	VSS146	M28
AD28	VSS29	VSS147	M29
AD29	VSS30	VSS148	N11
AD4	VSS31	VSS149	N12
AD5	VSS32	VSS150	N13
AD6	VSS33	VSS151	N14
AD7	VSS34	VSS152	N15
AD9	VSS35	VSS153	N16
AE12	VSS36	VSS154	N17
AE13	VSS37	VSS155	N18
AE14	VSS38	VSS156	N26
AE16	VSS39	VSS157	N27
AE17	VSS40	VSS158	P12
AE2	VSS41	VSS159	P13
AE20	VSS42	VSS160	P14
AE24	VSS43	VSS161	P15
AE3	VSS44	VSS162	P16
AE4	VSS45	VSS163	P17
AE6	VSS46	VSS164	P2
AE9	VSS47	VSS165	P23
AF13	VSS48	VSS166	P28
AF16	VSS49	VSS167	P29
AF18	VSS50	VSS168	P4
AF22	VSS52	VSS169	P7
AH26	VSS53	VSS170	R11
AE26	VSS54	VSS171	R12
AE27	VSS55	VSS172	R13
AF5	VSS56	VSS173	R14
AF7	VSS57	VSS174	R15
AF9	VSS58	VSS175	R16
AG13	VSS59	VSS176	R17
AG16	VSS60	VSS177	R18
AG18	VSS61	VSS178	R28
AG20	VSS62	VSS179	T12
AG23	VSS63	VSS180	T13
AG3	VSS64	VSS181	T14
AG6	VSS65	VSS182	T15
AG9	VSS66	VSS183	T16
AH12	VSS67	VSS184	T17
AH14	VSS68	VSS185	T23
AH17	VSS70	VSS186	B26
AH19	VSS71	VSS187	U12
AH2	VSS72	VSS188	U13
AH22	VSS73	VSS189	U14
AH25	VSS74	VSS190	U15
AH28	VSS75	VSS191	U16
AH5	VSS76	VSS192	U17
AH8	VSS78	VSS193	AD23
AJ12	VSS80	VSS194	U26
AJ14	VSS82	VSS195	U27
AJ17	VSS83	VSS196	U3
AJ8	VSS84	VSS197	V1
B11	VSS88	VSS198	V13
B14	VSS90	VSS199	V15
B17	VSS91	VSS200	V23
B2	VSS92	VSS201	V28
B20	VSS93	VSS202	V29
B23	VSS94	VSS203	V4
B5	VSS95	VSS204	V5
B8	VSS98	VSS205	W26
C26	VSS100	VSS206	W27
C27	VSS101	VSS207	W3
E11	VSS102	VSS208	Y1
E14	VSS103	VSS209	Y28
E18	VSS104	VSS210	Y29
E2	VSS105	VSS211	Y4
E21	VSS106	VSS212	Y5
E24	VSS107	VSS213	AG28
E5	VSS108	VSS214	AH6
F8	VSS109	VSS215	AF2
F16	VSS110	VSS216	B25
F28	VSS111	VSS217	
F29	VSS112	VSS218	
G12	VSS113	VSS219	A1
G14	VSS114	VSS220	A2
G18	VSS115	VSS221	A28
G21	VSS116	VSS222	A29
G24	VSS117	VSS223	AH
G26	VSS118	VSS224	AH29
G27	VSS119	VSS225	AJ1
G8	VSS120	VSS226	AJ2
H2	VSS121	VSS227	AJ28
H23	VSS122	VSS228	AJ29
H28	VSS123	VSS229	B1
H29	VSS124	VSS230	B29
	VSS125	VSS231	

ICH9M
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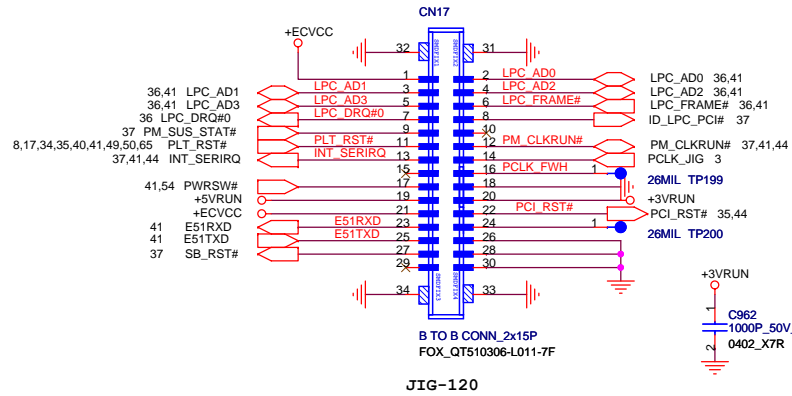
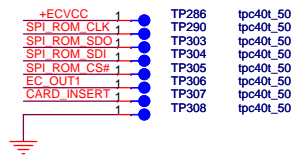
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		CPBG - R&D Division	
Title			
ICH9-M(GND) 5/5			
Size	Document Number		Rev
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Date:	Friday, June 13, 2008	Sheet	39 of 79



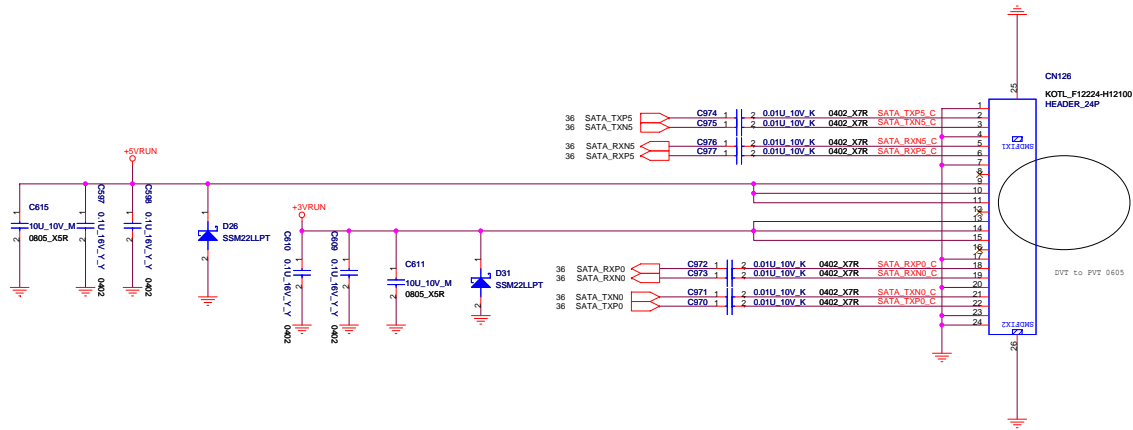
41 SPI_ROM_SDI \rightarrow SPI_ROM_SDI
 41 SPI_ROM_SDO \rightarrow SPI_ROM_SDO
 41 SPI_ROM_CLK \rightarrow SPI_ROM_CLK



EXTERNAL SPI ROM INTERFACE

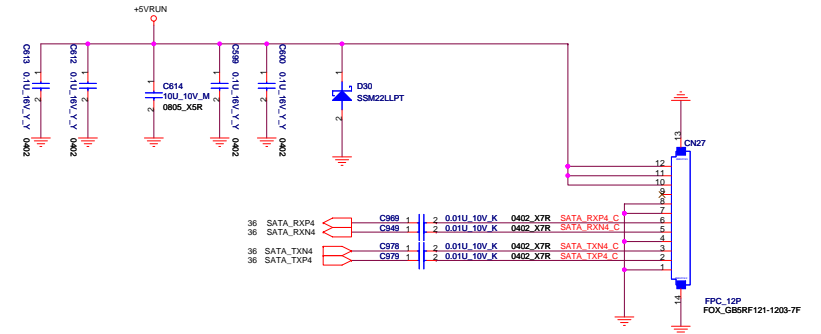


SATA HDD CONN (FPC)

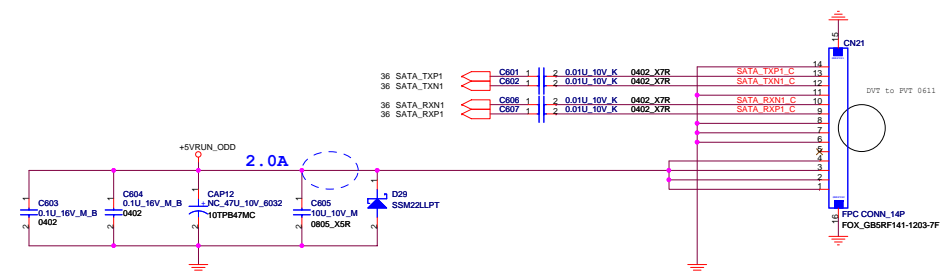


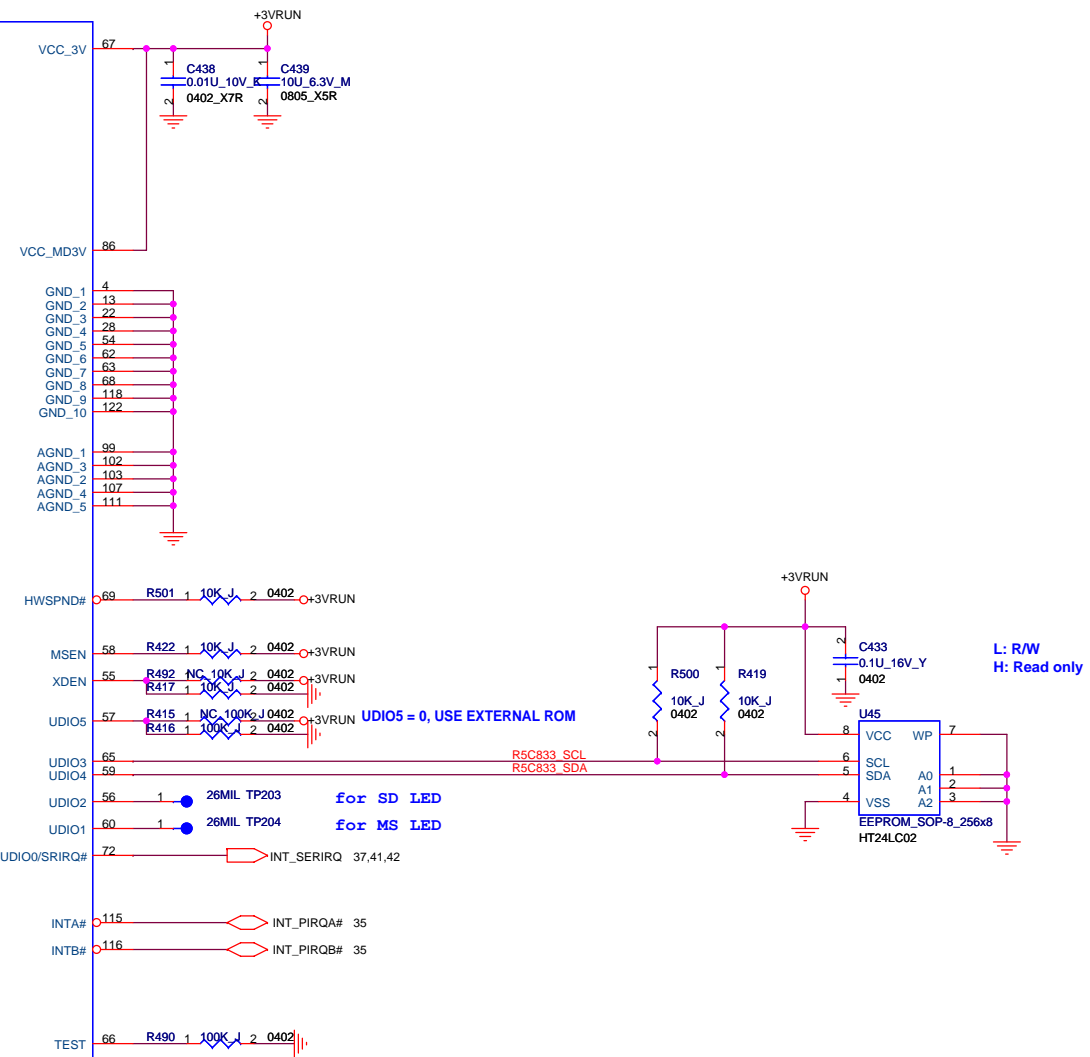
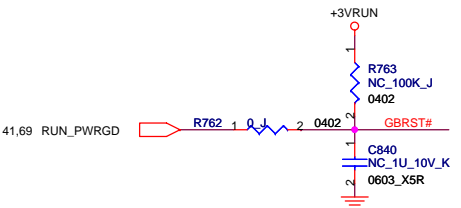
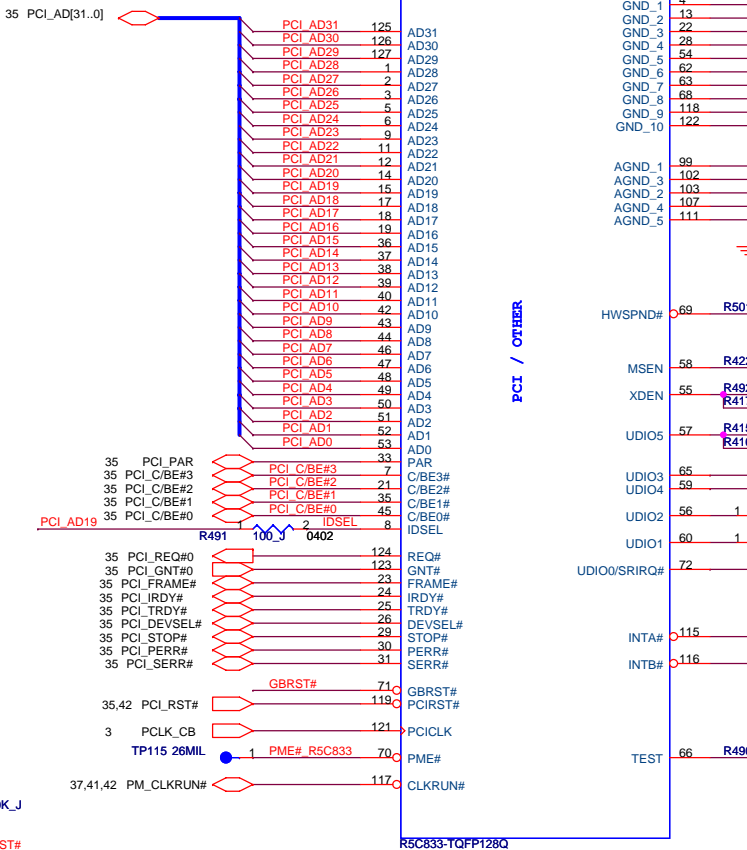
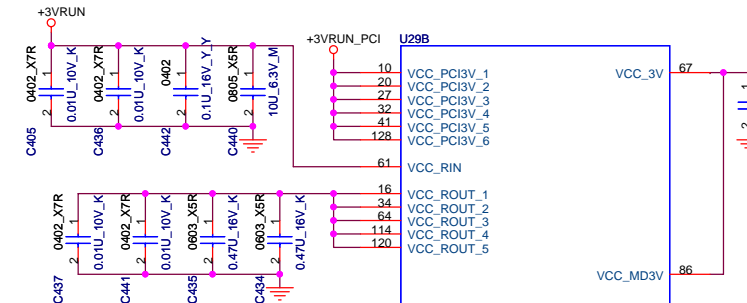
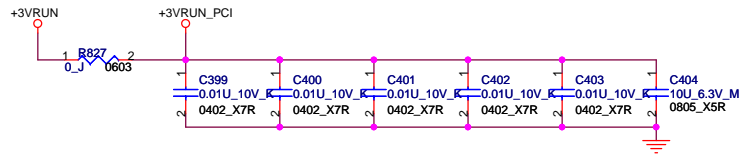
SATA0 : HDD or SSD (just connect to 24 Pin connector)
 SATA1 : ODD (fixed)
 SATA4 : HDD.(fixed for Single HDD connector)
 SATA5 : SSD.(just connect to 24 Pin connector)

SATA HDD CONN1 (FPC)



SATA ODD CONN (FPC)





PCI / OTHER

UDIO5 = 0, USE EXTERNAL ROM

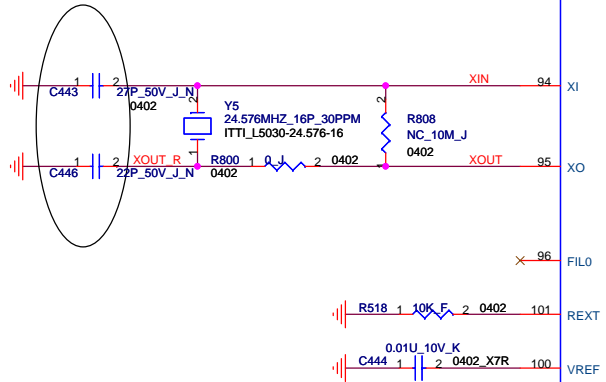
for SD LED

for MS LED

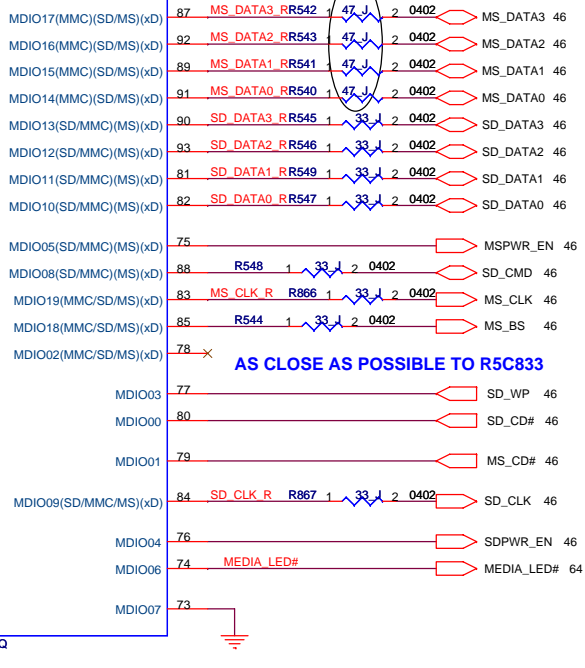
L: R/W
H: Read only

FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title: PCI (PCI BUS)	
Size: A3	Document Number: M780(MBX-194)
Date: Friday, June 13, 2008	Rev: 0.1
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DVT to PVT 0612



IEEE1394/SD

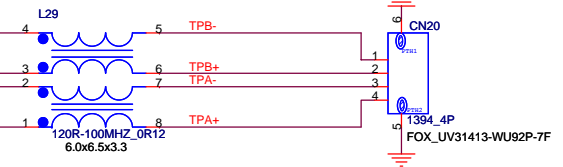


AS CLOSE AS POSSIBLE TO R5C833

204. (Page 45) 07/11/27 change iLink CONN from FOX_UV31413-WR56P-7F to FOX_UV31413-WZ03P-7F.

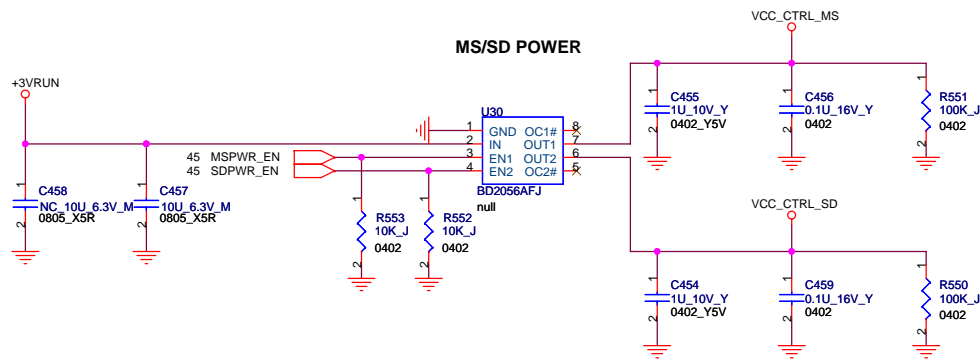
iLink CONN.

118. (Page 30) 07/11/12 Change L29 from 1L-FTR1DB6-5600 to 1L-F0D6560-TE00.

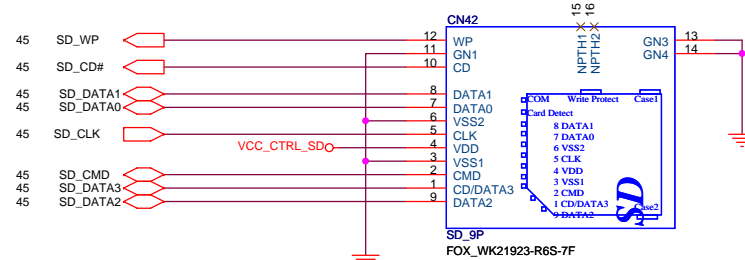


iLink CONN.

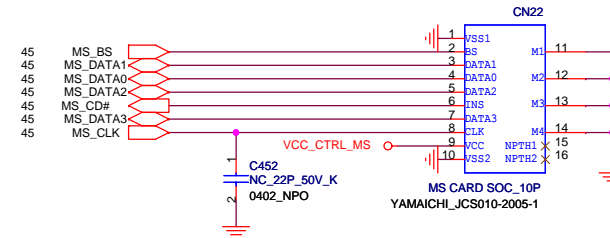
FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title PCI (ILink)	
Size A3	Document Number M780(MBX-194)
Date: Sunday, June 29, 2008	Rev 0.1
Sheet 45	of 79



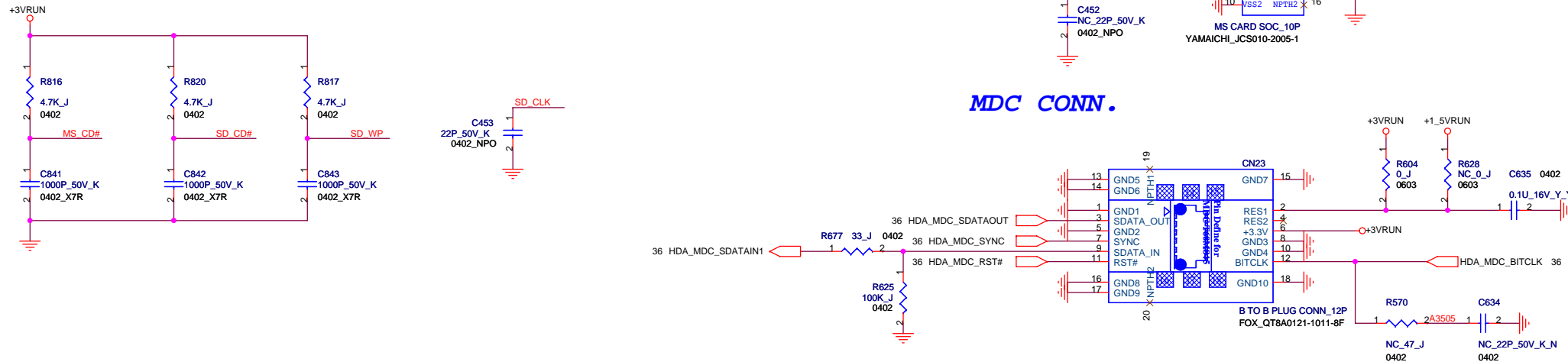
SD CONN.



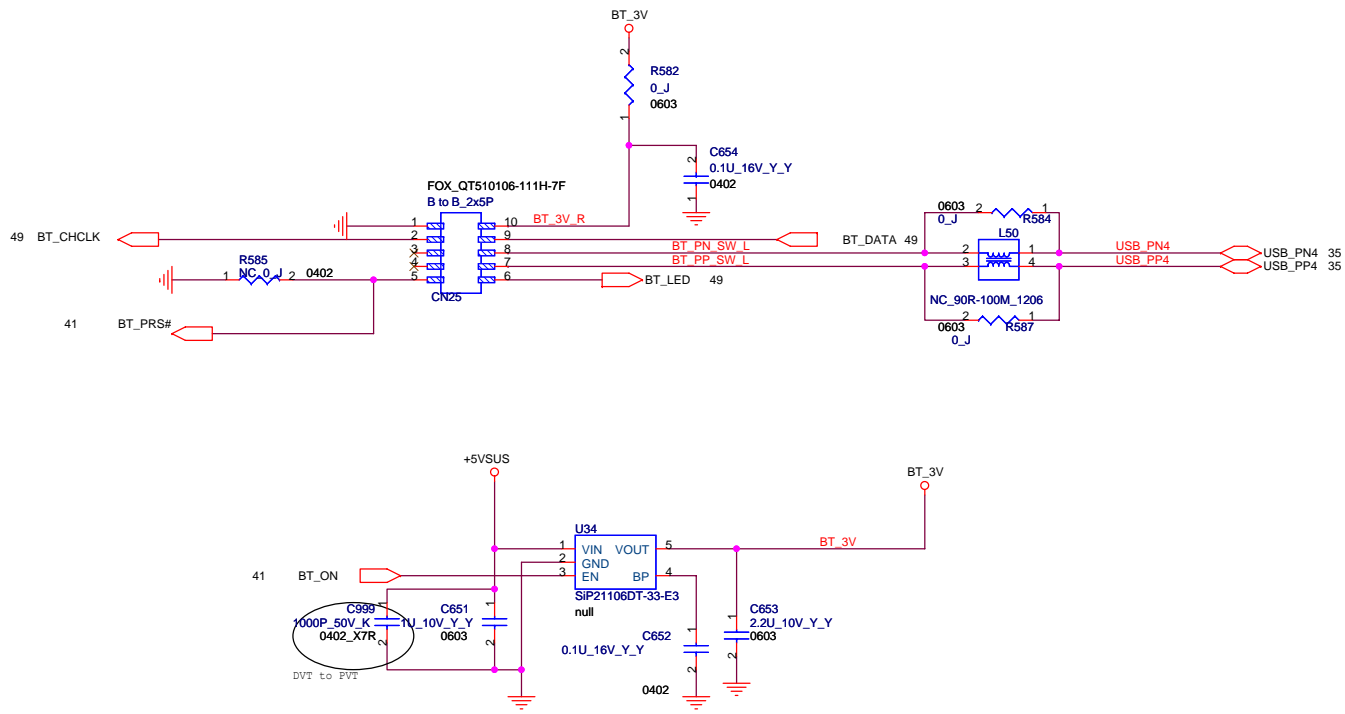
MS STD/DUO CONN.



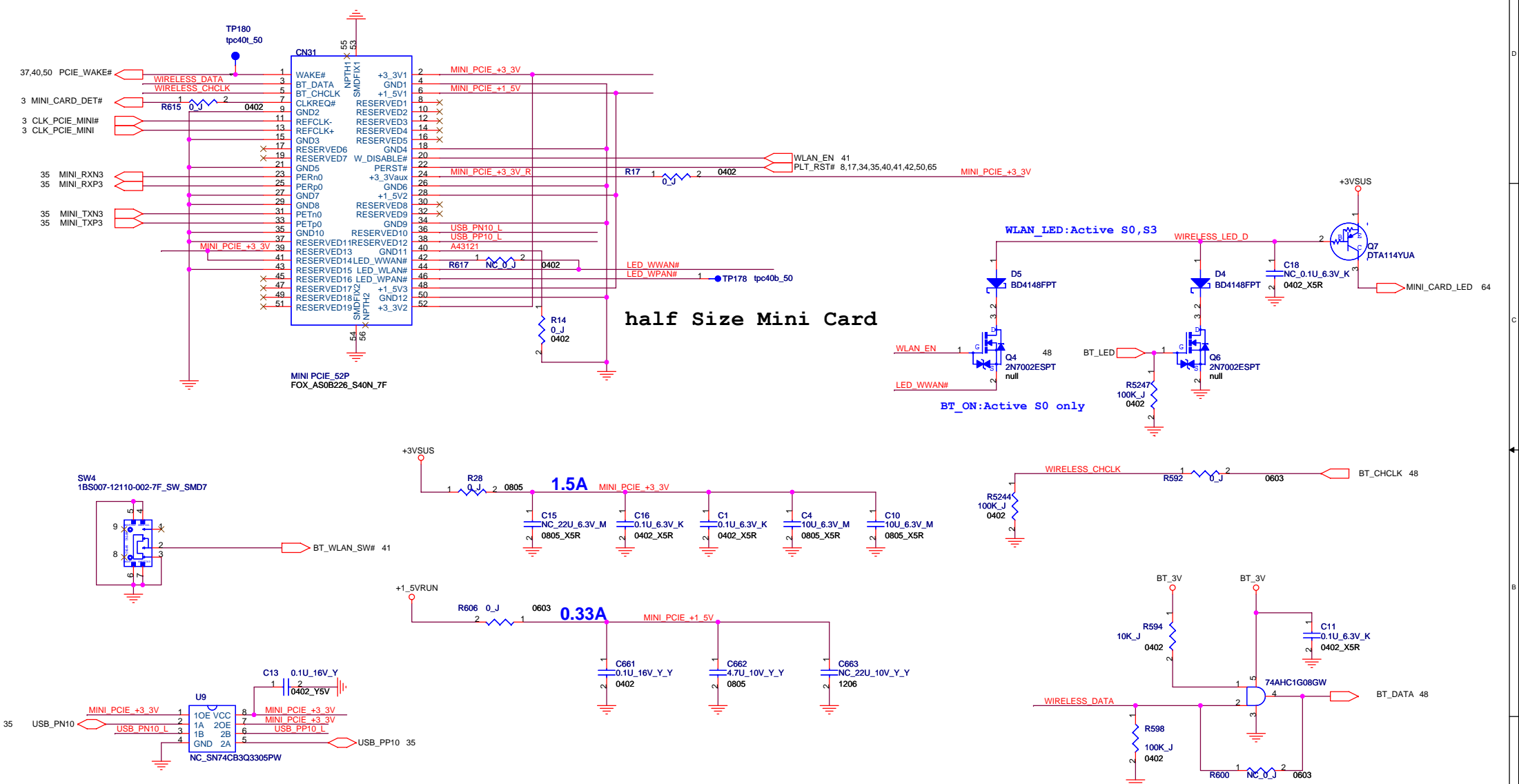
MDC CONN.



Bluetooth connector



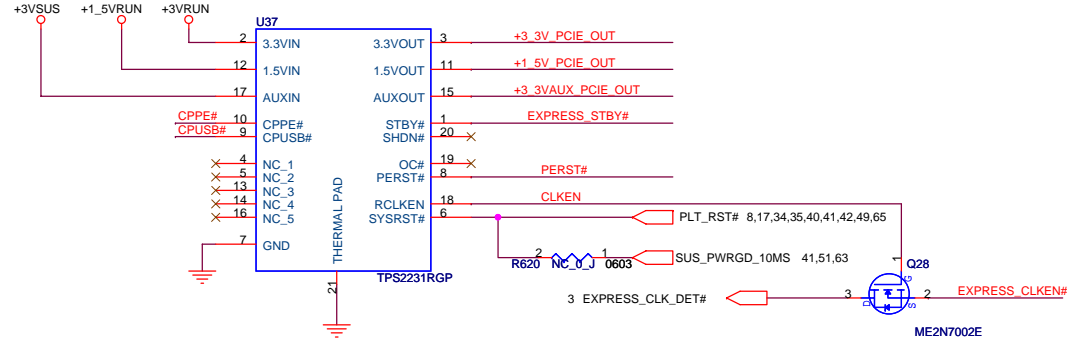
Mini-PCIE Card connector(WLA)



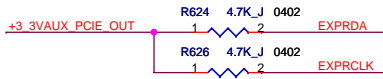
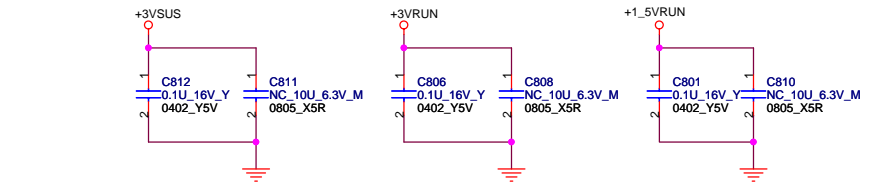
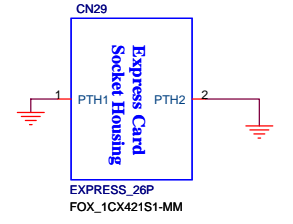
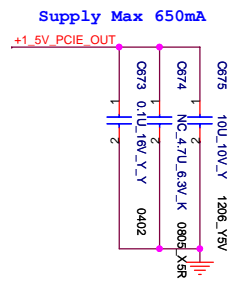
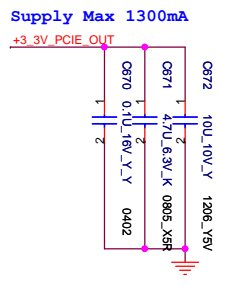
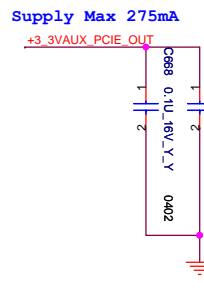
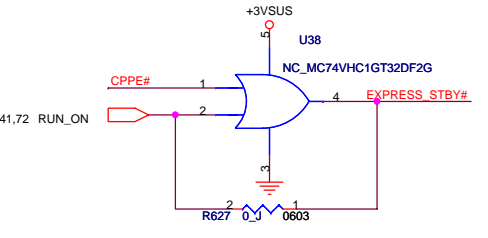
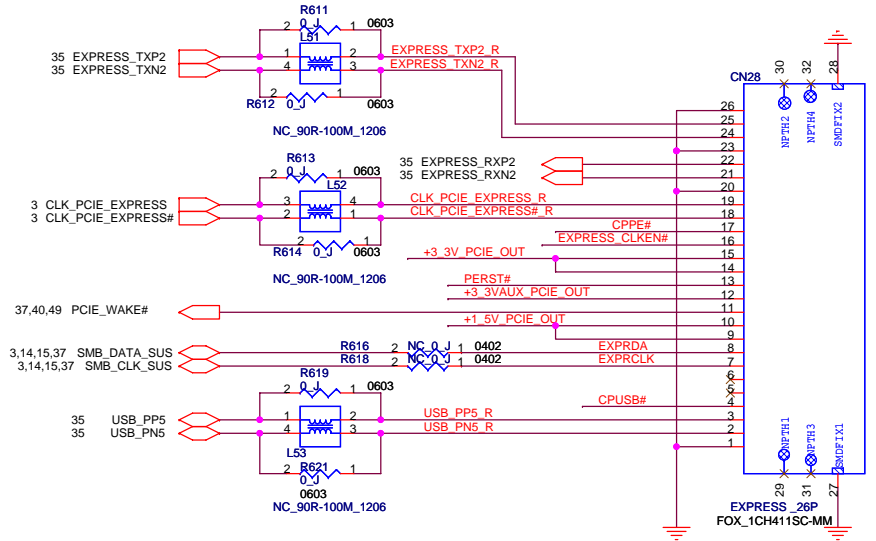
FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title Mini-PCIE Card(WLA)		
Size	Document Number	Rev
A3	M780(MBX-194)	0.1
Date:	Friday, June 13, 2008	Sheet 49 of 79

VOLTAGE INPUTS ⁽¹⁾					LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT			
Off	x	x	x	x	x	Off	Off	Off			OFF
On	x	x	0	x	x	GND	GND	GND			Shutdown
On	x	x	1	x	1	GND	GND	GND			No Card
On	On	On	1	0	0	Off	Off	Off			Standby
On	On	On	1	1	0	On	On	On			Card Inserted

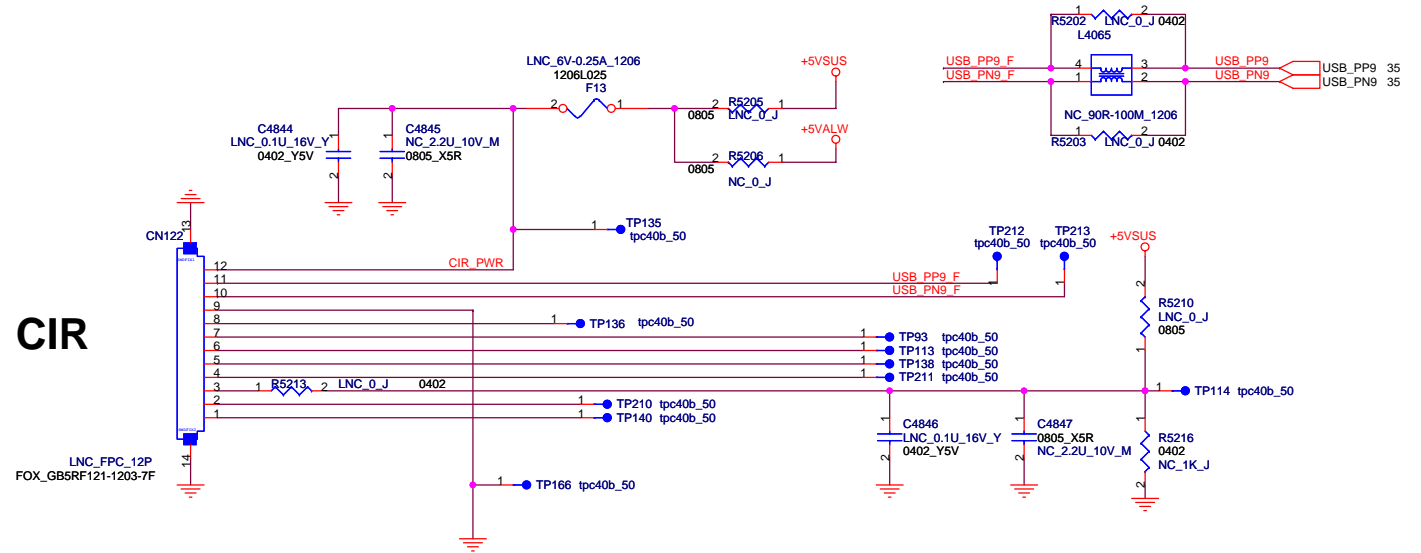
+1_5V=>0.65A
+3_3VAux=>0.275A
+3_3V=>1.3A



EXPRESS Card Slot

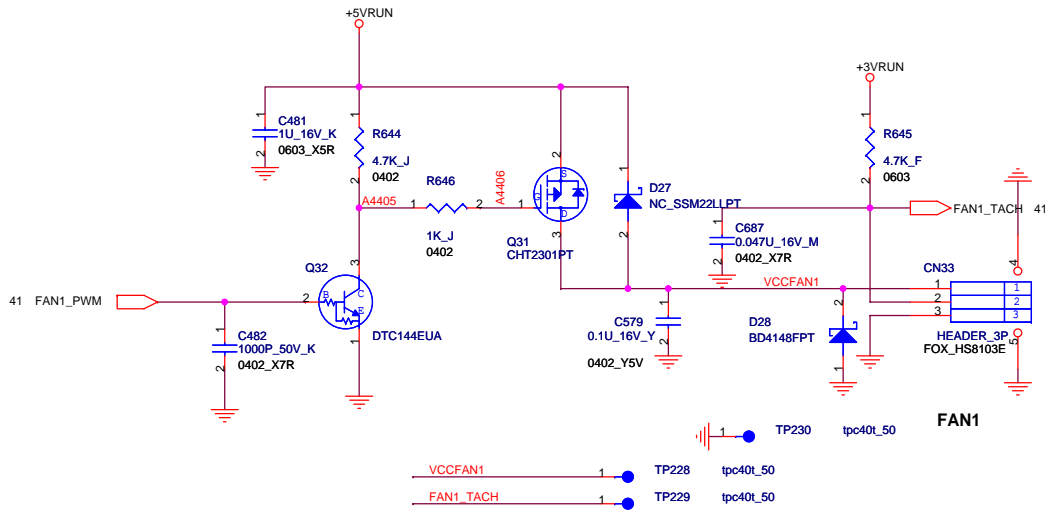


IR Receiver connector

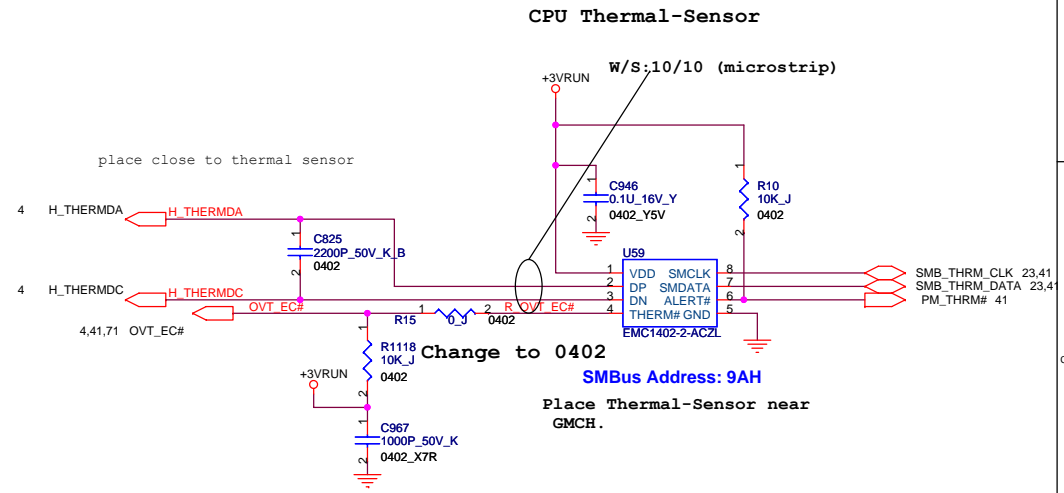


FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
CIR Reciver			
Size	Document Number		Rev
A3	M780(MBX-194)		0.1
Date:	Friday, June 13, 2008		Sheet 52 of 79

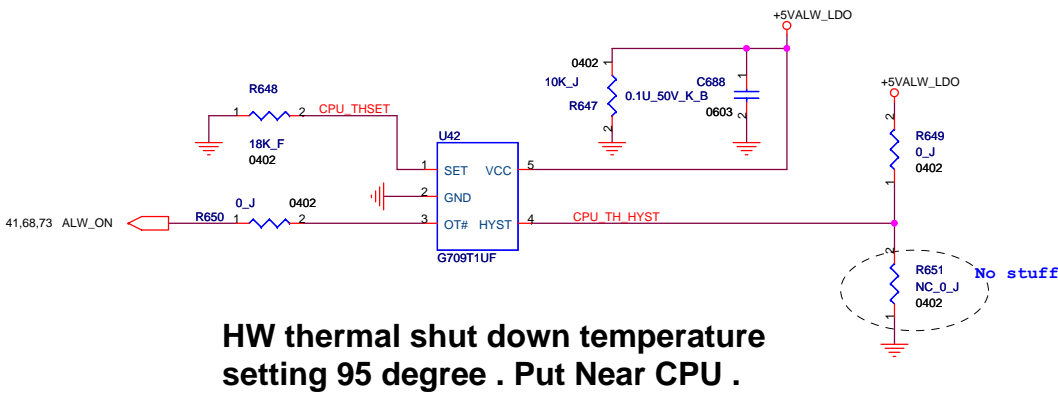
FAN circuit



CPU Thermal-Sensor

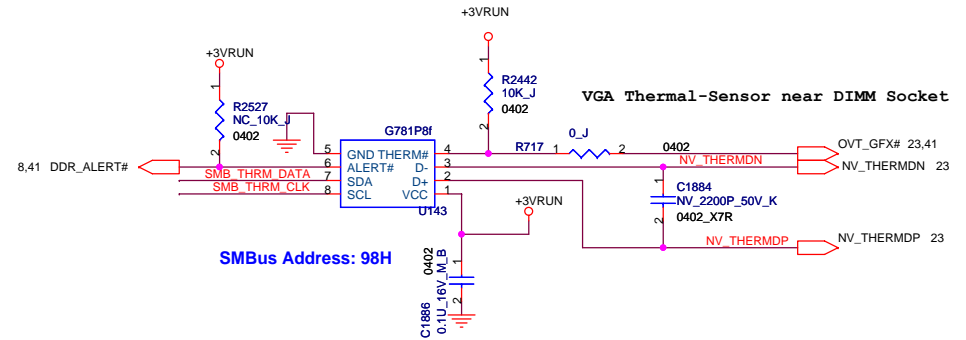


HW THERMAL PROTECTION

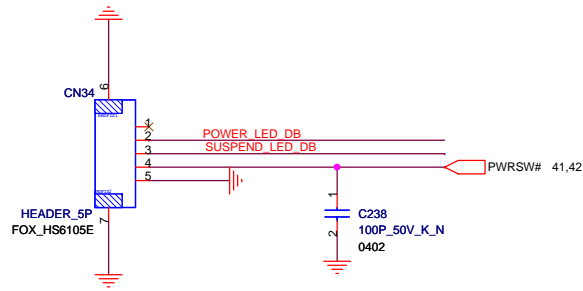


HW thermal shut down temperature setting 95 degree . Put Near CPU .

VGA Thermal-Sensor



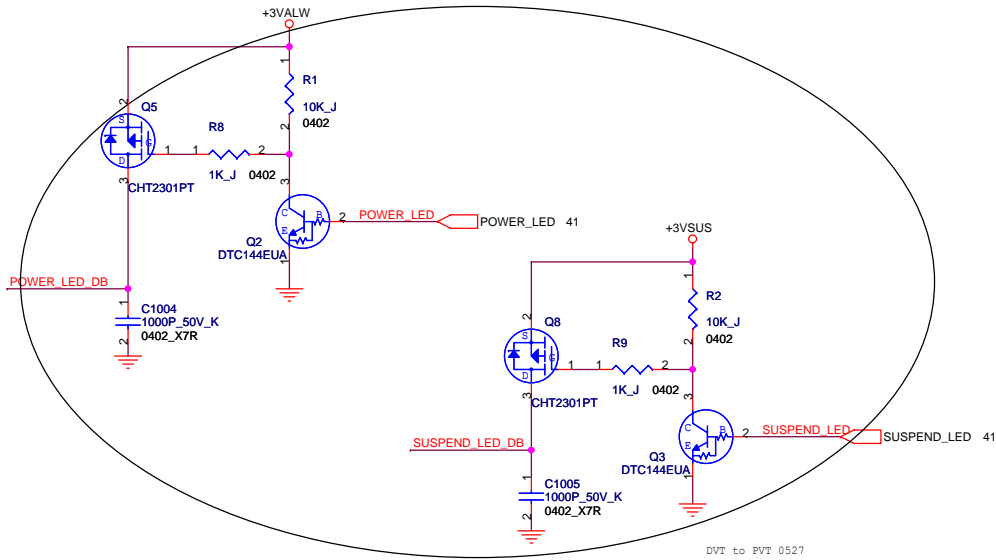
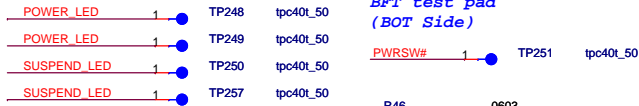
To Power Button Board Connector



BFT test pad (TOP Side)



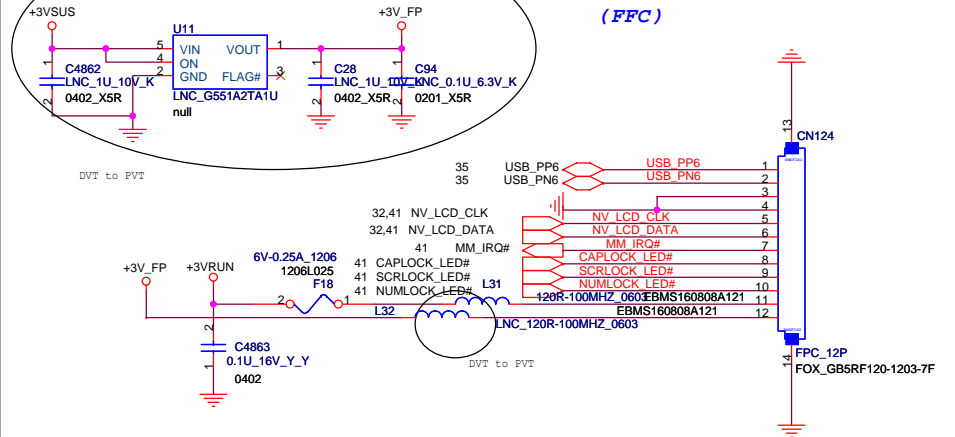
BFT test pad (BOT Side)



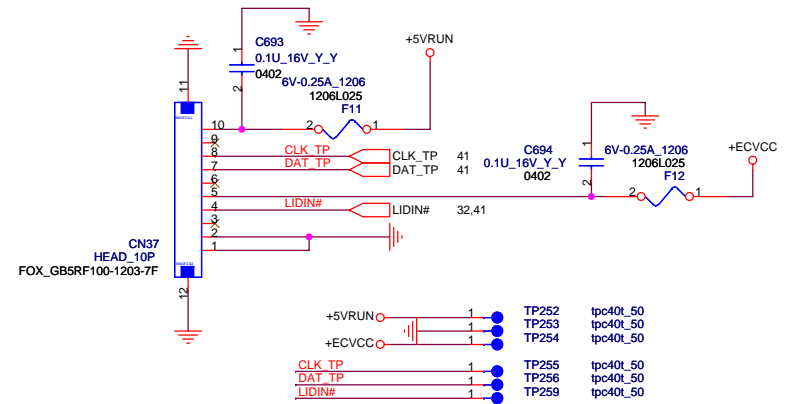
DVT to FVT 0527

To TV Function Board Connector

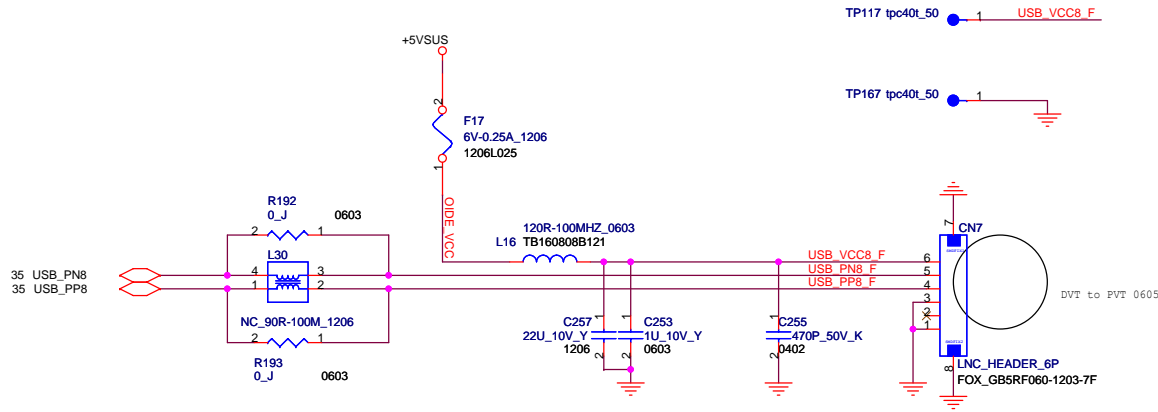
(FFC)



To Touch Pad Board Connector (FFC)

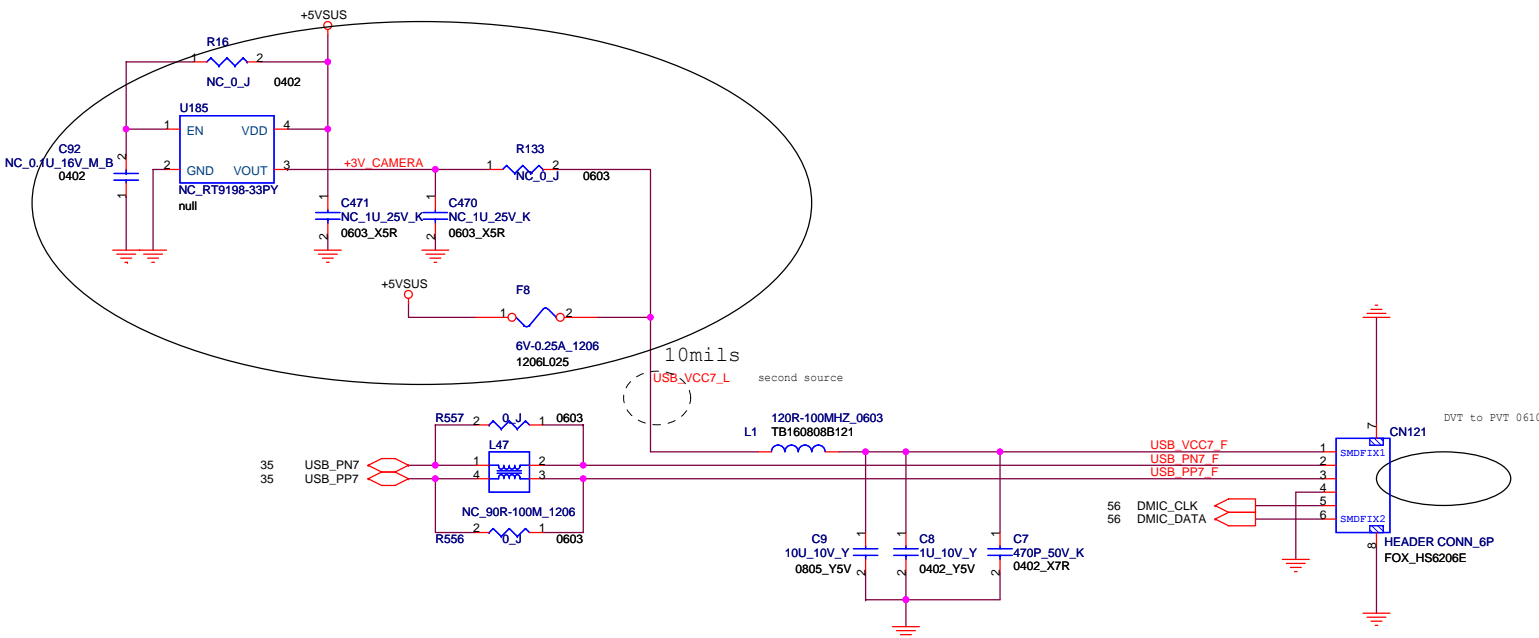


OIDE Connector



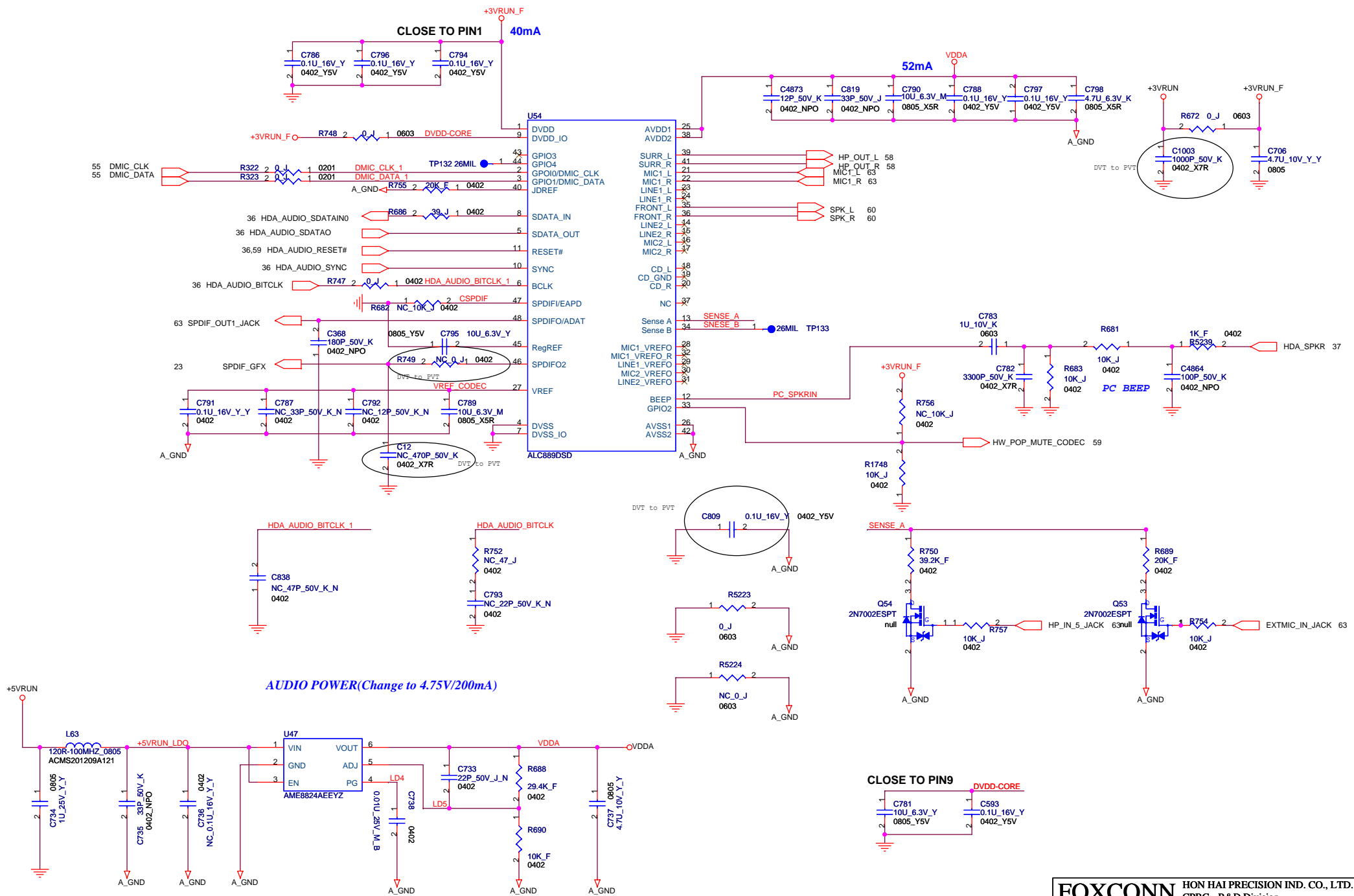
CAMERA +MIC CONN.

DVT to PVT 0611

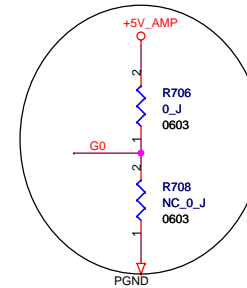
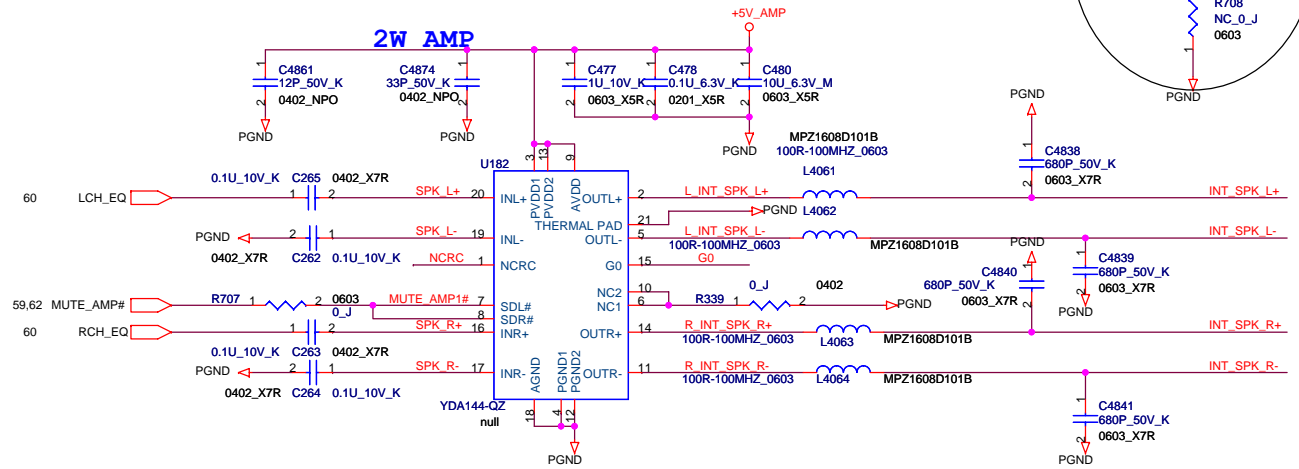


- TP51 tpc40t_50 1 USB_VCC7_F
- TP126 tpc40t_50 1 USB_PN7_F
- TP128 tpc40t_50 1 USB_PP7_F
- TP127 tpc40t_50 1
- TP139 tpc40t_50 1 DMIC_CLK
- TP160 tpc40t_50 1 DMIC_DATA

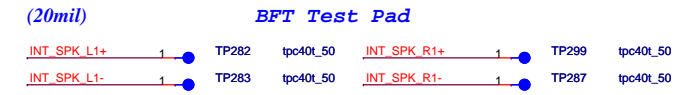
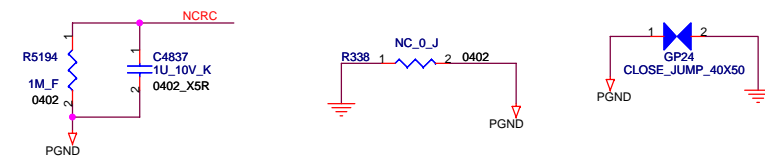
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	OIDE/CAM	
Size	Document Number	Rev
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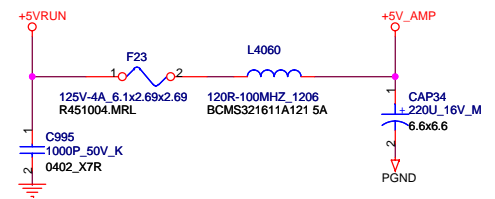
SPEAKER AMP



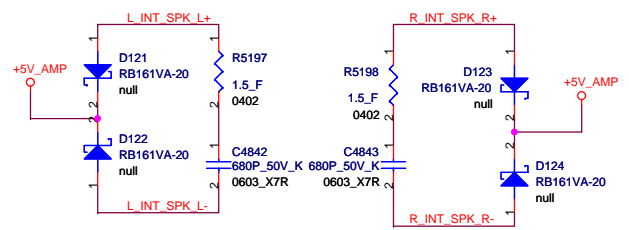
INTERNAL SPEAKER Connector



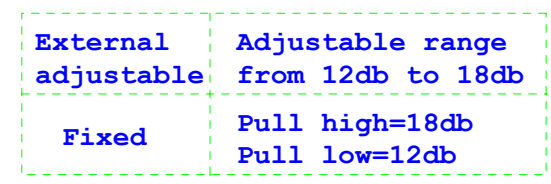
SPEAKER POWER

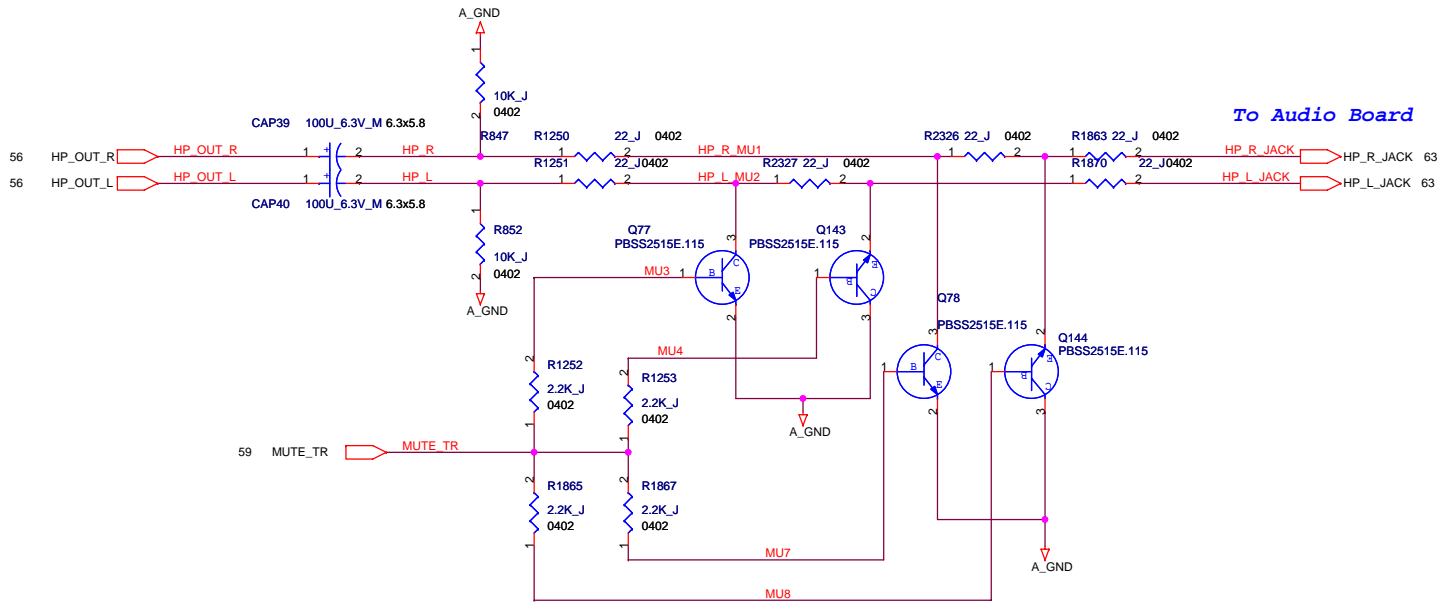


Close to Amp

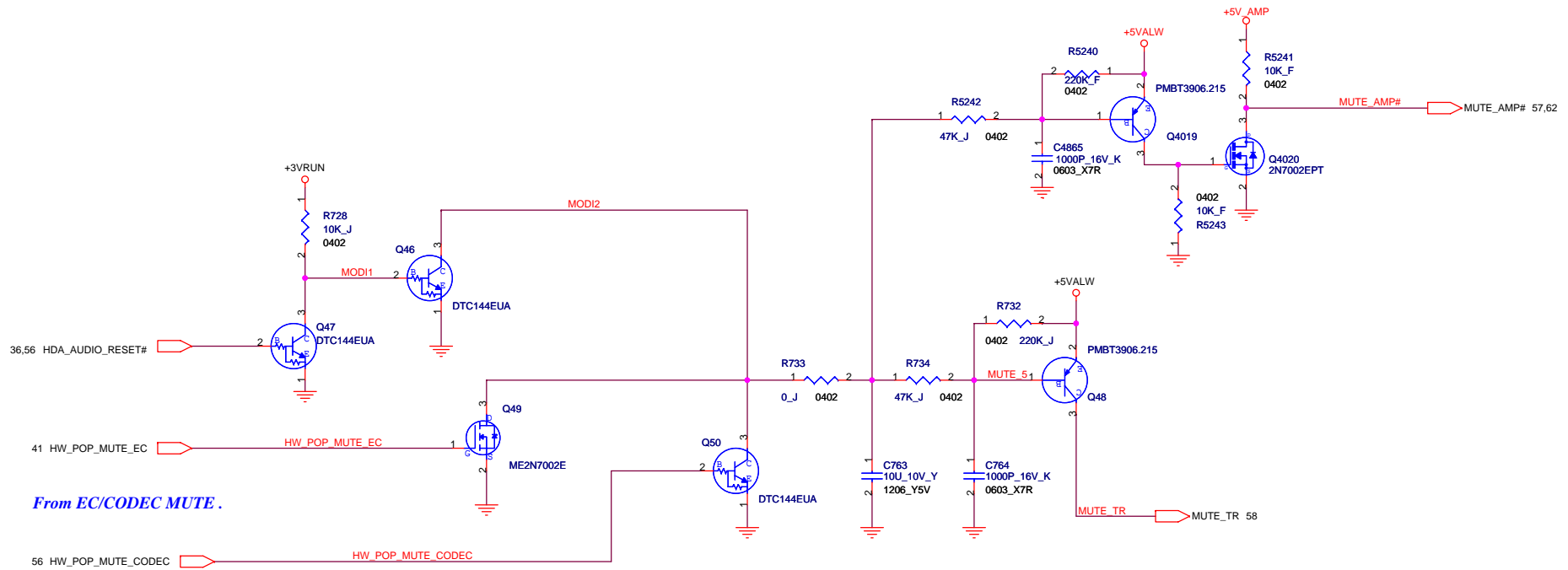


GAIN

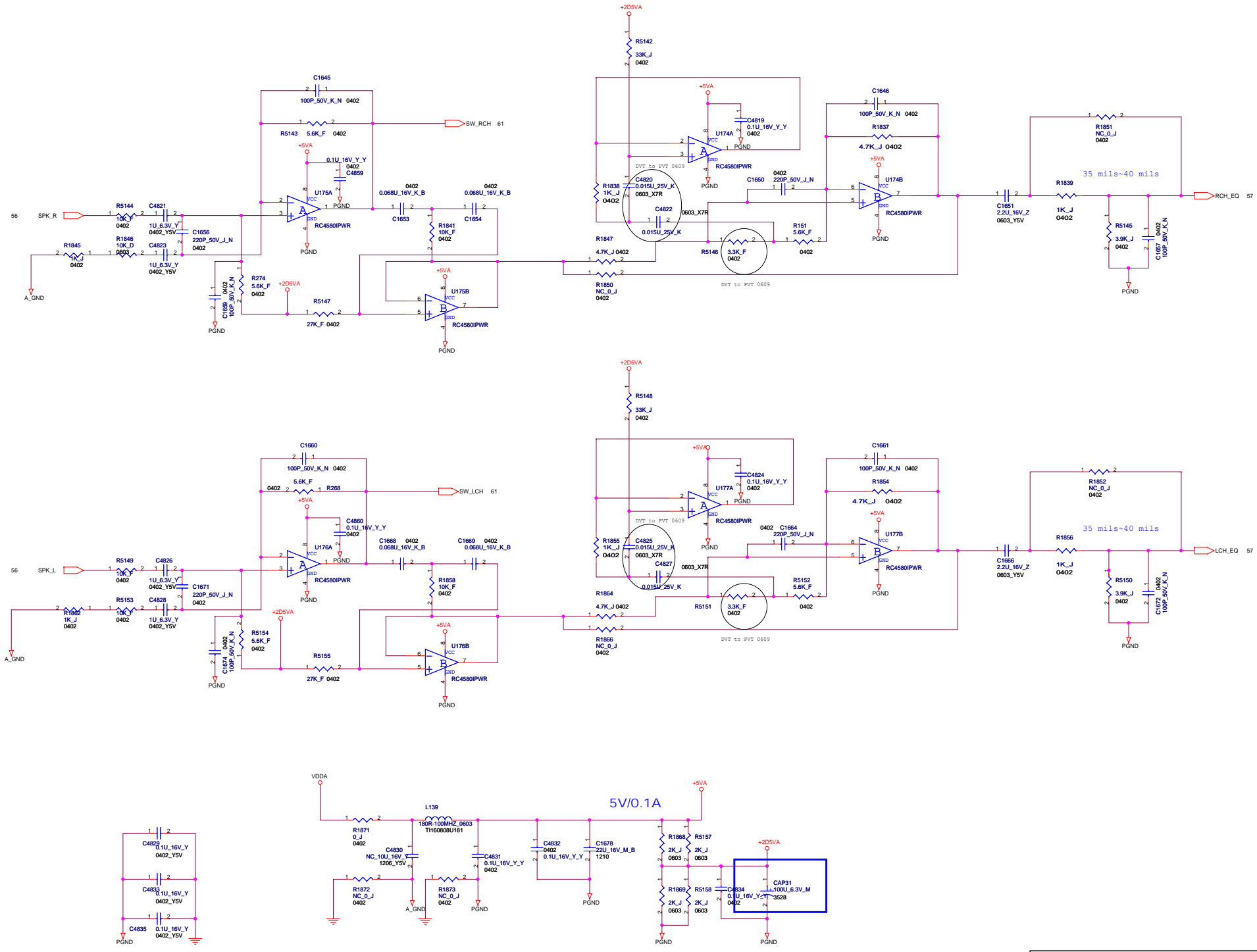




FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
AUDIO (HP)			
Size	Document Number		Rev
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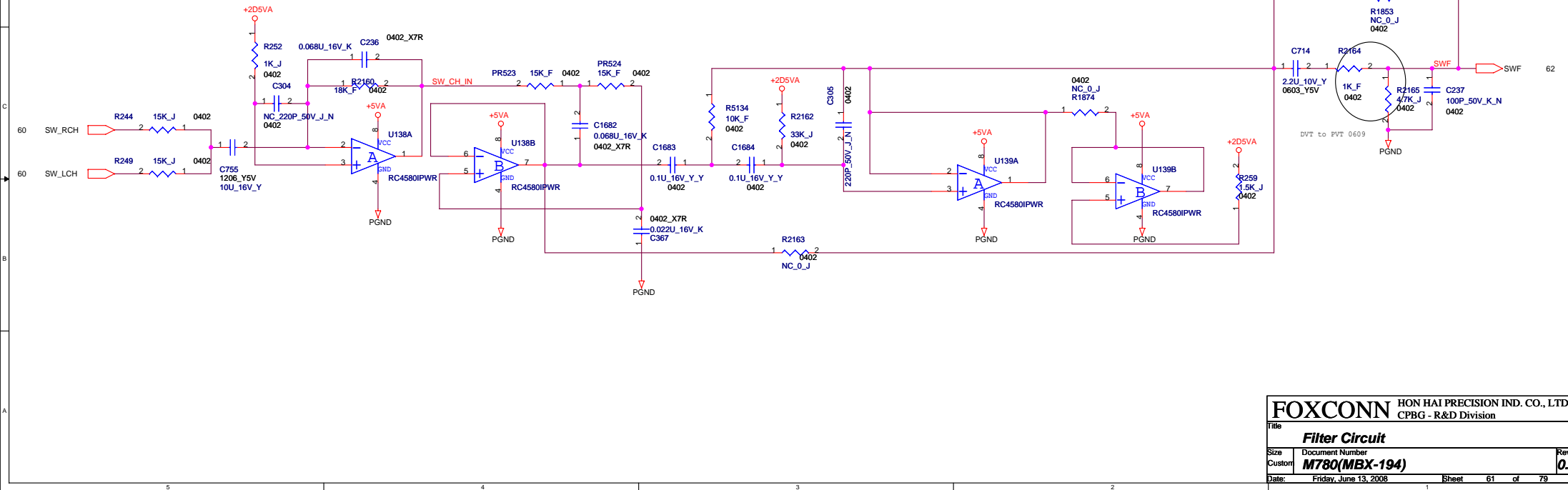


From EC/CODEC MUTE .



Filter Circuit

Vendor recommendation not use for
 1) Input impedance
 As described in the datasheet (P5), match input impedance at IN+ and IN-.
 We are afraid of pop noise on this board.
 Current SWF impedance is too big, so we recommend to reduce SWF output impedance.
 Does R2164, R2165 and C237 Circuit need?

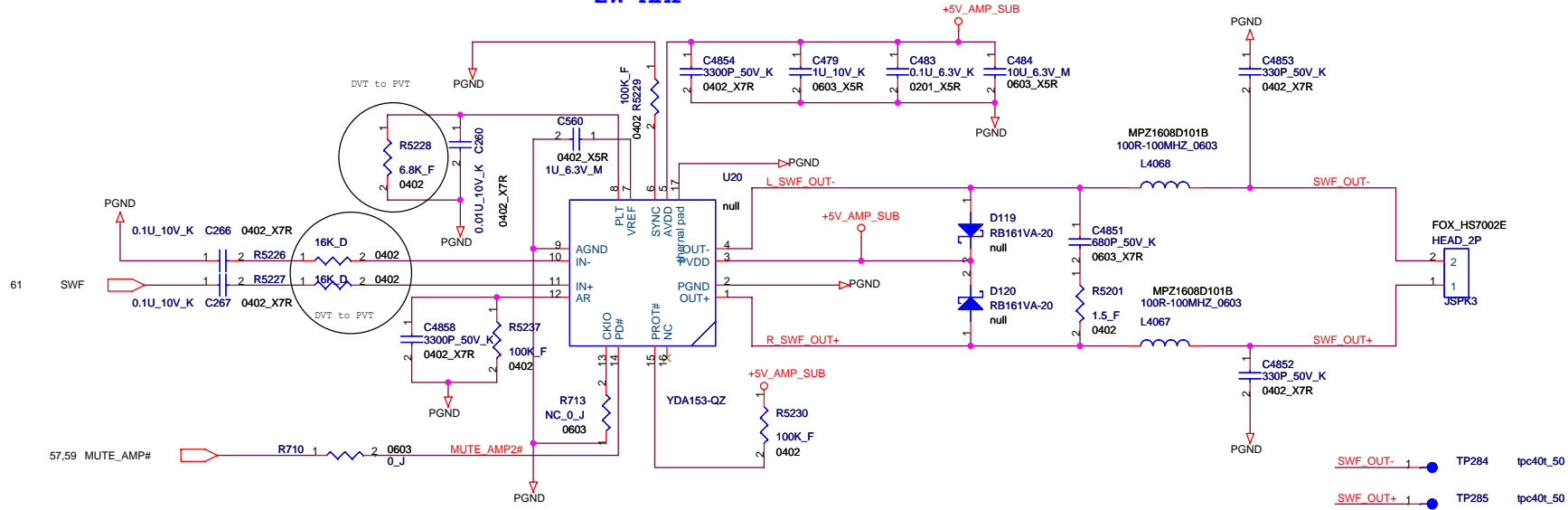


FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title Filter Circuit	
Size Custom	Document Number M780(MBX-194)
Date: Friday, June 13, 2008	Rev 0.1
Sheet 61 of 79	

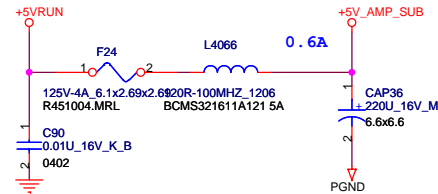
SUB_WOOFER AMP

C479, C484
Locate them close to PVDD pin

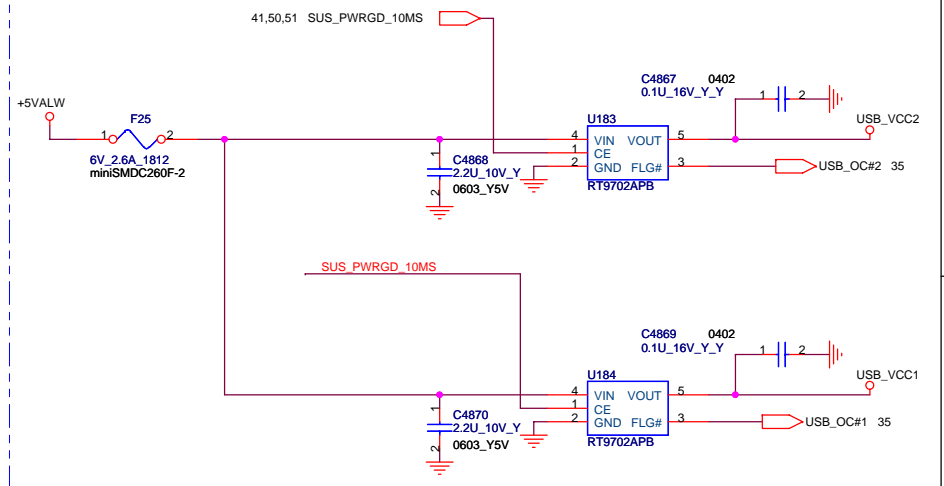
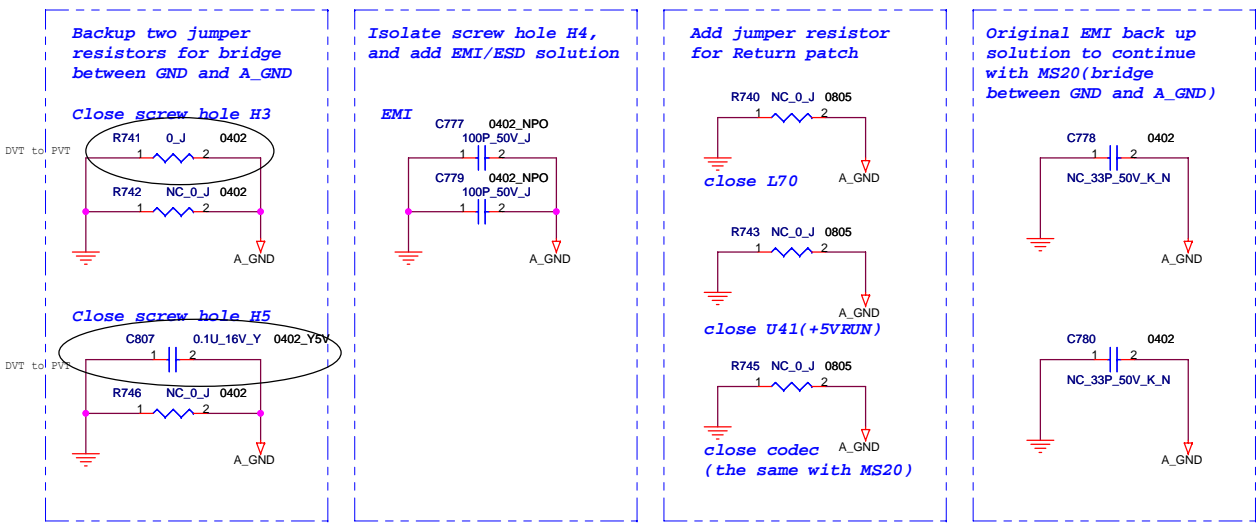
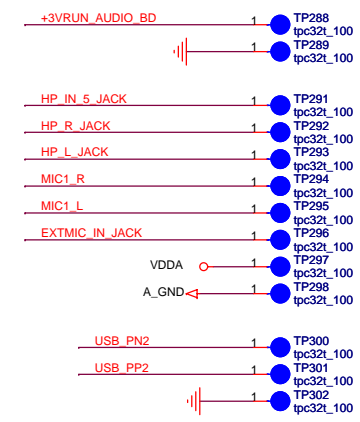
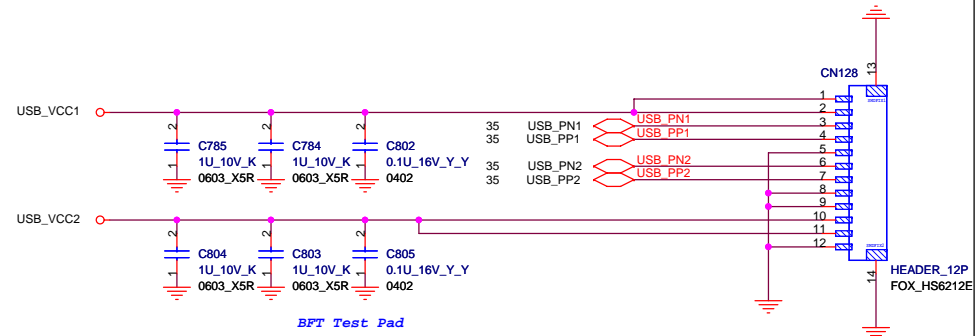
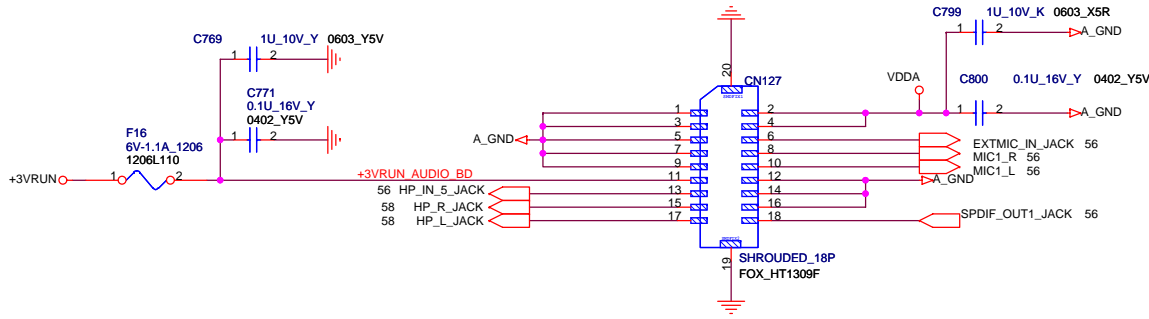
2W AMP



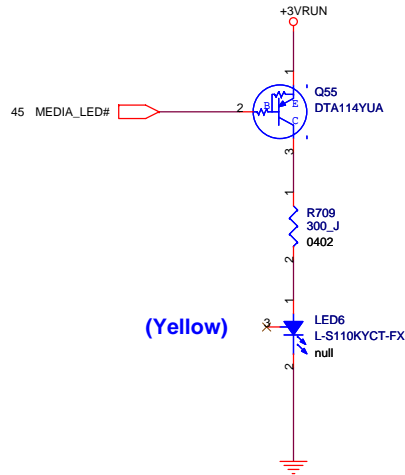
SUB_WOOFER POWER



Audio Board connector

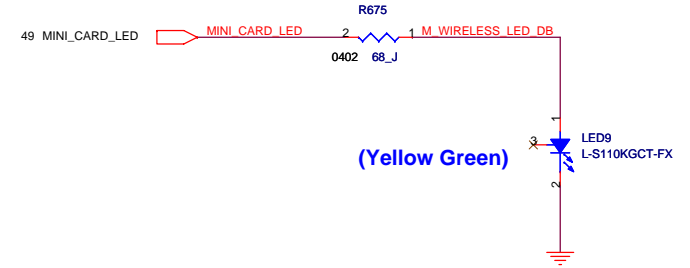


MS/SD LED



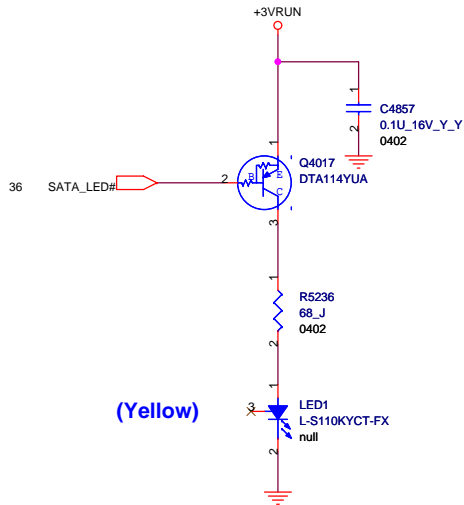
230. (Page 64) 07/12/05 Change MS/SD LED control signal share one LED

WLAN/BLUETOOTH LED

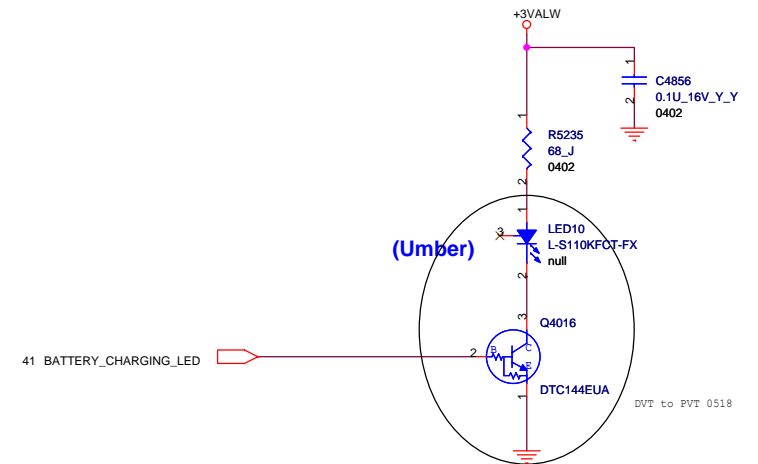


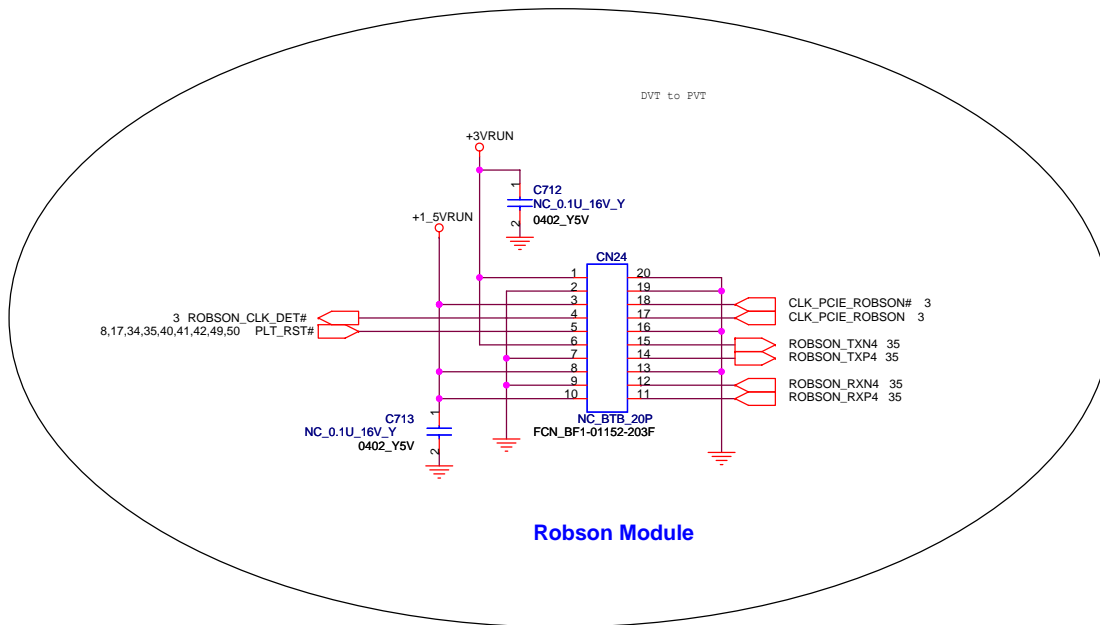
232. (Page 64) 07/12/05 Change Wireless/Bluetooth LED control signal share one LED

HDD/ODD LED

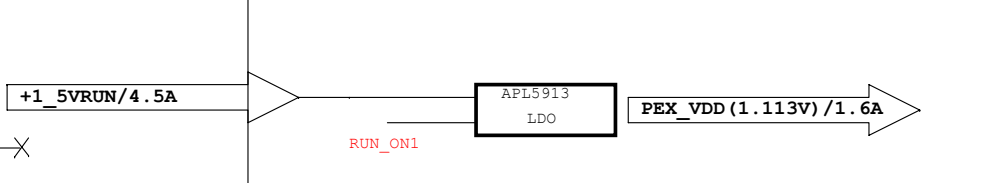
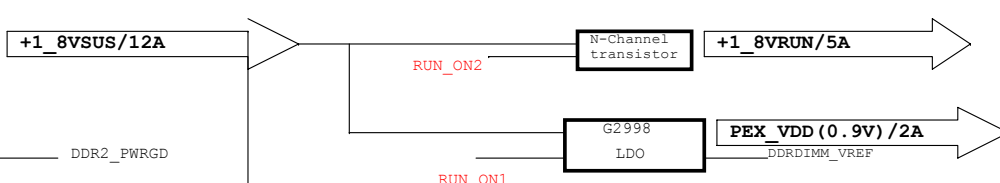
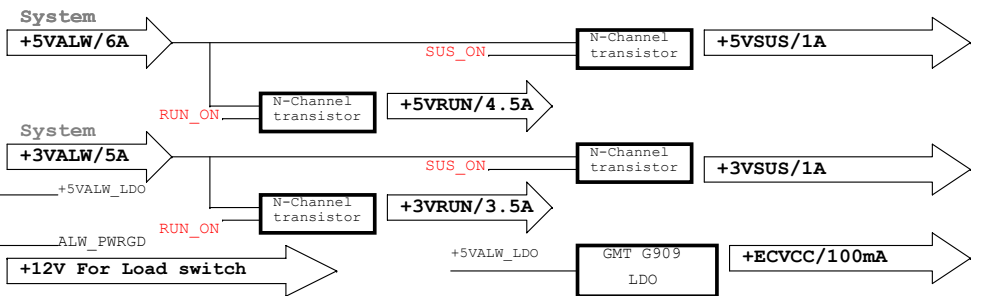
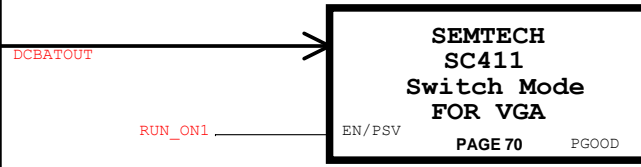
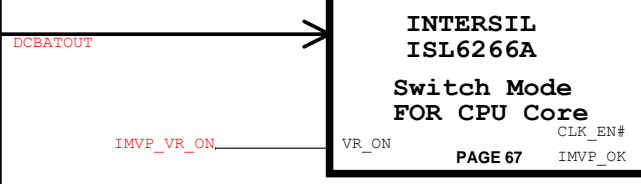
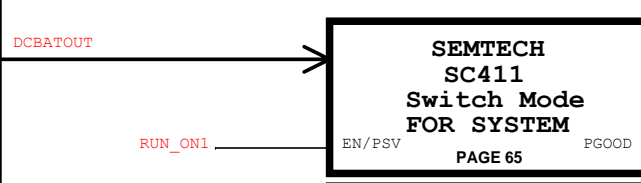
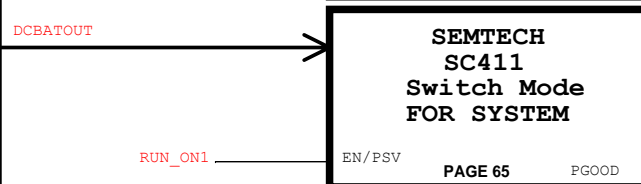
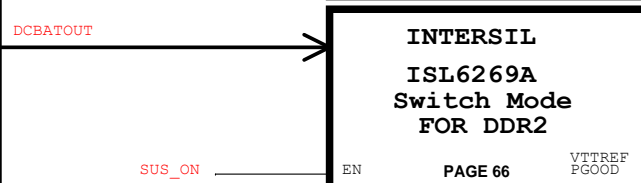
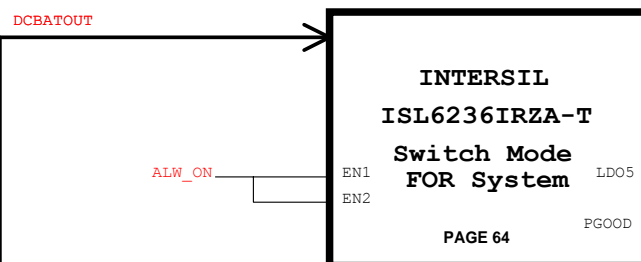
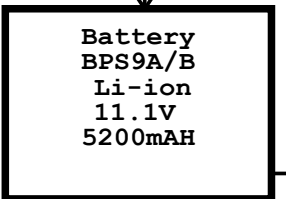
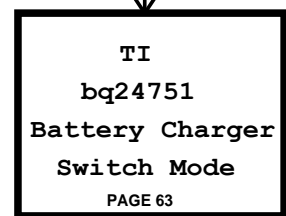
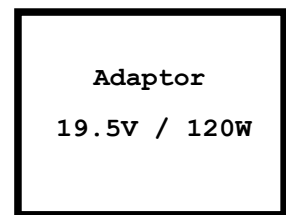


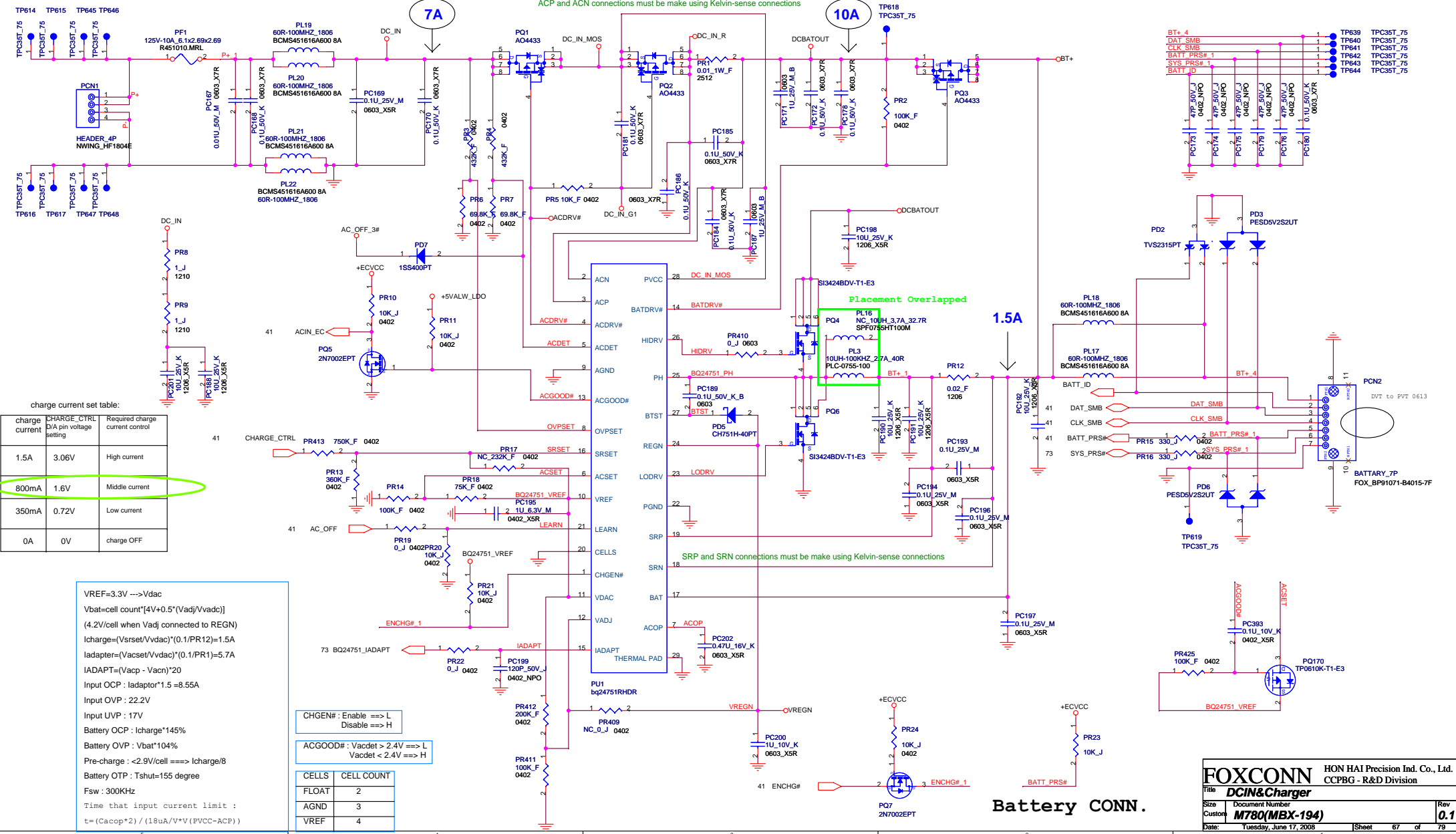
Charge LED





FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
Robson1.6 Connector			
Size	Document Number		Rev
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charge current set table:

Charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
800mA	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V --->Vdac
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdac})]$
 (4.2V/cell when Vadj connected to REGN)
 $I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR12) = 1.5A$
 $I_{adaptor} = (V_{vacset} / V_{vdac}) * (0.1 / PR1) = 5.7A$
 $IADAPT = (V_{vacp} - V_{vacn}) * 20$
 Input OCP : $I_{adaptor} * 1.5 = 8.55A$
 Input OVP : 22.2V
 Input UVP : 17V
 Battery OCP : $I_{charge} * 145\%$
 Battery OVP : $V_{bat} * 104\%$
 Pre-charge : $< 2.9V / \text{cell} ==> I_{charge} / 8$
 Battery OTP : $T_{shut} = 155 \text{ degree}$
 $F_{sw} = 300KHz$
 Time that input current limit :
 $t = (C_{acop} * 2) / (18uA / V * V (PVCC - ACP))$

CHGEN# : Enable ==> L	Disable ==> H
ACGOOD# : Vacdet > 2.4V ==> L	Vacdet < 2.4V ==> H
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

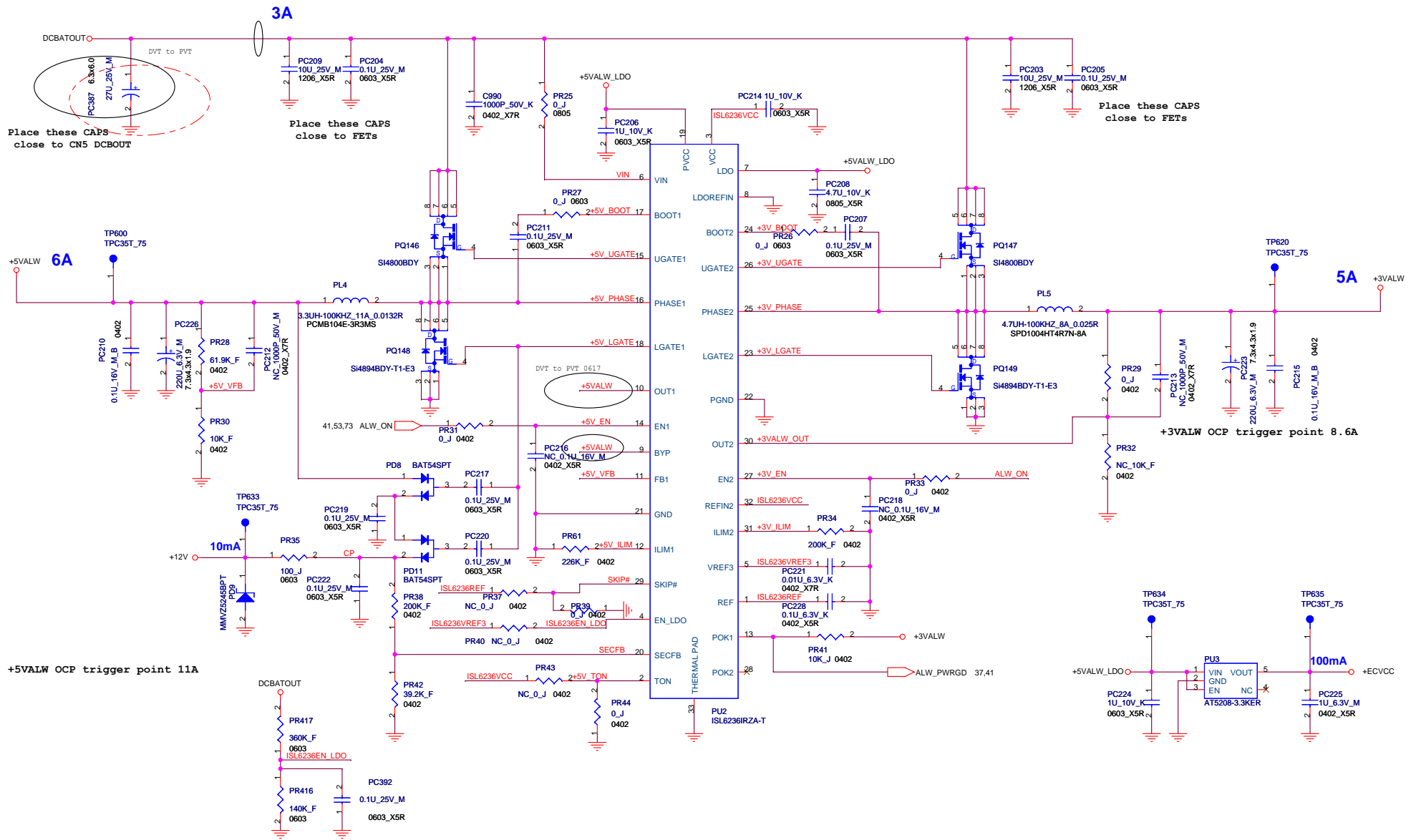
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

Title: **DCIN&Charger**

Size: Document Number
 Custom: **M780(MBX-194)** Rev: **0.1**

Date: Tuesday, June 17, 2008 | Sheet: 67 of 79

Battery CONN.



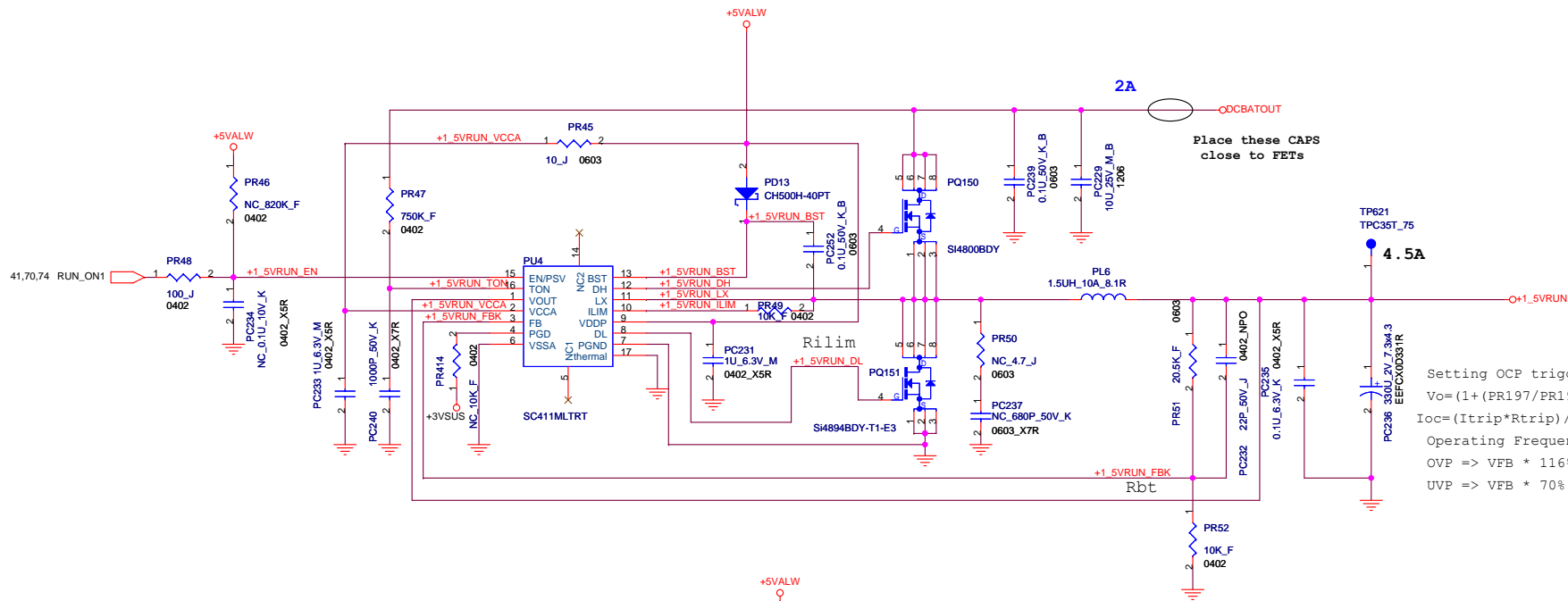
TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

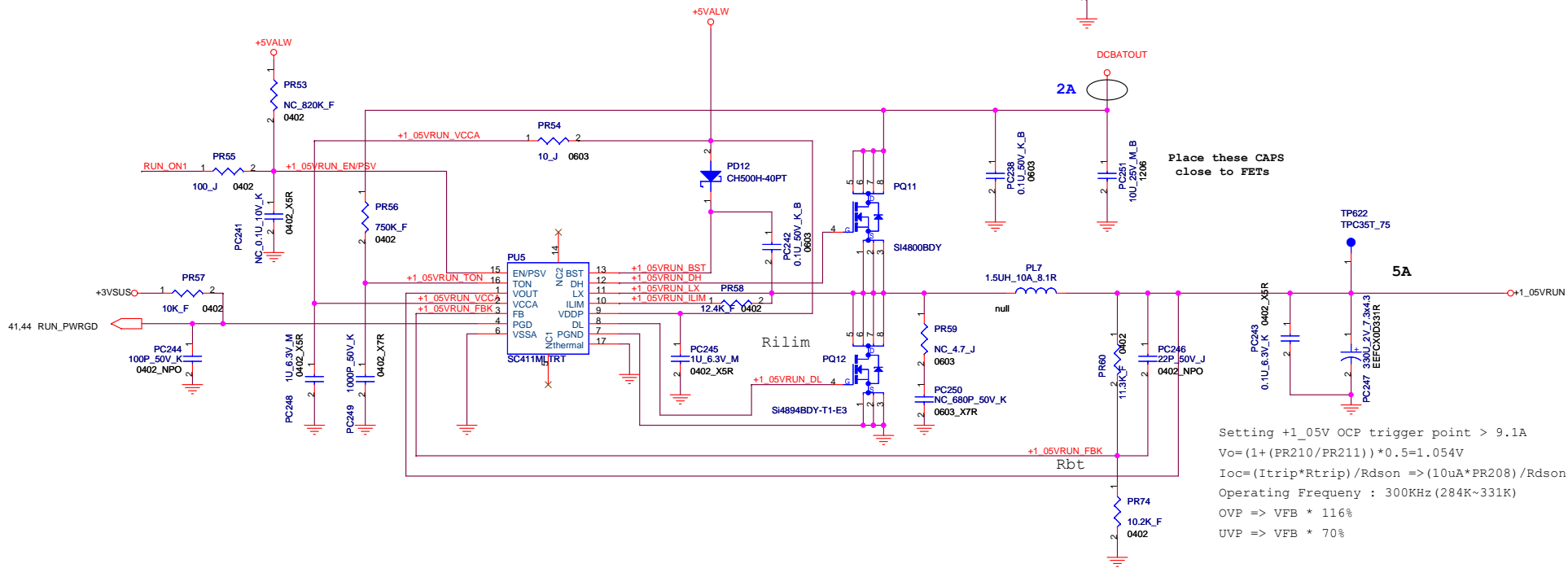
$$L = VOUT (VIN - VOUT) / (VIN * f * LIR * ILOAD (MAX))$$

$$Rocp = (Iocp - Iripple / 2) * (10 * Rds(on)) / 5u$$

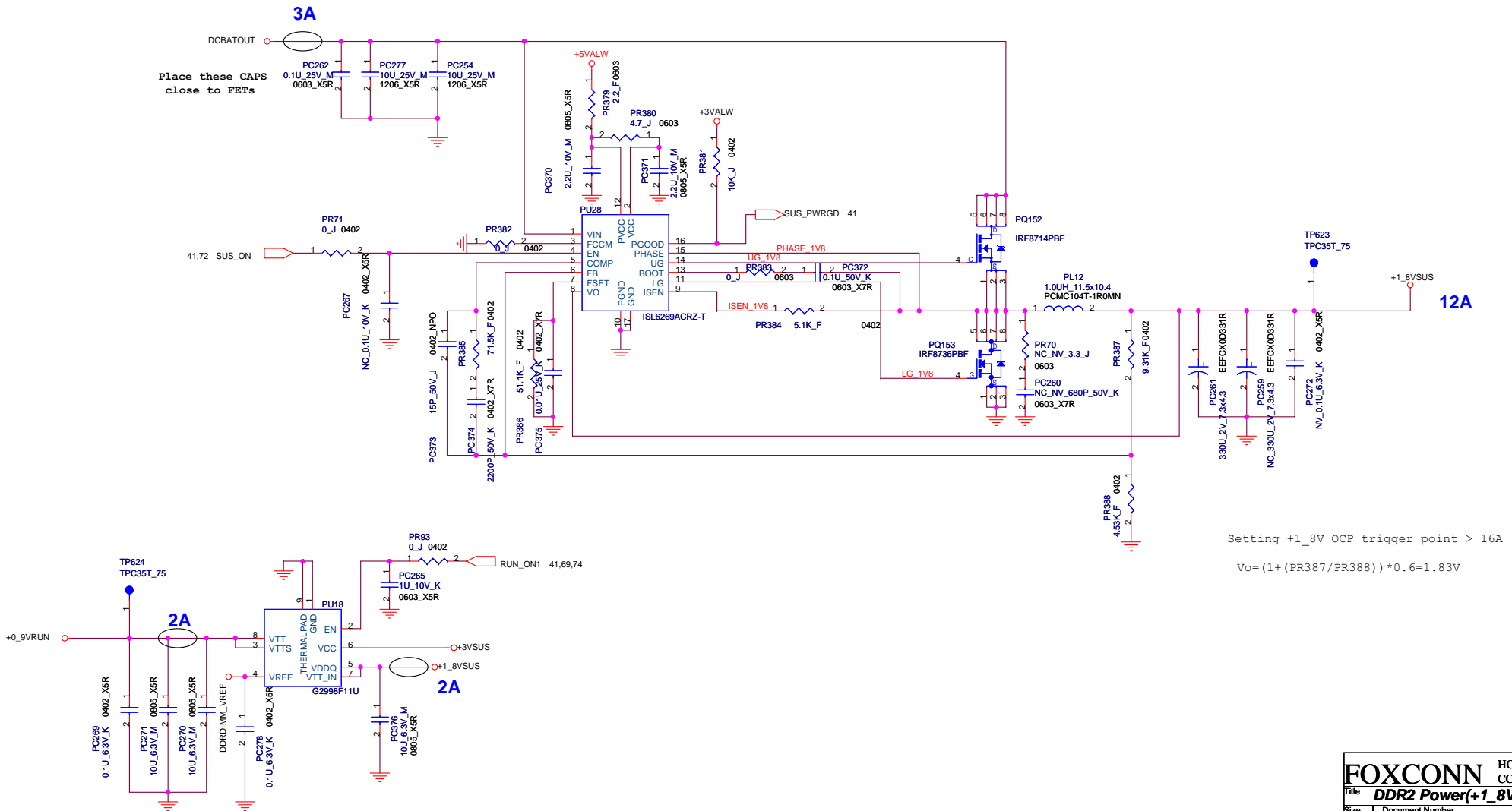
$$+5VALW = ((PR28 / PR30) + 1) * VFB1$$

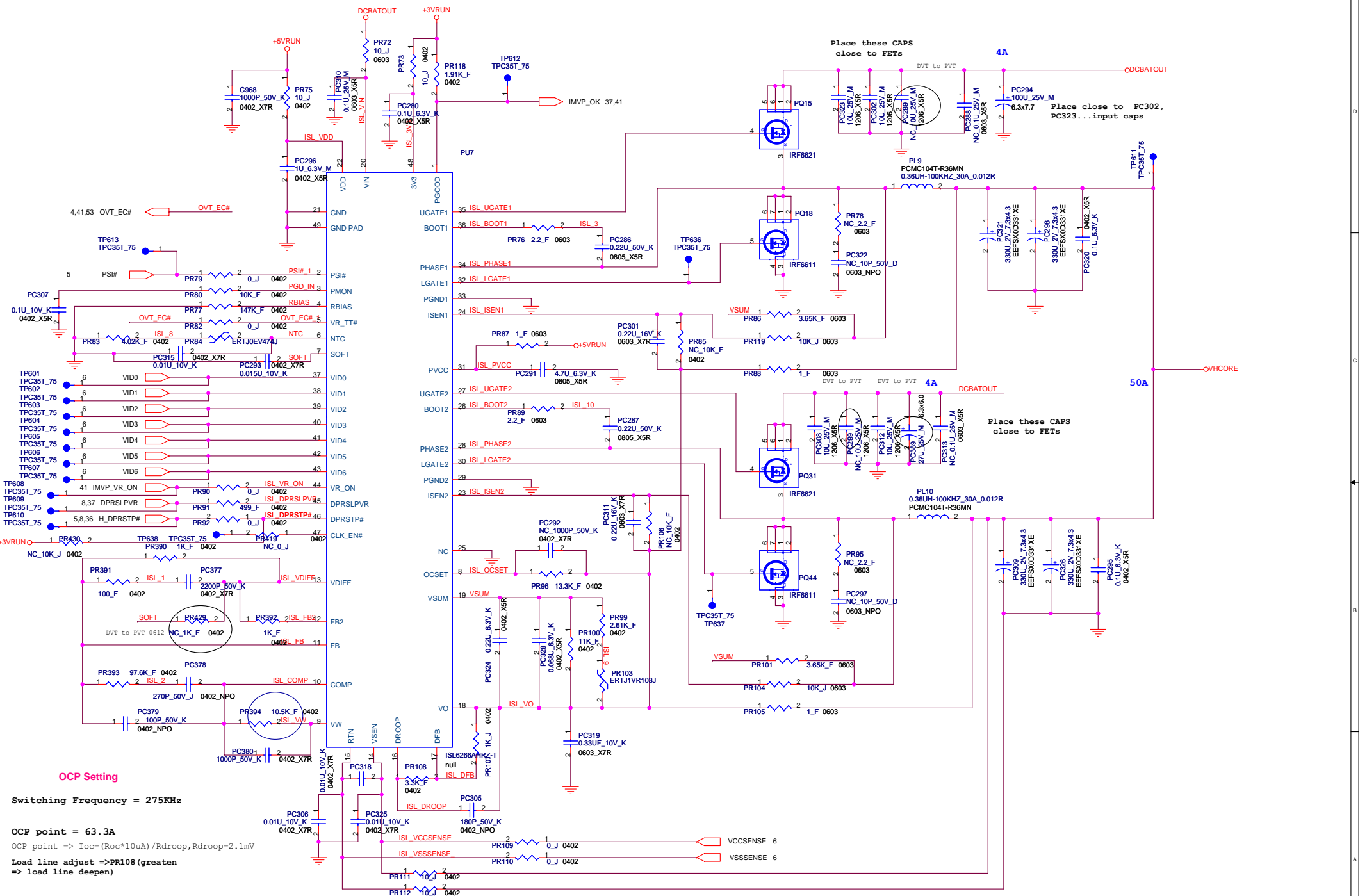


Setting OCP trigger point > 7.5A
 $V_o = (1 + (PR197/PR198)) * 0.5 = 1.525V$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR194) / R_{dson}$
 Operating Frequency : 330KHz (308K~345K)
 OVP => VFB * 116%
 UVP => VFB * 70%



Setting +1.05V OCP trigger point > 9.1A
 $V_o = (1 + (PR210/PR211)) * 0.5 = 1.054V$
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR208) / R_{dson}$
 Operating Frequency : 300KHz (284K~331K)
 OVP => VFB * 116%
 UVP => VFB * 70%





Place these CAPS close to FETs

4A

Place close to PC302, PC323...input caps

Place these CAPS close to FETs

50A

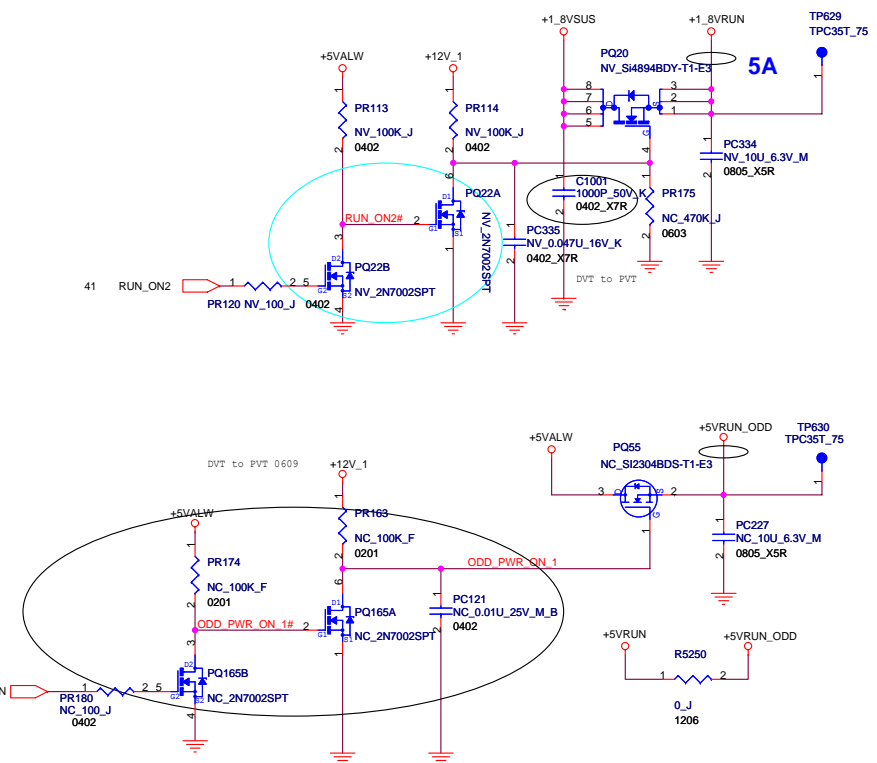
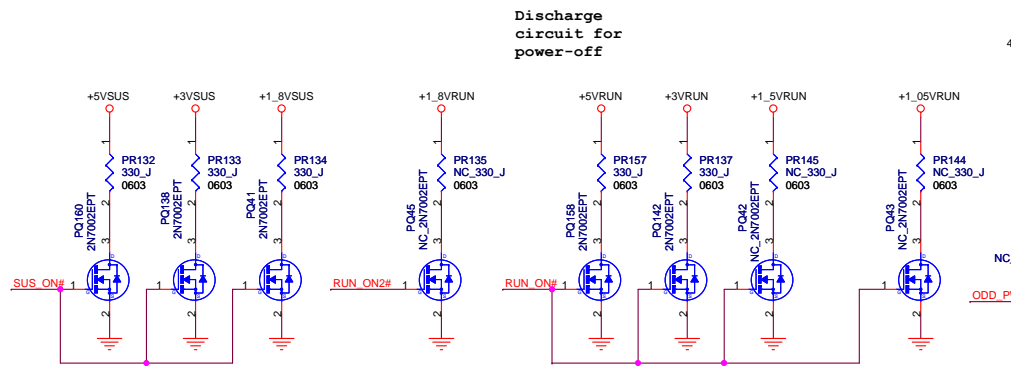
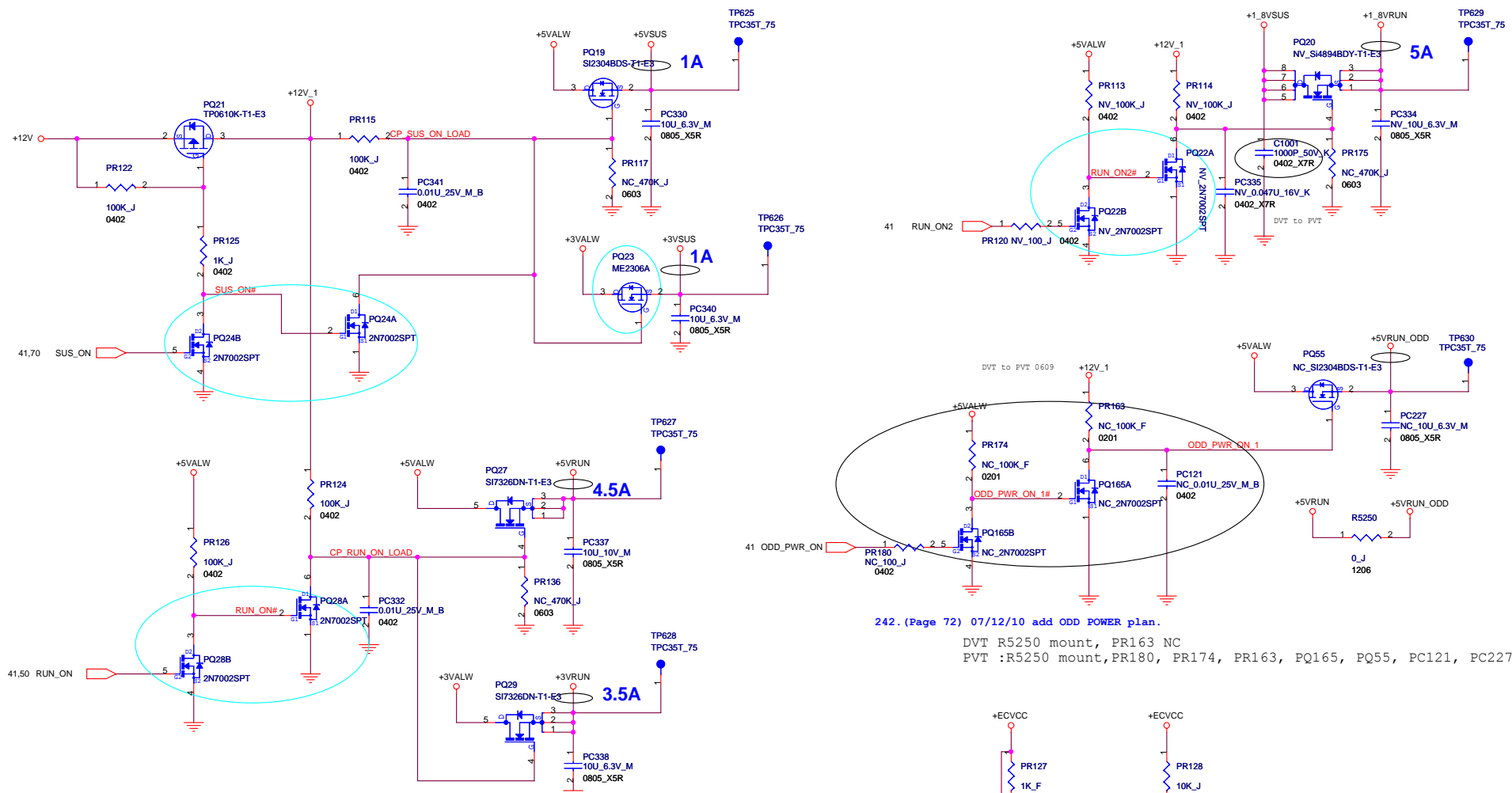
OCP Setting

Switching Frequency = 275KHz

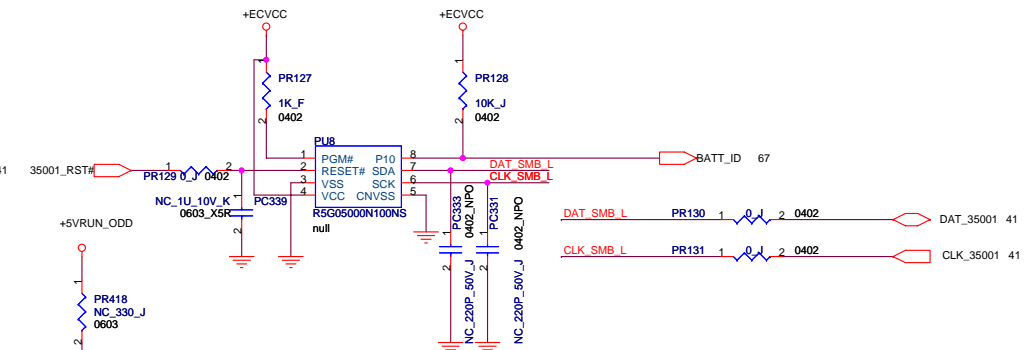
OCP point = 63.3A

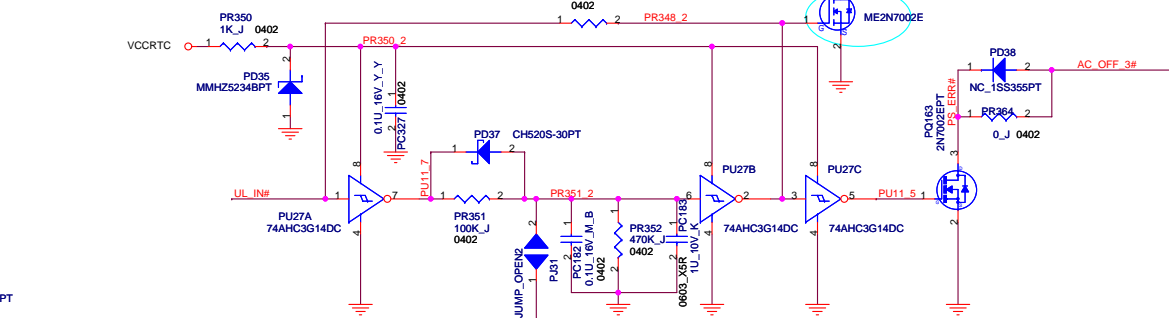
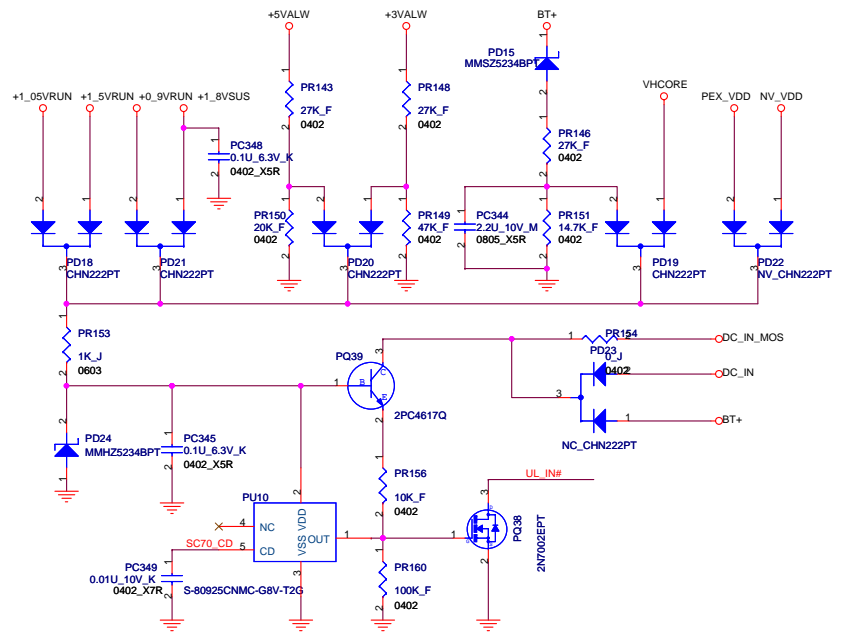
OCP point => $I_{oc} = (R_{oc} * 10uA) / R_{droop}$, $R_{droop} = 2.1mV$

Load line adjust => PR108 (greater => load line deepen)

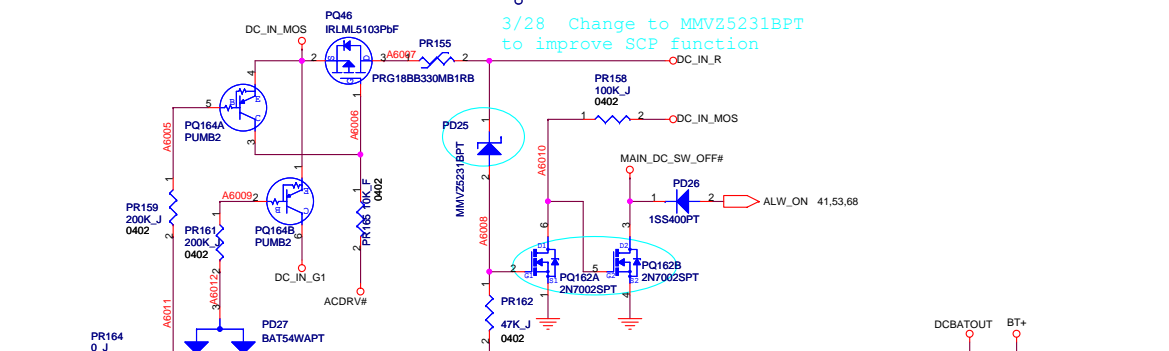


242. (Page 72) 07/12/10 add ODD POWER plan.
 DVT :R5250 mount, PR163 NC
 PVT :R5250 mount, PR180, PR174, PR163, PQ165, PQ55, PC121, PC227 all NC



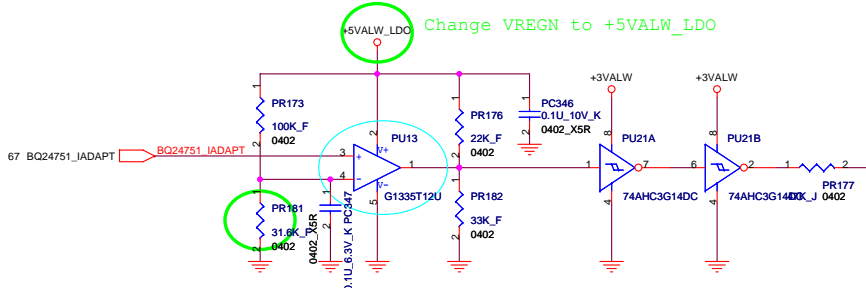


3/28 Change to MMV25231BPT to improve SCP function



System SCP protect

Battery UVP protect



120W adaptor

PWRLIMIT	1.2V/114W
----------	-----------

Adaptor max load: 7.7A under 3 sec
Adaptor OCP: 9.7A typ
11A max

3/28 Add battery UVP protect circuit to separate SCP and OCP function.

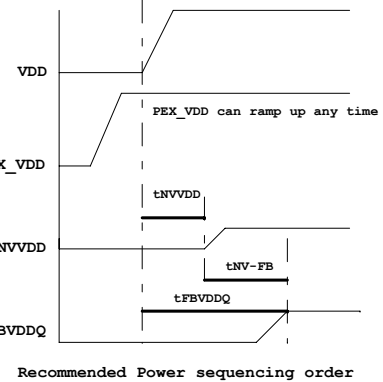
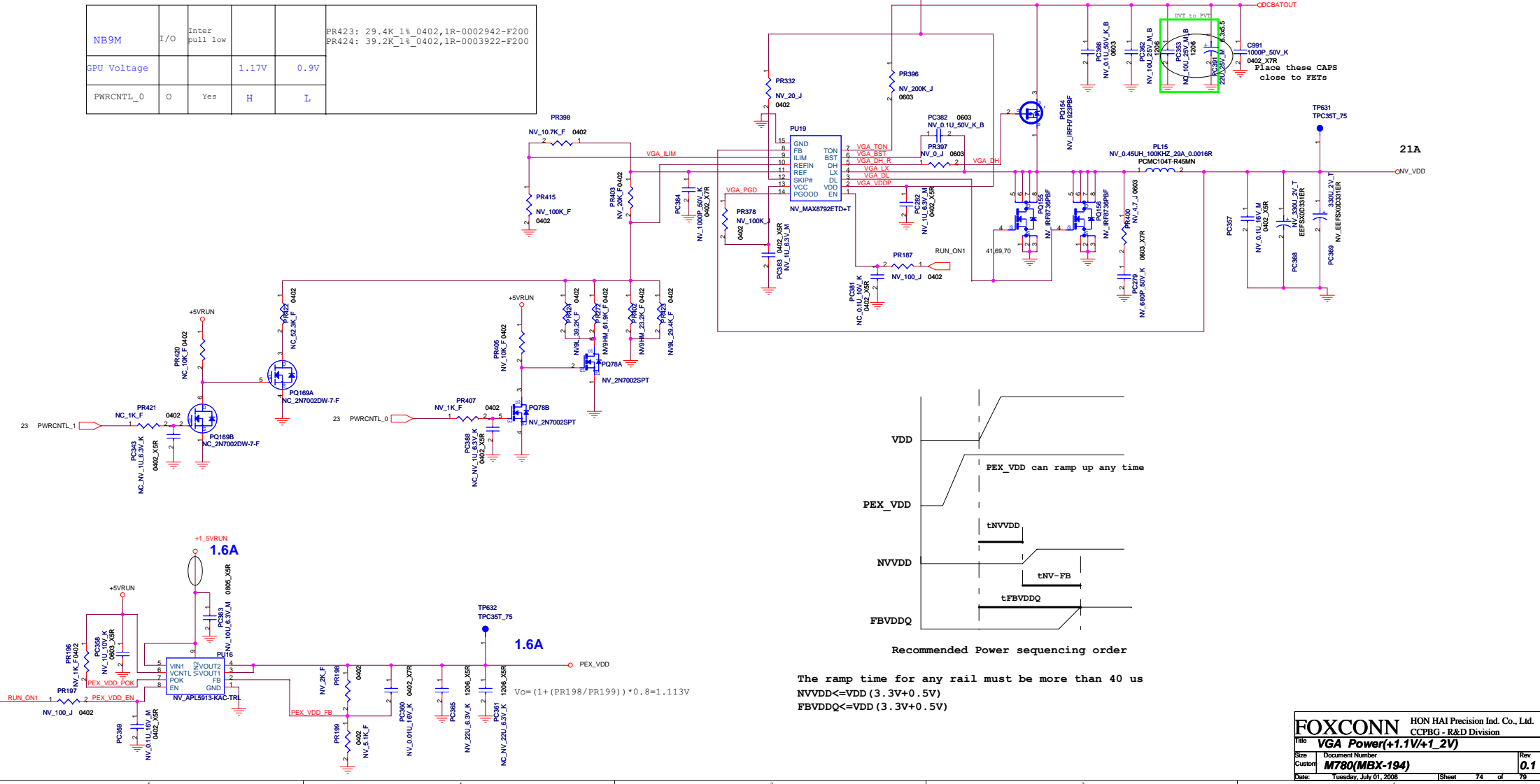
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
OVP protection			
Size	Document Number		Rev
Custom	M780(MBX-194)		0.1
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TABLE (01/08)

NB9P	I/O	Inter pull low			PR402: 23.2K 1%_0402,1R-0002322-F200 PR272: 61.9K 1%_0402,1R-0006192-F200
GPU Voltage			1.05V	0.9V	
PWRCNTL_0	O	Yes	H	L	

NB9M	I/O	Inter pull low			PR423: 29.4K 1%_0402,1R-0002942-F200 PR424: 39.2K 1%_0402,1R-0003922-F200
GPU Voltage			1.17V	0.9V	
PWRCNTL_0	O	Yes	H	L	

Setting current limit trigger point >25A
 $V_o = V_i$; $V_f = ((PR272 + PR402) / (PR403 + PR272 + PR402)) * 2$
 $V_{lim} = 20 [I_o - I_r / 2] * R_{low-dsn} * 1.2$
 Operating Frequency : 300KHz
 OVP => $V_o + 0.25V$
 UVP =< $V_{FB} - 0.16V$

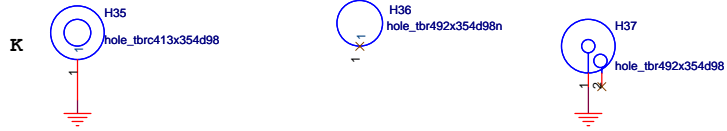


Recommended Power sequencing order
 The ramp time for any rail must be more than 40 us
 $NVVDD \leq VDD (3.3V + 0.5V)$
 $FBVDDQ \leq VDD (3.3V + 0.5V)$

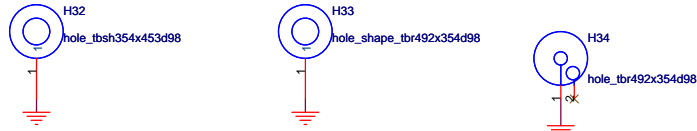
HOLE (TOP SIDE)

HOLE (BOTTOM SIDE)

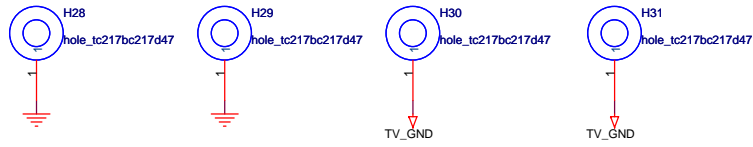
Type 1



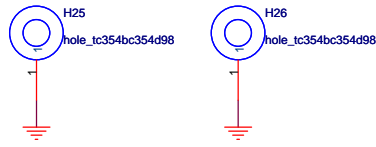
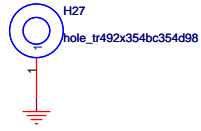
Type 2



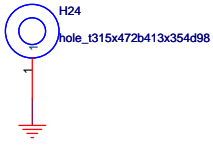
Type 3



Type 4



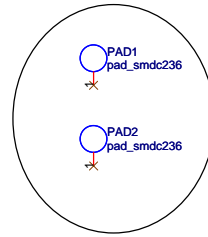
Type 5



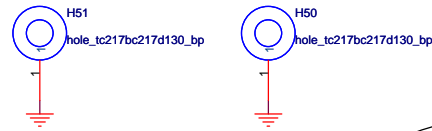
Type 6



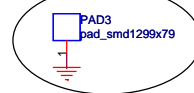
DVT to PVT 0617



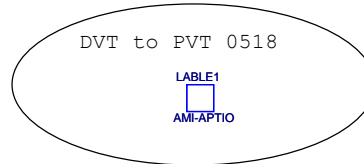
Robason Hole



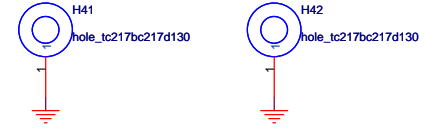
DVT to PVT



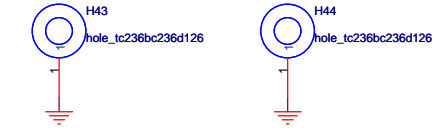
DVT to PVT 0518



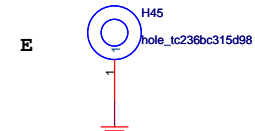
Type 2



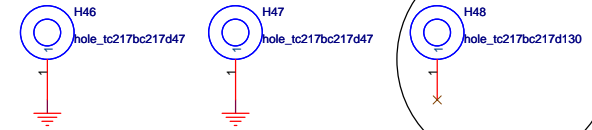
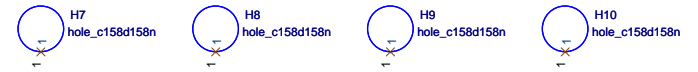
Type 3



Type 4



Type CPU



DVT to PVT 0611

FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title	HOLE & BOSS	
Size	Document Number	Rev
A3	M780(MBX-194)	0.1
Date:	Wednesday, June 25, 2008	Sheet 75 of 79

M780 EVT Change History

- (Page 37) 07/08/21 As IC9N LAN_RST# need to pull low to GND, Add 10K to GND.
(Page 41) 07/08/21 Change EC Ping3(RUN GM2) pull low value from 100K to 4.7K.
(Page 38) 07/08/29 Put to HDA bus is changed to 1.5V level, HDA_CODEC_RST# signal is not fling...

POWER Change History

- (Page 44) 07/09/28 Change PQ6 IRK7904 to PQ146/PQ148:SI4800B/SI4894 ==>component cost down
(Page 44) 07/09/28 Change P14 from 3.3V(CT) to 4.7V(A05)==>component cost down
(Page 44) 07/09/28 Change PQ9 IRK7904 to PQ177/PQ149:SI4800B/SI4894==>component cost down

- (Page 20) 07/11/06 delete head 171 for IPFMA_OVERRIDE.
(Page 22) 07/11/06 delete H172 for IPFMA_OVERRIDE.
(Page 22) 07/11/06 add 100ohm pull to GND for IPFMA_OVERRIDE.
(Page 27) 07/11/06 Change R4799,R4800,R4812,R4801 and C556 to MC.
(Page 27) 07/11/06 delete R1775,R815 for VPU portion.

- (Page 45) 07/11/06 add GPIO PIN 32,REST_ICH,CF_REST_CARD8 for CF timing.
(Page 34) 07/11/06 delete Mini Pideo Jack,B-Video IN for MOR request.
(Page 43) 07/11/06 updated EC GPIO pin table for EC team request.
(Page 12) 07/11/06 updated VCC Power portion for yellow mark.
(Page 32) 07/11/07 Change U16 from G548R2P1U to G528R1C1U by the comment from MOR side.

EE Change History

- (Page 41) 07/11/27 change power plane from +5V8UN to +5V8UN
(Page 51) 07/11/27 change power plane from +5V8UN to +5V8UN
(Page 49) 07/11/27 change power plane from +5V8UN to +5V8UN
(Page 49) 07/11/27 change power plane from +5V8UN to +5V8UN
(Page 53) 07/11/27 change power plane from +5V8UN to +5V8UN

- (Page 54) 07/11/15 Change EXPRESS CARD Connector(CN28),(CN29) for design require.
(Page 50) FR_CAL_TERM_GND is 400
(Page 51) 07/11/16 Add CN123,CN124 for Design require
(Page 47) 07/11/16 Change U168 from GMT to RICOH
(Page 34) 07/11/19 Change ground TV power sequence.
(Page 58) 07/11/19 Change CAP34 from 100u to 220u for MOR request.

- (Page 68) 7/11/22 change PR13 from 499K to 360K for charge current set table change.
(Page 68) 07/11/22 change PR412 from 191K to 260K for charge voltage set .
(Page 68) 07/11/22 delete P04 200K for Leakage current issue .
(Page 68) 07/11/22 add 2nd source SPR195M.
(Page 69) 07/11/22 delete R4814 because the 3V3V pwn f change from 400k/500k to 400k/300k

EE Change History

- (Page 41) 07/11/27 change power plane from +5V8UN to +5V8UN
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(Page 49) 07/11/27 change power plane from +5V8UN to +5V8UN
(Page 53) 07/11/27 change power plane from +5V8UN to +5V8UN

- (Page 64) 07/12/05 Change Wireless/BluetoothLED control signal share one LED
(Page 64) 07/12/05 Delete bluetooth NET_BT_PIO#
(Page 43) 07/12/05 Delete ODD_Net_ODD_P#
(Page 53) 07/12/06 Change thermal sensor US9 to 78R01P81U
(Page 49) 07/12/06 Change WIA Conn CN31 to FOX_A08226_R40N_7F.

- (Page 68) 7/11/22 change PR13 from 499K to 360K for charge current set table change.
(Page 68) 07/11/22 change PR412 from 191K to 260K for charge voltage set .
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EE Change History

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FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
History(EVT to MP)
Document Number: M780(MX-194)
Rev: 0.1

EVT TO DVT

Page 20 .Add power source for FB_DLLAVDD1 & FB_PLLAVDD1

Page 61. change R2164 from 1K to 2.7K for MOR request

Page 57. change SPK AMP Gain setting to 18dB for MOR request

Page 48,49. change BT LED control signal source from BT module directly

Page 32,41. Use SW1 one pin to disable Fan monitor function

Page 54. F11,F12,F18,F19 change from 350mA to 250mA

Page 59. Change Q4019 pin 2 from +3VALW to +5VALW

Page 37. Change EC_OUV1 pin to GPIO12

Page 41. Add R572,R573,R574 pull low

Page 61. R259 NC

Page 41. Add C465,C466 47pF pull low

Page 24. Add R586,R590 for MOR request.

Page 3. Add R5248 in series for MCH_CLK_REQ#.

Page 47. Add F27 Poly switch for CF card protection.

Page 37. Add D9 diode for RUNTIME_SCI# leakage.

Page 41. Add D17,D24 for EC_RCIN#,EC_A20GATE leakage.

Page 23. Add R1779 for PWR_CNTL_0 pull high.

Page 37. Add R455 for Finger print Detect.

Page 60,63. Remove C4830,R740,R743,R745 for MOR request.

Page 33. Add R340,Q122,R2373,Q123 for HDMI drop issue.

Page 3. Add C820 ,C821 for Robson CLK to match rising and falling time spec.

Page 52. Add F13 for CIR FFC protection.

Page 40. Add R75 ,R5249,C138 for 8057 used

Page 49. Remove C18,add R617 for MOR request.

Page 41. Add C913 for EMI.

Page 42. Add C962 for EMI.

Page 53. Add C967 for EMI.

Page 71. Add C968 for EMI.

Page 68. Add C990 for EMI.

Page 74. Add C991 for EMI.

Page 32. Add C992 for EMI.

Page 56. Add C368 for TV .

Page 60. change C4820,C4822,C4825,C4827 to 0.047U
R5146,R5151 to 1.8k R151,R5152 t o5.6k

Page 61. change R244,R249 to 15k R2160 to 18k, PR523,PR524 to 15k, C367 to 0.022U, R2164 to 1.8k.

Page 31. Add C467,C468,C469 for EMI.

Page 46. Mount C453 for EMI.

Page 41. Add R575 for CF always power on.

Page 37. Remove R455,R486 for FP_DET#,change by BIOS detect.

Page 6. add C88,C89 for MOR request.

Page 72. add R5250 for MOR request.

Page 34. add C370,C369 for EMI

Page 41. add C371 for EMI

Page 29. add C993 for EMI

Page 26. add C994 for EMI

Page 41. change charge LED to high active.

Page 57. add C995 for EMI.

Page 33. add C997 for EMI.

Page 62. add C90 for EMI.

Page 41. add C91 for EMI.

Page 54. add C238 for EMI.

Page 47. add U17 ,R91,R92 for CF solution.

Page 73. change PR181 from 34k to 31.6k for changing power limit from 118W to 114W

DVT to PVT

Page 64(LED Status) .charging LED logic change

Page 75(HOLE & BOSS) .Add AMI label on M/BD

Page 31(CRT) .change VSYNC and HSYNC resistor and capacitor for SI test fail.

Page 54(Daughter Board Conn) .change PWR and Suspend LED logic same as M760 for more brightness.

Page 47(PCI CF) .separate CF controller power and card power for hot-plug issue.

Page .change NV9P,9M ,HDCP KEY HH P/N

Page 17(VGA (PCI-E) 1/9) .L4049 change vendor

Page 41(EC+KBC (WPCE775L) .change RP24,RP25 to +3VALW

Page 67(DCIN&Charger) .Delete PJ1 and PJ2

Page 68(SYS Power (+3 3V/+5V) .Delete PJ3 and PJ4

Page 69(SYS Power(+1 5V/+1 05V) .Delete PJ7 and PJ8

Page 70(DDR2 Power(+I 8V/+0 9V) .Delete PJ10 and PJ13

Page 71(CPU Vcore---ISL6266A) .Delete PJ12

Page 74(VGA Power(0.9V/+1 05V) .Delete PJ15,PJ16,PJ17

Page 43(SATA HDD/CD-ROM) .change CN126 to KOTL

Page 3(CLOCK GEN (SL28648BLC) .U123 change HH P/N

Page 18(VGA (PCI-E BUS)Strap 2/9) .add samsung VRAM strap pin

Page 55(OIDE/CAM) .change OIDE connector to LNC PVT 0605.pdf

Page 60(AUDIO(EQ) .C4820,C4822,C4825,C4827; Change from 0.047u/50V to 0.015u/25V,R5146,R5151; Change from 1.8k to 3.3k

Page 61(AVD20 (Filter Circuit) .R2164 change to 1k,R2165 change to 4.7k

Page 72(Others power plan) .R5250 mount,PR180, PR174, PR163, PQ165, PQ55, PC121, PC227 all NC

Page 51(USB 2.0) .add USB connector TID No.

Page 55(OIDE/CAM) .change camera connector for easy to unplug.

Page 43(SATA HDD/CD-ROM) .change ODD connector to 14 pin

Page 75(HOLE & BOSS) .change H48 to PTH type

Page 55(OIDE/CAM) .reserve 3.3V for camera module.

Page 47(PCI CF) .change discharge circuit for CF card power,add 4.7U for CF card power ,change CF card LED power source.

Page 45(PCI (LINK) .change Y5 capacitor for accuracy.

Page 71(CPU Vcore---ISL6266A) .PR429 NC

Page 67(DCIN&Charger) .PCN2 add two pillars to fix position for our production line smoothly. PVT 0613.pdf

Page 1(index) .change HH P/N

Page 75(HOLE & BOSS) .add two PAD for ME request

Page 68(SYS Power (+3 3V/+5V) .PU2 Pin9 ,pin10 connect from +5VALW_PWM to +5VALW PVT 0617.pdf

Page 41(EC+KBC (WPCE775L) .mount R516,C592 for EMI

Page 24(VGA (INTER DISPLAY) 8/9) .mount C828 for EMI

Page 41(EC+KBC (WPCE775L) .add C998 for EMI

Page 48(blueetooth) .add C999 for EMI

Page 40(Marvell GLAN(88E8055) .add C1000 for EMI

Page 72(Others power plan) .add C1001 for EMI

Page 41(EC+KBC (WPCE775L) .add C1002 for EMI

Page 56(AUDIO(CODEC & POWER) .add C1003 for EMI

Page 54(Daughter Board Conn) .add C1004,C1005 for EMI

Page 54(Daughter Board Conn) .add L31,L32 for EMI

Page 23(VGA (XTAL/GPIO) 7/9) . reserve D10,R5251,R5252,C93,R1780 for HDMI Audio issue.

Page 56(AUDIO(CODEC & POWER) . reserve R749,C12 for HDMI Audio issue.

Page 63(Audio BOARD conn) . mount R741,change R744 to C807 0.1u for EMI

Page 56(AUDIO(CODEC & POWER) .change R5222 to C809 0.1uf for EMI.

Page 42(AUDIO(Flash ROM/SPI) .CN16 change from 1200 to 1203 for EOL issue.

Page 65(Robson 1.7 Connector) .remove CN24,C712,C713 for Robson no used.

Page 65(AUDIO (SUBWOOFER AMP) .change R5228 from 68k to 6.8k for MOR request.

Page 75(HOLE & BOSS) .Add PAD 3 for ME request.

Page 75(LVDS) .reserve C472 for invertor power PVT 0625.pdf

Page 31(CRT) .change L25,L26,L27 to 120R bead,C467,C468,C469 to NC.

Page 62(AUDIO (SUBWOOFER AMP) .change R5226,R5227 to 0.5% resistors

Page 54(Daughter Board Conn) .add U11 for finger print protection. PVT 0627.pdf

Page 71(CPU Vcore---ISL6266A) .PC389 NC,PC299,PC289 mount for solid cap issue.

Page 68(SYS Power (+3 3V/+5V) .PC387 NC for solid cap issue

Page 74(VGA Power(0.3V/+1 05V) .PC391 NC,PC353 mount for solid cap issue.

Page 32(LVDS) .Add C472 for solid cap issue.

Page 45(PCI (LINK) .change R540-R543 to 47 ohm for MS overshoot and undershoot issue.

Page 41(EC+KBC (WPCE775L) .R516,C592 NC for signal quality.

Page 3(CLOCK GEN (SL28648BLC) .change R767 to 47 ohm for EMI issue. PVT 0629.pdf

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