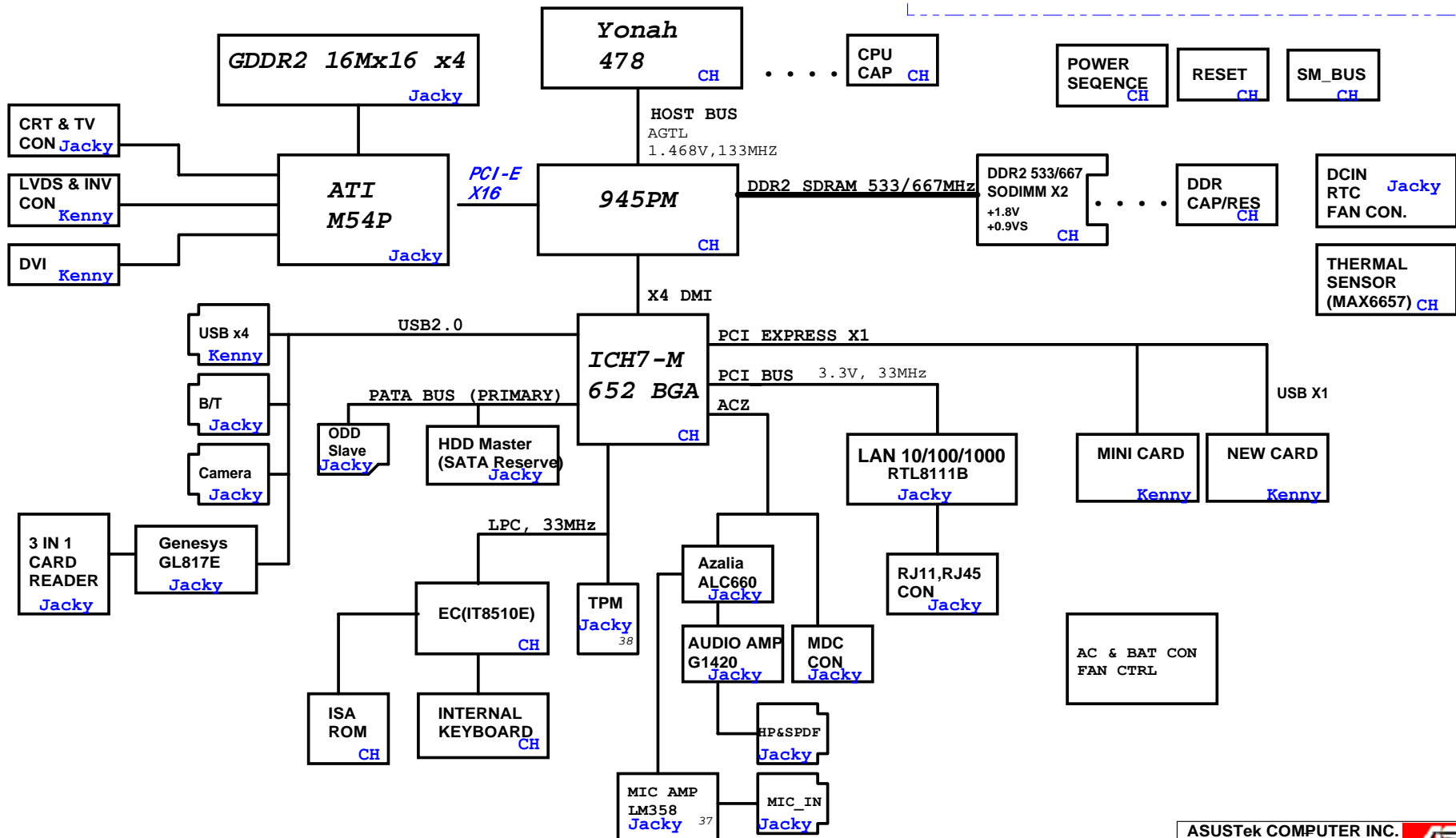
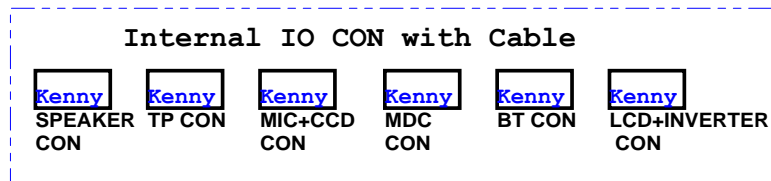
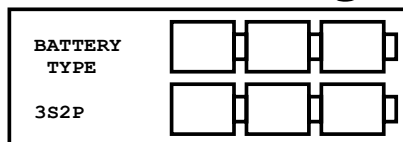


# F2J SCHEMATIC R11(ER)

PAGE	Content	PAGE	Content
	<b>SYSTEM PAGE REF.</b>		<b>POWER PAGE REF.</b>
4	YONAH CPU (1)	50	POWER_VCORE
5	YONAH CPU (2)	51	POWER_SYSTEM
6	CPU CAP/THERMAL SENSOR	52	POWER_I/O_1.5VS & 1.05VS
7	CLOCK GEN.	53	POWER_I/O_DDR & VTT
8	Calistoga--CPU	54	POWER_I/O_+3VAO & +2.5VS
9	Calistoga--PCIE	55	POWER_VGA_CORE & RAM
10	Calistoga--DDR2	56	POWER_+1.2VSP
11	Calistoga--POWER	57	POWER_CHARGER
12	Calistoga--GND	58	POWER_PIC (Empty)
13	Calistoga--Strap	59	POWER_DETECT
14	DDR2 SO-DIMM_0	60	POWER_PROTECT
15	DDR2 SO-DIMM_1	61	POWER_LOAD SWITCH
16	DDR2 ADDRESS TERMINATION	62	POWER_FLOWCHART
17	VGA_ATI_M54P_MAIN(1)	63	POWER_SIGNAL
18	VGA_ATI_M54P_Memory(2)		
19	VGA_ATI_M54P_PCI-E(3)		
20	VGA_ATI_M54P_POWER(4)		
21	DVI CON		
22	VGA_ATI_M54P_VRAM_B(5)		
23	LVDS & INVERTER CONNECTOR		
24	CRT & TV_OUT		
25	ICH7M--CPU, IDE, AUDIO		
26	ICH7M--GPIO		
27	ICH7M--PCI, PCI-E, USB		
28	ICH7M--VCC, GND		
29	HDD & CD-ROM CONN		
30	USB PORTS		
31	PCI-E--MINI CARD		
32	PCI-E--NEW CARD		
33	PCIE--LAN_RTL8111B		
34	EC-IT8510E		
35	ISA ROM & Touch Pad & KB& FP		
36	Debug CON & FAN CONTROL		
37	MDC & TPM CON & LAN		
38	Instant Key & LED		
39	Front side LED & BT		
40	Card Reader GL817E		
41	DISCHARGE		
42	AZALIA - ALC660-GR		
43	AUDIO_AMPLIFIER		
44	MICROPHONE		
45	DC & BAT IN		
46	SREW HOLE		

# F2J Yonah/Calistoga BLOCK DIAGRAM

CLOCK GEN.  
ICS954310  
CH



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Title		
BLOCK DAIGRAM		
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EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	N/A	I
37	PWM3/GPA3	N/A	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/O
164	SMDAT0/GPB4	SMB0_DAT	I/O
5	GA20/GPB5	GA20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	N/A	I
47	CLKOUT/GPC0	N/A	O
169	SMCLK1/GPC1	SMB1_CLK	I/O
170	SMDAT1/GPC2	SMB1_DAT	I/O
171	GPC3	N/A	
172	TMR10/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCH#/GPD3	EXT_SC#	O
41	GPD4	N/A	
42	GINT/GPD5	N/A	
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	N/A	
87	ADC4/GPE0	COLOREN#	
88	ADC5/GPE1	INTERNET#	
89	ADC6/GPE2	MARATHON#	
90	ADC7/GPE3	DISTP#	
2	PWRSW/GPE4	PWR_SW#	
44	WUI5/GPE5	N/A	
24	LPCPD#/WUI6/GPE6	LID_EC#	
25	CLKRUN#/WUI7/GPE7	N/A	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/O
115	PS2DAT1/GPF3	/	I/O
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16_SWAP	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	
28	LPC80LL/GPG7	AC_APPR_UC#	

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	O
55	GPH2	CPUPWR_GD#	O
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	GAIN_AMP#_K	O
155	GPI3	CHG_EN#	O
156	GPI4	/	
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts


SM\_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
Thermal Sensor ( MAX6657)	1001100x ( 98 )
VGA Thermal IC(G781-1)	1001101x ( 9A )

ICH7M\_GPIO

Pin	Use As	Signal Name	Power
GPIO 00	i GPI	PM_BMBUSY#	+3VS
GPIO 01	i GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i GPO	BT_LED_EN	+3VS
GPIO 07	i GPI	RF_ON_SW#	+3VS
GPIO 08	i GPI	EXTSMI#	+3VSUS
GPIO 09	i GPI	CPPE#_DET	+3VSUS
GPIO 10	i GPI	N/A	+3VSUS
GPIO 11	i Native	SMB_ALERT#	+3VSUS
GPIO 12	i GPI	KBC_SC#	+3VSUS
GPIO 13	i GPI	N/A	+3VSUS
GPIO 14	i GPI	N/A	+3VSUS
GPIO 15	i GPO	802_LED_EN	+3VSUS
GPIO 16	O 0 GPO	PM DPRSLPVR	+3VS
GPIO 17	O 1 GPO	PCI_GNT#5	+3VS
GPIO 18	O 1 GPO	STP_PCI#	+3VS
GPIO 19	i 1 GPI	N/A	+3VS
GPIO 20	O 1 GPO	STP_CPU#	+3VS
GPIO 21	i 1 GPO	N/A	+3VS
GPIO 22	i 1 Native	PCI_REQ#4	+3VS
GPIO 23	i 1 Native	N/A	+3VS
GPIO 24	O 0 GPO	MSK_PCIRST	+3VSUS
GPIO 25	O 1 GPO	RST#_NEWCARD	+3VSUS
GPIO 26	O 0 GPO	CPPE_EN	+3VSUS
GPIO 27	O 0 GPO	WLAN_ON#(Reserved)	+3VSUS
GPIO 28	O 0 GPI	BT_DET#	+3VSUS
GPIO 29	i 0 Native	USB_OC#5	+3VSUS
GPIO 30	i 0 Native	USB_OC#6	+3VSUS
GPIO 31	i 0 Native	USB_OC#7	+3VSUS
GPIO 32	O 1 GPO	PM_CLKRUN#	+3VS
GPIO 33	O 1 GPO	BT_ON#	+3VS
GPIO 34	O 0 GPO	CPU_Select	+3VS
GPIO 35	O 0 GPO	TP_LEDON	+3VS
GPIO 36	i 0 GPO	N/A	+3VS
GPIO 37	i 0 GPI	PCB_ID0	+3VS
GPIO 38	i 0 GPI	PCB_ID1	+3VS

Pin	Use As	Signal Name	Power
GPIO 39	i 0 GPI	PCB_ID2	+3VS
GPIO [40:47]	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS
GPIO 49	Native	H_PWRGD	+VCORE

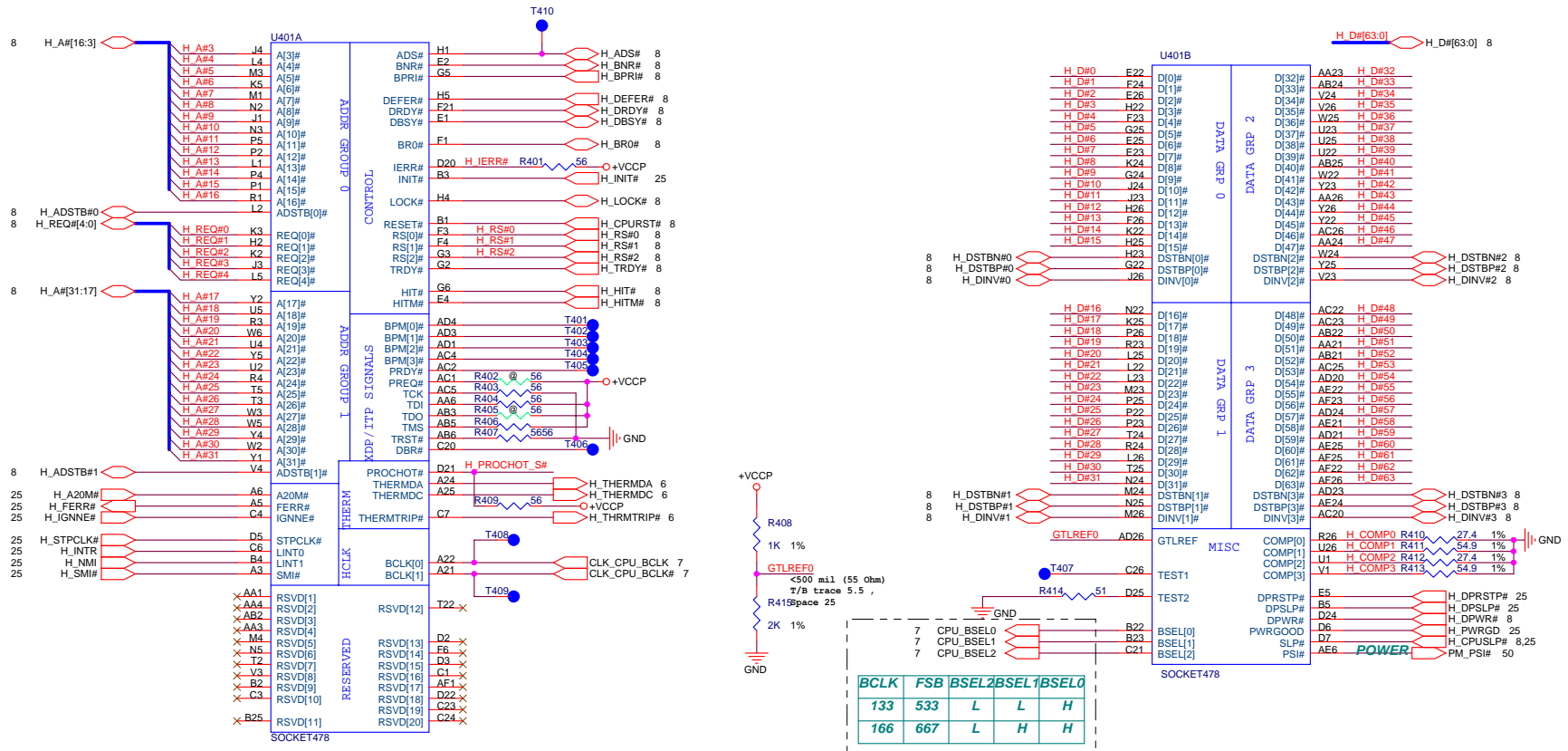
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File: SCHEMATICS REF.

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+VCCP ○ → +VCCP 12.41.52



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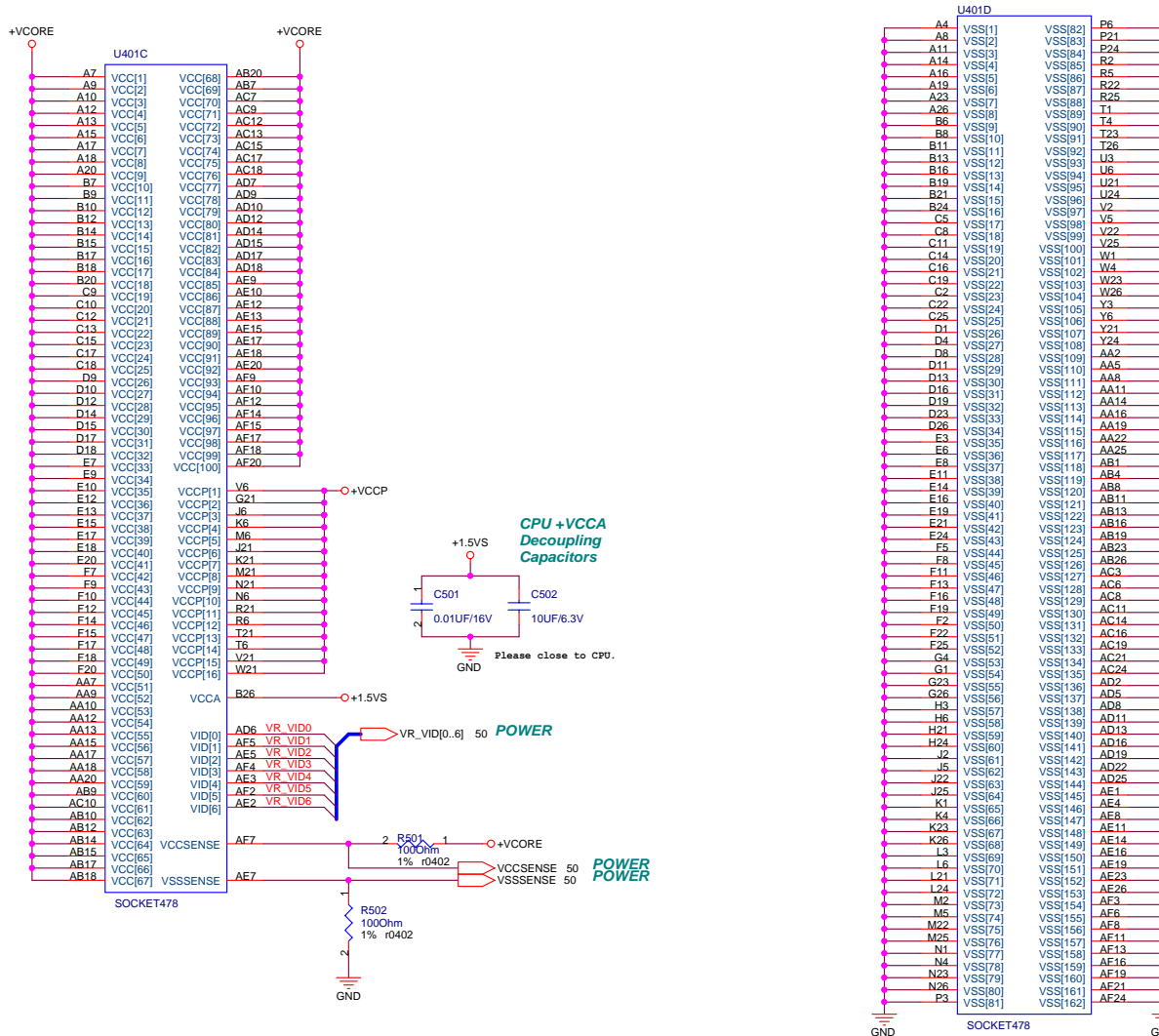
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Title: **YONAH CPU1**

Size	Document Number	Rev
Custor	<b>F2J</b>	1.1

Date: Thursday, April 27, 2006 Sheet 4 of 22

+VCCP	12,41,52
+1.5VS	32,41,52
+VCORE	41,50

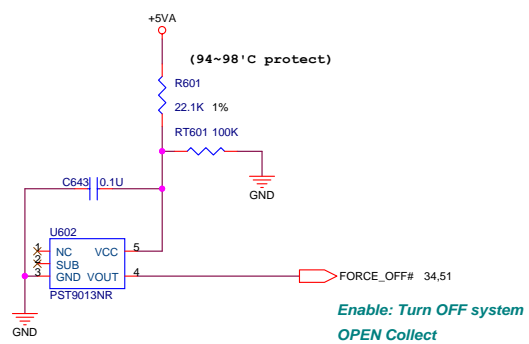
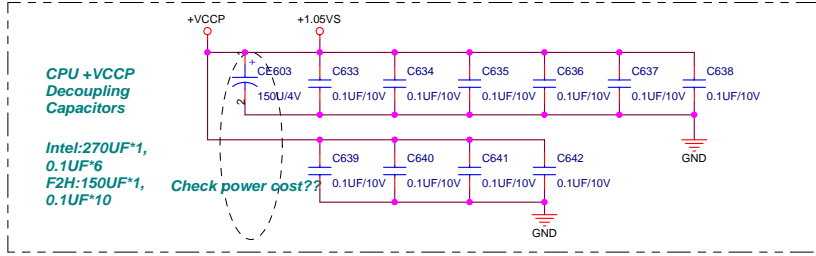
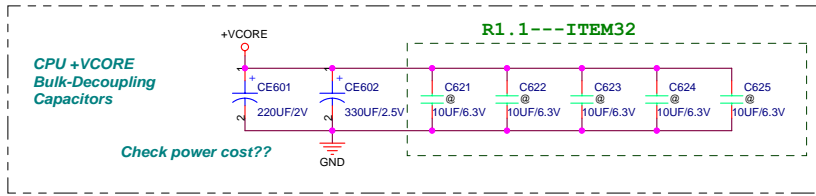
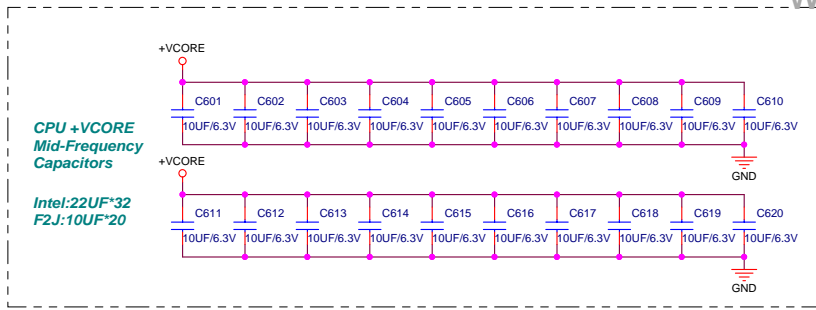


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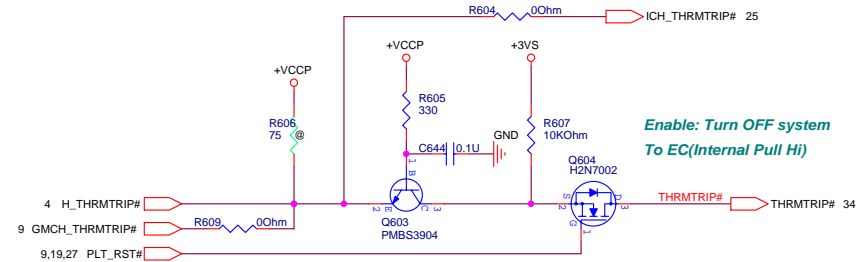
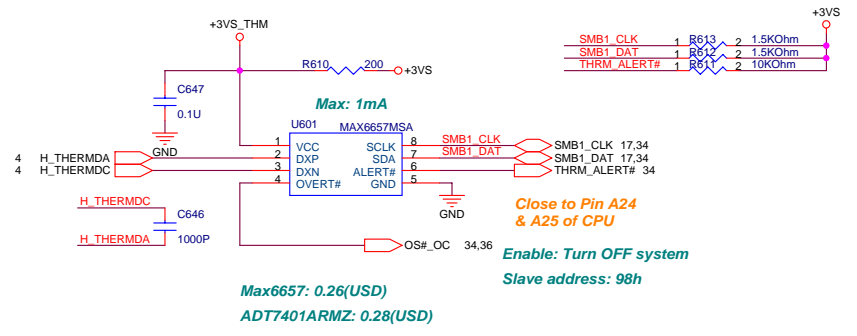
Title: **YONAH CPU2**

Size	Document Number	Rev
Custom	<b>F2J</b>	1.1
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+VCCP	+VCCP	12,41,52
+VCORE	+VCORE	41,50
+3VS	+3VS	17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61
+5VA	+5VA	51,54

### Thermal Sensor



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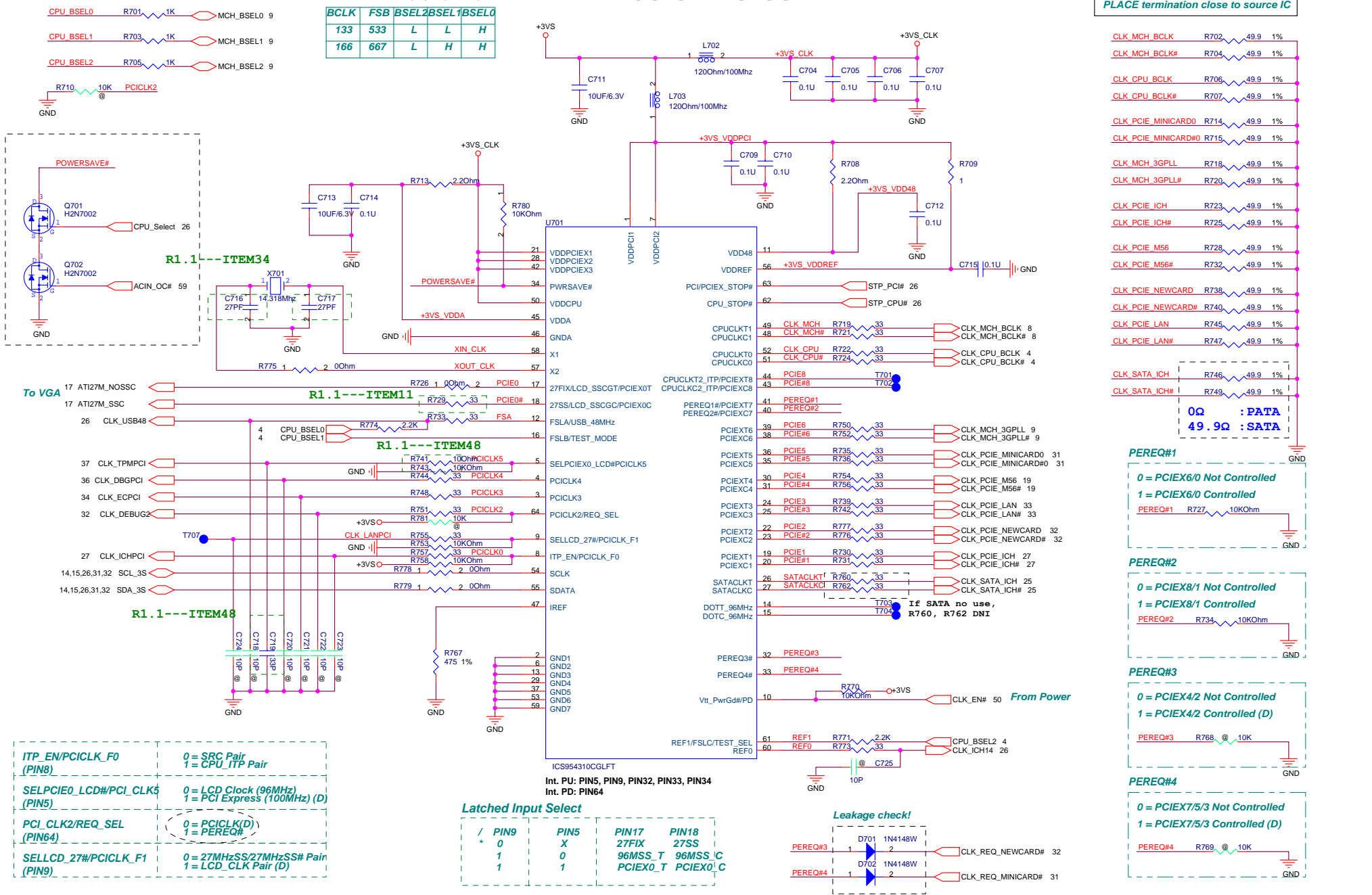
Title: **CPU CAP,THERMAL SENSOR**

Size	Document Number	Rev
Custom	<b>F2J</b>	1.1
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PLACE termination close to source IC

FSLC FSLB FSLA

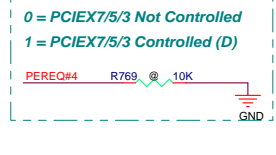
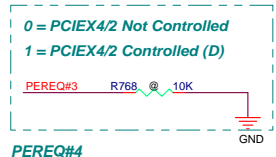
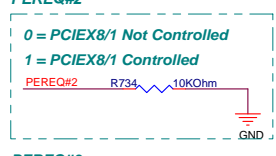
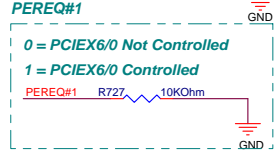
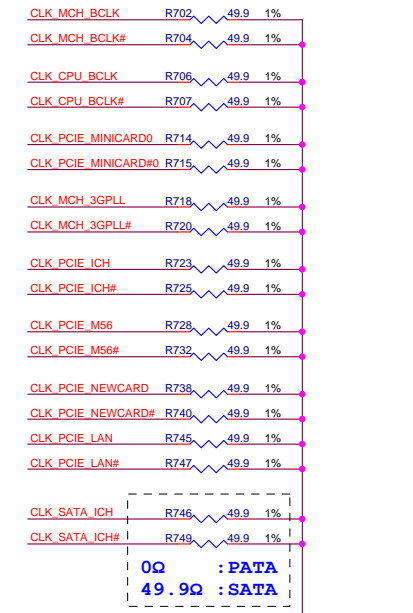
BCLK	F5B	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



To VGA

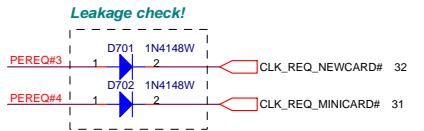
Latched Input Select

/	PIN9	PIN5	PIN17	PIN18
	0	X	27FIX	27SS
*	1	0	96MSS_T	96MSS_IC
	1	1	PCIE_X0_T	PCIE_X0_C



ITP_EN/PCICLK_F0 (PIN8)	0 = SRC Pair 1 = CPU_I/P Pair
SELPCIE0_LCD#/PCI_CLK5 (PIN5)	0 = LCD Clock (96MHz) 1 = PCI Express (100MHz) (D)
PCI_CLK2/REQ_SEL (PIN64)	0 = PCICLK(D) 1 = PEREQ#
SELLCD_27#/PCICLK_F1 (PIN9)	0 = 27MHzSS/27MHzSS# Pair 1 = LCD_CLK Pair (D)

Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34  
Int. PD: PIN64



+3VS → +3VS 17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61

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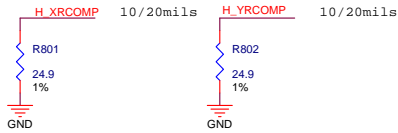
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File: **CLK ICS954310AGLF**

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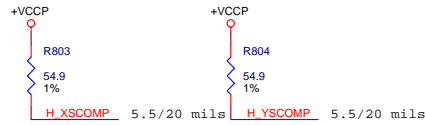
### RCOMP

For Calibrating FSB I/O Buffer



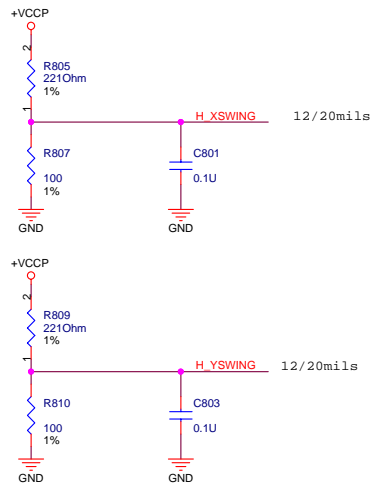
### SCOMP

For Slew Rate Compensation on the FSB



### Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP Circuit



4 H\_D#[0..63] H\_D#[0..63]

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

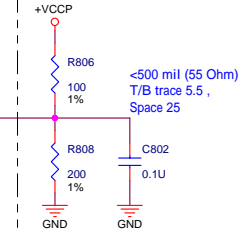
H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U11	H_YSCOMP
H_YSWING	W1	H_YSWING
7 CLK_MCH_BCLK	CLK_MCH_BCLK	AG2
7 CLK_MCH_BCLK#	CLK_MCH_BCLK#	AG1
H_CLKIN		H_CLKIN
H_CLKIN#		H_CLKIN#

H\_A#[3..31] H\_A#[3..31] 4

HOST

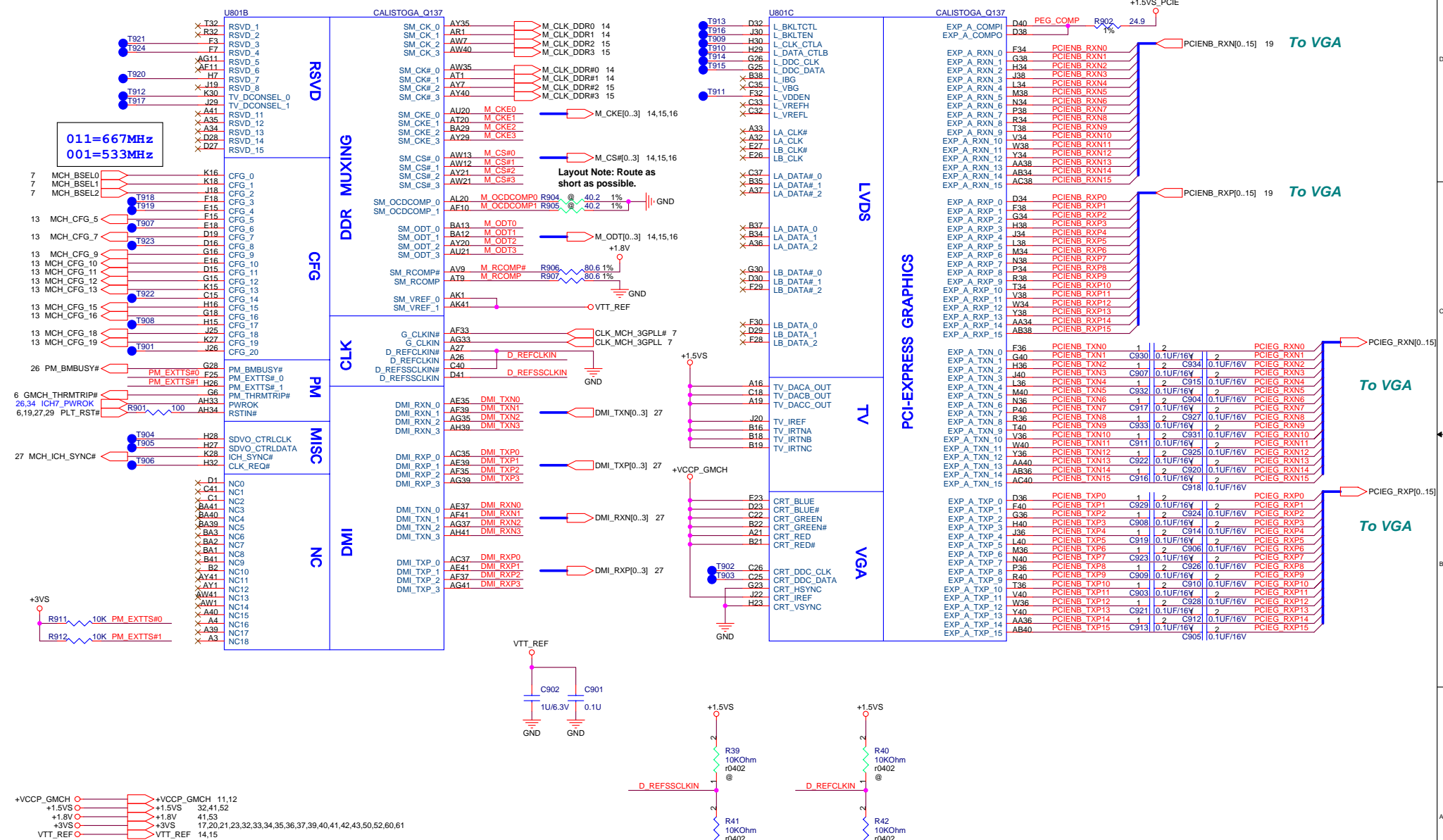
H_A#_3	H_A#3	H_A#_3
H_A#_4	C9	H_A#4
H_A#_5	E11	H_A#5
H_A#_6	G11	H_A#6
H_A#_7	F11	H_A#7
H_A#_8	G12	H_A#8
H_A#_9	F9	H_A#9
H_A#_10	H11	H_A#10
H_A#_11	J12	H_A#11
H_A#_12	G14	H_A#12
H_A#_13	D9	H_A#13
H_A#_14	J14	H_A#14
H_A#_15	H13	H_A#15
H_A#_16	J15	H_A#16
H_A#_17	F14	H_A#17
H_A#_18	A11	H_A#18
H_A#_19	C11	H_A#19
H_A#_20	A12	H_A#20
H_A#_21	A13	H_A#21
H_A#_22	E13	H_A#22
H_A#_23	G13	H_A#23
H_A#_24	F12	H_A#24
H_A#_25	B12	H_A#25
H_A#_26	B14	H_A#26
H_A#_27	C12	H_A#27
H_A#_28	A14	H_A#28
H_A#_29	C14	H_A#29
H_A#_30	D14	H_A#30
H_A#_31		H_A#31
E8	H_ADS#	H_ADS# 4
B9	H_ADSTB#0	H_ADSTB#0 4
C13	H_ADSTB#1	H_ADSTB#1 4
J13	H_VREF	H_VREF 4
C6	H_BNR#	H_BNR# 4
F6	H_BPR#	H_BPR# 4
C7	H_BR0#	H_BR0# 4
B7	H_CPURST#	H_CPURST# 4
A7	H_DBSY#	H_DBSY# 4
C3	H_DEFER#	H_DEFER# 4
J9	H_DPWR#	H_DPWR# 4
H8	H_DRDY#	H_DRDY# 4
K13		
J7	H_DINV#0	H_DINV#0 4
W8	H_DINV#1	H_DINV#1 4
U3	H_DINV#2	H_DINV#2 4
AB10	H_DINV#3	H_DINV#3 4
K4	H_DSTBN#0	H_DSTBN#0 4
T7	H_DSTBN#1	H_DSTBN#1 4
Y5	H_DSTBN#2	H_DSTBN#2 4
AC4	H_DSTBN#3	H_DSTBN#3 4
K3	H_DSTBP#0	H_DSTBP#0 4
T6	H_DSTBP#1	H_DSTBP#1 4
AA5	H_DSTBP#2	H_DSTBP#2 4
AC5	H_DSTBP#3	H_DSTBP#3 4
D3	H_HIT#	H_HIT# 4
D4	H_HITM#	H_HITM# 4
B3	H_LOCK#	H_LOCK# 4
D8	H_REQ#0	
G8	H_REQ#1	
B8	H_REQ#2	
F8	H_REQ#3	
A8	H_REQ#4	
B4	H_RS#0	
E6	H_RS#1	
D6	H_RS#2	
E3	H_SLPCPU#	
E7	H_TRDY#	
H_REQ#		H_REQ#[4..0] 4
H_RS#		H_RS#[0..2] 4
H_CPLSP#	R811 00hm	H_CPLSP# 4,25
H_TRDY#		H_TRDY# 4

### AGTL+ I/O Voltage Reference



H\_CPURST# T801





14 M\_A\_DQ[0..63]

15 M\_B\_DQ[0..63]

U801D

CALISTOGA Q137

U801E

CALISTOGA Q137

M_A DQ0	AJ35	SA_DQ0
M_A DQ1	AJ34	SA_DQ1
M_A DQ2	AM31	SA_DQ2
M_A DQ3	AM33	SA_DQ3
M_A DQ4	AJ36	SA_DQ4
M_A DQ5	AK35	SA_DQ5
M_A DQ6	AJ32	SA_DQ6
M_A DQ7	AH31	SA_DQ7
M_A DQ8	AN35	SA_DQ8
M_A DQ9	AP33	SA_DQ9
M_A DQ10	AR31	SA_DQ10
M_A DQ11	AP31	SA_DQ11
M_A DQ12	AN38	SA_DQ12
M_A DQ13	AM36	SA_DQ13
M_A DQ14	AM34	SA_DQ14
M_A DQ15	AN33	SA_DQ15
M_A DQ16	AK26	SA_DQ16
M_A DQ17	AL27	SA_DQ17
M_A DQ18	AM26	SA_DQ18
M_A DQ19	AN24	SA_DQ19
M_A DQ20	AK28	SA_DQ20
M_A DQ21	AL28	SA_DQ21
M_A DQ22	AM24	SA_DQ22
M_A DQ23	AP26	SA_DQ23
M_A DQ24	AP23	SA_DQ24
M_A DQ25	AL22	SA_DQ25
M_A DQ26	AP21	SA_DQ26
M_A DQ27	AN20	SA_DQ27
M_A DQ28	AL23	SA_DQ28
M_A DQ29	AP24	SA_DQ29
M_A DQ30	AP20	SA_DQ30
M_A DQ31	AT21	SA_DQ31
M_A DQ32	AR12	SA_DQ32
M_A DQ33	AR14	SA_DQ33
M_A DQ34	AP13	SA_DQ34
M_A DQ35	AP12	SA_DQ35
M_A DQ36	AT13	SA_DQ36
M_A DQ37	AT12	SA_DQ37
M_A DQ38	AL14	SA_DQ38
M_A DQ39	AL12	SA_DQ39
M_A DQ40	AK9	SA_DQ40
M_A DQ41	AN7	SA_DQ41
M_A DQ42	AK8	SA_DQ42
M_A DQ43	AK7	SA_DQ43
M_A DQ44	AP9	SA_DQ44
M_A DQ45	AN9	SA_DQ45
M_A DQ46	AT5	SA_DQ46
M_A DQ47	AL5	SA_DQ47
M_A DQ48	AY2	SA_DQ48
M_A DQ49	AW2	SA_DQ49
M_A DQ50	AP1	SA_DQ50
M_A DQ51	AN2	SA_DQ51
M_A DQ52	AY2	SA_DQ52
M_A DQ53	AT3	SA_DQ53
M_A DQ54	AN1	SA_DQ54
M_A DQ55	AL2	SA_DQ55
M_A DQ56	AG7	SA_DQ56
M_A DQ57	AF9	SA_DQ57
M_A DQ58	AG4	SA_DQ58
M_A DQ59	AF6	SA_DQ59
M_A DQ60	AG9	SA_DQ60
M_A DQ61	AH6	SA_DQ61
M_A DQ62	AF4	SA_DQ62
M_A DQ63	AF8	SA_DQ63

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M_A_BS#0 14,16
SA_BS_1	AV14	M_A_BS#1 14,16
SA_BS_2	BA20	M_A_BS#2 14,16
SA_BS_2	AY13	M_A_CAS# 14,16
SA_DM_0	AJ33	M_A_DM0
SA_DM_1	AM35	M_A_DM1
SA_DM_2	AL26	M_A_DM2
SA_DM_3	AN22	M_A_DM3
SA_DM_4	AM14	M_A_DM4
SA_DM_5	AL9	M_A_DM5
SA_DM_6	AR3	M_A_DM6
SA_DM_7	AH4	M_A_DM7
SA_DQS_0	AK33	M_A_DQS0
SA_DQS_1	AT33	M_A_DQS1
SA_DQS_2	AN28	M_A_DQS2
SA_DQS_3	AM22	M_A_DQS3
SA_DQS_4	AN12	M_A_DQS4
SA_DQS_5	AN8	M_A_DQS5
SA_DQS_6	AP3	M_A_DQS6
SA_DQS_7	AG5	M_A_DQS7
SA_DQS#_0	AK32	M_A_DQS#0
SA_DQS#_1	AU33	M_A_DQS#1
SA_DQS#_2	AN27	M_A_DQS#2
SA_DQS#_3	AM21	M_A_DQS#3
SA_DQS#_4	AM12	M_A_DQS#4
SA_DQS#_5	AL8	M_A_DQS#5
SA_DQS#_6	AN3	M_A_DQS#6
SA_DQS#_7	AH5	M_A_DQS#7
SA_MA_0	AY16	M_A_A0
SA_MA_1	AU14	M_A_A1
SA_MA_2	AW16	M_A_A2
SA_MA_3	BA16	M_A_A3
SA_MA_4	BA17	M_A_A4
SA_MA_5	AU16	M_A_A5
SA_MA_6	AV17	M_A_A6
SA_MA_7	AU17	M_A_A7
SA_MA_8	AW17	M_A_A8
SA_MA_9	AT16	M_A_A9
SA_MA_10	AU13	M_A_A10
SA_MA_11	AT17	M_A_A11
SA_MA_12	AV20	M_A_A12
SA_MA_13	AV12	M_A_A13
SA_RAS#	AW14	M_A_RAS# 14,16
SA_RCVENIN#	AK23	T1001
SA_RCVENIN#	AK24	T1003
SA_WE#	AY14	M_A_WE# 14,16

M\_A\_A[0..13] 14,16

M\_A\_RAS# 14,16

M\_A\_WE# 14,16

M_B DQ0	AK39	SB_DQ0
M_B DQ1	AJ37	SB_DQ1
M_B DQ2	AP39	SB_DQ2
M_B DQ3	AR41	SB_DQ3
M_B DQ4	AJ38	SB_DQ4
M_B DQ5	AK38	SB_DQ5
M_B DQ6	AN41	SB_DQ6
M_B DQ7	AR41	SB_DQ7
M_B DQ8	AT40	SB_DQ8
M_B DQ9	AV41	SB_DQ9
M_B DQ10	AU38	SB_DQ10
M_B DQ11	AV38	SB_DQ11
M_B DQ12	AP38	SB_DQ12
M_B DQ13	AR40	SB_DQ13
M_B DQ14	AW38	SB_DQ14
M_B DQ15	AV38	SB_DQ15
M_B DQ16	BA38	SB_DQ16
M_B DQ17	AV36	SB_DQ17
M_B DQ18	AR36	SB_DQ18
M_B DQ19	AP36	SB_DQ19
M_B DQ20	BA36	SB_DQ20
M_B DQ21	AU36	SB_DQ21
M_B DQ22	AP35	SB_DQ22
M_B DQ23	AP34	SB_DQ23
M_B DQ24	BA33	SB_DQ24
M_B DQ25	BA33	SB_DQ25
M_B DQ26	AT31	SB_DQ26
M_B DQ27	AU29	SB_DQ27
M_B DQ28	AU31	SB_DQ28
M_B DQ29	AV31	SB_DQ29
M_B DQ30	AV29	SB_DQ30
M_B DQ31	AW29	SB_DQ31
M_B DQ32	AM19	SB_DQ32
M_B DQ33	AL19	SB_DQ33
M_B DQ34	AP14	SB_DQ34
M_B DQ35	AN14	SB_DQ35
M_B DQ36	AN17	SB_DQ36
M_B DQ37	AM16	SB_DQ37
M_B DQ38	AP15	SB_DQ38
M_B DQ39	AL15	SB_DQ39
M_B DQ40	AJ11	SB_DQ40
M_B DQ41	AH10	SB_DQ41
M_B DQ42	AJ9	SB_DQ42
M_B DQ43	AN10	SB_DQ43
M_B DQ44	AK13	SB_DQ44
M_B DQ45	AH11	SB_DQ45
M_B DQ46	AK10	SB_DQ46
M_B DQ47	AJ8	SB_DQ47
M_B DQ48	BA10	SB_DQ48
M_B DQ49	AW10	SB_DQ49
M_B DQ50	BA4	SB_DQ50
M_B DQ51	AW4	SB_DQ51
M_B DQ52	AY10	SB_DQ52
M_B DQ53	AY9	SB_DQ53
M_B DQ54	AW5	SB_DQ54
M_B DQ55	AY5	SB_DQ55
M_B DQ56	AW4	SB_DQ56
M_B DQ57	AR5	SB_DQ57
M_B DQ58	AK4	SB_DQ58
M_B DQ59	AK3	SB_DQ59
M_B DQ60	AT4	SB_DQ60
M_B DQ61	AK5	SB_DQ61
M_B DQ62	AJ5	SB_DQ62
M_B DQ63	AJ3	SB_DQ63


DDR SYSTEM MEMORY B

SB_BS_0	AT24	M_B_BS#0 15,16
SB_BS_1	AV23	M_B_BS#1 15,16
SB_BS_2	AY28	M_B_BS#2 15,16
SB_BS_2	AR24	M_B_CAS# 15,16
SB_DM_0	AK36	M_B_DM0
SB_DM_1	AR38	M_B_DM1
SB_DM_2	AT36	M_B_DM2
SB_DM_3	BA31	M_B_DM3
SB_DM_4	AL17	M_B_DM4
SB_DM_5	AH8	M_B_DM5
SB_DM_6	BA5	M_B_DM6
SB_DM_7	AN4	M_B_DM7
SB_DQS_0	AM39	M_B_DQS0
SB_DQS_1	AT39	M_B_DQS1
SB_DQS_2	AU35	M_B_DQS2
SB_DQS_3	AR29	M_B_DQS3
SB_DQS_4	AR16	M_B_DQS4
SB_DQS_5	AR10	M_B_DQS5
SB_DQS_6	AR7	M_B_DQS6
SB_DQS_7	AN5	M_B_DQS7
SB_DQS#_0	AM40	M_B_DQS#0
SB_DQS#_1	AU39	M_B_DQS#1
SB_DQS#_2	AT35	M_B_DQS#2
SB_DQS#_3	AP29	M_B_DQS#3
SB_DQS#_4	AP16	M_B_DQS#4
SB_DQS#_5	AT10	M_B_DQS#5
SB_DQS#_6	AT7	M_B_DQS#6
SB_DQS#_7	AP5	M_B_DQS#7
SB_MA_0	AY23	M_B_A0
SB_MA_1	AW24	M_B_A1
SB_MA_2	AY24	M_B_A2
SB_MA_3	AR28	M_B_A3
SB_MA_4	AT27	M_B_A4
SB_MA_5	AT28	M_B_A5
SB_MA_6	AU27	M_B_A6
SB_MA_7	AV28	M_B_A7
SB_MA_8	AW27	M_B_A8
SB_MA_9	AV27	M_B_A9
SB_MA_10	AV24	M_B_A10
SB_MA_11	BA27	M_B_A11
SB_MA_12	AY27	M_B_A12
SB_MA_13	AR23	M_B_A13
SB_RAS#	AU23	M_B_RAS# 15,16
SB_RCVENIN#	AK16	T1002
SB_RCVENIN#	AK18	T1004
SB_WE#	AR27	M_B_WE# 15,16

M\_B\_A[0..13] 15,16

M\_B\_RAS# 15,16

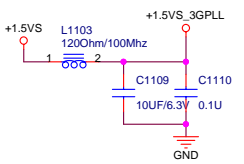
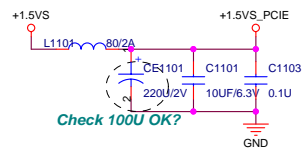
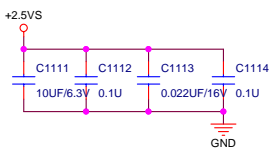
M\_B\_WE# 15,16

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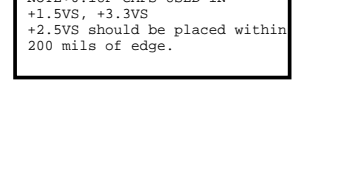
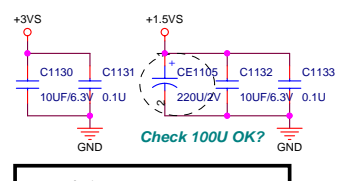
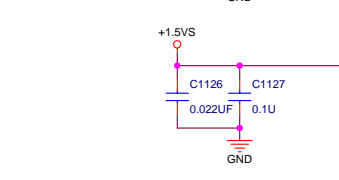
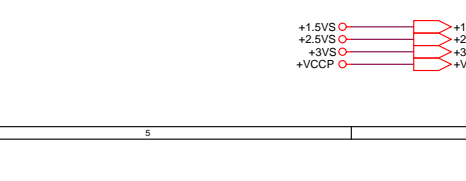
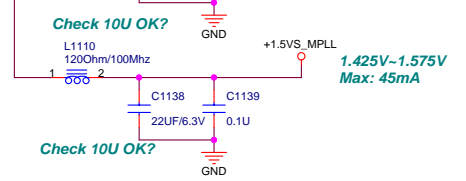
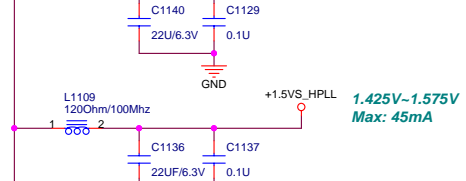
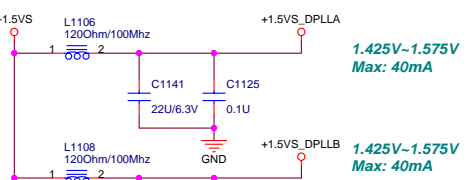
4 FL., No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

Title: **Calistoga--DDR2**

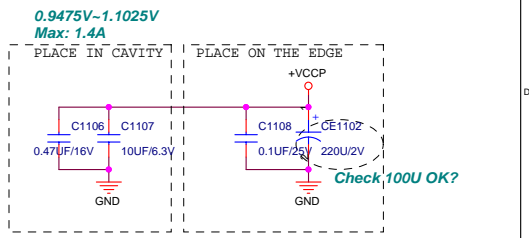
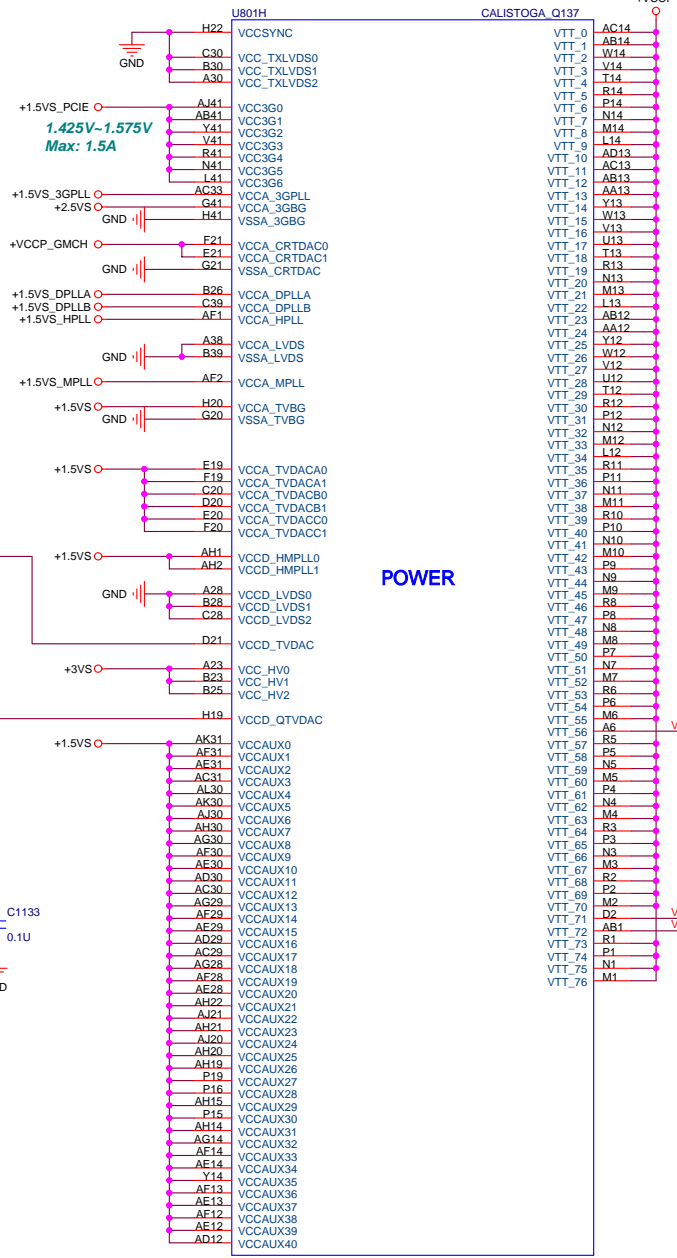
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Date: Thursday, April 27, 2006	Sheet	10 of 22



NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.



NOTE: 0.1uF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.



POWER

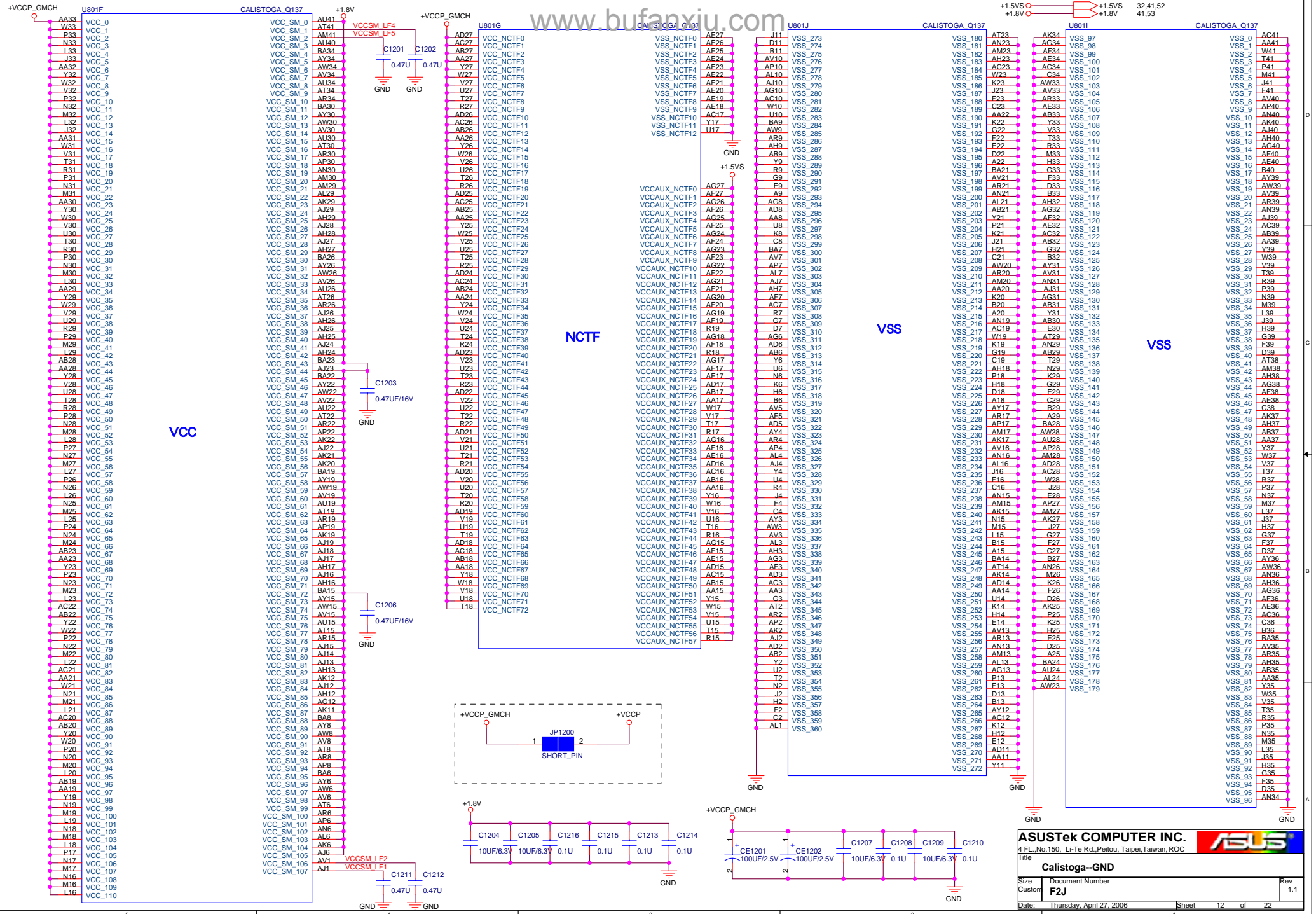
+1.5VS	+1.5VS	32,41,52
+2.5VS	+2.5VS	17,20,41,54
+3VS	+3VS	17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61
+VCCP	+VCCP	12,41,52

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Title: **Calistoga--PWR**

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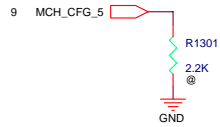
**ASUSTek COMPUTER INC.**  
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Title: **Calistoga--GND**

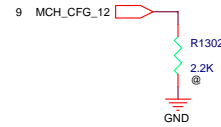
Size: F2J  
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Document Number: [Blank]  
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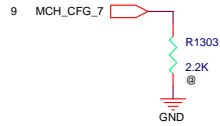


**CFG5 : DMI STRAP**  
 LOW = DMI X 2  
**HIGH = DMI X 4 (Default)**

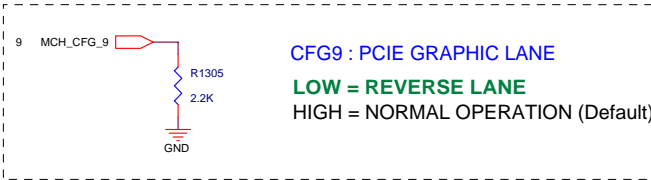


**CFG[13:12] : GMCH TEST MODE SELECT**

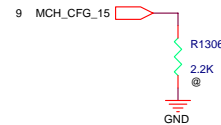
00 = Partial CLK gating disable  
 01 = XOR Mode Enable  
 10 = ALL Z Mode Enable  
**11 = NORMAL OPERATION (Default)**



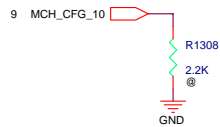
**CFG7 : CPU STRAP**  
 LOW = RESERVED  
**HIGH = Mobile Yonah CPU (Default)**



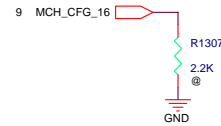
**CFG9 : PCIE GRAPHIC LANE**  
**LOW = REVERSE LANE**  
 HIGH = NORMAL OPERATION (Default)



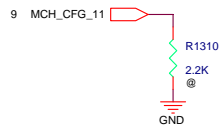
**CFG15 : ICH RESET Disable**  
 LOW = ICH RESET Disabled  
**HIGH = Normal Operation (Default)**



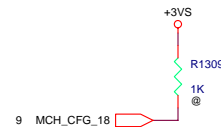
**CFG10 : HOST PLL VCO SELECT**  
 LOW = RESERVED  
**HIGH = MOBILITY (Default)**



**CFG16 : FSB Dynamic ODT**  
 LOW = Dynamic ODT Disabled  
**HIGH = Dynamic ODT Enabled (Default)**

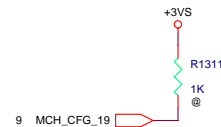


**CFG11 : PSB 4x CLK ENABLE**  
 LOW = 4X ENABLED  
**HIGH = 8X ENABLED (Default)**



**CFG18 : GMCH Core Voltage Level**  
**LOW = 1.05V (Default)**  
 HIGH = 1.5V

CFG[17..3] have internal pullup resistors.  
 CFG[19..18] have internal pulldown resistors.  
 SDVOCRTL\_DATA has internal pulldown resistors.

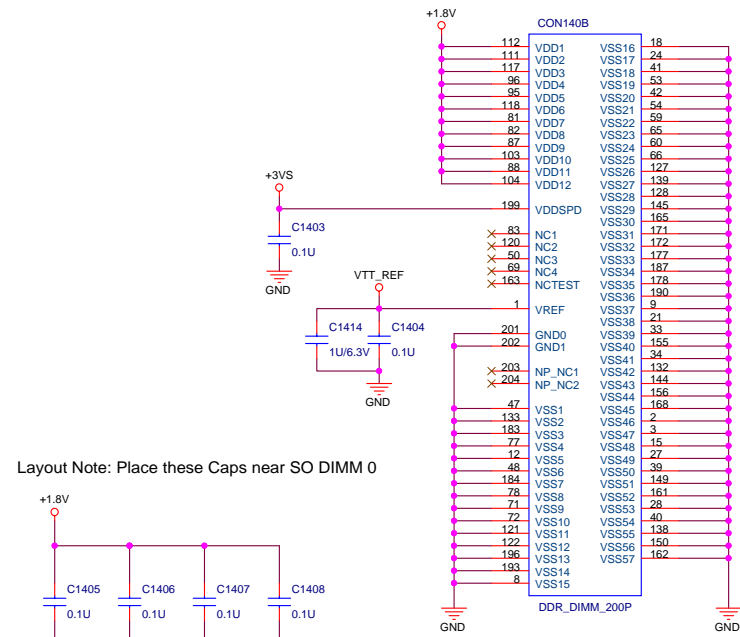
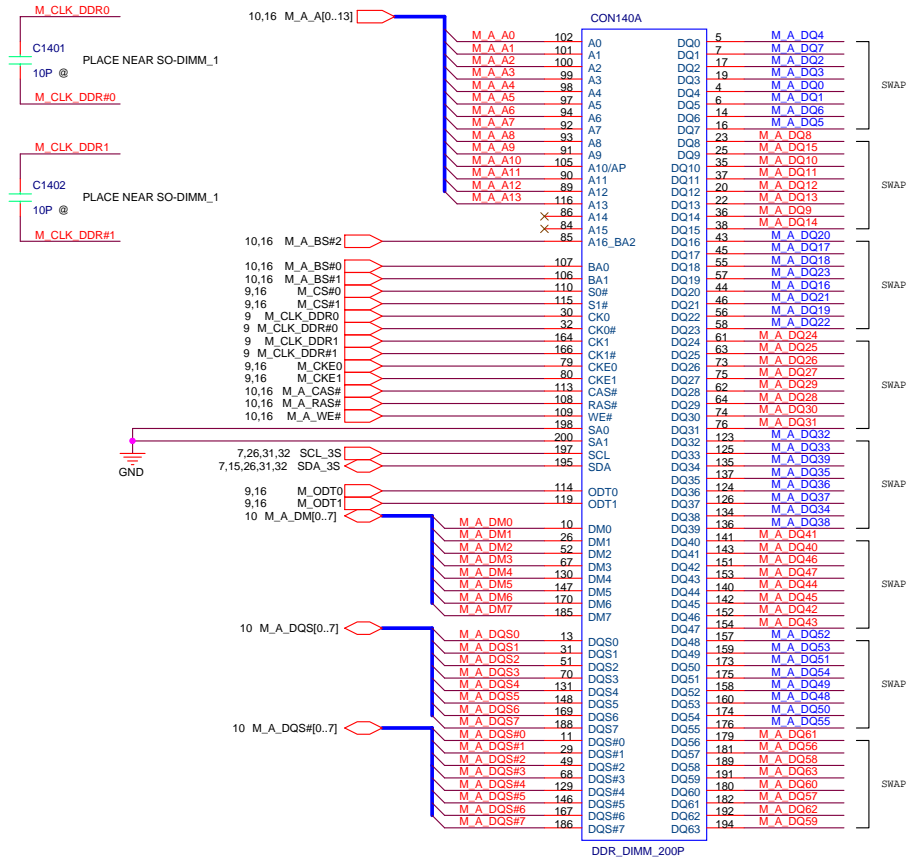


**CFG19 : DMI LANE REVERSAL**  
**LOW = NORMAL (Default)**  
 HIGH = LANES REVERSED

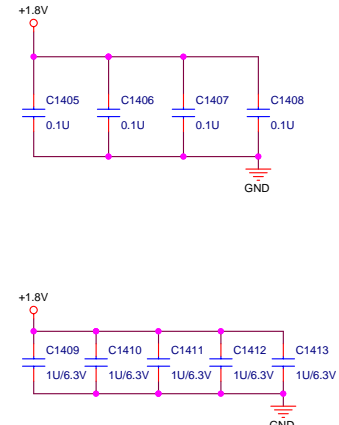
# STANDARD TYPE

P/N change to FOXCON??---->L2G025122000

+1.8V  $\rightarrow$  +1.8V 41,53  
+3VS  $\rightarrow$  +3VS 17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61



Layout Note: Place these Caps near SO DIMM 0



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Title: **DDR2 SO-DIMM0**

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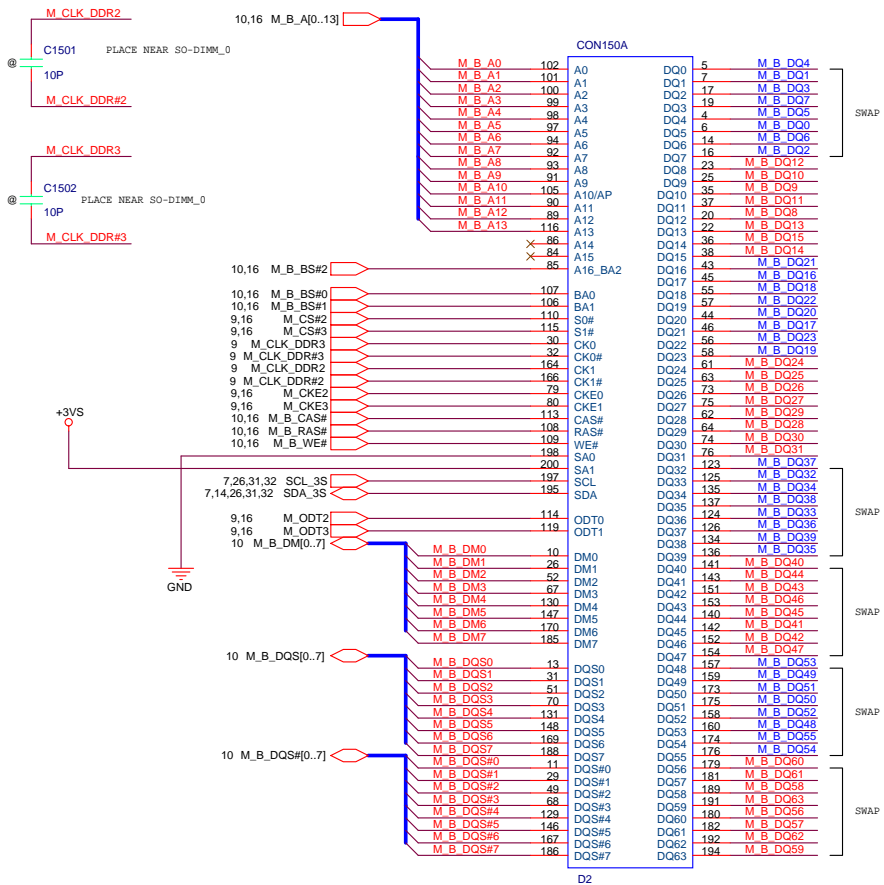
# REVERS TYPE

P/N change to FOXCON??---->12G025332003

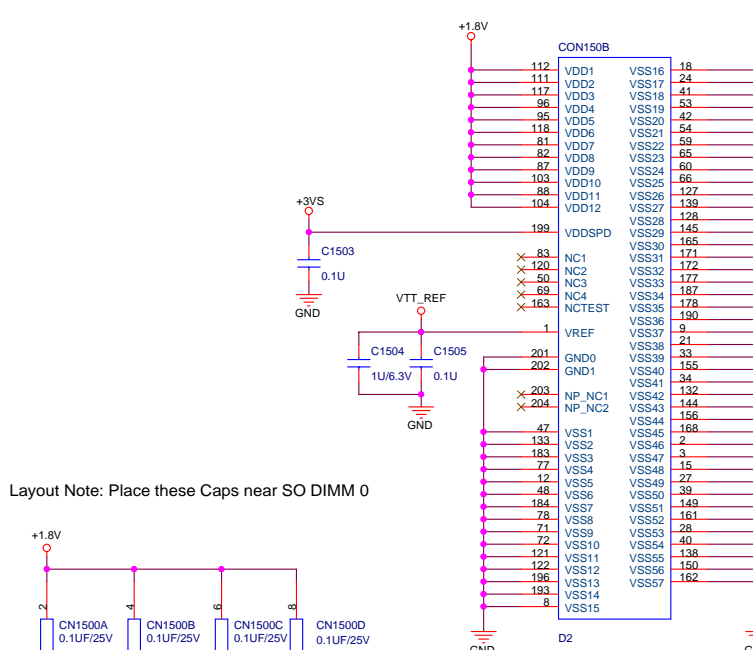
10 M\_B\_DQ[0..63] M\_B\_DQ[0..63]

+1.8V  
+3VS  
+5V

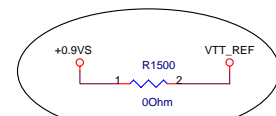
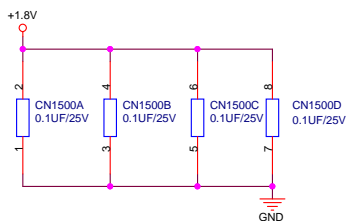
41,53  
17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61  
32,41,59,61



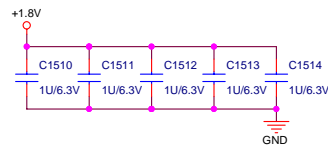
P/N: 12G025122006



Layout Note: Place these Caps near SO DIMM 0



Note: A5 & W1 add Bead (120 ohm/100MHz).



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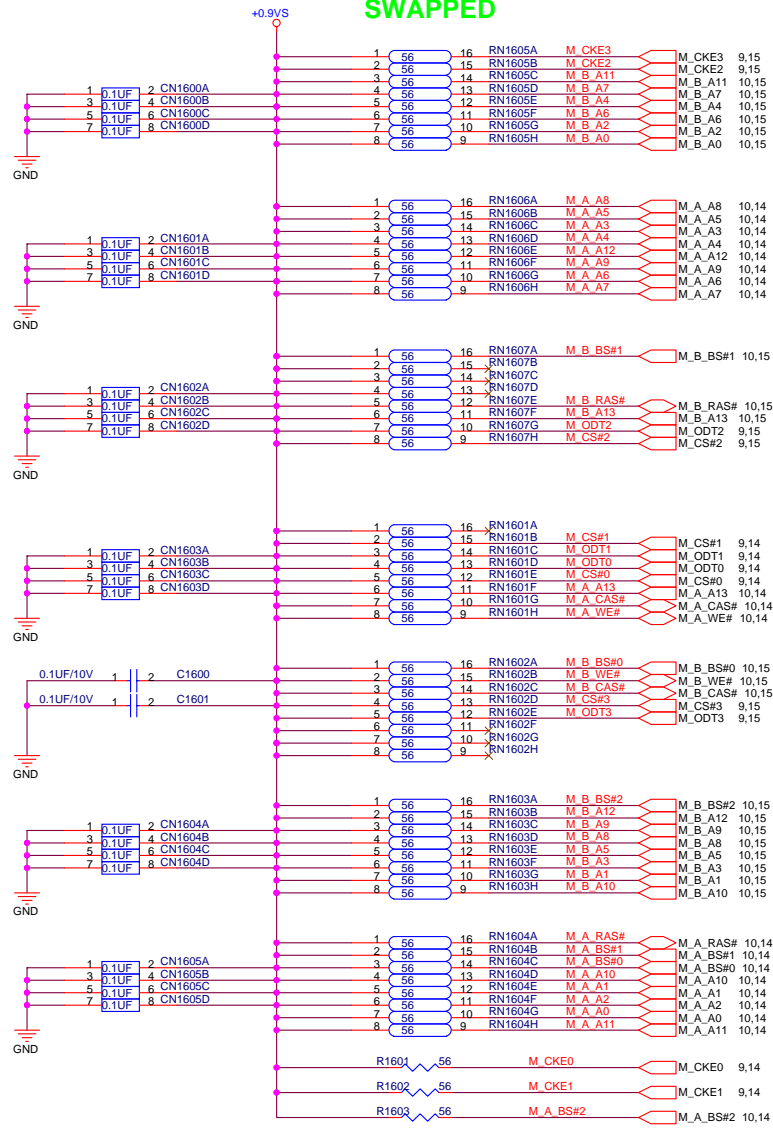
4 FL. No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

Title: **DDR2 SO-DIMM1**

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SWAPPED

+0.9VS  $\rightarrow$  +0.9VS 15.22.41.53

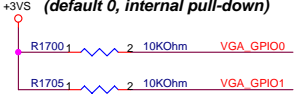


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

Title			Rev
DDR2 ADDRESS TERMINATION			1.1
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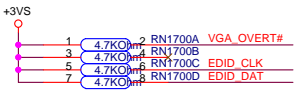


**GPIO[0]: Tx Power Savings Enable**  
**0: 50% Tx output swing**  
**1: full Tx output swing (recommended)**  
**(default 0, internal pull-down)**

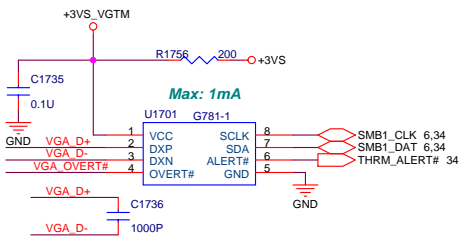


**GPIO[1]: Tx De-emphasis Enable**  
**0: Tx de-emphasis disable**  
**1: Tx de-emphasis enable**  
**(default 0, internal pull-down)**

R1.1---ITEM42

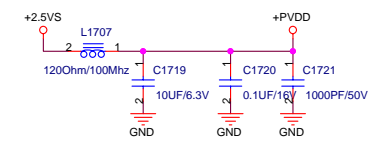
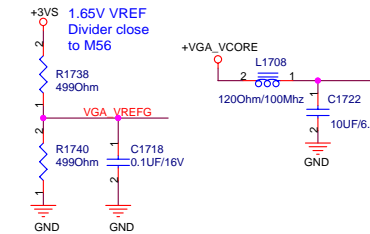
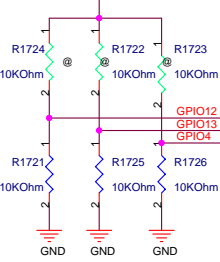


Slave Address: 9A

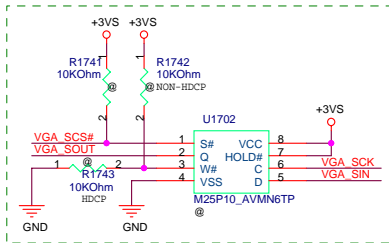


**Memory Aperture Size Select:**

**GPIO[13:12] = 00: 128M memory aperture, same as ROM strap 00**  
**GPIO[13:12] = 01: 256M memory aperture, same as ROM strap 01**  
**GPIO4 Debug Access:**  
**0 = OFF, 1 = ON**

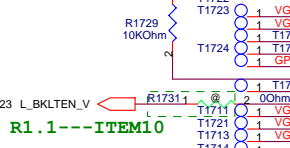
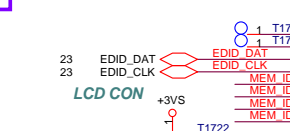
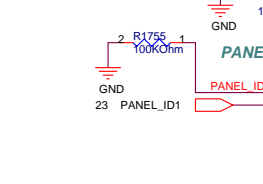


R1.1---ITEM13

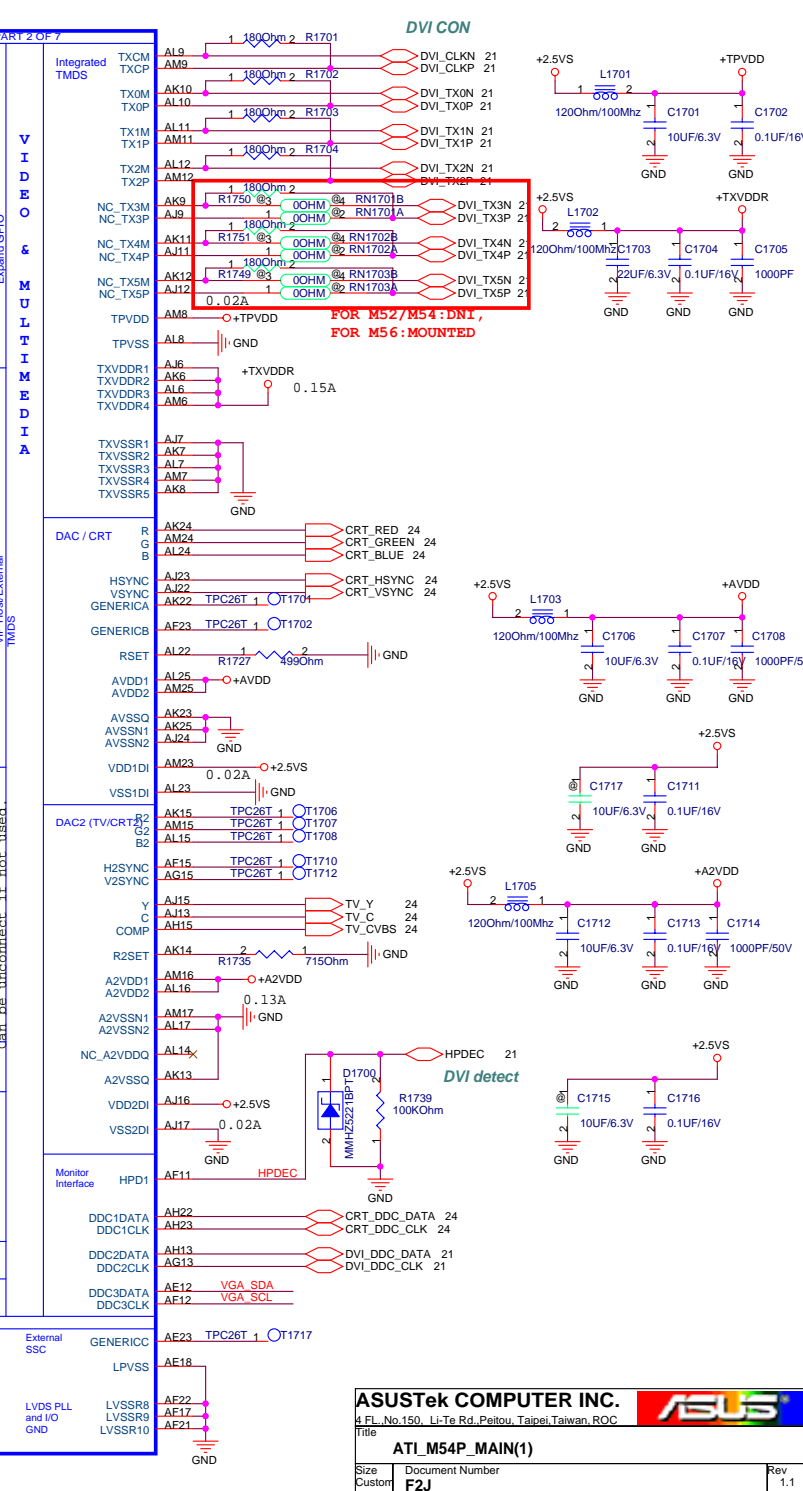
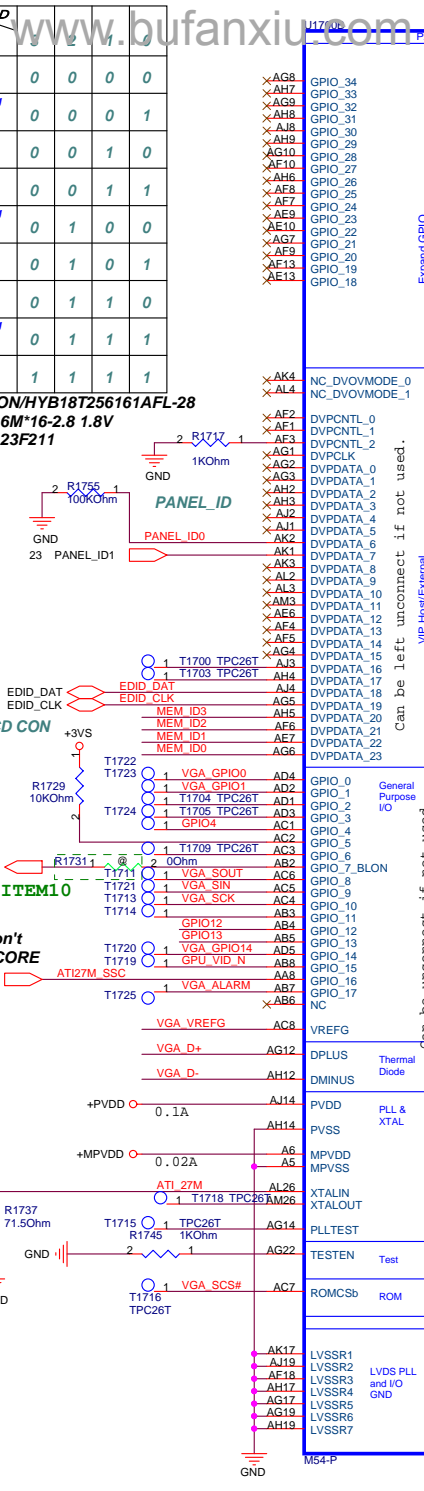


Vendor	SIZE	1	2	3	4
Infineon	128M	0	0	0	0
Samsung	128M	0	0	0	1
Hynix	128M	0	0	1	0
Infineon	256M	0	0	1	1
Samsung	256M	0	1	0	0
Hynix	256M	0	1	0	1
Infineon	64M	0	1	1	0
Samsung	64M	0	1	1	1
Hynix	64M	1	1	1	1

**INFINEON/HYB18T256161AF-L28**  
**DDR2 16M\*16-2.8 1.8V**  
**03G15123F211**



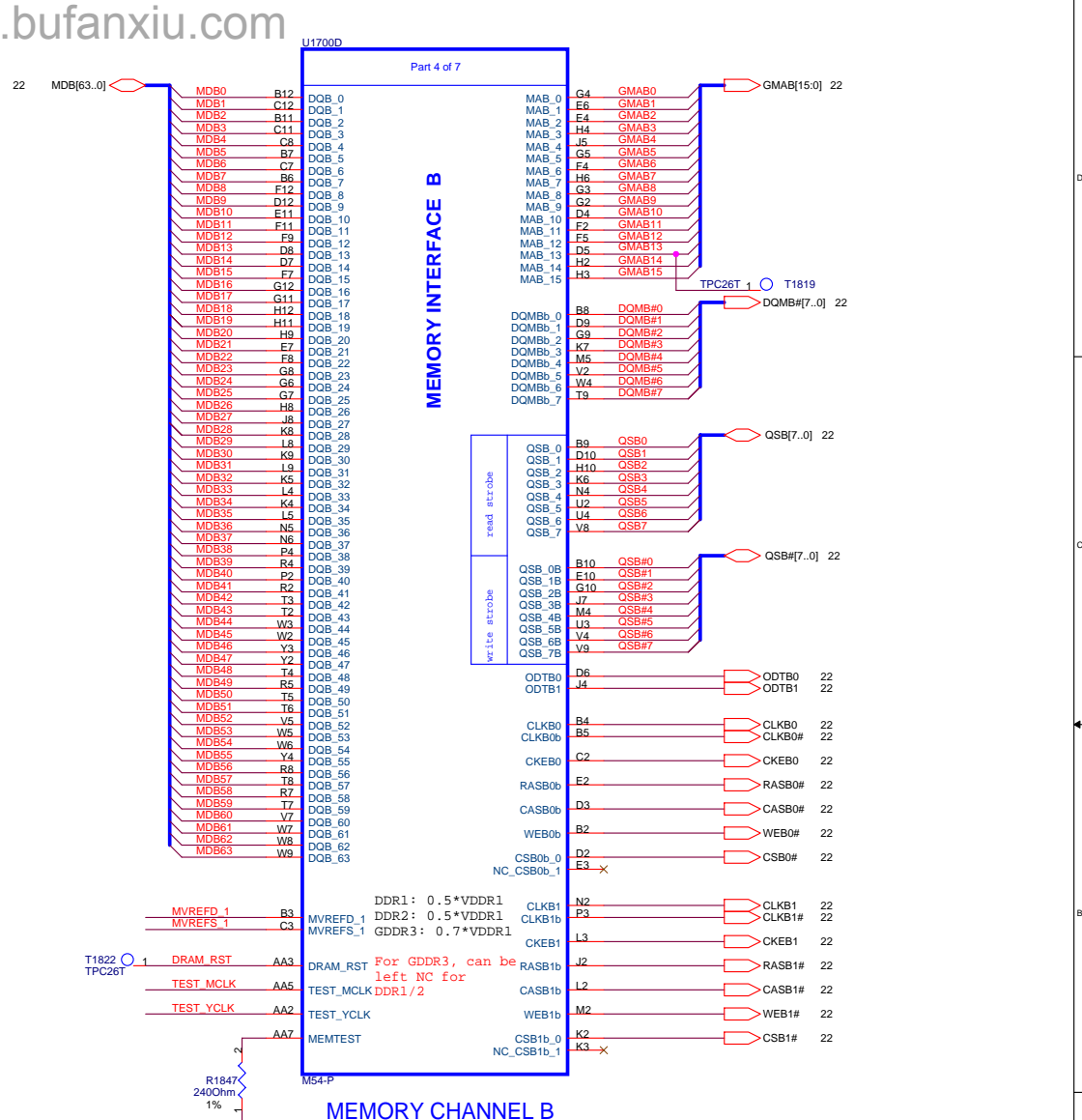
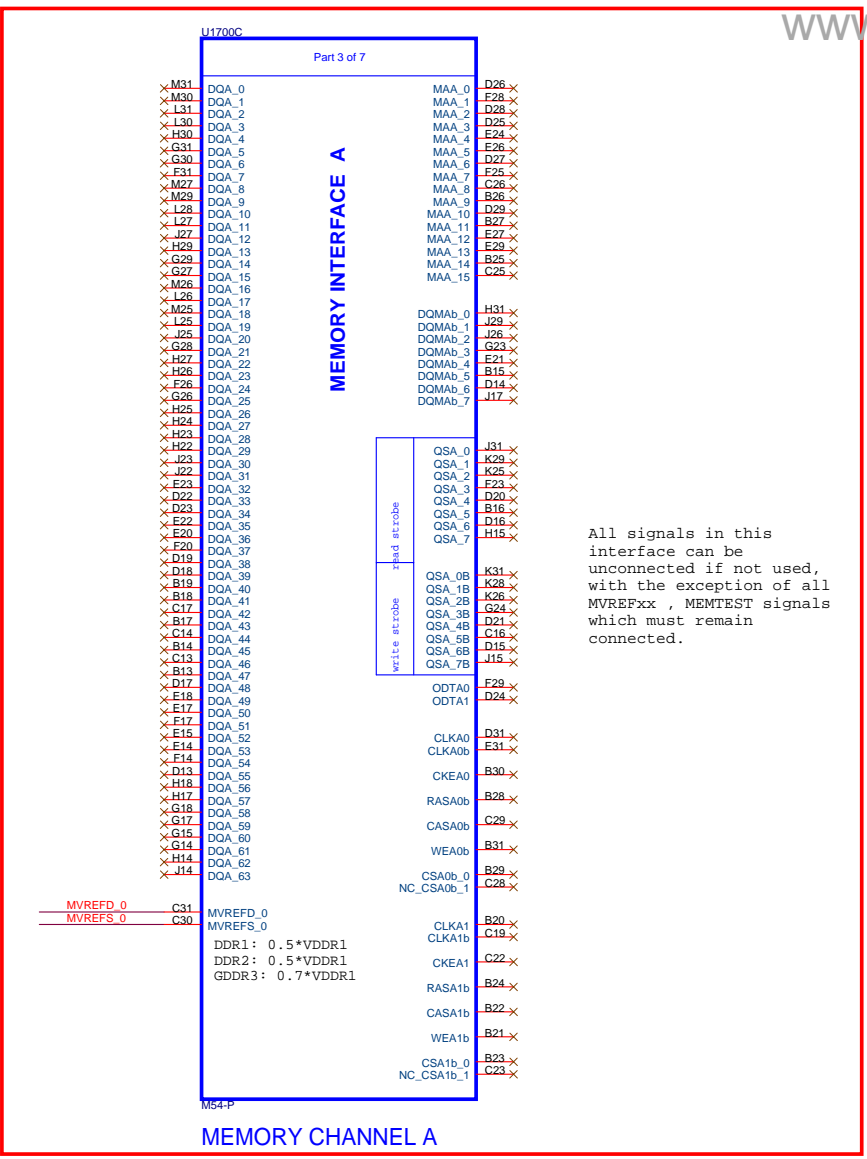
**POWER PLAY Don't Switch the VGA CORE**



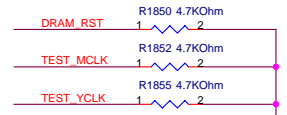
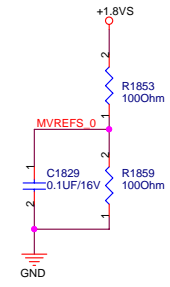
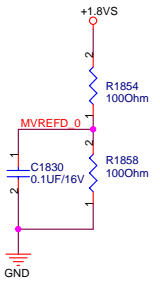
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**ATI\_M54P\_MAIN(1)**

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All signals in this interface can be unconnected if not used, with the exception of all MVREFxx, MEMTEST signals which must remain connected.



GDDR3: 0.7 \* VDDR1  
DDR1/2: 0.5 \* VDDR1

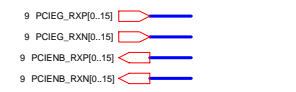
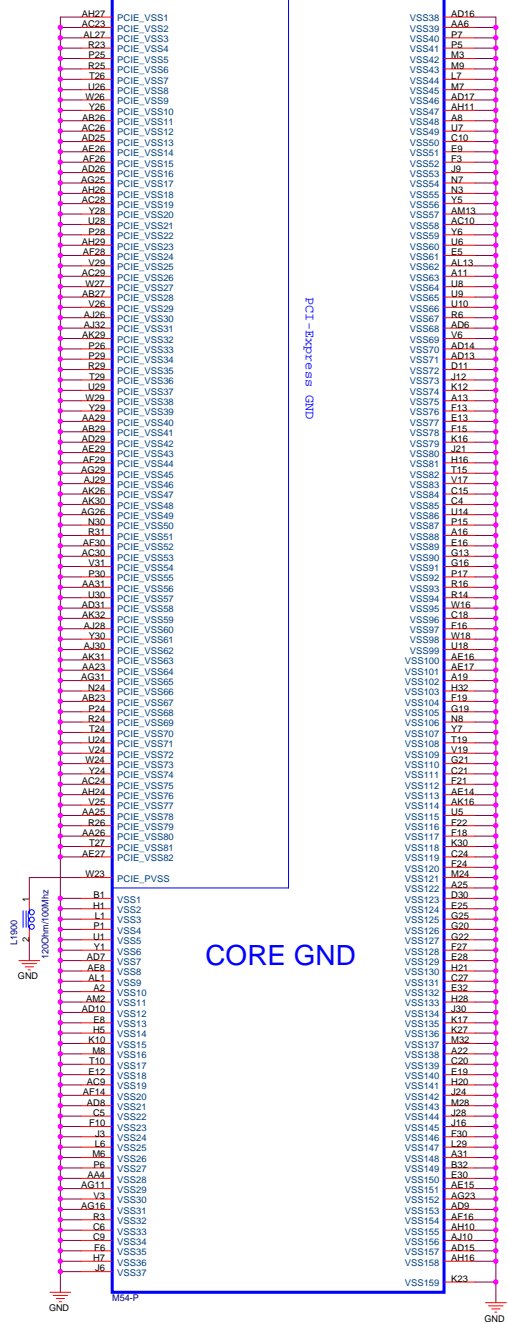
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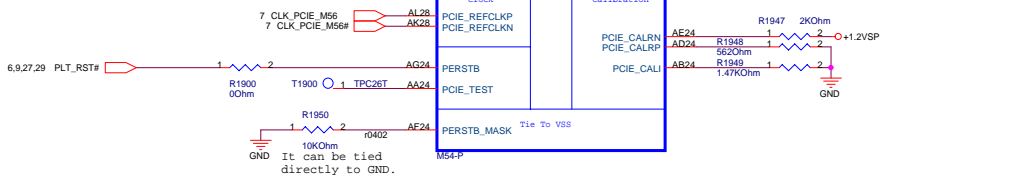
File: **ATI\_M54P\_MAIN(2)**

Size	Document Number	Rev
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U1700F Part 6 of 7

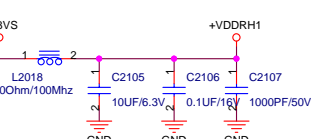
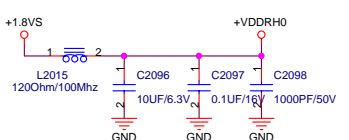
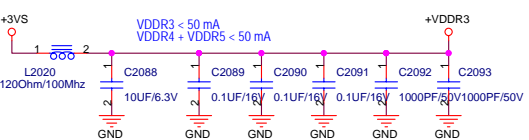
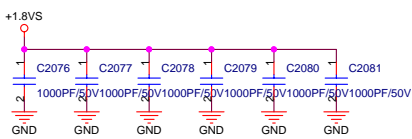
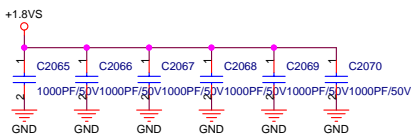
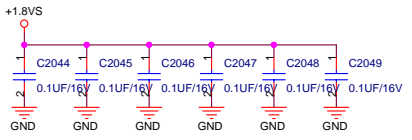
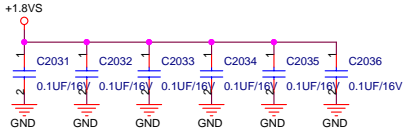
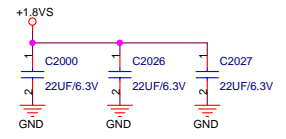


U1700A PART 1 OF 7



PCI-Express Bus: polarity inversion Lane Reversal

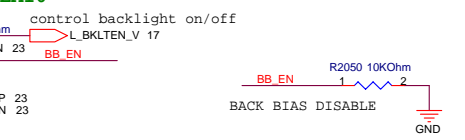
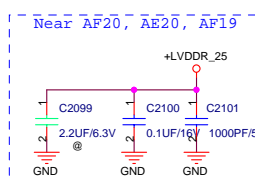
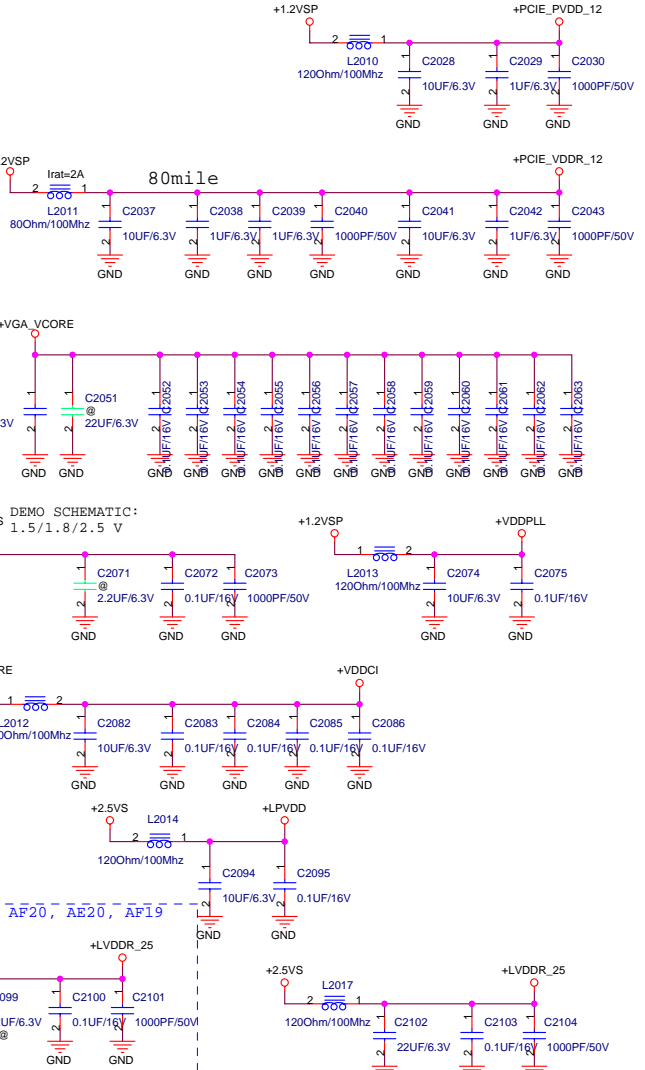
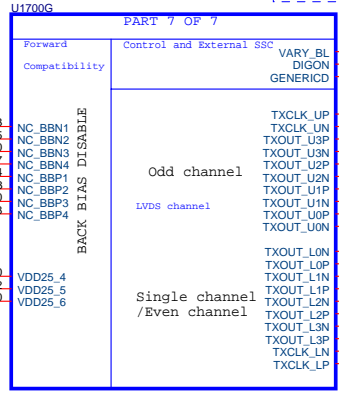
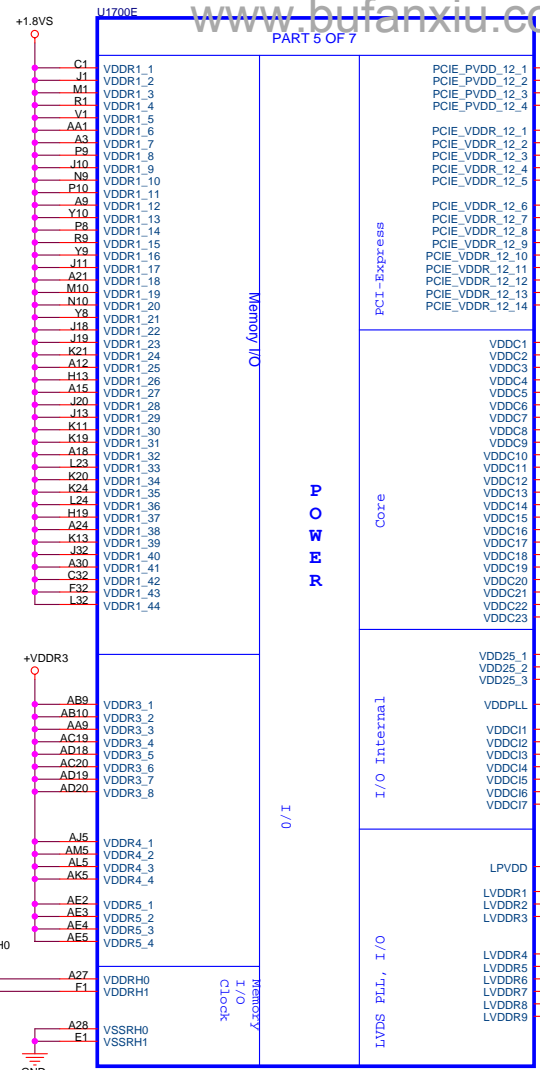
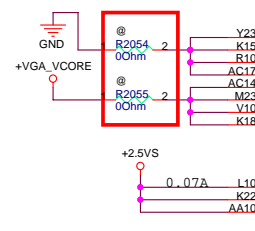
GDDR3/DDR1: 1.8V  
 DDR2: 1.8 ~ 2 V  
 GDDR3: 2A  
 DDR1: 0.8A



**+BBP>=VGA\_CORE**  
**-BBP<= 0V**

**BB\_EN=0 : -BBN=0V , +BBP =VGA\_CORE**  
**BB\_EN=1 : -BBN=-0.5V , +BBP = +1.8V (M56 B13:+1.5V)**

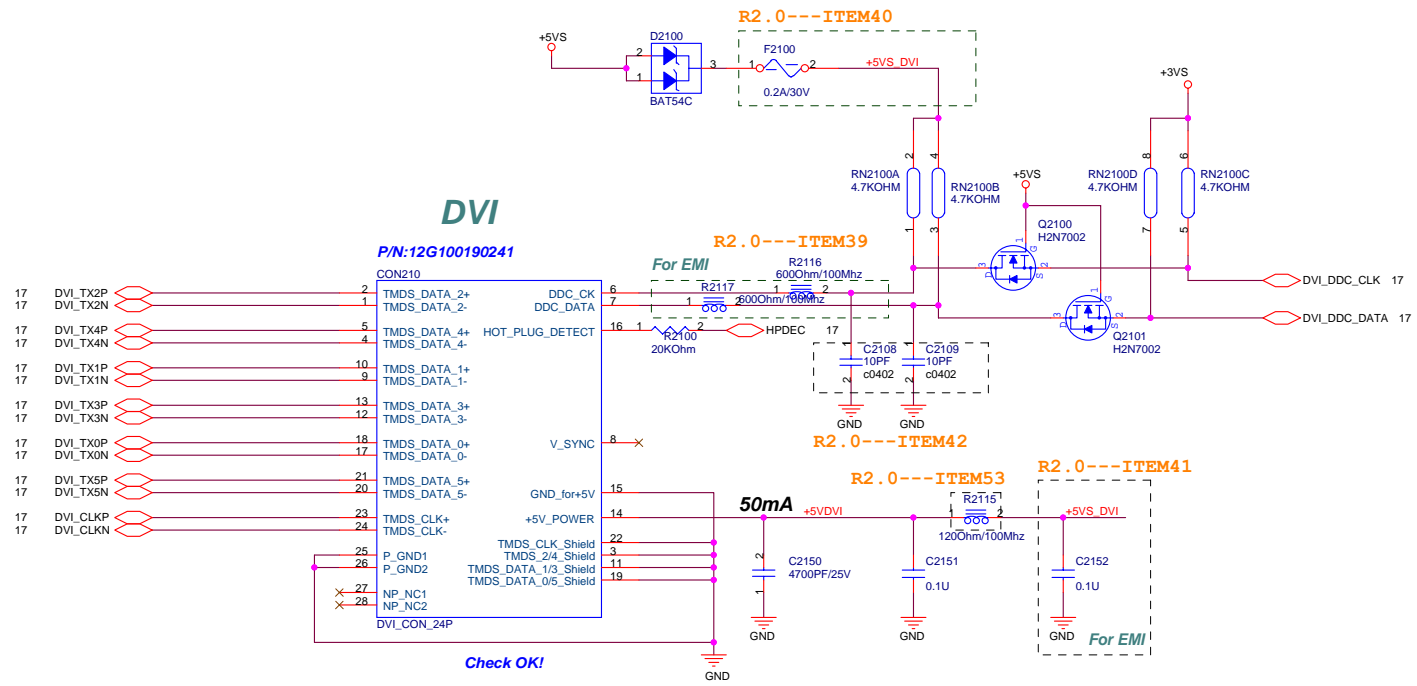
**FOR M52/M54 : DNI ,  
 FOR M56 : MOUNTED**



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**ATI\_M54P\_MAIN(4)**

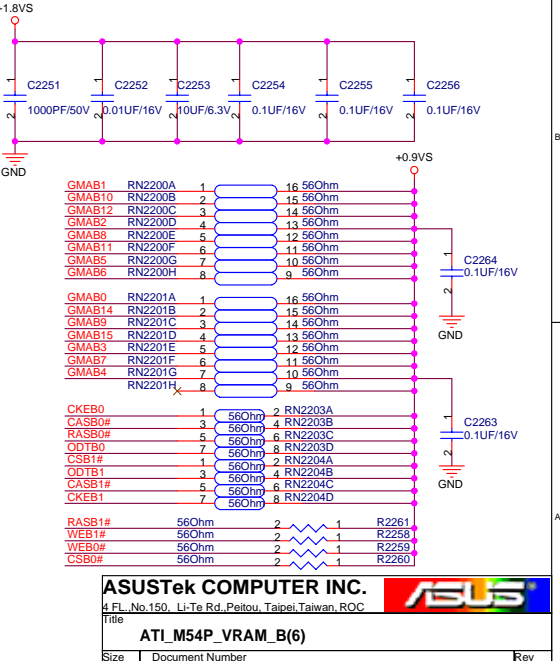
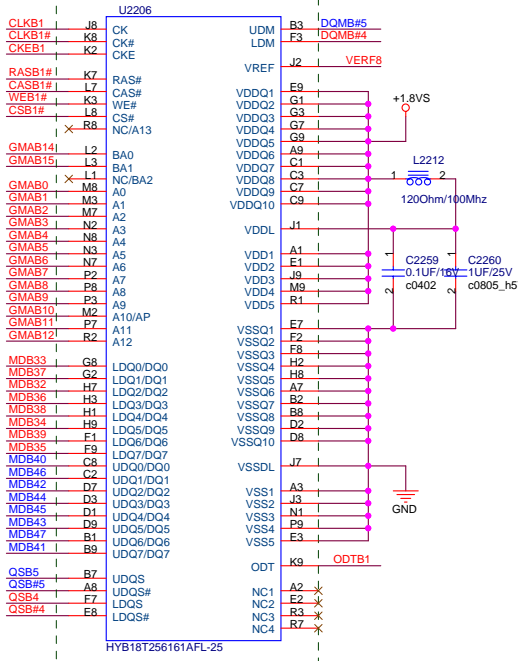
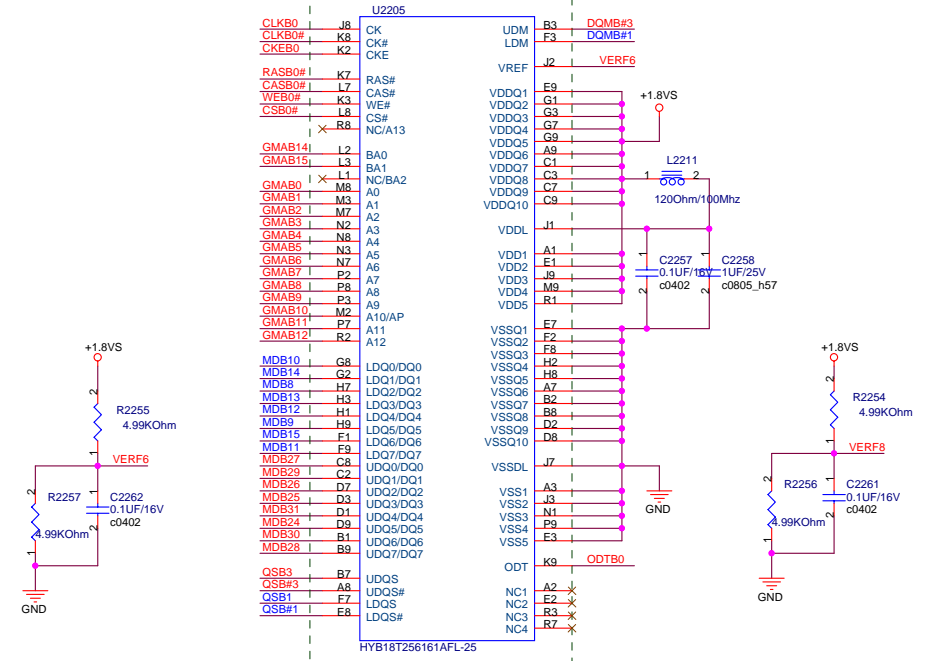
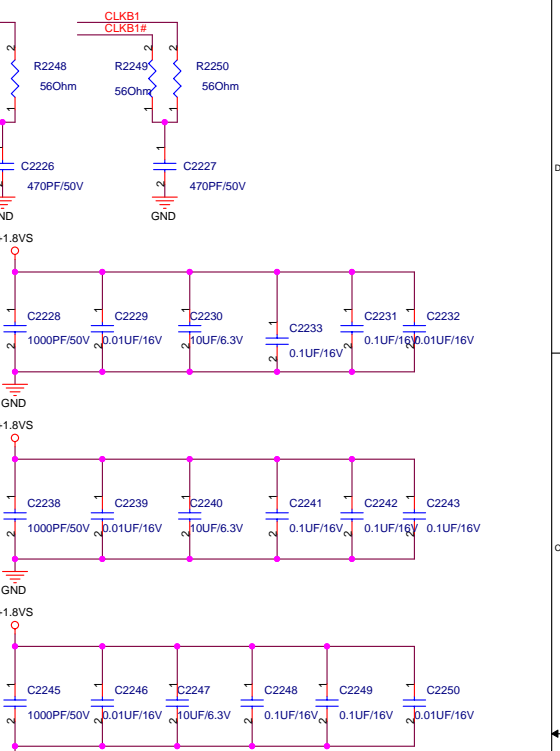
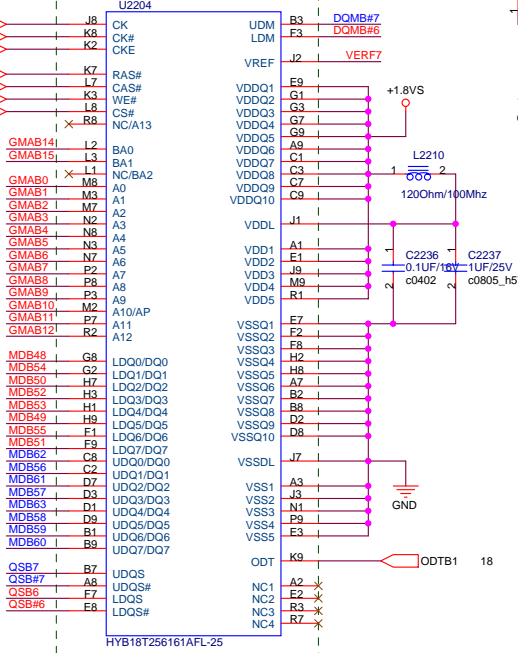
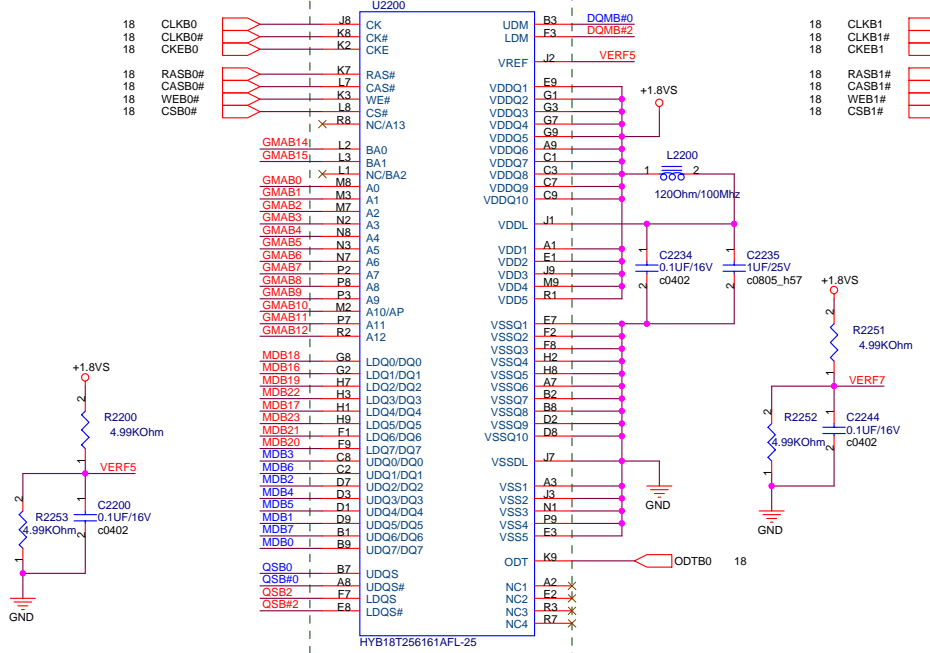
Size Custom Document Number **F2J** Rev 1.1  
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- 18 GMAB[15..0]
- 18 OSB[7..0]
- 18 QSB# [7..0]
- 18 DQMB# [7..0]

R1.1---ITEM25

R1.1---ITEM25



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**ATI\_M54P\_VRAM\_B(6)**

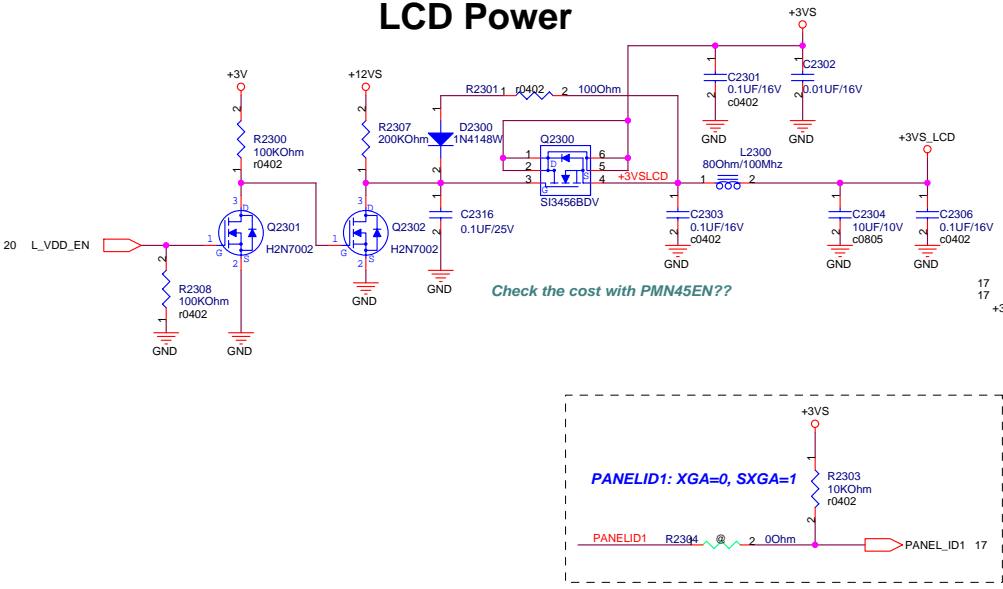
Size	Document Number	Rev
Customer	F2J	1.1

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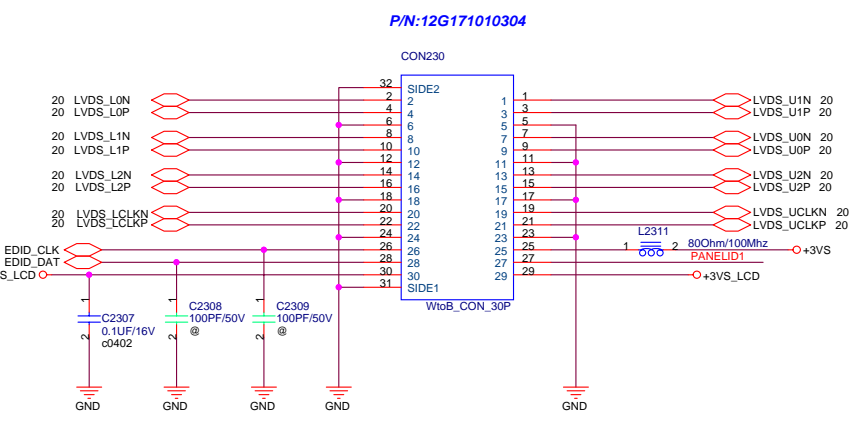
# LCD Backlight Control

Panel Requirement:  
 Impedance: 100 ohm +/- 10%  
 Length Mismatch <= 10 mils  
 Twisted Pair(Not Ribbon)  
 Maximum Length <= 16"

## LCD Power



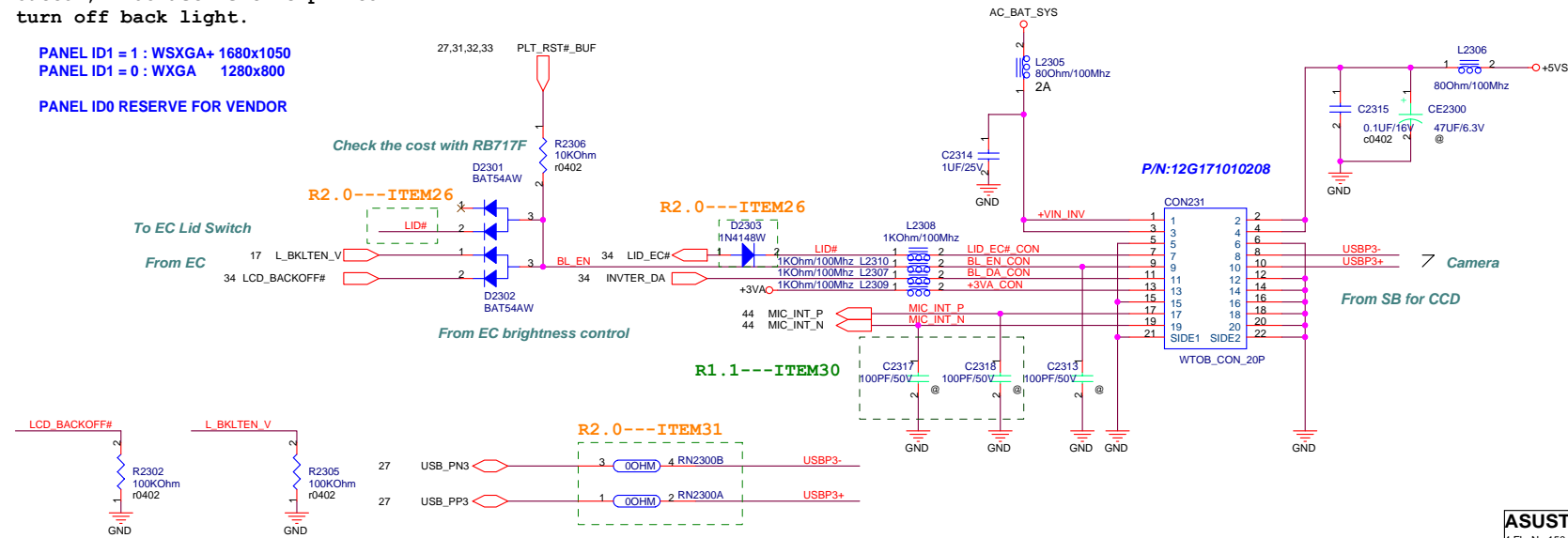
## LCD LVDS Interface



BIOS  
**BACK\_OFF#**: When user push "Fn+F7"  
 button, BIOS active this pin to  
 turn off back light.

- PANEL ID1 = 1 : WSXGA+ 1680x1050
- PANEL ID1 = 0 : WXGA 1280x800
- PANEL ID0 RESERVE FOR VENDOR

## INVERTER/INTERNAL MIC/CCD CONN



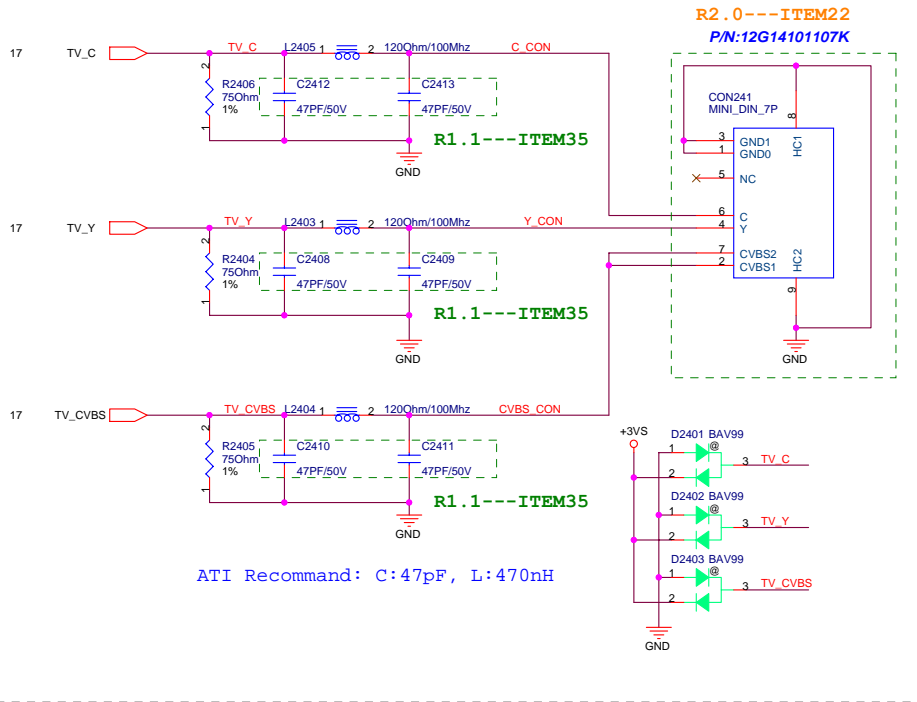
**ASUSTek COMPUTER INC.**

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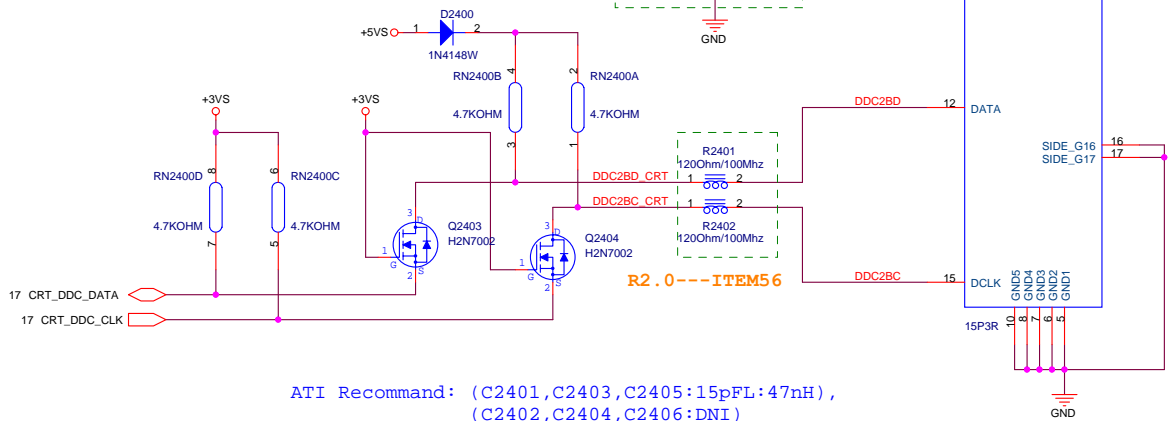
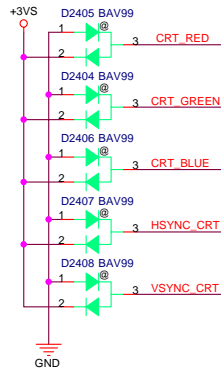
File: **LVDS & INVERTER**

Size	Document Number	Rev
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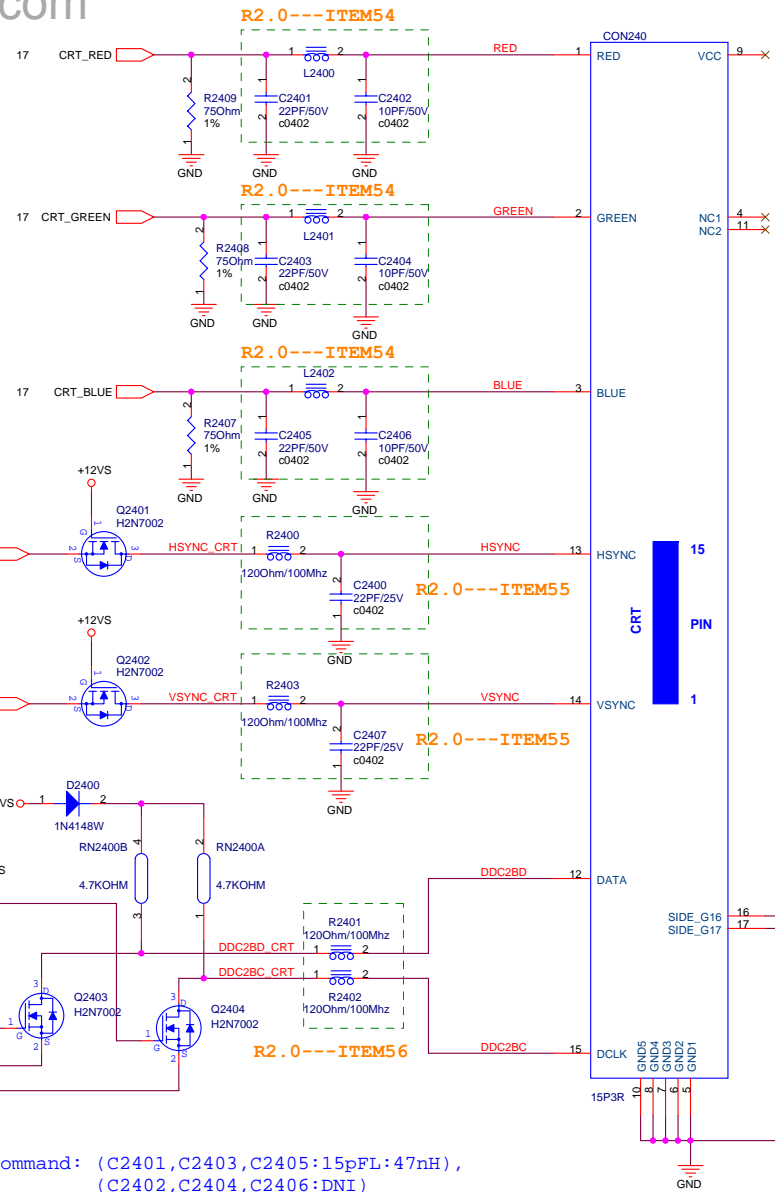
# TV



+2.5VS	17,20,41,54
+3VS	17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61
+5V	32,41,59,61
+5VS	21,23,34,35,36,38,39,41,42,43,50,61



P/N:12G10110015N



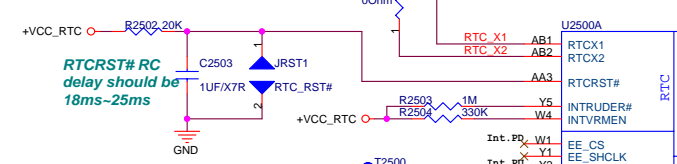
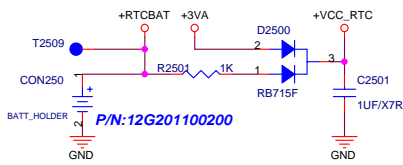
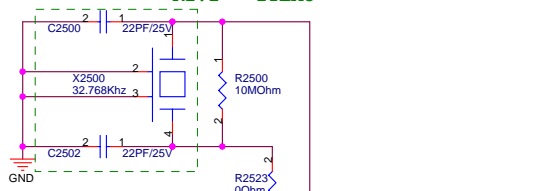
**ASUSTek COMPUTER INC.**  
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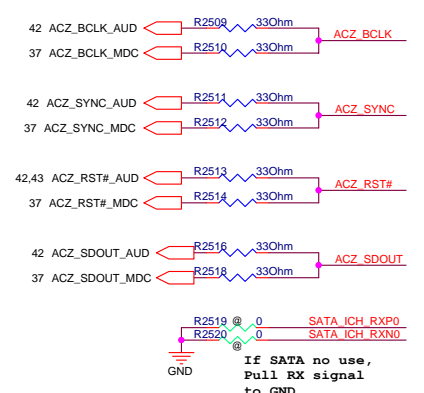
CRT & TV OUT		Rev 1.1
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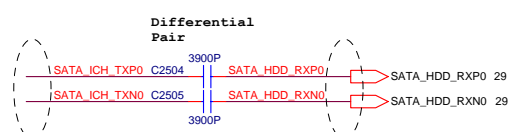
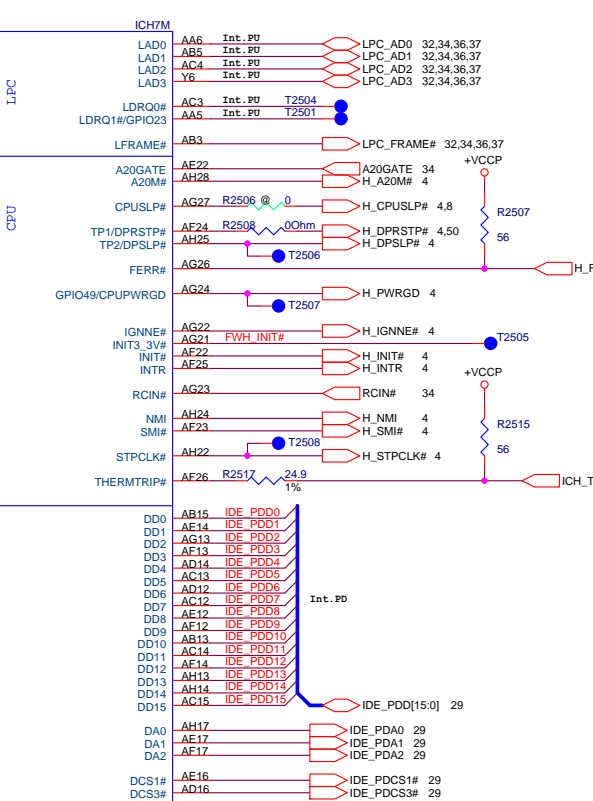
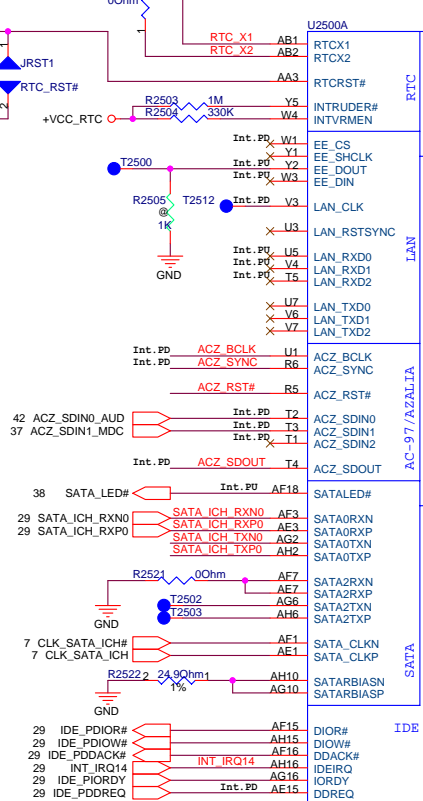
Request of CSC for CMOS clear function  
R1.1---ITEM8



RTC\_RST# RC delay should be 18ms~25ms



If SATA no use, Pull RX signal to GND.



If SATA no use, C2504, C2505 DNI

+3VA → +3VA 23,34,41,54,59  
+VCCP → +VCCP 12,41,52

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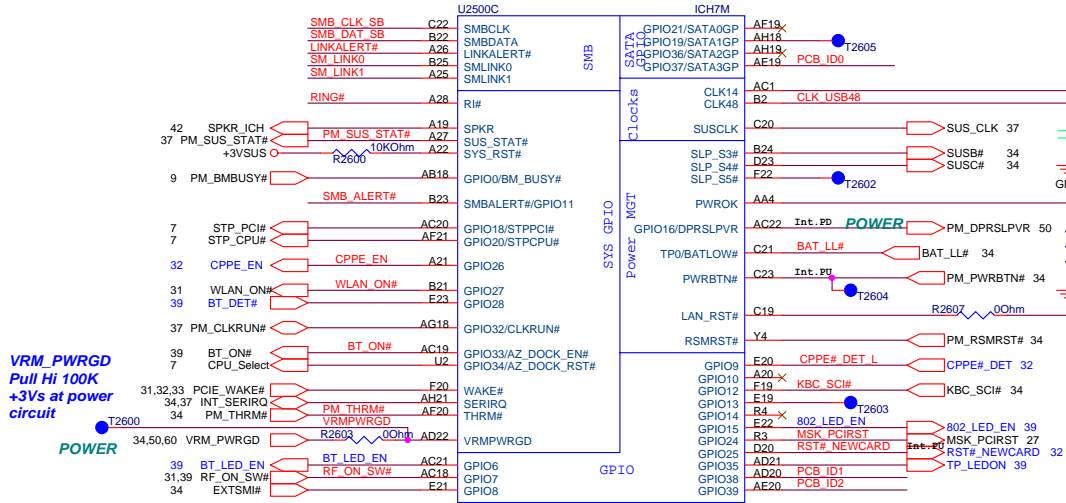
Title: **ICH7M-CPU,IDE,AUDIO**

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+3VS  
+5VS  
+3VSUS

17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61  
21,23,34,35,36,38,39,41,42,43,50,61  
31,33,37,43,51

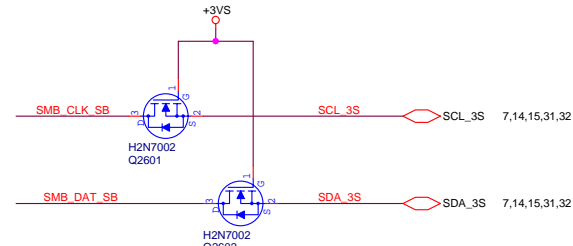
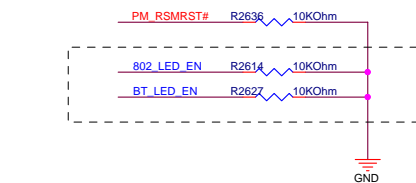
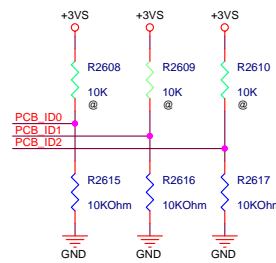
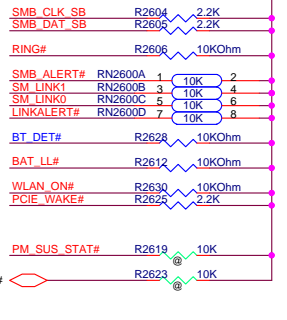
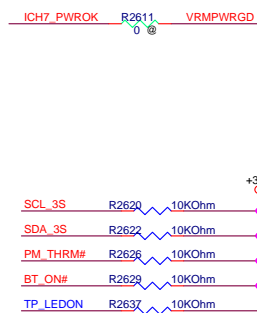
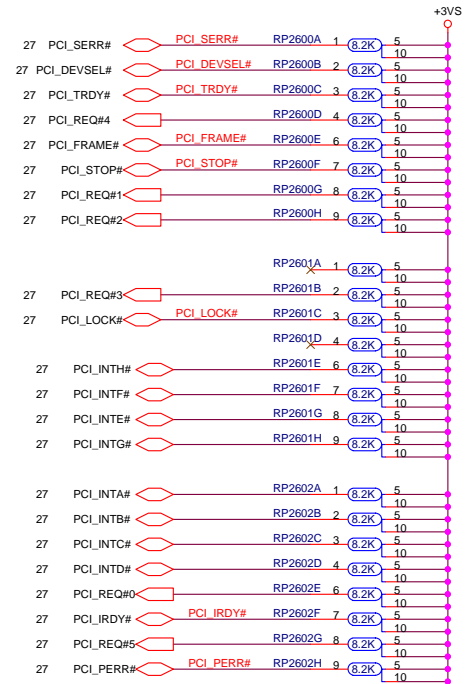
To new card check power plane



VRM\_PWRGD  
Pull Hi 100K  
+3Vs at power  
circuit

PCB\_VID3 : PROJECT CODE

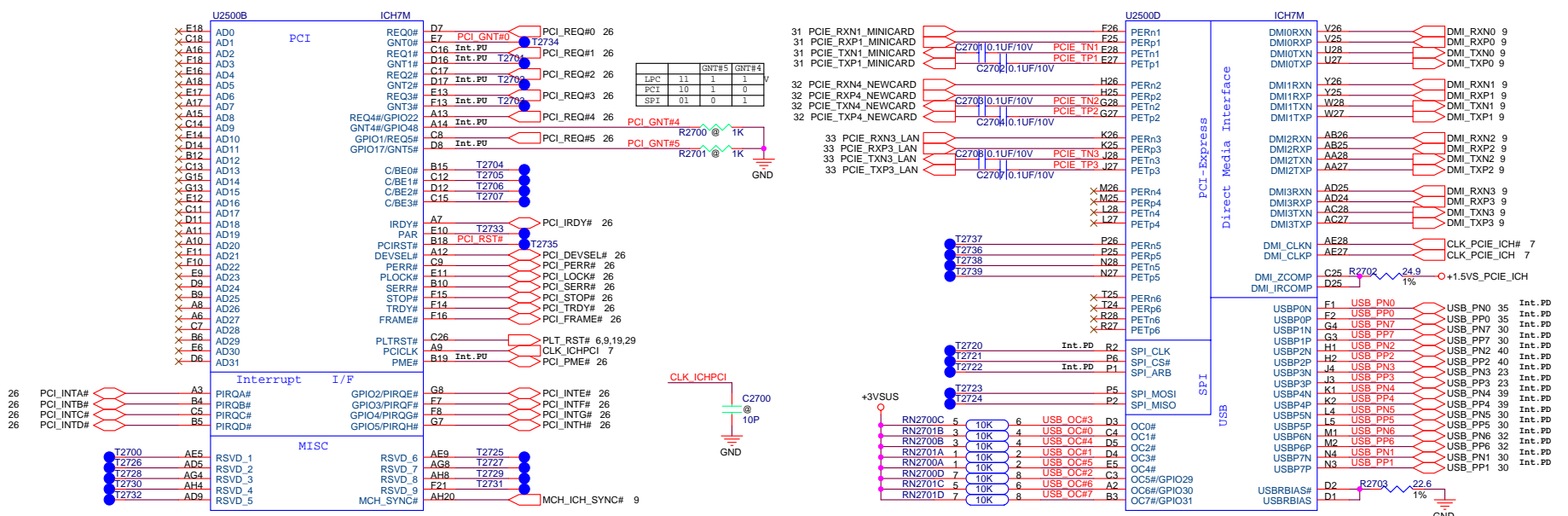
PCB\_VID 0 1 2  
MB F2J 0 0 0  
MB F2F 0 0 1  
MB F2H 0 1 0



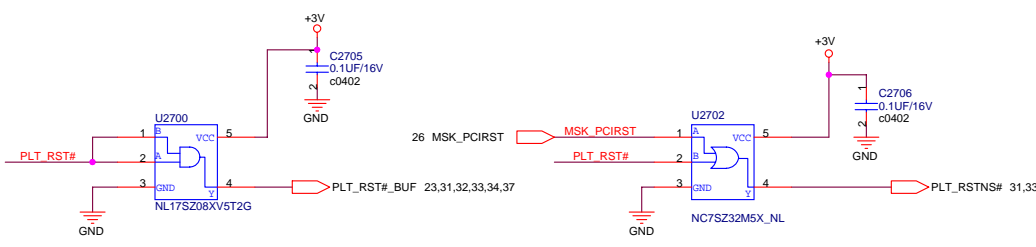
Clock Generator  
DDR2 SO-DIMM  
Mimi Card  
New Card

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Title		
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USB 0	Finger Printer
USB 1	USB Conn.
USB 2	Card Reader
USB 3	CMOS Camera
USB 4	Bluetooth
USB 5	USB Conn.
USB 6	Newcard
USB 7	USB Conn.

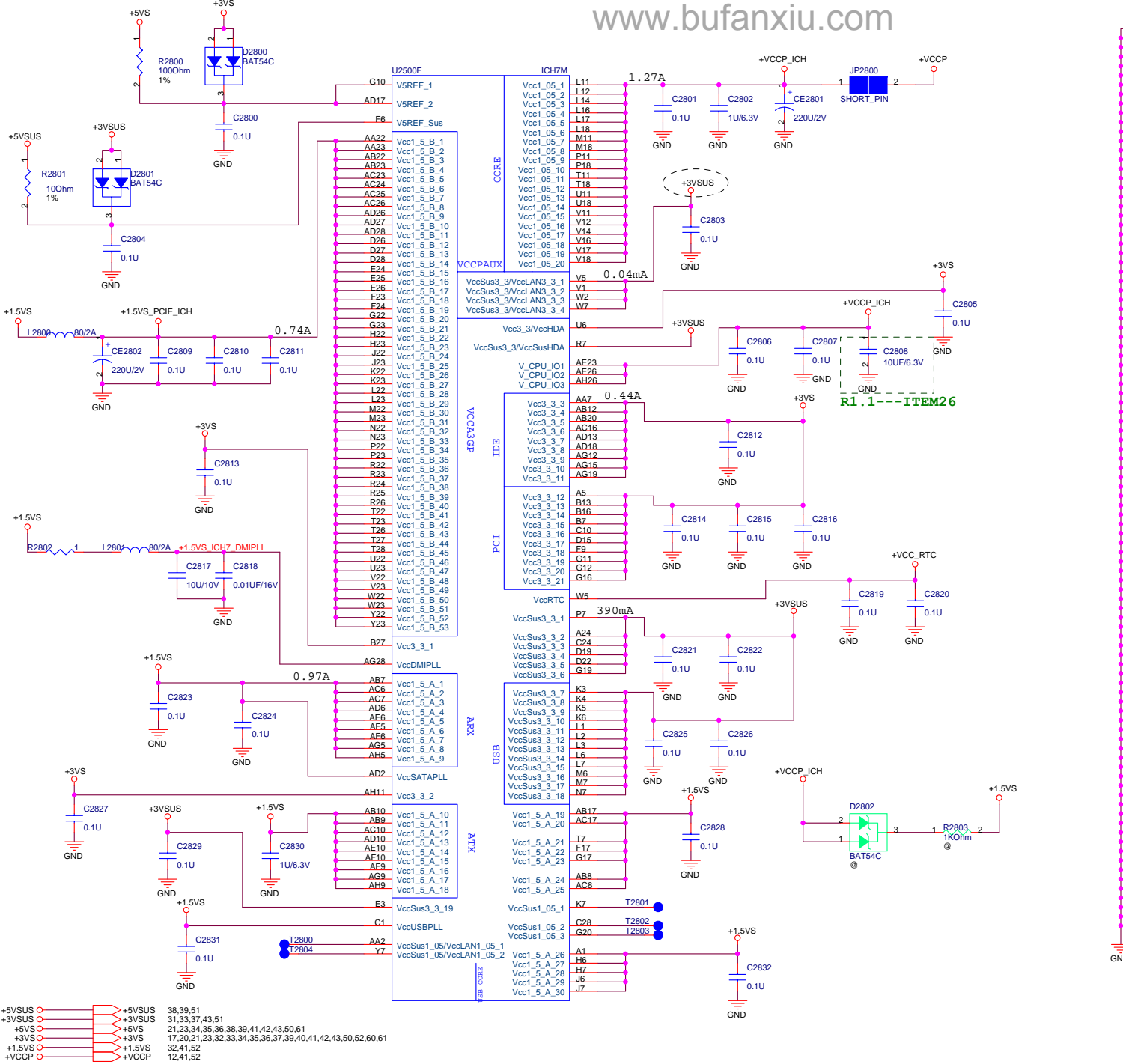


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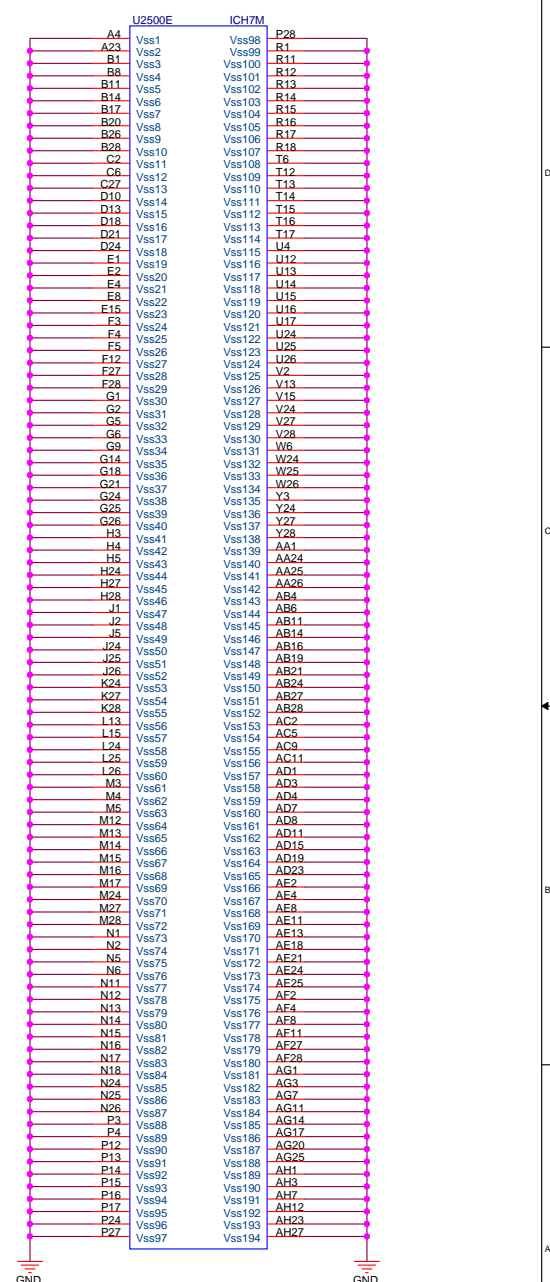
4 FL, No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

Title: **ICH7M-PCI-E,USB**

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+5VSUS	38,39,51
+3VSUS	31,33,37,43,51
+5VS	21,23,34,35,36,38,39,41,42,43,50,61
+3VS	17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61
+1.5VS	32,41,52
+VCCP	12,41,52



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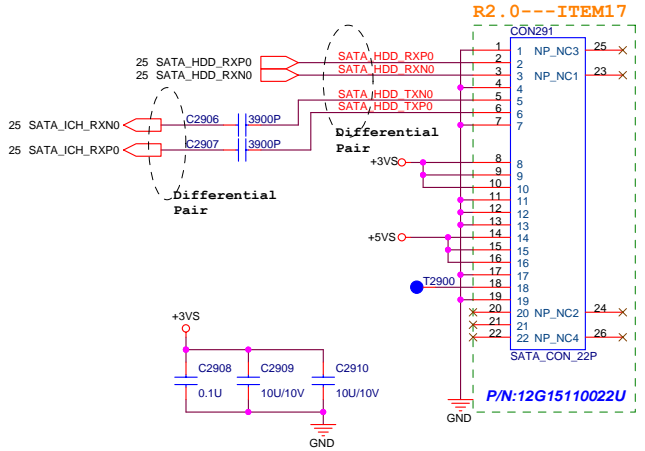
4 FL, No.150, Li-Te Rd, Peitou, Taipei, Taiwan, ROC

Title: **ICH7M-VCC\_GND**

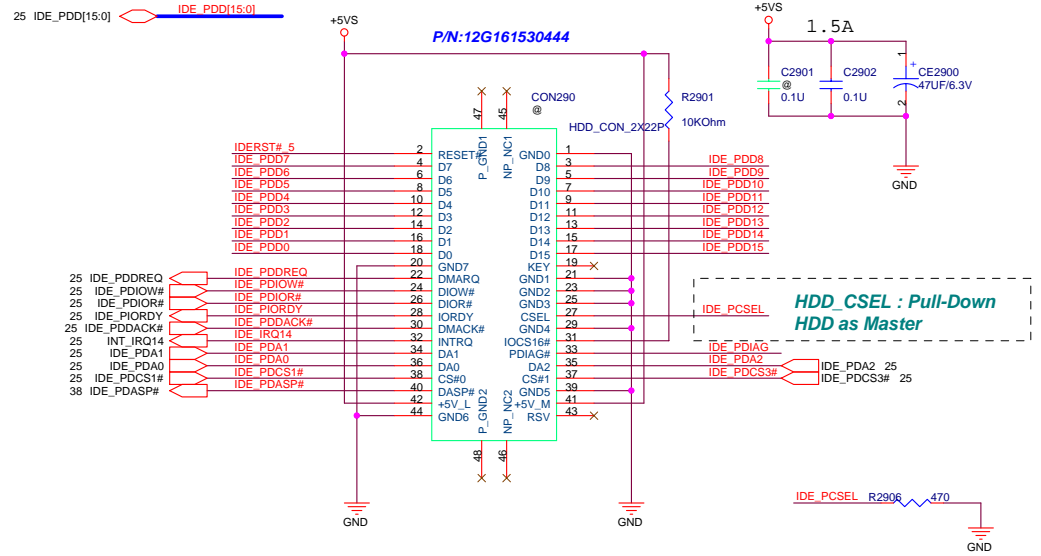
Size	Document Number	Rev
Custom	<b>F2J</b>	1.1

Date: Thursday, April 27, 2006 Sheet 28 of 63

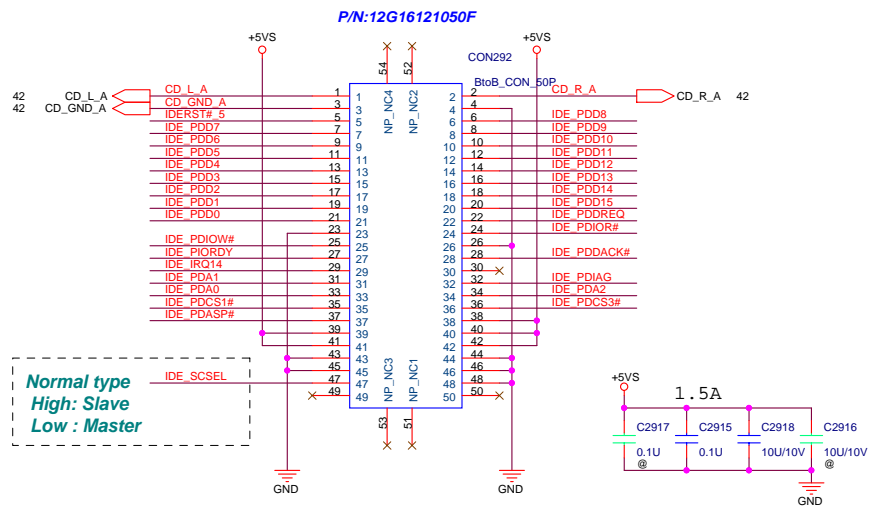
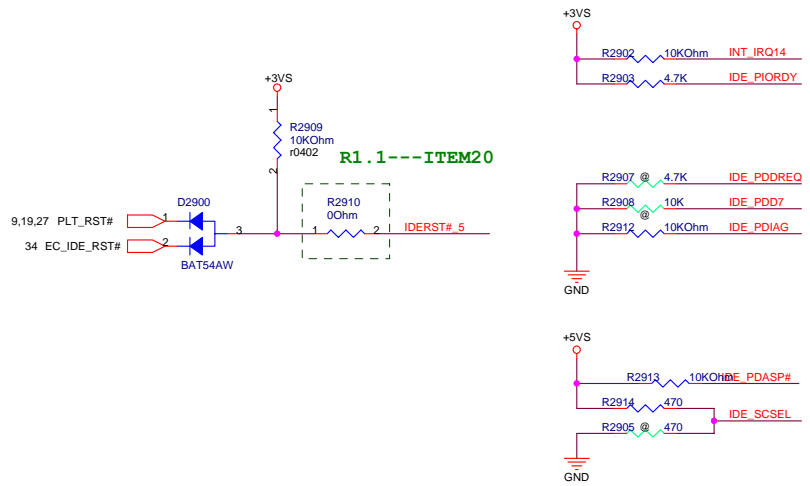
### SATA HDD CON



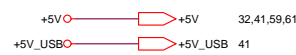
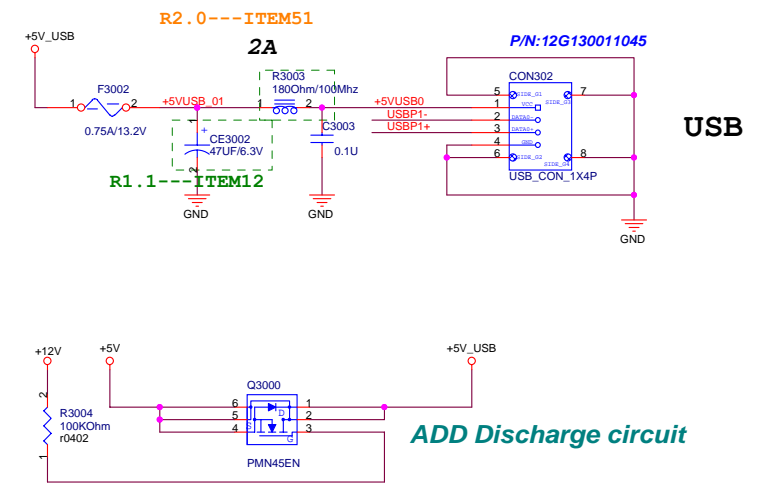
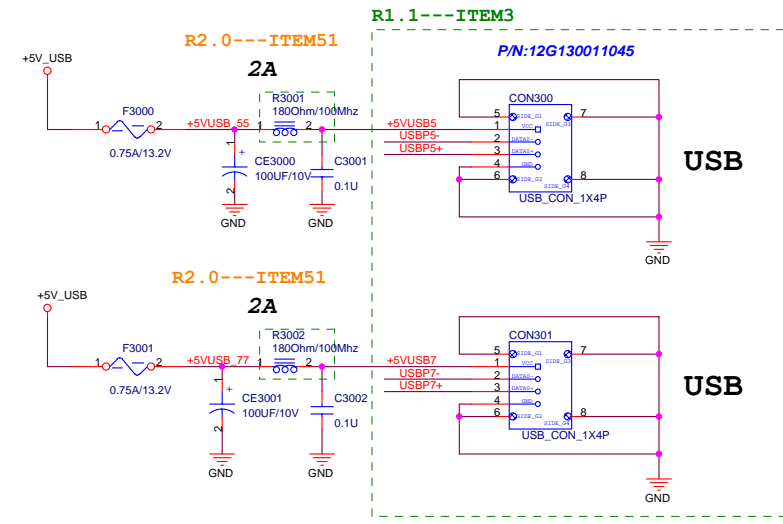
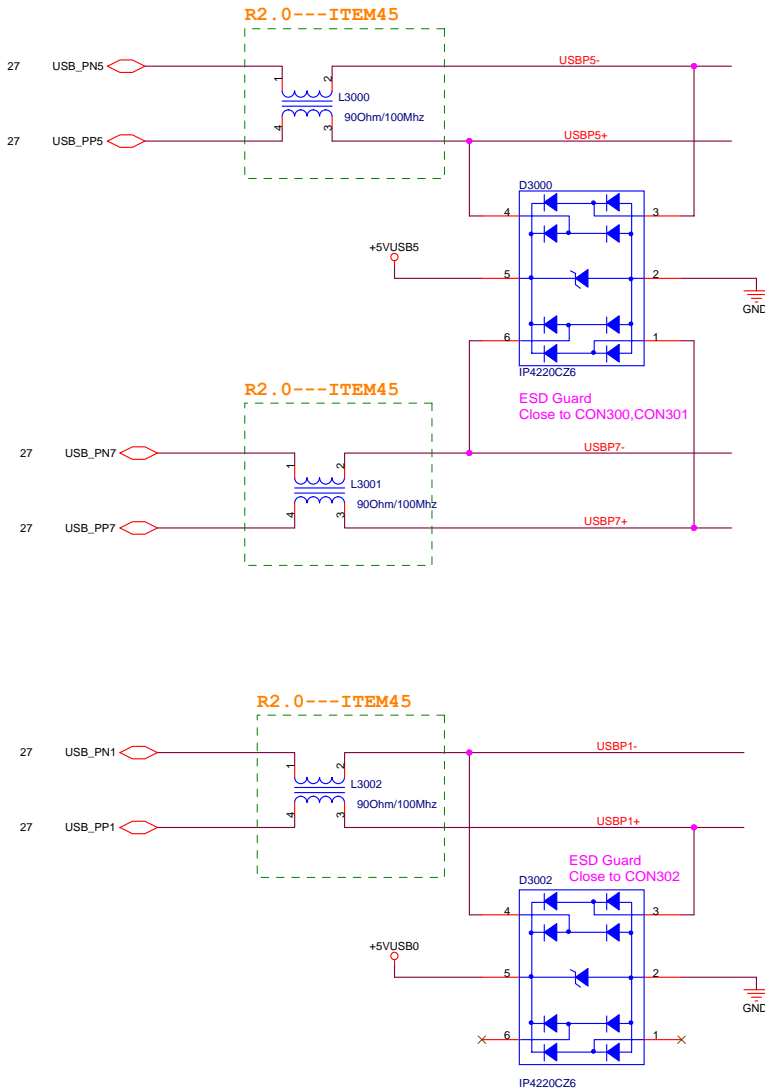
### PATA HDD CON



### PATA CD-ROM CON



+3VS ○ → +3VS 17,20,21,23,32,33,34,35,36,37,39,40,41,42,43,50,52,60,61  
 +5VS ○ → +5VS 21,23,34,35,36,38,39,41,42,43,50,61  
 +5V ○ → +5V 32,41,59,61



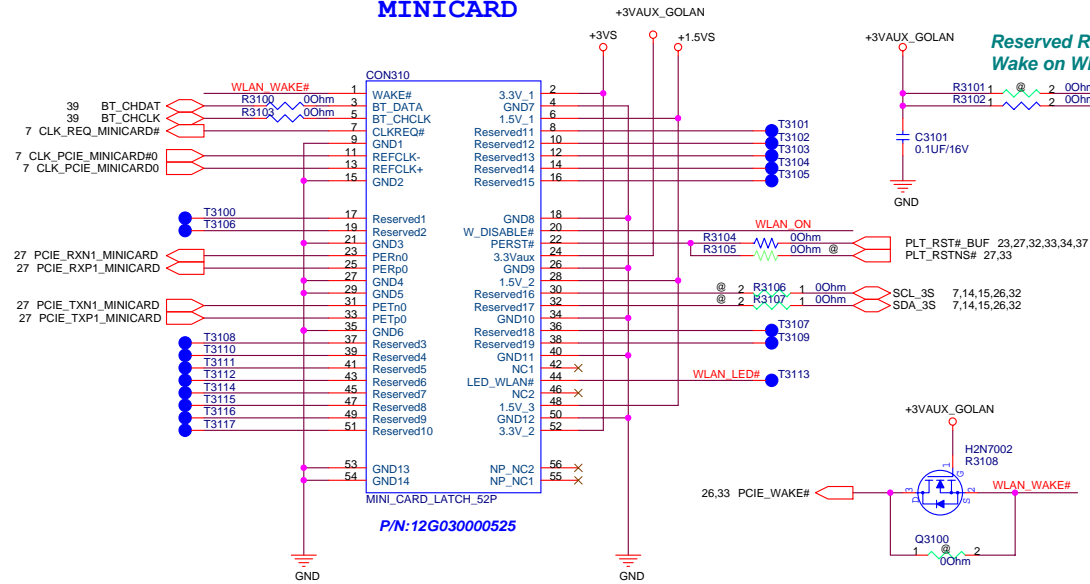
ASUSTek COMPUTER INC.		
4 FL., No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC		
Title		
USB PORTS		
Size	Document Number	Rev
Custom	F2J	1.1
Date:	Thursday, April 27, 2006	Sheet 30 of 63

**POWER CONSUMPTION:**  
**+3VS: +3.003V~+3.597V**  
**Max= 750 mA**

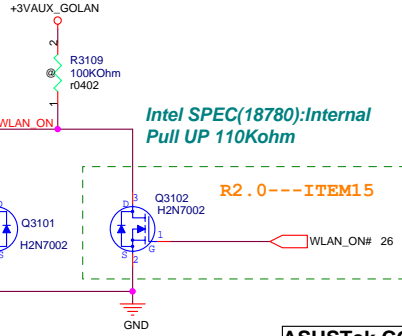
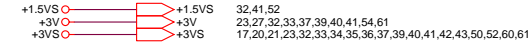
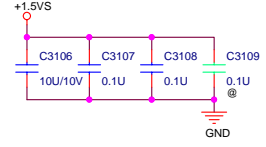
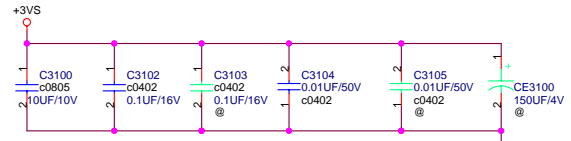
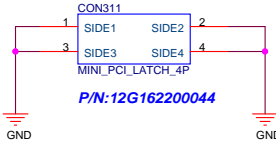
**+1.5VS: +1.425V~+1.575V**  
**Max= 375 mA**

**+3VAUX\_GOLAN: +3.003V~+3.597V**  
**Max= 250 mA**

**MINICARD**



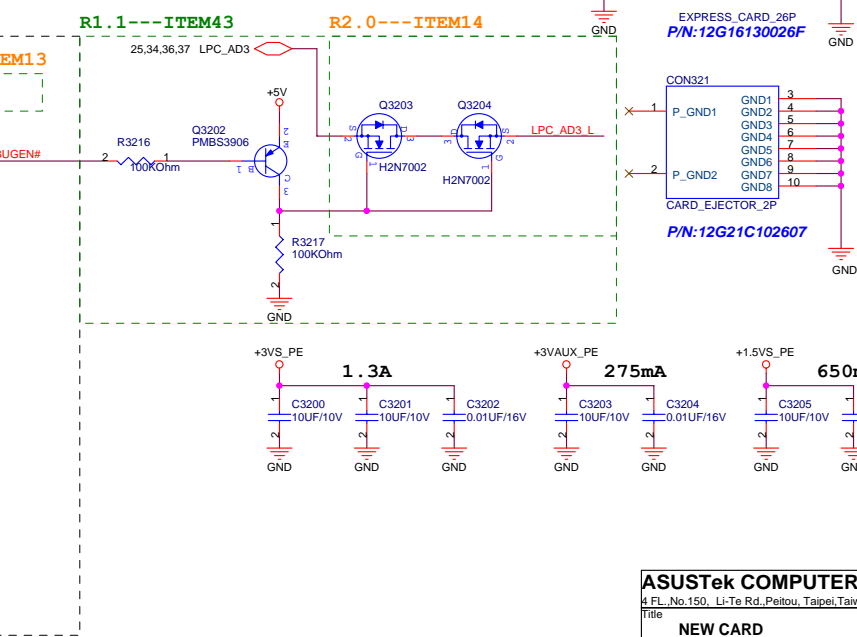
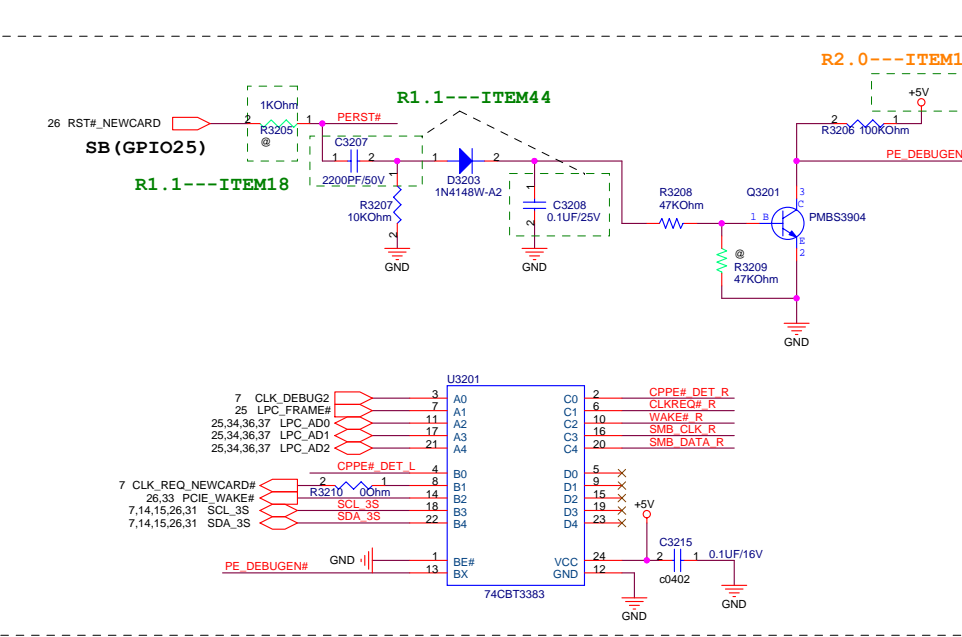
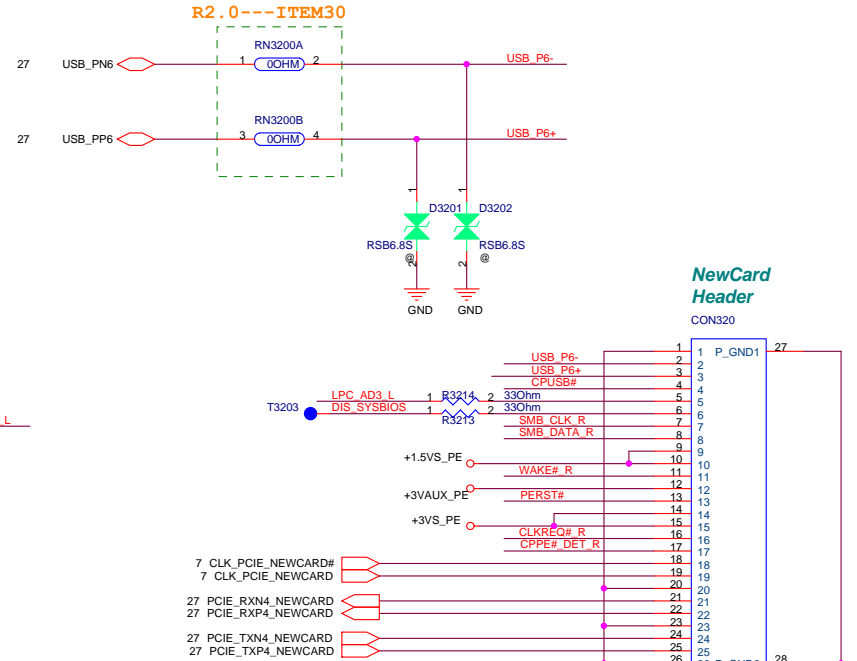
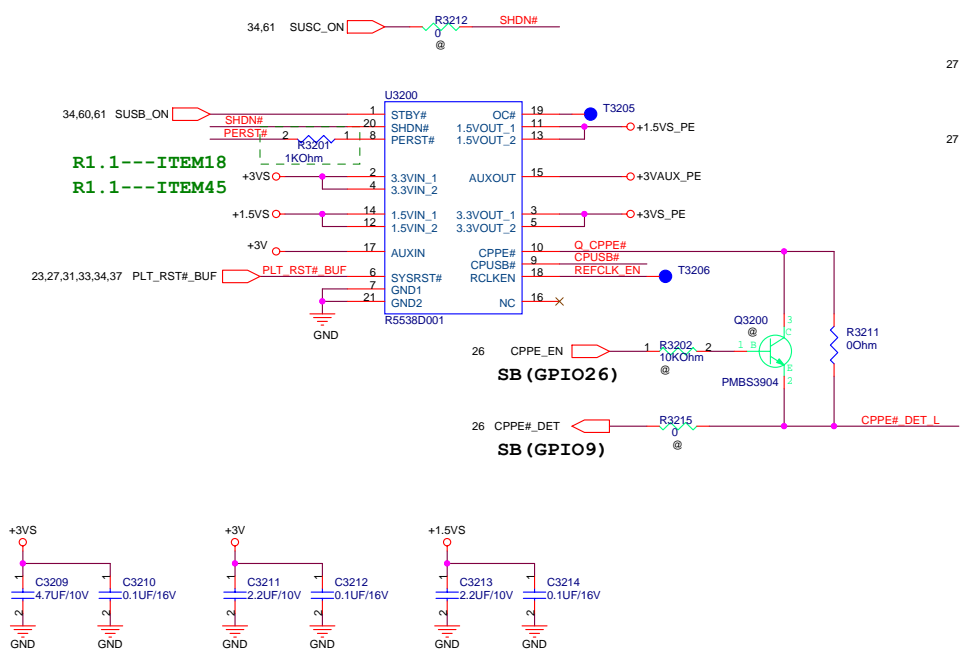
Reserved R to +3VSUS for Wake on WLAN function!



Intel SPEC(18780):Internal Pull UP 110Kohm

R2.0---ITEM15

<b>ASUSTek COMPUTER INC.</b>		
4 FL_No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC		
Title: <b>MINI CARD</b>		
Size: Custom	Document Number: <b>F2J</b>	Rev: 1.1
Date: Thursday, April 27, 2006	Sheet: 31	of 63



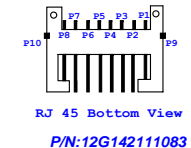
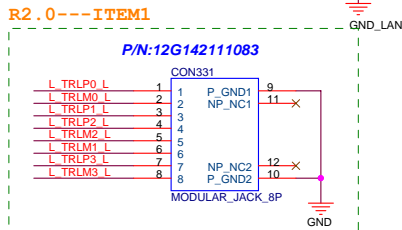
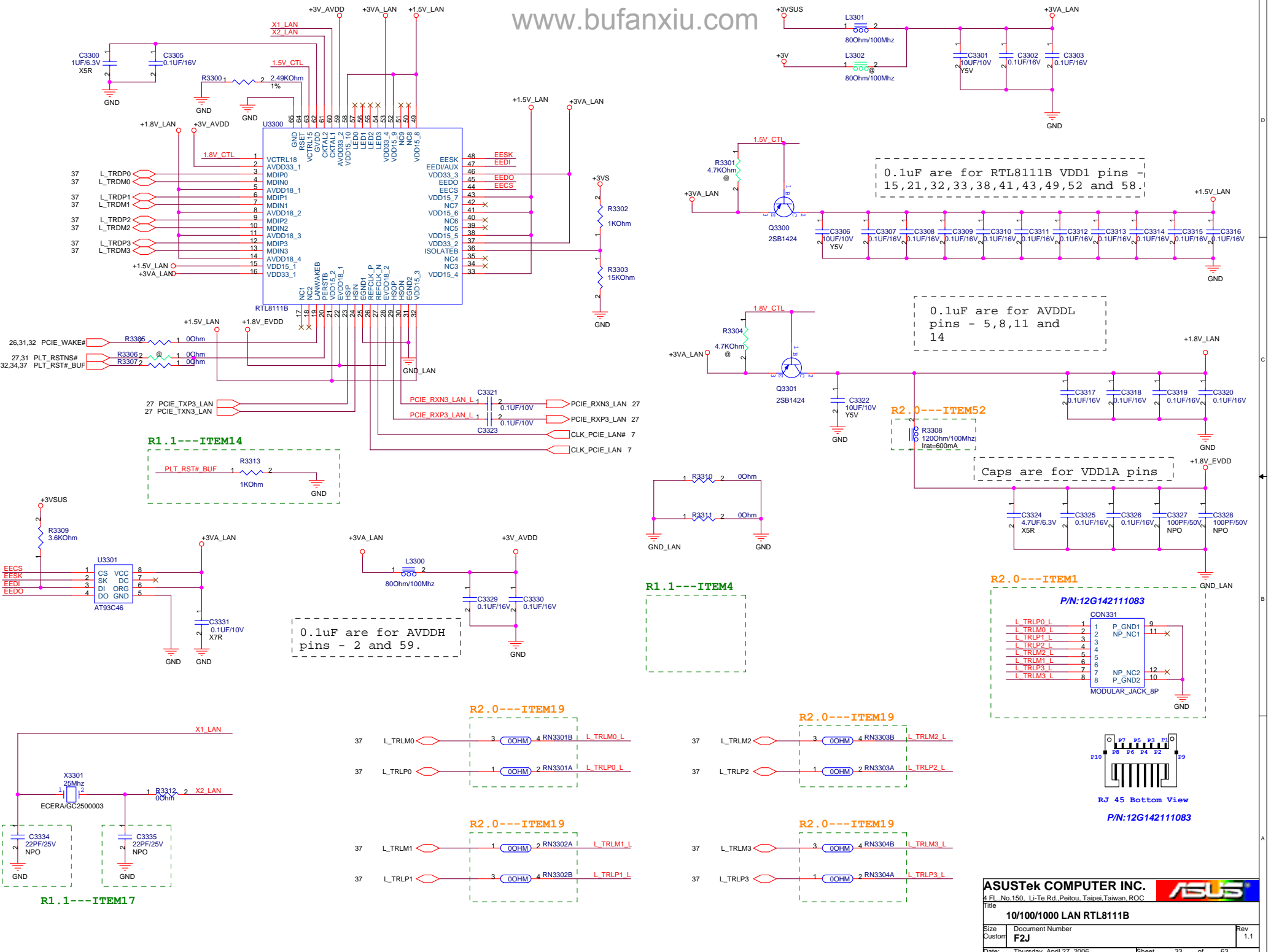
**ASUSTek COMPUTER INC.**

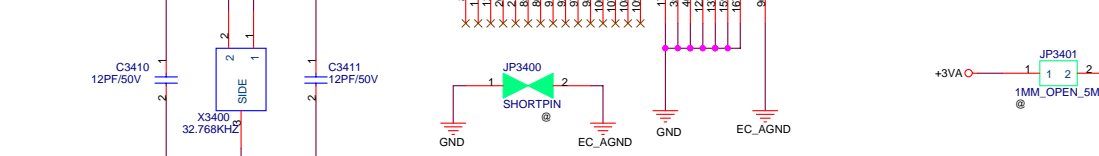
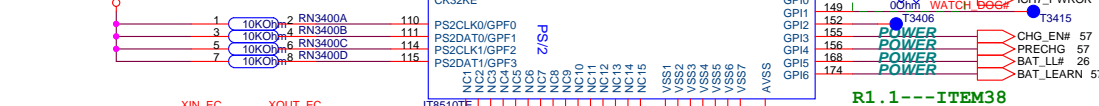
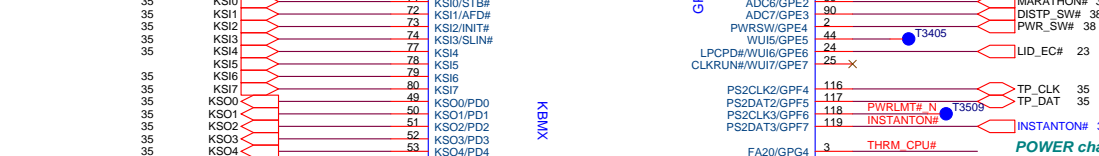
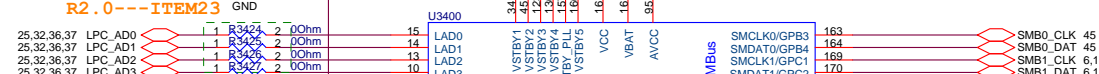
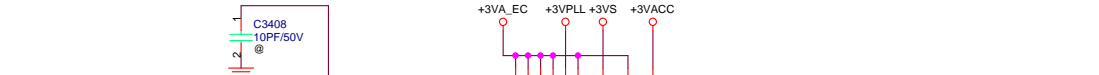
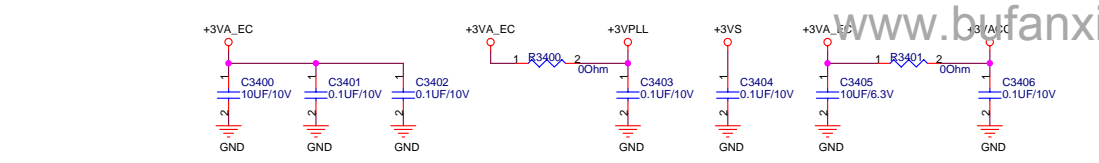
4 FL, No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

**NEW CARD**

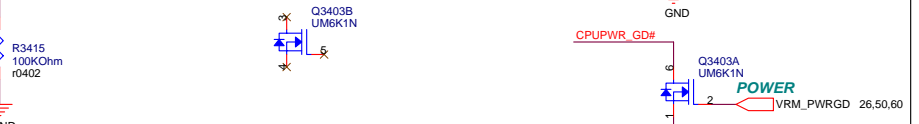
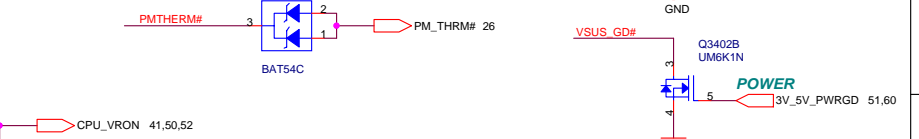
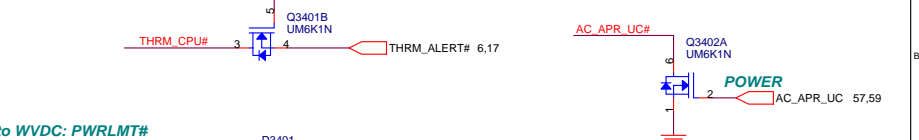
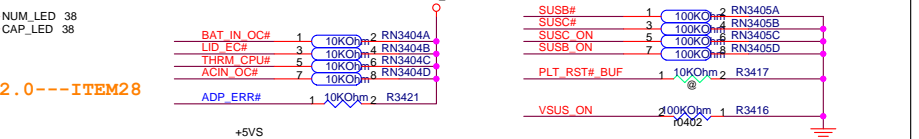
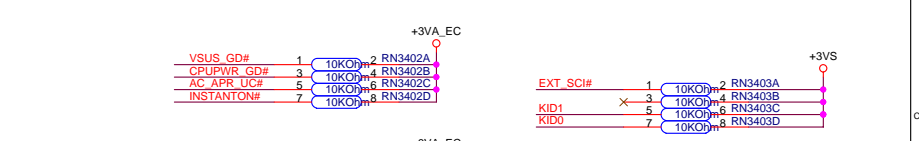
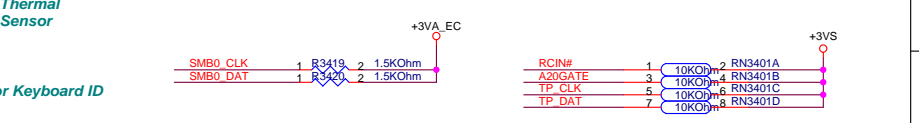
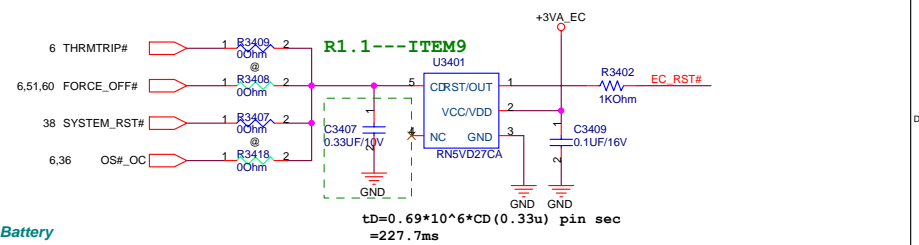
Size Custom	Document Number	Rev
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Check Reset & CLK timing



**ASUSTek COMPUTER INC.**

4 FL, No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

**EC-IT8510E**

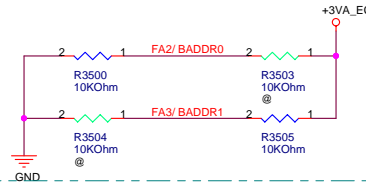
Size	Document Number	Rev
Custom	F2J	1.1

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EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

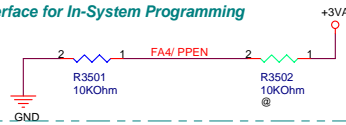
- 00: PNPENG Access Register Pair Are 002Eh and 002Fh
- 10: PNPENG Access Register Pair Are 004Eh and 004Fh
- 01: PNPENG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.
- 11: Reserved



Note: Sampled at VSTBY Power Up Reset

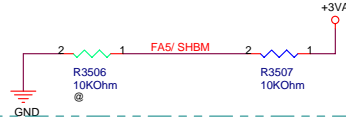
FA4/ PPEN

- 0: Normal
- 1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

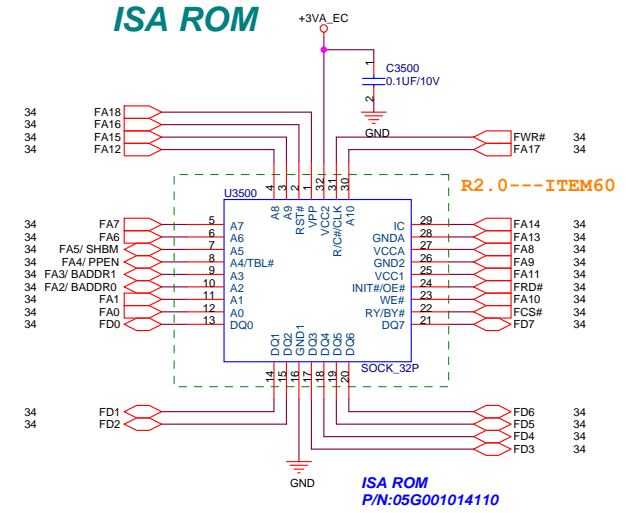


FA5/ SHBM

- 0: Disable Shared Memory with Host BIOS
- 1: Enable Shared Memory with Host BIOS

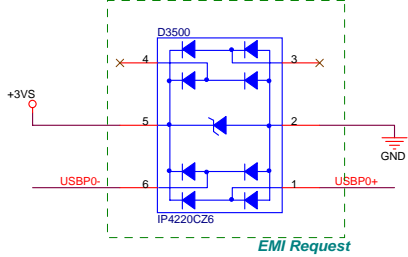


ISA ROM



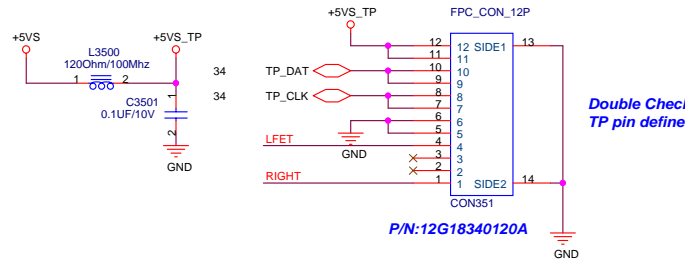
ISA ROM P/N:05G001014110

R2.0---ITEM32



EMI Request

For Touch-Pad

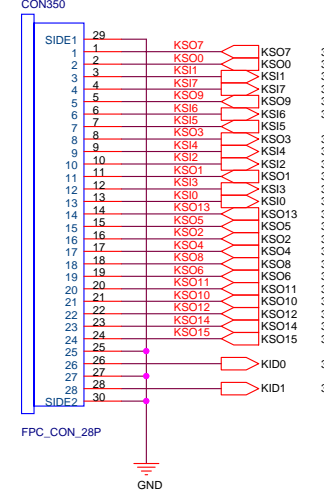


Double Check TP pin define

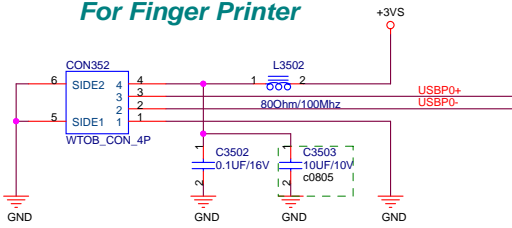
P/N:12G18340120A

For Keyboard

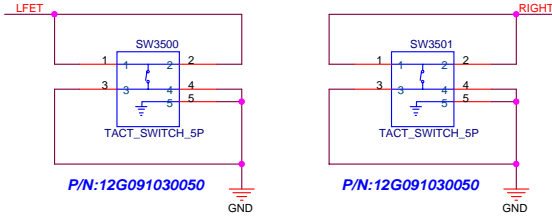
P/N:12G182402806 keyboard Matrix follow A7



For Finger Printer



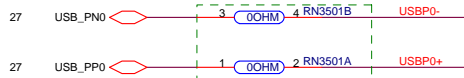
R2.0---ITEM32



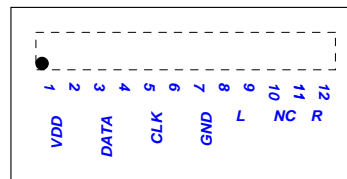
P/N:12G091030050

P/N:12G091030050

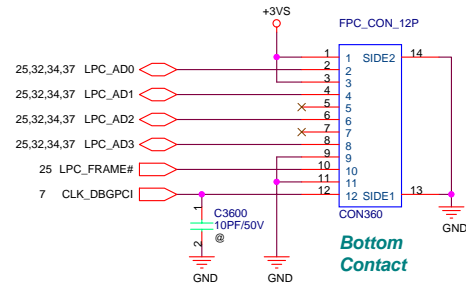
R2.0---ITEM21



TM42PU-351 (UP)---4:3



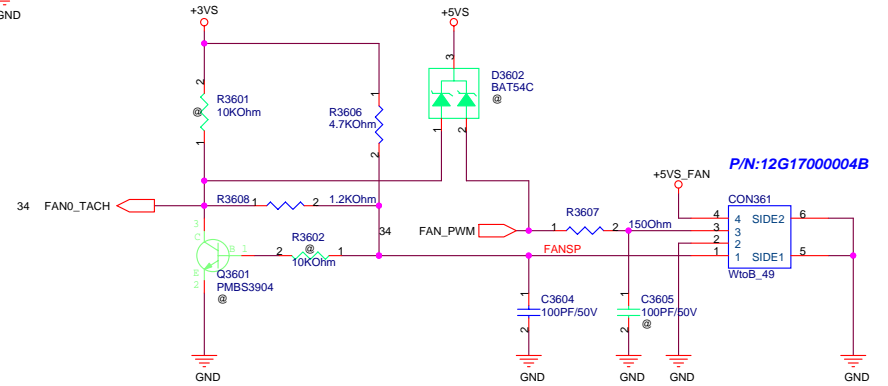
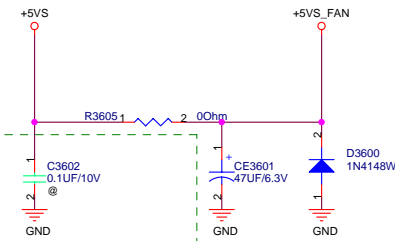
For Debug



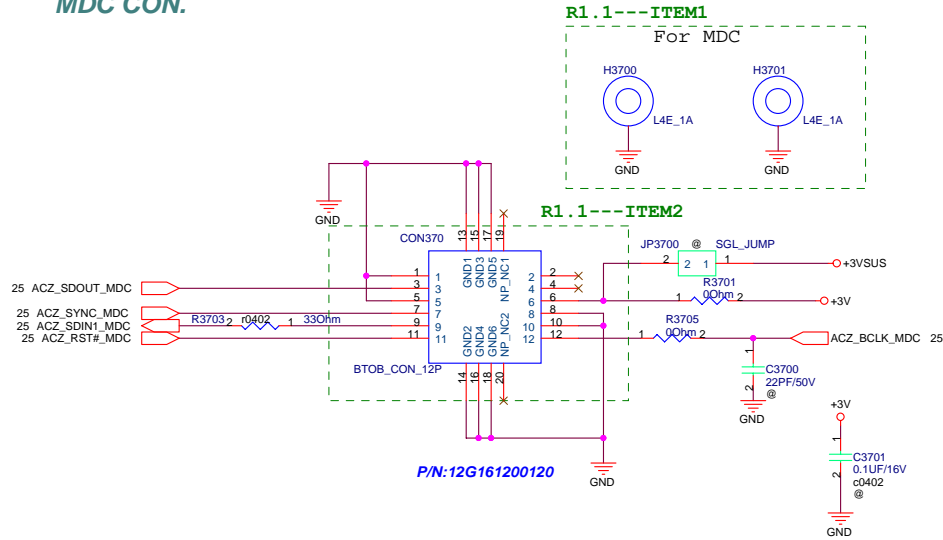
R2.0---ITEM46

DC FAN Control

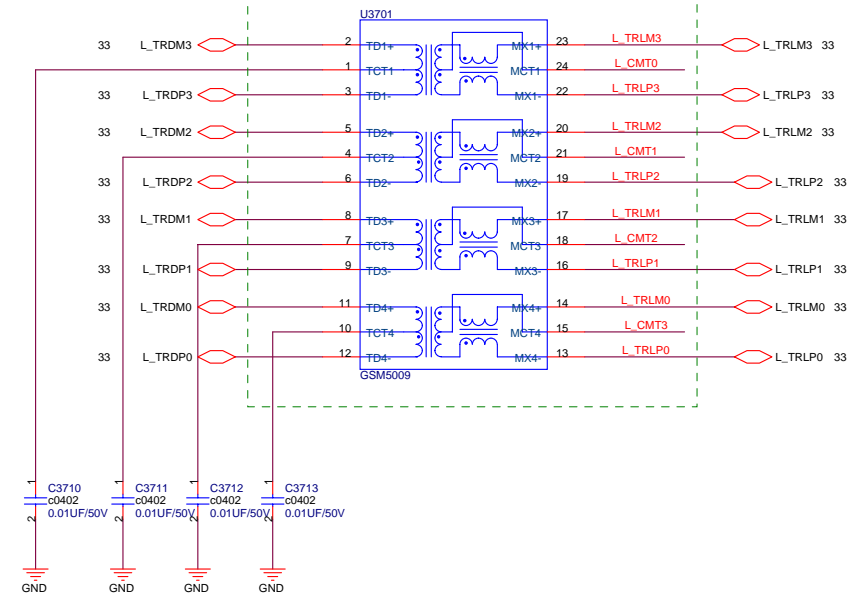
CPU FAN will be forced on:  
 1) Thermal Sensor Over-temperature  
 2) WATCHDOG asserted by EC



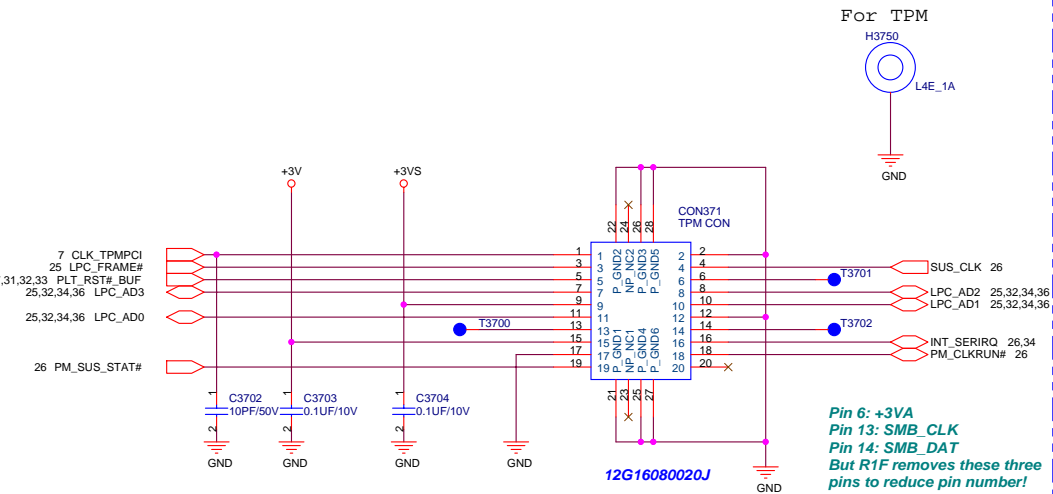
**MDC CON.**



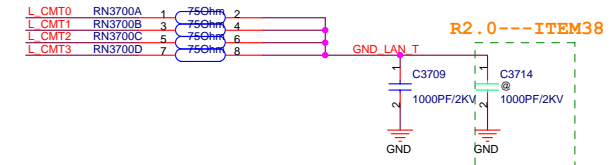
**R1.1---ITEM15**

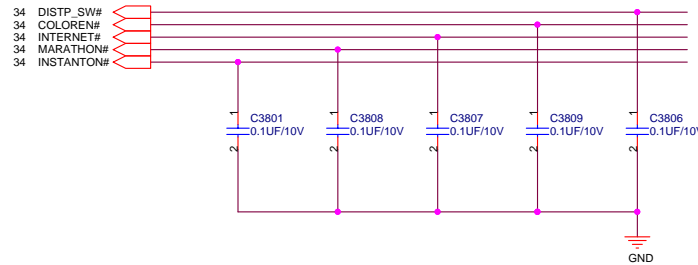
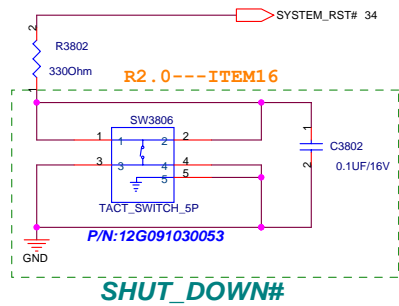
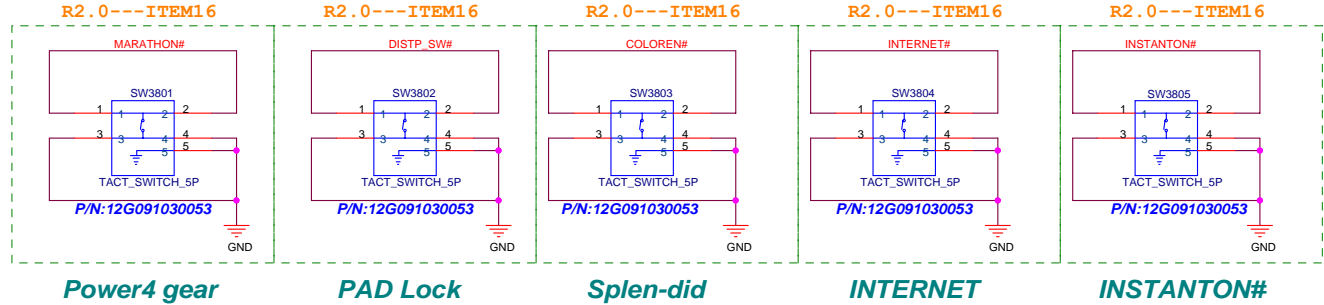
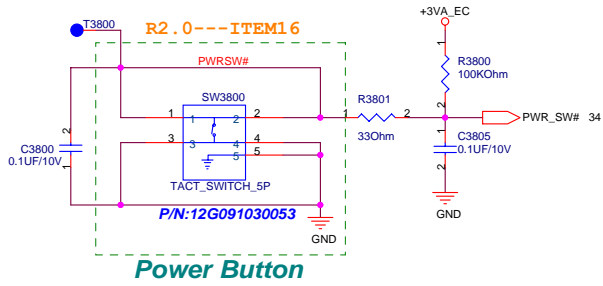


**TPM CON.**

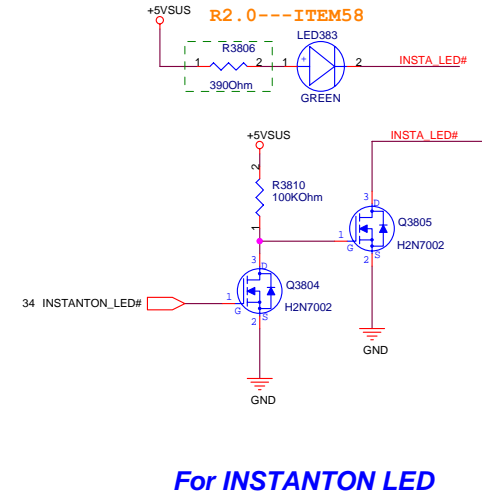
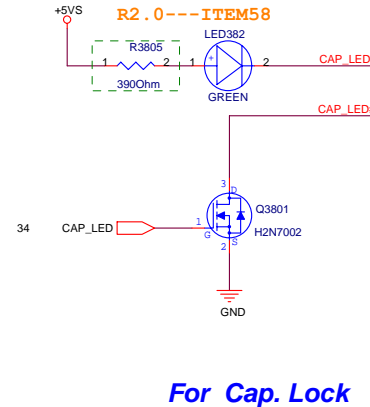
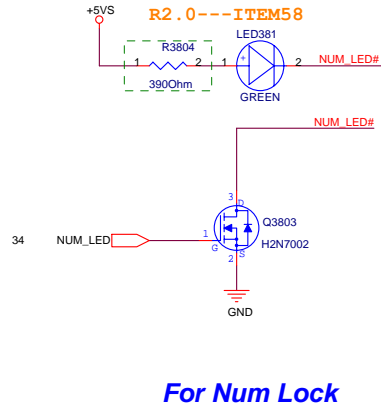
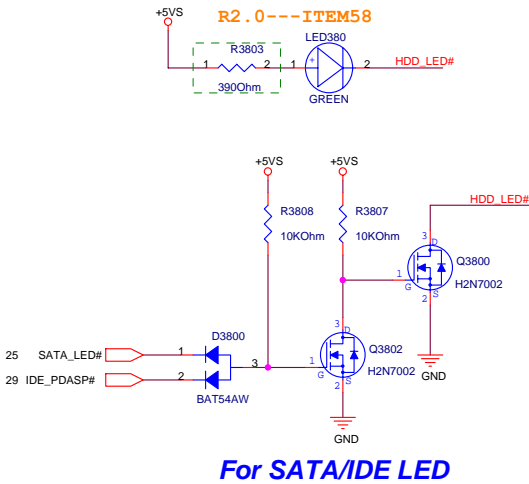


Pin 6: +3VA  
Pin 13: SMB\_CLK  
Pin 14: SMB\_DAT  
But R1F removes these three pins to reduce pin number!

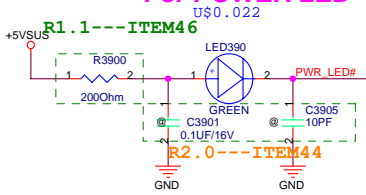




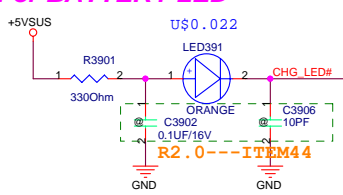
### 4 LED ABOVE INSTANT KEY



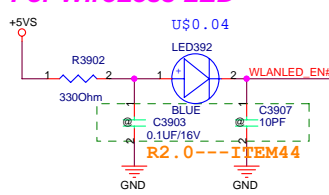
### For POWER LED



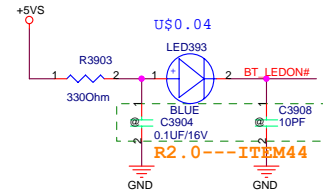
### For BATTERY LED



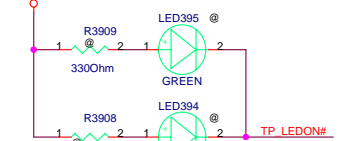
### For Wireless LED



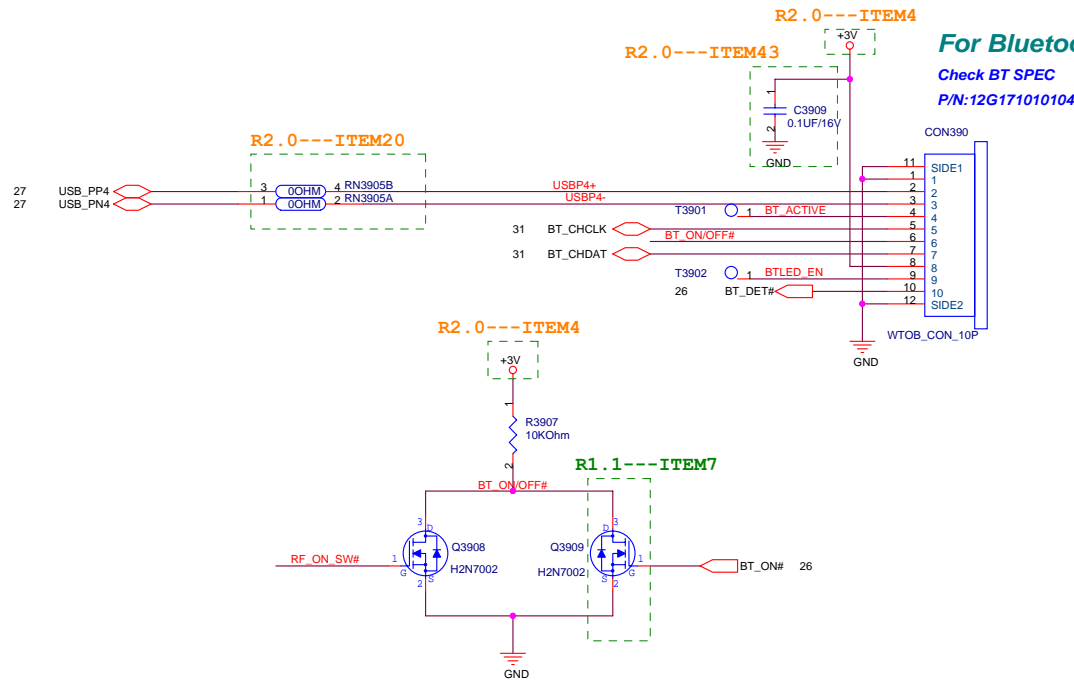
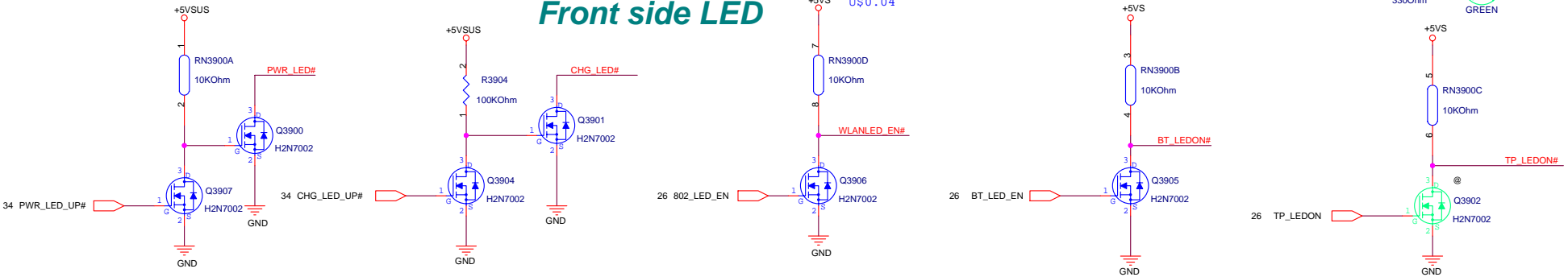
### For BT LED



### For TP LED



## Front side LED

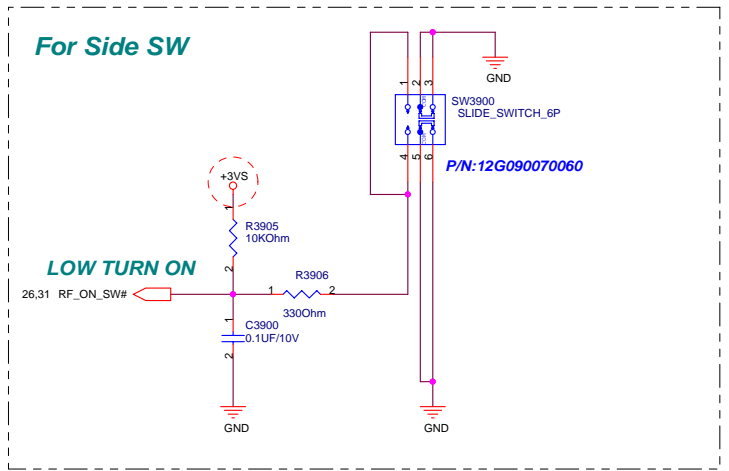


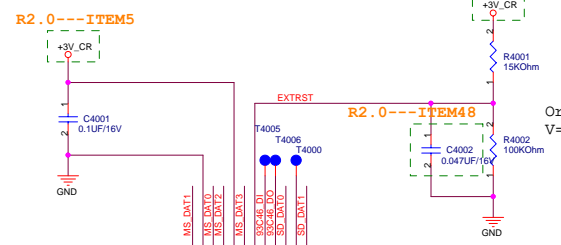
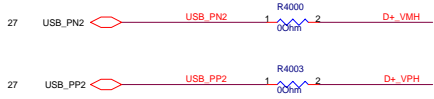
### For Bluetooth

Check BT SPEC  
P/N:12G171010104

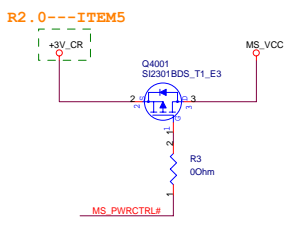
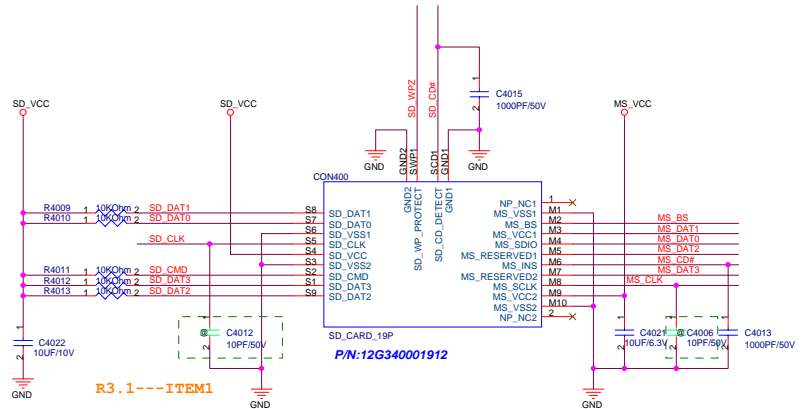
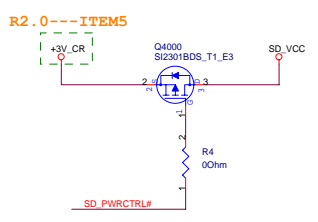
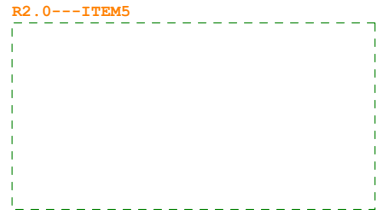
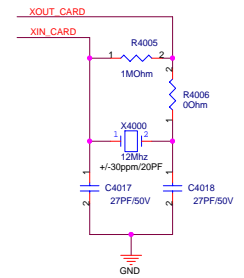
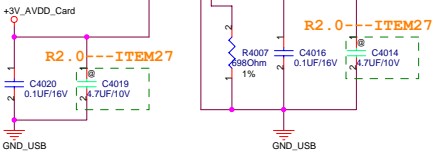
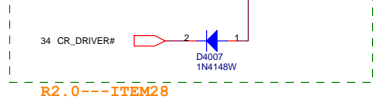
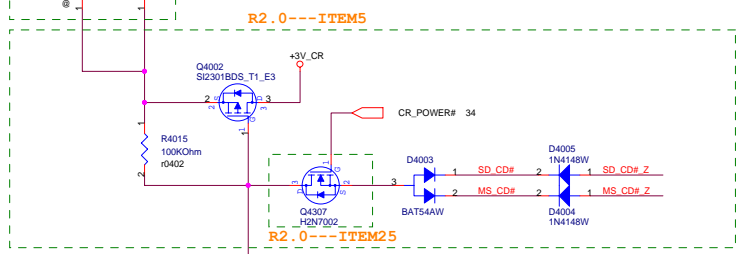
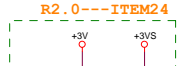
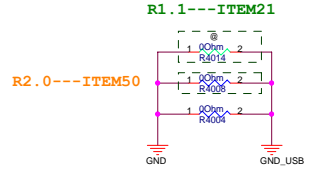
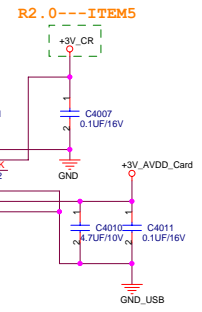
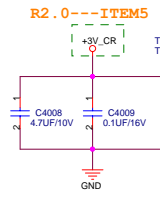
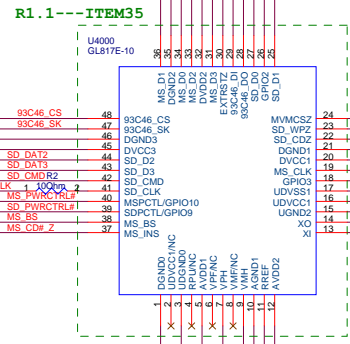
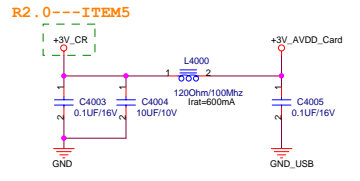
Follow W5/F3  
ON <---> OFF

### For Side SW

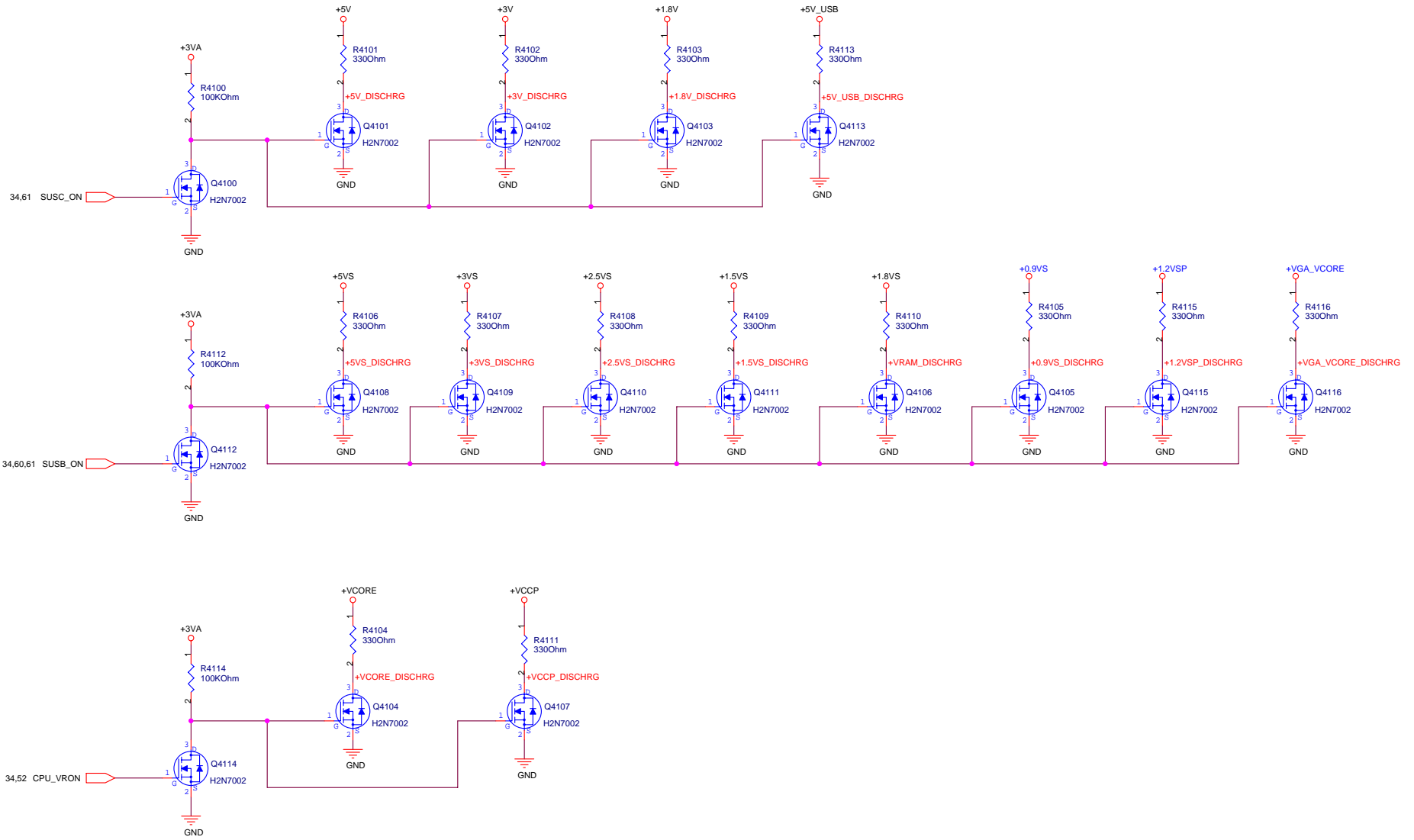


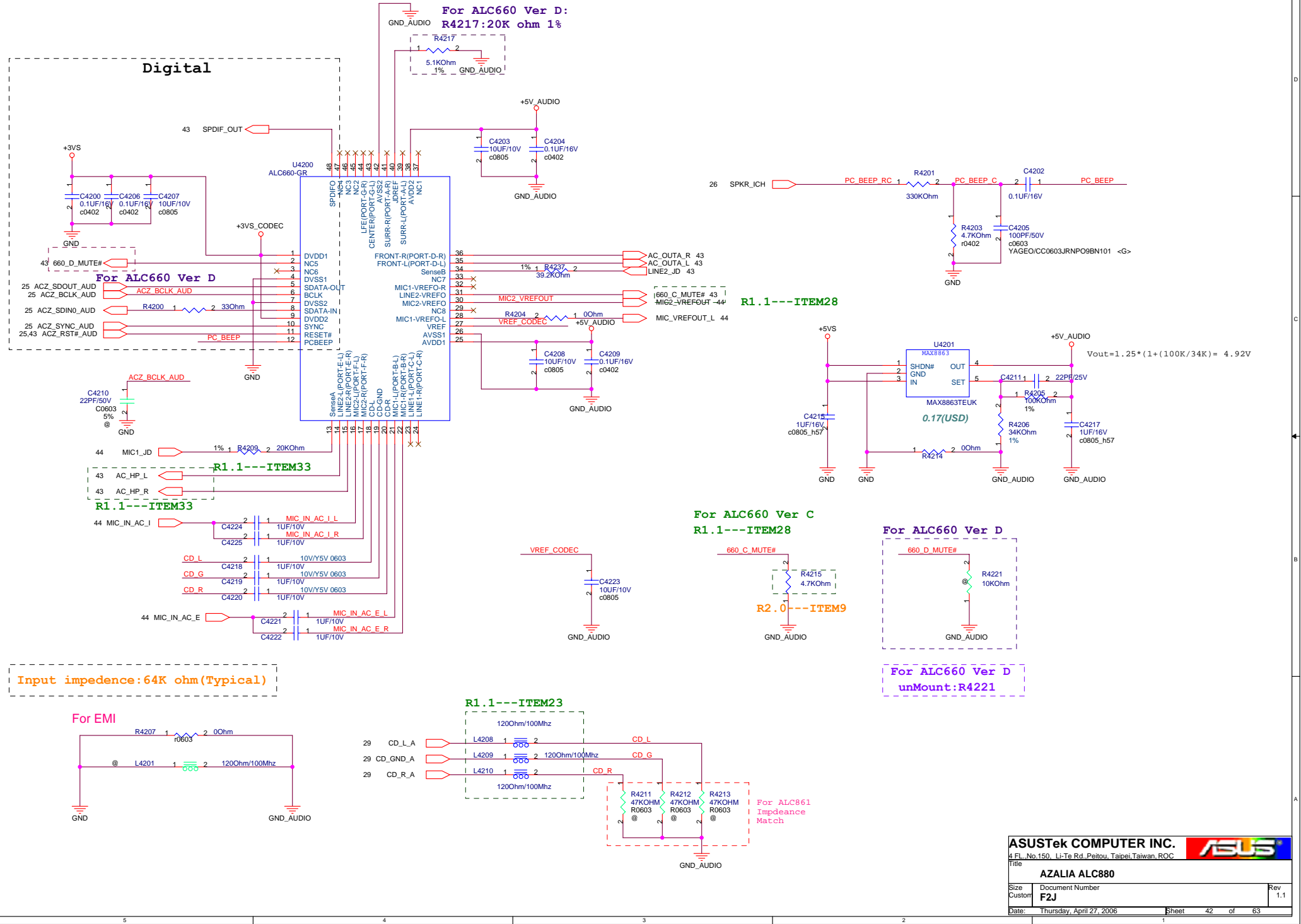


Original value:36K & 240K,  
 $V=3.3*36k/(240k+36k)=2.87$



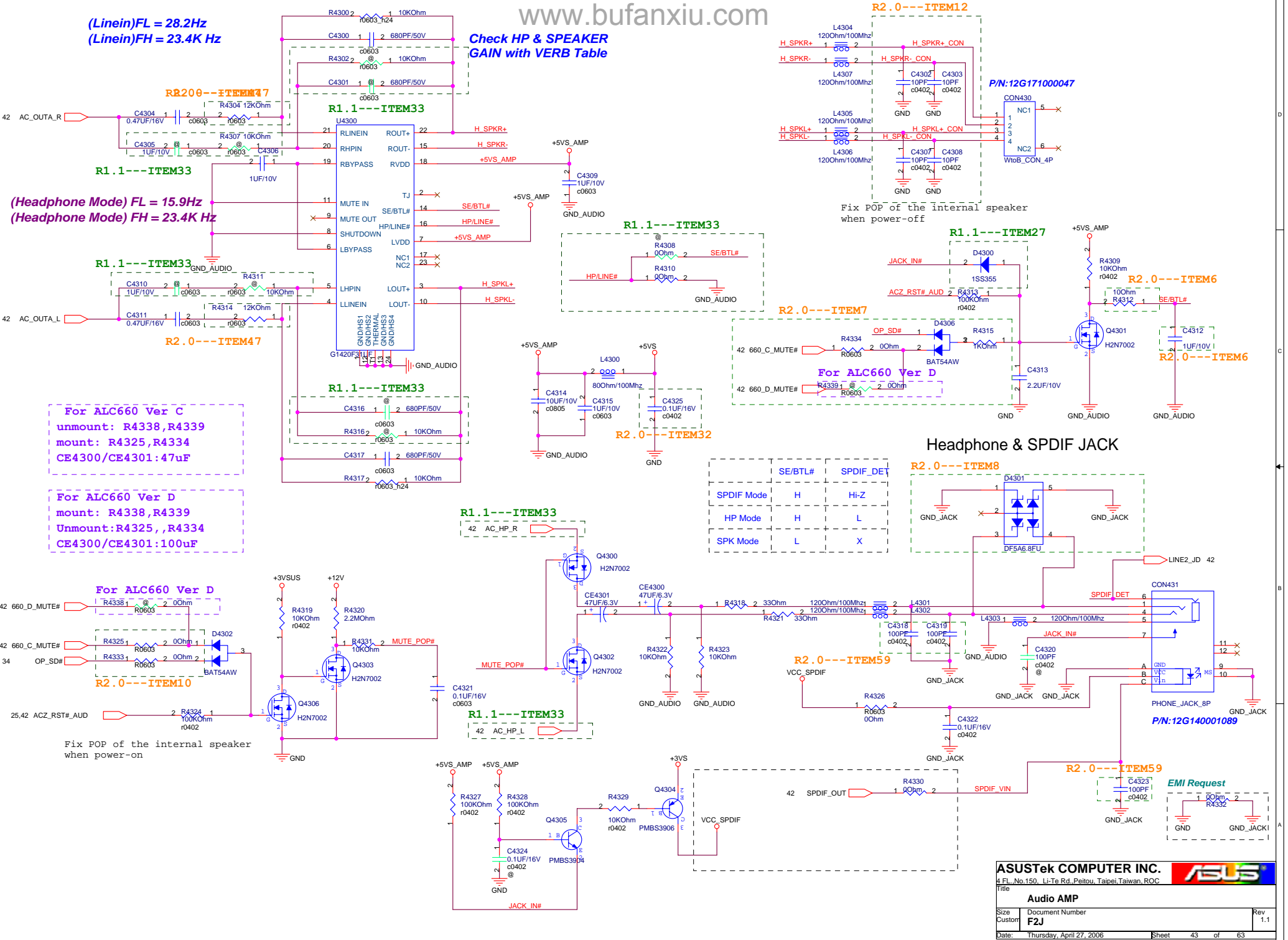






(Linein)FL = 28.2Hz  
(Linein)FH = 23.4K Hz

Check HP & SPEAKER GAIN with VERB Table

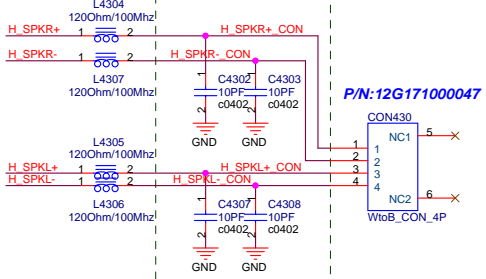


(Headphone Mode) FL = 15.9Hz  
(Headphone Mode) FH = 23.4K Hz

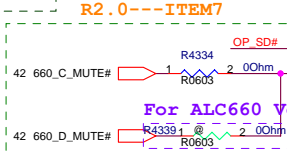
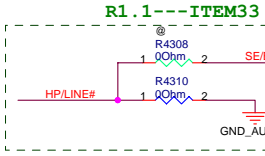
For ALC660 Ver C  
Unmount: R4338, R4339  
mount: R4325, R4334  
CE4300/CE4301: 47uF

For ALC660 Ver D  
Unmount: R4325, R4334  
mount: R4338, R4339  
CE4300/CE4301: 100uF

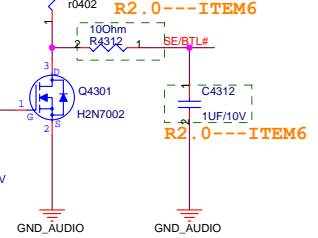
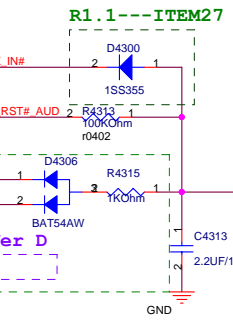
R2.0---ITEM12



Fix POP of the internal speaker when power-off

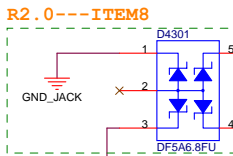


For ALC660 Ver D

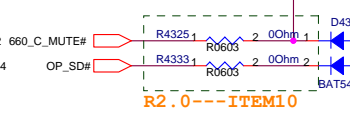


Headphone & SPDIF JACK

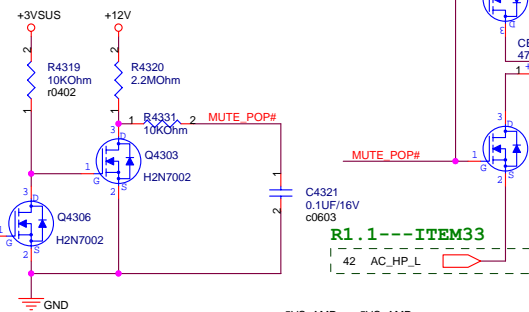
	SE/BTL#	SPDIF_DET
SPDIF Mode	H	Hi-Z
HP Mode	H	L
SPK Mode	L	X



For ALC660 Ver D



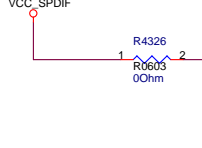
Fix POP of the internal speaker when power-on



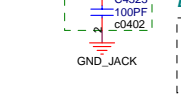
R2.0---ITEM32



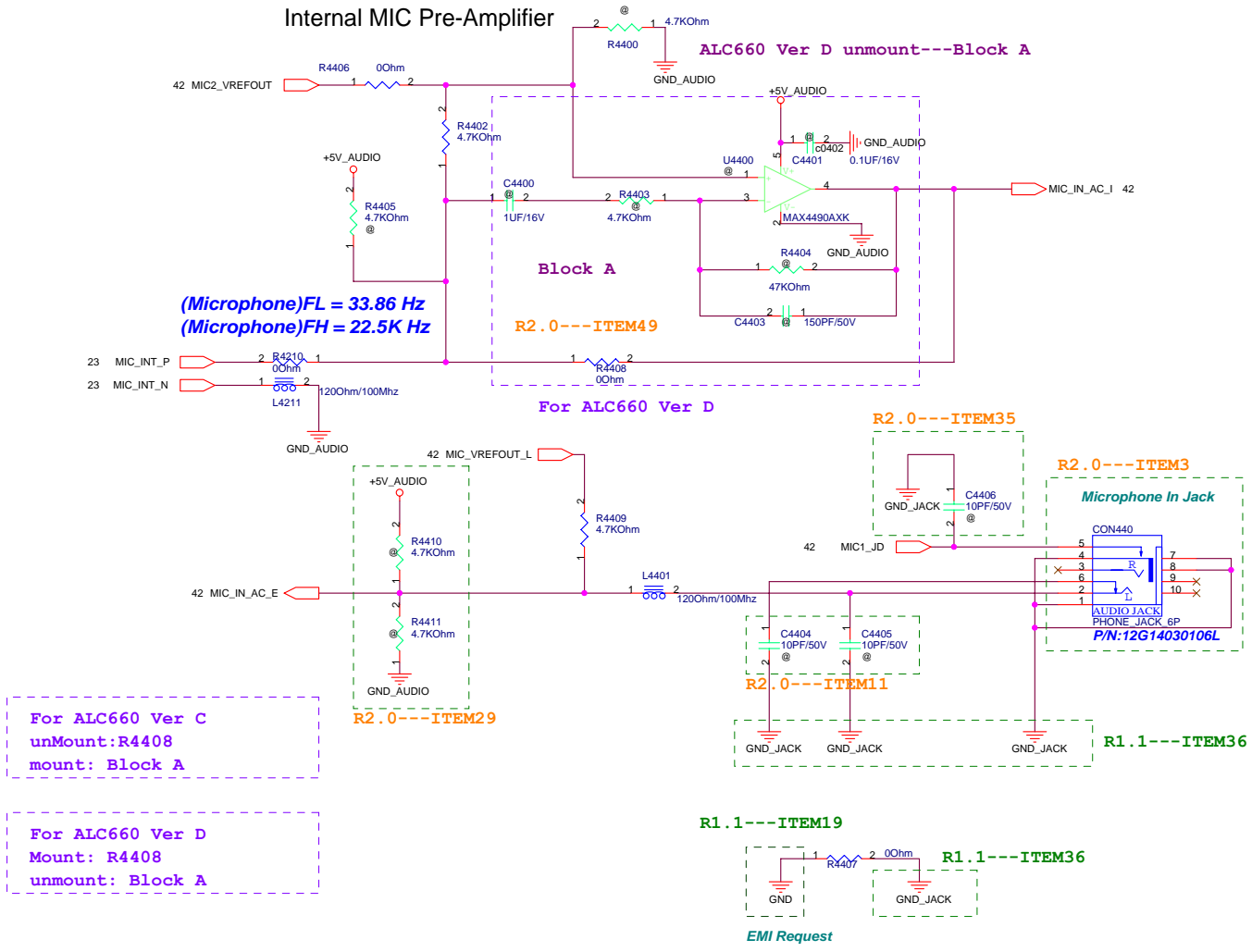
R2.0---ITEM59



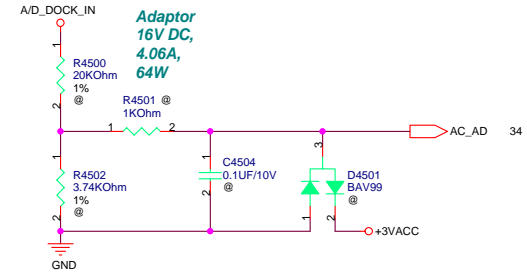
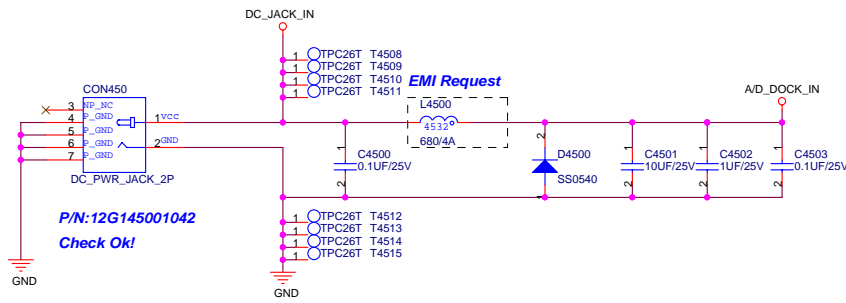
R2.0---ITEM59



ASUSTEK COMPUTER INC.

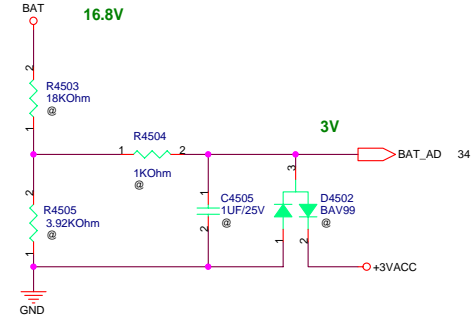
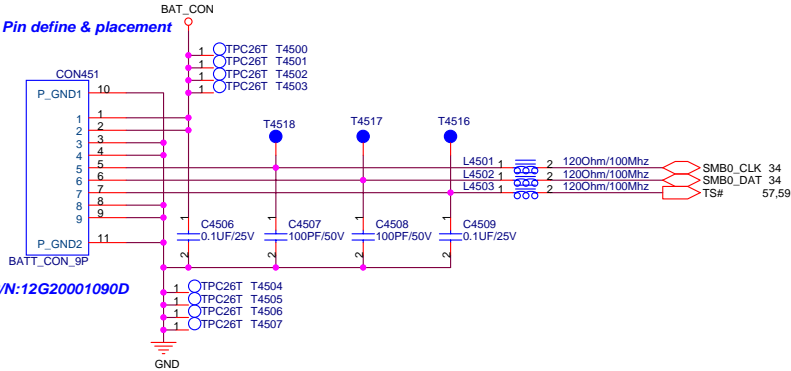


DC IN

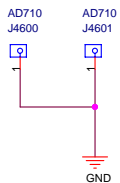


BAT IN

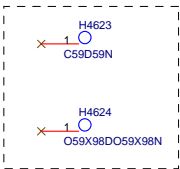
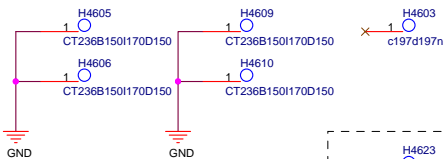
Check Pin define & placement



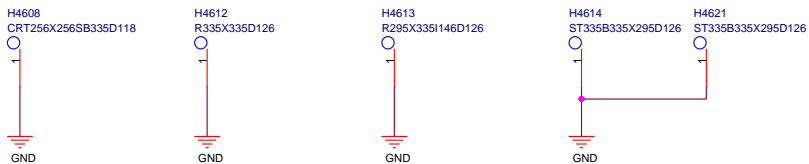
EMI SPRING



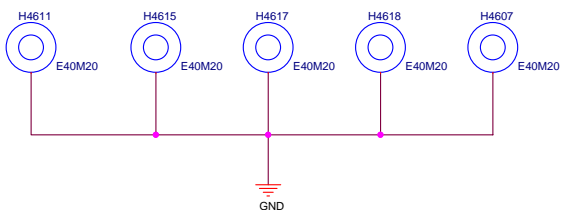
CPU(PTH)



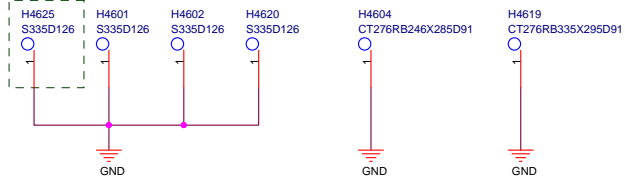
PTH



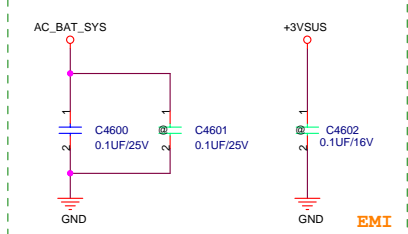
VGA & FAN(NUT)



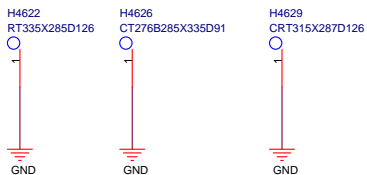
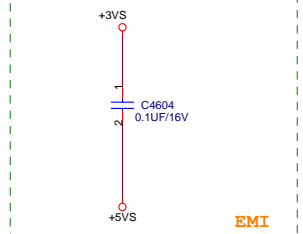
R1.1---ITEM29



R2.0---ITEM36



R2.0---ITEM37



## F2J SR\_0309 (R1.0---->R1.1)

- (1)MDC NUT( H3700, H3701) change to 13GN7510M270(H:3mm).---Page37
- (2)MDC CON change the mating height to 3mm(12G161200120).---Page37
- (3)Change USB CON(CON300,CON301) to 12G130011045 for ID request.---Page30
- (4)Del (2pin MDC CON,CON332) ,C3336,C3337---Page33
- (5)Change DVI CON(CON210) to black type.(P/N:12G100190241)---Page21
- (6)Change LAN CON(CON331) to 12G142111081 for ID change---Page33
- (7)Mount Q3909(2N7002) to fix BT can't turn off with Hot key(FN+F2) issue.---Page39
- (8)Change SB crystal X2500(32.768kHz) source.NOTE:C2500/C2502 change to 22pF.---Page25
- (9)Change C3407 from 0.1uF to 0.33uF to meet EC EC\_RST# & CLK timing.---Page34
- (10)Mount R2048(0ohm) , uumount R1731 to fix the LCD screen show white color Background during the boot beginning.---Page17, Page20.
- (11)Mount R729(33ohm) to support M54 27MHz spread spectrum(down spread -0.5%) for EMI request.---Page7
- (12)USB CAP(CE3002) change to Niobium Oxide Capacitor(47uF) for ESD issue.---Page30
- (13)Reserved HDCP (High-Bandwidth Digital Content Protection) for DVI: Reserved R1741-R1743(10K ohm) , U1702(M25P10\_AVMN6TP)---Page17
- (14)Add pull low RES R3313(1Kohn) to PLT\_RST#\_BUF.  
NOTE:RTL8111B(pin20,PERSTB) has leakage current problem(about 0.6V).---Page33
- (15)Change 1000 BASE-T TRANSFORMER(U3701) to BOTHHAND/GSM5009.---Page37
- (16)Change Microphone In Jack CON440 to 12G140001067 for EMI request.(Without metal ring)---Page44
- (17)Change X3301 External capacitance(C3335,C3334) from 27pF to 22pF.---Page33
- (18)Express card reset signal control by R5538D001:
  - a.R3205 Mark DNI.
  - b Mount R3201& change from 1K ohm to 2.2K ohm.(For ASUS Debug card issue)
- (19)MIC CON GND R4407 tie to digital GND for EMI request.---Page44
- (20)Add R2910 0ohm to IDERST for EMI request.---Page29
- (21)GND\_USB Reserved RES 0 ohm( R4008, R4014) to GND for ESD issue.--- Page40.
- (22)Speaker signal R4301,R4303,R4305,R4306 change to 120 ohm bead/600mA(L4304,L4307,L4305,L4306) & Mount 100pF Cap:C4302,C4303,C4307,C4308 for EMI request.---Page43
- (23)R4208,R4209,R4210 change to 120 ohm bead for EMI request.---Page42
- (24)Add Poly Pulse(F2100,0.2A) to +5VS\_DVI for safety request.---Page21
- (25)Change VRAM(U2200,U2204,U2205,U2206) to INFINEON HYB18T256161AFL-25---Page22
- (26)Change C2808 to 11G233210625361(10uF/0603/X5R) for high limitation(under moden module).---Page28
- (27)Change D4300 to 1SS355 for space limitation.---page43
- (28)Add depop signal 660\_C\_MUTE# for Reltek recomment.---Page42,43.
- (29)Add H4625 for EMI request.---Page46

## F2J SR\_0225 (R1.0---->R1.1)

- (30)Reserved C2317, C2318(100pF) for EMI request.---Page23
- (31)R4304, R4314 change from 10K to 11K to meet speaker(1W). (Note: about 0.84W)---Page43
- (32)Reserved C621-C625 to Vcore power for EMI request.---Page6
- (33)Reserved audio co-layout schematic for vista(ALC861-VD) in the future.---Page42-Page44
  - a. Every codec port must connect to one and only audio jack. No shared-port thing is allowed in vista---internal MIC & external MIC separated, HP & speaker separated.
  - b.Internal MIC: Version C---Add per AMP, Version D---Del per AMP.

## F2J SR\_0227 (R1.0---->R1.1)

- (34)Changed external cap C716 & C717 of X701(xtal=14.317893 MHz) from 22 PF to 27pF. (To solve TV Burst frequency fail issue)---Page7
- (35)Card Reader Control(U4000, GL817E) change to version 10.P/N update to 02G730000410.---Page40
- (36)GND\_MIC change to GND\_JACK.
- (37)Mount C4404,C4405, reserved C4406 to solve MIC CON ESD issue---Page44.

## F2J SR\_0306 (R1.0---->R1.1)

- (38)Add R3422,R3423(0ohm) for ICT test.---Page34
- (39)Change the MIC CON--CON440(pin5,pin4) to normal open type to meet vista request.---Page44
- (40)SWAP RN3320,L3306 for layout request.---Page33
- (41)Change SATA CON(CON291) to 12G15110022R for SMT issue.---Page29
- (42)Change VGA thermal sensor (U1701) to G781-1(SLAVE address:9A) & connect SMBUS to EC.---Page17.
- (43)Add Q3202-Q3204, R3216,R3217,T3207 for newcard debug card.

## F2J SR\_0313 (R1.0---->R1.1)

- (44)Component change for debug-card detection circuit:C3207(1000p) to 2200p and C3208(2200p) to 0.1u.---Page32
- (45)R3201 change from 2.2K to 1K.(New card debug card will modify 11KHz CLK damping RES).---Page32
- (46)R3900 change from 330ohm to 200ohm to enhance power LED luminance for ME request.---Page39

## F2J SR\_0315 (R1.0---->R1.1)

- (47)C4404,C4405 change from 1000pF to 100pF for EMI request.---Page44
- (48)TPMCLK: Mount C719(33pF), R741 changed from 33ohm to 10ohm for EMI request.---Page7
- (49)CRT filter:L2401-L2402 change to 56NH, C2402,C2404,C2406 mark DNI.---Page24

- (1)con331 change to P/N:12G142111083.(防呆)--Page33
- (2)Add TP for ATS test: +RTCBAT--R2501(pin2), PWRSW#--SW3800(pin1), L4501( pin1),L4502(pin1) ,L4503(pin1)
- (3)MIC JACK(CON440) change to 12G14030106L(no metal ring) for ID request.--page44
- (4)To solve S3 resume time too long issue: Blue Tooth power change from +3VS to +3V: CON390(pin8),R3907(pin1).---Page39
- (5)Modify Card Reader circuit to solve can't into C3/C4 & S3 aging fail issue:---Page40
  - a.Del EEPROM(U4001), C4014. It's not necessary.
  - b.Add PMOS(Q4002), R4015, D4003, D4004, D4005.(Use card detect pin to turn on chip power)
  - c. Rename +3V power change to +3V\_CR.
- (6)To solve system shutdown "speaker POP" noise issue: C4312 chnage from 2.2uF to 1uF/10V,R4312 change from 100K to 10 ohm.--Page43
- (7)To solve system into S3/S4 "speaker POP" noise issue: Add R4334(0ohm), D4306 & Reserved R4339(0ohm), R4315 change from 10K to 1K ohm.--Page43
- (8)Mount D4301 for ESD issue.
- (9)R4215 change to 4.7K to make sure 660\_C\_MUTE# low DC leve about 0.4V at Q4306(pin1), Q4313(pin1).
- (10)To solve HP "pop" noise: Mount R4333(0ohm), R4325(0ohm).
- (11)MIC CON change to no metal ring(Don't have ESD issue): Mark C4404,C4405 to DNI.--Page44
- (12)C4302,C4303,C4307,C4308 change from 100pF to 10pF/50V for ESD.--Page43
- (13)R3206 pull Hi change to +5V---Page32
- (14)Modify LPC\_AD3\_L Q3204 circuit for new card debug card.---Page32
- (15)Mount Q3102 to solve Aragon wireless lan module can't turn off with hot key(Fn+F2) issue.---Page31
- (16)Change the materia of SW3800-SW3806 to stainless steel to improve the yield rate.---Page38
- (17)Change SATA CON(CON291) to 12G15110022U.更改魚叉長度(改短)---Page29
- (18)Del L3000, L3001, L3002 EMI co-lay common chock.---Page30.
- (19)Del L3303.L3304.L3305.L3306 EMI co-lay common chock.---Page33.
- (20)Del L3900 EMI co-lay common chock.---Page39.
- (21)Del L3501 EMI co-lay common chock.---Page35.
- (22)Chang S-vedio(CON241) from 12G141011077 to 12G14101107K to improve the yield rate.---Page24
- (23)Reserved R3424-R347(0ohm) for new card debug card.---Page34
- (24)Card Reader POWER change from +3V to +3VS(Mount :R4017, 0603 0ohm, Reserved:R4016)---Page40(Fix S3 device disappear issue)
- (25)Add CR\_POWER# signal to fix reboot card reader disappear issue. (Add Q4307, EC(pin41,GPD4)---Page34,40
- (26)Modify LID signal circuit(Add D2303) to avoide the LID signal to damage the EC(pin24).---Page23
- (27)Reserved Cap C4014,C4019(4.7uF) for card reader AVDD power.
- (28)Add CR\_DRIVER# signal & D4007 to solve install card reader driver issue.---Page40,34
- (29)Reserved R4410 & R4411 for external MIC VREF.---Page44.
- (30)Del L3200 EMI co-lay common chock.---Page32
- (31)Del L2320 EMI co-lay common chock.---Page23
- (32)Add C4325(0.lu) to +5VS for EMI request.---Page43
- (33)Mount D3500 & C3503(10uF) for finger printer ESD issue.---Page35
- (34)Reserved PC5025(0.luF) to VR\_PWRGD for ESD.---Page50---check power.
- (35)Reserved C4406(10pF) to MIC1\_JD for ESD issue.---Page44
- (36)Add C4600,C4601(0.luF/25V) to AC\_BAT\_SYS & C4602(0.luF/16V) to +3VSUS for EMI request.---Page46
- (37)Add moat cap C4604(0.luF) for EMI request. (+3VS & +5VS).---Page46
- (38)Reserved C3714(1000pF) for EMI request.---Page37(Check LAN eye patten).
- (39)R2116,R2117 change to 600ohm/bead for DVI EMI issue.---Page39.
- (40)DVI polyfuse F2100 change to 07G0140200L.(It has TUV/UL)---Page21.

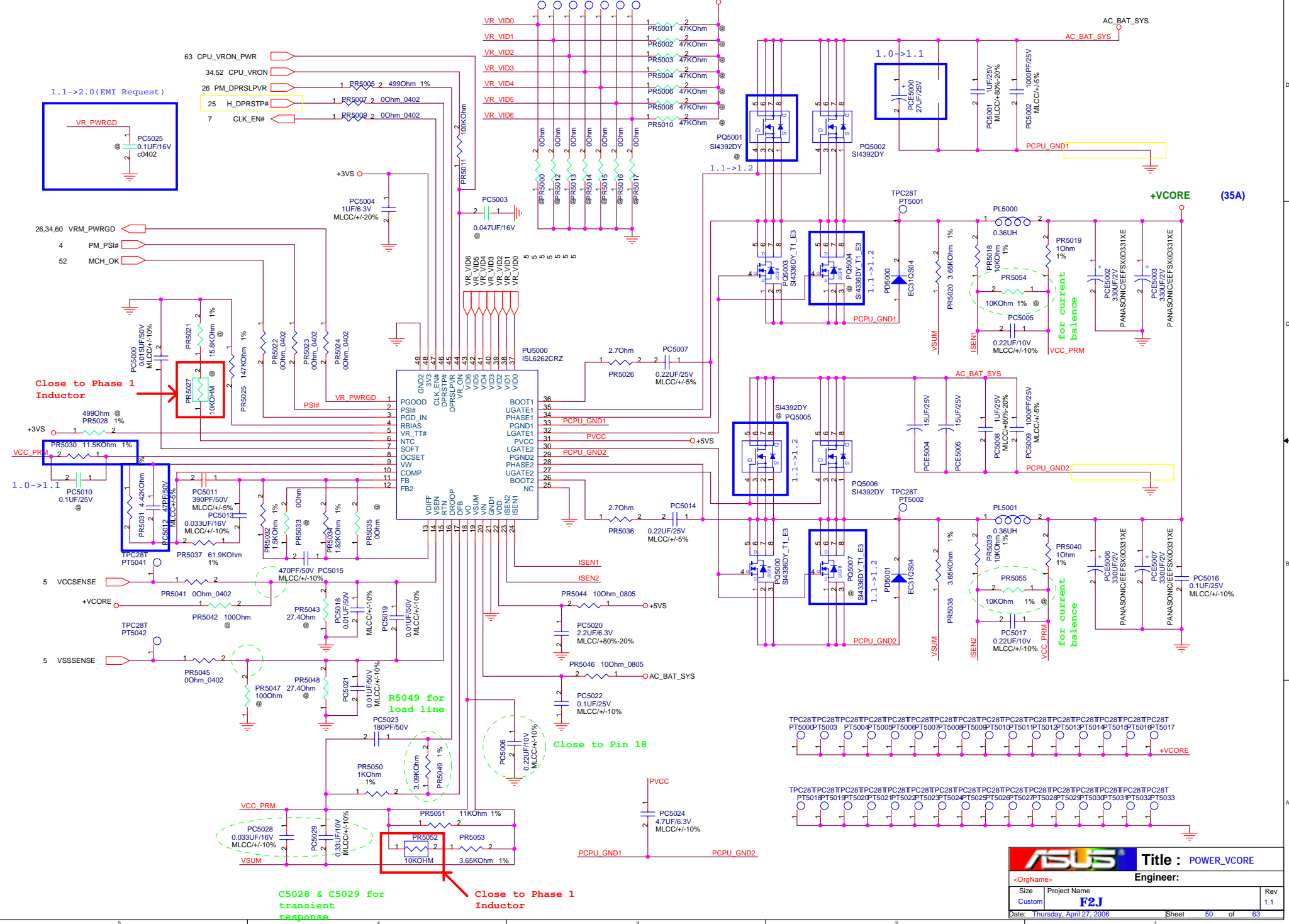
- (41)Add C2152(0.luF) to +5VS\_DVI for EMI request.---Page21
- (42)Mount C2108 & C2109(10pF) to DVI DDC CLK/DAT for EMI request.---Page21.
- (43)Add C3909(0.luF/16V) to BT power(+3VS) for EMI request.---Page39
- (44)Rerved C3901-C3904(0.luF) & C3905-C3908(10pF) for EMI request.---Page39
- (45)USB external port add common mode chock L3000-L3002 for EMI request. ---Page30
- (46)Del FAN DA circuit(It's not necessary) ---Page36
- (47)R4304 change from 11K ohn to 12K ohm to meet speaker 1W(1KHz, about 0.857 W).
- (48)C4002 change from 330pF to 0.047uF to meet card reader reset timming.(1.03ms)
- (49)Del internal MIC PRE-AMP.(Audio dirver continue using F3J,It's not necessary)---Page44  
Del:C4400,R4403,U4400,R4400,C4403,C4401  
Mount:R4408
- (50)Mount R4008 for EMI request.(card reader ESD issue).
- (51)USB power R3001-R3003 change to 180 ohm/bead.(2A) for EMI request.
- (52)R3308 change to 120 ohm/bead (600mA) for EMI request.---Page33.
- (53)R2115 change from 0ohm to bead (120ohm/600mA) for DVI EMI issue.---Page21
- (54)For CRT EMI issue:(EE check R,G,B signal quality "OK".)---Page24  
Mount C2402,C2404,C2406 10pF,  
Change L2400,L2401,L2402 from 56nH to 82nH.  
Change C2401,C2403,C2405 from 15pF to 22pF.
- (55)For CRT EMI issue:(HSYC,VSVC)---Page24  
Change R2400,R2403 from 0ohm to bead/120hm/600mA.  
Mount C2400,C2407 22pF.---EE must check signal quility.
- (56)For CRT EMI issue:(DDC)---Page24  
Change R2401,R2402 from 0ohm to bead/120hm/600mA.
- (58)Change R3803-R3806 from 330ohm to 390ohm for ID request.(Reduce the LED illumination)
- (59)Mount C4323, C4319, C4318(100pF) for EMI request.---Page43
- (60)ISA ROM(U3500) P/N change to 05G001014110.(Del socket)---Page35

F2J PR\_0501 (R3.0---->R3.1)

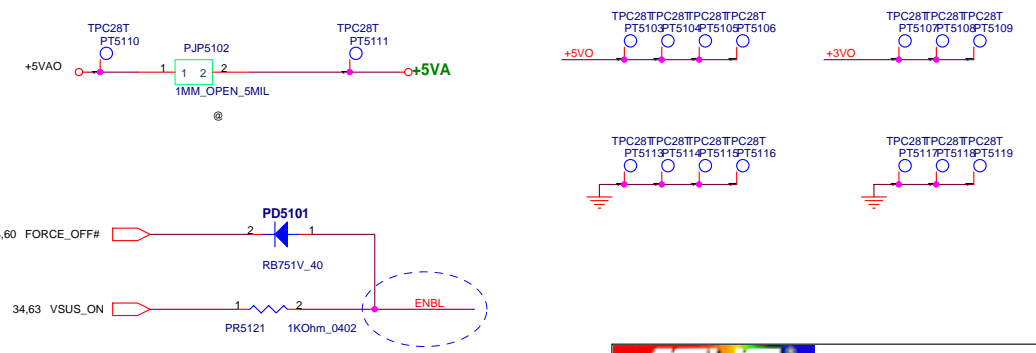
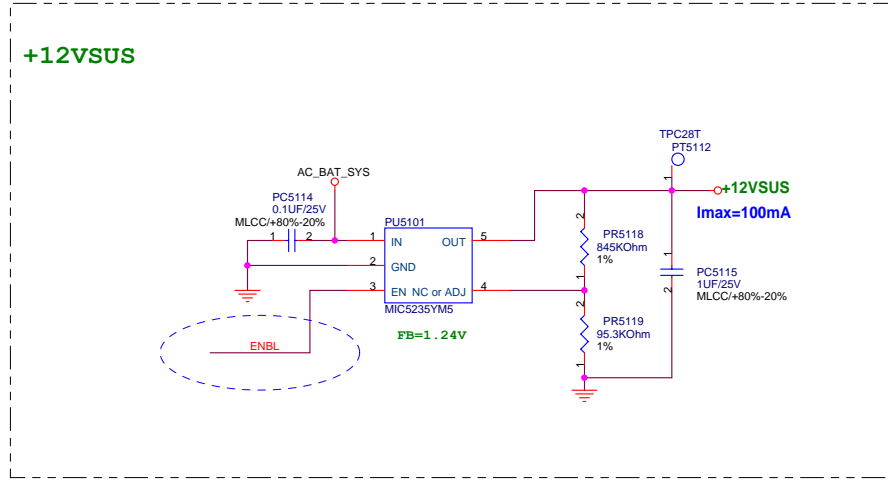
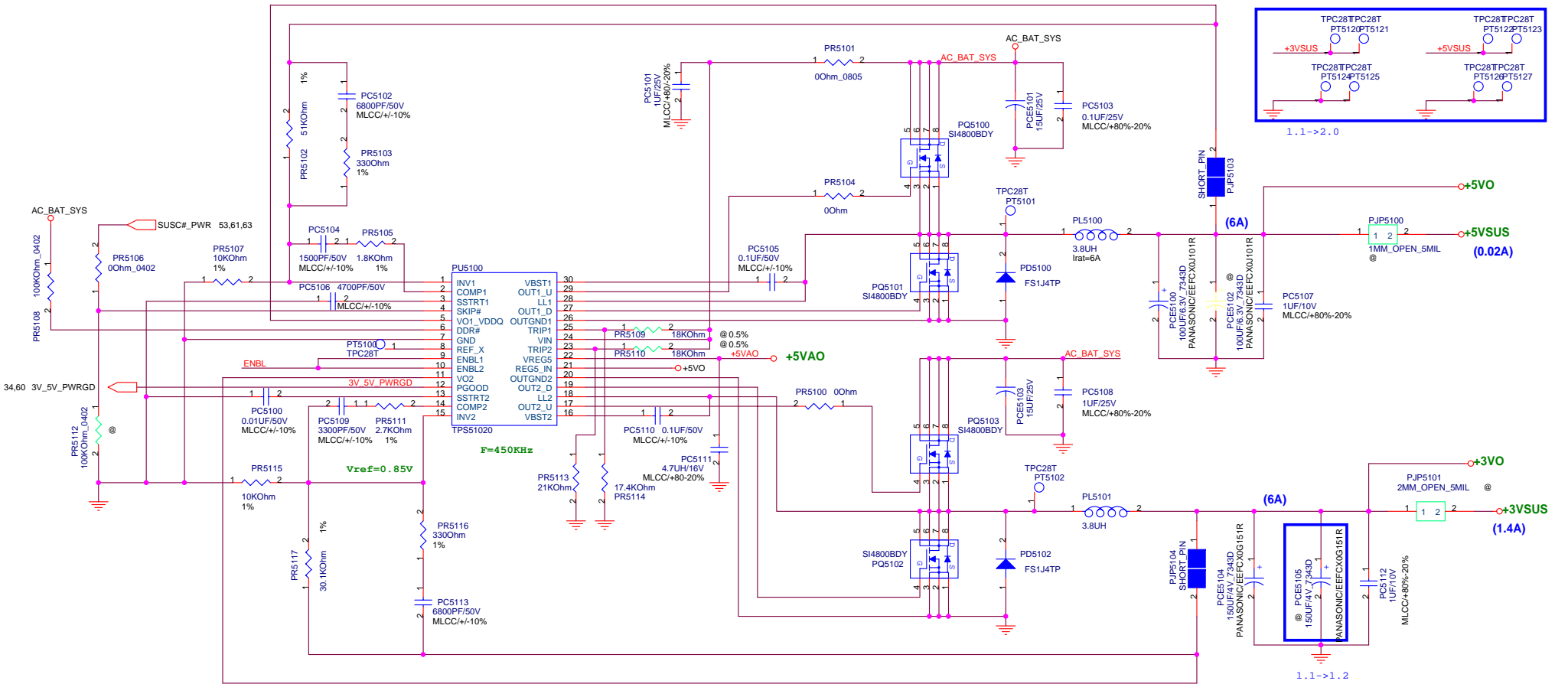
- (1)C4002,C4016 change the package from 0805 to 0402(10pF).---Page40.

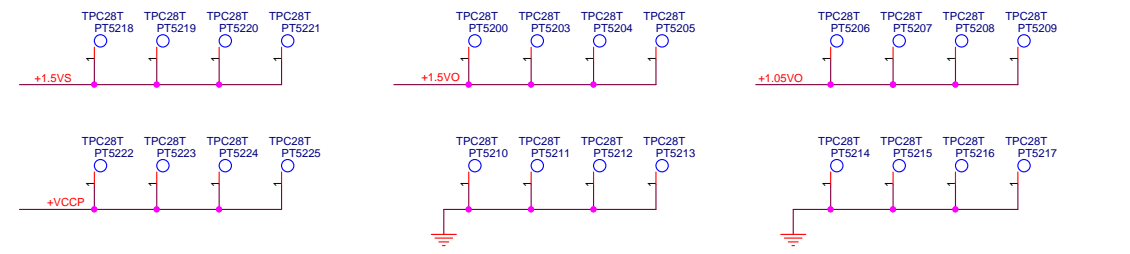
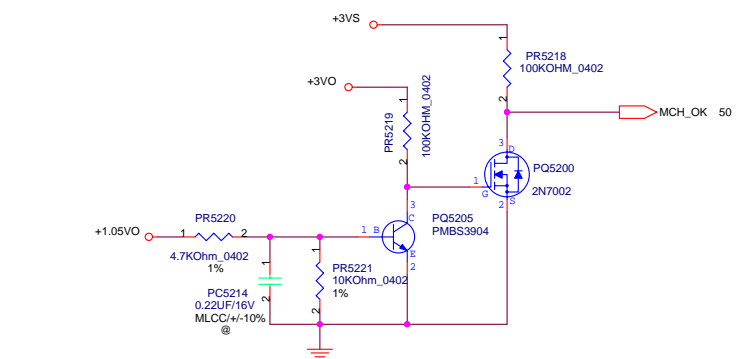
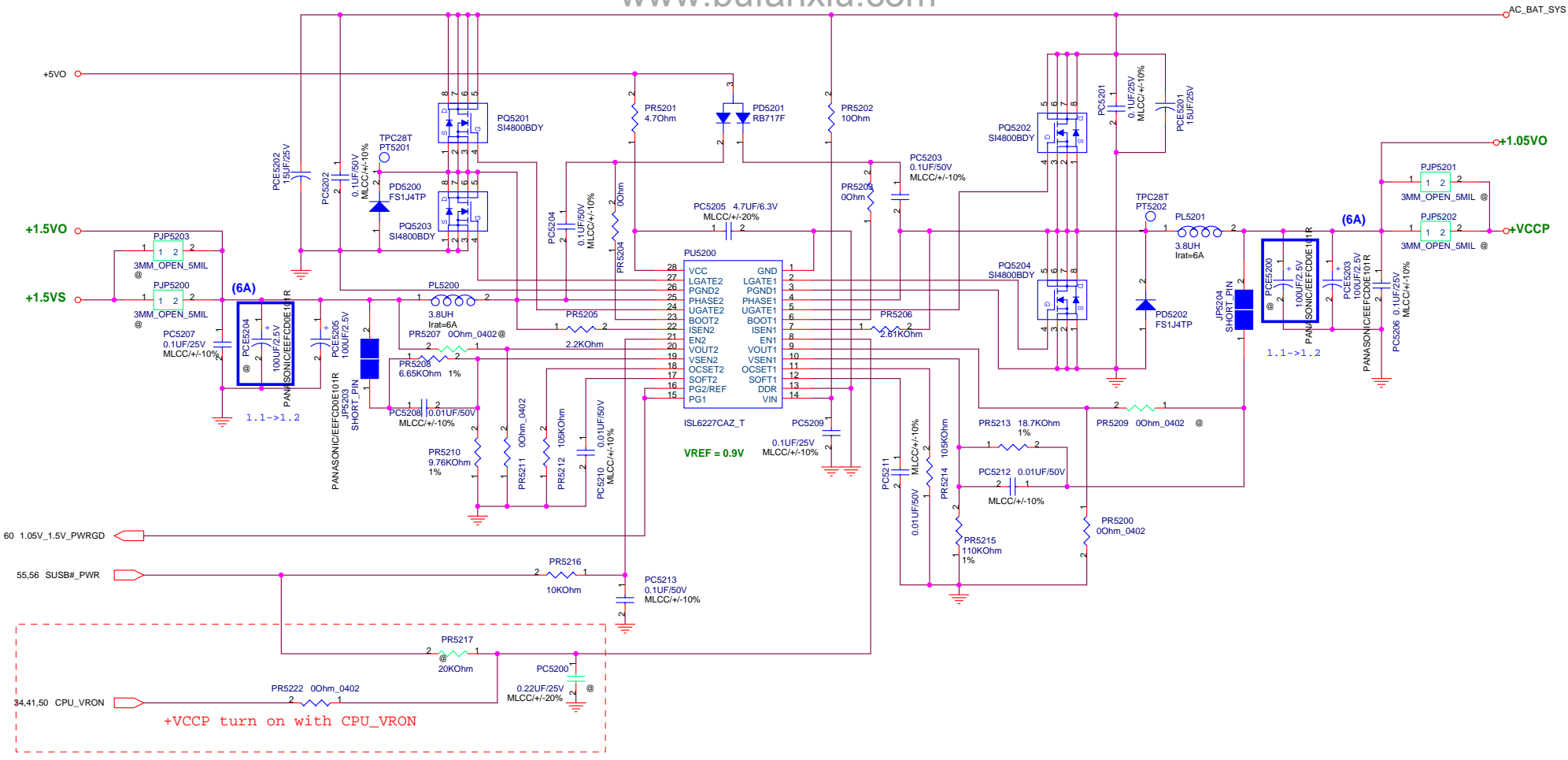


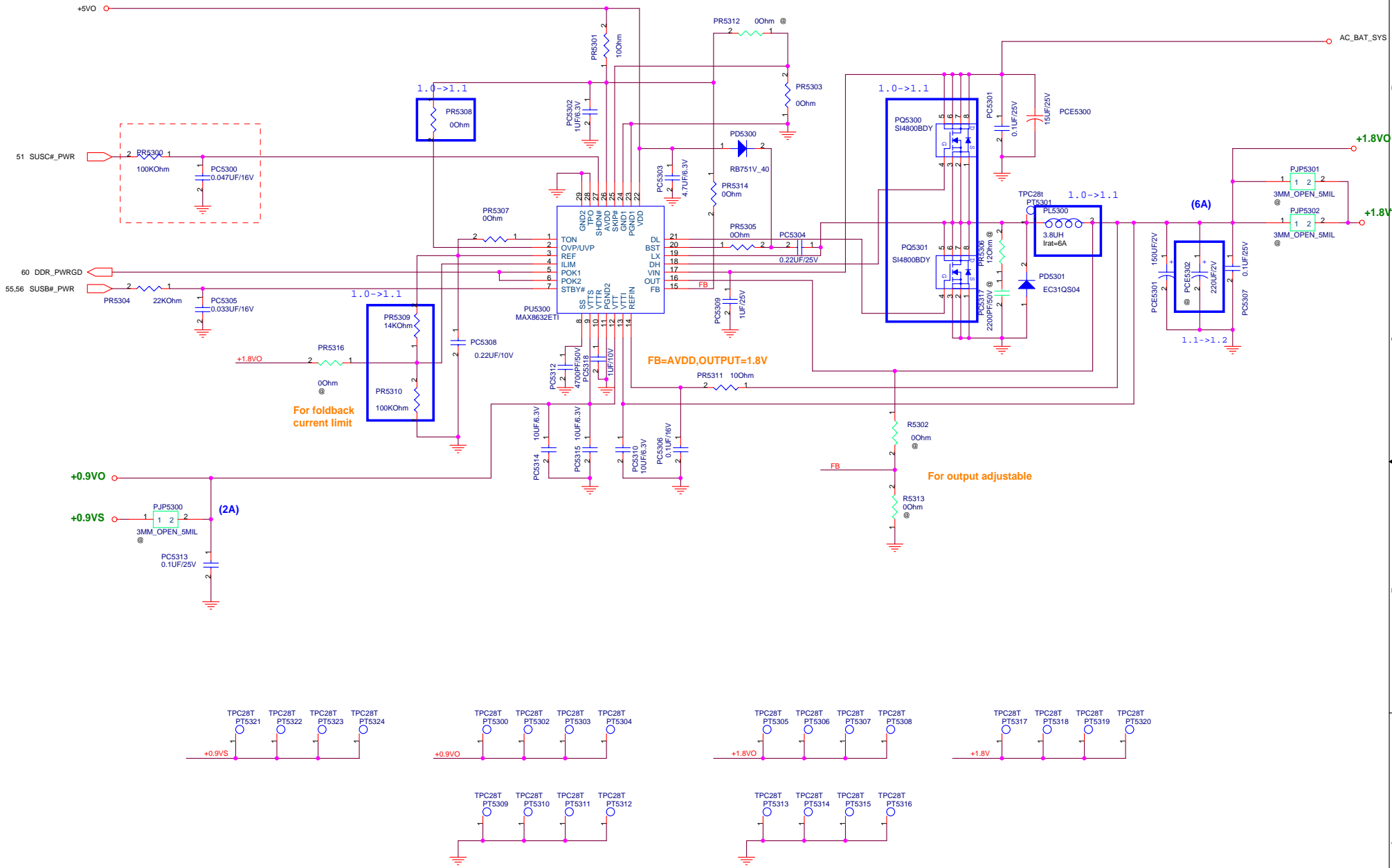
- (1)Modify +1.8V OCP, PL5300 change to 3.8UH, PR5308 change to 0 Ohm, PR5309 change to 14K Ohm, PR5310 change to 100K Ohm---Page53
- (2)Change +VGA\_VCORE\_0 to 1.1V, PR5504 change to 1.05K Ohm/1%.---Page55
- (3)Charger circuit modify PC5704 change to 1U/25V/0805, Add PQ5714 to fix bug---Page57
- (4)Disable PWRLMT# function, Unmount PR5725, PR5726, PC5717, PU5701, PC5718, PD5703, PR5724 ,PC5719, PC5720, PQ5712---Page57
- (5)Disable adapter error function, Unmount PR5905, PC5908, PR5907, PU5902, PC5906, PD5901, PR5906, PC5907, PR5908, PU5903, PQ5903---Page59
- (6)Modify BAT OVP circuit PR6010 change to 316K ohm /0.1%, PR6013 change to 75K Ohm/0.1%, unmount PR6015---Page60
- (7)Change PQ6106 to FDW2501 for VGS issue---Page61
- (8)Change input capacity, delete PCE5000 & PCE5001 15UF/25V, add PCE5000 27UF/25V,---Page50
- (9)Change capacity, PCE5701 & PCE5700 change to 27UF/25V,---Page57
- (10)Change Vcore OCP, PR5030 change to 11.5K Ohm--Page50
- (11)Vcore IC issue, PR5031 change to 4.42K Ohm & PC5012 change to 47PF ---Page50
- (12)Modify net name, change MAX1909\_REF to MAX8725\_REF ---Page57
- (13)Change input capacity, PC5903 change to 4.7UF/25V ---Page59



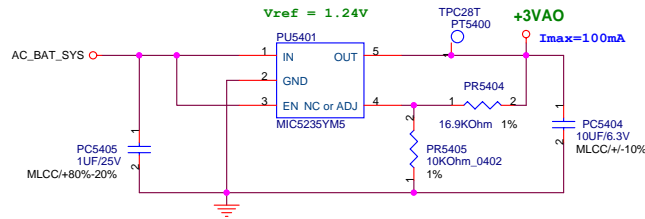
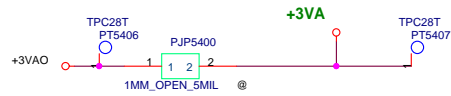
<b>ASUS</b>		<b>Title : POWER_VCORE</b>	
<OrigName>		Engineer:	
Size	Project Name	Rev	
Custom	<b>F2J</b>	1.1	
Date:	Thursday, April 27, 2006	Sheet	50 of 63



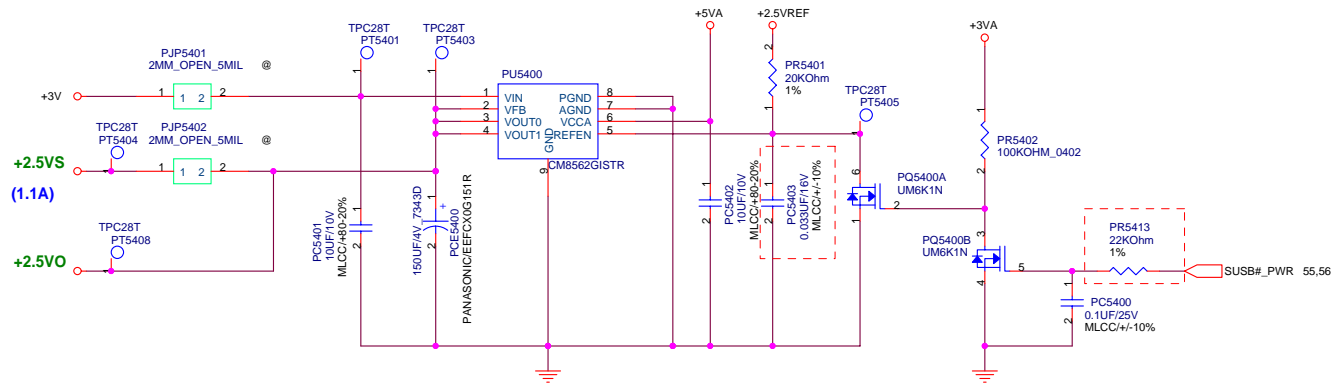


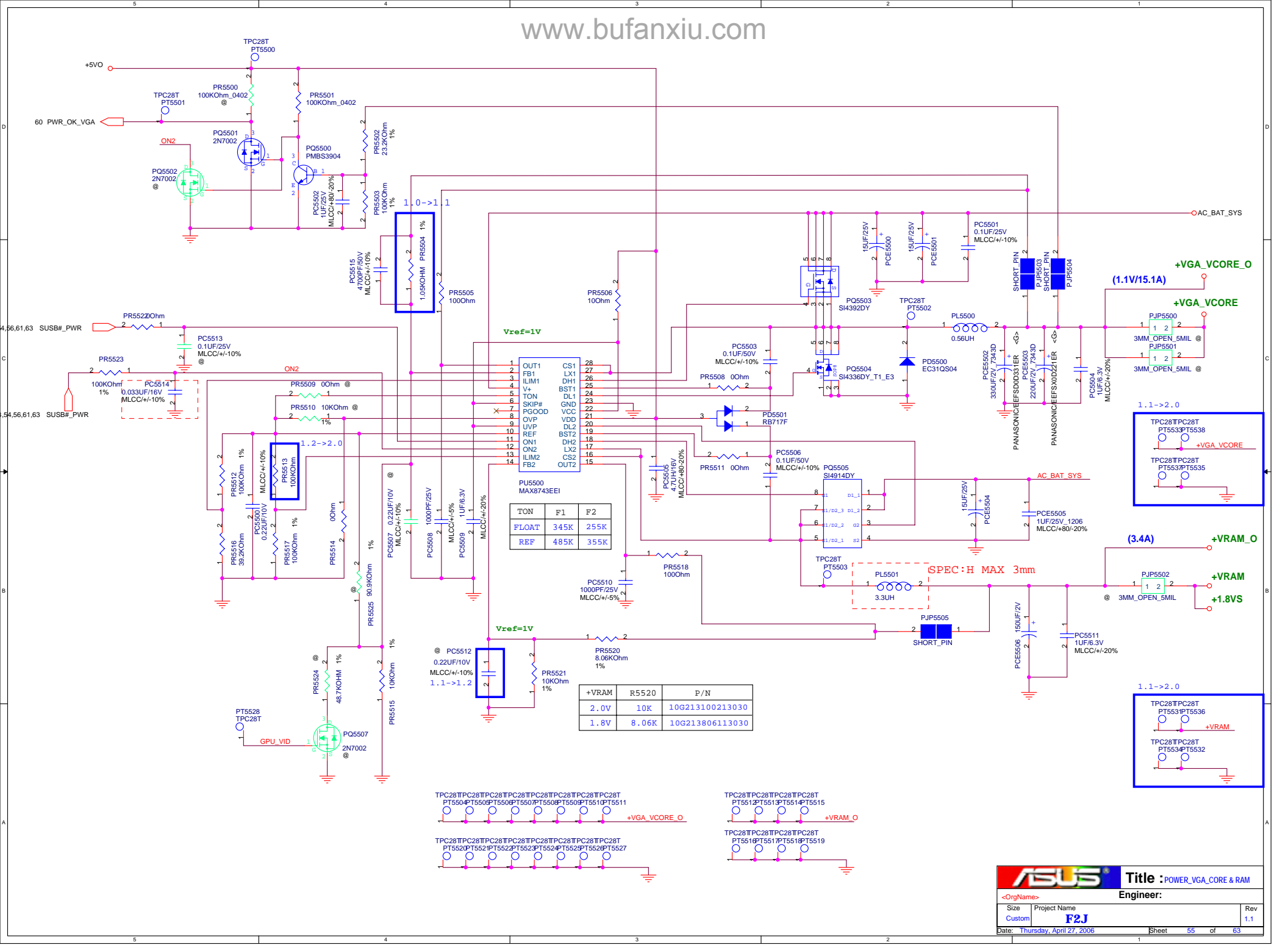


+3VAO



+2.5VS





Vref=1V

Vref=1V

TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

+VRAM	R5520	P/N
2.0V	10K	10G213100213030
1.8V	8.06K	10G213806113030

TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28  
PT5504PT5505PT5506PT5507PT5508PT5509PT5510PT5511

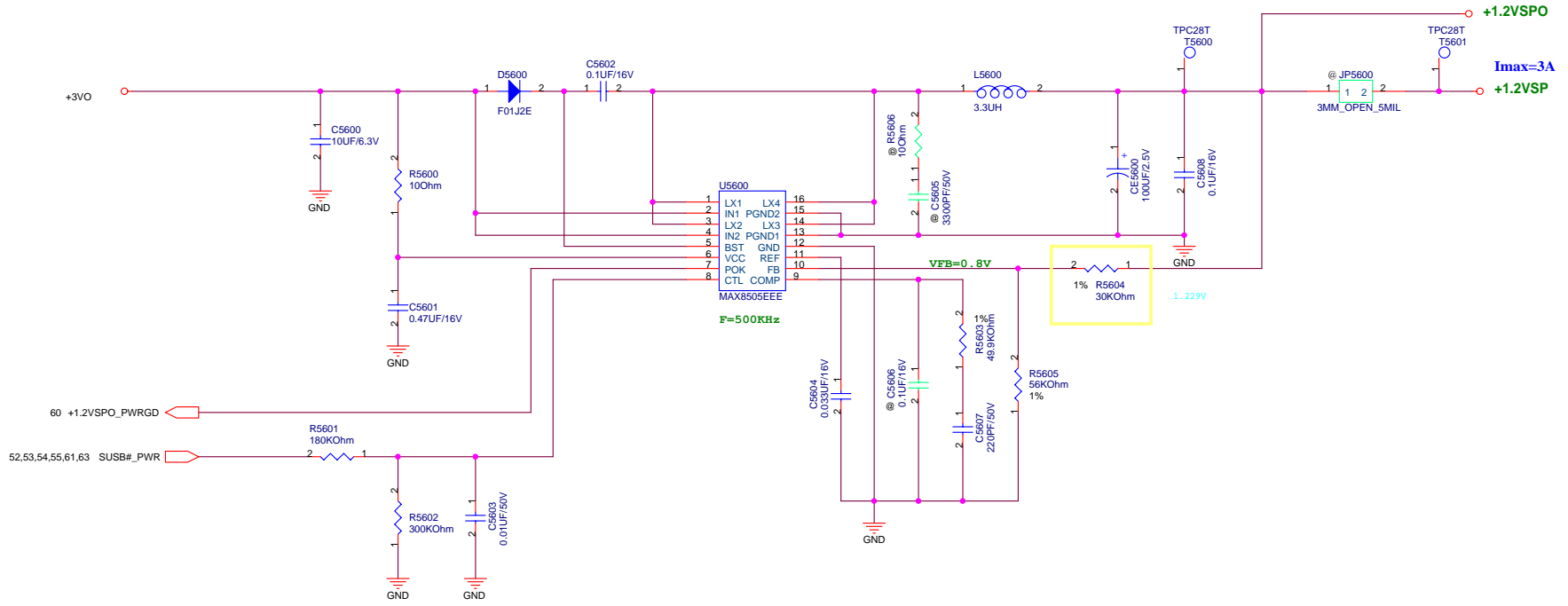
TPC28TPC28TPC28TPC28TPC28  
PT5512PT5513PT5514PT5515

TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28TPC28  
PT5501PT5502PT5503PT5504PT5505PT5506PT5507PT5508PT5509PT5510PT5511

TPC28TPC28TPC28TPC28TPC28  
PT5516PT5517PT5518PT5519

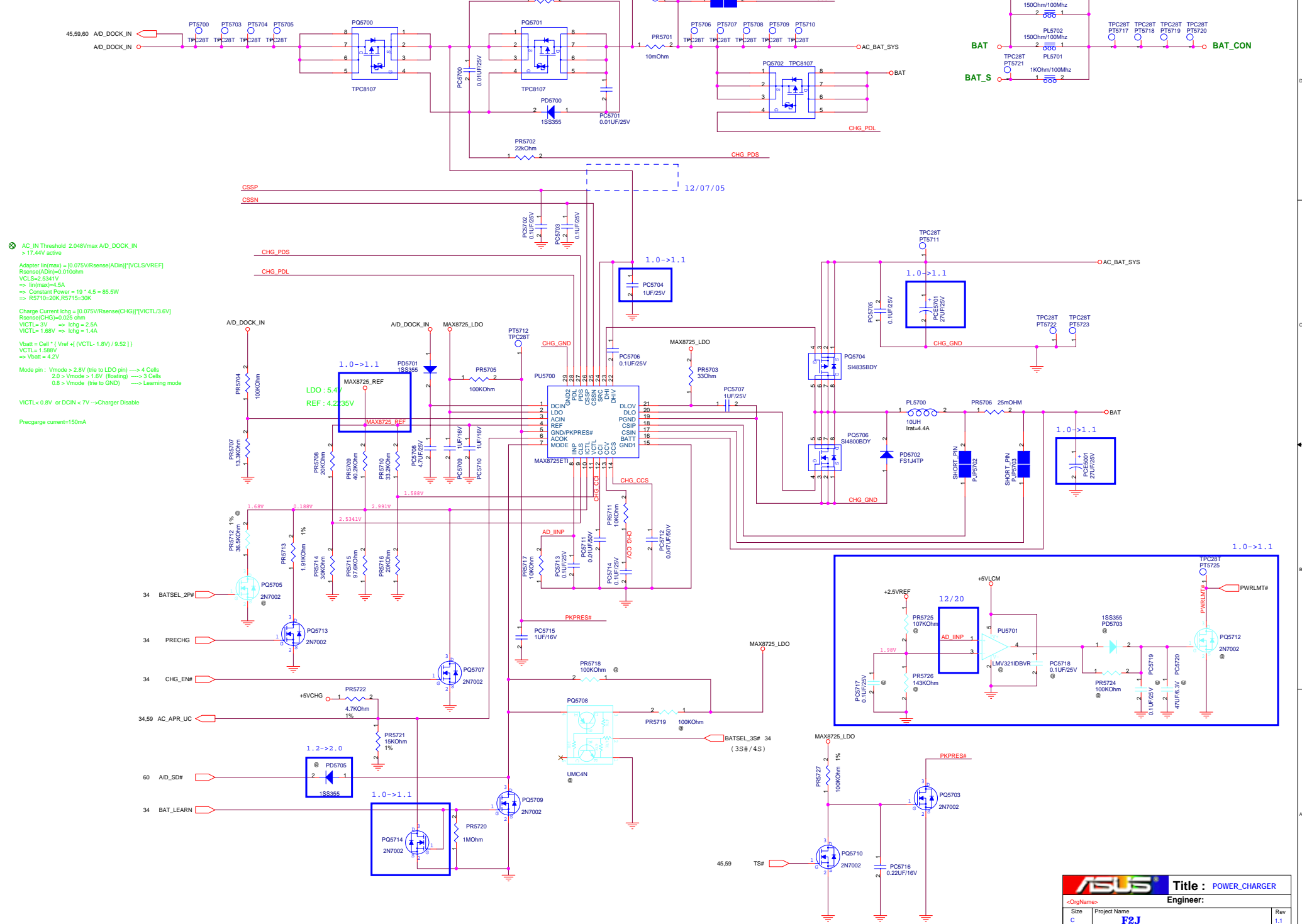
**ASUS** Title : POWER\_VGA\_CORE & RAM  
 <OrgName> Engineer:  
 Size Project Name  
 Custom F2J  
 Date: Thursday, April 27, 2006 Sheet 55 of 63

+1.2VSP

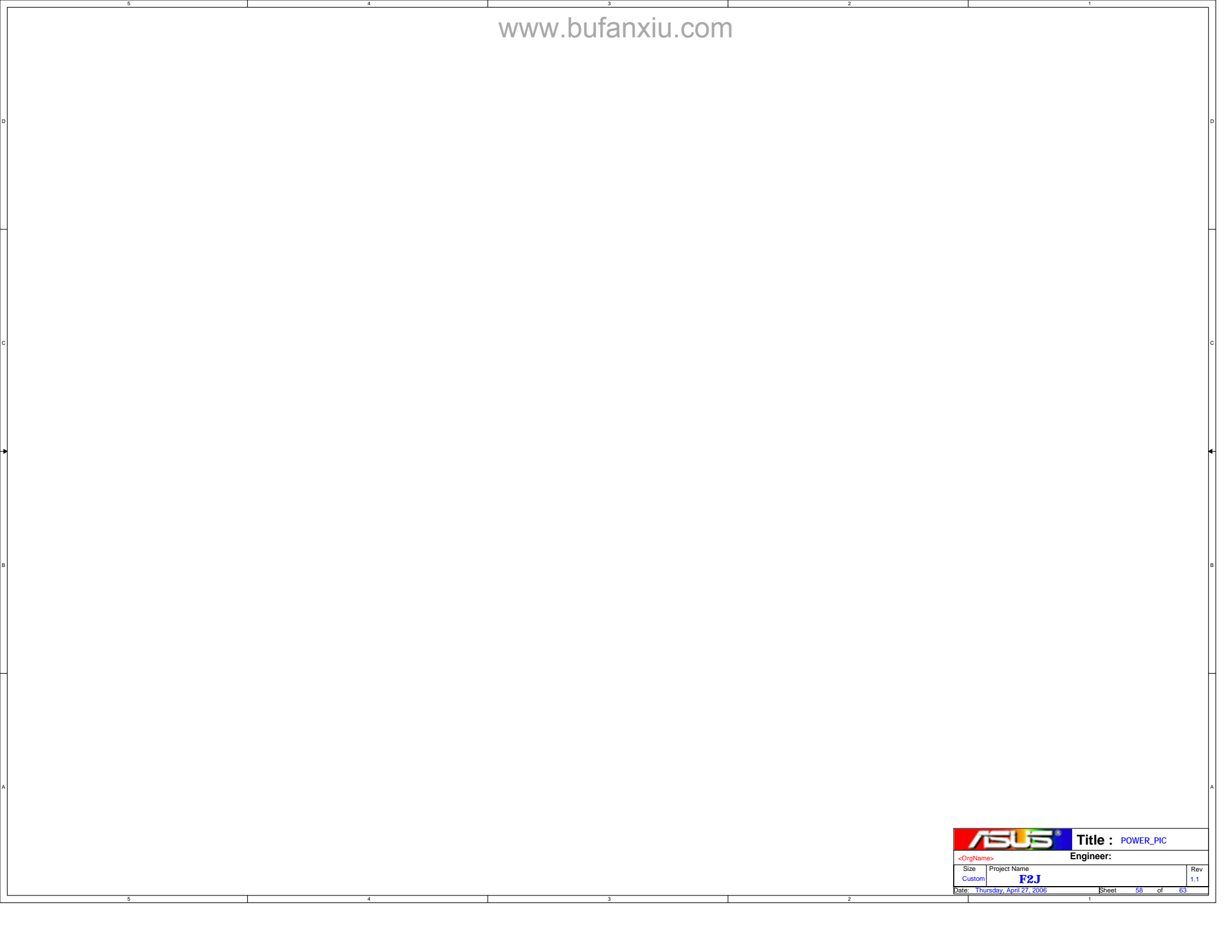




POWER PATH & BAT\_LEARN

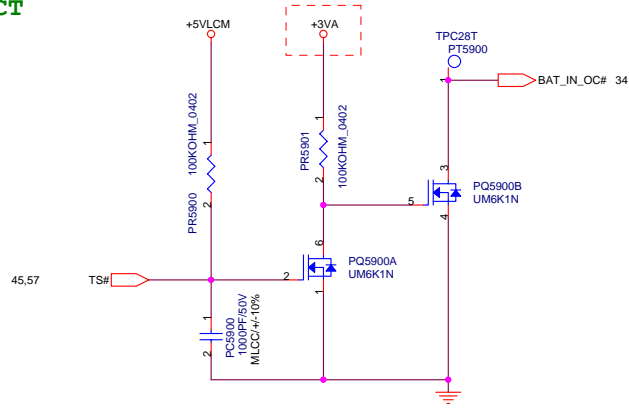


AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN > 17.44V active  
 Adapter In(max) = [0.075V/Rsense(Adin)]\*[VCLS/VREF]  
 Rnsense(Adin)=0.010ohm  
 VCLS=2.5341V  
 => In(max)=4.5A  
 => Constant Power = 19 \* 4.5 = 85.5W  
 => R5710=20K, R5715=30K  
 Charge Current Ichg = [0.075V/Rsense(CHG)]\*[VICTL/3.6V]  
 Rnsense(CHG)=0.025 ohm  
 VICTL= 3V => Ichg = 2.5A  
 VICTL= 1.68V => Ichg = 1.4A  
 Vbatt = Cell \* (Vref + (VCTL - 1.8V) / 9.52)  
 VCTL = 1.58V  
 => Vbatt = 4.2V  
 Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells  
 2.0 > Vmode > 1.6V (floating) -> 3 Cells  
 0.8 > Vmode (tie to GND) -> Learning mode  
 VICTL < 0.8V or DCIN < 7V -> Charger Disable  
 Precharge current=150mA

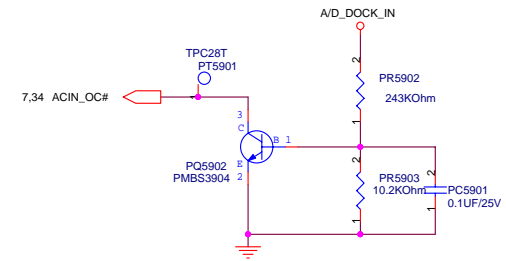


		<b>Title :</b> POWER_PIC	
<OrgName>		<b>Engineer:</b>	
Size	Project Name		Rev
Custom	<b>F2J</b>		1.1
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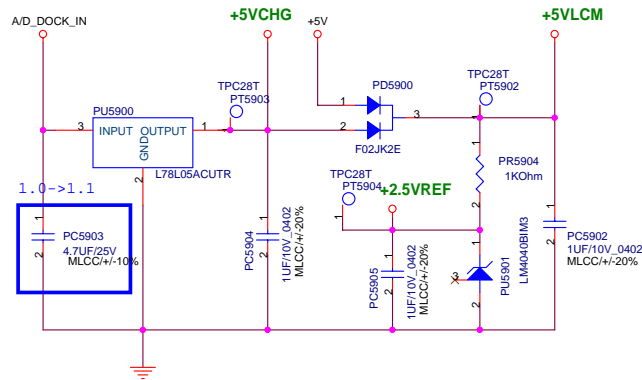
### BATTERY IN DETECT



### ADAPTER IN DETECT



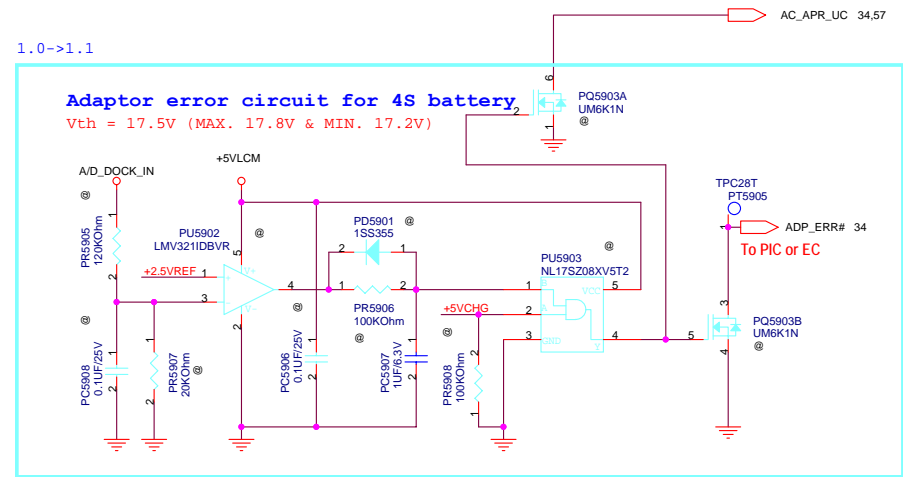
### +5VLCM, +5VCHG & +2.5VREF



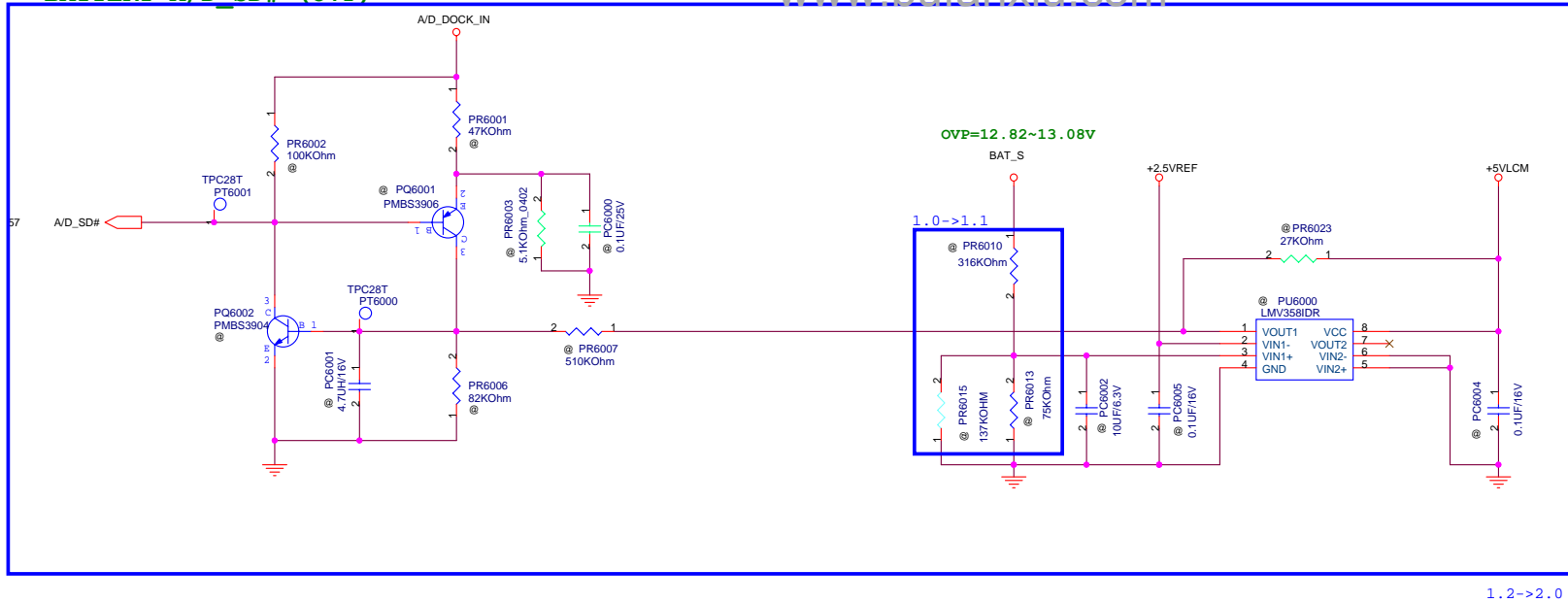
1.0->1.1

### Adaptor error circuit for 4S battery

Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)

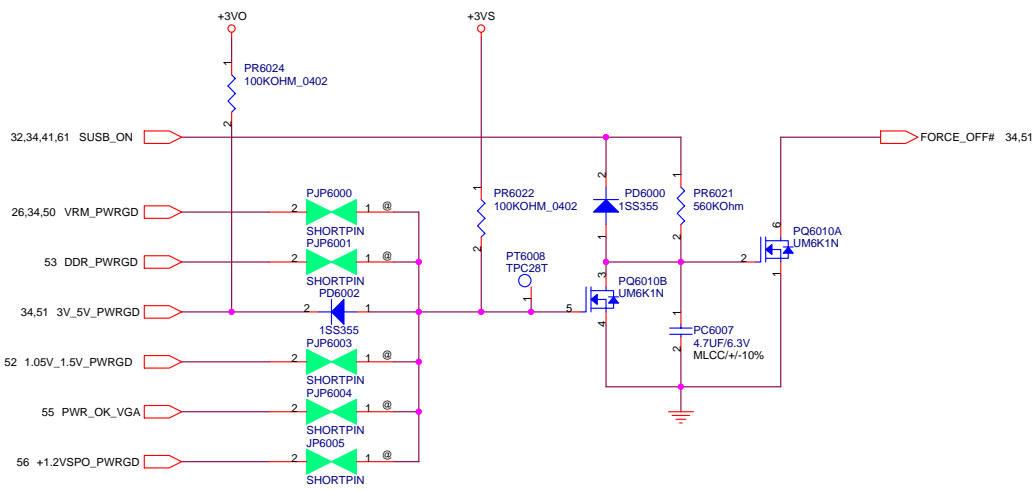


BATTERY A/D\_SD# (OVP)



1.2->2.0

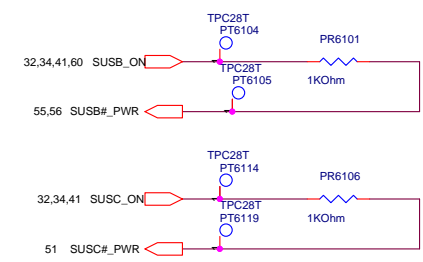
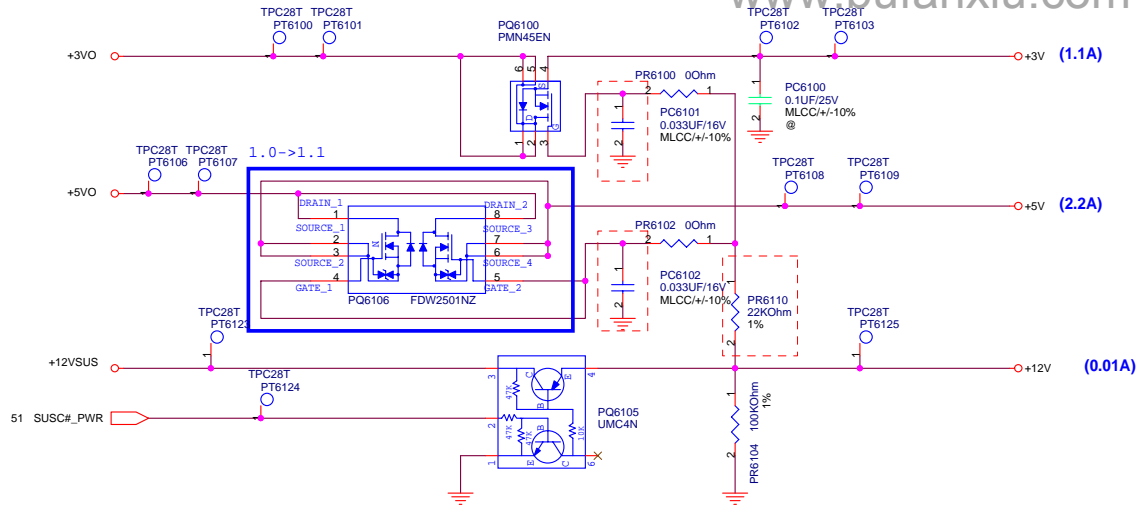
POWER GOOD DETECTOR



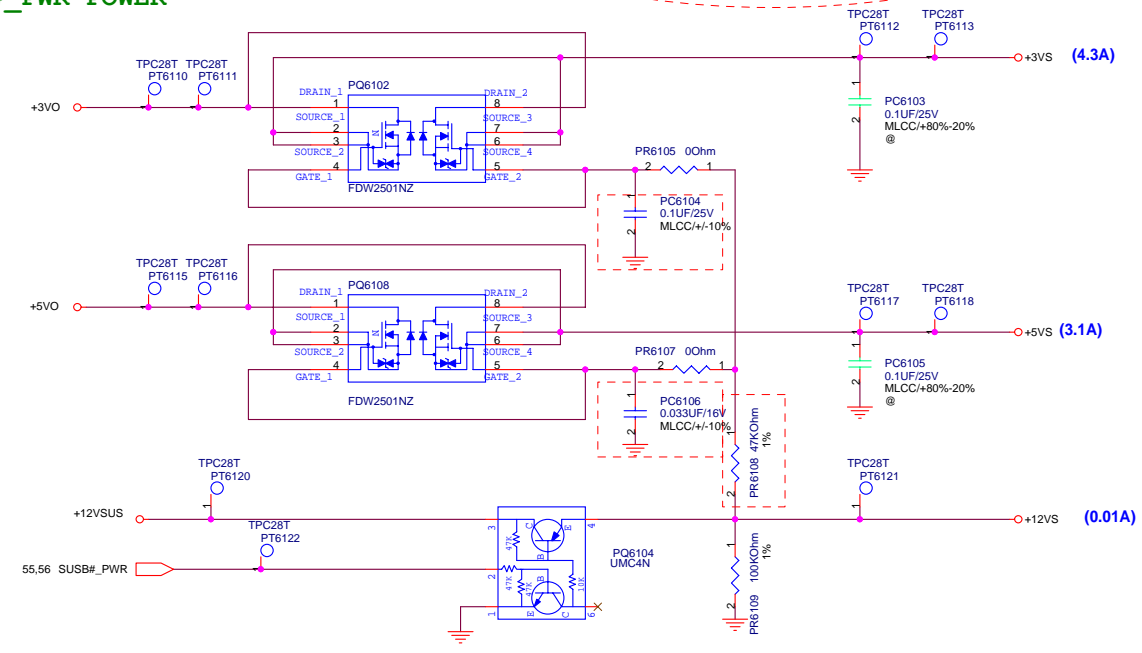
- TPC28T PT6003 1 VRM\_PWRGD
- TPC28T PT6004 1 DDR\_PWRGD
- TPC28T PT6005 1 3V\_5V\_PWRGD
- TPC28T PT6006 1 1.05V\_1.5V\_PWRGD
- TPC28T PT6007 1 PWR\_OK\_VGA

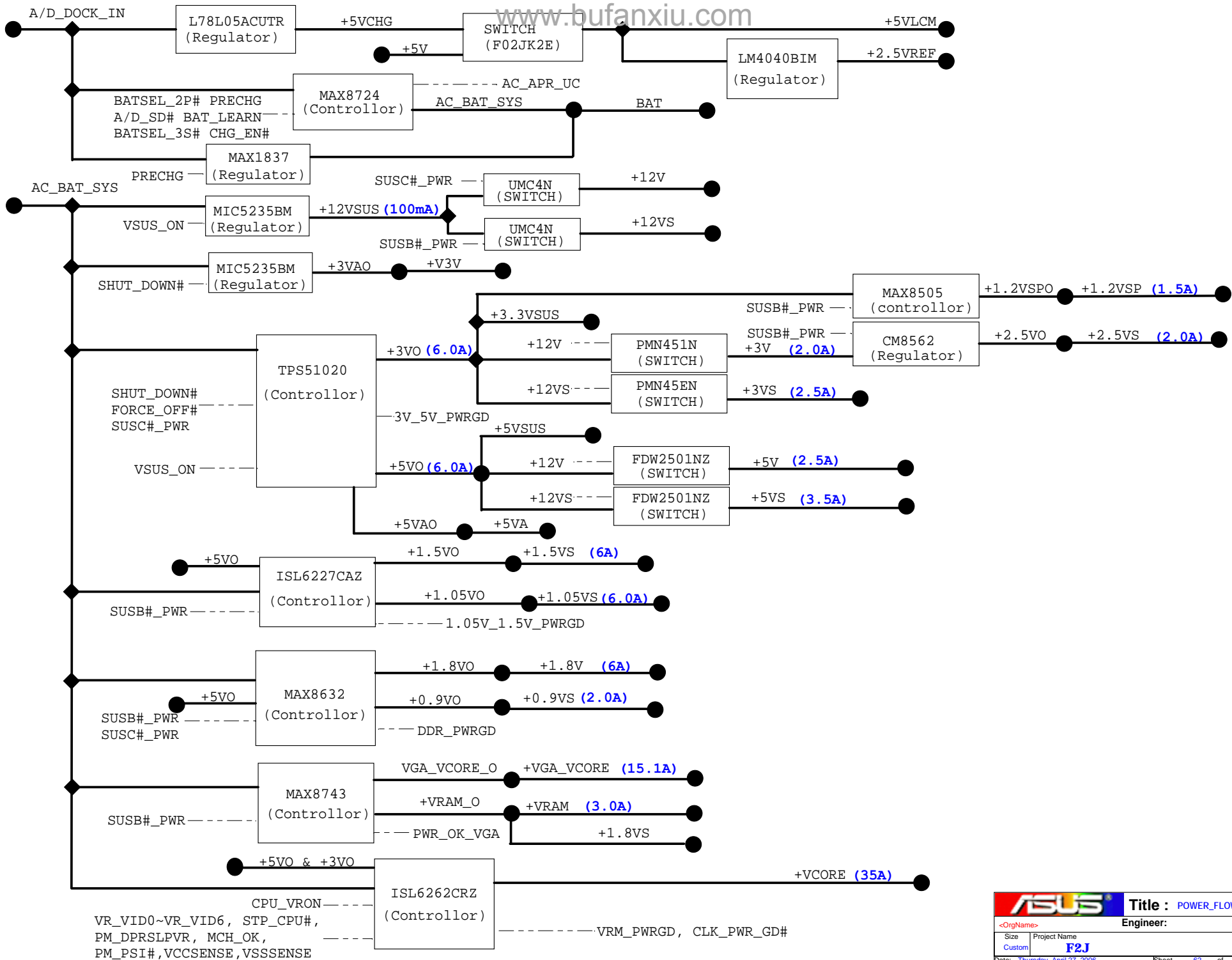
<b>ASUS</b>		<b>Title : POWER_PROTECT</b>	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	<b>F2J</b>	1.1	
Date: Thursday, April 27, 2006		Sheet	60 of 63

SUSC#\_PWR POWER

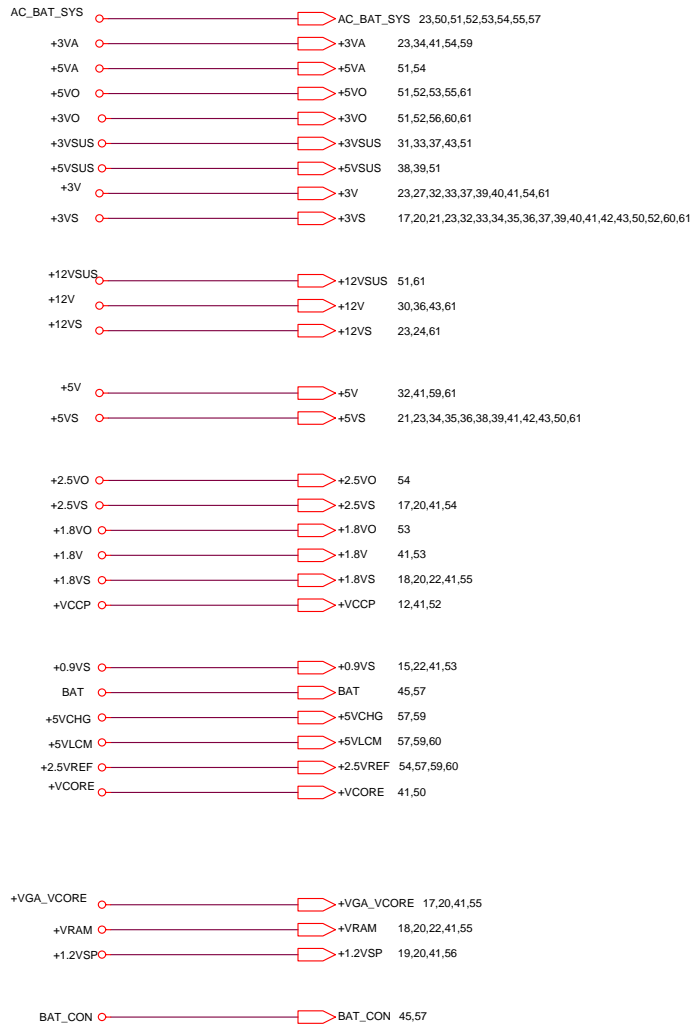


SUSB#\_PWR POWER





			<b>Title :</b> POWER_FLOWCHART		
<OrgName>			Engineer:		
Size	Project Name				Rev
Custom	<b>F2J</b>				1.1
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FOR POWER TEST

