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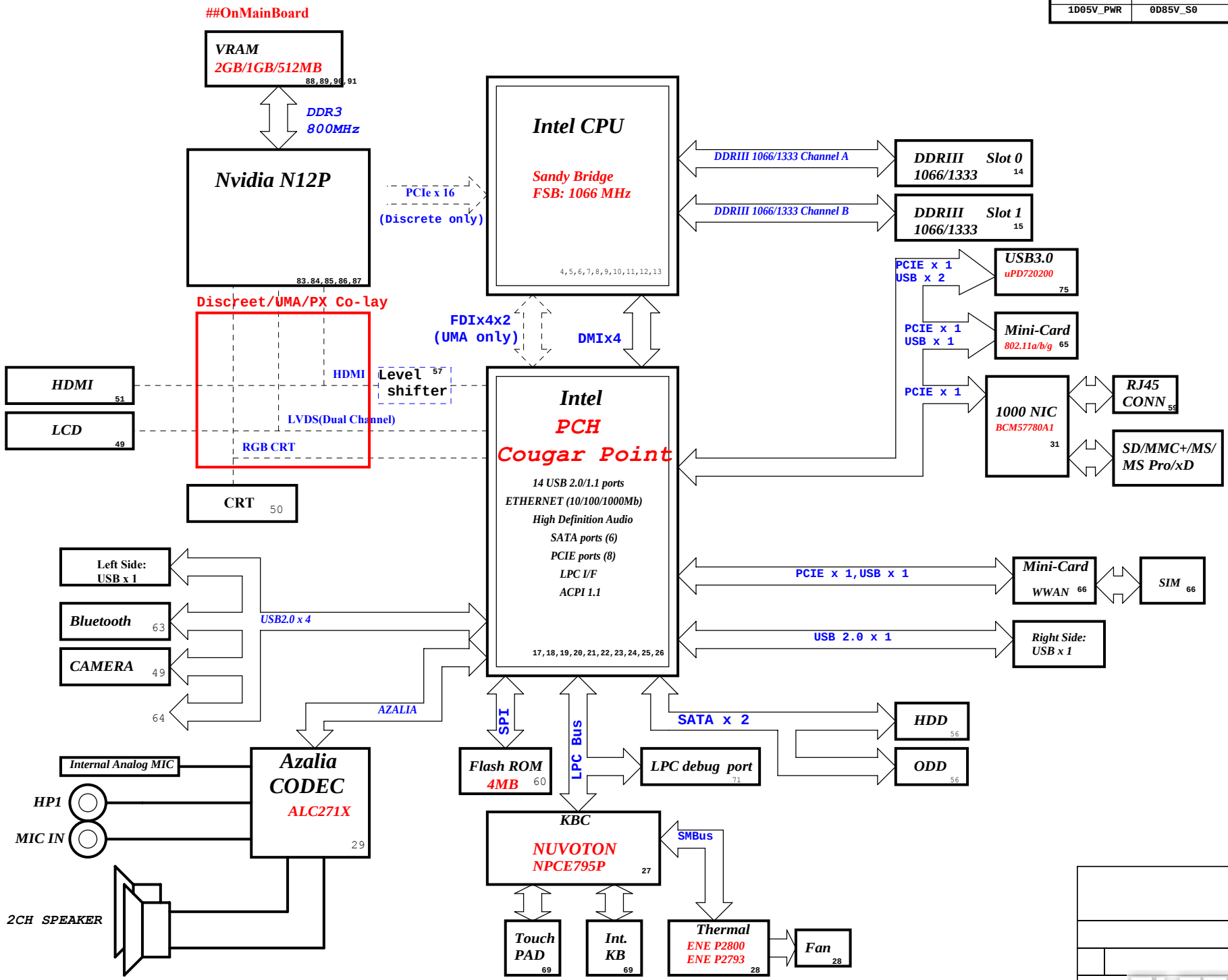

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

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Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

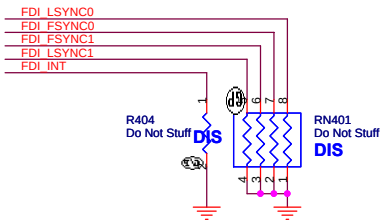
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.



SANDY

DMI
- 19 DMI_TXN[3:0] → DMI_TXN0 B27, DMI_TXN1 B25, DMI_TXN2 A25, DMI_TXN3 B24 → DMI_RX#0, DMI_RX#1, DMI_RX#2, DMI_RX#3
- 19 DMI_TXP[3:0] → DMI_TXP0 B28, DMI_TXP1 B26, DMI_TXP2 A24, DMI_TXP3 B23 → DMI_RX0, DMI_RX1, DMI_RX2, DMI_RX3
- 19 DMI_RXN[3:0] → DMI_RXN0 G21, DMI_RXN1 E22, DMI_RXN2 F21, DMI_RXN3 D21 → DMI_TX#0, DMI_TX#1, DMI_TX#2, DMI_TX#3
- 19 DMI_RXP[3:0] → DMI_RXP0 G22, DMI_RXP1 D22, DMI_RXP2 F20, DMI_RXP3 C21 → DMI_TX0, DMI_TX1, DMI_TX2, DMI_TX3

Intel(R) FDI
- 19 FDI_TXN[7:0] → FDI_TXN0 A21, FDI_TXN1 H19, FDI_TXN2 E19, FDI_TXN3 F18, FDI_TXN4 B21, FDI_TXN5 C20, FDI_TXN6 D18, FDI_TXN7 E17 → FDI0_TX#0, FDI0_TX#1, FDI0_TX#2, FDI0_TX#3, FDI1_TX#0, FDI1_TX#1, FDI1_TX#2, FDI1_TX#3
- 19 FDI_TXP[7:0] → FDI_TXP0 A22, FDI_TXP1 G19, FDI_TXP2 E20, FDI_TXP3 G18, FDI_TXP4 B20, FDI_TXP5 C19, FDI_TXP6 D19, FDI_TXP7 F17 → FDI0_TX0, FDI0_TX1, FDI0_TX2, FDI0_TX3, FDI1_TX0, FDI1_TX1, FDI1_TX2, FDI1_TX3
- 19 FDI_FSYNC0 J18, 19 FDI_FSYNC1 J17 → FDI0_FSYNC, FDI1_FSYNC
- 19 FDI_INT H20 → FDI_INT
- 19 FDI_LSYNC0 J19, 19 FDI_LSYNC1 H17 → FDI0_LSYNC, FDI1_LSYNC

eDP
- 1D05V_VTT → R402 24D9R2F-L-GP → DP_COMP A18; R403 10KR2J-3-GP → eDP_HPD A17
- EDP_COMPIO A18, EDP_ICOMPO A17, EDP_HPD B16
- EDP_AUX C15, EDP_AUX# D15
- EDP_TX0 C17, EDP_TX1 F16, EDP_TX2 C16, EDP_TX3 G15
- EDP_TX#0 C18, EDP_TX#1 F16, EDP_TX#2 D16, EDP_TX#3 F15

PCI EXPRESS* - GRAPHICS

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PEG_ICOMPI J22, PEG_ICOMPO J21, PEG_RCOMPO H22
PEG_IRCOMP_R → R401 24D9R2F-L-GP → 1D05V_VTT

PEG_RX#0	K33	PEG_RXN15
PEG_RX#1	M35	PEG_RXN14
PEG_RX#2	L34	PEG_RXN13
PEG_RX#3	J35	PEG_RXN12
PEG_RX#4	J32	PEG_RXN11
PEG_RX#5	H34	PEG_RXN10
PEG_RX#6	H31	PEG_RXN9
PEG_RX#7	G33	PEG_RXN8
PEG_RX#8	G30	PEG_RXN7
PEG_RX#9	F35	PEG_RXN6
PEG_RX#10	E34	PEG_RXN5
PEG_RX#11	E32	PEG_RXN4
PEG_RX#12	D33	PEG_RXN3
PEG_RX#13	D31	PEG_RXN2
PEG_RX#14	B33	PEG_RXN1
PEG_RX#15	C32	PEG_RXN0

PEG_RXN[0..15] 83

PEG_RX0	J33	PEG_RXP15
PEG_RX1	L35	PEG_RXP14
PEG_RX2	K34	PEG_RXP13
PEG_RX3	H35	PEG_RXP12
PEG_RX4	H32	PEG_RXP11
PEG_RX5	G34	PEG_RXP10
PEG_RX6	G31	PEG_RXP9
PEG_RX7	F33	PEG_RXP8
PEG_RX8	F30	PEG_RXP7
PEG_RX9	E35	PEG_RXP6
PEG_RX10	E33	PEG_RXP5
PEG_RX11	E32	PEG_RXP4
PEG_RX12	D34	PEG_RXP3
PEG_RX13	E31	PEG_RXP2
PEG_RX14	C33	PEG_RXP1
PEG_RX15	B32	PEG_RXP0

PEG_RXP[0..15] 83

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

PEG_TX#0	M29	PEG_C_TXN15	C401	DIS_PX_Muxless	Do Not Stuff
PEG_TX#1	M32	PEG_C_TXN14	C402	DIS_PX_Muxless	Do Not Stuff
PEG_TX#2	M31	PEG_C_TXN13	C403	DIS_PX_Muxless	Do Not Stuff
PEG_TX#3	L32	PEG_C_TXN12	C404	DIS_PX_Muxless	Do Not Stuff
PEG_TX#4	L29	PEG_C_TXN11	C405	DIS_PX_Muxless	Do Not Stuff
PEG_TX#5	K31	PEG_C_TXN10	C406	DIS_PX_Muxless	Do Not Stuff
PEG_TX#6	K28	PEG_C_TXN9	C407	DIS_PX_Muxless	Do Not Stuff
PEG_TX#7	J30	PEG_C_TXN8	C408	DIS_PX_Muxless	Do Not Stuff
PEG_TX#8	J28	PEG_C_TXN7	C409	DIS_PX_Muxless	Do Not Stuff
PEG_TX#9	H29	PEG_C_TXN6	C410	DIS_PX_Muxless	Do Not Stuff
PEG_TX#10	G27	PEG_C_TXN5	C411	DIS_PX_Muxless	Do Not Stuff
PEG_TX#11	E29	PEG_C_TXN4	C412	DIS_PX_Muxless	Do Not Stuff
PEG_TX#12	F27	PEG_C_TXN3	C413	DIS_PX_Muxless	Do Not Stuff
PEG_TX#13	D28	PEG_C_TXN2	C414	DIS_PX_Muxless	Do Not Stuff
PEG_TX#14	F26	PEG_C_TXN1	C415	DIS_PX_Muxless	Do Not Stuff
PEG_TX#15	E25	PEG_C_TXN0	C416	DIS_PX_Muxless	Do Not Stuff

PEG_TX0	M28	PEG_C_TXP15	C417	DIS_PX_Muxless	Do Not Stuff
PEG_TX1	M33	PEG_C_TXP14	C418	DIS_PX_Muxless	Do Not Stuff
PEG_TX2	M30	PEG_C_TXP13	C419	DIS_PX_Muxless	Do Not Stuff
PEG_TX3	L31	PEG_C_TXP12	C420	DIS_PX_Muxless	Do Not Stuff
PEG_TX4	L28	PEG_C_TXP11	C421	DIS_PX_Muxless	Do Not Stuff
PEG_TX5	K30	PEG_C_TXP10	C422	DIS_PX_Muxless	Do Not Stuff
PEG_TX6	K27	PEG_C_TXP9	C423	DIS_PX_Muxless	Do Not Stuff
PEG_TX7	J29	PEG_C_TXP8	C424	DIS_PX_Muxless	Do Not Stuff
PEG_TX8	J27	PEG_C_TXP7	C425	DIS_PX_Muxless	Do Not Stuff
PEG_TX9	H28	PEG_C_TXP6	C426	DIS_PX_Muxless	Do Not Stuff
PEG_TX10	G28	PEG_C_TXP5	C427	DIS_PX_Muxless	Do Not Stuff
PEG_TX11	E28	PEG_C_TXP4	C428	DIS_PX_Muxless	Do Not Stuff
PEG_TX12	F28	PEG_C_TXP3	C429	DIS_PX_Muxless	Do Not Stuff
PEG_TX13	D27	PEG_C_TXP2	C430	DIS_PX_Muxless	Do Not Stuff
PEG_TX14	F26	PEG_C_TXP1	C431	DIS_PX_Muxless	Do Not Stuff
PEG_TX15	D25	PEG_C_TXP0	C432	DIS_PX_Muxless	Do Not Stuff

PEG_TXN[0..15] 83
PEG_TXP[0..15] 83

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

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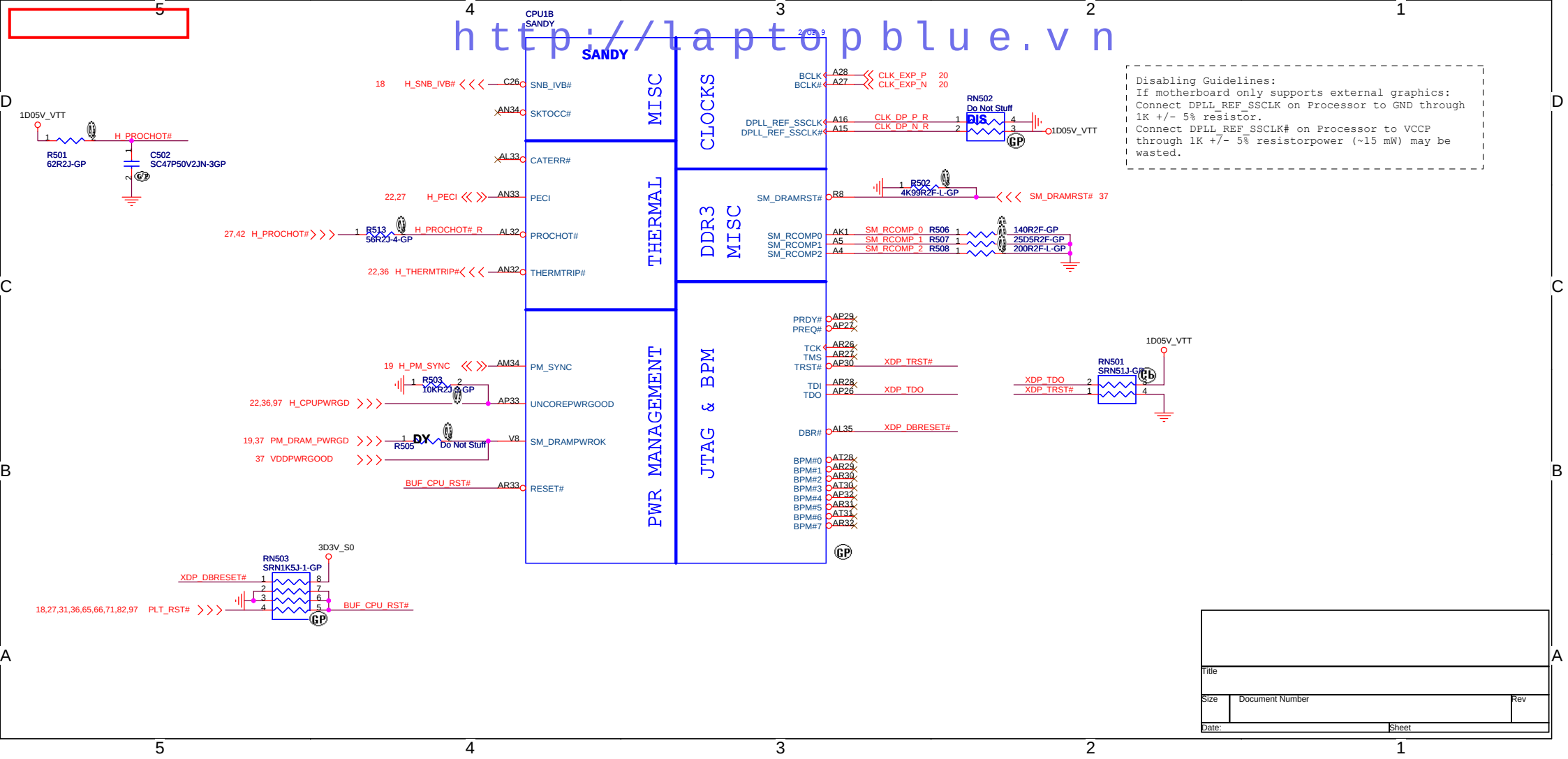

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

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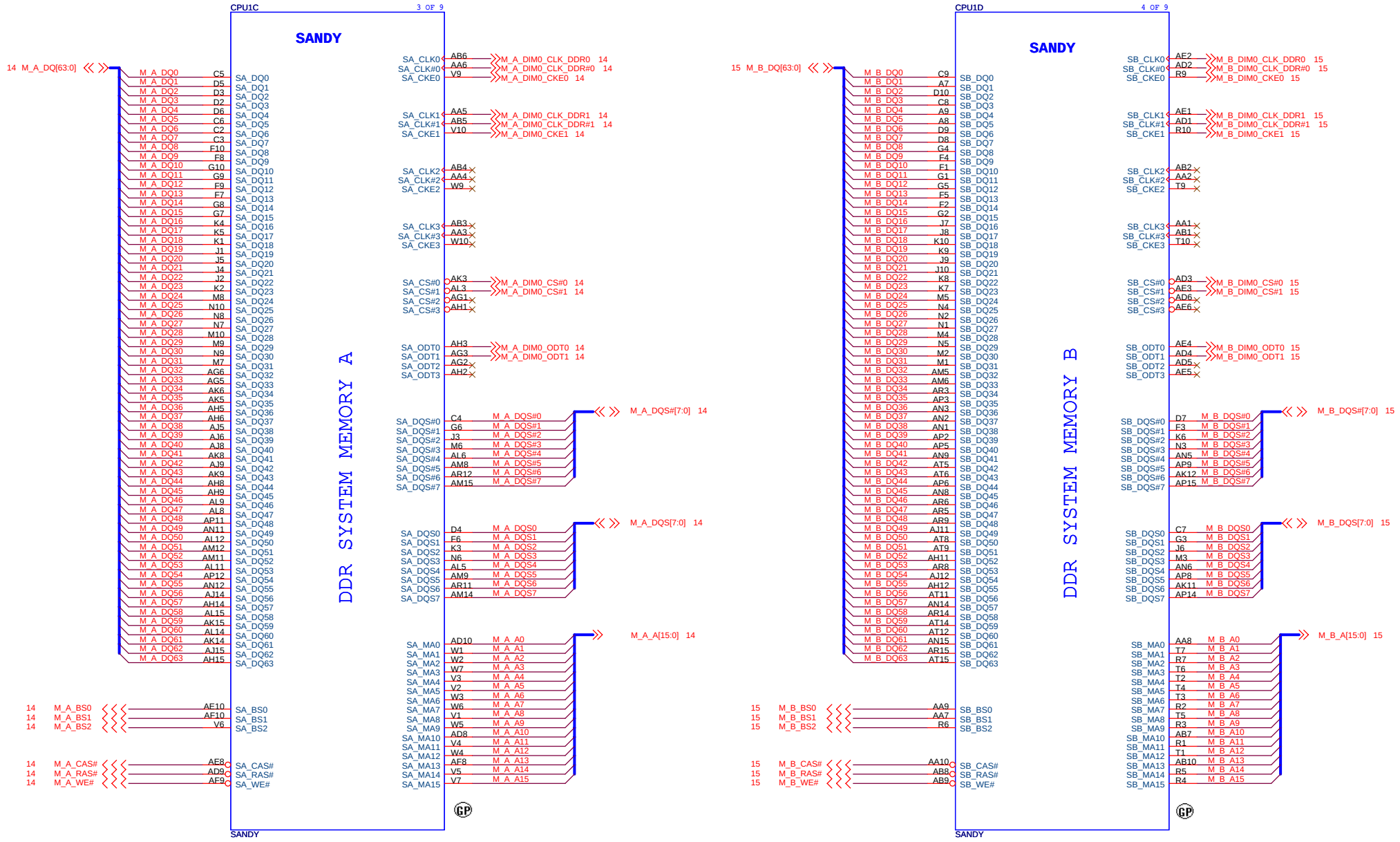

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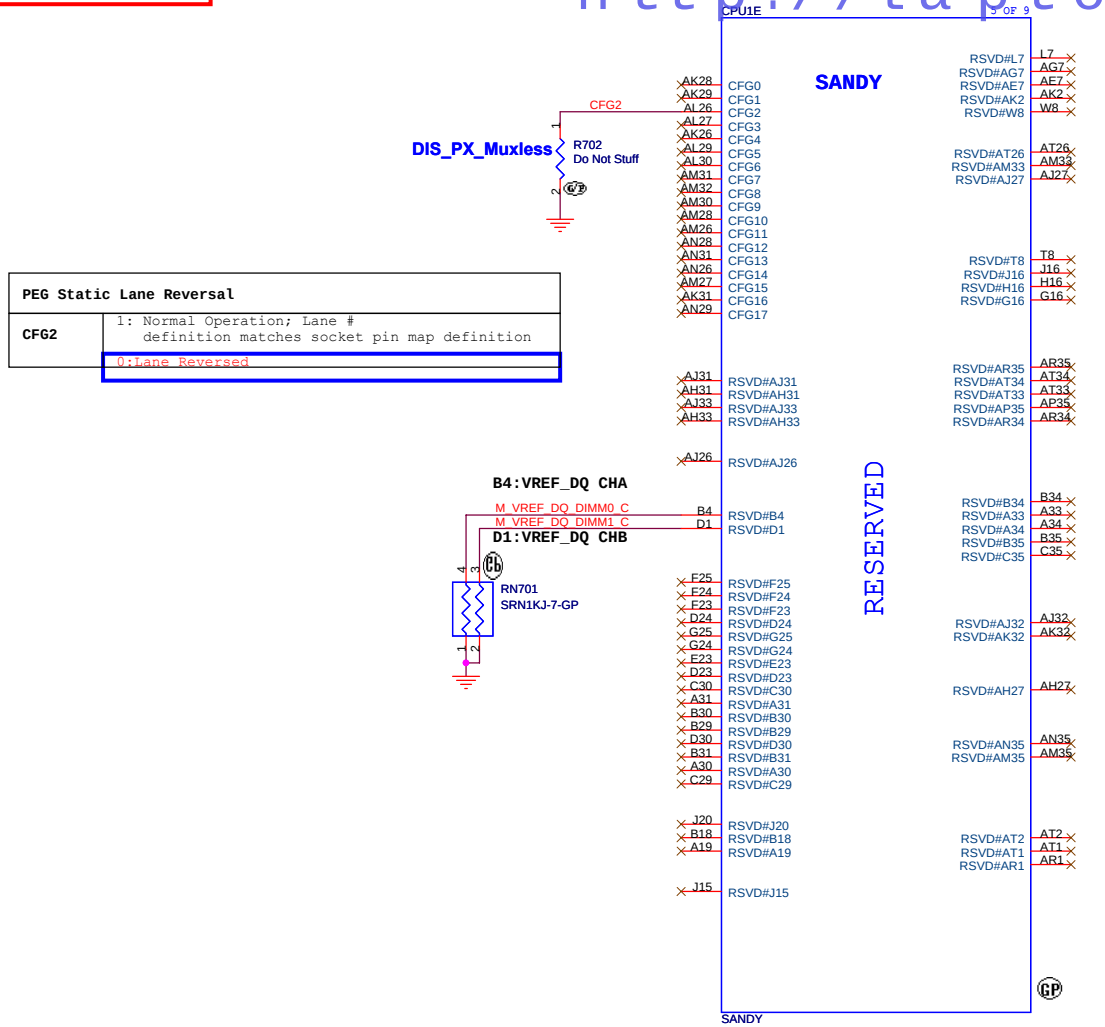

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POWER

PROCESSOR CORE POWER

53A

VCC_CORE

C801 Do Not Stuff
C802 Do Not Stuff
C803 Do Not Stuff
C804 Do Not Stuff
C811 Do Not Stuff
C820 Do Not Stuff
C819 Do Not Stuff
C818 Do Not Stuff
C817 Do Not Stuff
C815 Do Not Stuff
DY

C816 SC10U6D3V5KX-1GP
C821 Do Not Stuff
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 Do Not Stuff
C831 Do Not Stuff
C828 SC10U6D3V5KX-1GP

CPU1F

SANDY

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

CORE SUPPLY

PEG AND DDR

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

1D05V_VTT

C805 SC10U6D3V5KX-1GP
C806 SC10U6D3V5KX-1GP
C807 SC10U6D3V5KX-1GP
C809 SC10U6D3V5KX-1GP
C810 SC10U6D3V5KX-1GP
C838 SC10U6D3V5KX-1GP
C839 SC10U6D3V5KX-1GP
C840 SC10U6D3V5KX-1GP
C841 SC10U6D3V5KX-1GP

1D05V_VTT

C812 SC10U6D3V5KX-1GP
C813 SC10U6D3V5KX-1GP
C814 SC10U6D3V5KX-1GP
C829 SC10U6D3V5KX-1GP
C830 SC10U6D3V5KX-1GP
C842 Do Not Stuff
C843 Do Not Stuff
C844 SC10U6D3V5KX-1GP
C845 SC10U6D3V5KX-1GP
DY

SVID

VIDALERT# AJ29 — H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 — H_CPU_SVIDCLK 42
VIDSOUT AJ28 — H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT
H_CPU_SVIDDAT — R804 130R2F-1-GP

SENSE LINES

VCC_CORE
R801 100R2F-L1-GP-U
VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42
R802 100R2F-L1-GP-U
VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

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VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff DY
C902 SC10U6D3V5KX-1GP
C903 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP
C905 SC10U6D3V5KX-1GP
C906 Do Not Stuff DY
UMA_PX_Muxless

C907 Do Not Stuff DY
C908 SC10U6D3V5KX-1GP
C918 Do Not Stuff DY
C919 SC10U6D3V5KX-1GP
C920 SC10U6D3V5KX-1GP
C921 SC10U6D3V5KX-1GP DY
UMA_PX_Muxless

VCC_GFXCORE

R903 Do Not Stuff DIS
R904 Do Not Stuff DIS
R905 Do Not Stuff DIS
R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

CPU1G — SANDY — 7 OF 9

GRAPHICS: AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

SENSE LINES: VAXG_SENSE AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF: SM_VREF AL1 — +V_SM_VREF_CNT 37

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

1D5V_S0

PROCESSOR VDDQ: 10A

C909 Do Not Stuff DY
C910 SC10U6D3V5KX-1GP
C911 SC10U6D3V5KX-1GP
C912 SC10U6D3V5KX-1GP
C913 SC10U6D3V5KX-1GP
C914 Do Not Stuff DY

DDR3 -1.5V RAILS: VDDQ AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 Do Not Stuff DY
C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

SA RAIL: VCCSA M27 M26 L26 J26 J25 J24 H26 H25

0D85V_S0
R902 10R2J-2-GP
R902 need be close to pin H23.
VCCSA_SENSE H23 — VCCUSA_SENSE — TP901 Do Not Stuff

MISC: FC_C22 C22 — H_FC_C22
VCCSA_VID1 C24 — VCCSA_SEL 48
RN901 SRN1KJ-7-GP

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C922 SC1U10V2KX-1GP

1.8V RAIL: VCCPLL B6 A6 A2

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

SANDY

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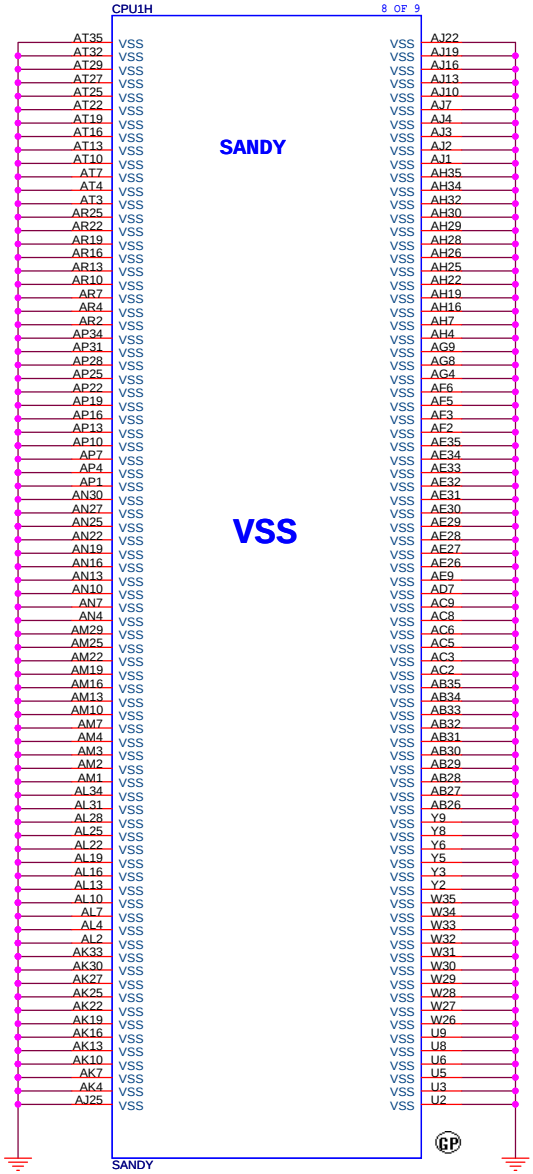

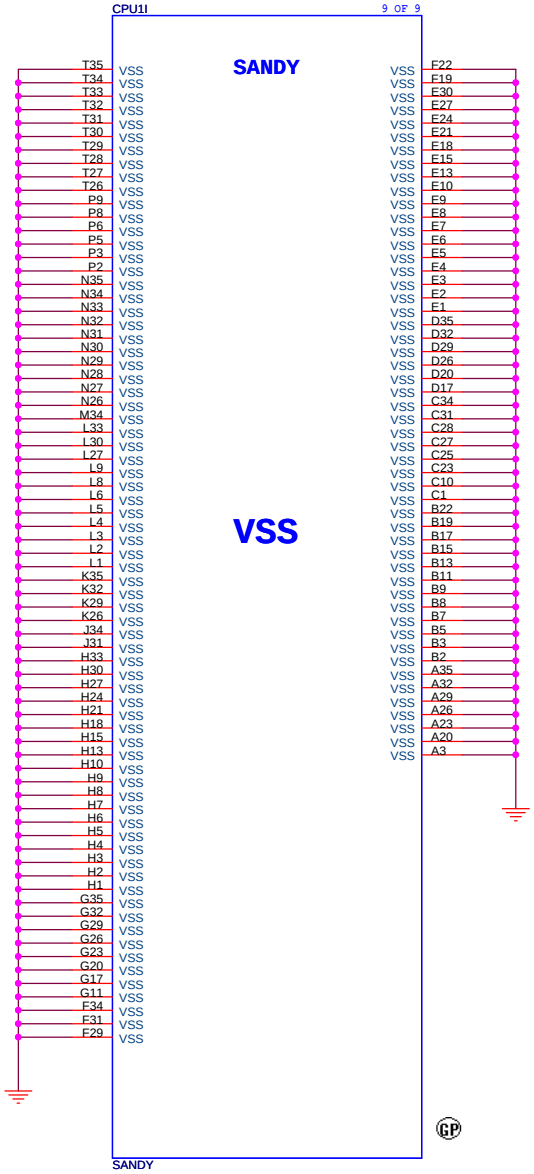

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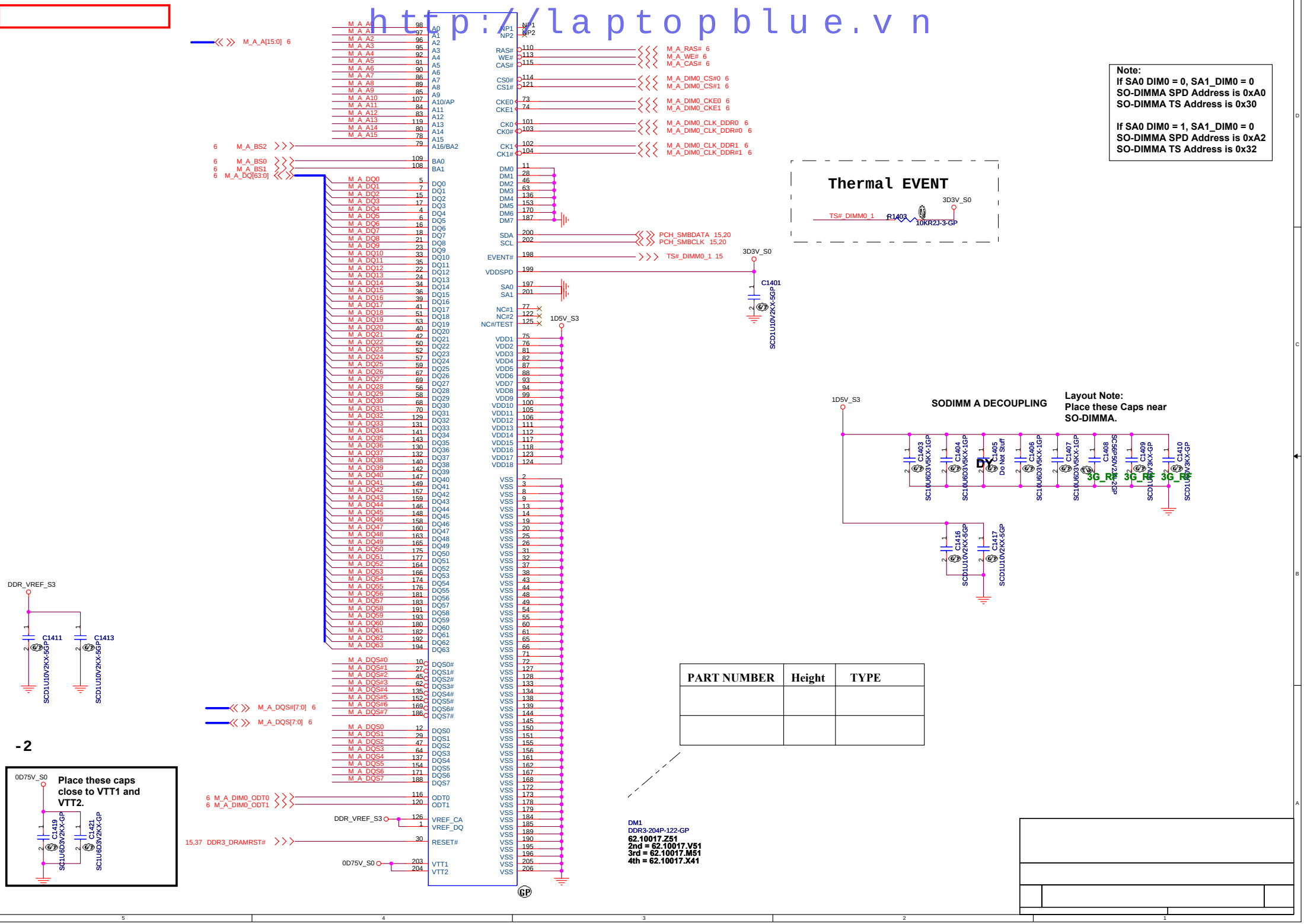

SSID = MEMORY

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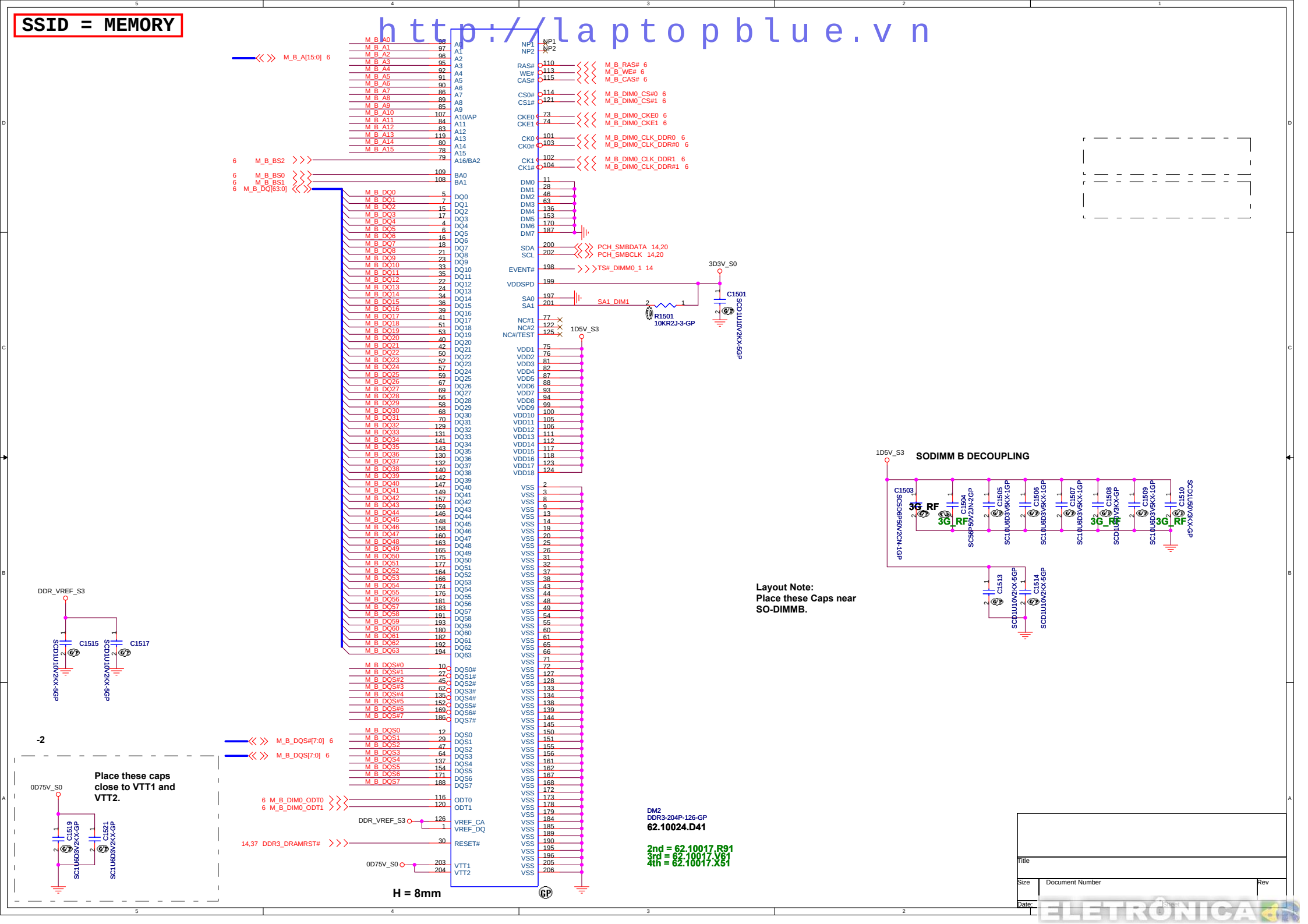

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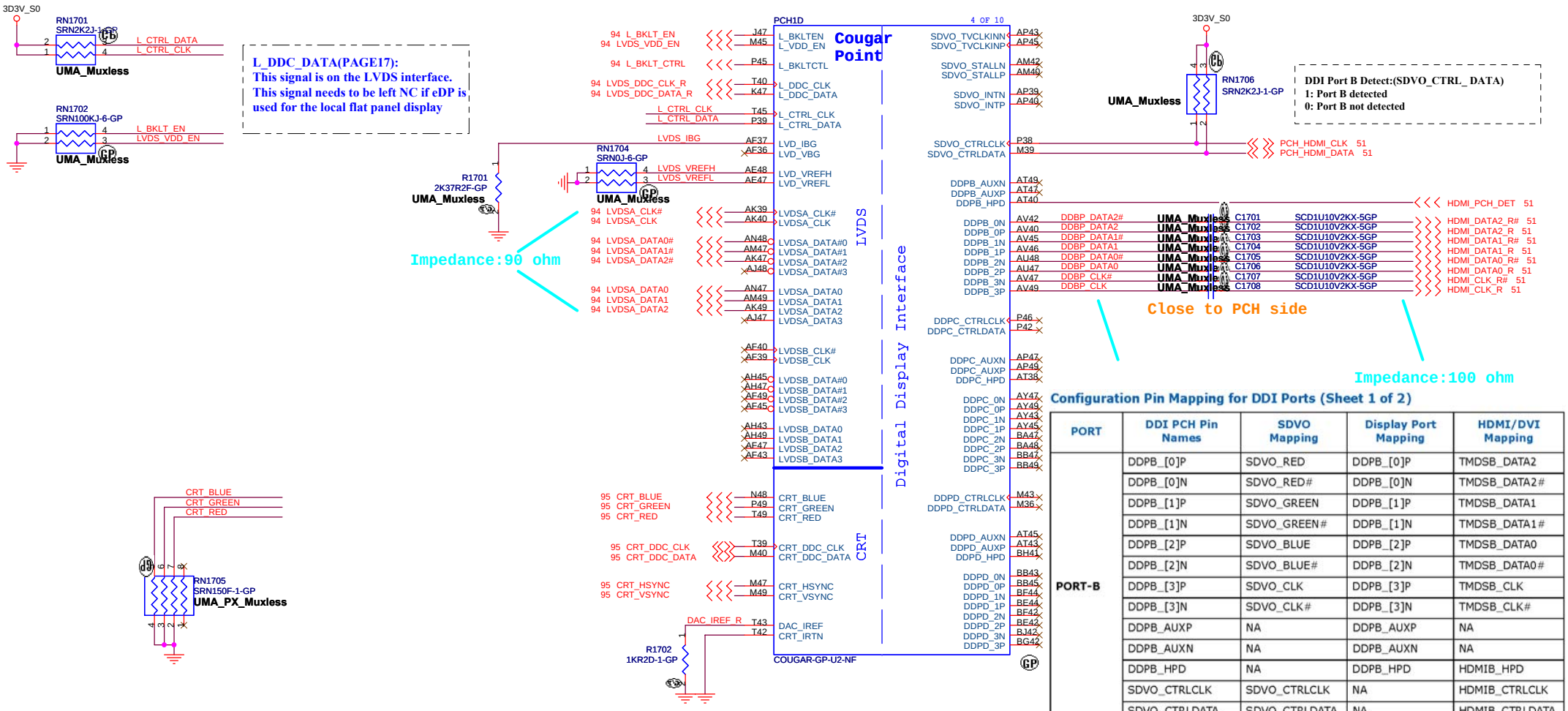

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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SSID = PCH

RN1801
SRN8K2J-2-GP-U

INT_PIRQH#	1	10	3D3V_S0
INT_PIRQB#	2	9	INT_PIRQD#
INT_PIRQF#	3	8	INT_PIRQE#
INT_PIRQA#	4	7	INT_PIRQC#
3D3V_S0	5	6	USB30_SMI#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
		SPI(Default)

PCH1E — 5 OF 10 — Cougar Point — COUGAR-GP-U2-NF

RSVD: TP1–TP20, AY7, AV7, AU3, BG4, AT10, BC8, AU2, AT4, AT3, AT1, AY3, AT5, AV3, AV1, BB1, BA3, BB5, BB3, BB7, BE8, BD4, BF6, AV5, AY1, AV10, AT8, AY5, BA2, AT12, BF3, TP21–TP24, TP25–TP40

NVRAM: DF_TVS

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

1D8V_S0
R1808 2K2R2J-2-GP
NV_CLE — R1809 1KR2J-1-GP — H_SNB_IVB# 5

RN1803
SRN10KJ-5-GP
DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1
4

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB: USBP0N/P … USBP13N/P

USB_PN0 66	USB_PP0 66
USB_PN1 61	USB_PP1 61
USB_PN3 63	USB_PP3 63
USB_PN4 66	USB_PP4 66
USB_PN5 32	USB_PP5 32
USB_PN8 82	USB_PP8 82
USB_PN9 61	USB_PP9 61
USB_PN11 65	USB_PP11 65
USB_PN12 49	USB_PP12 49

USBRBIAS# — C33 — USB_RBIAS — R1811 22D6R2F-L1-GP
USBRBIAS — B33

PCI: PIRQA#/GPIO0, PIRQB#/GPIO5, PIRQC#/GPIO6, PIRQD#/GPIO7, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#, CLKOUT_PCI0–4

Do Not Stuff TP1806 — 83 DGPU_HOLD_RST# — DGPU_SELECT# — C46, C44
93 DGPU_PWR_EN# — E40
Do Not Stuff TP1804 — DGPU_PWM_SELECT# — D47, F42, F46

R1813 Do Not Stuff
56 SATA_ODD_DA#
82 USB30_SMI#
INT_PIRQE# — G42
INT_PIRQF# — G40, C42
INT_PIRQH# — D44

5,27,31,36,65,66,71,82,97 PLT_RST# — C6

71 CLK_PCI_LPC — R1804 22R2J-2-GP — CLK_PCI_LPC_R — H49
20 CLK_PCI_FB — R1805 22R2J-2-GP — CLK_PCI_FB_R — H43
27 CLK_PCI_KBC — R1806 22R2J-2-GP — CLK_PCI_KBC_R — J48
K42, H40

EC1803 DY Do Not Stuff
EC1802 DY Do Not Stuff
EC1801 DY Do Not Stuff

OC0#/GPIO59, OC1#/GPIO40, OC2#/GPIO41, OC3#/GPIO42, OC4#/GPIO43, OC5#/GPIO9, OC6#/GPIO10, OC7#/GPIO14
3D3V_S5
R1820 10KR2J-3-GP

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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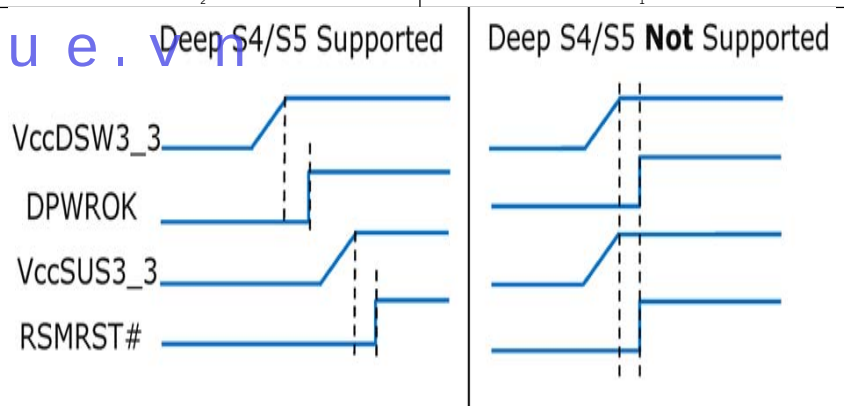

PCH1C — Cougar Point — 3 OF 10

DMI: DMI0RXN DMI1RXN DMI2RXN DMI3RXN / DMI0RXP DMI1RXP DMI2RXP DMI3RXP / DMI0TXN DMI1TXN DMI2TXN DMI3TXN / DMI0TXP DMI1TXP DMI2TXP DMI3TXP

FDI: FDI_RXN0-7 / FDI_RXP0-7 / FDI_INT / FDI_FSYNC0 / FDI_FSYNC1 / FDI_LSYNC0 / FDI_LSYNC1 / FDI_TXN0-7 / FDI_TXP0-7 / FDI_INT

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29

SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

DMI_ZCOMP, DMI_IRCOMP, DMI2RBIAS

COUGAR-GP-U2-NF

1D05V_VTT
R1901 49D9R2F-GP DMI_COMP_R
R1902 750R2F-GP RBIAS_CPY

R1926 Do Not Stuff
R1904 100KR2J-1-GP
SYS_PWROK
PWROK

0628 Modify:
Change R1904 to 100K 0402 from 10K and default stuff.

SUS_PWR_ACK
3D3V_S0
R1905 10KR2J-3-GP
SYS_RESET#
36 SYS_PWROK
27,42 S0_PWR_GOOD
R1924 Do Not Stuff
PWROK

R1910 Do Not Stuff
R1911 Do Not Stuff
PCH_DPWROK
PM_RSMRST#
RTC_AUX_S5

PCIE_WAKE# 31,65,66,82
PM_CLKRUN# 27
PCH_SUSCLK_KBC 27
PM_SLP_S4# 27,46
PM_SLP_S3# 27,36,37,47,92
H_PM_SYNC 5

5,37 PM_DRAM_PWRGD
PM_RSMRST#
27 SUS_PWR_ACK
27,97 PM_PWRBTN#
27 AC_PRESENT
BATLOW#
PM_RI#

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

RTC_AUX_S5
R1917 330KR2J-L1-GP
DSWODVREN
R1918 Do Not Stuff

R1919 8K2R2J-3-GP
3D3V_S0
PM_CLKRUN#

3D3V_S5
RN1901 SRN10KJ-6-GP
BATLOW#
PM_RI#
AC_PRESENT
SUS_PWR_ACK
R1921 10KR2J-3-GP
PCIE_WAKE#

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP
PM_RSMRST#

3D3V_AUX_S5
R1909 100KR2J-1-GP
R1916 10KR2J-3-GP
3V_5V_POK_#
R1912 1KR2J-1-GP
PM_RSMRST#
RSMRST#_KBC 27
3V_5V_POK 41
Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

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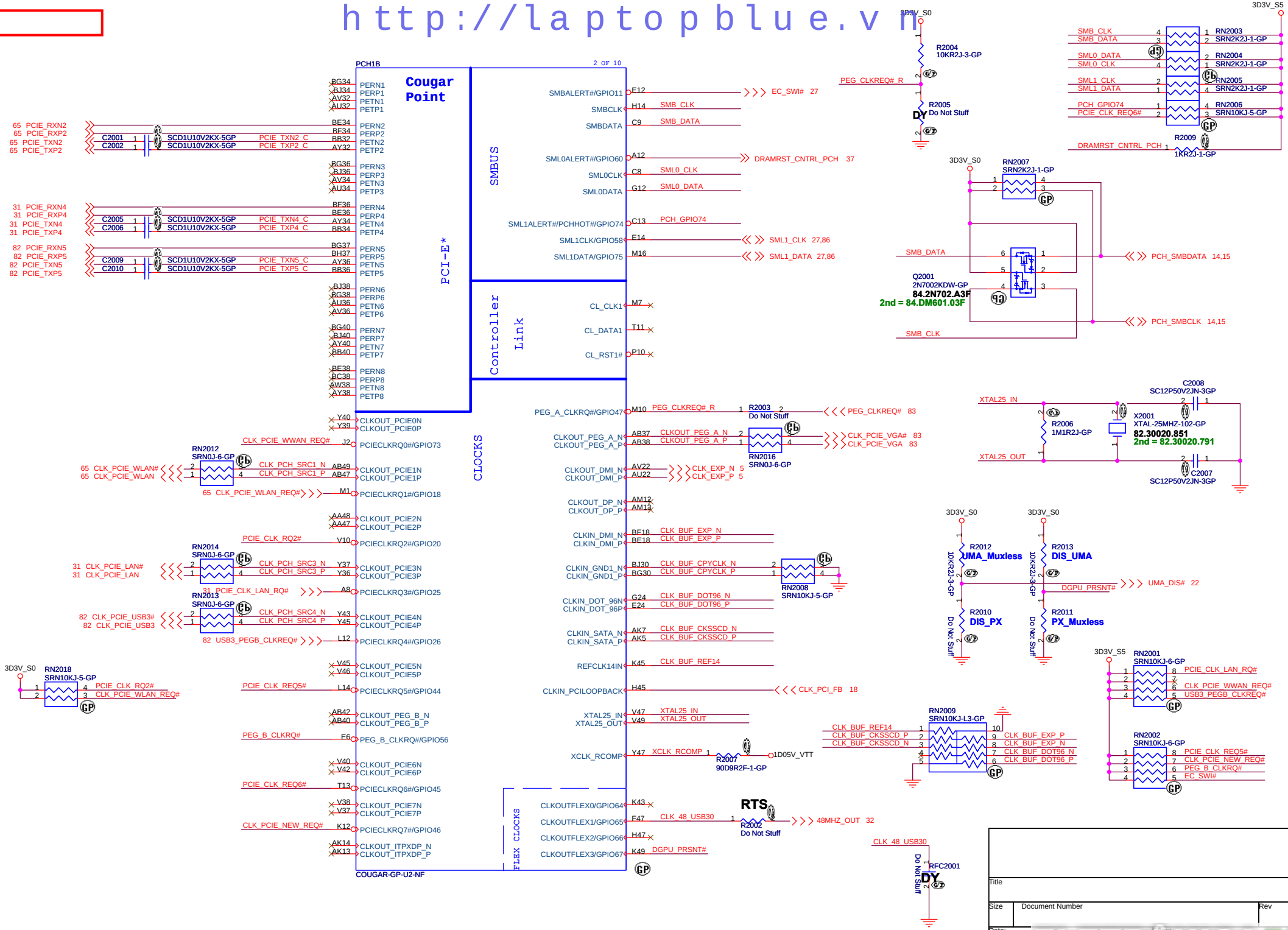

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RTC_AUX_S5

RTC_X1

RTC_X2

R2101 10MR2J-L-GP

X2101
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21

C2101 SC5P50V2CN-2GP

C2102 SC5P50V2CN-2GP

RN2104 SRN20KJ-GP-U

C2103 SC1U6D3V2KX-GP

C2104 SC1U6D3V2KX-GP

G2101 Do Not Stuff

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

R2104 1M1R2J-GP

R2105 330KR2F-L-GP

RTC_X1
RTC_X2
RTC_RST#
SRTC_RST#
SM_INTRUDER#
PCH_INTVRMEN

R2122 33R2J-2-GP DY
R2123 33R2J-2-GP

29 HDA_CODEC_SYNC
29 HDA_CODEC_SDOUT
HDA_SYNC
HDA_SDOUT

29 HDA_CODEC_RST#
29 HDA_CODEC_BITCLK
HDA_RST#
HDA_BITCLK

RN2102 SRN33J-5-GP-U

Flash Descriptor Security Overide

HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO

R2102 Do Not Stuff DY

HDA_SDOUT

No Reboot Strap

HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO

R2103 1KR2J-1-GP

HDA_SYNC

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

5V_S0

Q2101 Do Not Stuff
Do Not Stuff
2ND = 84.2N702.031

R2124 Do Not Stuff

HDA_SYNC_R

HDA_CODEC_SYNC

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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Cougar Point

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17

IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32

JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1

SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3

LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5

SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5, SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10, SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4, SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1, SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP/GPIO21 V14, SATA1GP/GPIO19 P1

COUGAR-GP-U2-NF

LPC_AD[0..3] 27,71
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME# 27,71
INT_SERIRQ 27

SATA_RXN0 56
SATA_RXP0 56
SATA_TXN0 56
SATA_TXP0 56

HDD1

SATA_RXN4 56
SATA_RXP4 56
SATA_TXN4 56
SATA_TXP4 56

ODD

ESATA

1D05V_VTT
SATA_COMP R2112 37D4R2F-GP
1D05V_VTT
SATA3_COMP R2113 49D9R2F-GP
RBIAS_SATA3 R2114 750R2F-GP

SATA_LED# 68
SATA_DET#0

27 ME_UNLOCK R2107 1KR2J-1-GP HDA_SDOUT

R2121 4K7R2J-2-GP PCH_JTAG_TCK_BUF

R2108 33R2J-2-GP PCH_SPI_CLK
R2109 33R2J-2-GP PCH_SPI_CS0#
R2110 33R2J-2-GP PCH_SPI_SI

27,60 SPI_CLK_R
27,60 SPI_CS0#_R
27,60 SPI_SI_R
27,60 SPI_SO_R

HDA_CODEC_BITCLK
HDA_CODEC_SDOUT
SPI_CS0#_R

EC2102 DY Do Not Stuff
EC2103 DY Do Not Stuff
EC2101 DY Do Not Stuff

22 PSW_CLR#

RN2103 SRN10KJ-6-GP
3D3V_S0
SATA_LED#
INT_SERIRQ
SATA_DET#0

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Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

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POWER

Cougar Point

PCH1G

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COUGAR-GP-U2-NF

1D05V_VTT

1.3A

(1uFx3)
(10uFx1_0603)

C2301 SC10U6D3V5KX-1GP
C2302 SC1U6D3V2KX-GP
C2303 SC1U6D3V2KX-GP
C2304 SC1U6D3V2KX-GP

VCC CORE

AA23 AC23 AD21 AD23 AE21 AE23 AG21 AG23 AG24 AG26 AG27 AG29 AJ23 AJ26 AJ27 AJ29 AJ31 VCCCORE

AN19 VCCIO

BJ22 VCCAPLLEXP

2.925A(Total current of VCCIO)

(1uF x4)

C2306 DY Do Not Stuff
C2307 SC1U6D3V2KX-GP
C2308 SC1U6D3V2KX-GP
C2309 SC1U6D3V2KX-GP

AN16 AN17 AN21 AN26 AN27 AP21 AP23 AP24 AP26 AT24 AN33 AN34 VCCIO

VCCIO

0.266A (Totally VCC3_3 current)

(0.1uF x1)

3D3V_S0

C2310 SCD1U10V2KX-5GP

BH29 VCC3_3

0.159A(Totally current of VCCVRM)

VCCVRM_S0 AP16 VCCVRM

BG6 VCCAFDIPLL

1D05V_VTT AP17 VCCIO

1D05V_VTT AU20 VCCDMI

0.042A (Totally current of VCCDMI)

CRT

LVDS

HVCMOS

DMI

NAND / SPI

FDI

VCCADAC U48 +VCCA_DAC_1_2

VSSADAC U47

VCCALVDS AK36 +3VS_VCCA_LVDS

VSSALVDS AK37

VCCTX_LVDS AM37
VCCTX_LVDS AM38
VCCTX_LVDS AP36
VCCTX_LVDS AP37

VCC3_3 V33
VCC3_3 V34

VCCVRM AT16

VCCDMI AT20

VCCCLKDMI AB36

VccDFTERM AG16
VccDFTERM AG17
VccDFTERM AJ16
VccDFTERM AJ17

VCCSPI V1

(0.1uF/0.01uF x1)
(10uF x1_0603)

R2301 Do Not Stuff
3D3V_S0
3D3V_DAC_S0
R2315 Do Not Stuff

C2313 SCD01U50V2KX-3GP
C2314 SCD01U50V2KX-5GP
C2315 DY Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

0.001A

R2304 0R3J-0-U-GP
UMA_PX_Muxless

R2303 DIS Do Not Stuff

0.06A

R2309 DIS Do Not Stuff
C2316 SCD01U50V2KX-3GP
C2317 SCD01U50V2KX-3GP
C2318 DY Do Not Stuff
+1.8VS_VCCTX_LVDS

UMA_PX_Muxless UMA_PX_Muxless

R2305 0R5J-5-U-GP
1D8V_S0
UMA_PX_Muxless

(0.01uF x2)
(22uF x1)

3D3V_S0

C2319 SCD1U10V2KX-5GP

VCCVRM_S0

1D05V_VTT

(1uF x1)

C2320 SC1U6D3V2KX-GP

0.02A

+1.05VS_VCC_DMI_CCI

L2303 IND-10UH-218-GP
68.10050.10Y
2nd = 68.10090.10B

(1uFx1)
(10uFx1)

C2321 SC1U6D3V2KX-GP
C2325 DY Do Not Stuff

1D8V_S0

0.19A

C2326 SCD1U10V2KX-5GP
C2322 SCD1U10V2KX-5GP

0.02A

3D3V_S5

(1uFx1)

C2323 SC1U6D3V2KX-GP

5V_S0

U2301
G9091-330T11U-GP
74.09091.J3F
2nd = 74.09198.G7F

VIN GND EN VOUT NC#4

C2311 SC1U6D3V2KX-1GP
C2312 SC1U6D3V2KX-GP
C2327 SC1U6D3V3MX-GP

UMA_PX_Muxless UMA_PX_Muxless UMA_PX_Muxless

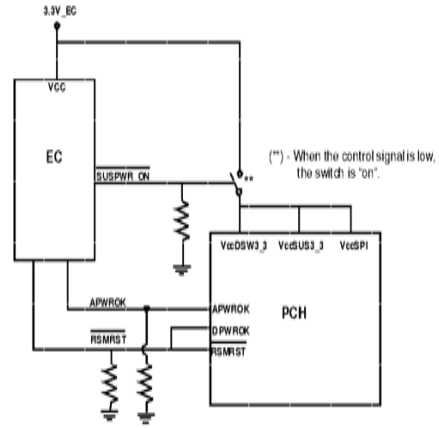
3D3V_S0 1D5V_S0 VCCVRM_S0

U2302
G913CF-GP
74.00913.A3F

SHDN# GND IN SET OUT

C2328 DY SC1U10V3KX-3GP
C2329 DY SC4D7U6D3V3KX-GP
C2330 DY SC22P50V2JN-4GP
C2331 DY SCD1U10V2KX-5GP
R2316 DY 2K8R2F-GP
R2317 DY 10KR2J-3-GP

Refer to NPCE795 shared SPI flash architecture



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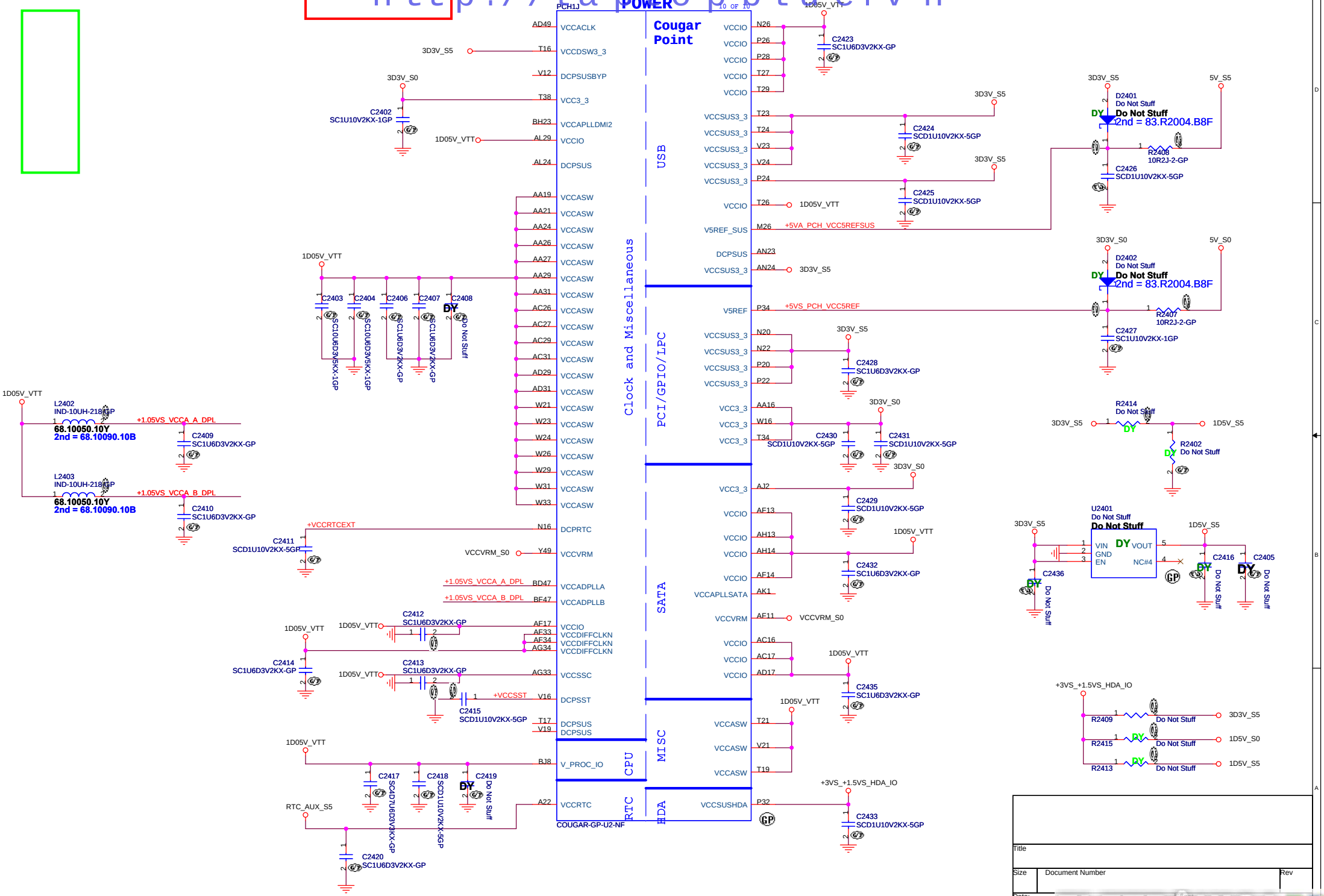

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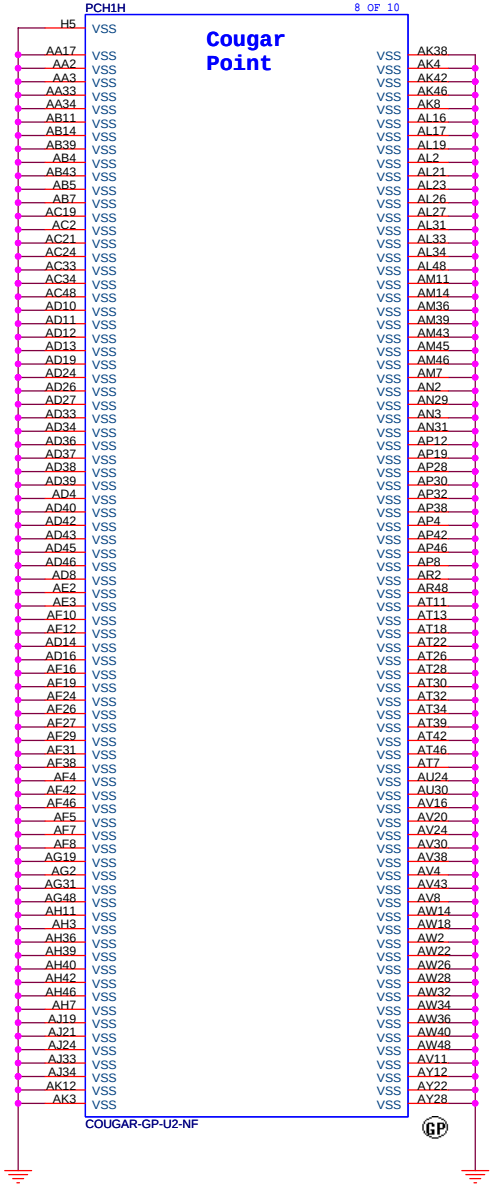

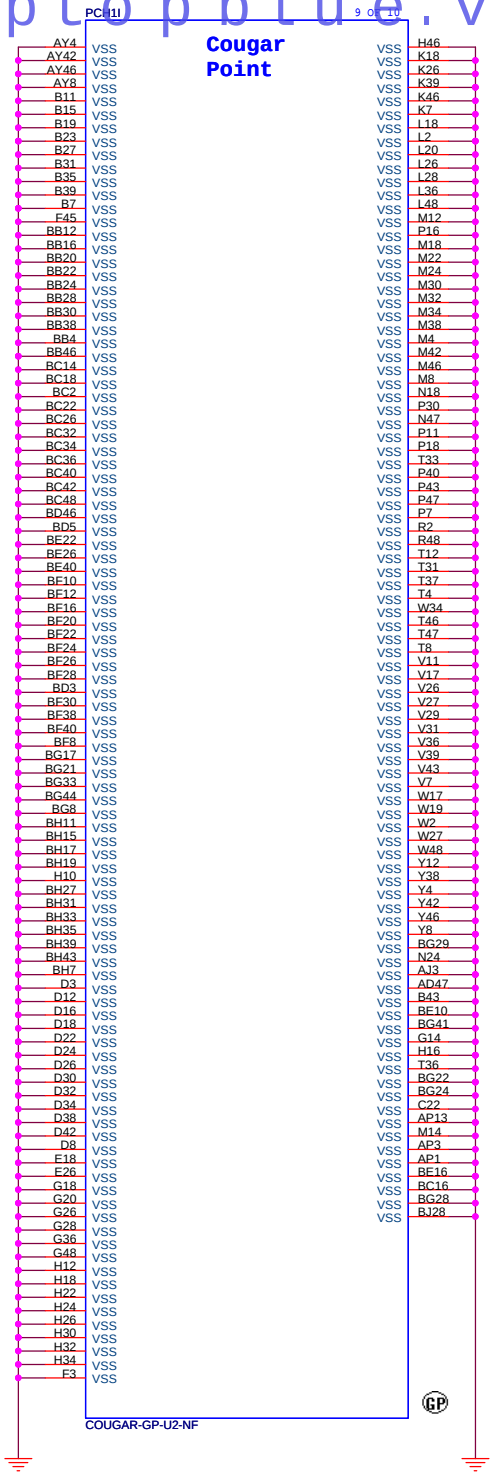

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SSID = KBC

PCB VERSION A/D(PIN96)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K		3.0V
SB			2.75V
		47.0K	
		64.9K	
Reserved		76.8	
Reserved			1.65V

PSL SOLUTION
(Power Switch Control Logic)

Q2703 Do Not Stuff
Do Not Stuff
2ND = 84.03413.A31

Q2705 Do Not Stuff
Do Not Stuff
2ND = 84.2N702.031

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K		0.55V
120W	33.0K		0.82V
	47.0K		1.06V
	64.9K	100.0K	

ELETRÔNICA

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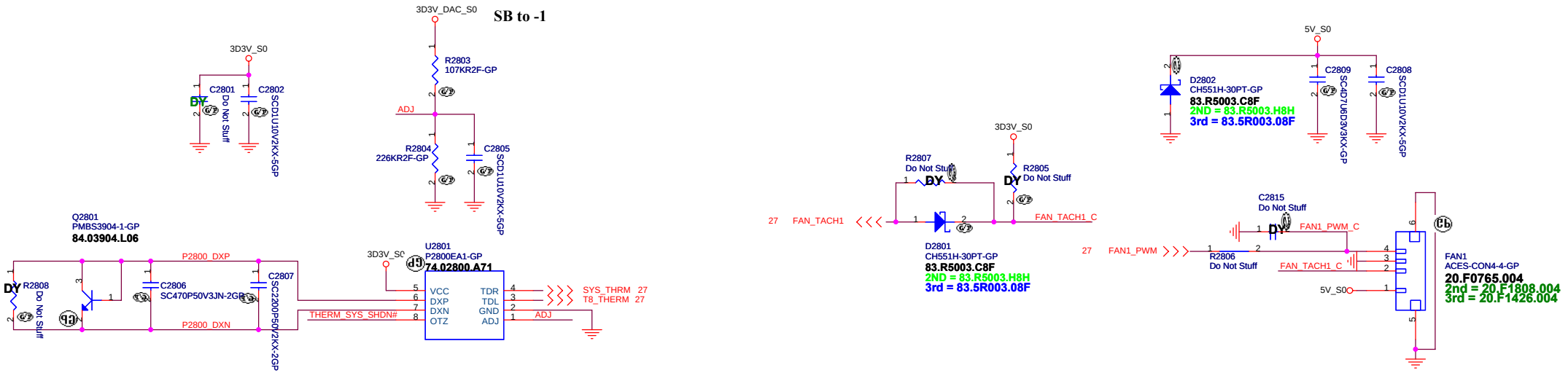
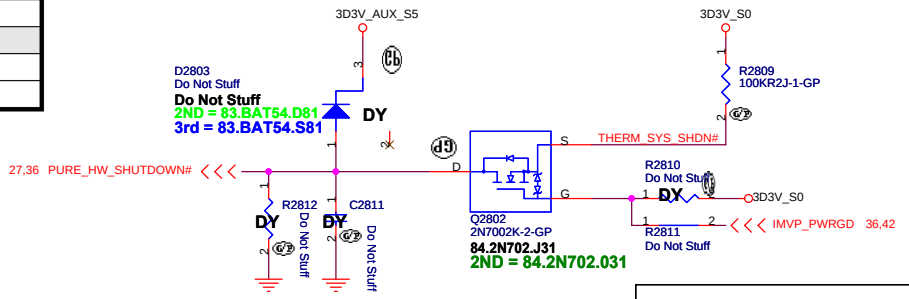


ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9



CONFID

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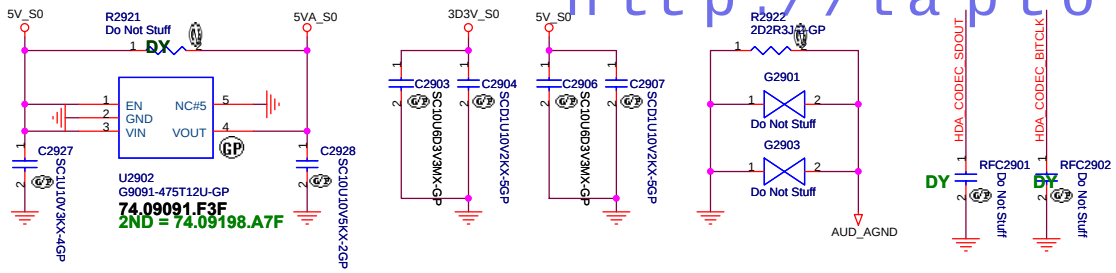
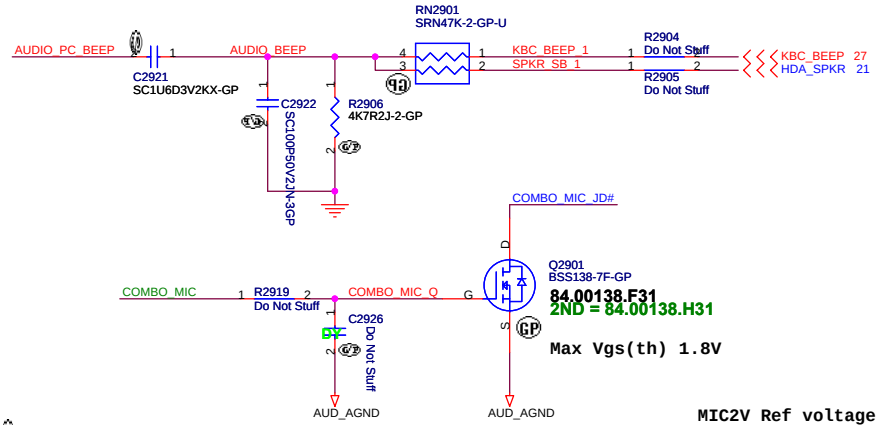
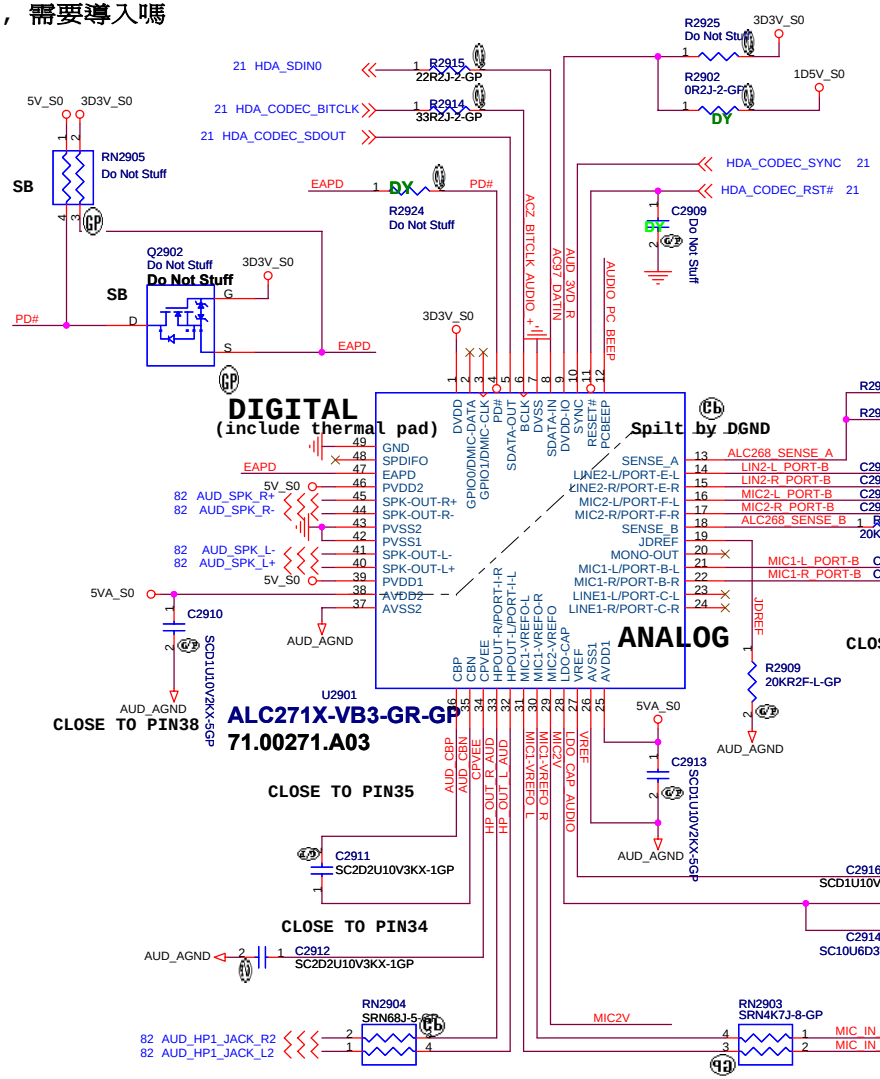


CLOSE TO PIN39 and 46

-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎





MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing

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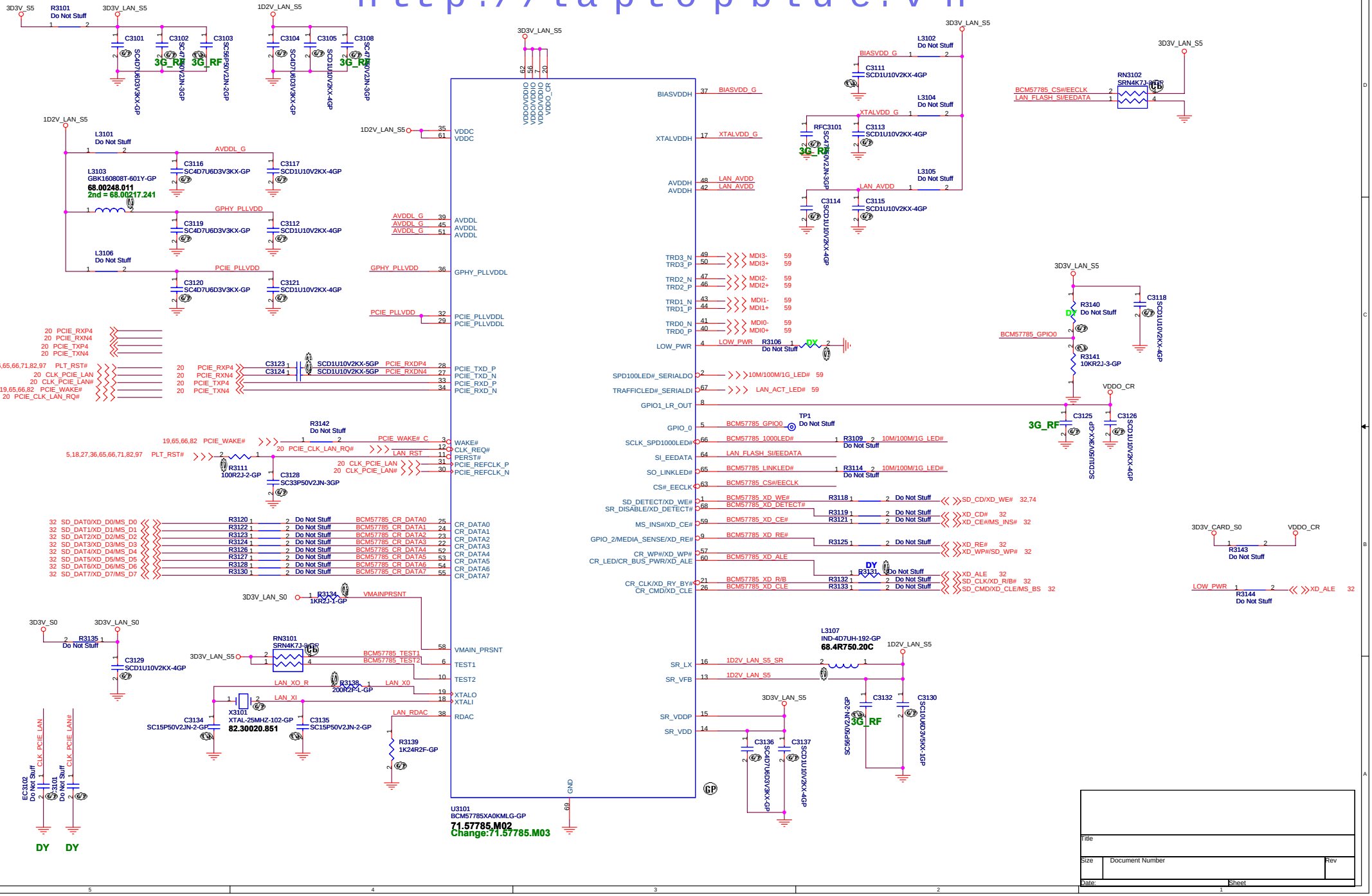
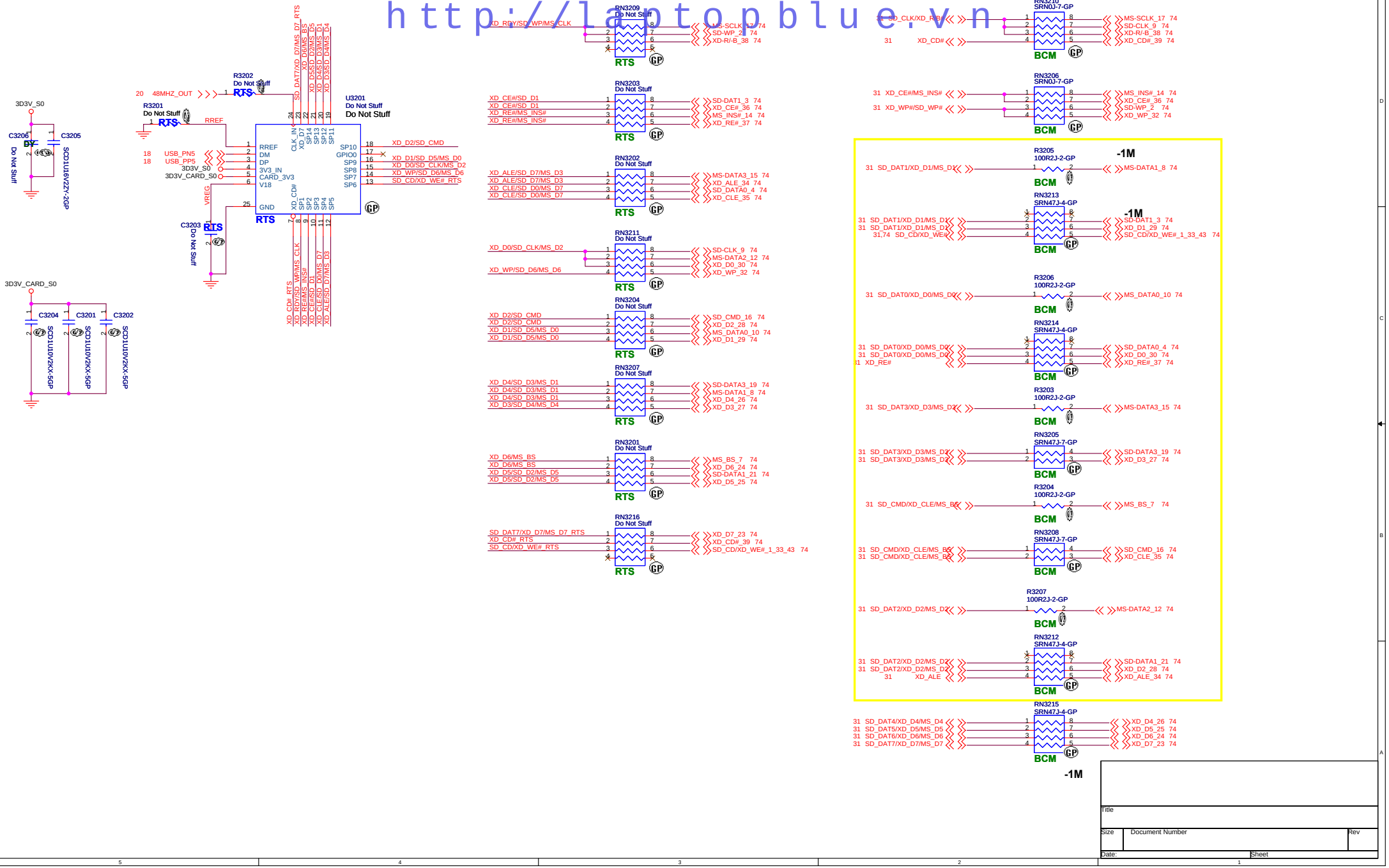


http://laptopblue.vn



ELETRÔNICA

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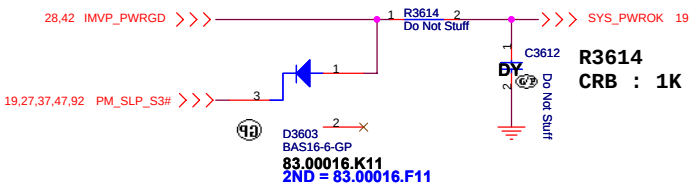
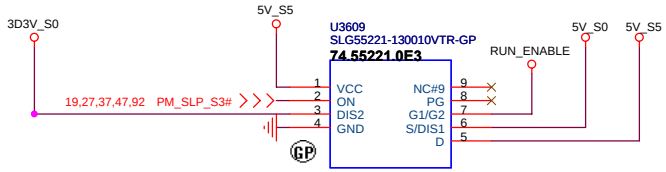
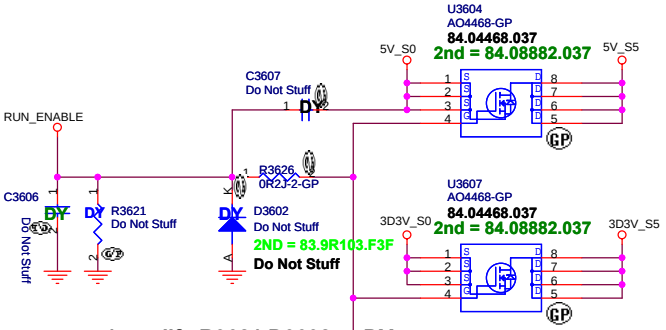
Power Sequence



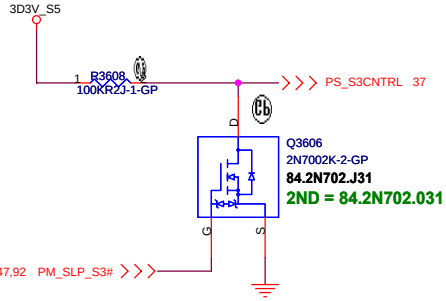
R3614
CRB : 1K

ANNIE Run Power



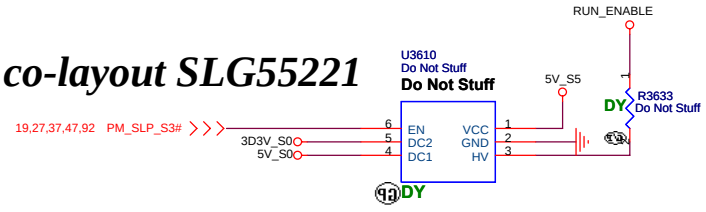


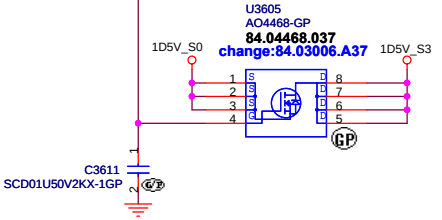
-1 modify R3621,D3602 to DY



SB modify part number

-1 co-layout SLG55221

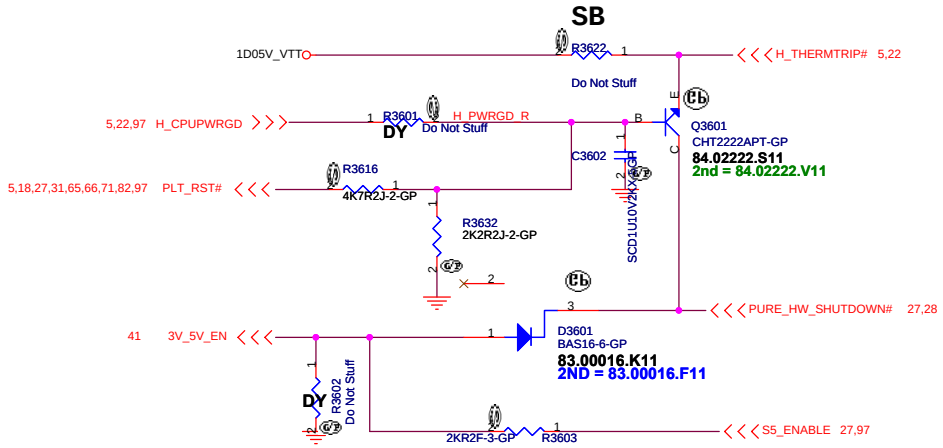




1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

SB



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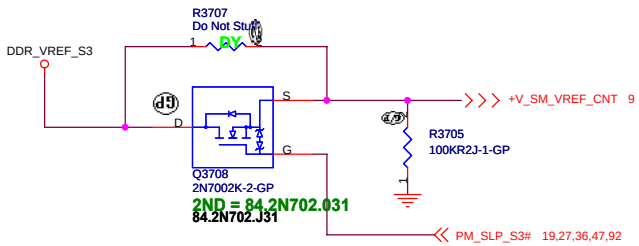

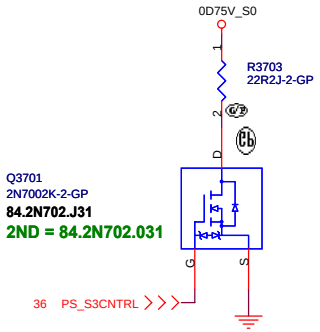

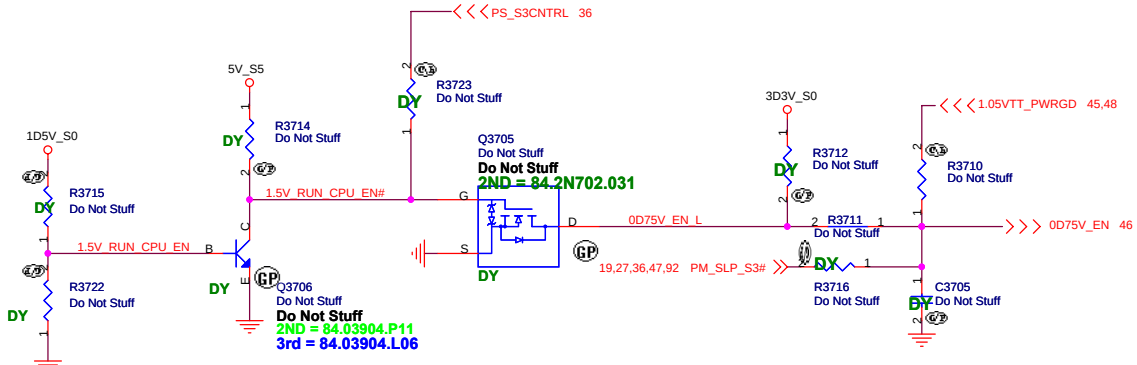

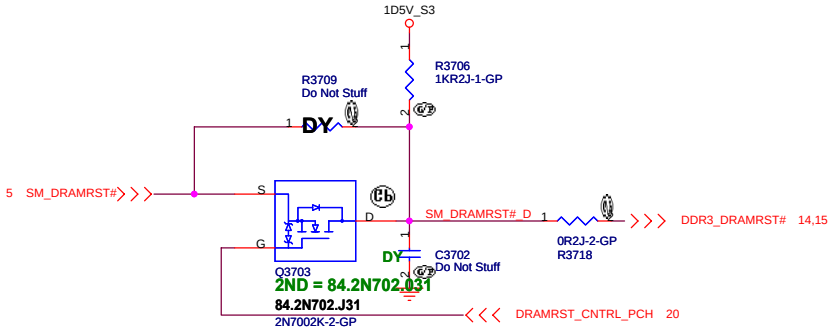

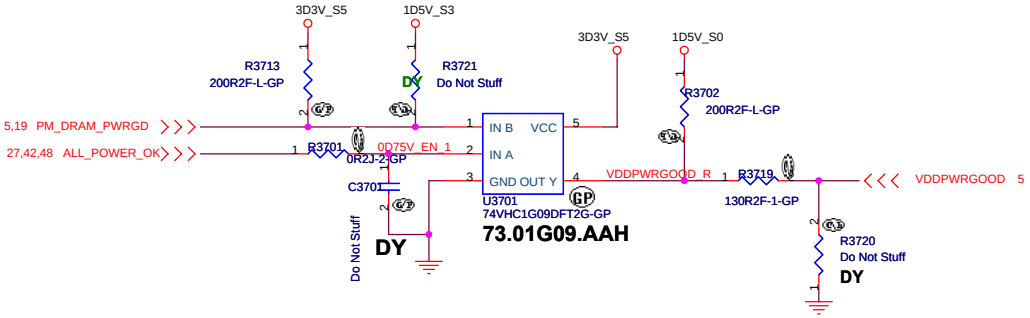

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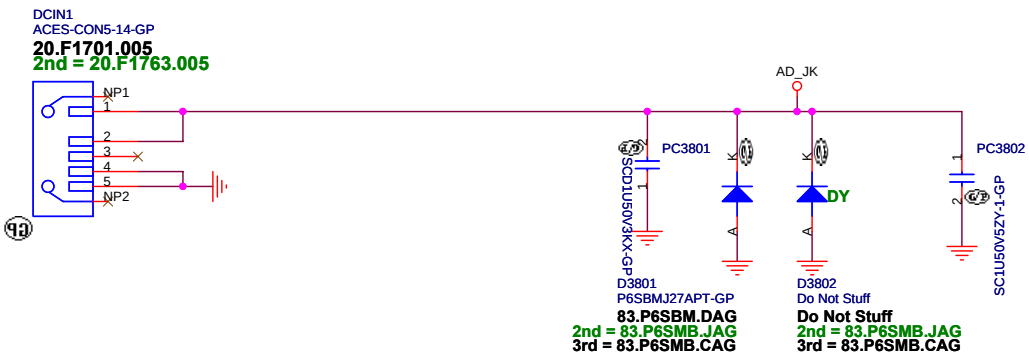

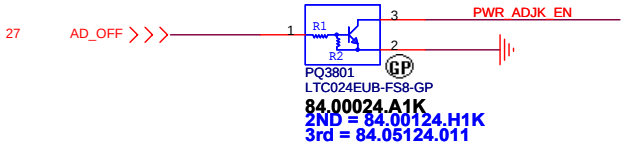

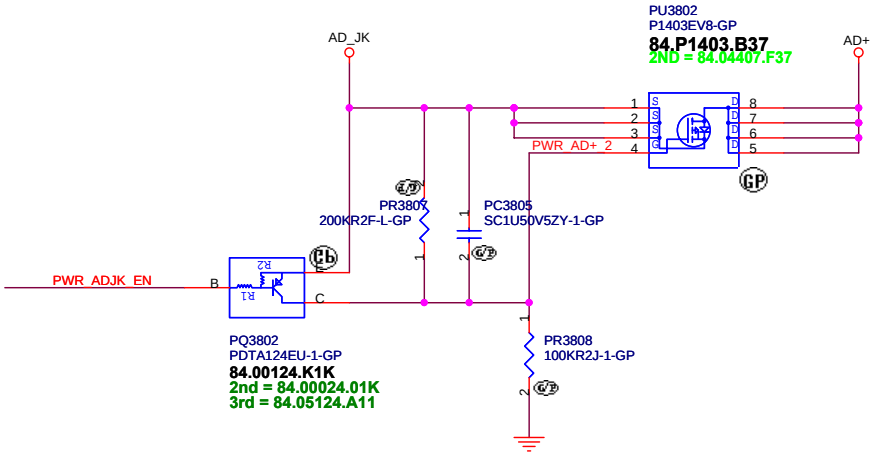

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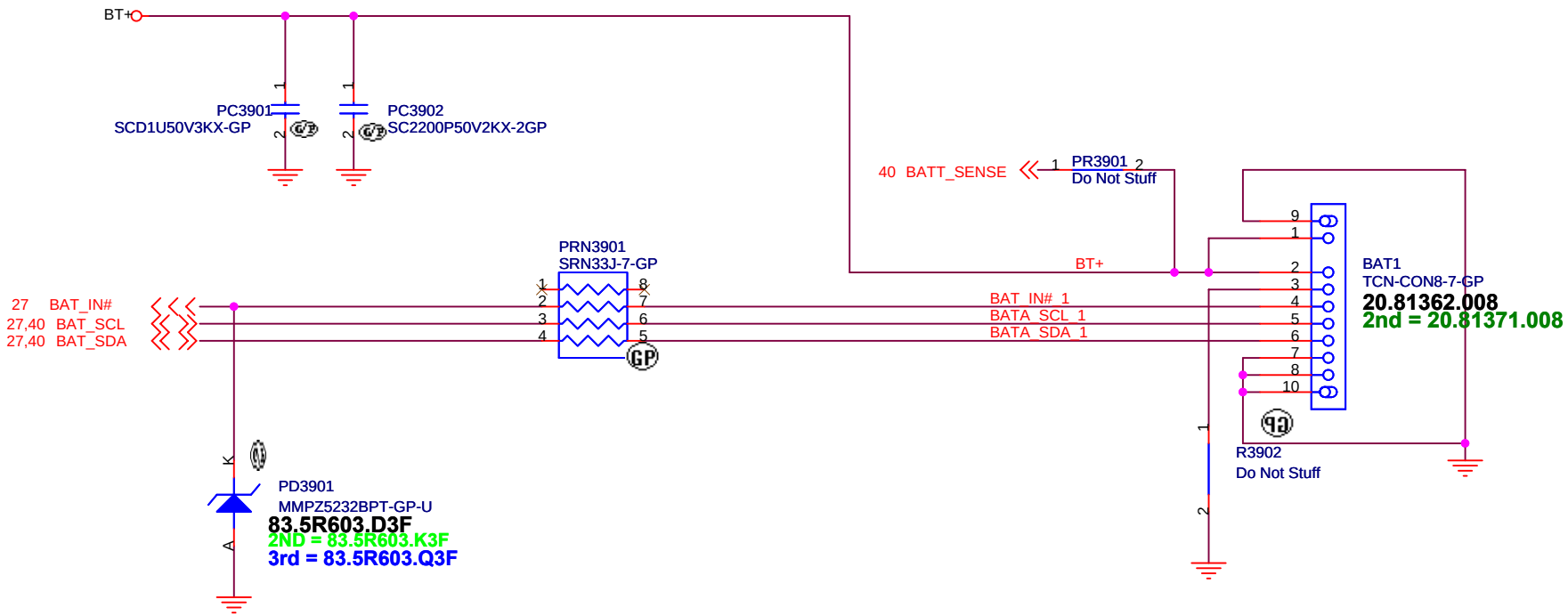

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AD+ total power	R1	R2	AD+ total power		
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

20100706 Wayne

20101018

-1M

-1M

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SBcheck power team

20100715

20100715

20100715

20100715

Iomax=6A
OCP>9A

SB to -1 change 7K32

Close to VFB Pin (pin5)

-1 EE modiyf PR4115 to 33K2 for SIV

Close to VFB Pin (pin2)

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

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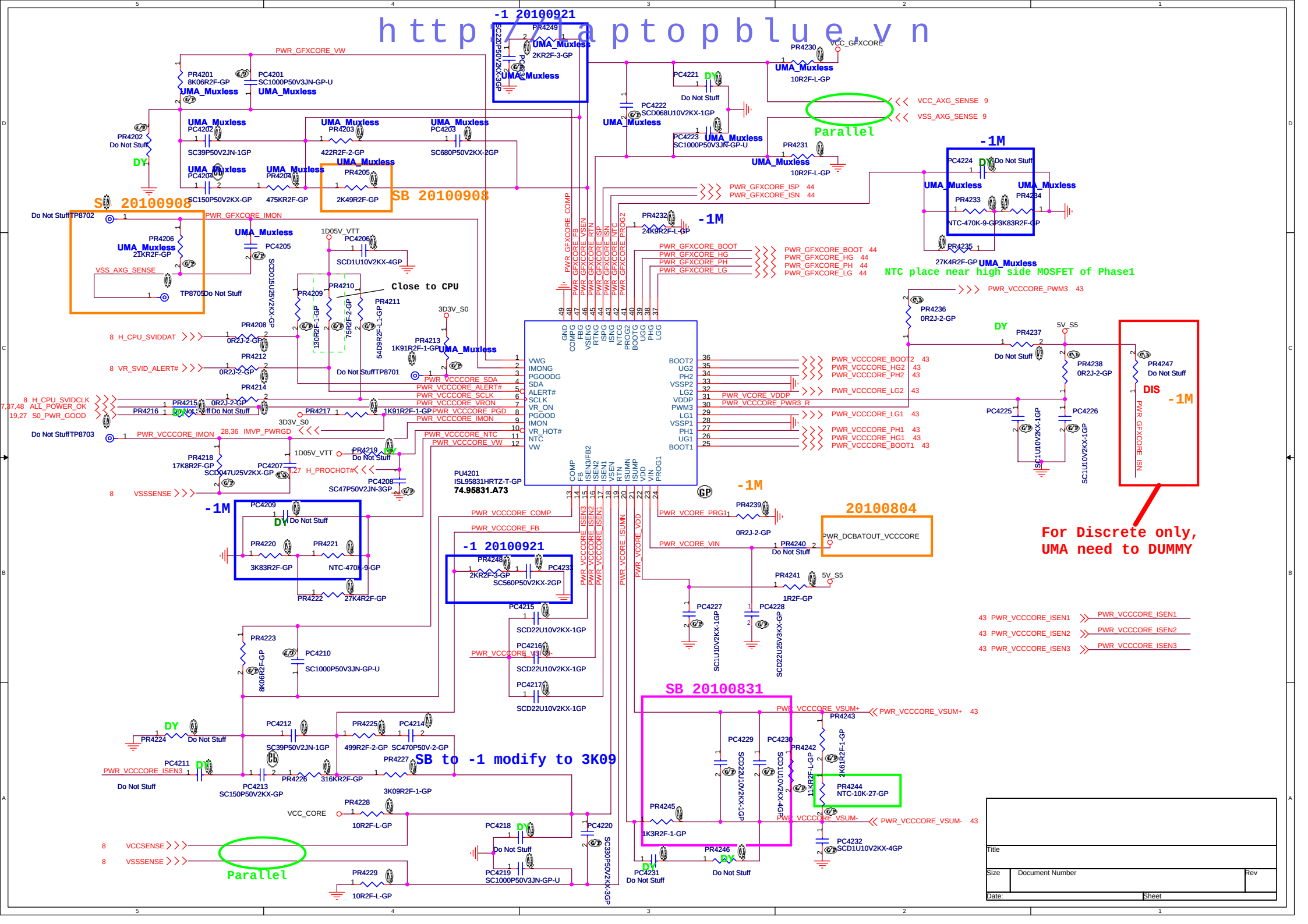

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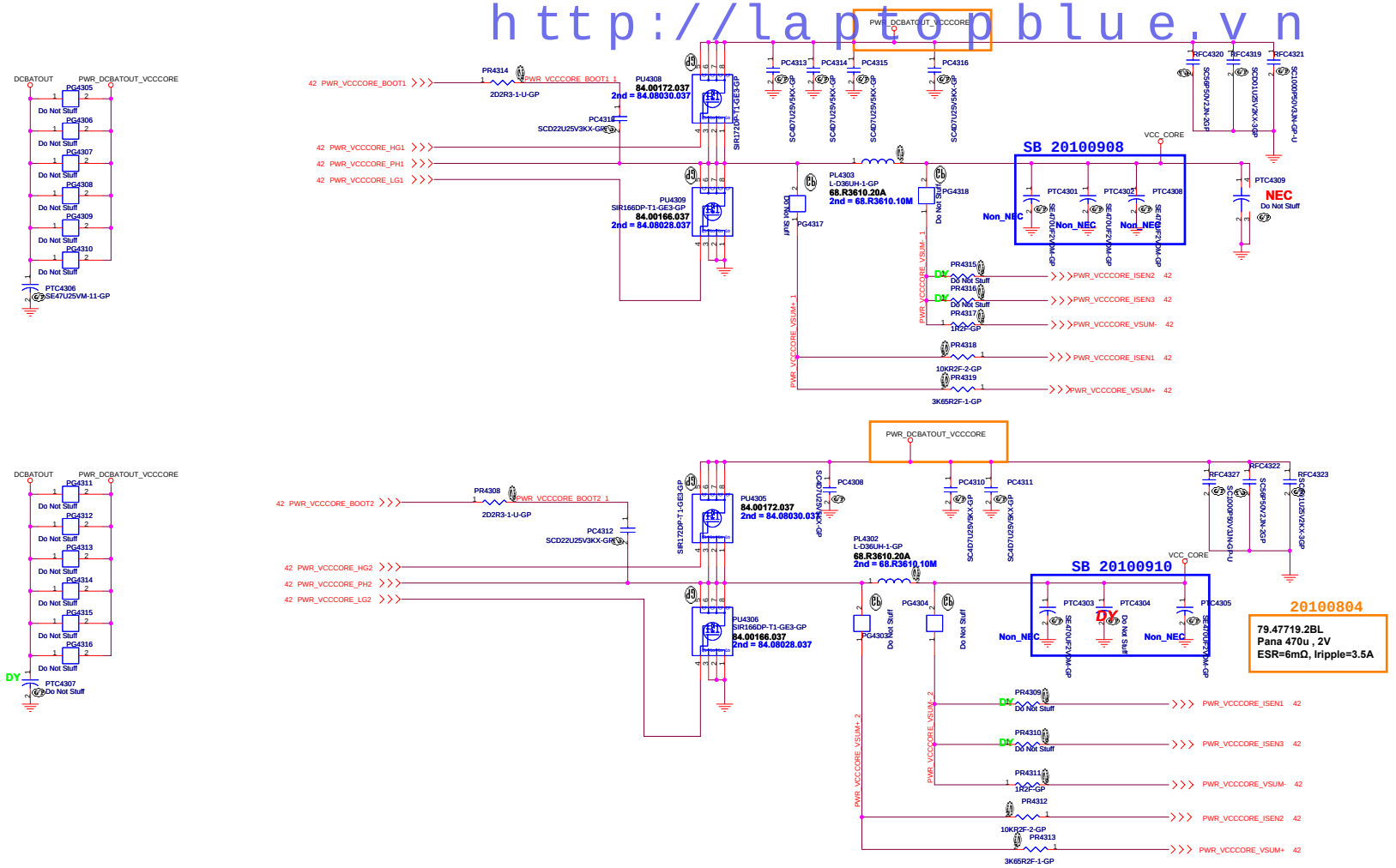

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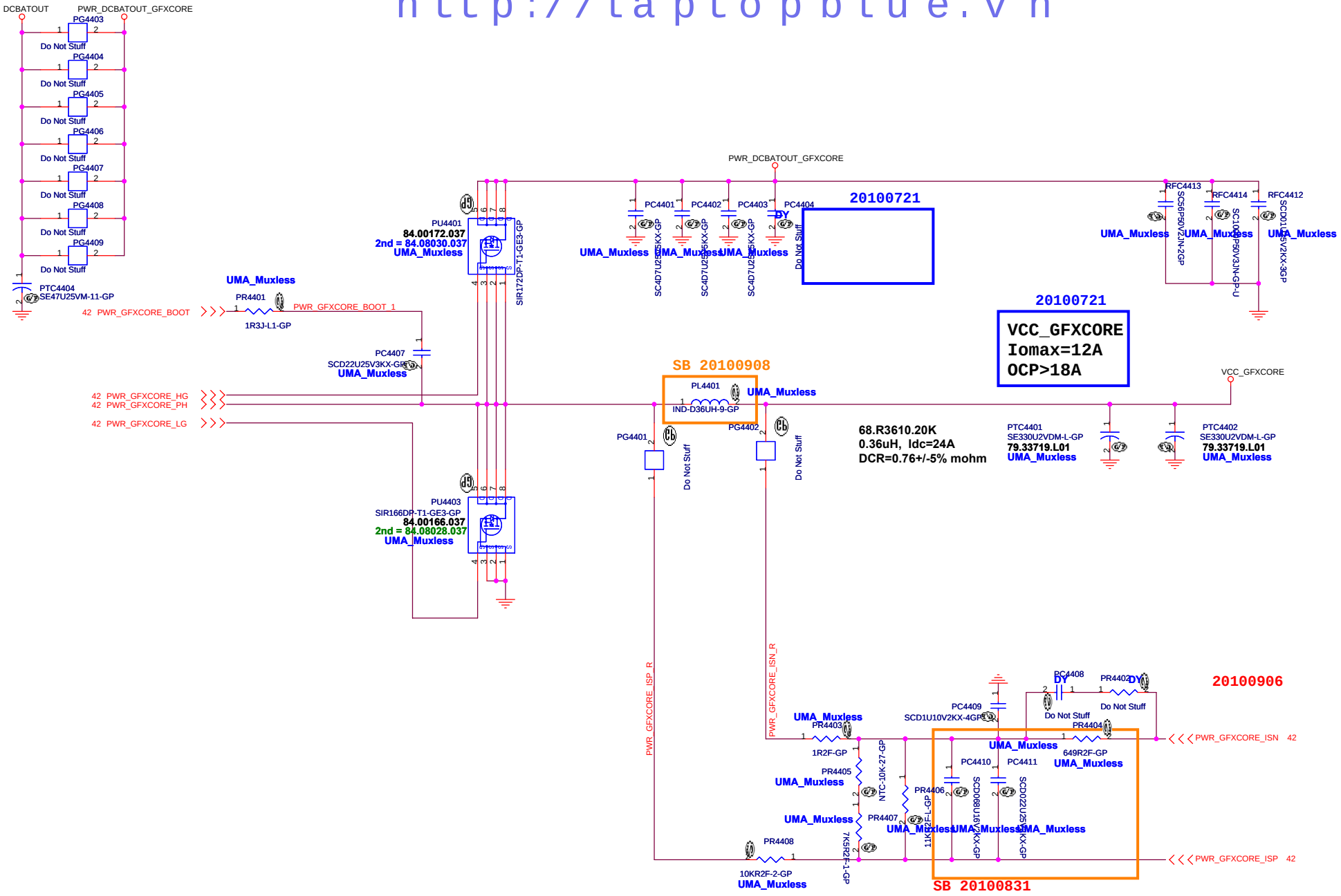

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TPS51218D for 1D05V

DCBATOUT PWR_DCBATOUT_1D05V
PG4501 Do Not Stuff
PG4502 Do Not Stuff
PG4503 Do Not Stuff
PG4504 Do Not Stuff
PTC4501 Do Not Stuff
DY

PWR_DCBATOUT_1D05V
RFC4512 SC56P50V2JN-2GP
RFC4513 SC100P50V3JN-GP-U
RFC4514 SCD01U25V2KX-3GP

1D05V_VTT PG4513 PG4514 PG4515 PG4516 PG4517 PG4518 PG4519 PG4520 Do Not Stuff
1D05V_PWR PG4505 PG4506 PG4507 PG4508 PG4510 PG4509 PG4511 PG4512 Do Not Stuff

PWR_DCBATOUT_1D05V
PC4504 SC47U25V5KX-GP
PC4506 SC47U25V5KX-GP
PC4507 SCD01U25V2KX-3GP
PC4511 SCD1U25V3KX-GP

20100728
Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

PU4502
84.15N03.037
2nd = 84.08065.037
RMW150N03FUBGPJU

2nd source 還未導入74.08237.073

Freq=360KHz

Iomax=14A
OCP>21A

Mag. 0.56uH 10*10*4
DCR=1.6~1.8mohm
Idc=25A, Isat=40A

3D3V_S0 PR4516 10KR2J-3-GP
37,48 1.05VTT_PWRGD
46,47 RUNPWROK PR4512 0R2J-2-GP
PR4504 82KR2F-1-GP
PC4505 SC1KP50V2KX-1GP
PR4503 470KR2F-GP

PU4501
TPS51218DSCR-GP-U1
74.51218.073
PGOOD TRIP EN VFB RF GND VBST DRVH SW V5IN DRVL
PWR_1D05V_IMAX PWR_1D05V_EN PWR_1D05V_VFB PWR_1D05V_CCM
PWR_1D05V_BOOT PWR_1D05V_UGATE PWR_1D05V_PHASE PWR_1D05V_LGATE

PR4505 2D2R3-1-U-GP
PC4503 SCD1U25V3KX-GP
PWR_1D05V_BOOT_R
5V_S5

SB 20100831

PU4503
84.18003.037
2nd = 84.08062.037
RMW180N03FUBTB-GP

20100906
PL4501
IND-D56UH-27-GP
68.R5610.10P
2nd = 68.R5610.20H

1D05V_PWR
PC4508 DY SC18P50V2JN-1GP
PC4509 SCD1U50V3KX-GP 1G_RF
PR4506 10R2F-L-GP
VTT_SENSE_L
PR4507 10KR2F-2-GP
PWR_1D05V_VFB
PR4508 20KR2F-L-GP
VSS_SENSE_L
PR4509 10R2F-L-GP
PTC4502 Do Not Stuff
PTC4503 SE330U2VDM-L-GP
Do Not Stuff
79.33719.L01
2nd = 77.C3371.051 2nd = 77.C3371.051

20100728
Id=19.4A
Qg=16.8~25.5nC
Rdson=4.9~6.1mohm

VTT_SENSE_L PR4510 DY Do Not Stuff
PC4510 DY Do Not Stuff
VSS_SENSE_L PR4511 DY Do Not Stuff
VCCIO_SENSE
VSSIO_SENSE

20100728
Vout=0.704*(1+R1/R2)

20100728

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SSID = PWR.Plane.Regulator_1p5v0p75v

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20100805

RT8207L for 1D5V

SB 20100831

20100728

Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

20100906

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Iomax=12A
OCP>20A

Close to pin23

Close to pin23

20100728

Close to output cap pin1, not inside of the output cap

2nd source 還未導入74.51116.073

-1 PR4608 需要將來都改32k4,將

Close to PIN9

Vout=0.75*(1+R1/R2)

20100728

SB R4608 chekc 修改31K6R
Vout 需再1.55V 以上

+0.75VS
Iomax: 1.2A

DY

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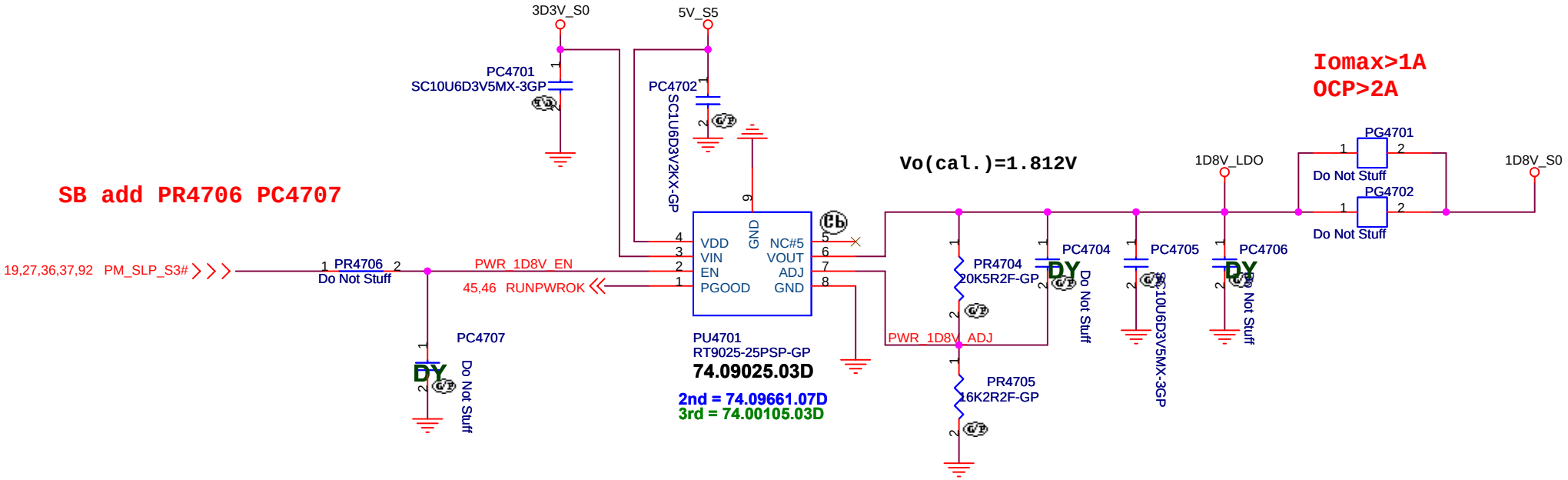
SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



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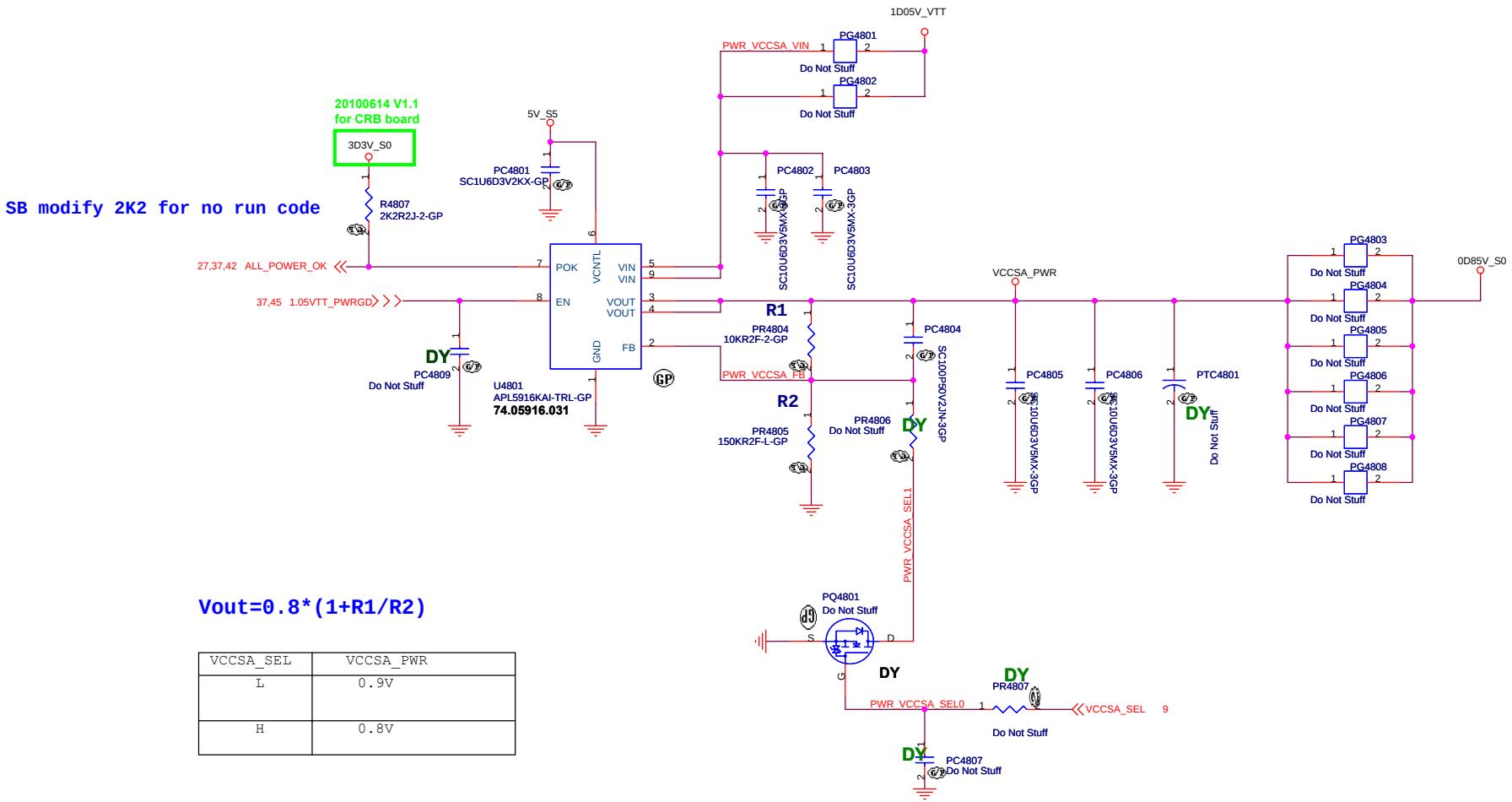
APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

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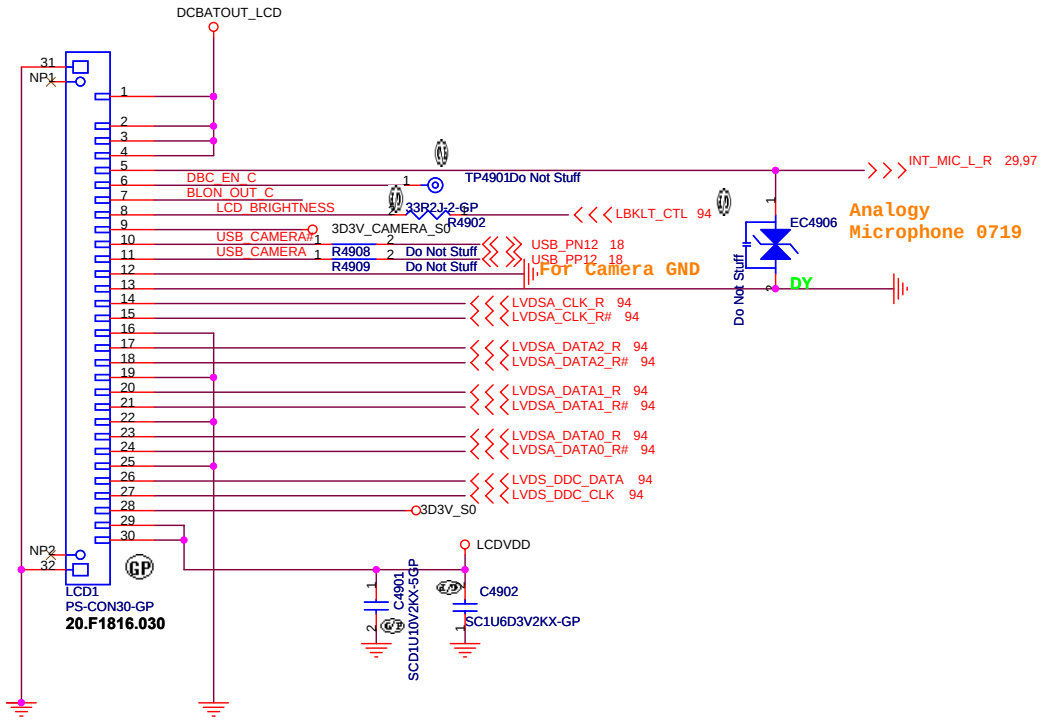
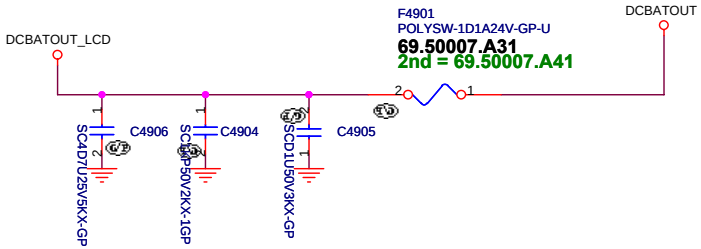
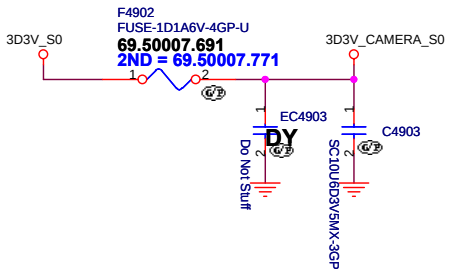
LVDS CONNECTOR



INVERTER POWER

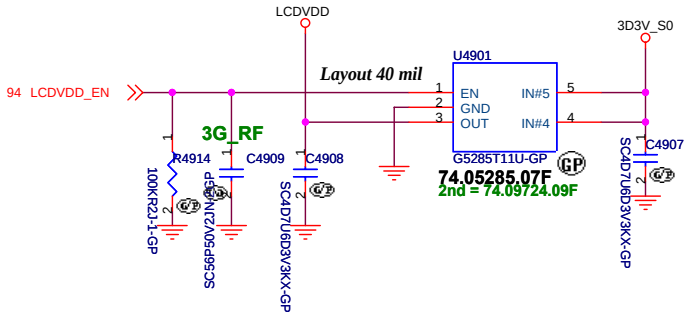


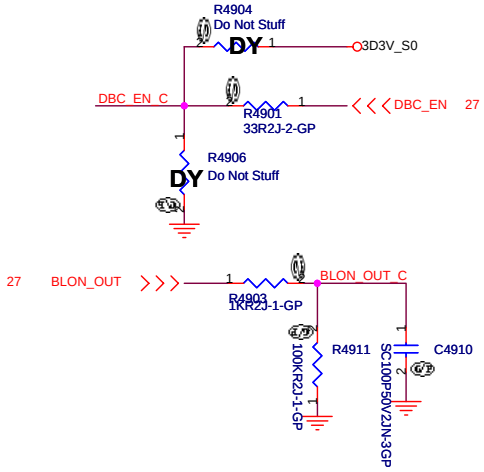
Camera Power



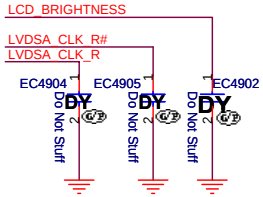
SSID = VIDEO

LCD POWER for ANNIE





For EMI request
Close to LVDS connector



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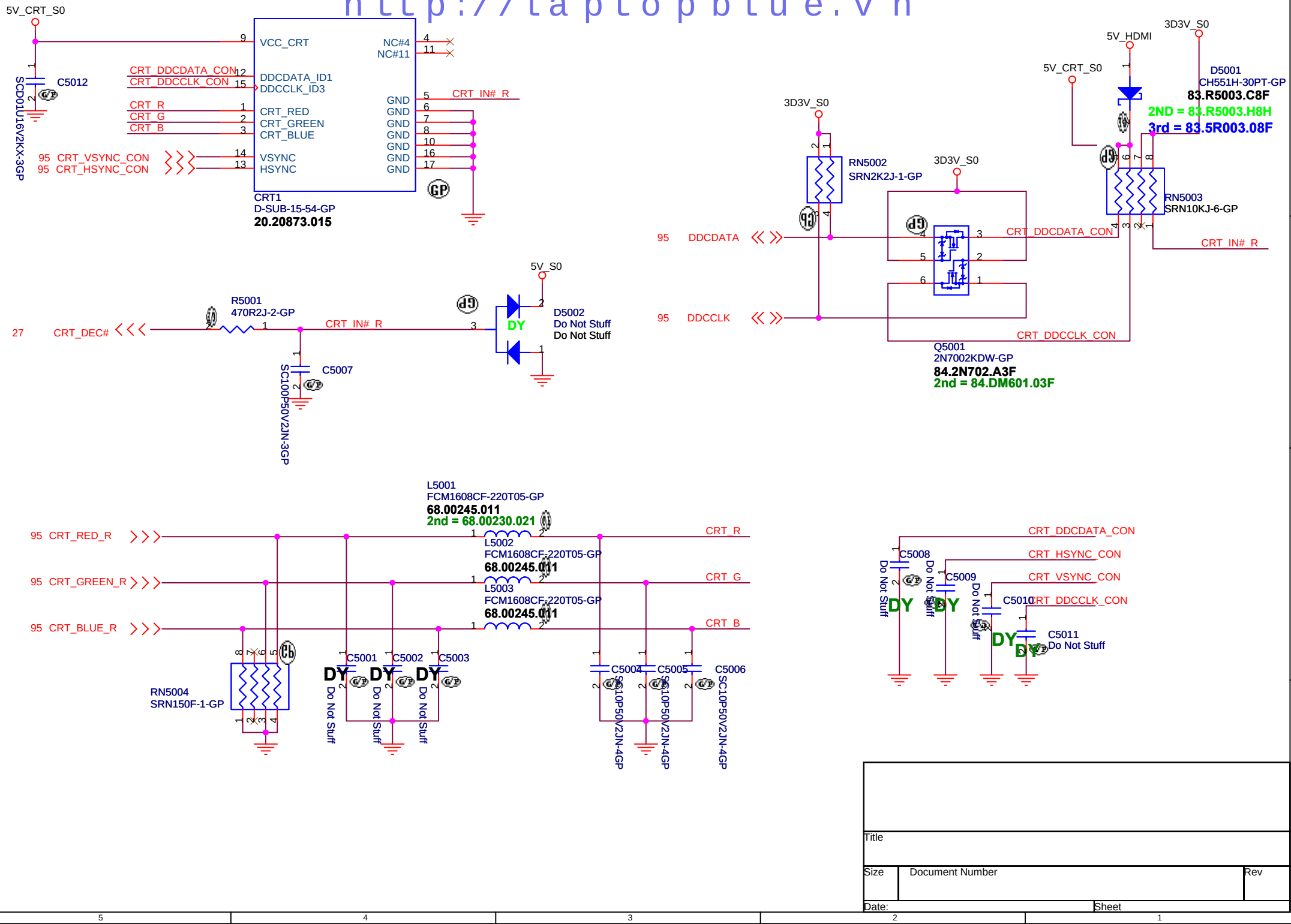

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HDMI Level Shifter & CONNECTOR

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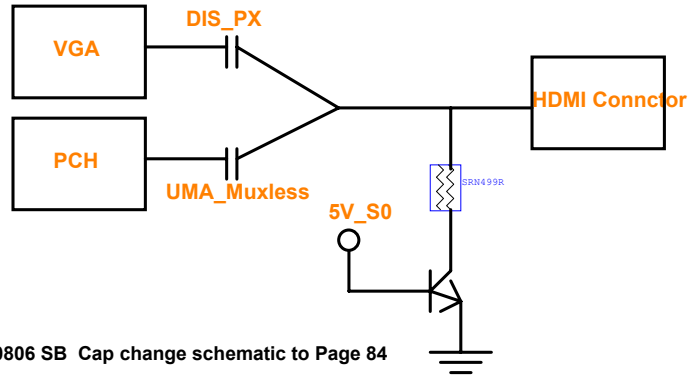
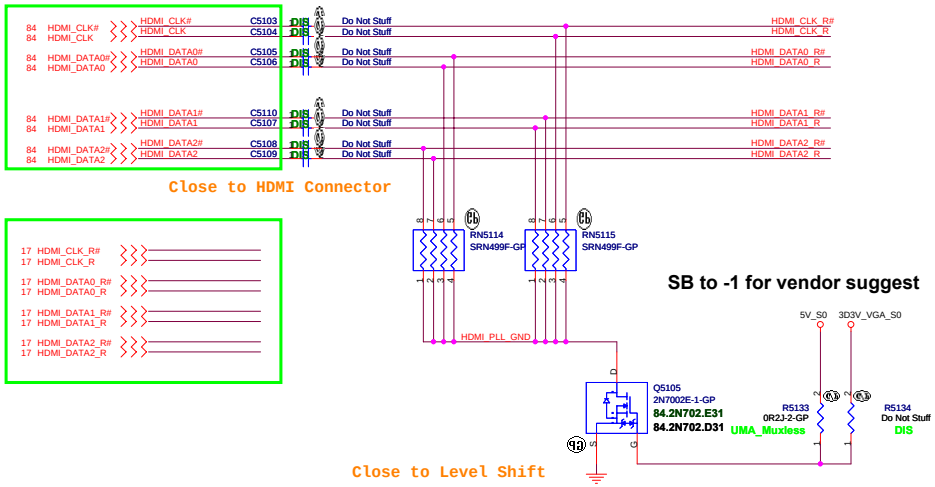
HDMI CONN

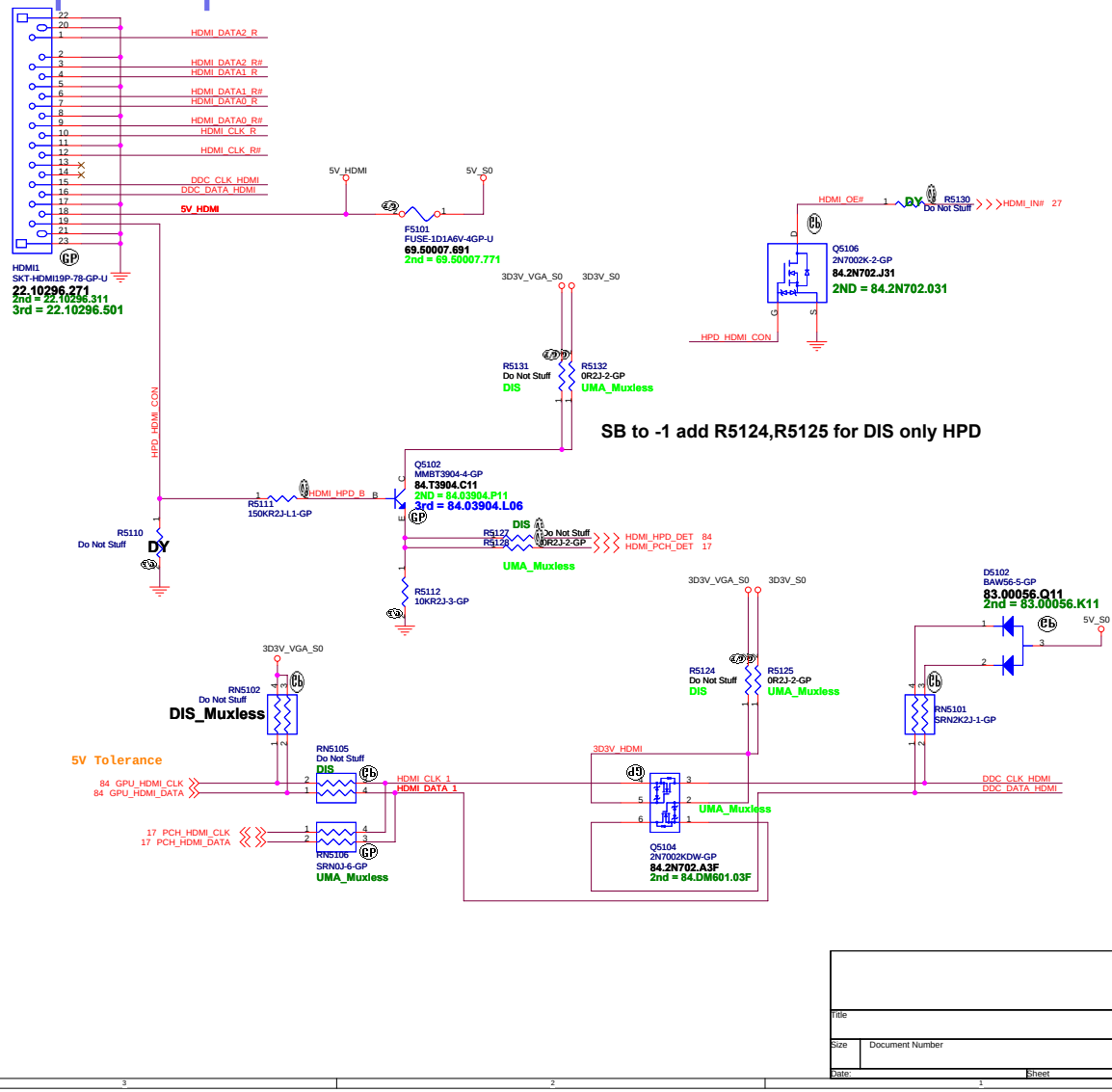
UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84





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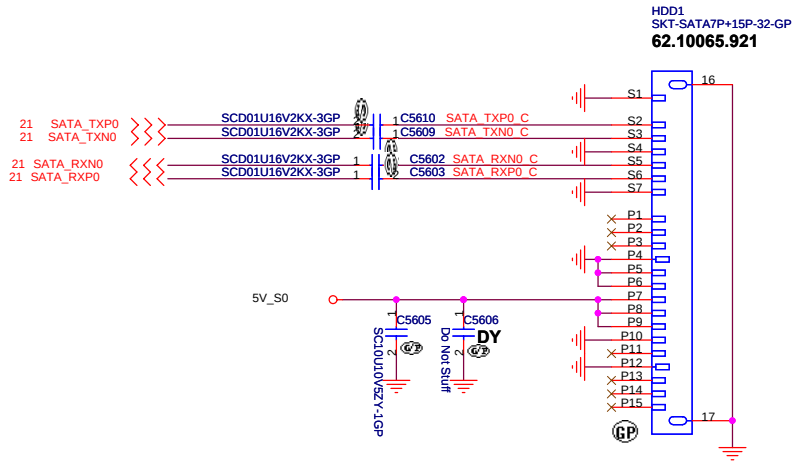
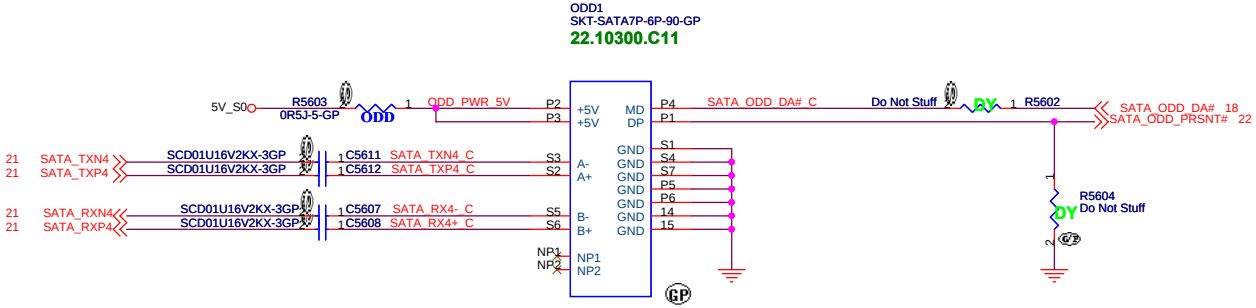
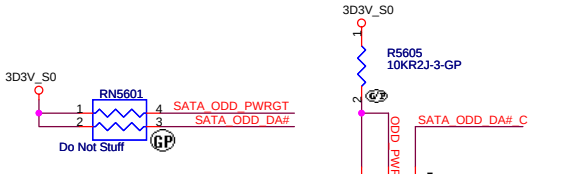


ODD Connector



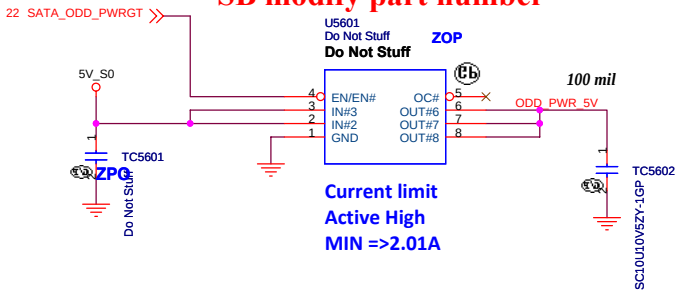


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



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GIGA Lan Transformer

SB modiyf Pin9 Pin10 SWAP

LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

MDI3+ MDI3- MDI2- MDI2+ MDI1+ MDI1- MDI0- MDI0+

XRF_TDC1 XRF_TDC2 XRF_TDC3 XRF_TDC4

C5901 C5902 C5903 C5904 SCD1U10V2KX-5GP

1CT:1CT Tx Side Rx Side

RJ45_7 MCT2 RJ45_8 RJ45_5 MCT1 RJ45_4 RJ45_3 MCT4 RJ45_6 RJ45_2 MCT3 RJ45_1

LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-)::ORANGE

CONN_PWR2 CONN_PWR RJ45_1 RJ45_2 RJ45_3 RJ45_4 RJ45_5 RJ45_6 RJ45_7 RJ45_8

31 10M/100M/1G_LED#
31 LAN_ACT_LED#

GREEN ORANGE

RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91

RN5901
SRN470J-4-GP-U
3D3V_S5

EC5901 EC5902 Do Not Stuff DY

SB modify For EMI

U5901 U5902 U5903 U5904
5V_S5
TVLST2304AD0-GP
SURGE

31 MDI1+ 31 MDI1-
31 MDI0+ 31 MDI0-
31 MDI3+ 31 MDI3-
31 MDI2+ 31 MDI2-

GDT1 GDT2 GDT3 GDT4
BSB063X2X2312T203-GP
SURGE

MCT1 MCT2 MCT3 MCT4

R5903 R5901 R5902 R5904
75R3J-L-GP
MCT_R

C5905 SC1KP2KV6KX-GP

C5916 C5917 C5918 C5919 Do Not Stuff DY

XRF_TDC1 XRF_TDC2 XRF_TDC3 XRF_TDC4

EC5910 EC5909 EC5903 EC5904 EC5905 EC5906 EC5908 EC5907
SCD28P50V2CN-GP

C5907 C5906 DY

LAN_ACT_LED#
10M/100M/1G_LED#

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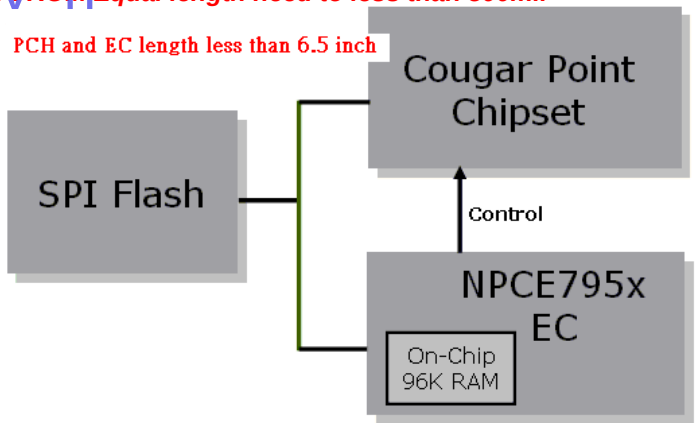
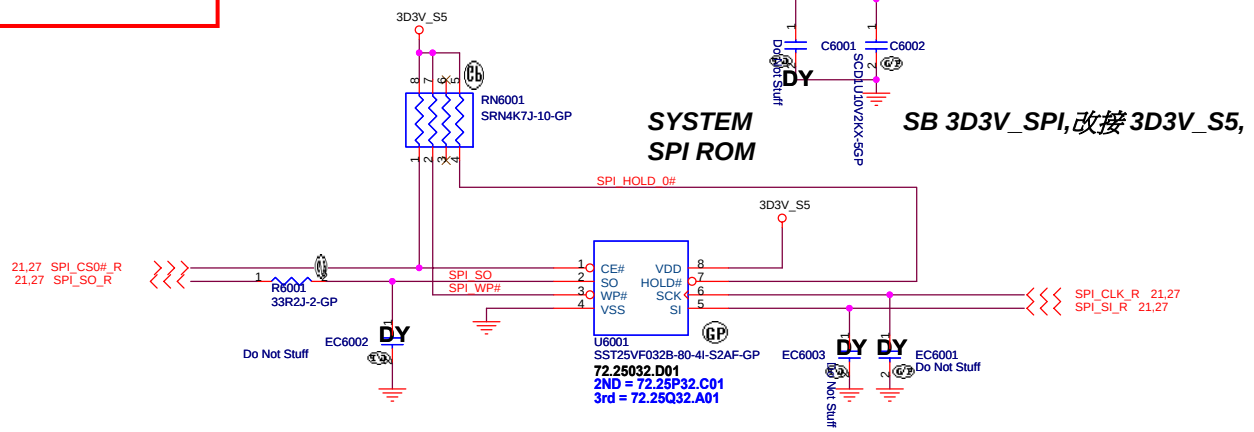
SPI FLASH ROM (4M byte) for PCH

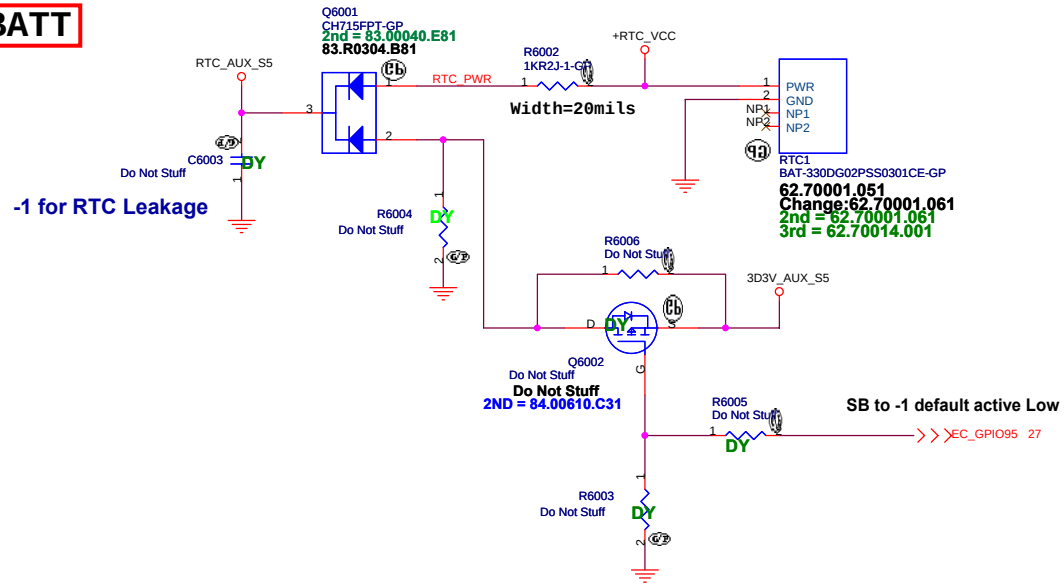
SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch





SSID = RBATT



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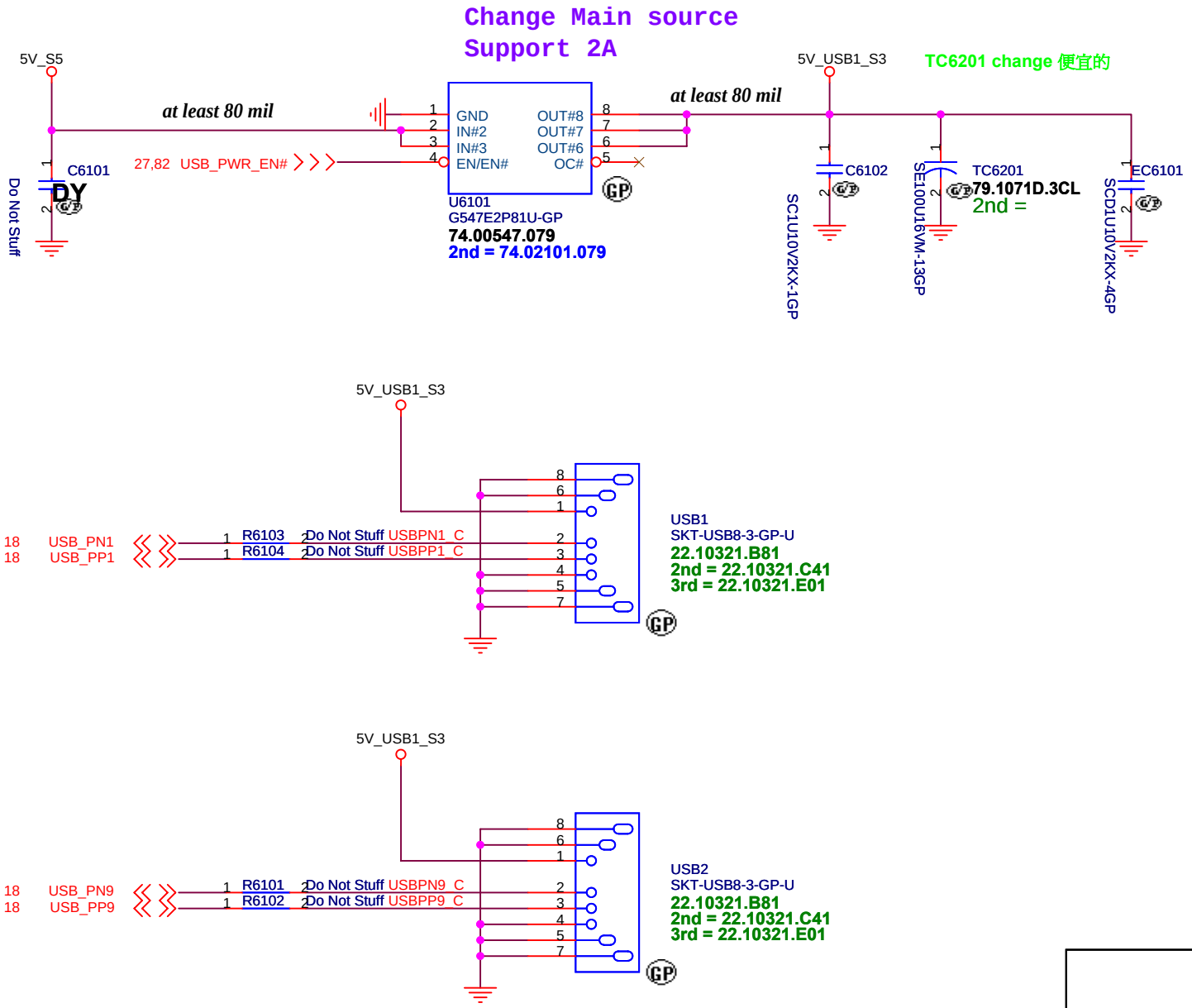

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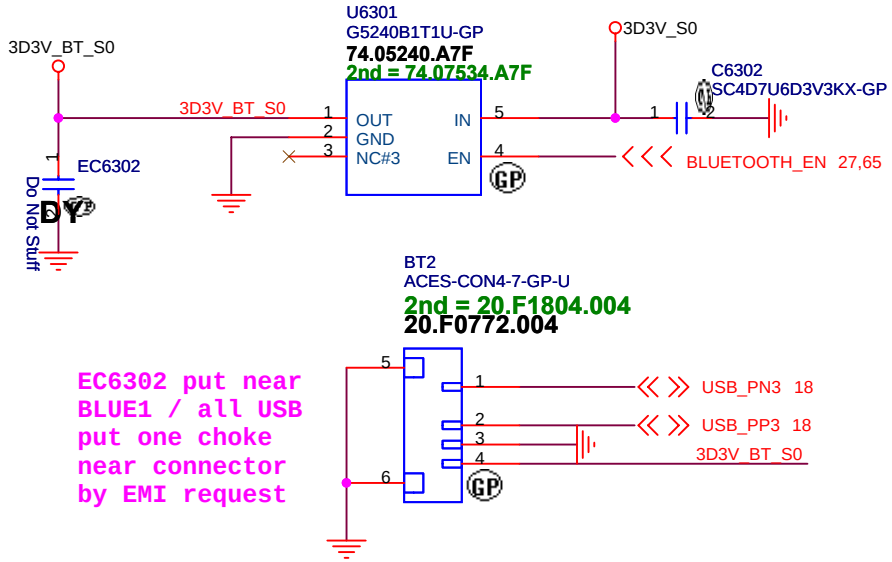
Bluetooth Module conn.

ANNIE Bluetooth Module



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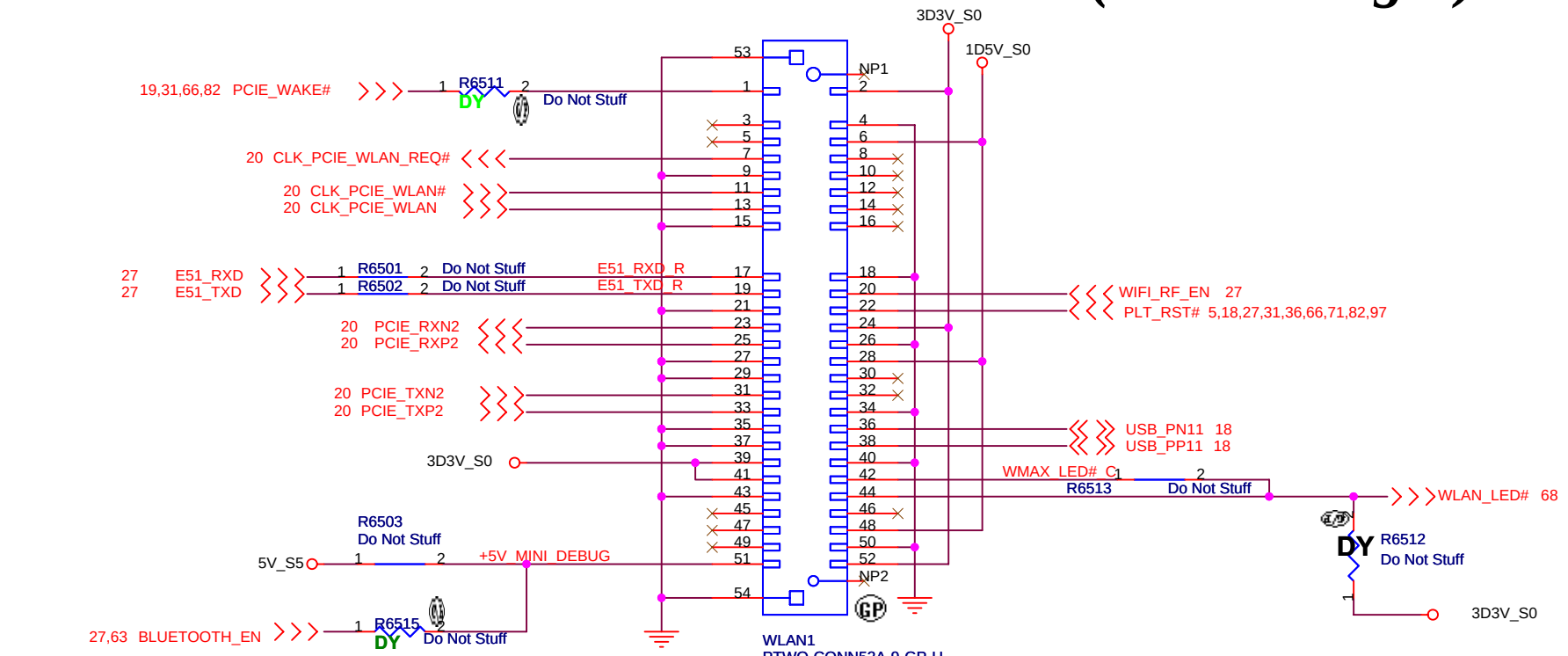
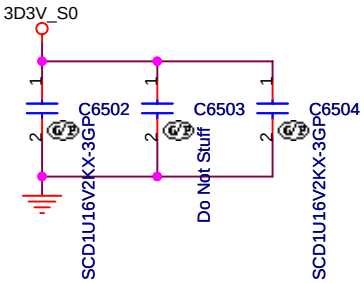
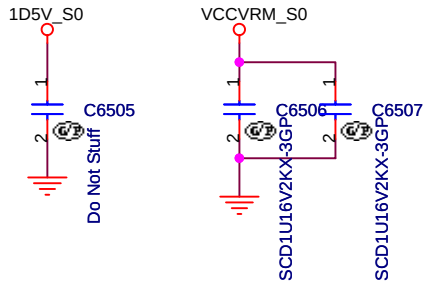
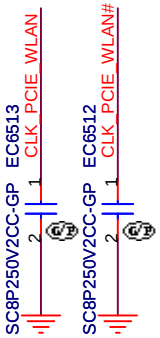
Mini Card Connector(802.11a/b/g/n)



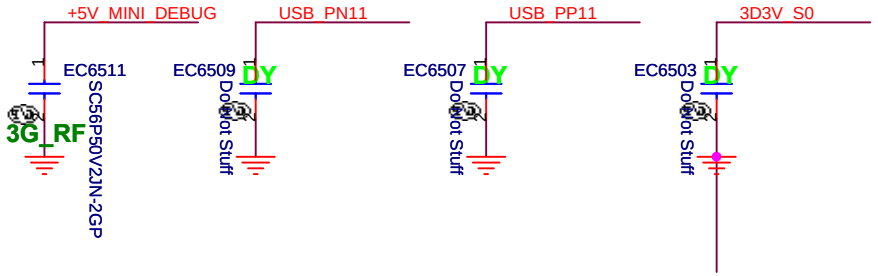


SB modify for SIV





RF suggestion



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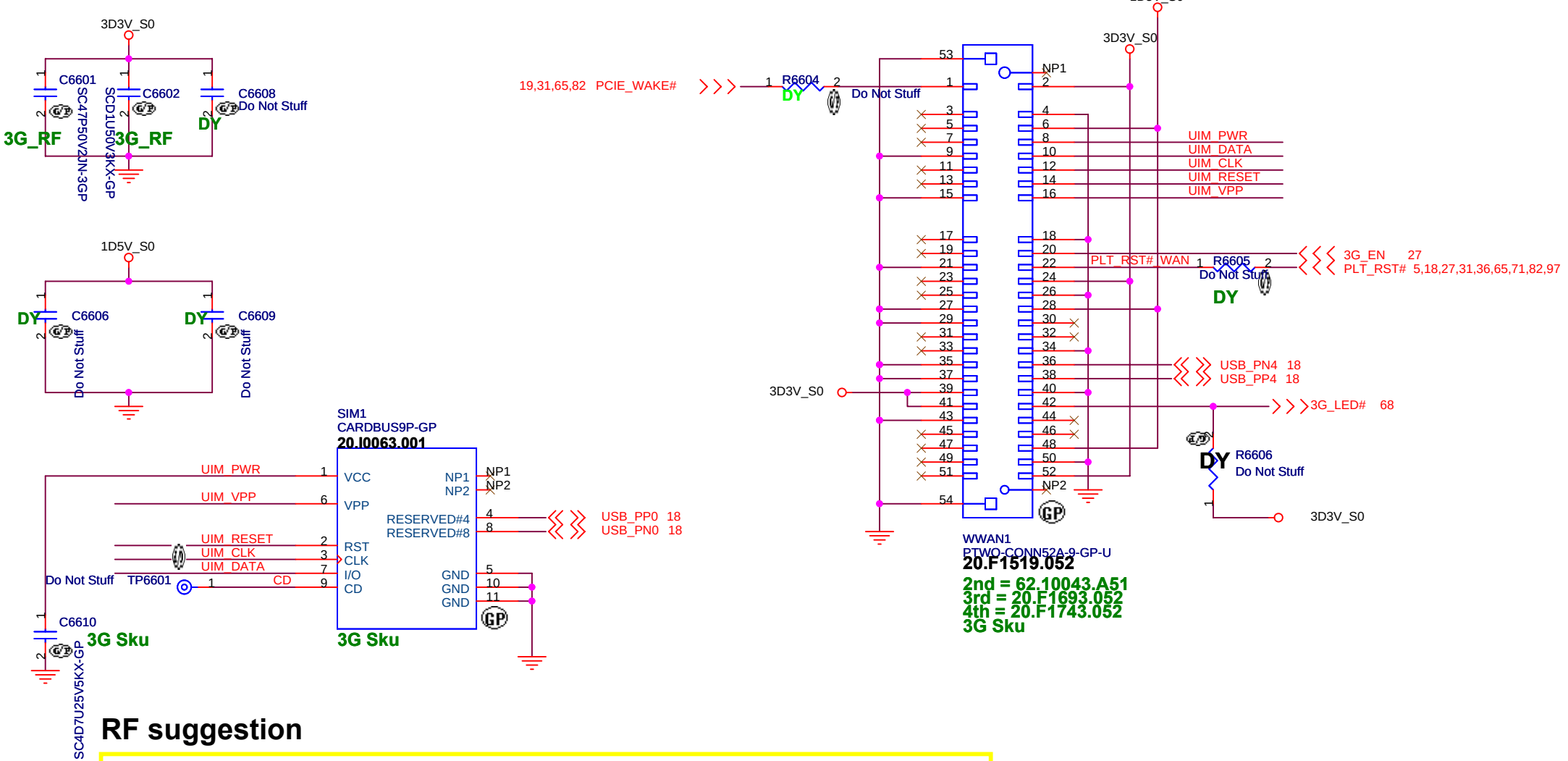
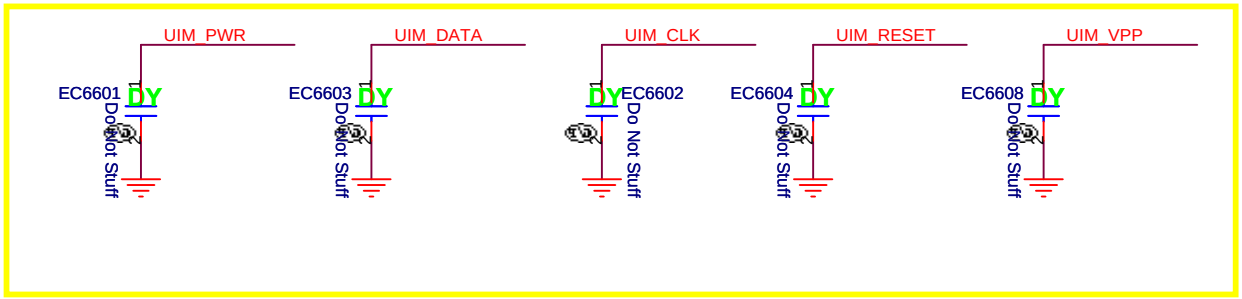
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



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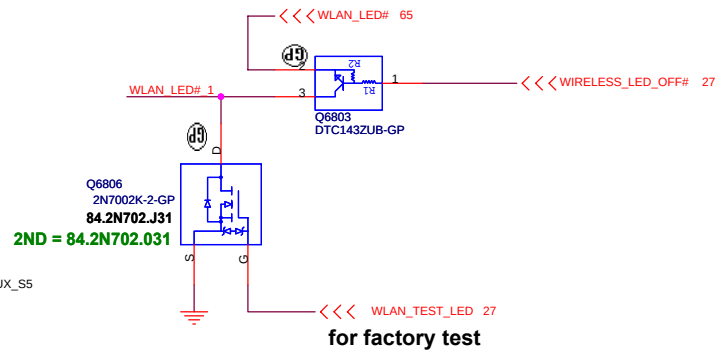
WLAN_LED

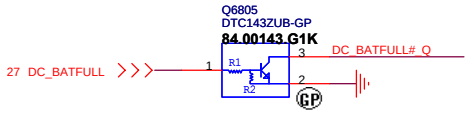
Power button LED

Power STDBY_LED

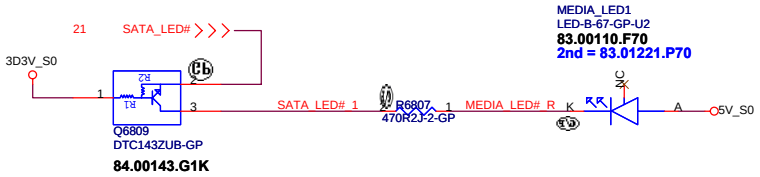
From module



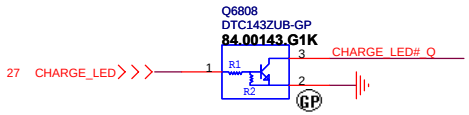
Battery LED2(DC_BATFULL)

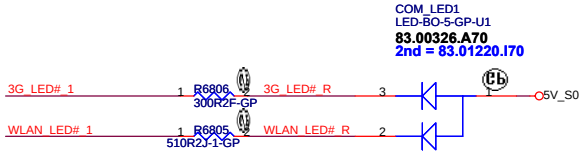


SATA HDD LED



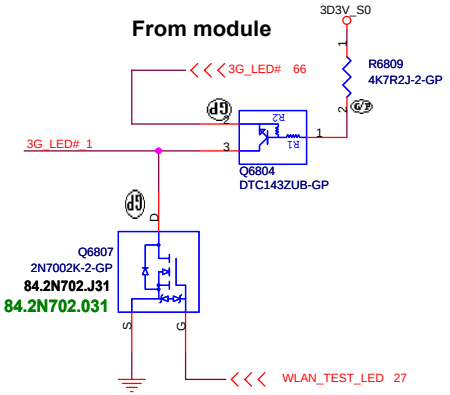
Battery LED1(CHARGE)





3G LED

From module



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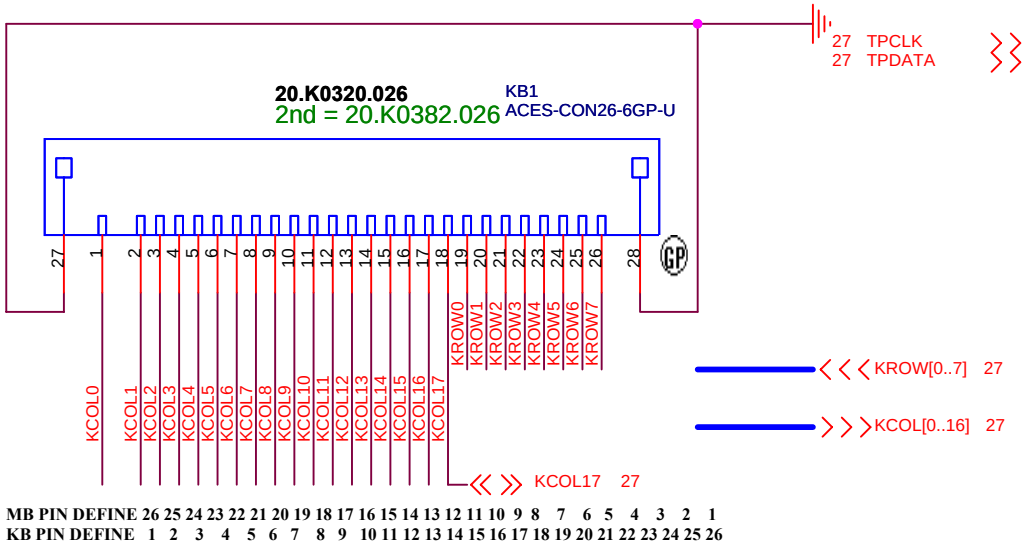
TOUCH PAD

FFC 異面

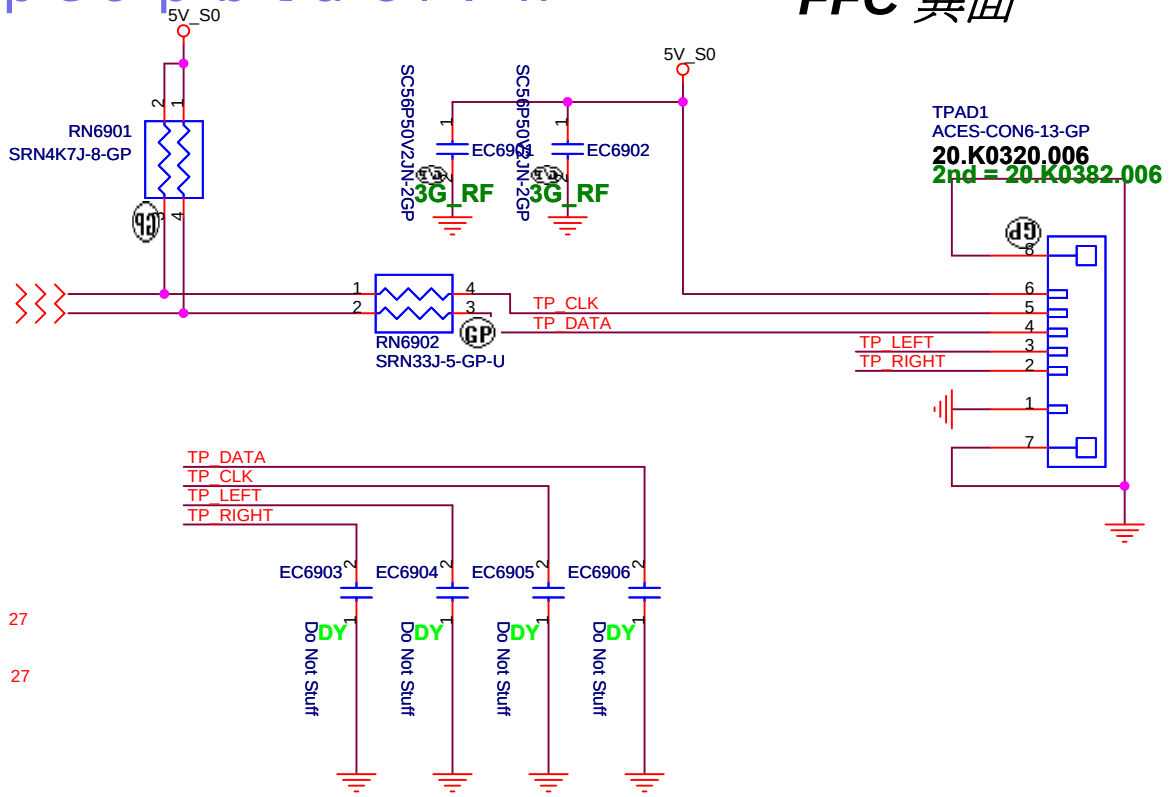
Internal KeyBoard Connector

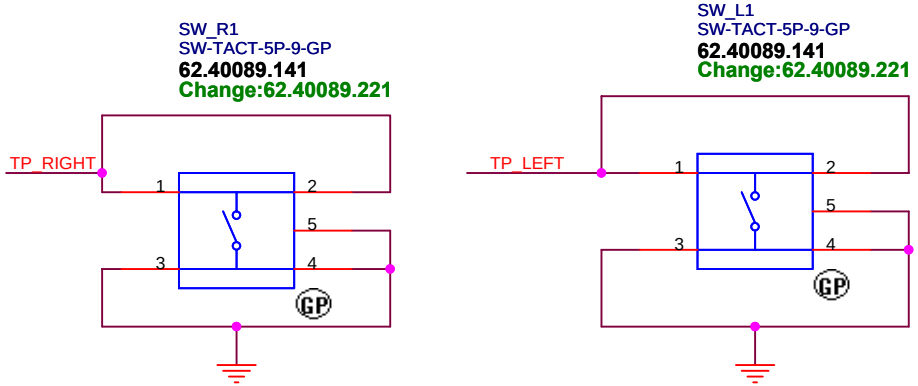


MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1

SB to -1 modify Part number





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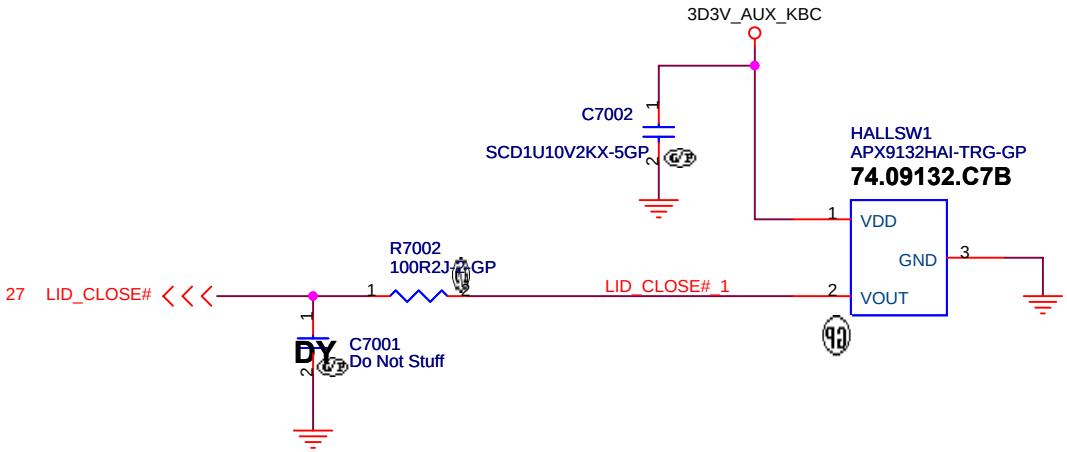

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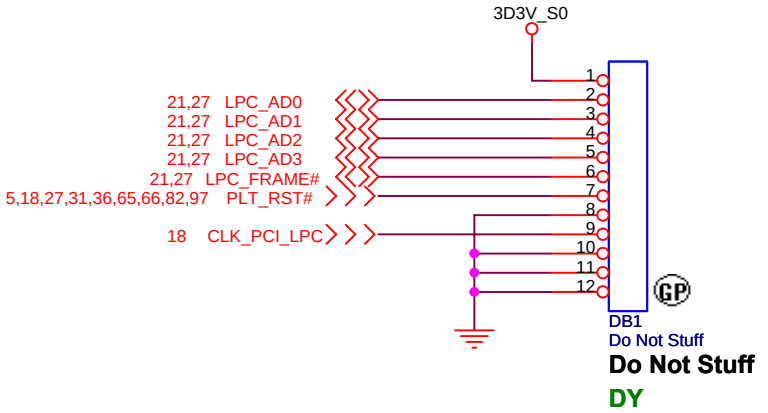

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SD/XD/MS Card Reader

32 SD-DATA3_19
32 SD_CMD_16
32 SD-CLK_9
32 SD_DATA0_4
32 SD-DAT1_3
32 SD-DATA1_21
32 SD-WP_2
31,32 SD_CD/XD_WE#

32 MS_BS_7
32 MS-DATA1_8
32 MS_DATA0_10
32 MS-DATA2_12
32 MS_INS#_14
32 MS-DATA3_15
32 MS-SCLK_17

32 XD_CD#_39
32 XD-R/-B_38
32 XD_RE#_37
32 XD_CE#_36
32 XD_CLE_35
32 XD_ALE_34
32 SD_CD/XD_WE#_1_33_43
32 XD_WP_32

32 XD_D0_30
32 XD_D1_29
32 XD_D2_28
32 XD_D3_27
32 XD_D4_26
32 XD_D5_25
32 XD_D6_24
32 XD_D7_23

CARD1

SD-DATA3_19 → 19 SD-DAT3/MMC-RSV
SD_CMD_16 → 16 SD-CMD/MMC-CMD
13 SD-VSS/MMC-VSS1
3D3V_CARD_S0 → 11 SD-VDD/MMC-VDD
SD-CLK_9 → 9 SD-CLK/MMC-CLK
6 SD-VSS/MMC-VSS2
SD_DATA0_4 → 4 SD-DAT0/MMC-DAT
SD-DAT1_3 → 3 SD-DAT1
SD-DATA1_21 → 21 SD-DAT2
SD-WP_2 → 2 SD-WP
SD_CD/XD_WE#_1_33_43 → 1 SD-CD#1
SD_CD/XD_WE#_1_33_43 → 43 SD-CD#43

5 MS-VSS/GND
MS_BS_7 → 7 MS-BS
MS-DATA1_8 → 8 MS-DATA1
MS_DATA0_10 → 10 MS-SDIO/DATA0
MS-DATA2_12 → 12 MS-DATA2
MS_INS#_14 → 14 MS-INS
MS-DATA3_15 → 15 MS-DATA3
MS-SCLK_17 → 17 MS-SCLK
3D3V_CARD_S0 → 18 MS-VCC
20 MS-VSS/GND

NP1 → NP1

XD-GND 40
XD-CD 39 → XD_CD#_39
XD-R/-B 38 → XD-R/-B_38
XD-RE 37 → XD_RE#_37
XD-CE 36 → XD_CE#_36
XD-CLE 35 → XD_CLE_35
XD-ALE 34 → XD_ALE_34
XD-WE 33 → SD_CD/XD_WE#_1_33_43
XD-WP 32 → XD_WP_32
XD-GND 31
XD-D0 30 → XD_D0_30
XD-D1 29 → XD_D1_29
XD-D2 28 → XD_D2_28
XD-D3 27 → XD_D3_27
XD-D4 26 → XD_D4_26
XD-D5 25 → XD_D5_25
XD-D6 24 → XD_D6_24
XD-D7 23 → XD_D7_23
XD-VCC 22 → 3D3V_CARD_S0

SD-VSS/MMC-VSS2/GND 44
GND 42
GND 41

NP2 → NP2

CARDBUS40P-SKT-2-GP

20.I0087.I21
2nd = 62.10024.B41

SD-WP_2 → EC7407 DY Do Not Stuff
XD_ALE_34 → EC7403 DY Do Not Stuff
XD-R/-B_38 → EC7401 DY Do Not Stuff
MS_BS_7 → EC7404 DY Do Not Stuff
SD_CD/XD_WE# → EC7405 DY Do Not Stuff
MS_INS#_14 → EC7406 DY Do Not Stuff
XD_RE#_37 → EC7402 DY Do Not Stuff

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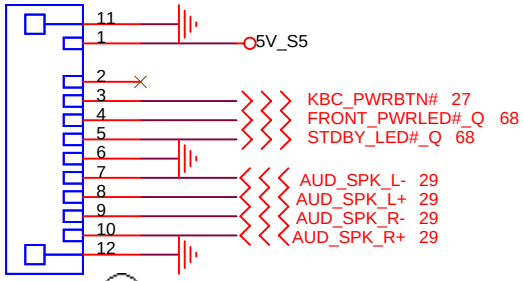
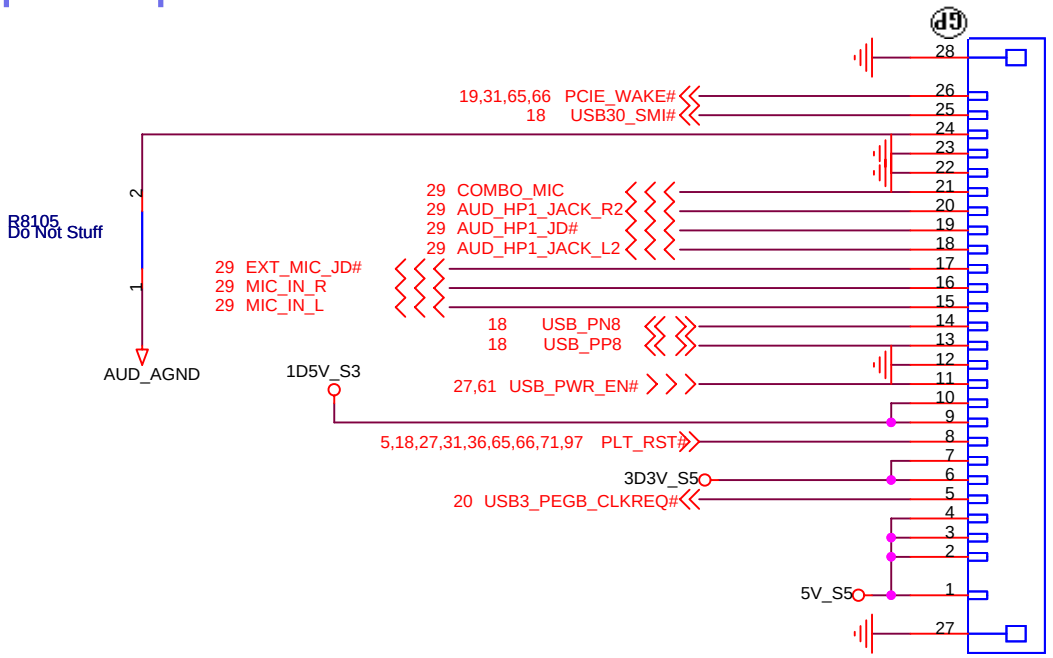
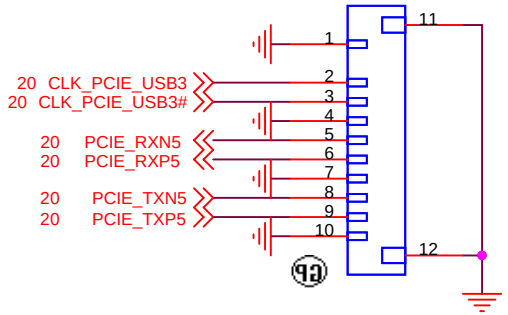


PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010



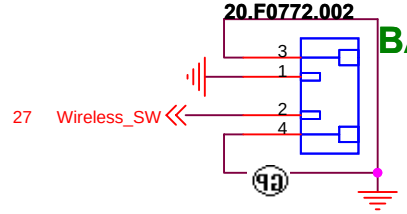
USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



RF_CN1
ACES-CON2-11-GP
20.F0772.002

BAE40



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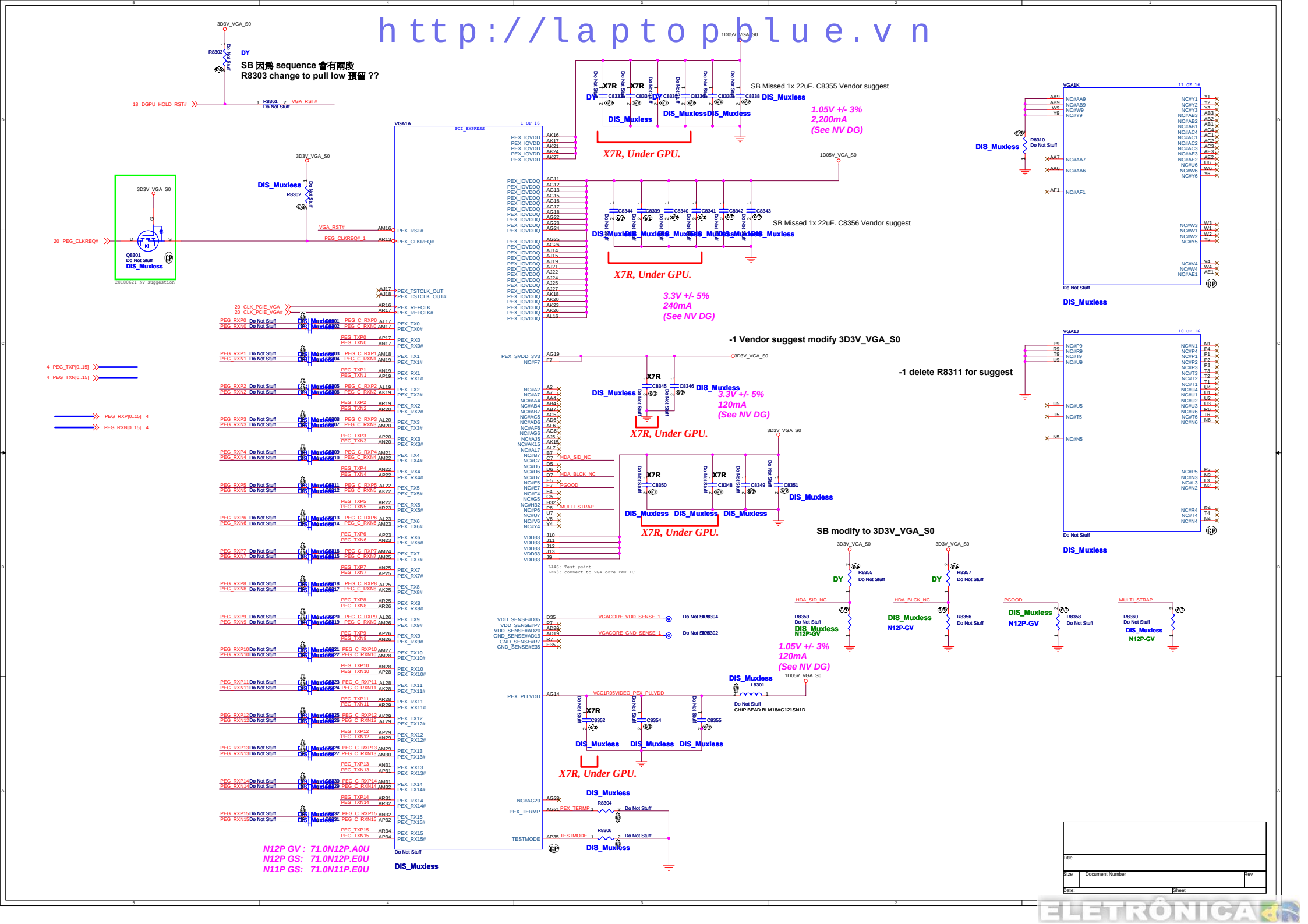

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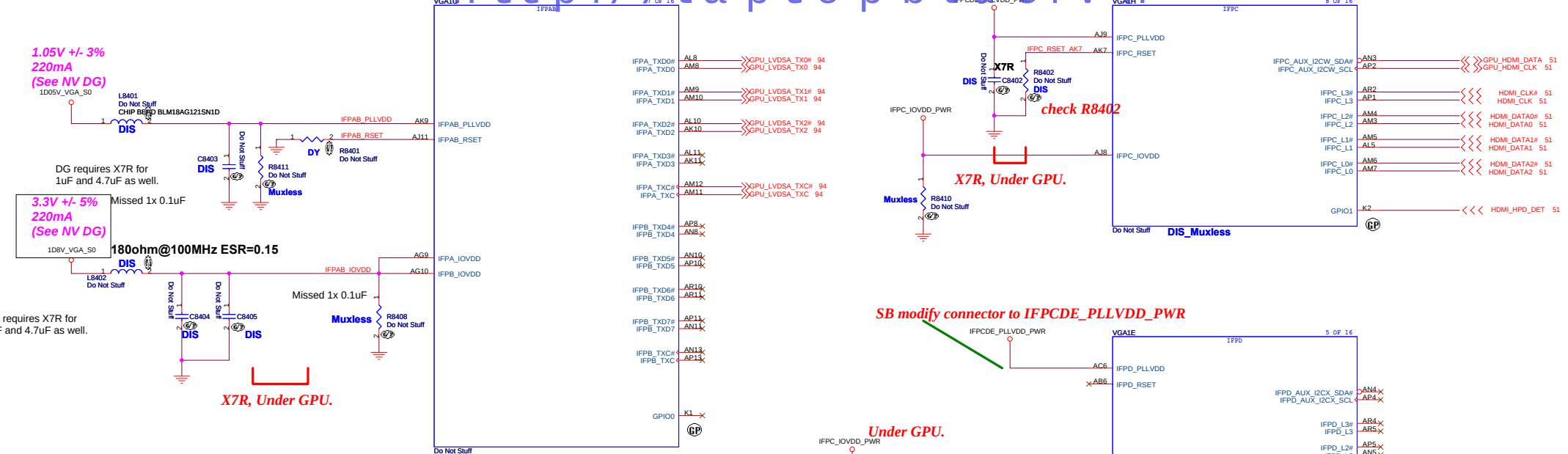
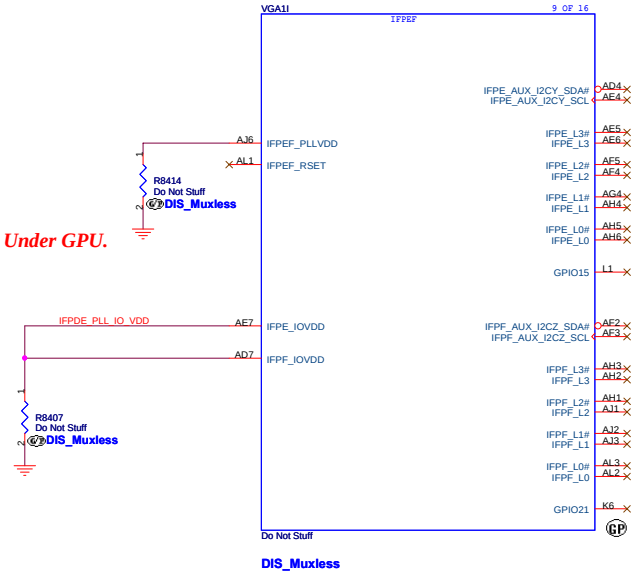
LVDS Interface

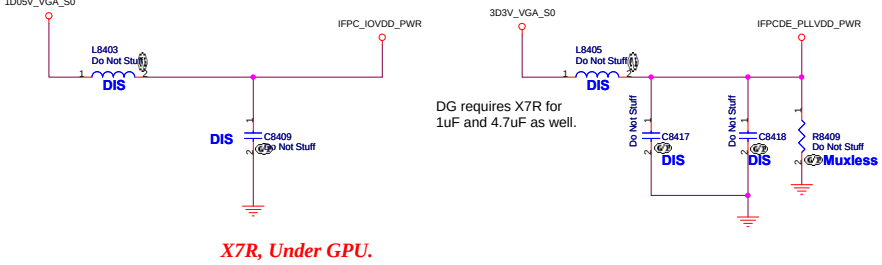


SB modify connector to IFPCDE_PLLVDD_PWR

SA R8412, R8413 change DY
SB R8412, R8413 change delete



HDMI Interface



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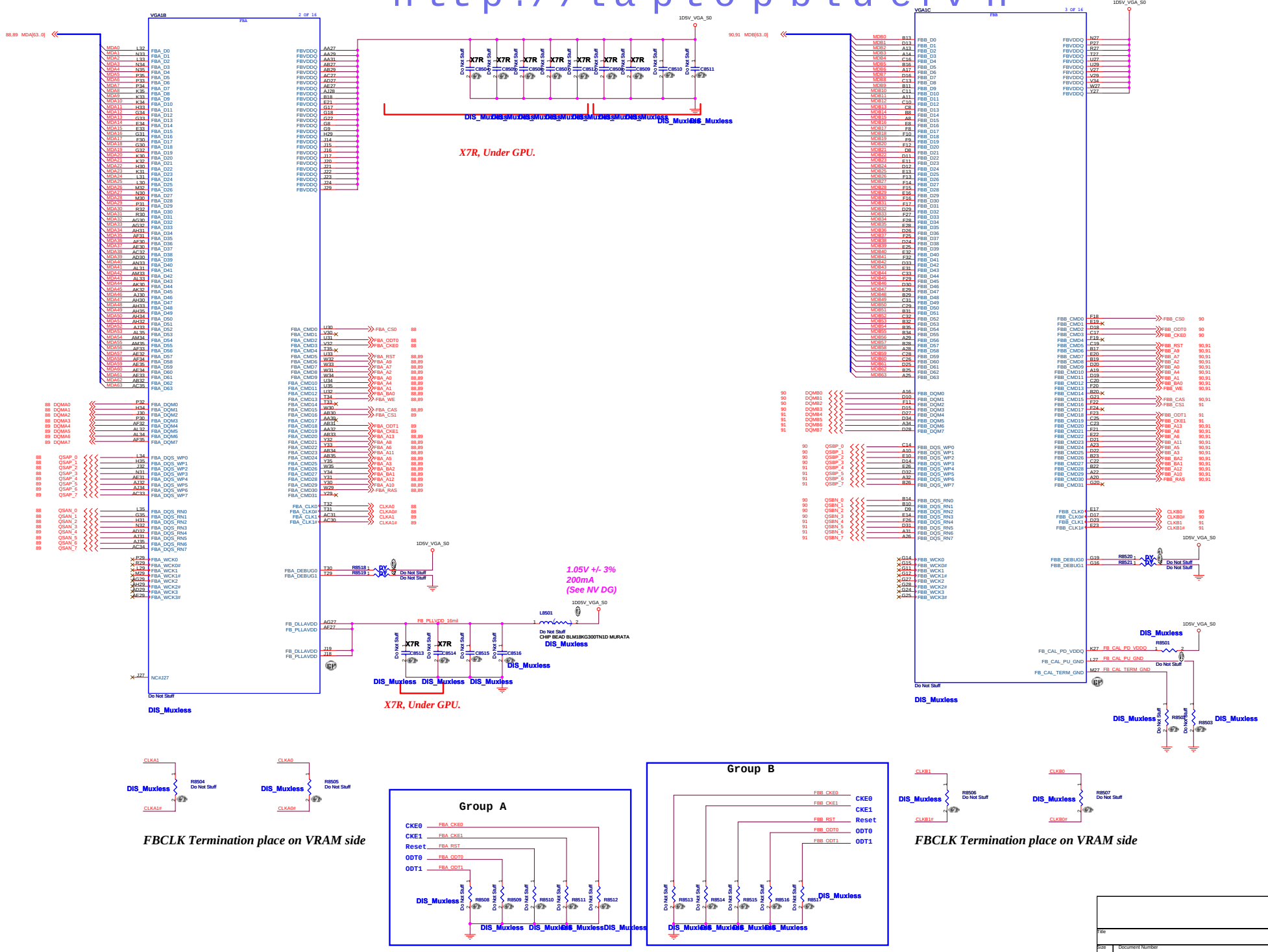

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3.3V +/- 5%
120mA
(See NV DG)

X7R, Under GPU.

delete 10K DY to GND

Missed 3x 0.1uF

SB DIS_Muxless 都要上件或DY??

SB HOSONIC modify to 12P, R8607 modify to 390R

VGA Thermal sensor P2800

Modify SMBUS

SB R8619 15" DY

SB 修改上件,才能跑全速

Pull high 在Page 94

预留0.9V

SB change 3D3V_VGA_S0, R8638 change DY

SJM50-CP SUPPORT							
P-STATE	NVVDD_ALT1	NVVDD_ALT0	N11M-GE1	N11M-GE2	N11M-OP1	N11P-GE1	N12P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.80V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.03V	1.03V	1.03V	0.95V	0.95V

NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU_ROM_SI
GPU_ROM_SO
GPU_ROM_SCLK

```
for 1Gbit   for 2Gbit   for 1Gbit   for 2Gbit
Hynix VRAM  Hynix VRAM  Samsung VRAM Samsung VRAM
RAM_CFG[0]=0 RAM_CFG[0]=0 RAM_CFG[0]=1 RAM_CFG[0]=1
RAM_CFG[1]=1 RAM_CFG[1]=1 RAM_CFG[1]=1 RAM_CFG[1]=1
RAM_CFG[2]=0 RAM_CFG[2]=1 RAM_CFG[2]=0 RAM_CFG[2]=1
RAM_CFG[3]=0 RAM_CFG[3]=0 RAM_CFG[3]=0 RAM_CFG[3]=0

VGA_DEVICE   =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417     =0 (High bit)

PEX_PLL_EN_TERM =0
SLOT_CLK_CFG    =1
SUB_VENDOR      =0
PCI_DEVID[4]    =1
```

N11P Fermi QS 1

```
Logical Strap Bit Mapping
Resistor  Pull-up Pull-down
5Kohms    1000    0000
10Kohms   1001    0001
15Kohms   1010    0010
20Kohms   1011    0011
25Kohms   1100    0100
30Kohms   1101    0101
35Kohms   1110    0110
45Kohms   1111    0111
```

Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

TABLE NVIDIA

-1 modify N12P GV setting

71.0N12P.E0U　　71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS — N12P-GV — N11P-GE Pull Low — N11P-GS Pull Low — N12P-GE

USE 1111 (45K)

STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 — USE 0110 (35K)

STRAP2
PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

N12PGS_N12PGV:64.49915.6DL

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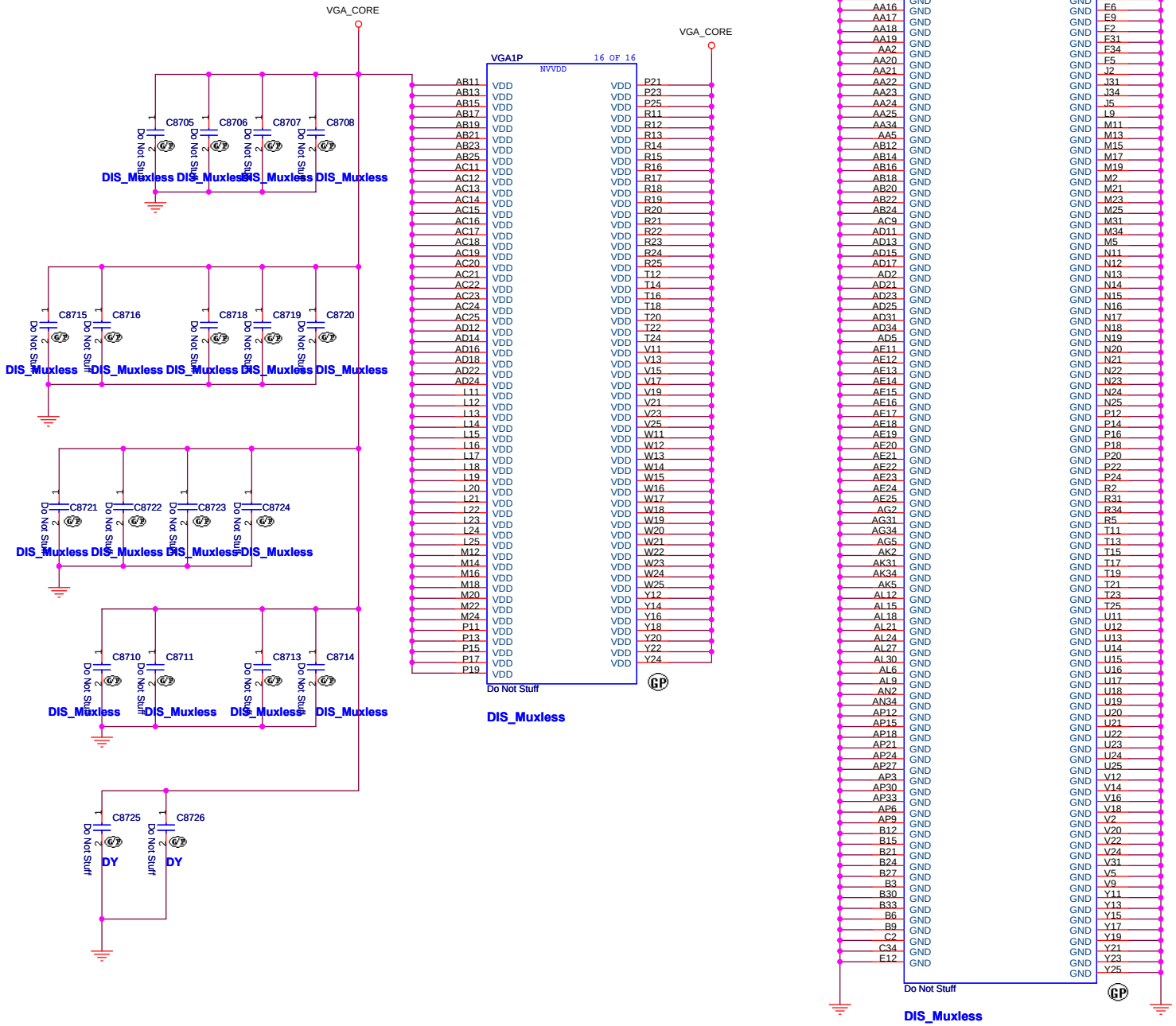

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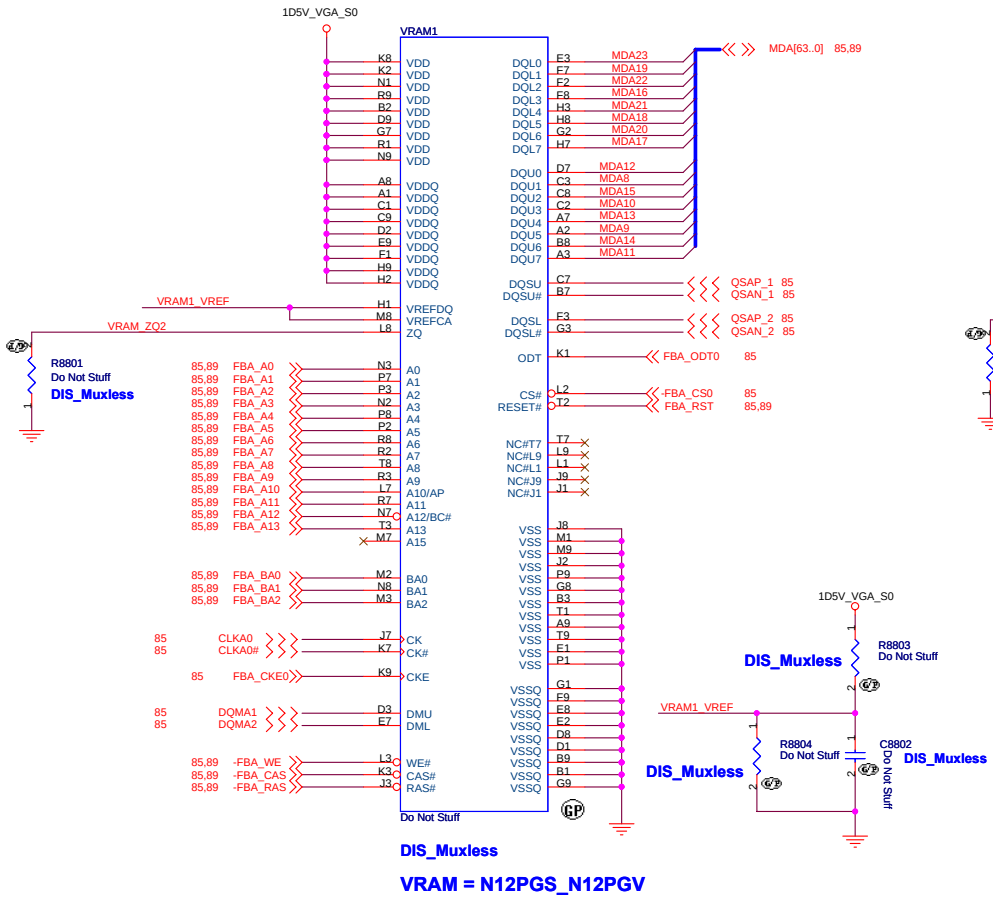
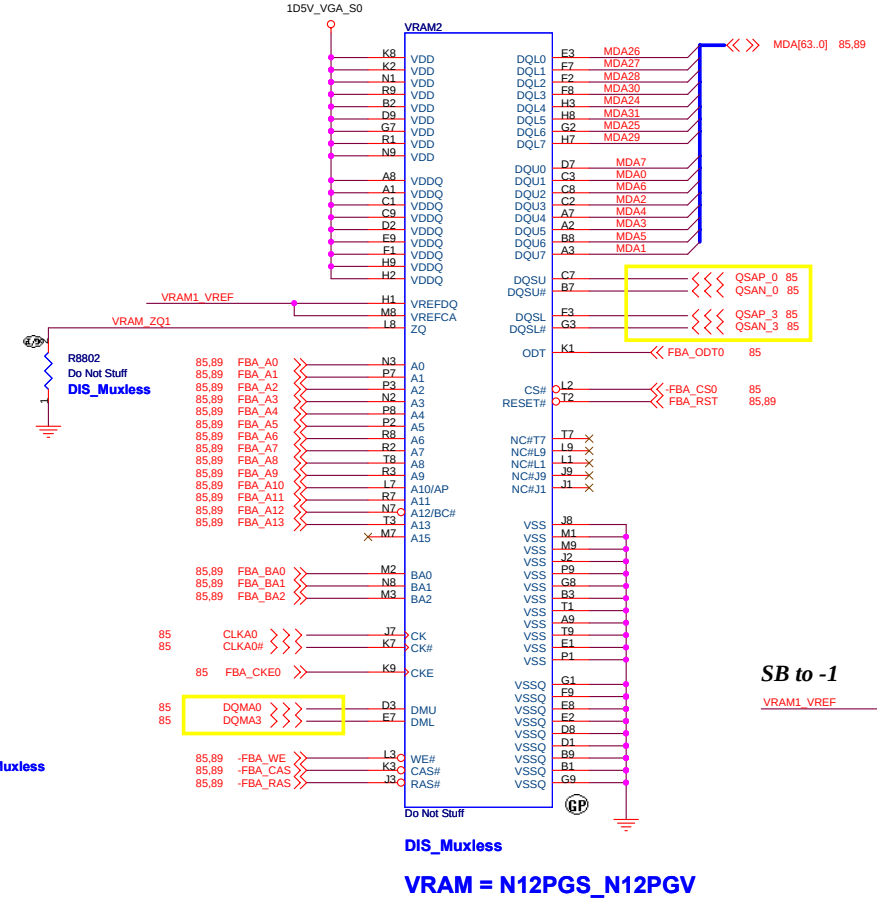
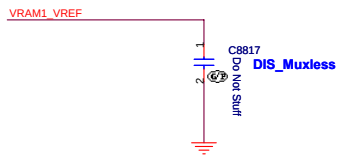
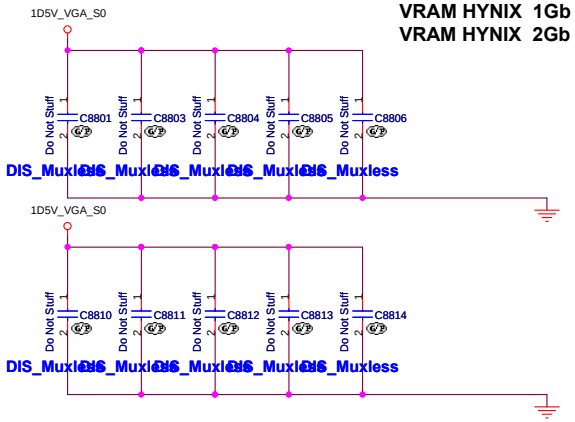


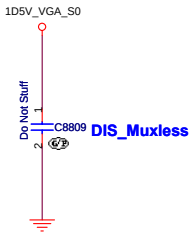


SB to -1



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001





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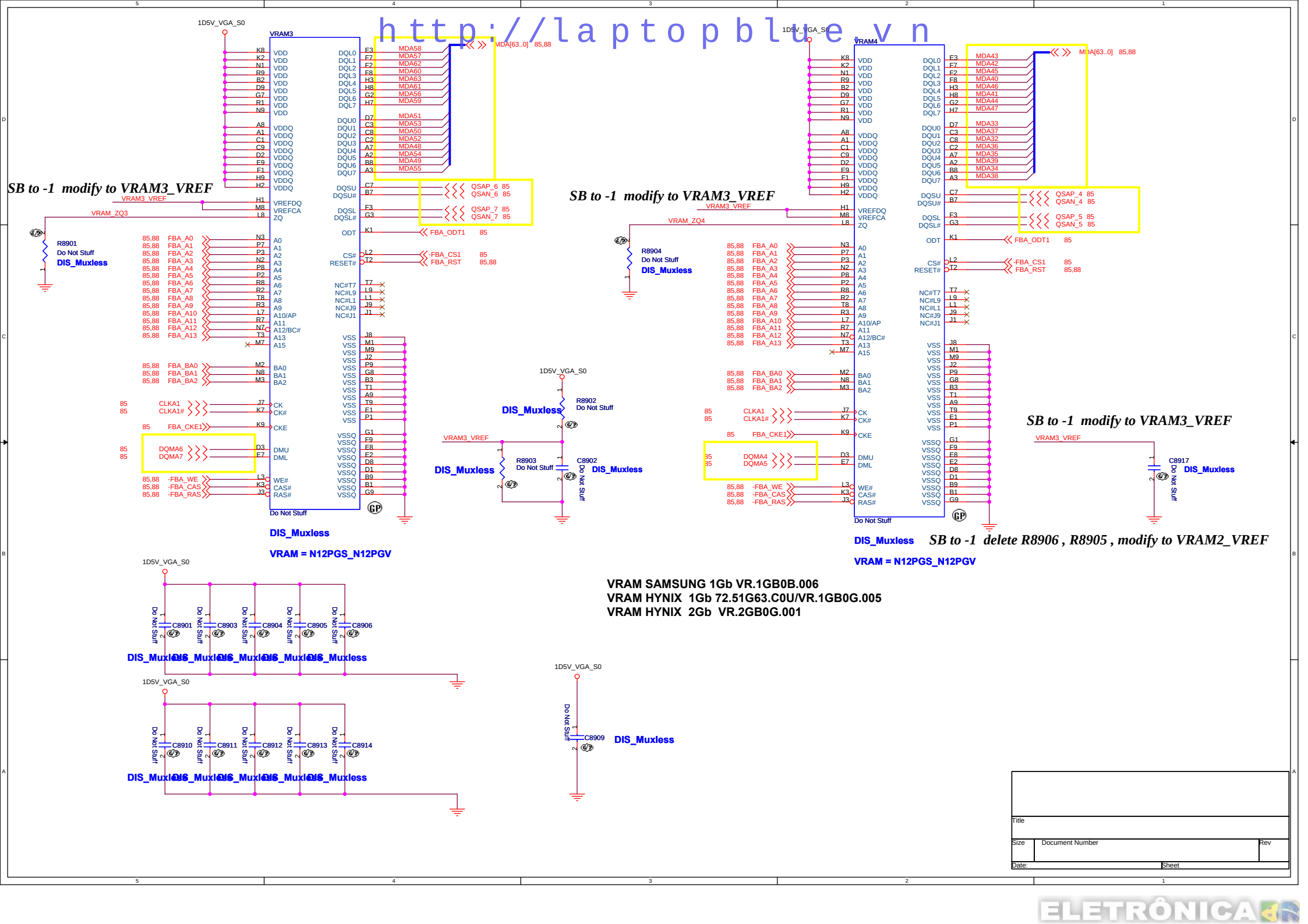

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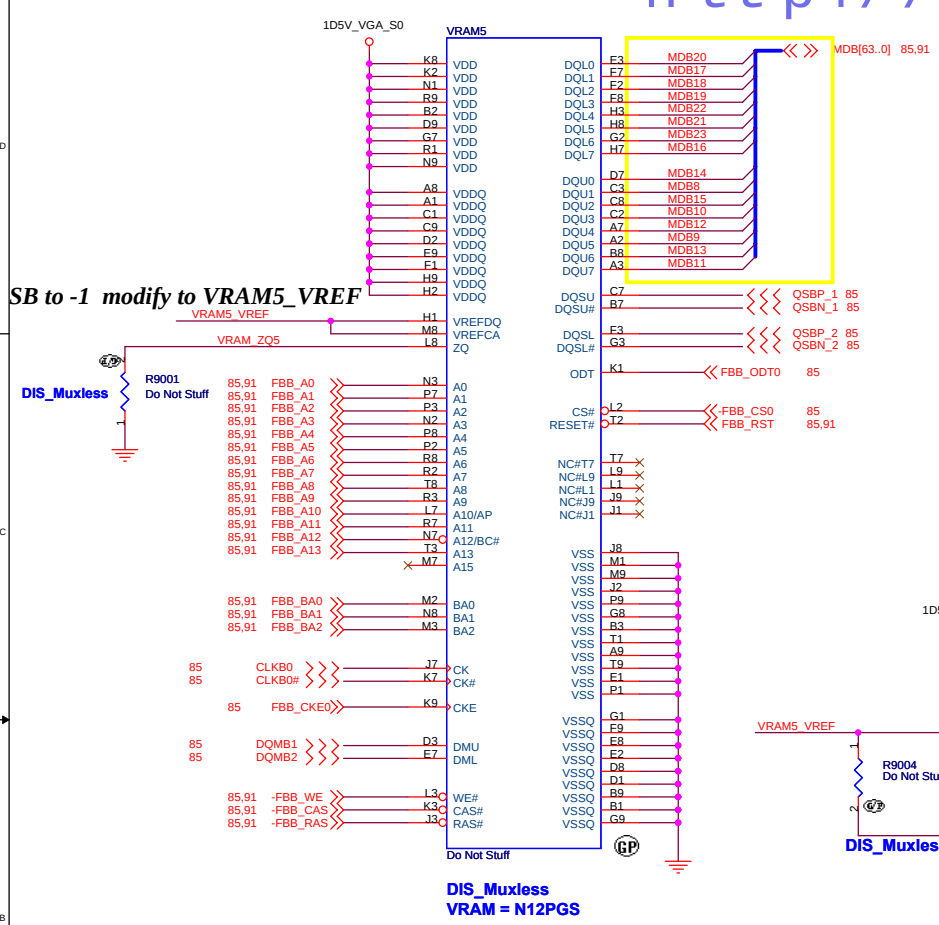
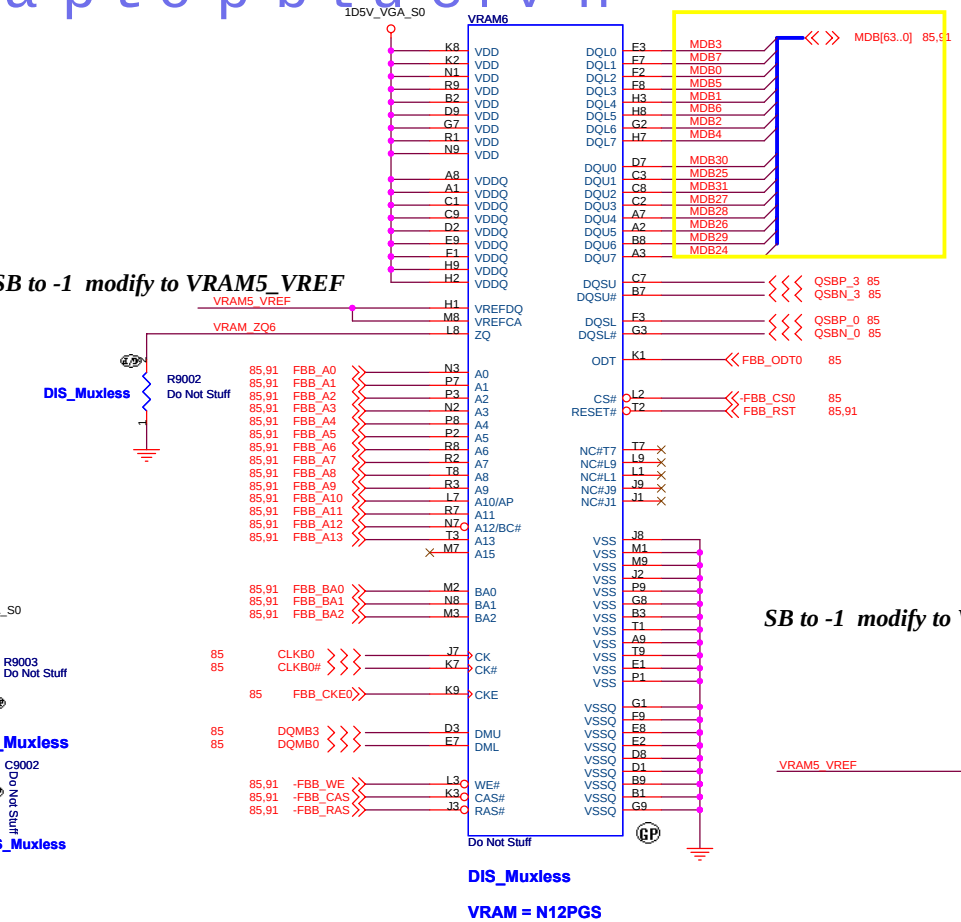
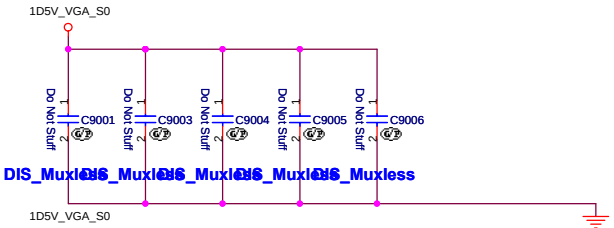
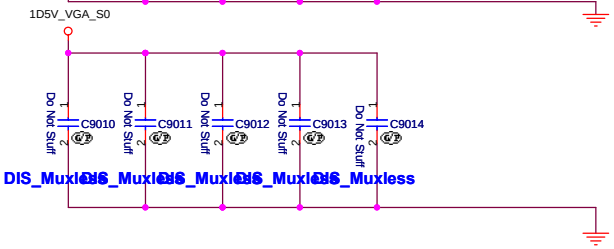
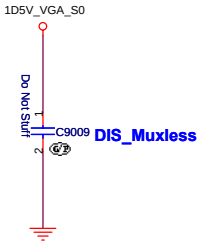




VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001







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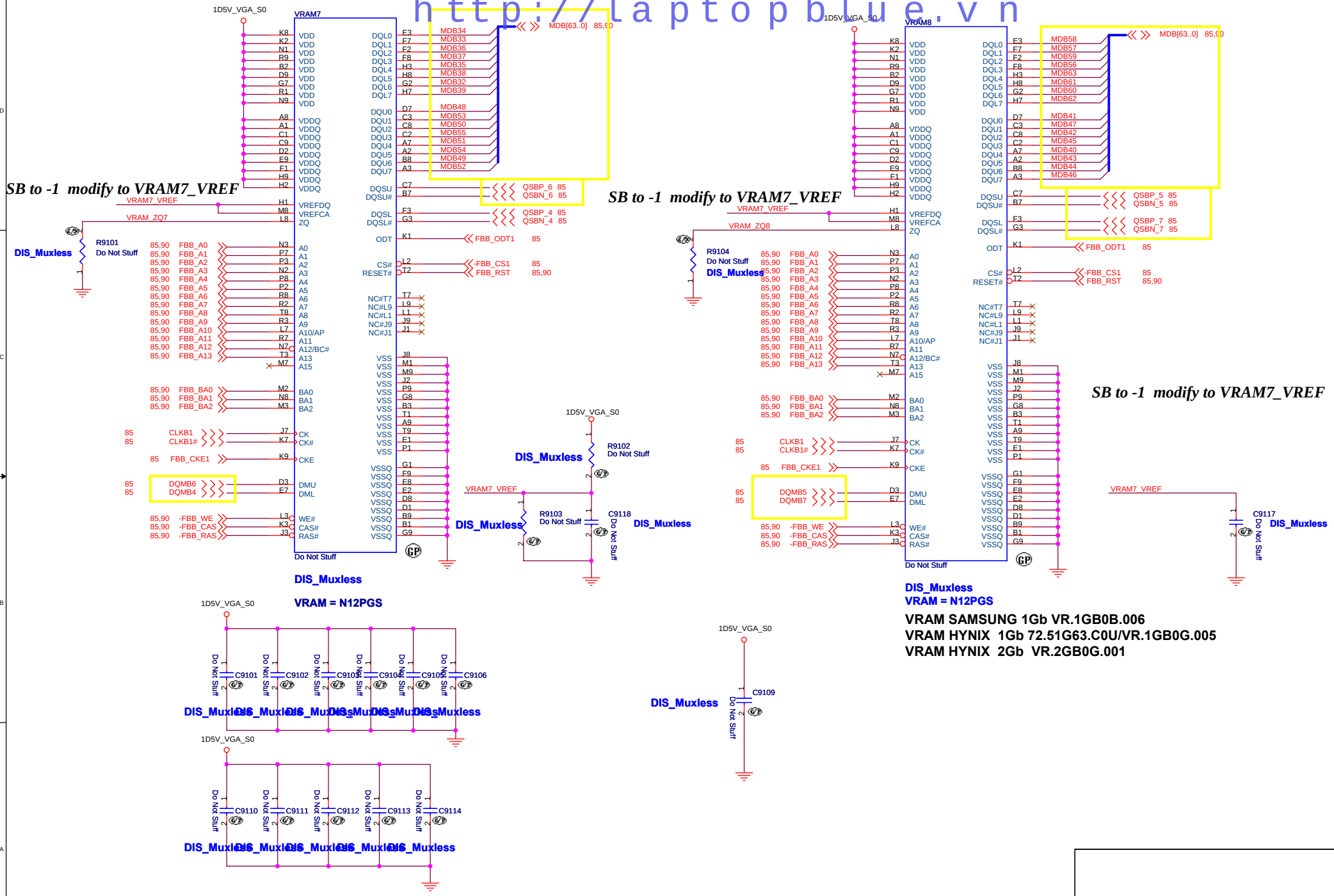

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SSID = PWR.Plane.Regulator_GFX

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20100715

20100719

SB 20100831

DCBATOUT

PWR_DCBATOUT_VGA_CORE

5V_S5

3D3V_VGA_S0

3D3V_AUX_S5

VGA_CORE

VGA_CORE_PWR

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

SB to -1 modify PR9213 VGA_Core to 1.05V

Vout=0.75V*(R1+R2)/R2

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

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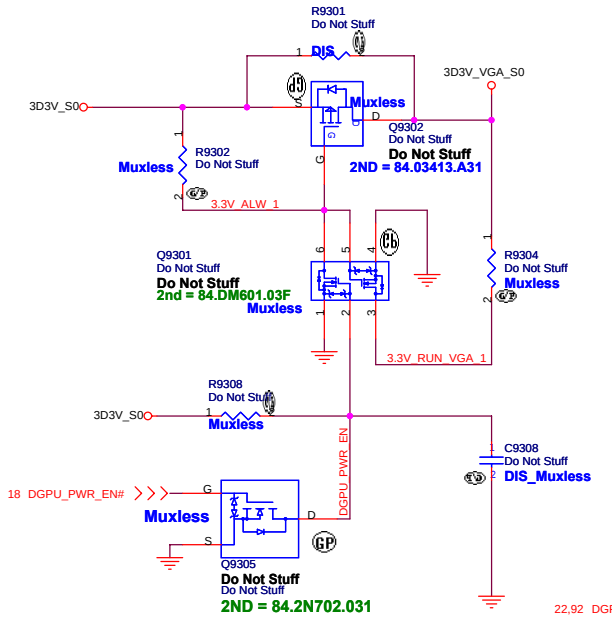
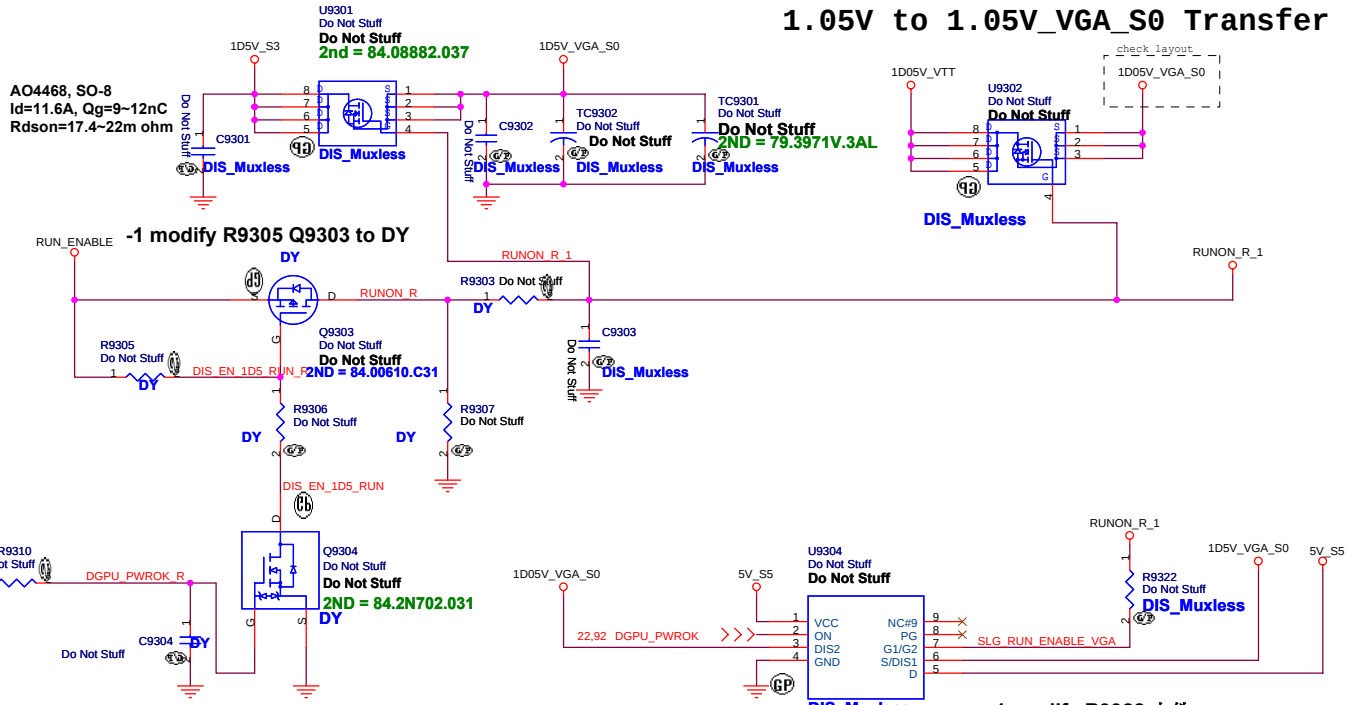
+3VS to 3.3V_DELAY Transfer



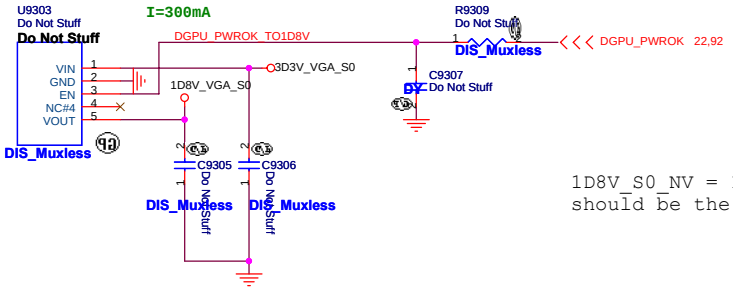
1D5V_VGA_S0

SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

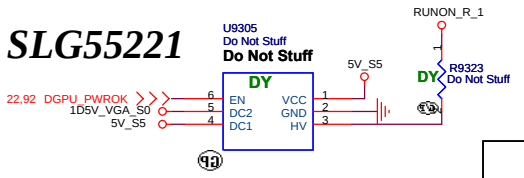


+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221



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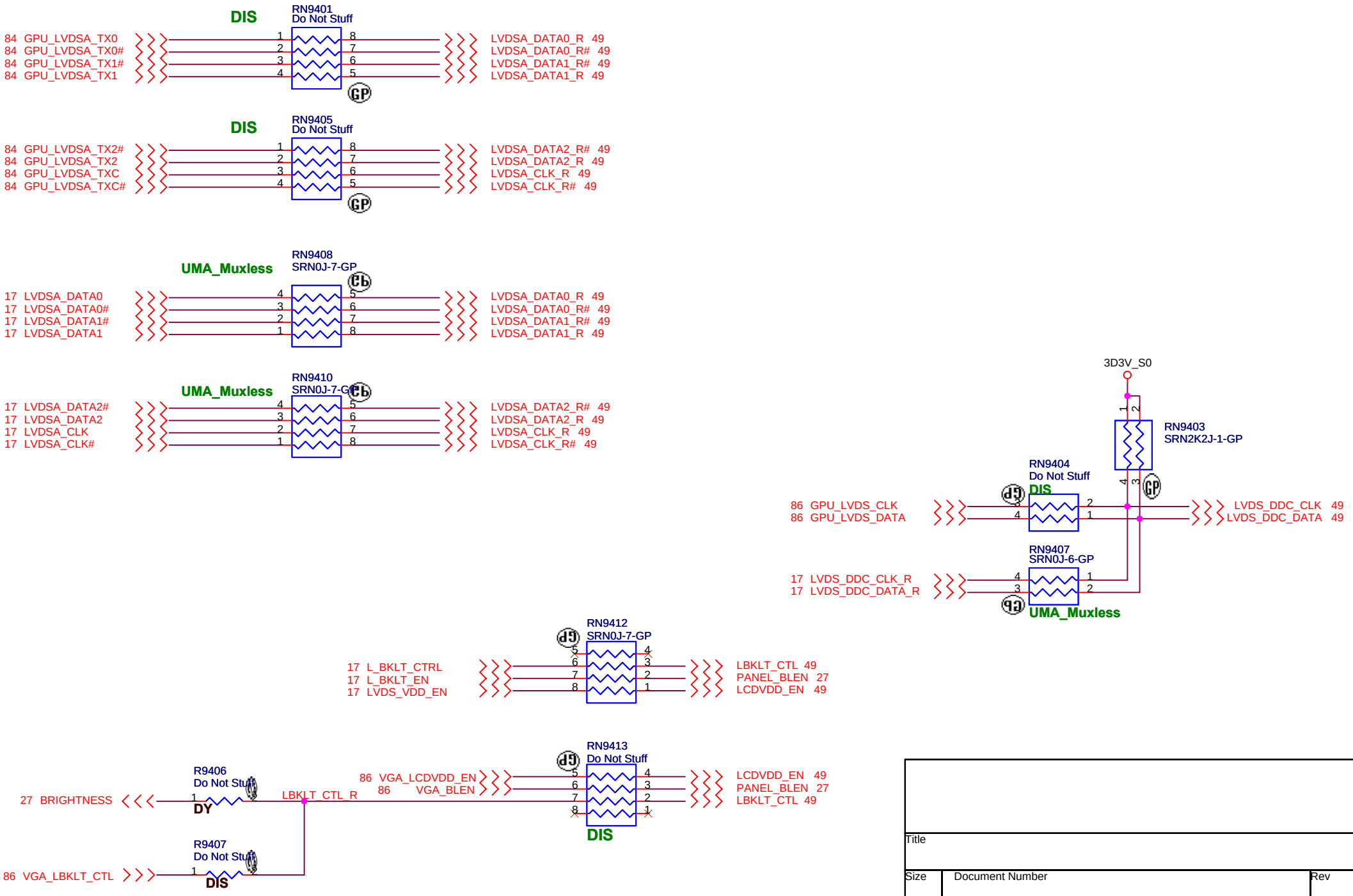

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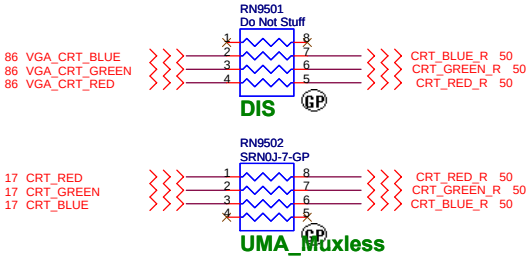

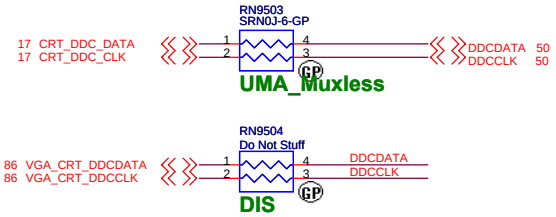

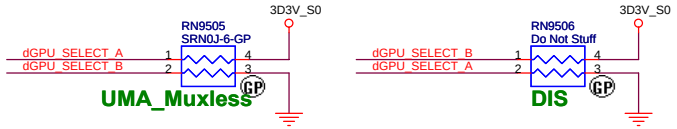

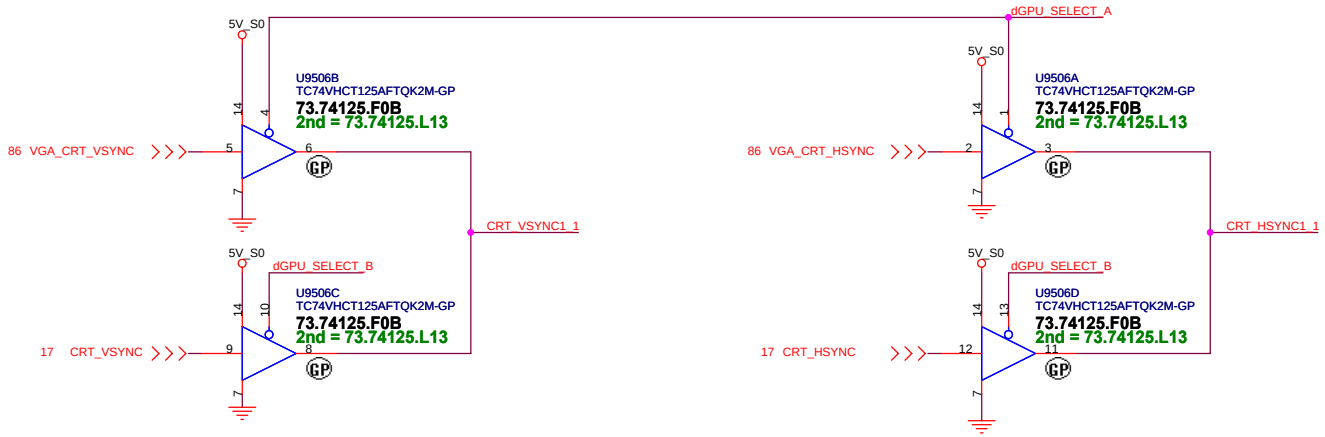

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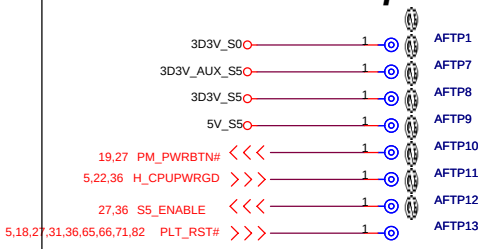
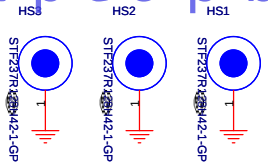
Check test point

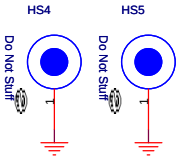


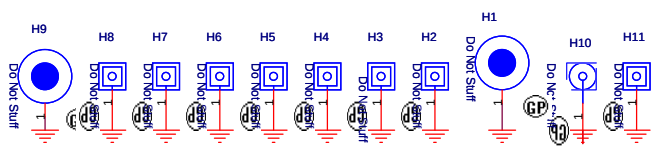
Test Point放在Dimm Door打開可量測處

CPU



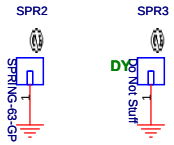
VGA



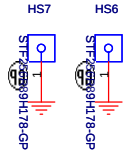


SB to -1 BOM add SPR2

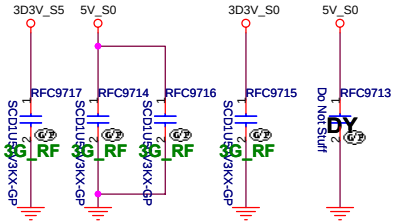
-2 delete SPR5

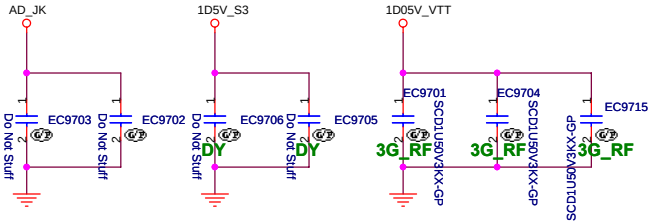


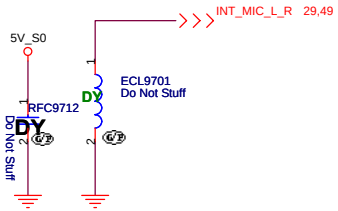
Change:34.40V16.001

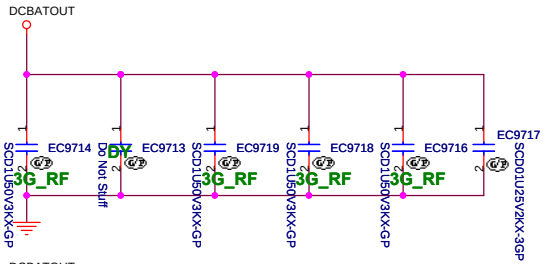


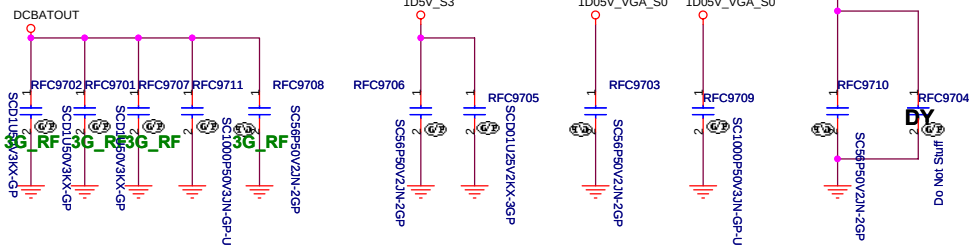
3G Sku

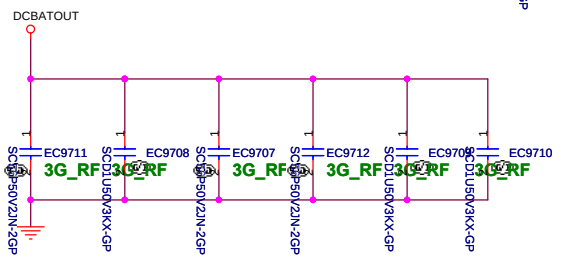












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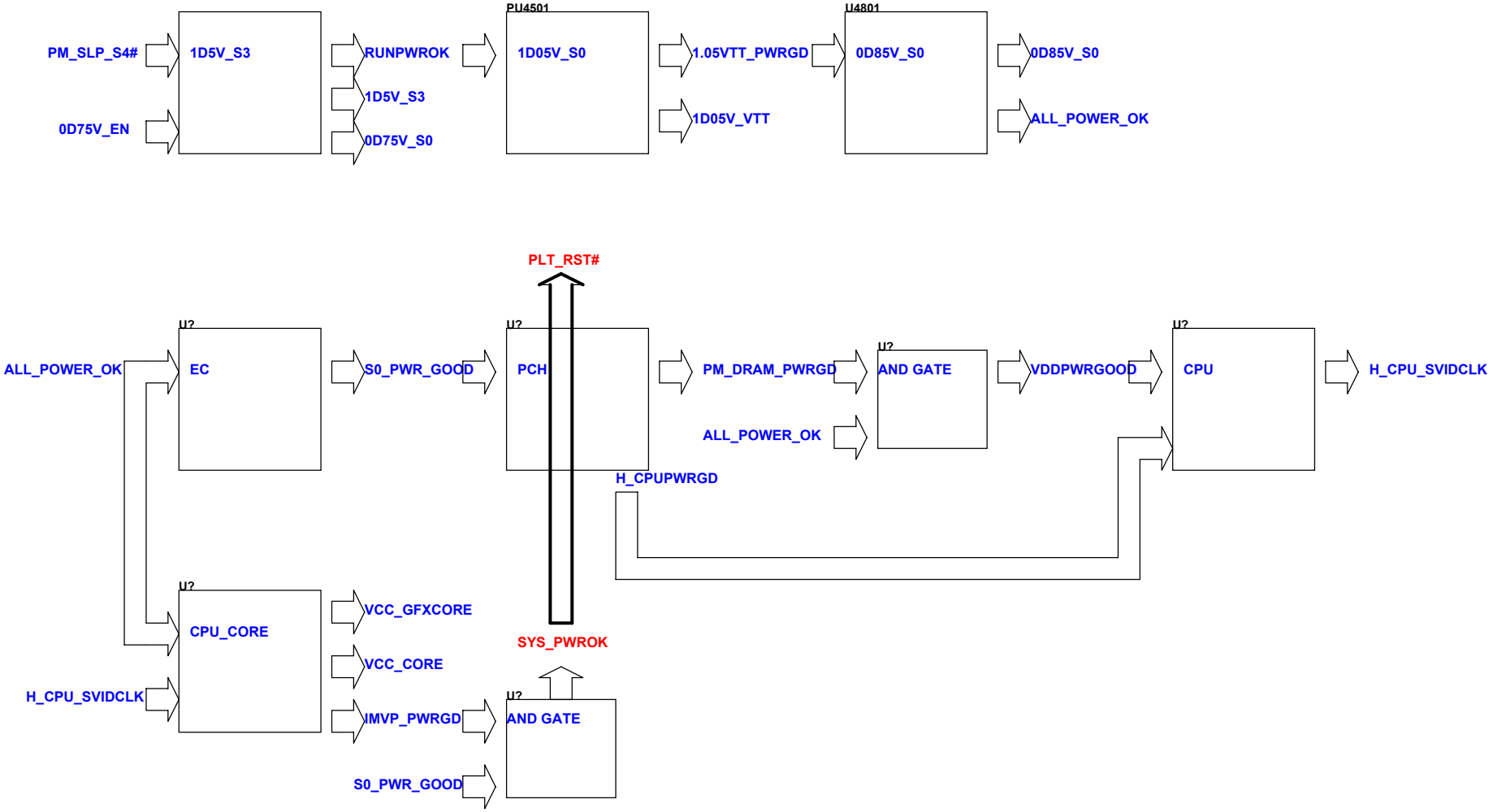

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Intel-Power Up Sequence

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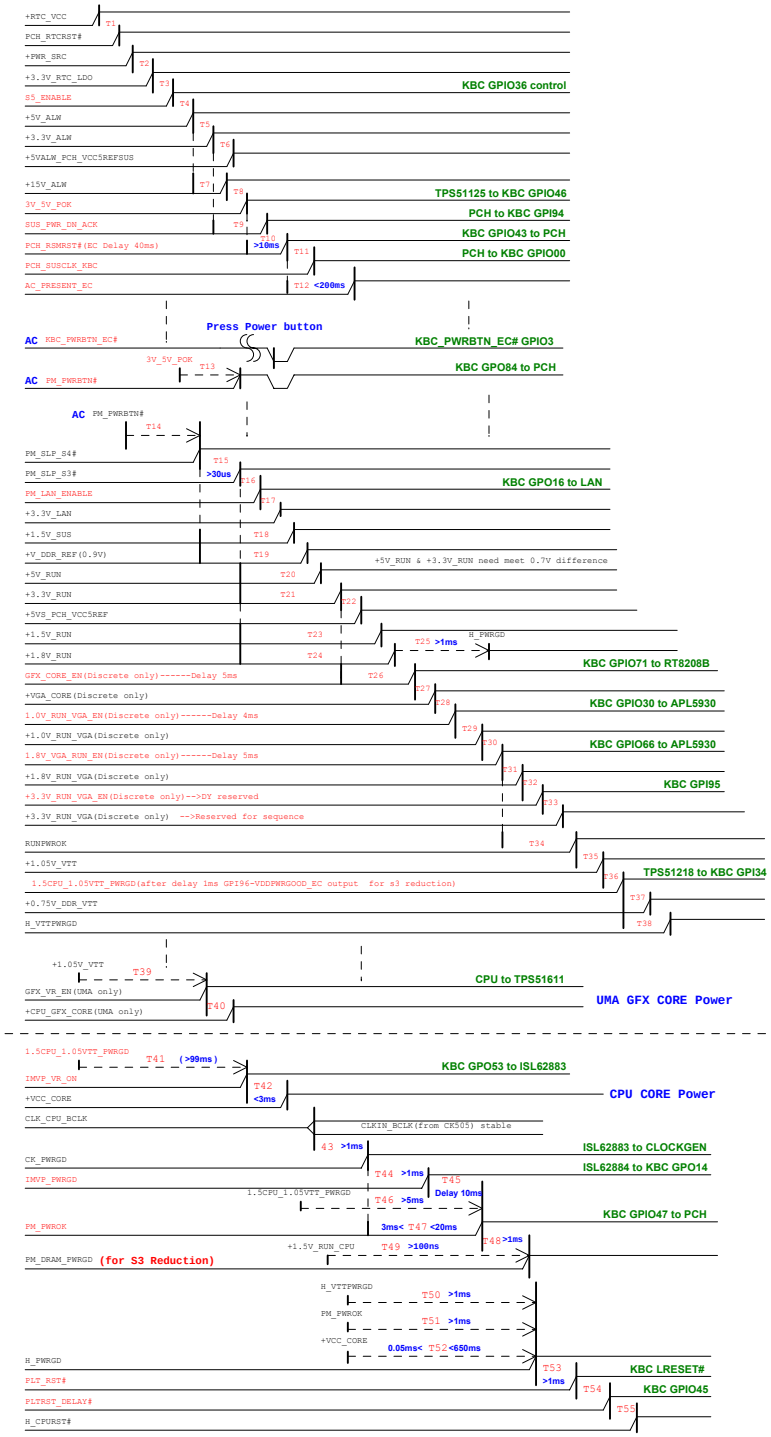
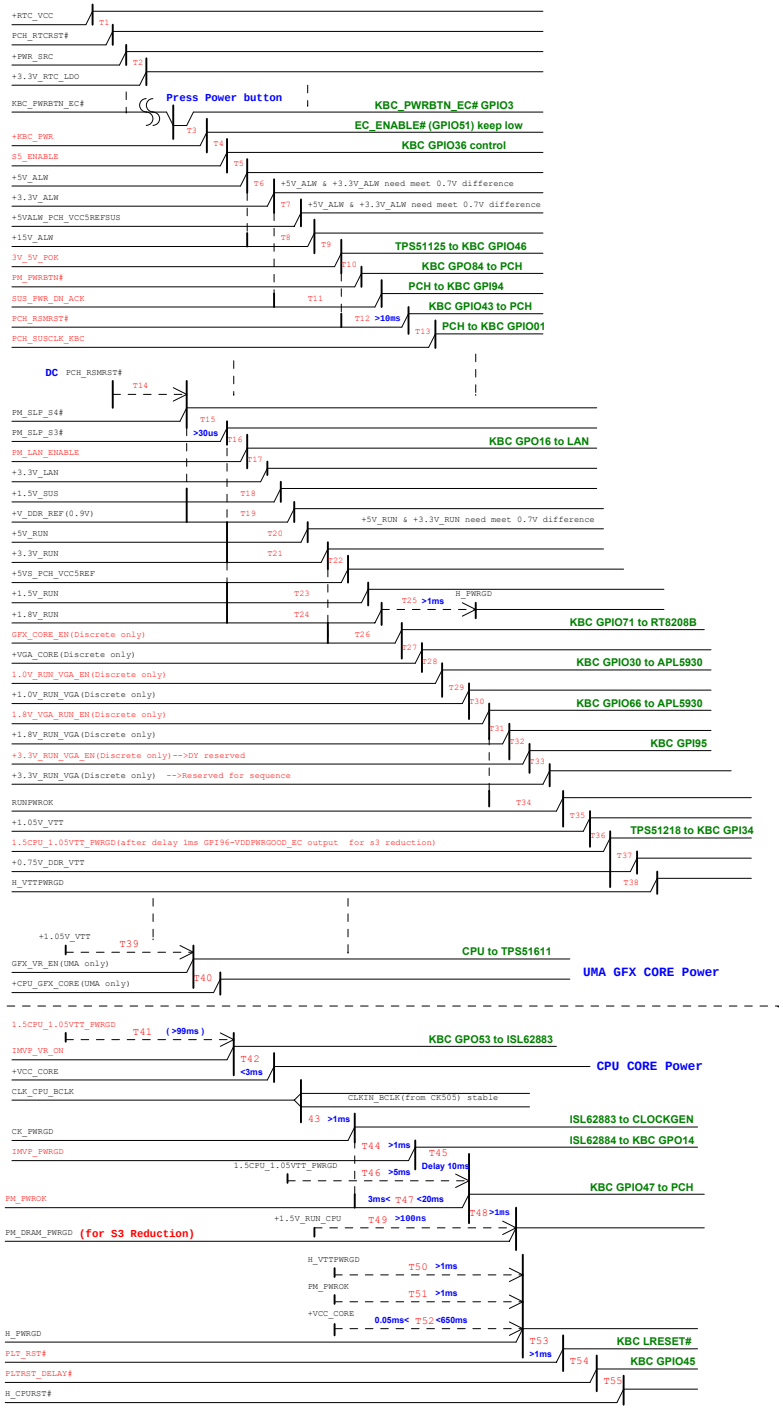
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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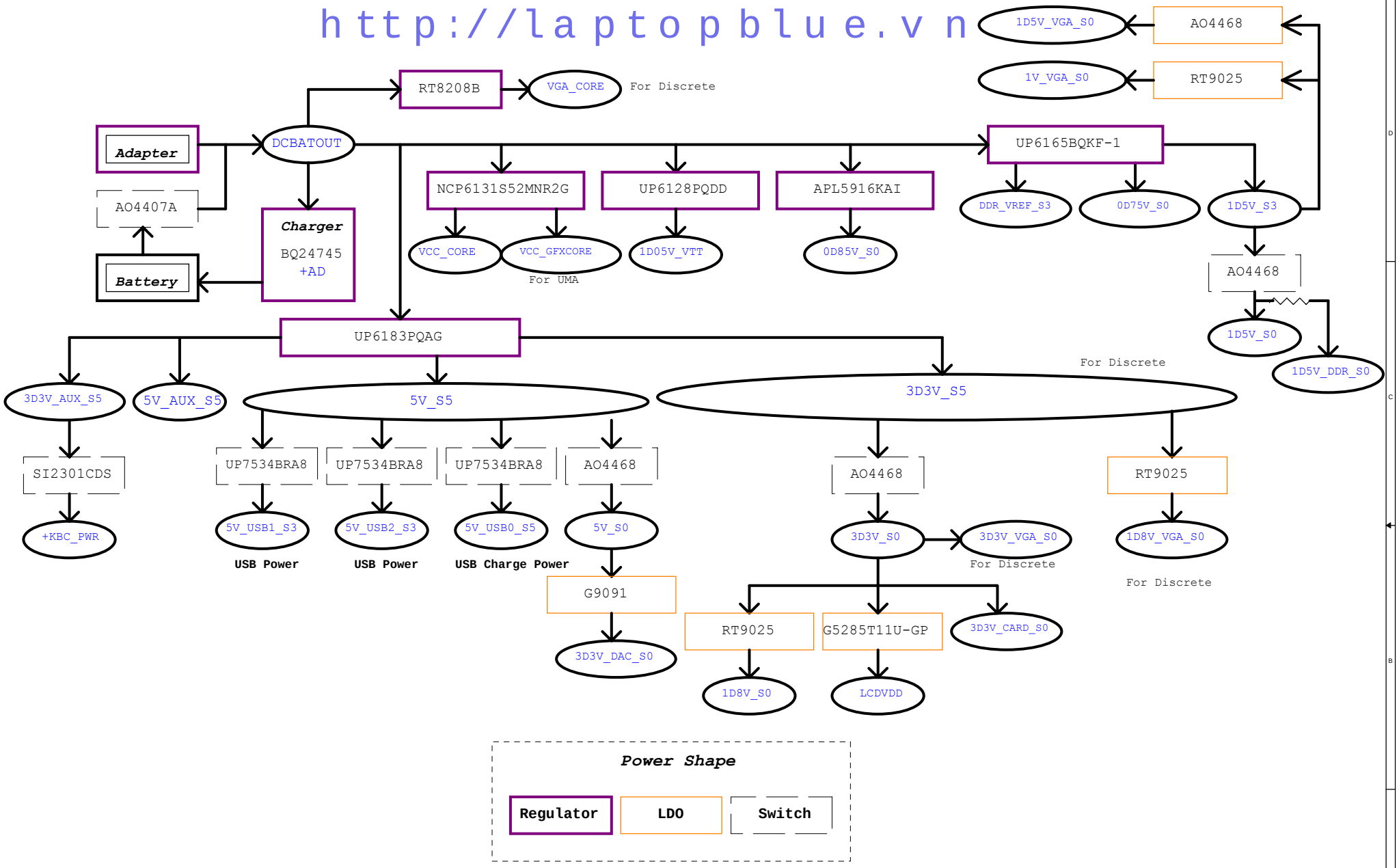

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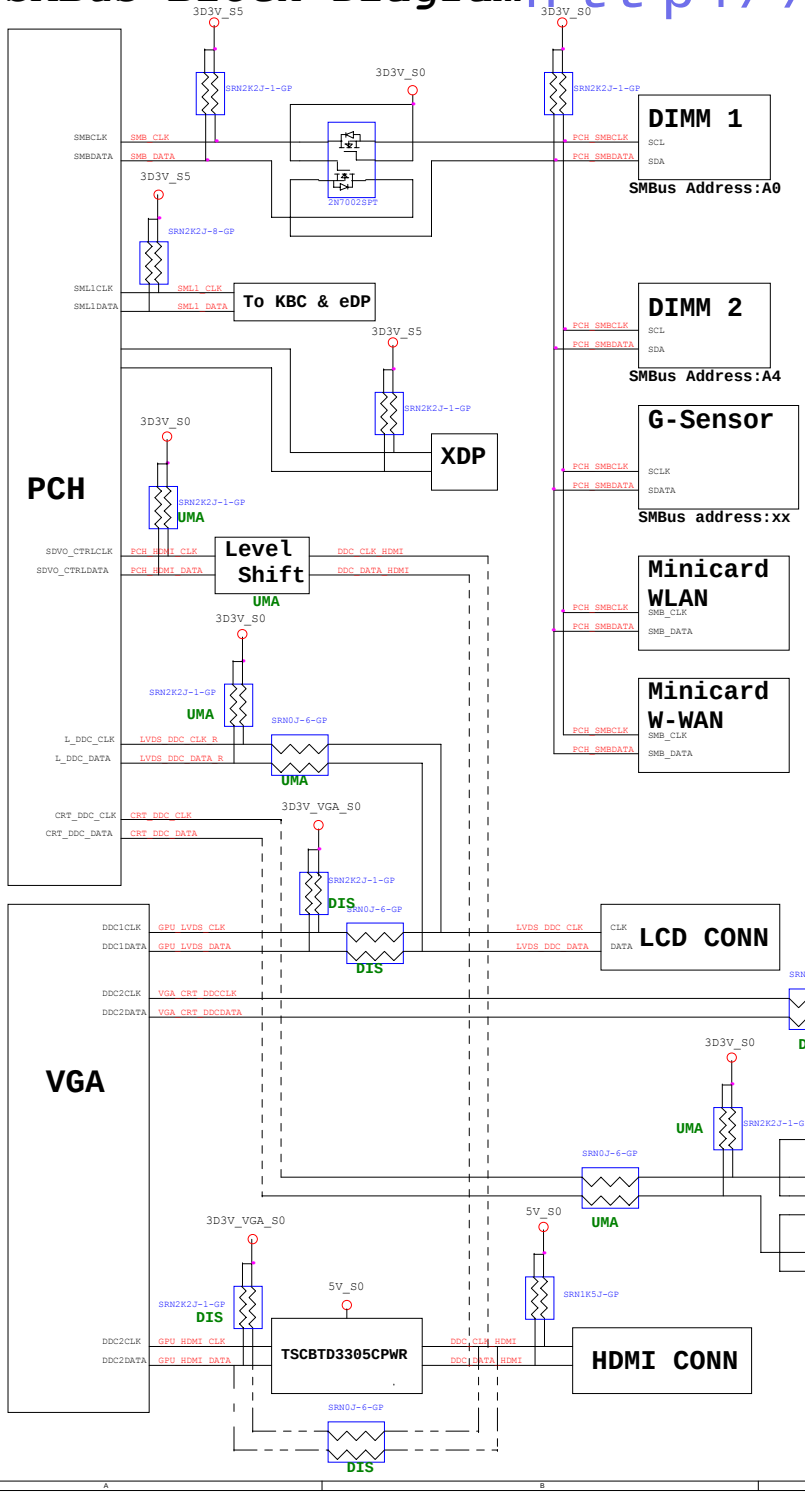
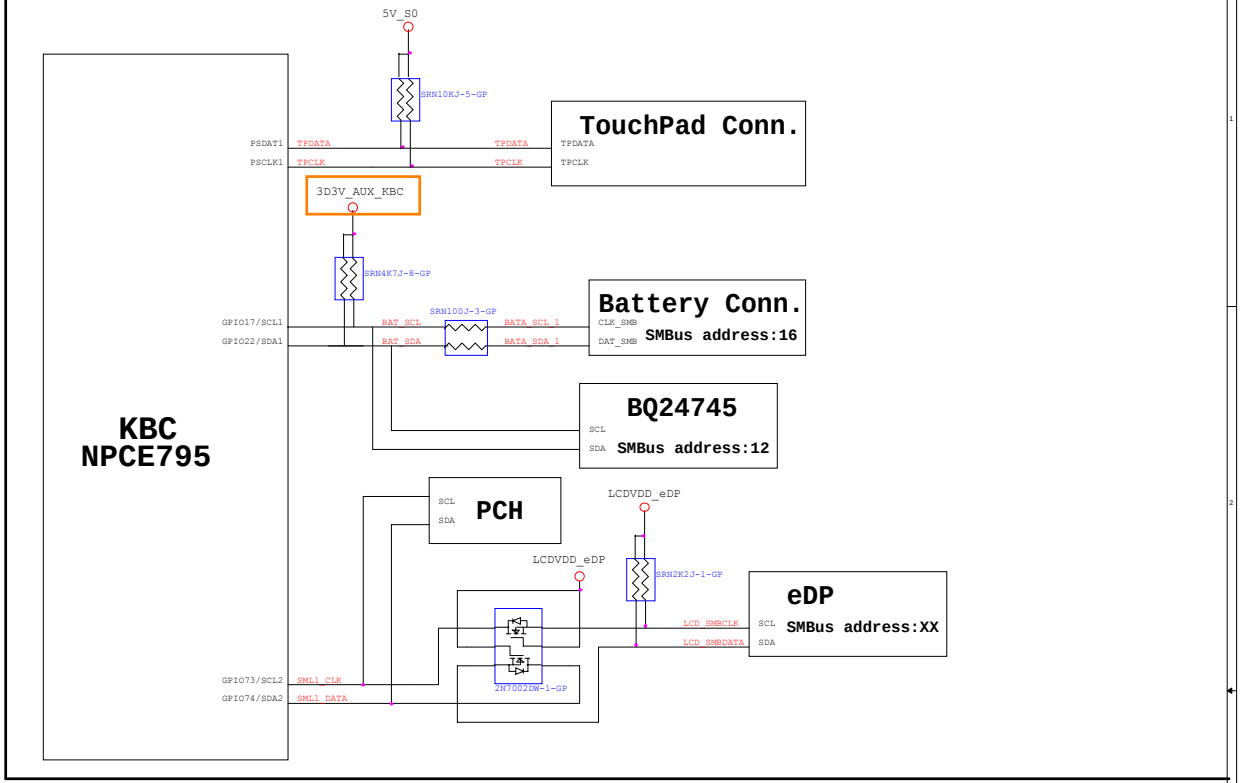
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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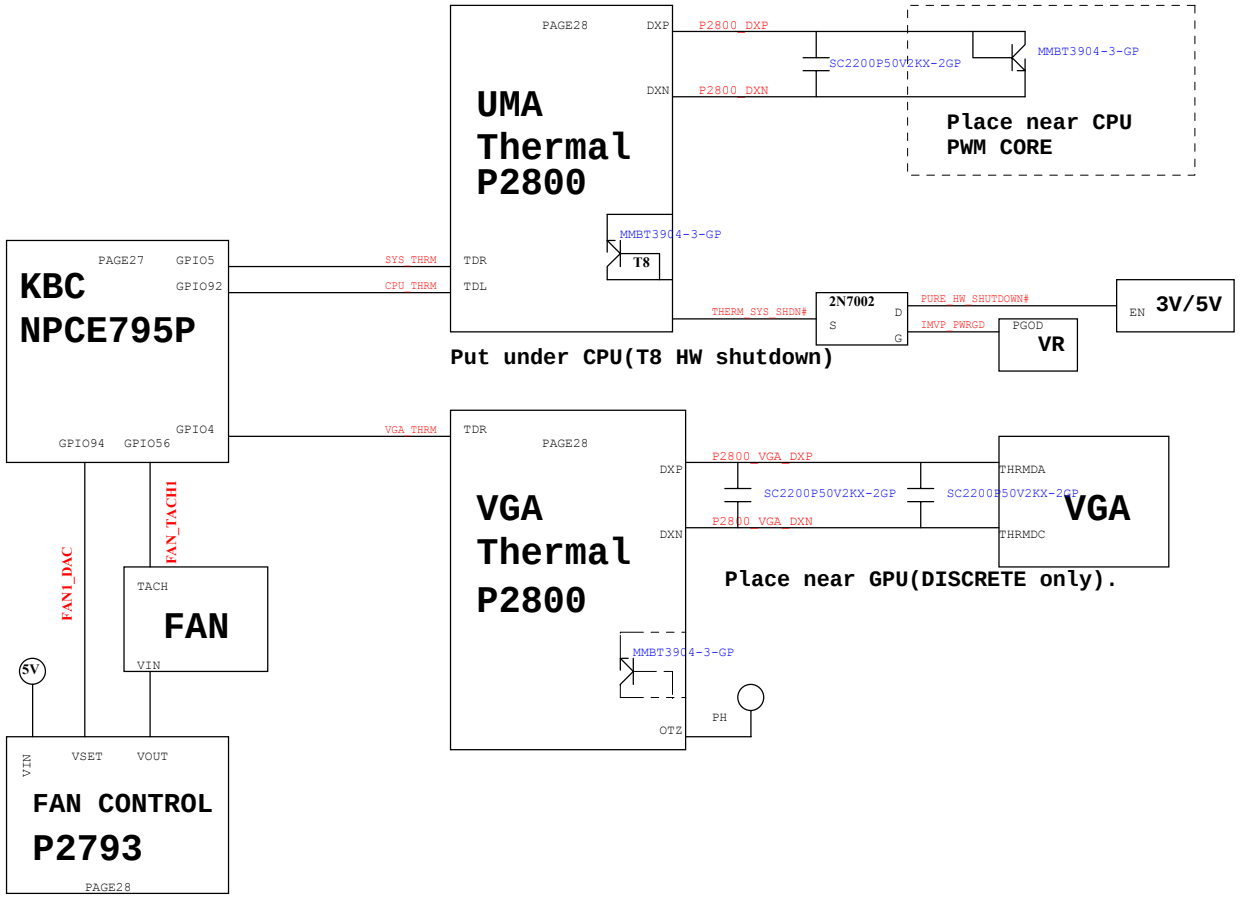
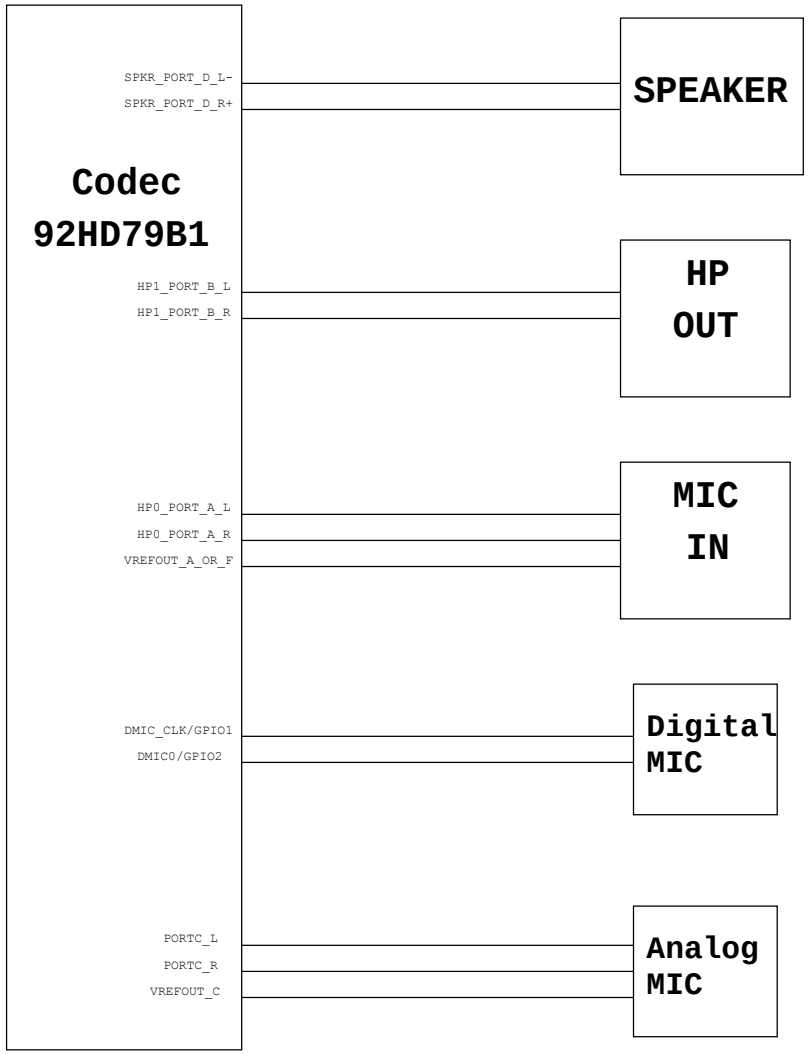
Thermal Block Diagram



Audio Block Diagram



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