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## 8. Block Diagram and Schematic

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	<p>CPU : Intel Penryn                  Chip Set : Intel Cantiga &amp; ICH9M                  Remarks : Montevina Platform</p>						
	<p>Model Name : Bremen-L                  PBA Name : MAIN                  PCB Code : GCE :                                    : NAN :                                    : HAN :</p> <p>Dev. Step : PV                  Revision : 1.0                  T.R. Date : 2009.10.27</p>						
	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Design</td> <td style="width: 35%;">CHECK</td> <td style="width: 35%;">APPROVAL</td> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> </table>	Design	CHECK	APPROVAL			
Design	CHECK	APPROVAL					
<p>Owner : SEC Mobile R &amp; D</p> <p style="text-align: right;">Signature : _____</p> <p style="text-align: right; margin-right: 20px;">X</p>							
<p>DATE: Jan 19 2008 10:00:08 TIME: Bremen-L                  CODE: YLANH DESKTOP MAIN                  APPROVAL: YLANH REV: PV COVER                  PRODUCT CODE: NLANH REV: 1.0</p> <p style="text-align: right;">October 27, 2009 14:27:43 PM</p>	<p style="text-align: center;"><b>SAMSUNG</b> ELECTRONICS</p> <p style="text-align: right;">PAGE 1 OF 59                  PART NO. BA413XXEA</p>						



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## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### BOARD INFORMATION

#### FC / SMB Address

Devices	Address	Hex	Bit
IC90N1	Master		SMBUS Master
CK580M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output/Disable
SOD1MM0	1010 000X	A4h	
SOD1MM1	1010 001X		
MICOM1	Master		
BATTERY	0001 011X	16h	
EMC2102	0111 101X	77h	

#### USB PORT Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCI_0	USB PORT (RIGHT, SUB)	UHCI_3	USB PORT (RIGHT, SUB)
UHCI_1	USB PORT (LEFT)	UHCI_4	CAMERA(17)
UHCI_2	CARP (CARPER/AUS336)	UHCI_5	CAMERA(15)
UHCI_2	BLUETOOTH(FBD)		

#### SATA Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA0		SATA1	

#### PCI EXPRESS Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCIE1	WLAN	PCIE2	Wired LAN
PCIE3		PCIE2	

#### Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHZ	IC93AM	
Crystal	10MHz	MICOM	
Crystal	14.319MHz	CLOCK-Generator	
Crystal	24MHz	LAN	

#### Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
VDC_ADP7	Primary DC system power supply (0 to 19V)	P1_05V_FEG	P1_05V (Direct Media Interface Compensation)
VDC_CMG	Charger Reference Voltage Source	P2_0V	3.0V Power Rail (off in S3-S5)
PRTC_BAT	3.3V supply for the RTC well.	P1_05V	1.05V Power Rail (off in S3-S5)
P5_0V_ALW	5.0V always power well	P1_05V_CORE	3.3V Power Rail (off in S3-S5)
P12_0V_ALW	12.0V always power well	P2_0V_AUX	5.0V Power Rail (off in S4-S5)
P1_V_VREF	Power Chip Reference	P3_3V_AUX	3.3V Power Rail (off in S4-S5)
P5_0V_VREF	Power Chip Reference	CHP_CORE	3.3V Power Rail (off in S4-S5)
P3_3V_MICOM	Output voltage of P3302SAGQW/ (if VDC is removed, it will be off)	AUD_P5V	5.0V supply for Audio
LCO_V003V	3.3V (LED LCO)	P4_75V_AUD	Audio Analog Voltage
KBC3_CHG42V	To charge battery	P5_0V_STB	Technique USB driver at sleep status
P12_3V_LAN	Internal Regulator's Power of LAN Controller	EGP_V_CORE	3.0V supply in S3-S5
P2_9V_LAN		P1_3V_AUX	1.3V Power Rail (off in S3-S5)
P3_3V_MCD	3.3V (3-pin-1-Stock)	P1_3V_AUX	1.3V Power Rail (off in S3-S5)

#### REVISION HISTORY

See rev notes for more information.

DATE	BY	REASON	REV	DESCRIPTION
2008.09.25	YK/ML	Initial	1.0	Initial

DATE	2008.09.25	REV	1.0
BY	YK/ML	REASON	Initial

DATE	2008.09.25	REV	1.0
BY	YK/ML	REASON	Initial

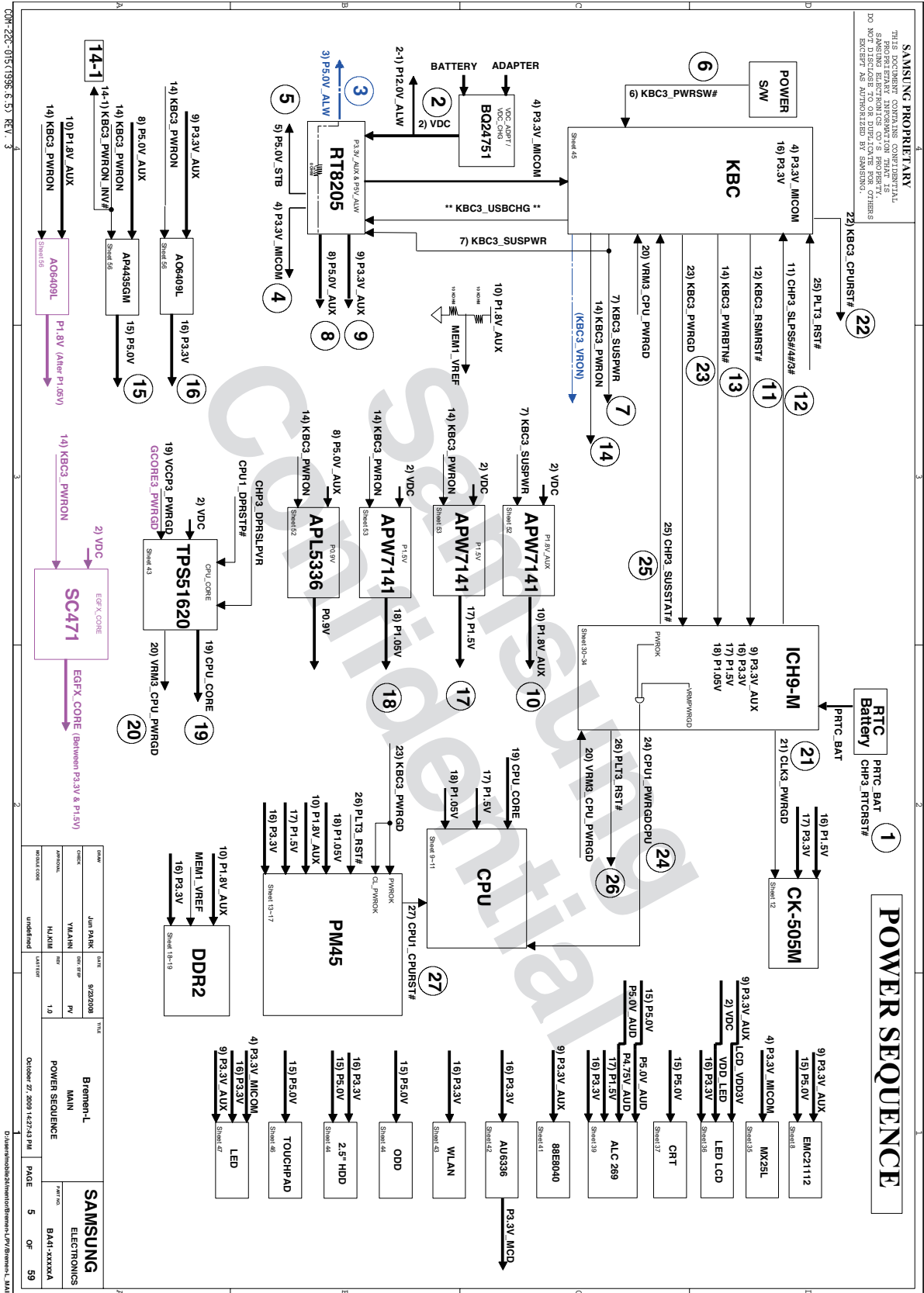
  

DATE	2008.09.25	REV	1.0
BY	YK/ML	REASON	Initial



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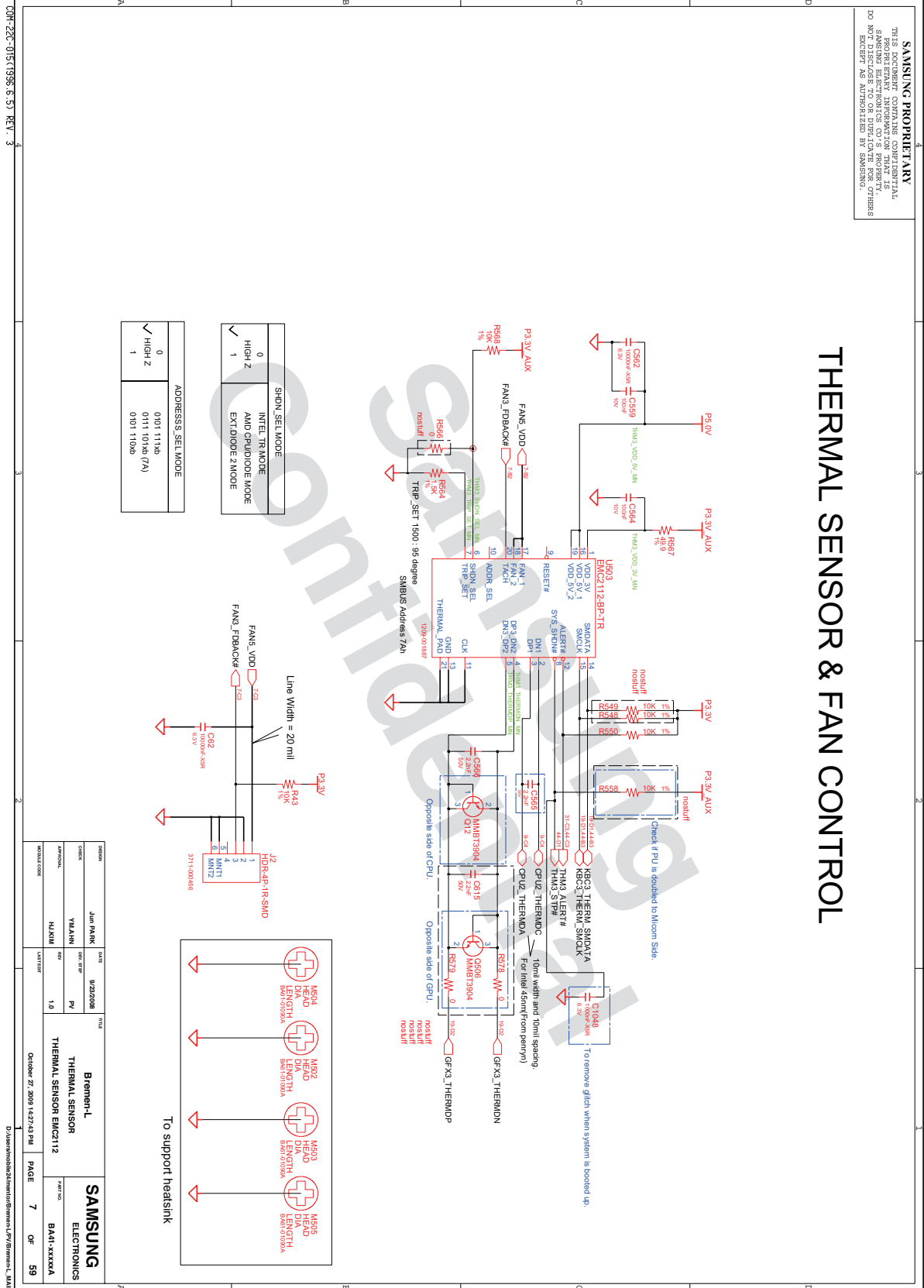


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# THERMAL SENSOR & FAN CONTROL



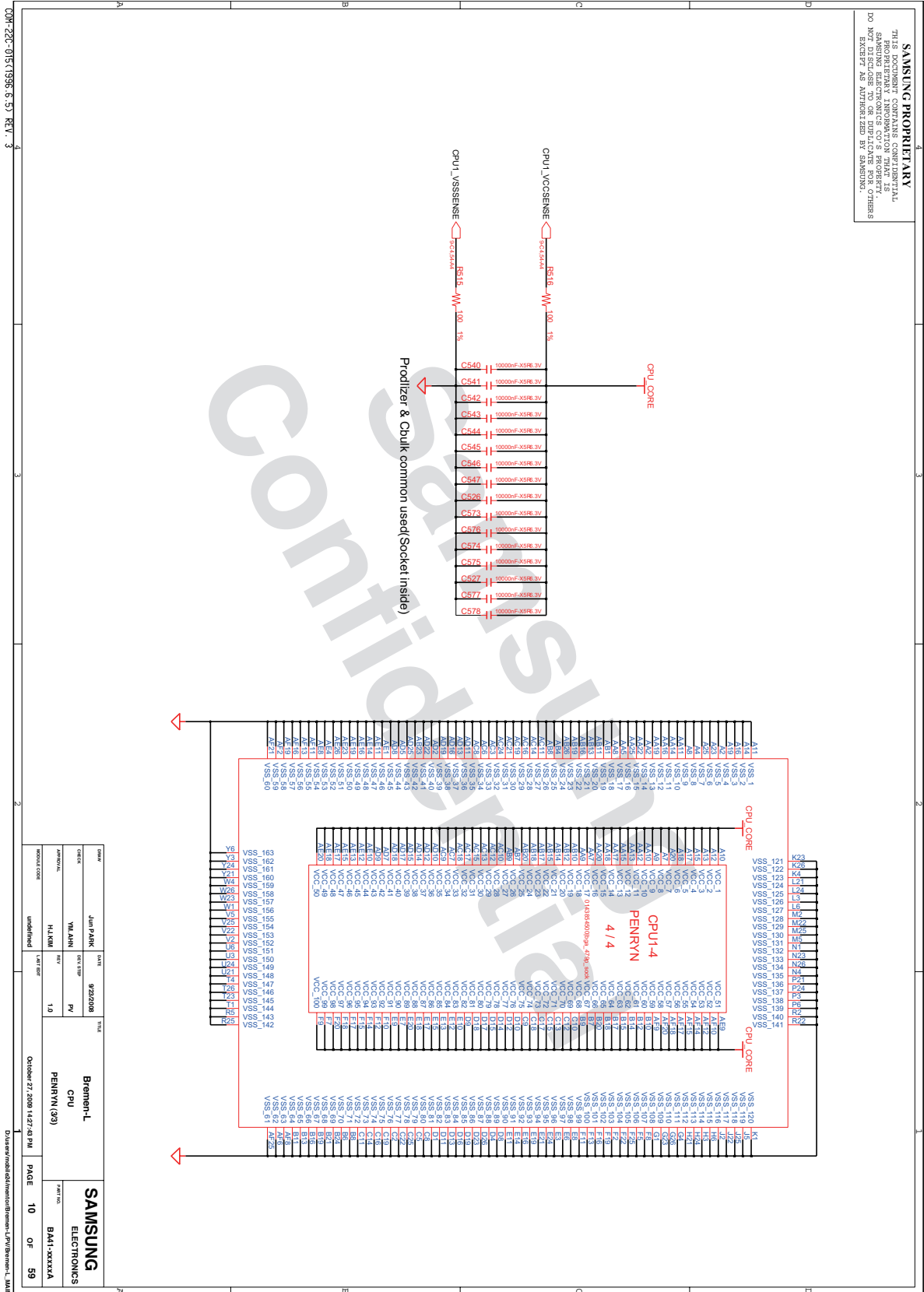






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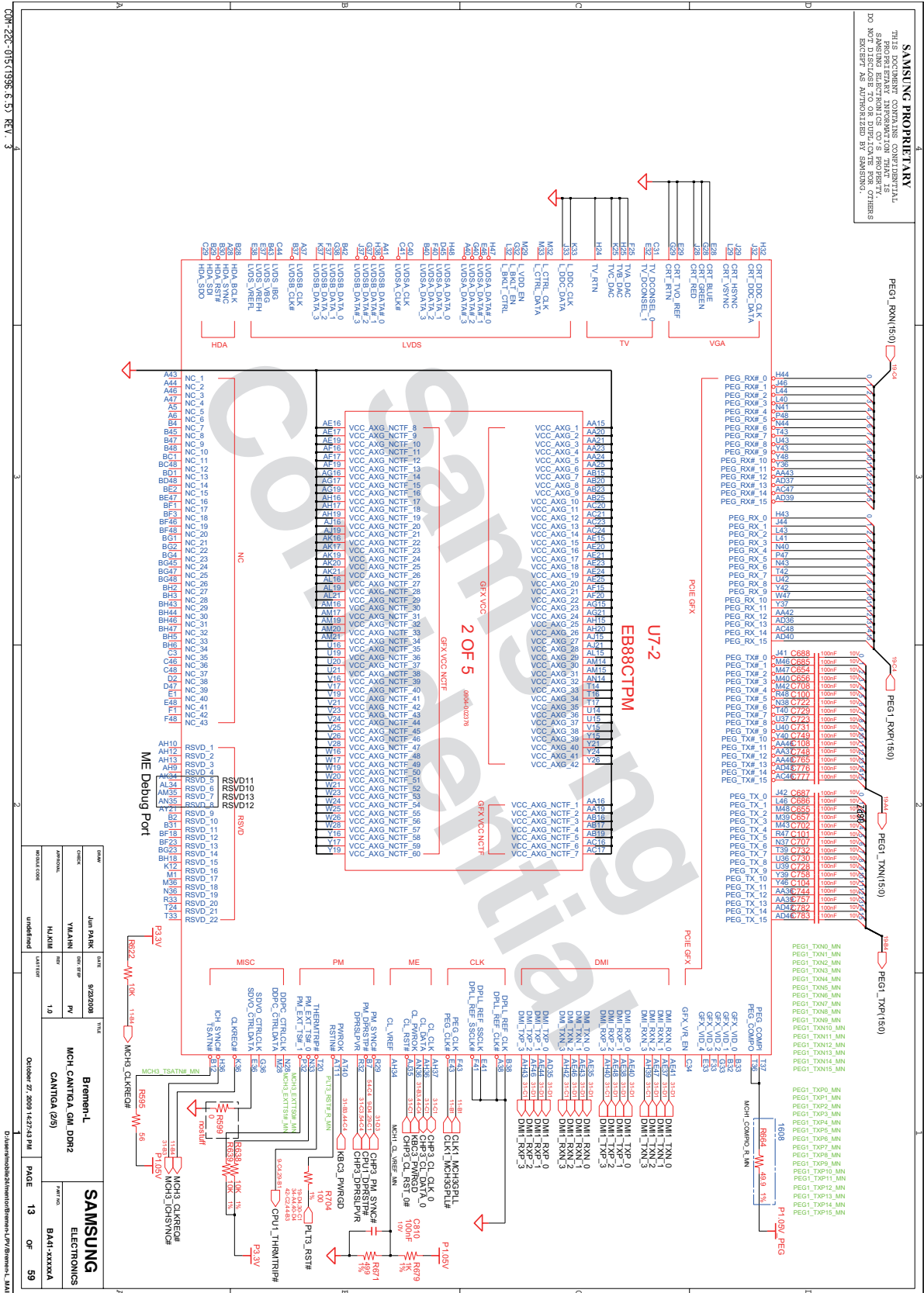






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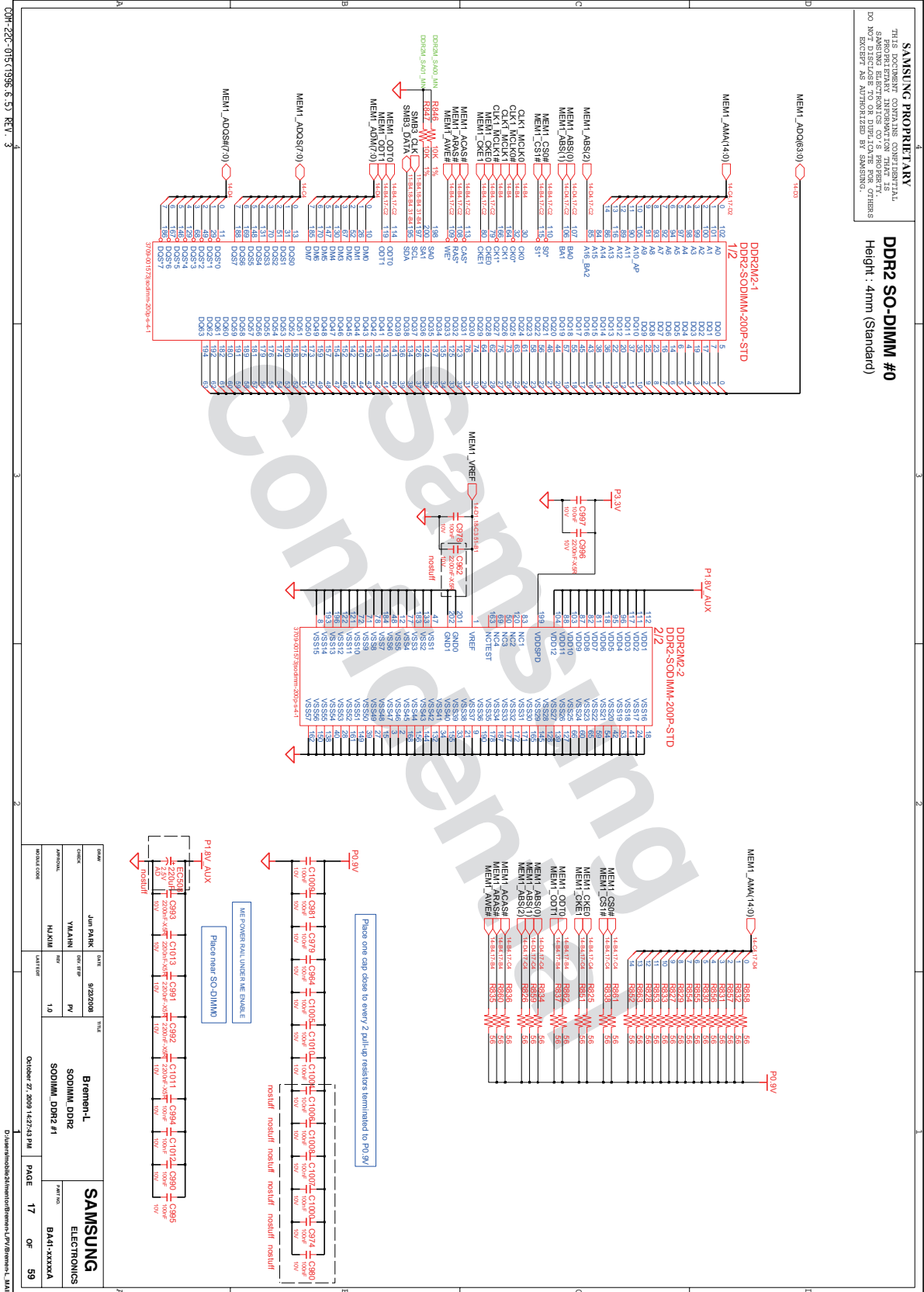






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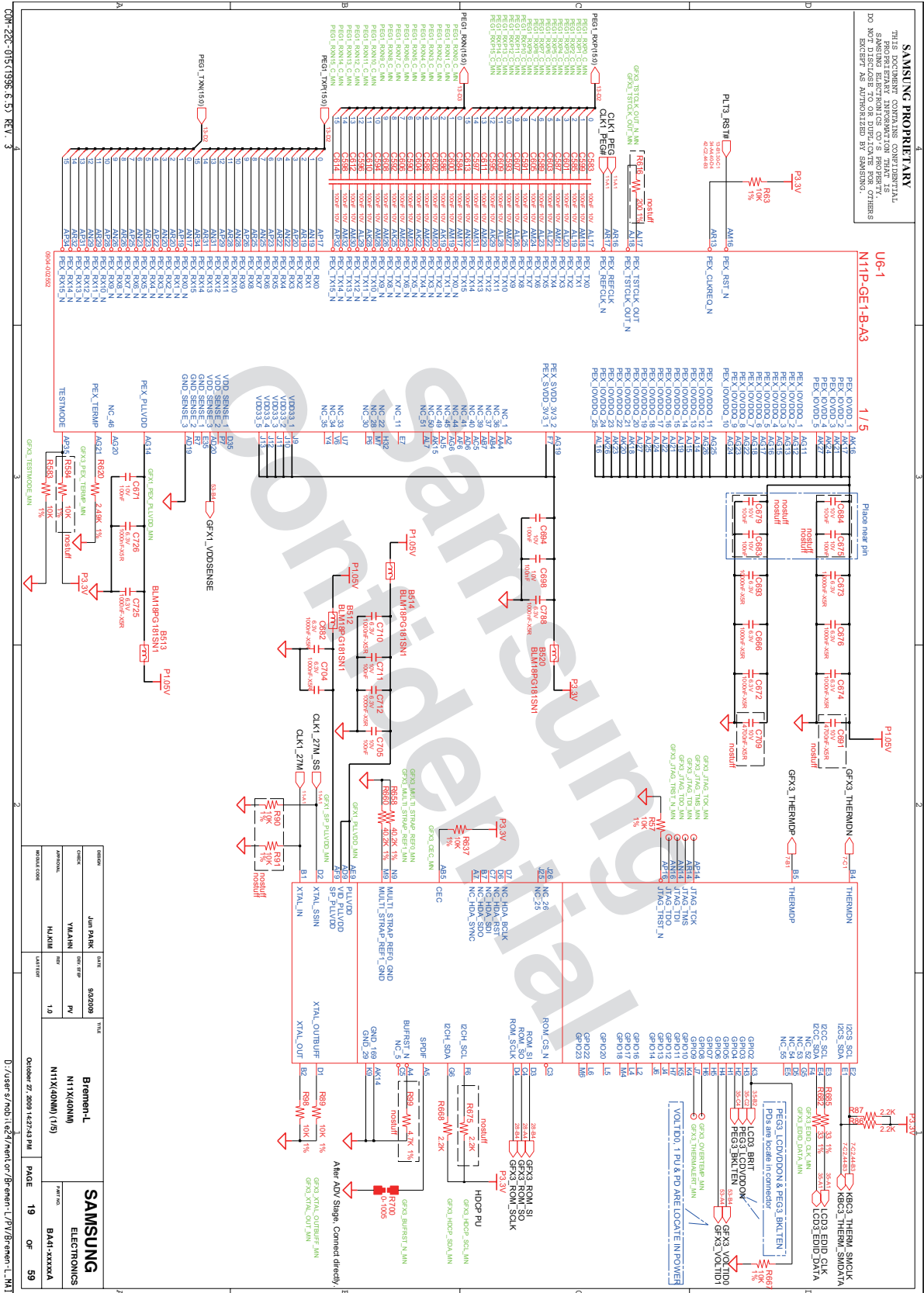
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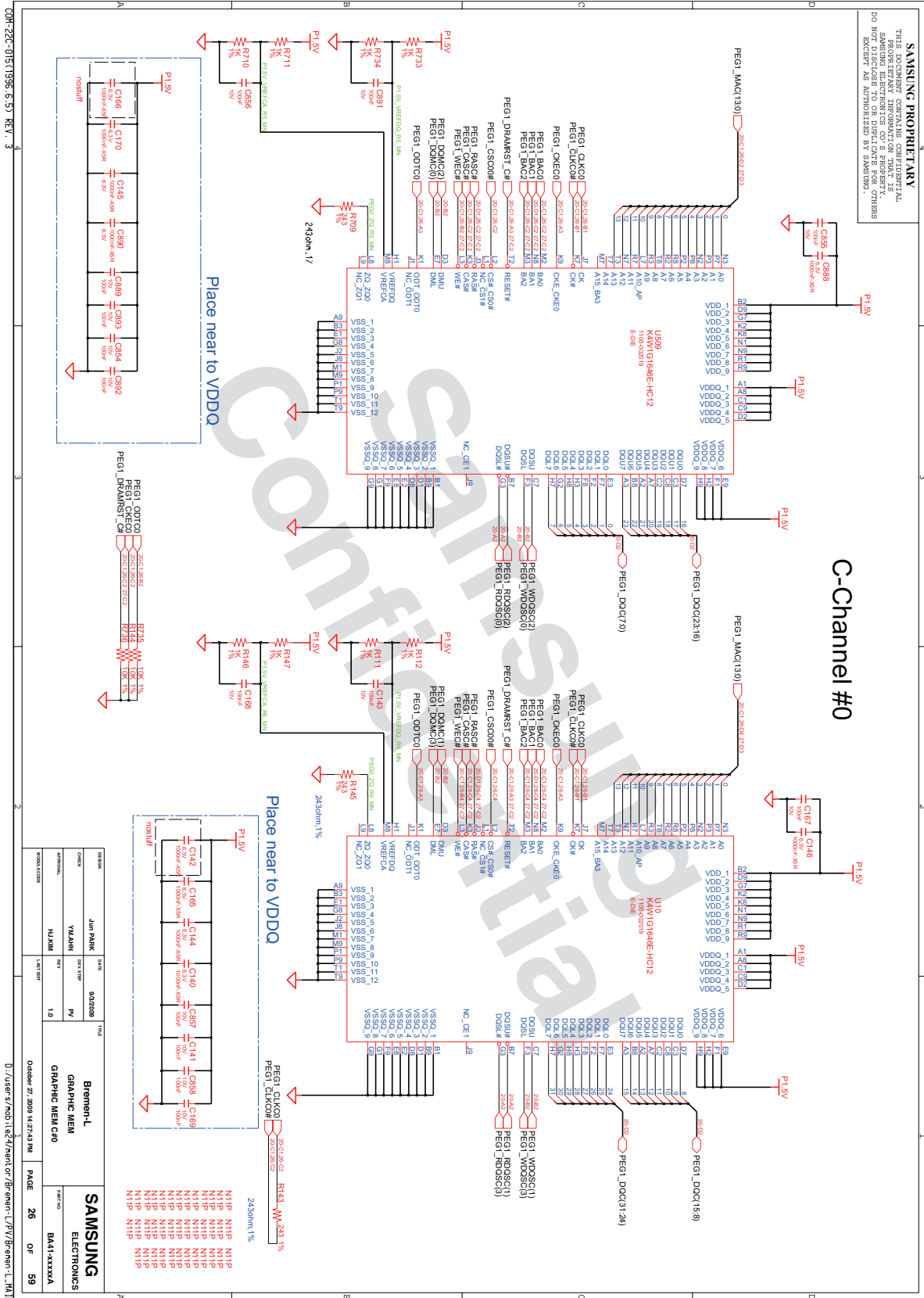






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### N11x\_40nm STRAP

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT 0
ROM_S0	XCLK_417	FG_0_BUR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PC1_DEV0D4	SUB_VENDOR	SLOT_CLK_CFG	PEX_PULL_EN_TERM
ROM_SI	RAMCFq3	RAMCFq2	RAMCFq1	RAMCFq0
STRAP1	PC1_DEV0D3	PC1_DEV0D2	PC1_DEV0D1	PC1_DEV0D0
STRAP2	3G10_PA0CFq3	3G10_PA0CFq2	3G10_PA0CFq1	3G10_PA0CFq0
STRAP0	USER03	USER02	USER01	USER00

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

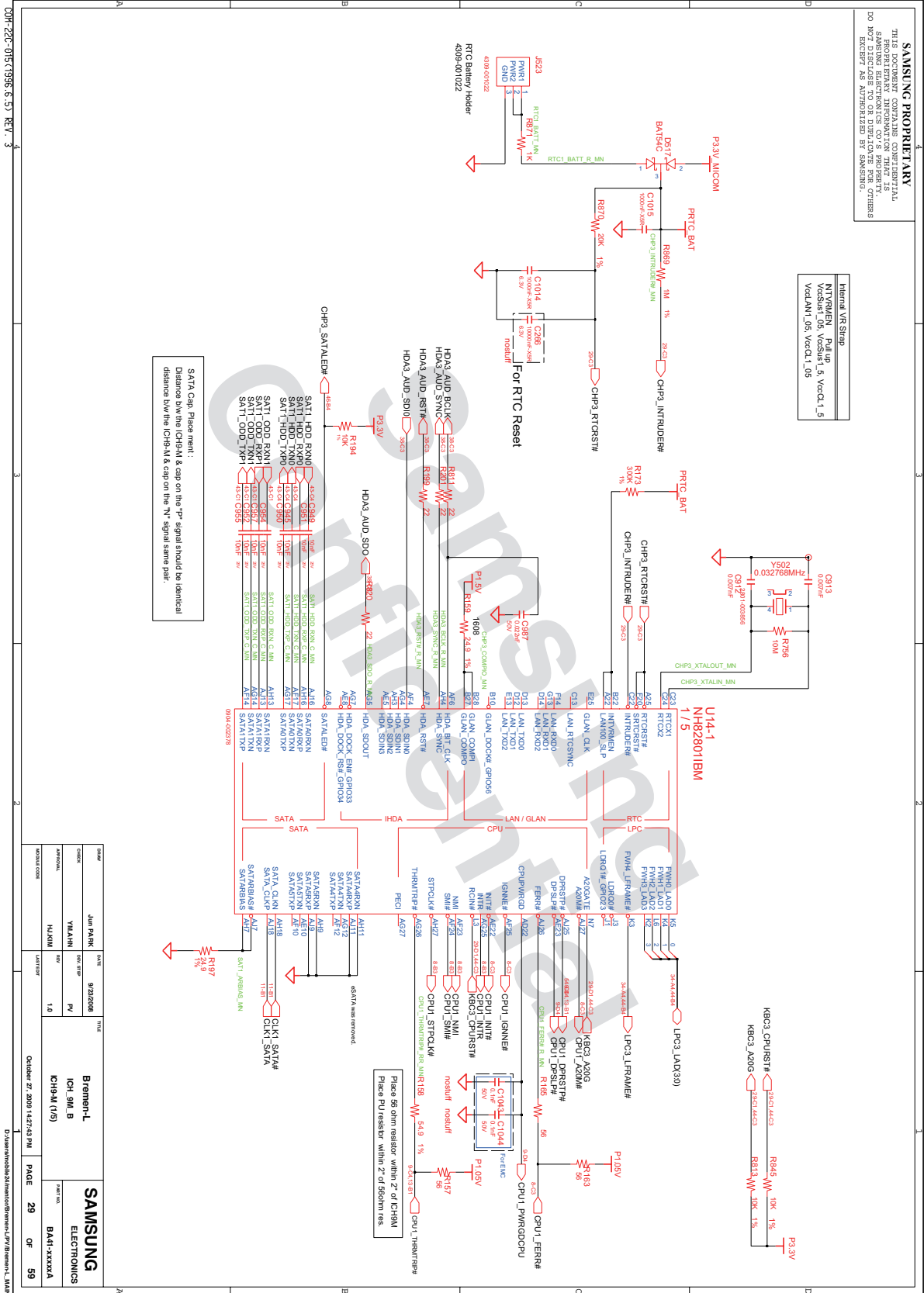
DESIGN	JUN PARK	DATE	09/20/09	TITLE	Bremon-L
CHECK	YI.MAN	CHK'd TIME	PV		HDMI
APPROVAL	H.KIM	REV	1.0		HDMI
WORK CODE		REV			

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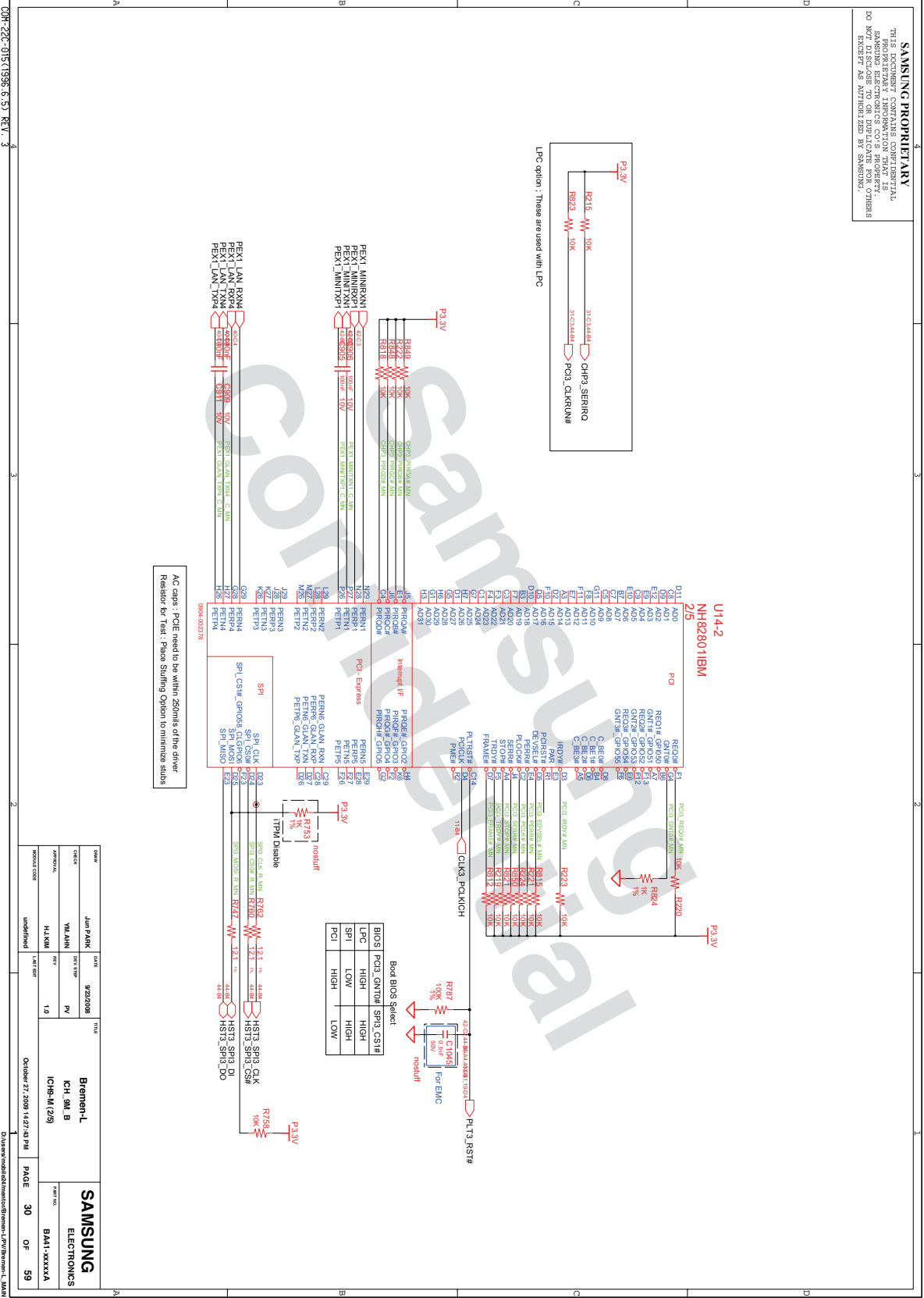
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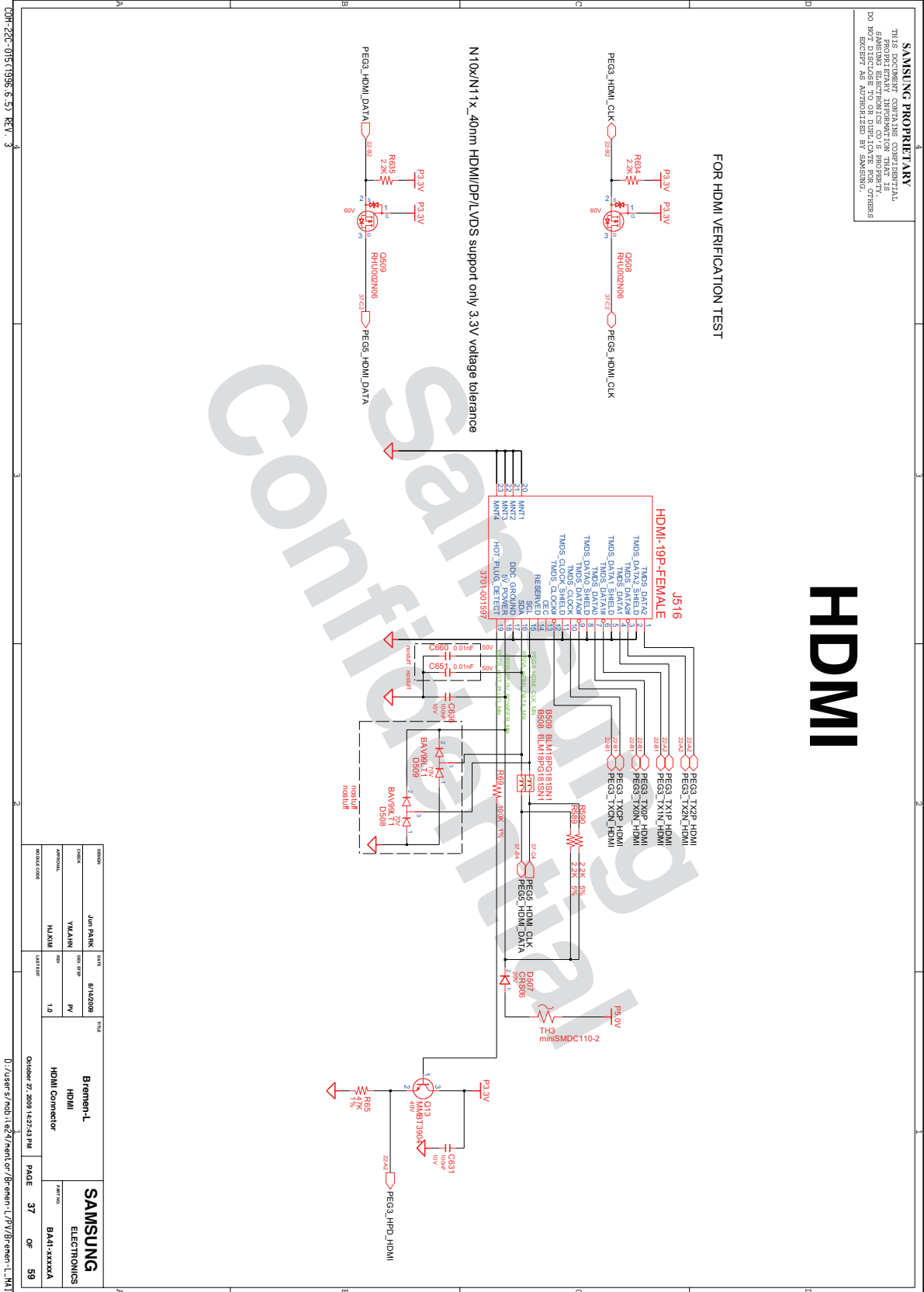






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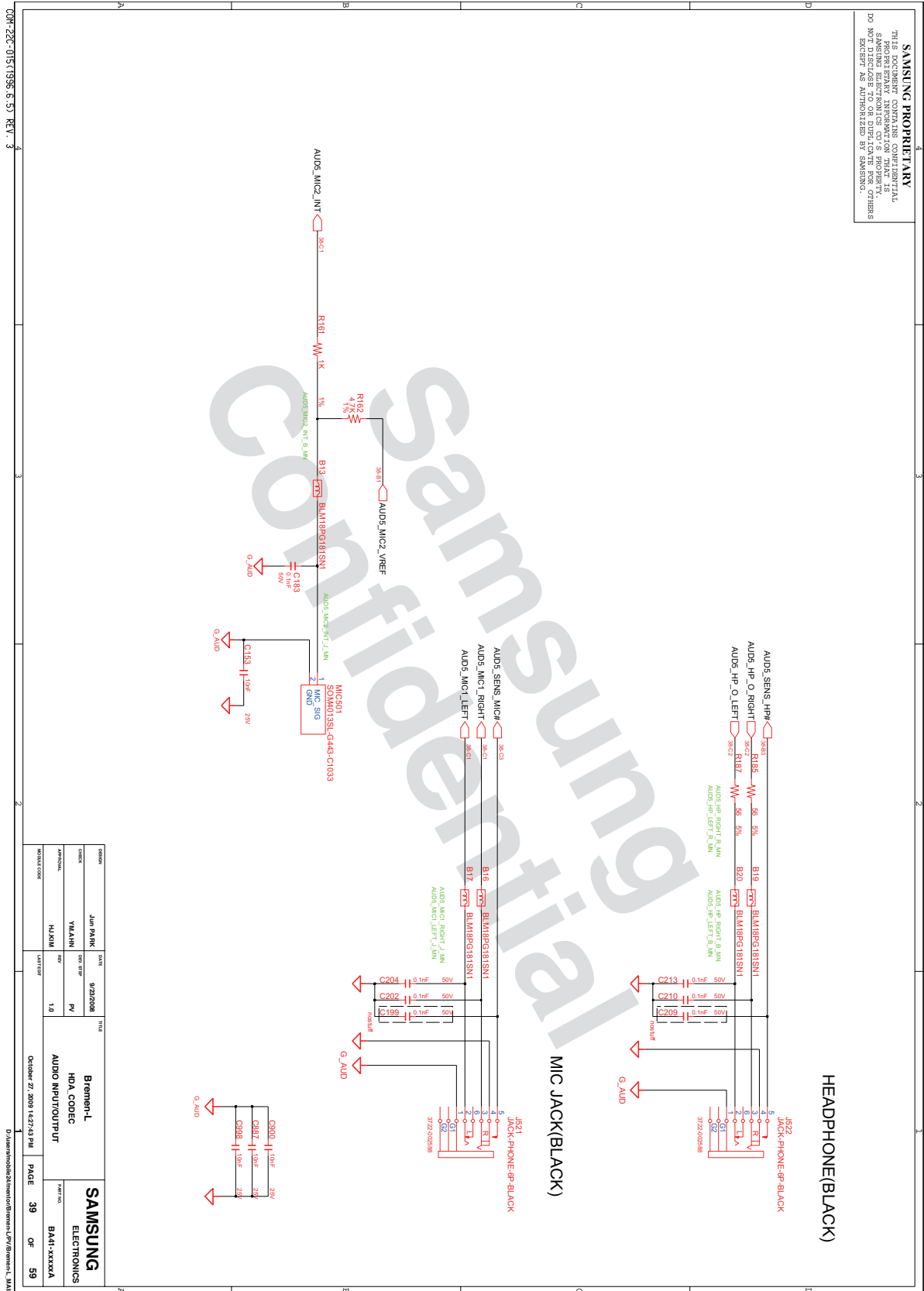
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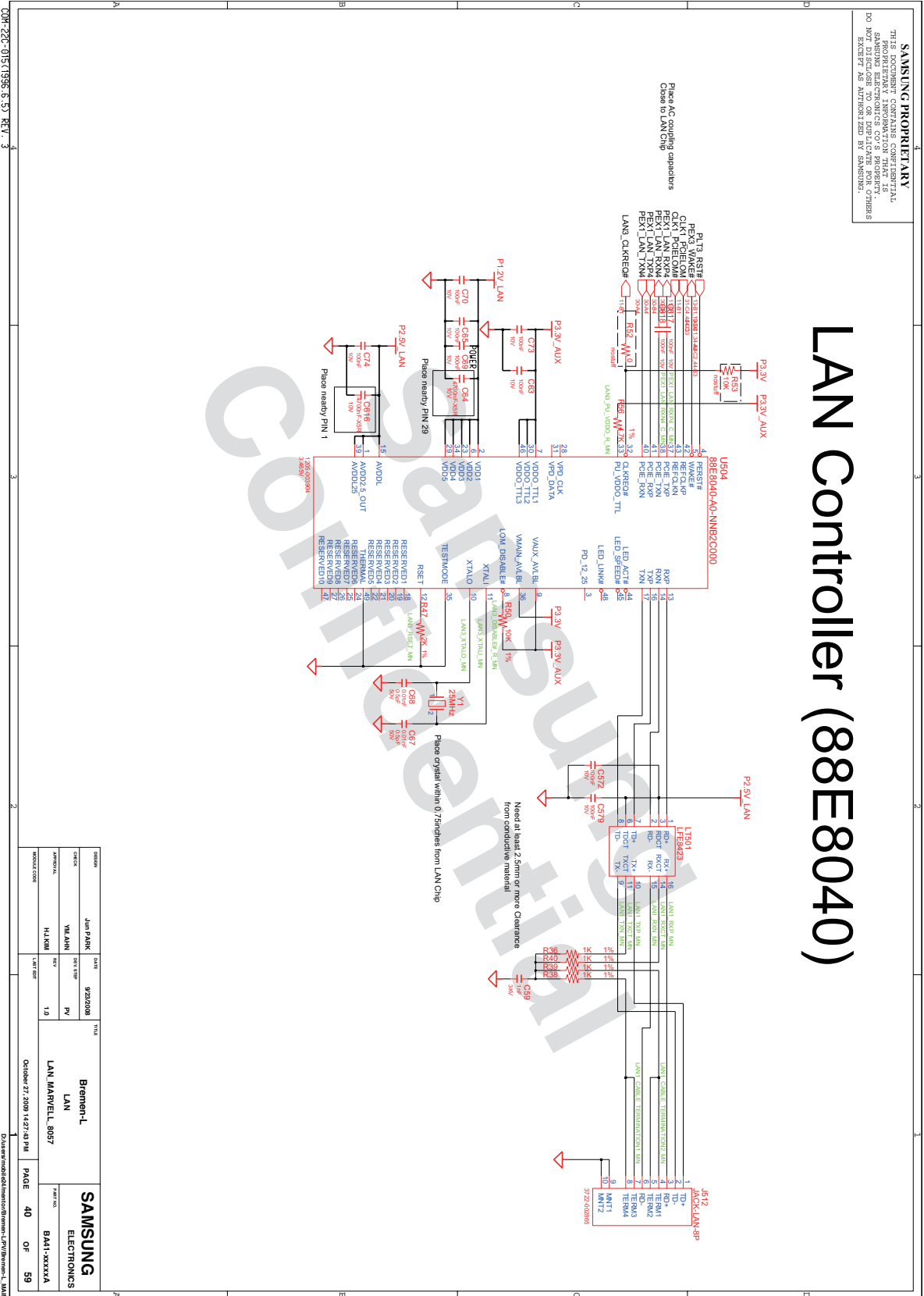
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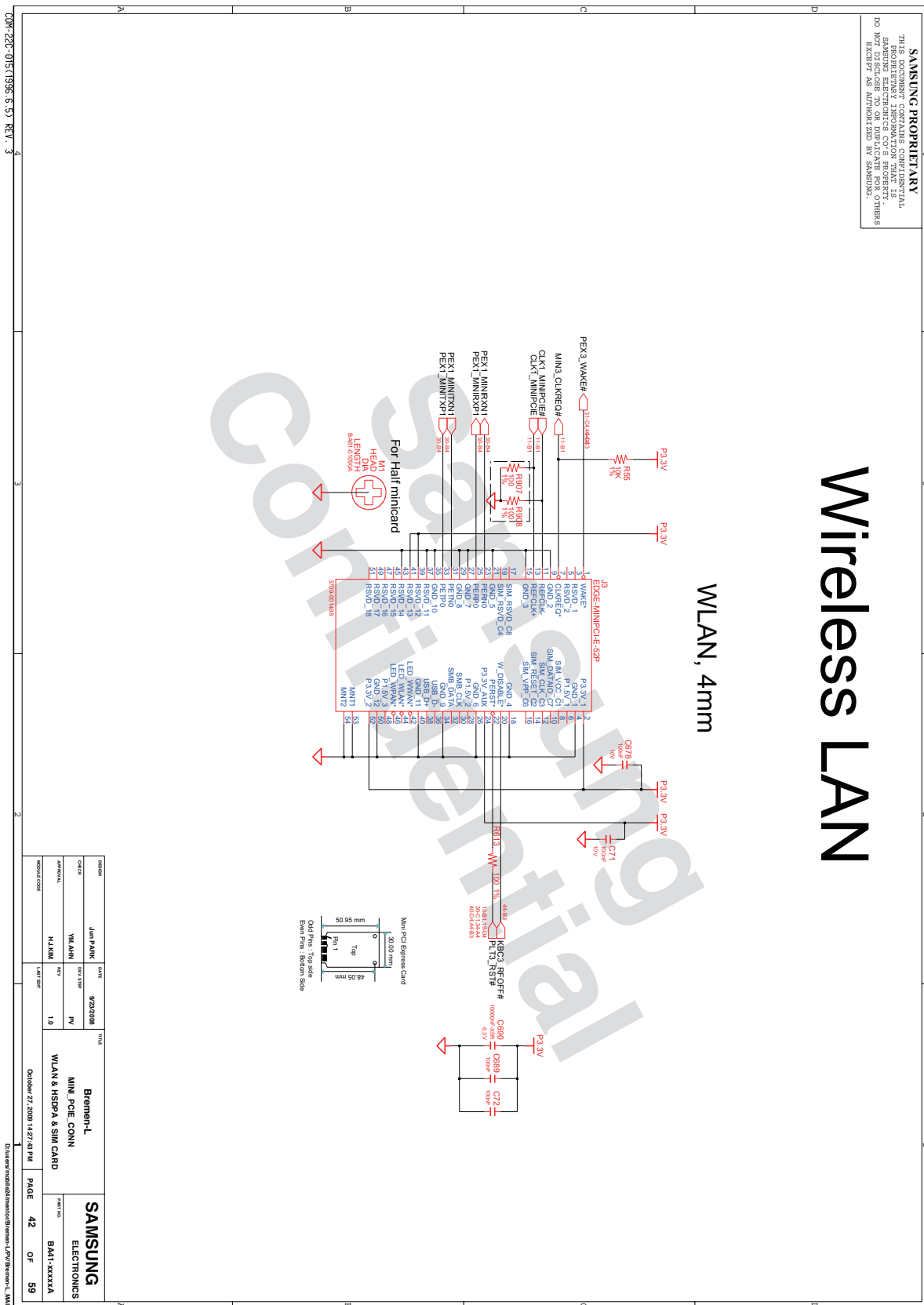






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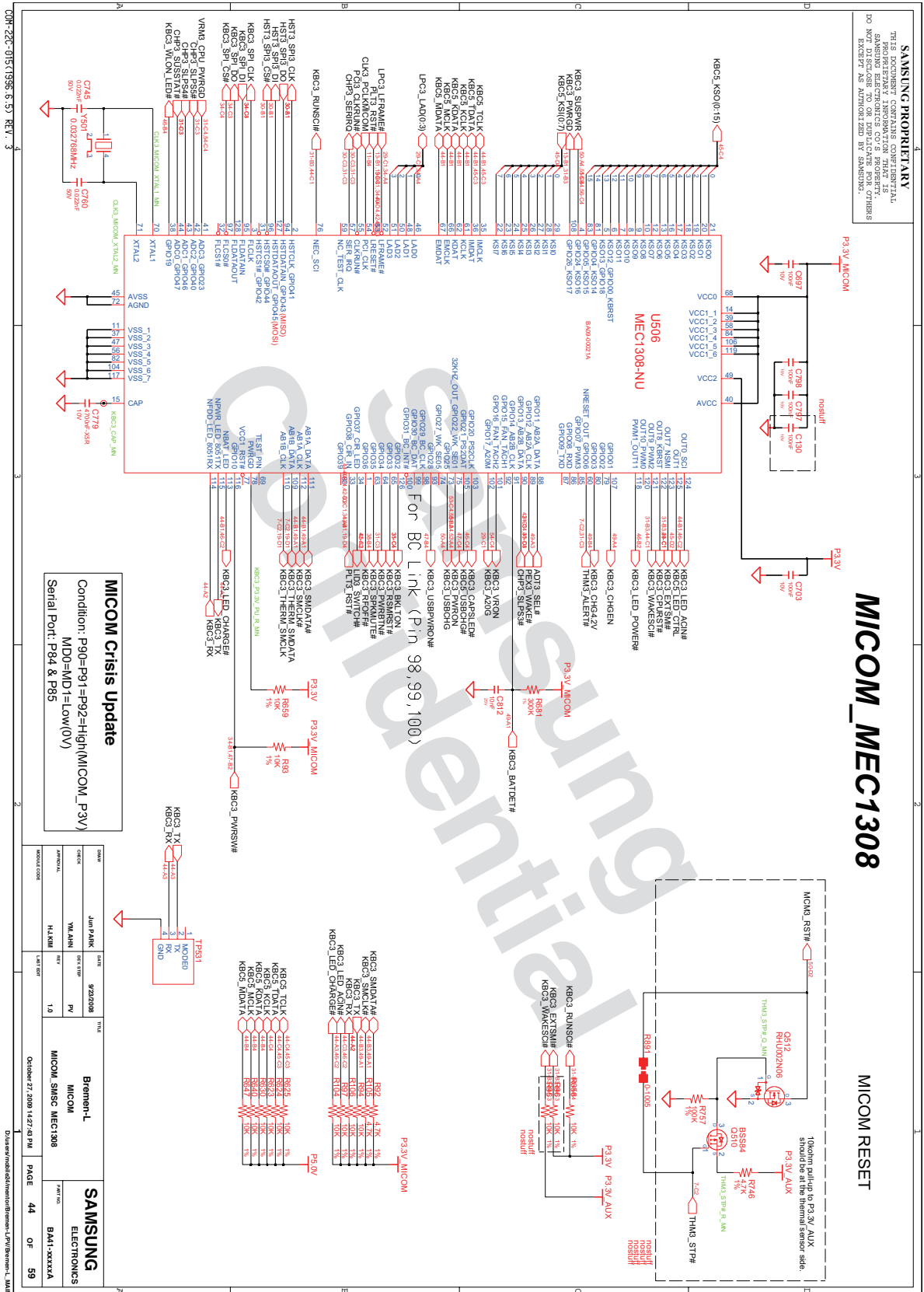
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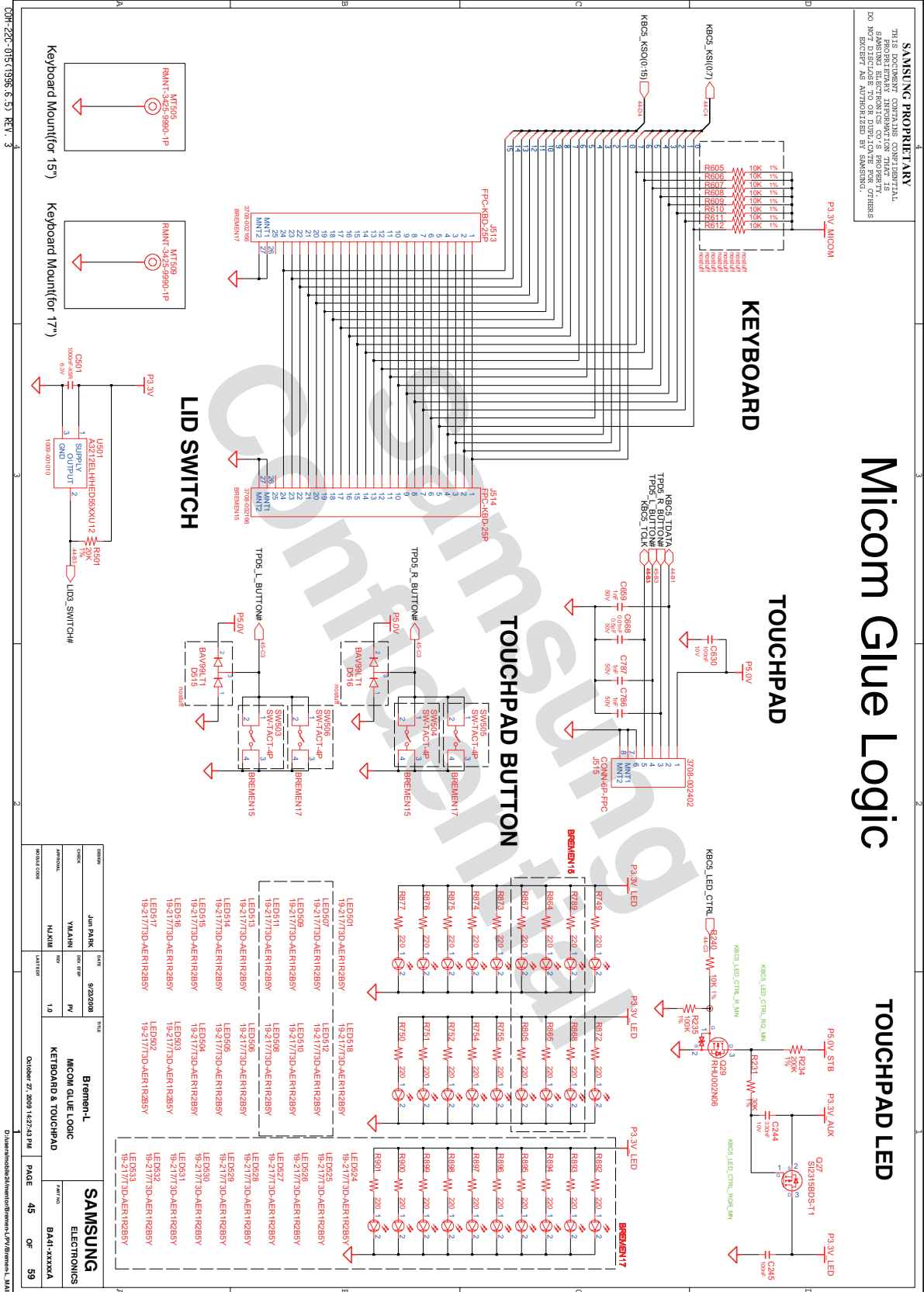
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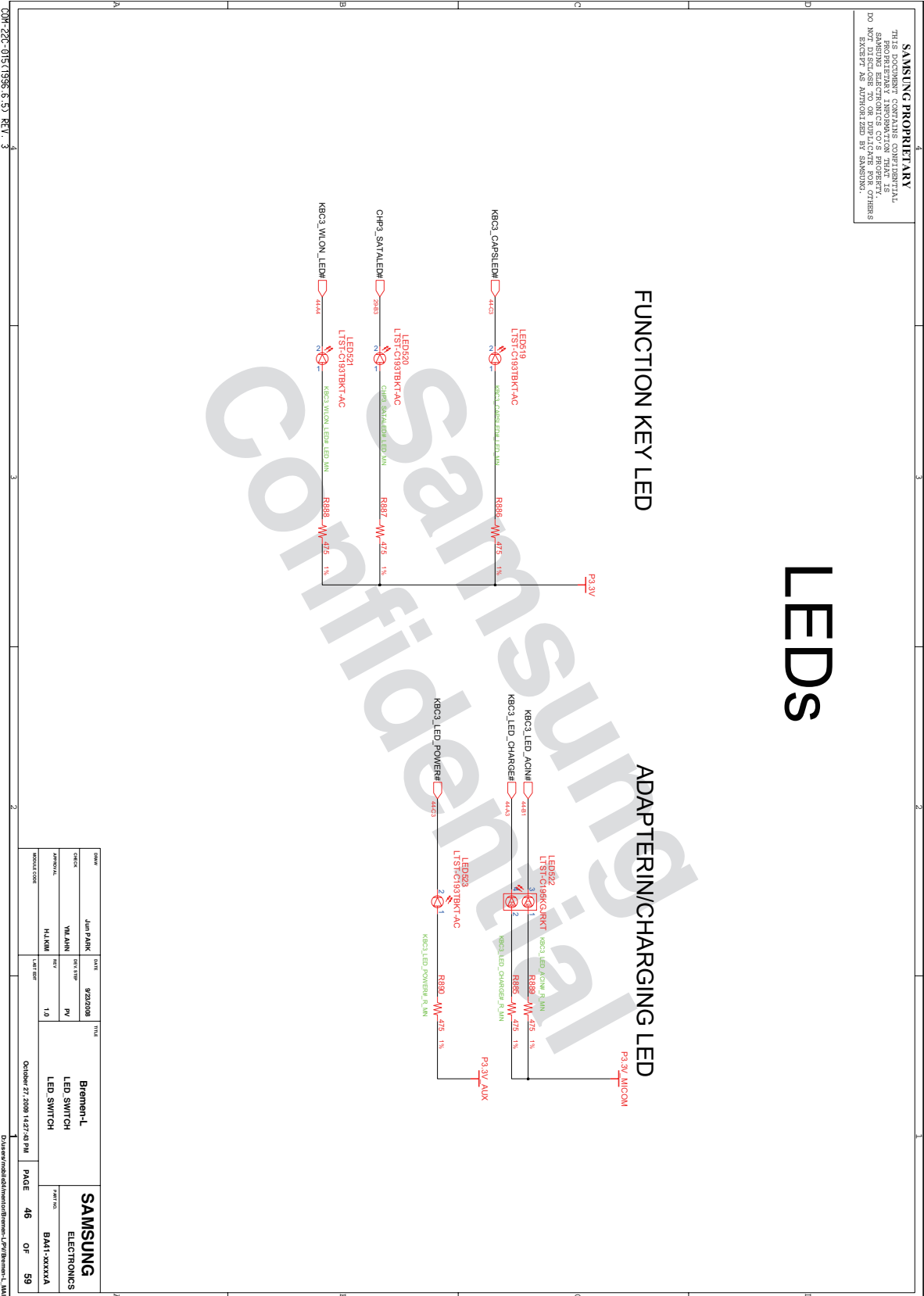
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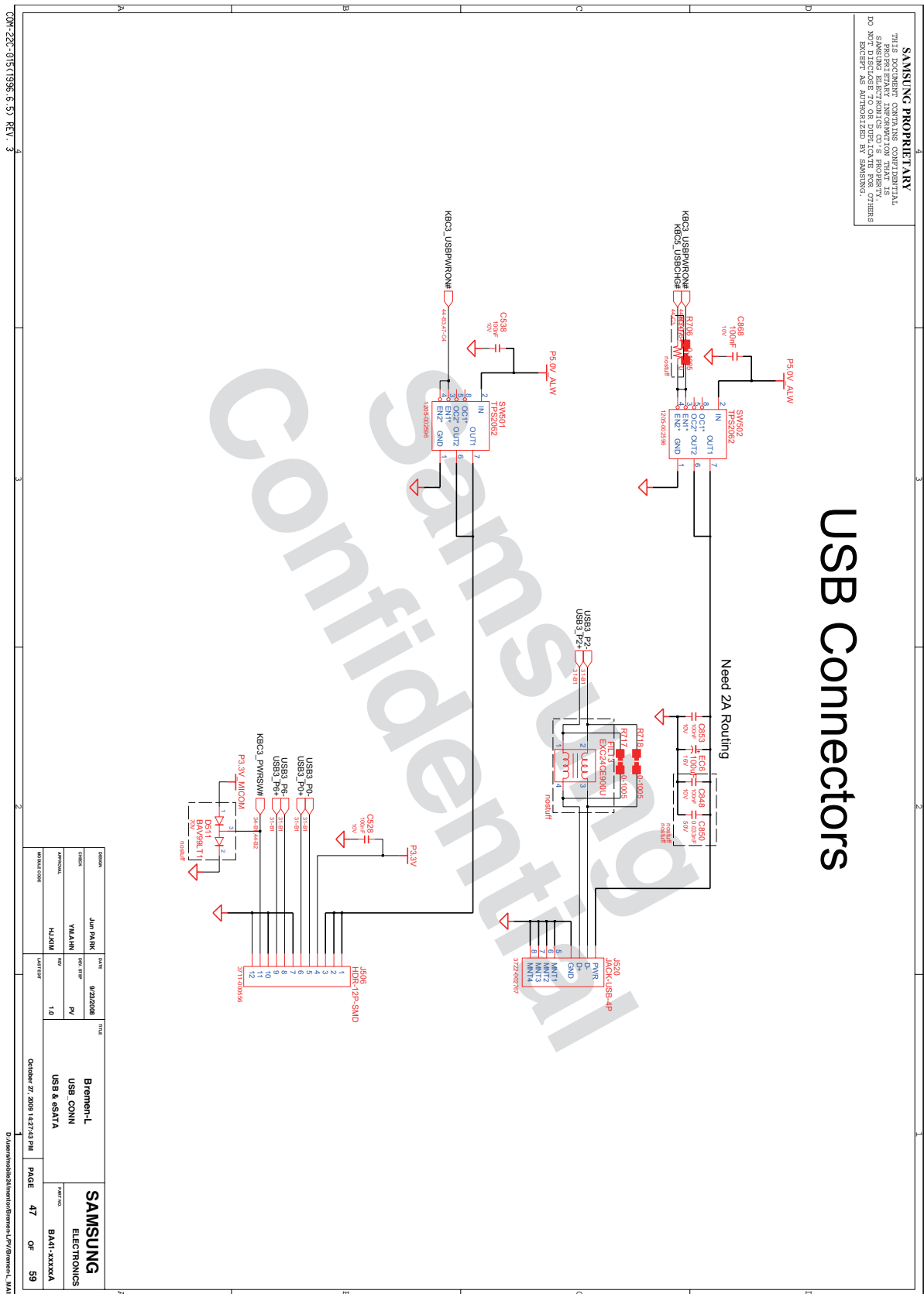
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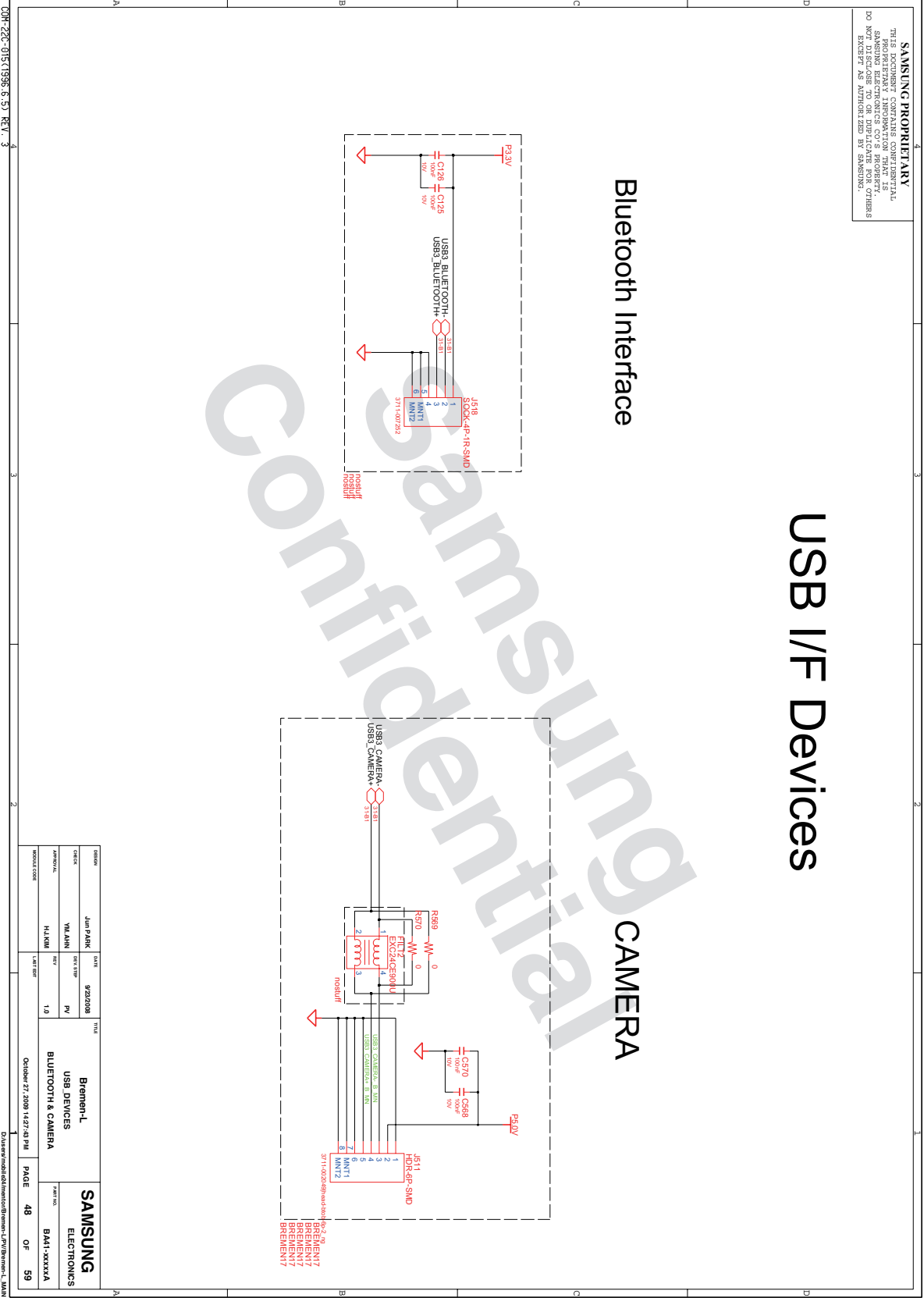
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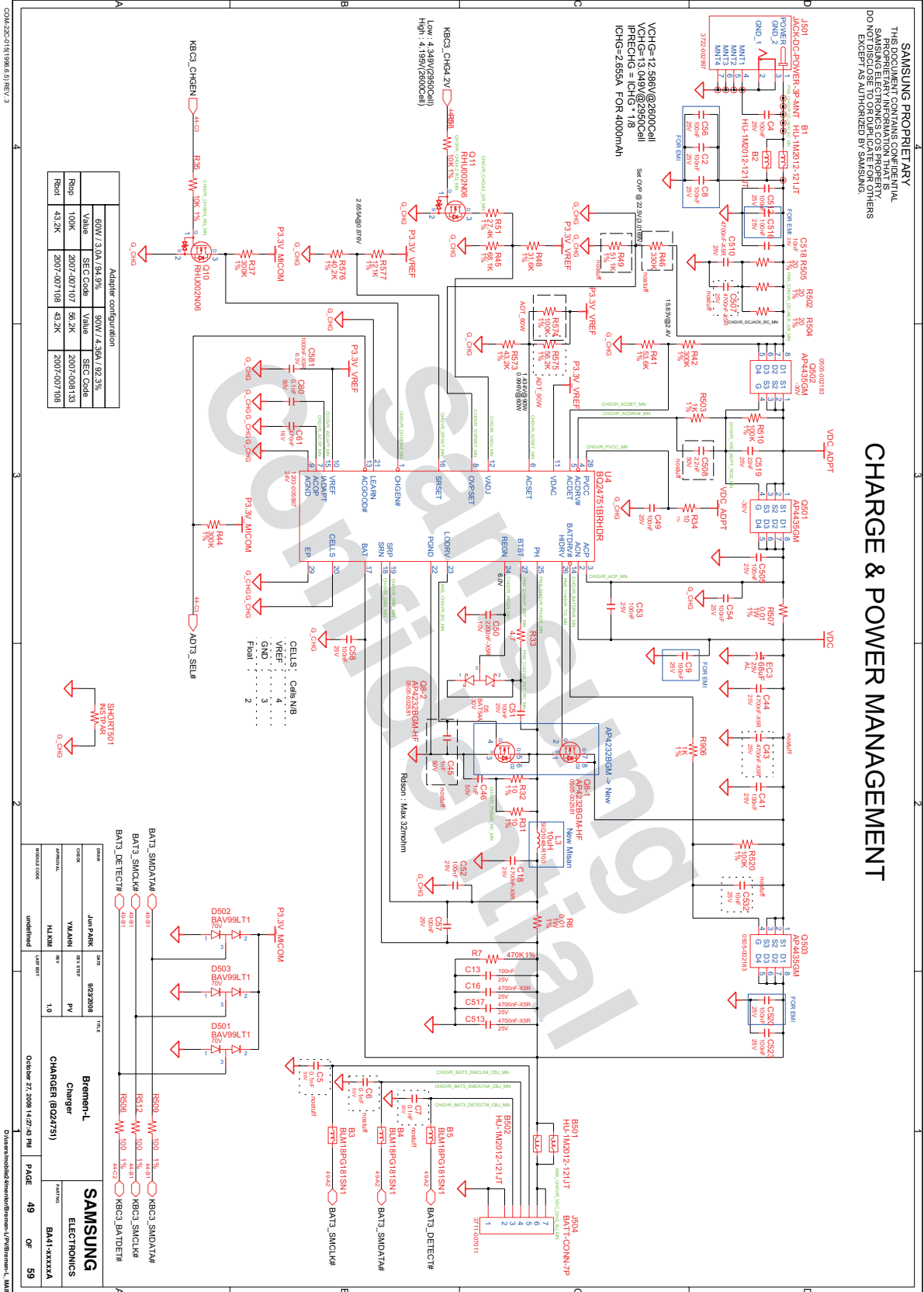
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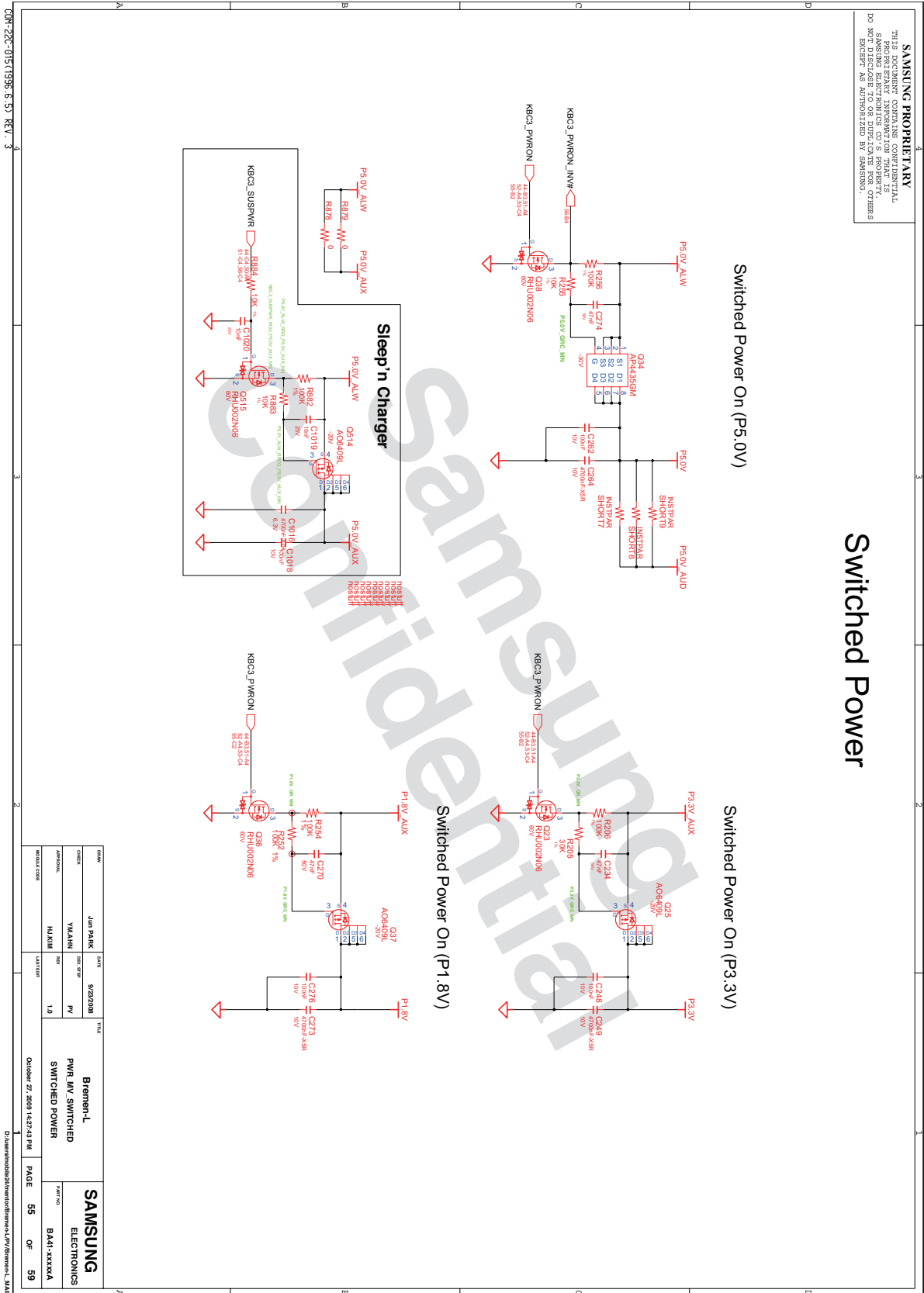






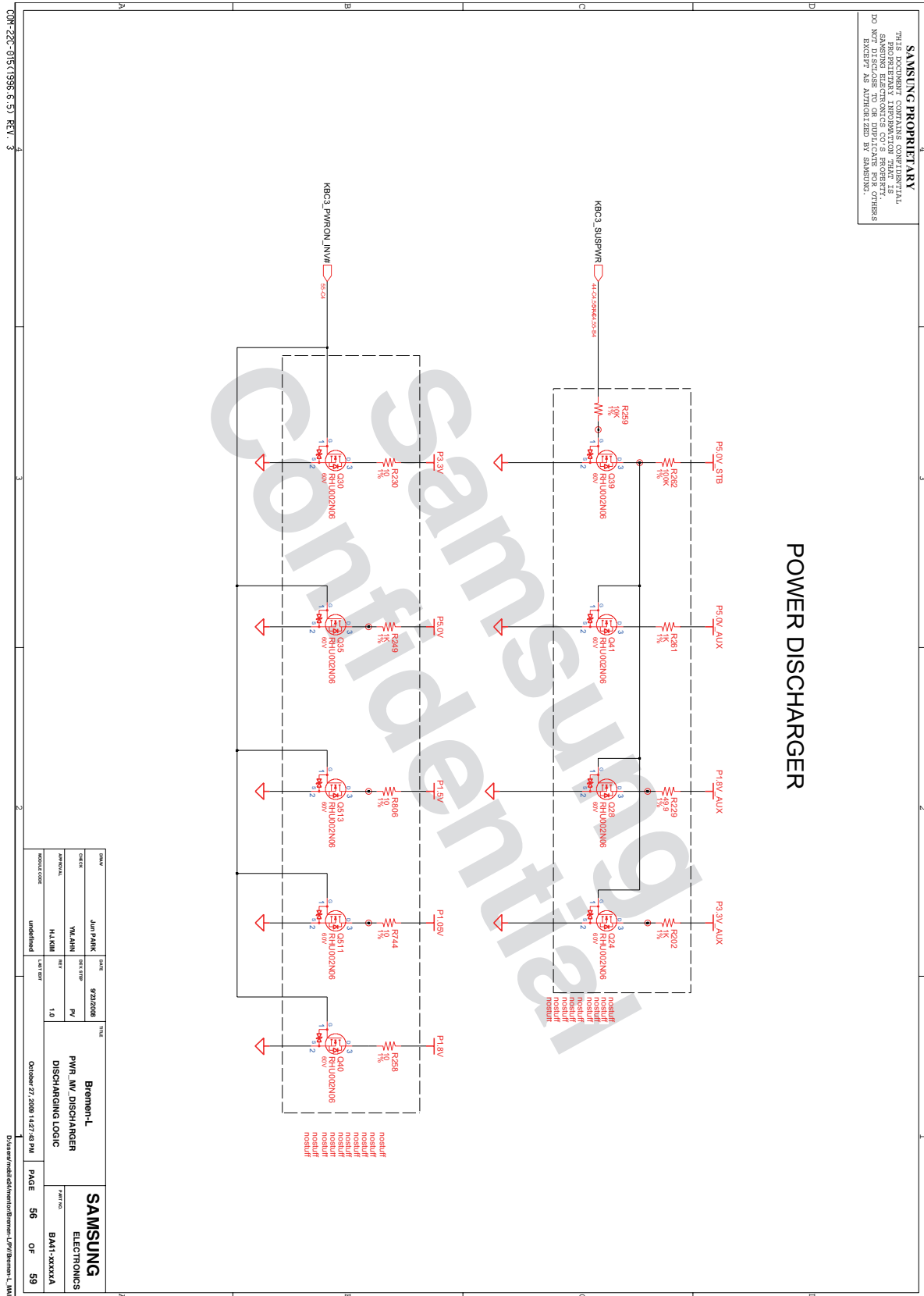
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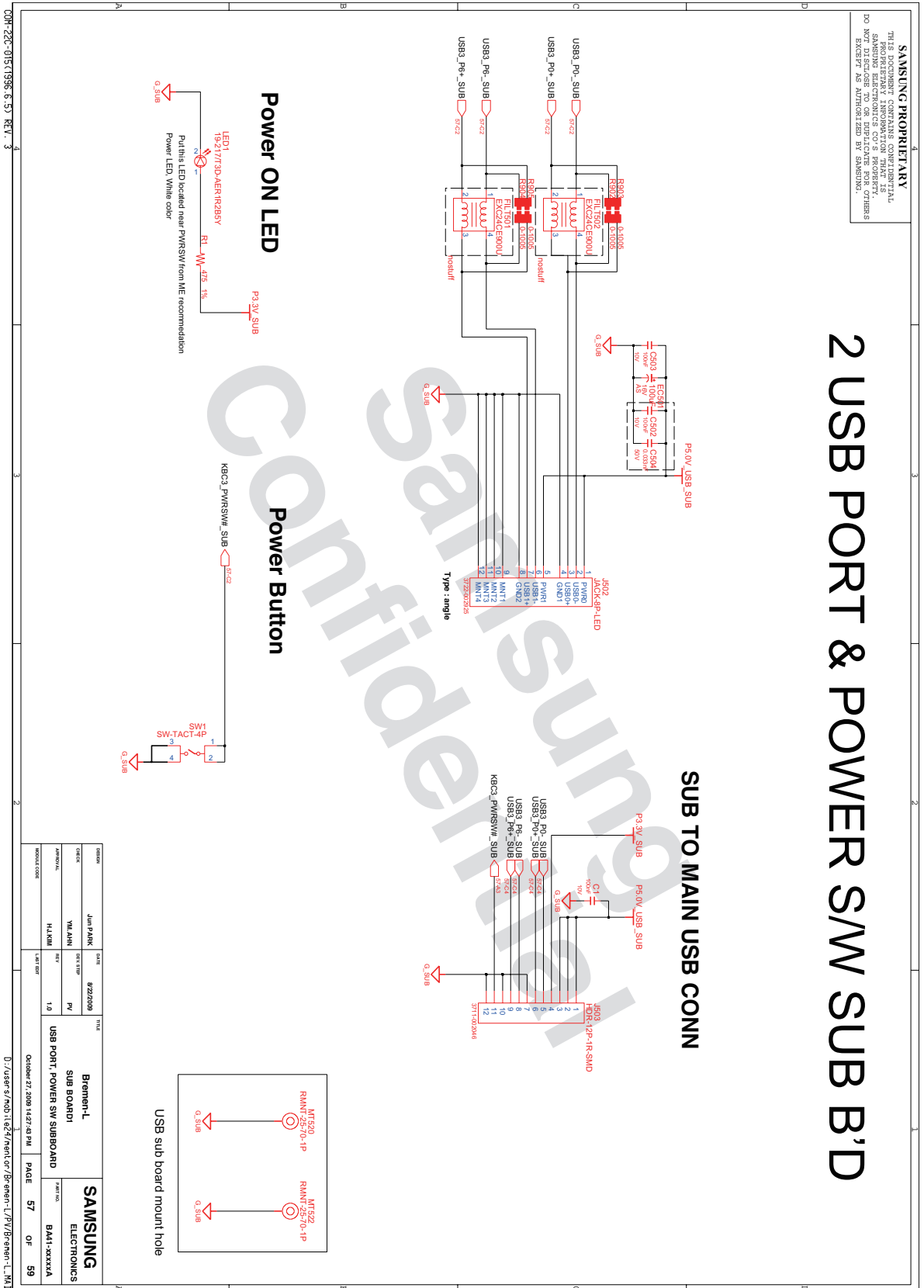
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# Bremen-UL

CPU : Intel Penryn  
 Chip Set : Intel Cantiga & ICH9M  
 Remarks : Montevina Platform

Model Name : Bremen-UL  
 PBA Name : MAIN  
 PCB Code : GCE : BA41-01177A  
                   : NAN : BA41-01178A  
                   : HAN : BA41-01179A  
 Dev. Step : PV  
 Revision : 1.0  
 T.R. Date : 2009.10.19

Design	CHECK	APPROVAL

Owner : SEC Mobile R & D      Signature : \_\_\_\_\_      X

NAME	TY/AM	DATE	TITLE
DESIGN	MAIN	10/19/2009	Bremen-UL MAIN COVER
APPROVAL	SJ/PJK	1.0	

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**BOARD INFORMATION**

**SCHEMATIC ANNOTATIONS AND BOARD INFORMATION**

**PCI Devices**

Devices	DSELU#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A, B, C
USB	AD20(Internal)	-	USB2.0#0 (USB0), A USB2.0#1 (USB1), A USB2.0#2 (USB4), C USB2.0#3 (USB5), E USB2.0#4 (USB6), H USB2.0#5 (USB7), H
Hub to PCI	AD30(Internal)	-	B
Internal MAC	AD33(Internal)	-	E
PCI bridge/IDE/AC97/SMBUS	AD24(Internal)	-	E, F
ACLink	-	-	-
CLink	-	-	-

**Voltage Rails**

Primary DC system power supply (0 to 20V)

VDC\_CORE Core Voltage for CPU @ ICH9M

VDC\_VDD Core Voltage for CPU @ ICH9M

F3.3V\_MCOM 3.3V always power rail (for Microm)

F1.8V 1.8V switched power rail (off in S3-S5)

F1.5V 1.5V switched power rail (off in S3-S5)

F1.8V\_AUX 1.8V power rail for DDR (off in S4-S5)

F3.3V 3.3V switched power rail (off in S3-S5)

F3.3V\_AUX 0.9V power rail for DDR (off in S3-S5)

F3.3V 3.3V switched power rail (off in S3-S5)

F3.3V\_AUX 3.3V switched power rail (off in S4-S5)

F5.0V 5.0V switched power rail (off in S3-S5)

F5.0V\_AUX 5.0V switched power rail (off in S4-S5)

F5.0V\_AUX 5.0V always power rail

USB PORT Assign	PCI Express Assign		
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Main Card 1 (WLAN)
2	SYSTEM PORT 2	2	LAN
3	NC	3	LAN
4	Bluetooth	4	Main Card 2 (ROBSON or DVB-T)
5	NC	5	NC
6	Main PCI Express 2		
7	Camera		
8	NC		
9	NC		

(This table will be update.)

**Crystal / Oscillator**

TYPE	FREQUENCY	DEVICE	USAGE
Ox/ytal	32.768KHz	ICH9M	Real Time Clock
Ox/ytal	14.318MHz	CLK	CLK
Ox/ytal	25MHz	LAN	LAN
Ox/ytal		LAN	RealTime 88EE8957

**LCD Panel Detect (TPD)**

Devices	Resolution	PANEL_DETECT_0

**I<sup>2</sup>C / SMB Address**

Devices	Address	Hex	Bus
ICH9M	Master	-	SMBUS Master
GPIO Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM1	1010 010x	4Ah	-
SODIMM2	0011 010x	3Ah	-
Terminal Sense on SODIMM1	0011 010x	3Ah	-
Terminal Sense on SODIMM2	0011 010x	3Ah	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

**REVISION HISTORY**

See rev notes for more information.

REV	DATE	DESCRIPTION	BY	CHK
00000000	undefined	Initial		

REV	DATE	DESCRIPTION	BY	CHK
00000000	undefined	Initial		

REV	DATE	DESCRIPTION	BY	CHK
00000000	undefined	Initial		

REV	DATE	DESCRIPTION	BY	CHK
00000000	undefined	Initial		

REV	DATE	DESCRIPTION	BY	CHK
00000000	undefined	Initial		

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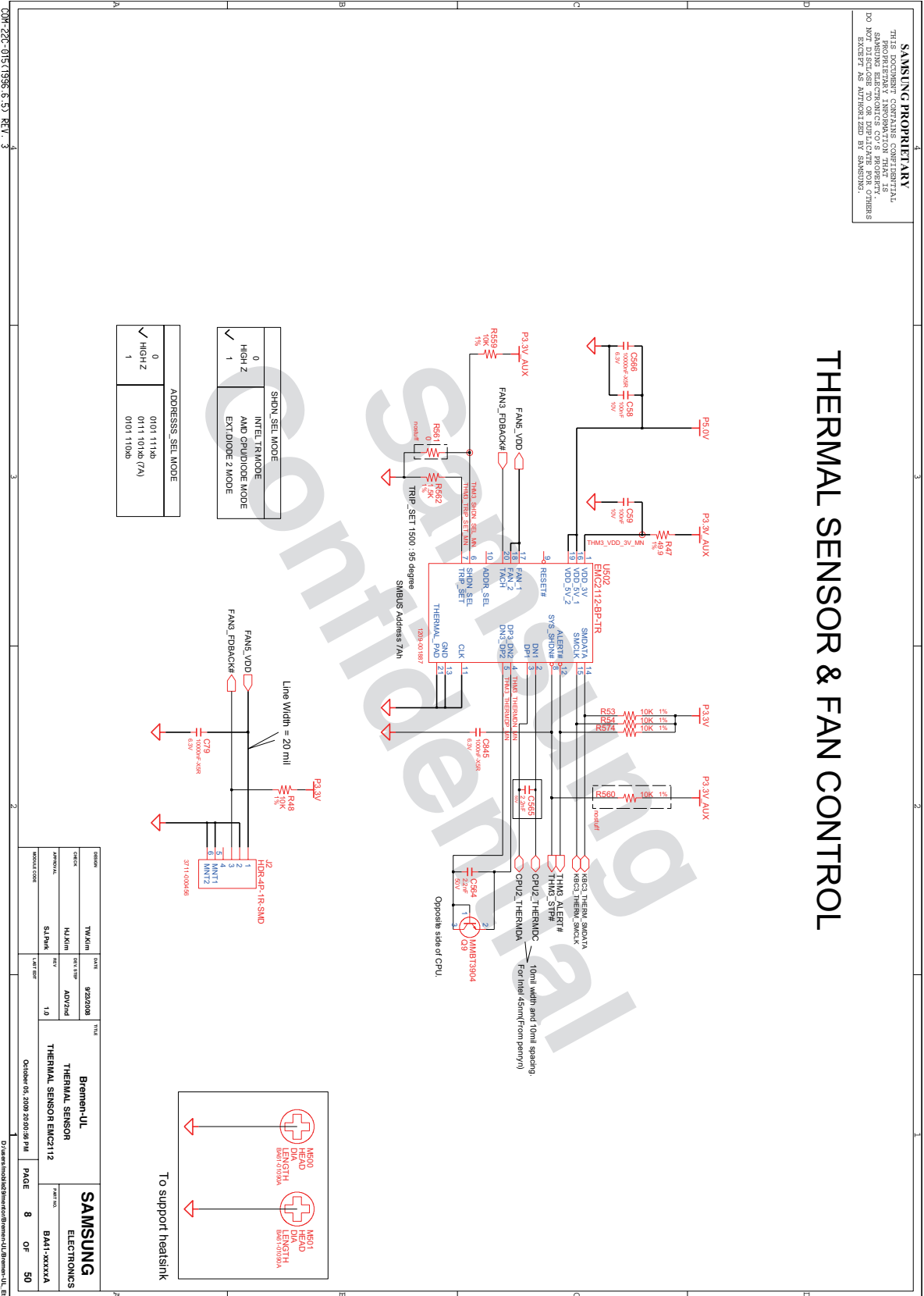
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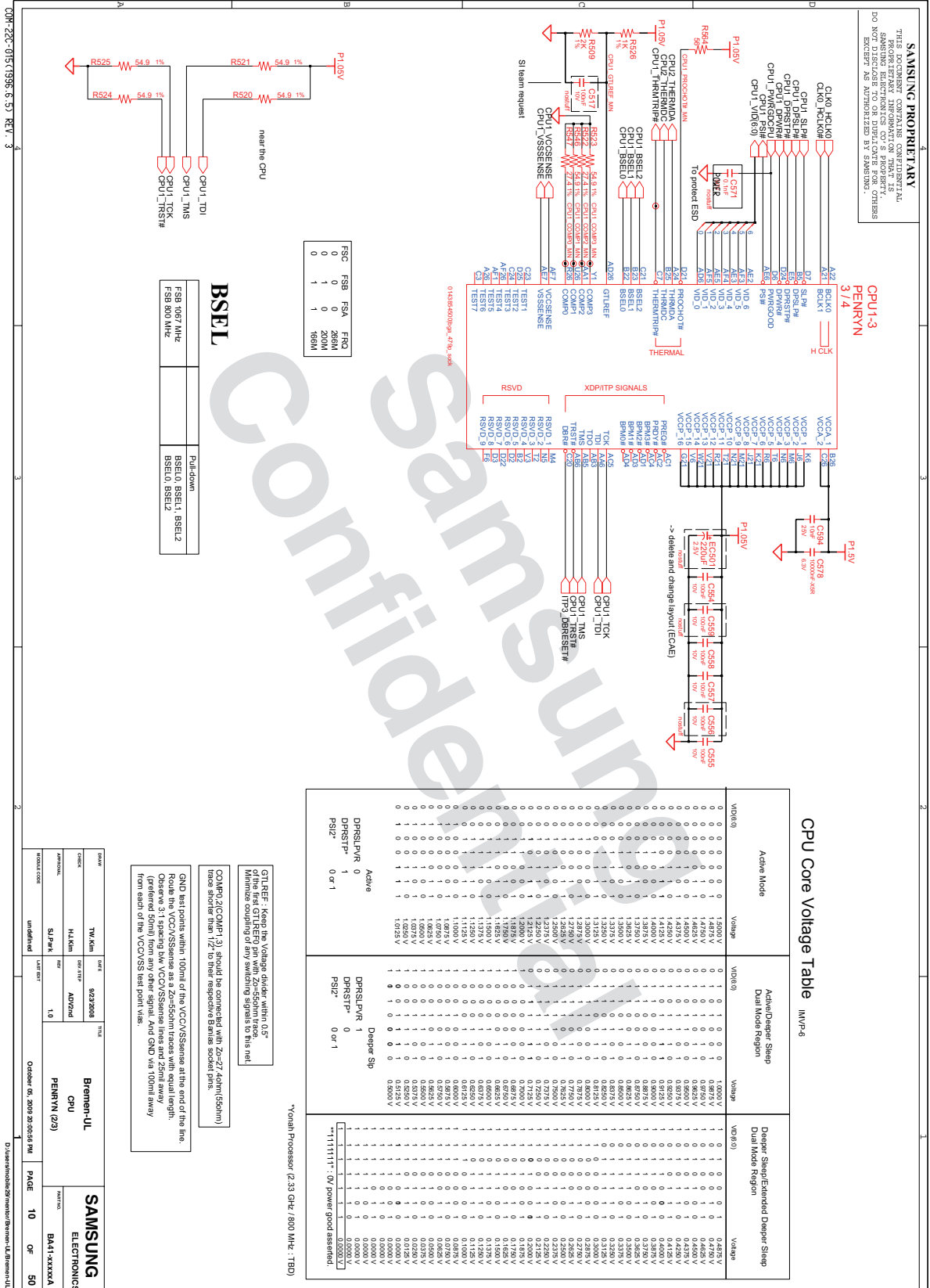






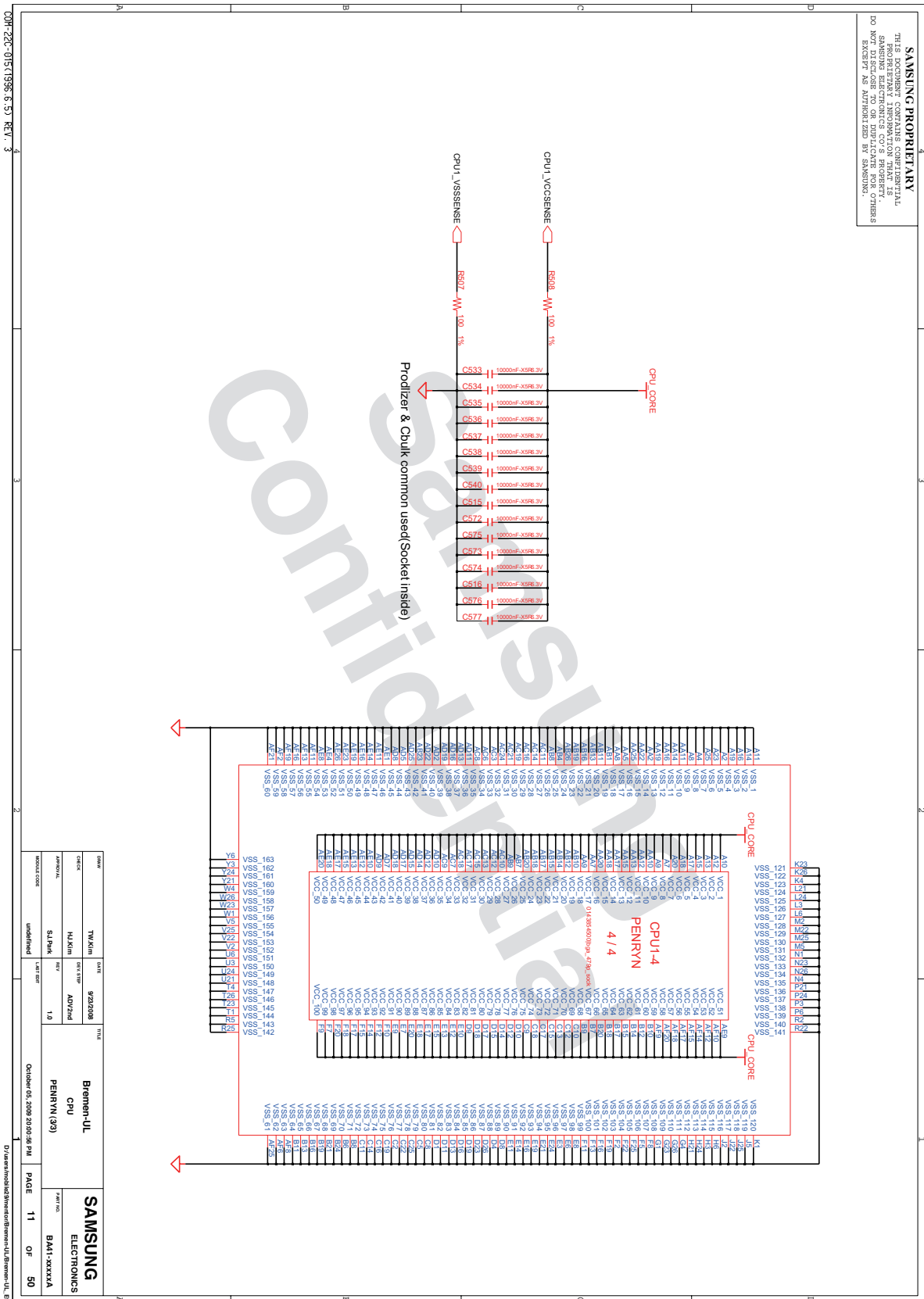
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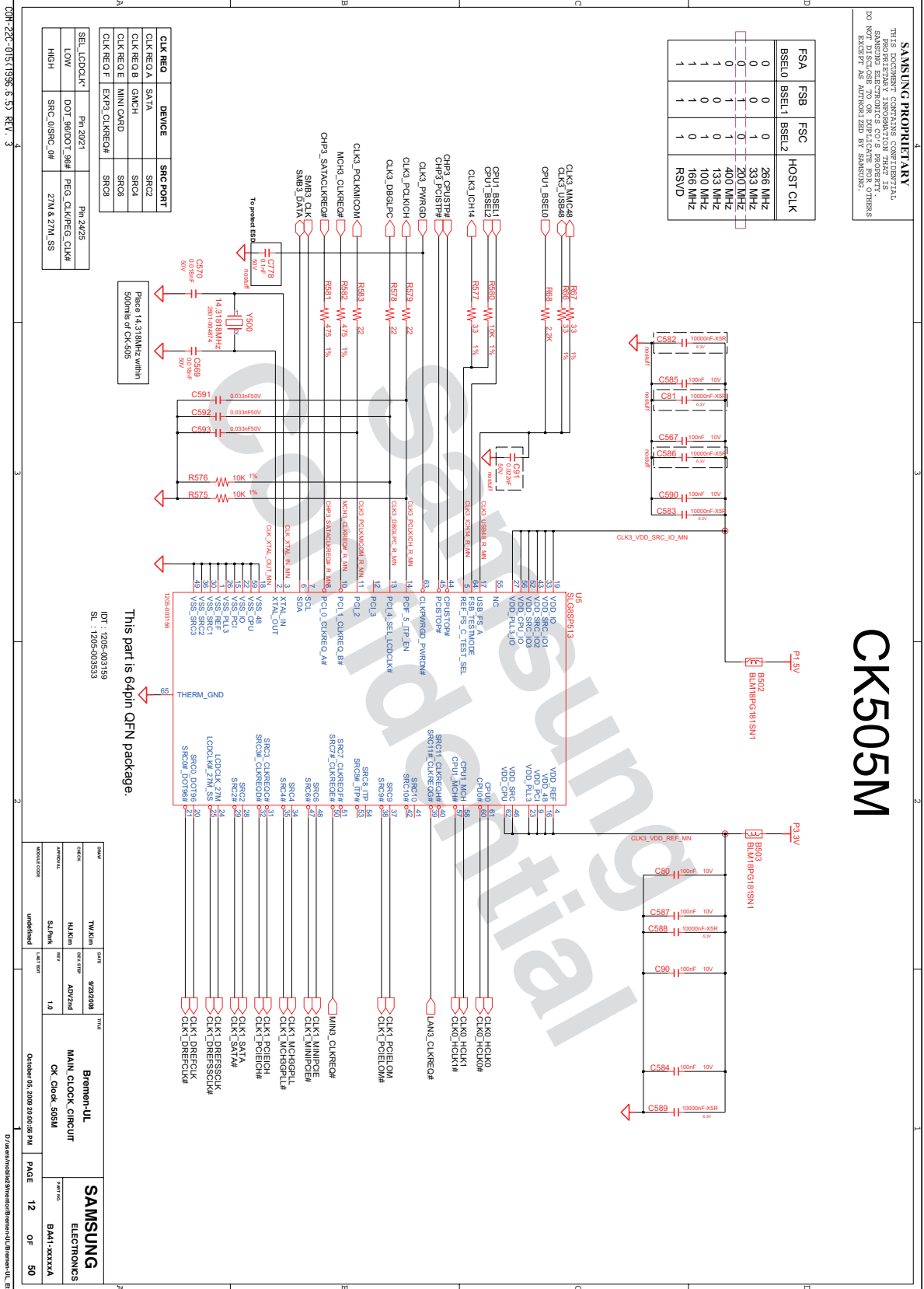
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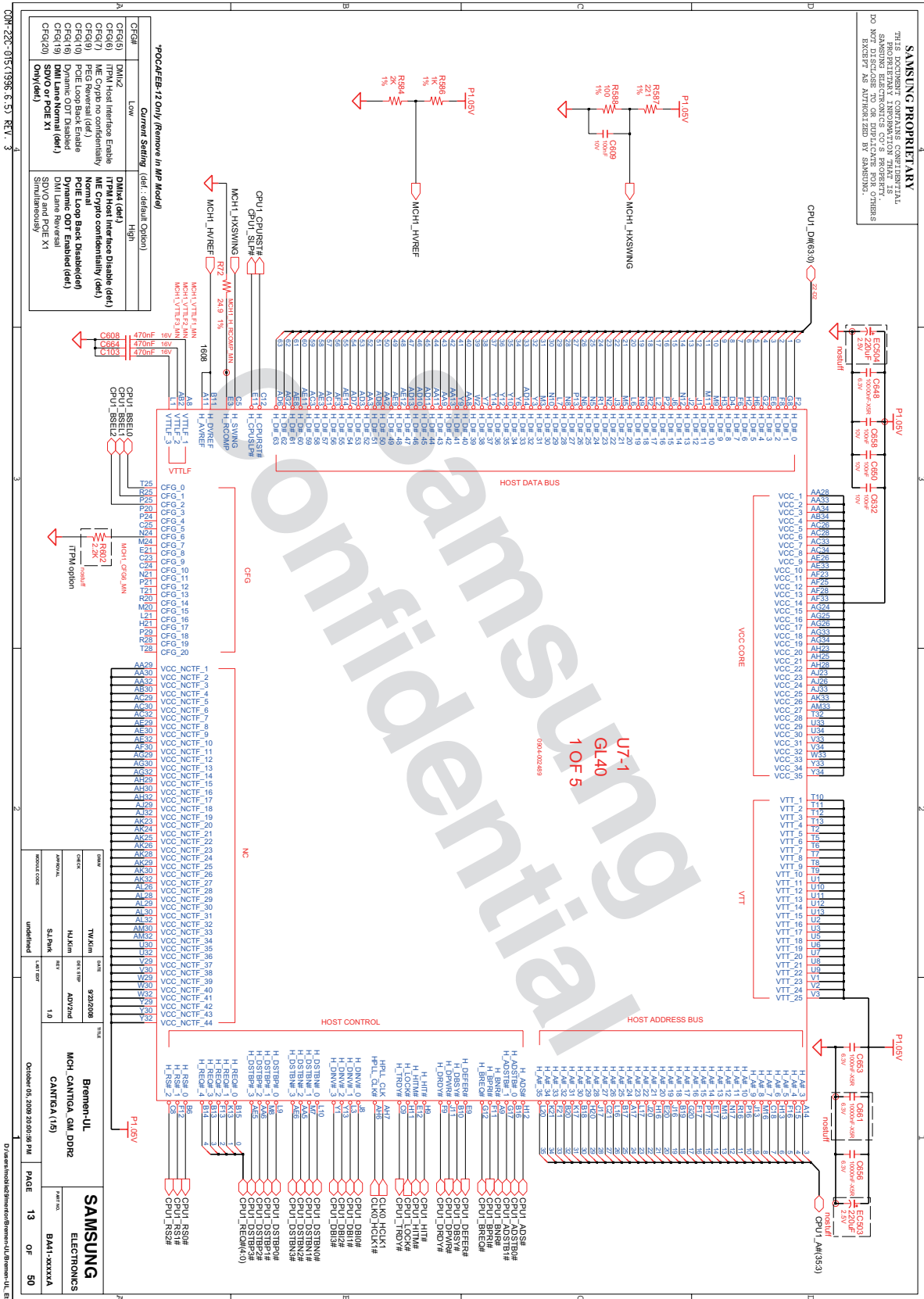
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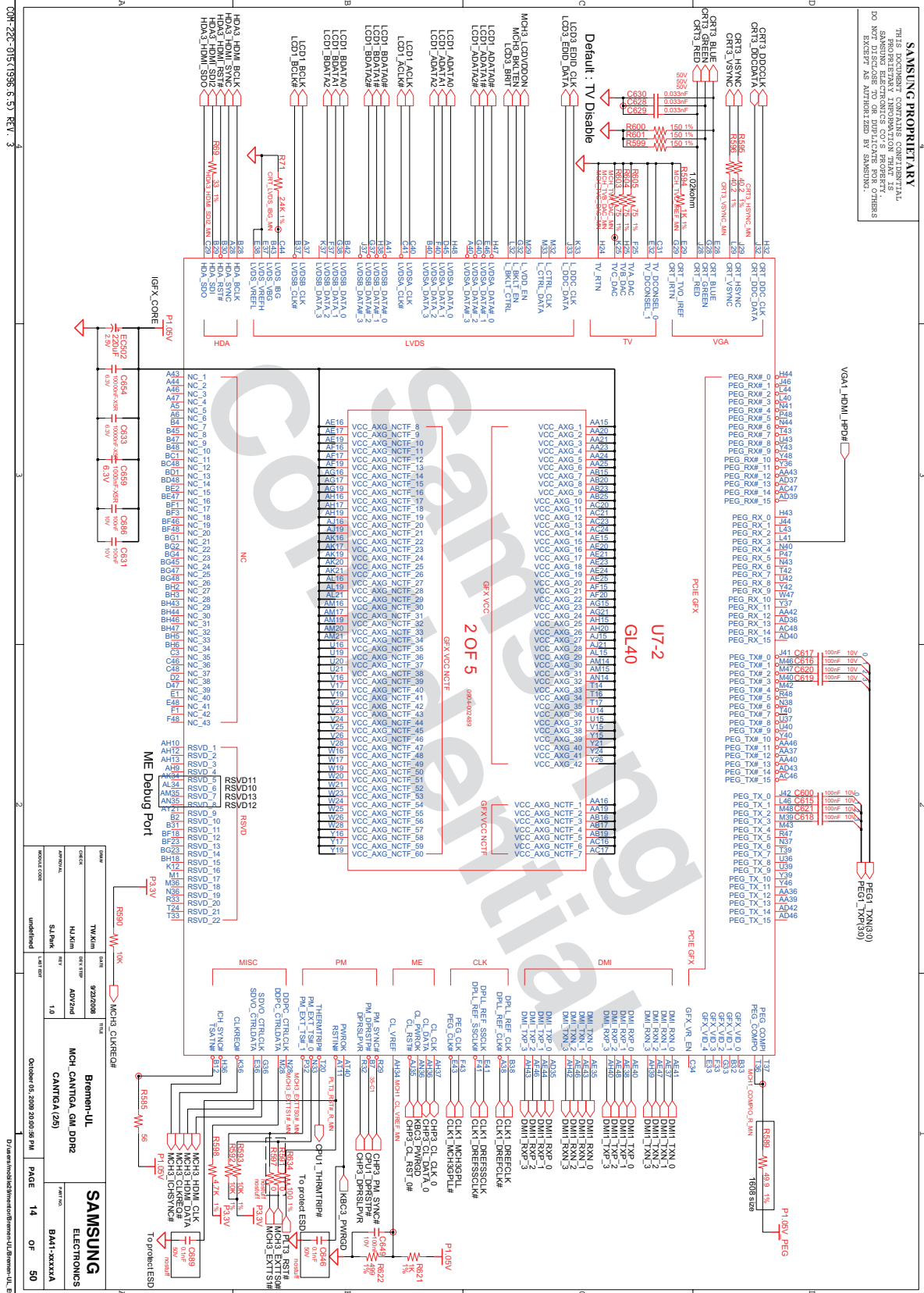
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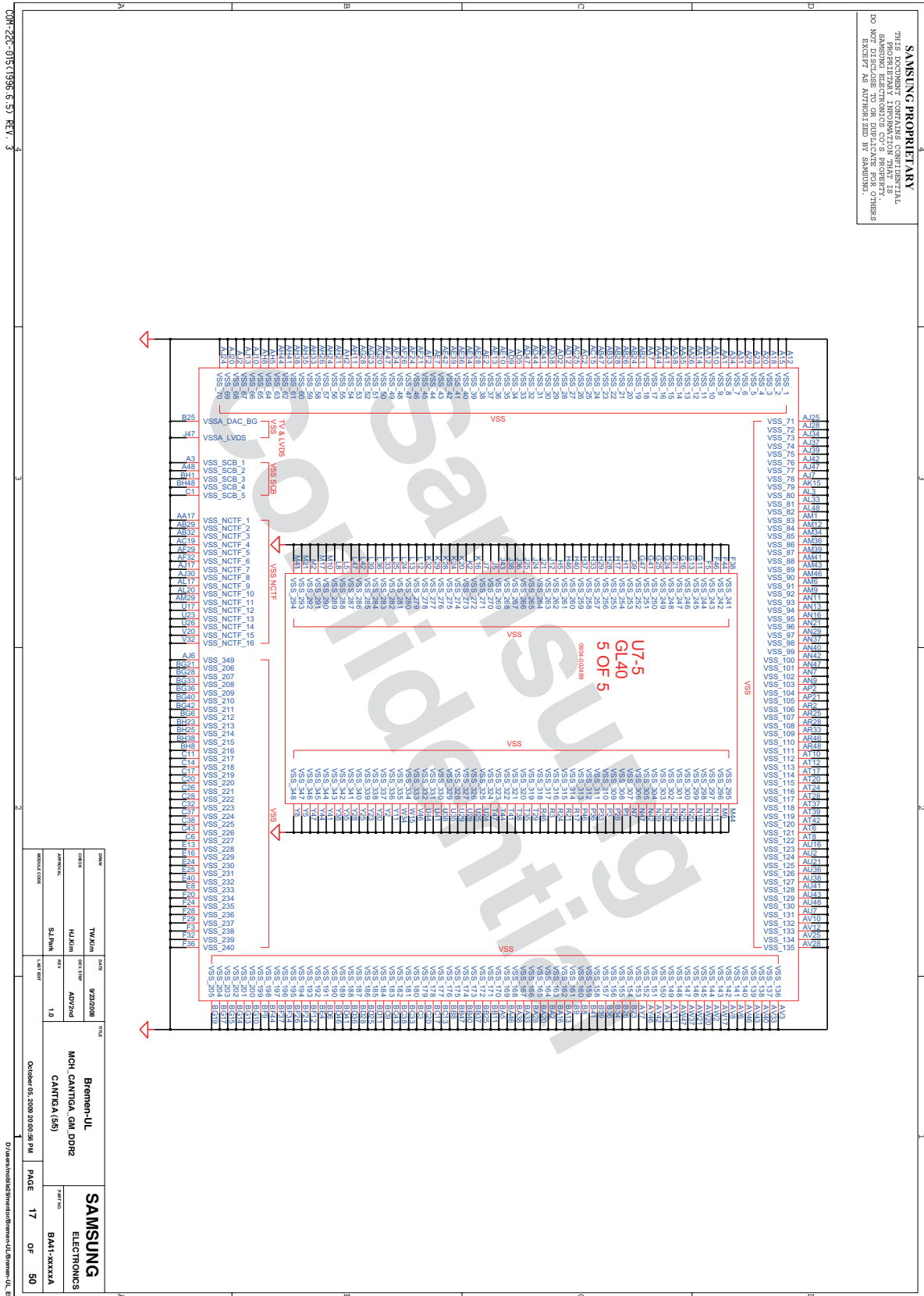






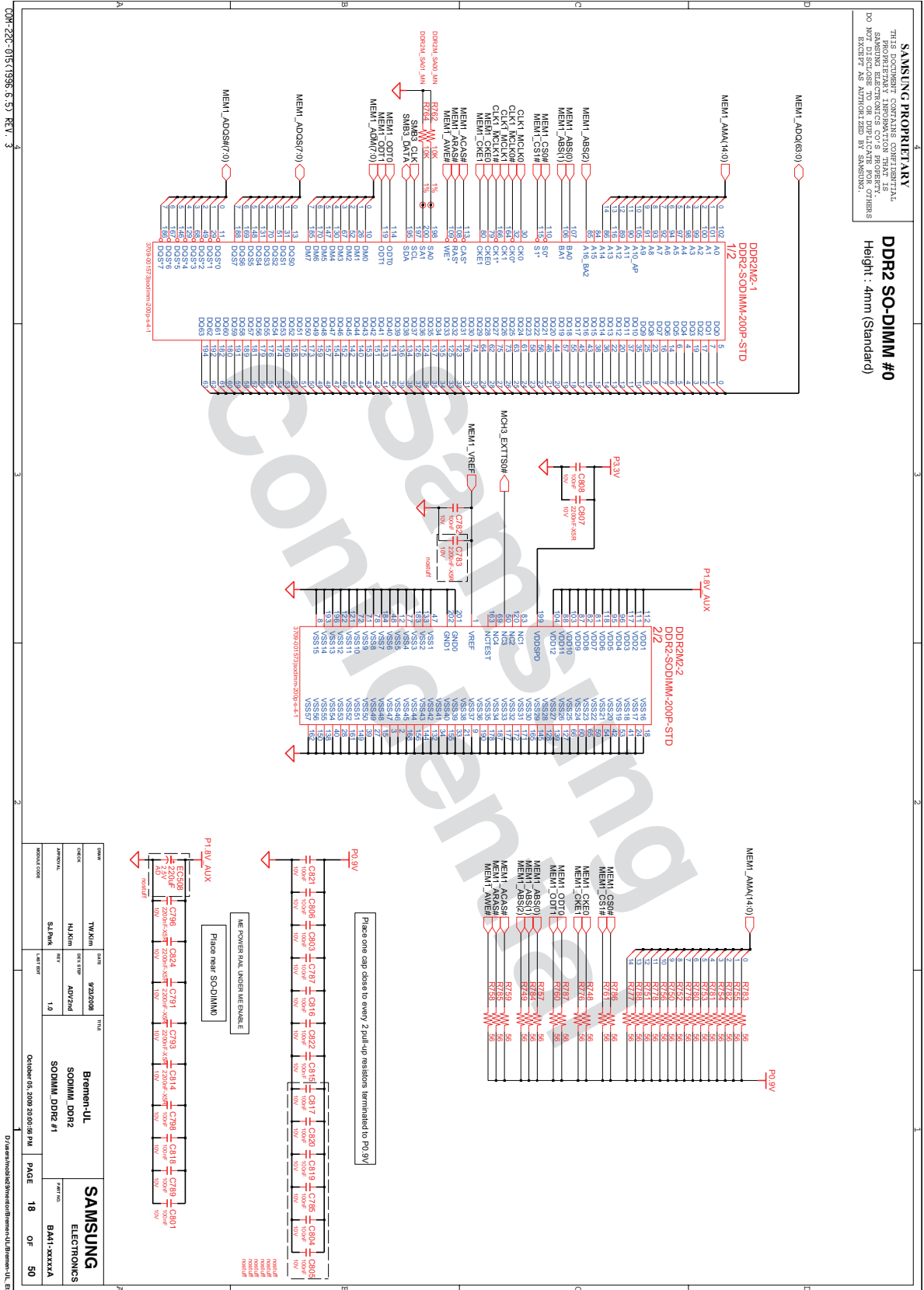
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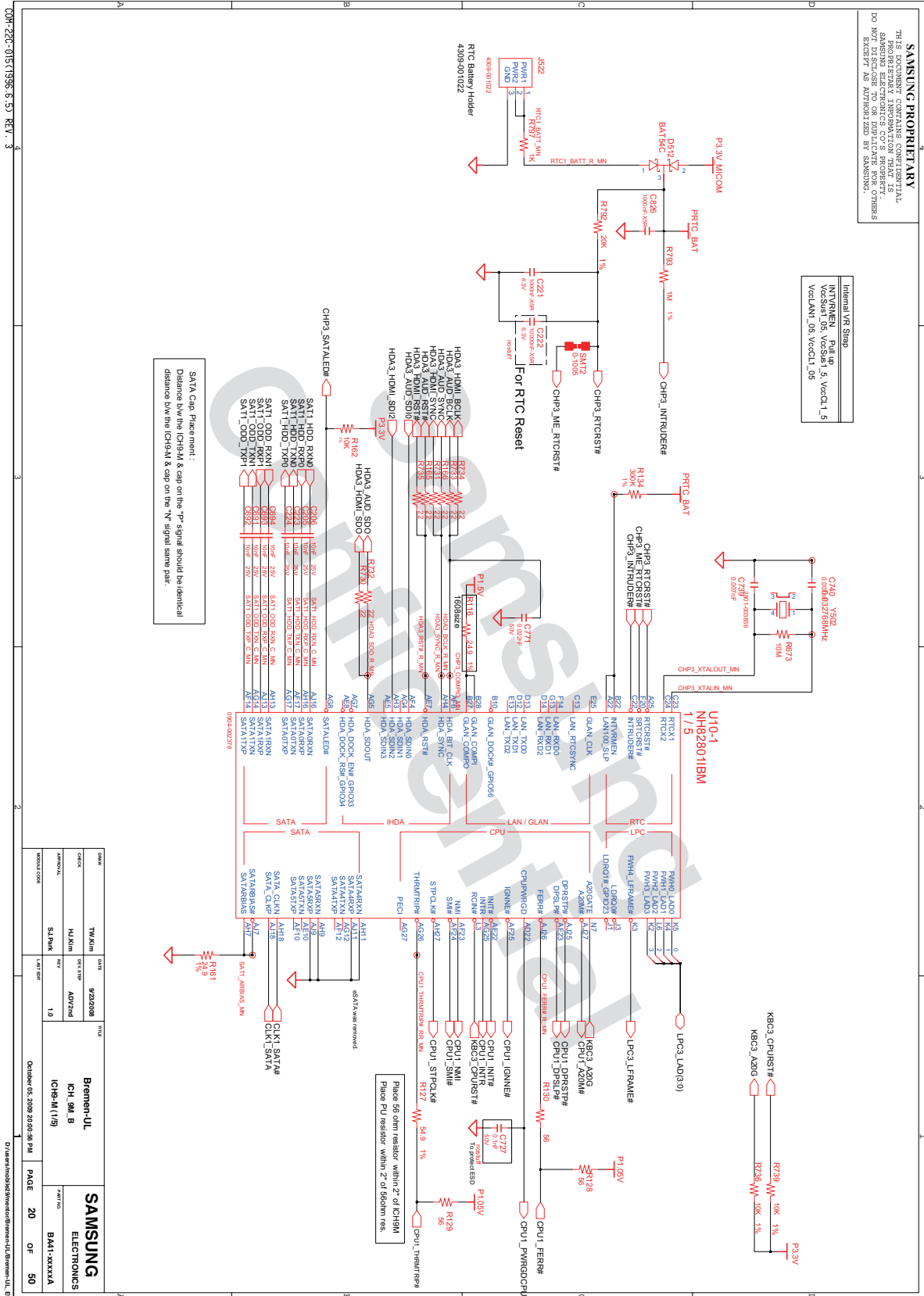
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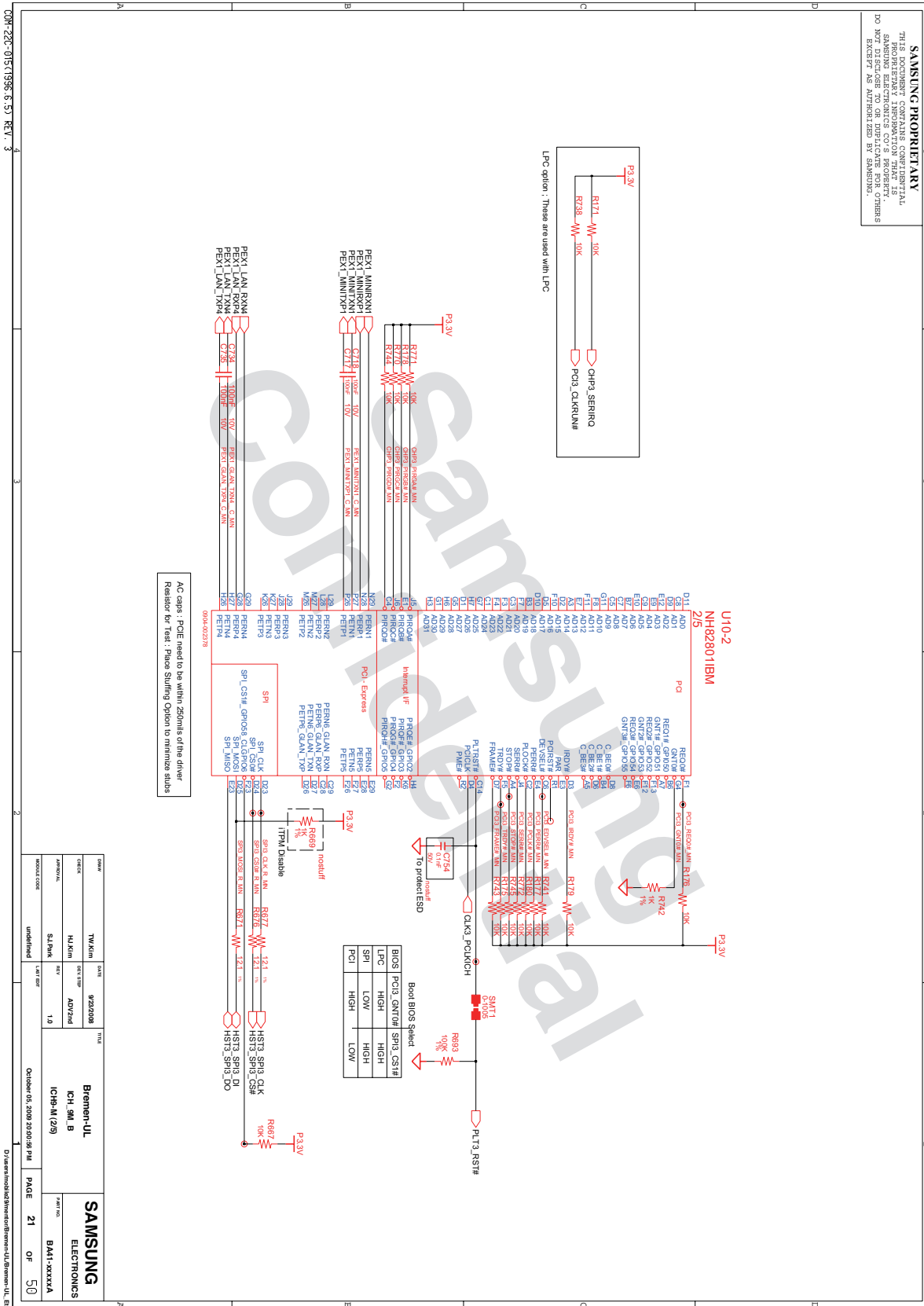
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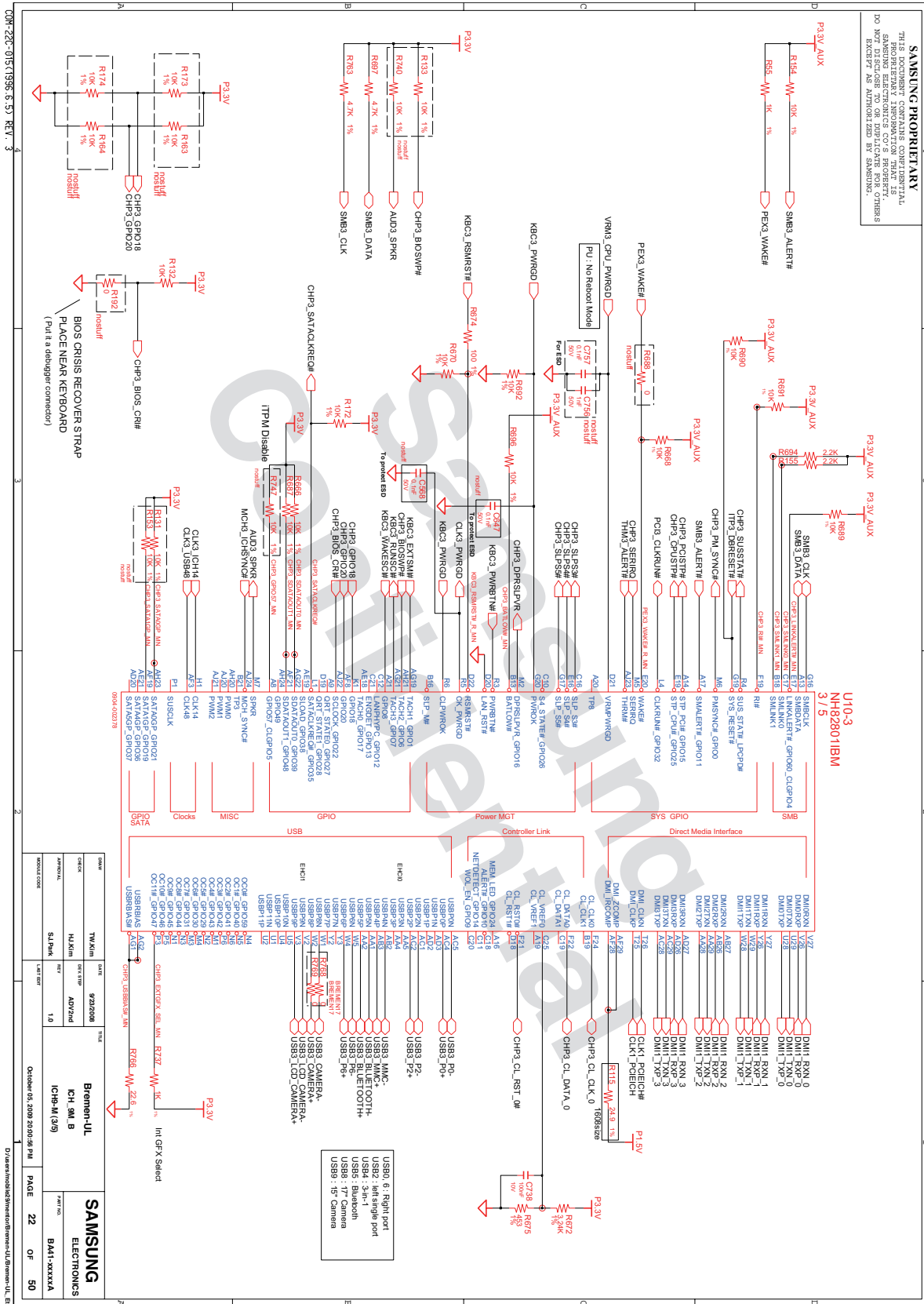
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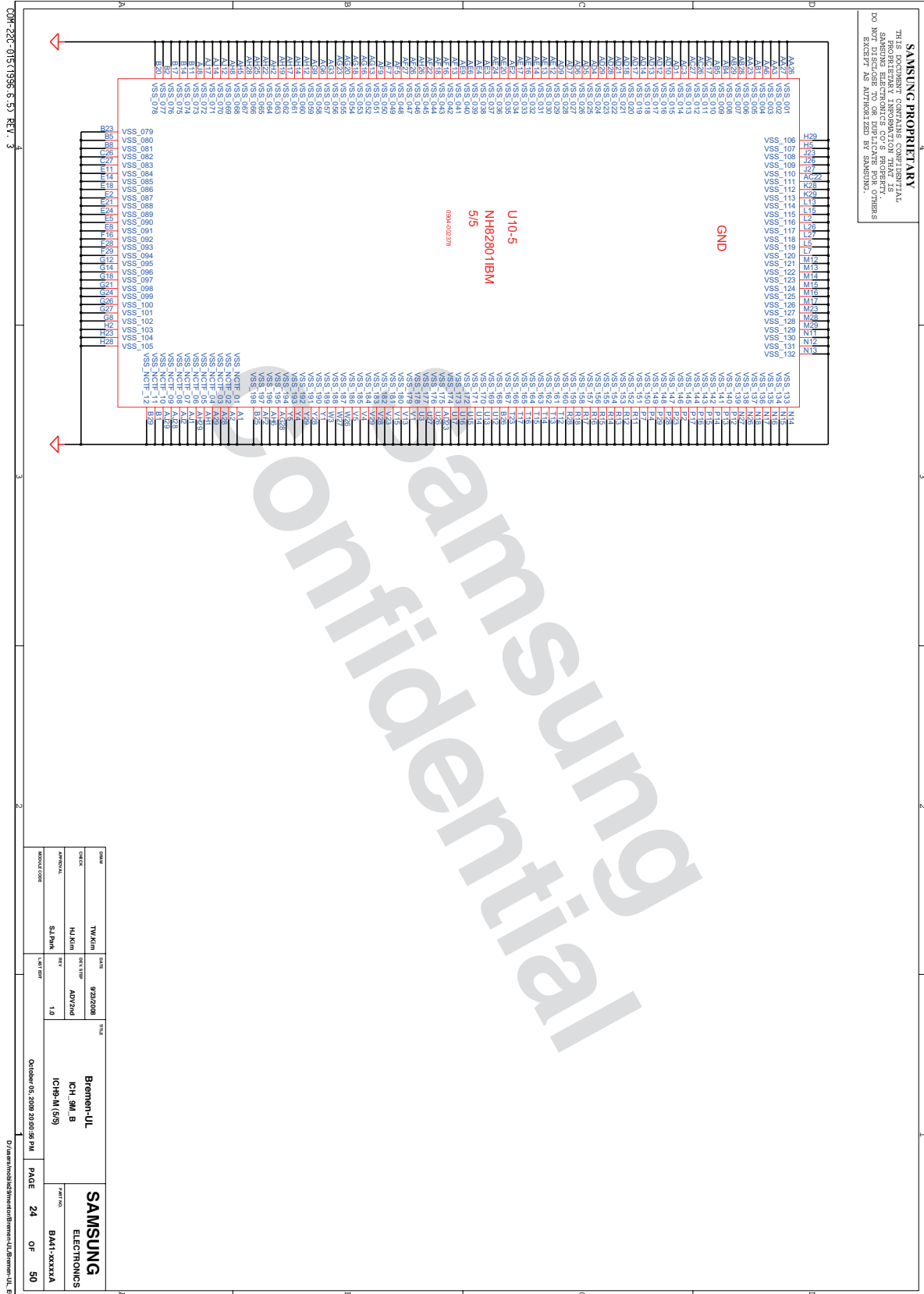
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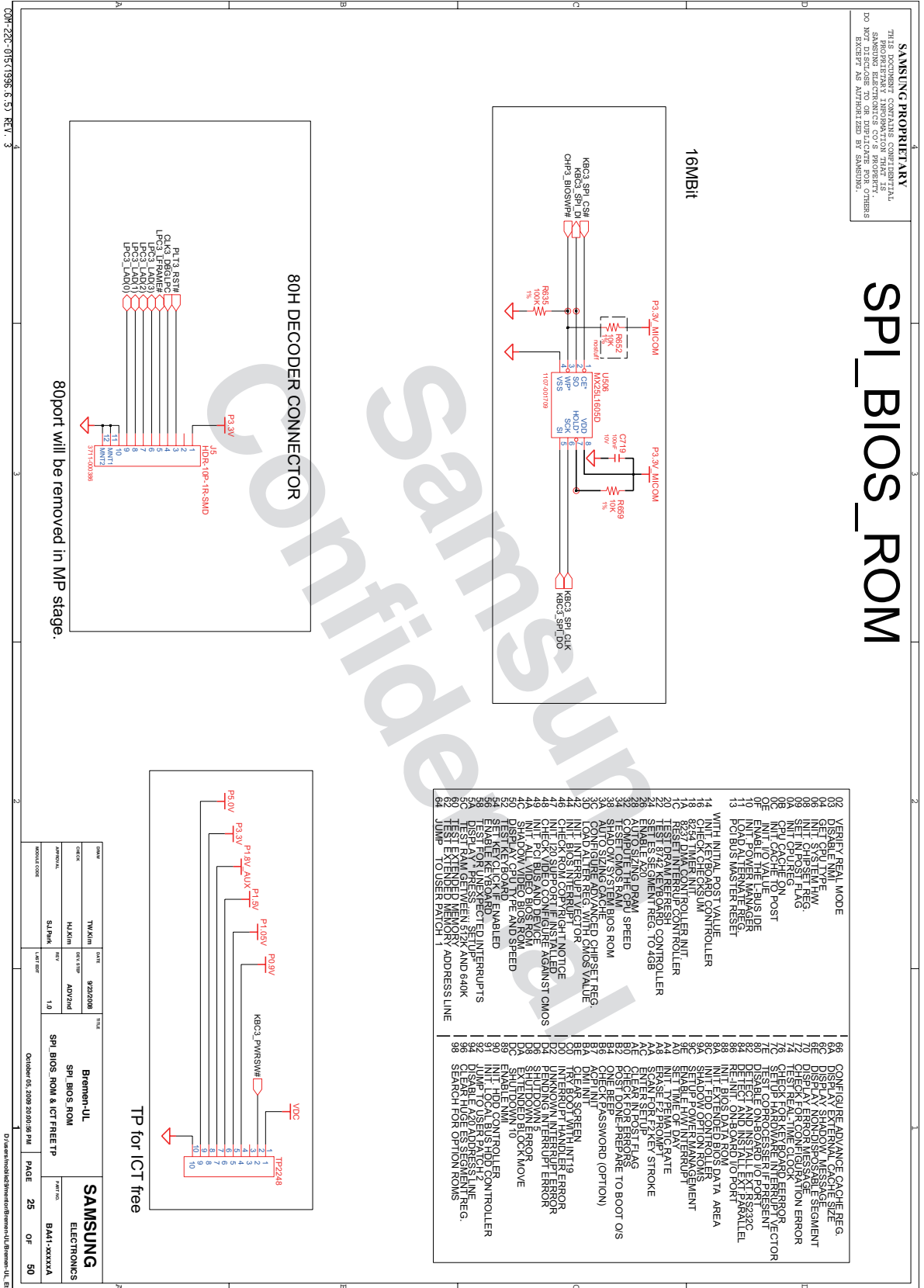
## 8. Block Diagram and Schematic





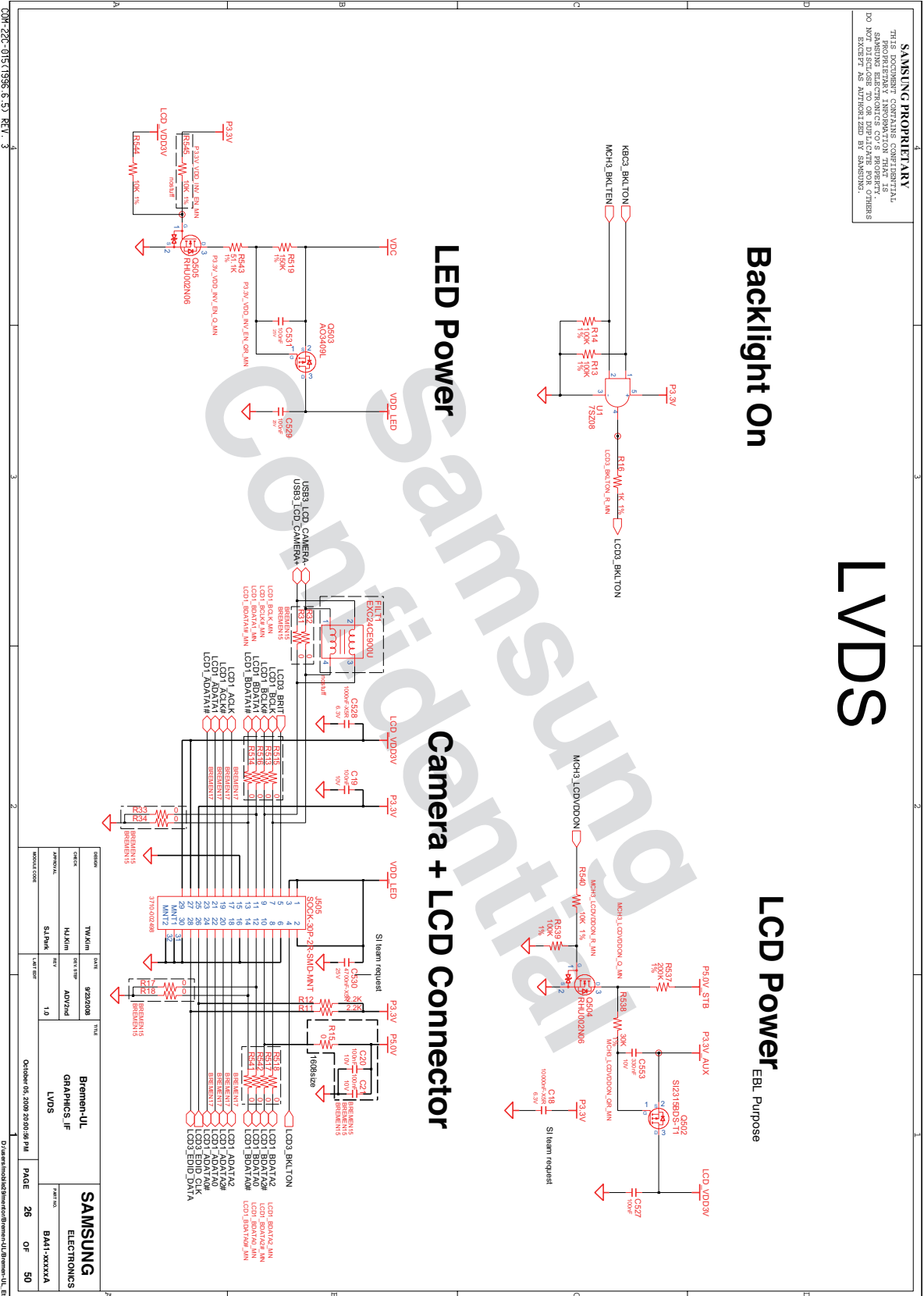
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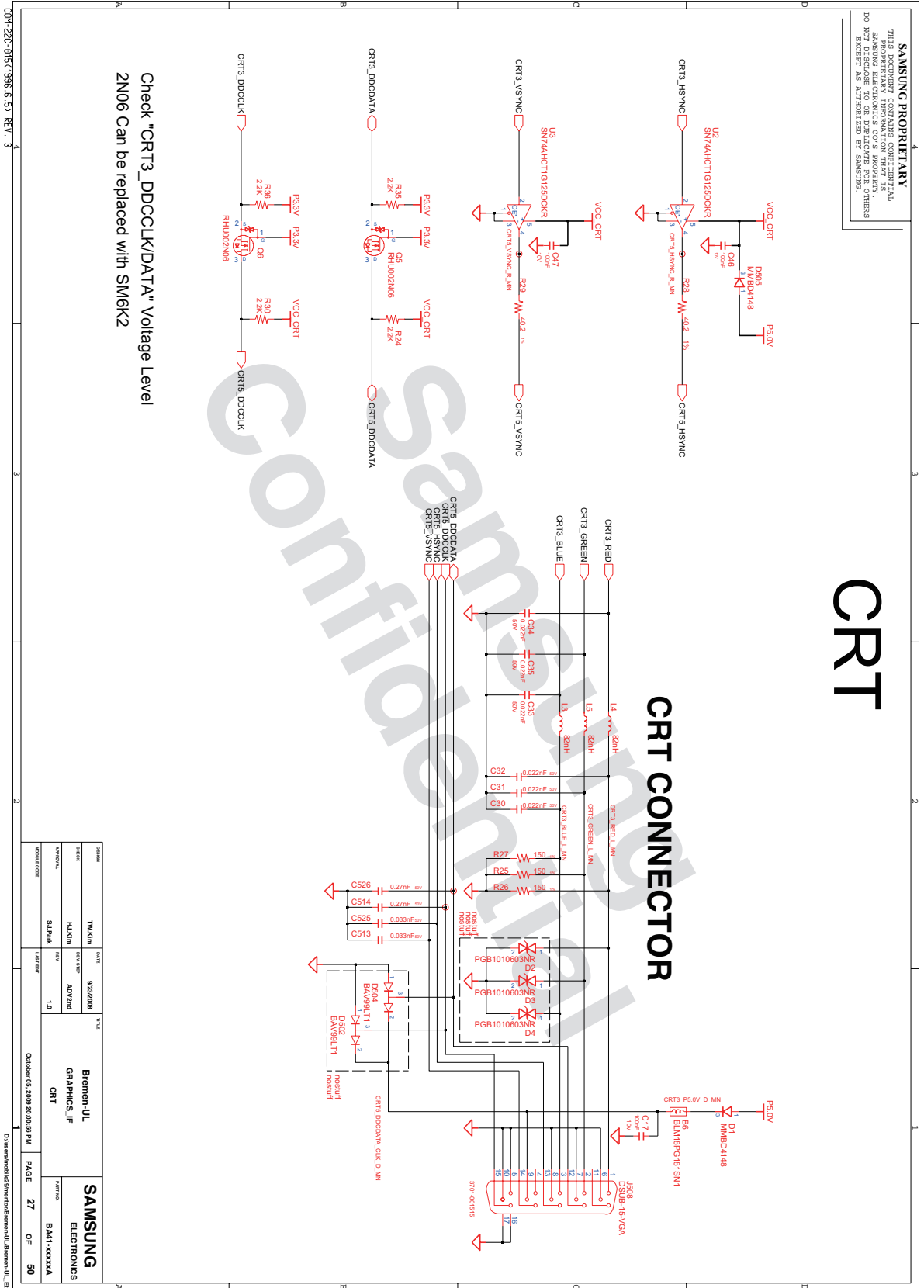
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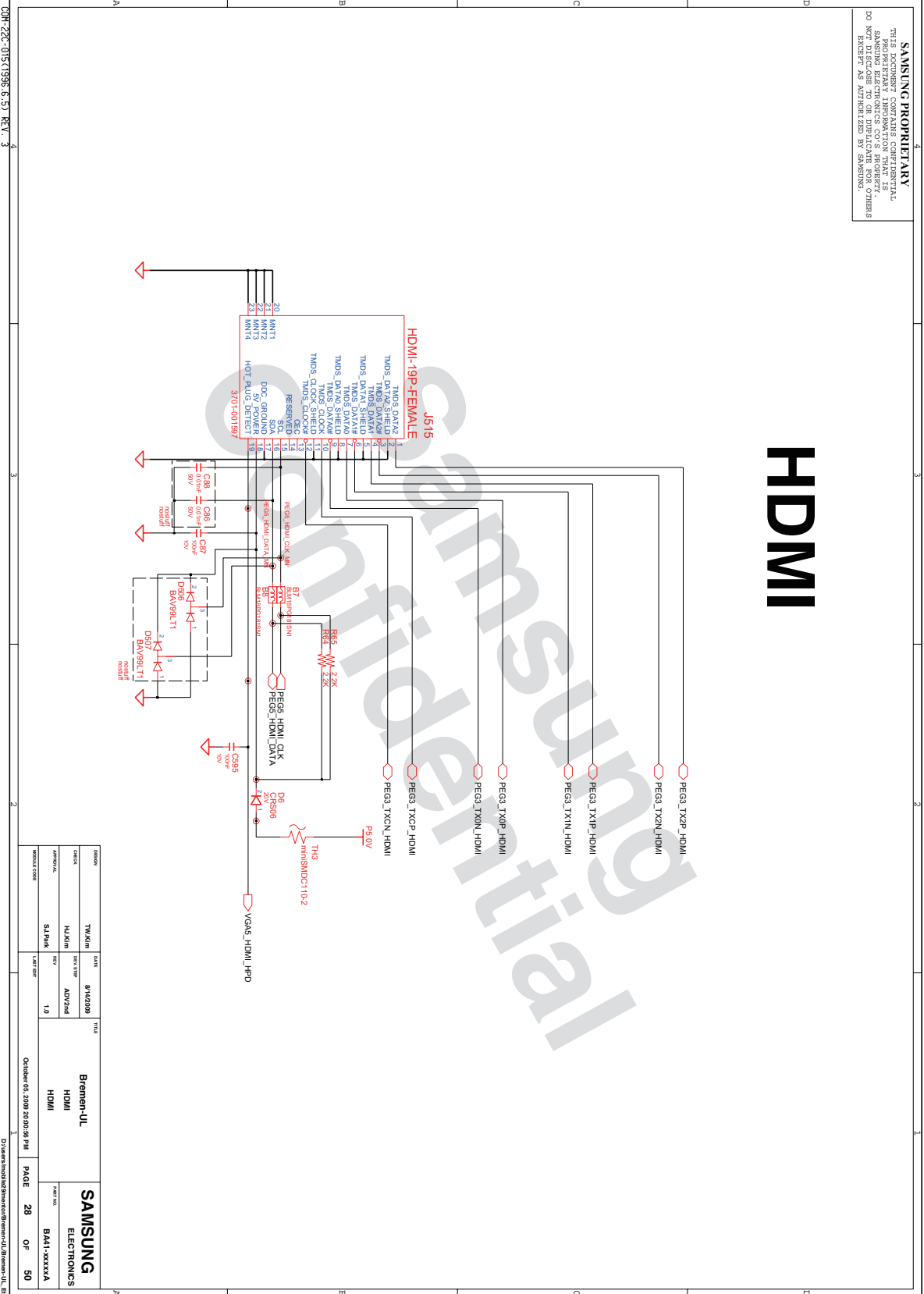
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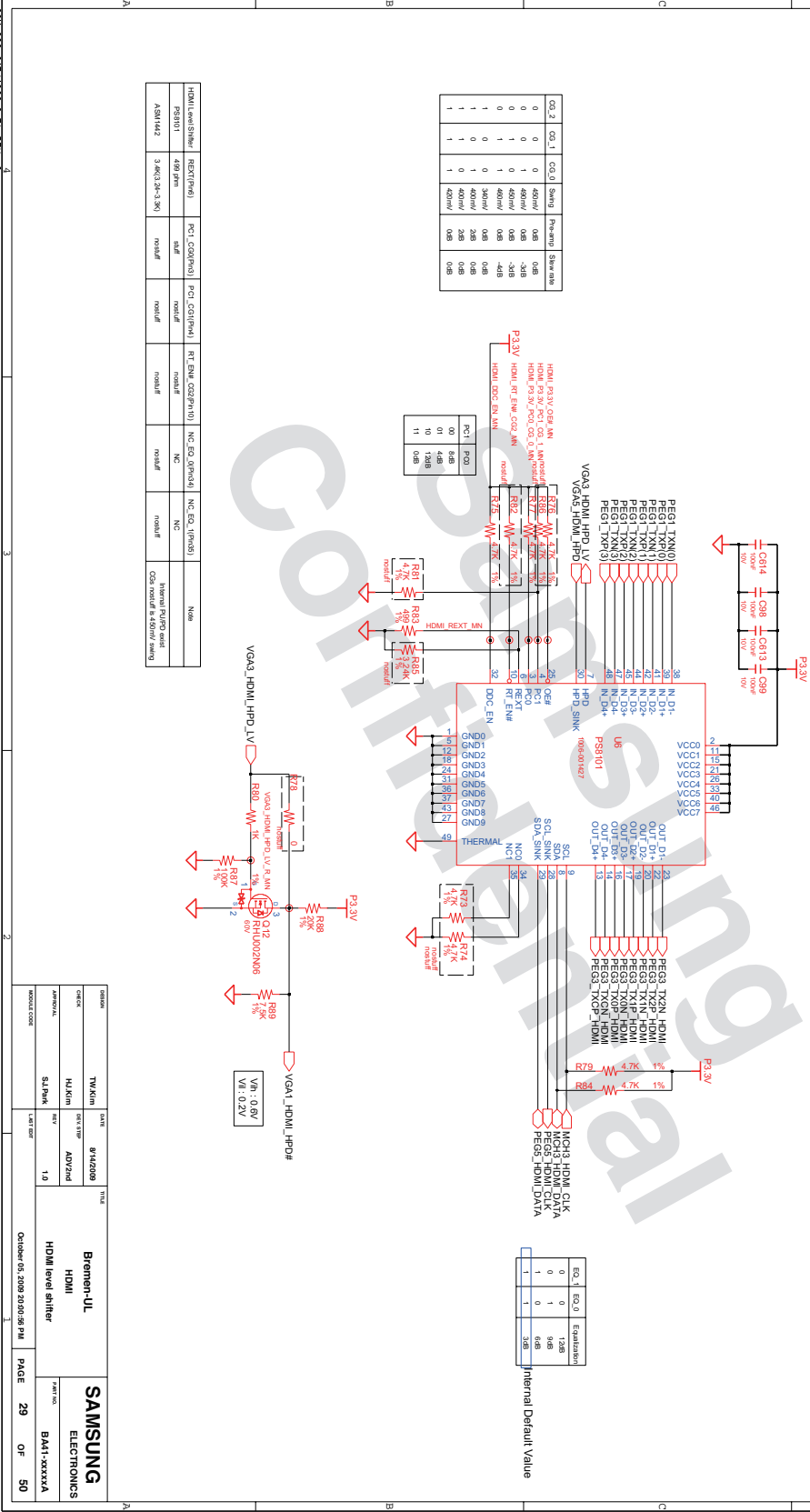


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# HDMI Level Shifter for Int. Graphic only



EQ.2	EQ.1	EQ.0	Swing	Priority	Sw. rate
0	0	1	400W	0x8	0x8
0	0	1	400W	0x8	3x8
0	1	0	400W	0x8	2x8
0	1	0	300W	0x8	0x8
1	0	1	400W	2x8	0x8
1	0	1	400W	2x8	0x8
1	1	1	400W	0x8	0x8

EQ.1	EQ.0	Sw. rate
0	1	0x8
0	1	3x8
1	0	0x8
1	1	0x8

EQ.1	EQ.0	Sw. rate
0	1	0x8
0	1	3x8
1	0	0x8
1	1	0x8

Internal Default Value

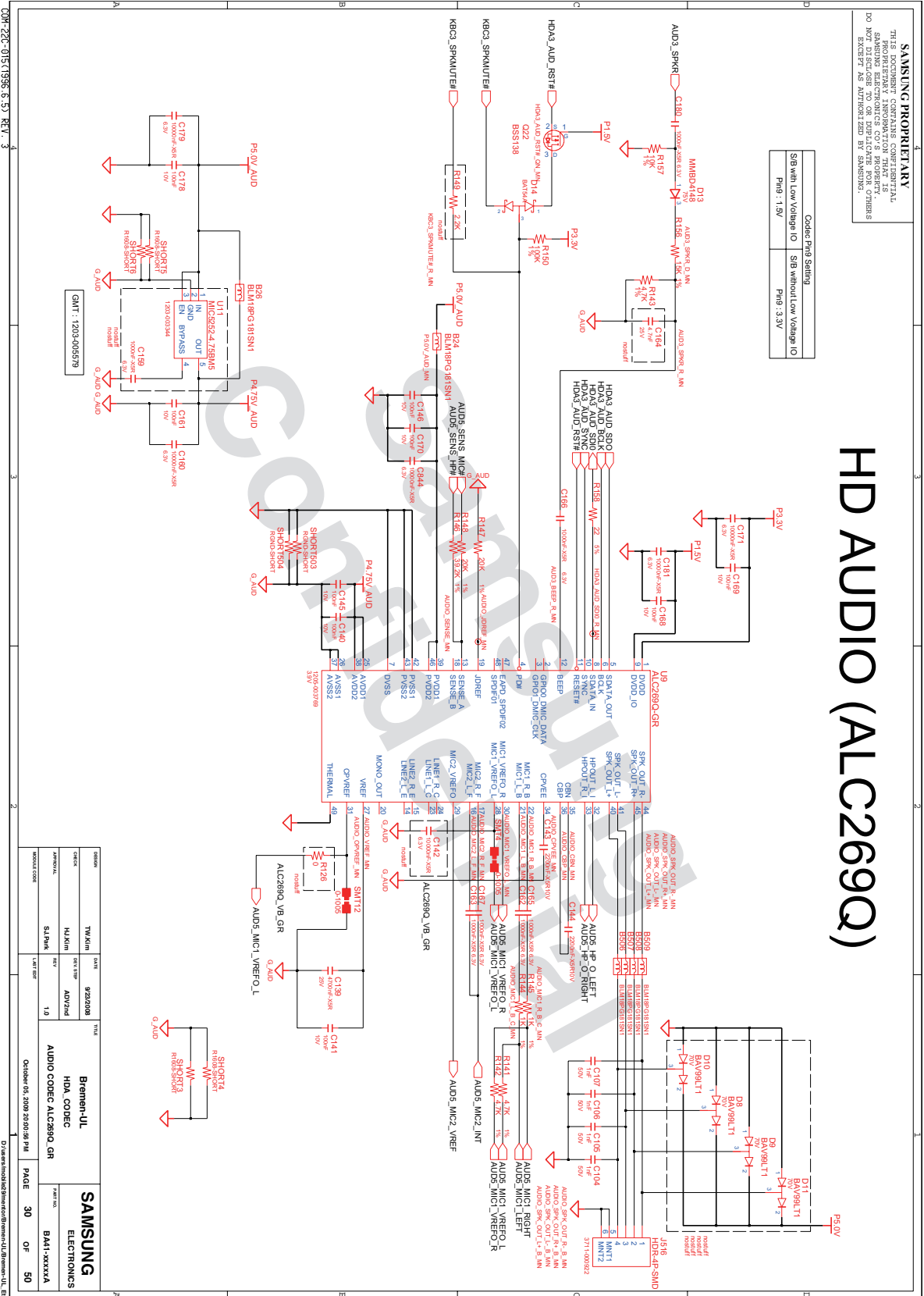
HSMT (low SW)	HSMT (high)	PCI_C00 (low)	PCI_C00 (high)	RT_SMT_C00 (P10)	NC_EQ_0 (P10)	NC_EQ_1 (P10)	NC	NC
ASMT142	3x8(2x3-3x)	low	low	low	low	low	low	low

COB-22C-015(1996:6.5) REV. 3

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 October 01, 2009 2:00:56 PM PAGE 29 OF 50  
 Revision: 1.0  
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## HD AUDIO (ALC269Q)

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Code: Pkg Setting	SIB without Low Voltage ID
Pkg: 1.9V	Pkg: 3.3V

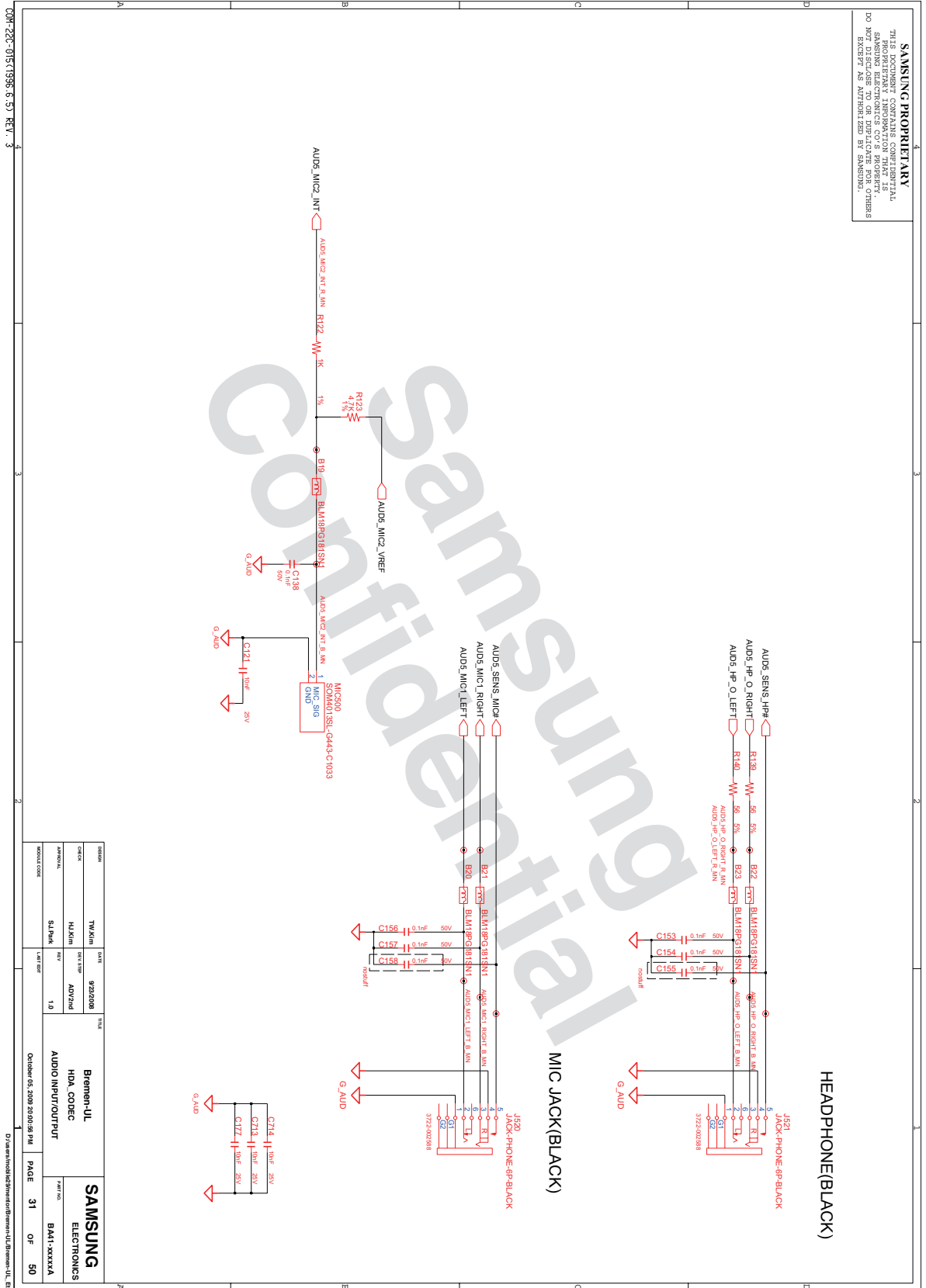
00P-226-015(1)S96.6.57 REV. 3

DESIGN	DATE	TIME	DESIGNER	DATE	TIME
TWAKIN	9/23/2008		Bremen-UL		
CHEK	9/23/2008		HD CODEC		
APRVAL	ADV2P2		AUDIO CODEC ALC269Q_GR		
SLFRNK	1.0				
WORK CODE					
DATE REV					
October 06, 2008 20:08:38 Pkt	PAGE	30	OF	50	

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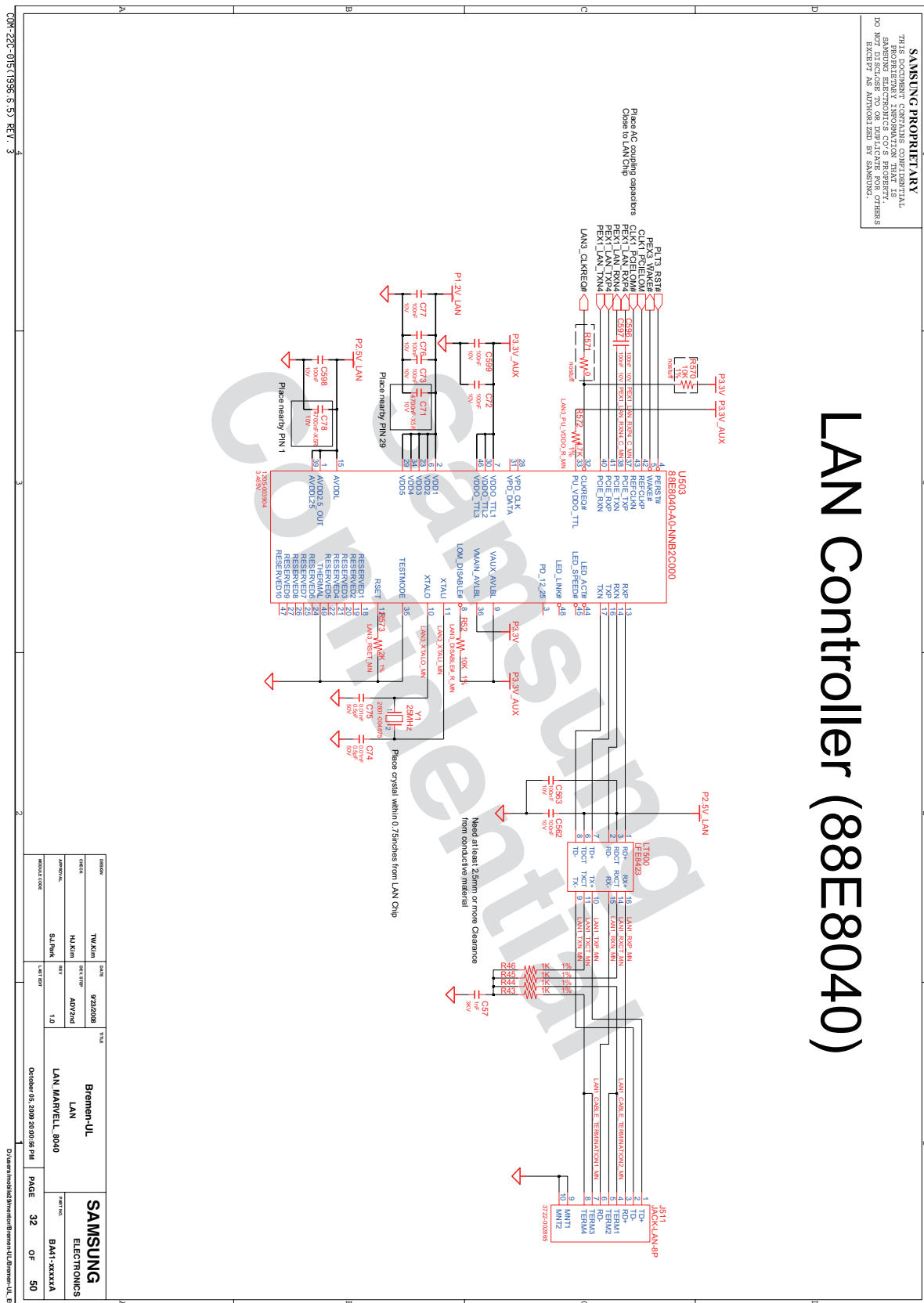


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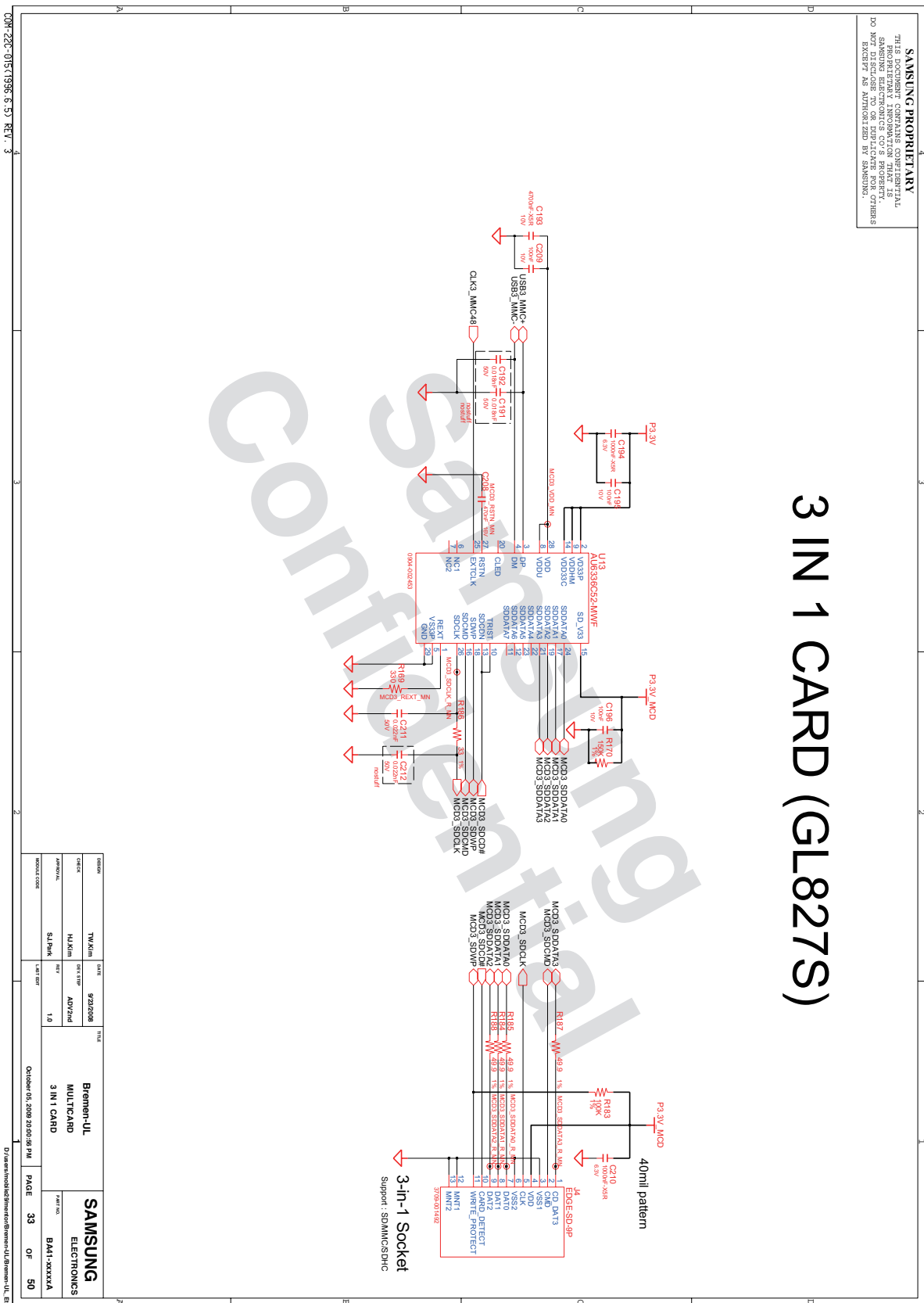
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## LAN Controller (88E8040)



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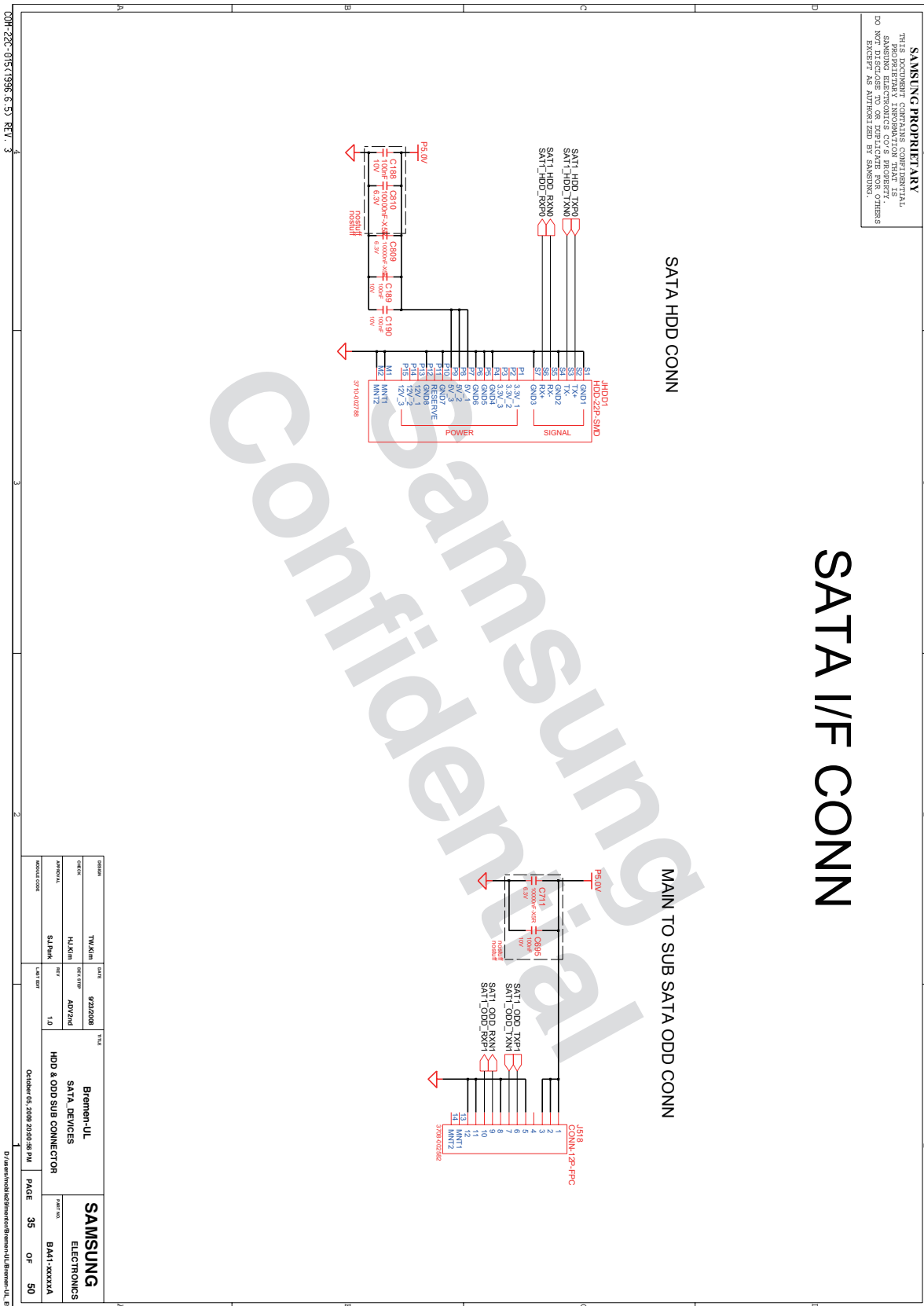
## 8. Block Diagram and Schematic





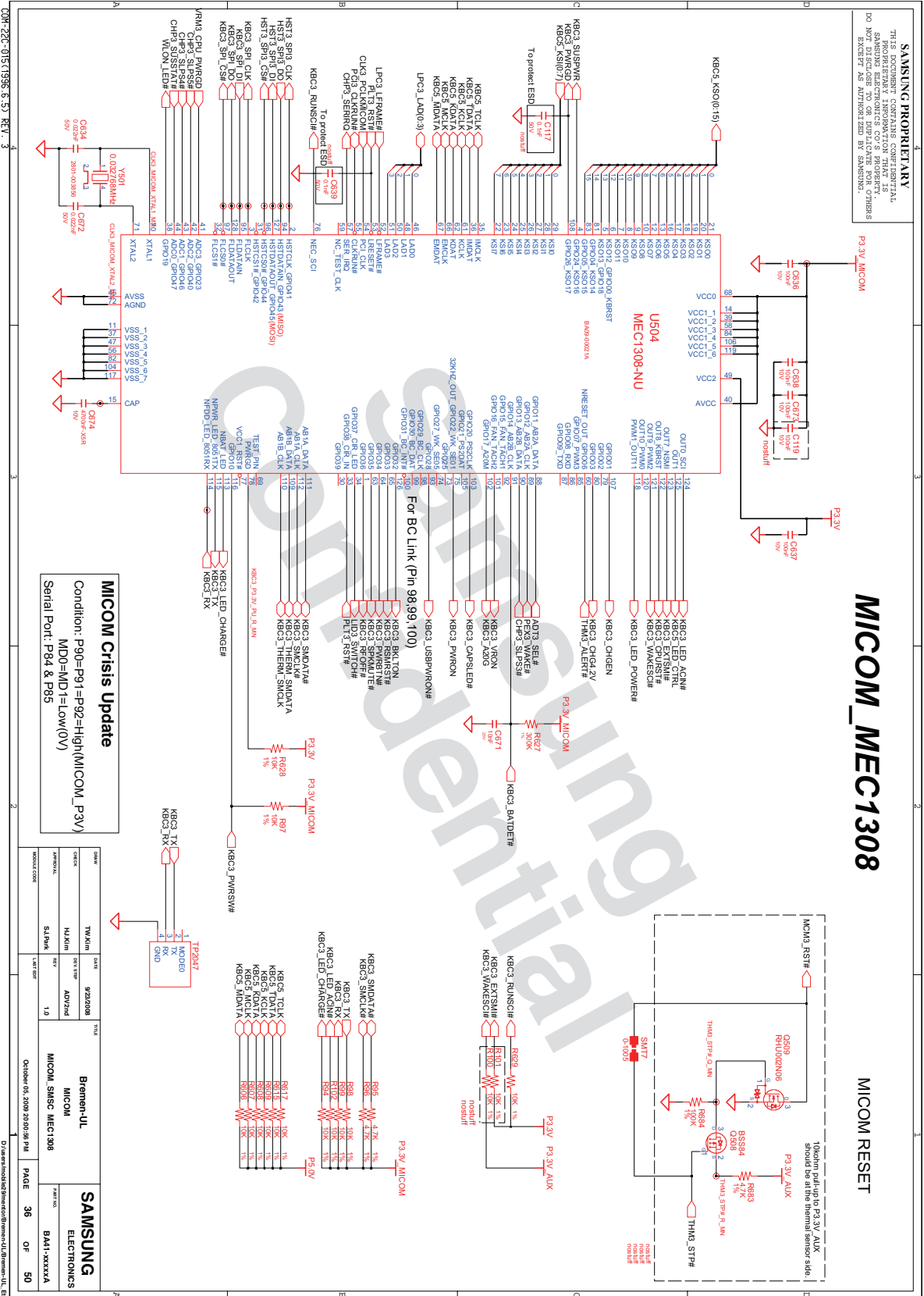
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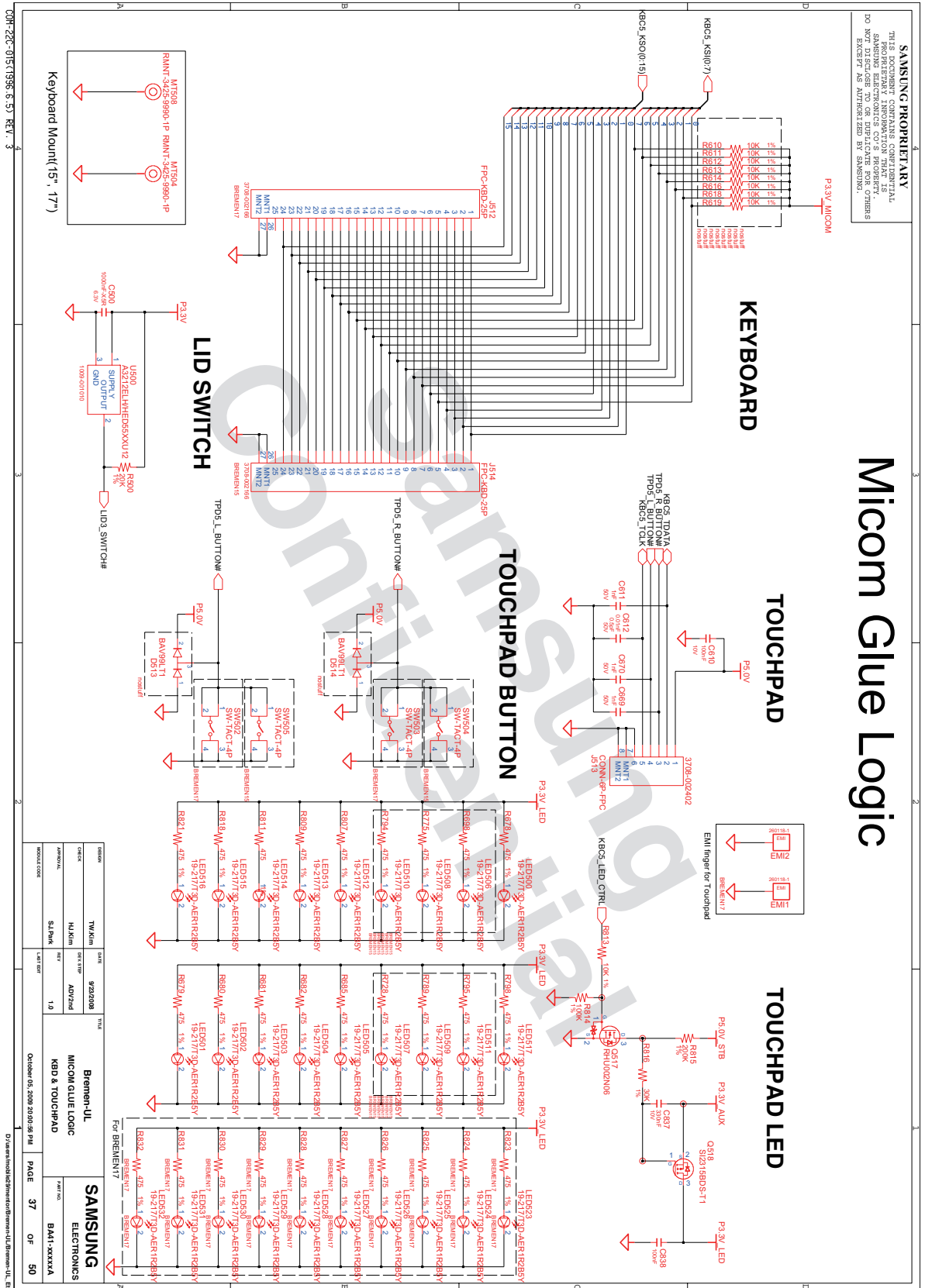
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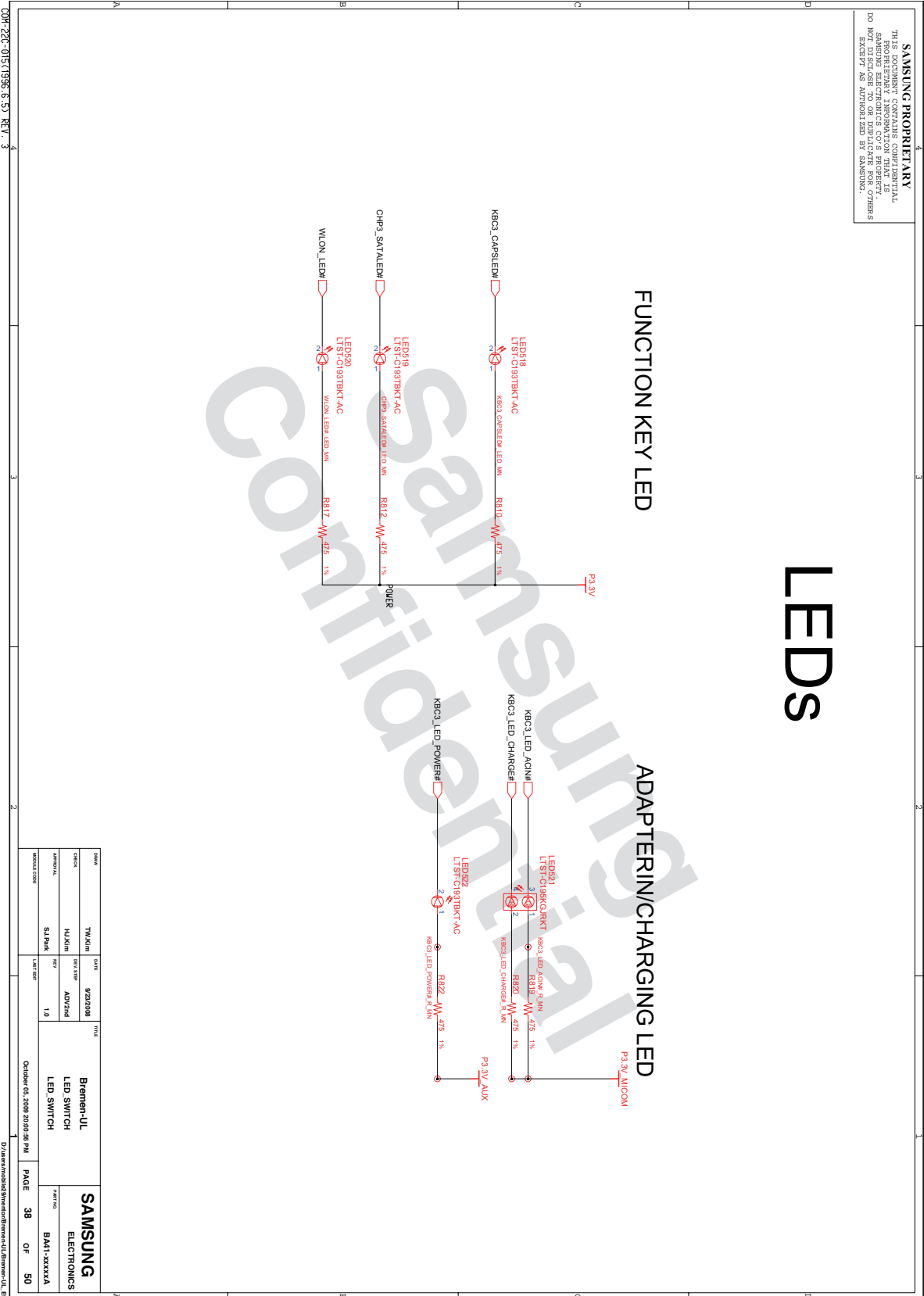
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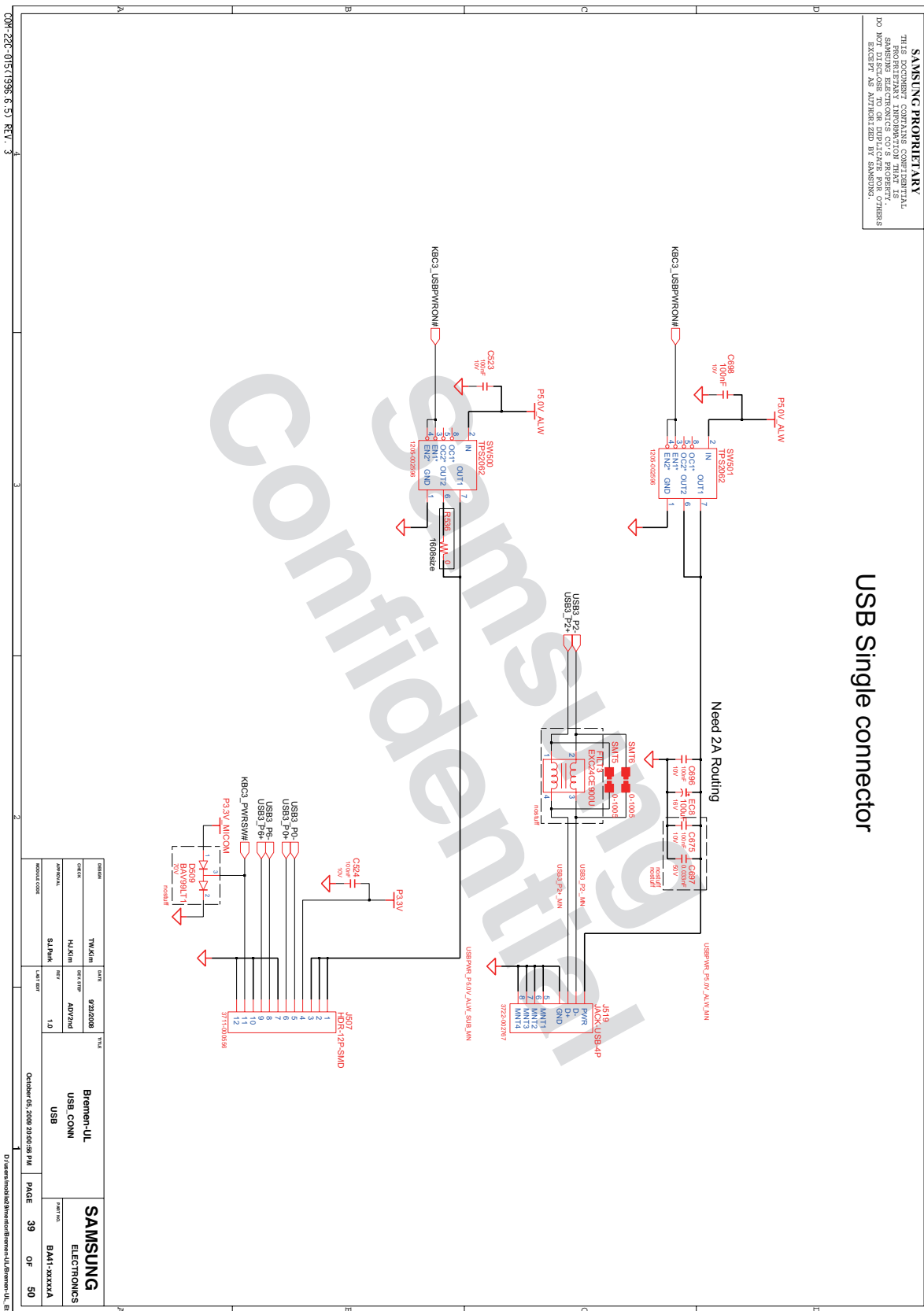
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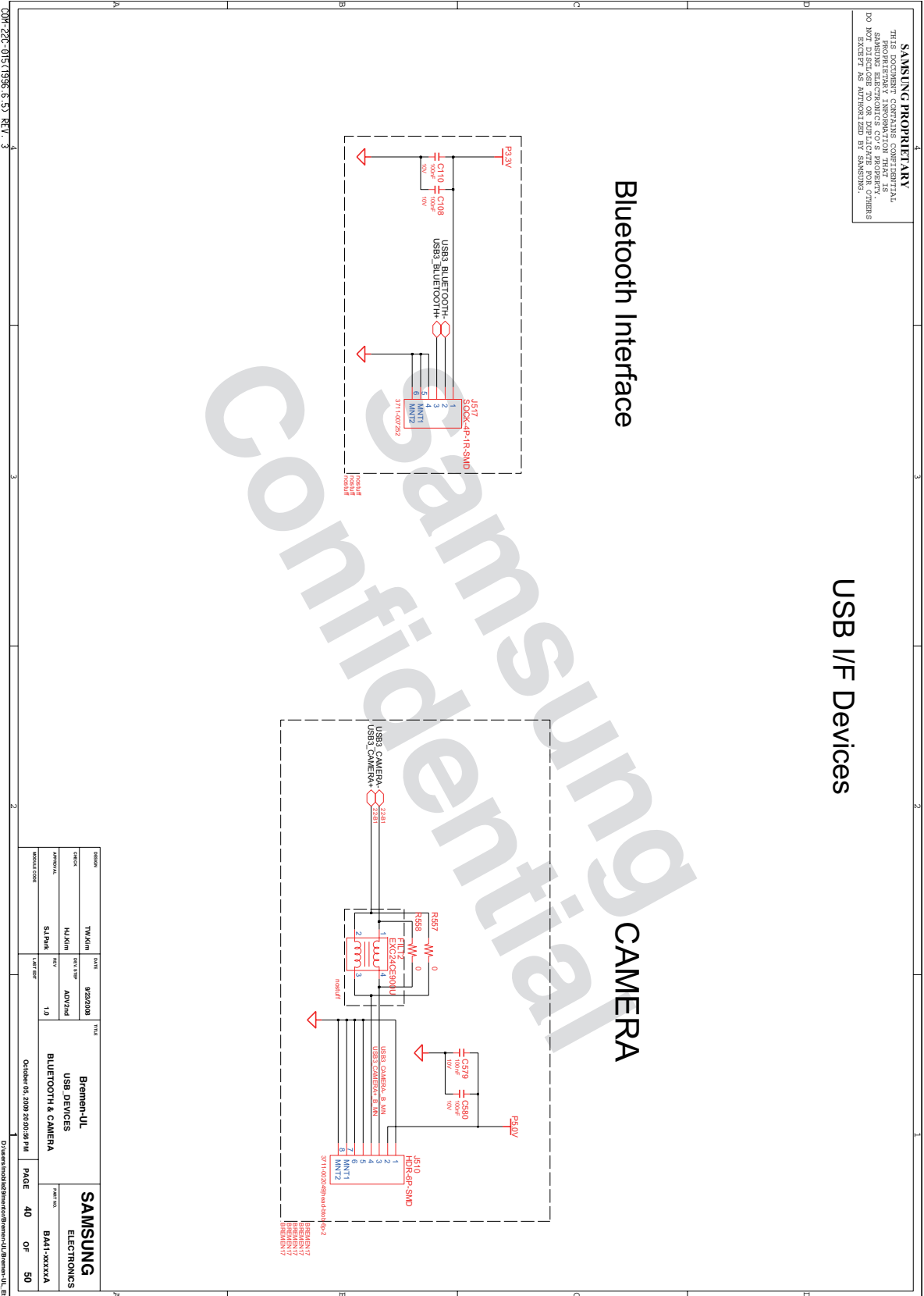
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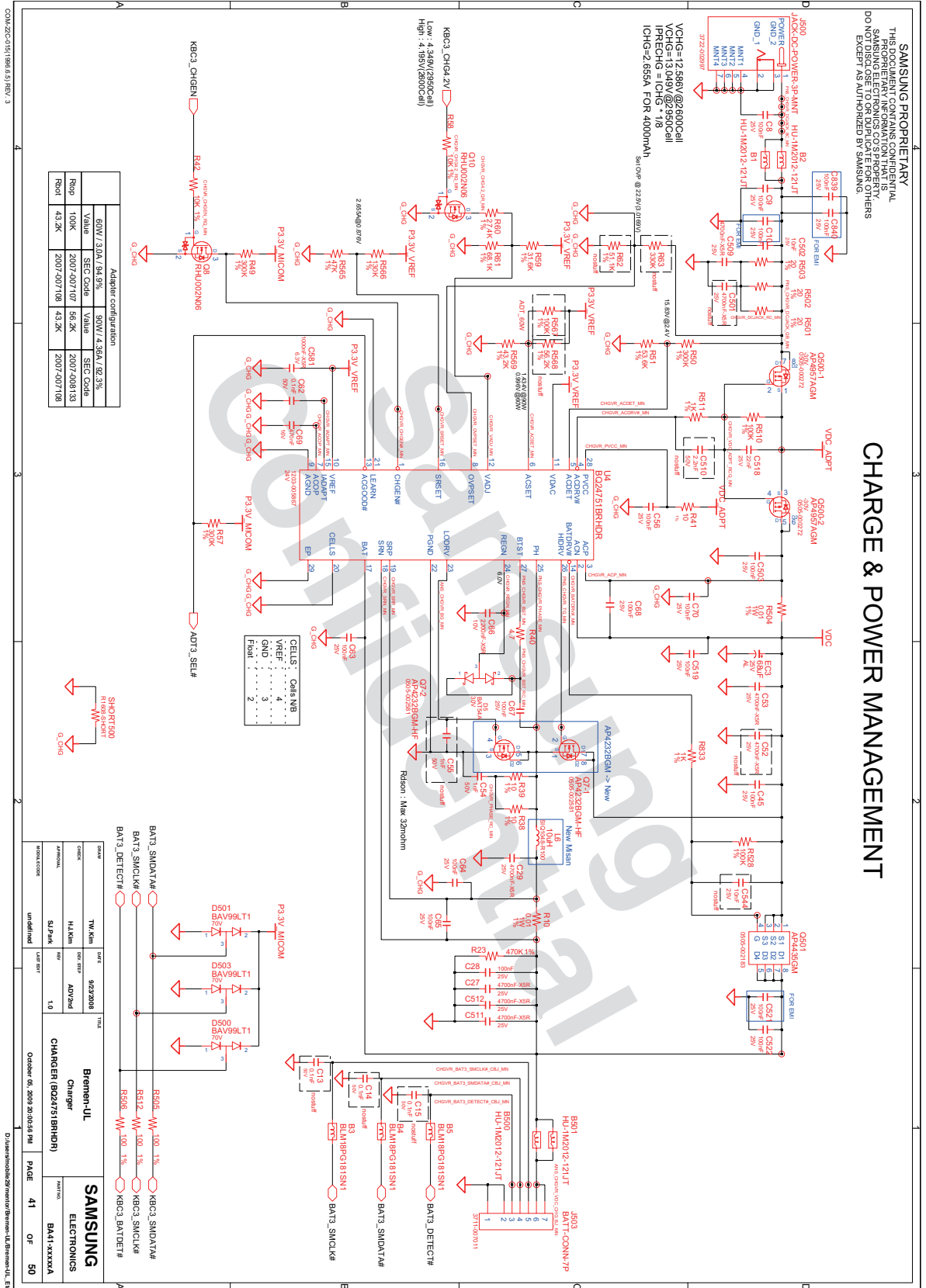
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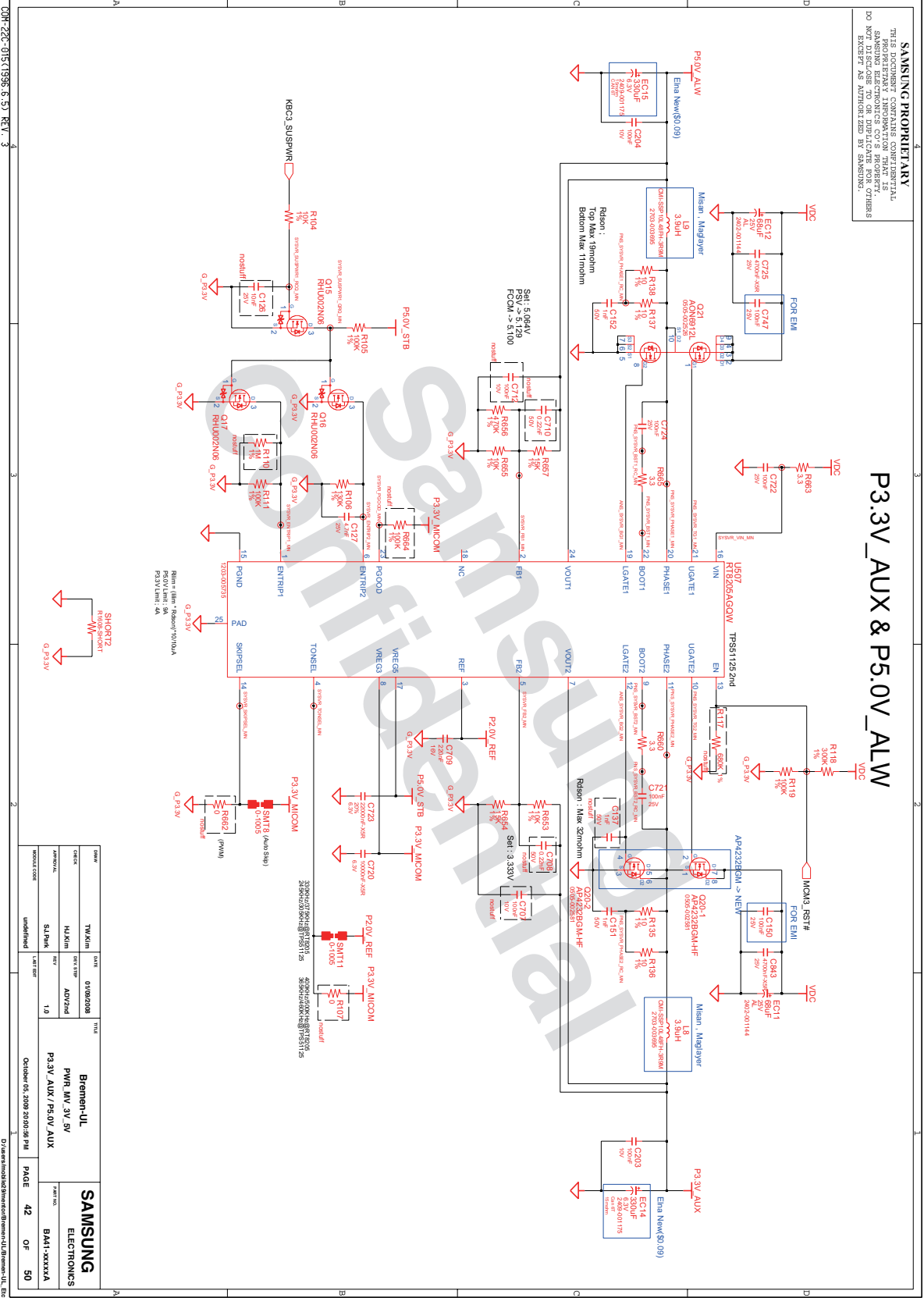
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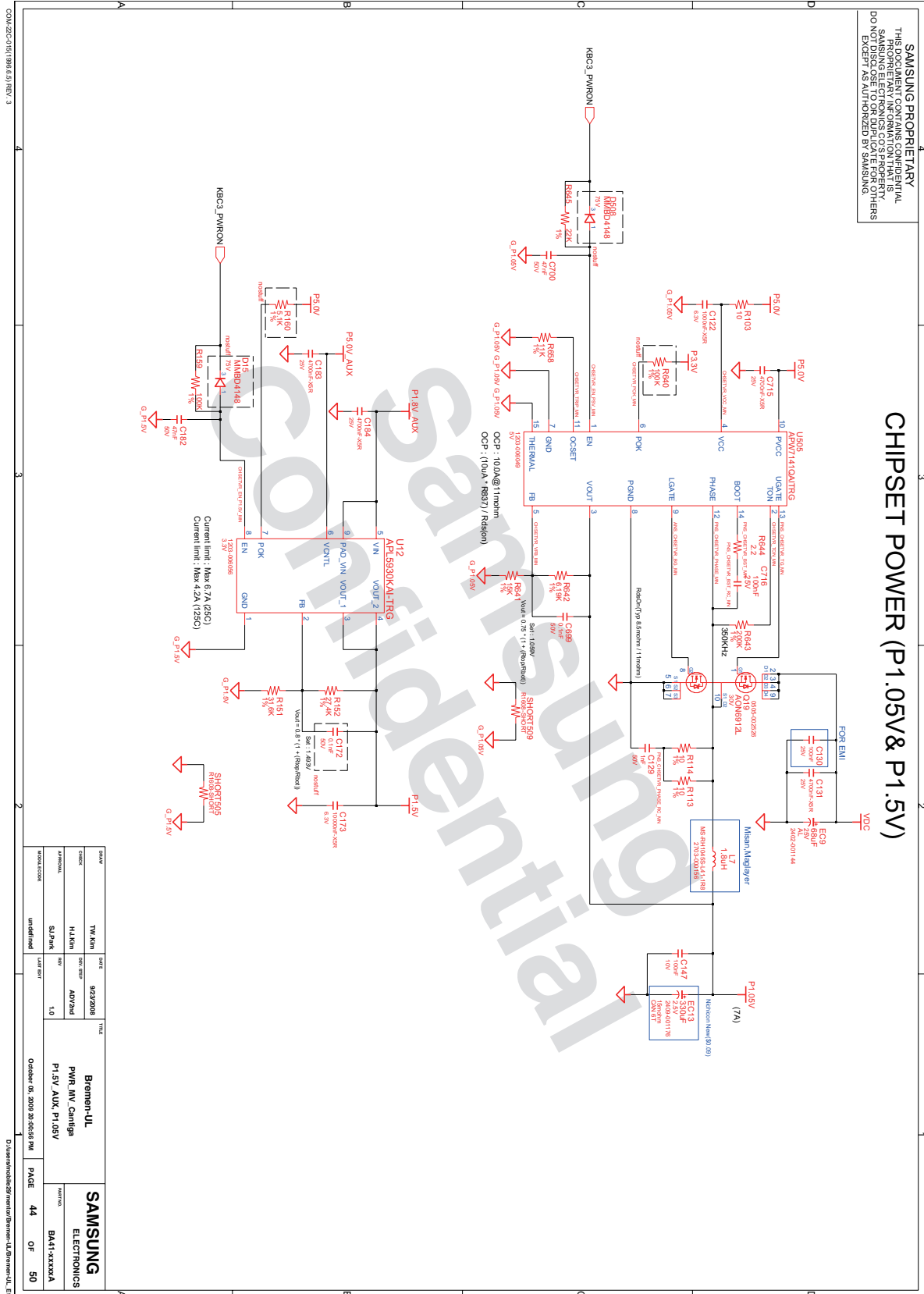
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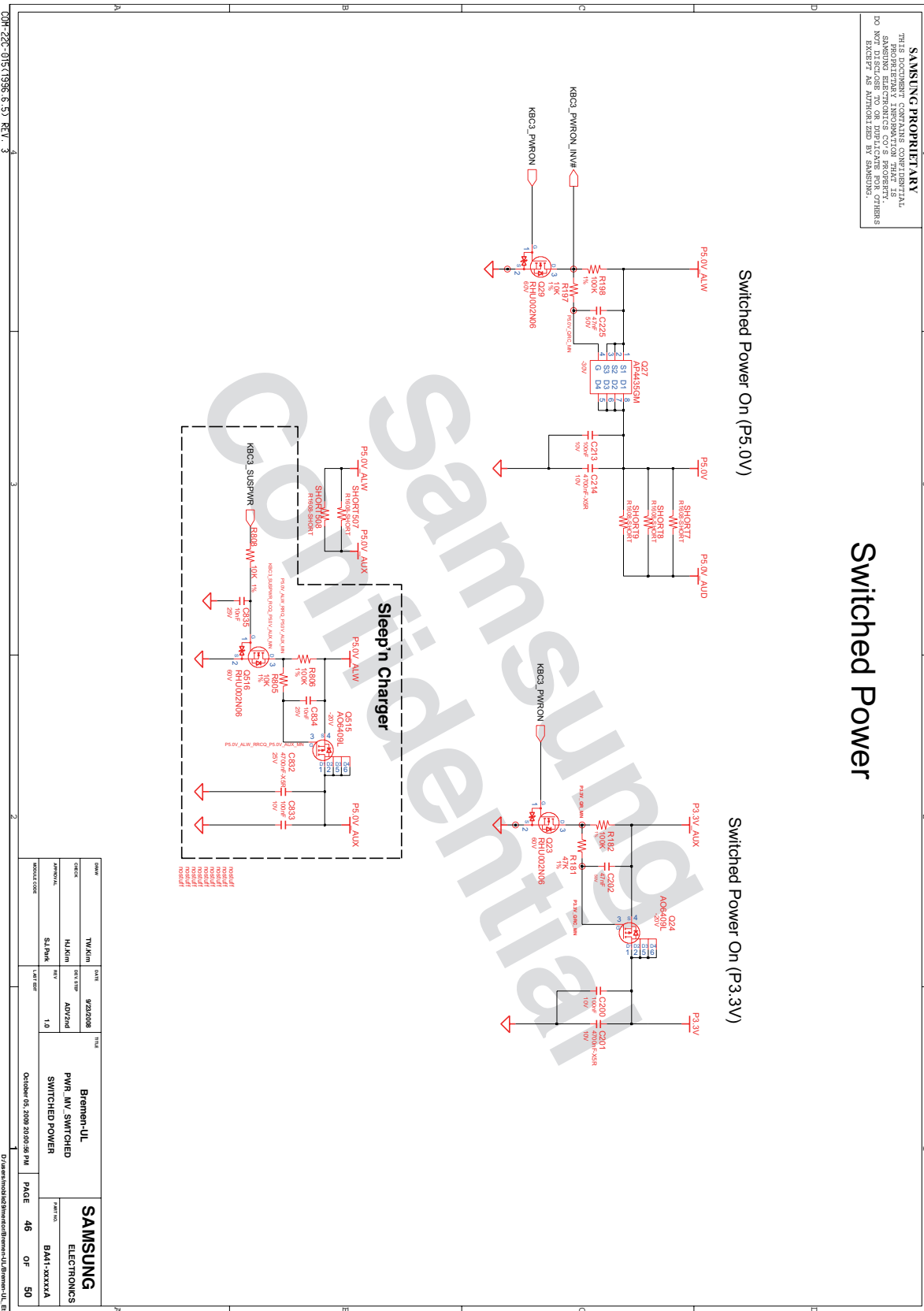
## 8. Block Diagram and Schematic





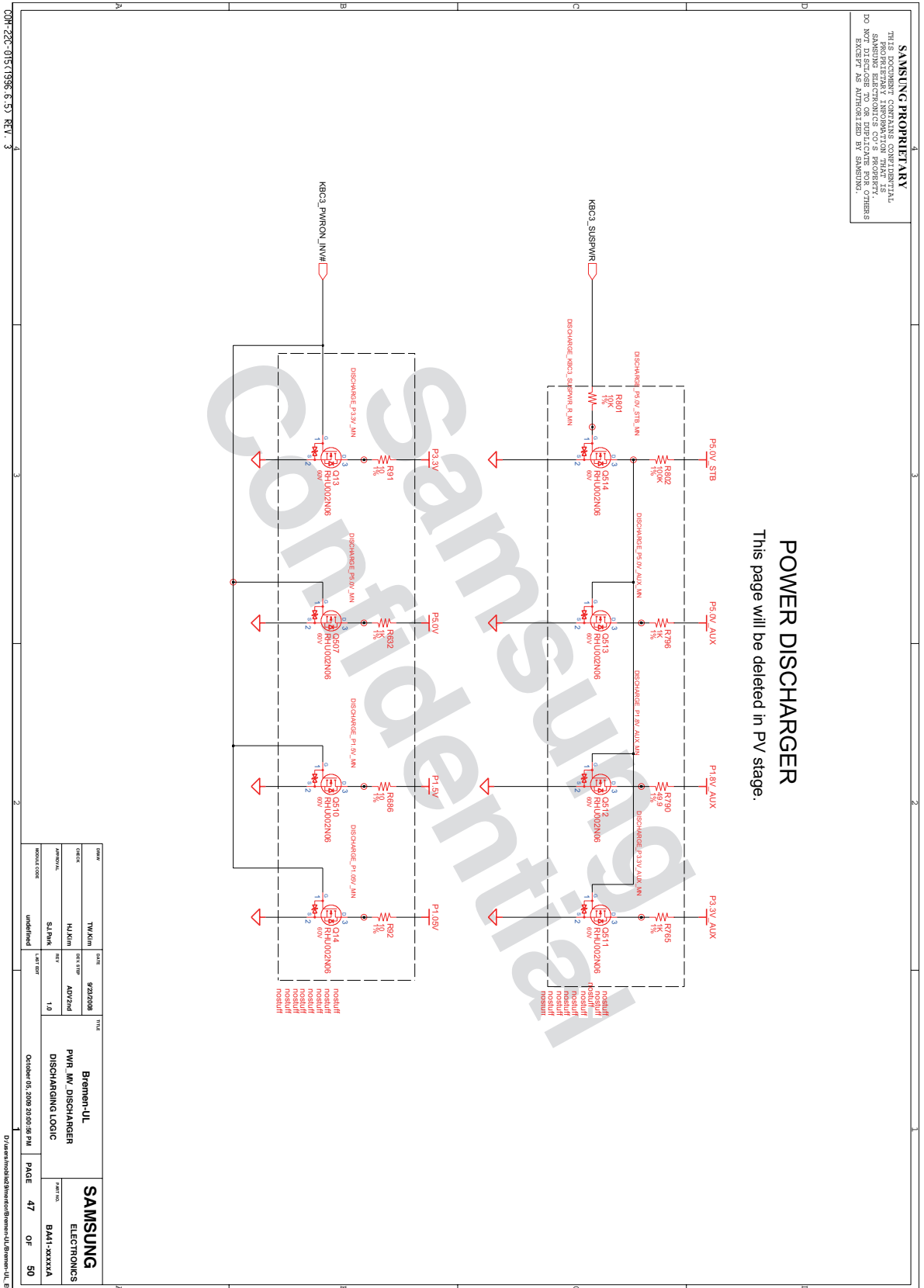
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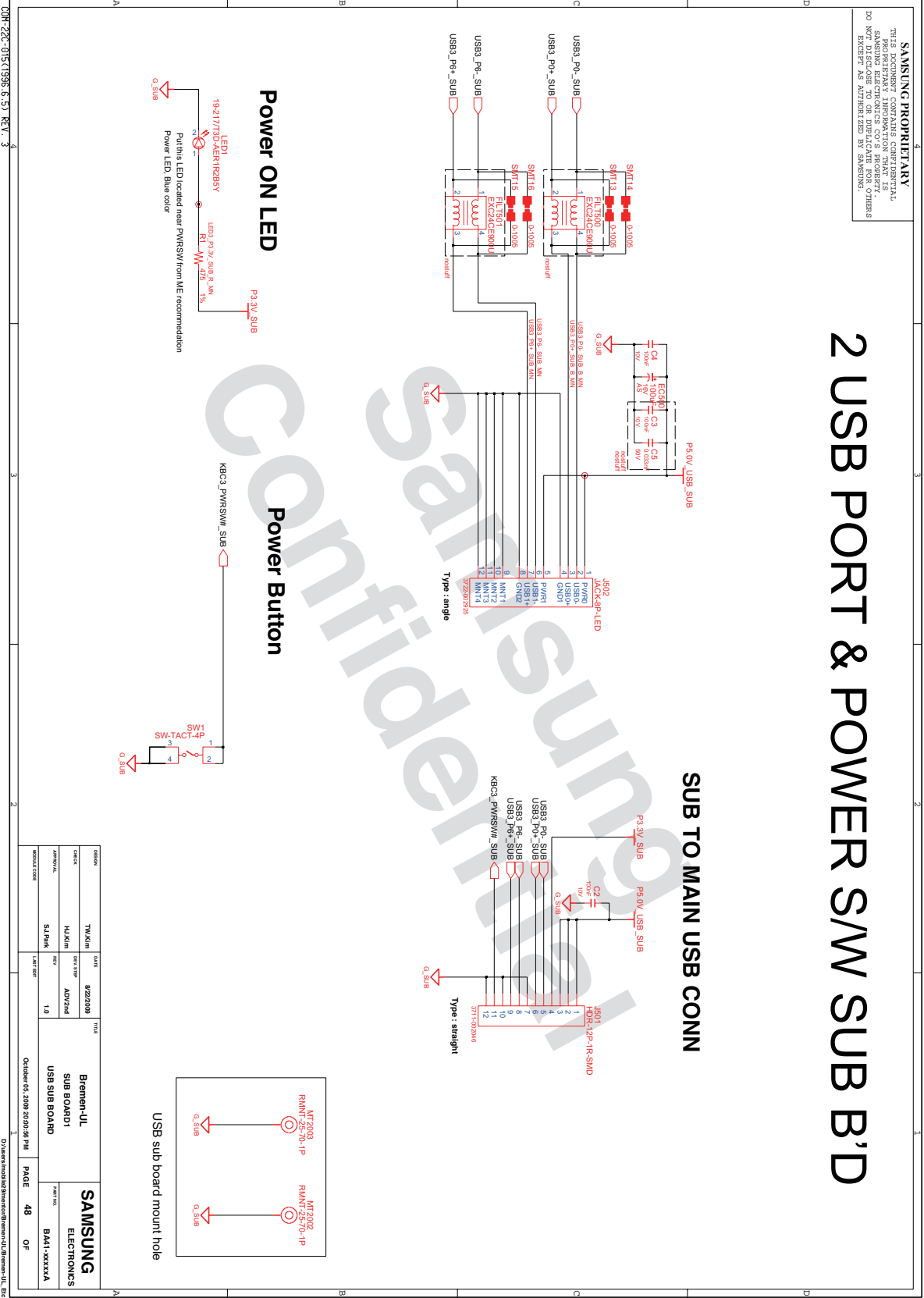
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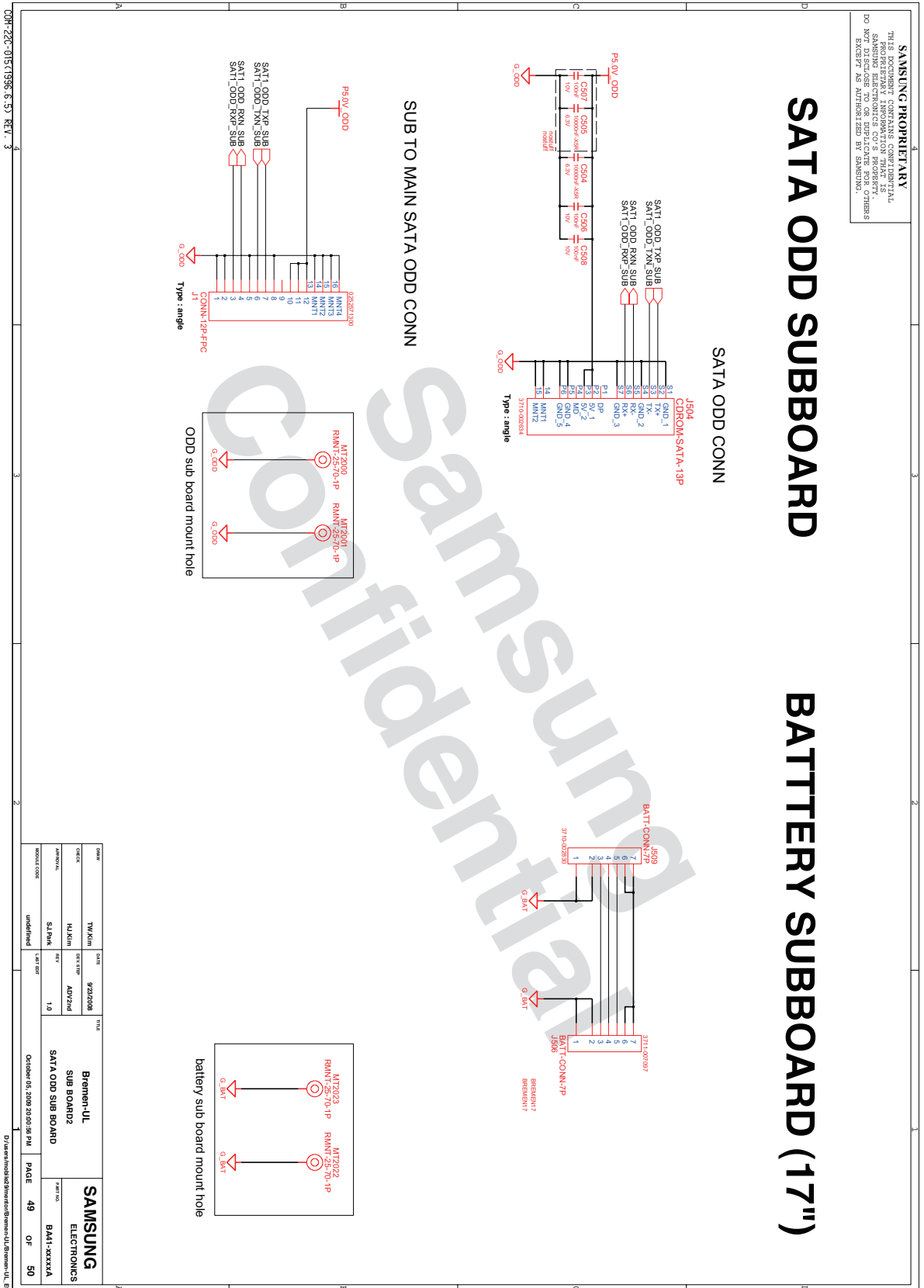
## 2 USB PORT & POWER SW SUB B'D





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