

R2 UMA(11.6")

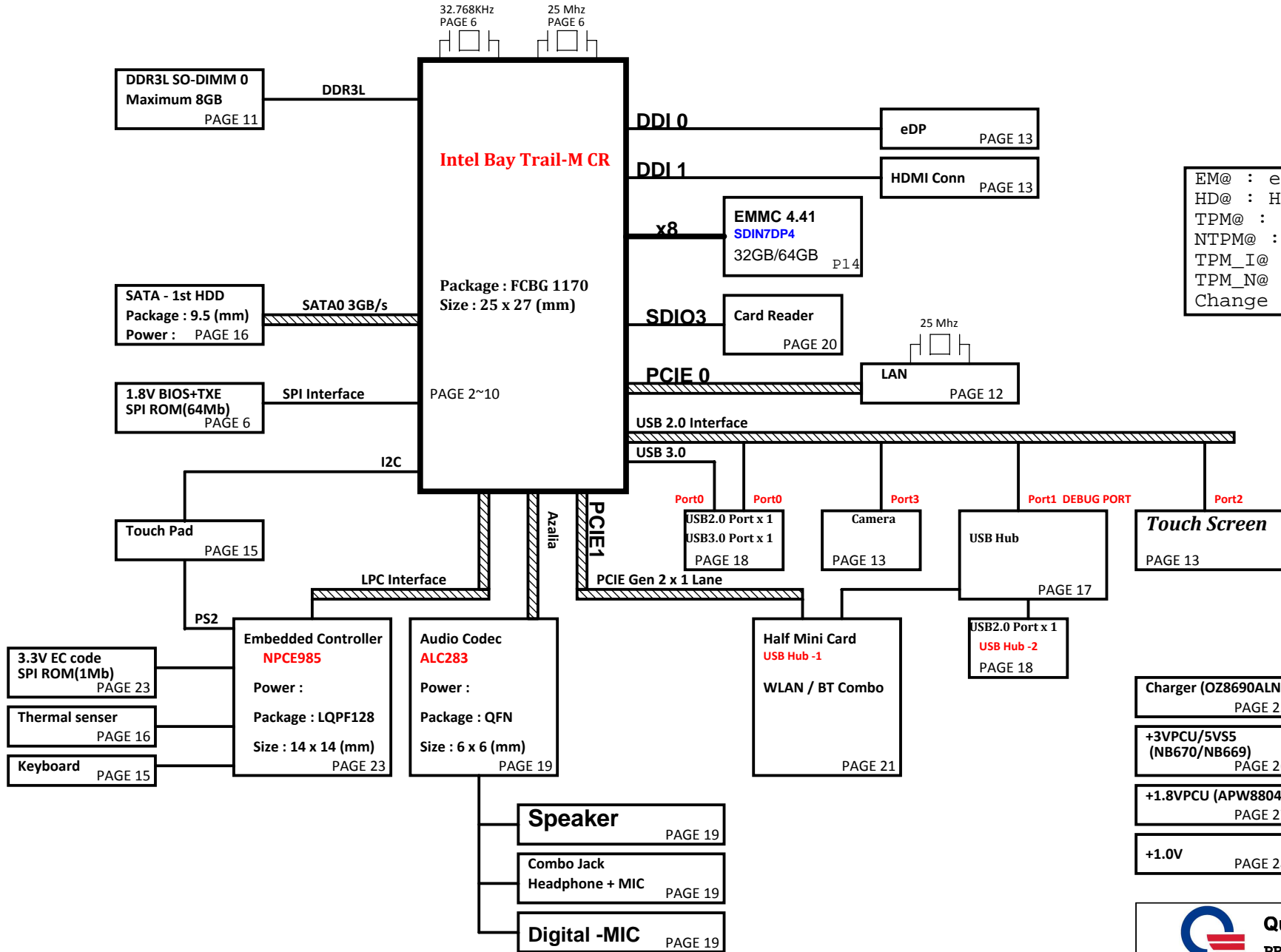
01

Intel Bay Trail-M Platform Block Diagram

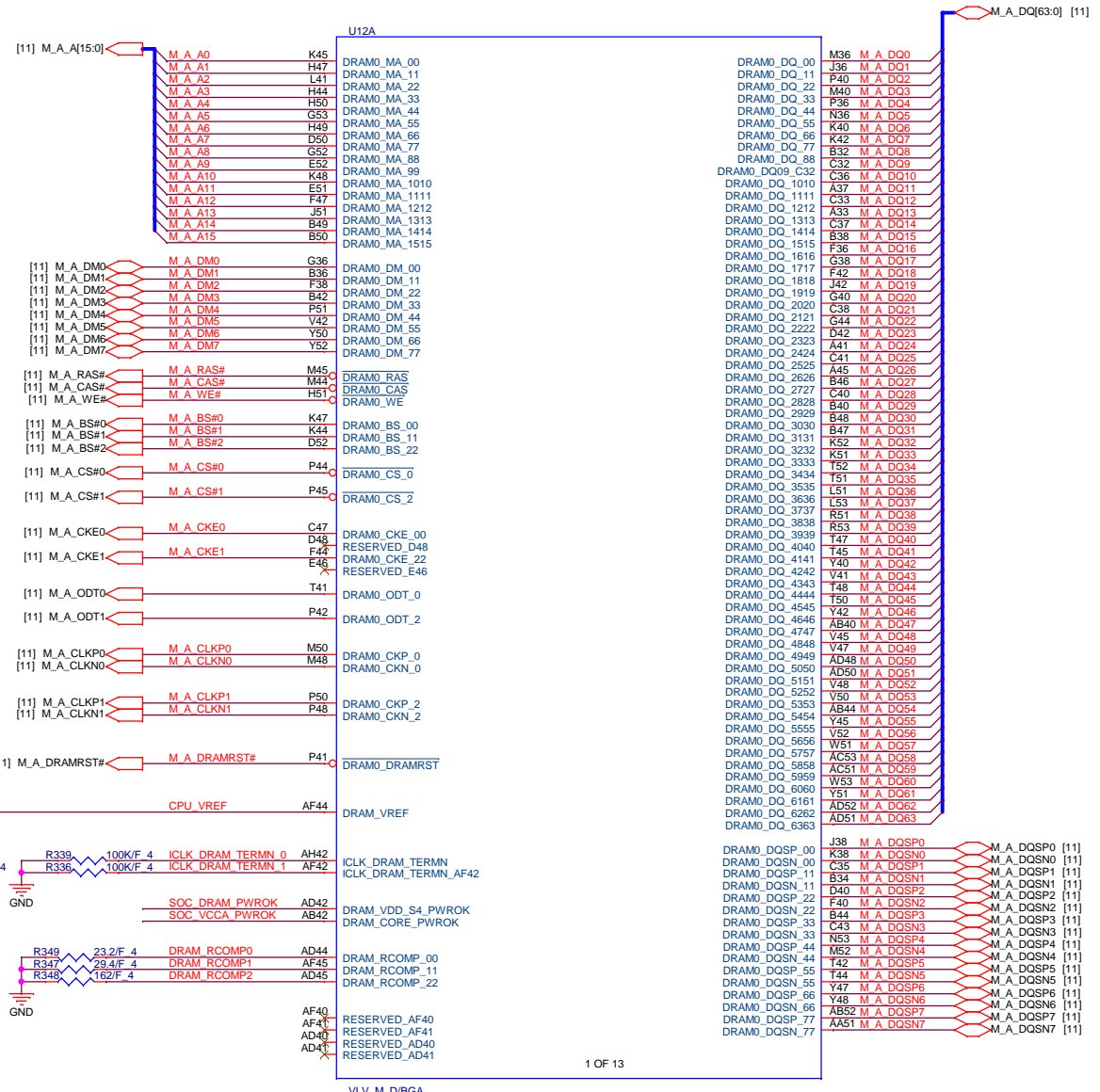
PCB 6L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : BOT

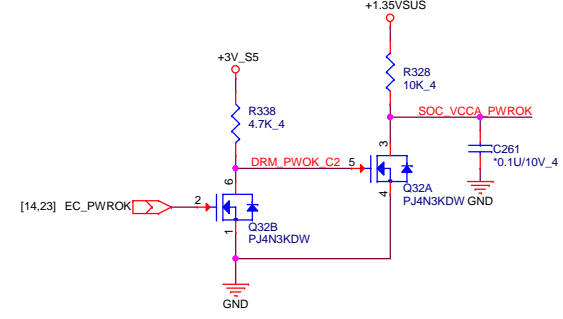
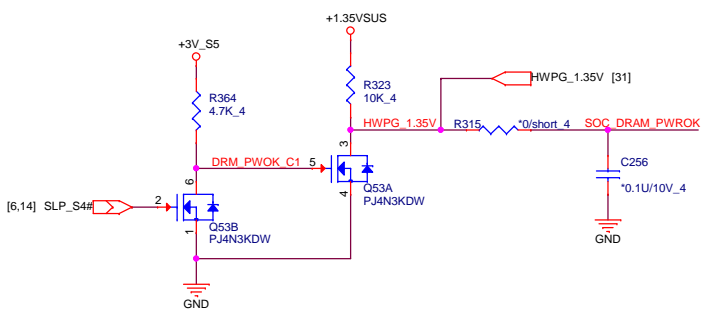
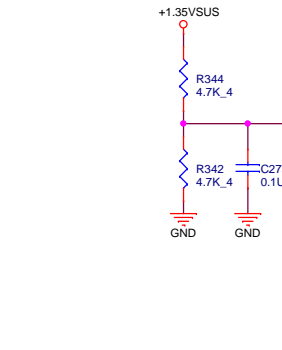
EM@ : eMMC
 HD@ : HDD
 TPM@ : TPM
 NTPM@ : Non-TPM
 TPM_I@ : 新唐
 TPM_N@ : 英飛凌
 Change CPU & Emmc P/N



Charger (OZ8690ALN) PAGE 25	+1.05V/1.5V PAGE 29
+3VPCU/5V55 (NB670/NB669) PAGE 26	+VCORE+VGFX(ISL95833) PAGE 30
+1.8VPCU (APW8804) PAGE 27	DDR3 (APW8819) PAGE 31
+1.0V PAGE 28	Dis-charge IC (G5934) PAGE 32




+1.35VSUS [8,11,31,32]
 +3V_S5 [9,12,14,15,16,17,21,23,29,30,32]



U12B

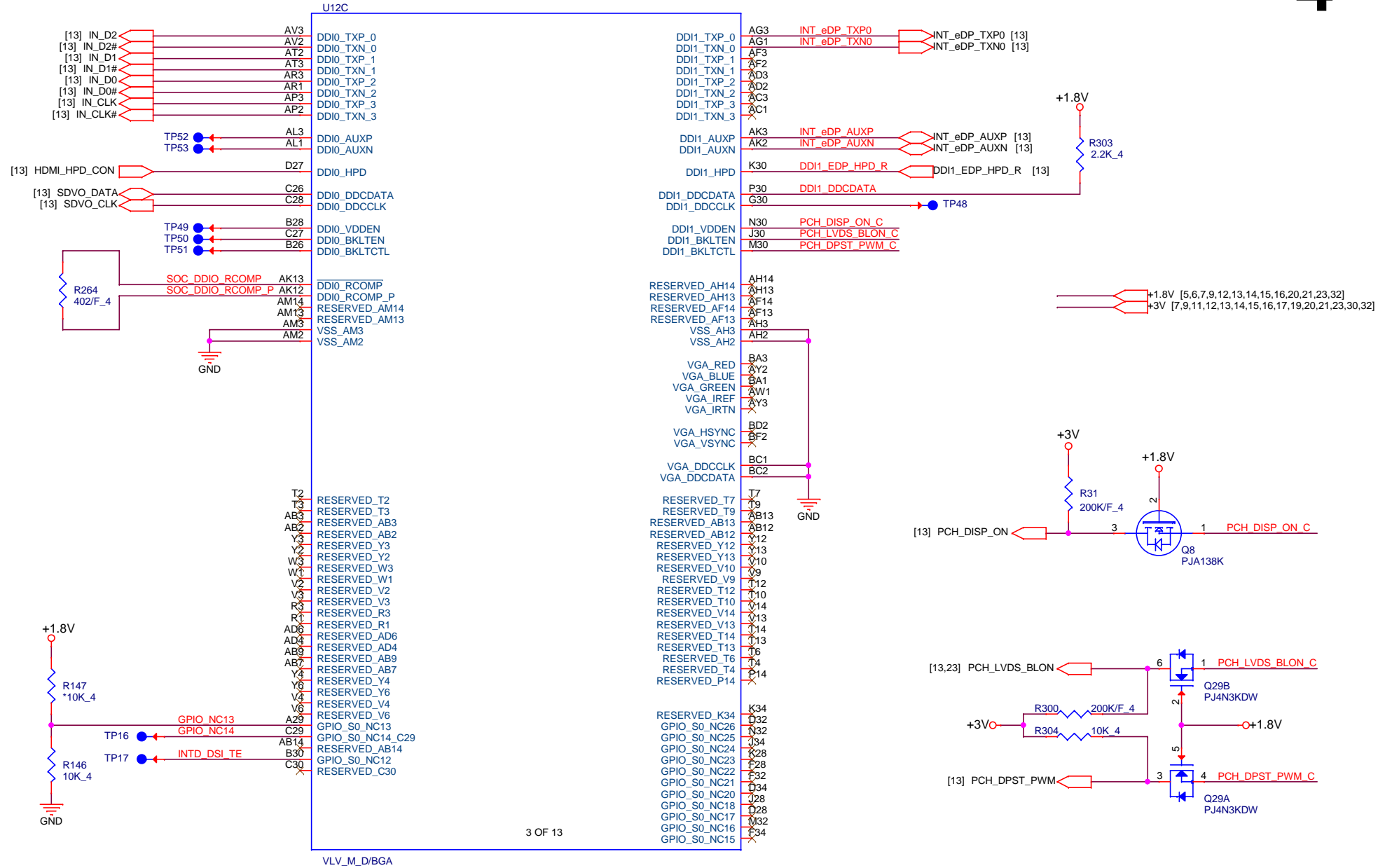
AY45	DRAM1_MA_00	DRAM1_DQ_00	BG38
BB47	DRAM1_MA_11	DRAM1_DQ_11	BC40
AW41	DRAM1_MA_22	DRAM1_DQ_22	BA42
BB44	DRAM1_MA_33	DRAM1_DQ_33	BD42
BB50	DRAM1_MA_44	DRAM1_DQ_44	BC38
BC53	DRAM1_MA_55	DRAM1_DQ_55	BD36
BB49	DRAM1_MA_66	DRAM1_DQ_66	BF42
BF50	DRAM1_MA_77	DRAM1_DQ_77	BC44
BC52	DRAM1_MA_88	DRAM1_DQ_88	BH32
BE52	DRAM1_MA_99	DRAM1_DQ_99	BG32
AY48	DRAM1_MA_1010	DRAM1_DQ_1010	BG36
BE51	DRAM1_MA_1111	DRAM1_DQ_1111	BJ37
BD47	DRAM1_MA_1212	DRAM1_DQ_1212	BG33
BA51	DRAM1_MA_1313	DRAM1_DQ_1313	BJ33
BH49	DRAM1_MA_1414	DRAM1_DQ_1414	BG37
BH50	DRAM1_MA_1515	DRAM1_DQ_1515	BH38
		DRAM1_DQ_1616	AU36
BD38	DRAM1_DM_00	DRAM1_DQ_1717	AT36
BH36	DRAM1_DM_11	DRAM1_DQ_1818	AV40
BC36	DRAM1_DM_22	DRAM1_DQ_1919	AT40
BH42	DRAM1_DM_33	DRAM1_DQ_2020	BA36
AT51	DRAM1_DM_44	DRAM1_DQ_2121	AV36
AM42	DRAM1_DM_55	DRAM1_DQ_2222	AY42
AK50	DRAM1_DM_66	DRAM1_DQ_2323	AY40
AK52	DRAM1_DM_77	DRAM1_DQ_2424	BJ41
		DRAM1_DQ_2525	BG41
AV45	DRAM1_RAS	DRAM1_DQ_2626	BJ45
AV48	DRAM1_CAS	DRAM1_DQ_2727	BH46
BB50	DRAM1_WE	DRAM1_DQ_2828	BG40
		DRAM1_DQ_2929	BH40
AY47	DRAM1_BS_00	DRAM1_DQ_3030	BH48
AY44	DRAM1_BS_11	DRAM1_DQ_3131	BH47
BF52	DRAM1_BS_22	DRAM1_DQ_3232	AY52
		DRAM1_DQ_3333	AY51
AT44	DRAM1_CS_0	DRAM1_DQ_3434	AP52
		DRAM1_DQ_3535	AP51
AT45	DRAM1_CS_2	DRAM1_DQ_3636	AV51
		DRAM1_DQ_3737	AV53
		DRAM1_DQ_3838	AR51
BG47	DRAM1_CKE_00	DRAM1_DQ_3939	AR53
BE46	RESERVED_BE46	DRAM1_DQ_4040	AP47
BD44	DRAM1_CKE_22	DRAM1_DQ_4141	AP45
BF48	RESERVED_BF48	DRAM1_DQ_4242	AK40
		DRAM1_DQ_4343	AM41
AP41	DRAM1_ODT_0	DRAM1_DQ_4444	AP48
		DRAM1_DQ_4545	AP50
AT42	DRAM1_ODT_2	DRAM1_DQ_4646	AK42
		DRAM1_DQ_4747	AH40
		DRAM1_DQ_4848	AM45
AV50	DRAM1_CKP_0	DRAM1_DQ_4949	AM47
AV48	DRAM1_CKN_0	DRAM1_DQ_5050	AF48
		DRAM1_DQ_5151	AF50
		DRAM1_DQ_5252	AM48
		DRAM1_DQ_5353	AM50
AT50	DRAM1_CKP_2	DRAM1_DQ_5454	AH44
AT48	DRAM1_CKN_2	DRAM1_DQ_5555	AK45
		DRAM1_DQ_5656	AM52
		DRAM1_DQ_5757	AL51
AT41	DRAM1_DRAMRST	DRAM1_DQ_5858	AG53
		DRAM1_DQ_5959	AG51
		DRAM1_DQ_6060	AL53
		DRAM1_DQ_6161	AK51
		DRAM1_DQ_6262	AF52
		DRAM1_DQ_6363	AF51
		DRAM1_DQSP_00	BF40
		DRAM1_DQSN_00	BD40
		DRAM1_DQSN_11	BG35
		DRAM1_DQSN_11	BH34
		DRAM1_DQSN_11	BA38
		DRAM1_DQSN_22	AY38
		DRAM1_DQSN_22	BH44
		DRAM1_DQSN_33	BG43
		DRAM1_DQSN_33	AU53
		DRAM1_DQSN_44	AV52
		DRAM1_DQSN_44	AP42
		DRAM1_DQSN_55	AP44
		DRAM1_DQSN_55	AK47
		DRAM1_DQSN_66	AK48
		DRAM1_DQSN_66	AH52
		DRAM1_DQSN_77	AJ51
		DRAM1_DQSN_77	AJ51

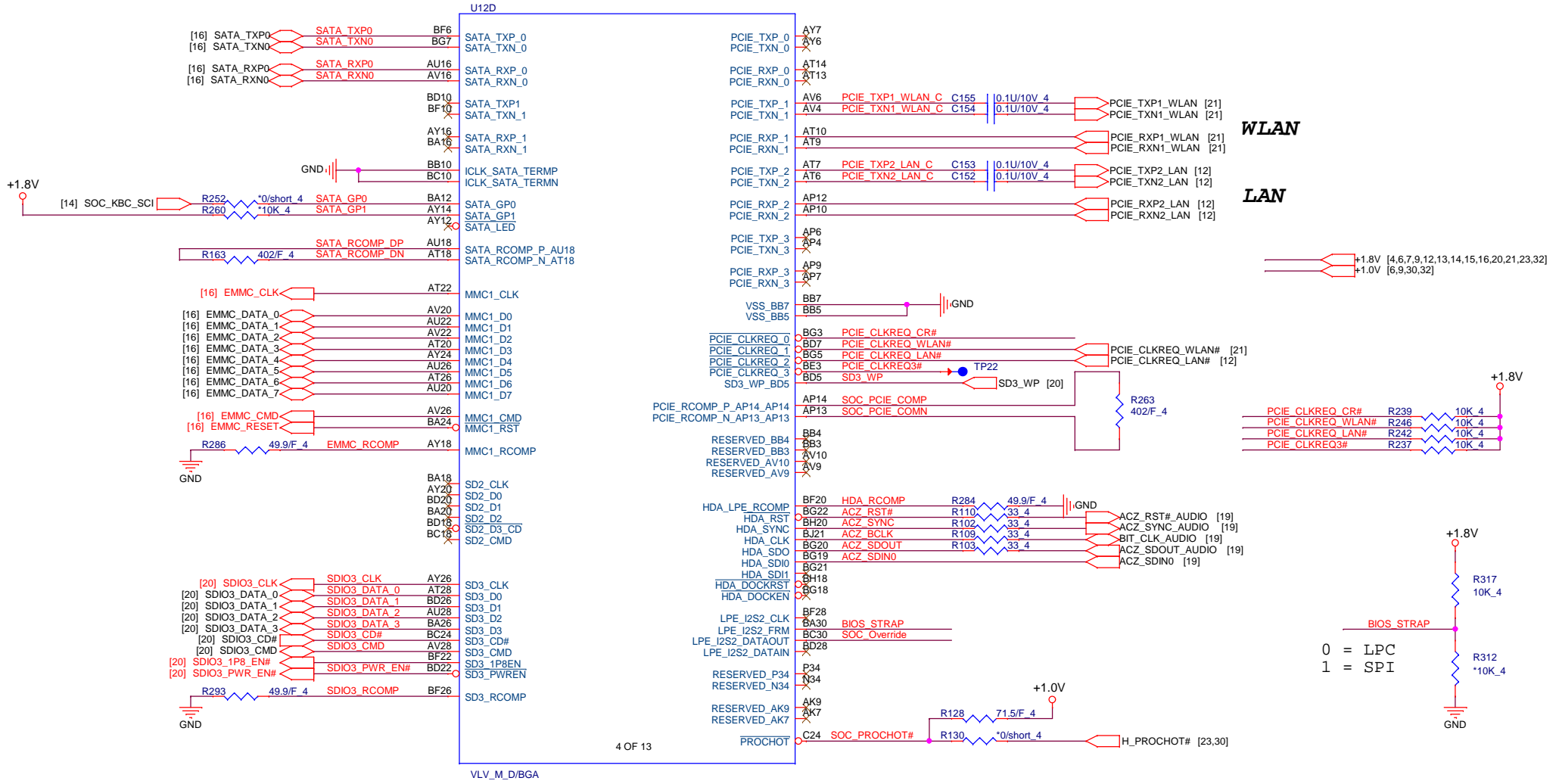
VLV_M_D/BGA



Quanta Computer Inc.
PROJECT : ZHK

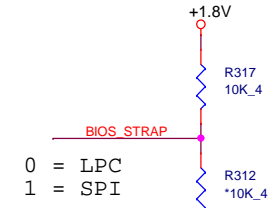
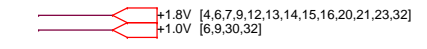
Size	Document Number	Rev
	Valley 2/9 (DDR8)	1A
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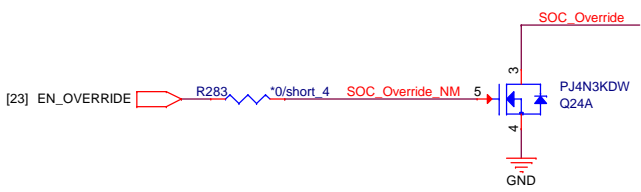


WLAN

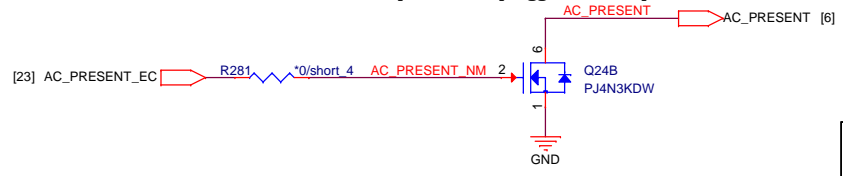
LAN



Security Flash Descriptors
0 = Override
1 = Normal Operation

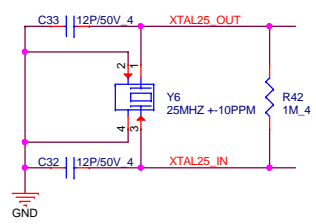


AC Present: This input pin indicates when the platform is plugged into AC power.



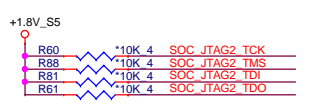
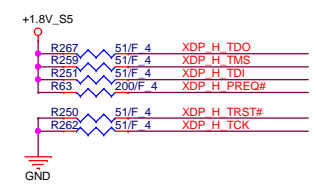
Quanta Computer Inc.
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Size	Document Number	Rev
	Valley 4/9 (SD/PCIE/SATA)	1A
Date:	Monday, June 30, 2014	Sheet 5 of 33



WLAN clk

LAN clk



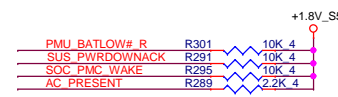
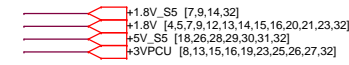
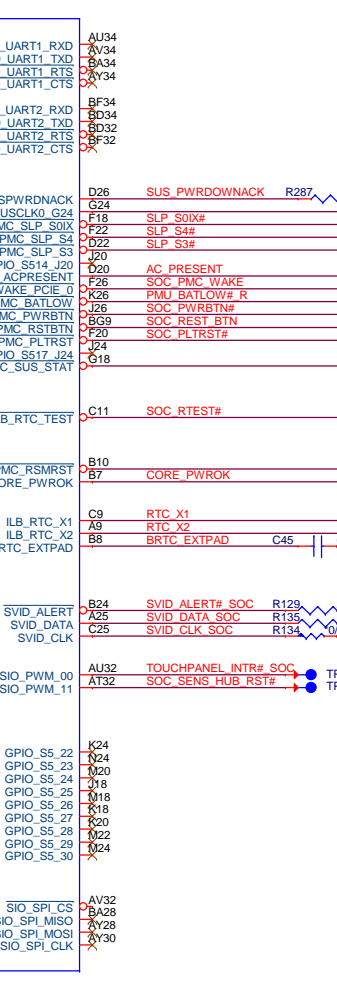
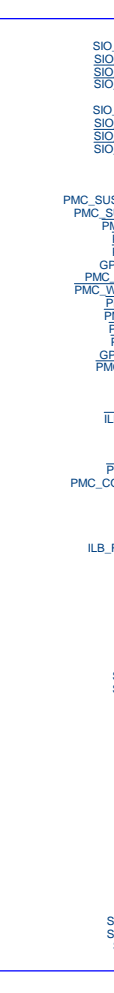
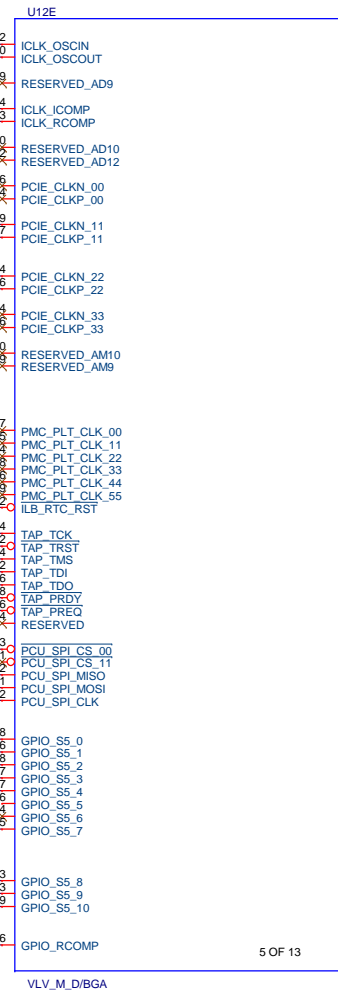
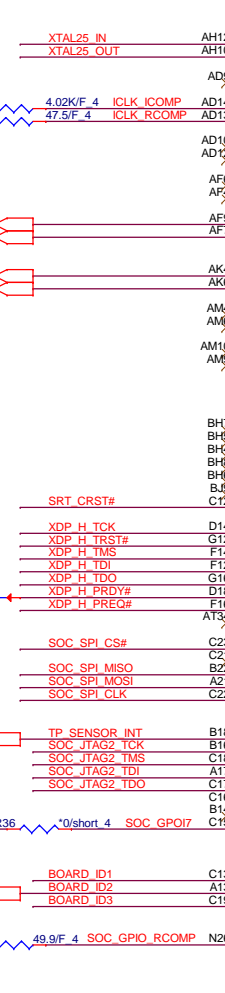
[21] CLK_PCIE_WLANN

[12] CLK_PCIE_LANN

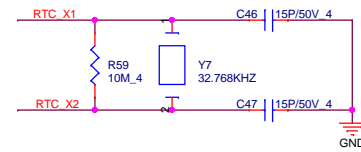
[14] TP_SENSOR_INT

[14] SOC_KCB_SMI

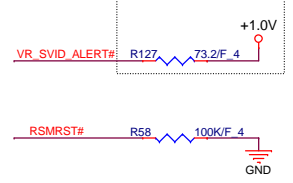
[13] BOARD_ID2



RTC Clock 32.768KHz

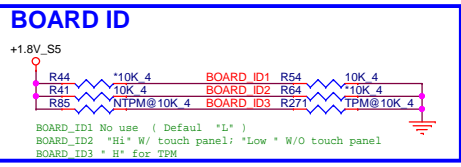
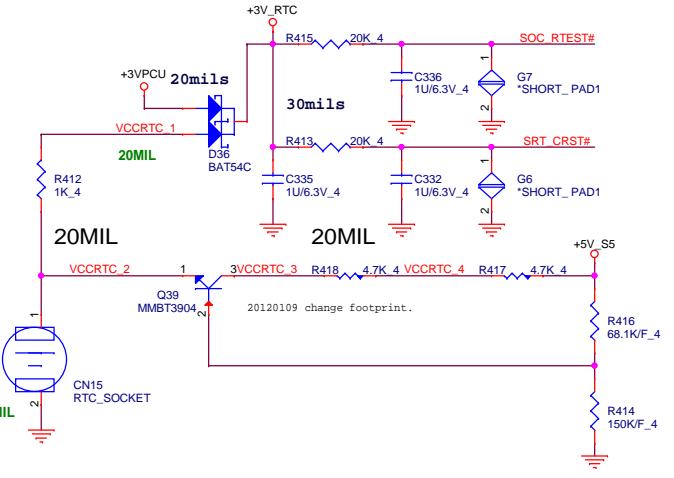


Close APU

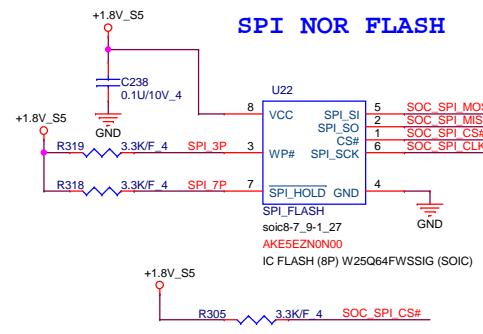


ML1220 Coin type
 AHL03001424 FDK (SAY) 15mAh
 AHL03017100 Panasonic (MAT) 17mAh

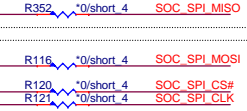
RTC Circuitry(RTC)



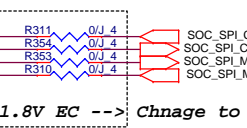
BOARD_ID1 No use (Default "L")
 BOARD_ID2 "Hi" N/ touch panel; "Low" W/O touch panel.
 BOARD_ID3 "H" for TPM



Close SPI ROM



Close APU



1.8V_EC --> Chnage to 22ohm

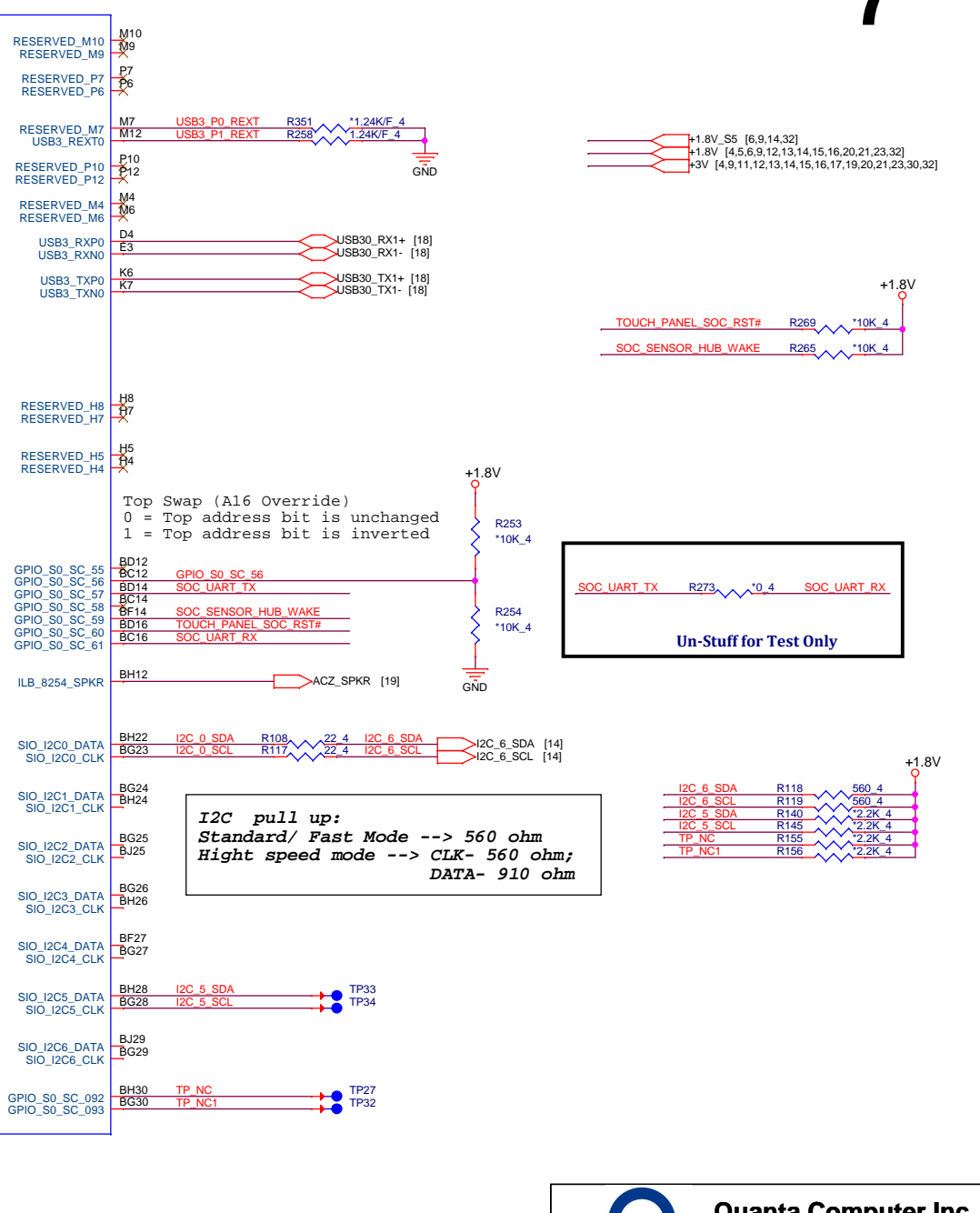
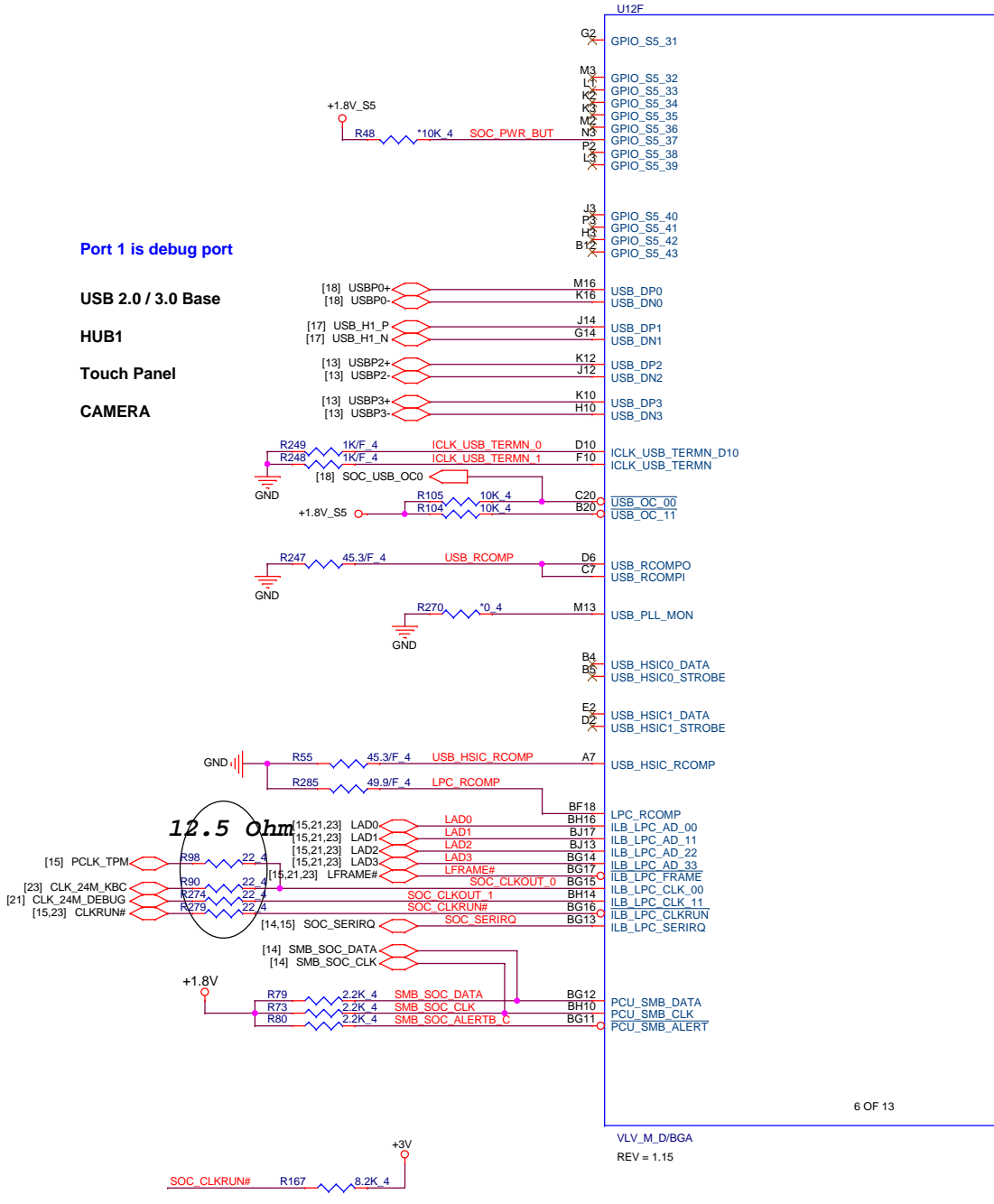
Port 1 is debug port

USB 2.0 / 3.0 Base

HUB1

Touch Panel

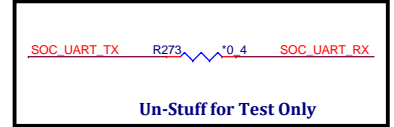
CAMERA



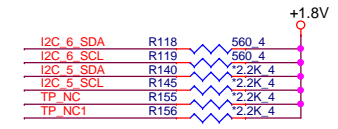
+1.8V_S5 [6,9,14,32]
 +1.8V [4,5,6,9,12,13,14,15,16,20,21,23,32]
 +3V [4,9,11,12,13,14,15,16,17,19,20,21,23,30,32]

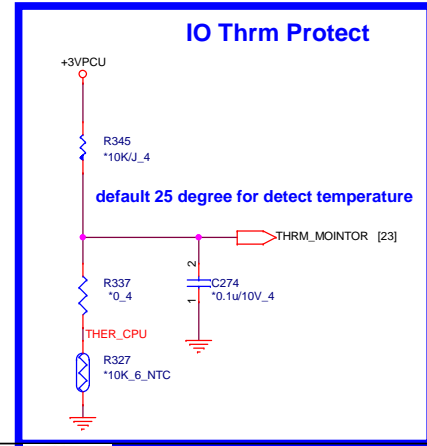
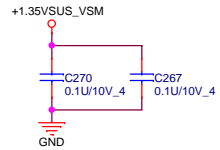
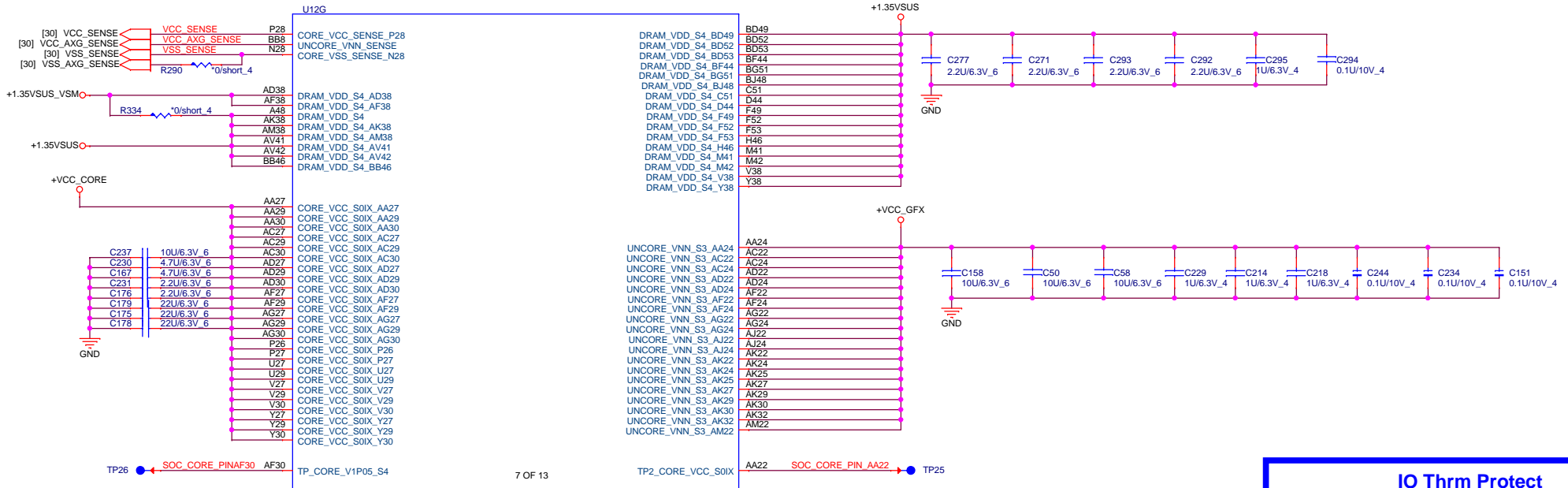
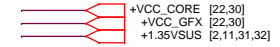
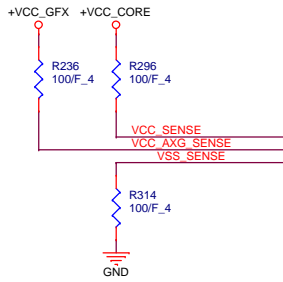
TOUCH PANEL SOC_RST# R269 *10K 4
 SOC_SENSOR_HUB_WAKE R265 *10K 4

Top Swap (A16 Override)
 0 = Top address bit is unchanged
 1 = Top address bit is inverted



I2C pull up:
 Standard/ Fast Mode --> 560 ohm
 High speed mode --> CLK- 560 ohm;
 DATA- 910 ohm



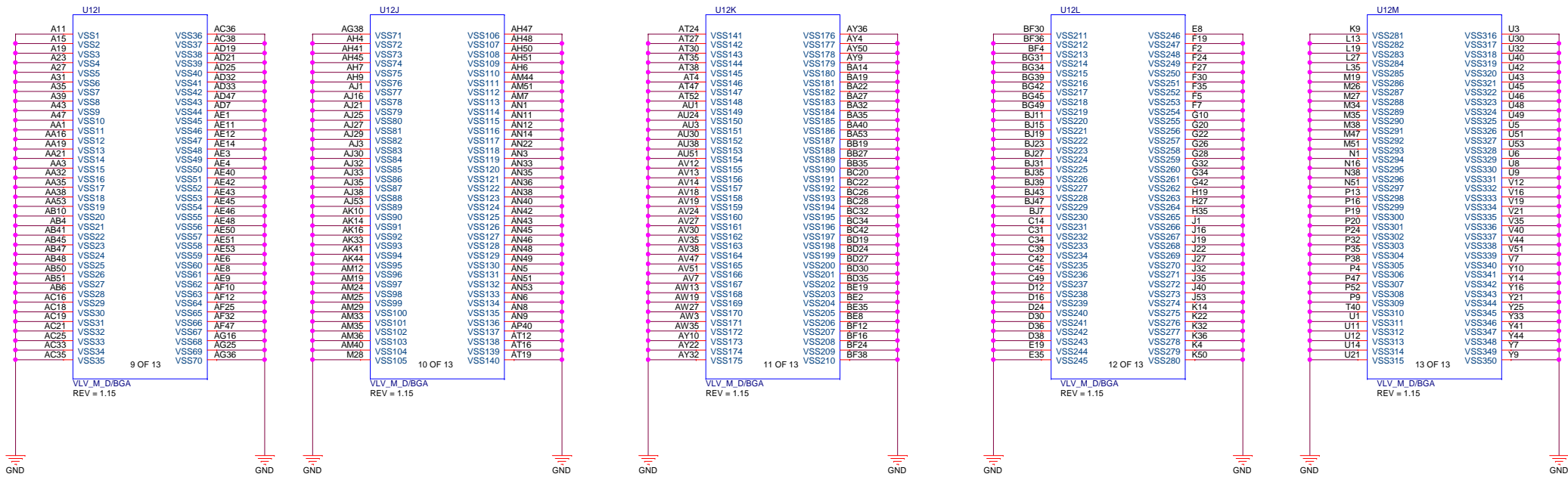


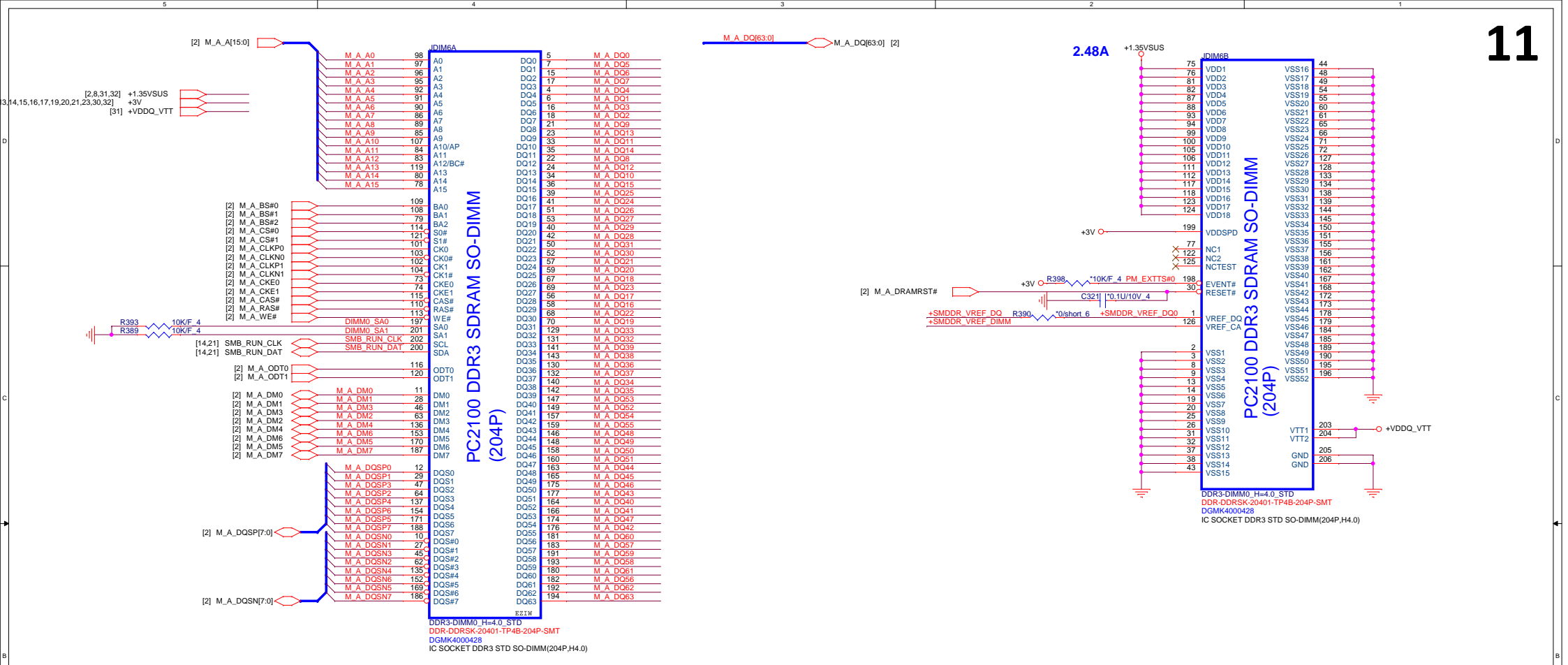
VLV_M_D/BGA
REV = 1.15

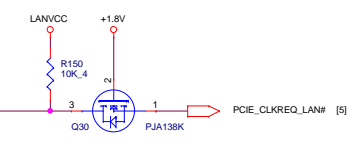
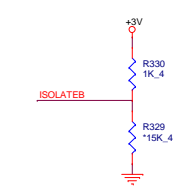
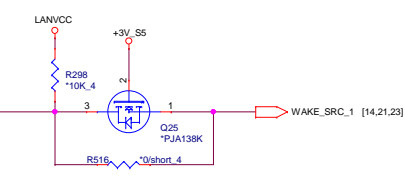
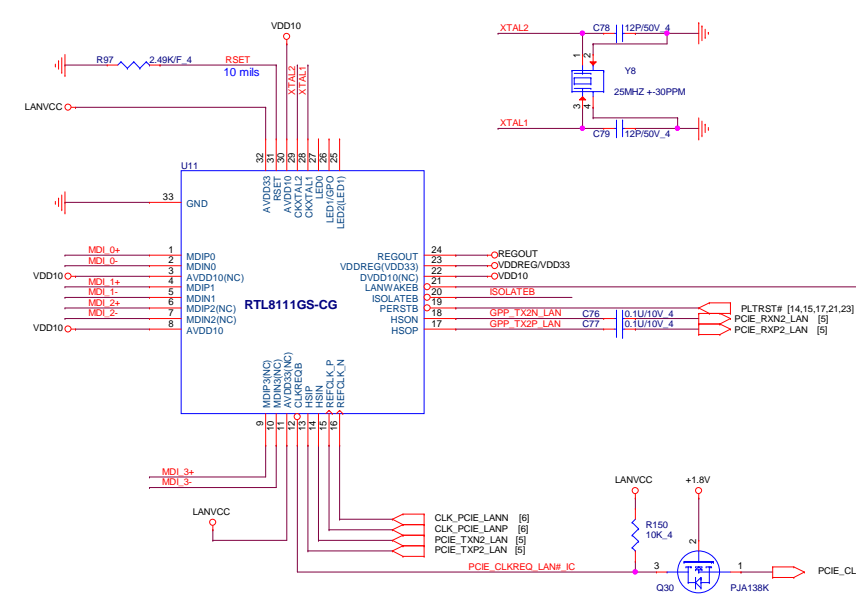
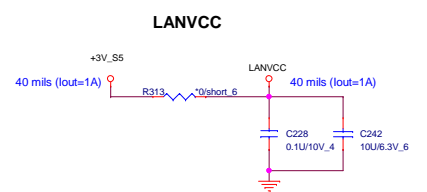
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Quanta Computer Inc.
PROJECT : ZHJ

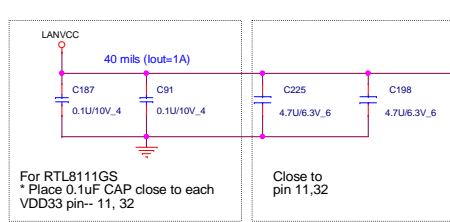
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	Valley 7/9 (Power 1)	2A
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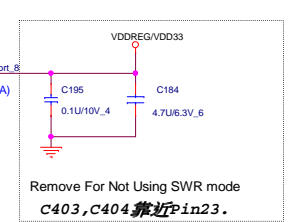


[2,9,14,15,16,17,21,22,29,30,32] +3V_S5
 [4,7,8,11,13,14,15,16,17,19,20,21,23,30,32] +3V

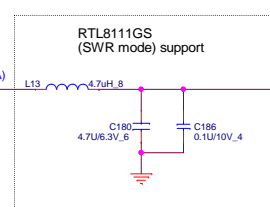


For RTL8111GS
 * Place 0.1uF CAP close to each VDD33 pin-- 11, 32

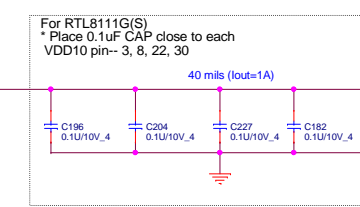
Close to pin 11,32



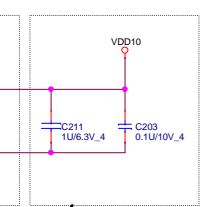
Remove For Not Using SWR mode
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Rev: B (C-test) L13 Remove CV-4708MN00 for SMT request, change P/N to CV-4710T201

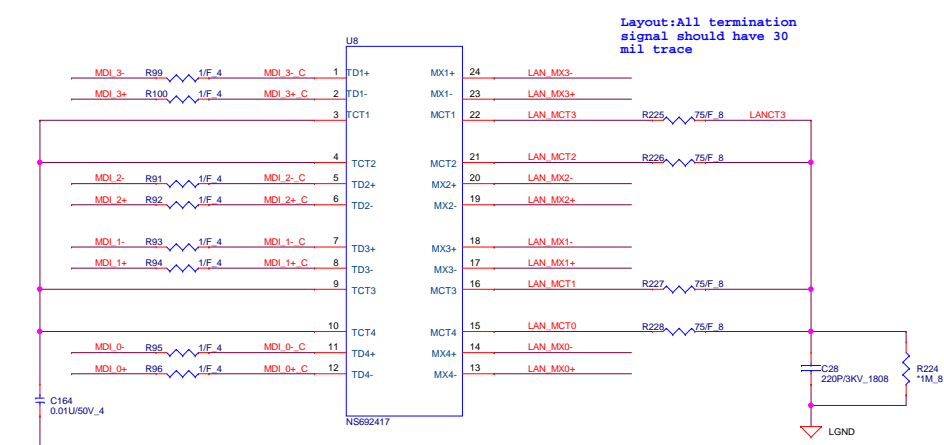


For RTL8111G(S)
 * Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30

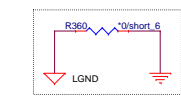


For RTL8111G(S)
 * Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

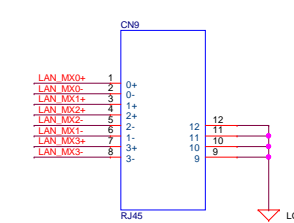
Transformer



Layout: All termination signal should have 30 mil trace

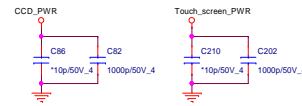
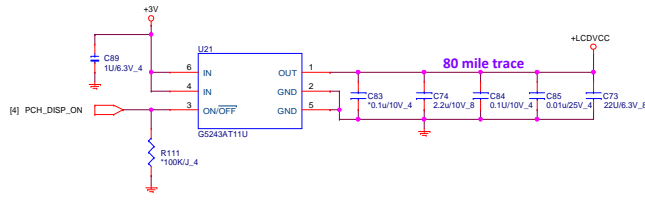


RJ45 Connector



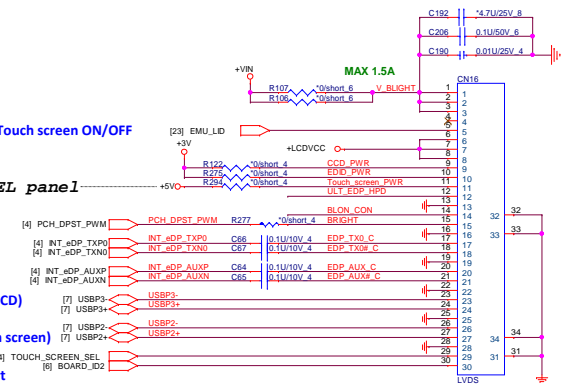
Rev: B (C-test) CN9 change main source P/N to DFTJ08FR414 2nd source : DFTJ08FR417

LVDS Conn.



For ANGEL panel

Touch screen ON/OFF



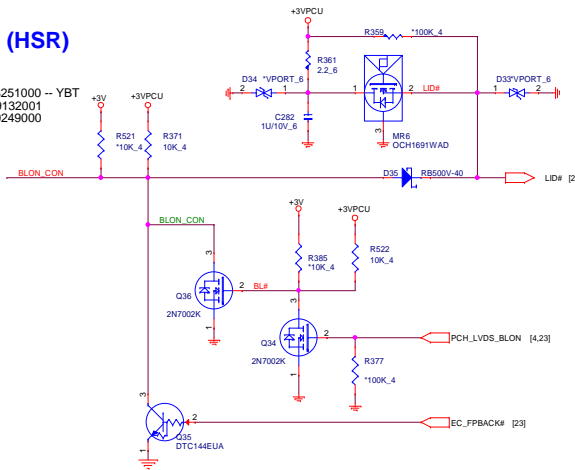
USB to Connector (CCD)

USB to Connector (Touch screen)

Touch screen SEL.
Auto enable/disable touch panel USB port

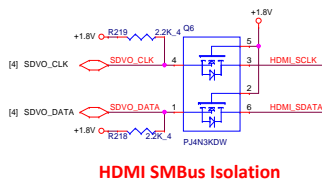
HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 - YBT
3rd source : AL009132001
4th source : AL009249000



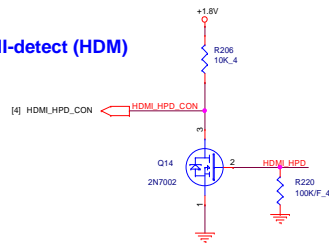
[4,7,9,11,12,14,15,16,17,19,20,21,23,30,32] +3V
[4,5,6,7,9,12,14,15,16,20,21,23,32] +1.8V
[16,19,32] +5V

HDMI Conn.

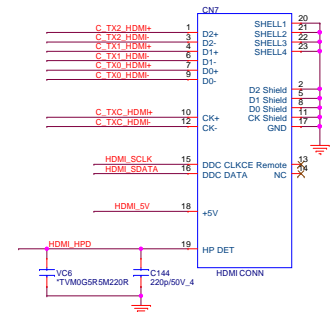
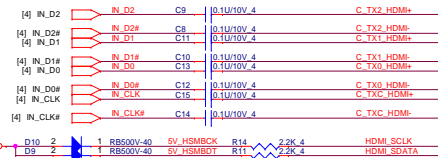
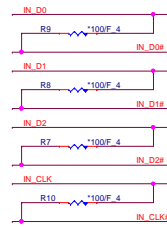


HDMI SMBus Isolation

HDMI-detect (HDM)

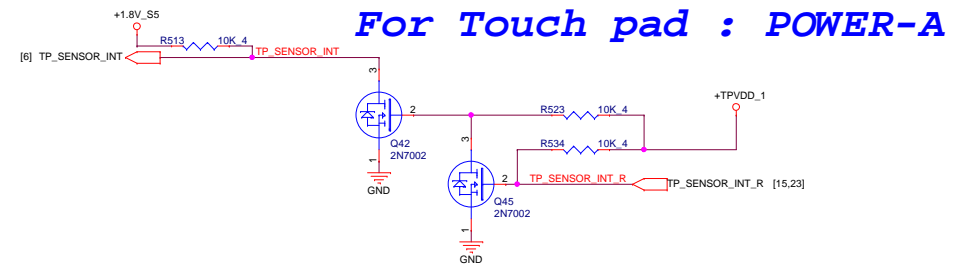
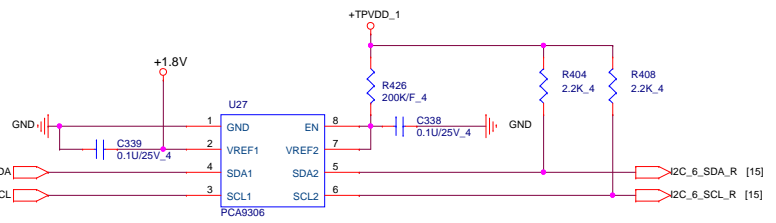
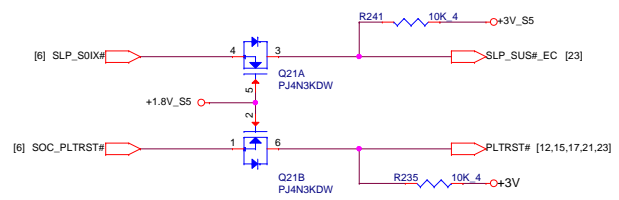
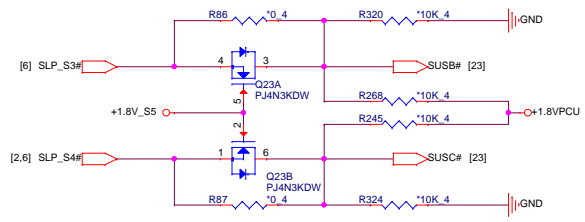
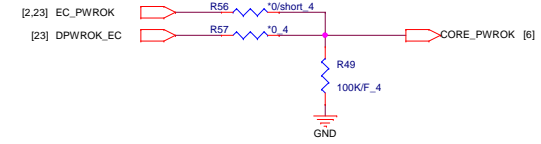
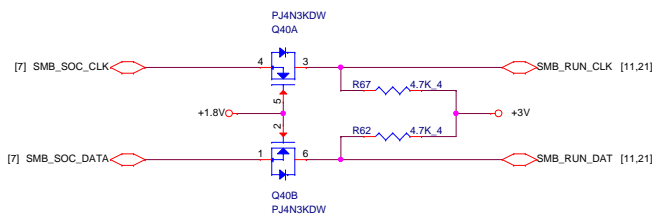
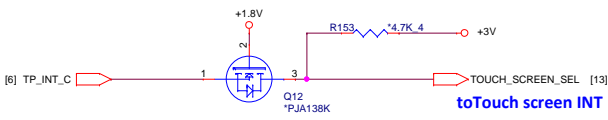
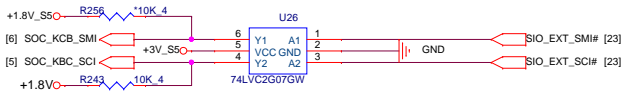
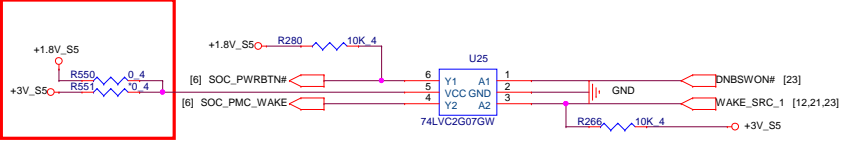
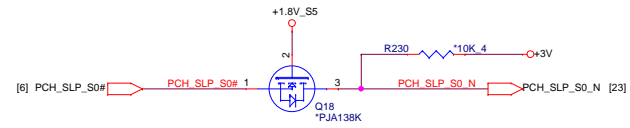
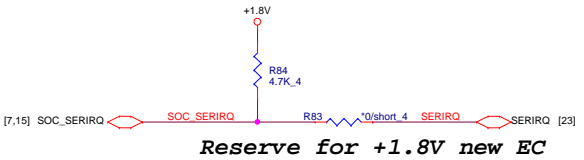


EMI (EMC)



Close to HDMI connector

[6,7,9,32] +1.8V_S5
 [2,9,12,15,16,17,21,23,29,30,32] +3V_S5
 [4,5,6,7,9,12,13,15,16,20,21,23,32] +1.8V
 [4,7,9,11,12,13,15,16,17,19,20,21,23,30,32] +3V



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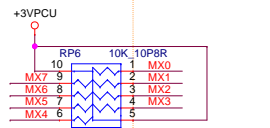
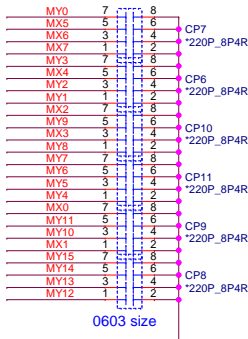
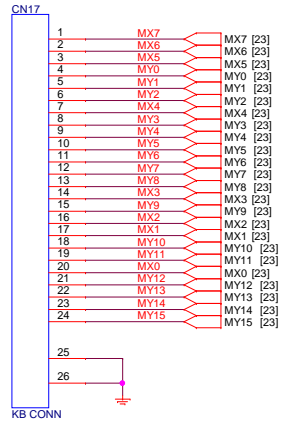
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	Level Shift	1A
Date:	Monday, June 30, 2014	Sheet 14 of 33

KEYBOARD (KBC)

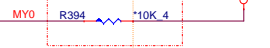
<20110214(E1A)>
Change CP1-CP6 footprint from 8p4r-0402-smt to 8P4R, for SMT open issue.

<EMI>

INTERNAL KEYBOARD STRIP SET (KBC)

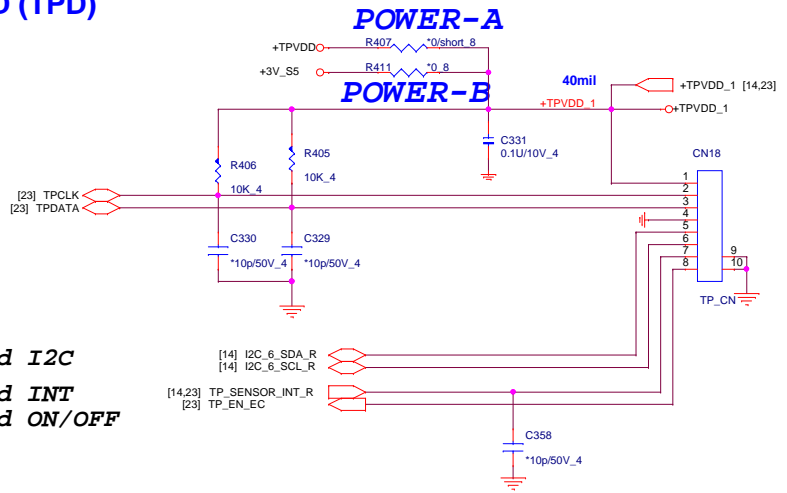


Unstuff



Rev: B (C-test) CN17 change ACS P/N from DFFC24FR000 to DFFC24FR110

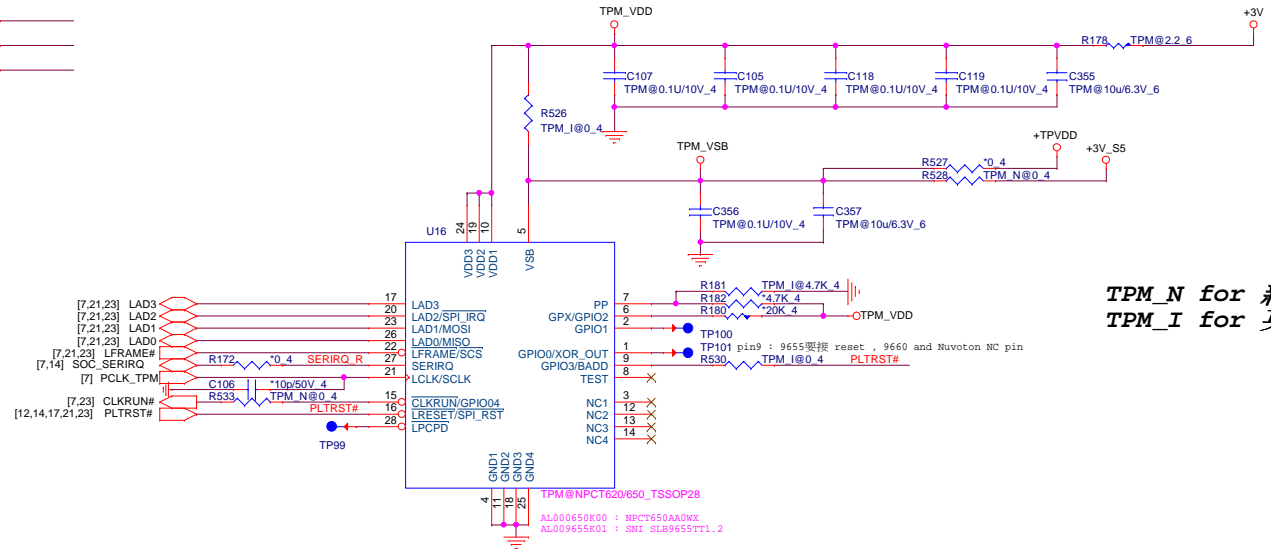
TOUCH PAD (TPD)



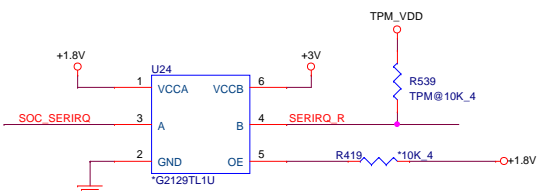
Touch pad I2C
 Touch pad INT
 Touch pad ON/OFF

ACER DEFINE
 VDD
 PS2-CLK
 PS2-DATA
 GND
 I2C-DATA
 I2C-CLK
 ATTN (INT)
 SER-OFF.

TPM (TPM)

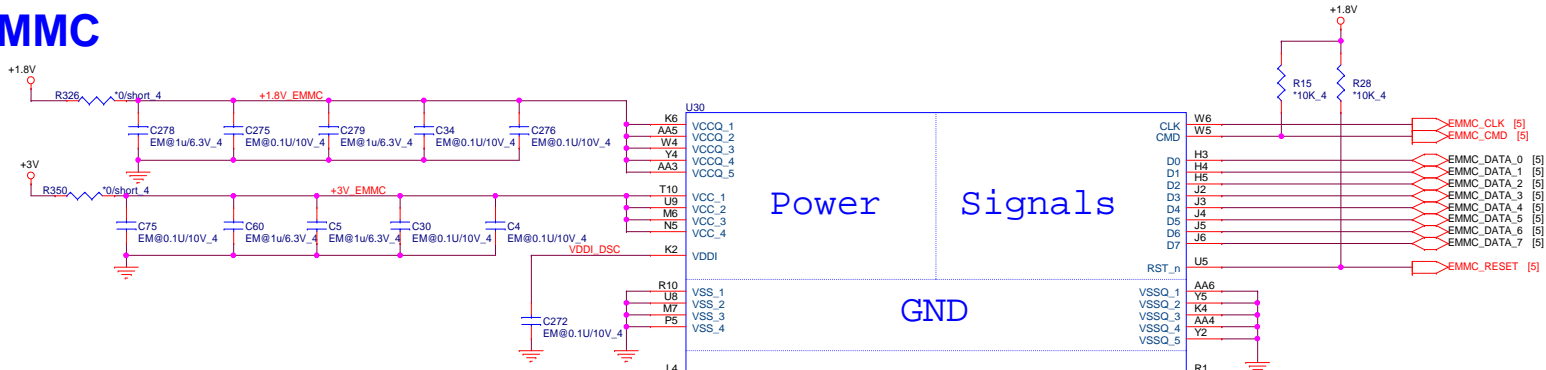


TPM_N for 新唐
 TPM_I for 英飛凌 --- default



note: serie need to add level shift

eMMC

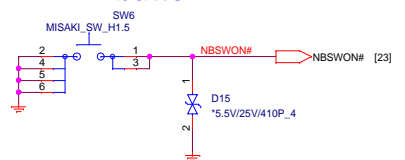


Vendor	P/N
SAMSUNG 64G	AKE3TZPT506
Samsung 32G	AKE5SZ0T501
HYNIX 64G	AKE34GPTW00
HYNIX 32G	AKE34ZPTW00
Sandisk 32G	AKE3SZ-T105

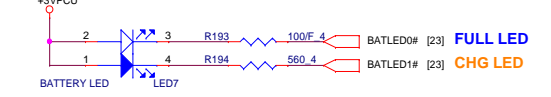
- A1_Index
- NC_1
- NC_2
- NC_3
- NC_4
- NC_5
- NC_6
- NC_7
- NC_8
- NC_9
- NC_10
- NC_11
- NC_12
- NC_13
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- NC_67
- NC_68
- NC_69

- +5V [13,19,32]
- +3VPCU [6,8,13,15,19,23,25,26,27,32]
- +3V [4,7,9,11,12,13,14,15,17,19,20,21,23,30,32]
- +3V_S5 [2,9,12,14,15,17,21,23,29,30,32]

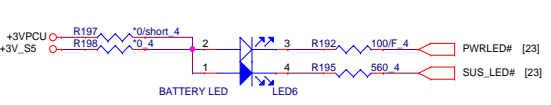
PWR button



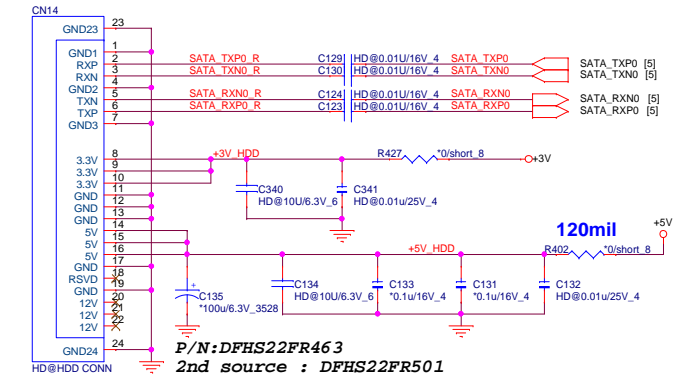
Battery indicator



PWR indicator

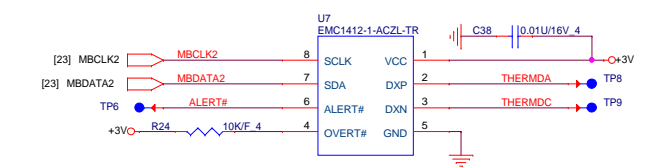


SATA HDD



P/N:DFHS22FR463
2nd source : DFHS22FR501

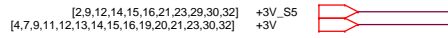
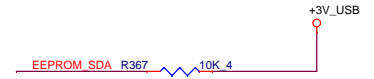
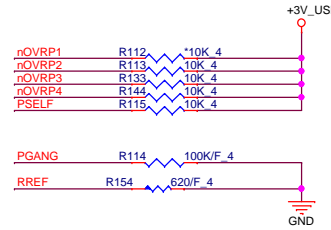
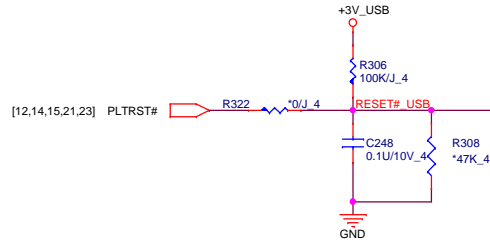
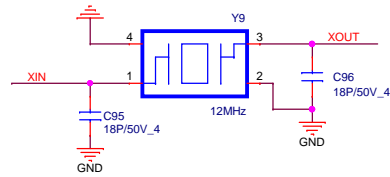
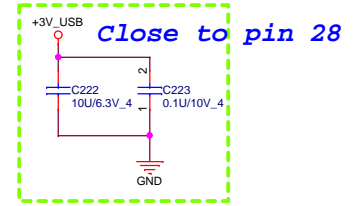
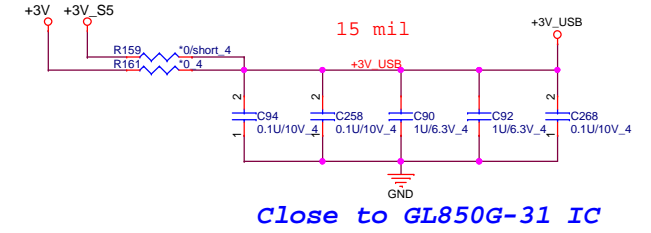
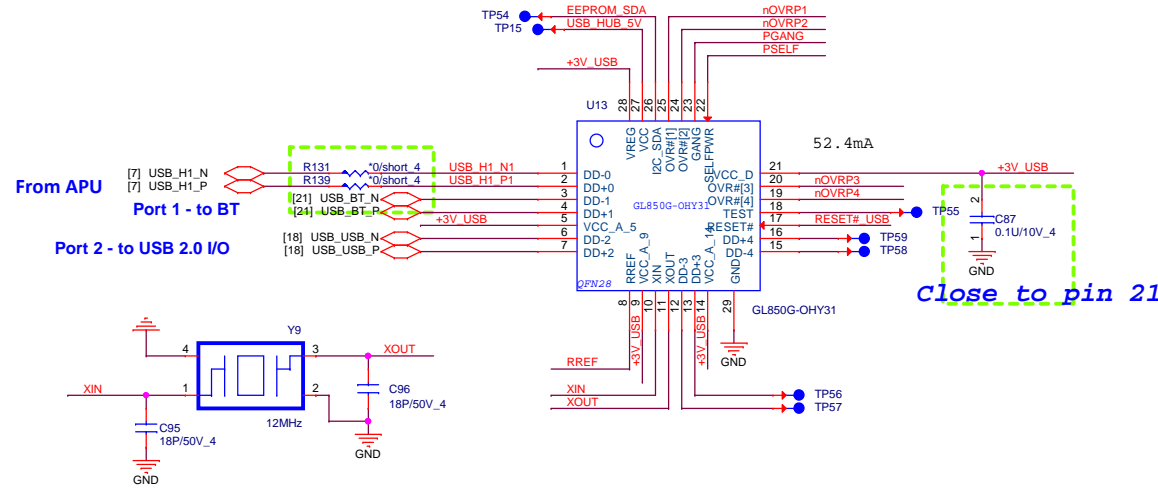
CPU Thermal sensor(THS) / MB Local TEMP




Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

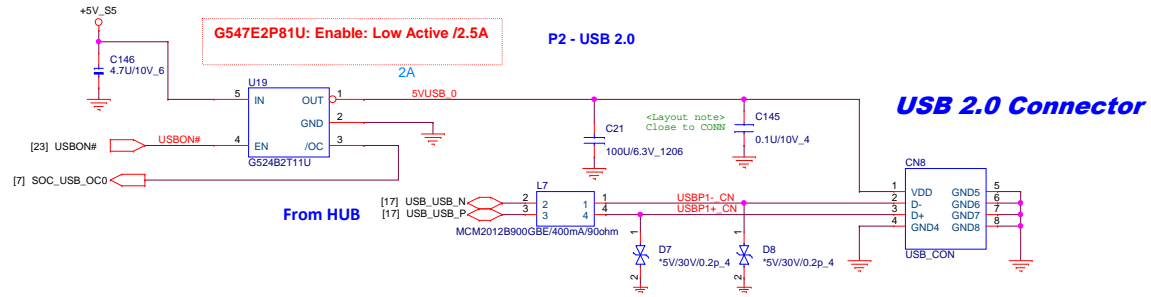
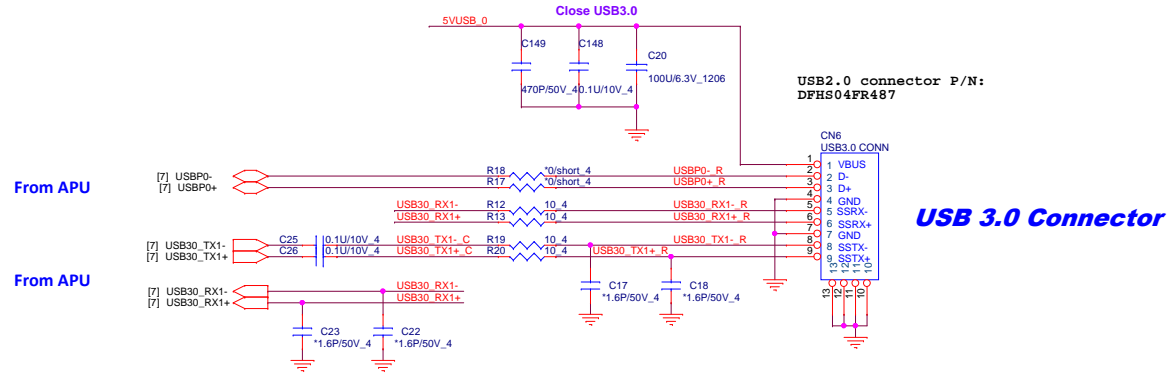
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	HDD/HalVeMMC/LED	1A
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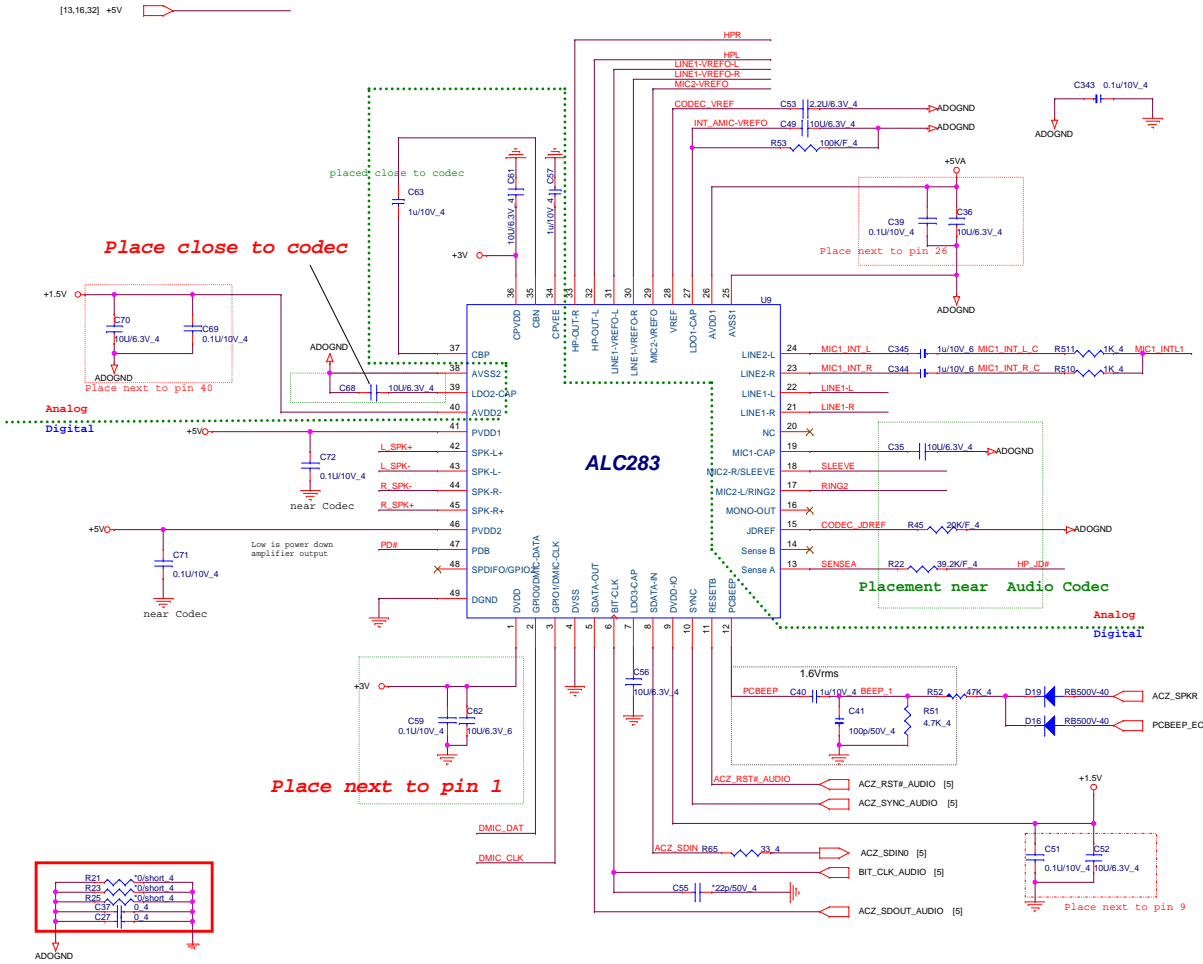


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Size	Document Number	Rev
	USB HUB -1	1A
Date:	Monday, June 30, 2014	Sheet 17 of 33

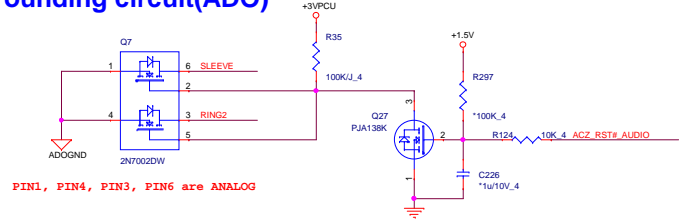
[6,26,28,29,30,31,32] +5V_S5



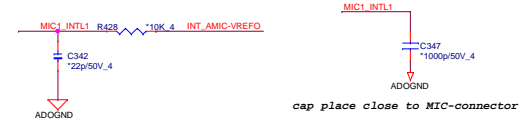
Codec(ADO)



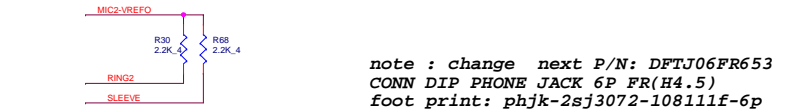
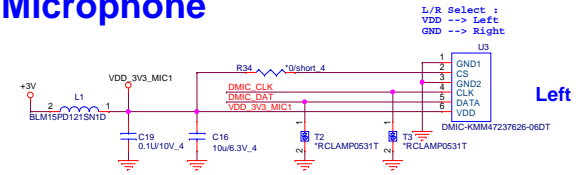
Grounding circuit(ADO)



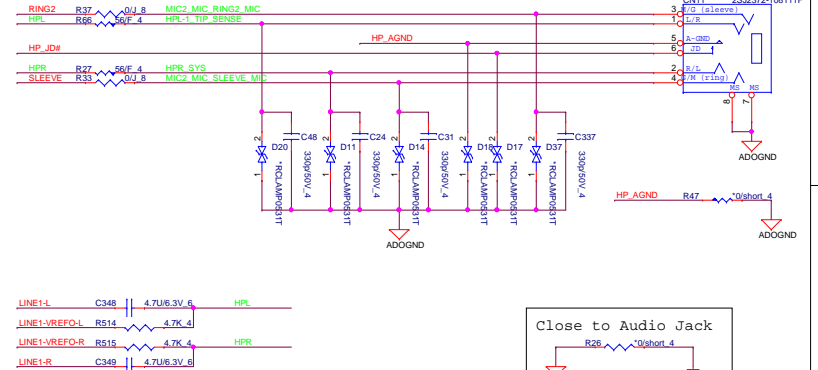
INT MIC array



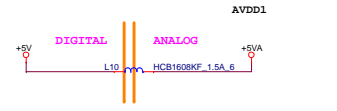
Microphone



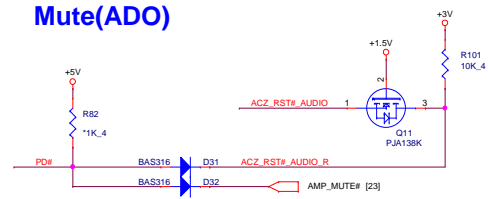
HP_MIC 上/下/左/右包裹AGND



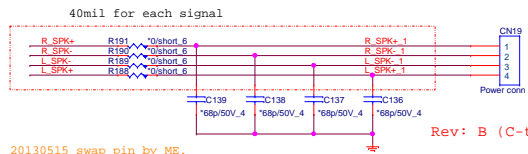
Codec PWR 5V(ADO)



Mute(ADO)



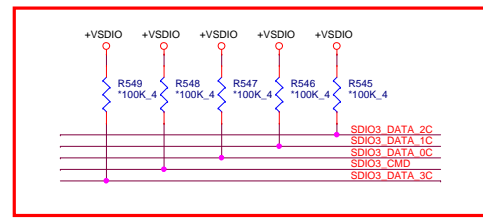
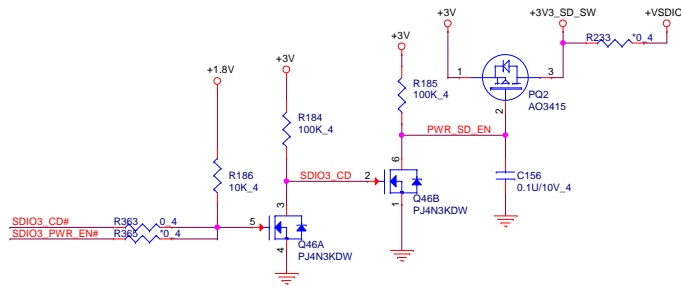
Internal Speaker



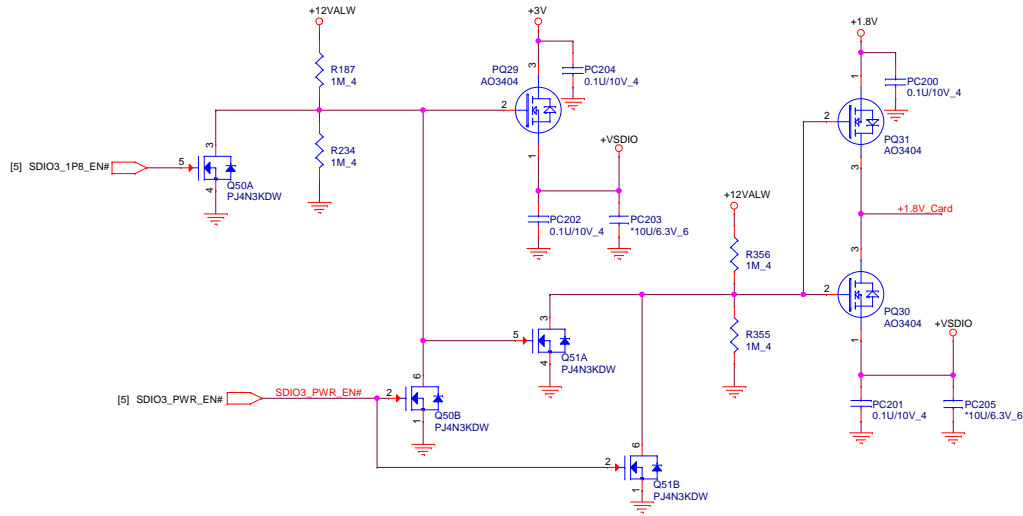
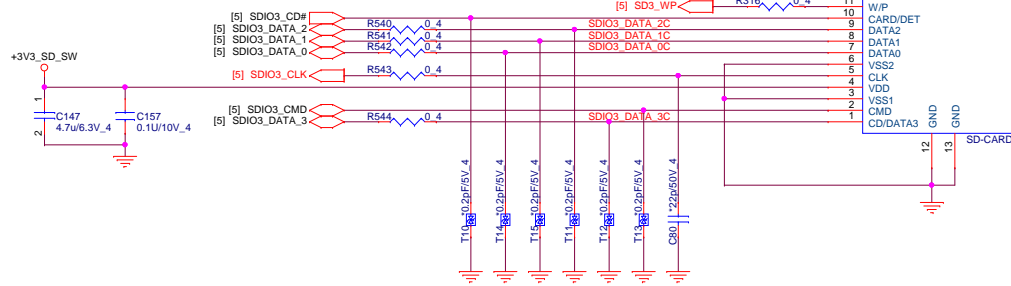
20130515 swap pin by ME.

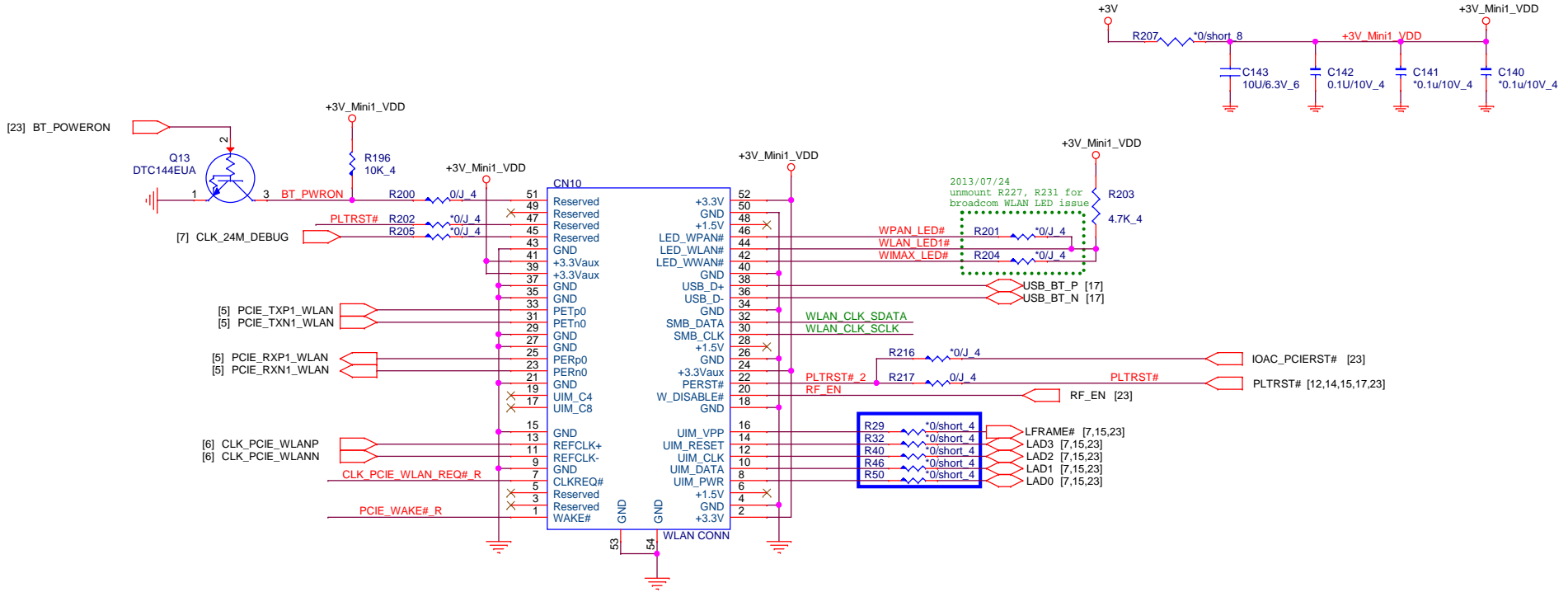
footprint 88266-040xx-xxx-4p-1

Rev: B (C-test) CN19 change ACS P/N from DFHD04MRA75 to DFHD04MR211



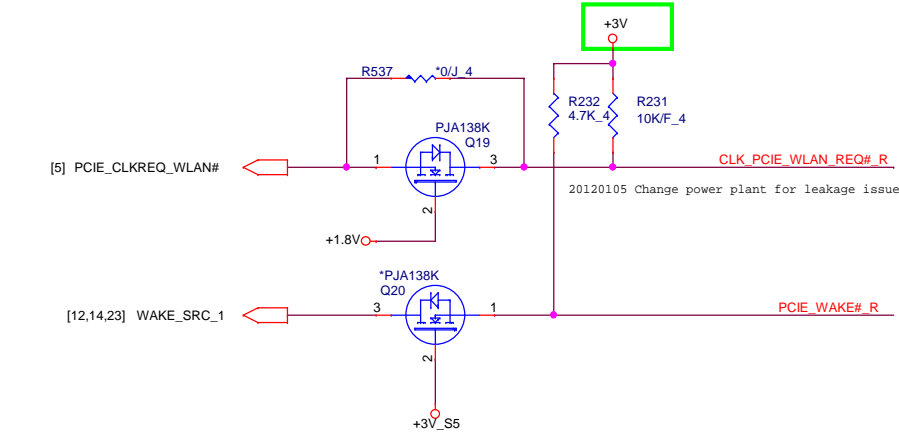
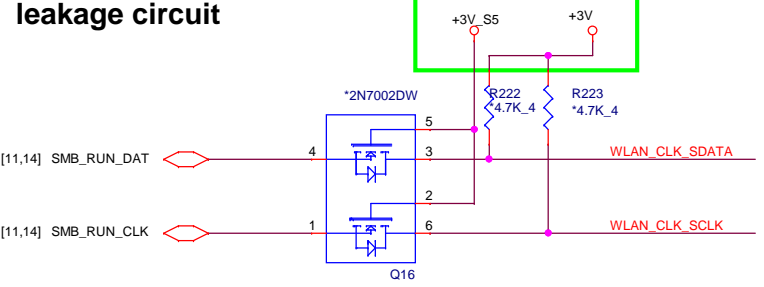
SD_CARD_DET_N
 L: Card inserted
 H: Card remove





leakage circuit

20120105 Change power plant for leakage issue.



- [4,5,6,7,9,12,13,14,15,16,20,23,32] +1.8V
- [4,7,9,11,12,13,14,15,16,17,19,20,23,30,32] +3V
- [2,9,12,14,15,16,17,23,29,30,32] +3V_S5

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HG-TC256BC354D118P2

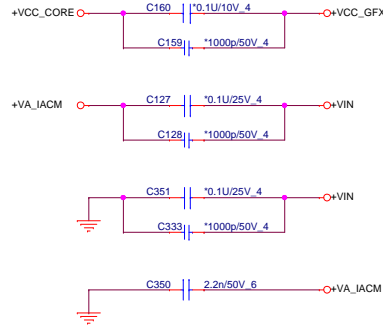
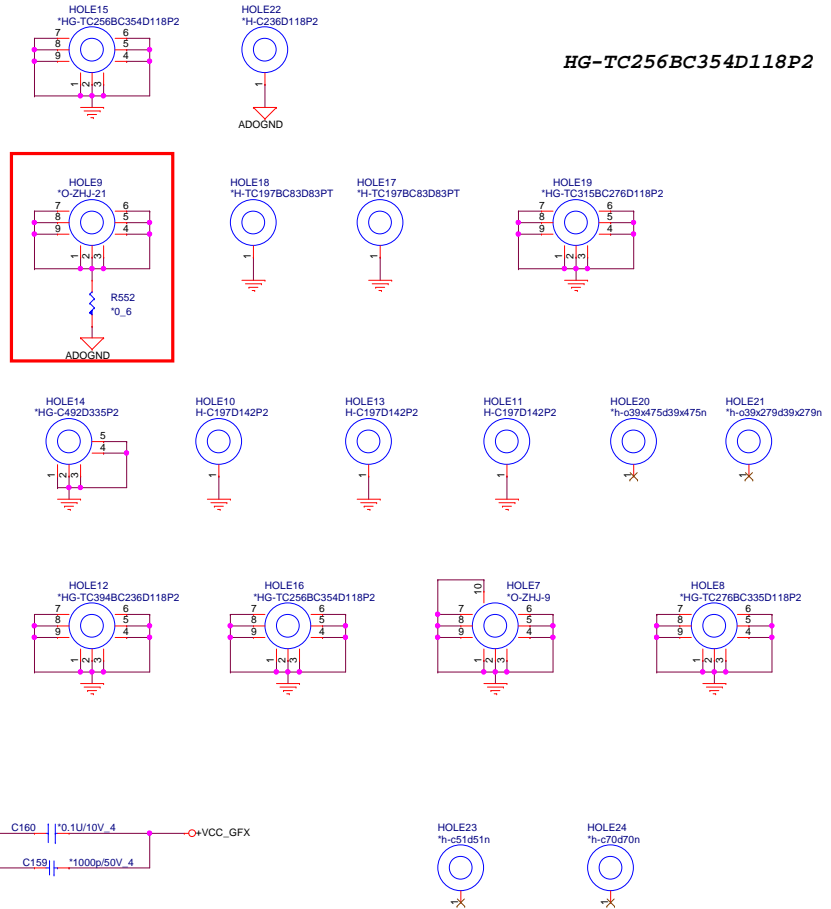
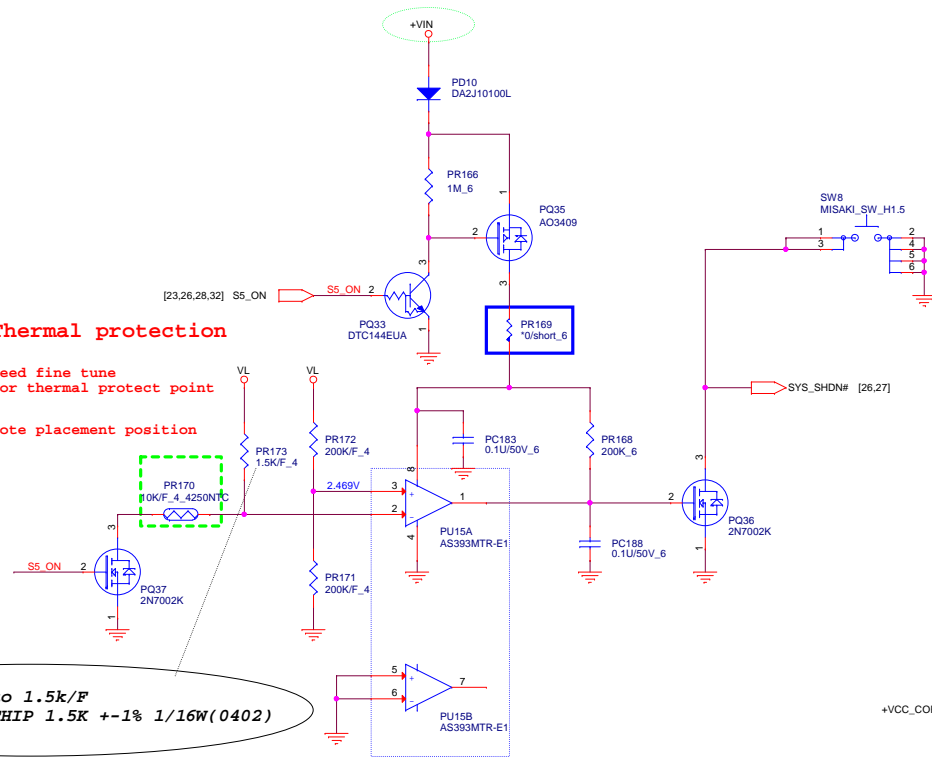
Thermal protection

Need fine tune for thermal protect point

Note placement position

note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K +-1% 1/16W(0402)

For EC control thermal protection (output 3.3V)

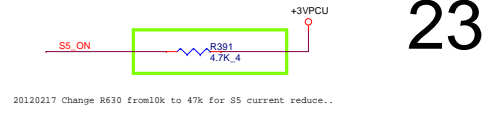


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Thermal / Hole		
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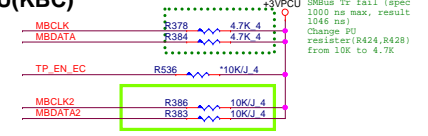
1.8V p/n: AJ009850F02
Description: IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

Note:
GPIO75 EMU_LIDTouch pad enable/disable#Follow Z&A -->ZHJ None
TP_EN_EC TP_EN_ECTouch pad enable/disable# -->ok
GPIO27 TP_INT_EC#Touch pad interrupt

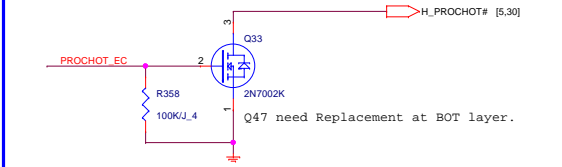


20120217 Change R630 from 10k to 47k for S5 current reduce..

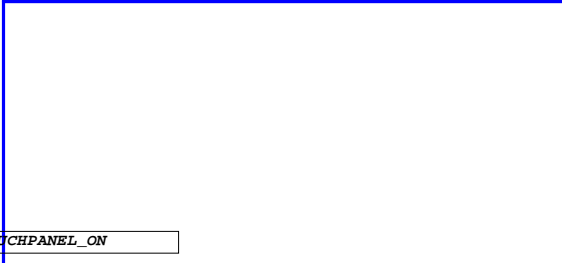
SM BUS PU(KBC)



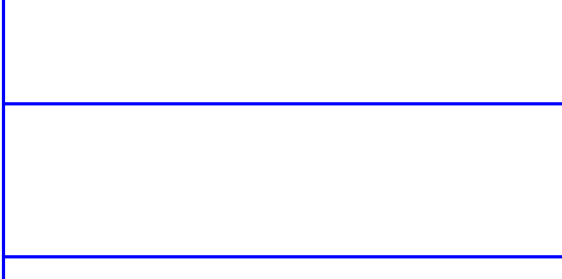
2013/07/31
SMbus Tr fail (spec 1000 ns max, result 1046 ns)
Change PU resistor (R424, R428) from 10K to 4.7K



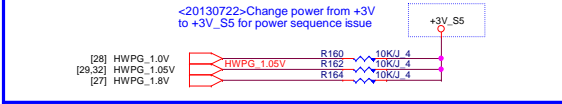
Q47 need Replacement at BOT layer.



Note: GPIO75 (pin82) for TOUCHPANEL_ON
pin91 in 985L is 1.8V only



<20090721_FAE suggestion>
Stuff 100K and close to EC side for improving power consumption

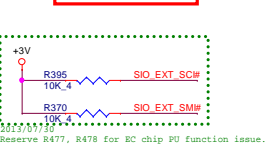
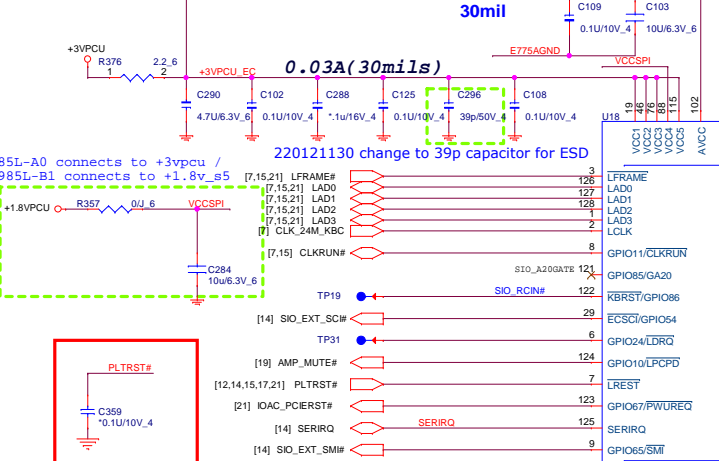


<20130722>Change power from +3V to +3V_S5 for power sequence issue

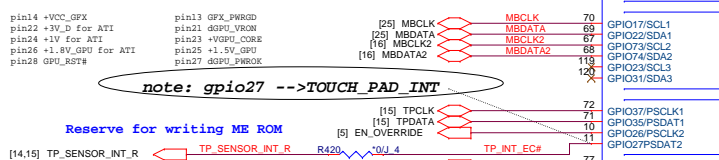
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

EC(KBC)

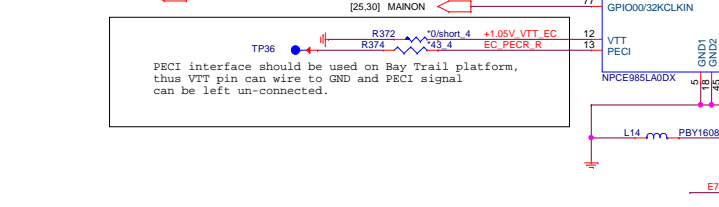


Reserve R477, R478 for EC chip PU function issue.

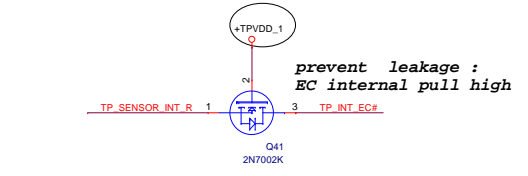


note: gpio27 -->TOUCH_PAD_INT

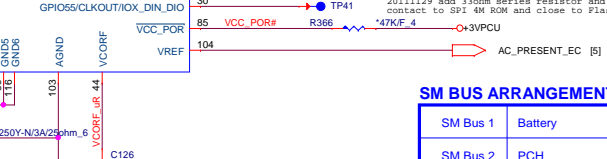
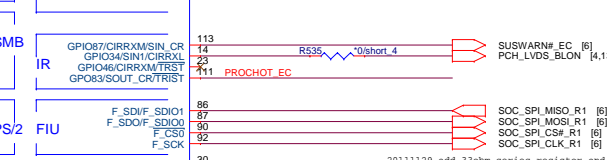
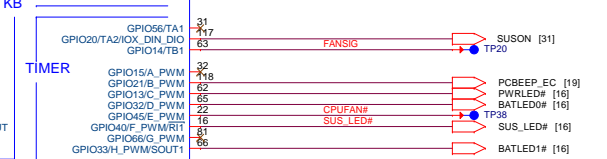
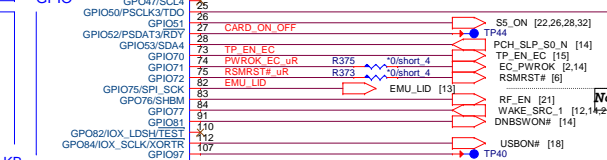
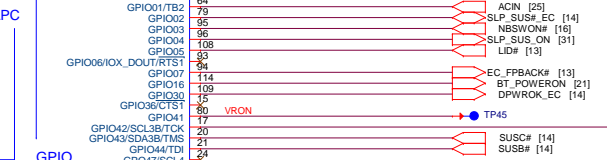
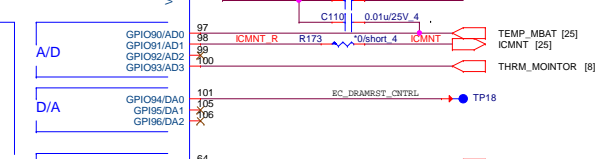
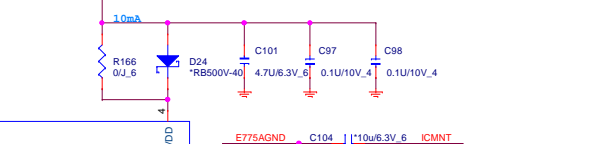
Reserve for writing ME ROM



PCI interface should be used on Bay Trail platform, thus VTT pin can wire to GND and P8C2 signal can be left un-connected.

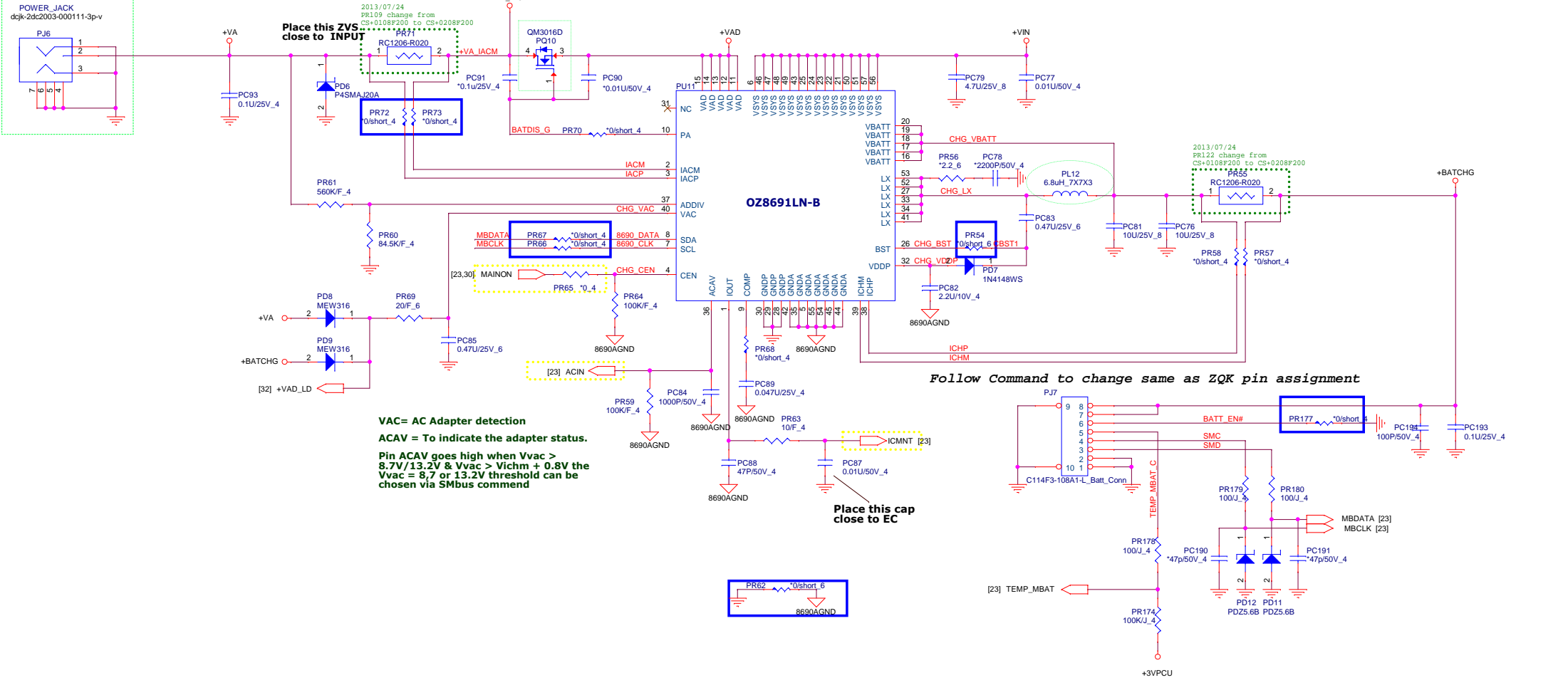
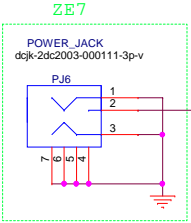


prevent leakage : EC internal pull high



Bay Trail-M S4/S5 to S0 (Power Up) Sequence





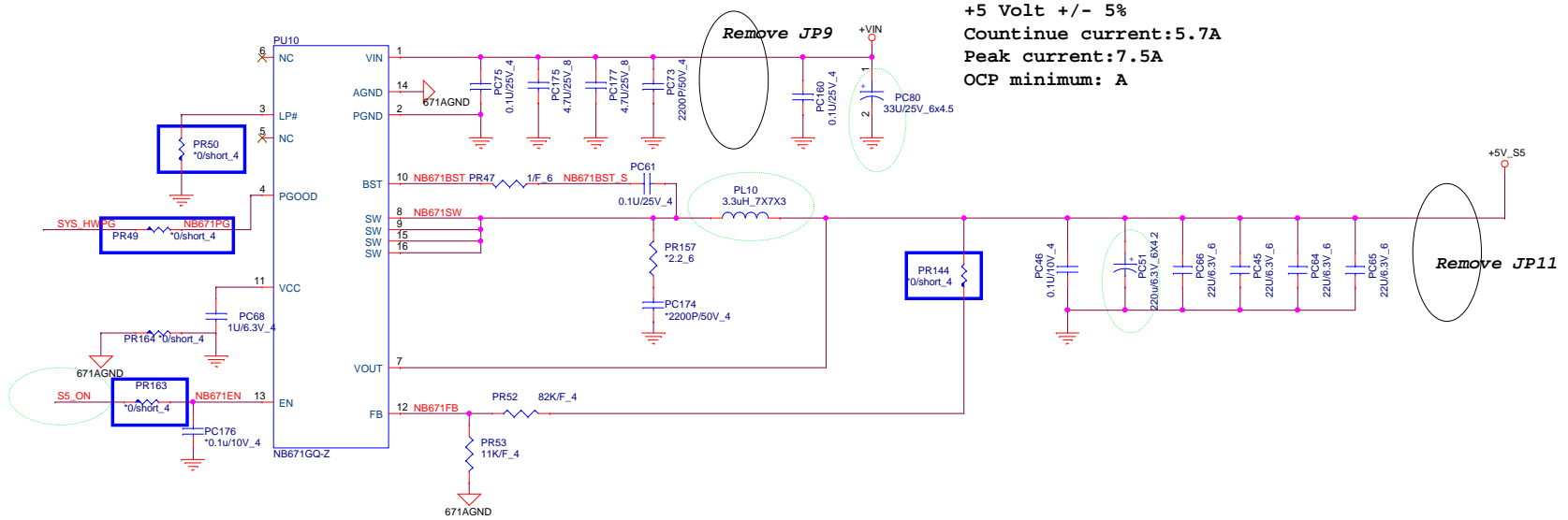
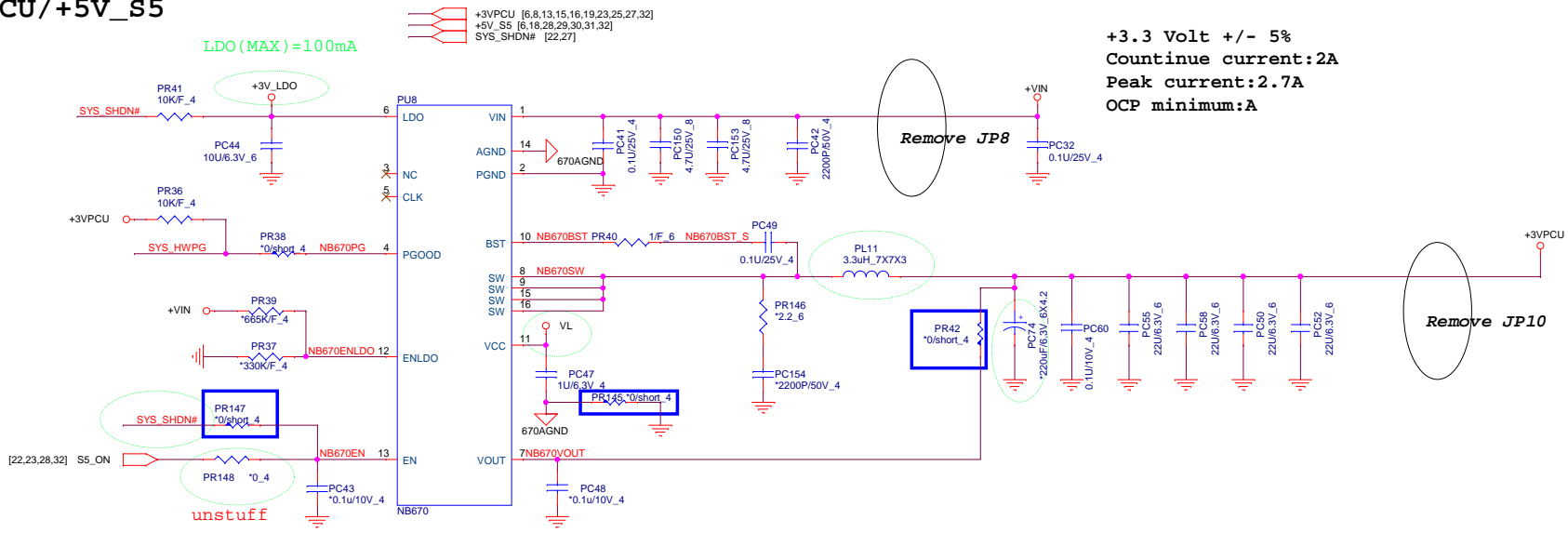
VAC= AC Adapter detection
ACAV = To indicate the adapter status.
Pin ACAV goes high when Vvac > 8.7V/13.2V & Vvac > Vichm + 0.8V the Vvac = 8,7 or 13.2V threshold can be chosen via Smbus command

Follow Command to change same as ZQK pin assignment

Place this cap close to EC

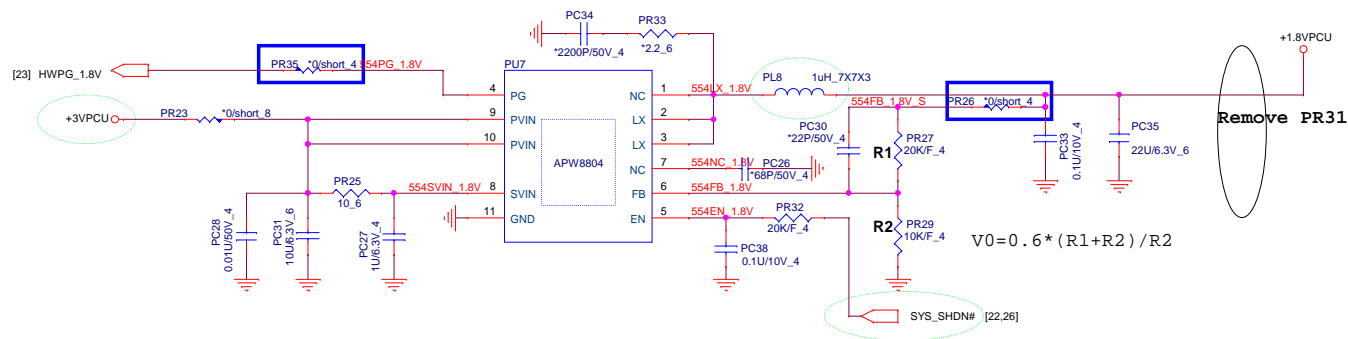
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DC/DC +3VPCU/+5V_S5



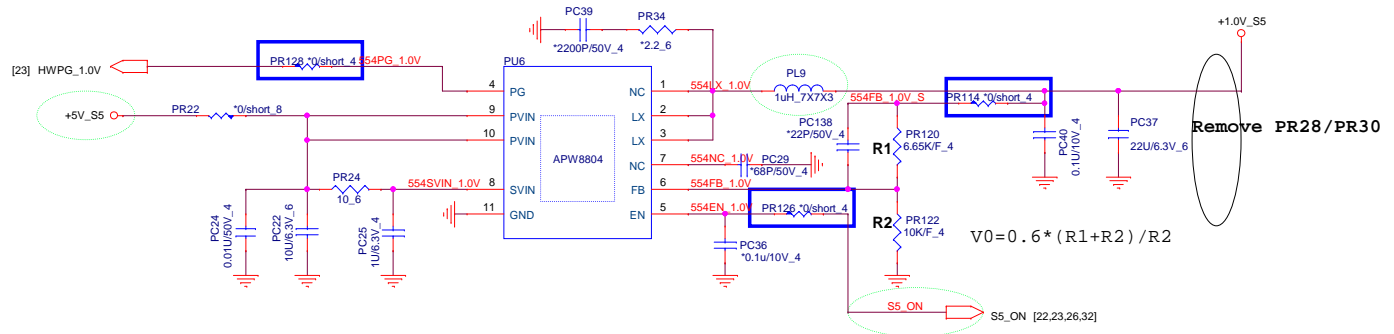
[14,23,32] +1.8VPCU
 [6,8,13,15,16,19,23,25,26,32] +3VPCU

+1.8V Volt +/- 5%
 Countinue current:0.08A
 Peak current:0.11A
 OCP minimum:A

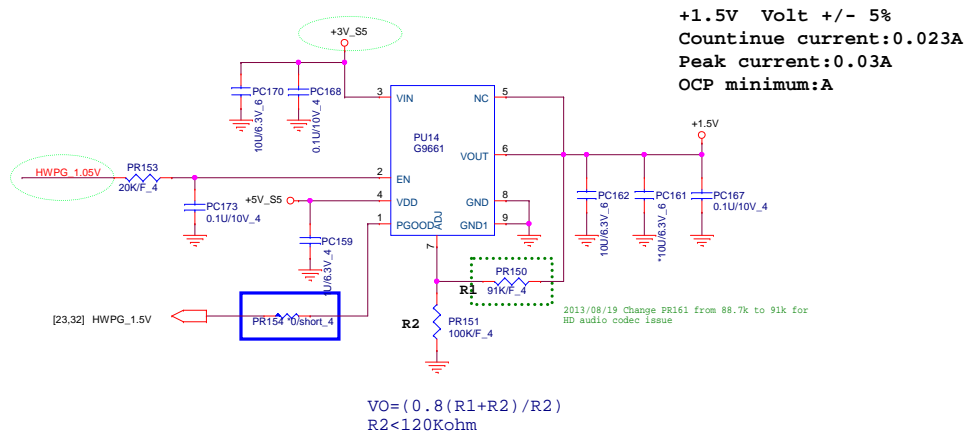
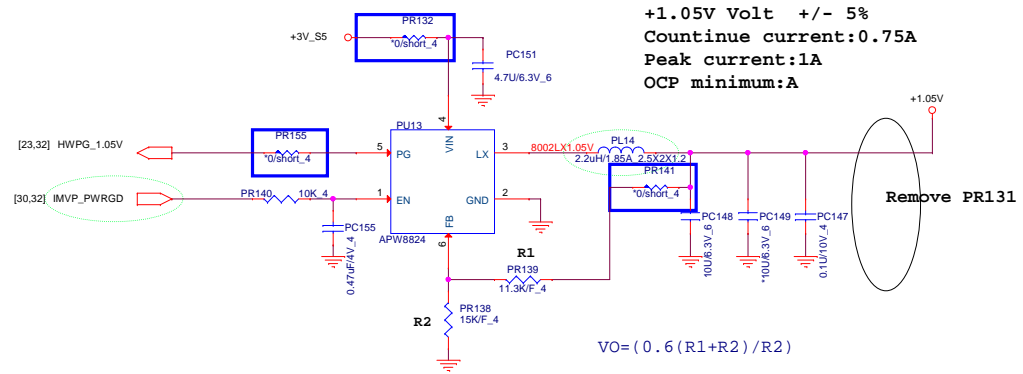


+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A

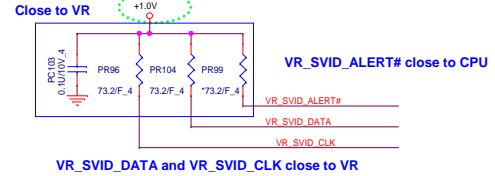
[9,32] +1.0V_S5
[6,18,26,29,30,31,32] +5V_S5



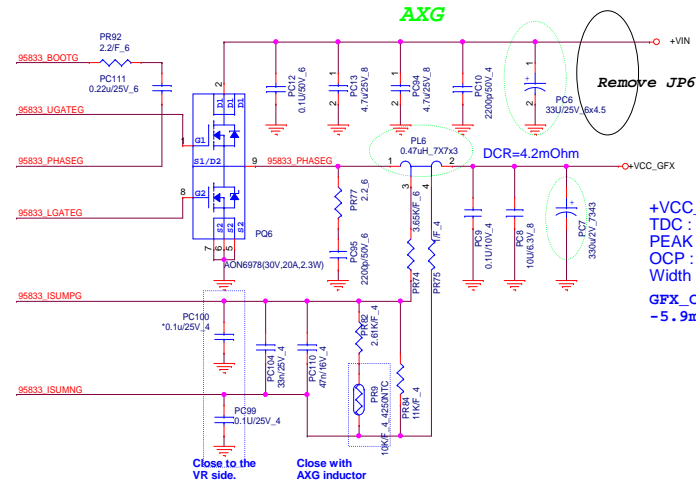
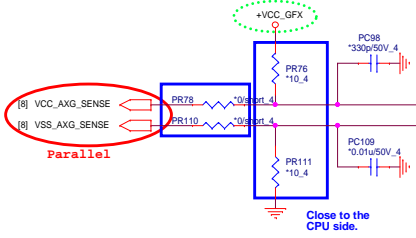
- [2,9,12,14,15,16,17,21,23,30,32] +3V_S5
- [9] +1.05V
- [9,19] +1.5V



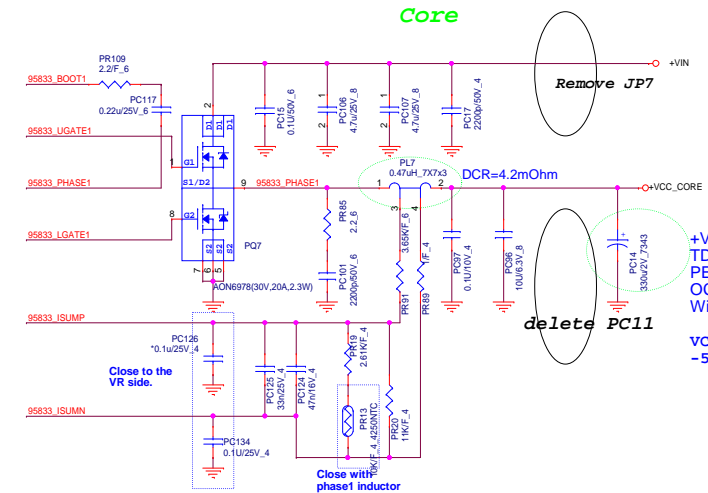
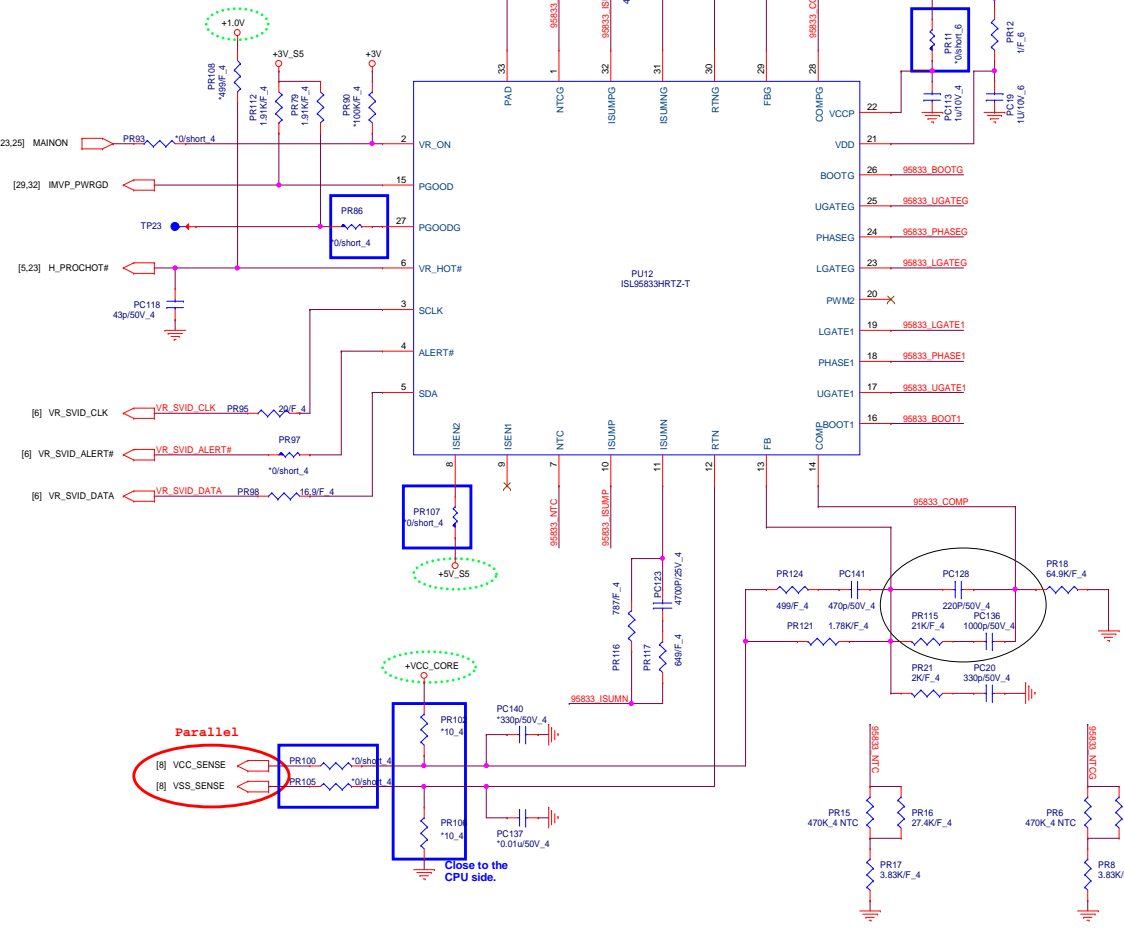
20130617 Change +1.05V to +1.0V



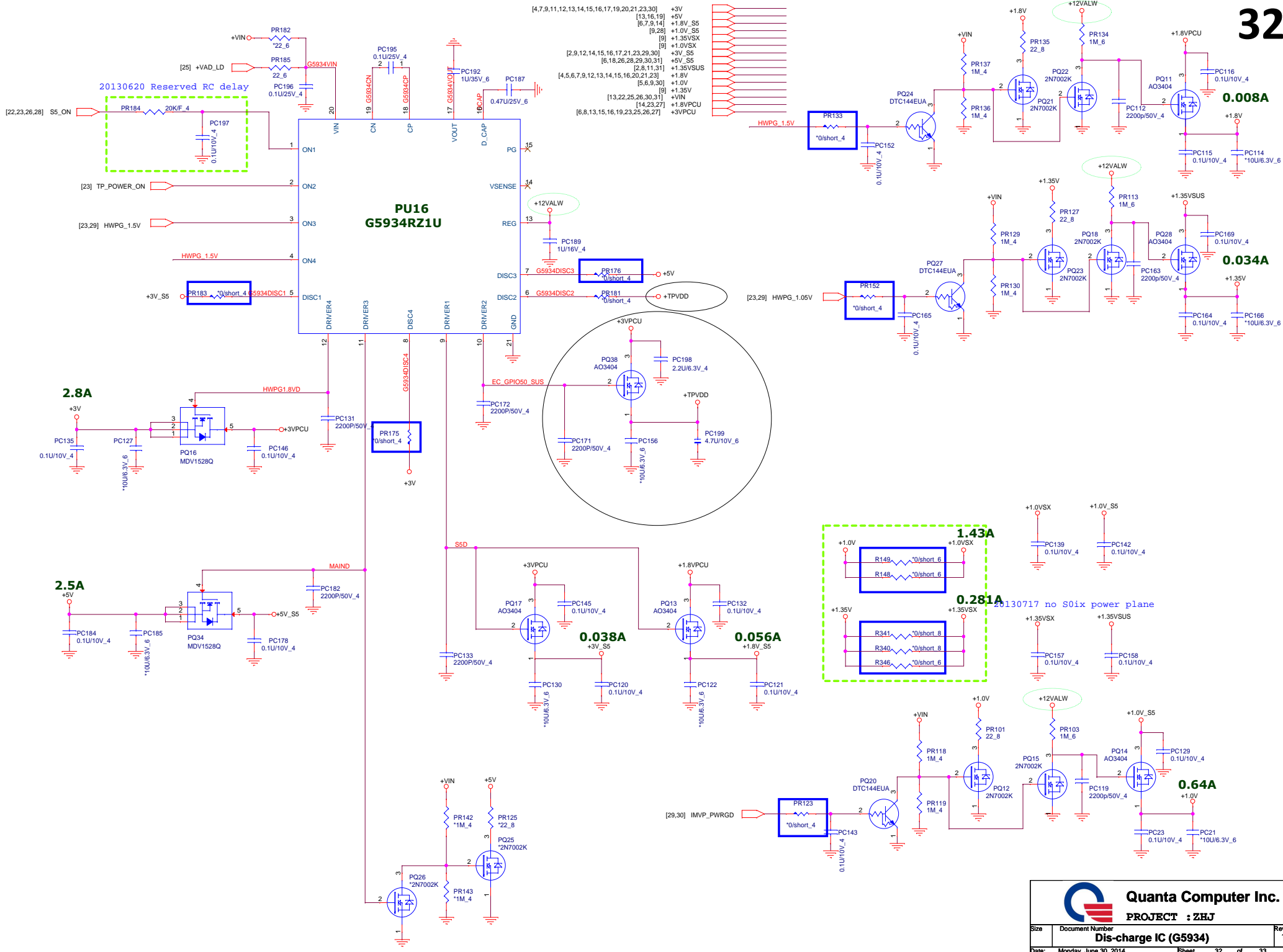
- [5,6,9,32] +1.0V
- [8,22] +VCC_GFX
- [13,22,25,26,31,32] +VIN
- [6,18,26,28,29,31,32] +5V_S5



+VCC_GFX
 TDC : A
 PEAK : 14A
 OCP : A
 Width : mil
 GFX_CORE Load Line :
 -5.9mV/A for 2.xW SDP



+VCC_CORE
 TDC : A
 PEAK : 12A
 OCP : A
 Width : mil
 CORE Load Line :
 -5.9mV/A for 2.xW SDP



CHANGE LIST

Model


Version

ZHK

3A

1. Stuff C27 & C37 for ESD. (page19)
2. Reserve CS9 for EMI (page21)
3. R361 Change 0 OHM to 2.2-ohm for ESD(page13)
4. Reserve RS45 ,RS46 ,RS47 ,RS48 & RS49 for Cardread function(page20)
5. Reserve RS52 for ESD (page21)
6. Reserve R70 & R71 for eDP AUX (page13)
7. Add PQ31 for cardread function.

DOC NO.	PROJECT MODEL	ZHK	APPROVED BY:	DATE:
	PART NUMBER:		DRAWING BY:	REVISION:



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PROJECT : ZHK
Change list

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