

VM9M Block Diagram Intel UMA

VER : F3B

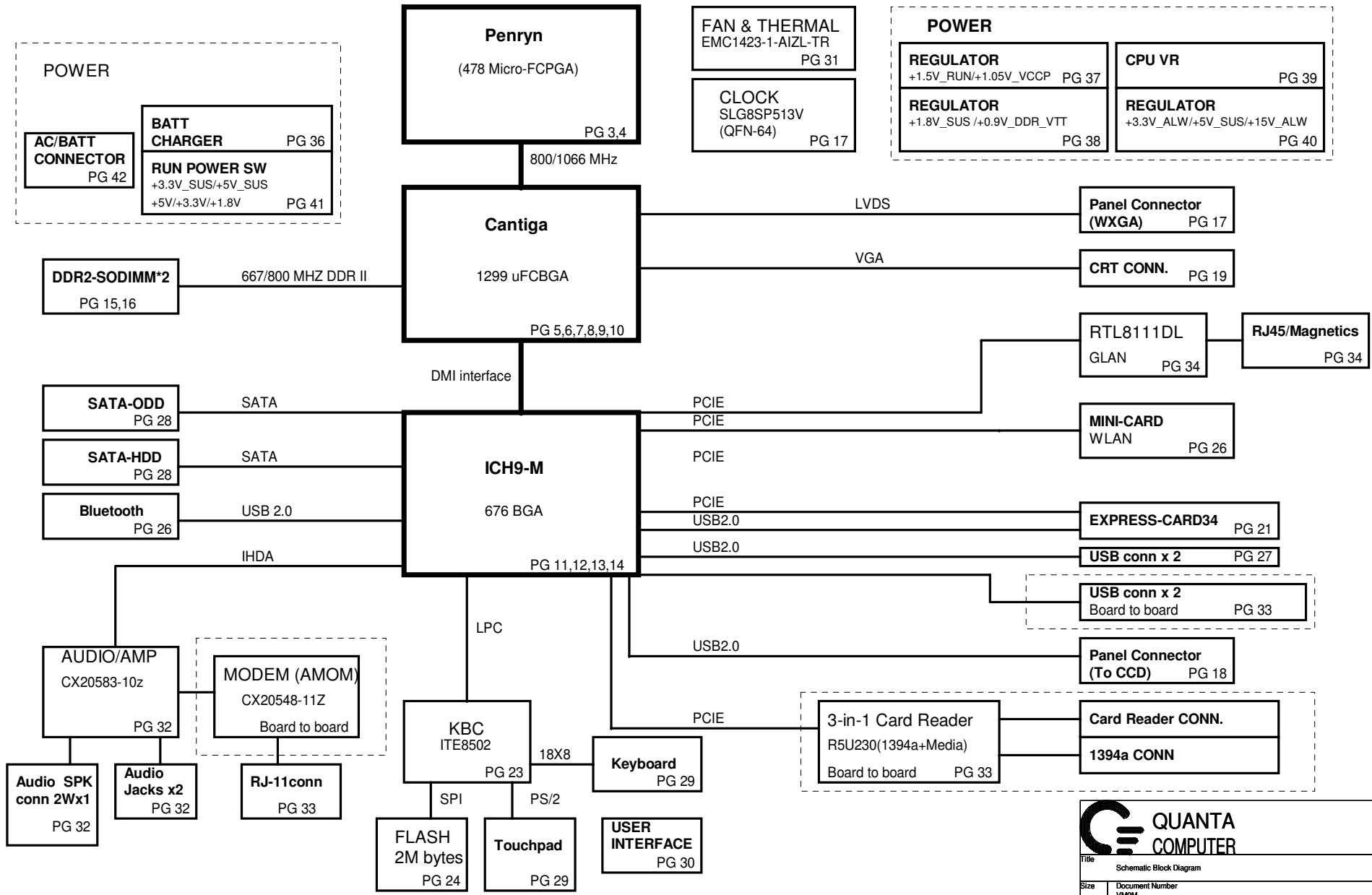



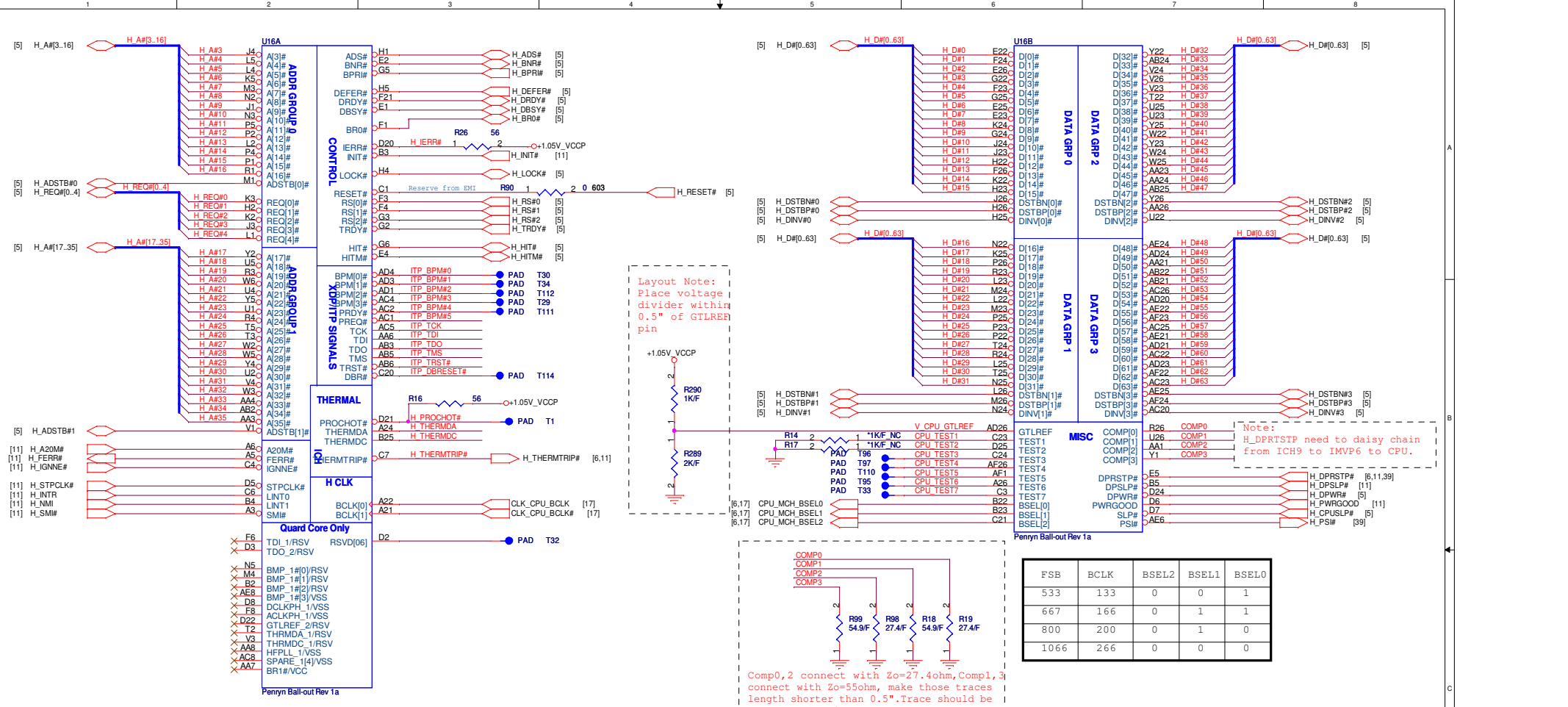
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Power States

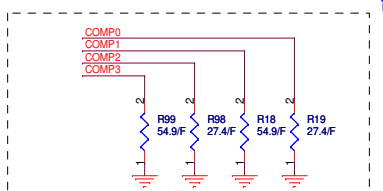
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,18,24,36,37,3,8,39,40,44	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,23,24	RTC		S0~S5
+3.3V_ALW	+3.3V	3,23,24,30,35,36,38,40,41,42,45	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	37,38,40,41,42	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	11,18,40,41	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	34	LAN POWER		
+5V_SUS	+5V	14,27,30,39,40,41,44	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,18,25,30,37,39,41,45	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,37,38,41	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,38,41	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,19,21,25,28,29,30,31,32,41,44	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,30,31,32,34,18,19,20,21,23,25,26,28,41,44,45	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,26,37,41,44	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,6,8,9,11,14,37,44	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,39	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	18	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	28	Module Power		
+5V_HDD	+5V	28	HDD Power		
+PBATT	+10V~+17V	42	MAIN BATTERY	CHG_PBATT	

GND PLANE	PAGE	DESCRIPTION
 GND	ALL	



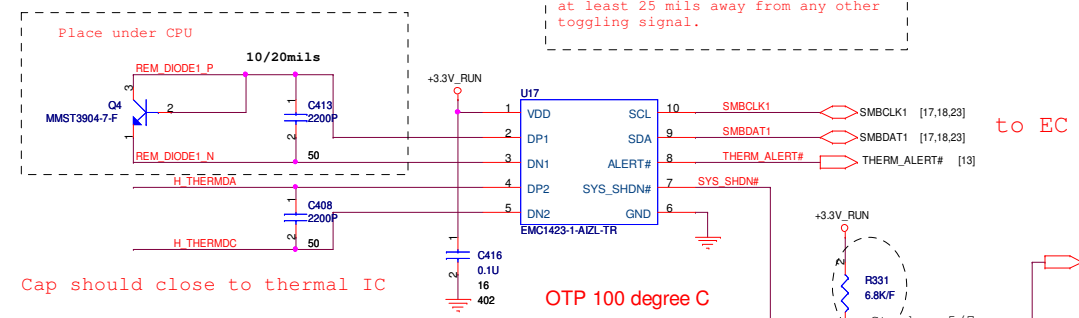
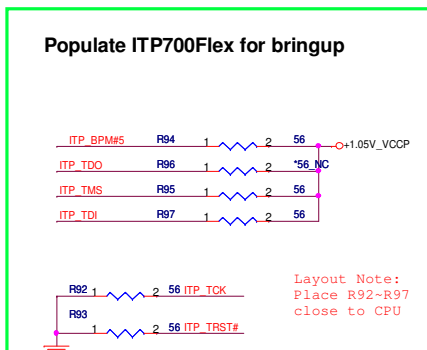
Layout Note:
Place voltage divider within 0.5" of GTLREF pin

Note:
H_DPRSTP need to daisy chain from ICH9 to INV6 to CPU.



Comp0,2 connect with Zo=27.4ohm, Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

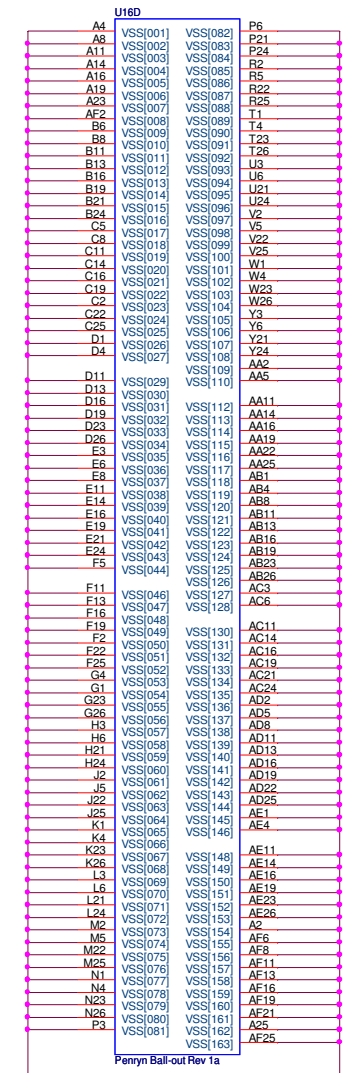
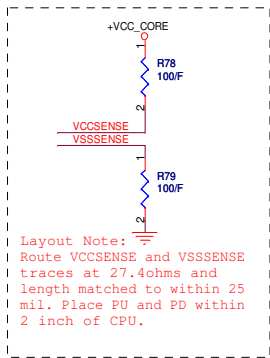
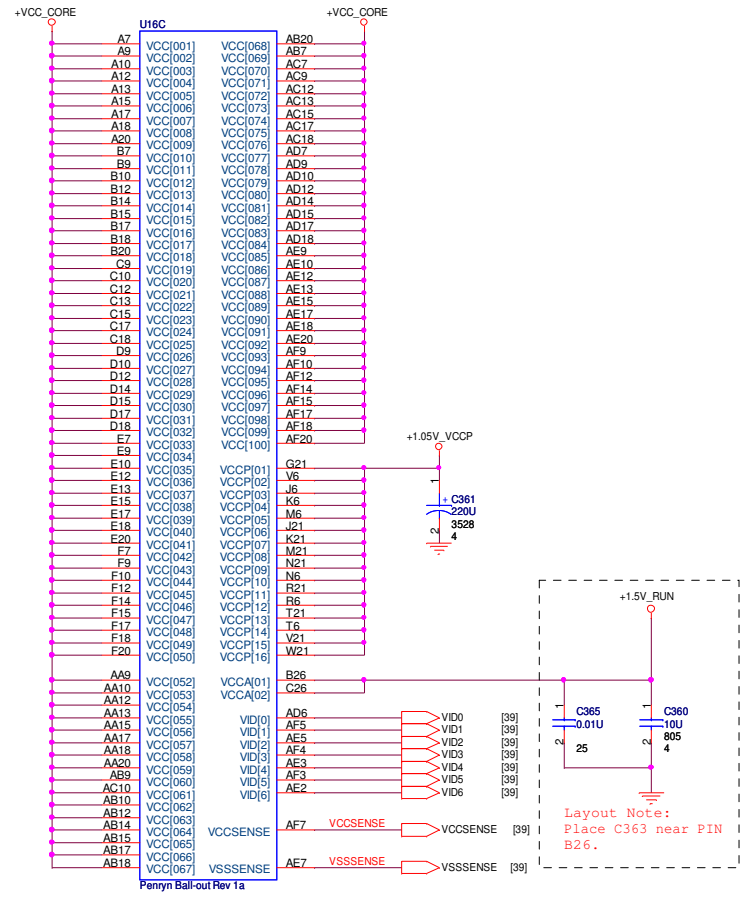
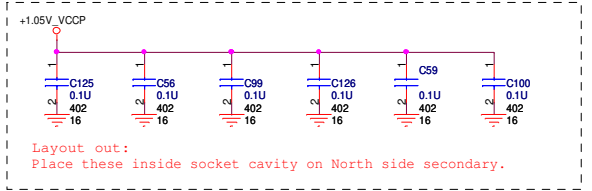
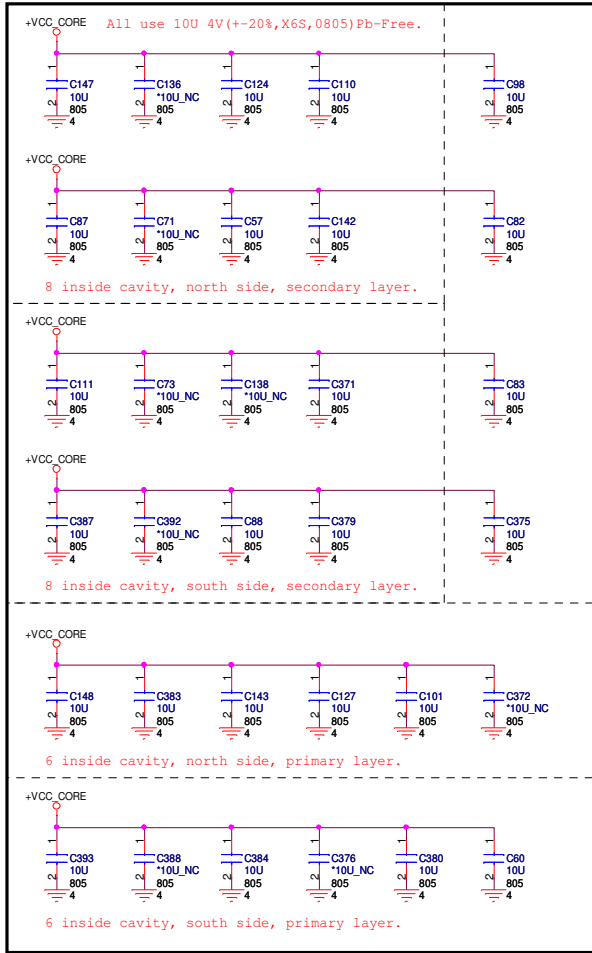


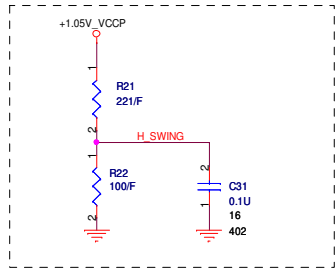
QUANTA COMPUTER

Title: Penryn Processor (HOST BUS)

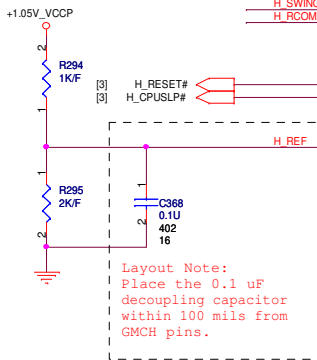
Size	Document Number	Rev
	VMSM	1A

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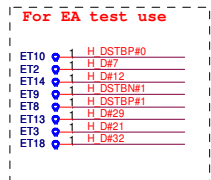
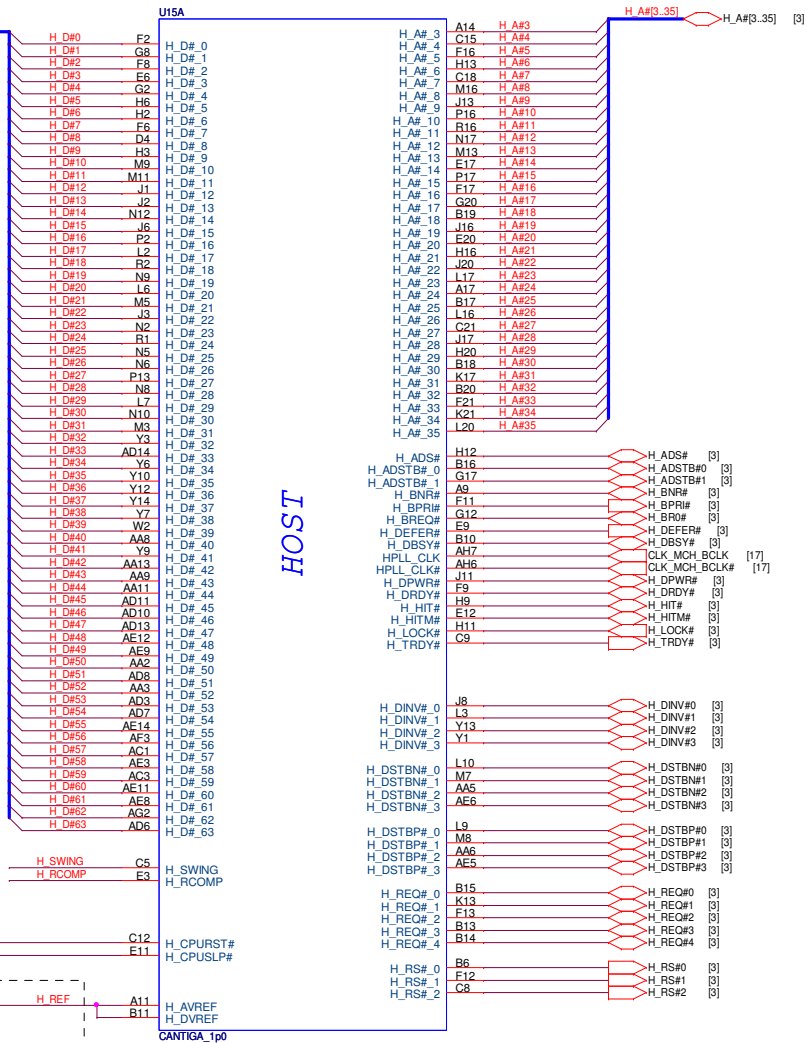




Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.



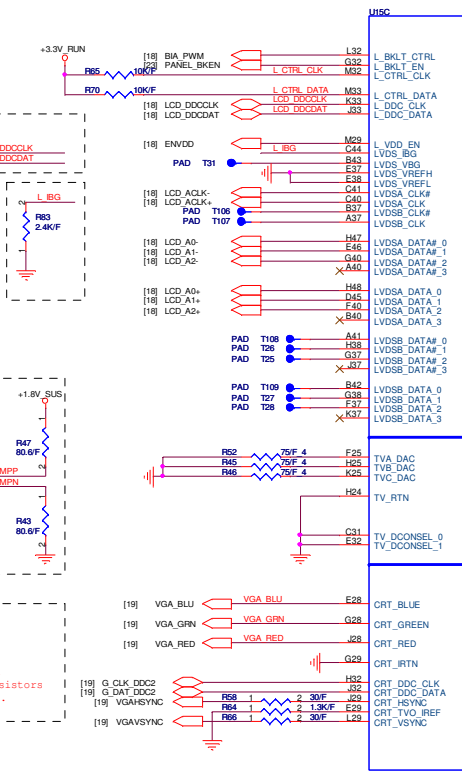
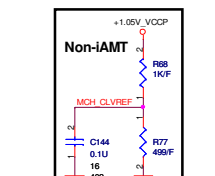
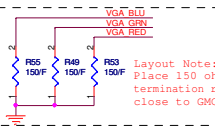
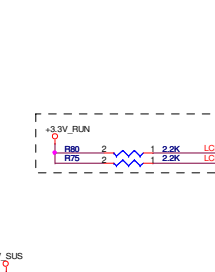
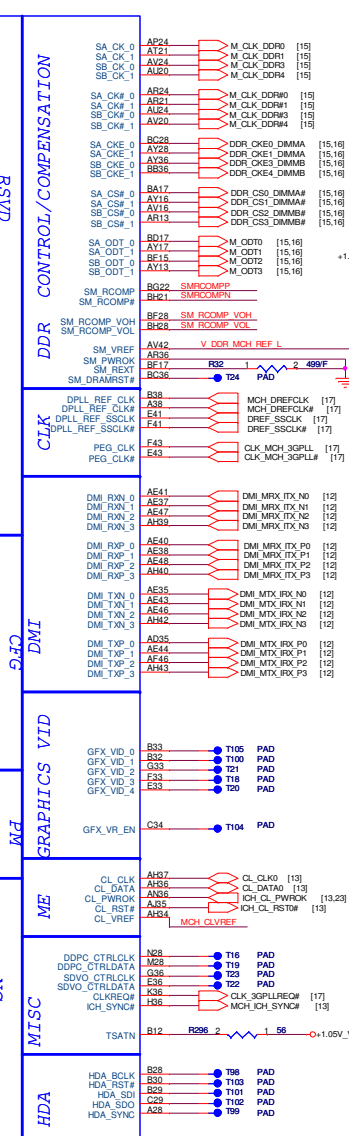
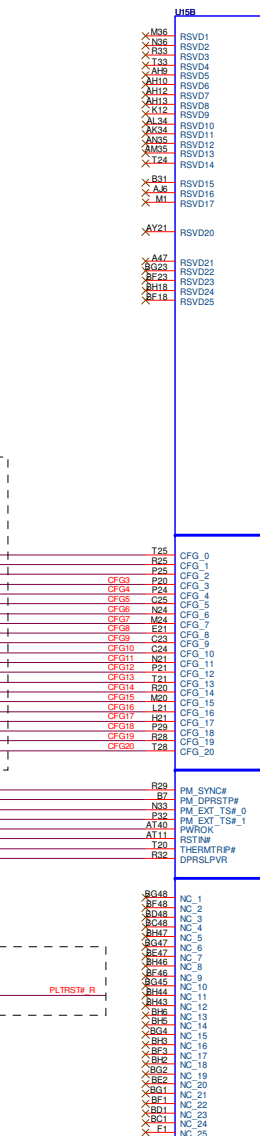
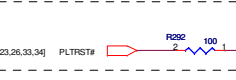
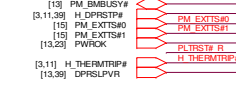
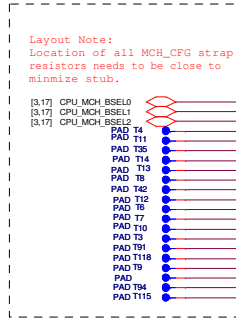
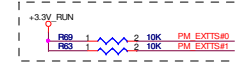
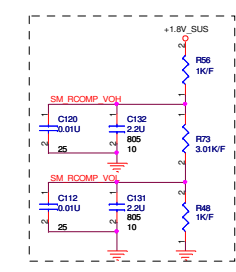
Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.



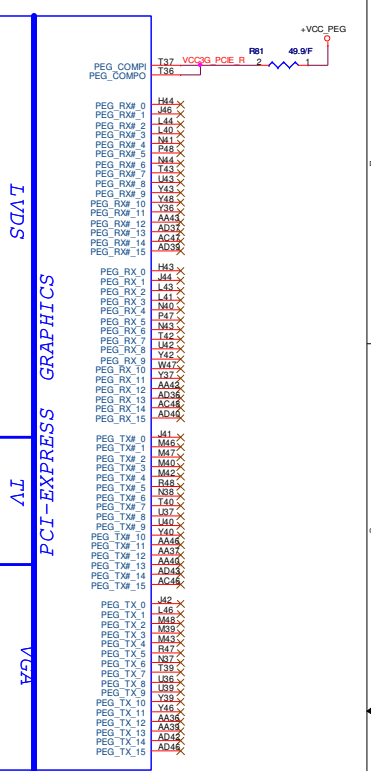
Title: Cantiga (HOST)

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Signal	Function	Default
CFG5	DMI X2 Select	Low=DMiX2 High=DMiX4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIe is operational (defaults) High=SDVO and PCIe are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present



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[15] DDR_A_D[0..63]

DDR A D0	AJ38	SA DO_0
DDR A D1	AJ41	SA DO_1
DDR A D2	AN38	SA DO_2
DDR A D3	AM38	SA DO_3
DDR A D4	AJ36	SA DO_4
DDR A D5	AJ46	SA DO_5
DDR A D6	AM44	SA DO_6
DDR A D7	AM42	SA DO_7
DDR A D8	AN43	SA DO_8
DDR A D9	AN44	SA DO_9
DDR A D10	AU40	SA DO_10
DDR A D11	AT38	SA DO_11
DDR A D12	AN41	SA DO_12
DDR A D13	AN39	SA DO_13
DDR A D14	AU44	SA DO_14
DDR A D15	AU42	SA DO_15
DDR A D16	AV39	SA DO_16
DDR A D17	AY44	SA DO_17
DDR A D18	BA40	SA DO_18
DDR A D19	BD43	SA DO_19
DDR A D20	AV41	SA DO_20
DDR A D21	AY43	SA DO_21
DDR A D22	BB41	SA DO_22
DDR A D23	BC40	SA DO_23
DDR A D24	AY37	SA DO_24
DDR A D25	BD38	SA DO_25
DDR A D26	AV37	SA DO_26
DDR A D27	AT36	SA DO_27
DDR A D28	AY39	SA DO_28
DDR A D29	BB38	SA DO_29
DDR A D30	BB38	SA DO_30
DDR A D31	AV36	SA DO_31
DDR A D32	BD13	SA DO_32
DDR A D33	AU11	SA DO_33
DDR A D34	BC11	SA DO_34
DDR A D35	BA12	SA DO_35
DDR A D36	AU13	SA DO_36
DDR A D37	AV13	SA DO_37
DDR A D38	BD12	SA DO_38
DDR A D39	BC12	SA DO_39
DDR A D40	BB9	SA DO_40
DDR A D41	BA9	SA DO_41
DDR A D42	AU10	SA DO_42
DDR A D43	AV9	SA DO_43
DDR A D44	BA11	SA DO_44
DDR A D45	BD9	SA DO_45
DDR A D46	AV8	SA DO_46
DDR A D47	BA6	SA DO_47
DDR A D48	AV5	SA DO_48
DDR A D49	AV7	SA DO_49
DDR A D50	AT9	SA DO_50
DDR A D51	AN8	SA DO_51
DDR A D52	AU5	SA DO_52
DDR A D53	AU6	SA DO_53
DDR A D54	AT5	SA DO_54
DDR A D55	AN10	SA DO_55
DDR A D56	AM11	SA DO_56
DDR A D57	AM5	SA DO_57
DDR A D58	AJ9	SA DO_58
DDR A D59	AJ8	SA DO_59
DDR A D60	AN12	SA DO_60
DDR A D61	AM13	SA DO_61
DDR A D62	AJ11	SA DO_62
DDR A D63	AJ12	SA DO_63

CANTIGA_Tp0

DDR SYSTEM MEMORY A

SA_BS_0	BD21	DDR A BS0	DDR A_BS0	[15,16]
SA_BS_1	BG18	DDR A BS1	DDR A_BS1	[15,16]
SA_BS_2	AT25	DDR A BS2	DDR A_BS2	[15,16]
SA_RAS#	BB20	DDR A RAS#	DDR_A_RAS#	[15,16]
SA_CAS#	BD20	DDR A CAS#	DDR_A_CAS#	[15,16]
SA_WE#	AY20	DDR A WE#	DDR_A_WE#	[15,16]
SA_DM_0	AM37	DDR A DM0	DDR_A_DM[0..7]	[15]
SA_DM_1	AT41	DDR A DM1		
SA_DM_2	AY41	DDR A DM2		
SA_DM_3	AU39	DDR A DM3		
SA_DM_4	BB12	DDR A DM4		
SA_DM_5	AY6	DDR A DM5		
SA_DM_6	AT7	DDR A DM6		
SA_DM_7	AJ5	DDR A DM7		
SA_DQS_0	AJ44	DDR A DQS0	DDR_A_DQS[0..7]	[15]
SA_DQS_1	AT44	DDR A DQS1		
SA_DQS_2	BA43	DDR A DQS2		
SA_DQS_3	BC37	DDR A DQS3		
SA_DQS_4	AW12	DDR A DQS4		
SA_DQS_5	BC8	DDR A DQS5		
SA_DQS_6	AU8	DDR A DQS6		
SA_DQS_7	AM7	DDR A DQS7		
SA_DQS#_0	AJ43	DDR A DQS#0	DDR_A_DQS#[0..7]	[15]
SA_DQS#_1	AT43	DDR A DQS#1		
SA_DQS#_2	BA44	DDR A DQS#2		
SA_DQS#_3	BD37	DDR A DQS#3		
SA_DQS#_4	AY12	DDR A DQS#4		
SA_DQS#_5	BD8	DDR A DQS#5		
SA_DQS#_6	AU9	DDR A DQS#6		
SA_DQS#_7	AM8	DDR A DQS#7		
SA_MA_0	BA21	DDR A MA0	DDR_A_MA[0..14]	[15,16]
SA_MA_1	BC24	DDR A MA1		
SA_MA_2	BG24	DDR A MA2		
SA_MA_3	BH24	DDR A MA3		
SA_MA_4	BG25	DDR A MA4		
SA_MA_5	BA24	DDR A MA5		
SA_MA_6	BD24	DDR A MA6		
SA_MA_7	BG27	DDR A MA7		
SA_MA_8	BF25	DDR A MA8		
SA_MA_9	AN24	DDR A MA9		
SA_MA_10	BC21	DDR A MA10		
SA_MA_11	BG26	DDR A MA11		
SA_MA_12	BH26	DDR A MA12		
SA_MA_13	BH17	DDR A MA13		
SA_MA_14	AY25	DDR A MA14		

[15] DDR_B_D[0..63]

DDR B D0	AK47	SB DO_0
DDR B D1	AH46	SB DO_1
DDR B D2	AP47	SB DO_2
DDR B D3	AP46	SB DO_3
DDR B D4	AP47	SB DO_4
DDR B D5	AJ48	SB DO_5
DDR B D6	AM48	SB DO_6
DDR B D7	AP48	SB DO_7
DDR B D8	AU47	SB DO_8
DDR B D9	AJ46	SB DO_9
DDR B D10	BA48	SB DO_10
DDR B D11	AY48	SB DO_11
DDR B D12	AT47	SB DO_12
DDR B D13	AP47	SB DO_13
DDR B D14	BA47	SB DO_14
DDR B D15	BC47	SB DO_15
DDR B D16	BC46	SB DO_16
DDR B D17	BC44	SB DO_17
DDR B D18	BC43	SB DO_18
DDR B D19	BF43	SB DO_19
DDR B D20	BE45	SB DO_20
DDR B D21	BC41	SB DO_21
DDR B D22	BF40	SB DO_22
DDR B D23	BF41	SB DO_23
DDR B D24	BG38	SB DO_24
DDR B D25	BF38	SB DO_25
DDR B D26	BH35	SB DO_26
DDR B D27	BG35	SB DO_27
DDR B D28	BH40	SB DO_28
DDR B D29	BG39	SB DO_29
DDR B D30	BG34	SB DO_30
DDR B D31	BH34	SB DO_31
DDR B D32	BH14	SB DO_32
DDR B D33	BG12	SB DO_33
DDR B D34	BH11	SB DO_34
DDR B D35	BG8	SB DO_35
DDR B D36	BH12	SB DO_36
DDR B D37	BF11	SB DO_37
DDR B D38	BF8	SB DO_38
DDR B D39	BG7	SB DO_39
DDR B D40	BC5	SB DO_40
DDR B D41	BC6	SB DO_41
DDR B D42	AV3	SB DO_42
DDR B D43	AY1	SB DO_43
DDR B D44	BF6	SB DO_44
DDR B D45	BF5	SB DO_45
DDR B D46	BA1	SB DO_46
DDR B D47	BD3	SB DO_47
DDR B D48	AV2	SB DO_48
DDR B D49	AJ3	SB DO_49
DDR B D50	AR3	SB DO_50
DDR B D51	AV2	SB DO_51
DDR B D52	AV2	SB DO_52
DDR B D53	AV1	SB DO_53
DDR B D54	AP3	SB DO_54
DDR B D55	AL1	SB DO_55
DDR B D56	AL1	SB DO_56
DDR B D57	AL2	SB DO_57
DDR B D58	AJ1	SB DO_58
DDR B D59	AH1	SB DO_59
DDR B D60	AM2	SB DO_60
DDR B D61	AM3	SB DO_61
DDR B D62	AH3	SB DO_62
DDR B D63	AJ3	SB DO_63

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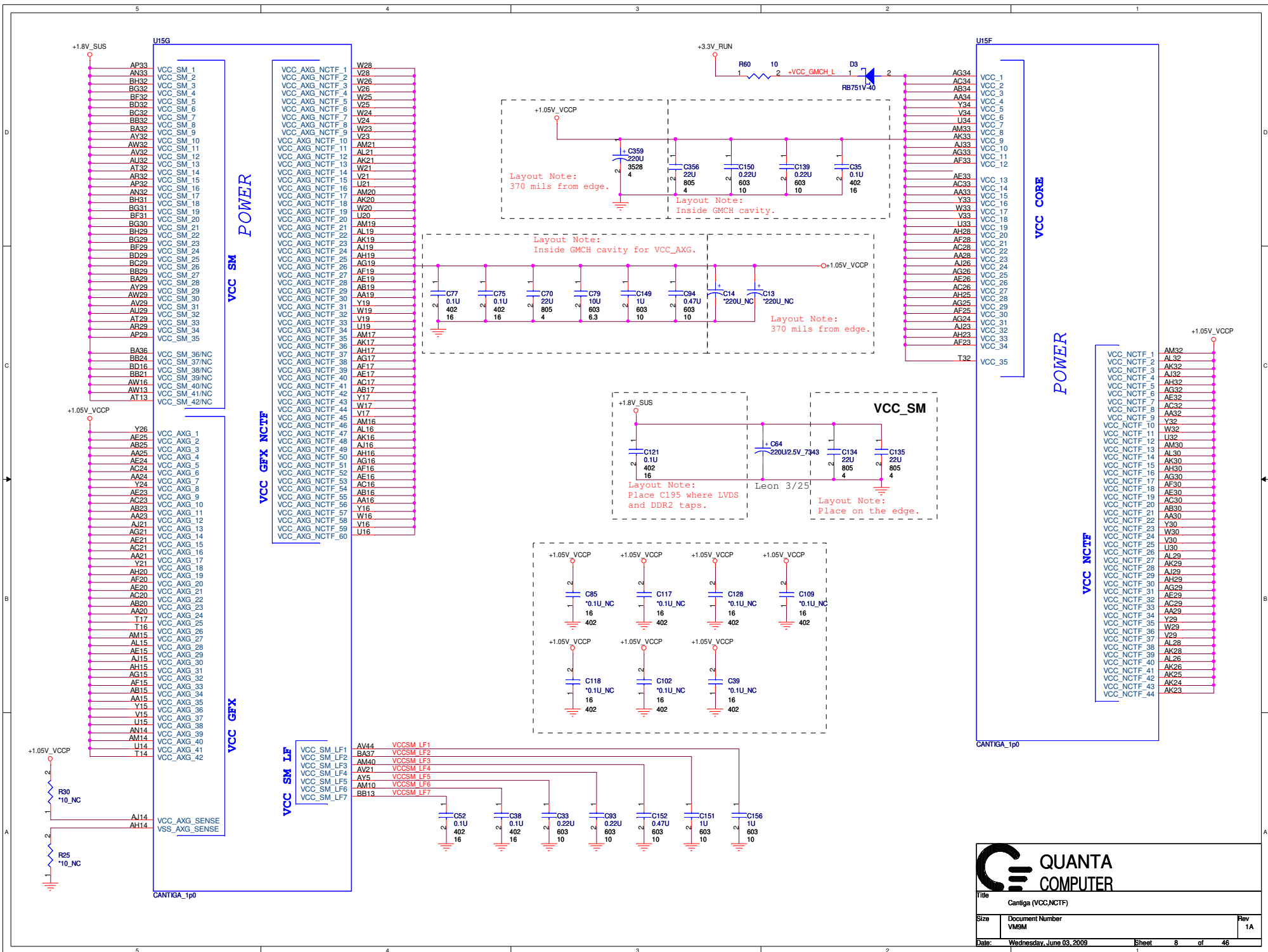
DDR SYSTEM MEMORY B

SB_BS_0	BC16	DDR B BS0	DDR_B_BS0	[15,16]
SB_BS_1	BB17	DDR B BS1	DDR_B_BS1	[15,16]
SB_BS_2	BB33	DDR B BS2	DDR_B_BS2	[15,16]
SB_RAS#	AU17	DDR B RAS#	DDR_B_RAS#	[15,16]
SB_CAS#	BG16	DDR B CAS#	DDR_B_CAS#	[15,16]
SB_WE#	BF14	DDR B WE#	DDR_B_WE#	[15,16]
SB_DM_0	AM47	DDR B DM0	DDR_B_DM[0..7]	[15]
SB_DM_1	AV47	DDR B DM1		
SB_DM_2	BD40	DDR B DM2		
SB_DM_3	BF35	DDR B DM3		
SB_DM_4	BG11	DDR B DM4		
SB_DM_5	BA3	DDR B DM5		
SB_DM_6	AP1	DDR B DM6		
SB_DM_7	AK2	DDR B DM7		
SB_DQS_0	AL47	DDR B DQS0	DDR_B_DQS[0..7]	[15]
SB_DQS_1	AV48	DDR B DQS1		
SB_DQS_2	BC41	DDR B DQS2		
SB_DQS_3	BG37	DDR B DQS3		
SB_DQS_4	BH9	DDR B DQS4		
SB_DQS_5	BB2	DDR B DQS5		
SB_DQS_6	AU1	DDR B DQS6		
SB_DQS_7	AN6	DDR B DQS7		
SB_DQS#_0	AL46	DDR B DQS#0	DDR_B_DQS#[0..7]	[15]
SB_DQS#_1	AV47	DDR B DQS#1		
SB_DQS#_2	BH41	DDR B DQS#2		
SB_DQS#_3	BH37	DDR B DQS#3		
SB_DQS#_4	BG9	DDR B DQS#4		
SB_DQS#_5	BC2	DDR B DQS#5		
SB_DQS#_6	AT2	DDR B DQS#6		
SB_DQS#_7	AN5	DDR B DQS#7		
SB_MA_0	AV17	DDR B MA0	DDR_B_MA[0..14]	[15,16]
SB_MA_1	BA25	DDR B MA1		
SB_MA_2	BC25	DDR B MA2		
SB_MA_3	AU25	DDR B MA3		
SB_MA_4	AV25	DDR B MA4		
SB_MA_5	BB28	DDR B MA5		
SB_MA_6	AU28	DDR B MA6		
SB_MA_7	AT33	DDR B MA7		
SB_MA_8	BD33	DDR B MA8		
SB_MA_9	BB16	DDR B MA9		
SB_MA_10	AW33	DDR B MA10		
SB_MA_11	AY33	DDR B MA11		
SB_MA_12	BH15	DDR B MA12		
SB_MA_13	AJ33	DDR B MA13		
SB_MA_14	AJ33	DDR B MA14		

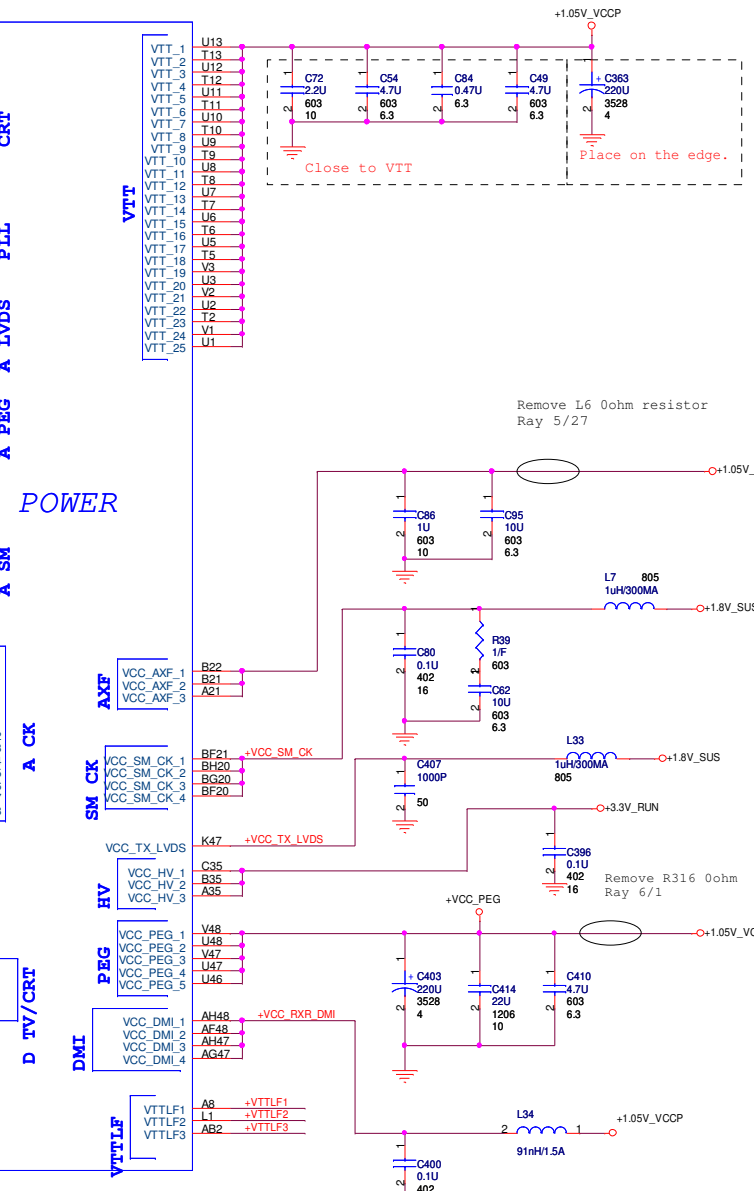
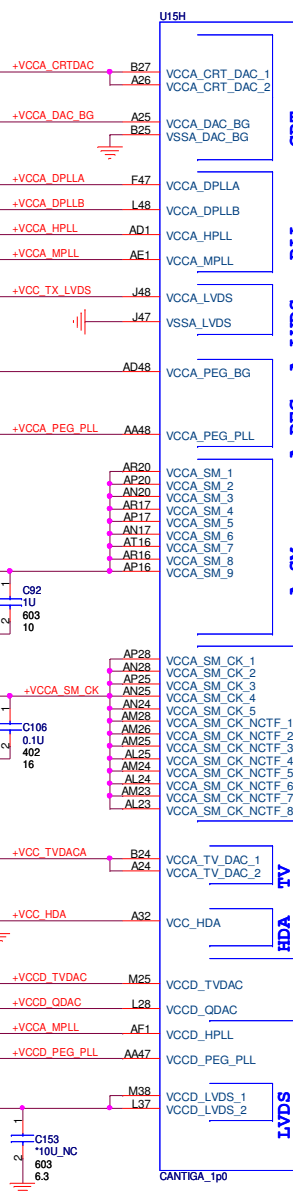
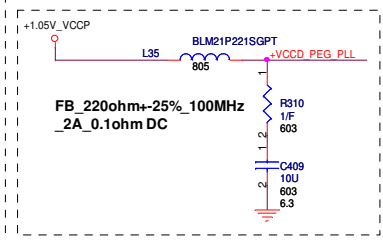
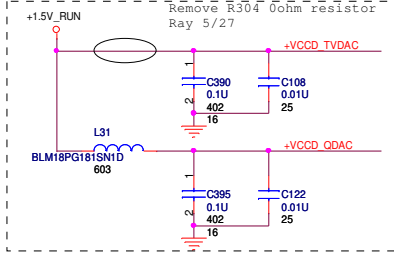
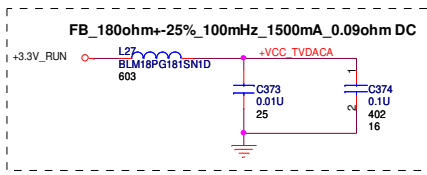
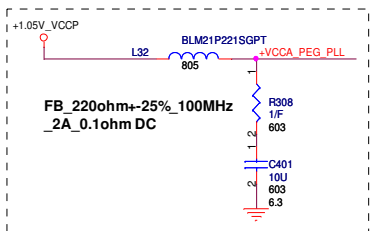
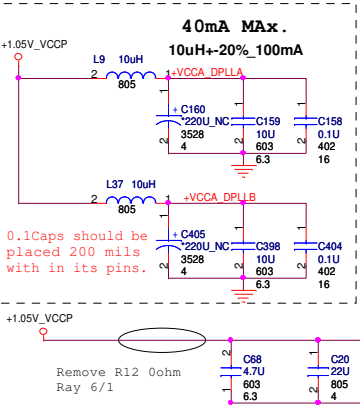
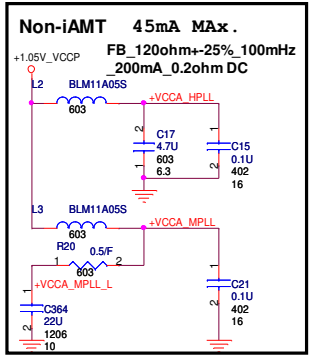
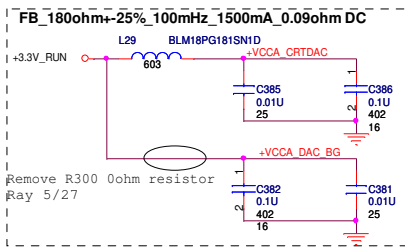


QUANTA COMPUTER

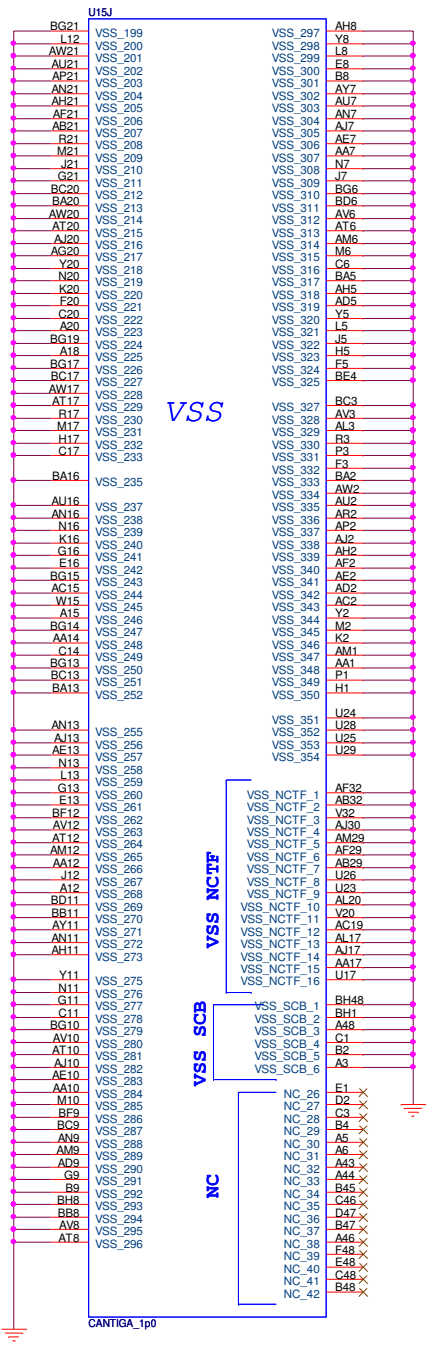
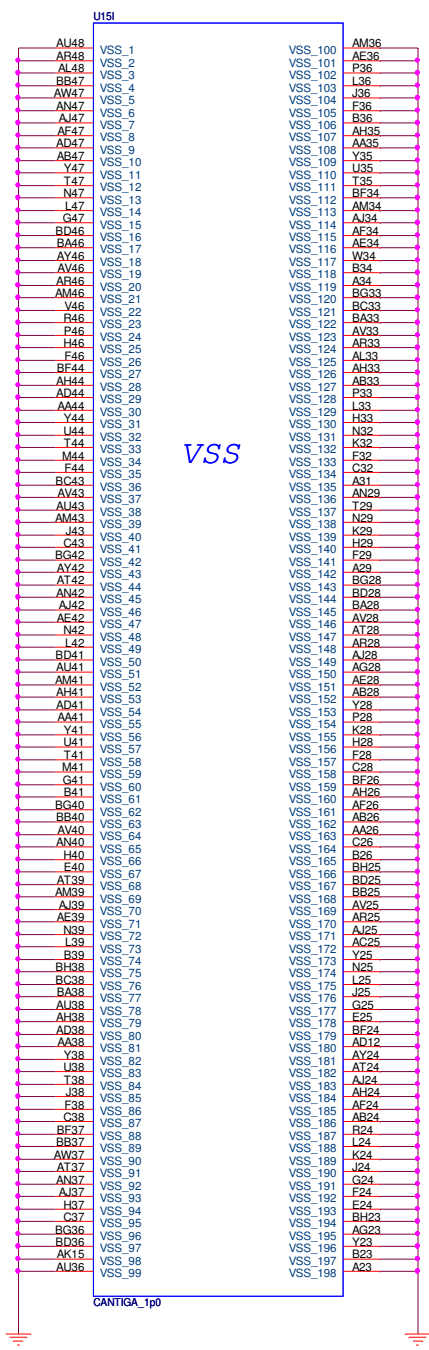
Title			Cantiga (DDR2)		
Size	Document Number	Rev			
	VMSM	1A			
Date:	Saturday, June 06, 2009	Sheet	7	of	46



Title Cantiga (VCC,NCTF)		
Size	Document Number VMSM	Rev 1A
Date:	Wednesday, June 03, 2009	Sheet 8 of 46



Title: Cantiga (POWER)		
Size: VMSM	Document Number:	Rev: 1A
Date: Saturday, June 06, 2009	Sheet: 9	of 46

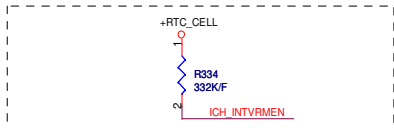
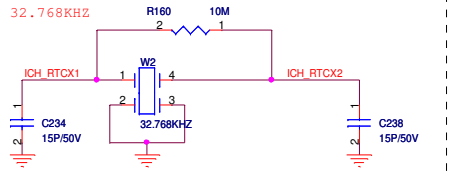


QUANTA
COMPUTER

Title: Cantiga (VSS)

Size	Document Number VMSM	Rev 1A
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Date: Wednesday, June 03, 2009 Sheet 10 of 46

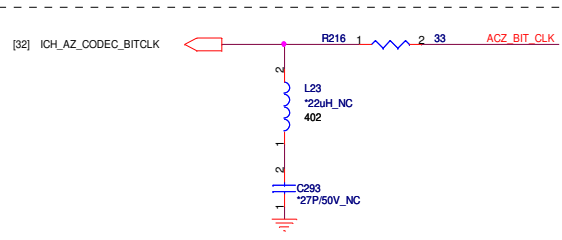
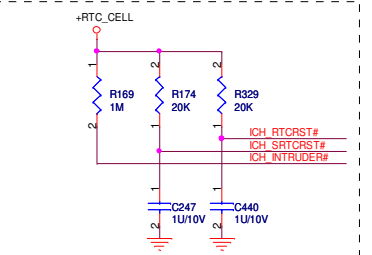


ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

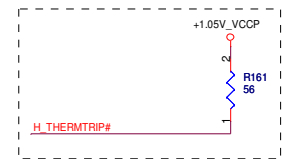
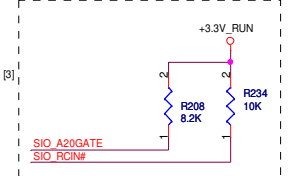
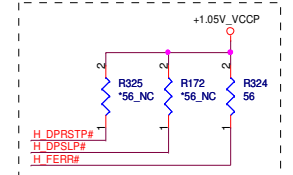
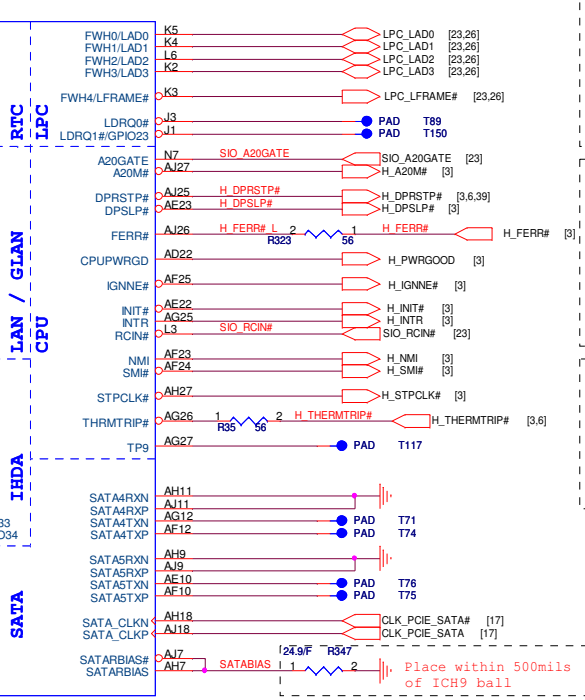
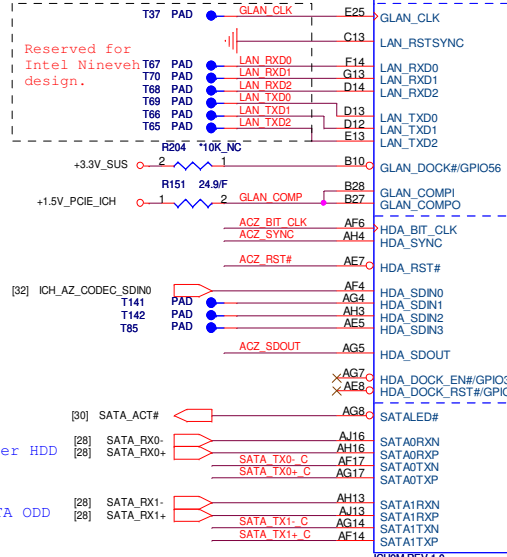
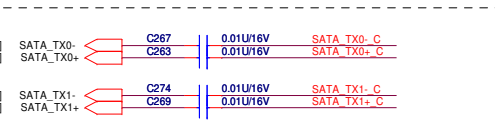
Low = Internal VR Disabled
High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)

Low = Internal VR Disabled
High = Internal VR Enabled(Default)



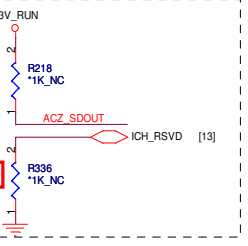
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source.



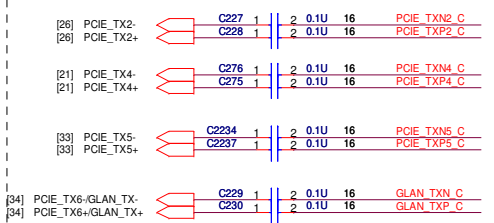
Master HDD

SATA ODD

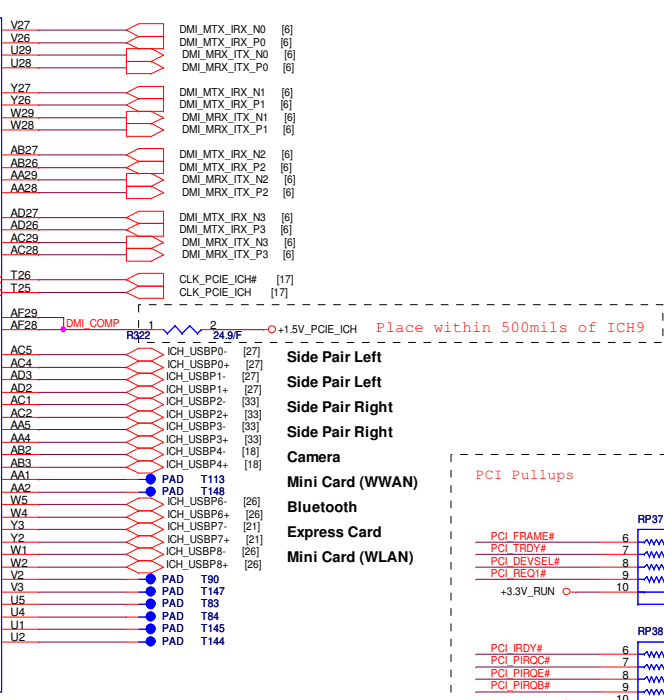
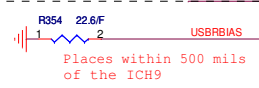
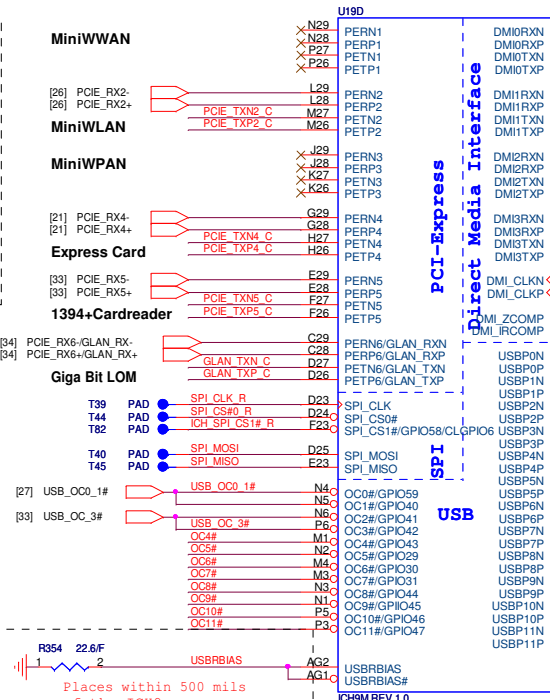
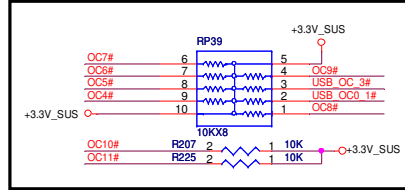
XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIe port config bit 1



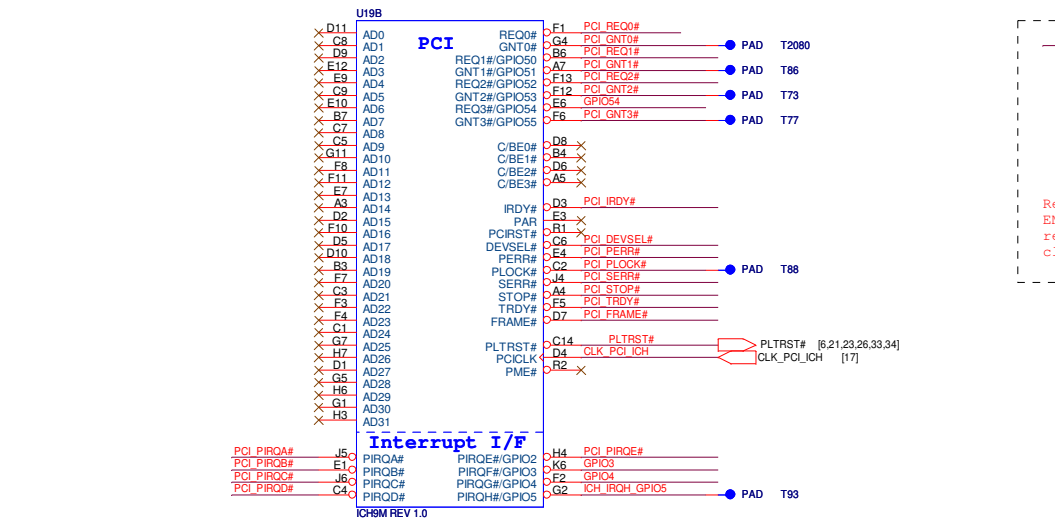
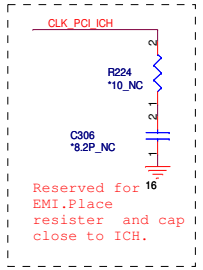
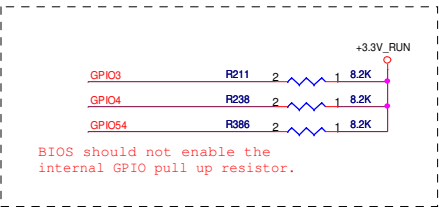
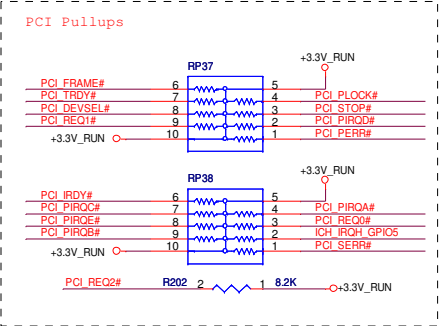
Place TX DC blocking caps close ICH9.



Boot BIOS Strap			
	GNT0#	SPI_CS1#	
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff



- Side Pair Left
- Side Pair Left
- Side Pair Right
- Side Pair Right
- Camera
- Mini Card (WWAN)
- Bluetooth
- Express Card
- Mini Card (WLAN)

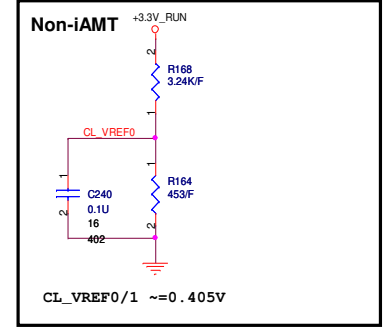
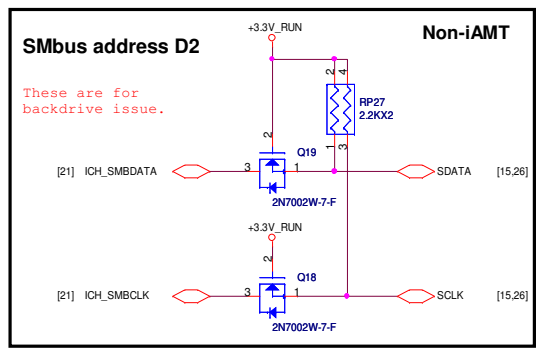
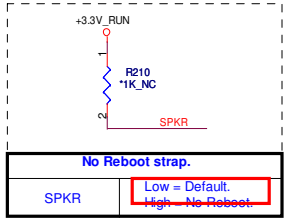
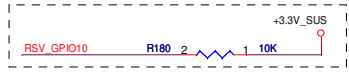
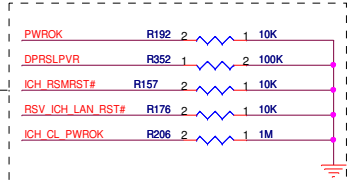
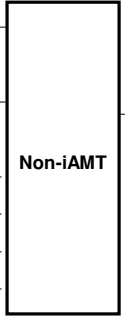
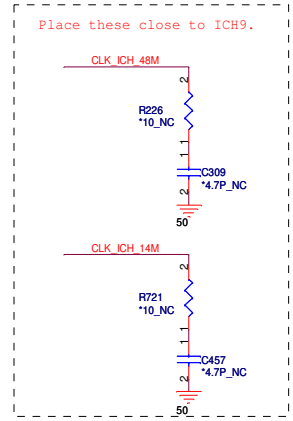
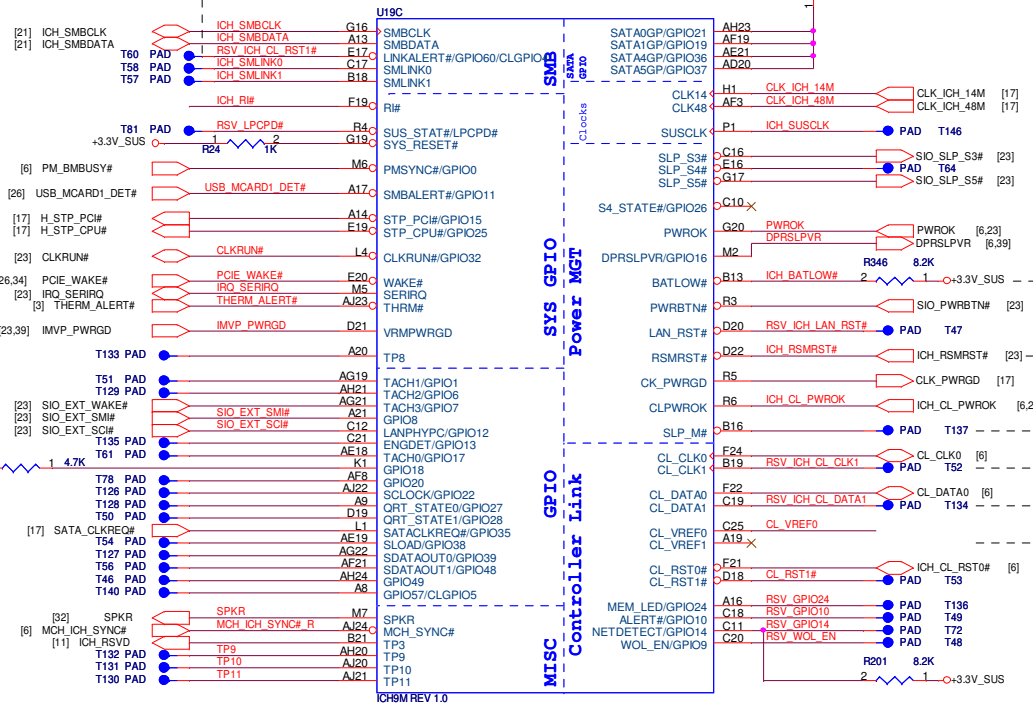
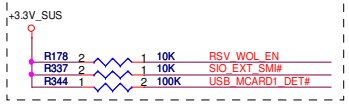
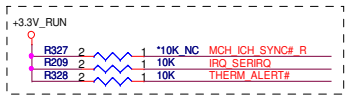
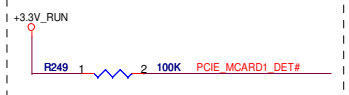
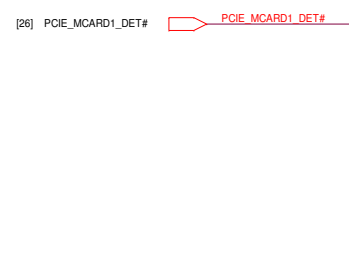
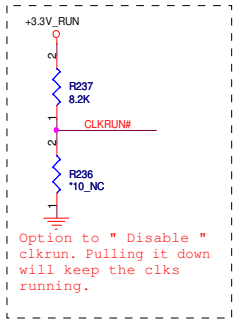
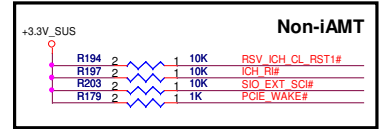
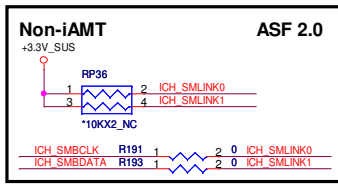
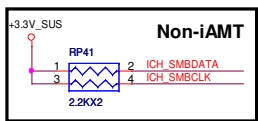


QUANTA COMPUTER

Title: ICH9-M (USB,DM,PCI,PCI)

Size: Document Number VMSM Rev 1A

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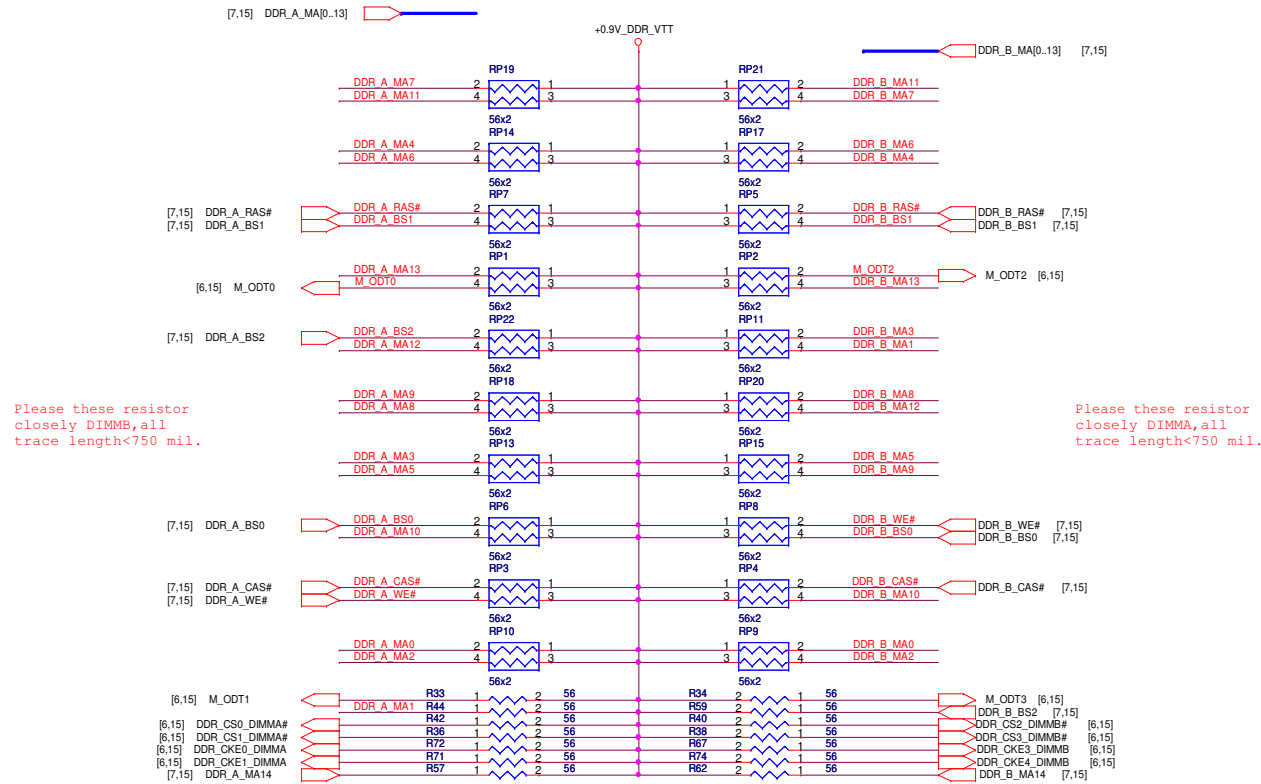
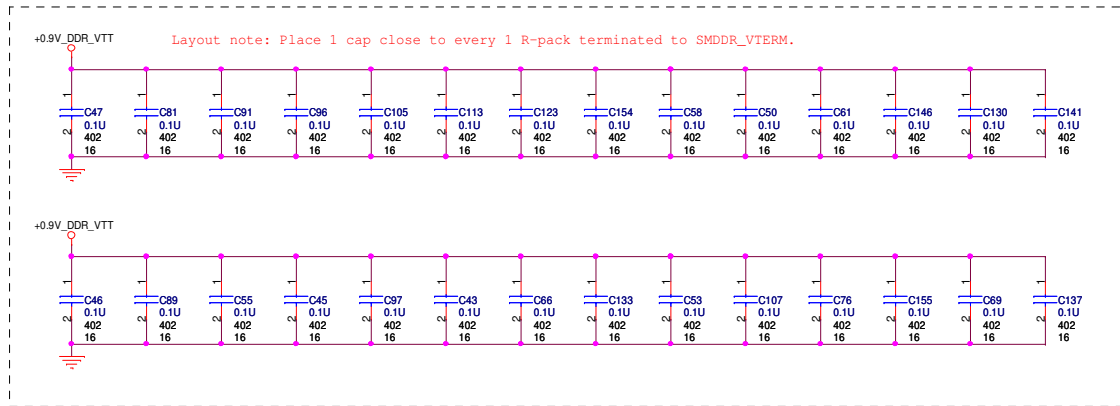


QUANTA COMPUTER

Title: ICH9-M (PM,GPIO,SMB,CL)

Size: Document Number VMSM Rev 1A

Date: Saturday, June 06, 2009 Sheet 13 of 46



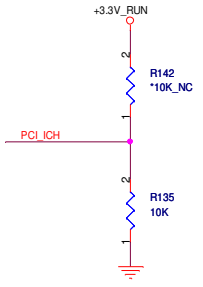
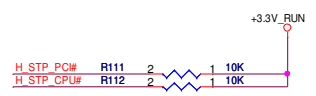
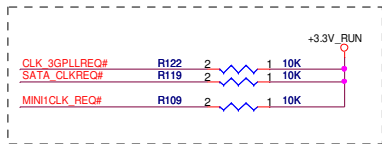
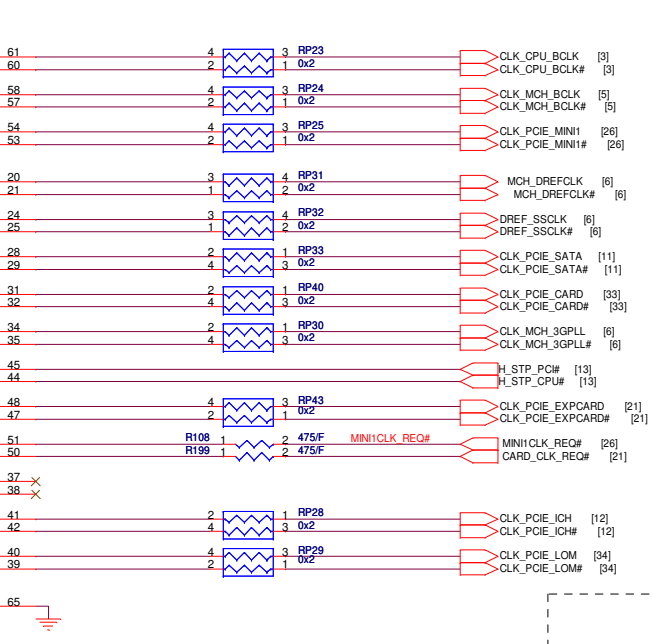
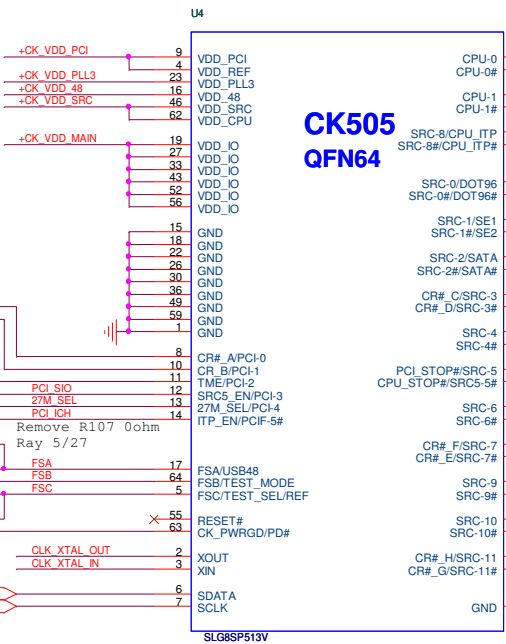
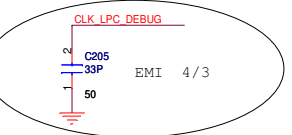
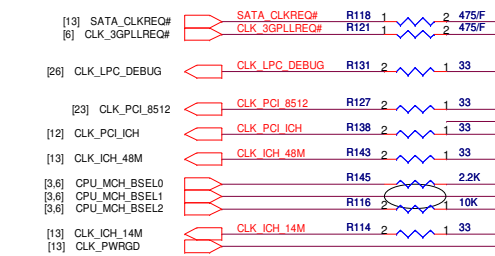
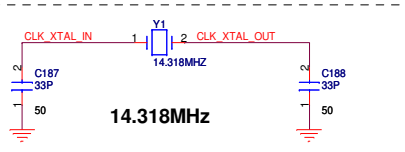
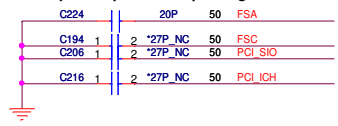
QUANTA COMPUTER

Title: DDR2 RES ARRAY

Size: Document Number VMSM Rev 1A

Date: Wednesday, June 03, 2009 Sheet 16 of 46

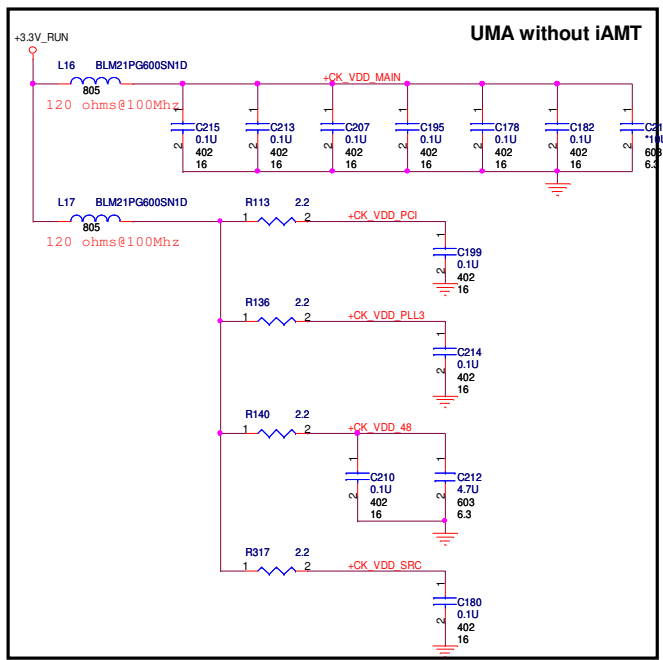
Add capacitor pads for improving WWAN.

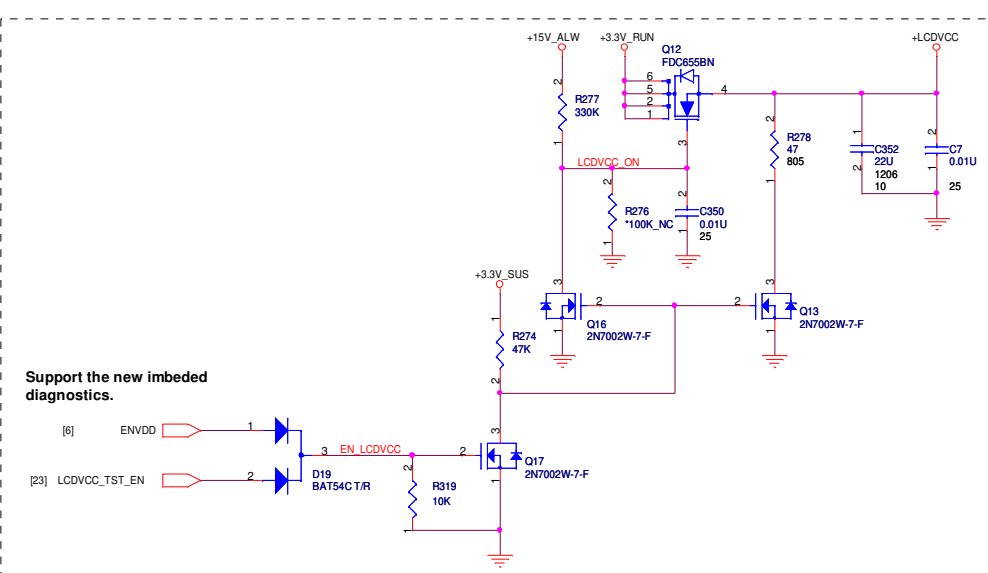


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	200	100	33
0	1	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

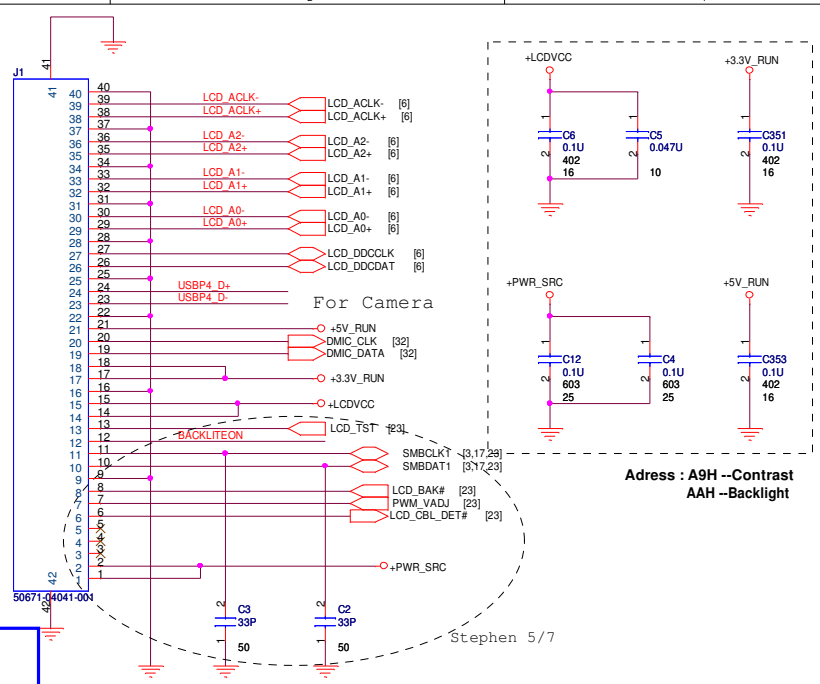
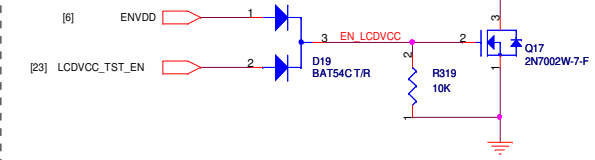
27M_SEL

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



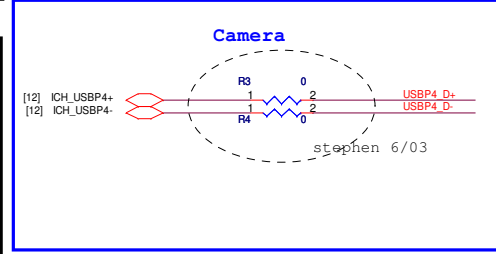
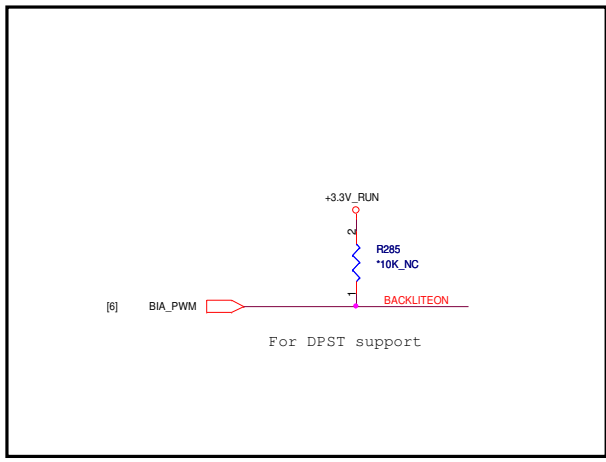


Support the new imbedded diagnostics.

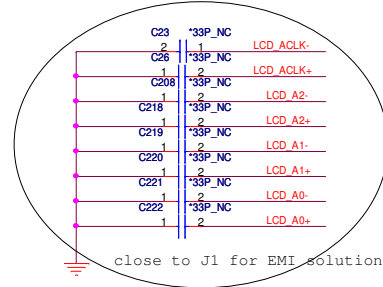
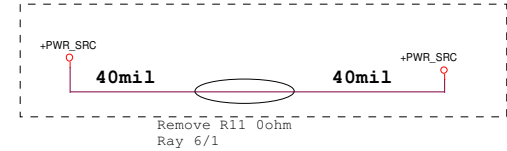


Address : A9H --Contrast
AAH --Backlight

Stephen 5/7

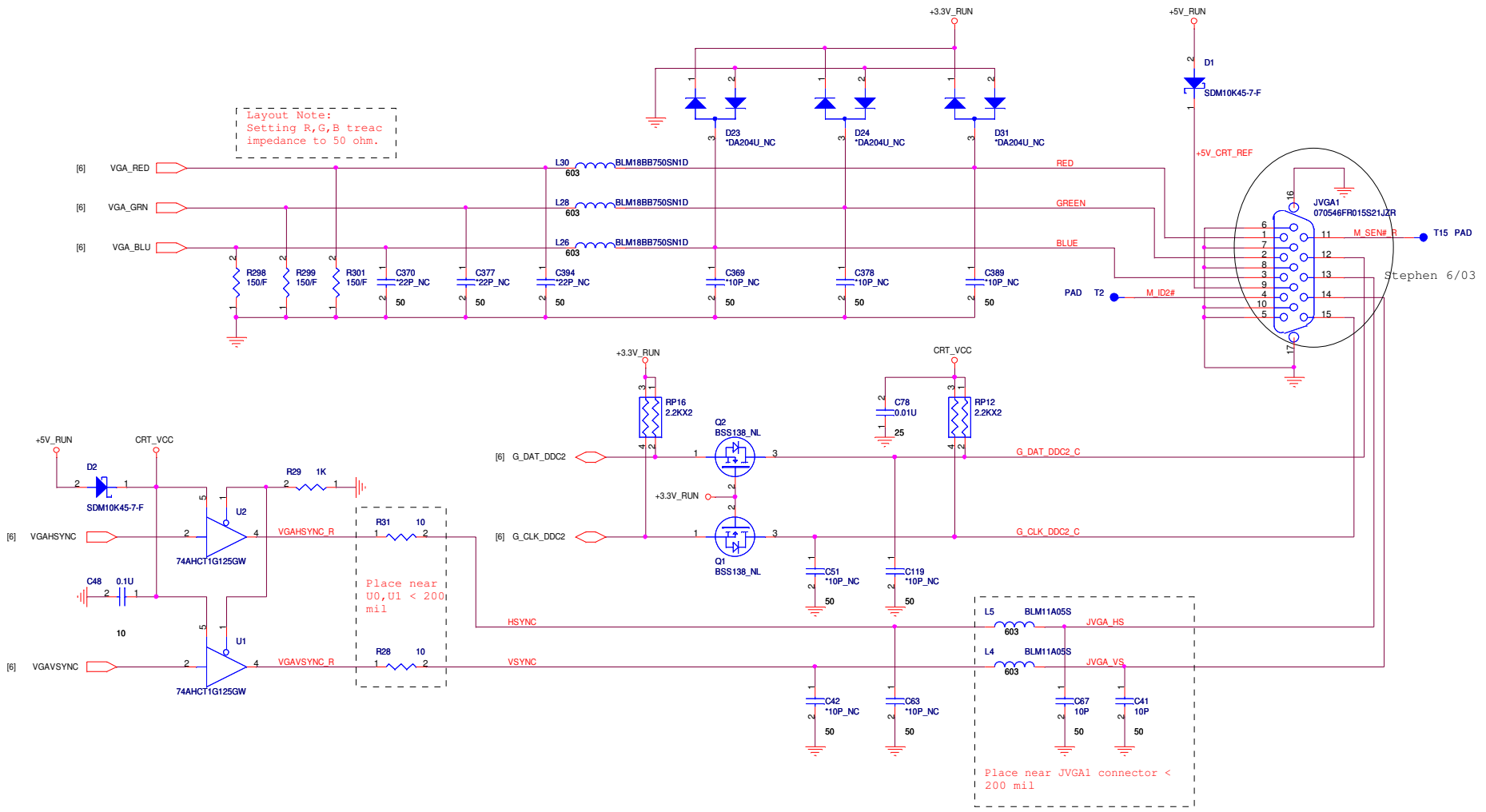


stephen 6/03



close to J1 for EMI solution

Layout Note:
Setting R,G,B treac
impedance to 50 ohm.



Title CRT&TV CONN		
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A

B

C

D

E

1

1

2


2

3

3

4

4

 QUANTA COMPUTER		
Title	Card Reader-RTS5158E	
Size	Document Number VM9M	Rev 1A
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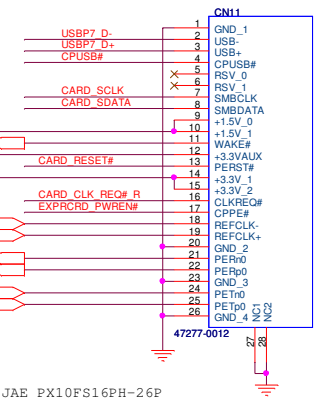
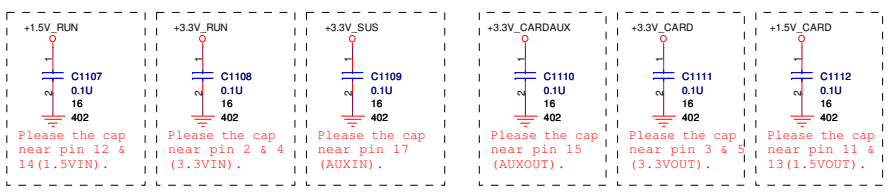
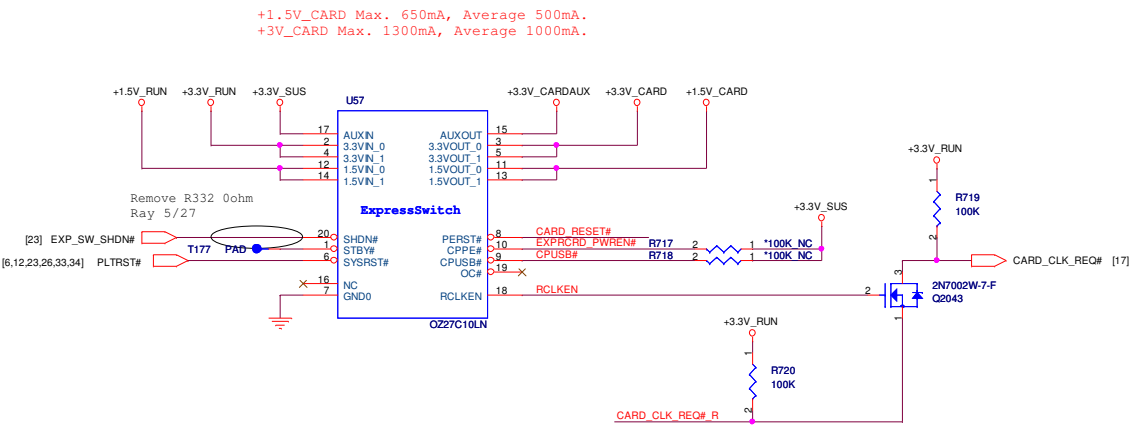
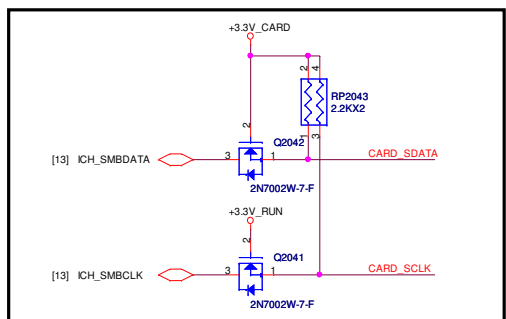
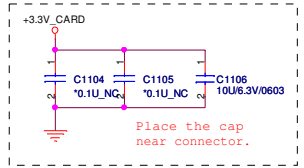
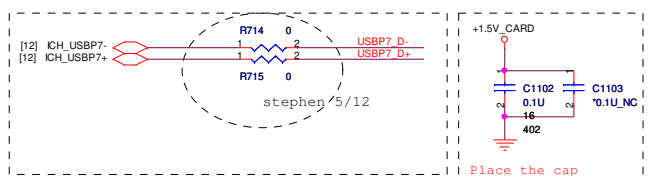
A

B

C

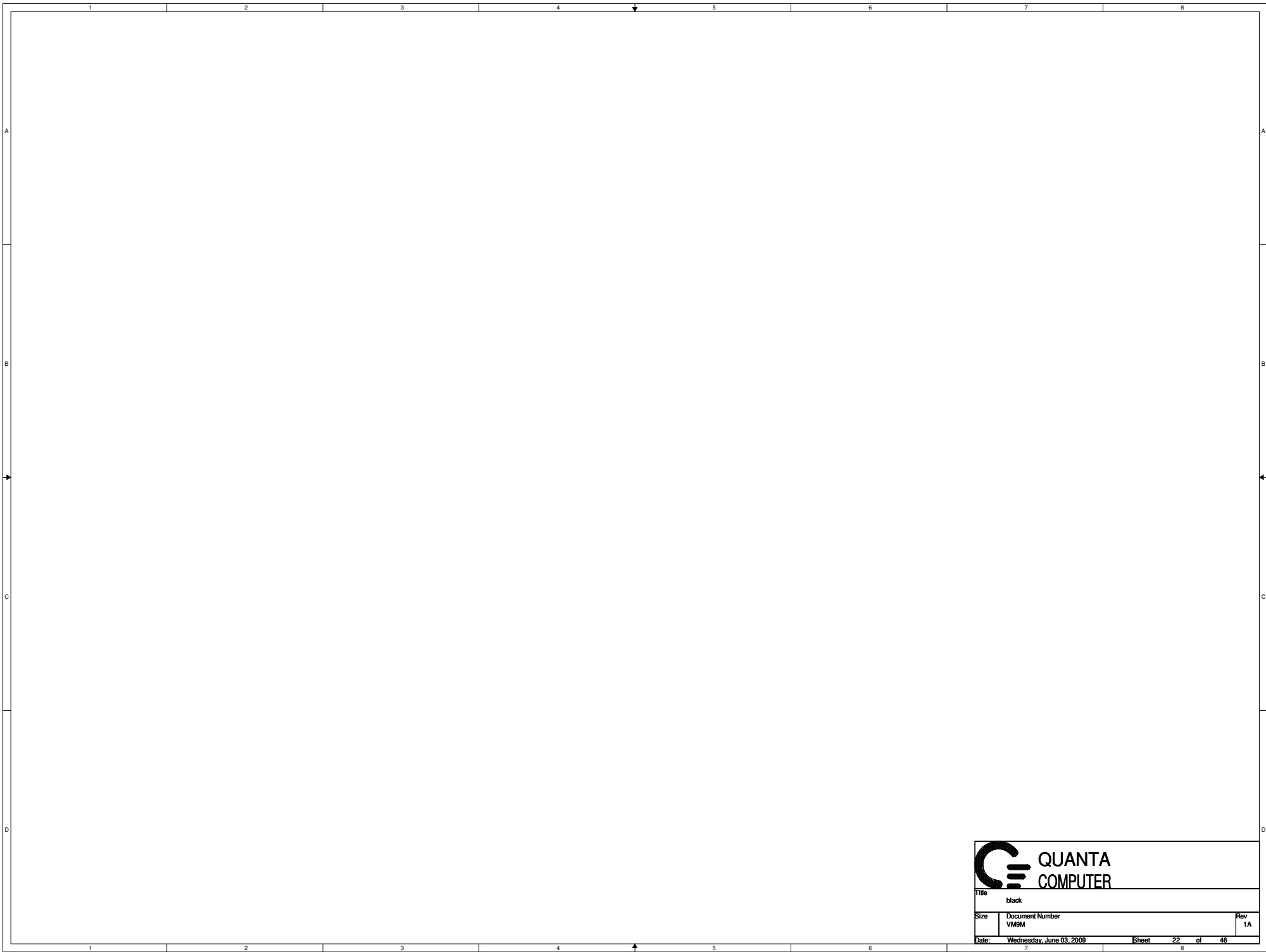
D

E



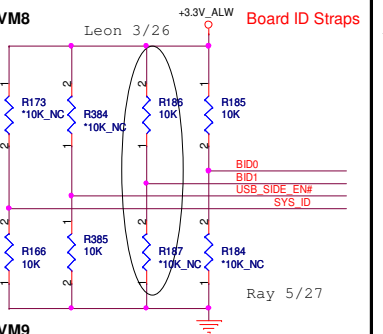
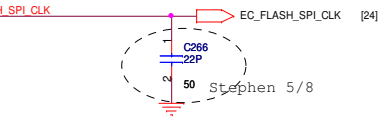
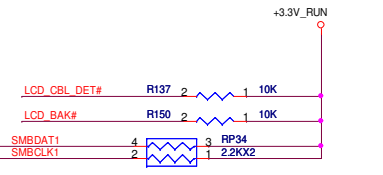
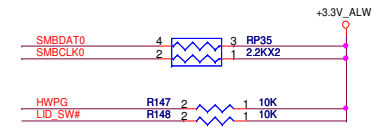
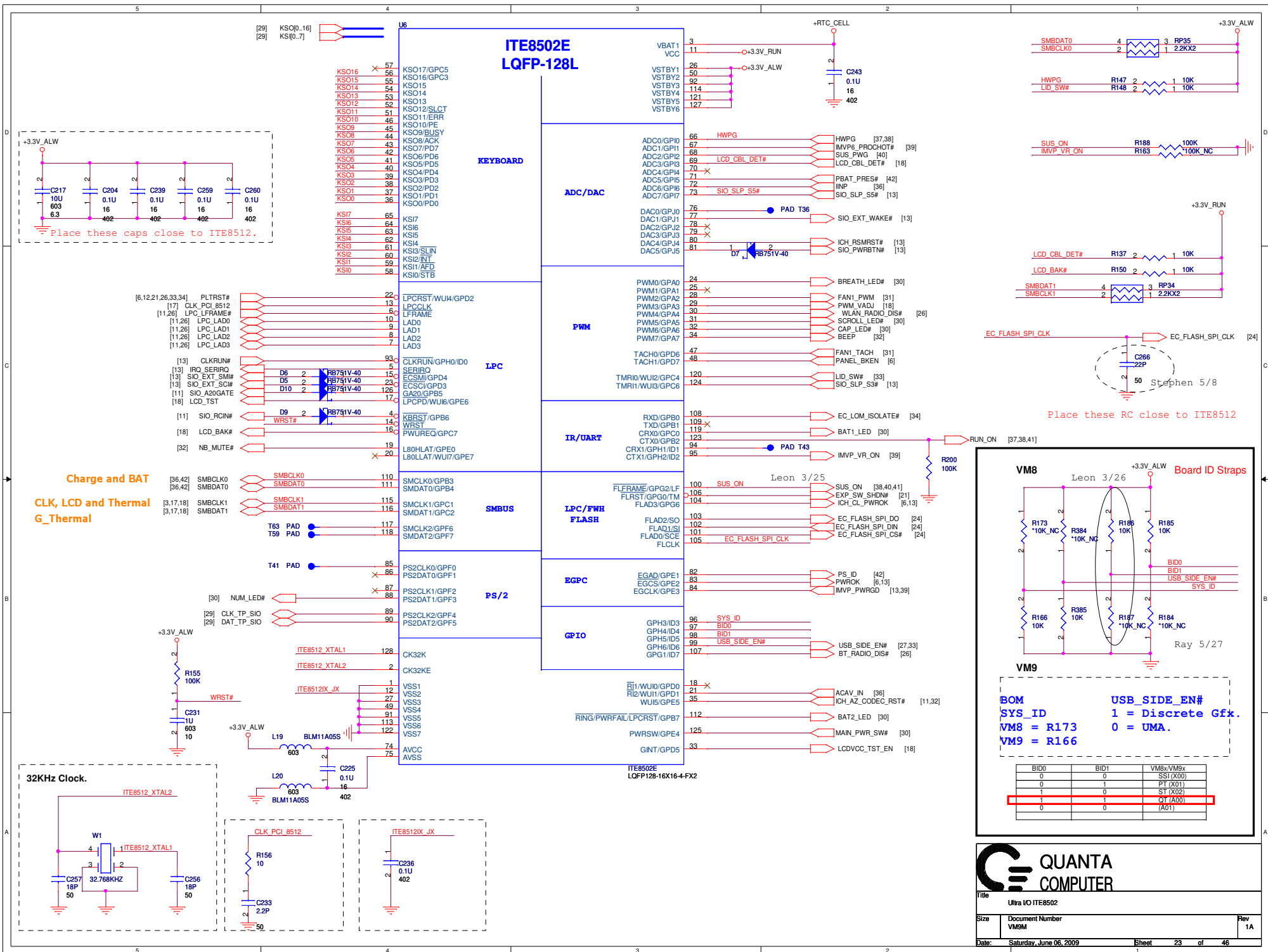
Express Card





QUANTA
COMPUTER

Title black		
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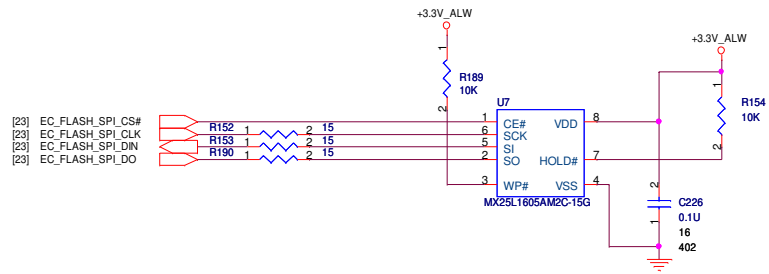
BOM: VM8 = R173, VM9 = R166

USB_SIDE_EN#:
1 = Discrete Gfx.
0 = UMA.

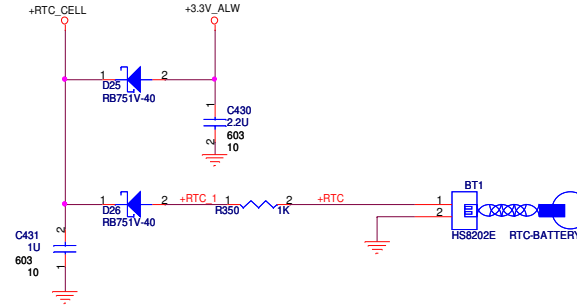
BID0	BID1	VM8x/VM9x
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	OT (A00)
0	0	(A01)

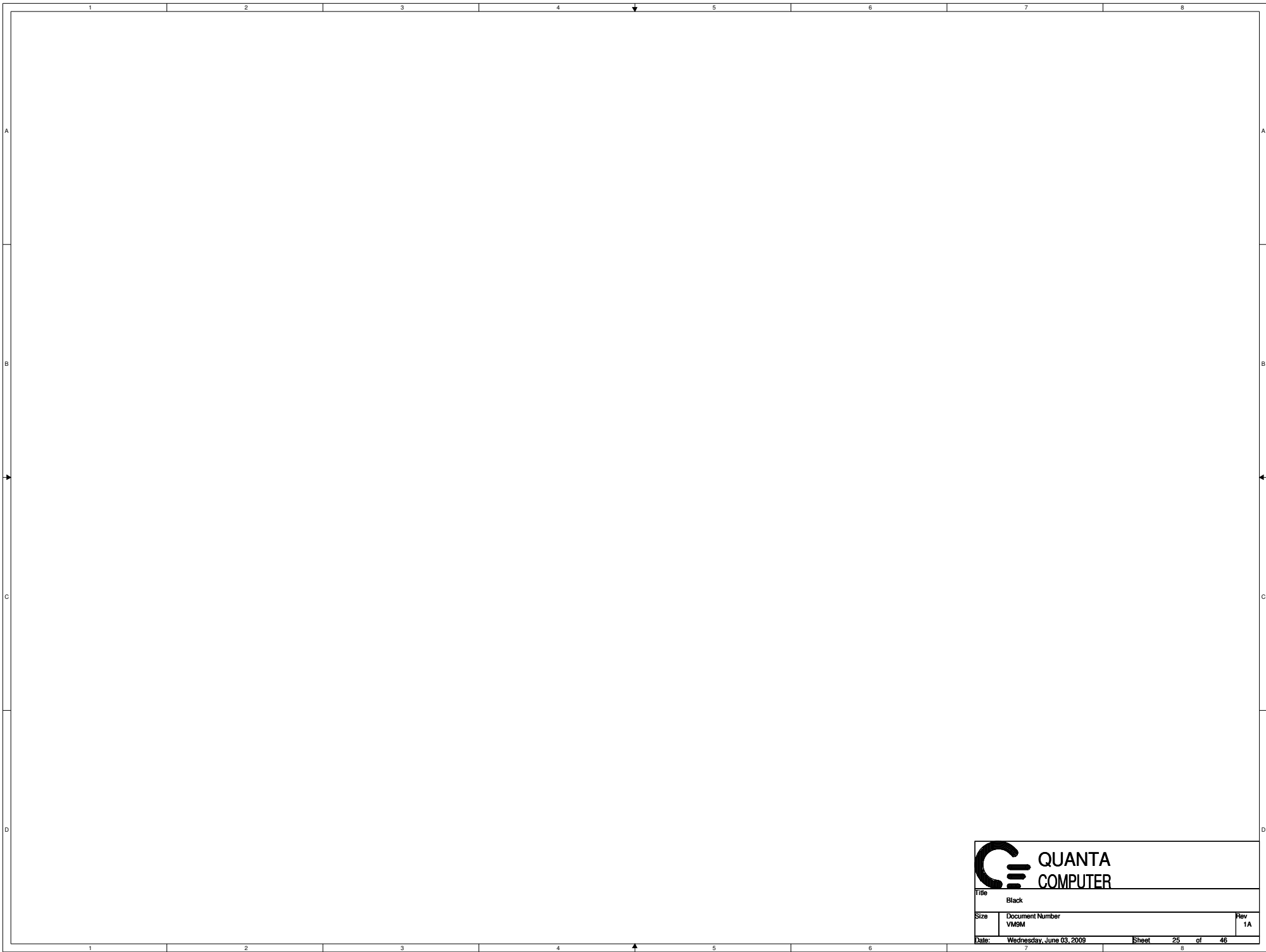


16Mbit (2M Byte), SPI



RTC BATTERY

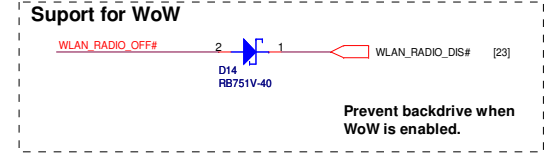
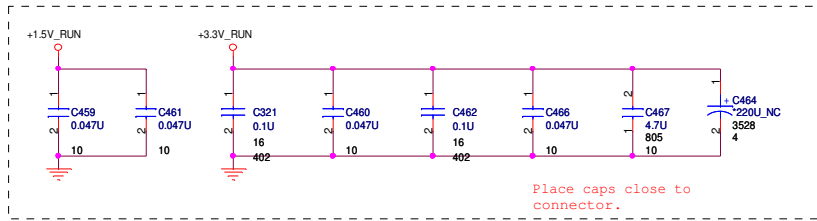
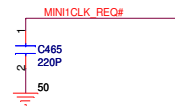
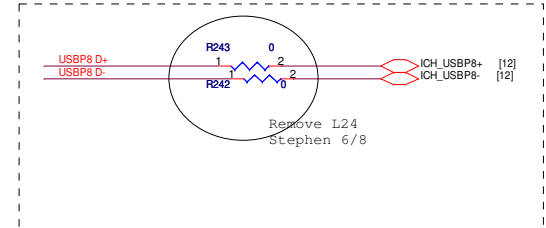
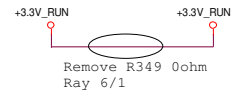
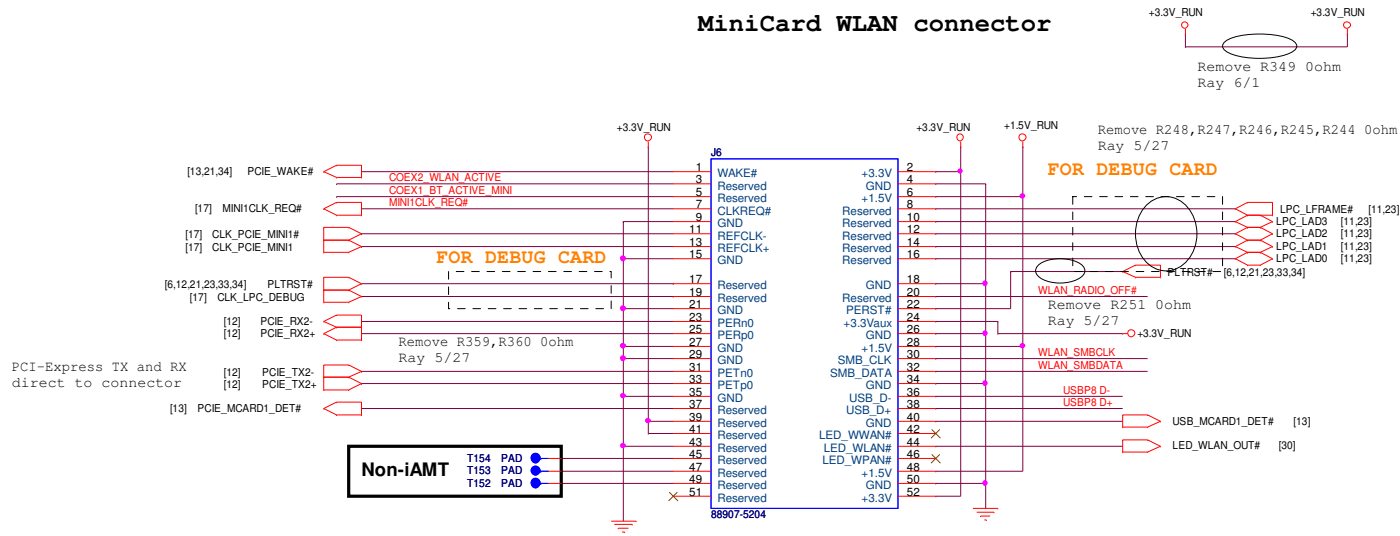




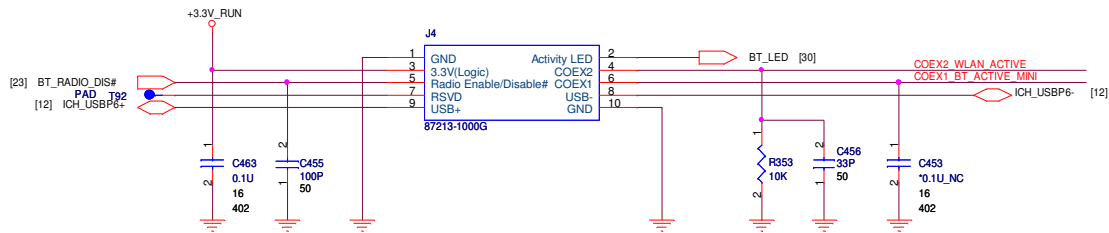
**QUANTA
COMPUTER**

Title		
Black		
Size	Document Number	Rev
VMSM		1A
Date: Wednesday, June 03, 2009		Sheet 25 of 46

MiniCard WLAN connector



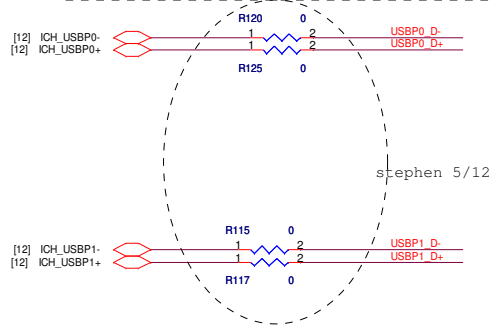
Bluetooth



QUANTA COMPUTER

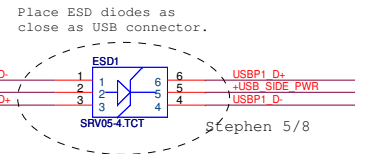
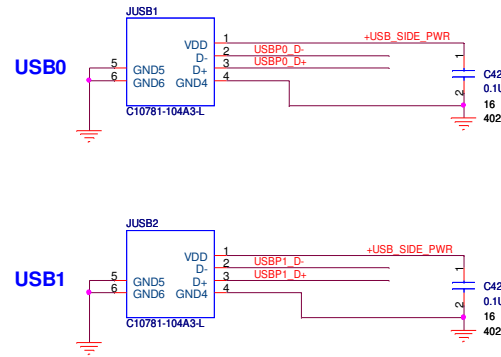
Title: MDC CONN.		
Size: VMSM	Document Number: VMSM	Rev: 1A
Date: Monday, June 08, 2009	Sheet: 26 of 46	

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



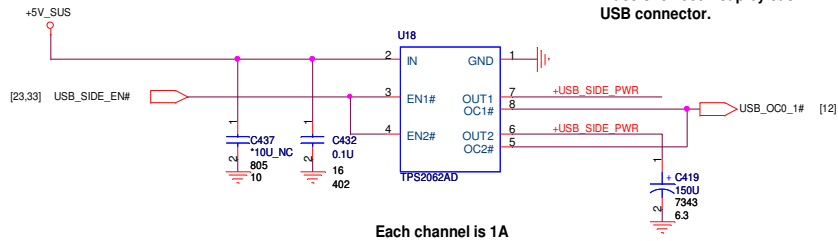
stephen 5/12

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.



Place ESD diodes as close as USB connector.

stephen 5/8

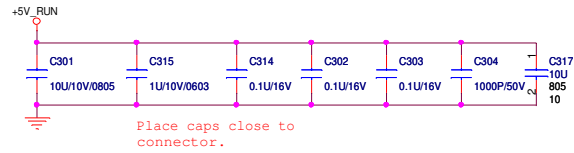
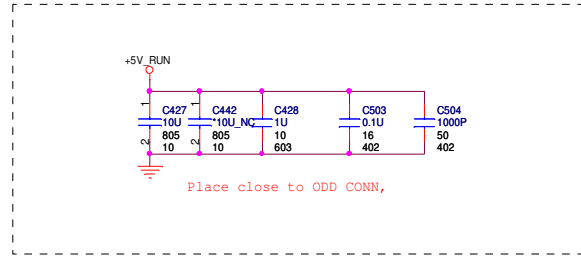
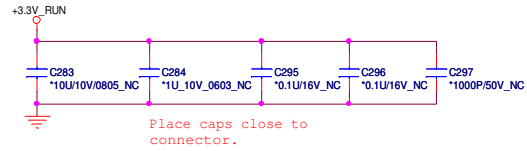
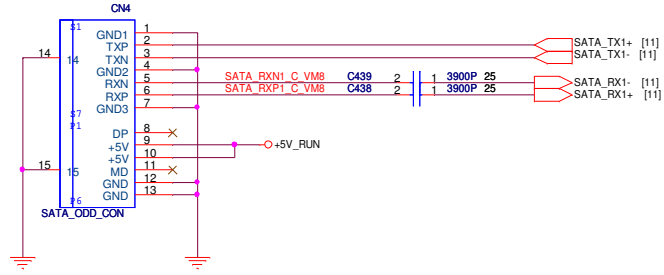
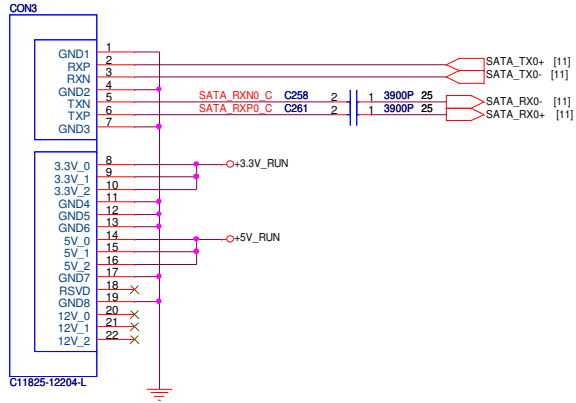


Place one 150uF cap by each USB connector.

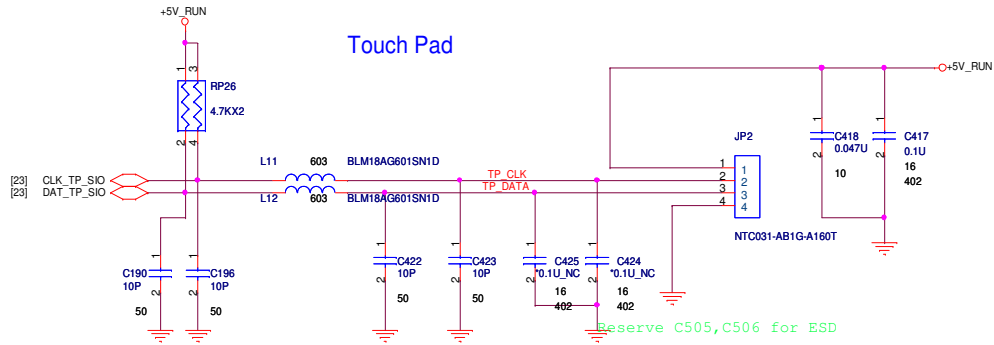
Each channel is 1A

SATA HDD Connector.

SATA ODD Connector.

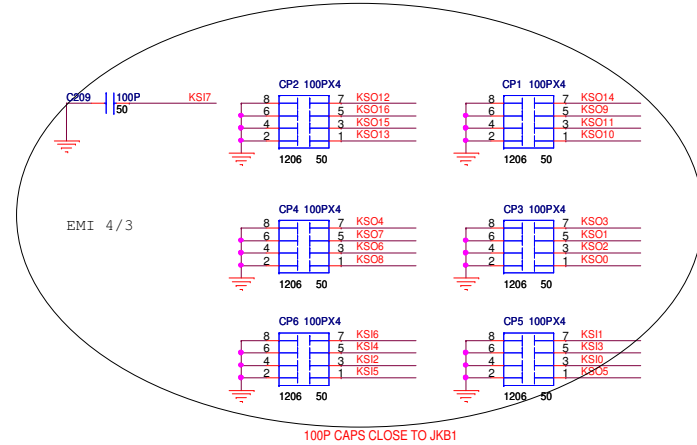
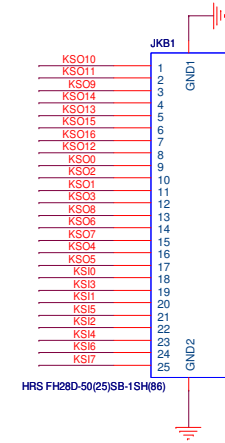


Touch Pad



KEYBOARD CONNECTOR

[23] KSO[0..16]
 [23] KSI[0..7]



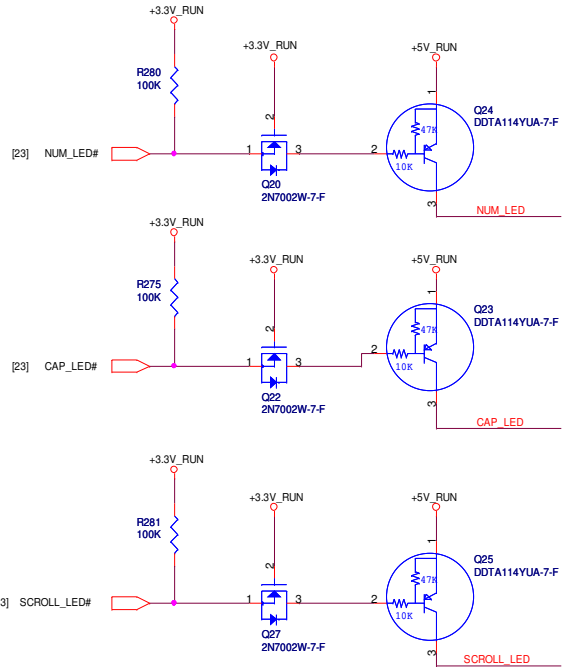
QUANTA COMPUTER

Title: TOUCH PAD, BULE TOOTH & FIR

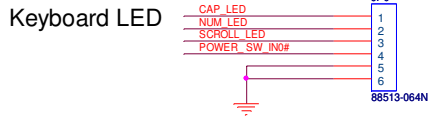
Size	Document Number VMSM	Rev 1A
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Date: Wednesday, June 03, 2009 Sheet 29 of 46

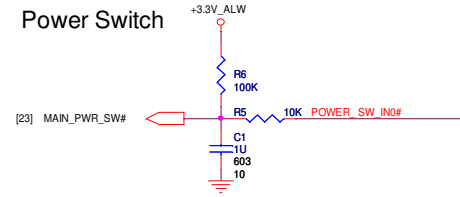
Keyboard LED



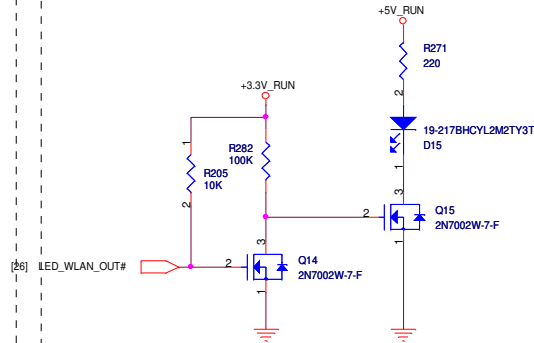
Dash board connector



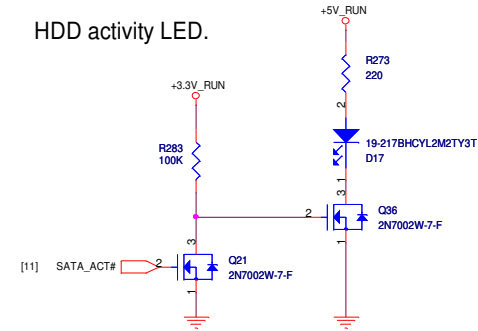
Power Switch



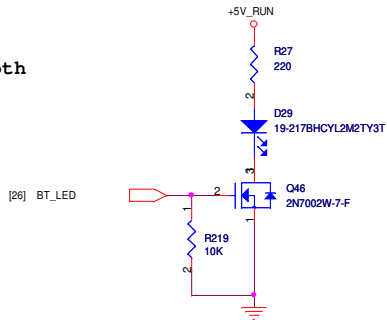
WLAN



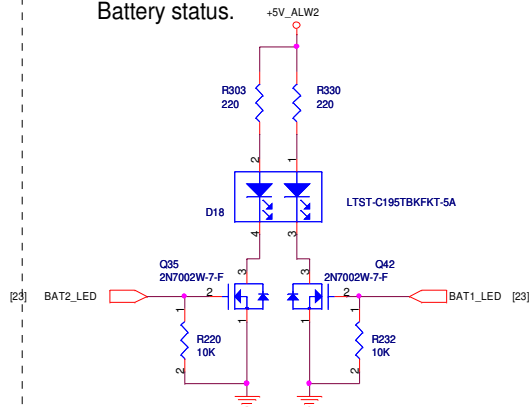
HDD activity LED.



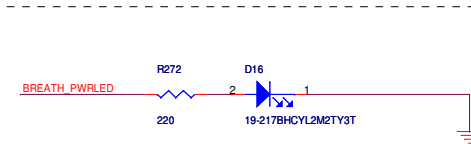
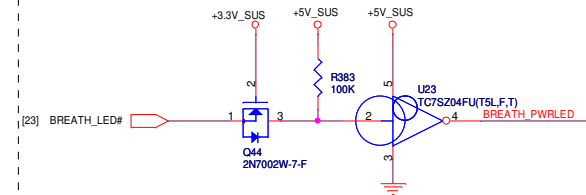
Bluetooth

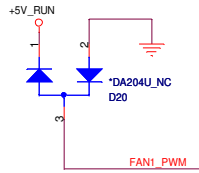
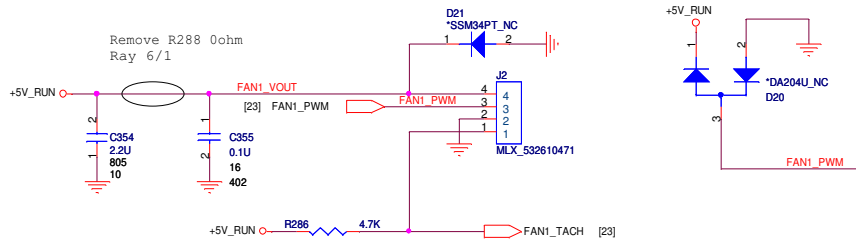


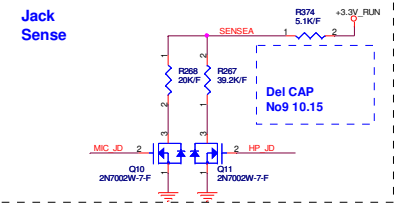
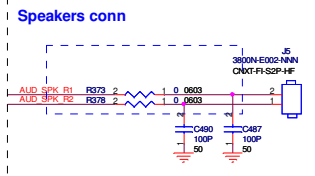
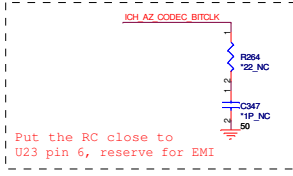
Battery status.



Power & Suspend.

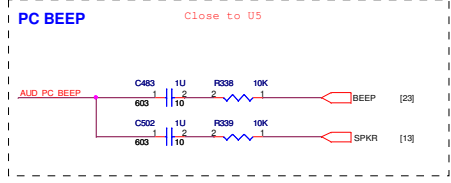
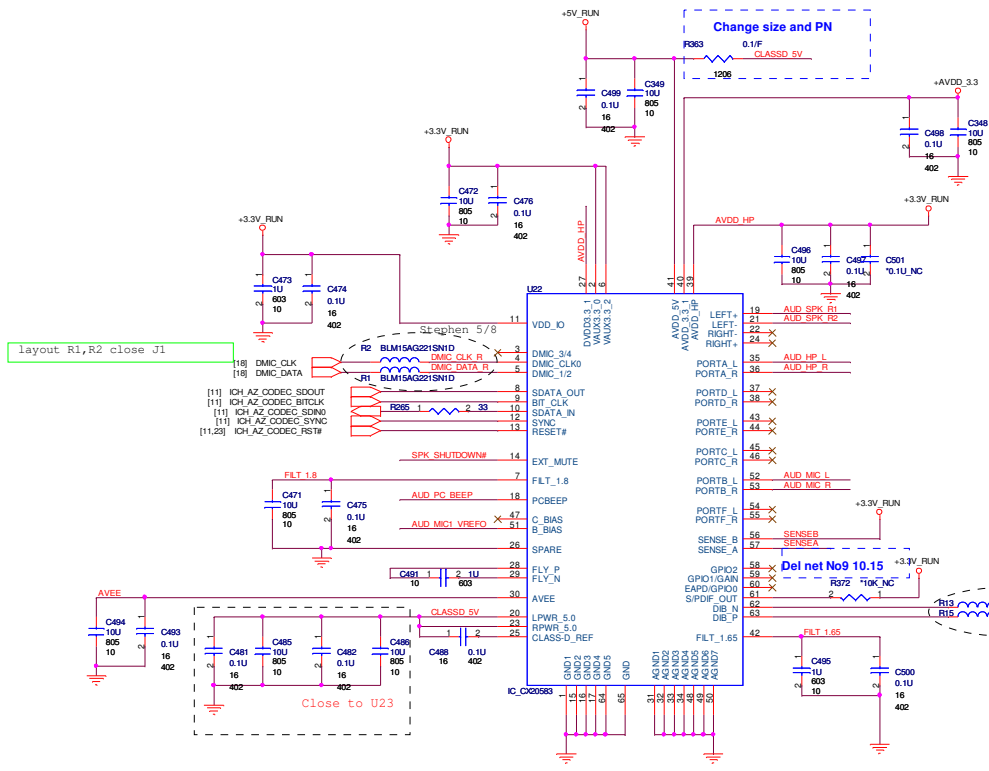




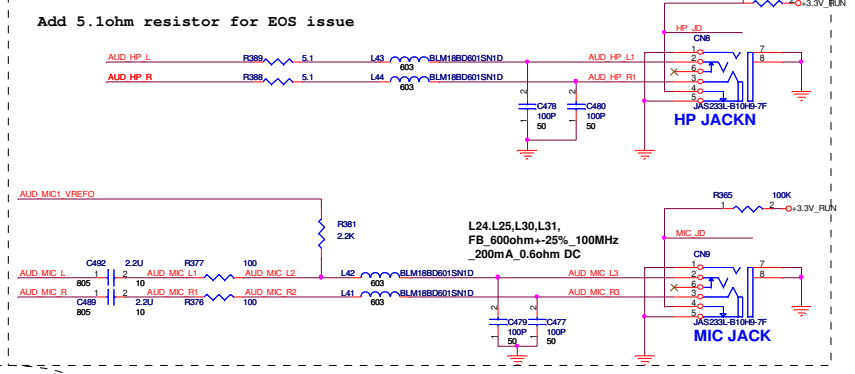


Add PC beep for system error circuit No9 10.14
Del PC beep No9 10.15

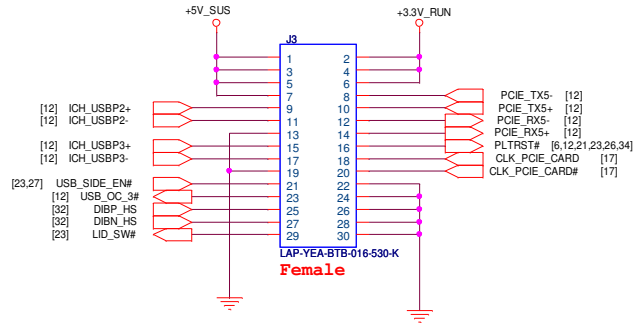
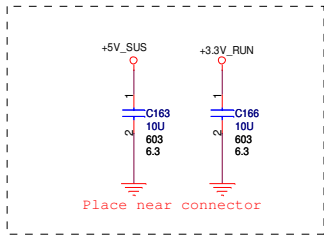
AUDIO CODEC



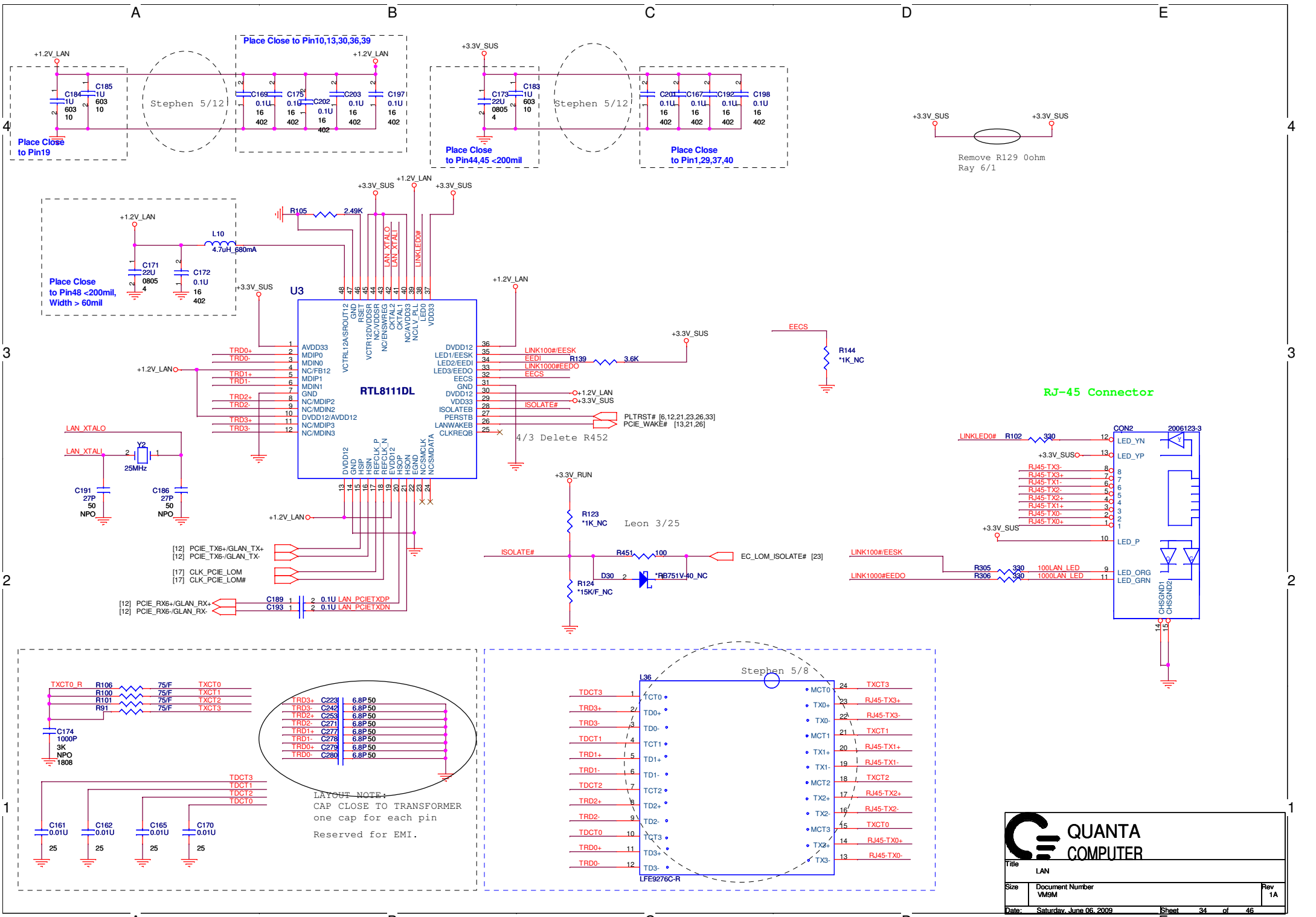
Audio Jacks



Title		
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Board to board connector (Modem Card + Cardreader+1394a+ 2 USB Port)



4

3

2

1

4

3

2

1

QUANTA COMPUTER

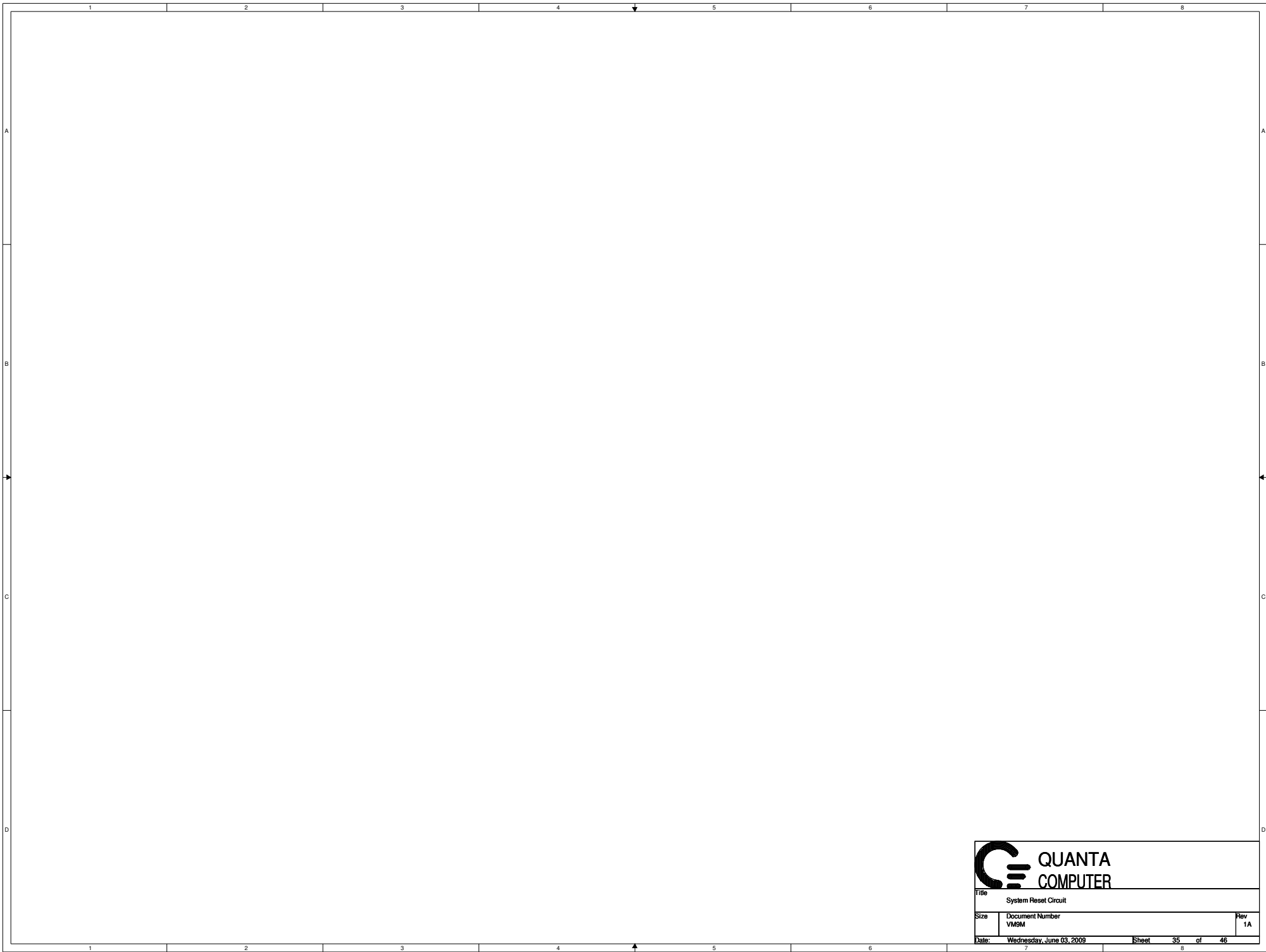
Title: LAN

Size: Document Number VM9M

Date: Saturday, June 06, 2009

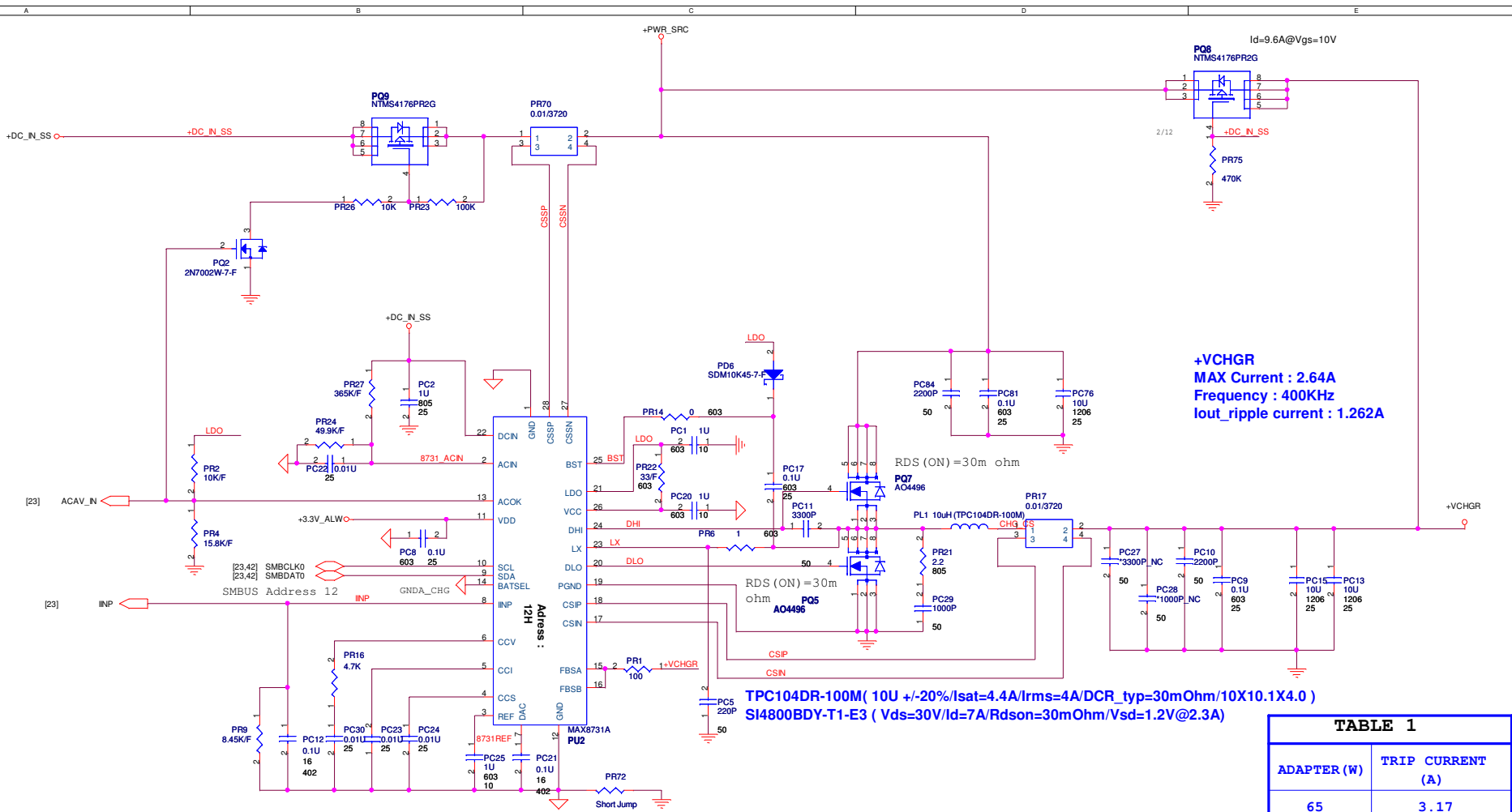
Sheet: 34 of 46

Rev: 1A



**QUANTA
COMPUTER**

Title		
System Reset Circuit		
Size	Document Number	Rev
	VMSM	1A
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+VCHGR
MAX Current : 2.64A
Frequency : 400KHz
Iout_ripple current : 1.262A

TPC104DR-100M (10U +/-20%/Isat=4.4A/Irms=4A/DCR_typ=30mOhm/10X10.1X4.0)
SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm/Vsd=1.2V@2.3A)

ADAPTER (W)	TRIP CURRENT (A)
65	3.17
90	4.43
130	6.43
150	7.43
200	9.75
230	11.28

QUANTA COMPUTER

Title: Charger (MAX8731A)

Size: Document Number VM9M Rev: 1A

Date: Saturday, June 06, 2009 Sheet: 36 of 46

Remove PR3 0ohm
Ray 6/3

[23.38.41] RUN_ON

[23.38] HWPG

Remove PR18 0ohm
Ray 6/3

PC7
0.1U_NC

SJ8

PR13
300.0603

PC19
1U10V/0603

PC16
0.1U_NC
50
603

PC16
0.1U_NC
50
603

PC16
0.1U_NC
50
603

PC16
0.1U_NC
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PC16
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PC16
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603

PC16
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50
603

PC16
0.1U_NC
50
603

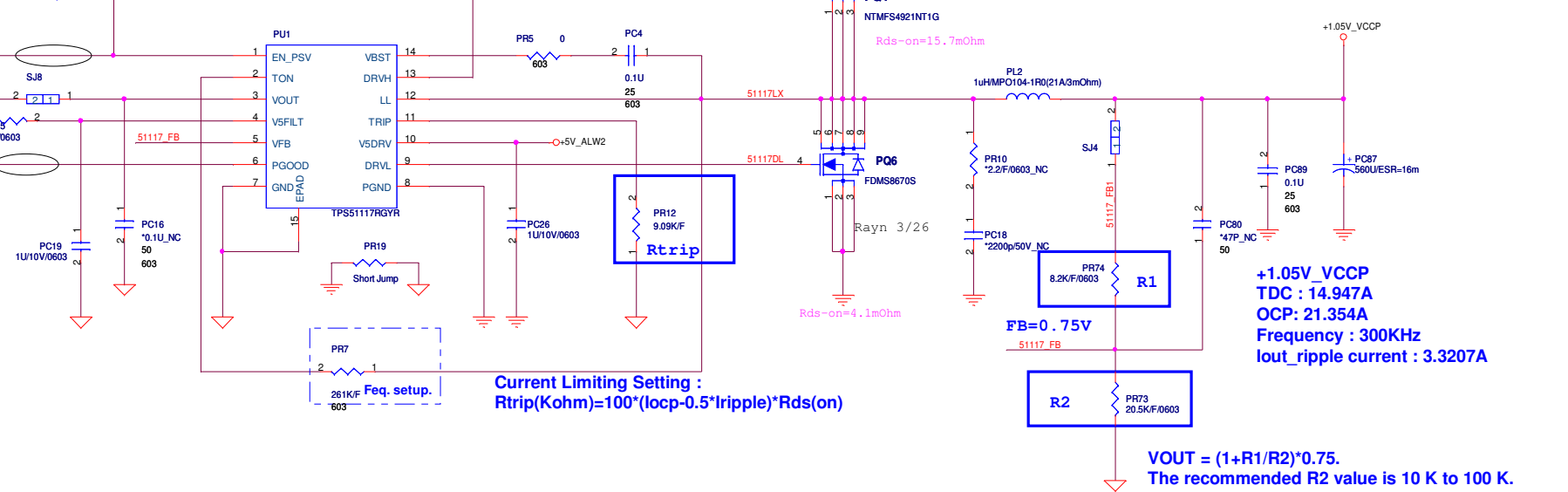
PC16
0.1U_NC
50
603

PC16
0.1U_NC
50
603

PC16
0.1U_NC
50
603

PC16
0.1U_NC
50
603

PC16
0.1U_NC
50
603



Current Limiting Setting :
 $R_{trip}(\text{Kohm}) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$

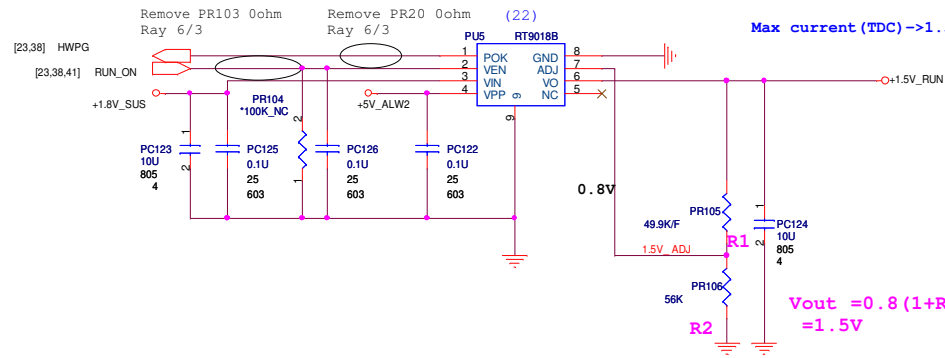
+1.05V_VCCP
TDC : 14.947A
OCP: 21.354A
Frequency : 300KHz
I_{out_ripple} current : 3.3207A

$V_{OUT} = (1 + R1/R2) * 0.75$
The recommended R2 value is 10 K to 100 K.

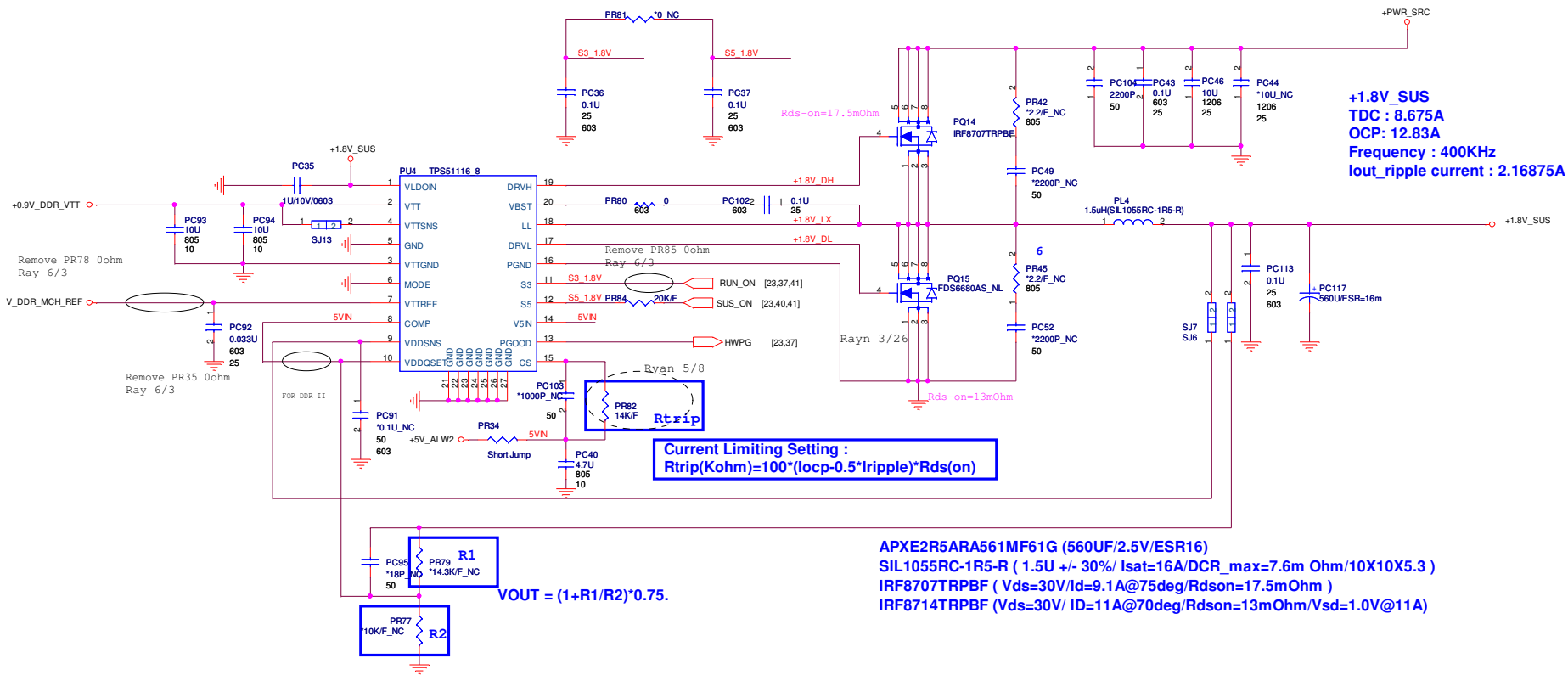
APXE2R5ARA561ME61G (560UF/2.5V/ESR16)
MPO104-1R0 (1.0U +/- 20% Isat=30A/DCR_max=3m Ohm/11.5X10X4)

NTMFS4921NT1G (V_{ds}=30V/I_d=10.2A@85deg/R_{ds(on)}=10.5mOhm)
NTMFS4946NT1G (V_{ds}=30V/ I_D=14.6A@85deg/R_{ds(on)}=5.1mOhm/V_{sd}=1.0V@30A)

Max current (TDC) -> 1.505A



$V_{out} = 0.8 (1 + R1/R2)$
 $= 1.5V$

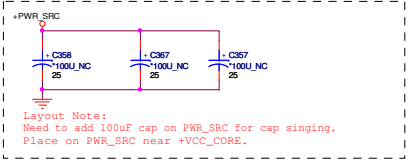


+1.8V_SUS
TDC : 8.675A
OCP: 12.83A
Frequency : 400KHz
Iout_ripple current : 2.16875A

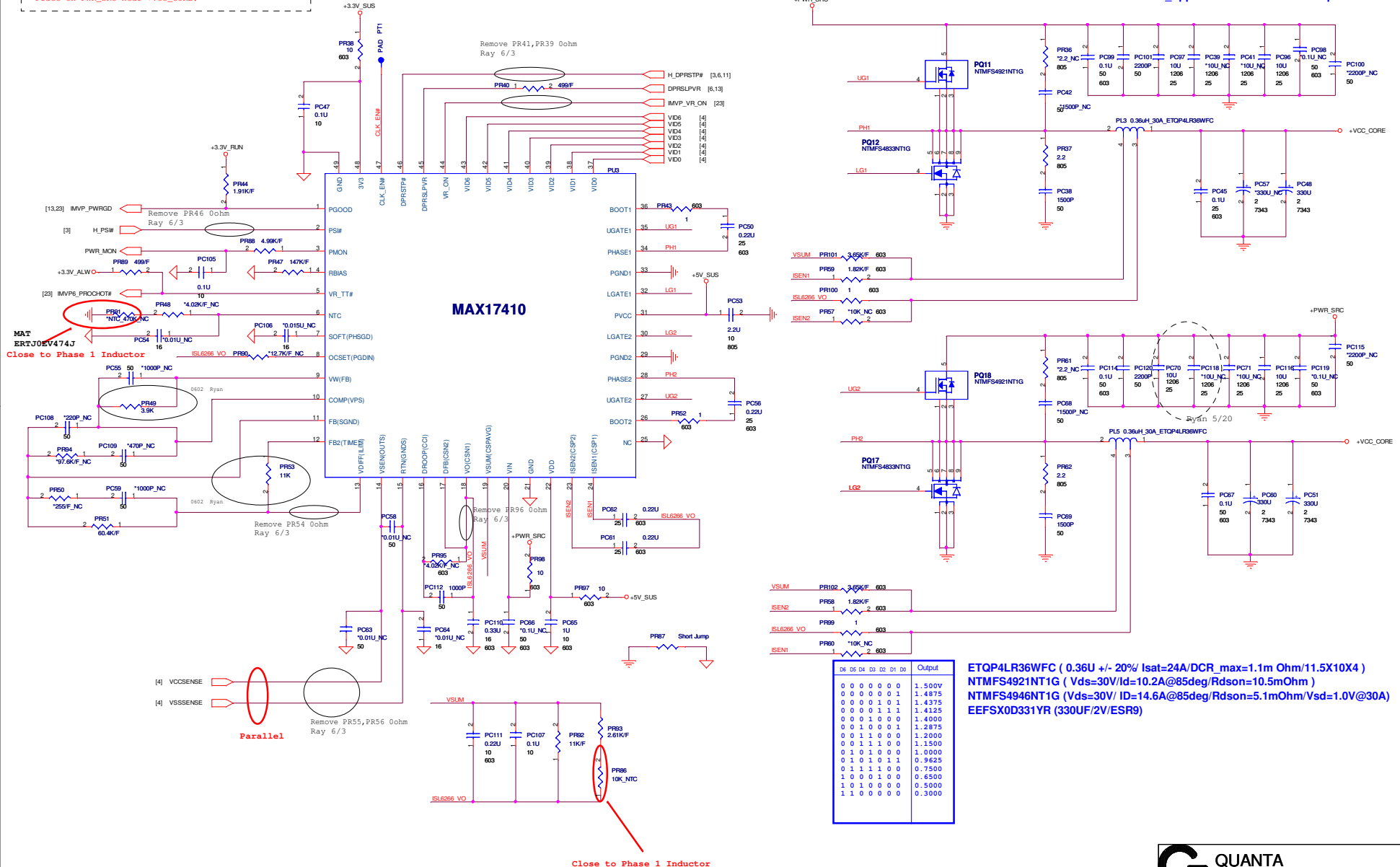
Current Limiting Setting :
 $R_{trip}(Kohm) = 100 * (I_{ocp} - 0.5 * I_{ripple}) * R_{ds(on)}$

APX2R5ARA561MF61G (560UF/2.5V/ESR16)
SIL1055RC-1R5-R (1.5U +/- 30%/ Isat=16A/DCR_max=7.6m Ohm/10X10X5.3)
IRF8707TRPBF (Vds=30V/Id=9.1A@75deg/Rdson=17.5mOhm)
IRF8714TRPBF (Vds=30V/ ID=11A@70deg/Rdson=13mOhm/Vsd=1.0V@11A)

$V_{OUT} = (1 + R1/R2) * 0.75.$



+VCC_CORE
TDC : 35A
MAX:47A
Frequency : 300KHz
Iout_ripple current : 9.64A of each phase.

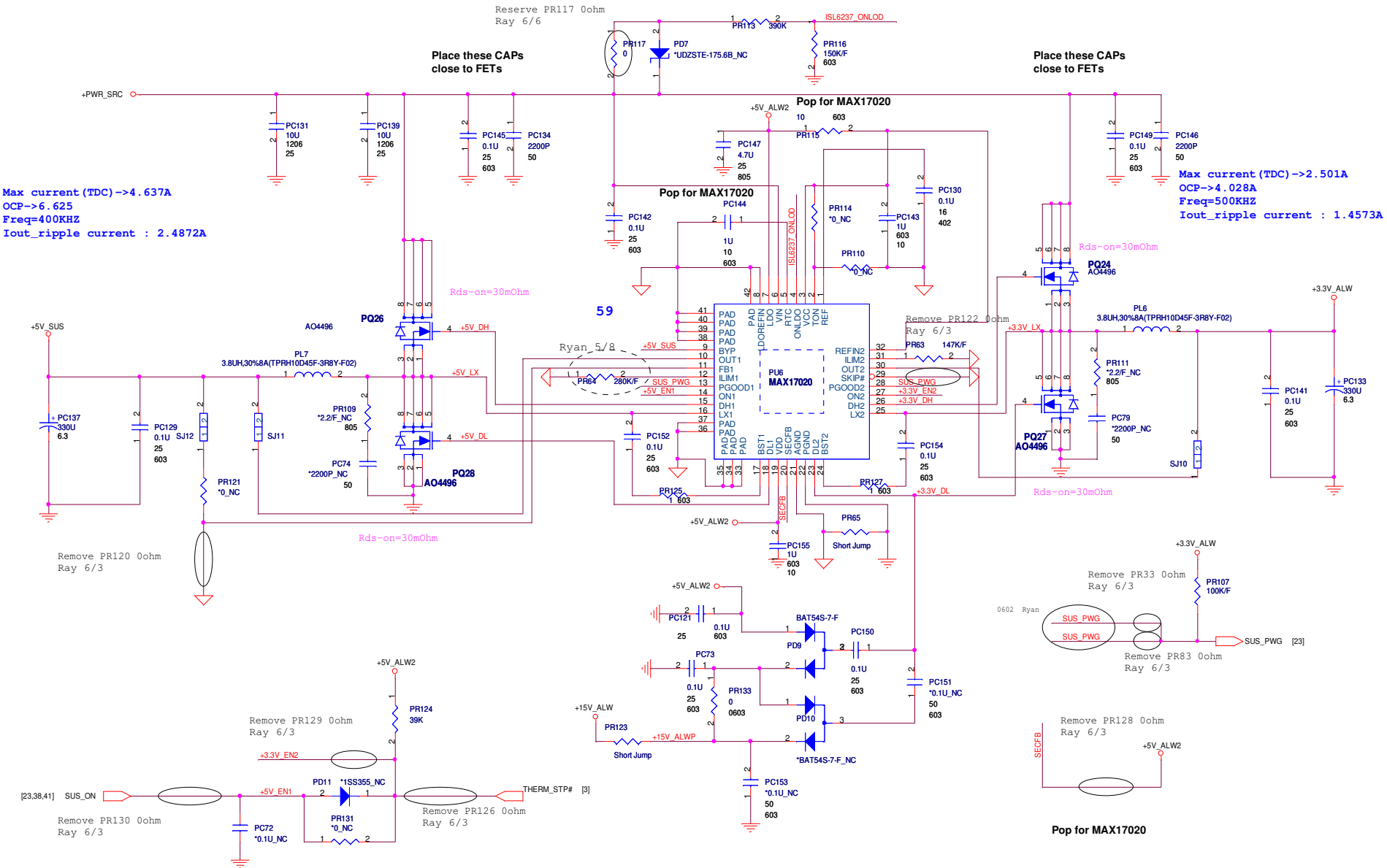


D6	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	0	1.500V
0	0	0	0	0	0	1	1.4875
0	0	0	1	0	1	1	1.4375
0	0	0	1	1	1	1	1.4125
0	0	0	1	1	0	0	1.4000
0	0	1	0	0	0	1	1.2875
0	0	1	1	0	0	0	1.2000
0	1	1	1	0	0	0	1.1500
0	1	0	1	0	0	0	1.0000
0	1	0	1	1	1	0	0.9625
0	1	1	1	1	0	0	0.7500
1	0	0	1	0	0	0	0.6500
1	0	1	0	0	0	0	0.5000
1	1	0	0	0	0	0	0.3000

ETQP4LR36WFC (0.36u +/- 20% /Isat=24A/DCR_max=1.1m Ohm/11.5X10X4)
 NTMFS4921NT1G (Vds=30V/Id=10.2A@85deg/Rdson=10.5mOhm)
 NTMFS4946NT1G (Vds=30V/ ID=14.6A@85deg/Rdson=5.1mOhm/Vsd=1.0V@30A)
 EEF5X0D331YR (330UF/2V/ESR9)



DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW



Max current (TDC) -> 4.637A
 OCP -> 6.625
 Freq=400KHZ
 Iout_ripple current : 2.4872A

Max current (TDC) -> 2.501A
 OCP -> 4.028A
 Freq=500KHZ
 Iout_ripple current : 1.4573A

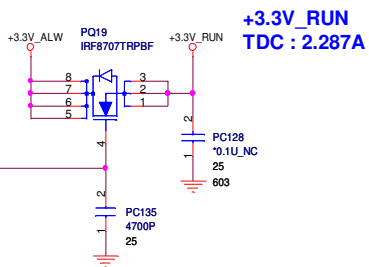
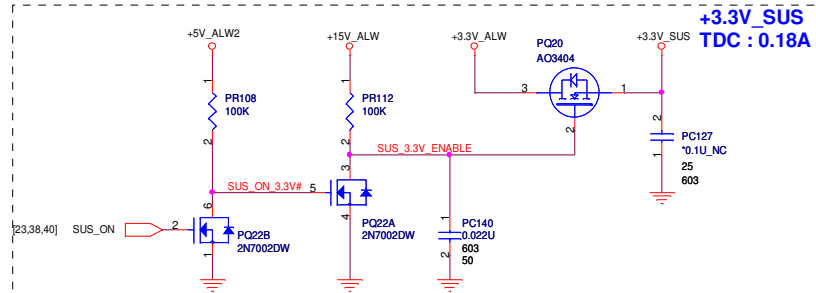
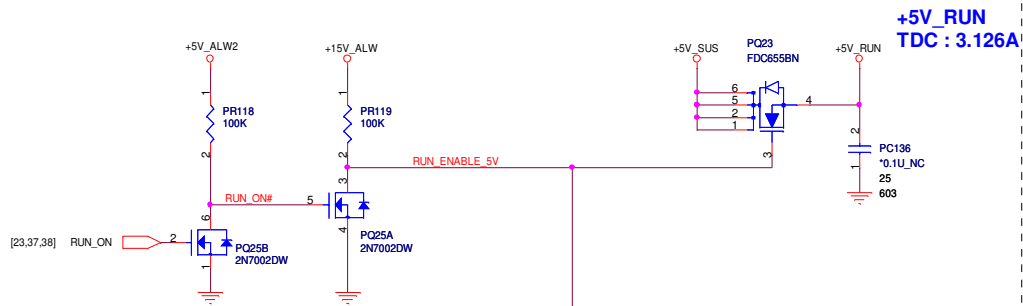
APX6R3ARA331MF61G (330UF/6.3V/ESR17)
 TPC104DR-3R8Y(3.8U +/- 30%/ Isat=6A/DCR_max=12m Ohm/10X10X4)
 SI4800BDY-T1-E3 (Vds=30V/Id=7A/Rdson=30mOhm/Vsd=1.2V@2.3A)

QUANTA COMPUTER

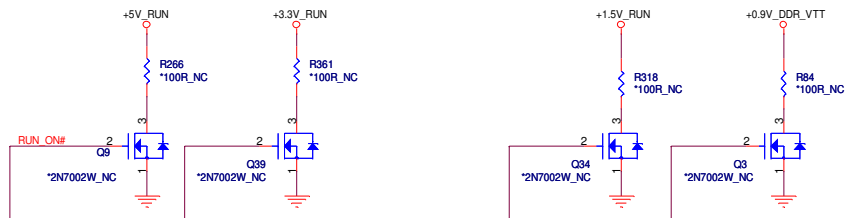
Title: 3VALW,5V,3V,(MAX17020)

Size: Document Number: VMSM Rev: 1A

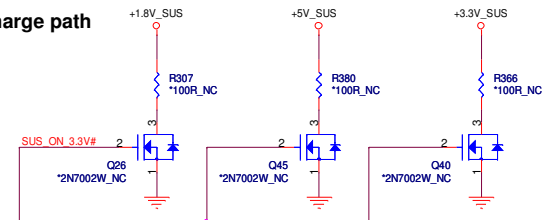
Date: Saturday, June 06, 2009 Sheet: 40 of 46



Reserve discharge path

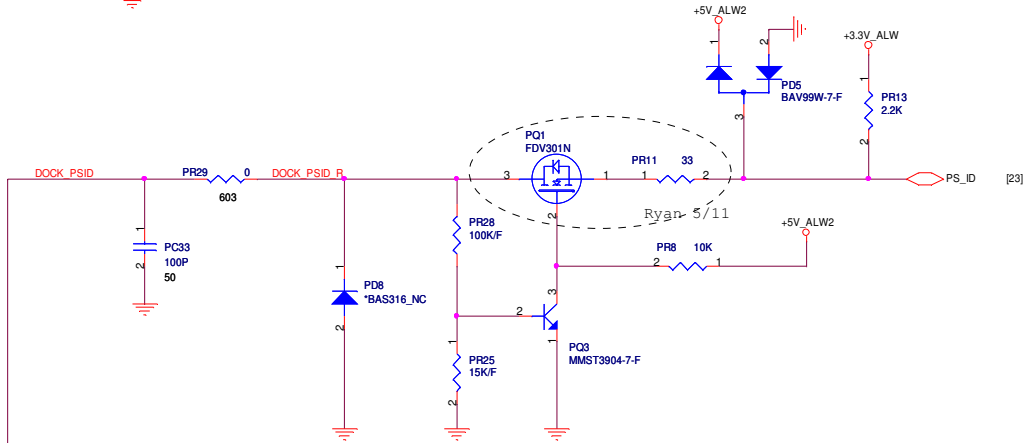
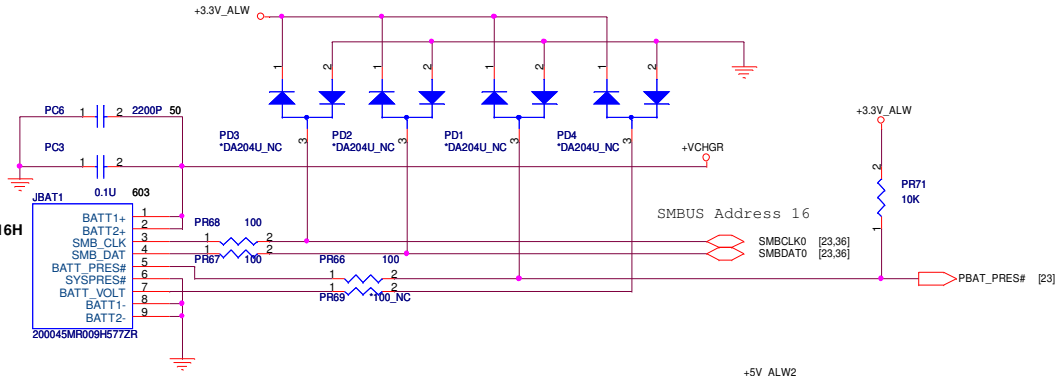


Reserve discharge path

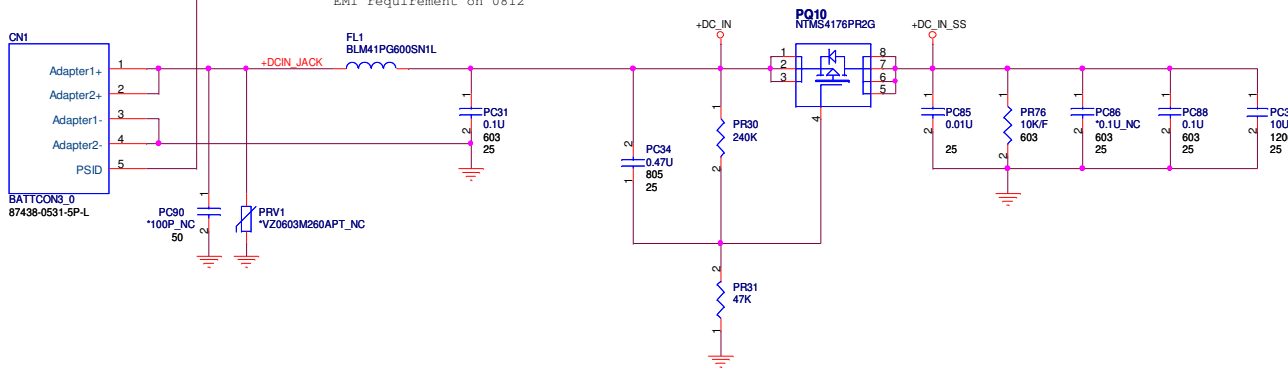



Title RUN POWER SW		
Size VMSM	Document Number VMSM	Rev 1A
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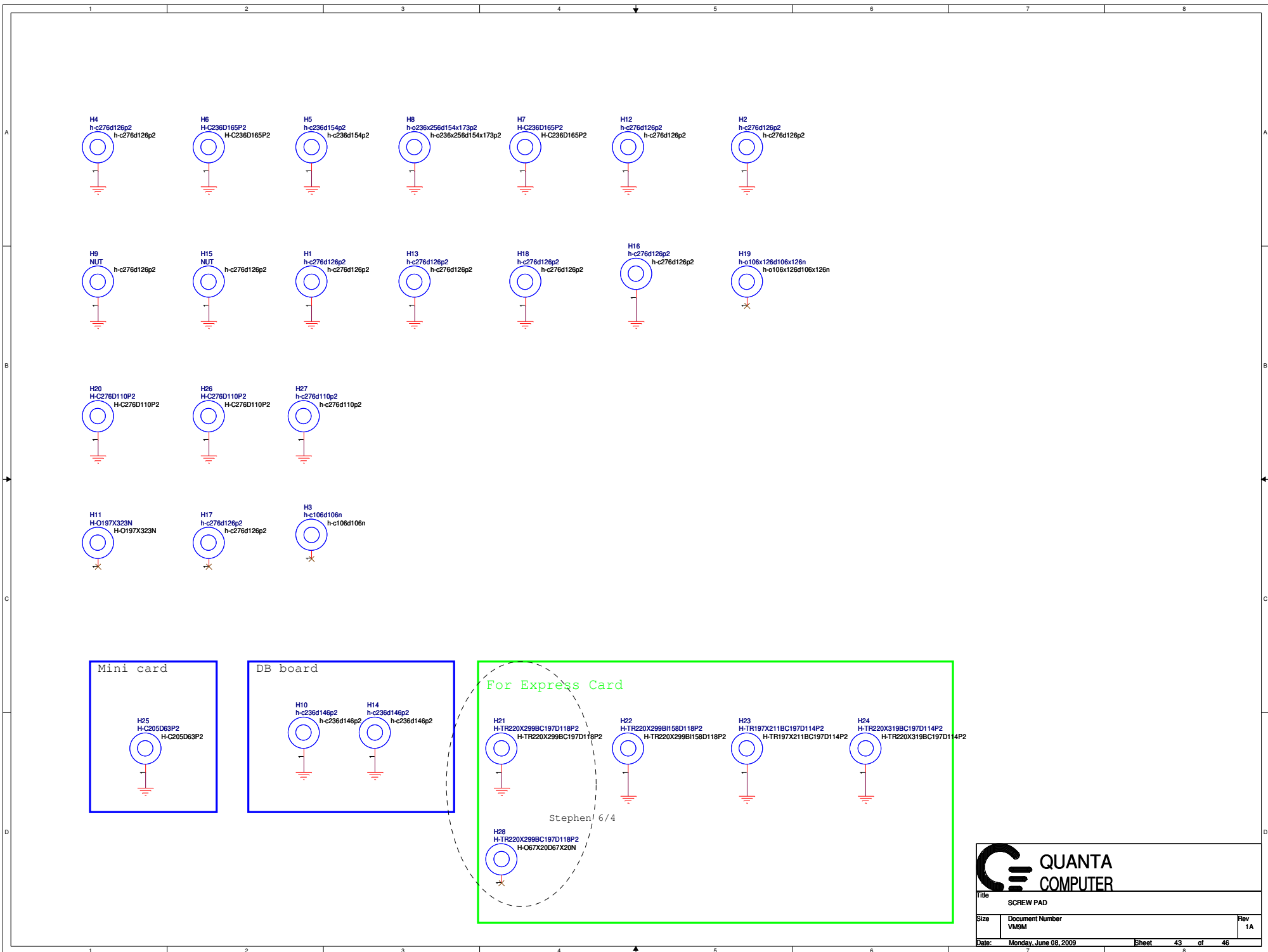
Adress : 16H



Change Value per GG updated
EMI requirement on 0812



 QUANTA COMPUTER		
File DCINBATT CONNECTOR		
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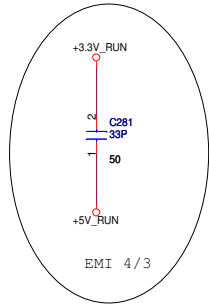
QUANTA COMPUTER


Title: SCREW PAD

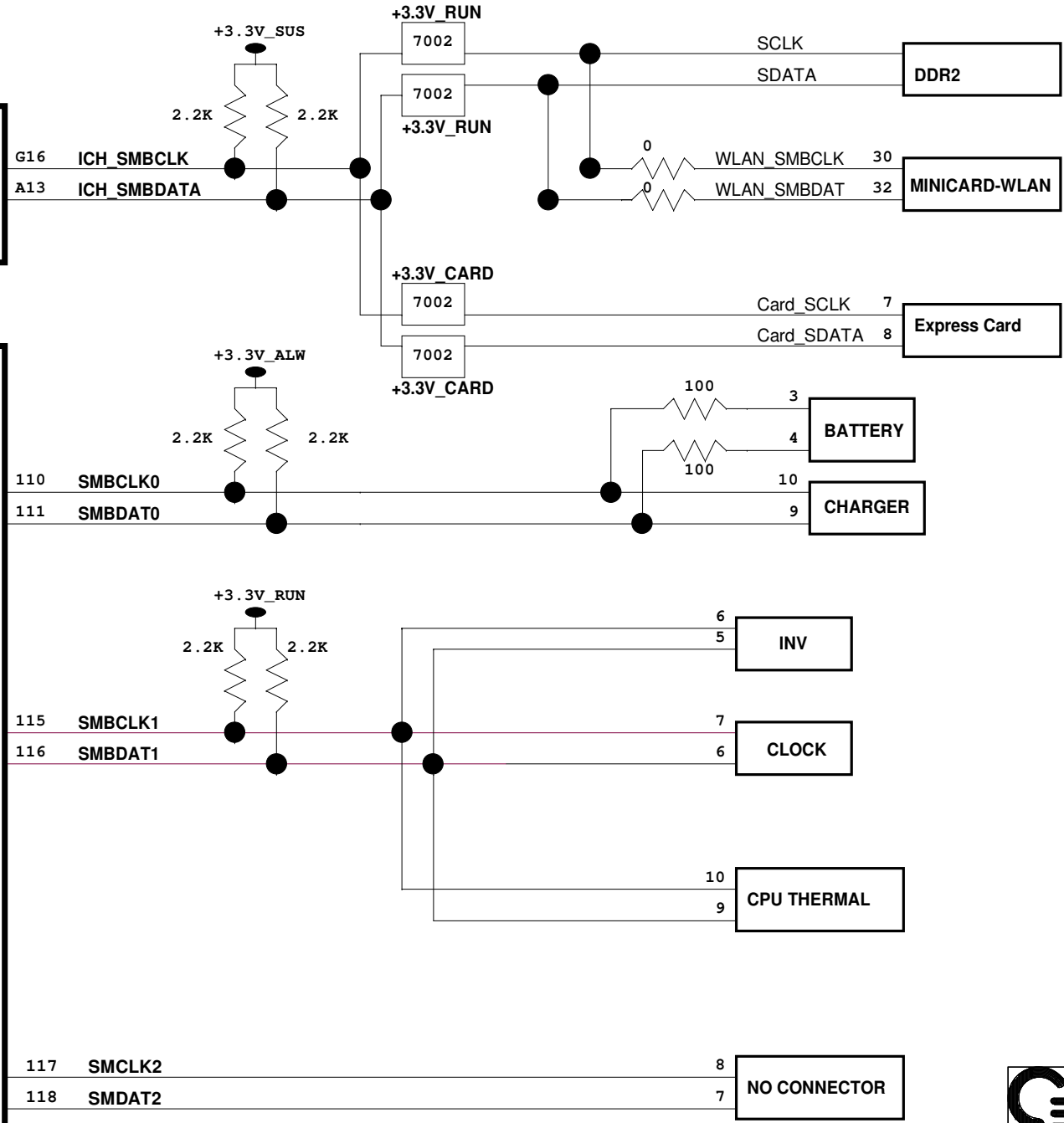
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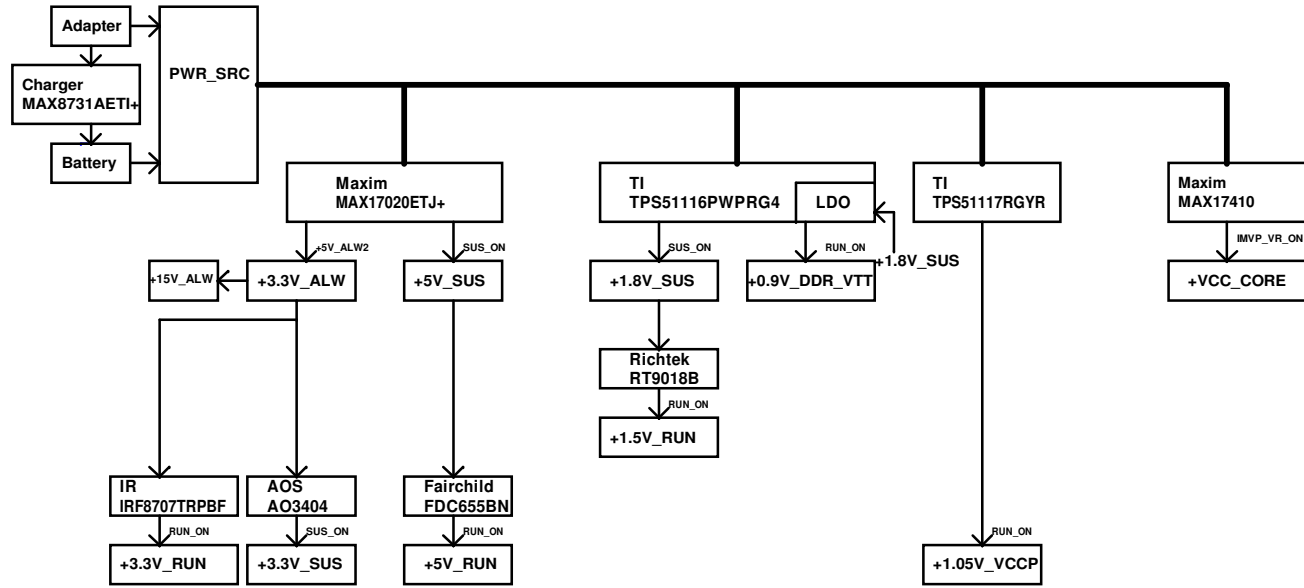
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