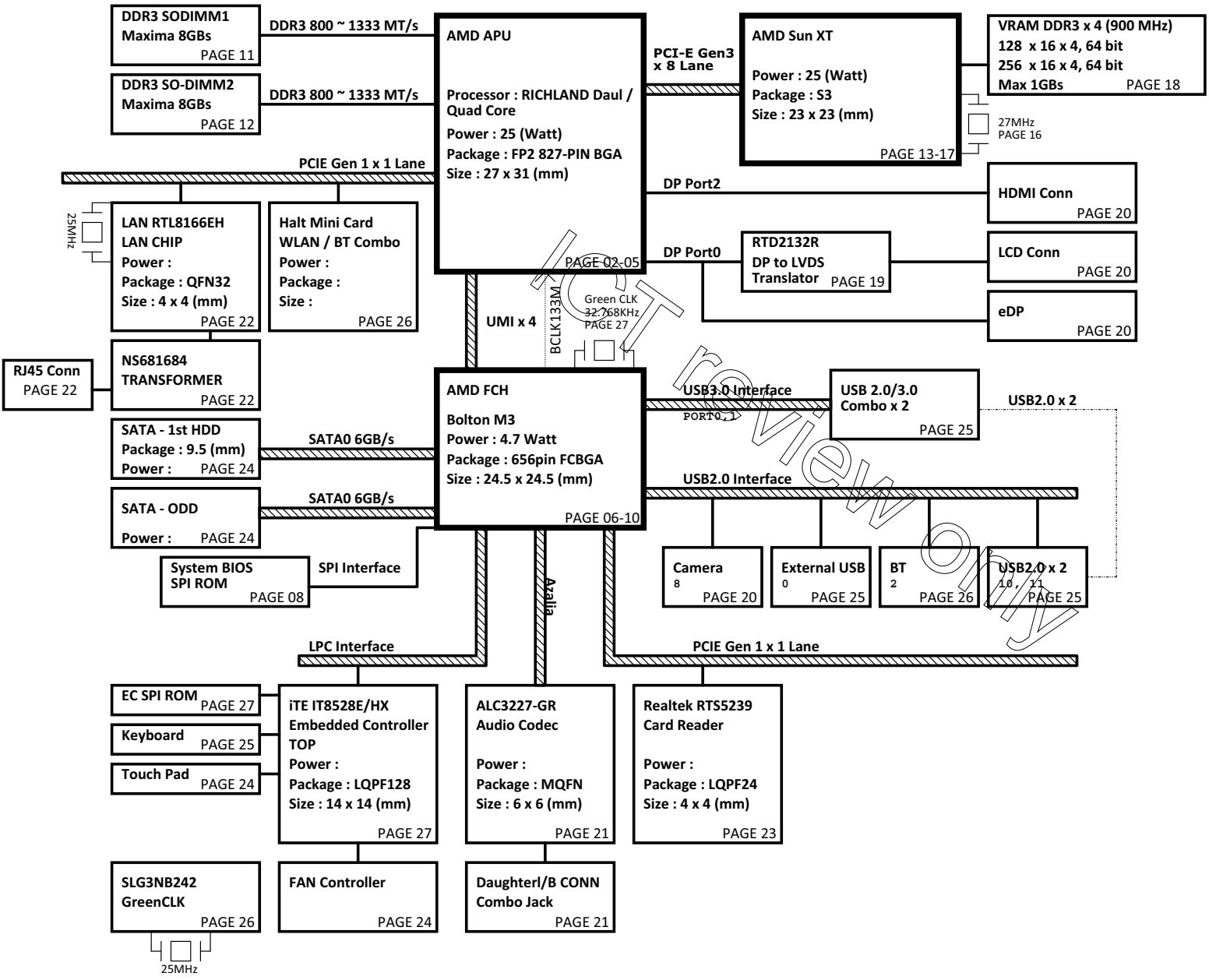


Perrier_AMD RICHLAND DIS/UMA (14"/15.6")



PCB 6L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : BOT

Power Source

BQ24728
 System Charge Power (+BATCHG)

G5934RZ1U
 System Discharge Power (+1.5V/+3V/+5V) (+3VSUSV/+3VLAVCC/+1.1V)

Ricktek RT8223PZ
 System Power (+3VPCU/+5VPCU/+3VS5/+5VS5)

SL6277/RT8228AZ/AP3407A/ISL6208BCRZ
 Processor Power (+VCC_CORE/+1.2V/+2.5V/+VDDNB_CORE)

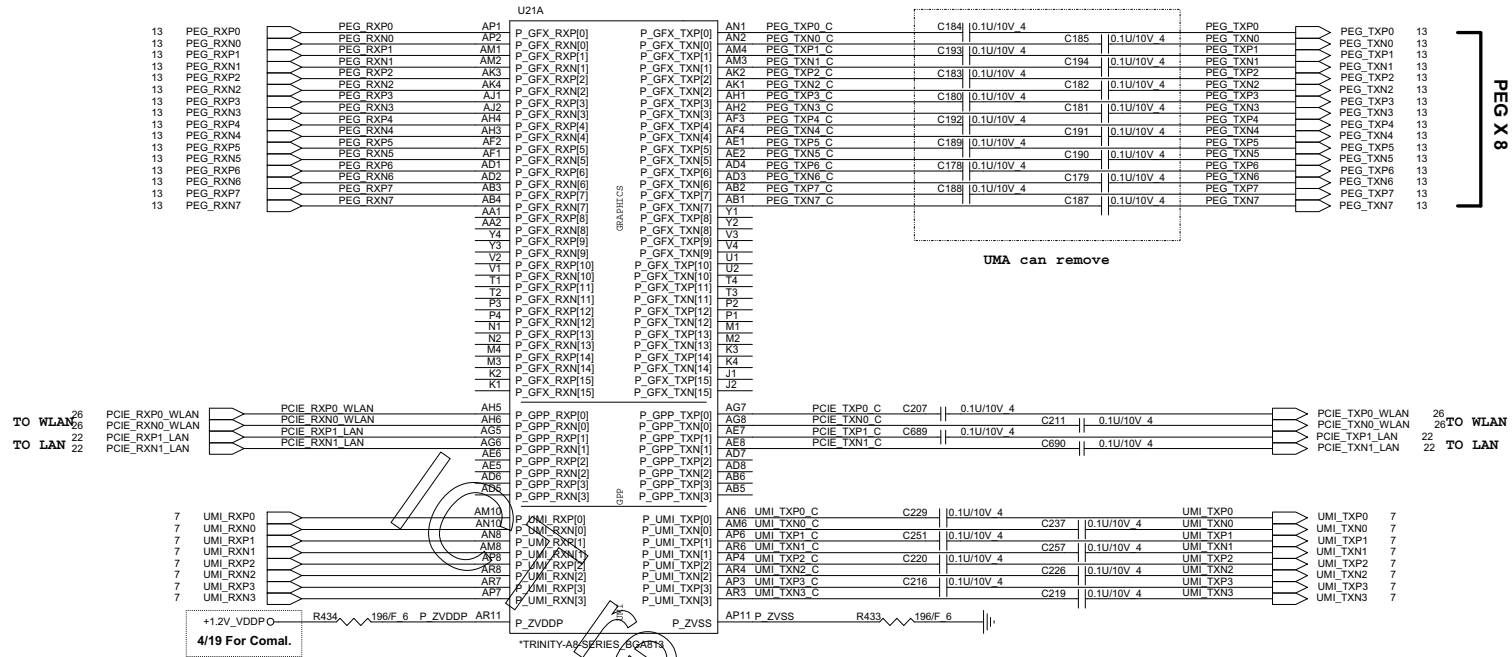
TP551216RUKR
 System Memory Power (+1.5VSUS/+0.75V_DDR_VTT)

AOZ1237QI-02
 PCH Power (+1.1VS5)

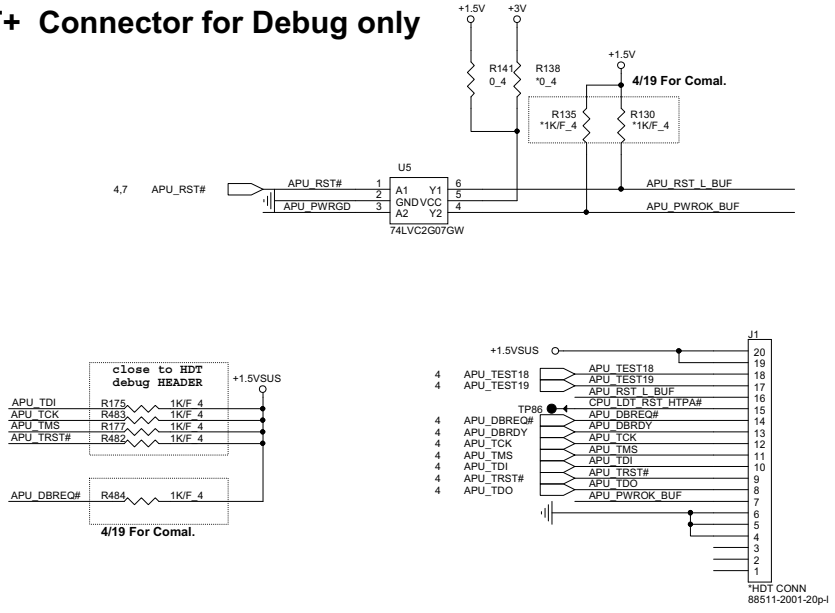
ADP3211A
 DGPU Power (+VGA_CORE/+1.0V_VGA/+3V_VGA/+1.5V_VGA/+1.8V_VGA/+VDDCI)

PROJECT : U92
 Quanta Computer Inc.

Size A3	Document Number Block Diagram	Rev 1A
Date: Wednesday, March 27, 2013	Sheet	1 of 37

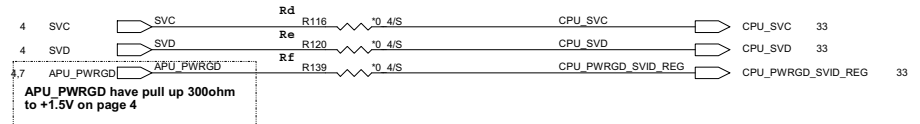


HDT+ Connector for Debug only



VID Override Circuit

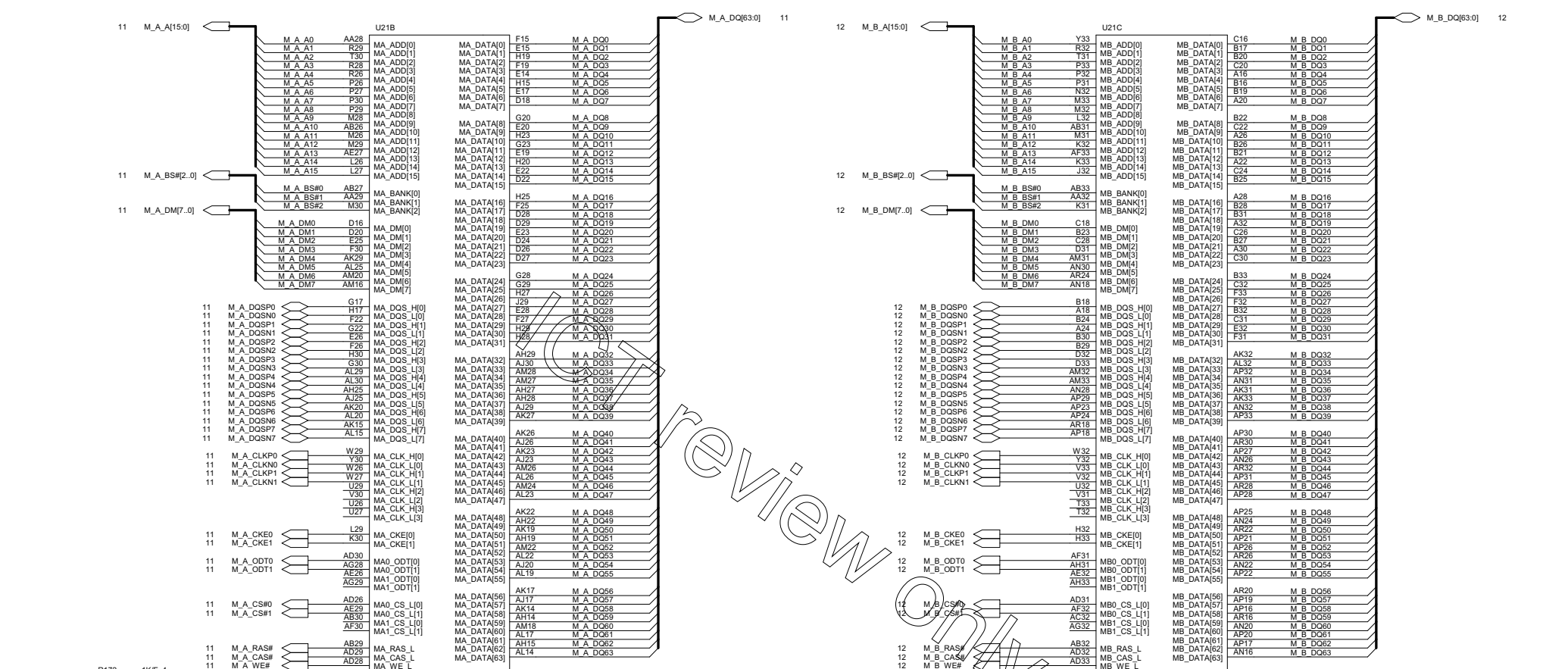
Note:
To override VID, Remove Rd, Re, Rf, install Rc
set VID via SVC2 & SVD option RES.



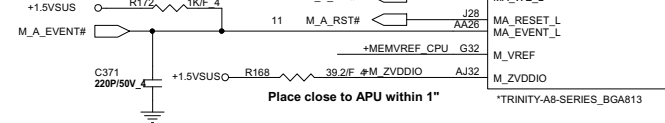
		BOOT VOLTAGE	
SVC	SVD	VFIX +VDD =VCC/GND	VFIX +VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

PROJECT : U92
Quanta Computer Inc.

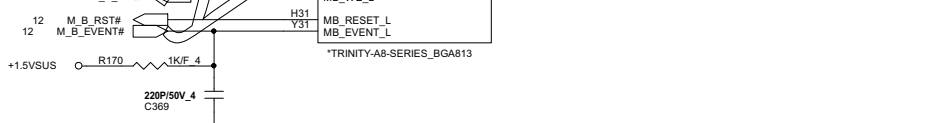
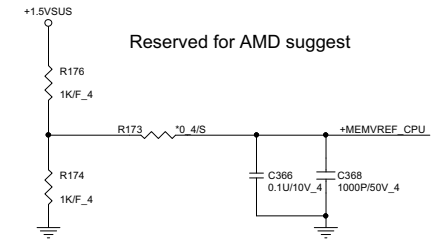
Size Custom Document Number **Liano PCIe/UMI/GPP** Rev 1A
Date: Wednesday, March 27, 2013 Sheet 2 of 37



Soldermask openings for all bottom side vias/TPs under FS1



Place close to APU within 1"



*TRINITY-A8-SERIES_BGA813

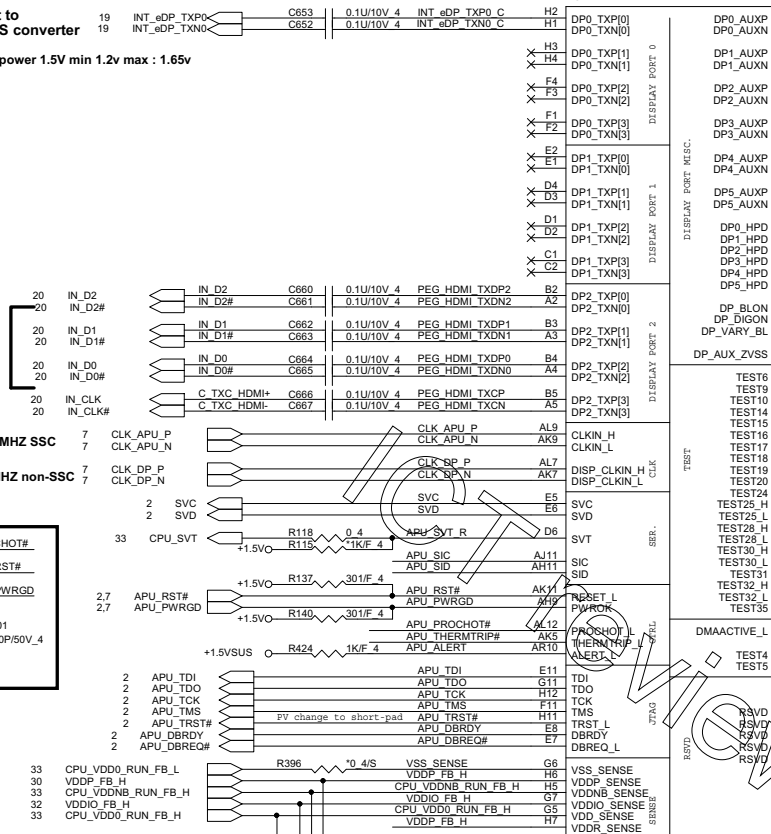
PROJECT : U92
Quanta Computer Inc.

Size Custom Document Number Liano DDR3 MEM I/F Rev 1A
 Date: Wednesday, March 27, 2013 Sheet 3 of 37

Place caps with APU < 1 inch
route PCIe as 85ohm +/- 10%

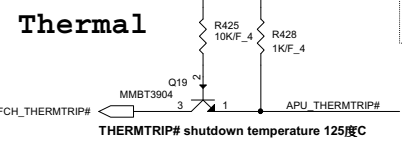
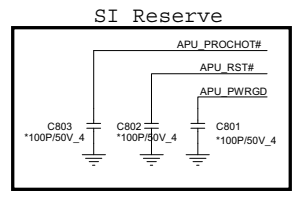
DP0 output to
eDP to LVDS converter

Display port power 1.5V min 1.2v max : 1.65v

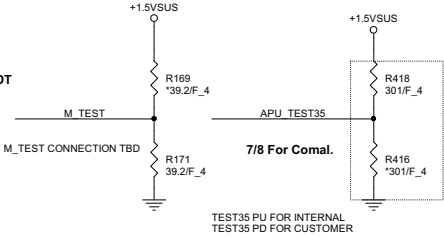
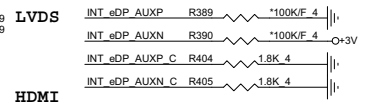


4/19 HDMI change to DP2 for Comal.
DP2 output to
HDMI connector
note --HDMI P&N can not swap

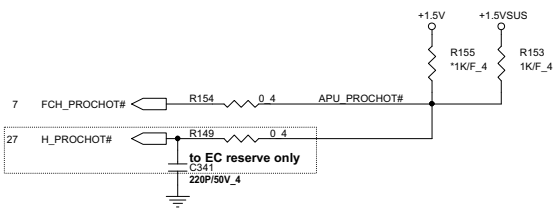
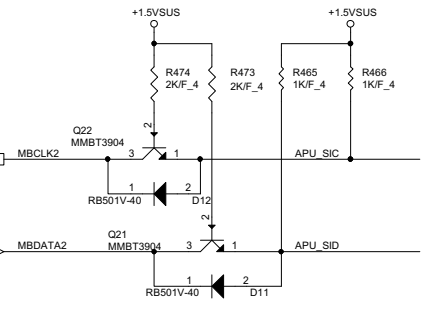
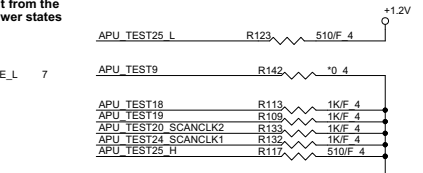
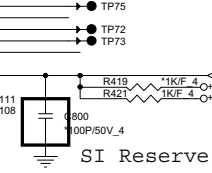
Note: CLK_APU_HCLKP/N is 100MHZ SSC
Note: CLK_DP_NSSCP/N is 100MHZ non-SSC



TP95
TP47
TP96
TP45
4/19 For Comal,
close to APU.



DMAACTIVE_L controls
entry and exit from the
sleep and power states

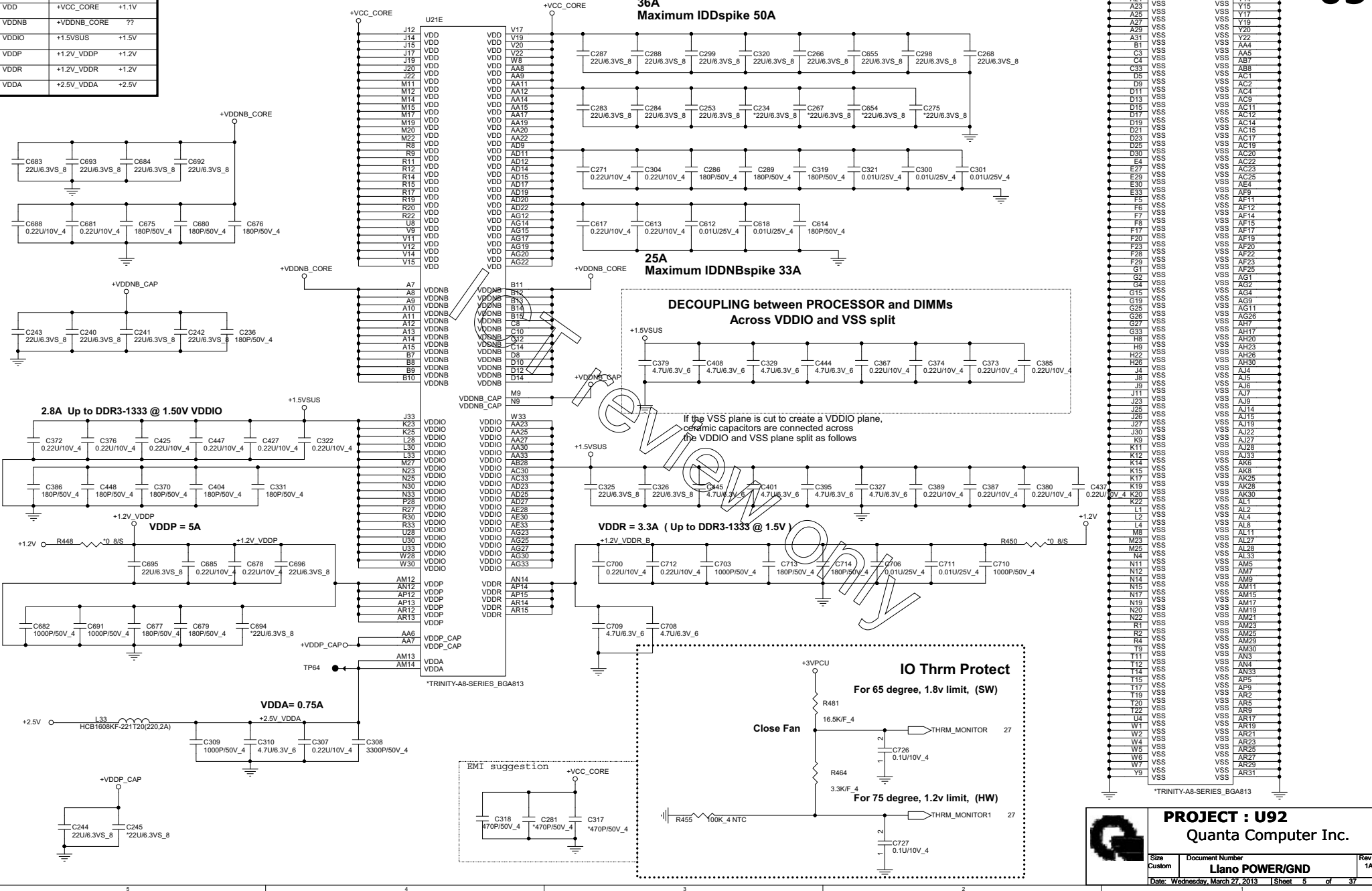


*TRINITY-A8-SERIES_BGA813

PROJECT : U92
Quanta Computer Inc.
Size Document Number Rev
Llano Display/Misc 1A
Date: Wednesday, March 27, 2013 Sheet 4 of 37

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



U21F

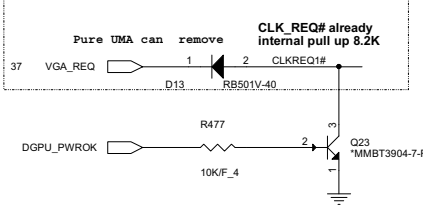
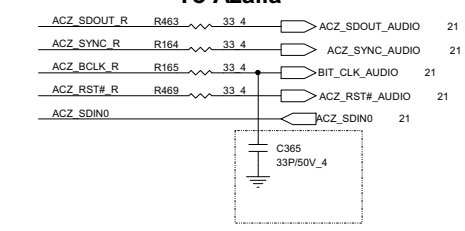
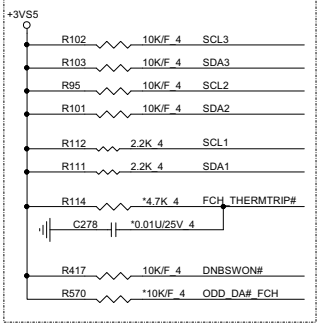
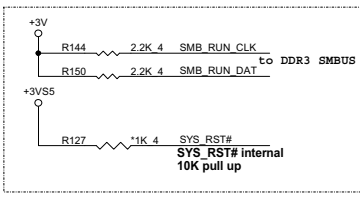
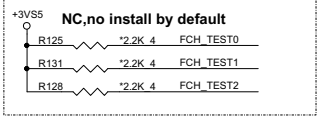
A17	VSS	Y11
A21	VSS	Y12
A23	VSS	Y14
A25	VSS	Y15
A27	VSS	Y17
A29	VSS	Y19
A31	VSS	Y22
B1	VSS	AA4
C3	VSS	AA5
C4	VSS	AB7
C33	VSS	AB8
D5	VSS	AC1
D9	VSS	AC2
D11	VSS	AC4
D13	VSS	AC9
D15	VSS	AC11
D17	VSS	AC12
D19	VSS	AC14
D21	VSS	AC15
D23	VSS	AC17
D25	VSS	AC19
D30	VSS	AC20
E4	VSS	AC22
E27	VSS	AC23
E29	VSS	AC25
E30	VSS	AE4
E33	VSS	AE6
F5	VSS	AF11
F6	VSS	AF12
F7	VSS	AF14
F8	VSS	AF15
F17	VSS	AF17
F20	VSS	AF19
F23	VSS	AF20
F28	VSS	AF22
F29	VSS	AF23
G1	VSS	AF25
G2	VSS	AG1
G4	VSS	AG2
G15	VSS	AG4
G19	VSS	AG9
G25	VSS	AG11
G26	VSS	AG26
G33	VSS	AG7
H8	VSS	AH20
H9	VSS	AH23
H22	VSS	AH26
H28	VSS	AH30
J4	VSS	AJ4
J8	VSS	AJ5
J9	VSS	AJ6
J11	VSS	AJ7
J23	VSS	AJ9
J25	VSS	AJ14
J28	VSS	AJ15
J27	VSS	AJ19
J30	VSS	AJ22
K9	VSS	AJ27
K11	VSS	AJ28
K12	VSS	AJ33
K14	VSS	AK6
K15	VSS	AK8
K17	VSS	AK25
K19	VSS	AK28
K20	VSS	AK30
K27	VSS	AL1
L1	VSS	AL2
L2	VSS	AL4
L4	VSS	AL8
L8	VSS	AL11
M8	VSS	AL27
M23	VSS	AL28
M25	VSS	AL33
M4	VSS	AM4
N11	VSS	AM5
N12	VSS	AM7
N14	VSS	AM9
N15	VSS	AM11
N17	VSS	AM15
N19	VSS	AM17
N20	VSS	AM19
N22	VSS	AM21
R1	VSS	AM23
R2	VSS	AM25
R4	VSS	AM29
R19	VSS	AM30
T11	VSS	AN3
T12	VSS	AN4
T14	VSS	AN33
T15	VSS	AP5
T17	VSS	AP9
T19	VSS	AR2
T20	VSS	AR5
T22	VSS	AR9
U4	VSS	AR17
W1	VSS	AR19
W2	VSS	AR21
W4	VSS	AR23
W5	VSS	AR25
W6	VSS	AR27
W7	VSS	AR29
Y9	VSS	AR31

**TRINITY-A8-SERIES_BGA813

PROJECT : U92
Quanta Computer Inc.

Size: Custom | Document Number: Liano POWER/GND | Rev: 1A

Date: Wednesday, March 27, 2013 | Sheet: 5 of 37



GEVENT0# internal pull Hi 8.2K to +3V
 GEVENT1# internal pull Hi 8.2K to +3V
 GEVENT23# internal pull Hi 8.2K to +3V
 GEVENT5# internal pull Hi 8.2K to +3VS5
 PCIe_WAKE# no need to pull Hi resistor from check list

CLK_REQ2# internal pull Hi 8.2K to +3V
 CLK_REQ3# internal pull Hi 8.2K to +3V
 CLK_REQ4# internal pull Hi 8.2K to +3V

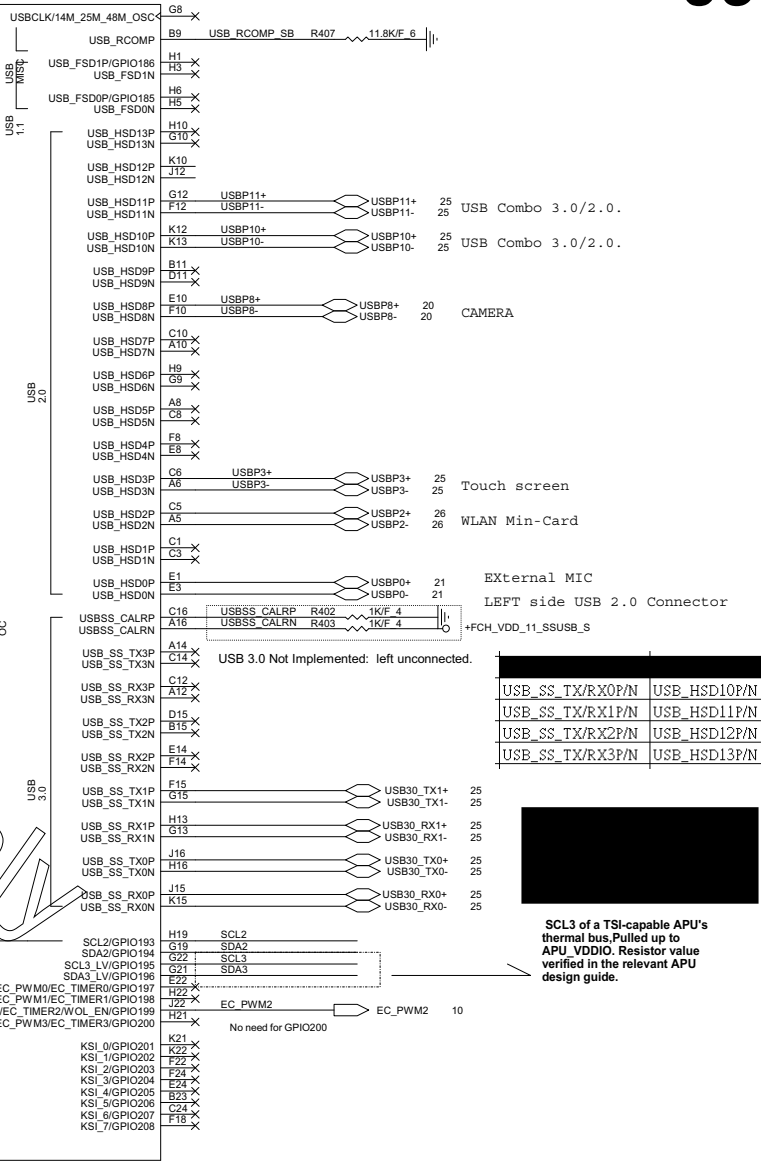
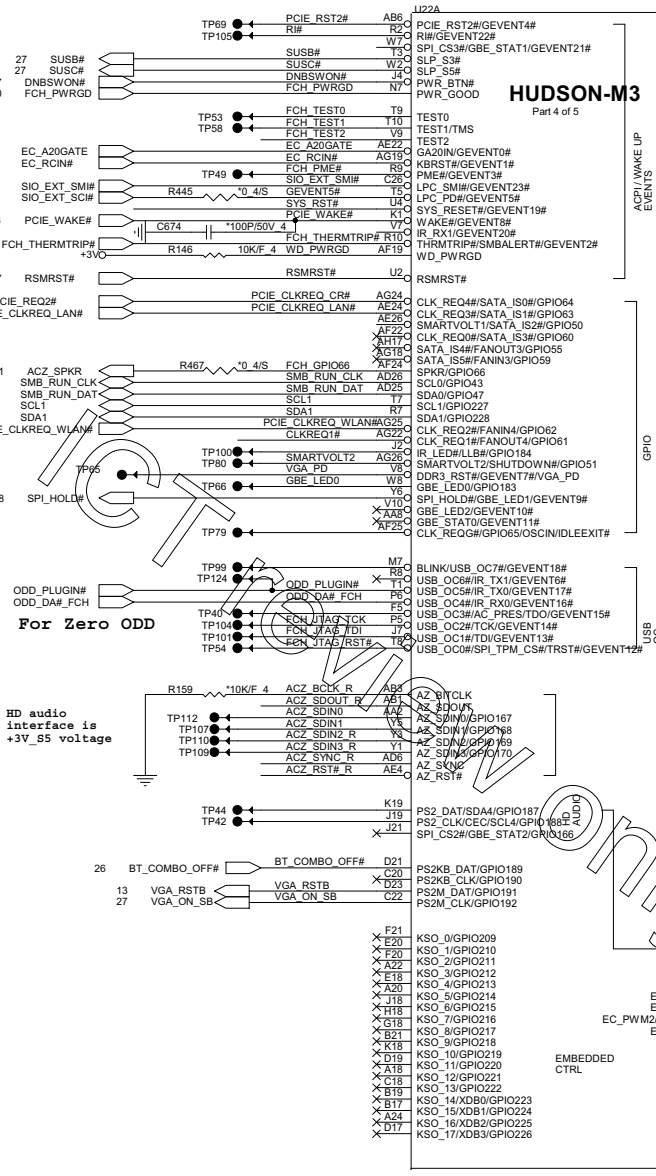
This pin is used to power down VGA DAC regulators when CRT no connected

GEVENT16# internal pull Hi 8.2K to +3VS5
 GEVENT15# internal pull Hi 8.2K to +3VS5

For Zero ODD

HD audio interface is +3V_S5 voltage

Pure UMA can remove CLK_REQ# already internal pull up 8.2K



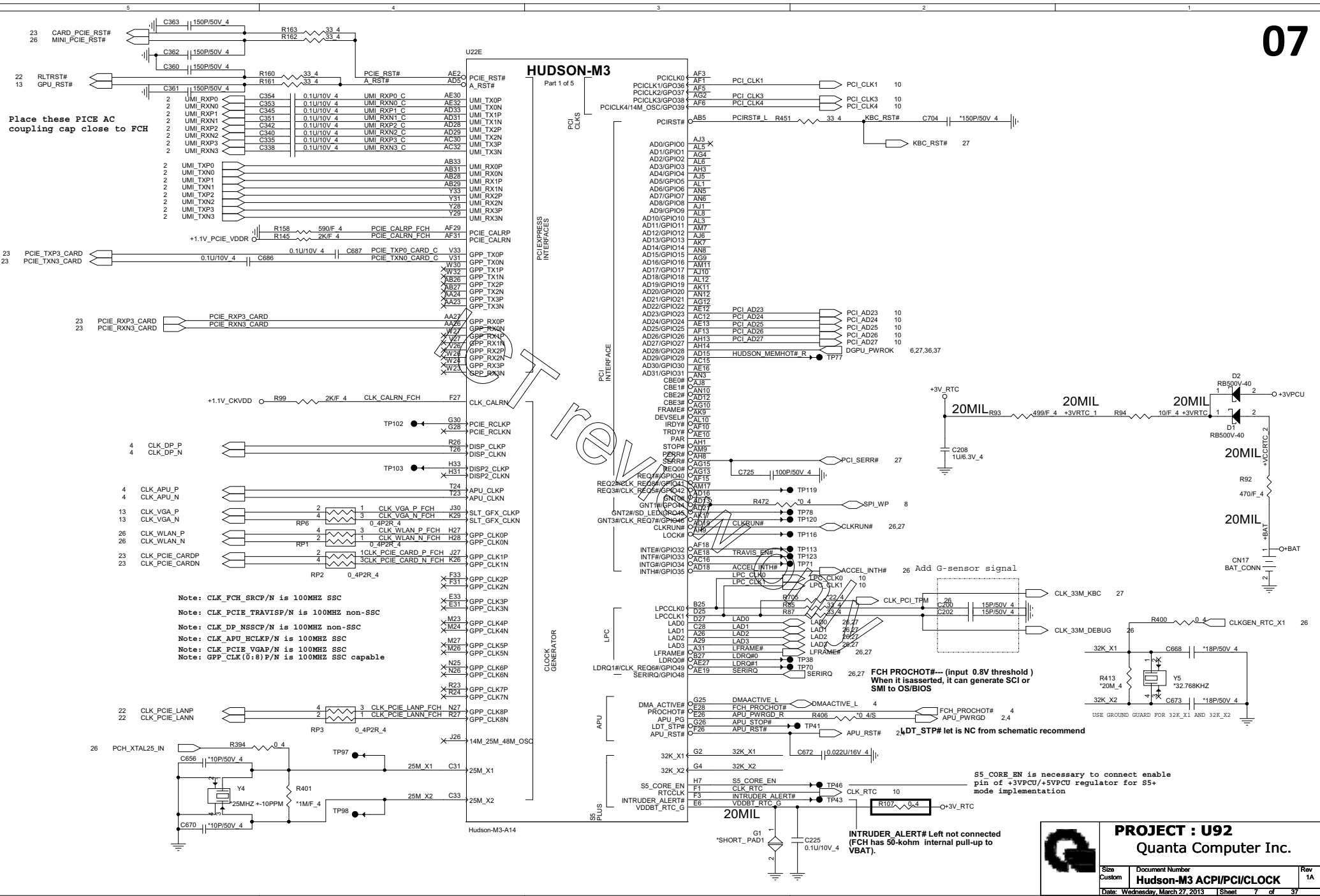
Hudson-M3-A14

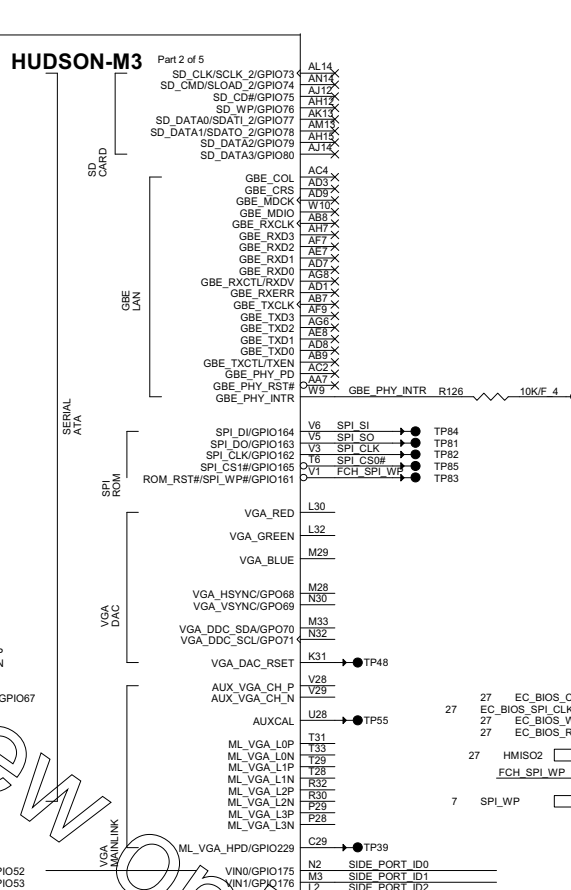
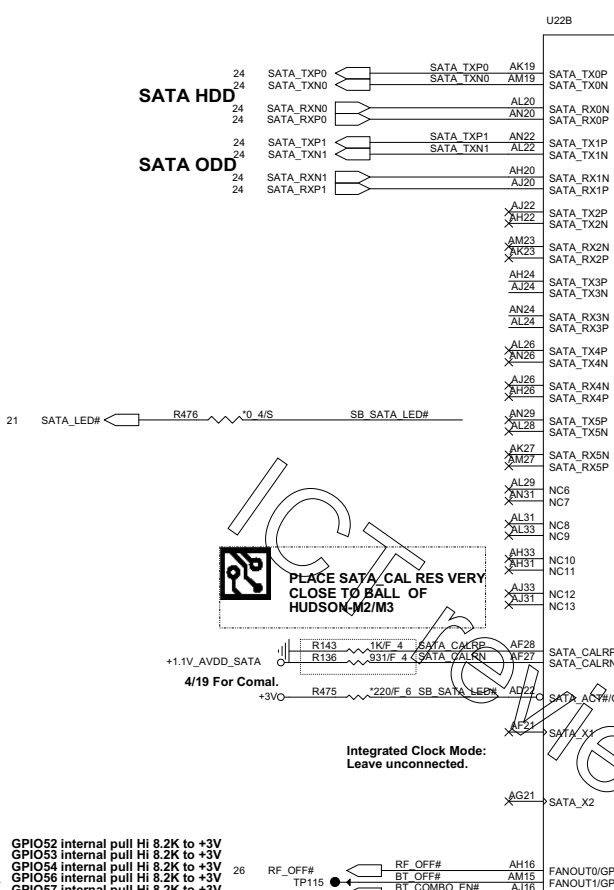
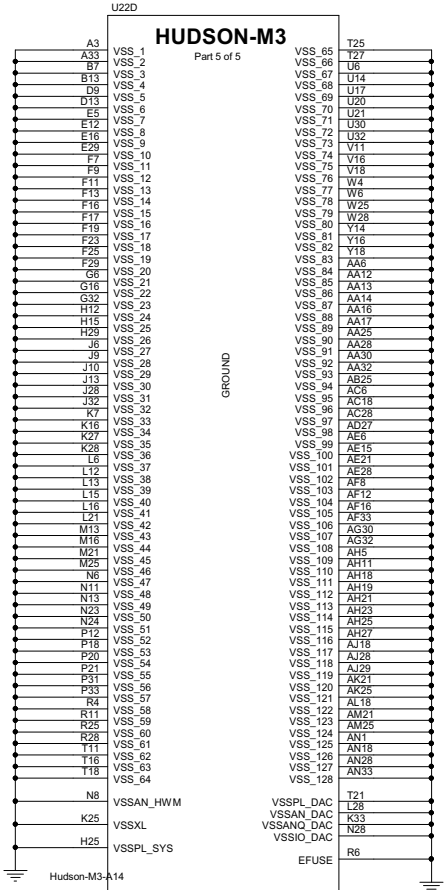
USB_SS_TX/RX0P/N	USB_HSD10P/N
USB_SS_TX/RX1P/N	USB_HSD11P/N
USB_SS_TX/RX2P/N	USB_HSD12P/N
USB_SS_TX/RX3P/N	USB_HSD13P/N

SCL3 of a TSI-capable APU's thermal bus. Pulled up to APU_VDDIO. Resistor value verified in the relevant APU design guide.

PROJECT : U92
 Quanta Computer Inc.

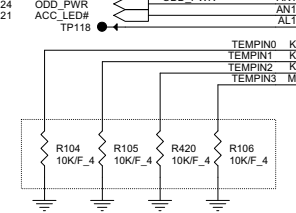
Size Custom Document Number Hudson-M3 GPIO/USB/AZ/RGMII Rev 1A
 Date: Wednesday, March 27, 2013 Sheet 6 of 37





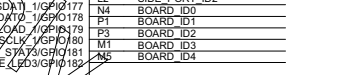
GPIOS2 internal pull Hi 8.2K to +3V
GPIOS3 internal pull Hi 8.2K to +3V
GPIOS4 internal pull Hi 8.2K to +3V
GPIOS5 internal pull Hi 8.2K to +3V
GPIOS7 internal pull Hi 8.2K to +3V
GPIOS8 internal pull Hi 8.2K to +3V

Integrated Clock Mode:
 Leave unconnected.

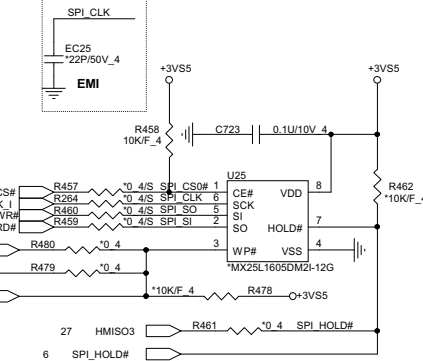
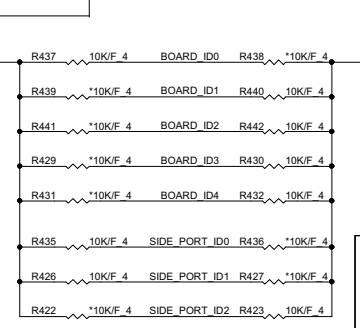


ID4	ID3	ID2	ID1	ID0	CONFIG	31- Level BOM	Item
0	0	0	0	0	UMA 14"		1
0	0	0	1	0	UMA 15"		2
0	0	1	0	0	eDP panel		3
0	0	1	1	0			4
0	1	0	1	0			5
1	0	0	1	0			6
1	0	0	1	0			7
1	0	1	1	0			8
0	0	0	0	1	SG / Muxless 14		9
0	0	0	1	1	SG / Muxless 15		10
1	0	0	1	1			11
1	0	1	1	1			12

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no support side port



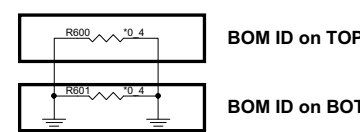
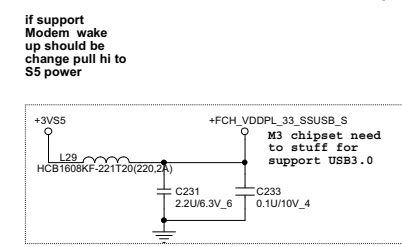
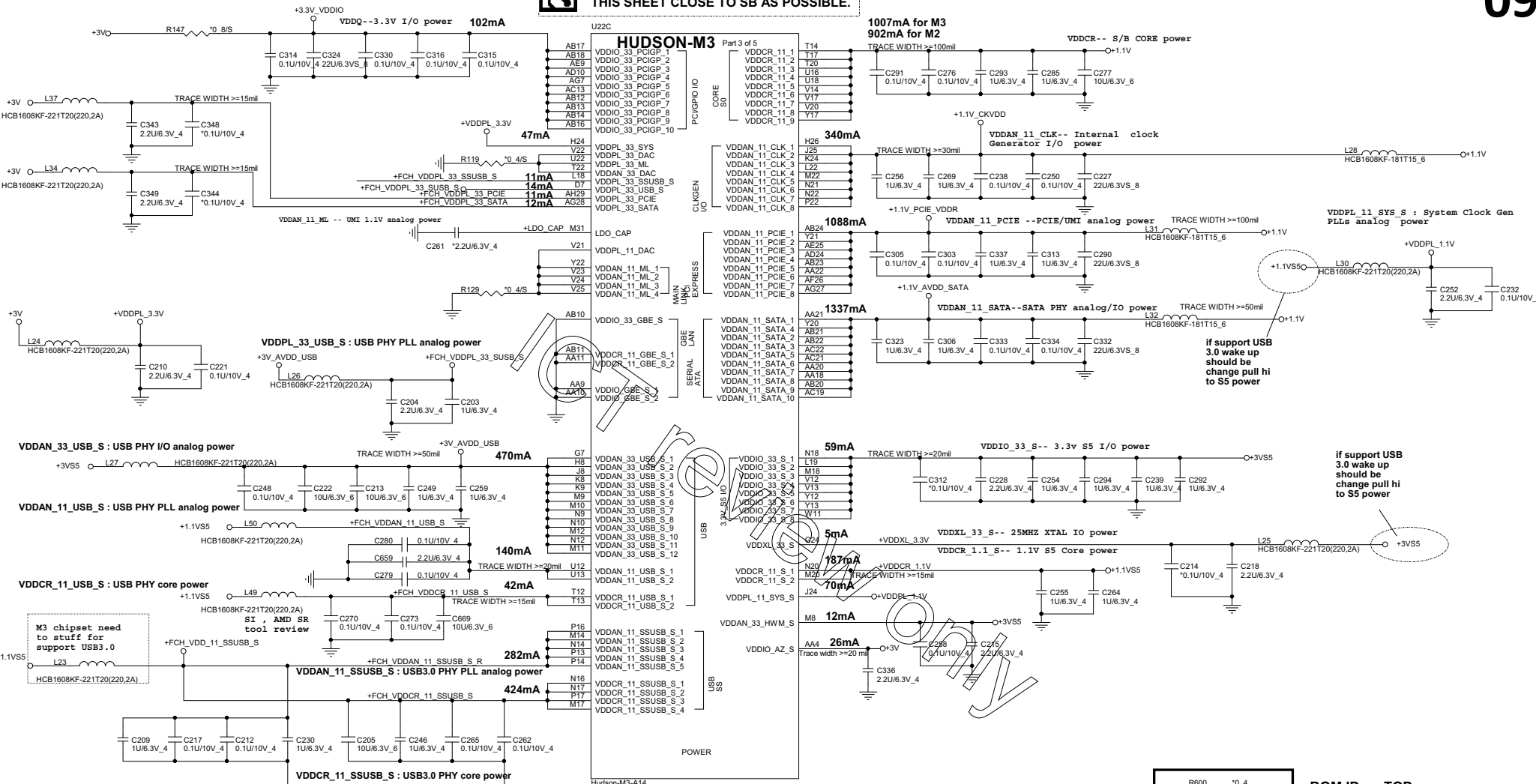
VIN (0 - 7)
 Voltage Monitor Not Implemented
 10-KΩ 5% pull-up to +3V5S
 or 10-KΩ 5% pull-down



PROJECT : U92
 Quanta Computer Inc.

Size Custom Document Number Hudson-M3 SATA/HWM/SPI Rev 1A
 Date: Wednesday, March 27, 2013 Sheet 8 of 37

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

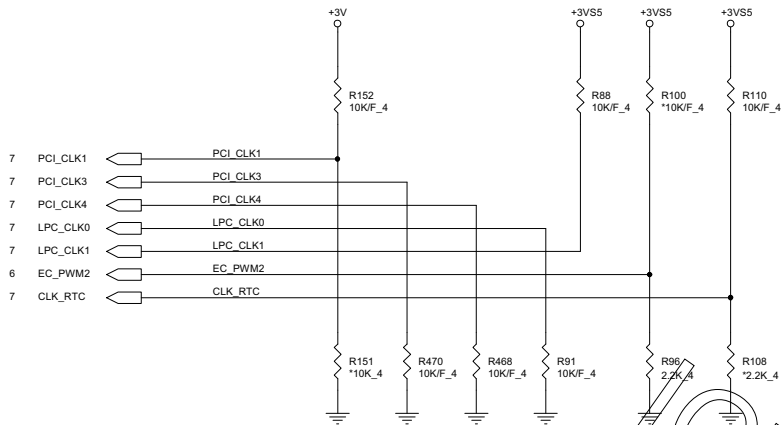


PROJECT : U92
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Hudson-M3 POWER/GND		
Date: Wednesday, March 27, 2013	Sheet 9	of 37

STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

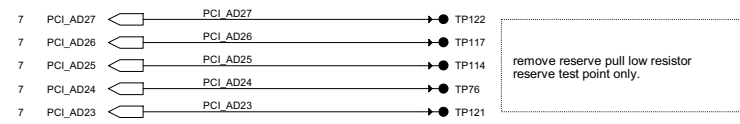


REQUIRED STRAPS

	-----	PCI_CLK1	-----	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	-----	ALLOW PCIe Gen2 DEFAULT	-----	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE ENABLED DEFAULT
PULL LOW	-----	FORCE PCIe Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE DISABLED

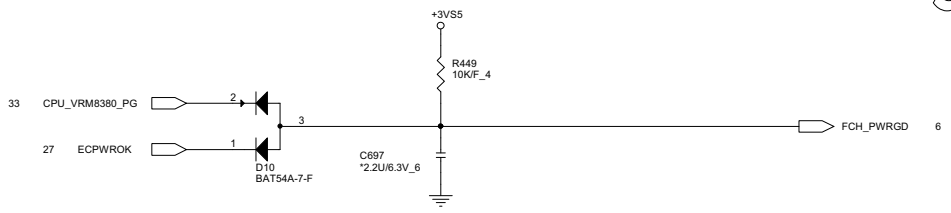
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



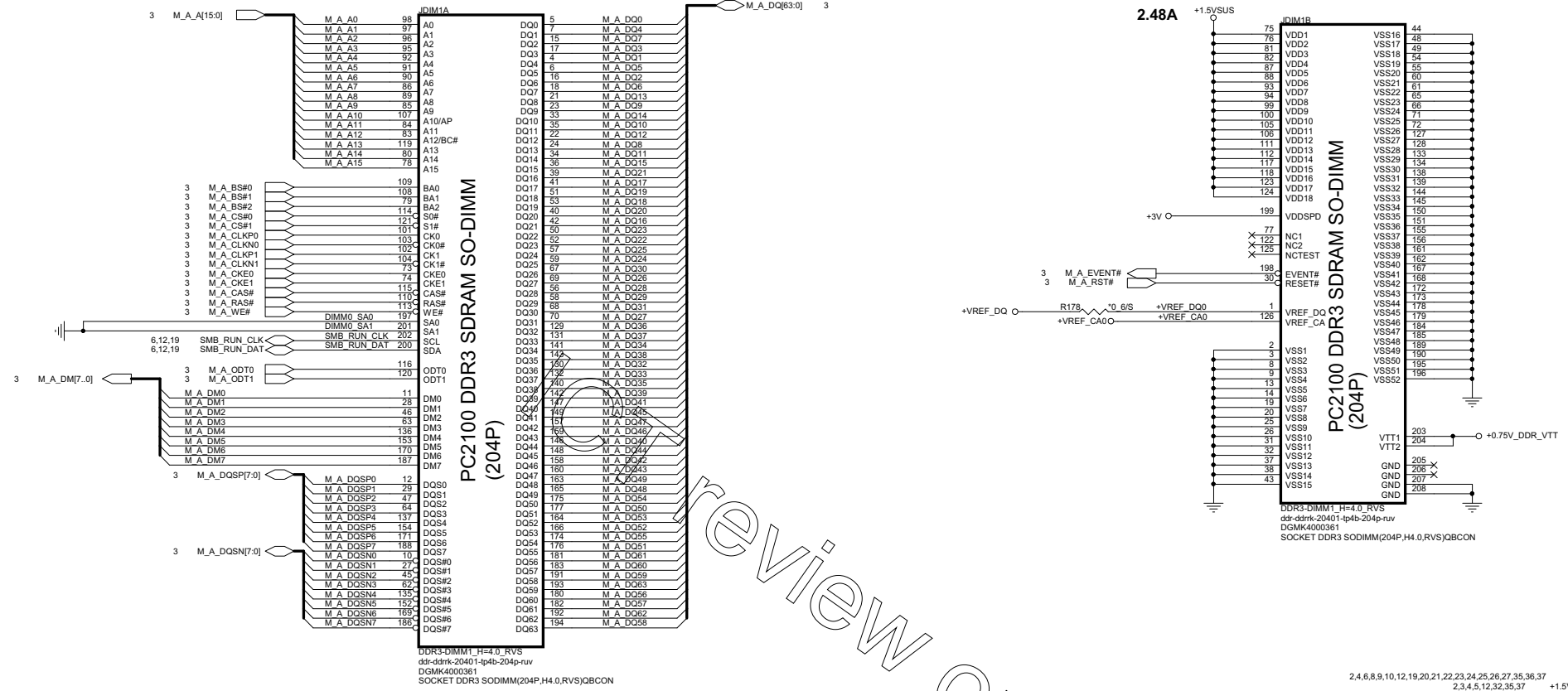
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

FCH PWRGD



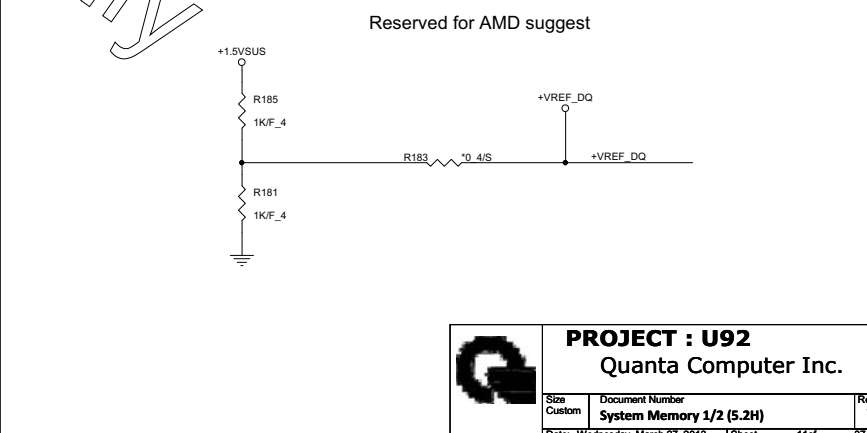
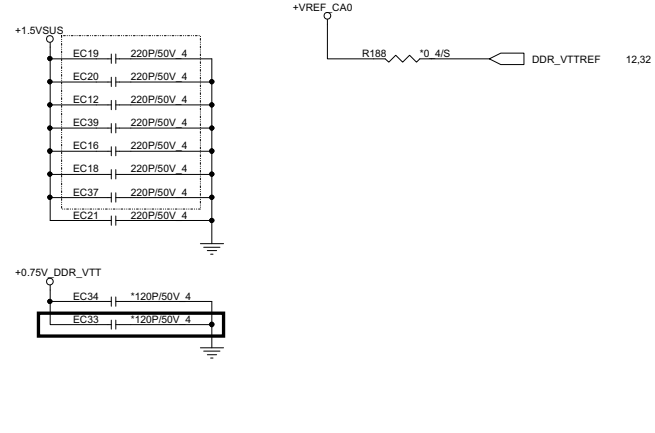
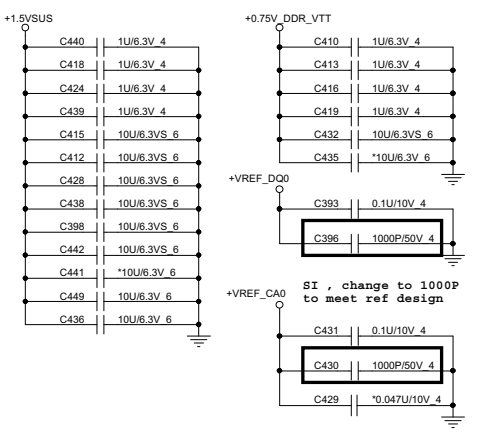
PROJECT : U92
Quanta Computer Inc.

Size Custom	Document Number Hudson-M3 STRAP/PWRGD	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 10 of 37		



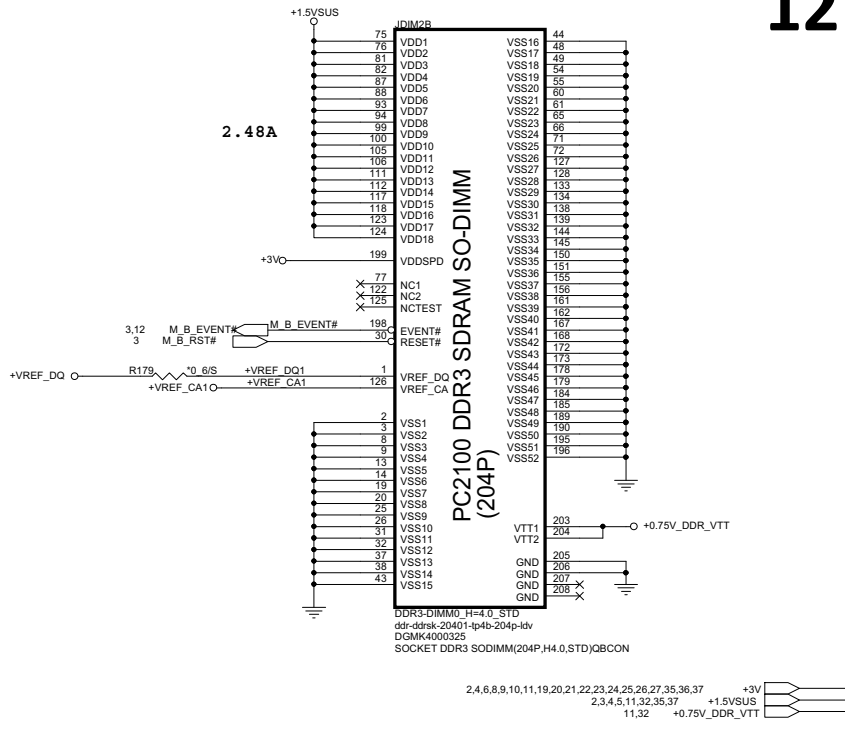
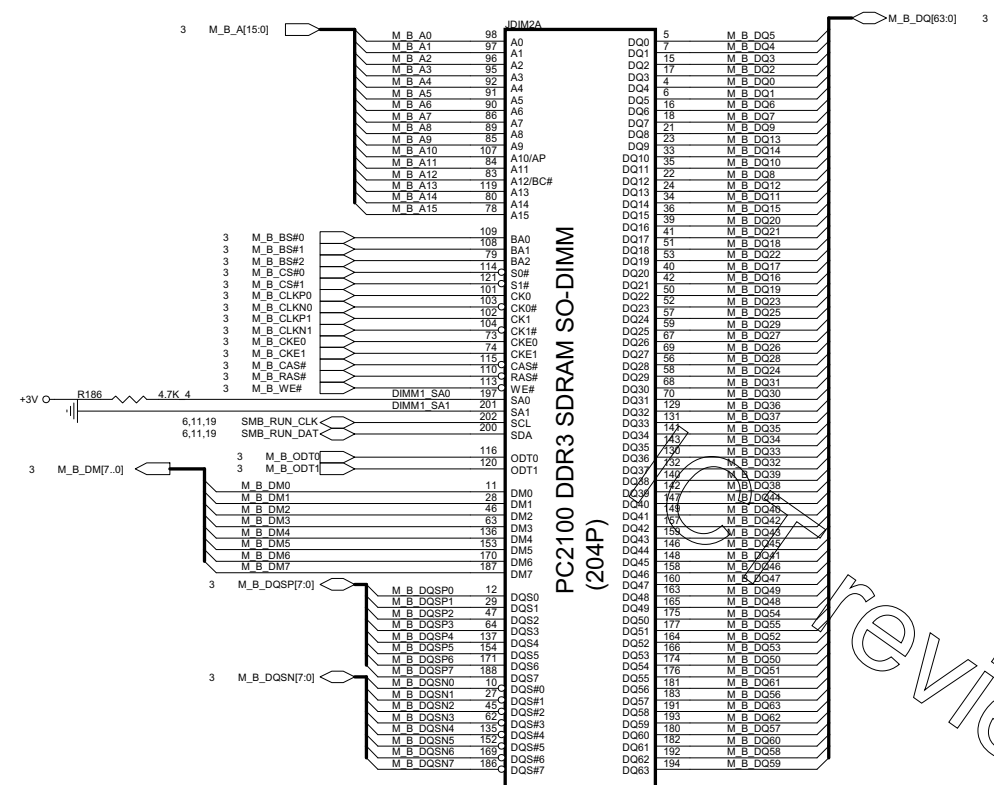
Review Only

Place these Caps near So-Dimm0.



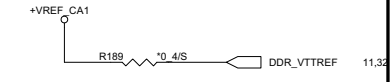
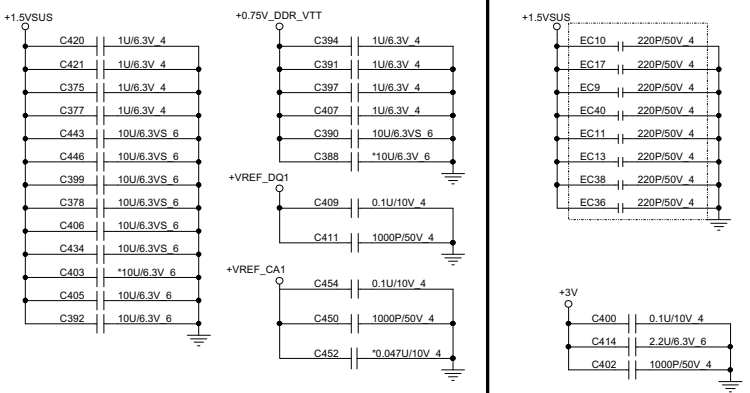
PROJECT : U92
Quanta Computer Inc.

Size Custom	Document Number System Memory 1/2 (5.2H)	Rev 1A
Date: Wednesday, March 27, 2013	Sheet 11 of	37

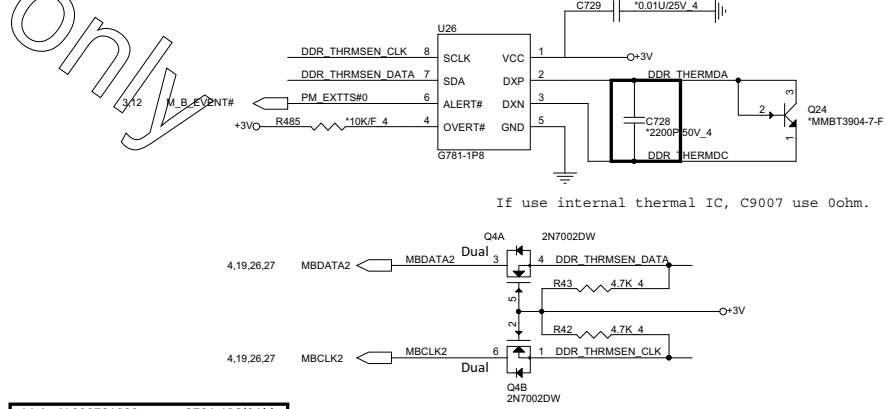


DDR3-DIMM0_H=4.0_STD
 ddr-ddrsk-20401-4b-204p-ldv
 DGMK4000325
 SOCKET DDR3 SODIMM(204P,H4.0,STD)QBCCN

Place these Caps near So-Dimm1.



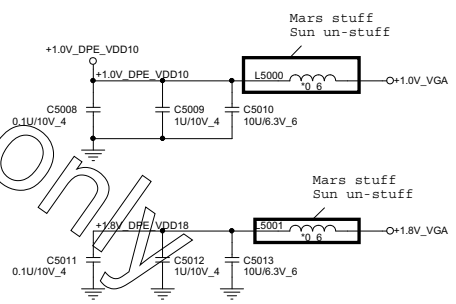
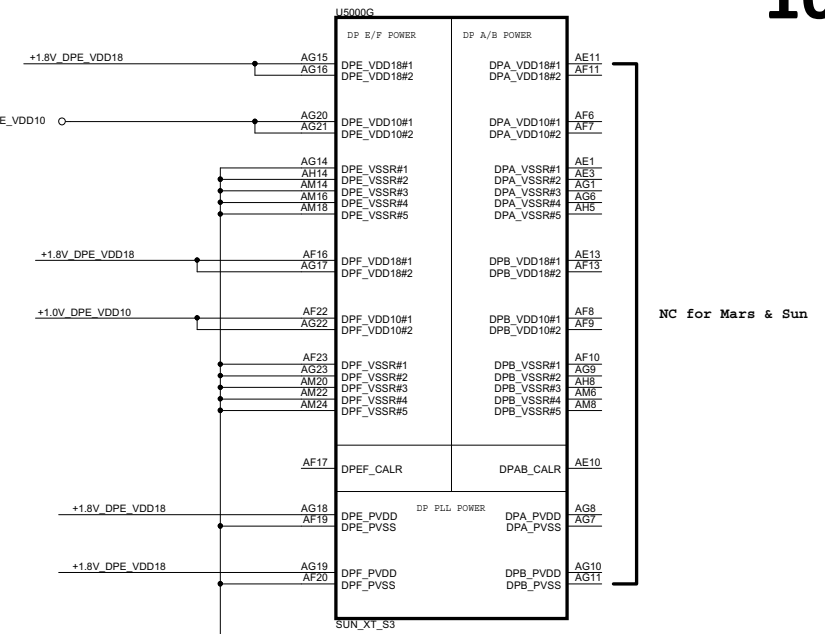
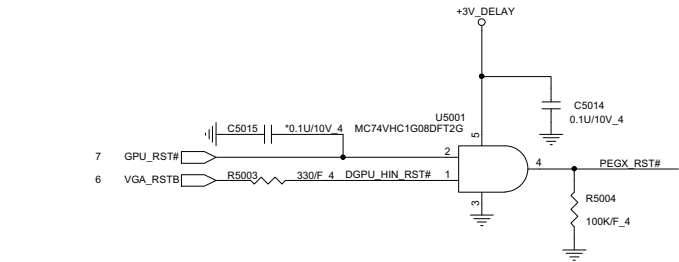
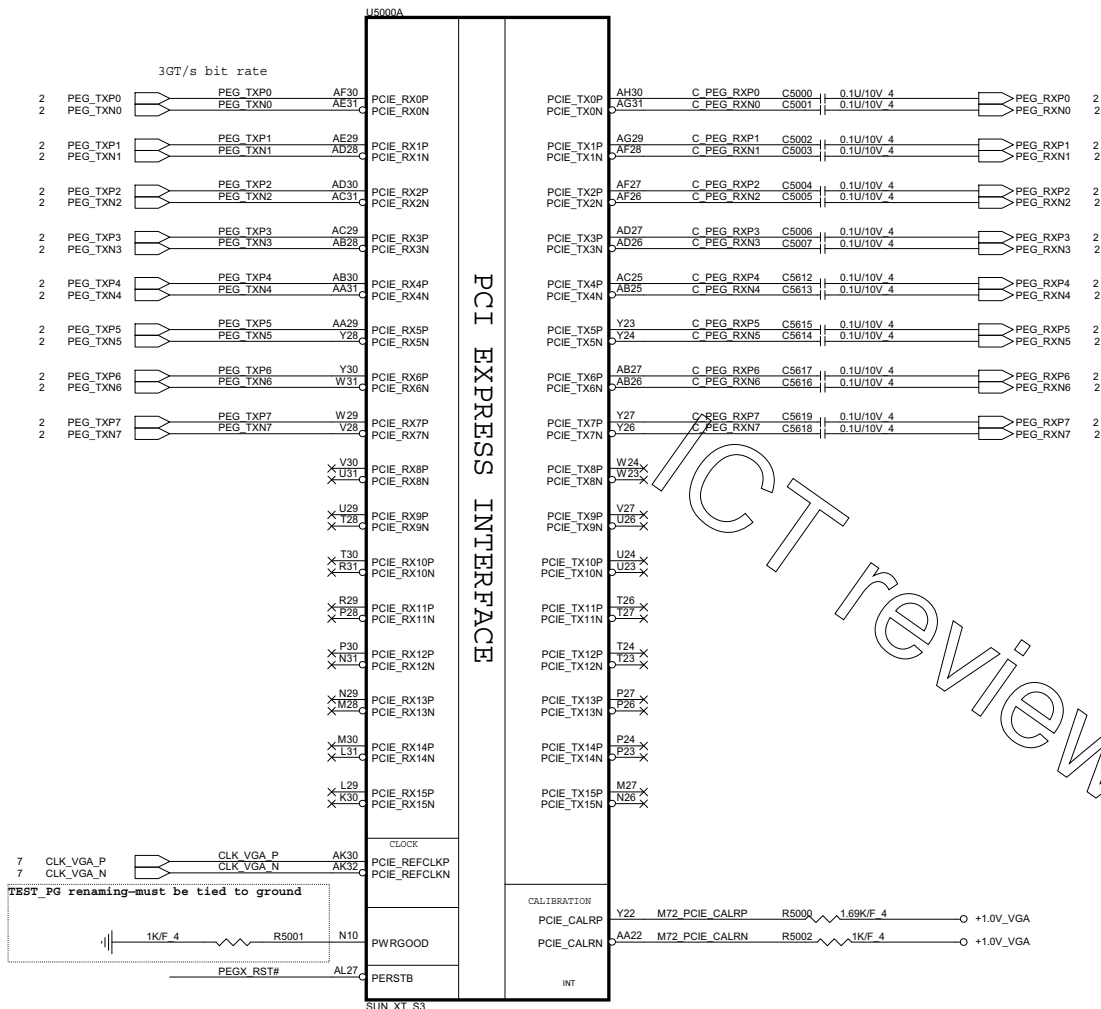
Local Thermal Sensor



- Main:AL000781039 G781-1P8(9Ah)
- 2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
- Main:AL001412003 EMC1412-1-ACZL-TR(98h)
- 2nd:AL000431014 TMP431ADGKR(98h)

PROJECT : U92
Quanta Computer Inc.

Size Custom Document Number System Memory 2/2 (9.2H) Rev 1A
 Date: Wednesday, March 27, 2013 Sheet 12 of 37



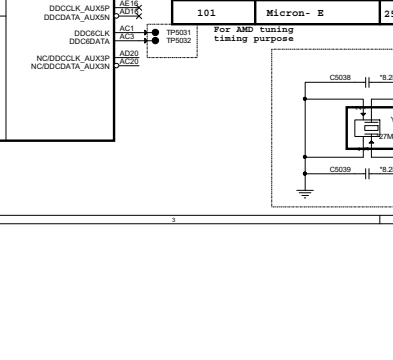
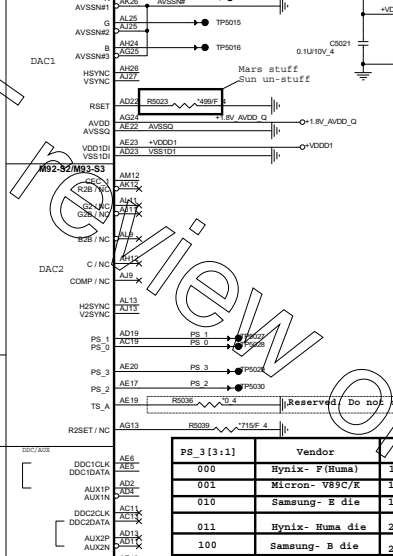
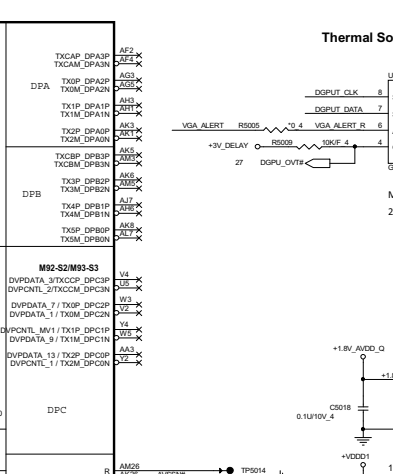
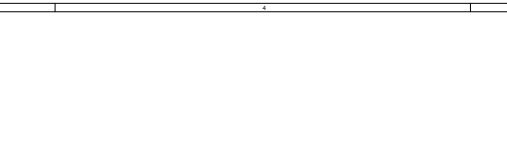
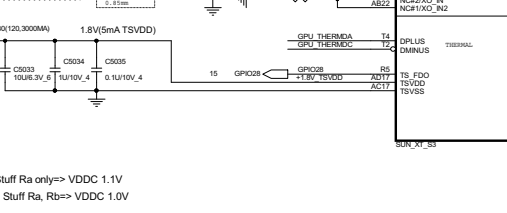
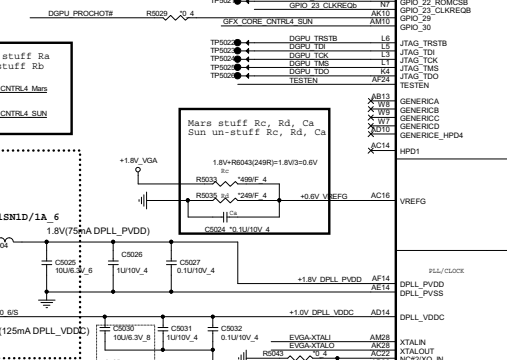
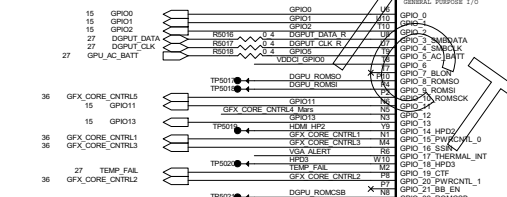
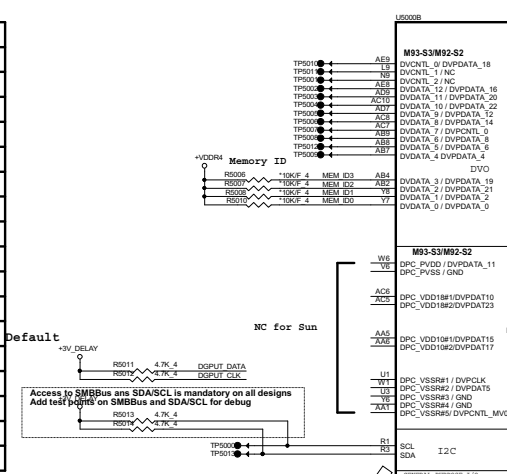
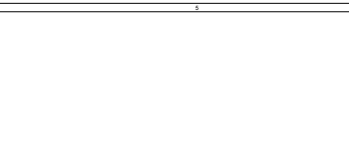
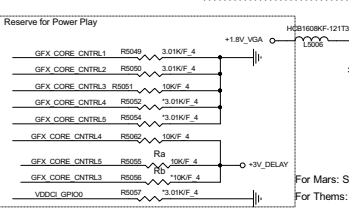
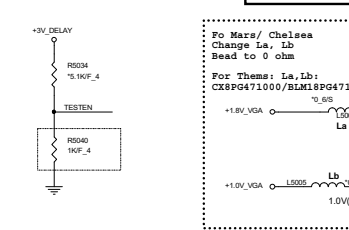
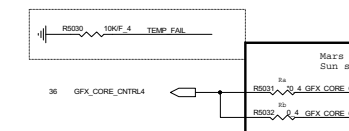
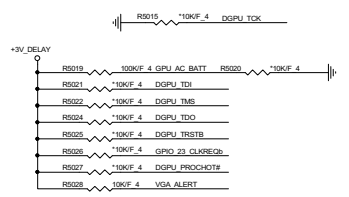
NC for Mars & Sun

+1.0V_VGA 14.16.37
+1.8V_VGA 14.16.26.37

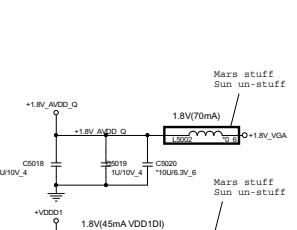
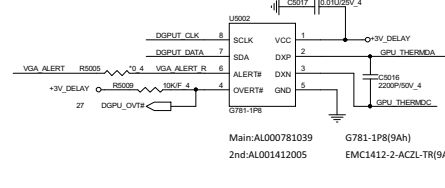
PROJECT : U92
Quanta Computer Inc.

Size Custom	Document Number Sun S3 PCIe_Interface	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 13 of 37		

GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun S3	V-CORE
0	1	1	0	1	1	1.175V
0	1	1	1	0	1	1.150V
0	1	1	1	1	1	1.125V
1	0	0	0	0	1	1.100V
1	0	0	0	1	1	1.075V
1	0	0	1	0	1	1.050V
1	0	0	1	1	1	1.025V
1	0	1	0	0	1	1.000V
1	0	1	0	1	1	0.975V
1	0	1	1	0	1	0.950V
1	0	1	1	1	1	0.925V
1	1	0	0	0	1	0.900V
1	1	0	0	1	1	0.875V
1	1	0	1	0	1	0.850V
1	1	0	1	1	1	0.825V
1	1	1	0	0	1	0.800V
1	1	1	0	1	1	0.775V



Thermal Solution(Close to GPU)

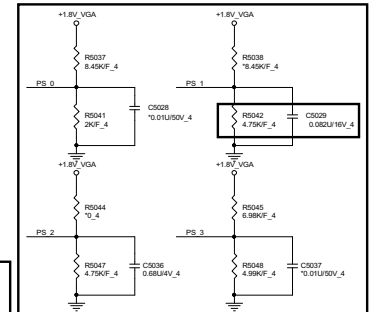
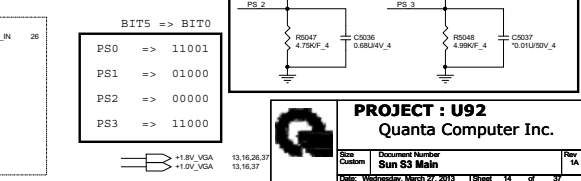
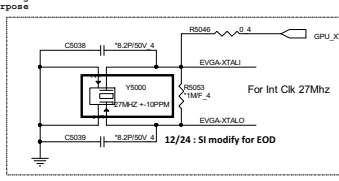


- MIPS Implementation**
- Connect GPIO_28 to 10K pulldown to enable MIPS
 - If any of PS_0[3:2] is not used, leave "no connect"
 - R_pu, R_pd and C must be properly populated per tables below
 - Place MIPS circuit components as close to the ASIC as possible
 - Total DC resistance of trace between PS pin and ground should be less than 2 ohms
 - Total DC resistance of trace between C and ground should be less than 2 ohms
 - Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table		Resistor Divider Lookup Table	
C (pF)	Bits(3,4)	R_pu (Ohm)	R_pd (Ohm)
680	00	NC	4750
82	01	8450	2000
10	10	4530	2000
NC	11	6960	4900
		4530	4950
		3340	5620
		3400	10000
		4750	NC

PS_0[3:1]	romidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidfg[2:0] define memory aperture size If bios_rom_en = 1, romidfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved		genk_vsync
PS_1[1]	bf_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bf_clk_pm_en	PCIe CLK PM capability: 1=CLKREQ supported	x	gpio_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwm_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dbl	VGA double: 1=Double the GPU as the system's VGA controller	0	gpio_5
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_3[5]	aud_port_cp[0]			

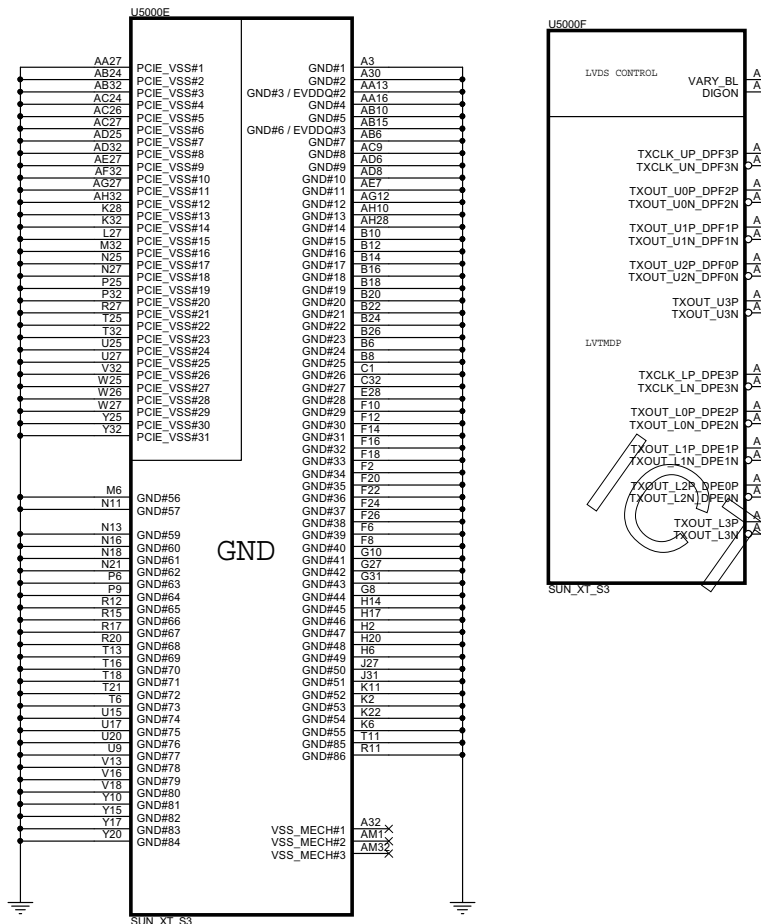
PS_3[3:1]	Vendor	Temp	Vendor P/N	R5045	R5048
000	Hynix - F (Huma)	128Mx16 #4, 900Mhz	H5TC3G63FPR-11C	NC	4.75K
001	Micron - V8C/R	128Mx16 #4, 910Mhz	MT41J128M163E-0930:E	8.45K	2K
010	Samsung - E die	128Mx16 #4, 900Mhz	K4W2G1646E-BC1A	4.53K	2K
011	Hynix - Huma die	256Mx16 #4, 900Mhz	H5TC4G63FAFR-11C	6.98K	4.99K
100	Samsung - B die	256Mx16 #4, 900Mhz	K4W4G1646E-BC1A	4.53K	4.99K
101	Micron - E	256Mx16 #4, 900Mhz	MT41J256M16RA-0930:E	3.24K	5.62K



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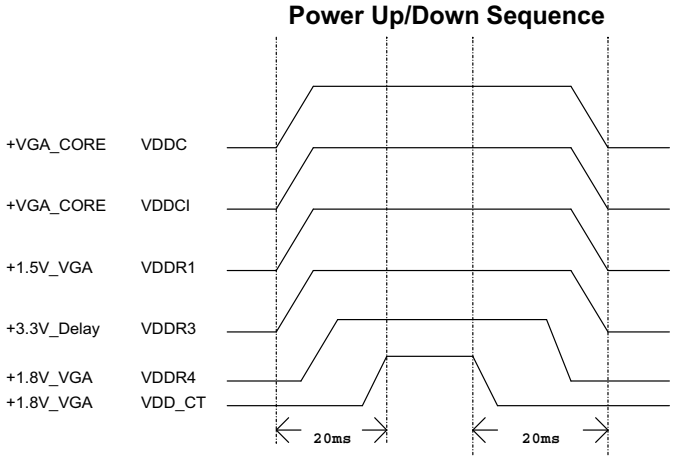


CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYSN	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

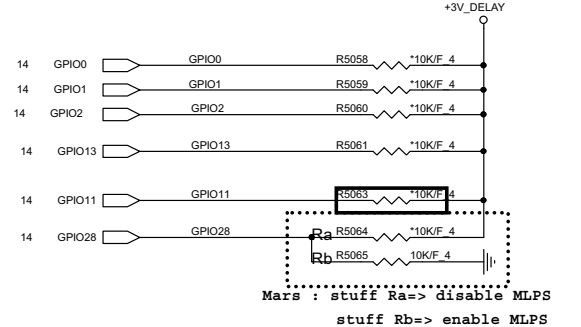
GPIO21	H2SYNC	GENERICC	GPIO8	GPIO2
--------	--------	----------	-------	-------



Memory Aperture size(Seymour)

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	1
0	2G	1	0
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

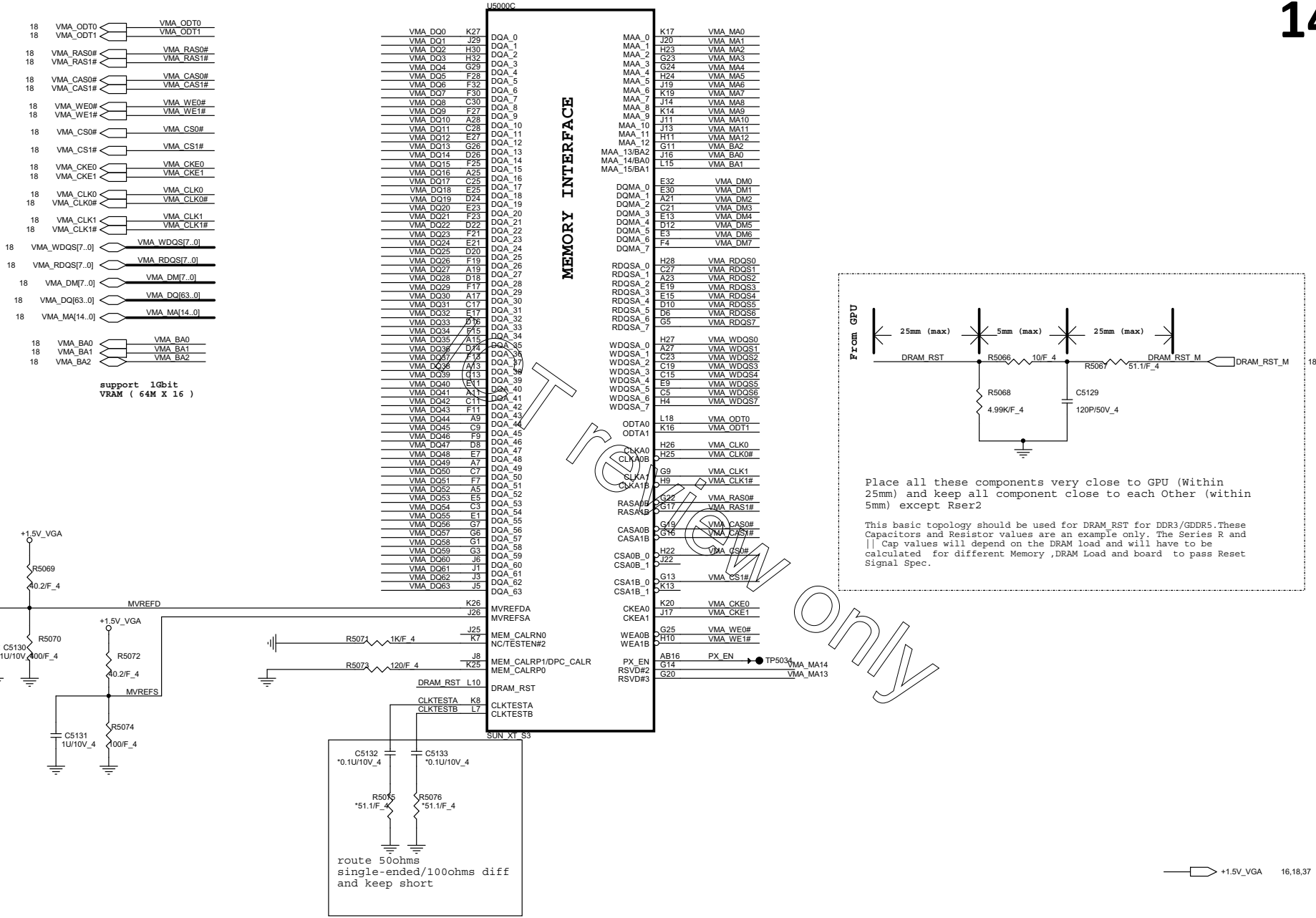


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Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
Date: Wednesday, March 27, 2013	Sheet 15 of 37	

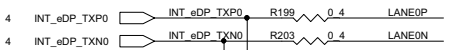
review only

MEMORY INTERFACE



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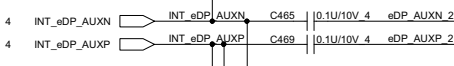
Size Custom	Document Number Sun S3 MEM Interface	Rev 1A
Date: Wednesday, March 27, 2013	Sheet 17 of 37	



To LVDS Converter



To eDP

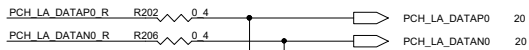


To LVDS Converter

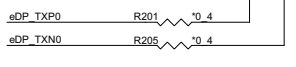


To eDP

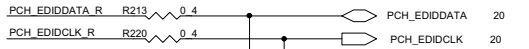
From LVDS Converter



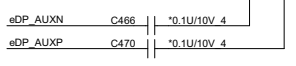
From APU



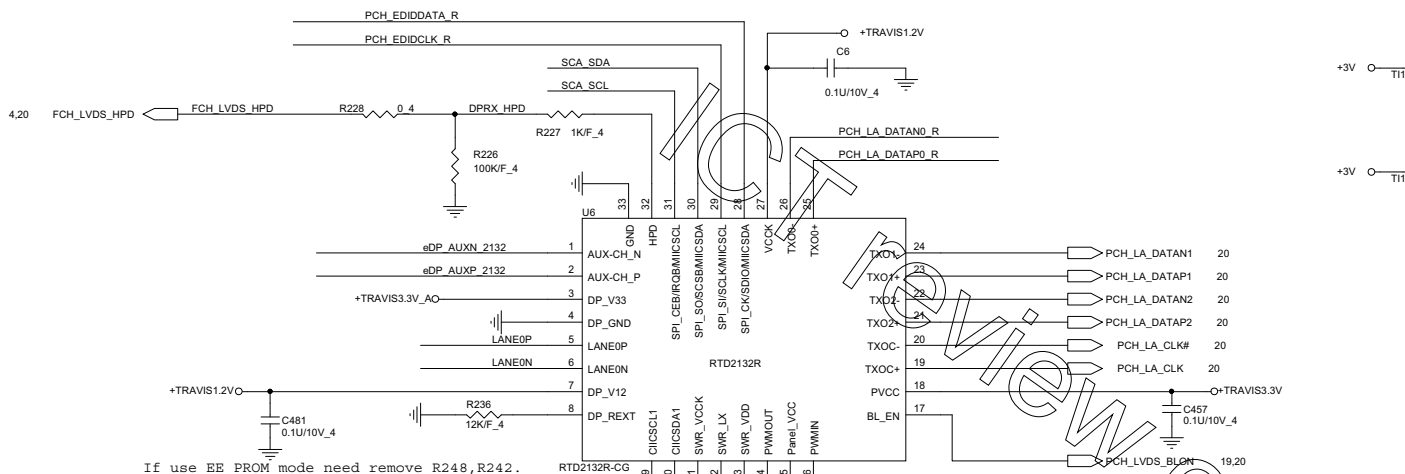
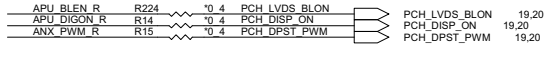
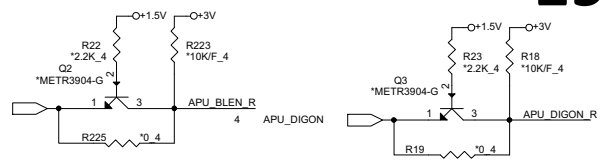
From LVDS Converter



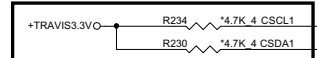
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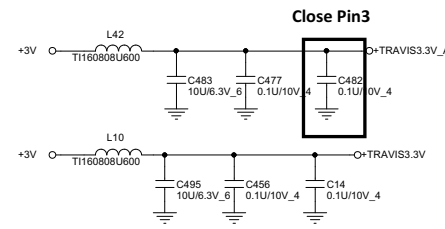
From APU



If use EE PROM mode need remove R248, R242.

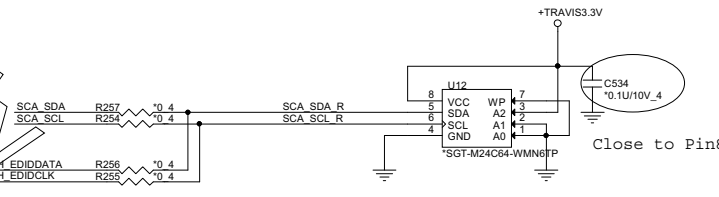


EE PROM R304, R308
EC OPTION R307, R305



Close Pin3

Address=0xA8



Close to Pin8

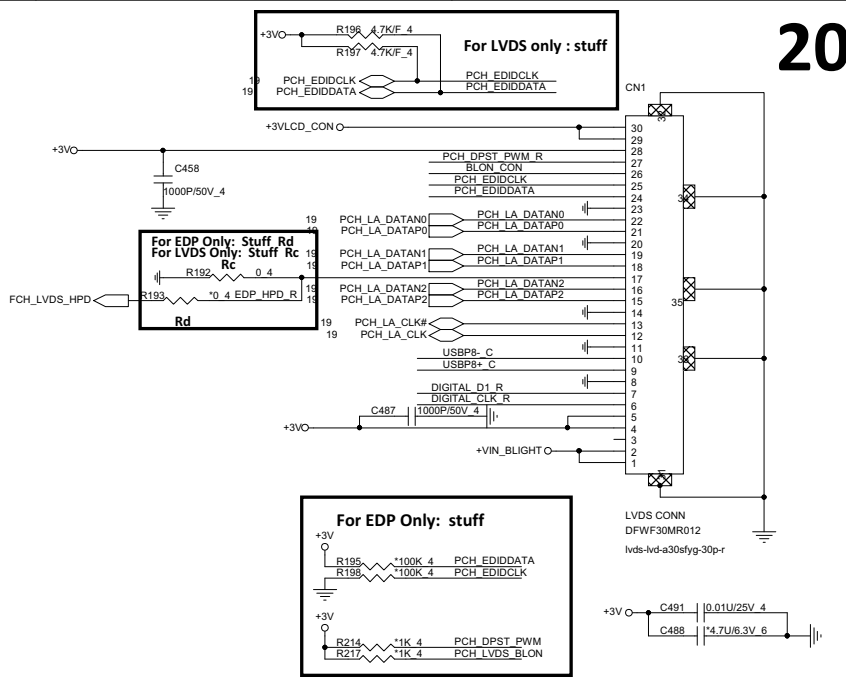
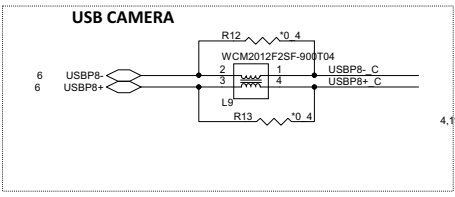
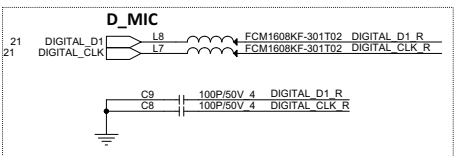
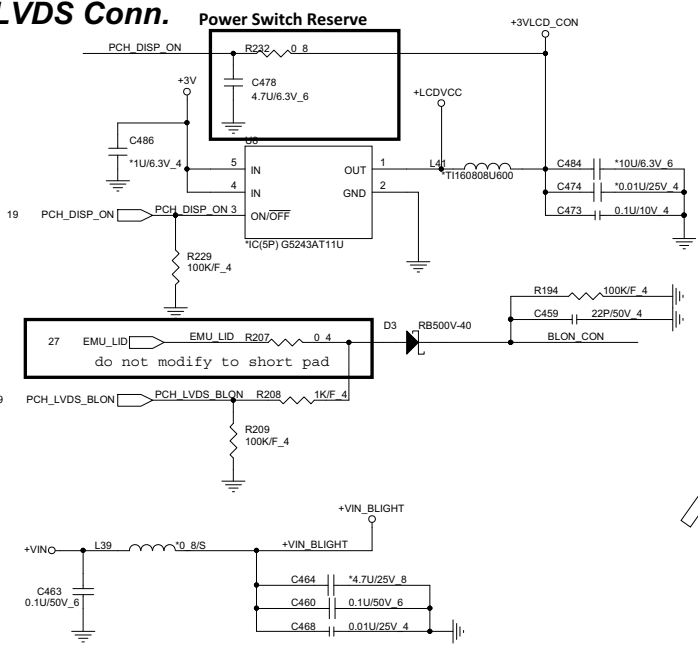
		MODE_CFG0(PIN30)	
		0	1
MODE_CFG1(PIN31)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



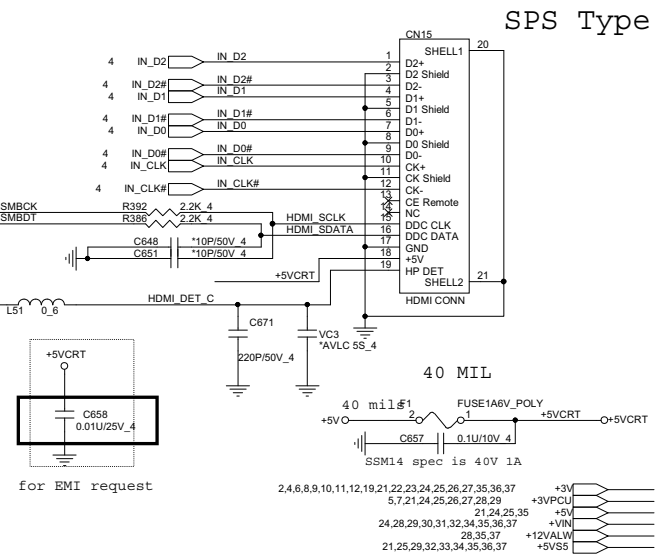
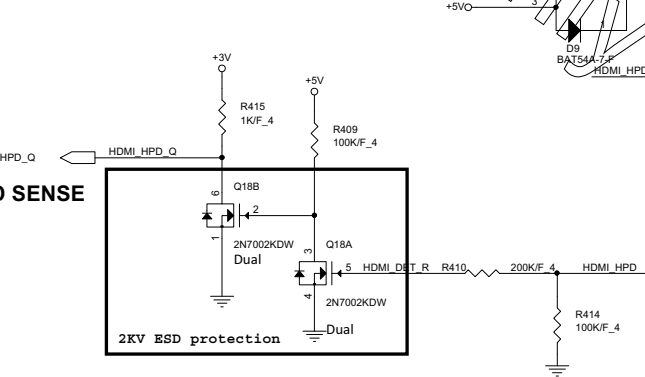
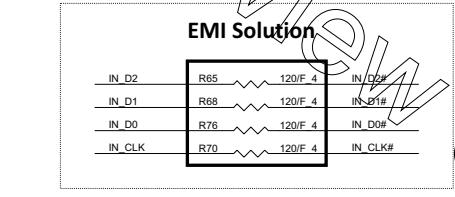
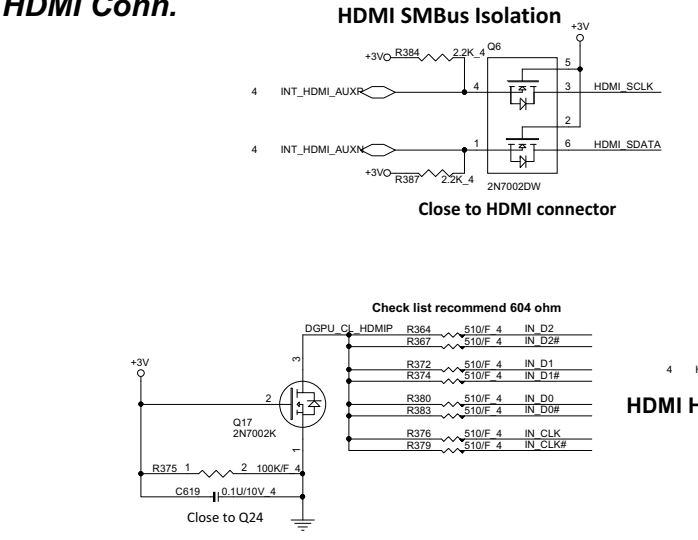
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Quanta Computer Inc.

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LVDS Conn.



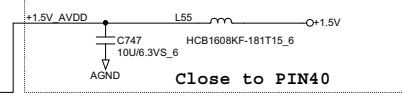
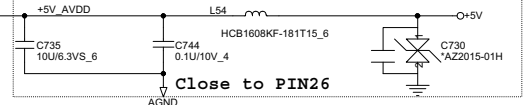
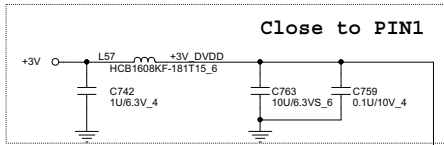
HDMI Conn.



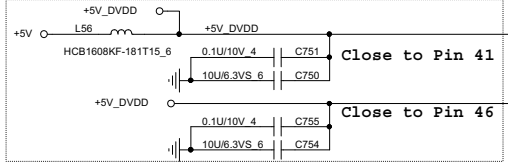
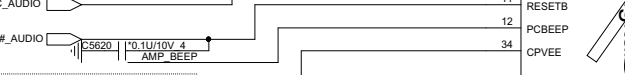
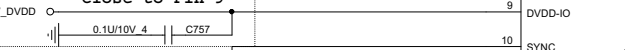
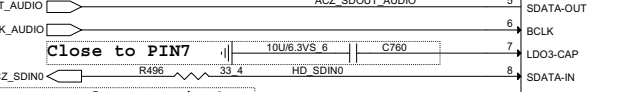
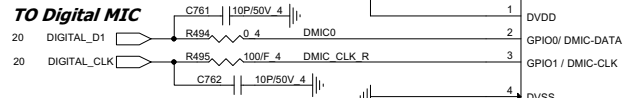
SPS Type

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Size Custom	Document Number	Rev 1A
LCD Connector (LVDS)		
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20.24,25.35
2.4,6.8,9,10,11,12,19,20,22,23,24,25,26,27,35,36,37
2.4,19,26,33,35



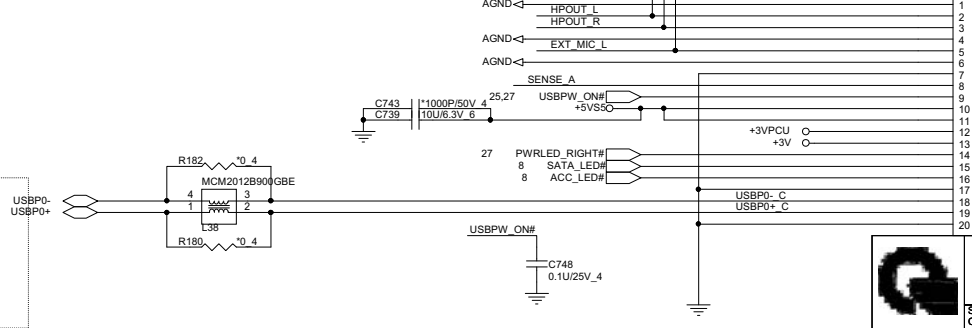
Analog

Digital

Check layout
mount location

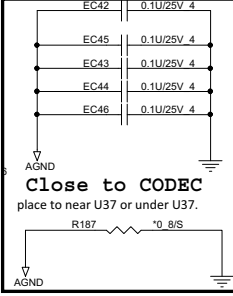
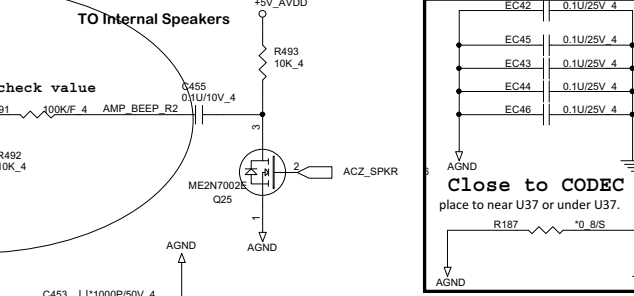
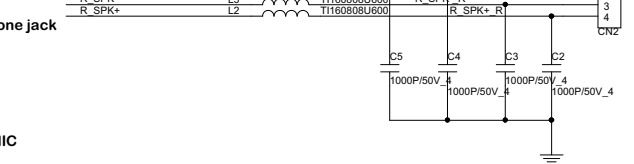
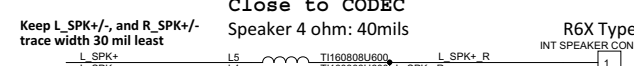
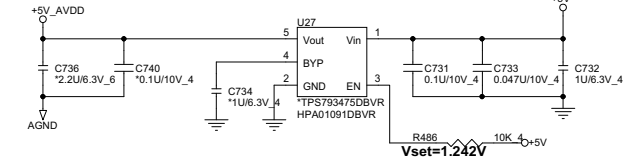
Close to codec

USB 2.0 AND AUDIO COMBO JACK



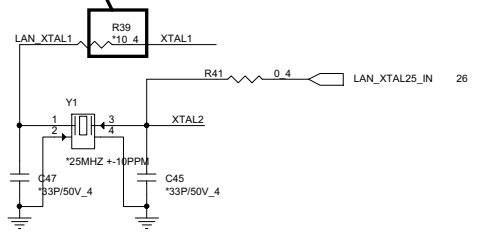
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BIT_CLK_AUDIO	EC14	*33P/50V 4	
ACZ_SDOOUT_AUDIO	EC35	*10P/50V 4	
ACZ_SYNC_AUDIO	EC15	*10P/50V 4	

FOR EMI

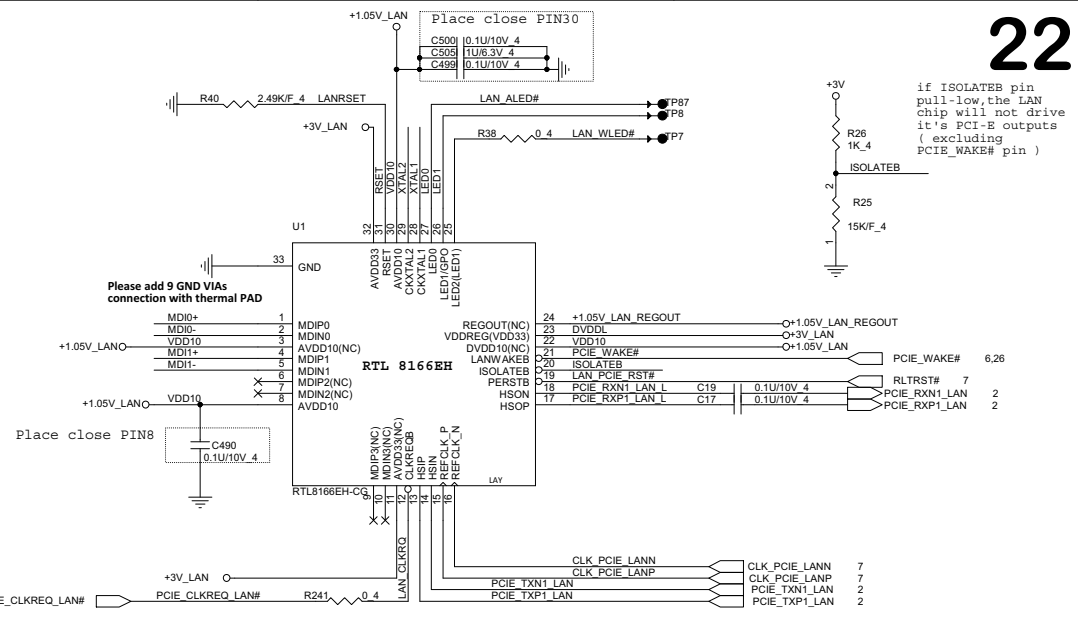
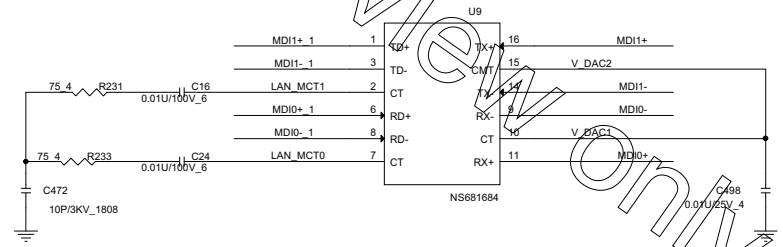
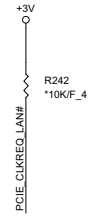
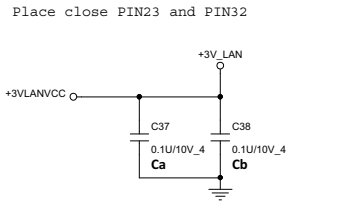
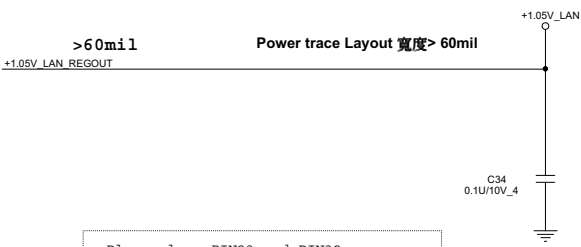


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Quanta Computer Inc.

For EMI 0 ~ 22 ohm

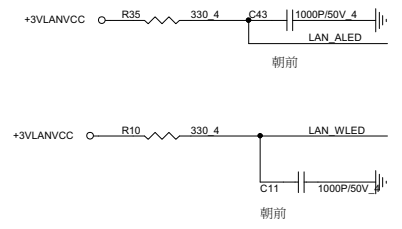
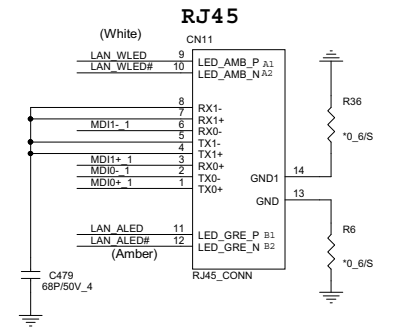


>60mil Power trace Layout 宽度 >60mil



if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

LAN conn TWD Type



2,4,6,8,9,10,11,12,19,20,21,23,24,25,26,27,35,36,37, 26,35



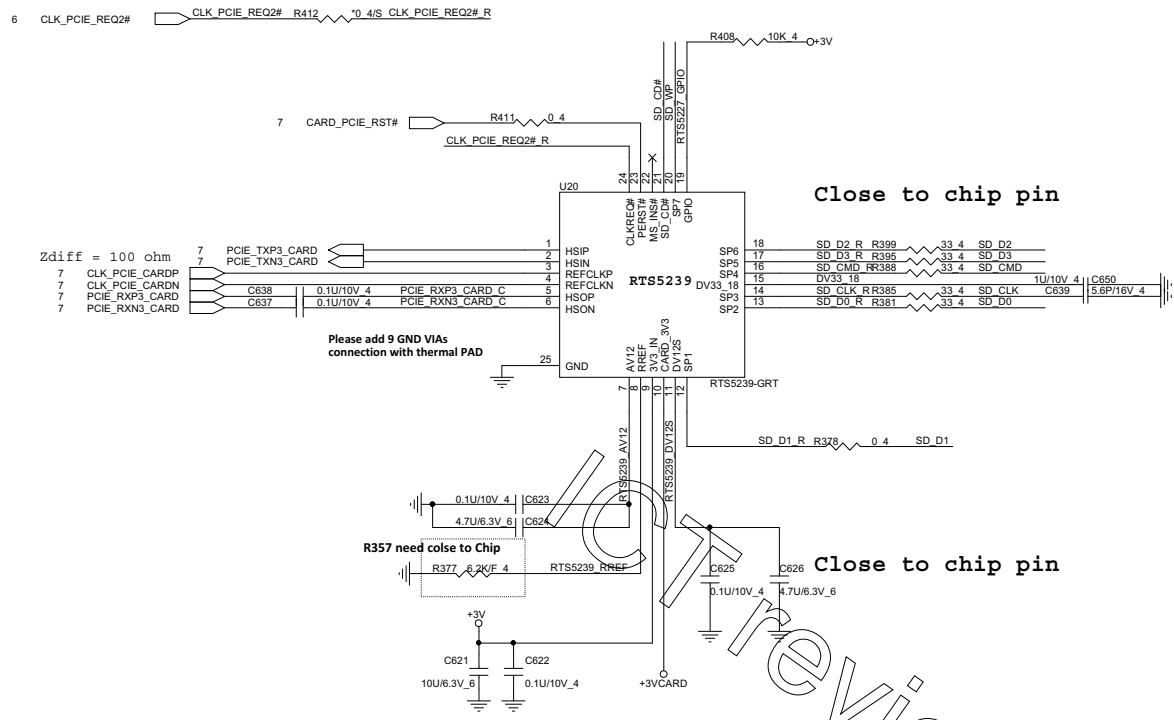
PROJECT : U92
Quanta Computer Inc.

Size Custom Document Number
RTL 8166EH/RJ45 Rev 1A

Date: Wednesday, March 27, 2013 Sheet 22 of 37

SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin

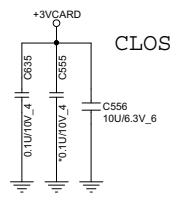


Close to chip pin

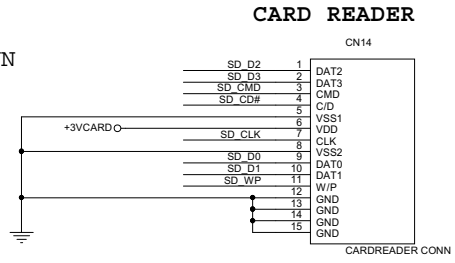
Close to chip pin

Reserve for EMI

SD D0	EC30	5.6P/16V 4
SD D1	EC29	5.6P/16V 4
SD D2	EC32	5.6P/16V 4
SD D3	EC31	5.6P/16V 4



CLOSE CONN



CARD READER

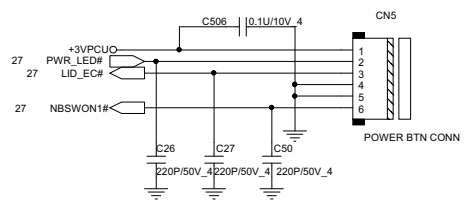
R3X Type

PROJECT : U92
Quanta Computer Inc.

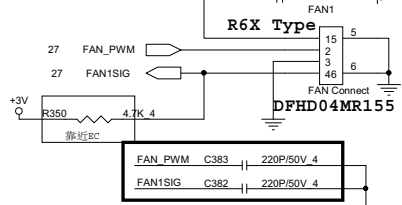
Size Custom	Document Number RTS5239 & CR SOCKET	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 23 of 37		

Power Button Connector

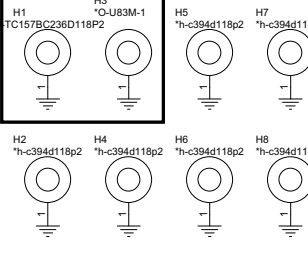
Pin1: +3VPCU(LIDSWITCH PWR)
 Pin2: POWER LED
 Pin3: LIDSWITCH
 Pin4: GND
 Pin5: GND
 Pin6: POWERON#



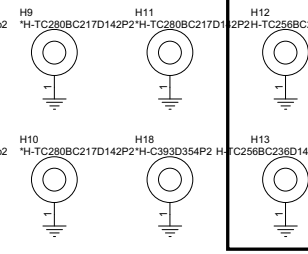
CPU FAN



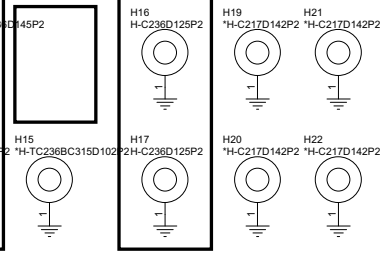
HoleSI change footprint



SI change FAN NUT P/N



SI Del WLAN NUT

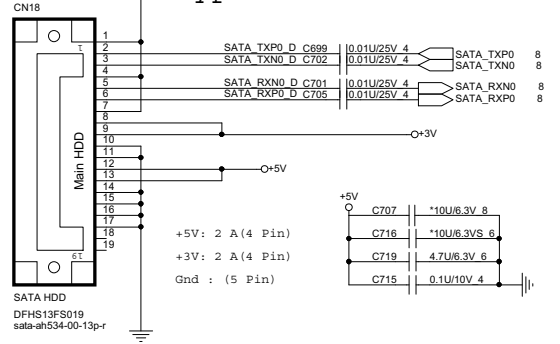


FAN NUT

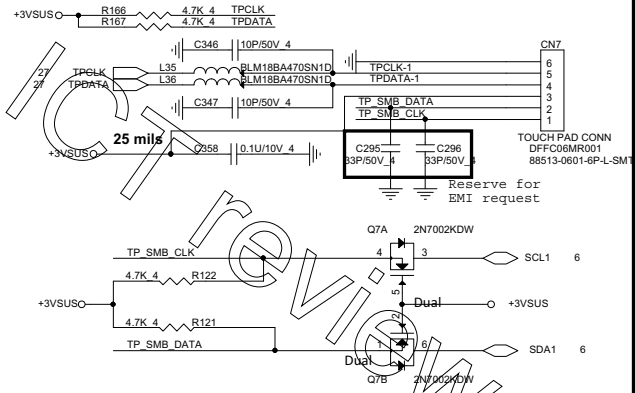
PCH NUT

SATA HDD Connector(Cable type)

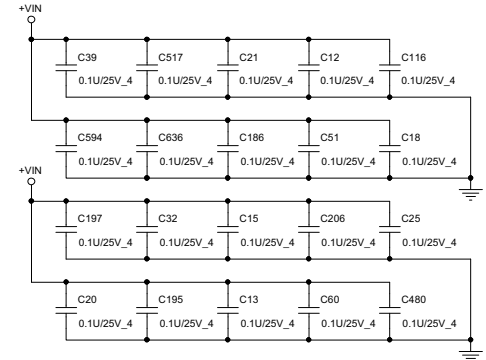
Bypass CAP close conn



Touch Pad



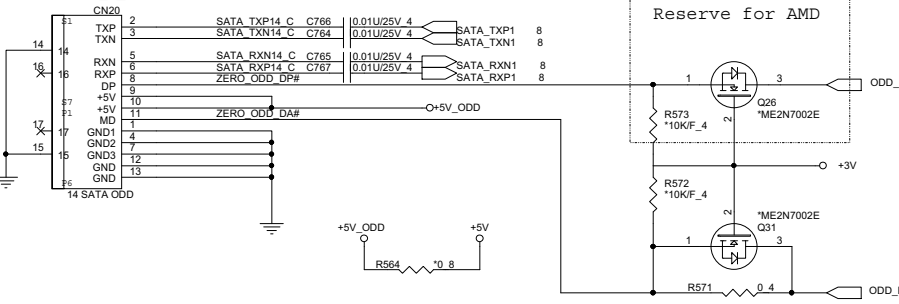
+VIN Cap



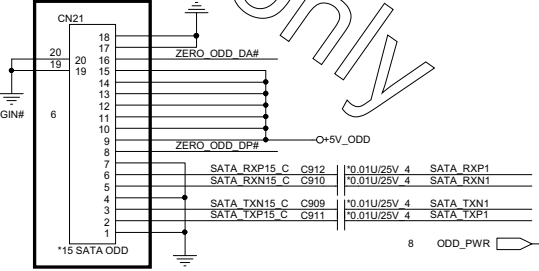
SATA ODD CONNECTOR

NEW Type

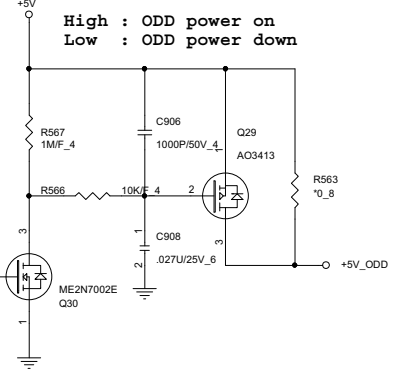
Bypass CAP close conn



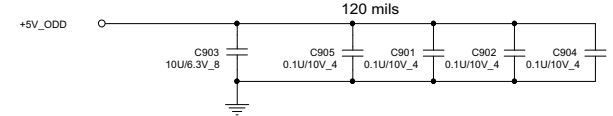
New Type



SI Change Footprint



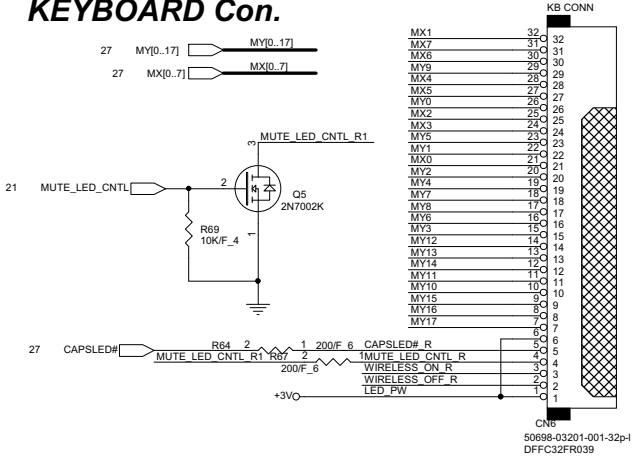
High : ODD power on
 Low : ODD power down



PROJECT : U92
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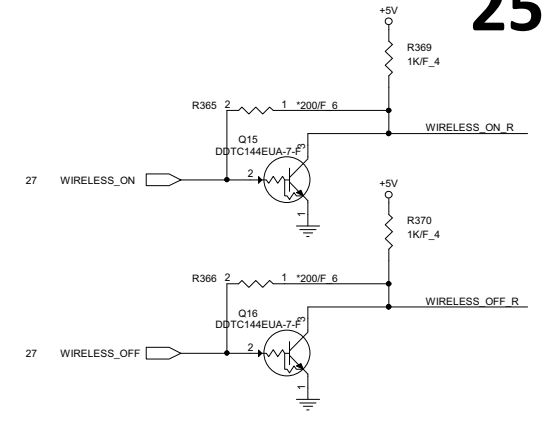
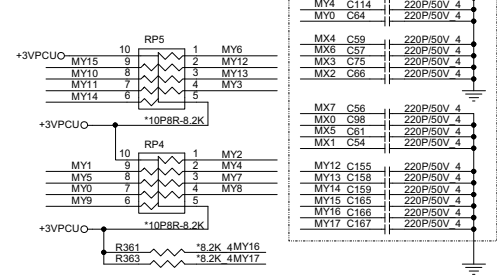
Size: Custom	Document Number: SATA HDD/ODD/MSATA CONN	Rev: 1A
Date: Wednesday, March 27, 2013	Sheet: 24of	37

KEYBOARD Con.

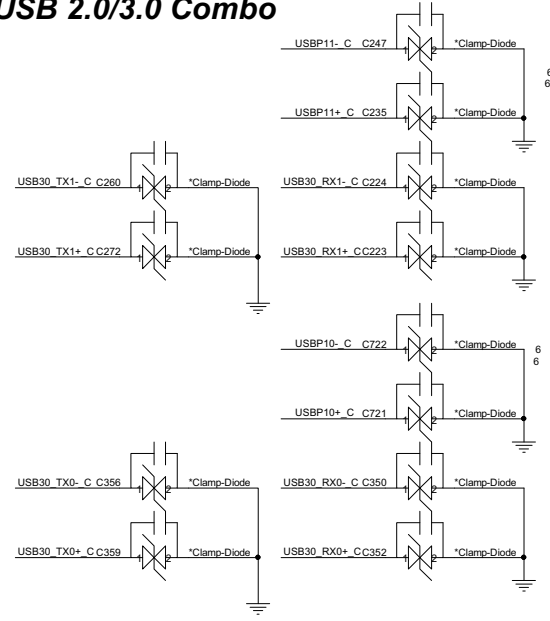


R6X Type

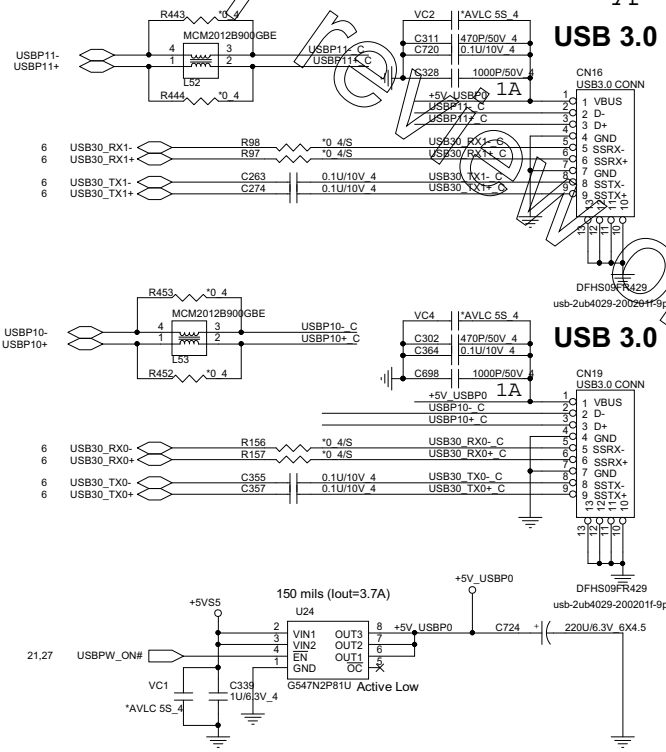
KEYBOARD PULL-UP



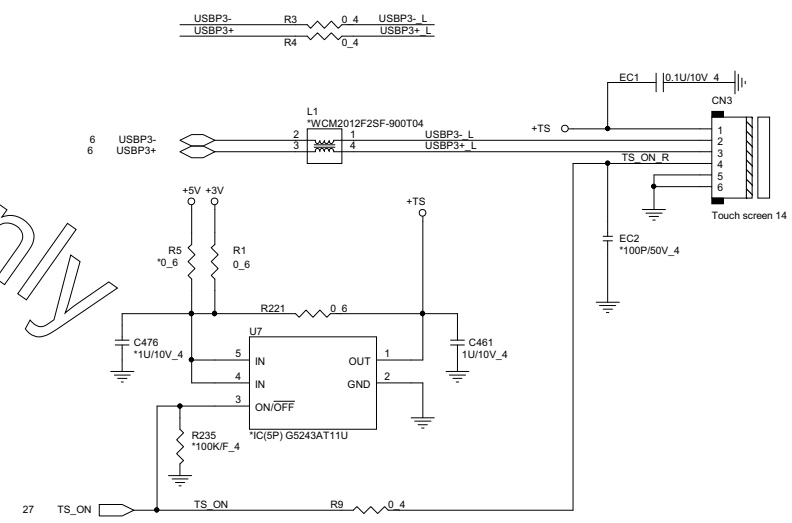
USB 2.0/3.0 Combo



SPS Type



Touch screen



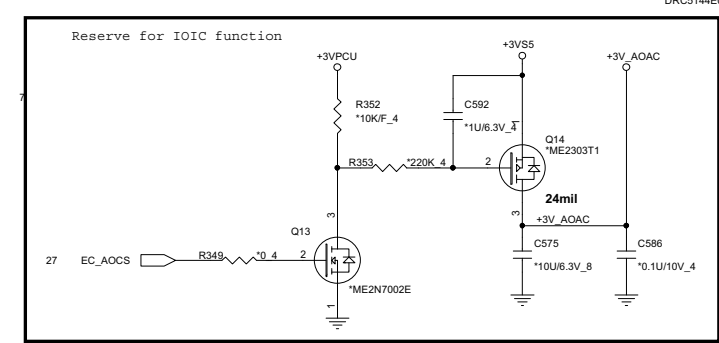
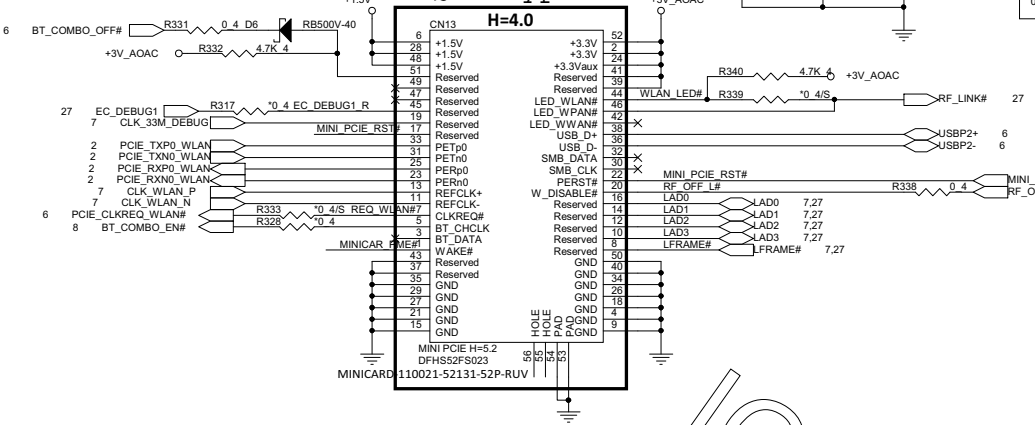
PROJECT : U92
Quanta Computer Inc.

Size Custom Document Number **USB 3.0/KB/Green CLK** Rev 1A
Date: Wednesday, March 27, 2013 Sheet 25 of 37

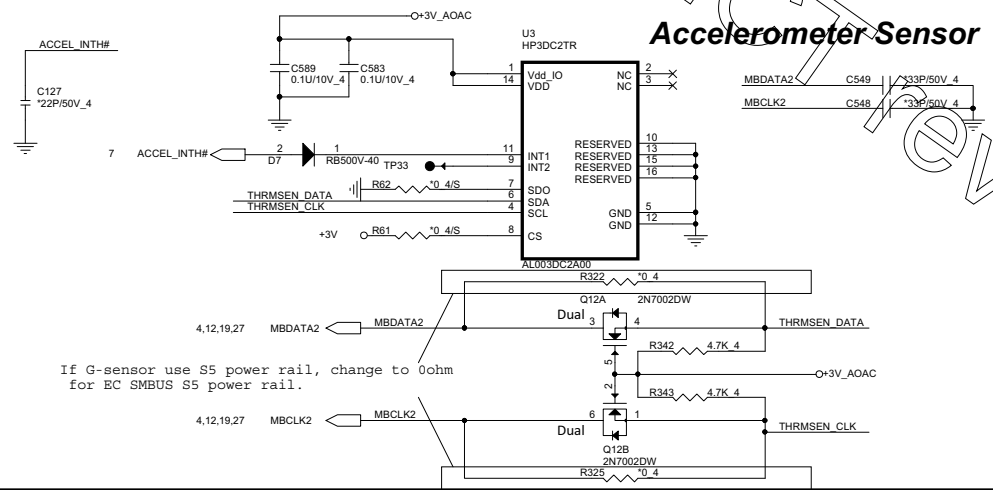
21,29,32,33,34,35,36,37
5.7,21,24,26,27,28,29

+5V5
+3VPCU

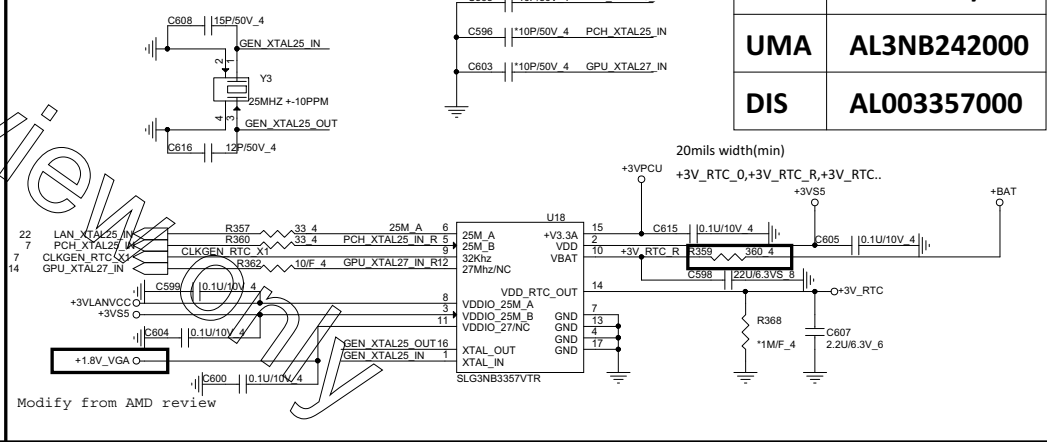
Mini Card WLAN/BT(Optional) SI change QI2 Type



Accelerometer Sensor

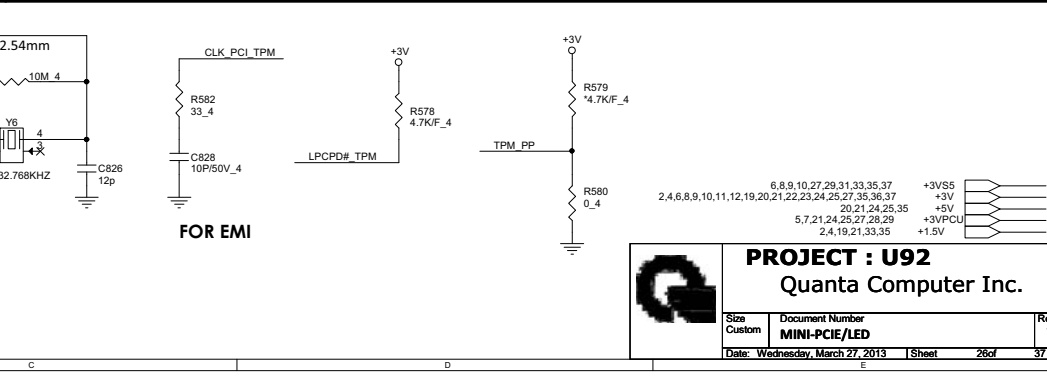
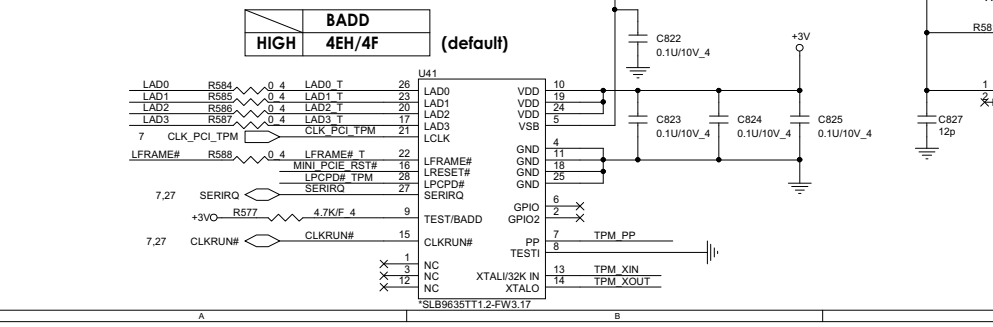


Green CLK Circuitry



G-CLK P/N	
UMA	AL3NB242000
DIS	AL003357000

TPM (1.2)

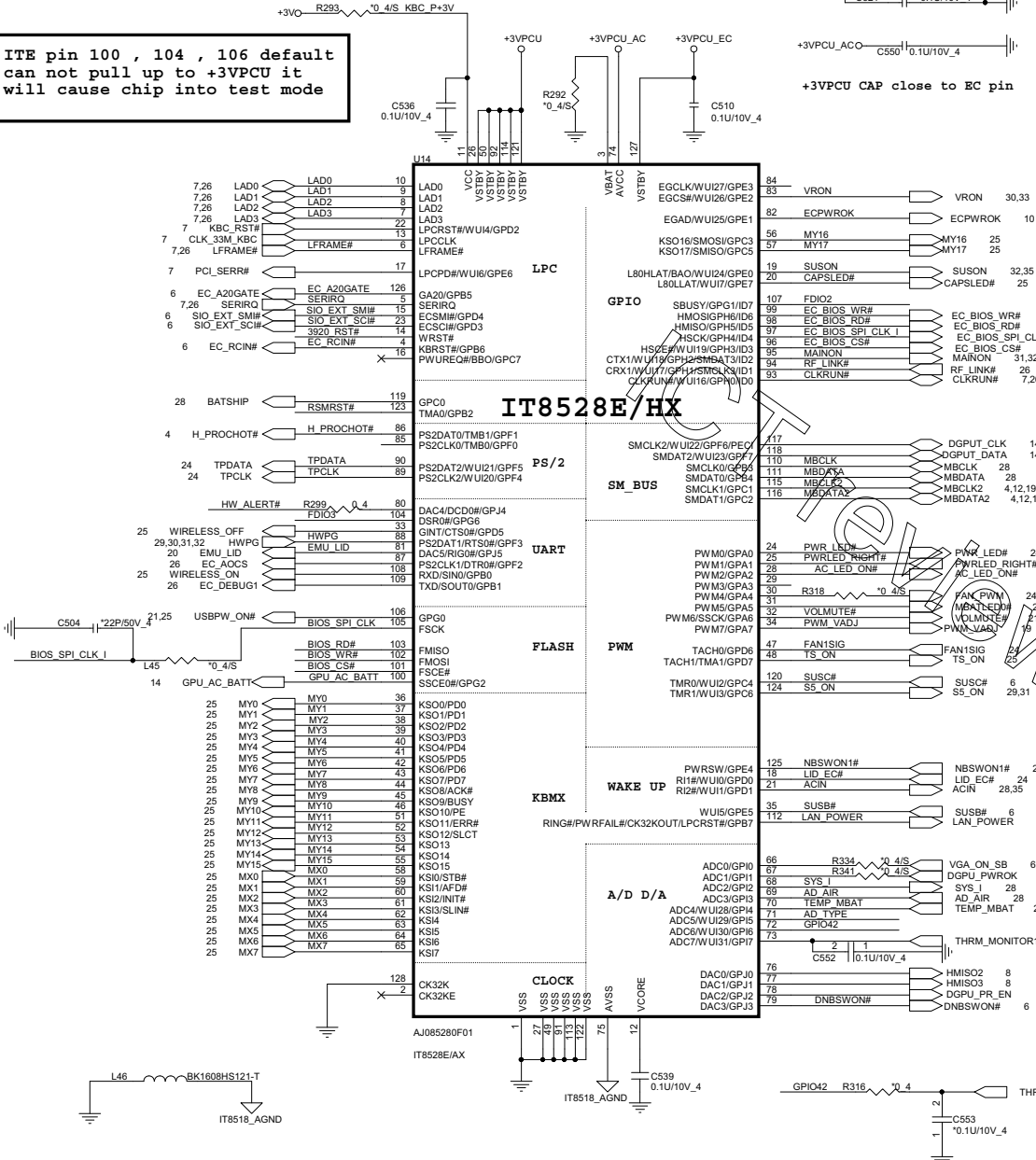


PROJECT : U92
Quanta Computer Inc.

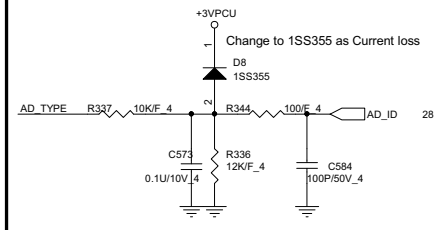
Size	Document Number	Rev
Custom	MINI-PCIE/LED	1A
Date: Wednesday, March 27, 2013	Sheet	26 of 37

2,4,6,8,9,10,11,12,19,20,21,22,23,24,25,26,35,36,37
5,7,21,24,25,26,28,29

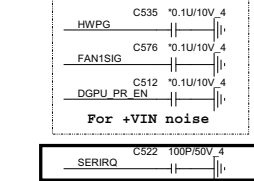
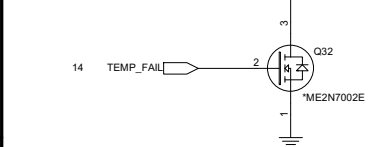
ITE pin 100, 104, 106 default can not pull up to +3VPCU it will cause chip into test mode



Smart adapter Type check

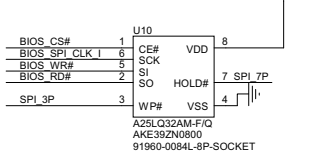


DGPU Thermal protect

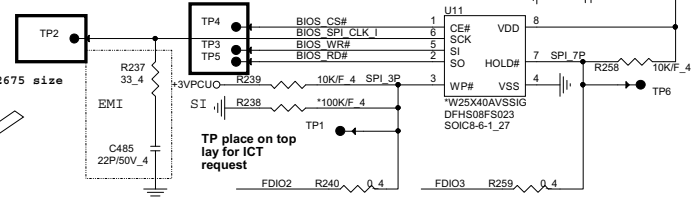


Vender	Size	P/N
AMIC	4M	AKE39F-0800
EON	4M	AKE392N0Q02
Socket		DFHS08FS023

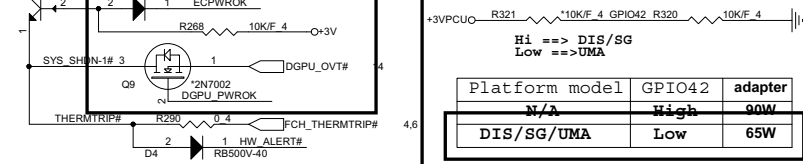
4M SPI EC ROM



128K byte SPI EC ROM



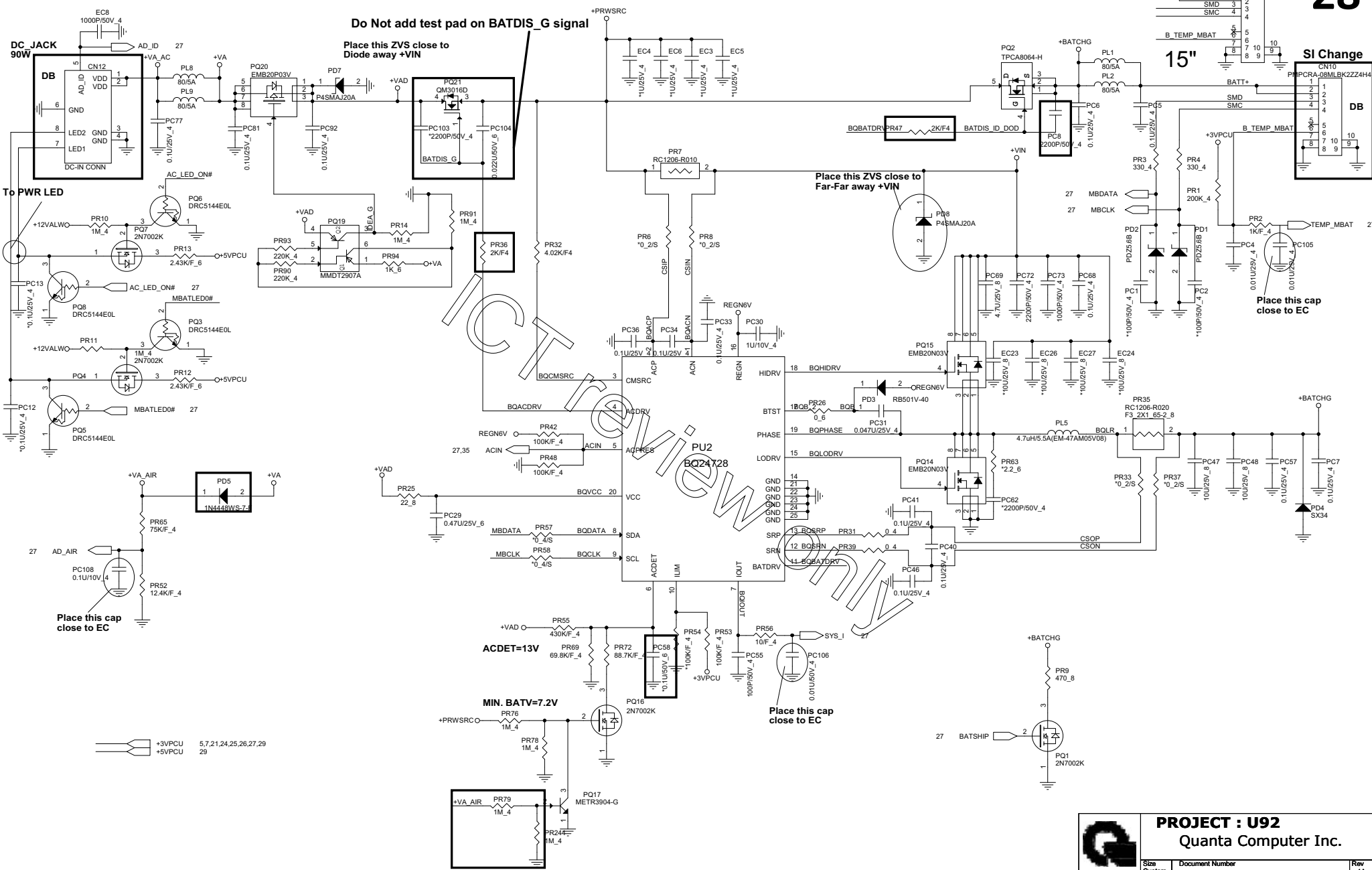
Adapter select



Platform model	GPIO42	adapter
N/A	High	90W
DIS/SG/UMA	Low	65W

PROJECT : U92
Quanta Computer Inc.

ADD VGA TEMP_FAIL function is active Hi



Do Not add test pad on BATDIS_G signal
Place this ZVS close to Diode away +VIN

Place this ZVS close to Far-Far away +VIN

15"

SI Change

Place this cap close to EC


Place this cap close to EC

Place this cap close to EC

- +3VPCU 5,7,21,24,25,26,27,29
- +5VPCU 29

ACDET=13V

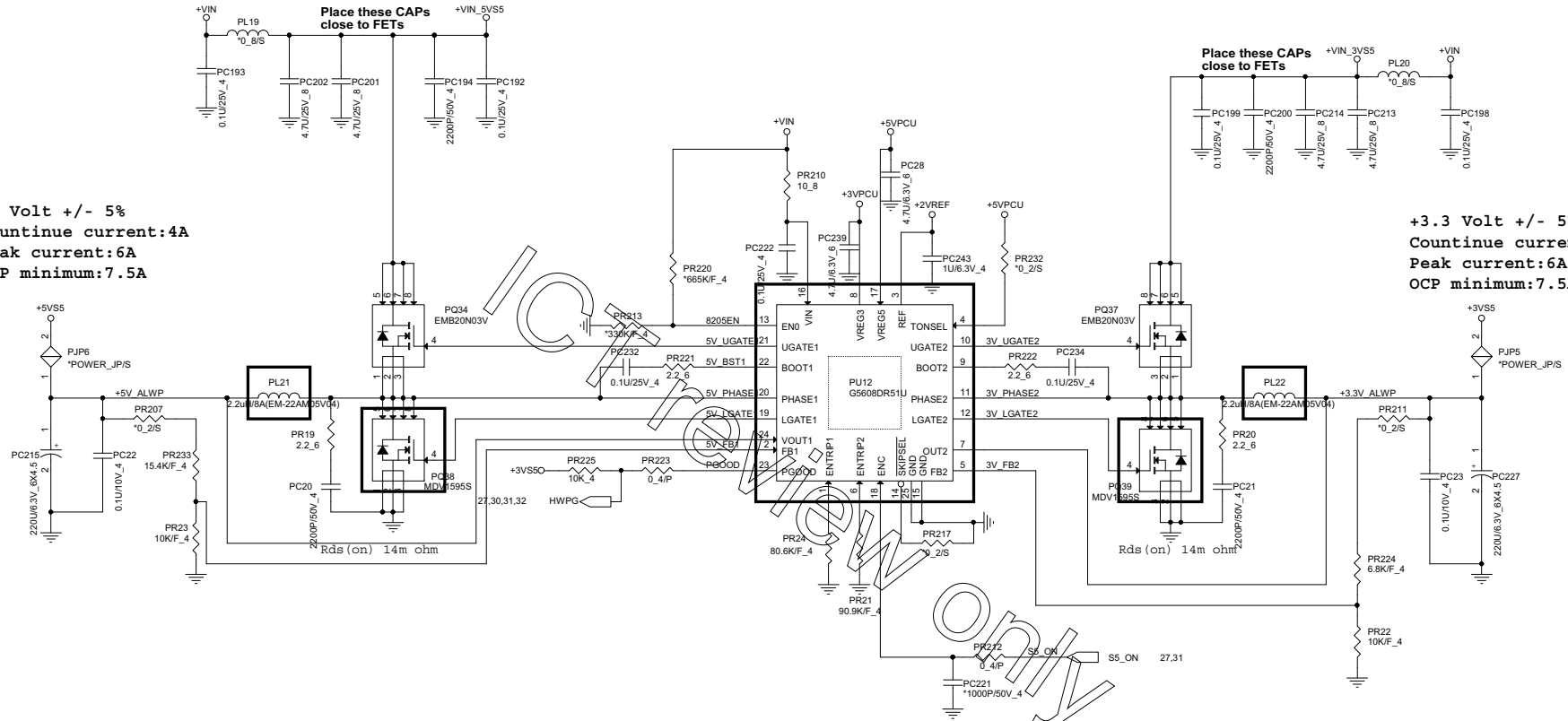
MIN. BATV=7.2V


		
PROJECT : U92		
Quanta Computer Inc.		
Size Custom	Document Number Charger (OZ8681)	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 28 of 37		

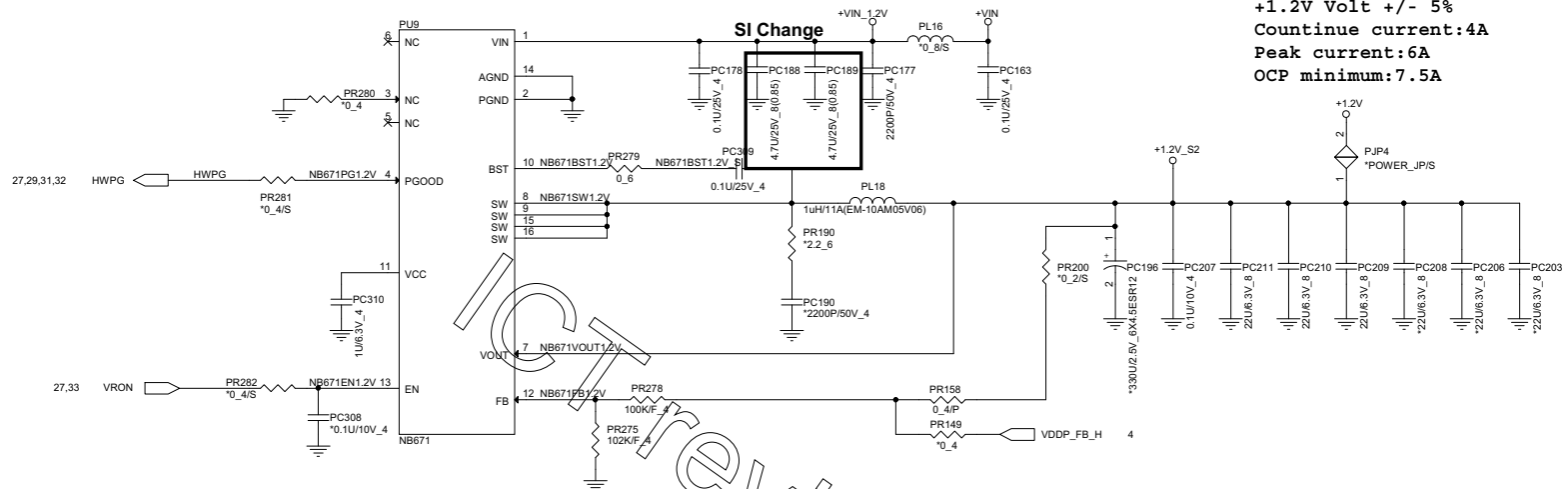
DC/DC +3VS5/+5VS5

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A


+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

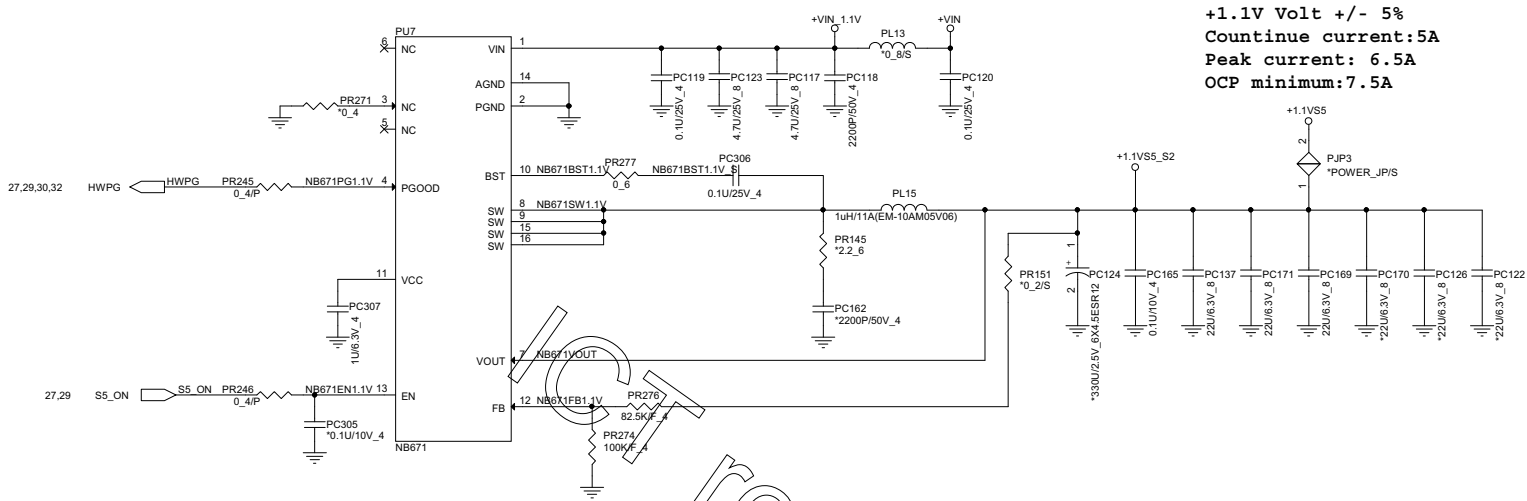


 NB5	PROJECT : R33 Quanta Computer Inc.	
	Size Custom Document Number 3/5VPCU(RT8223P)	Rev 1A
	Date: Wednesday, March 27, 2013 Sheet 29 of 37	

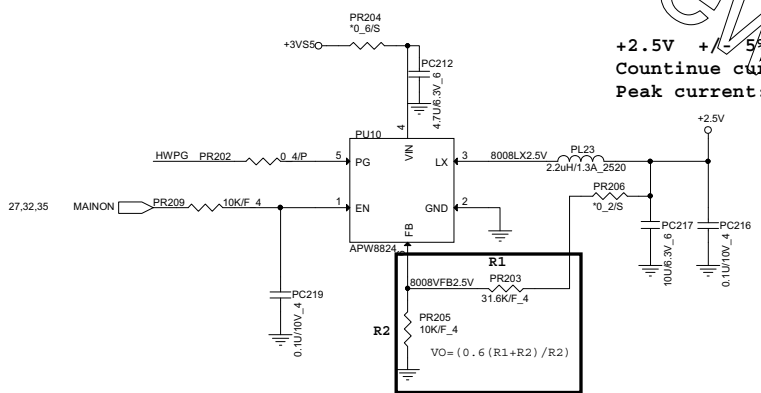


Review Only

	PROJECT : U92		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number +1.2V (RT8228)	Date: Wednesday, March 27, 2013 Sheet 30 of 37	



+1.1V Volt +/- 5%
Countinue current:5A
Peak current: 6.5A
OCP minimum:7.5A

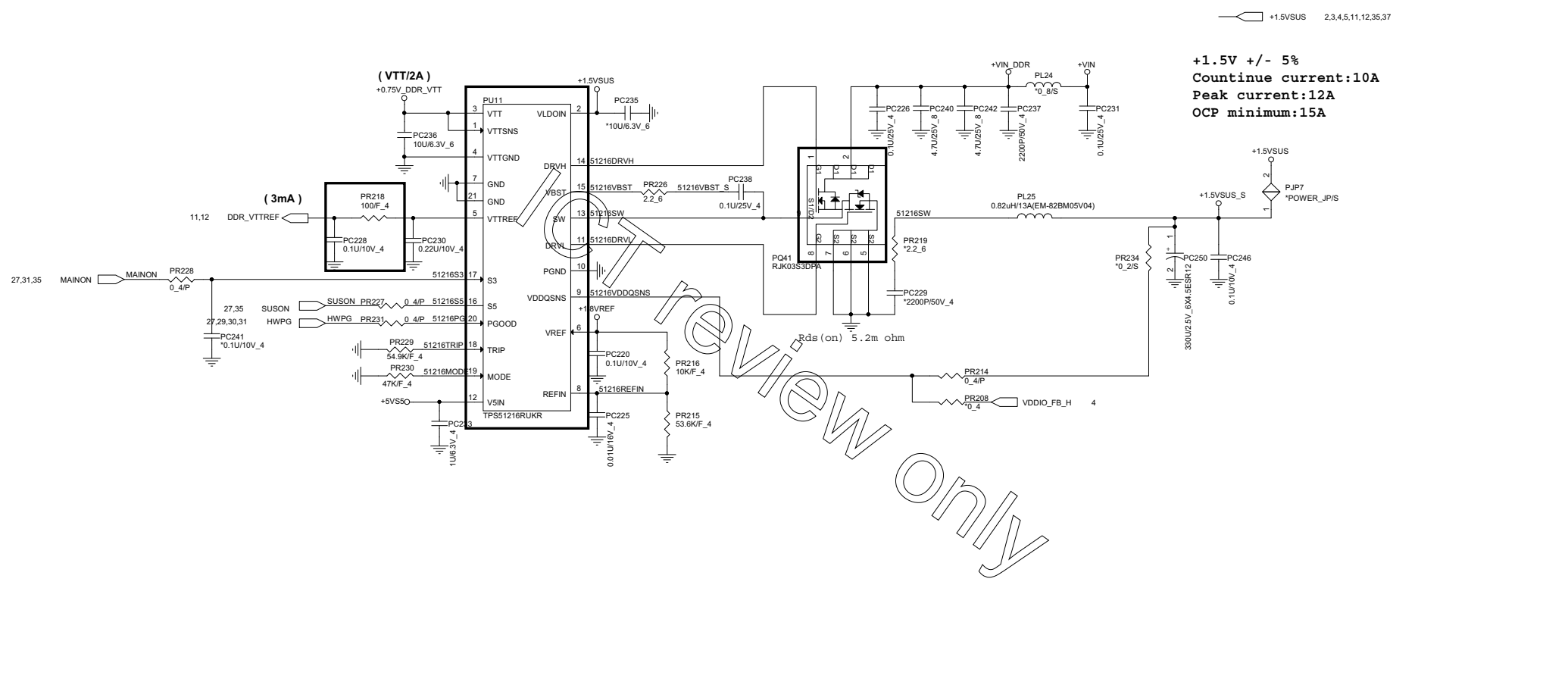


+2.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A

+VIN	20,24,28,29,30,32,34,35,36,37
+2.5V	5
+3VSS	6,8,9,10,26,27,29,33,35,37
+5VSS	21,25,29,32,33,34,35,36,37
+1.1VSS	9,35
+5VPCU	28,29

PROJECT : U92
Quanta Computer Inc.

Size Custom	Document Number +1.1VSS (RT8228)/2.5V	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 31 of 37		




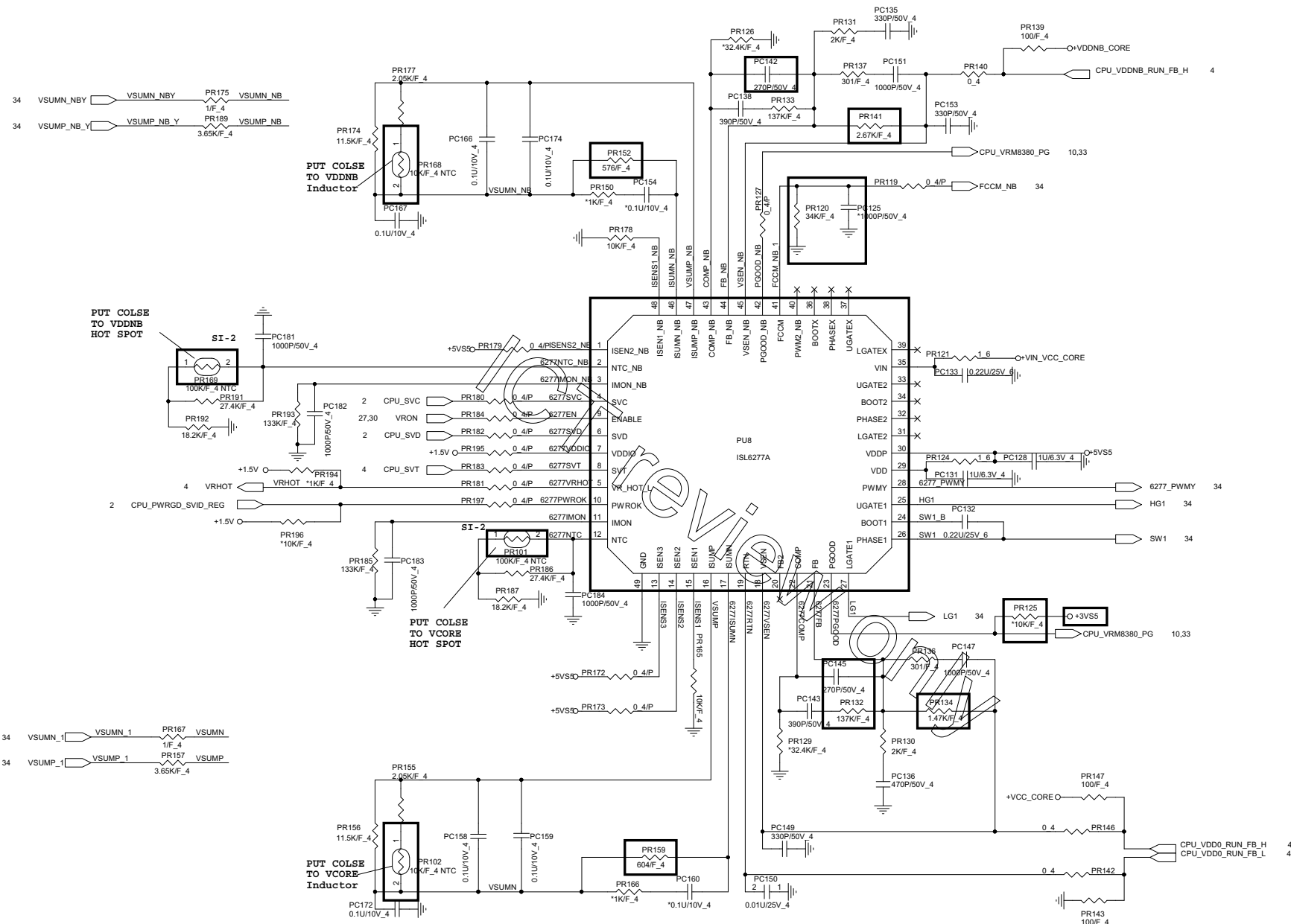
+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCP minimum:15A


+1.5VSUS 2,3,4,5,11,12,35,37

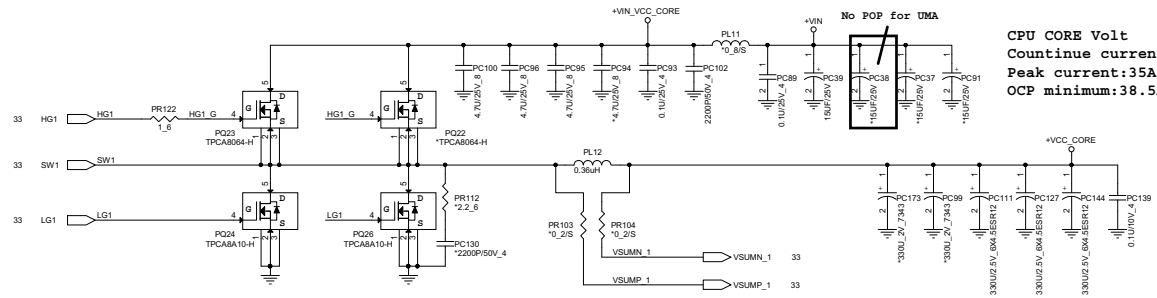
+1.5VSUS
 PJP7
 *POWER_JP/S

Review only

	PROJECT : U92		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3 (RT8207)	
Date: Wednesday, March 27, 2013		Sheet 32 of 37	



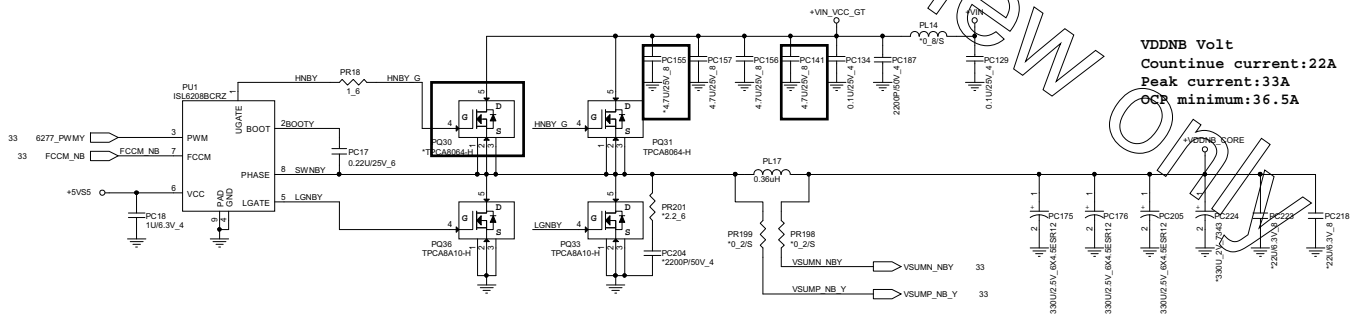
	PROJECT : U92		Rev 1A	
	Quanta Computer Inc.			
	Size Custom	Document Number		ISL6277
	Date: Wednesday, March 27, 2013			Sheet 33 of 37




CPU CORE Volt
 Continue current:22A
 Peak current:35A
 OCP minimum:38.5A

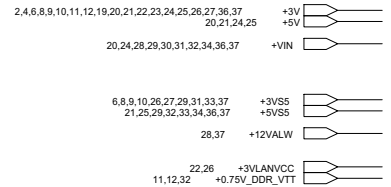
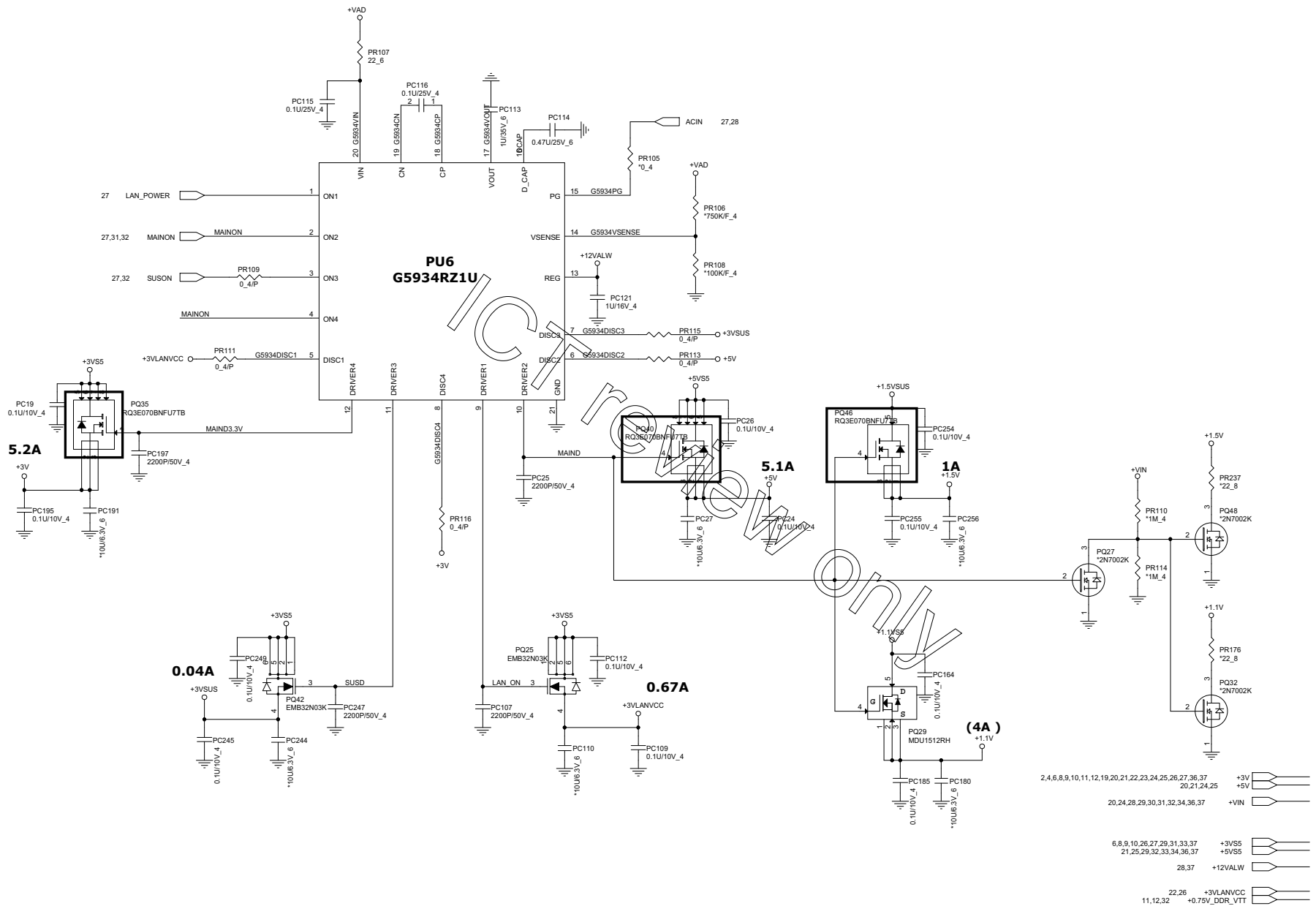
No POP for UMA


ICT review



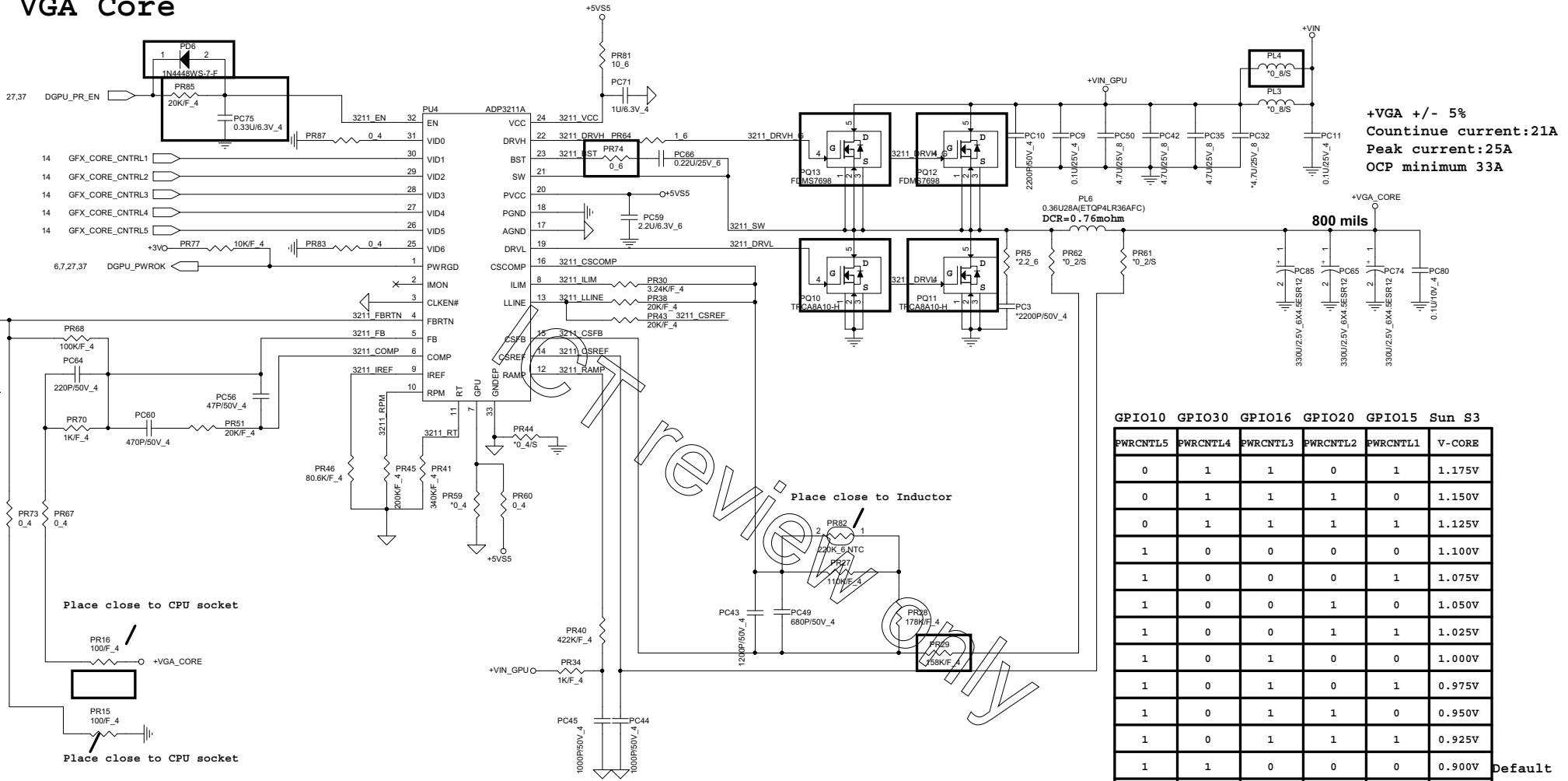
VDDNB Volt
 Continue current:22A
 Peak current:33A
 OCP minimum:36.5A

		
PROJECT : U92 Quanta Computer Inc.		
Size Custom	Document Number ISL6288	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 34 of 37		



 PROJECT : U92 Quanta Computer Inc.		
Date: Wednesday, March 27, 2013 Sheet 35 of 37		

VGA Core



+VGA +/- 5%
Countinue current:21A
Peak current:25A
OCP minimum 33A

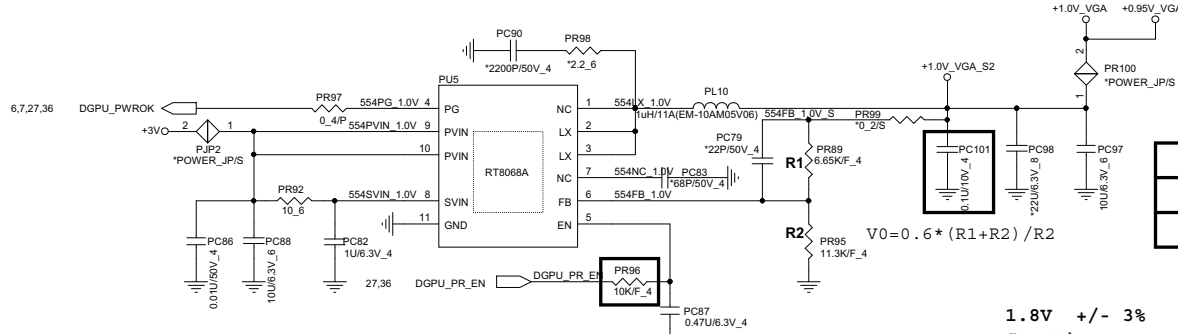
GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun S3	V-CORE
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1		
0	1	1	0	1		1.175V
0	1	1	1	0		1.150V
0	1	1	1	1		1.125V
1	0	0	0	0		1.100V
1	0	0	0	1		1.075V
1	0	0	1	0		1.050V
1	0	1	0	0		1.000V
1	0	1	0	1		0.975V
1	0	1	1	0		0.950V
1	0	1	1	1		0.925V
1	1	0	0	0		0.900V
1	1	0	0	1		0.875V
1	1	0	1	0		0.850V
1	1	0	1	1		0.825V
1	1	1	0	0		0.800V
1	1	1	0	1		0.775V

Default

PROJECT : U92
Quanta Computer Inc.

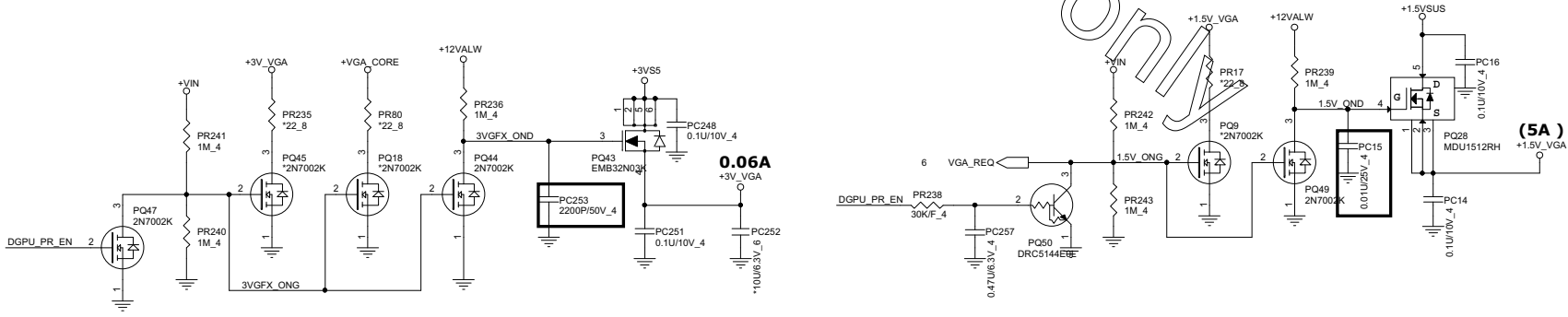
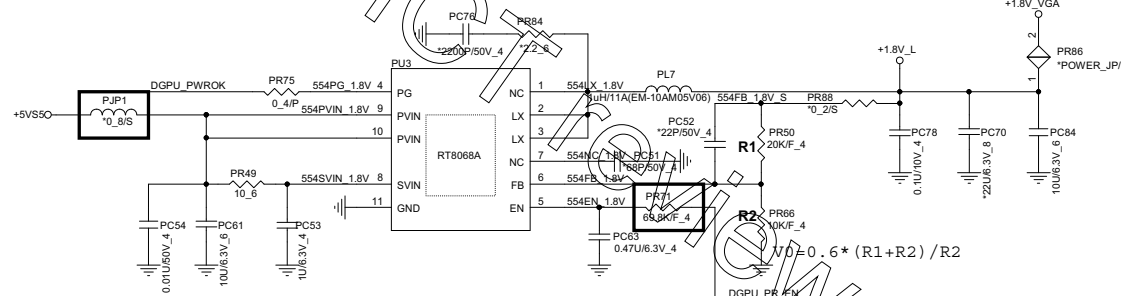
Size Custom	Document Number +VGA CORE NCP3218G	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 36 of 37		

+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



- +3V_VGA 16
- +1.0V_VGA 13,14,16
- +12VALW 28,35
- +1.8V_VGA 13,14,16,26

PROJECT : U92
Quanta Computer Inc.

Size Custom	Document Number +VGA POWER	Rev 1A
Date: Wednesday, March 27, 2013 Sheet 37 of 37		

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