

QT6 BLOCK DIAGRAM

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN2
LAYER 4 : SGND1
LAYER 5 : SVCC
LAYER 6 : IN2
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking

- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

PAGE 40

SYSTEM CHARGER(ISL6251AHAZ-T)
PAGE 41

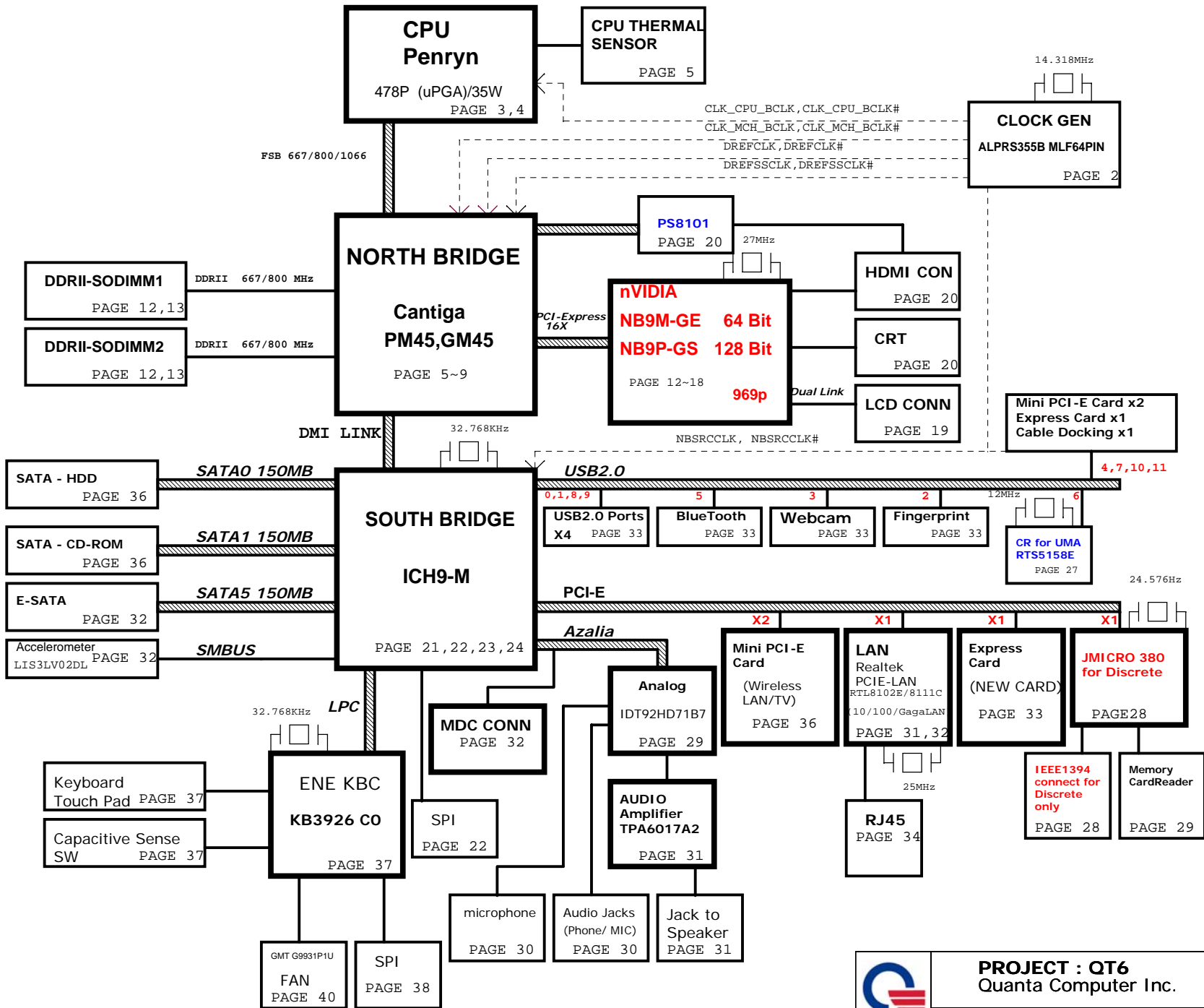
SYSTEM POWER ISL6237IRZ-T
PAGE 42

DDR II SMDR_VTERM
1.8V/1.8VSUS(TPSS51116REGR)
PAGE 46

VCCP +1.5V AND GMCH
1.05V(RT8204)
PAGE 43

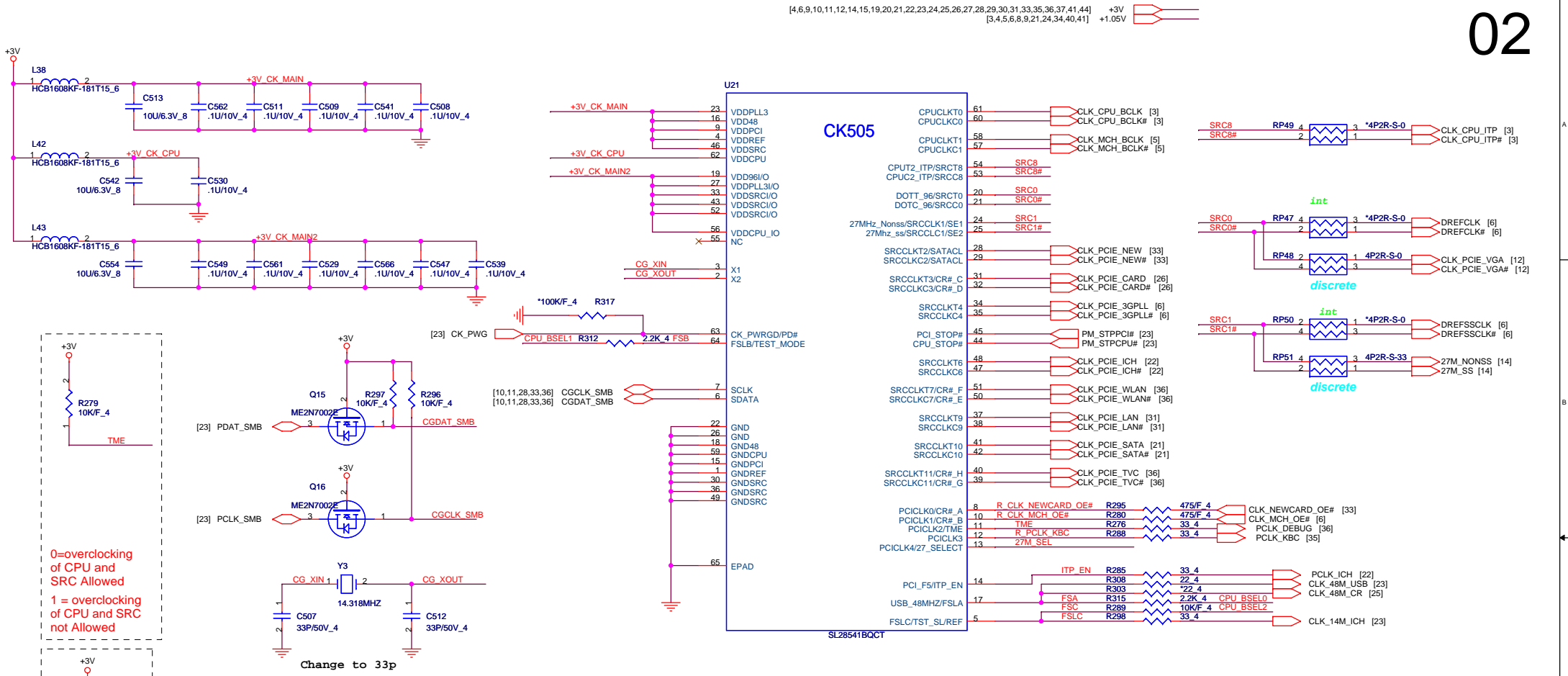
VGACORE(1.025V)Oz8118
PAGE 45

CPU CORE ISL6266A
PAGE 44

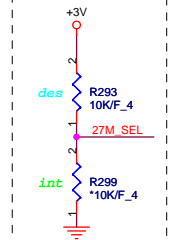


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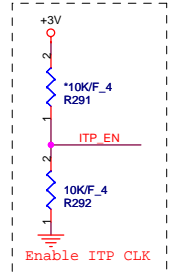
Size Custom Document Number NB5 Block Diagram Rev 1A
 Date: Tuesday, February 26, 2008 Sheet 1 of 44



0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed



0=UMA
1 = External VGA

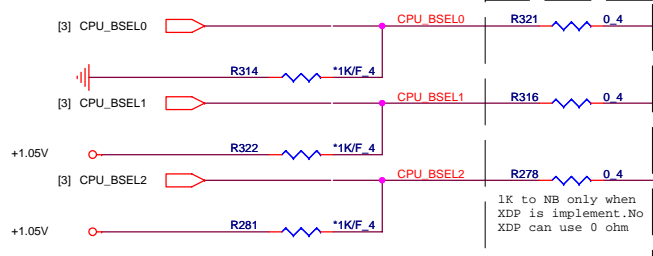


27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

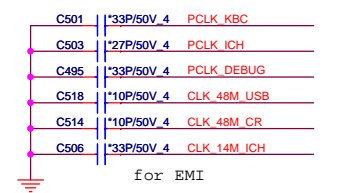
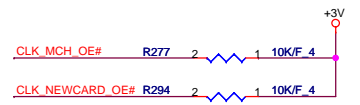
CK505 QFN64

ICS ICS9LPRS355BKLF ALPRS355000
Silego SLG8SP513VTR AL8SP513000
Realtek RTM875N-606-VD-GR AL000875000

CPU Clock select



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

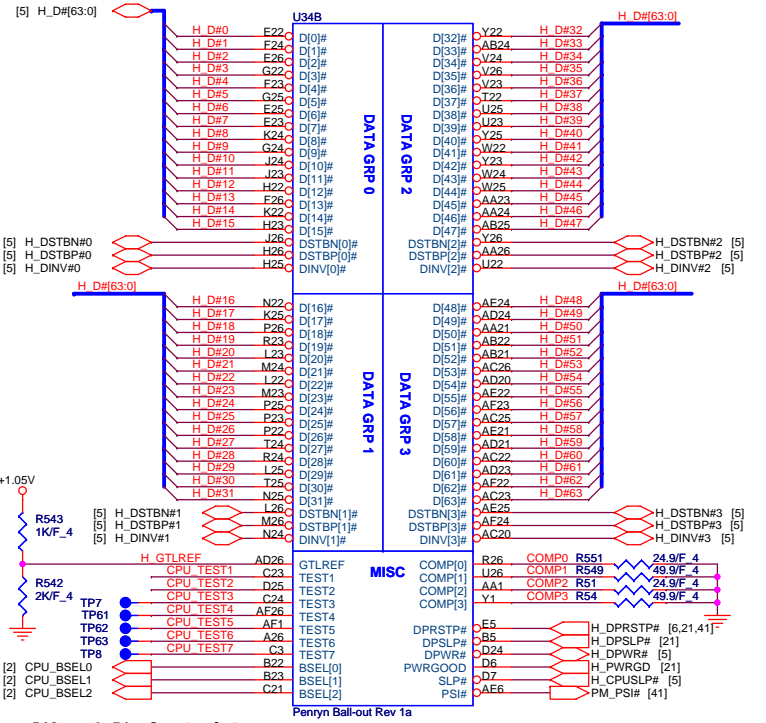
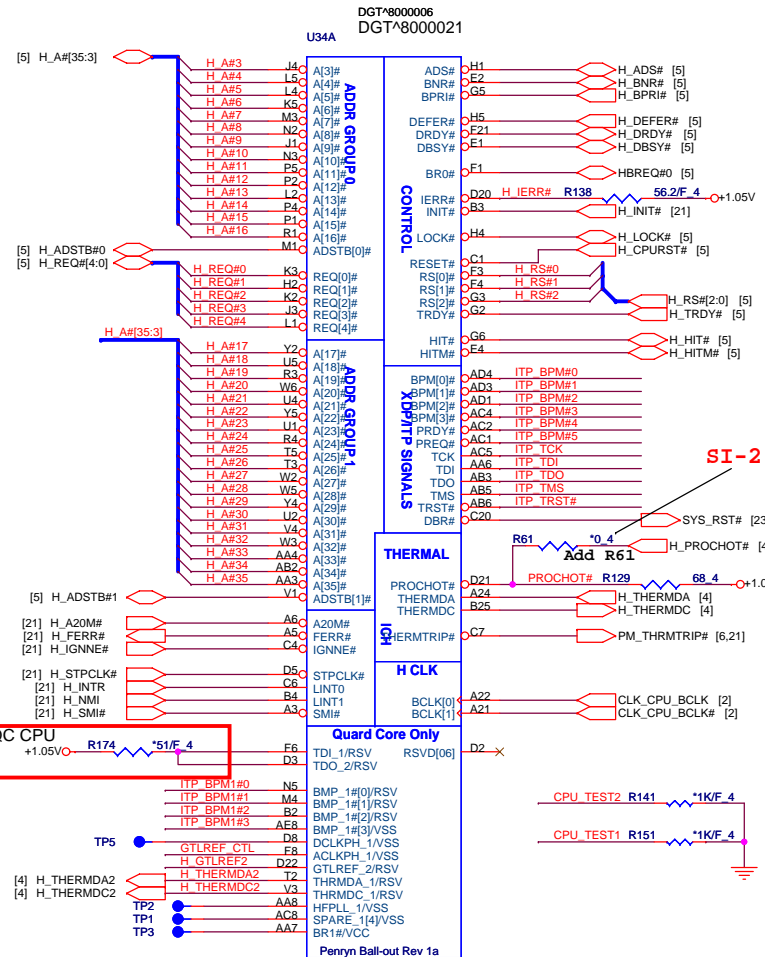


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Size Custom Document Number
Clock Generator

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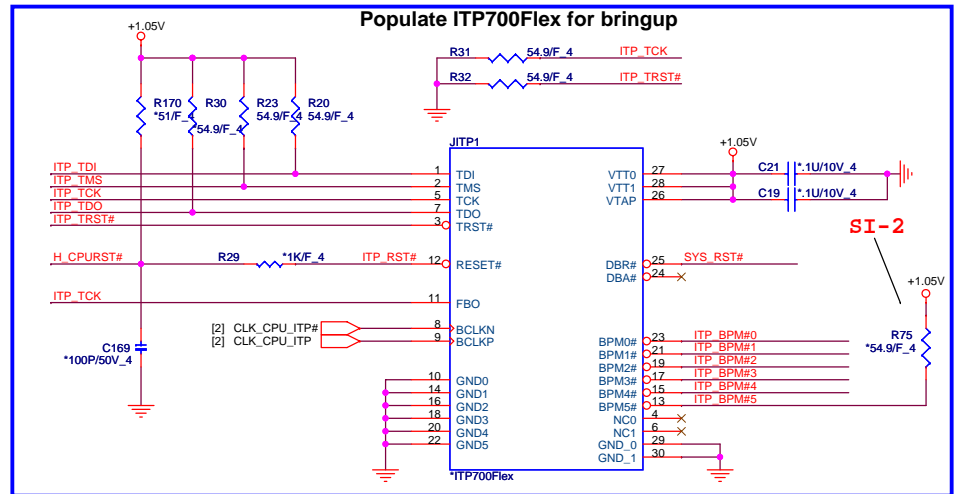
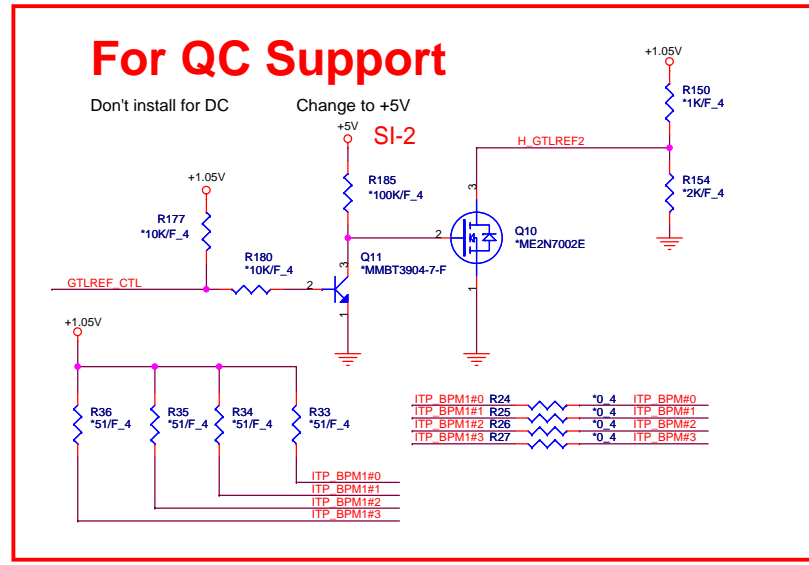
Rev 1A



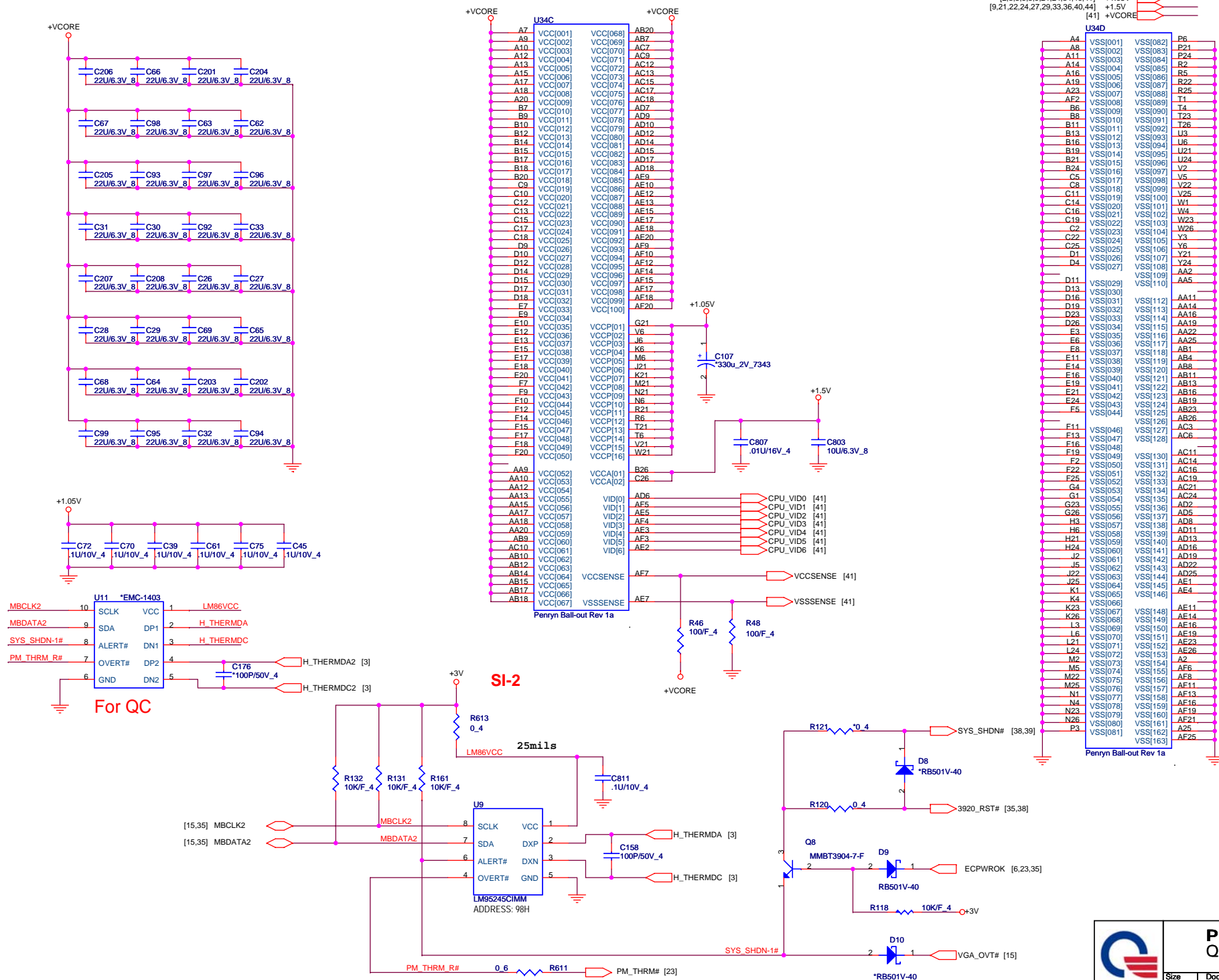
For QC CPU
+1.05V R174 *51/F_4

CPU_TEST2 R141 *1K/F_4
CPU_TEST1 R151 *1K/F_4

R542 --> 1.74K for Quad Core



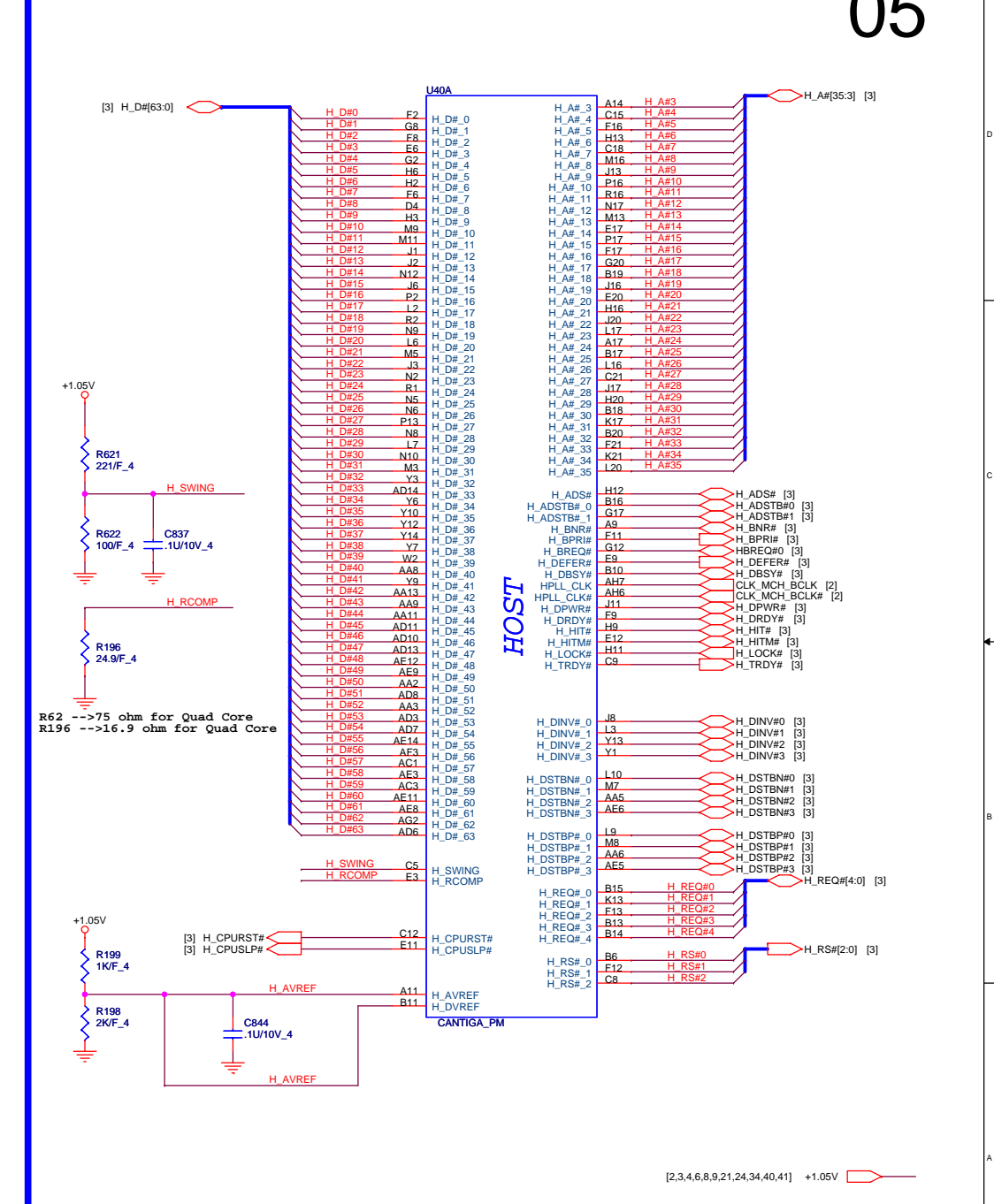
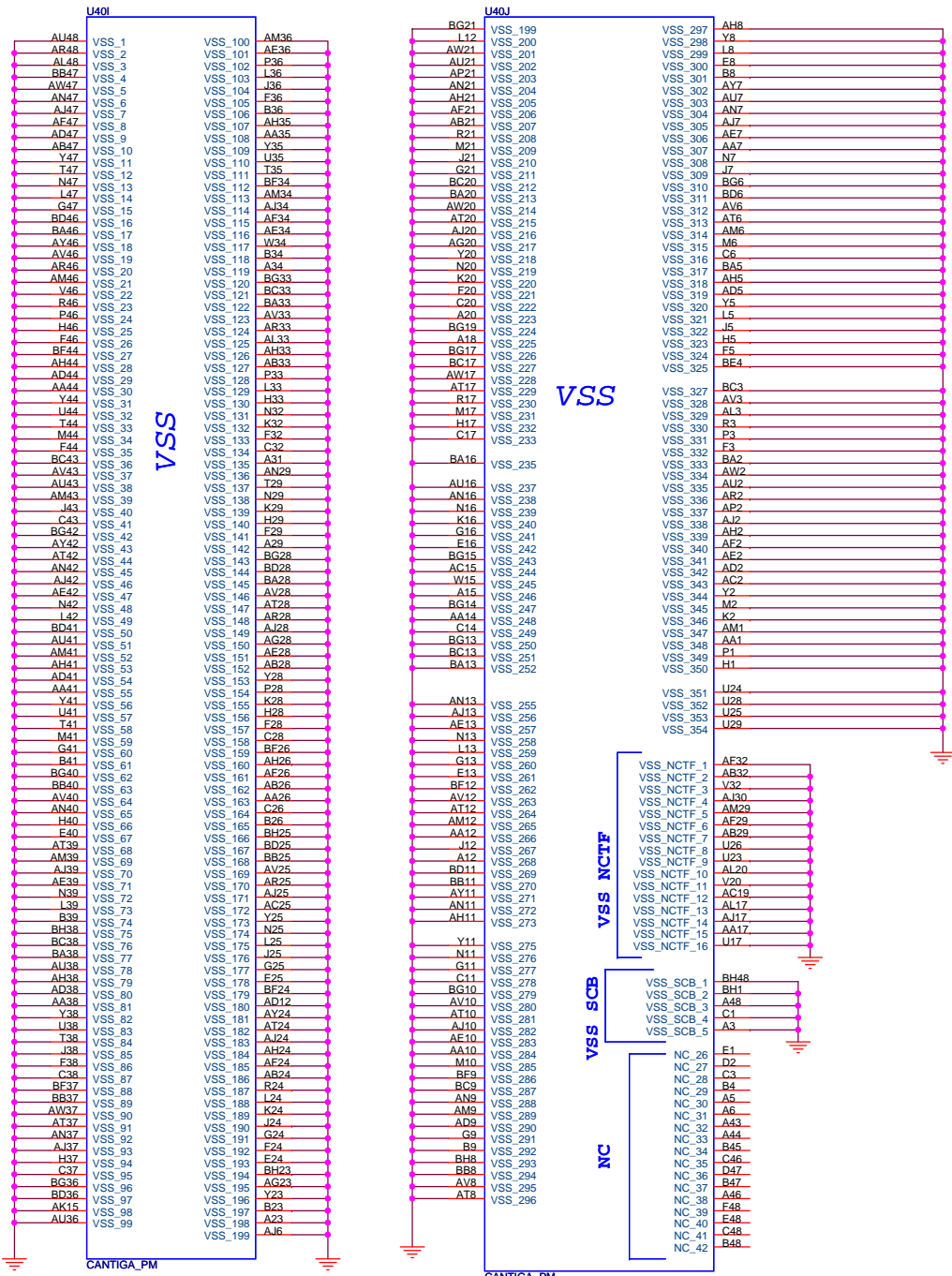
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NB5 Penryn & TH Monitor 2/2

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MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)
MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
Low = Reverse Lane
High = Normal operation(Default)
MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes

MCH_CFG_6 ITPM Host Interface
Low =The ITPM Host Interface is enabled2
High = The ITPM Host Interface is disabled (default)

MCH_CFG_7 Intel(R) Management Engine Crypto
Low = Intel(R) Management Engine Crypto
High = Intel(R) Management Engine Crypto

MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High = Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

Table with 2 columns: MCH_CFG_12, MCH_CFG_13. Rows include Reserved, XOR Mode enabled, All-Z Mode enabled, Normal operation (Default).

Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE
Low = Only digital display port (SDVO/DP/HDMI) or PCIE is operational (default)
High = Digital display port (SDVO/DP/HDMI) and PCIE are operating simultaneously with the DP port

MCH_CFG:0
000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved

MCH_CFG_3 MCH_CFG_4 MCH_CFG_5 MCH_CFG_6 MCH_CFG_7 MCH_CFG_8 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_12 MCH_CFG_13 MCH_CFG_14 MCH_CFG_15 MCH_CFG_16 MCH_CFG_17 MCH_CFG_18 MCH_CFG_19 MCH_CFG_20

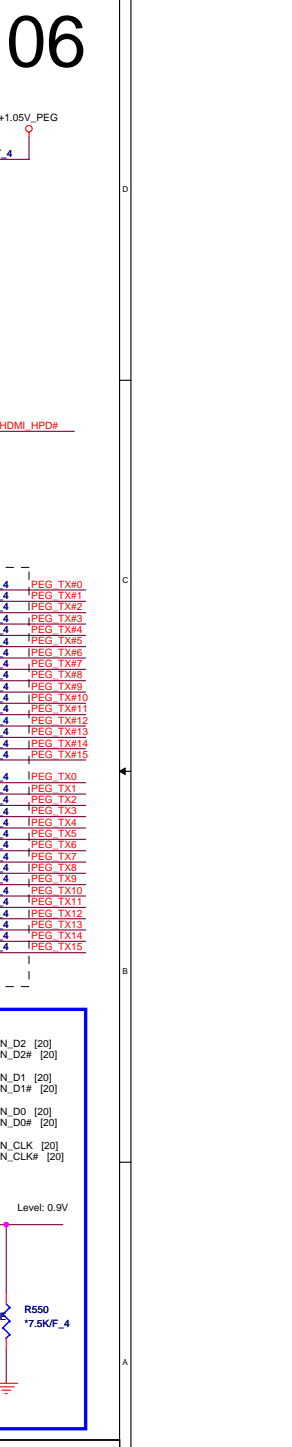
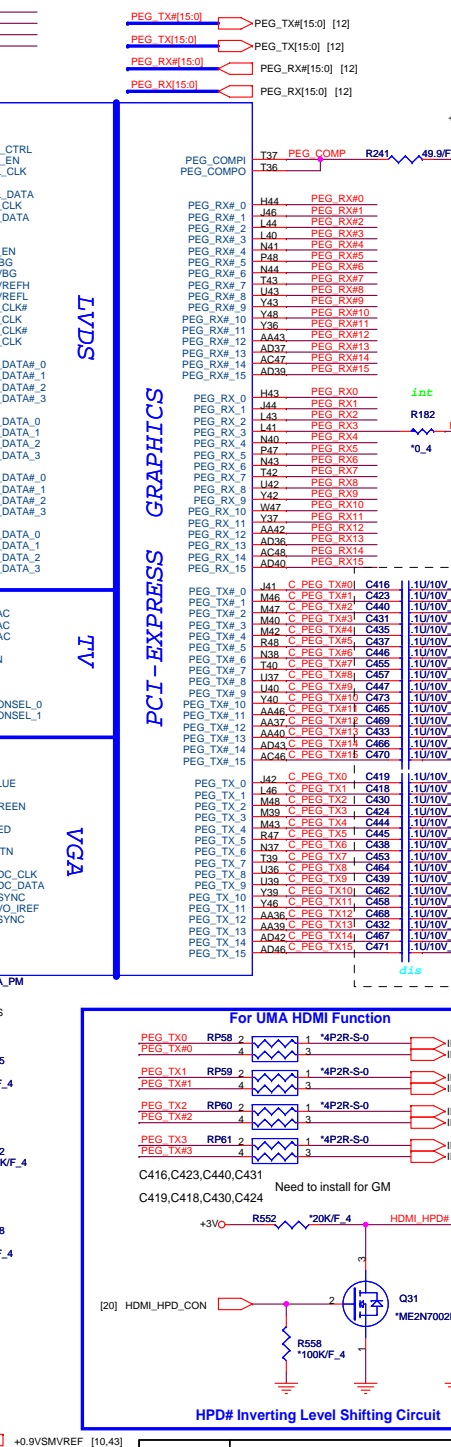
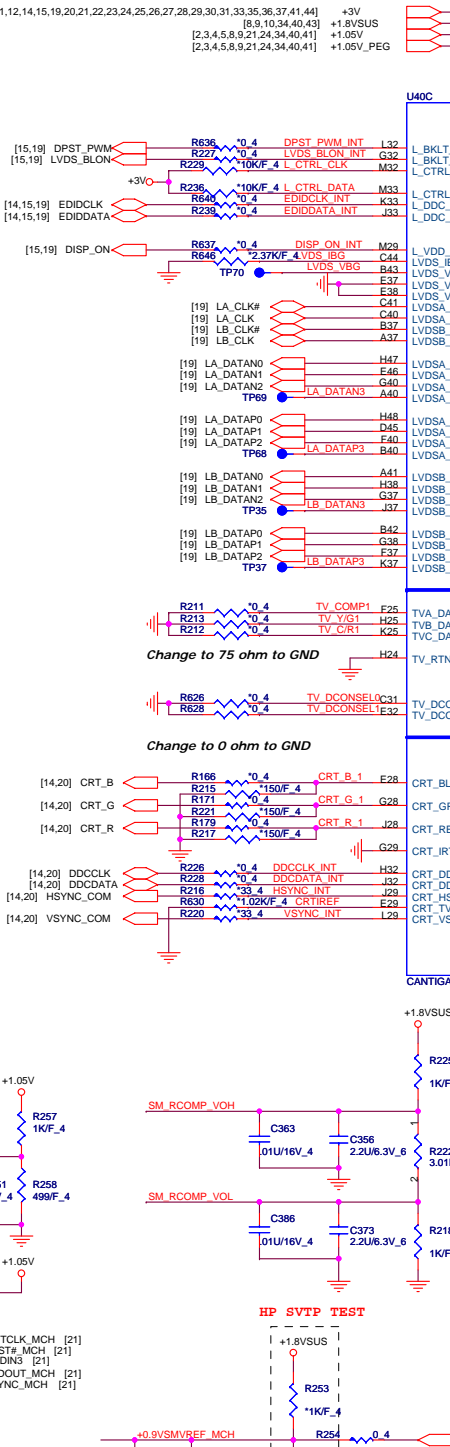
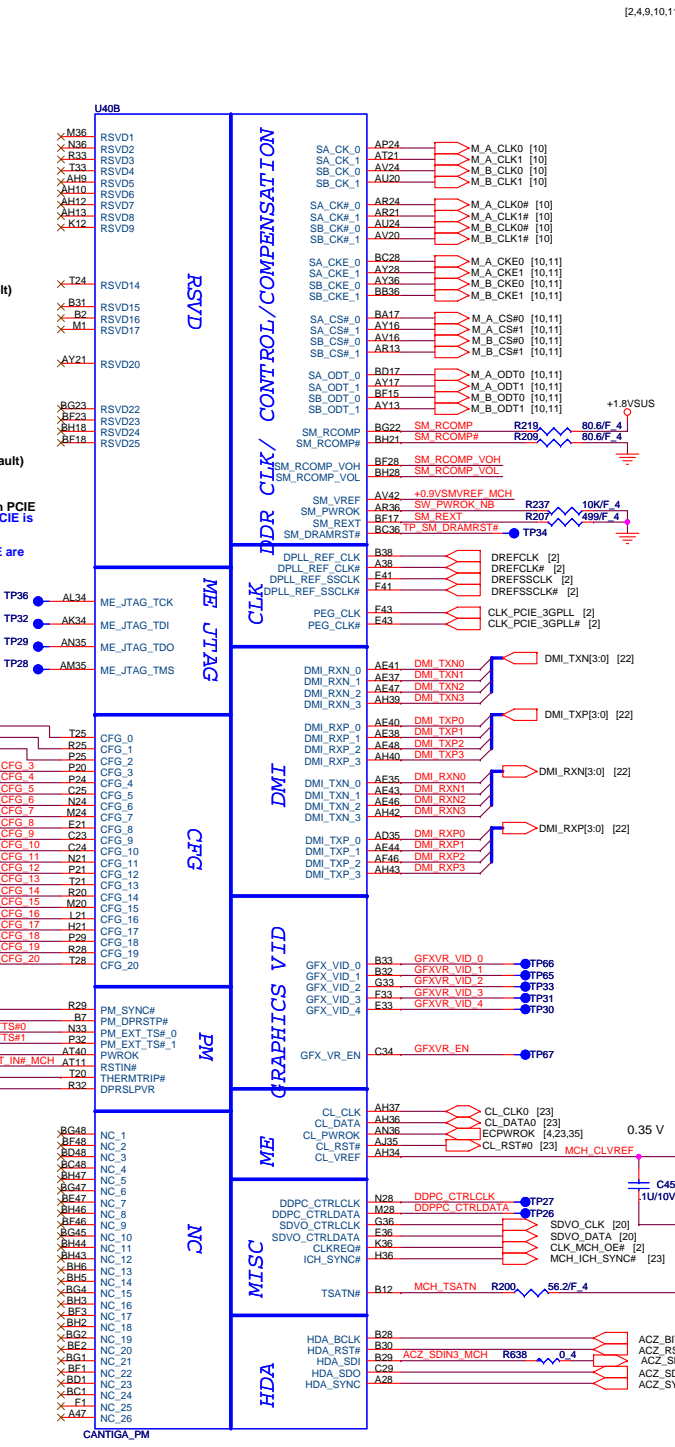
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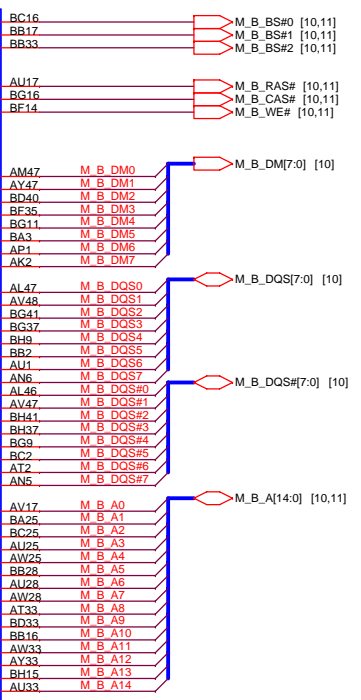
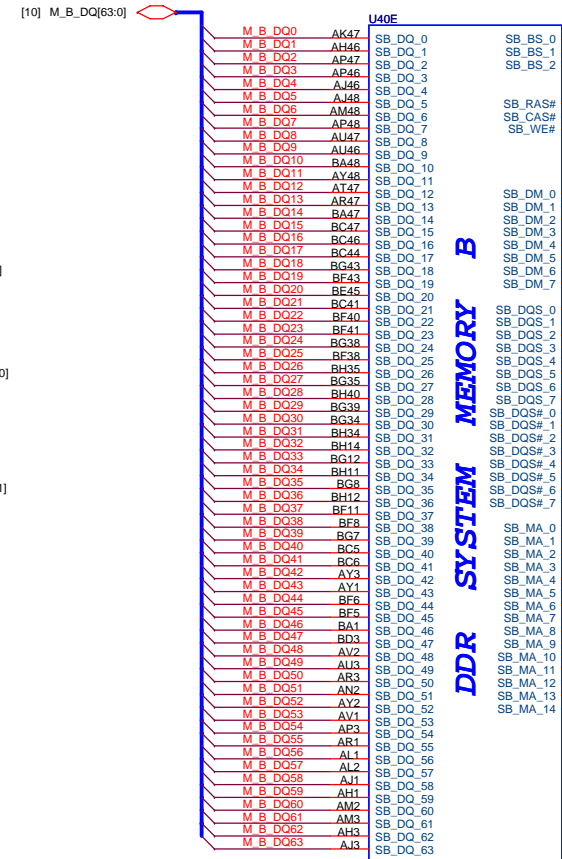
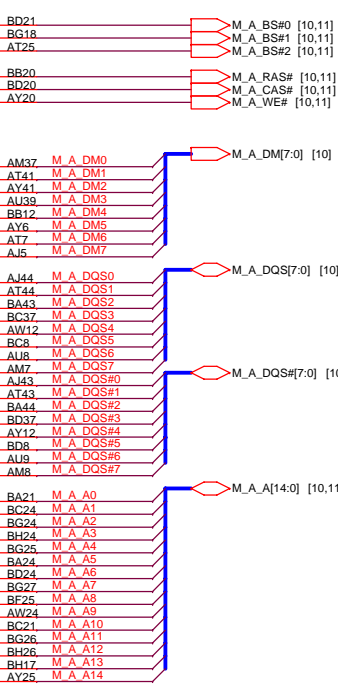
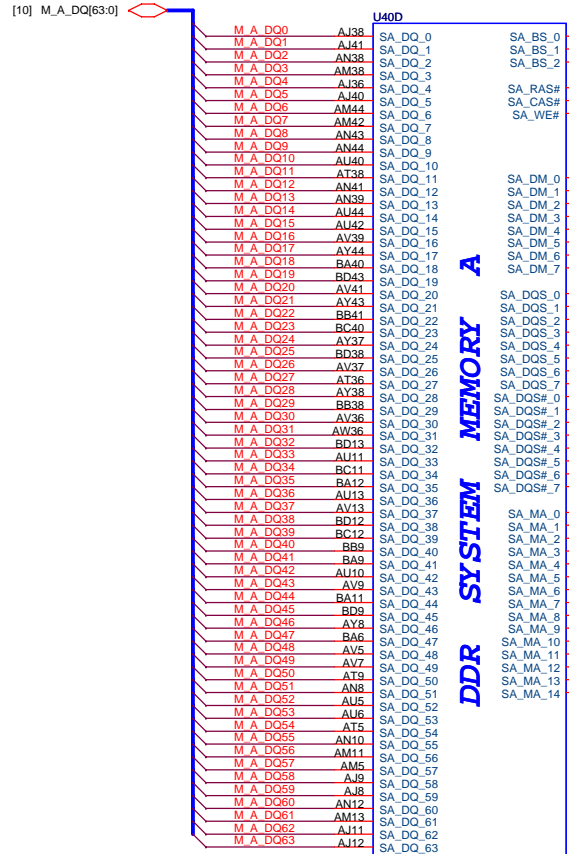
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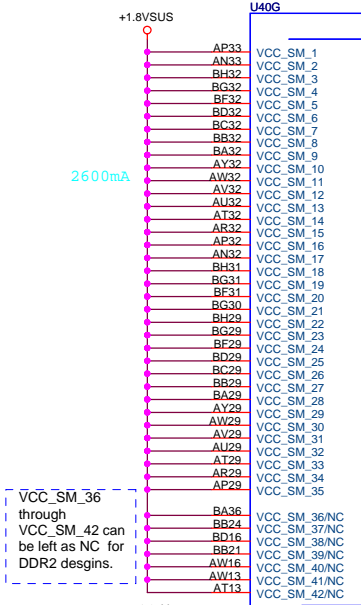
PM_SYNC# H_DPRSTP# PM_EXTTS#0 PM_EXTTS#1 DELAY_VR_PWRGOOD PLT_RST-R# PM_THRTRIP# DPRSLPVR

NC.1 NC.2 NC.3 NC.4 NC.5 NC.6 NC.7 NC.8 NC.9 NC.10 NC.11 NC.12 NC.13 NC.14 NC.15 NC.16 NC.17 NC.18 NC.19 NC.20 NC.21 NC.22 NC.23 NC.24 NC.25 NC.26

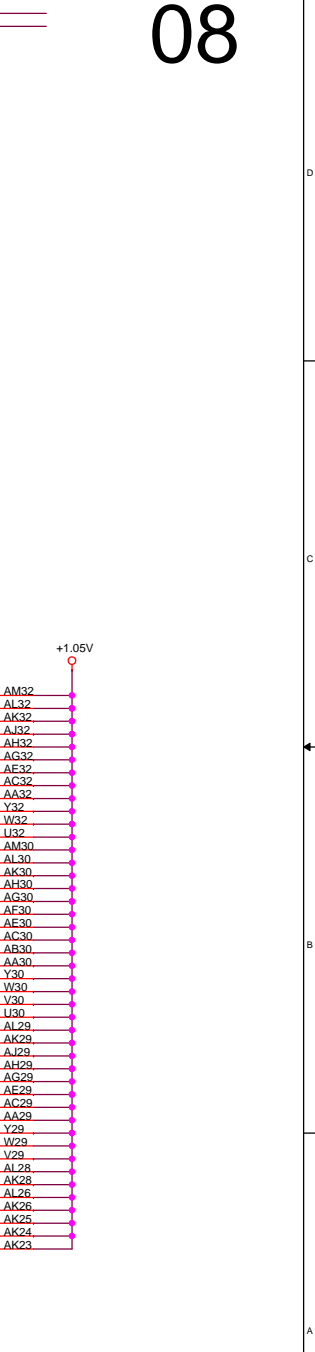
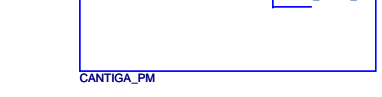
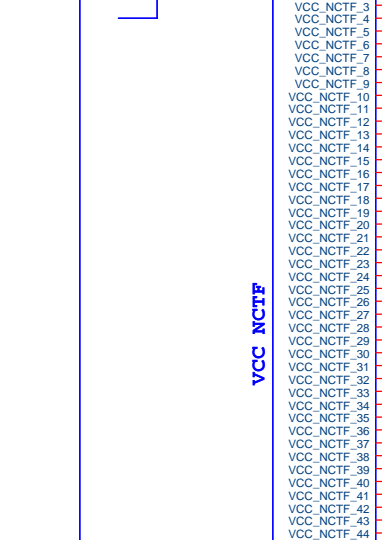
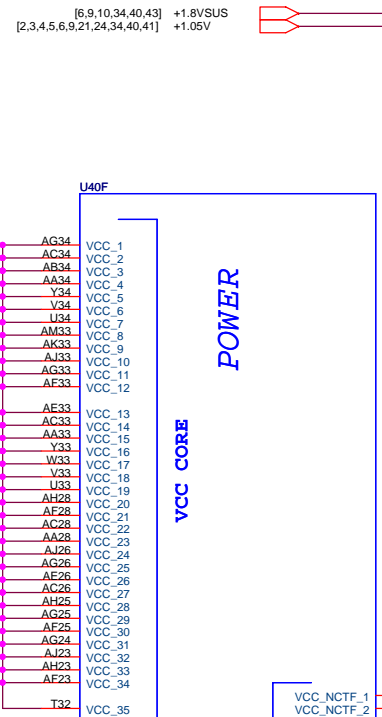
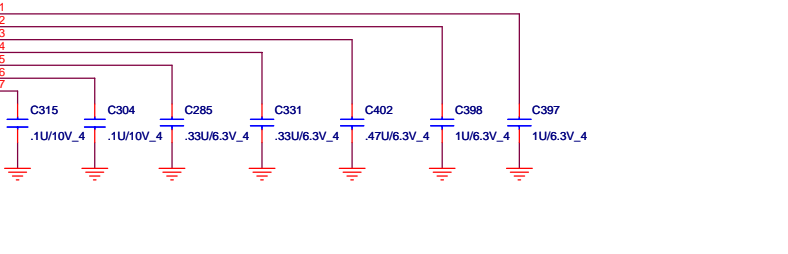
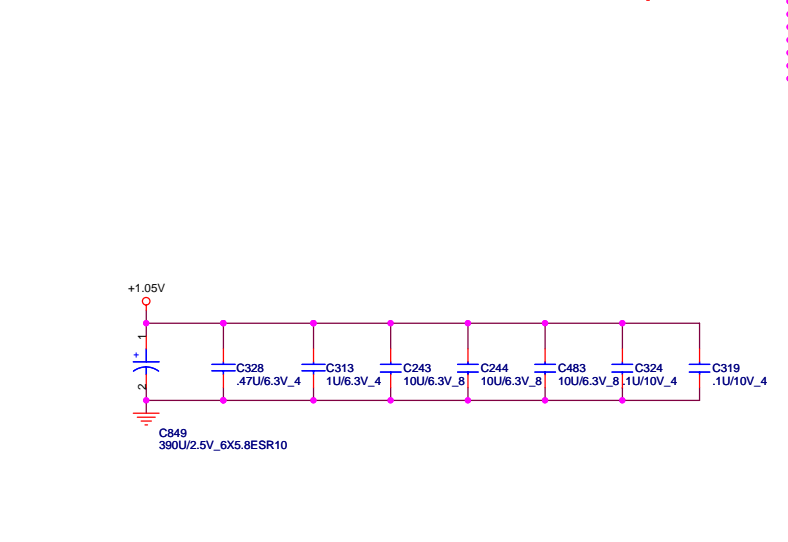
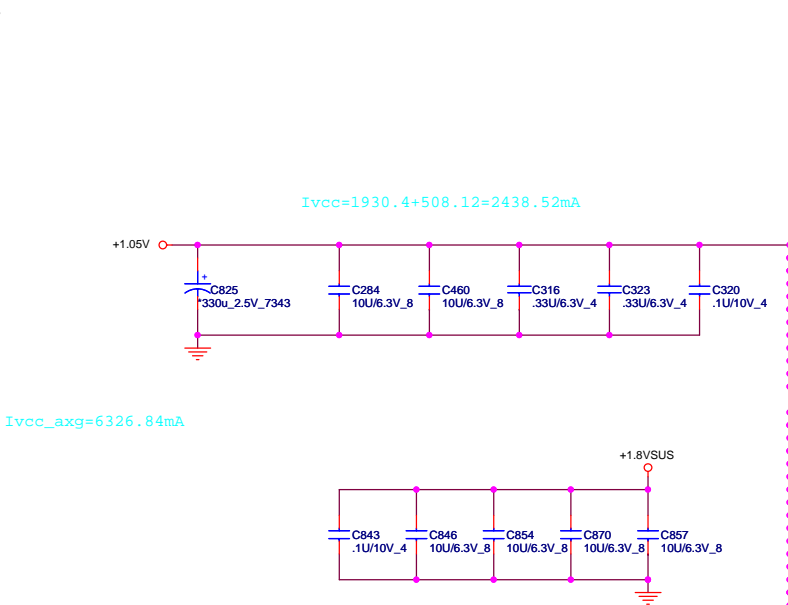
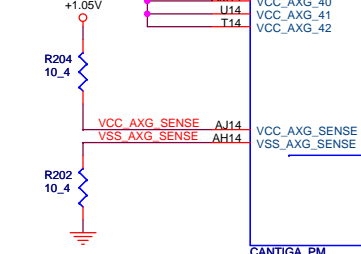
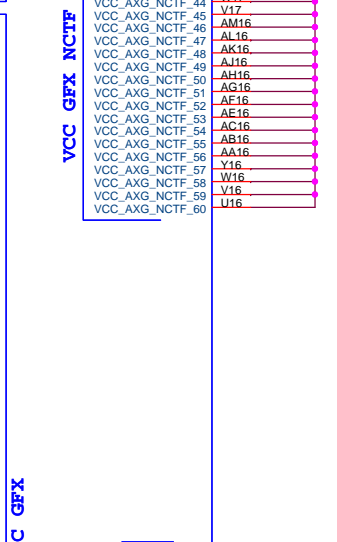
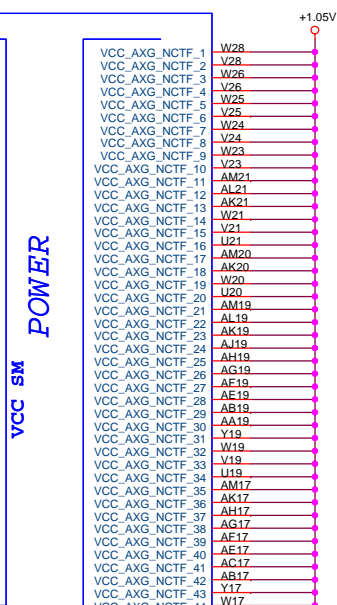
ACZ_BITCLK_MCH R34 *33.4 C874 *33P/50V_4

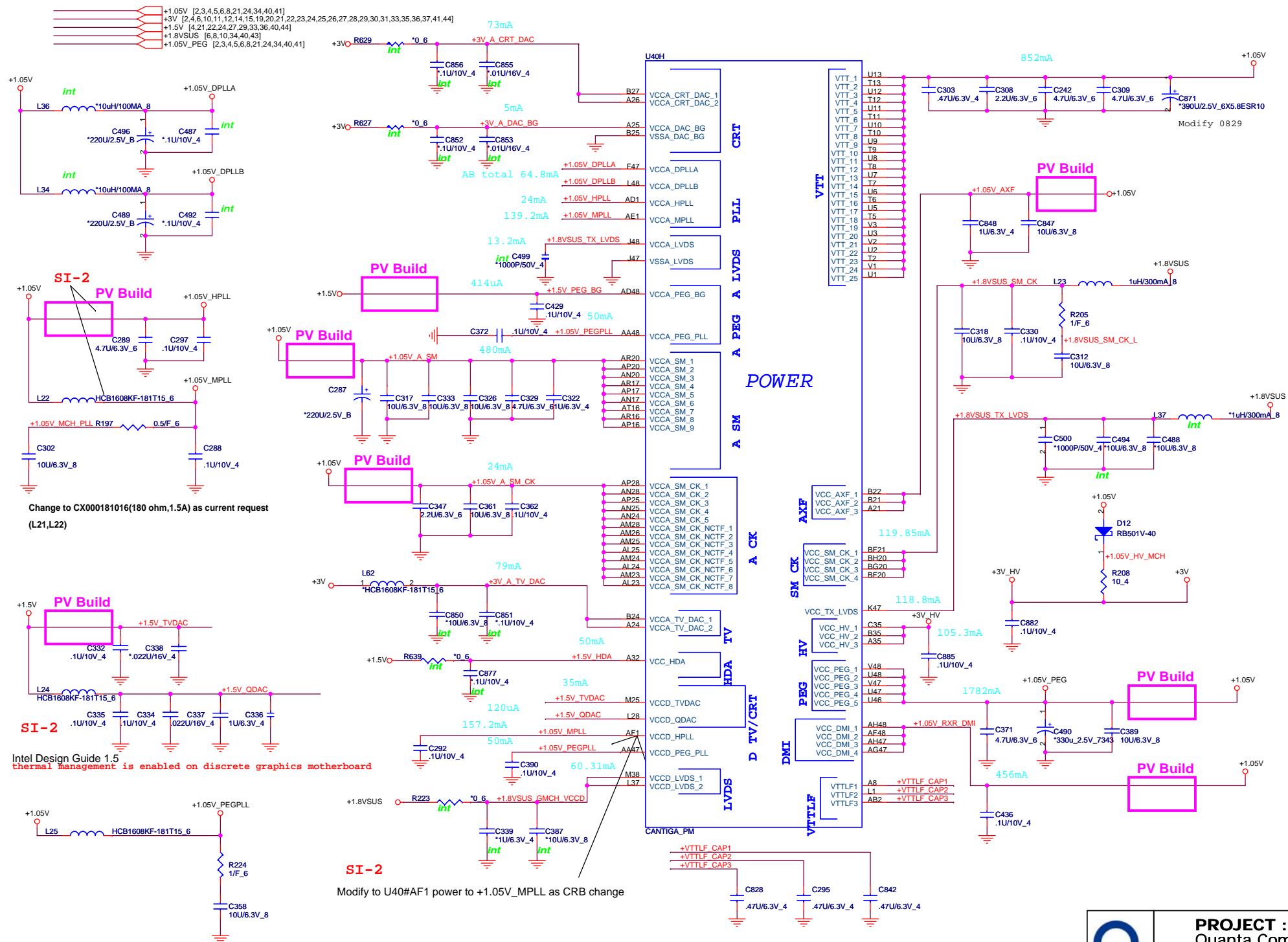






VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desigs.





Change to CX000181016(180 ohm,1.5A) as current request (L21,L22)

Intel Design Guide 1.5 thermal management is enabled on discrete graphics motherboard

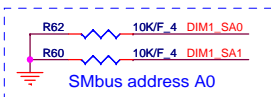
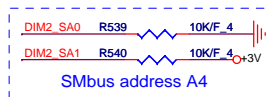
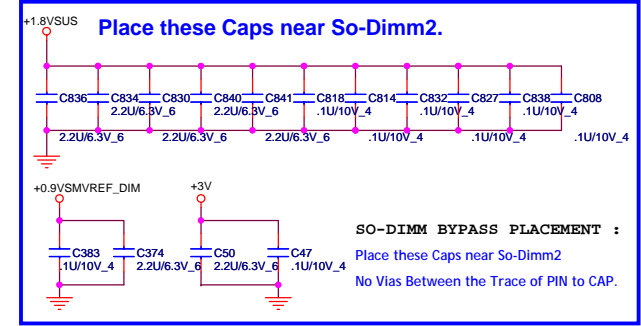
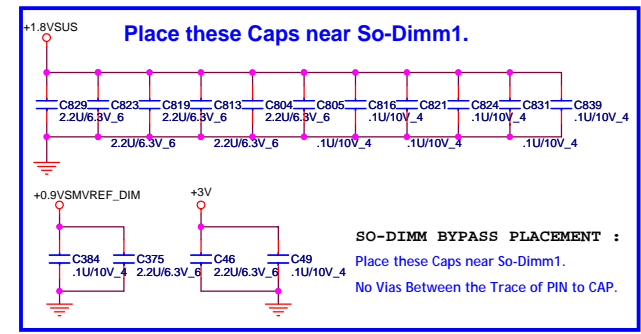
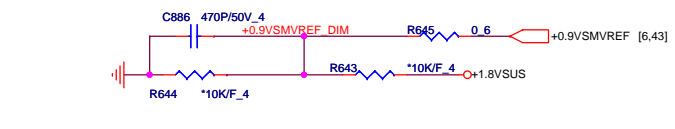
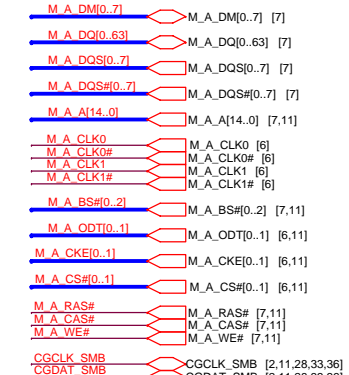
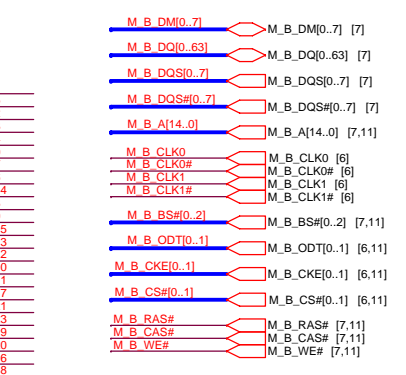
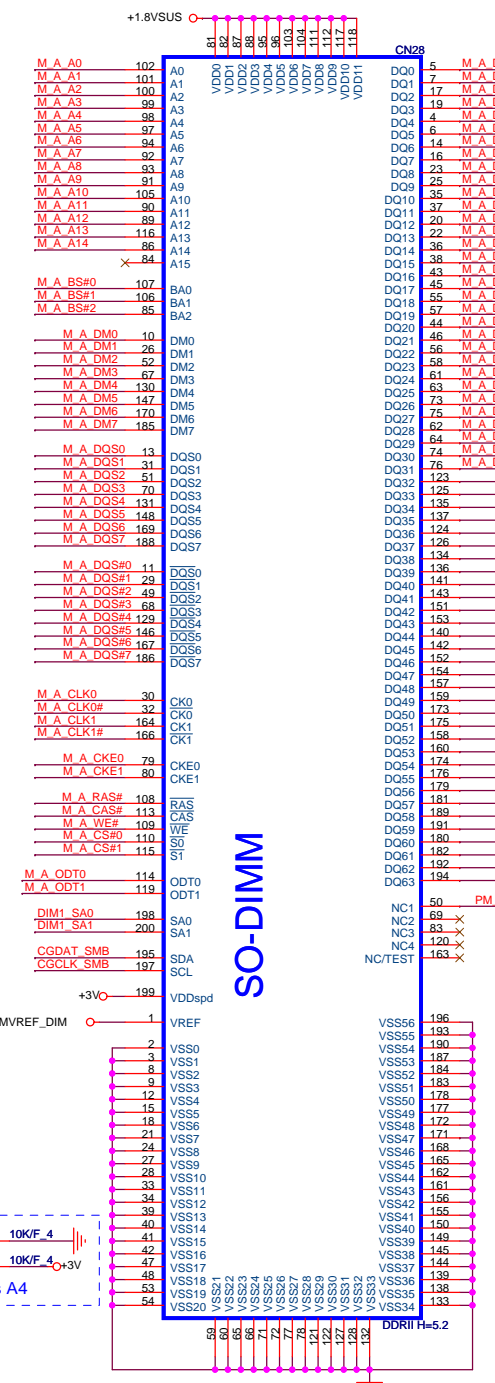
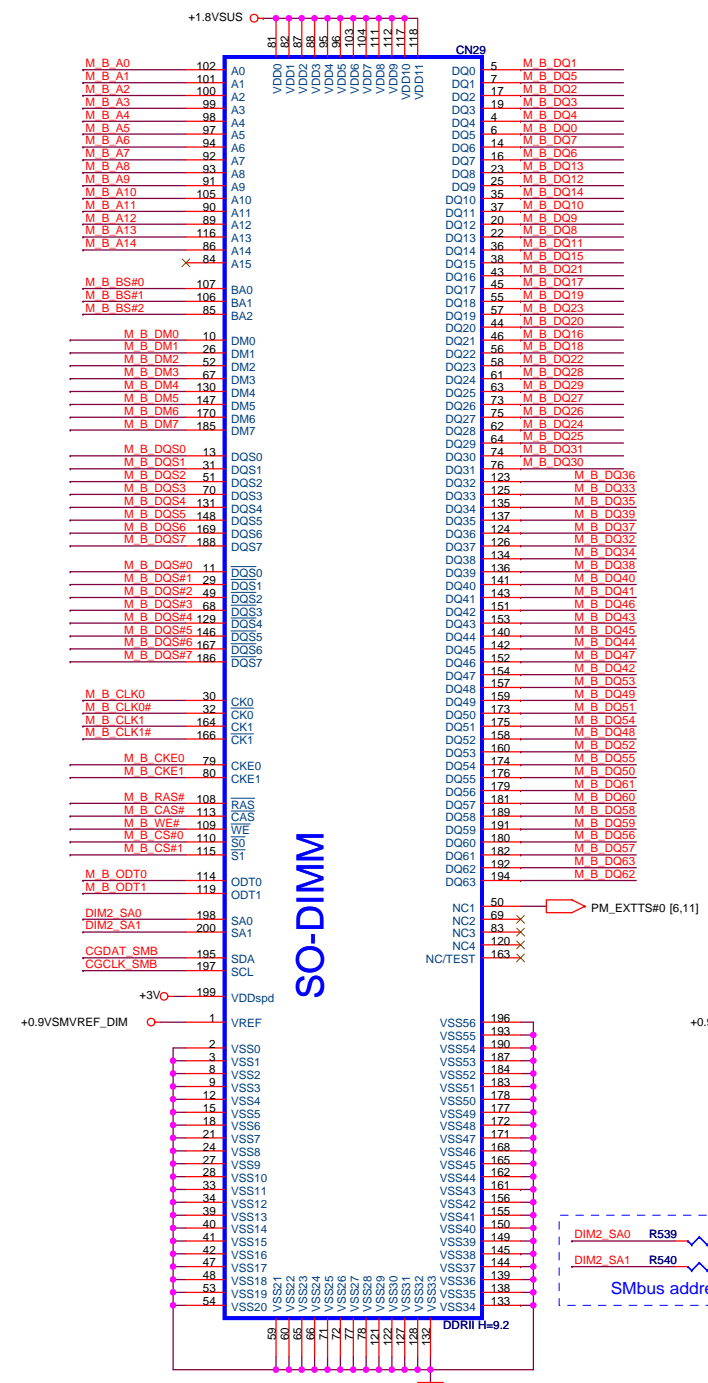
SI-2 Modify to U40#AF1 power to +1.05V_MPLL as CRB change

POWER

NB5

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Cantiga Power 5/5		
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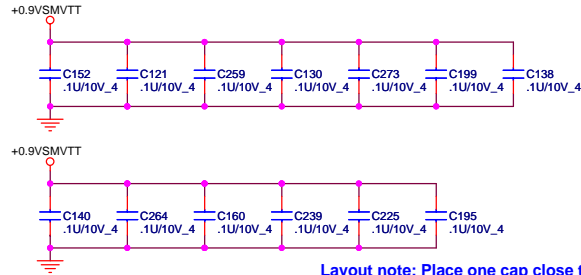
NB5

Size Custom Document Number **DDR2 DIMM** Rev 1A

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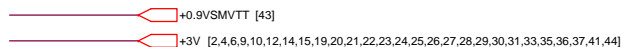
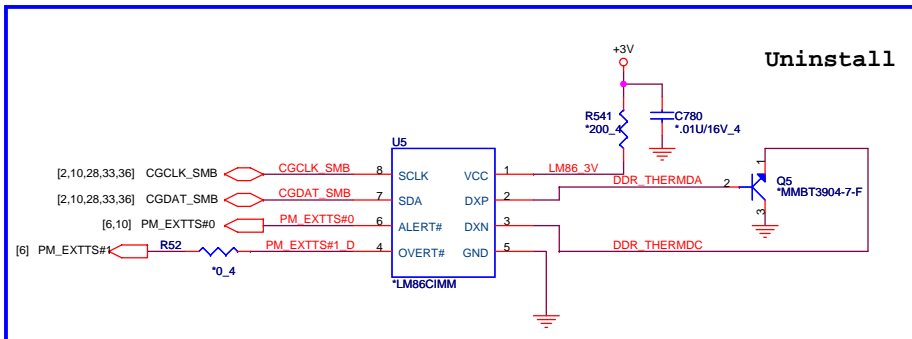
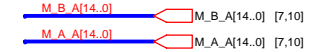
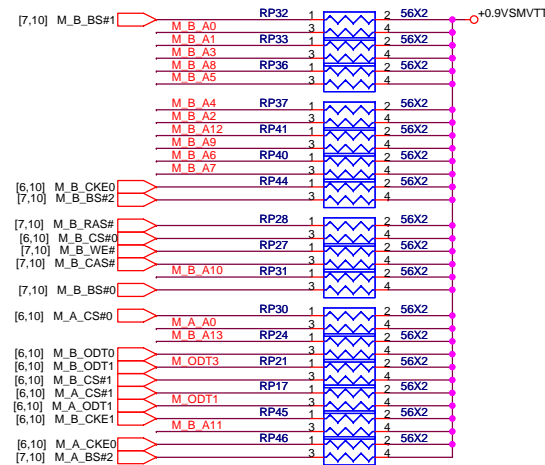
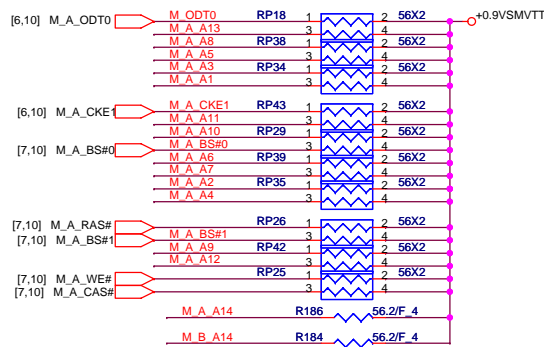
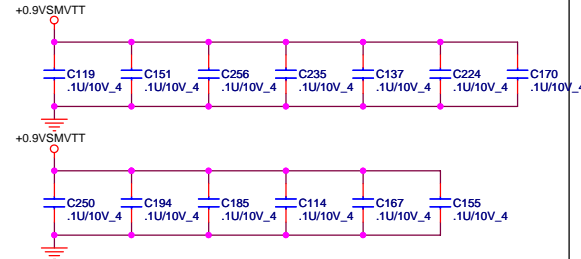
DDRII DUAL CHANNEL A,B.

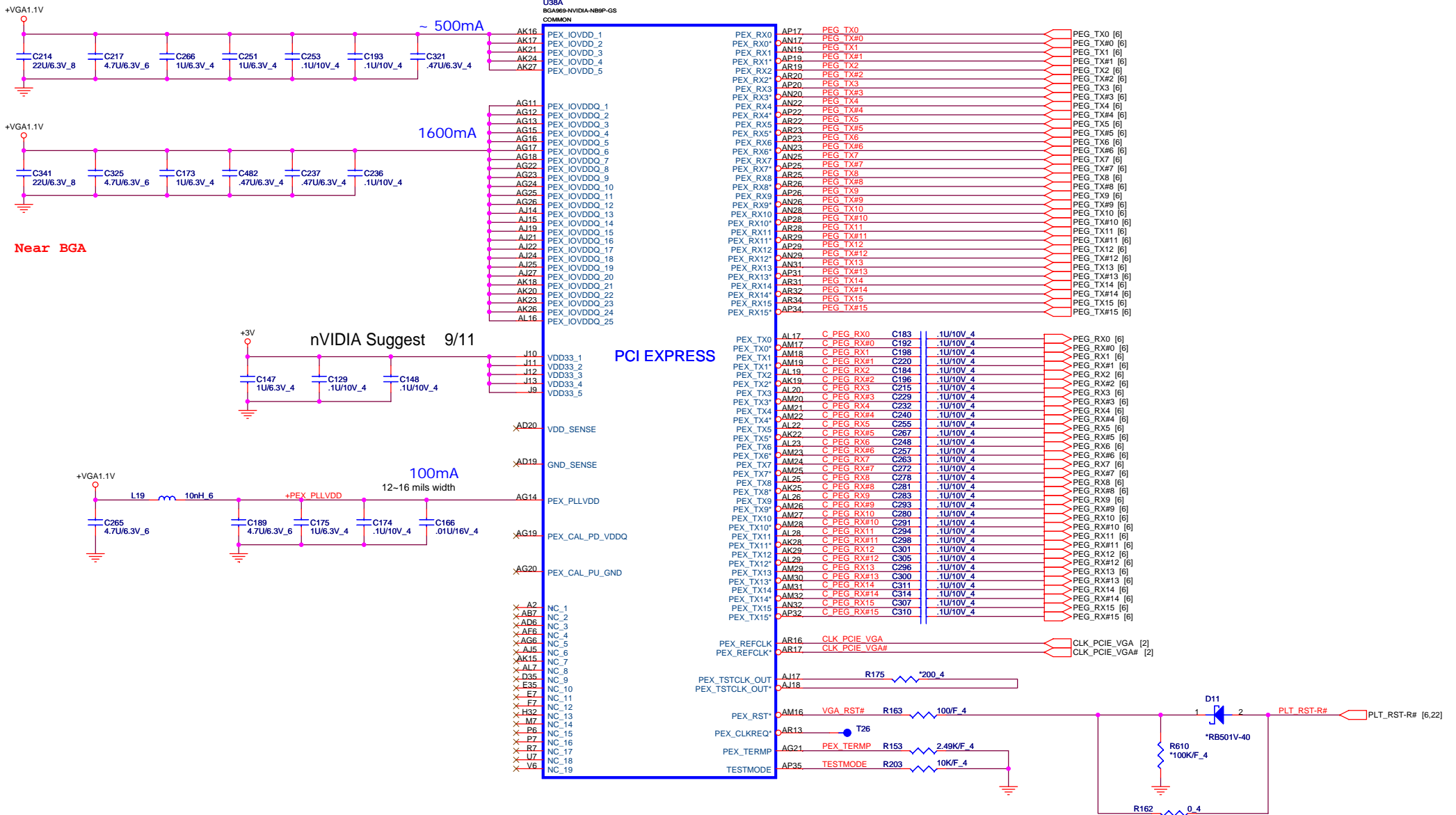
DDRII A CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

DDRII B CHANNEL





U38B
BGAR99-NVIDIA-NB9P-GS
COMMON

[17] VMA_MA3	Y32	FBA_CMD0
[17] VMA_MA0	W31	FBA_CMD1
[17] VMA_MA2	U31	FBA_CMD2
[17] VMA_MA1	Y32	FBA_CMD3
[17] VMA_MA3H	AB35	FBA_CMD4
[17] VMA_MA4H	AB34	FBA_CMD5
[17] VMA_MASH	W35	FBA_CMD6
[17] VMA_CS0#	W33	FBA_CMD7
[17] VMA_WE#	Y30	FBA_CMD8
[17] VMA_BA0	T35	FBA_CMD9
[17] VMA_CKE	AB31	FBA_CMD10
[17] VMA_ODT	X30	FBA_CMD11
[17] VMA_MA2H	Y34	FBA_CMD12
[17] VMA_MA12	W32	FBA_CMD13
[17] VMA_RAS#	AA30	FBA_CMD14
[17] VMA_MA11	AA32	FBA_CMD15
[17] VMA_MA10	Y33	FBA_CMD16
[17] VMA_BA1	U32	FBA_CMD17
[17] VMA_MA8	Y31	FBA_CMD18
[17] VMA_MA5	U34	FBA_CMD19
[17] VMA_MA6	Y35	FBA_CMD20
[17] VMA_MA9	W34	FBA_CMD21
[17] VMA_MA7	Y30	FBA_CMD22
[17] VMA_MA4	U35	FBA_CMD23
[17] VMA_CAS#	U30	FBA_CMD24
	U33	FBA_CMD25
	AB33	FBA_CMD26
	U33	FBA_CMD27
	T33	FBA_CMD28
	W29	FBA_CMD29
	W29	FBA_CMD30

VMA_DM0	P30	FBA_DM0#
VMA_DM1	P32	FBA_DM1#
VMA_DM2	J30	FBA_DM2#
VMA_DM3	H34	FBA_DM3#
VMA_DM4	AF34	FBA_DM4#
VMA_DM5	AF35	FBA_DM5#
VMA_DM6	AL32	FBA_DM6#
VMA_DM7	AL34	FBA_DM7#

VMA_WDQ00	N31	FBA_DQS_WP0
VMA_WDQ01	L34	FBA_DQS_WP1
VMA_WDQ02	J32	FBA_DQS_WP2
VMA_WDQ03	H35	FBA_DQS_WP3
VMA_WDQ04	AE31	FBA_DQS_WP4
VMA_WDQ05	AC33	FBA_DQS_WP5
VMA_WDQ06	AJ32	FBA_DQS_WP6
VMA_WDQ07	AJ34	FBA_DQS_WP7

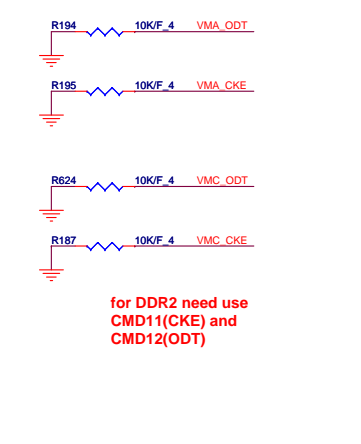
VMA_RDQ00	N32	FBA_DQS_RN0
VMA_RDQ01	L35	FBA_DQS_RN1
VMA_RDQ02	H31	FBA_DQS_RN2
VMA_RDQ03	G35	FBA_DQS_RN3
VMA_RDQ04	AD32	FBA_DQS_RN4
VMA_RDQ05	AC34	FBA_DQS_RN5
VMA_RDQ06	AJ31	FBA_DQS_RN6
VMA_RDQ07	AJ35	FBA_DQS_RN7

MEMORY I/F A

R30	VMA_DQ0
R32	VMA_DQ1
P31	VMA_DQ2
N30	VMA_DQ3
L31	VMA_DQ4
M32	VMA_DQ5
FBA_D4	VMA_DQ6
FBA_D5	VMA_DQ7
FBA_D6	VMA_DQ8
FBA_D7	VMA_DQ9
FBA_D8	VMA_DQ10
FBA_D9	VMA_DQ11
FBA_D10	VMA_DQ12
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FBA_D21	VMA_DQ23
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FBA_D25	VMA_DQ27
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FBA_D27	VMA_DQ29
FBA_D28	VMA_DQ30
FBA_D29	VMA_DQ31
FBA_D30	VMA_DQ32
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FBA_D32	VMA_DQ34
FBA_D33	VMA_DQ35
FBA_D34	VMA_DQ36
FBA_D35	VMA_DQ37
FBA_D36	VMA_DQ38
FBA_D37	VMA_DQ39
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FBA_D45	VMA_DQ47
FBA_D46	VMA_DQ48
FBA_D47	VMA_DQ49
FBA_D48	VMA_DQ50
FBA_D49	VMA_DQ51
FBA_D50	VMA_DQ52
FBA_D51	VMA_DQ53
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FBA_D55	VMA_DQ57
FBA_D56	VMA_DQ58
FBA_D57	VMA_DQ59
FBA_D58	VMA_DQ60
FBA_D59	VMA_DQ61
FBA_D60	VMA_DQ62
FBA_D61	VMA_DQ63
FBA_D62	VMA_DQ64
FBA_D63	VMA_DQ65

MEMORY I/F B

[17] VMA_DQ[63..0]	R194	VMA_ODT
[17] VMA_DM[7..0]	R195	VMA_CKE
[17] VMA_WDQS[7..0]	R624	VMC_ODT
[17] VMA_RDQS[7..0]	R187	VMC_CKE



U38C
BGAR99-NVIDIA-NB9P-GS
COMMON

C12	FBC_CMD0
B19	FBC_CMD1
D18	FBC_CMD2
F21	FBC_CMD3
D21	FBC_CMD4
B23	FBC_CMD5
X20	FBC_CMD7
C21	FBC_CMD8
F20	FBC_CMD9
F19	FBC_CMD10
F23	FBC_CMD11
A22	FBC_CMD12
C22	FBC_CMD13
B17	FBC_CMD14
F24	FBC_CMD15
C28	FBC_CMD16
E22	FBC_CMD17
C20	FBC_CMD18
B22	FBC_CMD19
A19	FBC_CMD20
D22	FBC_CMD21
D20	FBC_CMD22
E18	FBC_CMD23
F18	FBC_CMD24
F18	FBC_CMD25
FBC_CMD26	F18
FBC_CMD27	X19
FBC_CMD28	X20
FBC_CMD29	X20
FBC_CMD30	X20

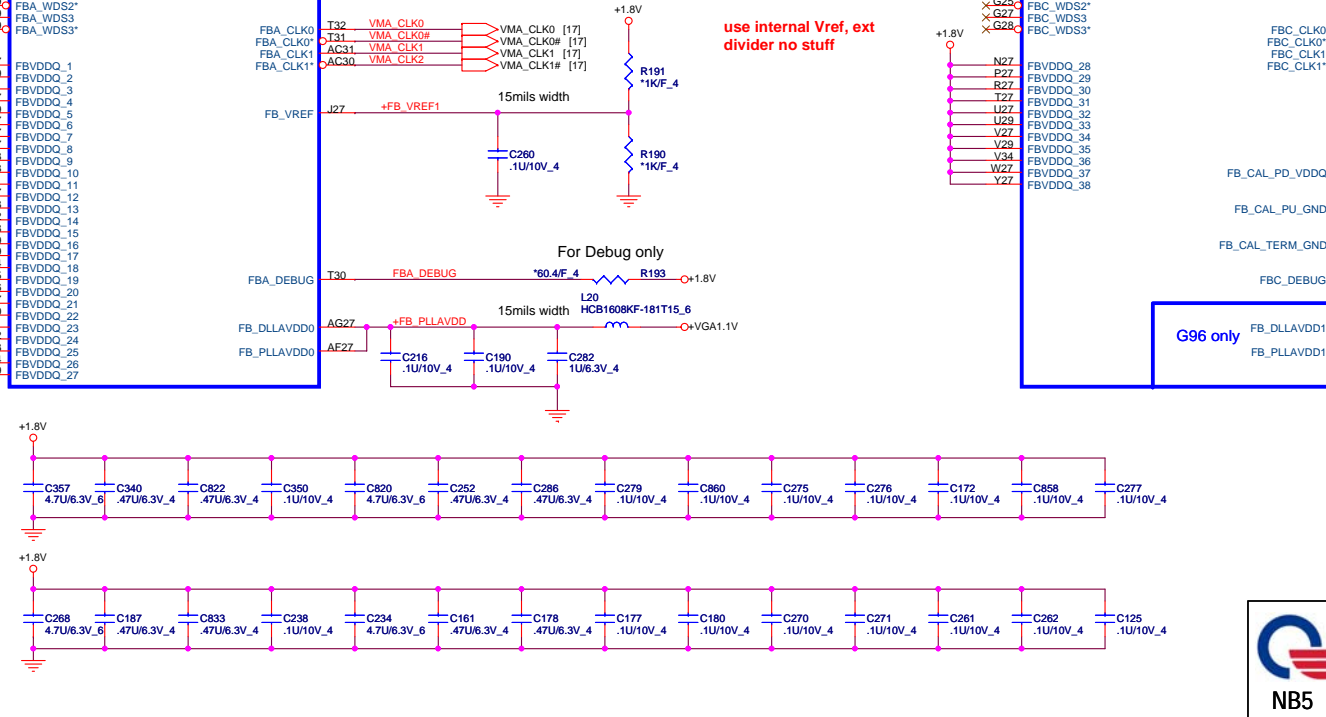
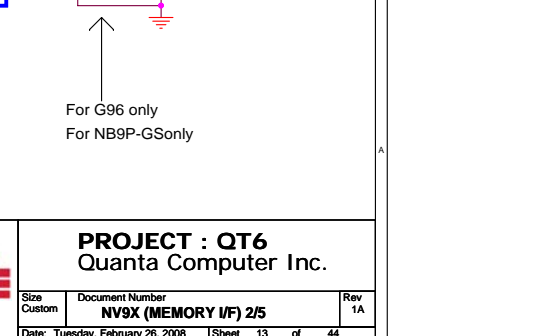
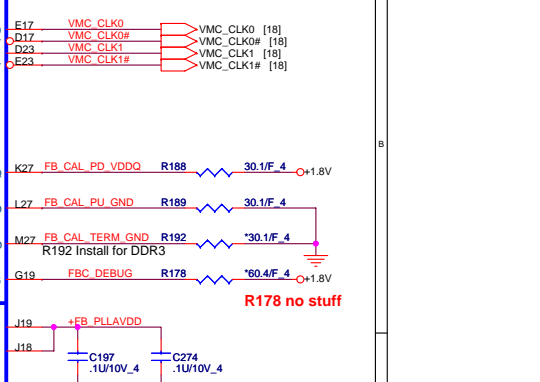
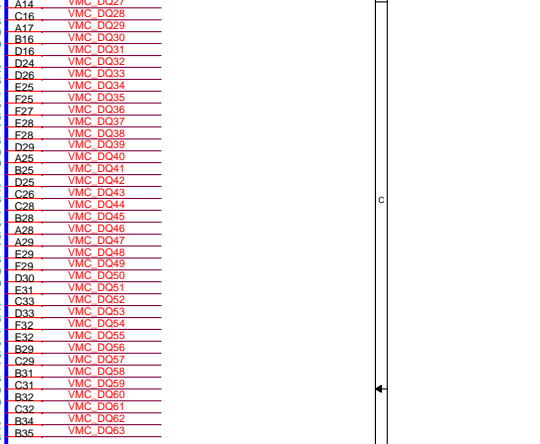
VMC_DM0	F11	FBC_DM0#
VMC_DM1	D10	FBC_DM1#
VMC_DM2	D15	FBC_DM2#
VMC_DM3	A16	FBC_DM3#
VMC_DM4	A16	FBC_DM4#
VMC_DM5	D28	FBC_DM5#
VMC_DM6	D34	FBC_DM6#
VMC_DM7	A34	FBC_DM7#

VMC_WDQ00	E10	FBC_DQS_WP0
VMC_WDQ01	A10	FBC_DQS_WP1
VMC_WDQ02	D14	FBC_DQS_WP2
VMC_WDQ03	C18	FBC_DQS_WP3
VMC_WDQ04	E26	FBC_DQS_WP4
VMC_WDQ05	B26	FBC_DQS_WP5
VMC_WDQ06	D32	FBC_DQS_WP6
VMC_WDQ07	A32	FBC_DQS_WP7

VMC_RDQ00	D9	FBC_DQS_RN0
VMC_RDQ01	B10	FBC_DQS_RN1
VMC_RDQ02	F18	FBC_DQS_RN2
VMC_RDQ03	B14	FBC_DQS_RN3
VMC_RDQ04	F26	FBC_DQS_RN4
VMC_RDQ05	A26	FBC_DQS_RN5
VMC_RDQ06	D31	FBC_DQS_RN6
VMC_RDQ07	A31	FBC_DQS_RN7

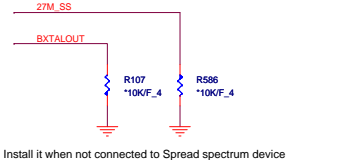
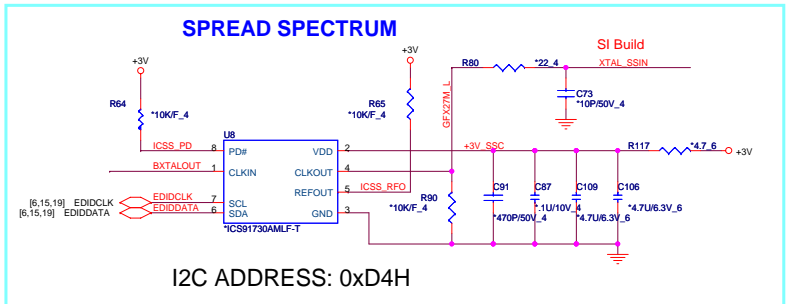
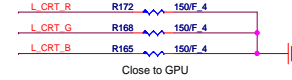
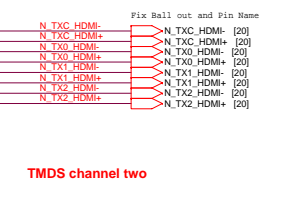
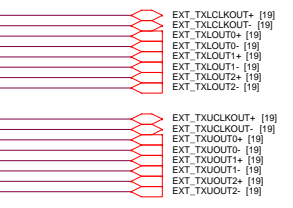
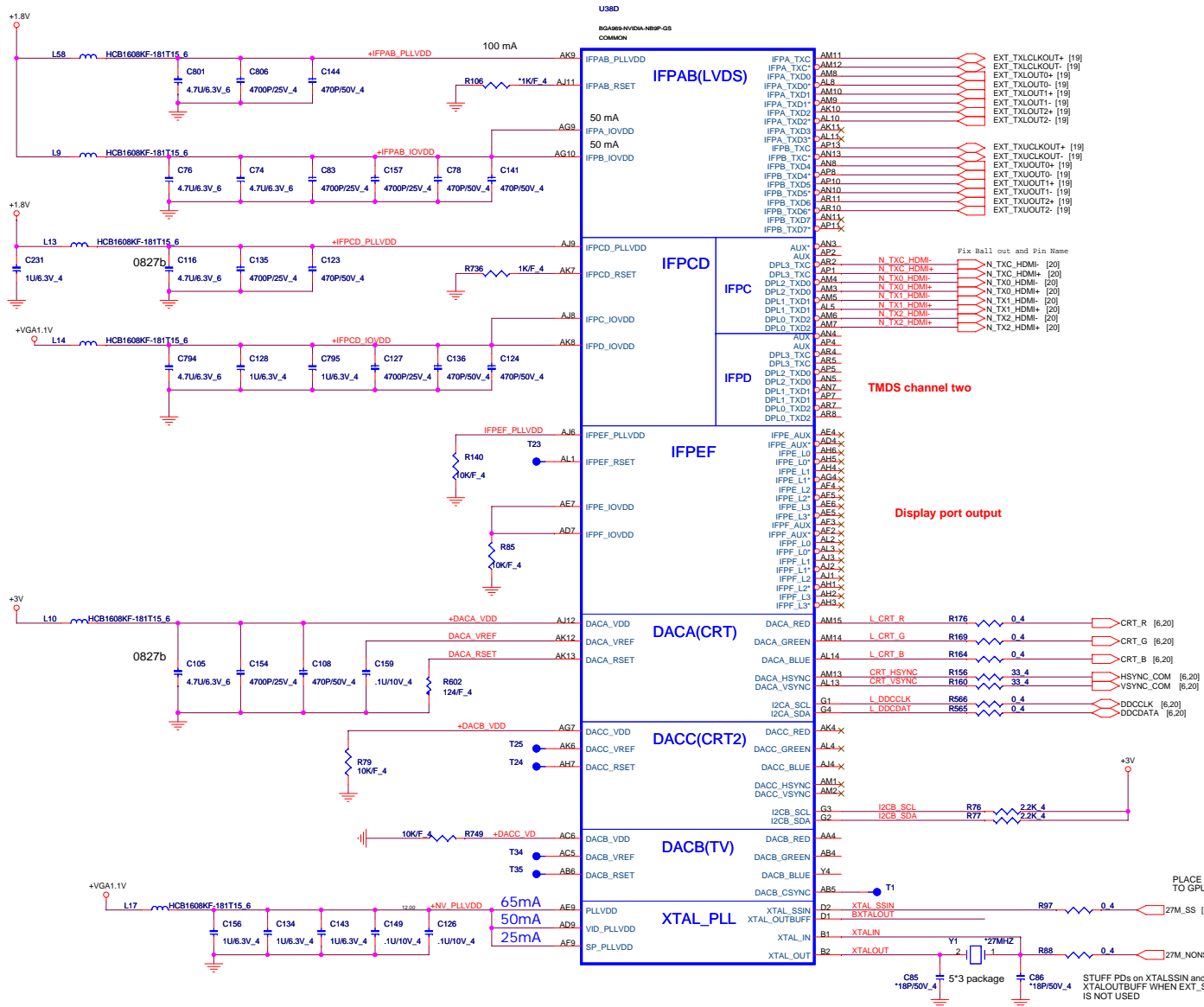
MEMORY I/F C

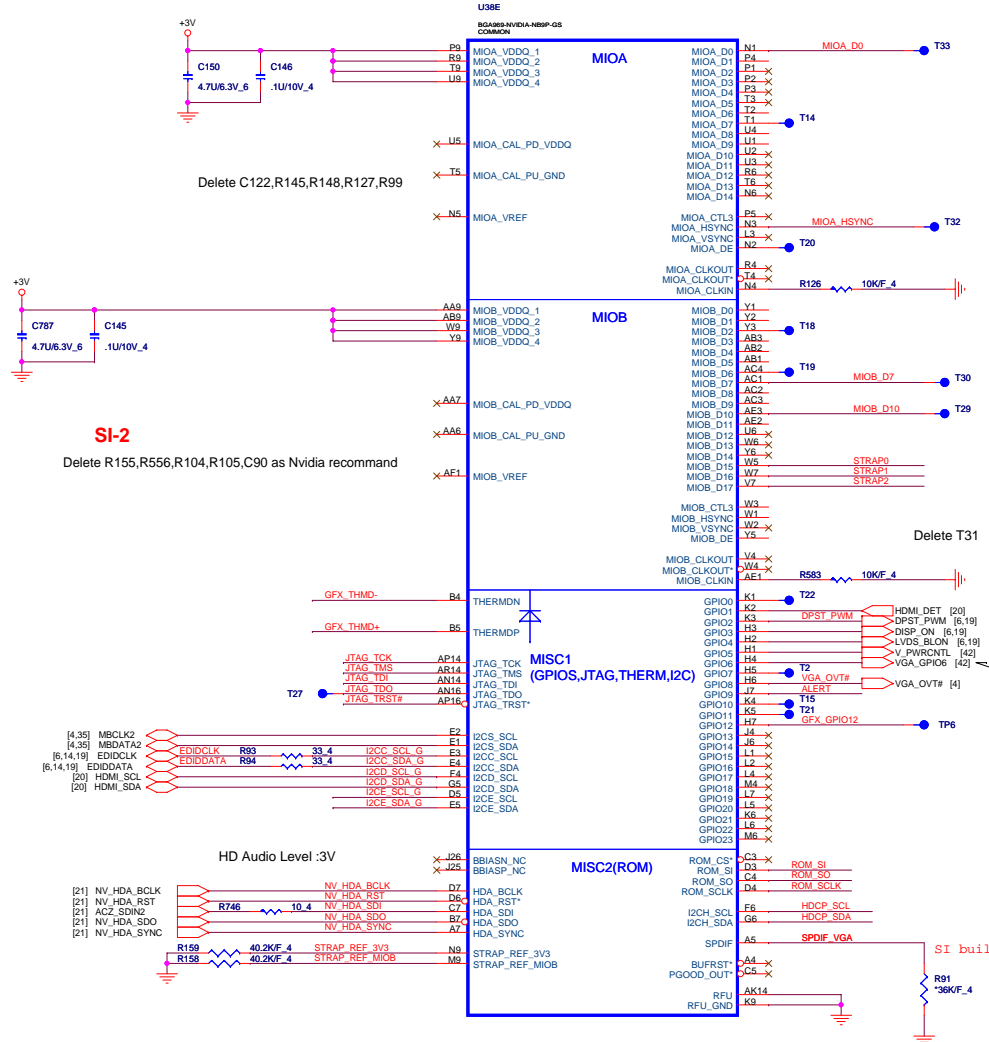
D11	VMC_DQ0
E11	VMC_DQ1
F10	VMC_DQ2
D8	VMC_DQ3
F8	VMC_DQ4
E9	VMC_DQ5
F8	VMC_DQ6
F12	VMC_DQ7
B11	VMC_DQ8
C11	VMC_DQ9
A11	VMC_DQ10
B8	VMC_DQ11
A8	VMC_DQ12
C8	VMC_DQ13
C11	VMC_DQ14
D12	VMC_DQ15
C10	VMC_DQ16
D12	VMC_DQ17
E13	VMC_DQ18
F17	VMC_DQ19
F15	VMC_DQ20
F16	VMC_DQ21
E16	VMC_DQ22
F14	VMC_DQ23
F13	VMC_DQ24
D13	VMC_DQ25
A13	VMC_DQ26
B13	VMC_DQ27
A14	VMC_DQ28
C16	VMC_DQ29
A17	VMC_DQ30
B16	VMC_DQ31
D16	VMC_DQ32
D24	VMC_DQ33
D26	VMC_DQ34
E25	VMC_DQ35
F25	VMC_DQ36
F25	VMC_DQ37
E28	VMC_DQ38
F28	VMC_DQ39
D29	VMC_DQ40
A25	VMC_DQ41
B25	VMC_DQ42
D25	VMC_DQ43
C26	VMC_DQ44
A26	VMC_DQ45
B28	VMC_DQ46
A28	VMC_DQ47
A29	VMC_DQ48
F29	VMC_DQ49
F29	VMC_DQ50
D30	VMC_DQ51
E31	VMC_DQ52
F31	VMC_DQ53
D33	VMC_DQ54
F32	VMC_DQ55
E32	VMC_DQ56
B29	VMC_DQ57
C29	VMC_DQ58
B31	VMC_DQ59
C31	VMC_DQ60
C32	VMC_DQ61
B34	VMC_DQ62
B35	VMC_DQ63



PROJECT : QT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (MEMORY I/F) 2/5	1A
Date:	Tuesday, February 26, 2008	Sheet 13 of 44





NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

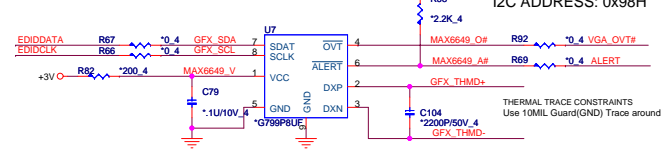
GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NV_VDD VID0
6	OUT	N/A	NV_VDD VID1
7	OUT	N/A	FB_VDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

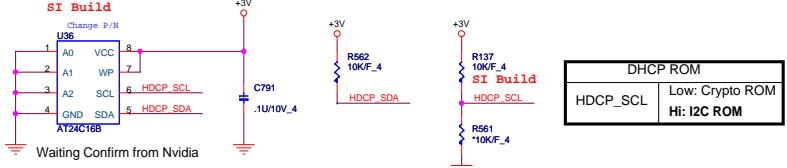
VGA THERMAL CIRCUIT



NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
0110	DDR2 32Mx16x8, 128bit, 512MB	Gilmonda
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
other	Reserved	

HDCP ROM



PCI_DEVID: STRAP2 R554

NB9M-GE 0x06E 8 1000 PU 5K
 NB9M-GS 0x06E 9 1001 PU 10K
 NB9P-GE2 0x064 8 1000 PU 5K
 NB9P-GS 0x064 9 1001 PU 10K

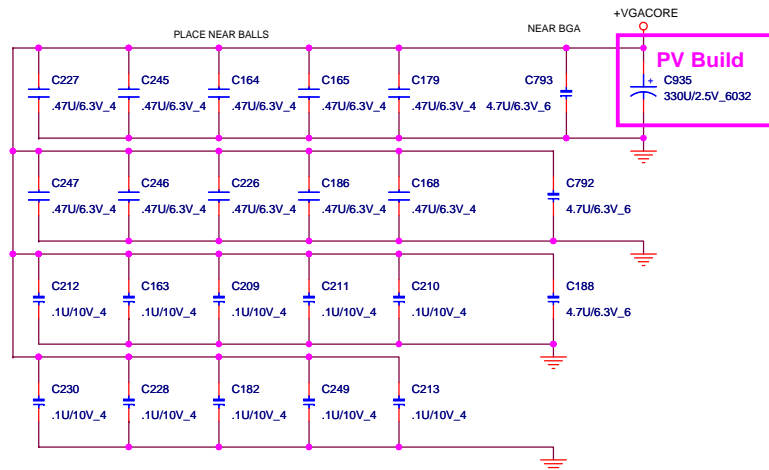
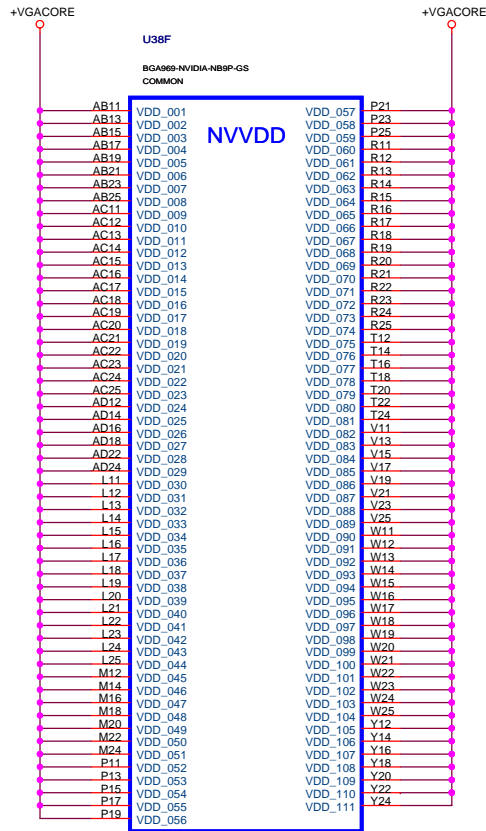
CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)
 CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

RAM ID: ROM_SI R585
 SAM 0101 PD 30.1K
 QIM 0110 PD 35.7K
 HYN 0111 PD 45.3K

PROJECT : QT6
Quanta Computer Inc.

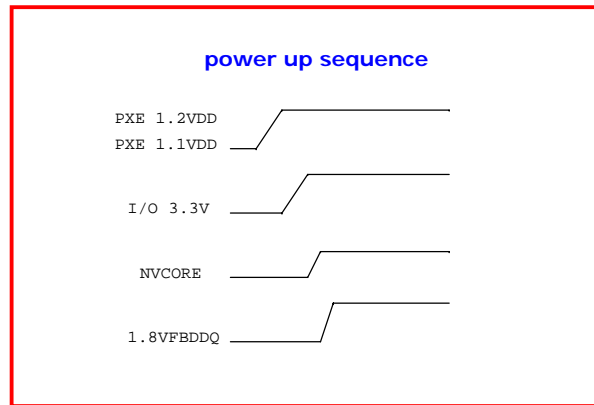
Size C Document Number **NV9X (GPIO & STRAPS) 4/5** Rev 28
 Date: Tuesday, February 26, 2008 1 Sheet 15 of 44

NVVDD Decoupling



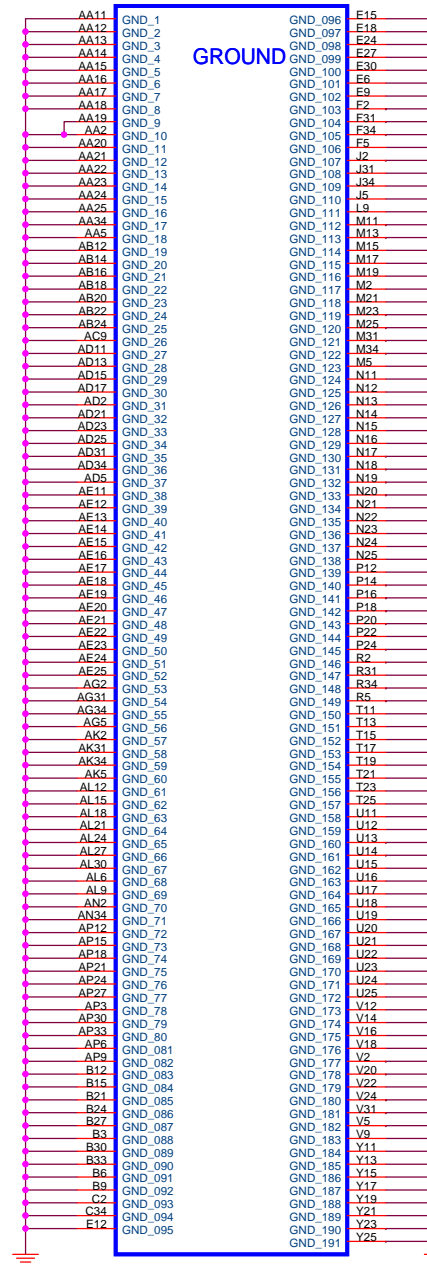
Follow Design Guide DG-03276-001 4.7uF x3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V



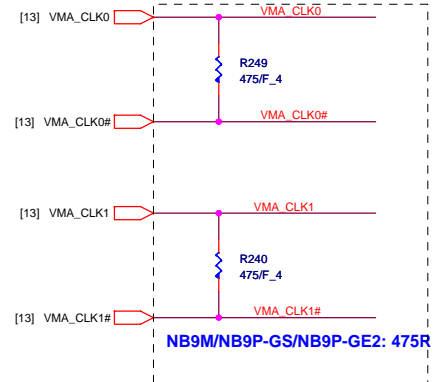
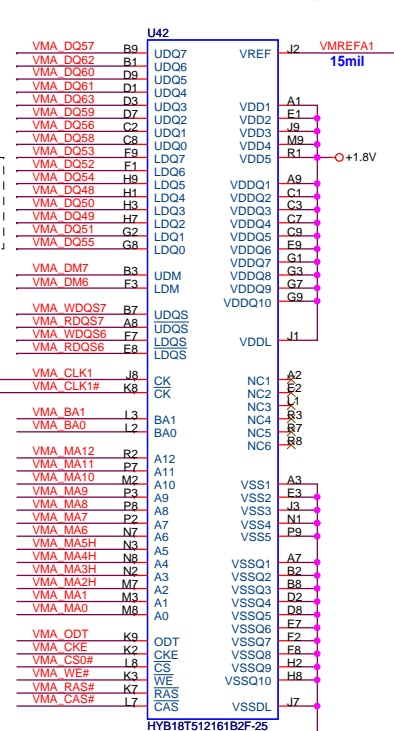
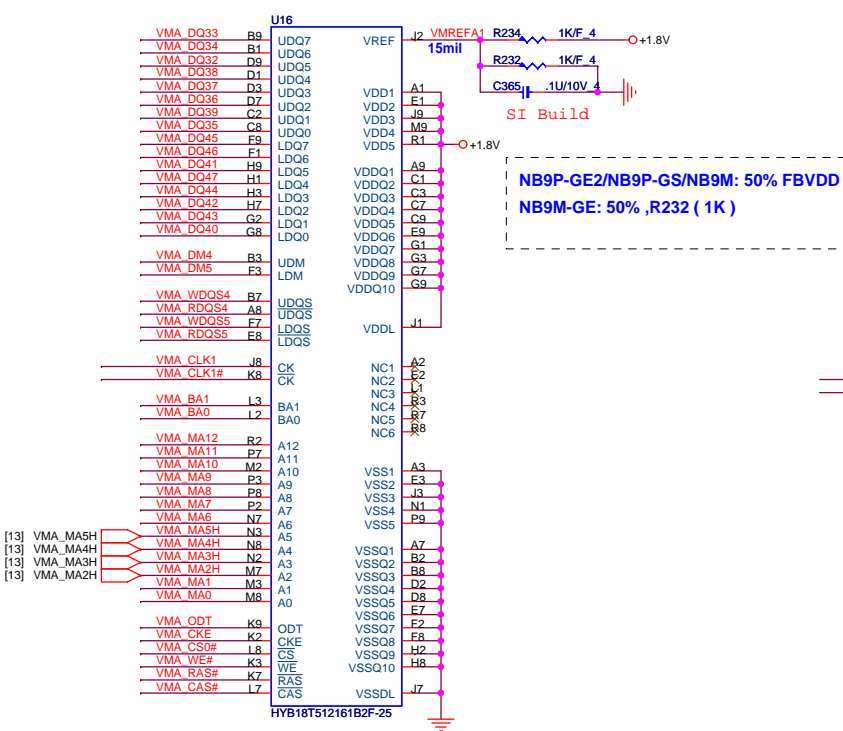
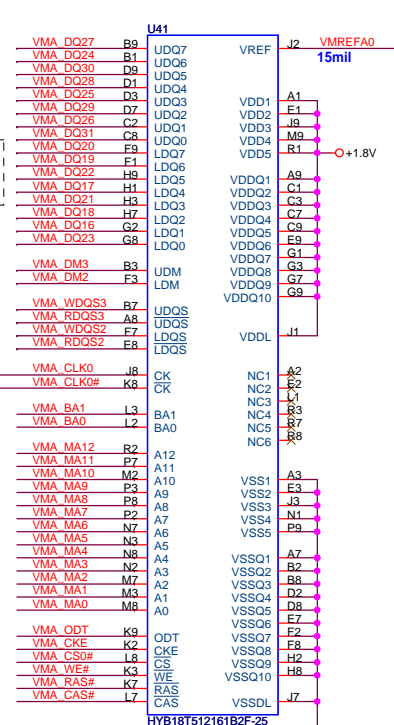
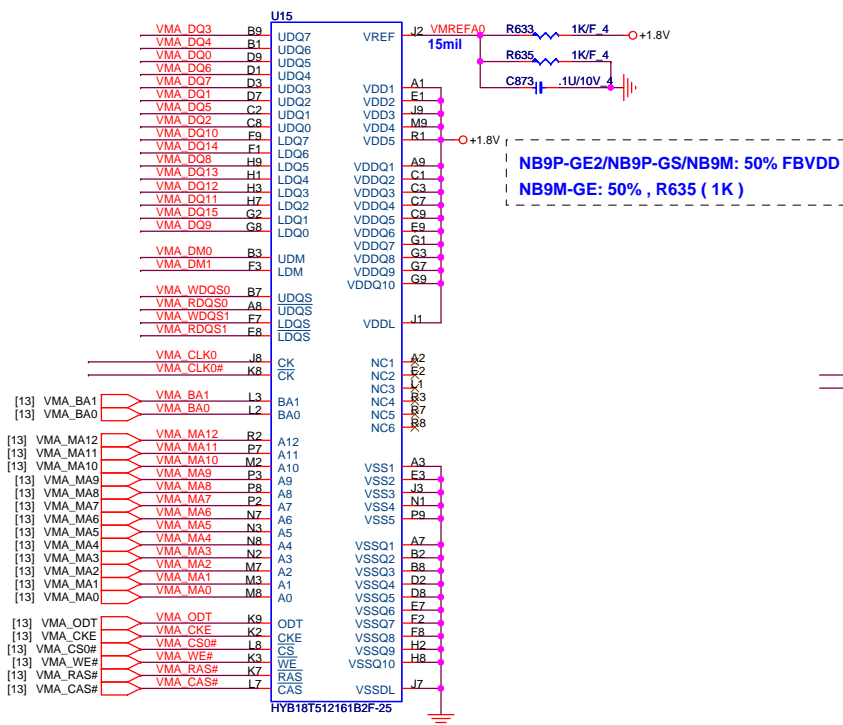
U38G

BGA969-NVIDIA-NB9P-GS
COMMON



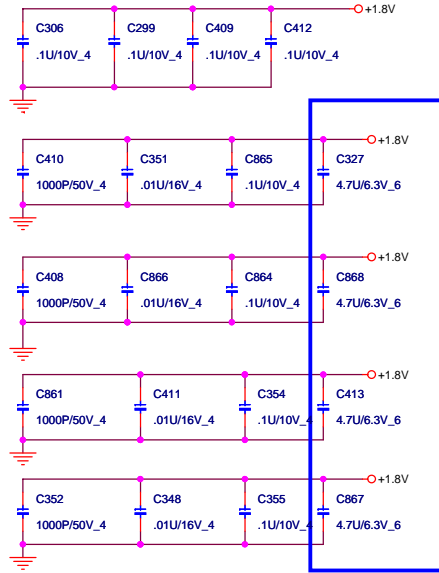
PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number NV9X (POWER & GND) 5/5	Rev 1A
Date: Tuesday, February 26, 2008		Sheet 16 of 44



CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

(By pass capacitor)



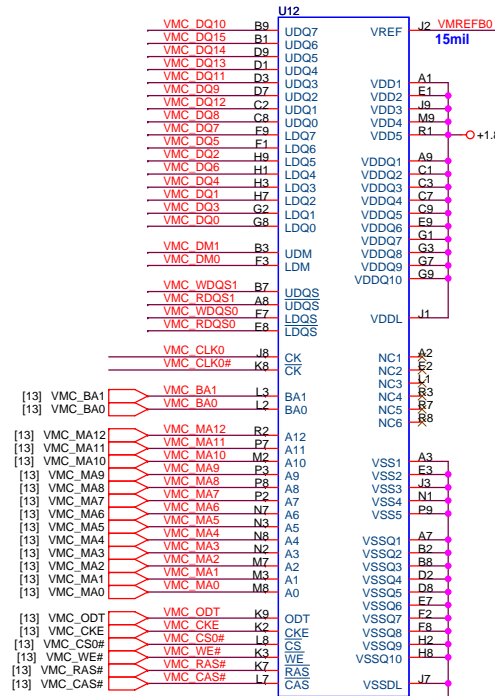
For DB:
 NB9P : AKD59G-T502(Samsung,32M*16)
 NB9M : AKD5FG-TW31(Hynix,32M*16)
 AKD5FG-T*03(Qimonda 32M*16)

- [13] VMA_DQ[63..0]
- [13] VMA_DM[7..0]
- [13] VMA_WDQS[7..0]
- [13] VMA_RDQS[7..0]

256Mb : AKD5JGAT*05
 512Mb : AKD59G-T*01

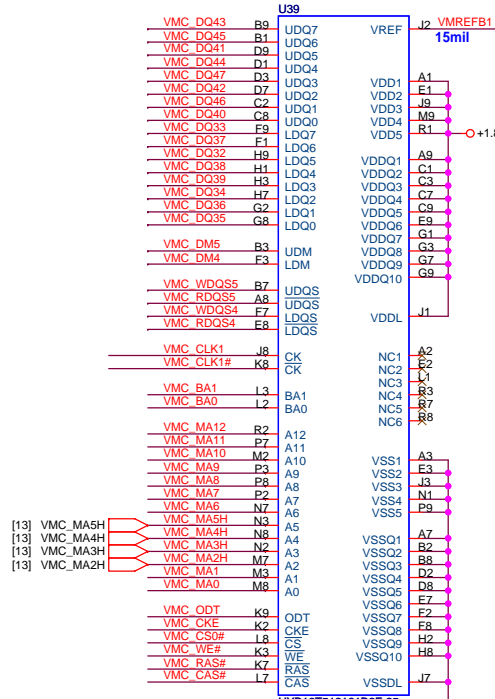
PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number NV9X VRAM-1(GDDR2 BGA84)	Rev 1A
Date: Tuesday, February 26, 2008 Sheet 17 of 44		

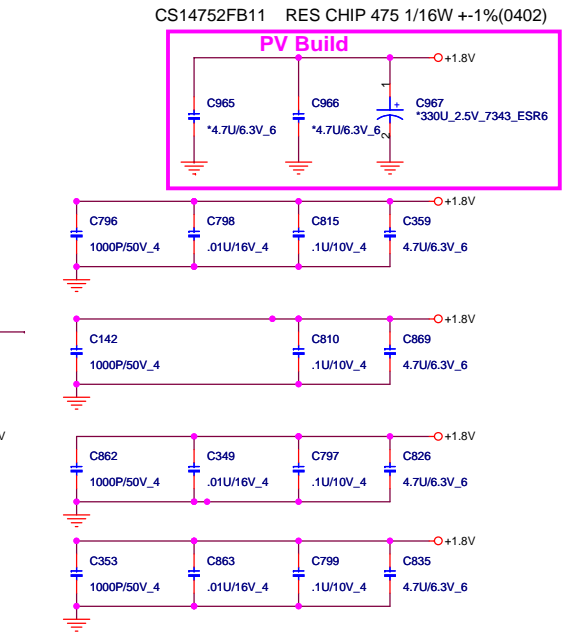
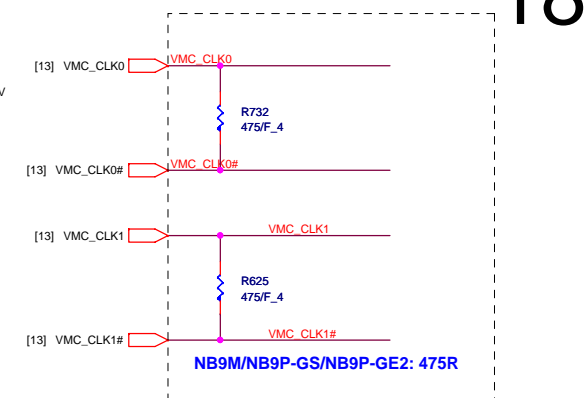
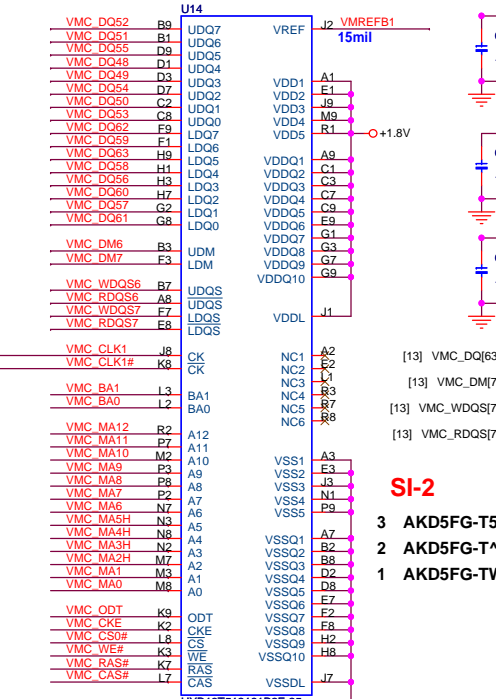
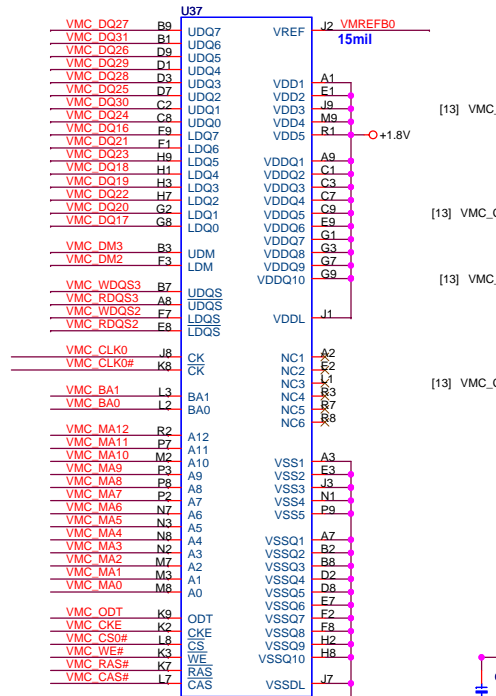


NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE:50%, R133(1K)

NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R632(1K)



VRAM Vendor
NB9M-GE 1 3
NB9P-GS 2



- [13] VMC_DQ[63..0]
- [13] VMC_DM[7..0]
- [13] VMC_WDQS[7..0]
- [13] VMC_RDQS[7..0]

SI-2

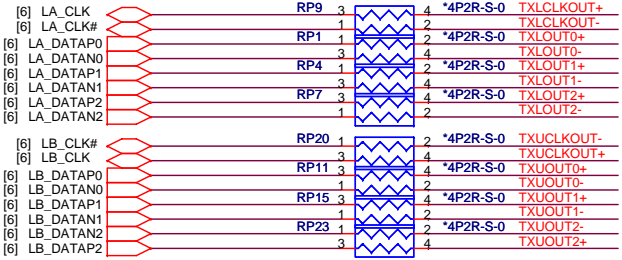
- 3 AKD5FG-T501 IC SDRAM(84P) K4N51163QG-HC25(FBGA) Samsung
- 2 AKD5FG-T*03 IC SDRAM(84P)HYB18T512161B2F-25(FBGA) Qimonda
- 1 AKD5FG-TW31 IC SDRAM(84P) HY5PS121621CFP-25(FBGA) Hynix

PROJECT : QT6
Quanta Computer Inc.

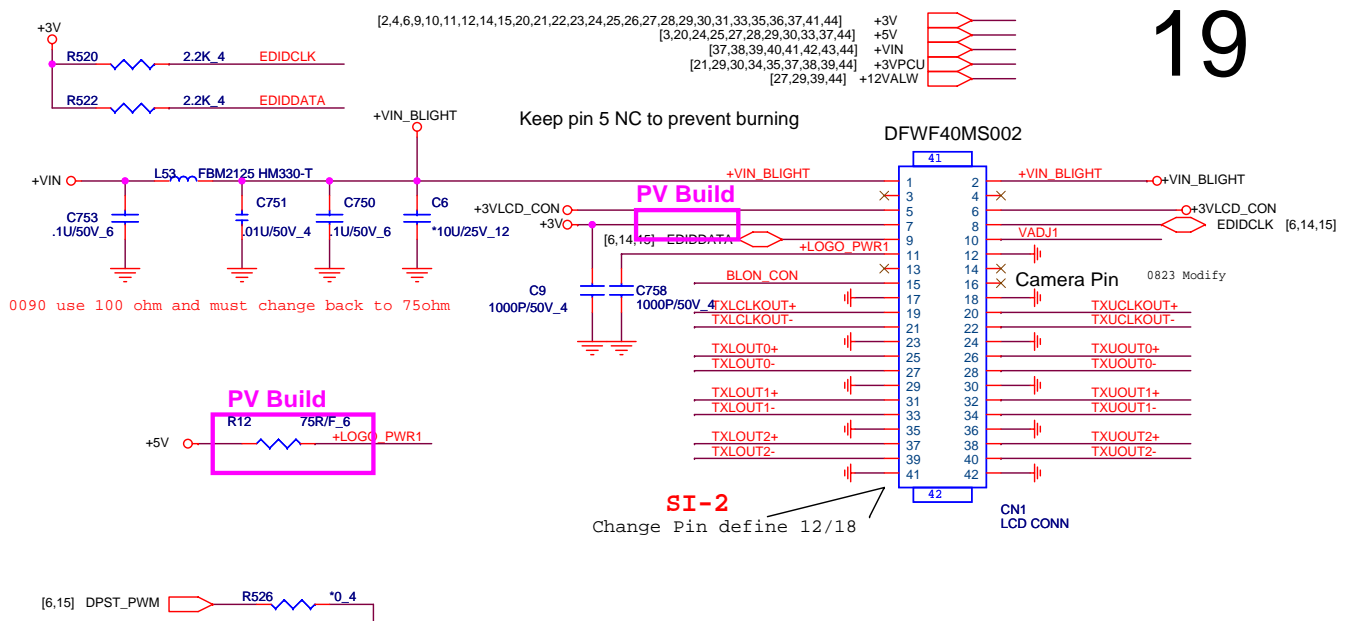
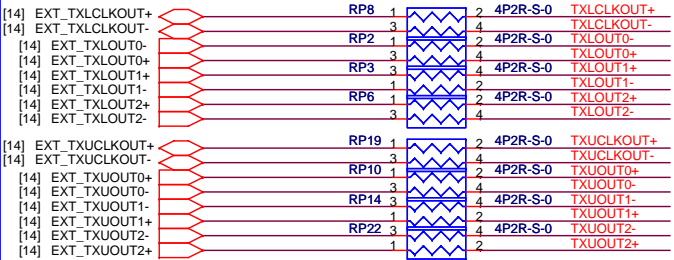
Size Custom	Document Number NV9X VRAM-2(GDDR2 BGA84)	Rev 1A
Date: Tuesday, February 26, 2008 Sheet 18 of 44		

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

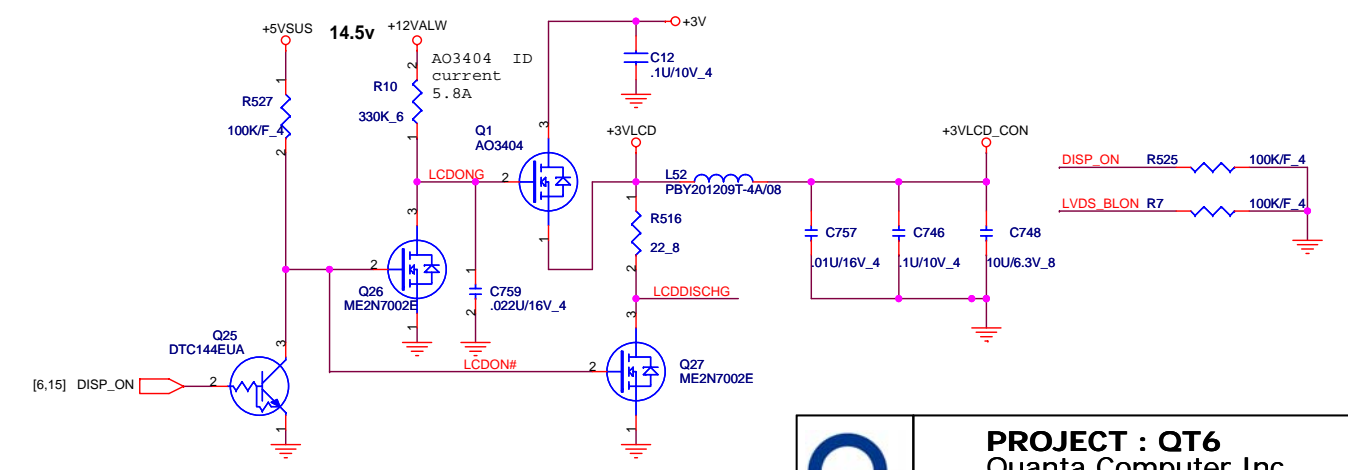
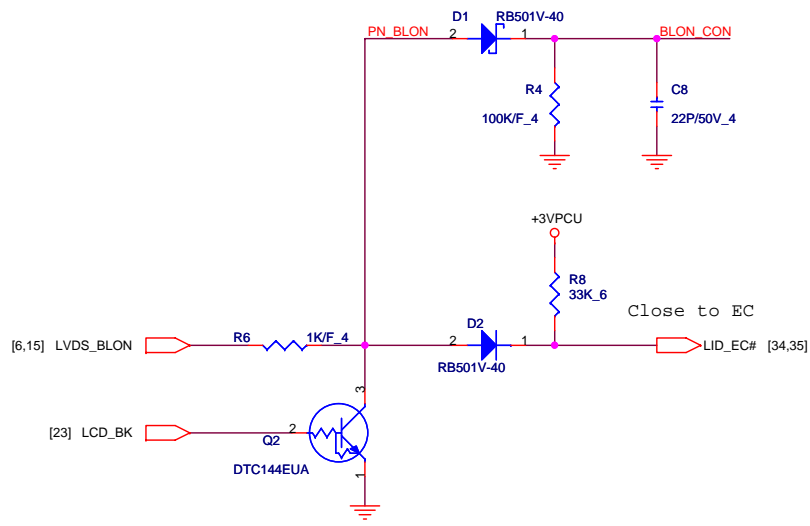
OPTION SIGNAL FROM NB FOR UMA VGA



OPTION SIGNAL FROM Nvidia to VGA

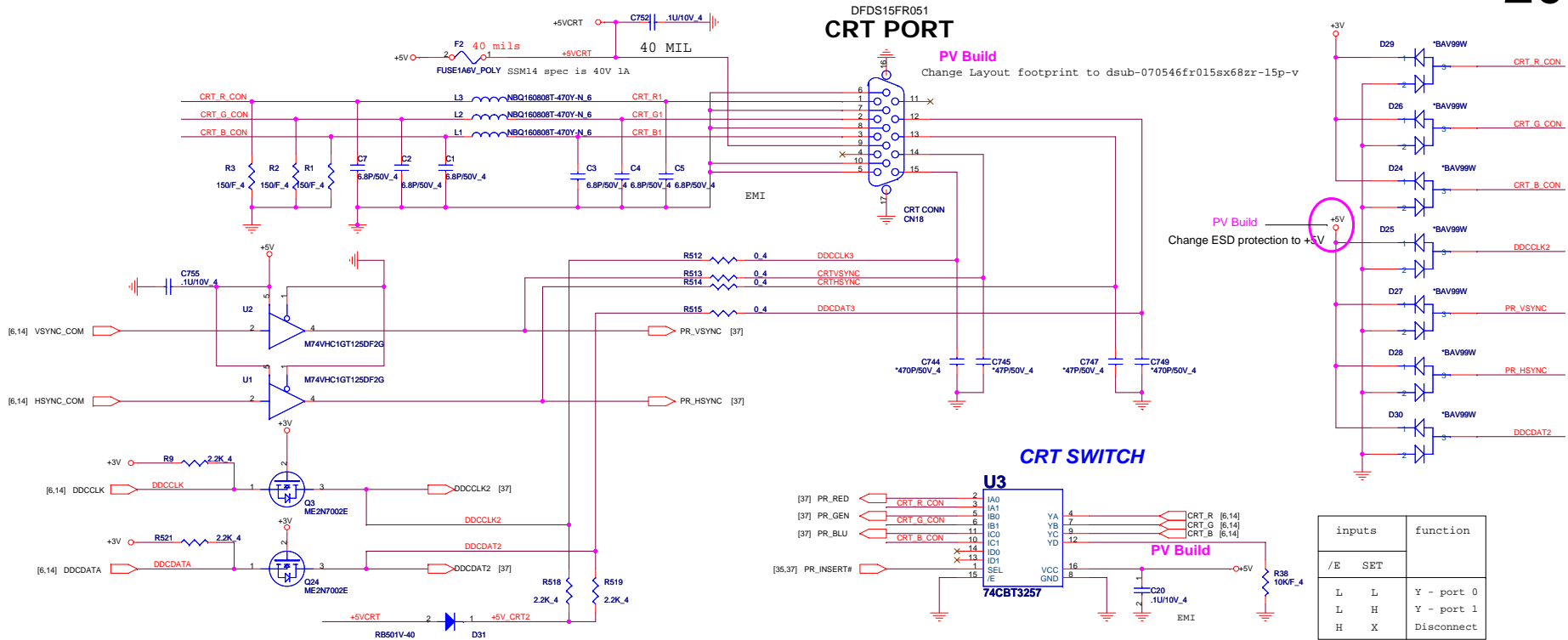


PV Build
Delete CN20,R63,C761(Remove Logo light2)

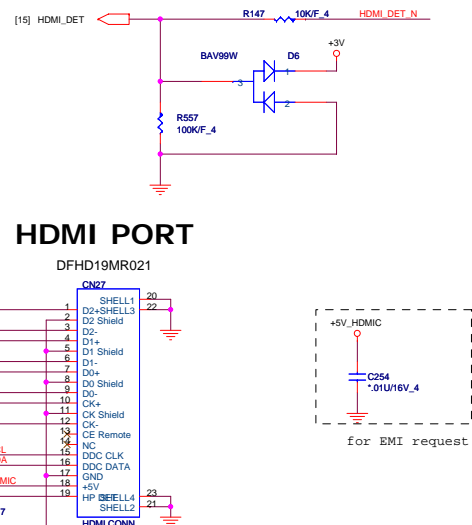
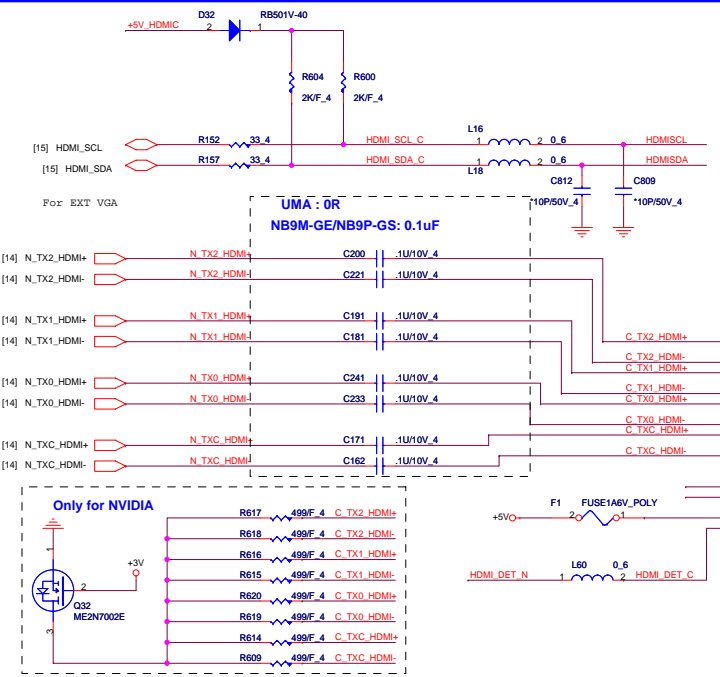
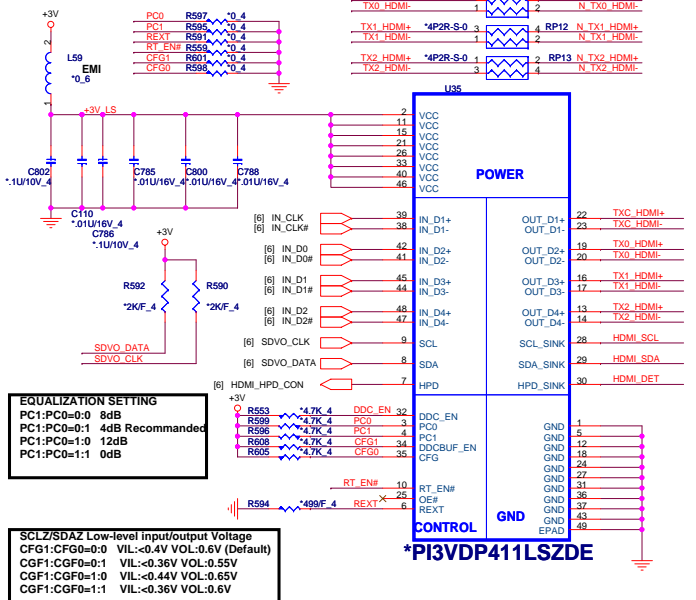


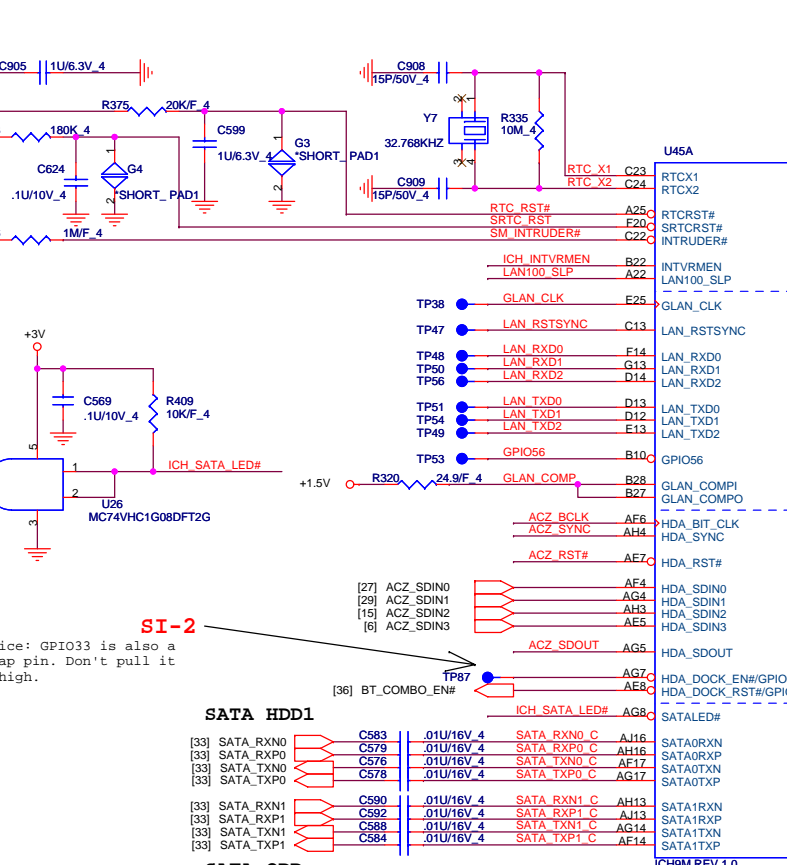
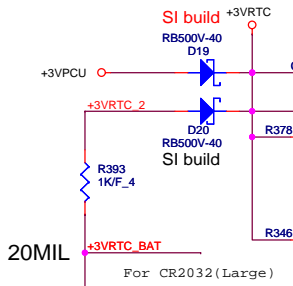
PROJECT : QT6
Quanta Computer Inc.

Size B	Document Number LCD CONN/Lid function	Rev 3A
Date: Tuesday, February 26, 2008 Sheet 19 of 44		



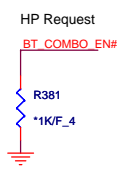
For UMA HDMI function





SI-2

Notice: GPIO33 is also a strap pin. Don't pull it to high.

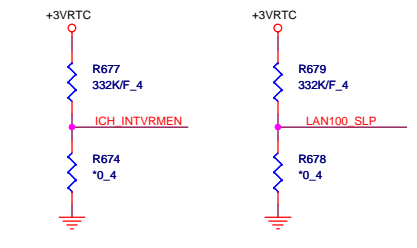


SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for Vccs1_05, VccsSus1_5 and VccCL1_5)

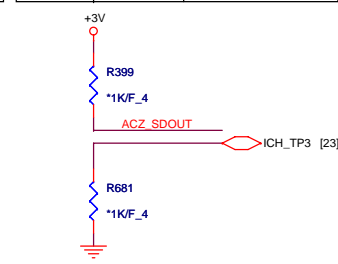
ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1



ICH9 Boot BIOS select

STRAP PCI_GNT0# SPI_CS#1

SPI	0	1
PCI	1	0
LPC	1	1

(default)



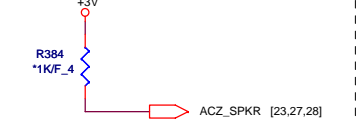
A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default
-----------	---



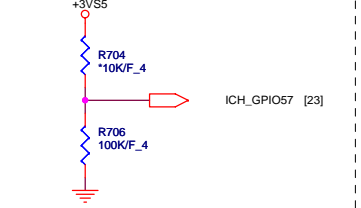
No Reboot Strap

ACZ_SPKR	Low: Default Hi: No reboot
----------	-------------------------------

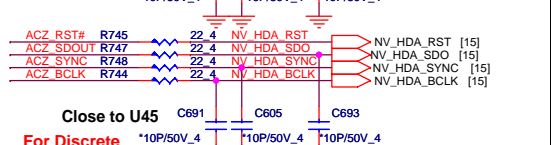
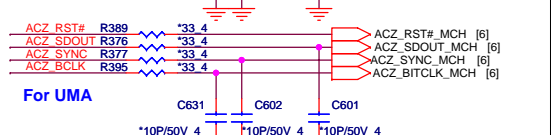
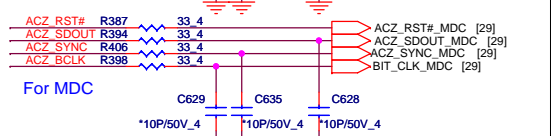
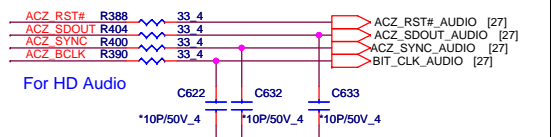


TPM physical presence

ICH_GPIO57	Low: Default
------------	--------------



E-SATA CONNECT



Close to U45

PROJECT : QT6
Quanta Computer Inc.

Size Custom Document Number ICH9-M Host 1/4 Rev 2B

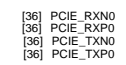
Date: Tuesday, February 26, 2008 Sheet 21 of 44

SWAP PCIE PORT6 TO PORT2 (Lan and New card swap) -->Rename the port name by function and port

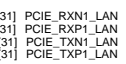
[4,9,21,24,27,29,33,36,40,44] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +3V
[23,25,30,36,40,41,42,44] +3VSUS



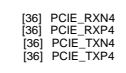
MINI CARD PCI-E(WLAN)



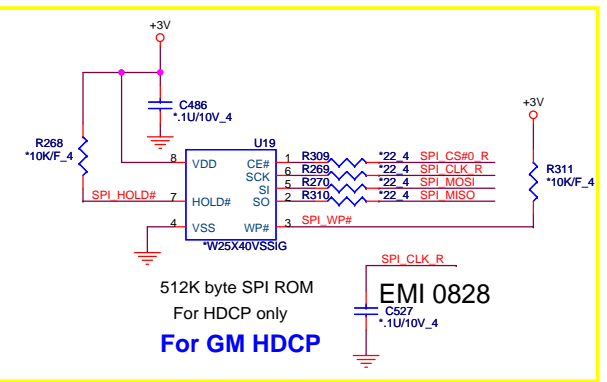
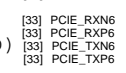
SI-2
PCIE-LAN



TV CARD PCI-E

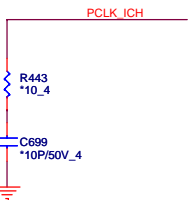


SI-2
EXPRESS CARD (NEW CARD)

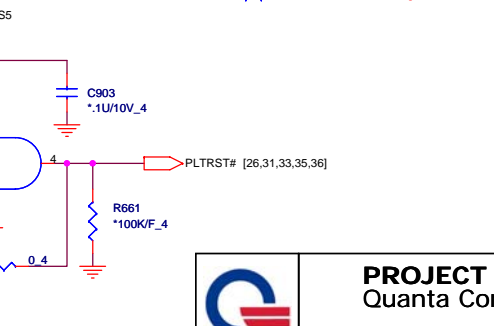
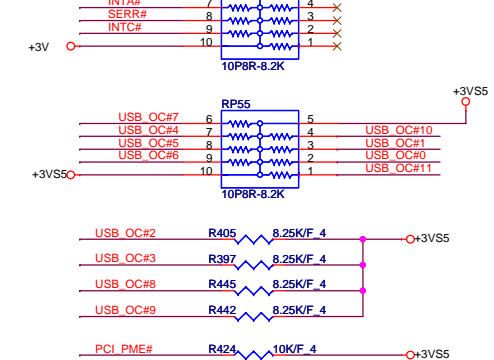
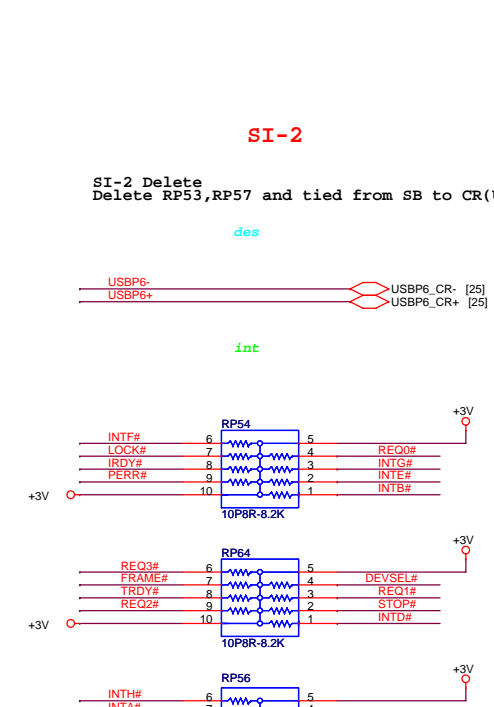
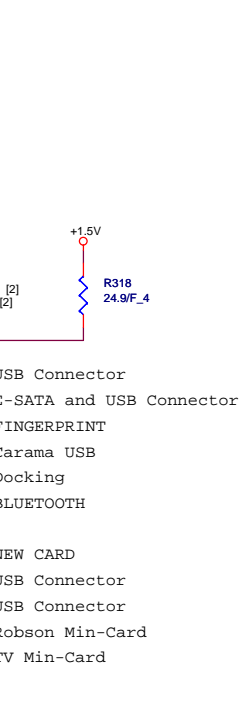
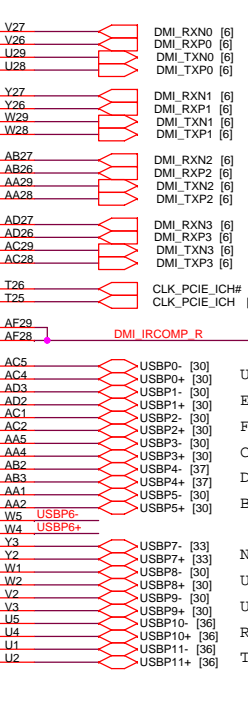
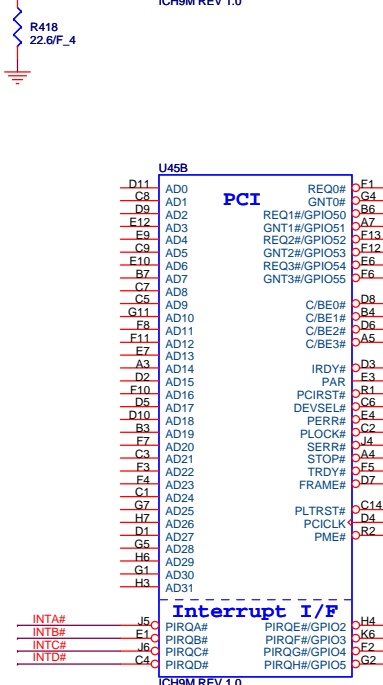
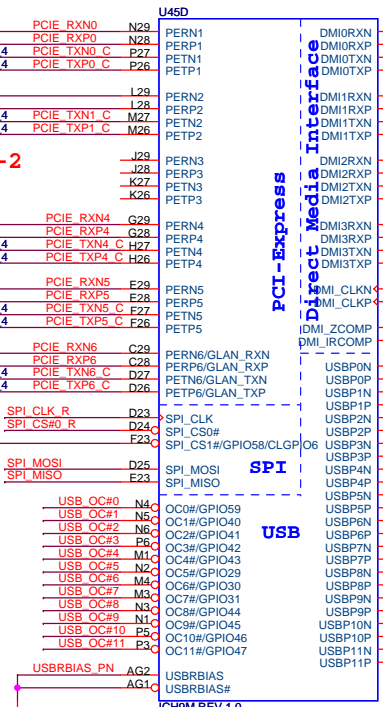


EMI 0828
C527
.1U/10V_4

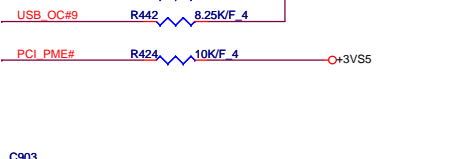
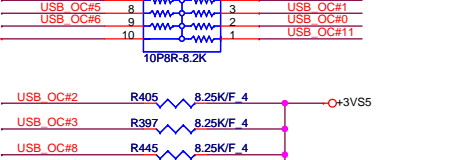
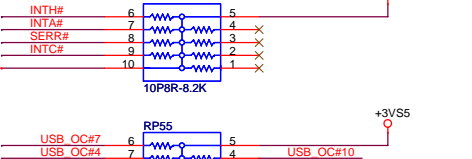
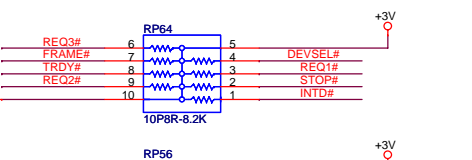
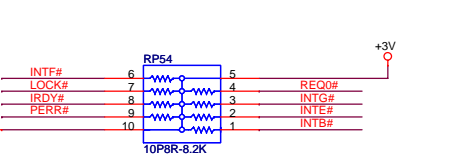
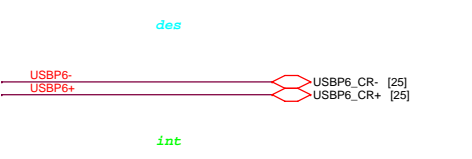
PV Build



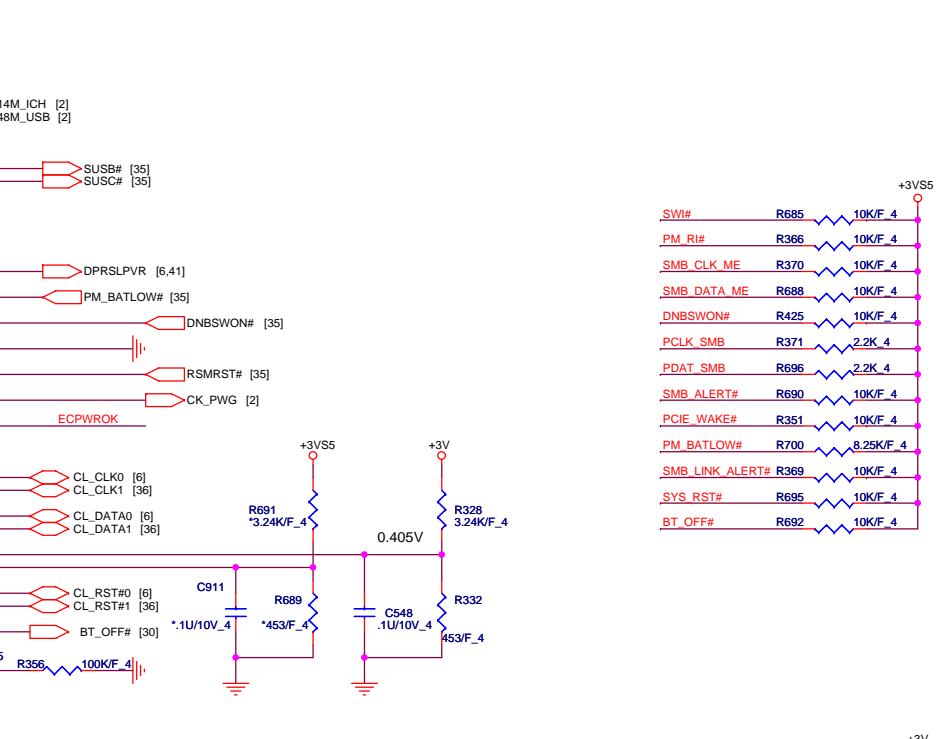
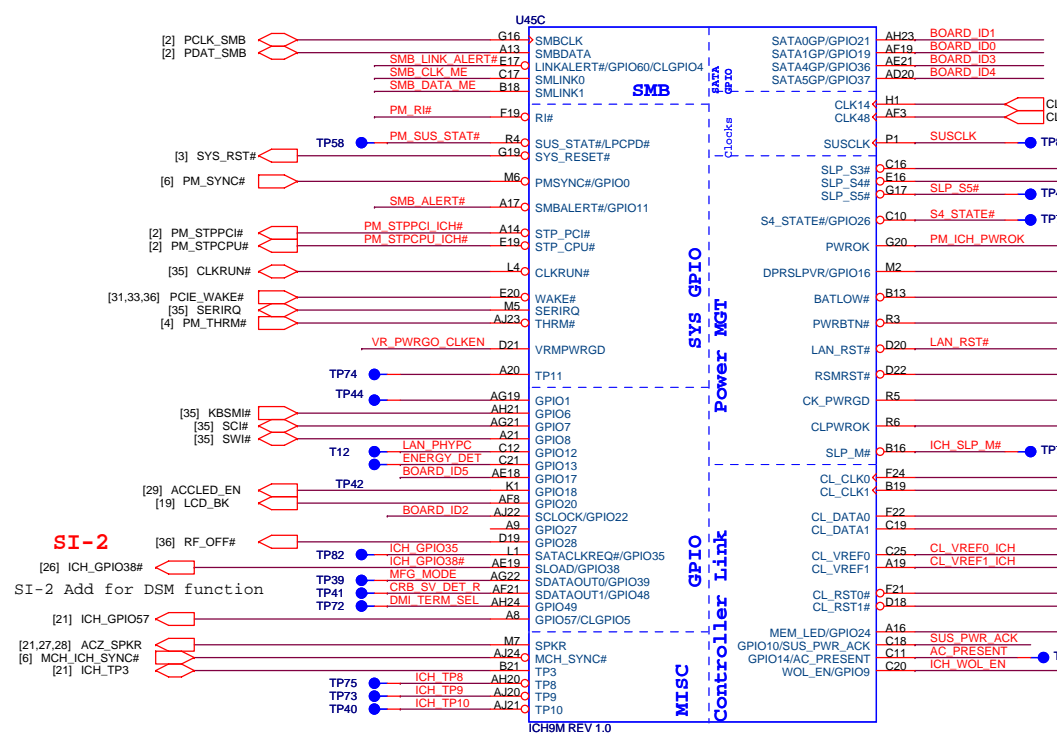
SPI CLK_R
C527
.1U/10V_4



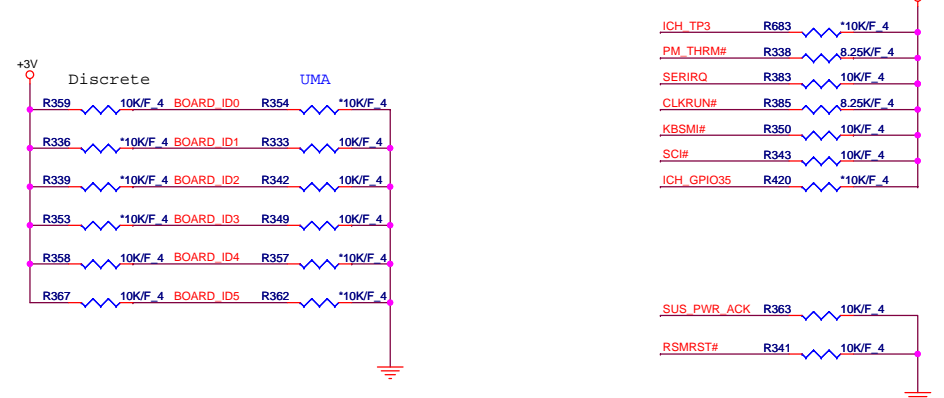
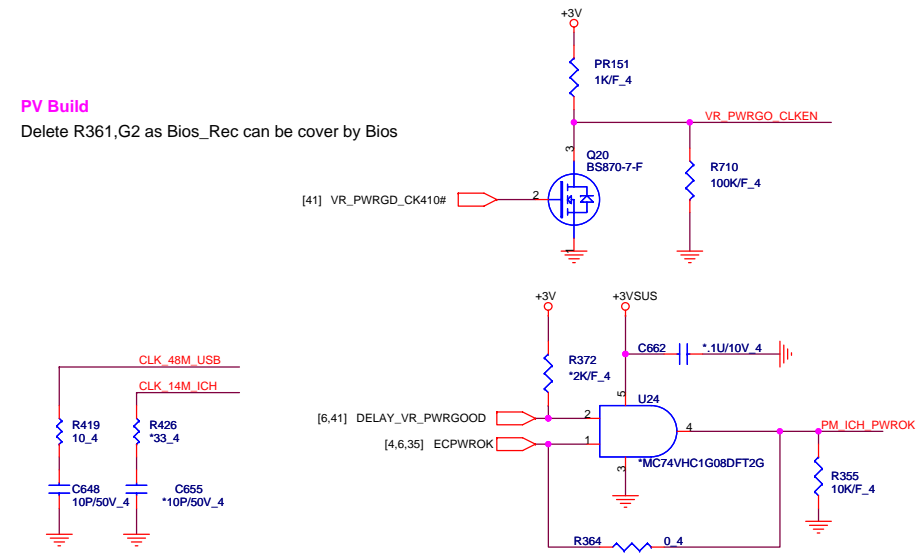
SI-2
SI-2 Delete
Delete RP53,RP57 and tied from SB to CR(USB6)



[4,9,21,22,24,27,29,33,36,40,44] +1.5V
 [2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +3V
 [21,22,24,33,44] +3VS5
 [25,30,36,40,41,42,44] +3VSUS



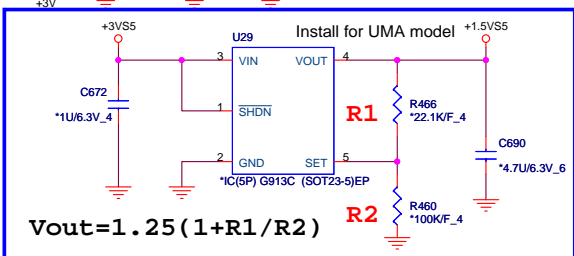
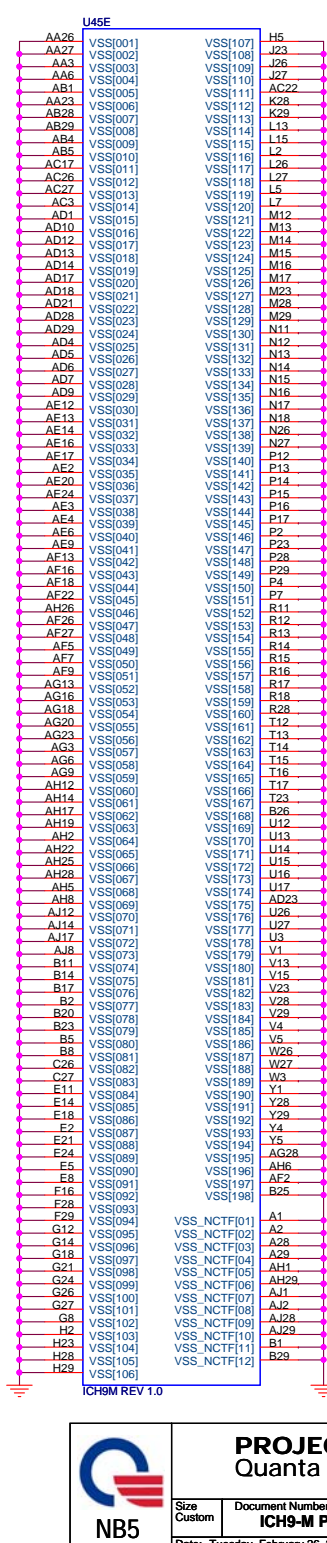
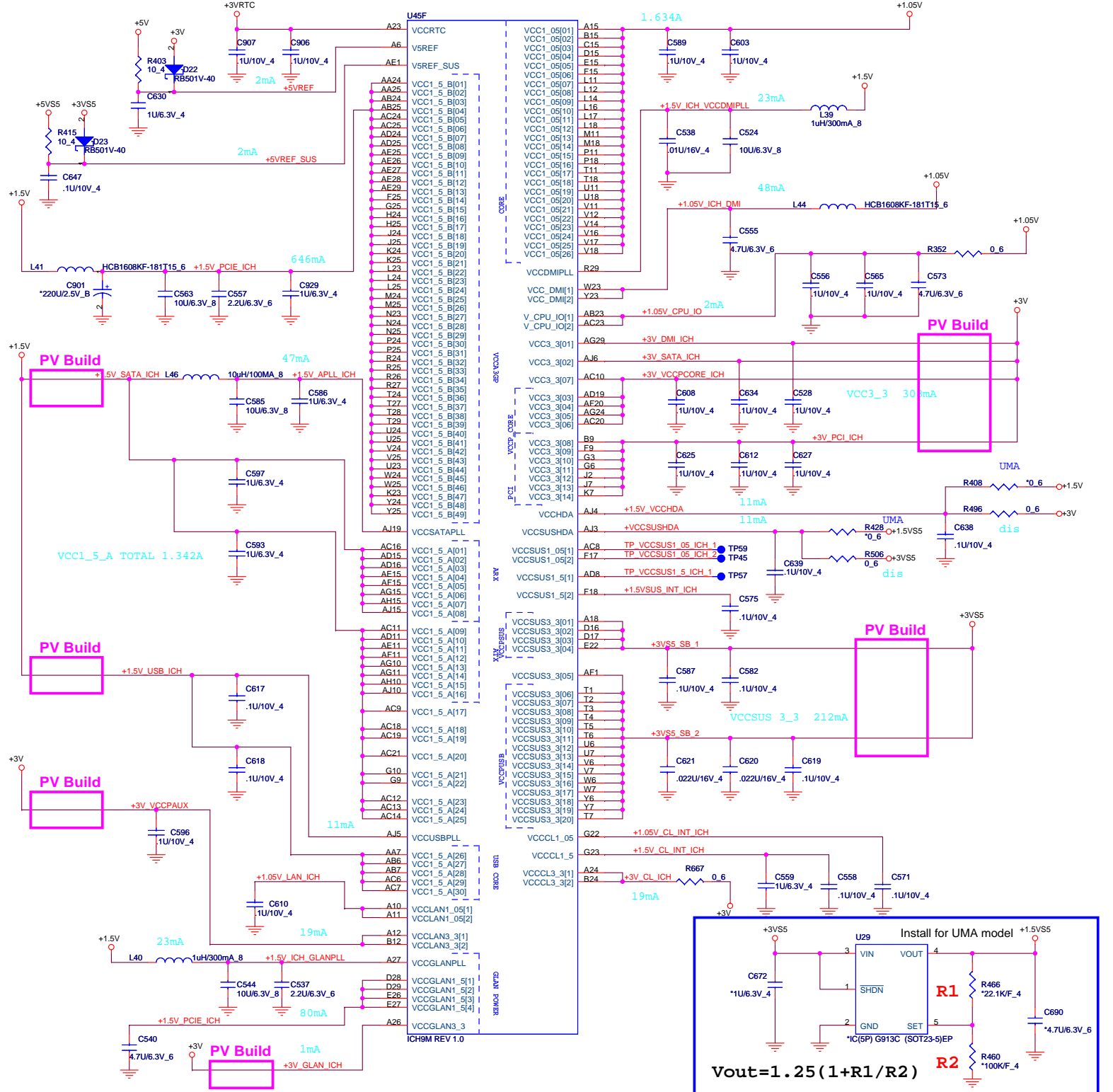
PV Build
 Delete R361,G2 as Bios_Rec can be cover by Bios



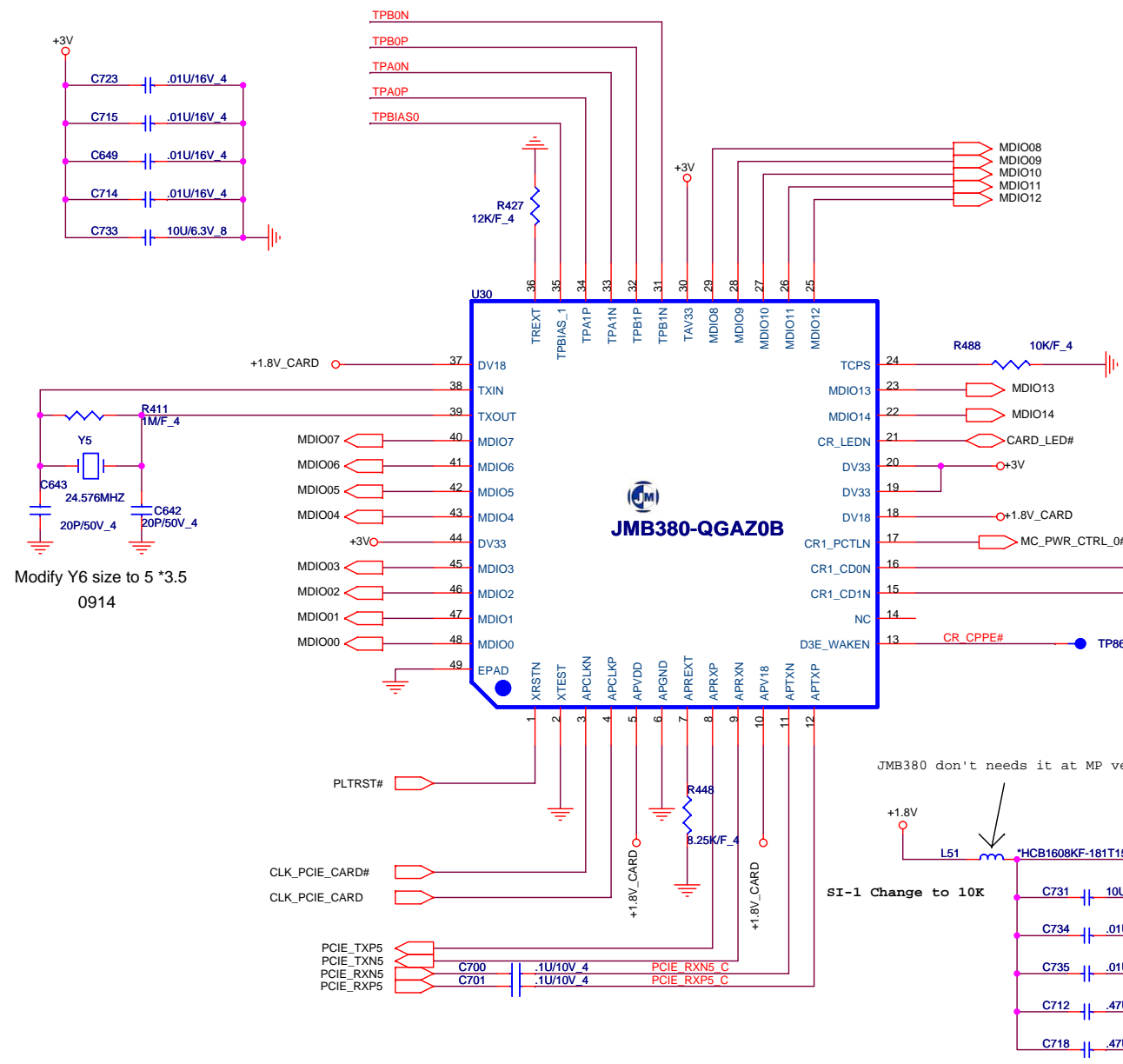
Board ID 0: 1-->Discrete , 0-->UMA
 Board ID 1
 Board ID 2
 Board ID 3
 Board ID 4
 Board ID 5

PROJECT : QT6
 Quanta Computer Inc.

Size Custom	Document Number ICH9-M GPIO 3/4	Rev 1A
Date: Tuesday, February 26, 2008 Sheet 23 of 44		

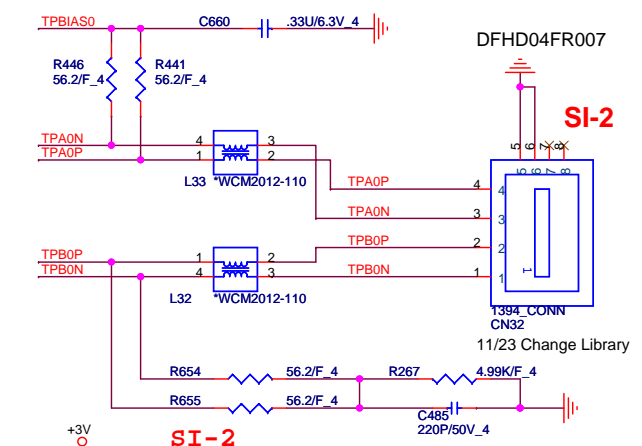


PROJECT : QT6
Quanta Computer Inc.

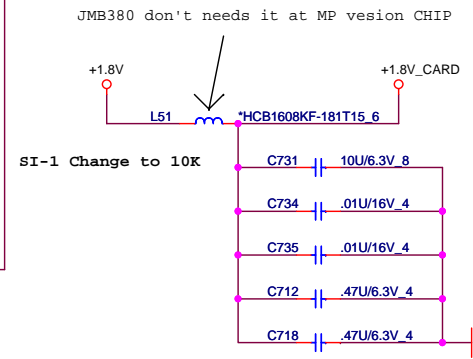
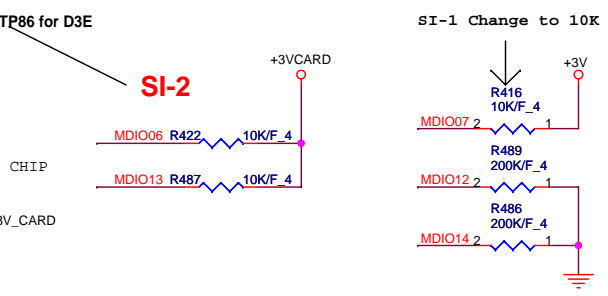
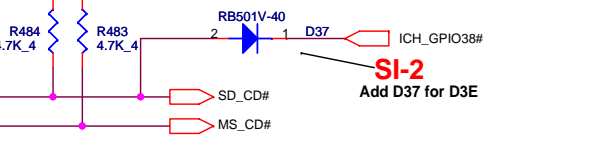


Modify Y6 size to 5 * 3.5
0914

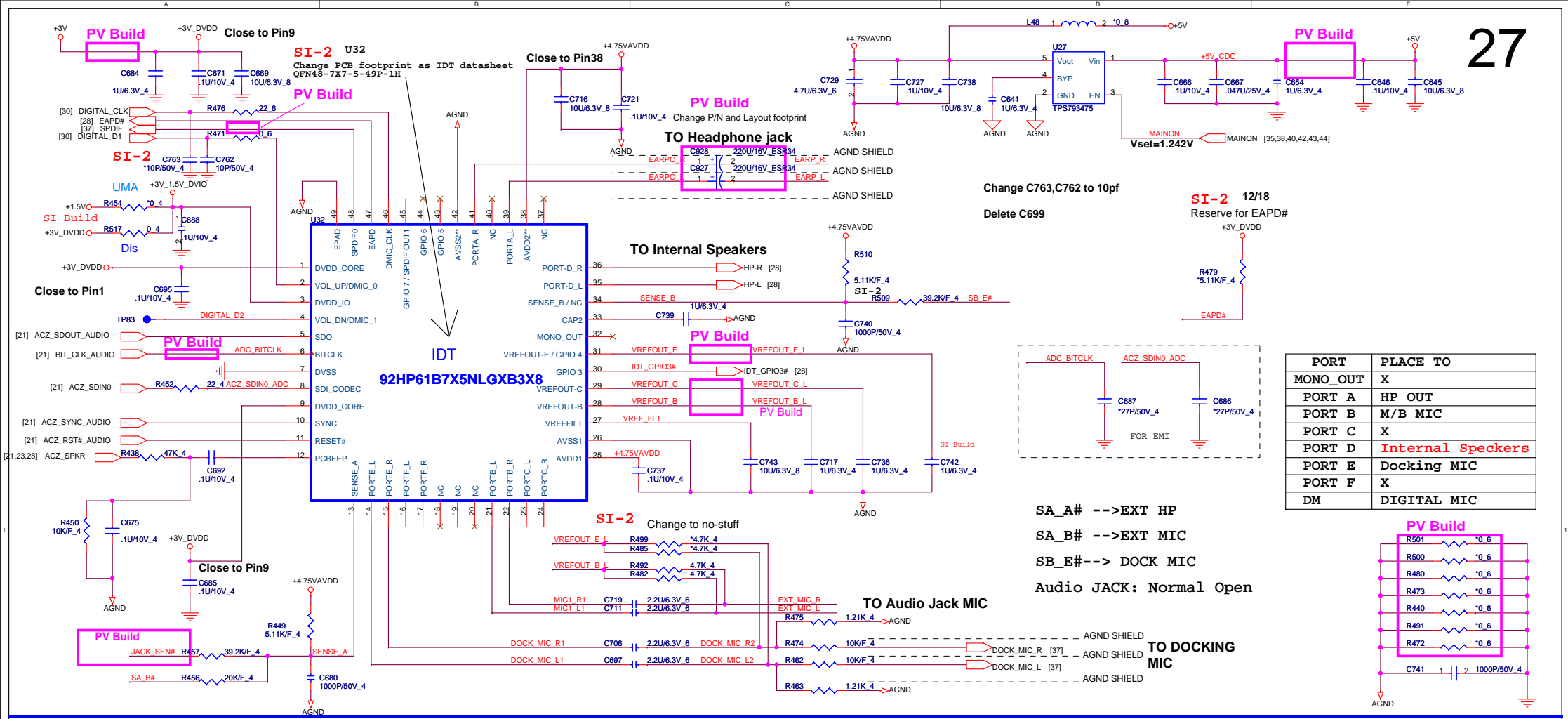
PV Build
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT6



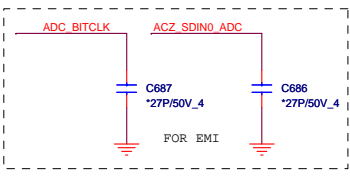
SI-2
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT8 (11/19)



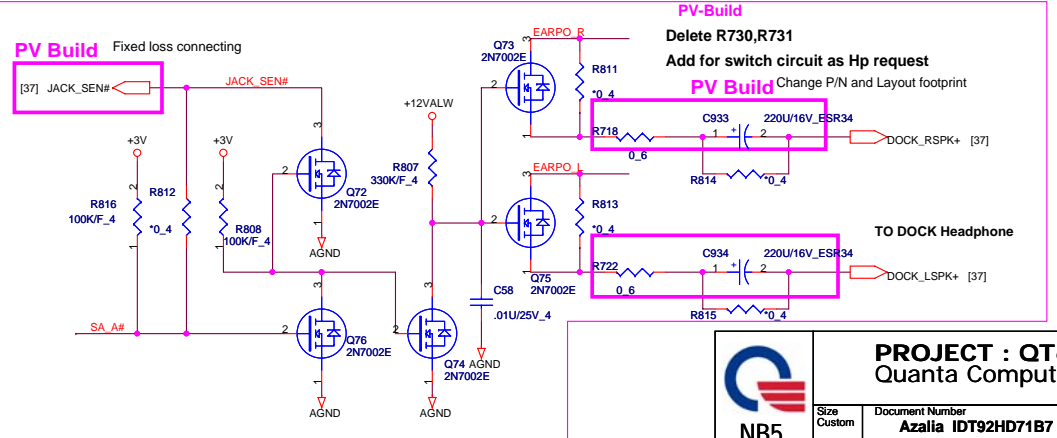
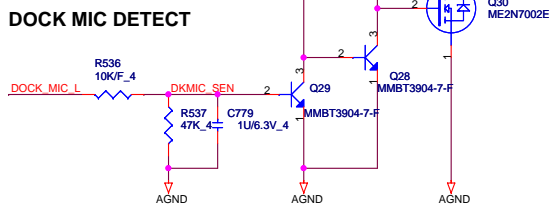
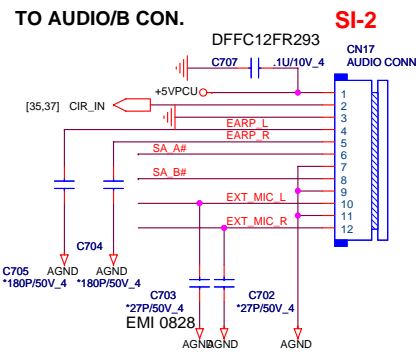
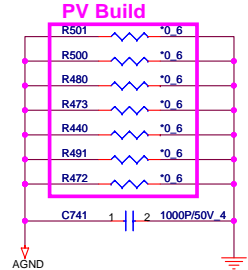
	PROJECT : QT6 Quanta Computer Inc.	
	Size B	Document Number JMB380 Controller/1394
Date: Tuesday, February 26, 2008 Sheet 26 of 44		



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speakers
PORT E	Docking MIC
PORT F	X
DM	DIGITAL MIC



SA_A# -->EXT HP
 SA_B# -->EXT MIC
 SB_E#--> DOCK MIC
 Audio JACK: Normal Open



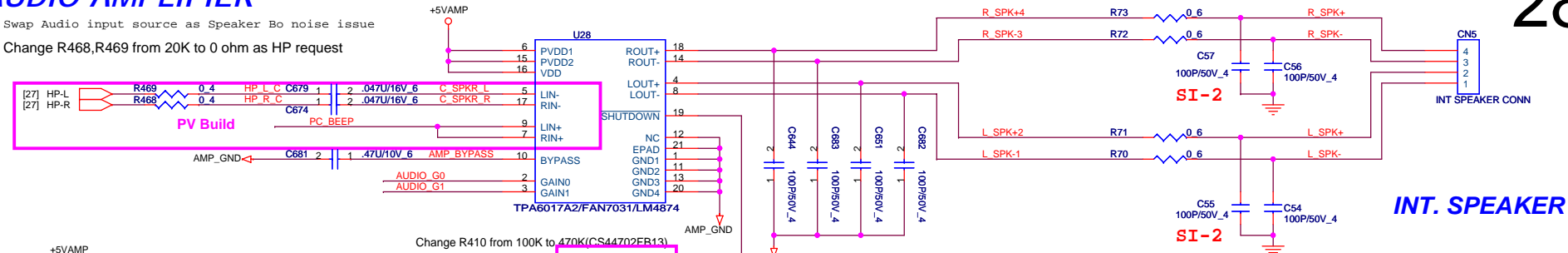
PROJECT : QT6
 Quanta Computer Inc.

Size Custom	Document Number Azalia IDT92HD71B7	Rev 3A
Date: Tuesday, February 26, 2008 Sheet 27 of 44		

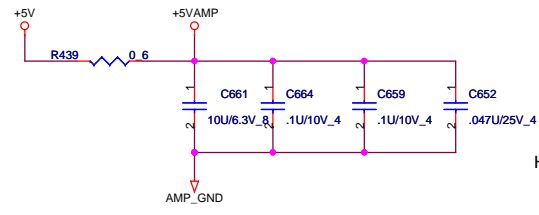
AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue

Change R468,R469 from 20K to 0 ohm as HP request



Change R410 from 100K to 470K(CS44702ER13)

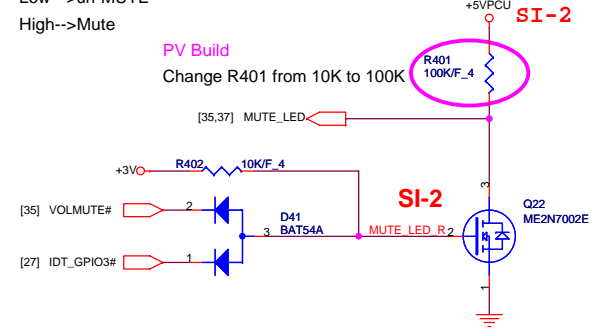


AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

MUTE_LED

Low --> un-MUTE
High --> Mute

Change Power source to +5VPCU as power situation

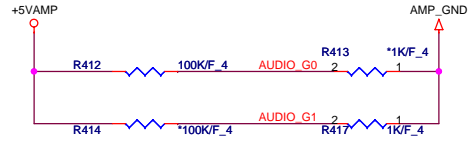
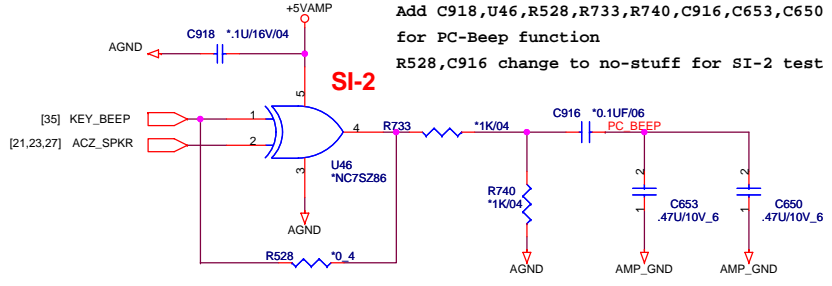


6017A2 Gain Table

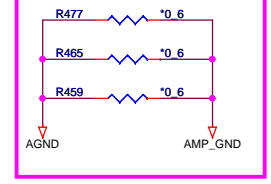
GAIN0	GAIN1	AV	RIN
0	0	6dB	90K
0	1	10dB	70K
1	0	15.6dB	45K
1	1	21.6dB	25K

Add in SI-2

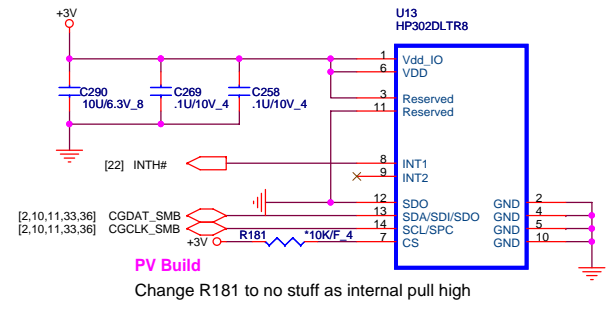
Add C918,U46,R528,R733,R740,C916,C653,C650 for PC-BEEP function
R528,C916 change to no-stuff for SI-2 test -->12/6



PV Build

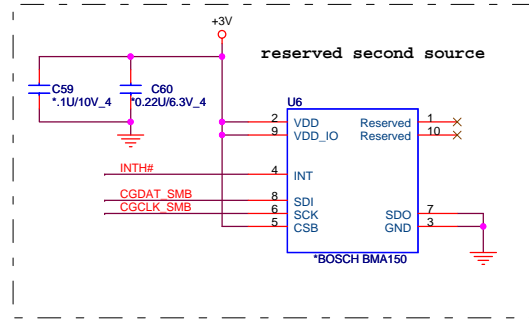


Accelerometer Sensor



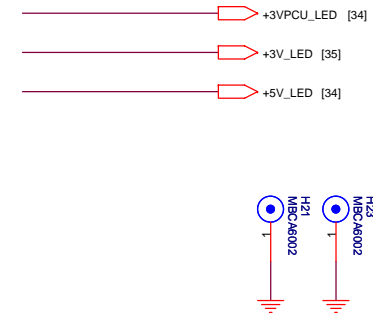
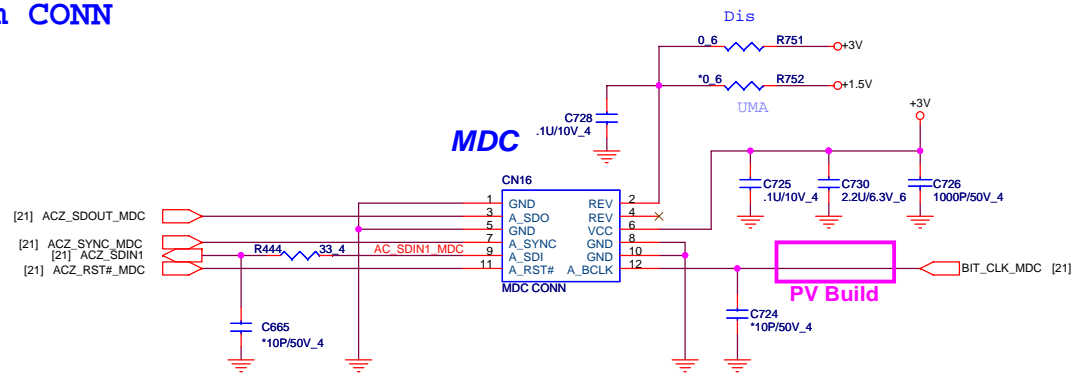
Change R181 to no stuff as internal pull high

Pin 12: Low 38hex
Pin 12: unconnected/floating 3Ahex



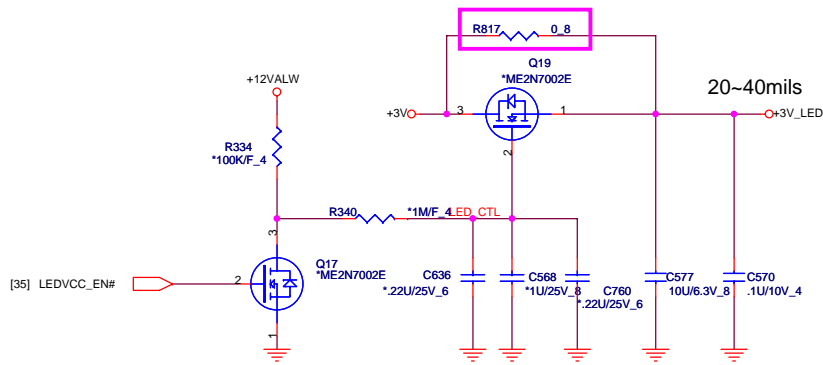
PROJECT : QT6
Quanta Computer Inc.

Size Custom	Document Number AMP_TPA6017/Accelerometer	Rev 3A
Date: Tuesday, February 26, 2008 Sheet 28 of 44		

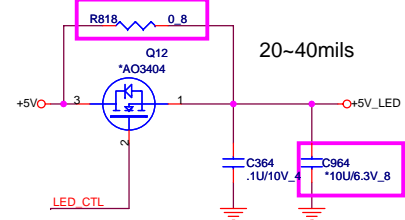


Needs to change Library as ME request

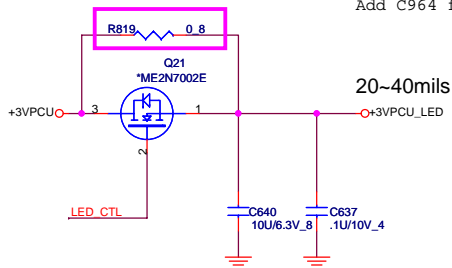
LED PWR CONTROL



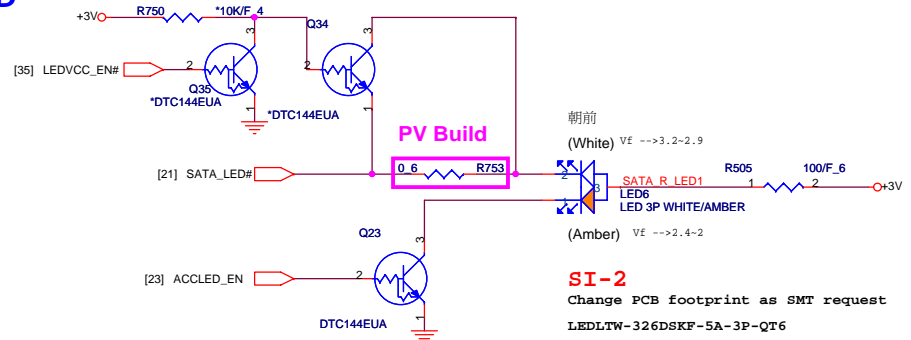
Change Q12 to AO3404 as LED current limited



PV Build
Add R817,R818,R819 as HP LED spec change
Add C964 for reserve



LED

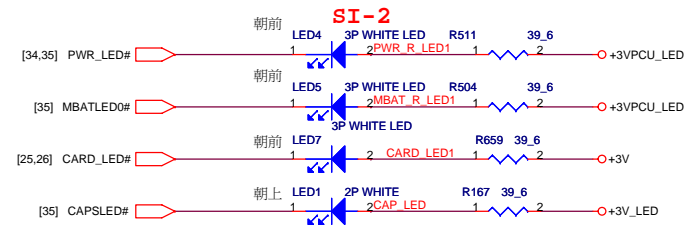


朝前 (White) Vf -->3.2-2.9
朝前 (Amber) Vf -->2.4-2

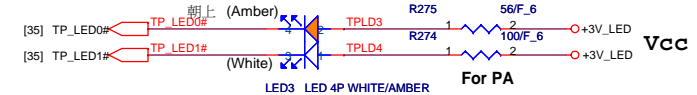
SI-2

Change PCB footprint as SMT request
LEDLTW-326DSKF-5A-3P-QT6
Swap pin , Pin 2 and Pin as Library pin

Modify LED4,LED5,LED7 layout footprint to ledl-s110kgct-3p-qt6 (11/19)



LED Vf

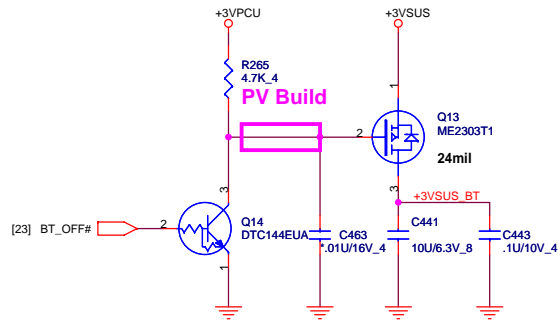


$$I = \frac{V_{cc} - V_f}{R}$$



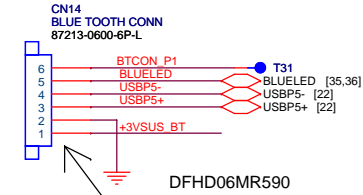
PROJECT : QT6
Quanta Computer Inc.

BLUETOOTH



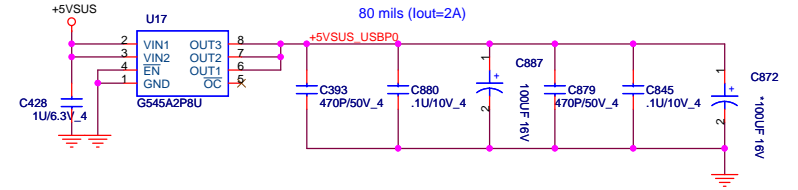
PV Build

Change CN14 P/N to DFHD06MR590

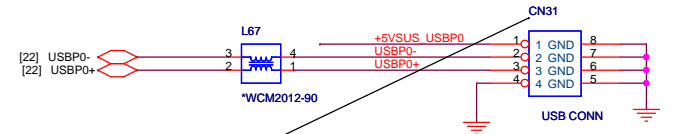


SI-2 CN14 and CN9 87213-0600-6P-L
Change footprint as ME request (pitch 1.25mm to 1.0mm)

LEFT SIDE USBX1 and E-SATA/USB COMBO 30



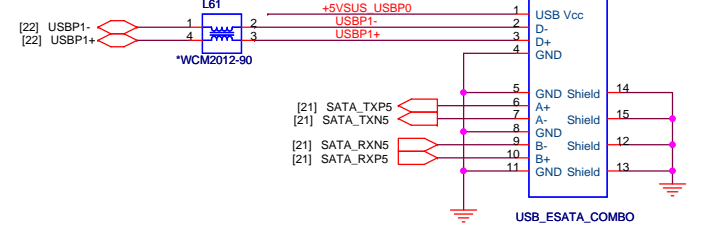
USB 0



SI-2 CN30, CN31 USB-020173MR004851BZR-4P-R-H

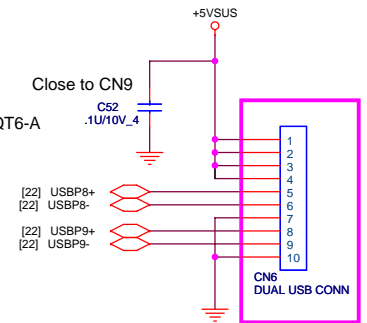
Change Connector layout type from SMD_PAD to Dip as SMT request

USB & ESATA



USB-C-2006102-11P-H-QT6

RIGHT SIDE USBX2



PV Build

Change CN6 to BL123-10R-10P-L-QT6-A

Close to CN9

C52 .1U/10V_4

Touch Screen

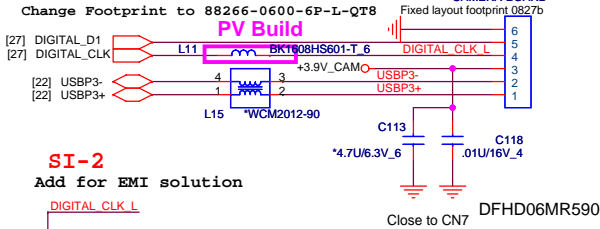
Delete Touch-Screen in SI-2

CN2, C10, L4

SI-2 Build

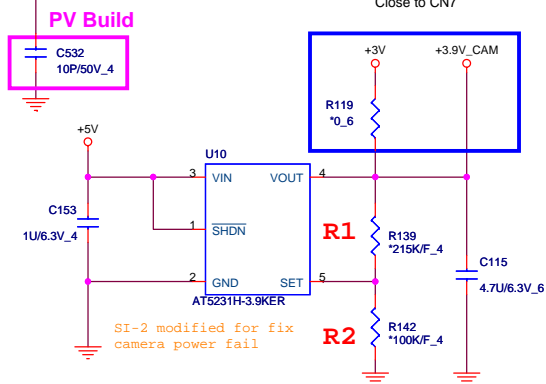
USB CAMERA /DIGITAL MIC CONNECT

SI-2 Build CN9 SI-2
Change Footprint to 88266-0600-6P-L-QT8 Fixed layout footprint 0827b



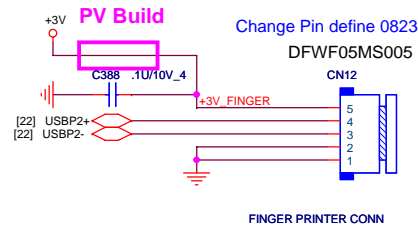
SI-2 Add for EMI solution

DIGITAL_CLK_L



$$V_{out} = 1.25(1 + R1/R2)$$

USB fingerprint CON



PV Build

Change CN12 to BL123-05R-5P-L-QT6-A

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

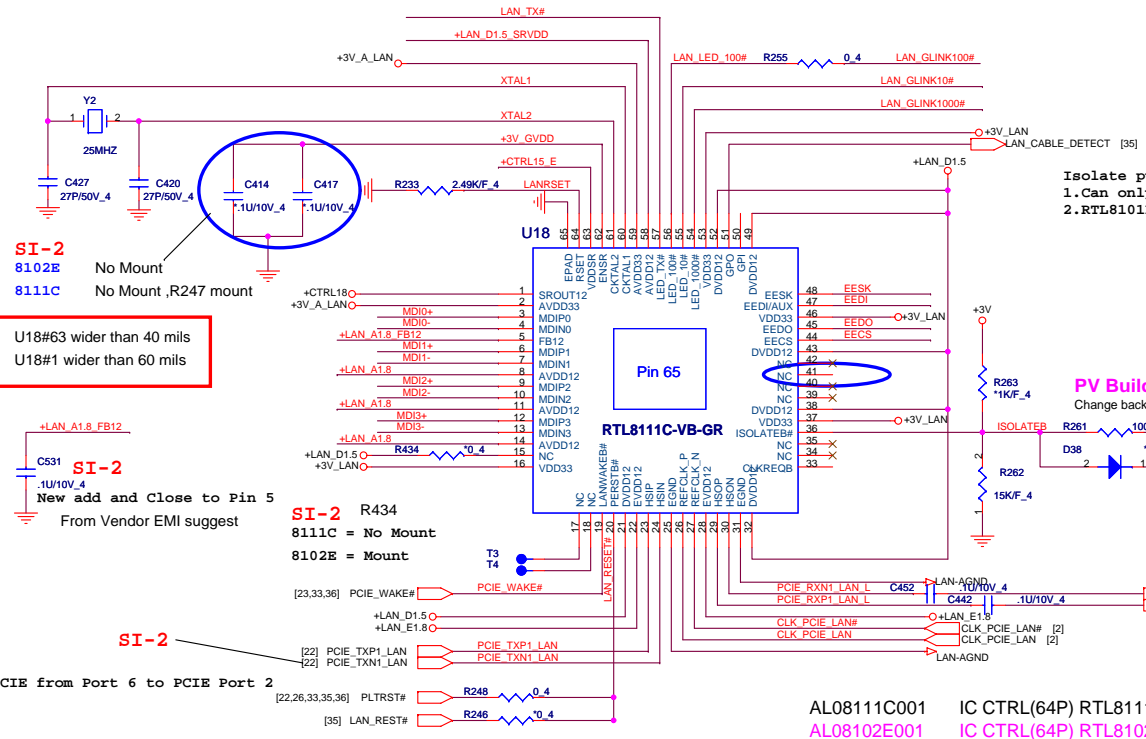
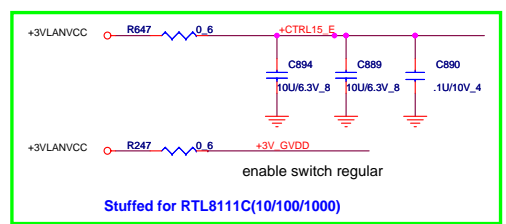
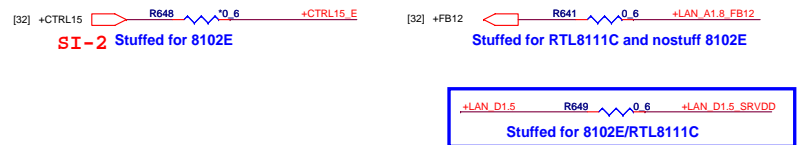


PROJECT : QT6
Quanta Computer Inc.

T : Stuffed for RTL8111C(10/100/1000)

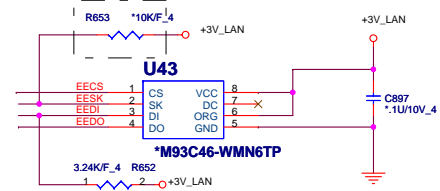
E : Stuffed for 8101E/8102E(10/100)

For 8102E/8111C



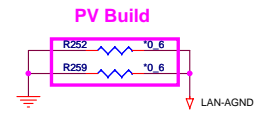
Isolate pull low:
 1.Can only disable RTL8111C.
 2.RTL8101E can't disable

for 93C56 used. NC if 93C46 is used.



PV Build
 Change back to R261 at 1/24

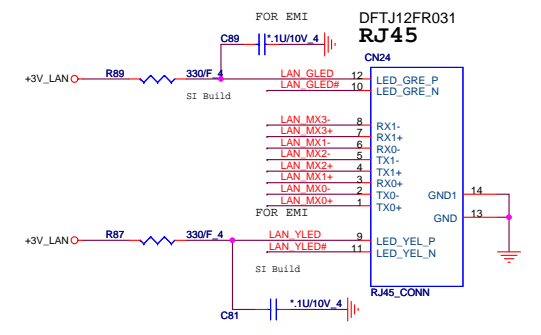
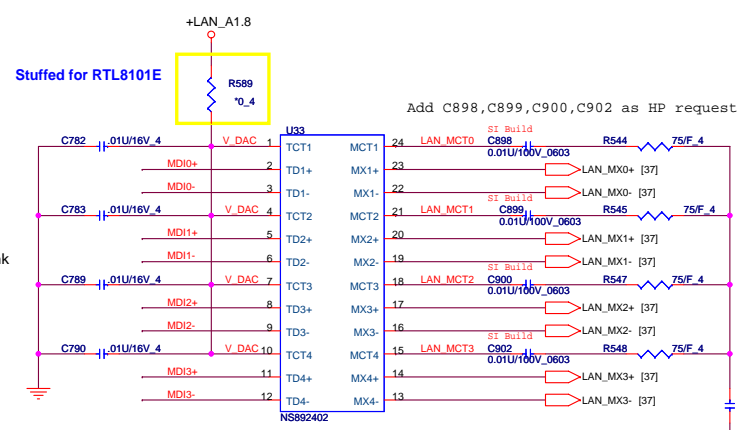
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)



- PV Build**
- Remove 8111B and 8101E support in PV Build
 - Delete R264 (For 8111B)
 - Delete R650 and T28
 - Delete R651 and U18#33 for 8111B support
 - Delete R231 as RSET
 - Delete R242,R243,R244,R245,C394,C395 8101E support

Swap PCIE from Port 6 to PCIE Port 2

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
 AL08102E001 IC CTRL(64P) RTL8102E-VB-GR(QFN)



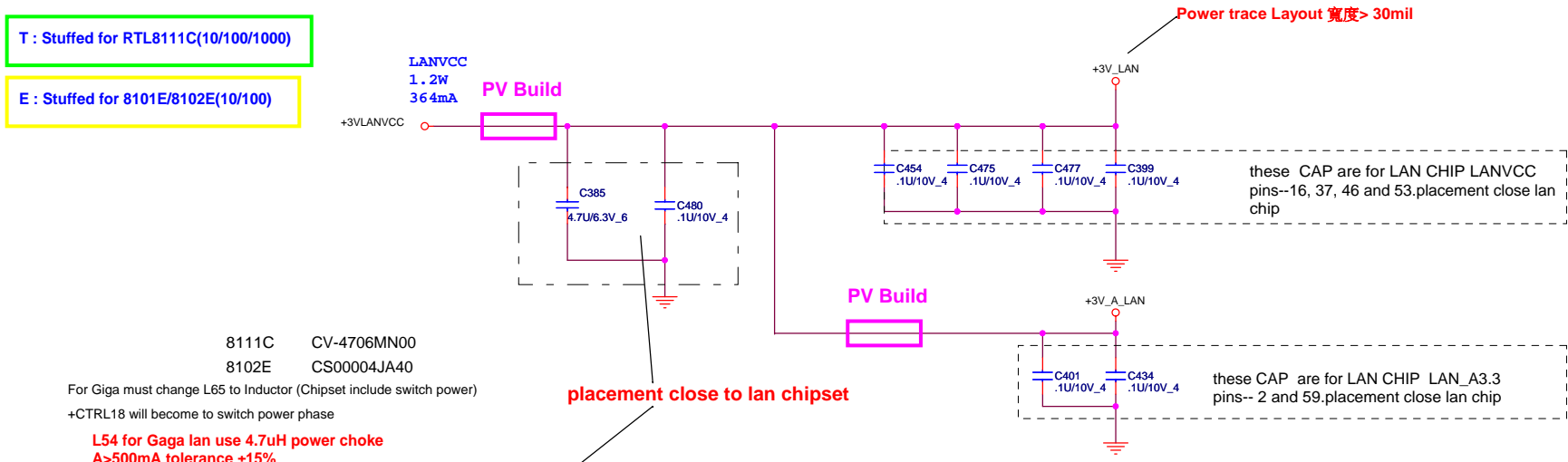
NS892402:GIGABIT DB0AT9LAN05
 NS892405:10/100 DB0ZB1LAN04

PROJECT : QT6
 Quanta Computer Inc.

Size Custom	Document Number	Rev
	RTL8111C/8101E/RJ45	2B
Date: Tuesday, February 26, 2008	Sheet	31 of 44

T : Stuffed for RTL8111C(10/100/1000)

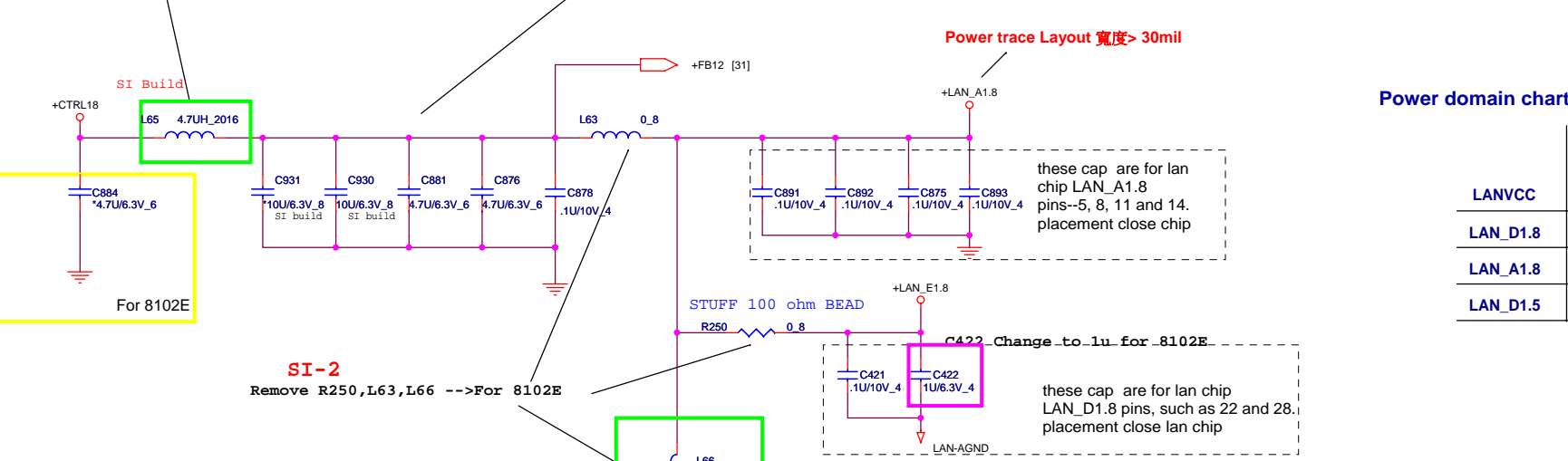
E : Stuffed for 8101E/8102E(10/100)



8111C CV-4706MN00
8102E CS00004JA40

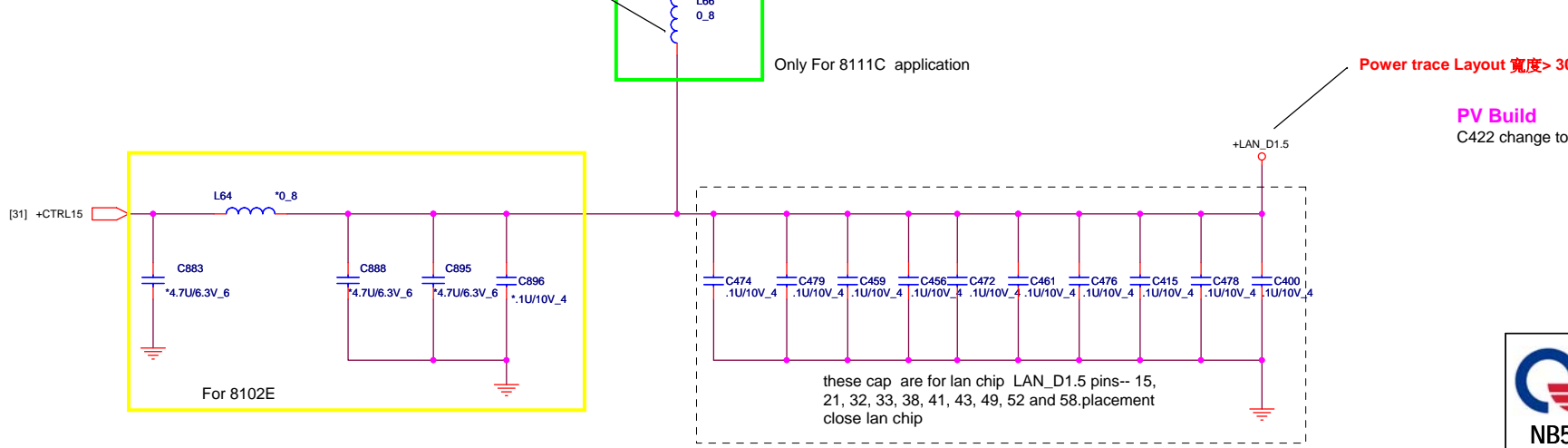
For Giga must change L65 to Inductor (Chipset include switch power)
+CTRL18 will become to switch power phase

**L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%**



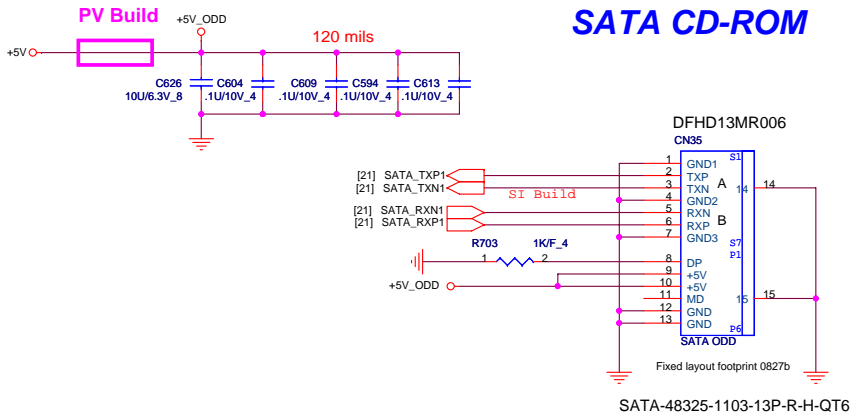
Power domain chart

	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

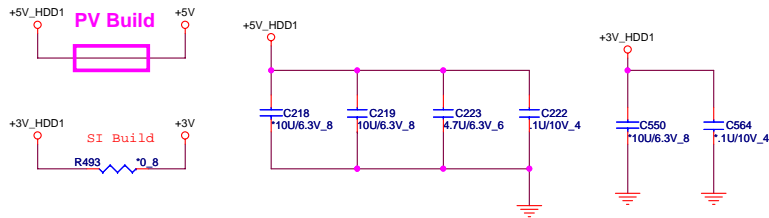
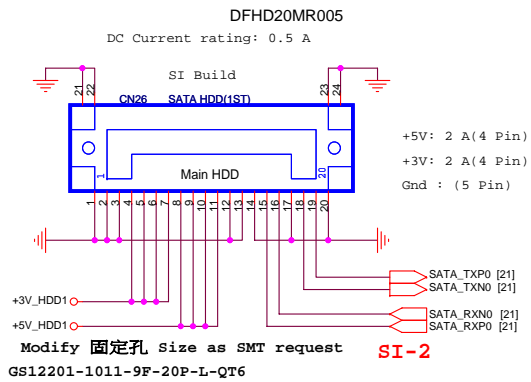


PV Build
C422 change to 1uf



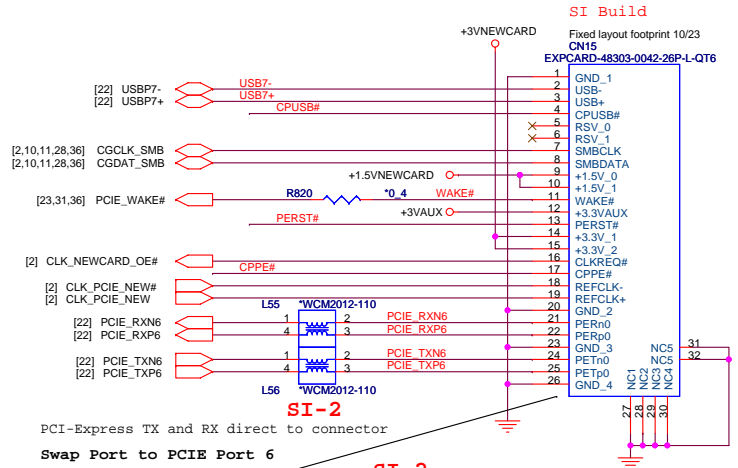


SATA HDD CONNECTOR

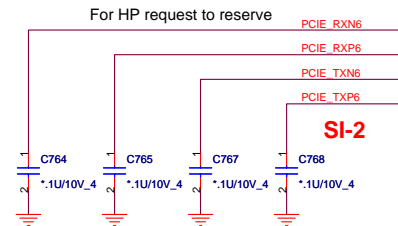
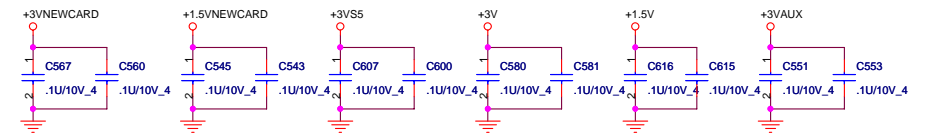
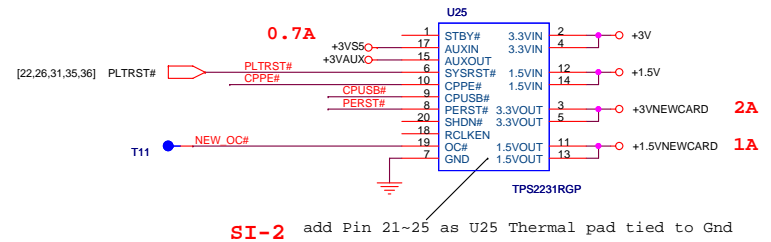


NEWCARD

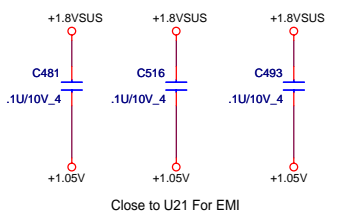
NEWCARD (PCIEXPRESS*1 + USB*1)



SI-2
Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



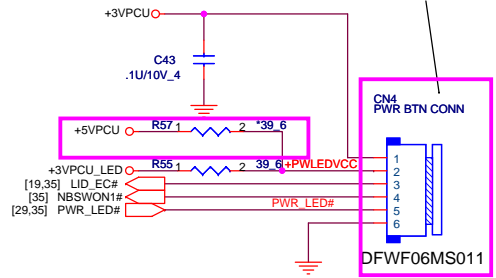
	PROJECT : QT6 Quanta Computer Inc.	
	Size Custom Document Number ODD/HDD/NEW CARD	Date: Tuesday, February 26, 2008 Sheet 33 of 44



Close to U21 For EMI

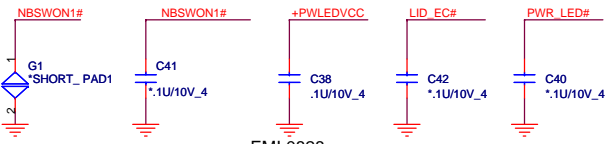
PV Build

Change CN4 to BL123-06R-6P-L-QT6-A



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

POWER BOTTON CONNECT



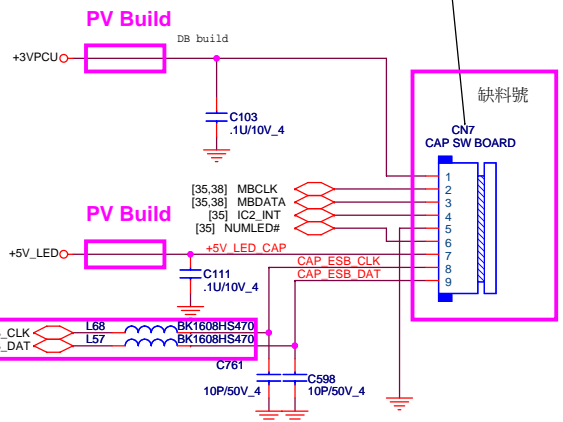
EMI 0828

POWER SW CONNECT

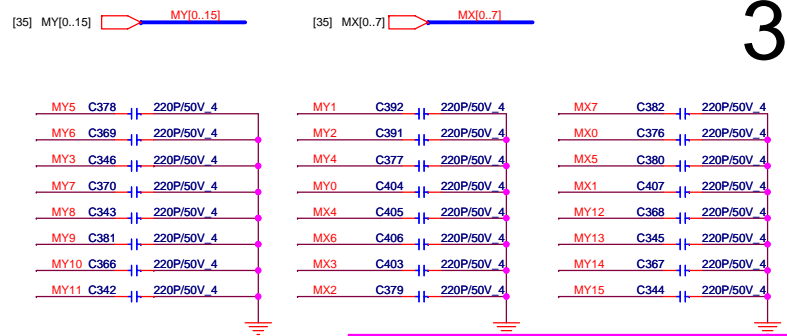
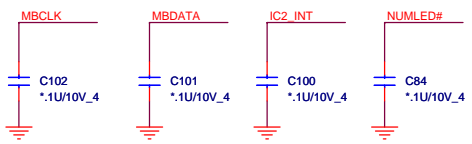
CAP SW CONNECT

PV Build

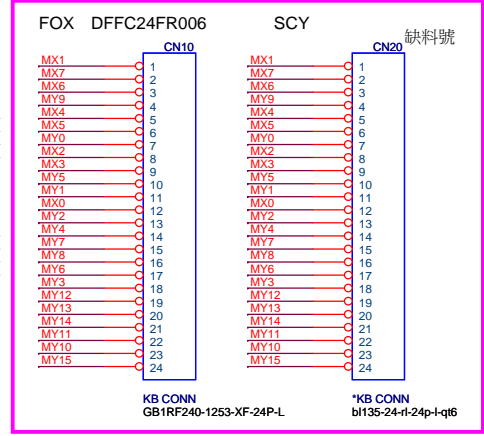
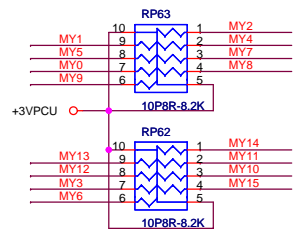
Change CN7 to BL123-09R-9P-L-QT6-A



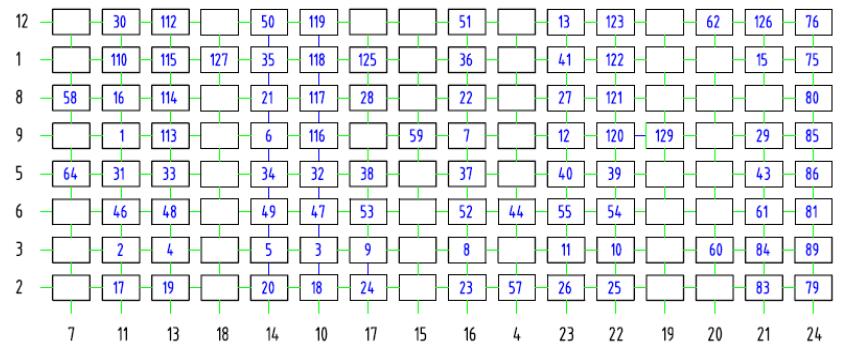
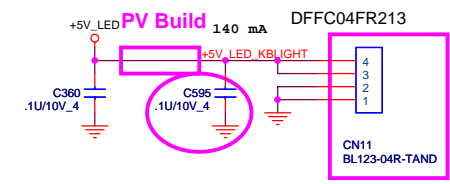
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT



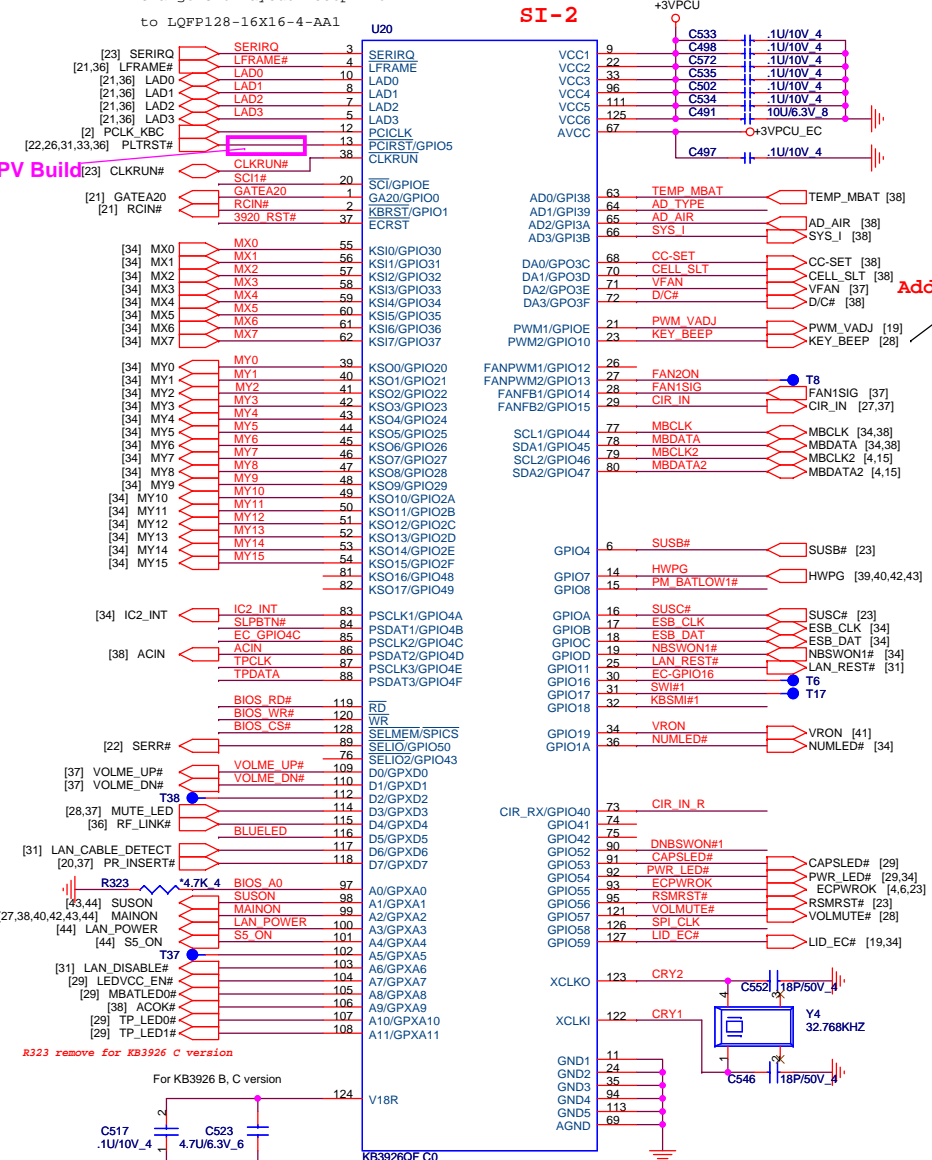
KEYBOARD PULL-UP



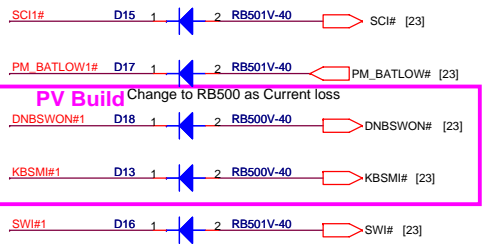
PV Build
Add C595 and close to CN11
Change CN11 to BL123-04R-4P-L-QT6-A
Change CN10 to GB1RF240-1253-XF-24P-L as Foxconn drawing



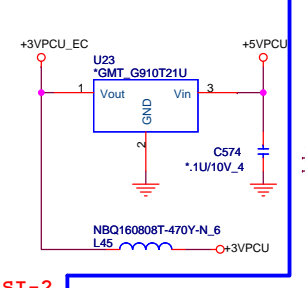
Change U20 layout footprint to LQFP128-16X16-4-AA1



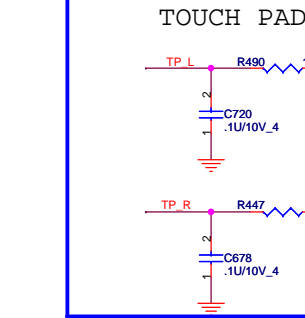
SI-2
 Add Pin 117,103 for DSM,116 for Bluetooth, Pin 23 for Key Beep to Amplifier
 Add T37,T38,T39 for EC
 Delete T10 and tie pin 117 from Lan for DSM



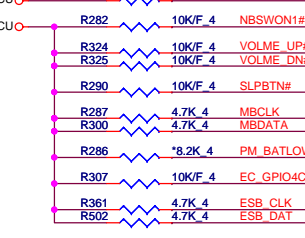
PV Build Change to RB501V-40 as Current loss



PV Build
 Change to SW2,SW3,SW6 to BA1G as vendor suggesst



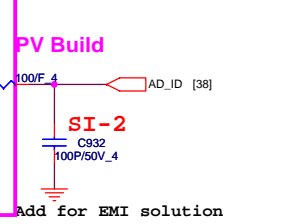
PV Build
 Add R430 and tied to U20 Pin 115 and change Q18 footprint to SOT23



SI-2
 Delete Q18 and tied to U20#116 direction

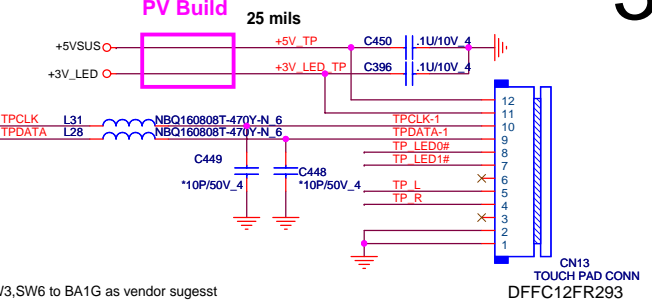


R273
 64.9K -->65W CS36492FB17
 33.2K -->90W CS33322FB13
 Change to 1S335 as Current loss

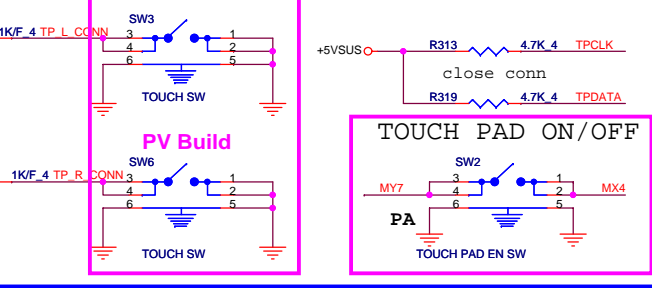


SI-2
 Add for EMI solution

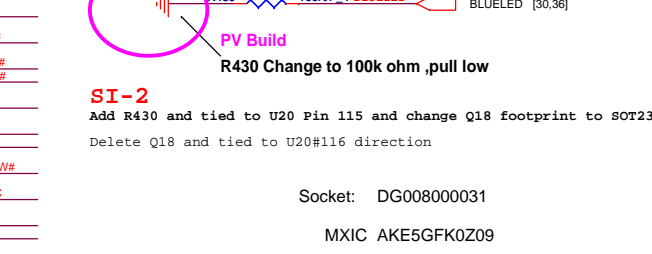
TOUCH PAD CONNECTOR



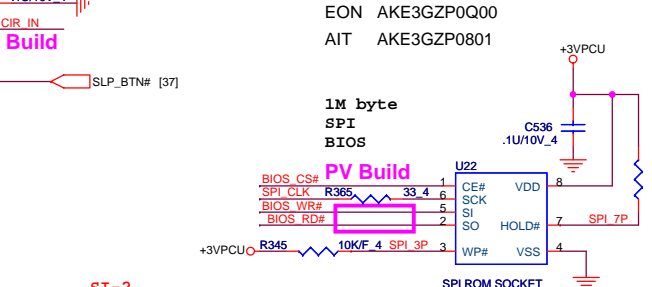
TOUCH PAD L/R



TOUCH PAD ON/OFF



BIOS



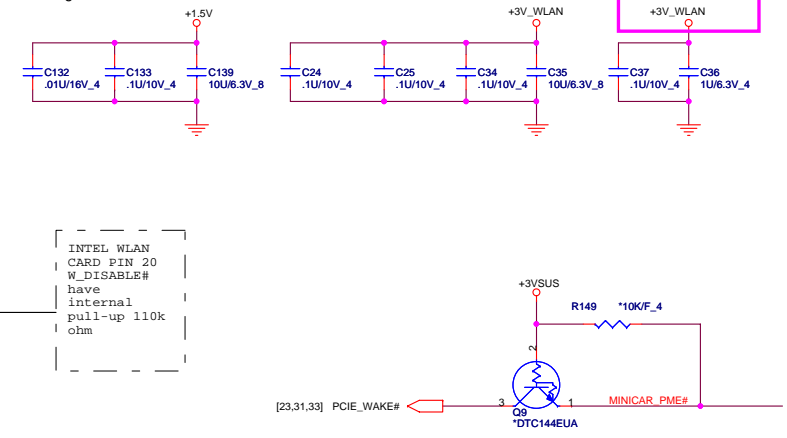
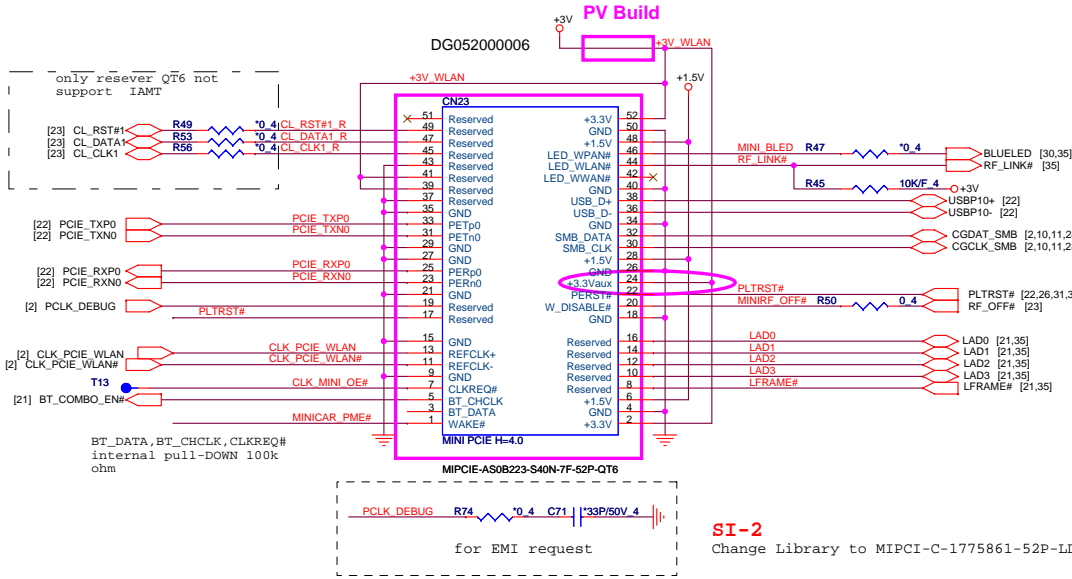
SI-2
 Change Layout footprint to X6179-10XXXX-8P-SOCKET(Socket)

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Quanta Computer Inc.

NB5	Size Custom	Document Number	Rev 3A
		KB3926/ROM/TP	
Date: Tuesday, February 26, 2008		Sheet 35 of 44	

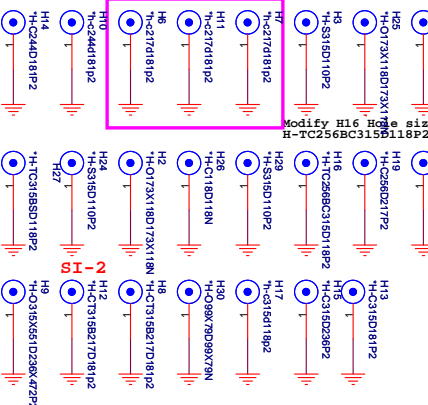
Mini PCI-E Card 1 WLAN

PV Build Delete R78 and tied the CN23#24 to R110 direction
Change CN23 layout footprint to MIPCI-E-AS0B223-S40N-7F-52P-QT6 as ME drawing

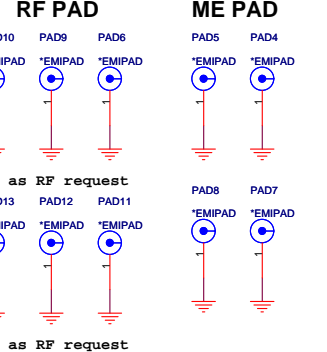


M/B Screw Hole

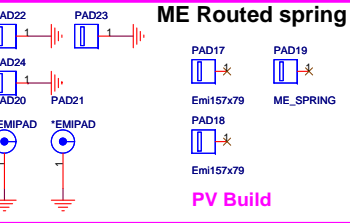
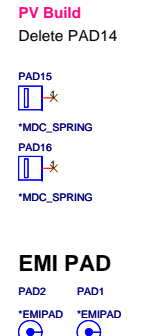
SI-2, h-e276x315d118p2



SI-2 New add as ME request

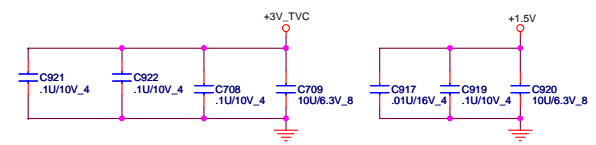
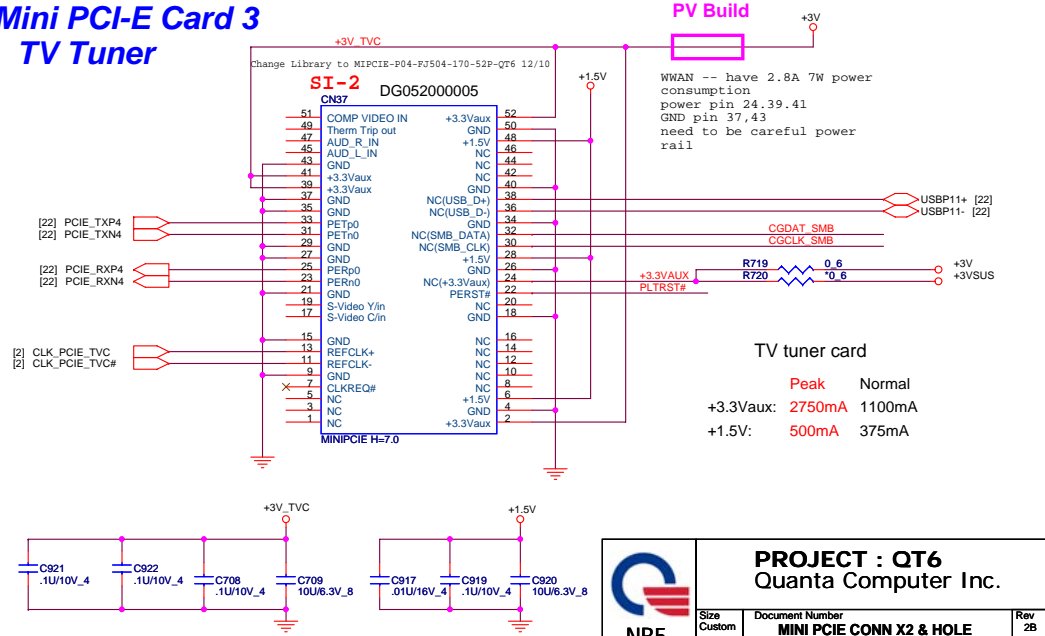


Routed spring



- PV Build**
- Change H1 to h-ctsbds118p2
 - Add PAD17 (Emi157x79)
 - Add PAD18 (Emi157x79)
 - Add PAD19 (Emi236x59)
 - Delete H4,H5 and modify battery connector
 - Change H6,H7,H11 to h-c217d181p2 as ME drawing update

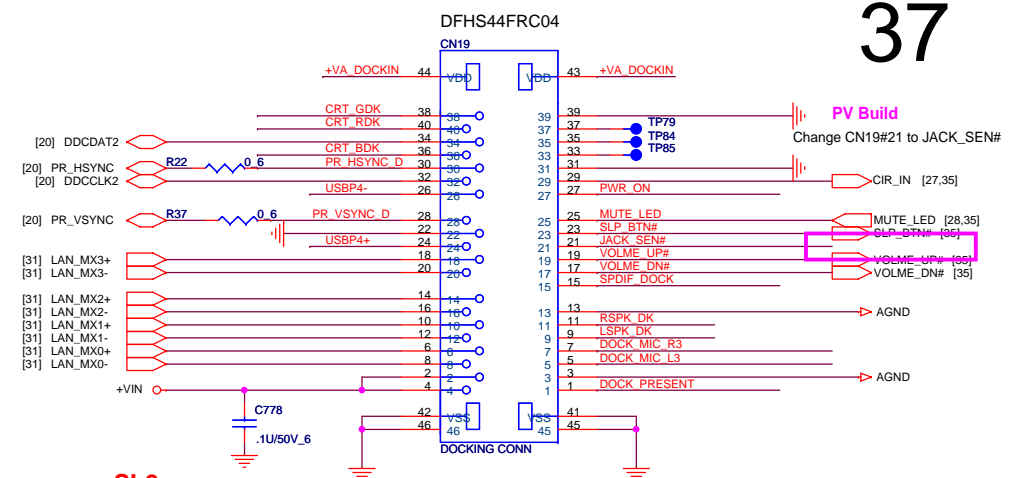
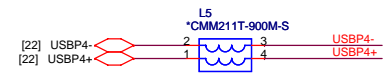
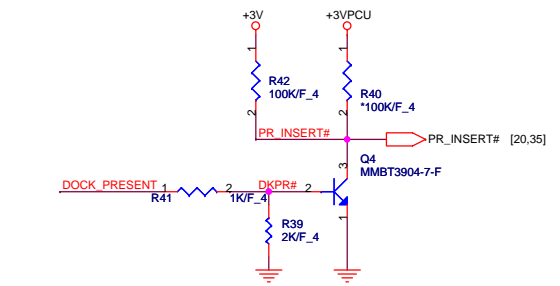
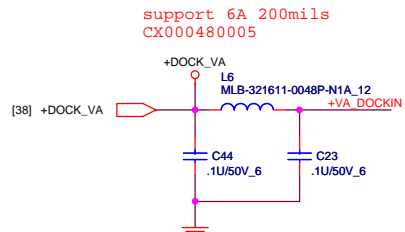
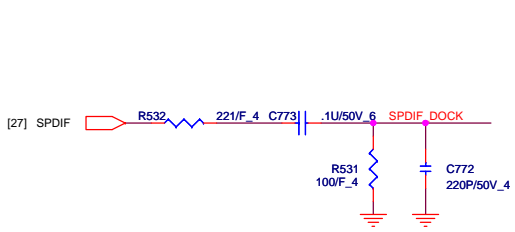
Mini PCI-E Card 3 TV Tuner



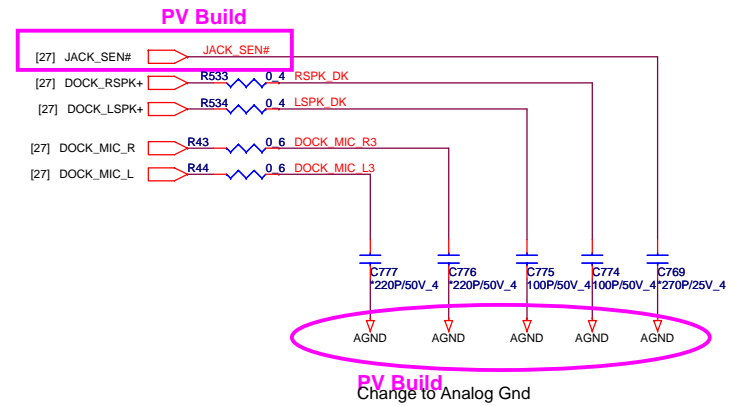
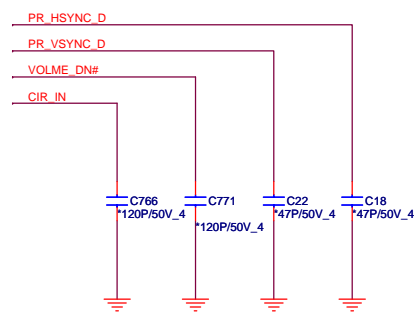
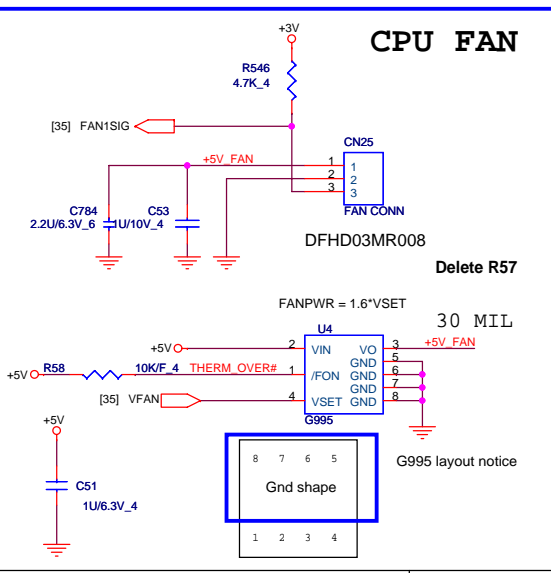
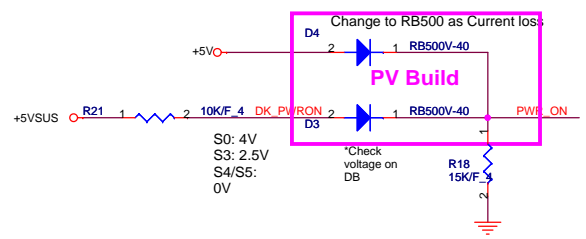
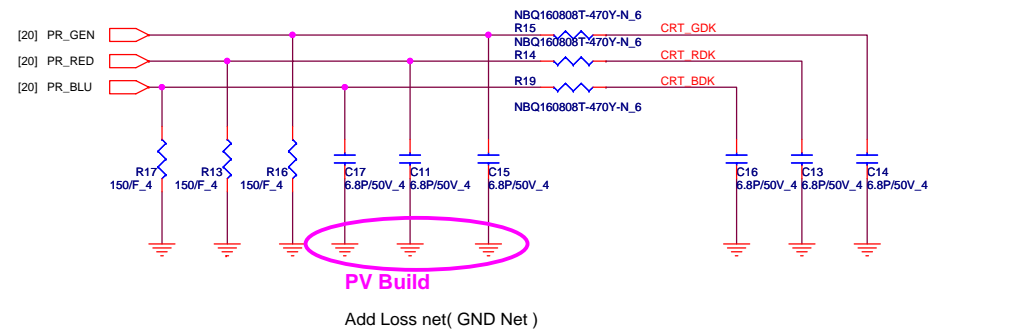
PROJECT : QT6
Quanta Computer Inc.

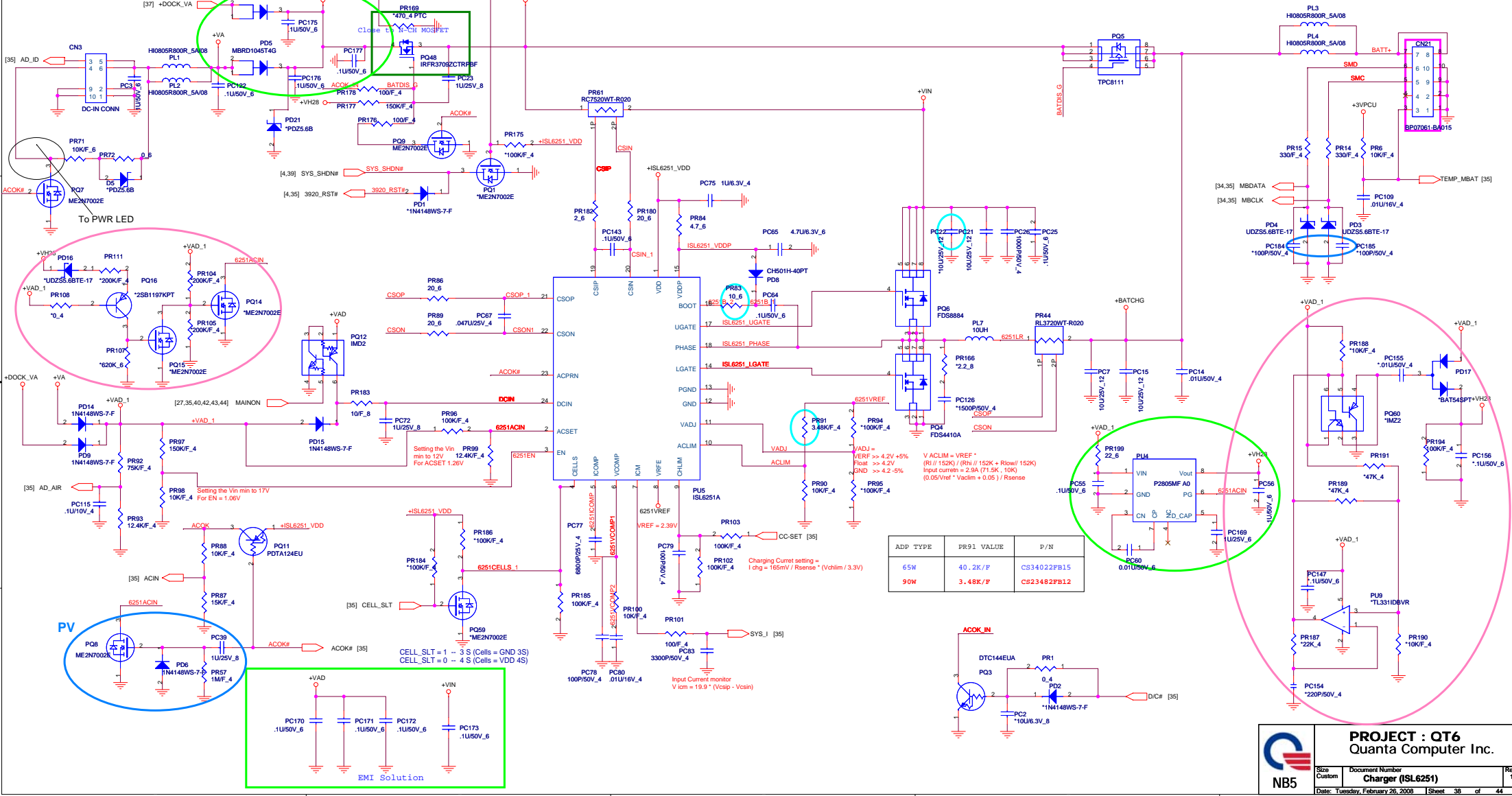
NBS

Size Custom	Document Number MINI PCIE CONN X2 & HOLE	Rev 2B
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SI-2
R13,R16,R17 Change to install





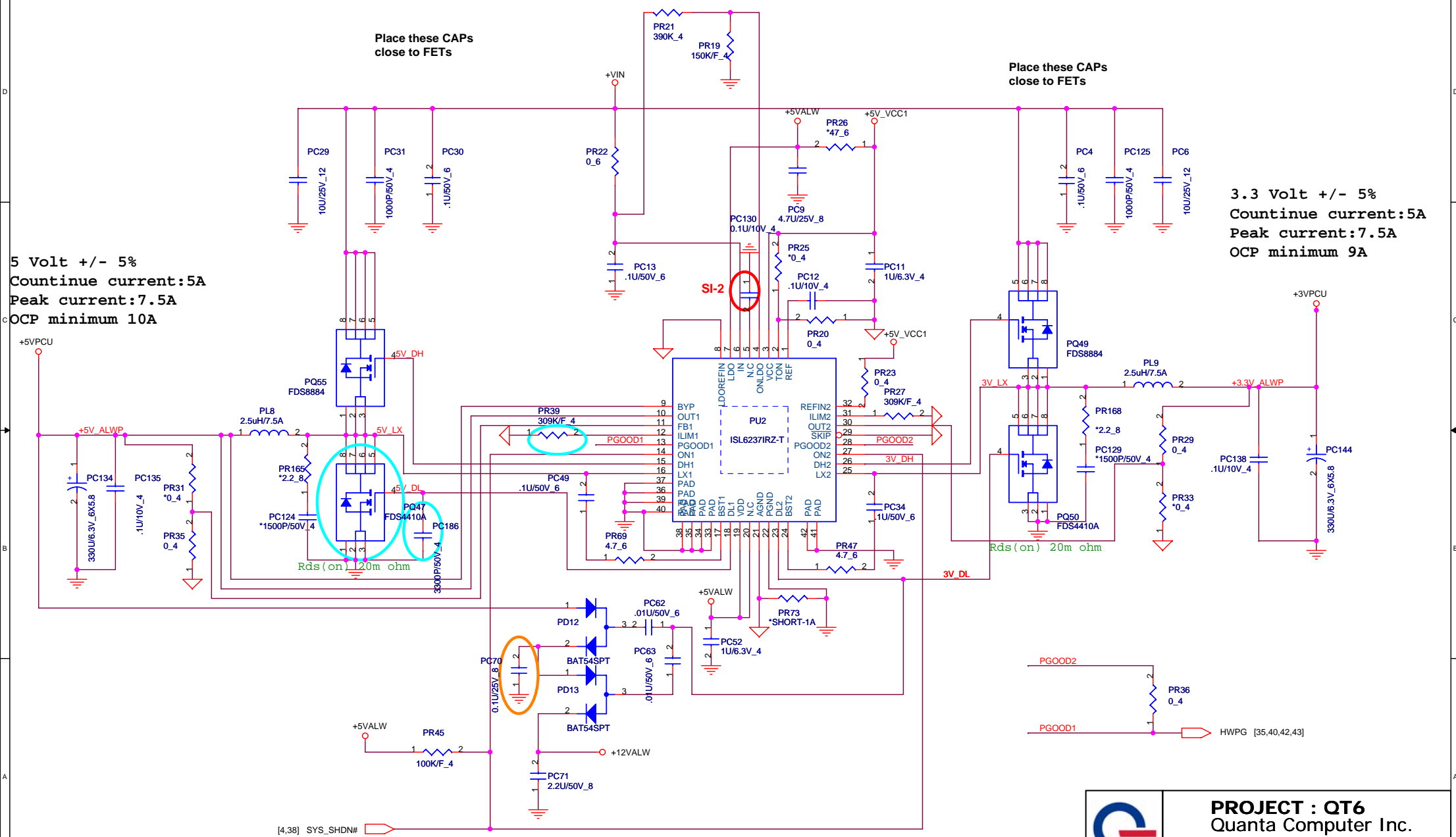
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 10A

3.3 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 9A

Place these CAPS
 close to FETs

Place these CAPS
 close to FETs



[4,38] SYS_SHDN#

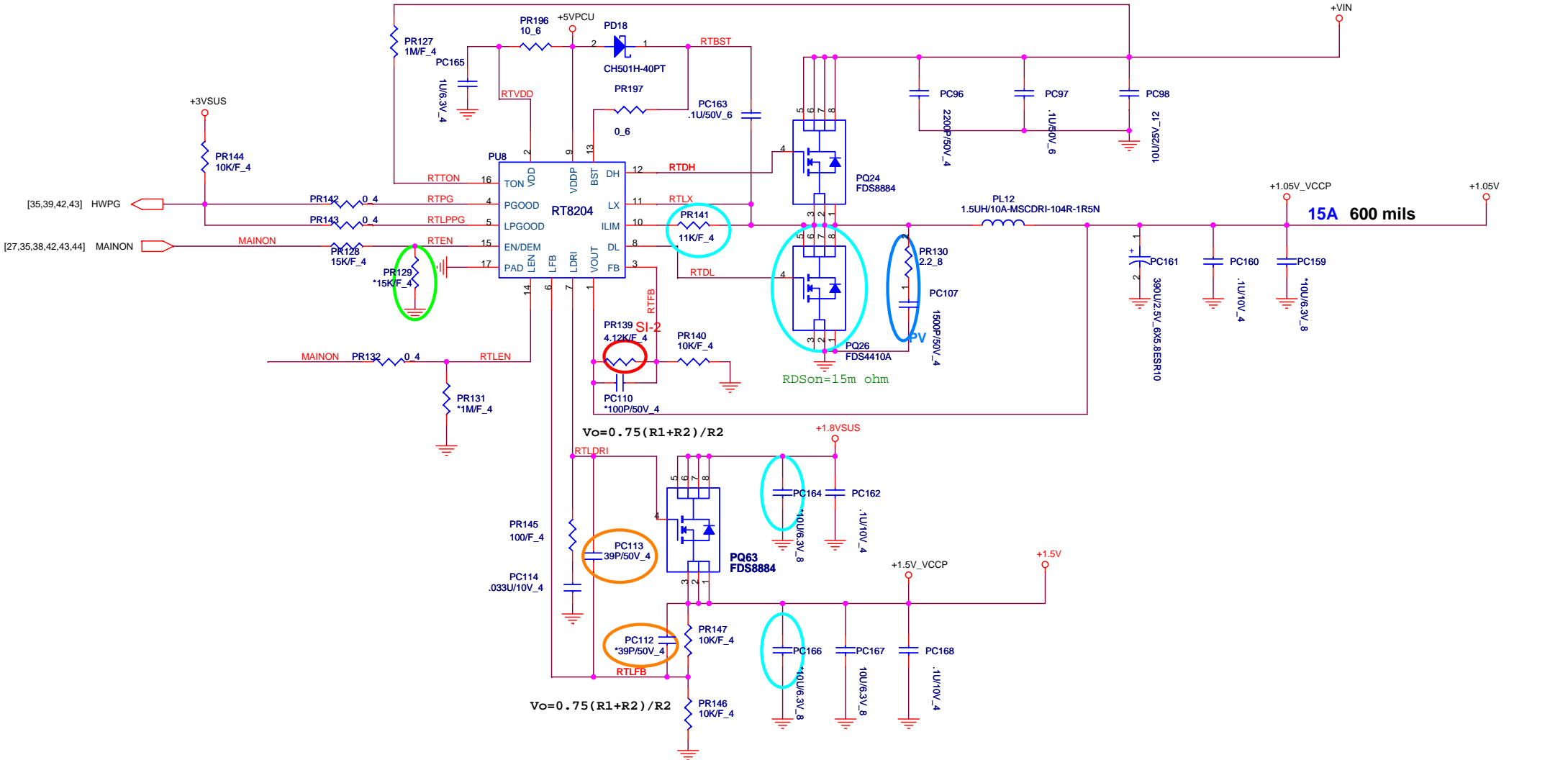



PROJECT : QT6
 Quanta Computer Inc.

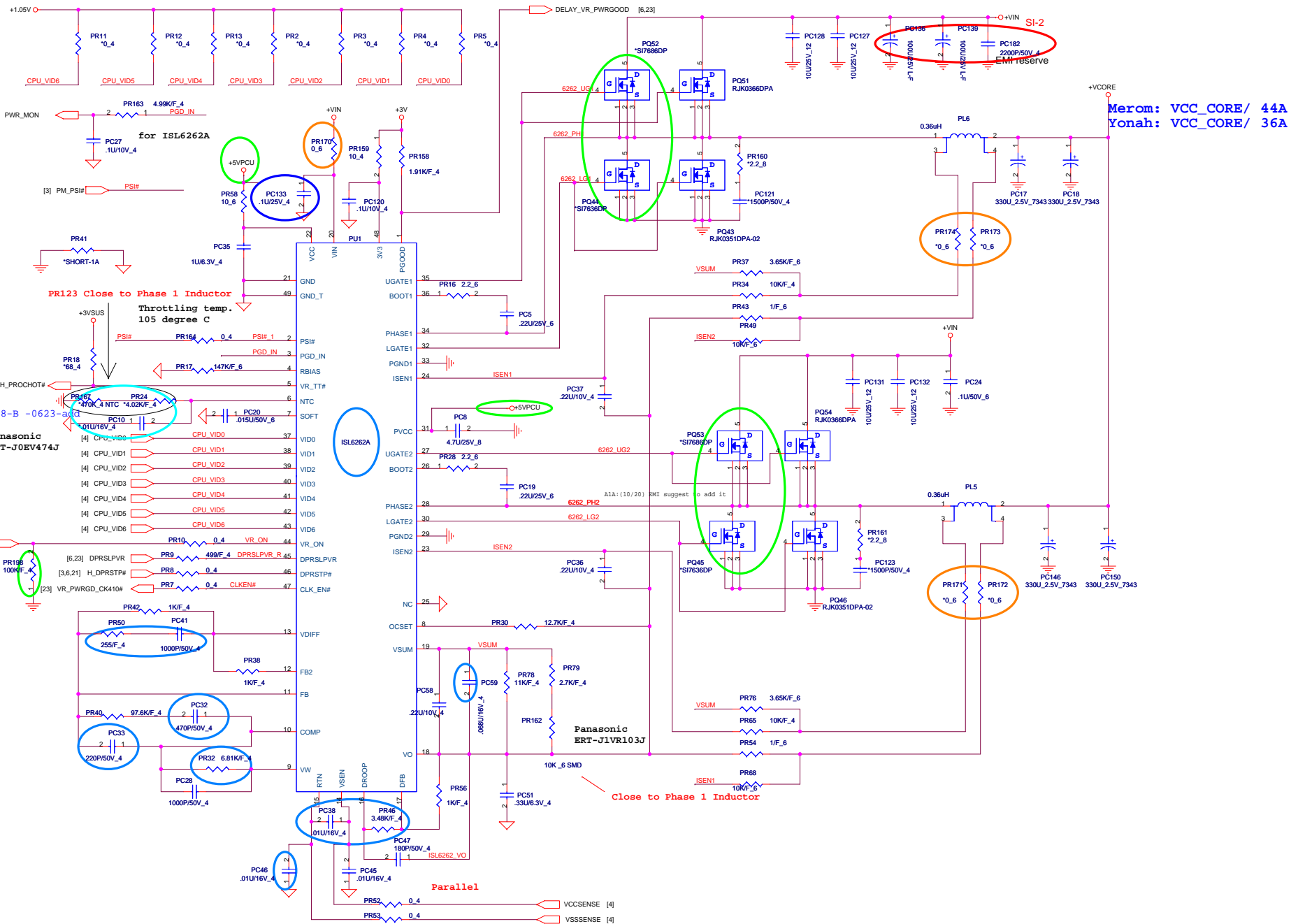
Size B	Document Number +5V/+3V (ISL6237)	Rev 1A
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VCCP1.05V & +1.5V

+1.05V Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A



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			Size B	Document Number +1.05V/+1.5V (RT8204)
Date: Tuesday, February 26, 2008			Sheet 40	of 44



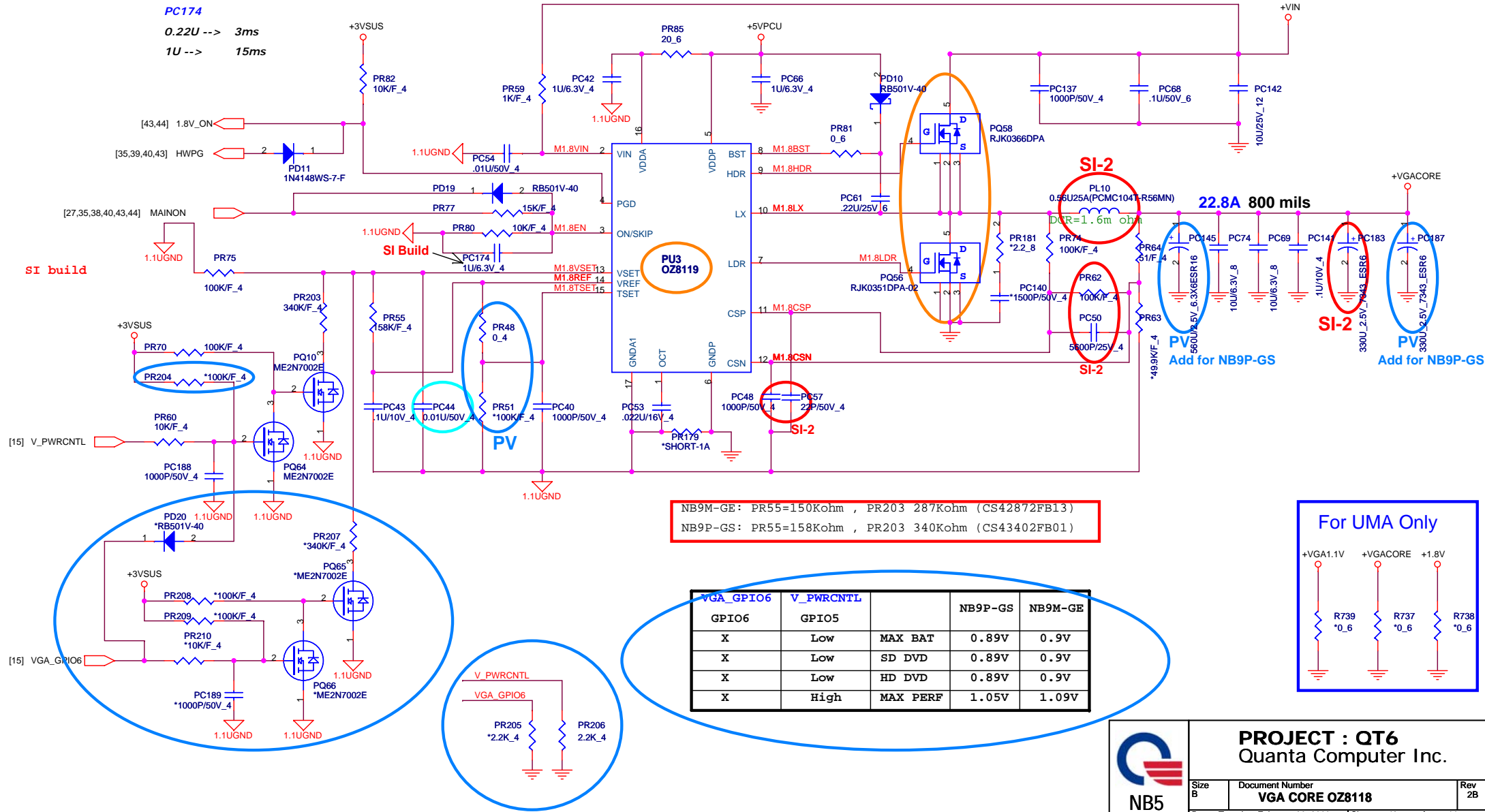
Merom: VCC_CORE/ 44A
 Yonah: VCC_CORE/ 36A

VGA Core & VCC1.1

+1.1Volt +/- 5%
 Countinue current:17.54A
 Peak current:22.8A
 OCP minimum 23A

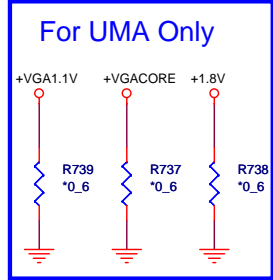
PC174

0.22U --> 3ms
 1U --> 15ms



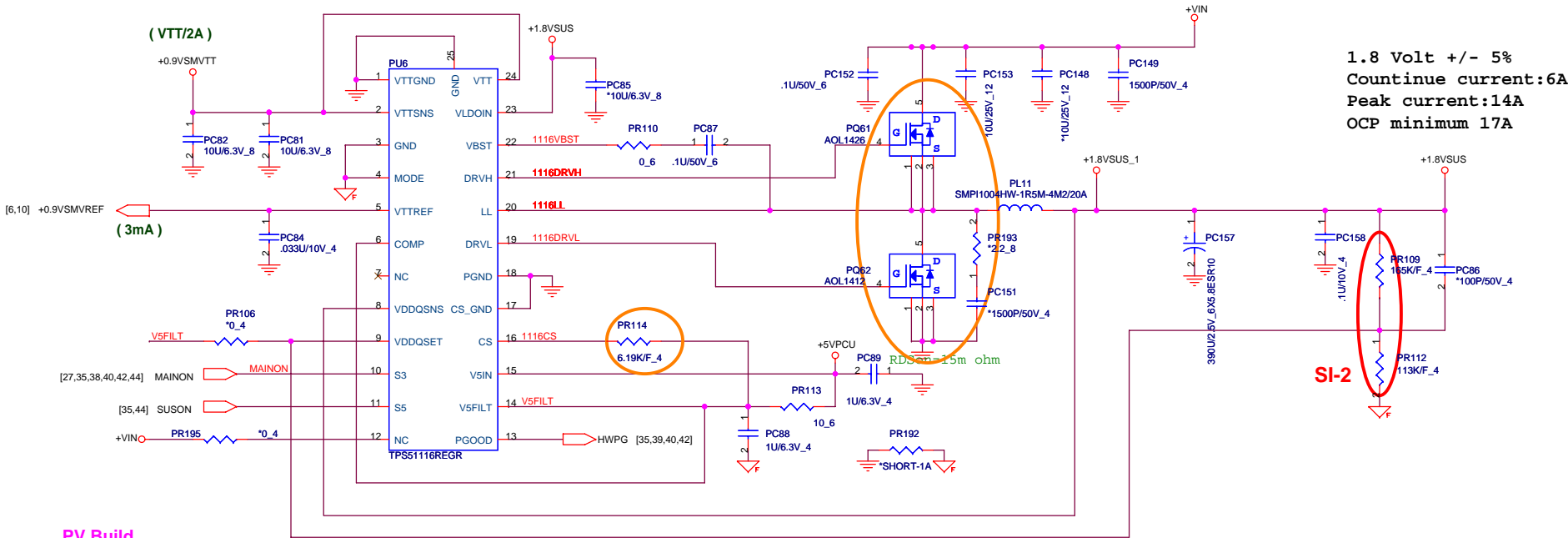
NB9M-GE: PR55=150Kohm , PR203 287Kohm (CS42872FB13)
 NB9P-GS: PR55=158Kohm , PR203 340Kohm (CS43402FB01)

VGA_GPIO6	V_PWRCTRL		NB9P-GS	NB9M-GE
X	Low	MAX BAT	0.89V	0.9V
X	Low	SD DVD	0.89V	0.9V
X	Low	HD DVD	0.89V	0.9V
X	High	MAX PERF	1.05V	1.09V



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 Quanta Computer Inc.

Size B	Document Number VGA CORE OZ8118	Rev 2B
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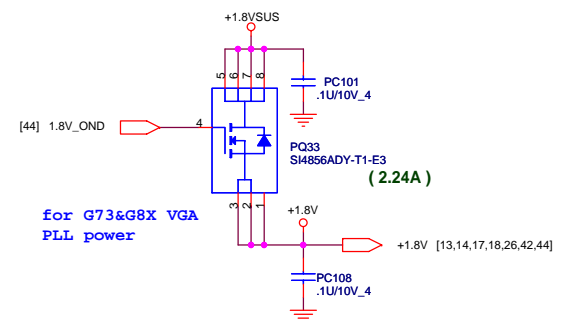
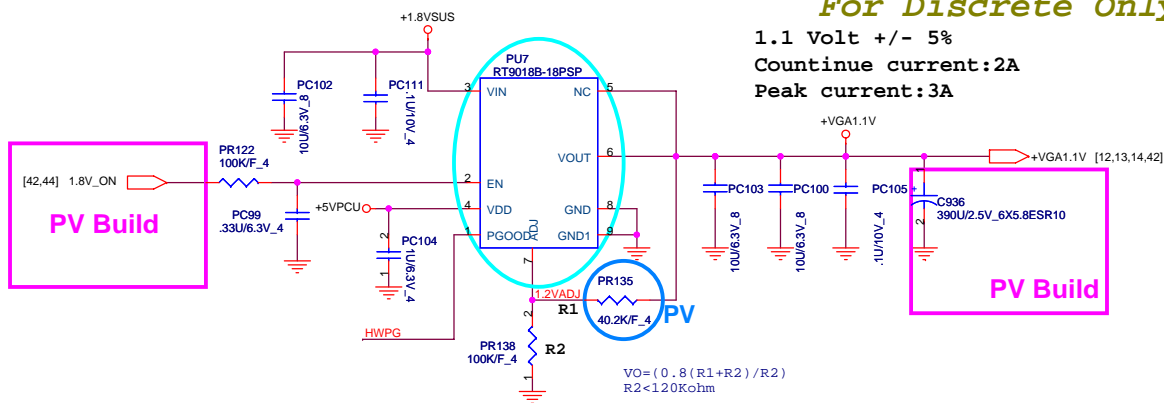


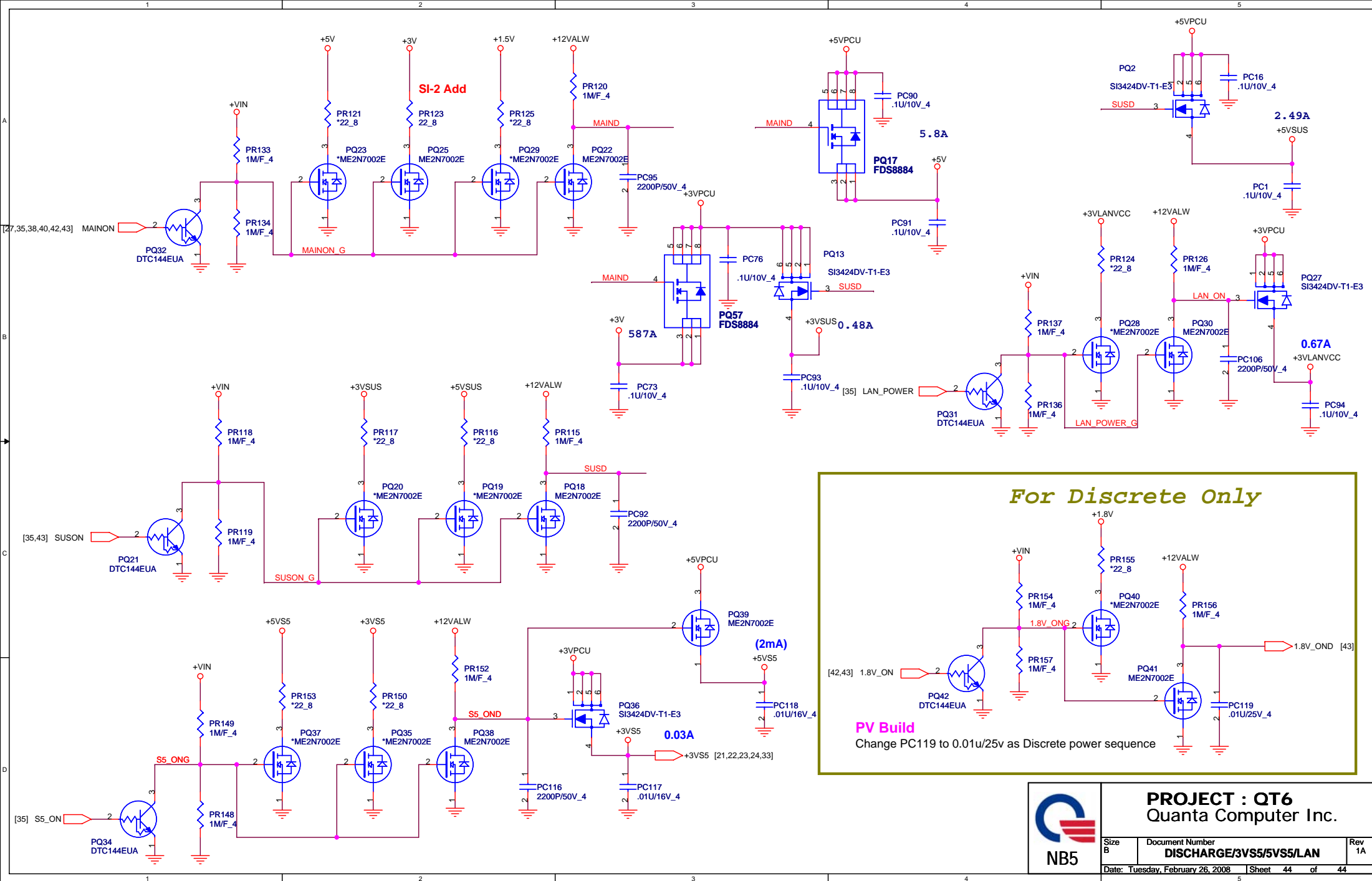
PV Build

Change PR122 tied to 1.8V_ON as power sequence request

For Discrete Only

1.1 Volt +/- 5%
 Continune current:2A
 Peak current:3A





For Discrete Only

PV Build
Change PC119 to 0.01u/25V as Discrete power sequence



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Size B	Document Number DISCHARGE/3VS5/5VS5/LAN	Rev 1A
Date: Tuesday, February 26, 2008	Sheet 44	of 44

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