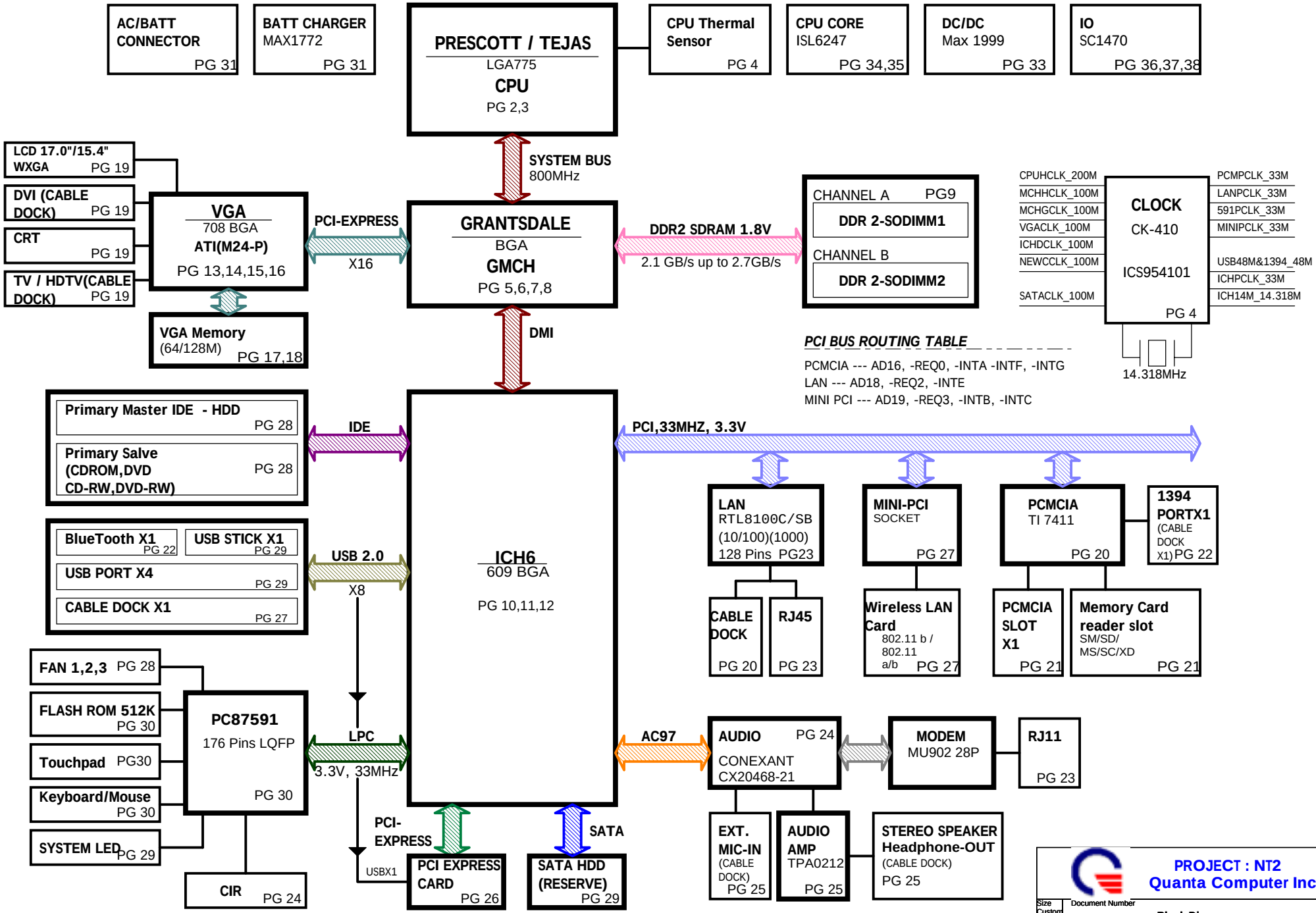
MODEL	REV	CHANGE LIST
NT2 M/B	1A	FIRST RELEASE
	2A	PAGE1: Change COREVTT power good circuit for CORE VCC Sequence. PAGE4,11: Add CPU PROCHOT CIRCUT (Throttle) at battery only. PAGE7: Because system 2.5V will change to 1.8V for support 1.8V VRAM so reserve one LED for support GMCH 2.5V voltage. PAGE11: Add one system ID for NT2B, and assign GPO19 pin to support CPU PROCHOT (Throttle) function. PAGE13: Add M24 GPIO14 to support TV_OUT select forTampa2, and reserve strap pin for VGA Memory tyep setting. PAGE14: Add LDO for VGA2.5 when system 2.5V change to 1.8V for suppport 1.8V VRAM. PAGE14: Reserve LDO of VGA1.5V for tune VGA power sequence. PAGE15: Add VGA BIOS "-ROMCS" control pin for support VRAM 256MB and reserve Memory type strip pin. PAGE16: Add Flash ROM for VGA BIOS. PAGE19: Modify DIODE Pin Deffine for BAV99 Part. PAGE21: Add pull up resister for XD "-CE" singnal. PAGE23: Reserve another LAN TRANSFORM FOR 10/100 and reserver one resister for LAN1.2V source and pull up resister for GIGA LAN transform terminal pin. PAGE24: Del CIR on board circuit and reserve CN37 for NT2B. PAGE24: Add resister to lower Cable Dock MIC signal and add more EMI PAD reserve. PAGE25: Modify Headphone CIRCUIT FOR CABLE DOCK. PAGE26: Change PCI EXPRESS Card power circuit - use TI TPS2331; and add CAP of Power plane bridge for EMI reserve. PAGE27: Cable Dock pin define change for match NP2 pin define and add one pin for TV-OUT select. PAGE27: Reserve always turn on the cable dock power circuit and change VA power to VAD. PAGE29: Add two connect for LED board and reserve two LED for NT2B. PAGE30: Add pull-up resister for Touch PAD power control and DIODE on "-SWI"&"-RUNSCI" for leakage, and reserve schottky diode and resister for VCC voltage undershoot issue. PAGE31: Add PD32 prevent power VAD with PWR_SRC leakage. PAGE31: Change PR146 and PR72 to 100K because PWM frequence change to 200Hz. PAGE32: Add 1.8V,VGACORE,VGA1.2V voltage discharge circuit. PAGE33: Add PR210 to fix MAX1999. PAGE34: Change PR180 to 0ohm and delete PC36 for COREVTTPWG signal delay time. PAGE34: Add PR203 NTC 4.7K to control cpu load line. PAGE36: Change 1.8VSUS and 1.5V power circuit of use MAX1845 for enhance transform efficiency. PAGE37: Change VGACORE of use LMV321 for enhance transform efficiency.

Model / Page	NT2 M/B BOARD FM	NT2 M/B BOARD TO
1	1A	2A
2	1A	
3	1A	
4	1A	2A
5	1A	
6	1A	
7	1A	2A
8	1A	
9	1A	
10	1A	
11	1A	2A
12	1A	
13	1A	2A
14	1A	2A
15	1A	2A
16	1A	2A
17	1A	
18	1A	
19	1A	2A
20	1A	
21	1A	
22	1A	
23	1A	2A
24	1A	2A
25	1A	2A
26	1A	2A
27	1A	2A
28	1A	
29	1A	2A
30	1A	2A
31	1A	2A
32	1A	2A
33	1A	2A
34	1A	2A
35	1A	2A
36	1A	2A
37	1A	2A
38	1A	2A

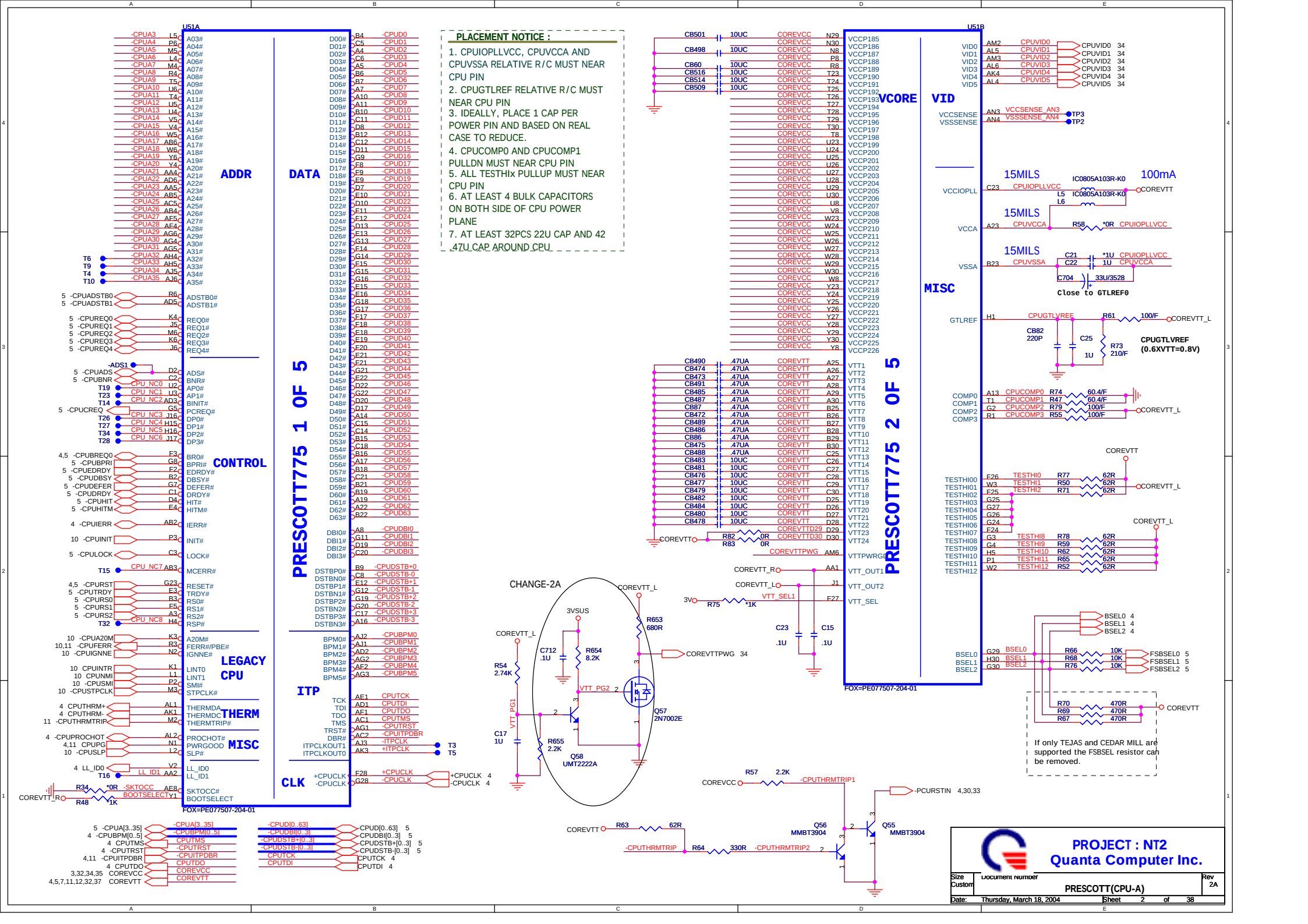
Quanta Computer Inc.	PROJECT:NT2	PCBA NO.	REV: 2A	DOC. NO: 204
	APPROVED BY :Tom Wang	CHECK BY:Carey Chen	DRAWING BY:Johnny O	DATE :03/05/2004 SHEET 1

NT2 - Block Diagram



PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A
Date: Thursday, March 18, 2004	Sheet 1 of 38	


PLACEMENT NOTICE :
1. CPUIOPLLVCC, CPUVCCA AND CPUVSSA RELATIVE R/C MUST NEAR CPU PIN
2. CPUGTLREF RELATIVE R/C MUST NEAR CPU PIN
3. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
4. CPUCOMP0 AND CPUCOMP1 PULLDN MUST NEAR CPU PIN
5. ALL TESTHIx PULLUP MUST NEAR CPU PIN
6. AT LEAST 4 BULK CAPACITORS ON BOTH SIDE OF CPU POWER PLANE
7. AT LEAST 32PCS 22U CAP AND 42 .47U CAP AROUND CPU
U51A
PRESCOTT775 1 OF 5
ADDR
DATA
CONTROL
LEGACY CPU
THERM
MISC
ITP
CLK
FOX=PE077507-204-01
U51B
PRESCOTT775 2 OF 5
VCORE
VID
MISC
FOX=PE077507-204-01
CHANGE-2A
If only TEJAS and CEDAR MILL are supported the FSBSEL resistor can be removed.
PROJECT : NT2
Quanta Computer Inc.
PRESCOTT(CPU-A)
Size: Custom
Document Number
Rev: 2A
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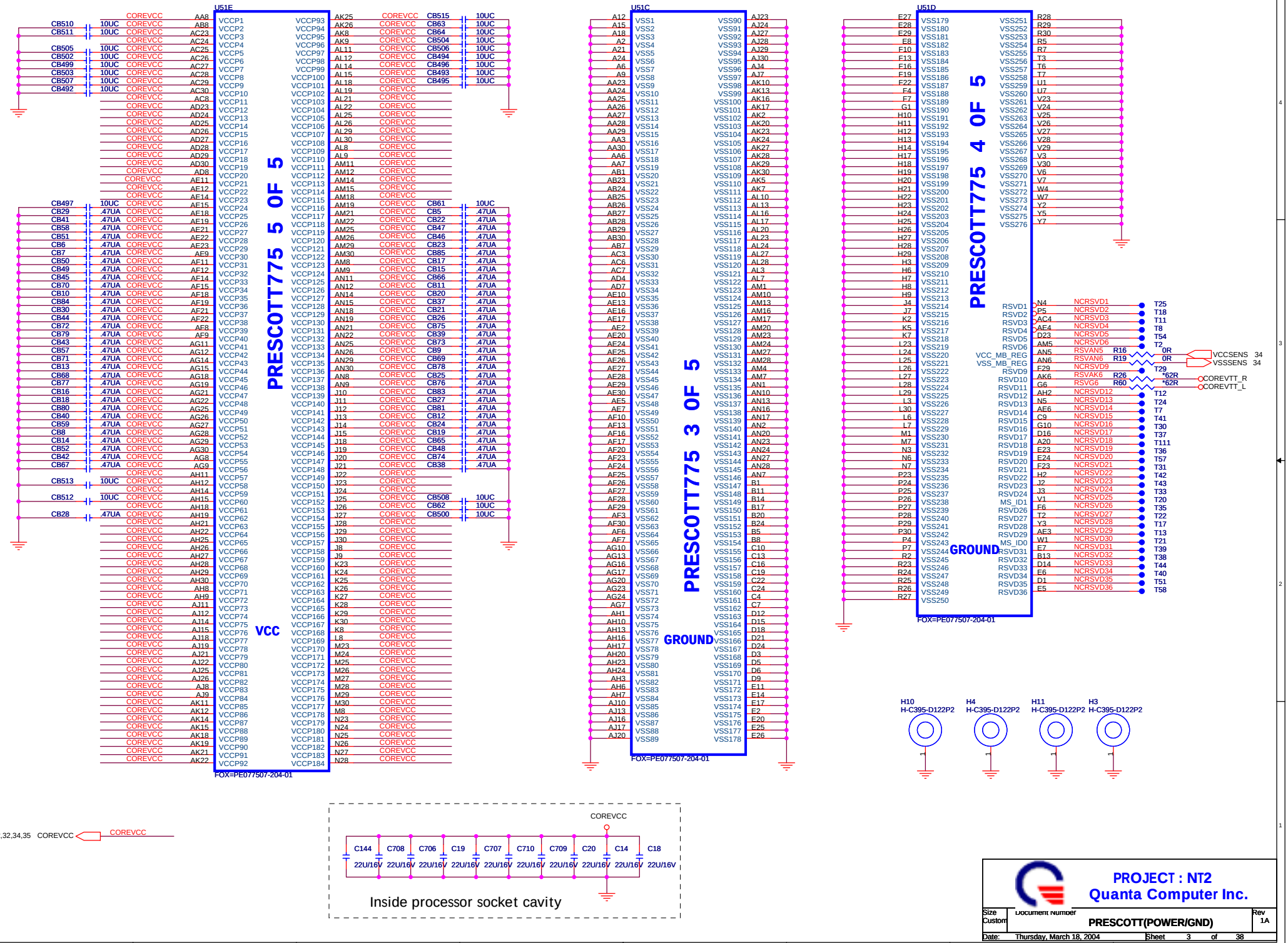
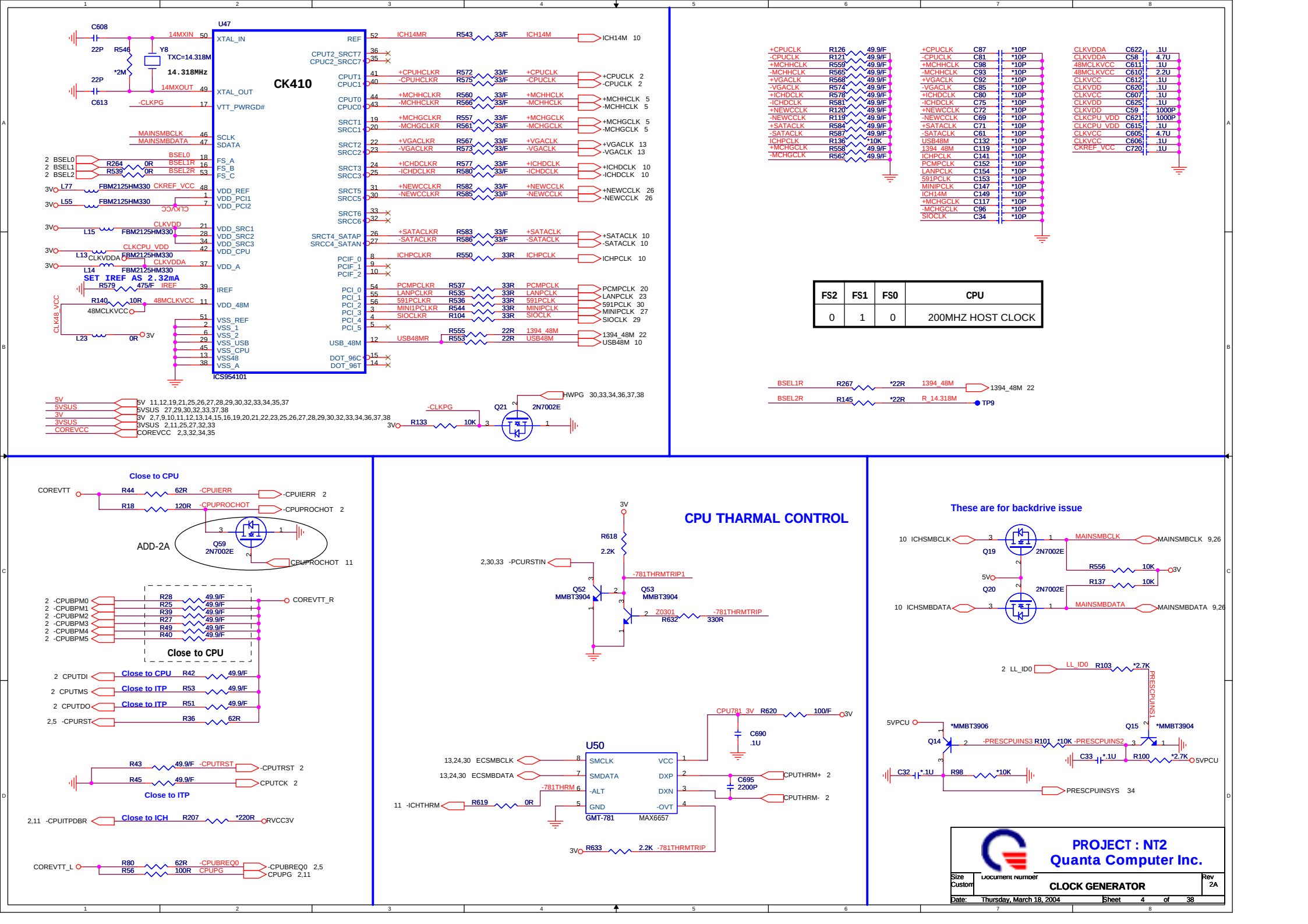

U51E
PRESCOTT775 5 OF 5
VCC
FOX=PE077507-204-01
U51C
PRESCOTT775 3 OF 5
GROUND
FOX=PE077507-204-01
U51D
PRESCOTT775 4 OF 5
GROUND
FOX=PE077507-204-01
2,32,34,35 COREVCC
COREVCC
C144 C708 C706 C19 C707 C710 C709 C20 C14 C18
22U/16V
Inside processor socket cavity
H10 H-C395-D122P2
H4 H-C395-D122P2
H11 H-C395-D122P2
H3 H-C395-D122P2
PROJECT : NT2
Quanta Computer Inc.
PRESCOTT(POWER/GND)
Size: Custom
Rev: 1A
Date: Thursday, March 18, 2004
Sheet 3 of 38


U47
CK410
ICS954101
XTAL_IN
XTAL_OUT
VTT_PWRGD#
SCLK
SDATA
FS_A
FS_B
FS_C
VDD_REF
VDD_PCI1
VDD_PCI2
VDD_SRC1
VDD_SRC2
VDD_SRC3
VDD_CPU
VDD_A
IREF
VDD_48M
VSS_REF
VSS_1
VSS_2
VSS_USB
VSS_CPU
VSS48
VSS_A
REF
CPUT2_SRCT7
CPUC2_SRCC7
CPUT1
CPUC1
CPUT0
CPUC0
SRCT1
SRCC1
SRCT2
SRCC2
SRCT3
SRCC3
SRCT5
SRCC5
SRCT6
SRCC6
SRCT4_SATAP
SRCC4_SATAN
PCIF_0
PCIF_1
PCIF_2
PCI_0
PCI_1
PCI_2
PCI_3
PCI_4
PCI_5
USB_48M
DOT_96C
DOT_96T
C608
22P
R546
*2M
Y8
TXC=14.318M
14.318MHz
22P
C613
14MXIN
14MXOUT
-CLKPG
MAINSMBCLK
MAINSMBDATA
BSEL0
BSEL1
BSEL2
R264
R539
0R
BSEL1R
BSEL2R
L77
FBM2125HM330
CKREF_VCC
L55
CLKVCC
CLKVDD
L15
CLKCPU_VDD
L13
CLKVDDA
L14
SET IREF AS 2.32mA
R579
475/F
IREF
R140
10R
48MCLKVCC
CLK48_VCC
L23
0R
3V
5V
5VSUS
3V
3VSUS
COREVCC
5V 11,12,19,21,25,26,27,28,29,30,32,33,34,35,37
5VSUS 27,29,30,32,33,37,38
3V 2,7,9,10,11,12,13,14,15,16,19,20,21,22,23,25,26,27,28,29,30,32,33,34,36,37,38
3VSUS 2,11,25,27,32,33
COREVCC 2,3,32,34,35
ICH14MR
R543
33/F
ICH14M
ICH14M 10
+CPUCLK 2
-CPUCLK 2
+MCHHCLK 5
-MCHHCLK 5
+MCHGCLK 5
-MCHGCLK 5
+VGACLK 13
-VGACLK 13
+ICHDCLK 10
-ICHDCLK 10
+NEWCCLK 26
-NEWCCLK 26
+SATACLK 10
-SATACLK 10
ICHPCLK
R550
33R
ICHPCLK 10
PCMPCLK
LANPCLK
591PCLK
MINIPCLK
SIOCLK
PCMPCLK 20
LANPCLK 23
591PCLK 30
MINIPCLK 27
SIOCLK 29
USB48MR
R553
22R
USB48M
1394_48M 22
USB48M 10
HWPG 30,33,34,36,37,38
-CLKPG
Q21
2N7002E
R133
10K
+CPUCLK R126 49.9/F
-CPUCLK R121 49.9/F
+MCHHCLK R569 49.9/F
-MCHHCLK R565 49.9/F
+VGACLK R568 49.9/F
-VGACLK R574 49.9/F
+ICHDCLK R578 49.9/F
-ICHDCLK R581 49.9/F
+NEWCCLK R120 49.9/F
-NEWCCLK R119 49.9/F
+SATACLK R584 49.9/F
-SATACLK R587 49.9/F
ICHPCLK R136 *10K
+MCHGCLK R558 49.9/F
-MCHGCLK R562 49.9/F
+CPUCLK C87 *10P
-CPUCLK C81 *10P
+MCHHCLK C98 *10P
-MCHHCLK C93 *10P
+VGACLK C92 *10P
-VGACLK C85 *10P
+ICHDCLK C80 *10P
-ICHDCLK C75 *10P
+NEWCCLK C72 *10P
-NEWCCLK C69 *10P
+SATACLK C71 *10P
-SATACLK C61 *10P
USB48M C132 *10P
1394_48M C119 *10P
ICHPCLK C141 *10P
PCMPCLK C152 *10P
LANPCLK C154 *10P
591PCLK C153 *10P
MINIPCLK C147 *10P
ICH14M C149 *10P
+MCHGCLK C117 *10P
-MCHGCLK C96 *10P
SIOCLK C34 *10P
CLKVDDA C622 .1U
CLKVDDA C58 4.7U
48MCLKVCC C611 .1U
48MCLKVCC C610 2.2U
CLKVCC C612 .1U
CLKVDD C620 .1U
CLKVCC C607 .1U
CLKVDD C625 .1U
CLKVDD C59 1000P
CLKCPU_VDD C621 1000P
CLKCPU_VDD C615 .1U
CLKVCC C605 4.7U
CLKVCC C606 .1U
CKREF_VCC C720 .1U
FS2 FS1 FS0 CPU
0 1 0 200MHZ HOST CLOCK
BSEL1R R267 *22R 1394_48M 1394_48M 22
BSEL2R R145 *22R R_14.318M TP9
Close to CPU
COREVTT
R44 62R -CPUIERR -CPUIERR 2
R18 120R -CPUPROCHOT -CPUPROCHOT 2
ADD-2A
Q59
2N7002E
CPUPROCHOT 11
2 -CPUBPM0
2 -CPUBPM1
2 -CPUBPM2
2 -CPUBPM3
2 -CPUBPM4
2 -CPUBPM5
R28 R25 R39 R27 R49 R40 49.9/F
COREVTT_R
Close to CPU
2 CPUTDI Close to CPU R42 49.9/F
2 CPUTMS Close to ITP R53 49.9/F
2 CPUTDO Close to ITP R51 49.9/F
2,5 -CPURST R36 62R
R43 49.9/F -CPUTRST -CPUTRST 2
R45 49.9/F CPUTCK 2
Close to ITP
2,11 -CPUITPDBR Close to ICH R207 *220R RVCC3V
COREVTT_L
R80 62R -CPUBREQ0 -CPUBREQ0 2,5
R56 100R CPUPG CPUPG 2,11
CPU THARMAL CONTROL
3V
R618
2.2K
2,30,33 -PCURSTIN
-781THRMTRIP1
Q52
MMBT3904
Q53
MMBT3904
Z0301
R632
330R
-781THRMTRIP
U50
SMCLK
SMDATA
-ALT
GND
VCC
DXP
DXN
-OVT
GMT-781
MAX6657
13,24,30 ECSMBCLK
13,24,30 ECSMBDATA
-781THRM
11 -ICHTHRM
R619
0R
CPU781_3V R620 100/F 3V
C690 .1U
C695 2200P
CPUTHRM+ 2
CPUTHRM- 2
3V R633 2.2K -781THRMTRIP
These are for backdrive issue
10 ICHSMBCLK
Q19
2N7002E
MAINSMBCLK
MAINSMBCLK 9,26
R556 10K 3V
5V
Q20
R137 10K
10 ICHSMBDATA
MAINSMBDATA
MAINSMBDATA 9,26
2 LL_ID0
LL_ID0 R103 *2.7K
PRESCPUINS1
5VPCU
*MMBT3906
Q14
Q15
*MMBT3904
-PRESCPUINS3 R101 *10K -PRESCPUINS2
C33 *.1U
R100 *2.7K 5VPCU
C32 *.1U
R98 *10K
PRESCPUINSYS 34
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
CLOCK GENERATOR
Rev 2A
Date: Thursday, March 18, 2004
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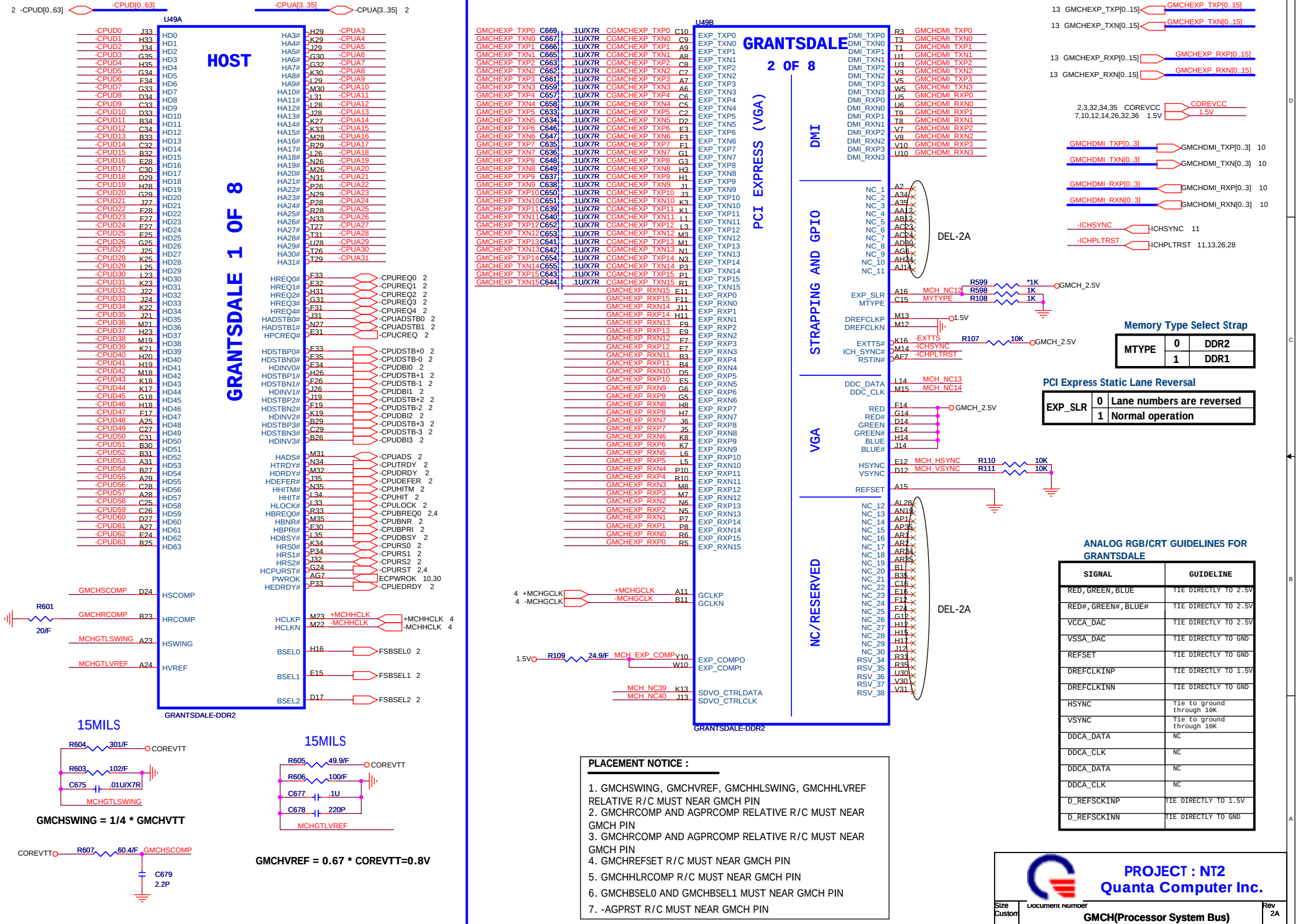
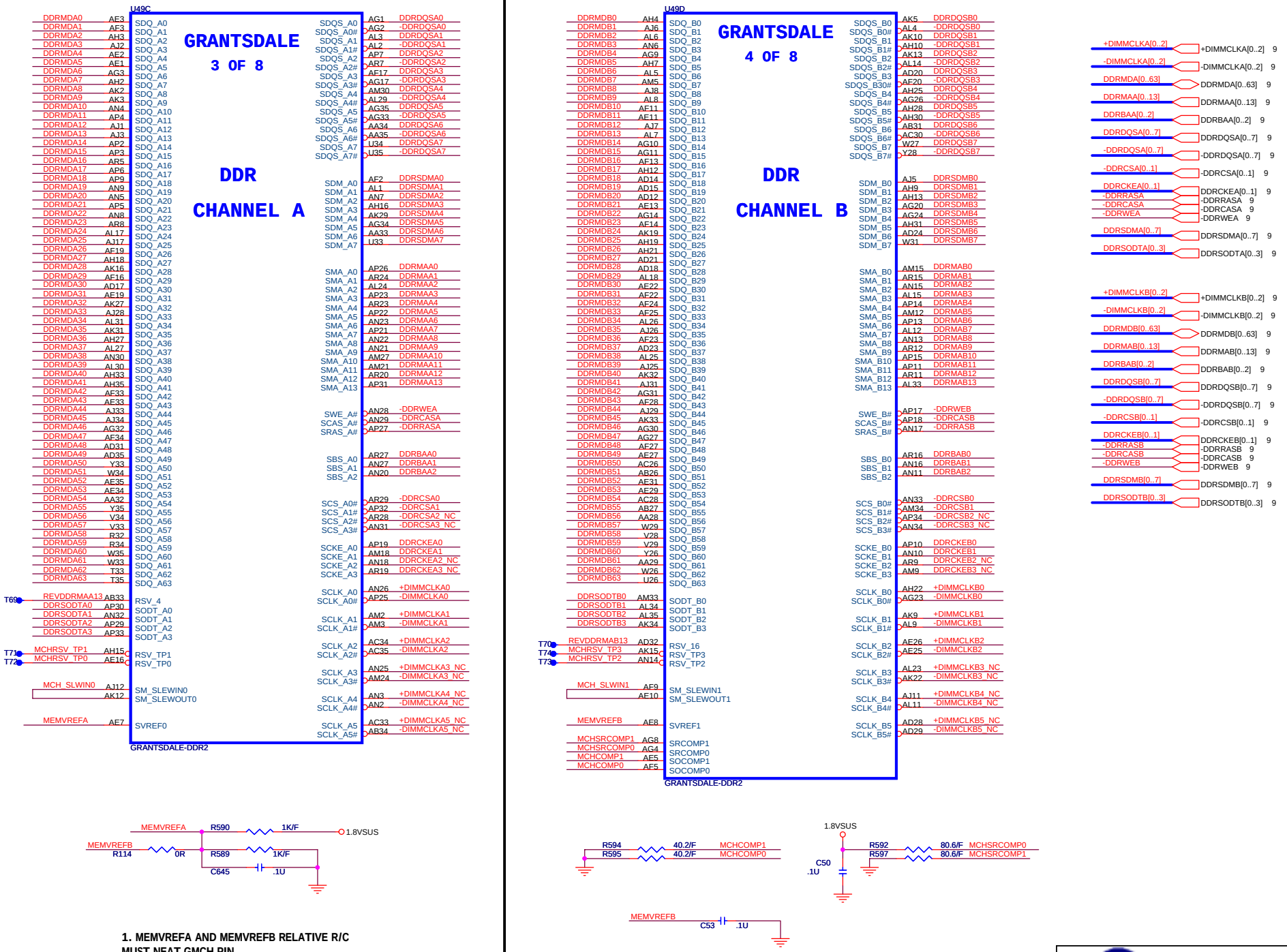

HOST
GRANTSDALE 1 OF 8
GRANTSDALE-DDR2
GRANTSDALE
2 OF 8
PCI EXPRESS (VGA)
DMI
STRAPPING AND GPIO
VGA
NC/RESERVED
DEL-2A
DEL-2A
GRANTSDALE-DDR2
Memory Type Select Strap
MTYPE 0 DDR2
1 DDR1
PCI Express Static Lane Reversal
EXP_SLR 0 Lane numbers are reversed
1 Normal operation
ANALOG RGB/CRT GUIDELINES FOR GRANTSDALE
SIGNAL GUIDELINE
RED,GREEN,BLUE TIE DIRECTLY TO 2.5V
RED#,GREEN#,BLUE# TIE DIRECTLY TO 2.5V
VCCA_DAC TIE DIRECTLY TO 2.5V
VSSA_DAC TIE DIRECTLY TO GND
REFSET TIE DIRECTLY TO GND
DREFCLKINP TIE DIRECTLY TO 1.5V
DREFCLKINN TIE DIRECTLY TO GND
HSYNC Tie to ground through 10K
VSYNC Tie to ground through 10K
DDCA_DATA NC
DDCA_CLK NC
DDCA_DATA NC
DDCA_CLK NC
D_REFSCKINP TIE DIRECTLY TO 1.5V
D_REFSCKINN TIE DIRECTLY TO GND
15MILS
GMCHSWING = 1/4 * GMCHVTT
15MILS
GMCHVREF = 0.67 * COREVTT=0.8V
PLACEMENT NOTICE :
1. GMCHSWING, GMCHVREF, GMCHHLSWING, GMCHHLVREF RELATIVE R/C MUST NEAR GMCH PIN
2. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
3. GMCHRCOMP AND AGPRCOMP RELATIVE R/C MUST NEAR GMCH PIN
4. GMCHREFSET R/C MUST NEAR GMCH PIN
5. GMCHHLRCOMP R/C MUST NEAR GMCH PIN
6. GMCHBSEL0 AND GMCHBSEL1 MUST NEAR GMCH PIN
7. -AGPRST R/C MUST NEAR GMCH PIN
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
GMCH(Processor System Bus)
Rev 2A
Date: Thursday, March 18, 2004
Sheet 5 of 38



1. MEMVREFA AND MEMVREFB RELATIVE R/C MUST NEAT GMCH PIN

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH DDR2 CHANNEL A	1A
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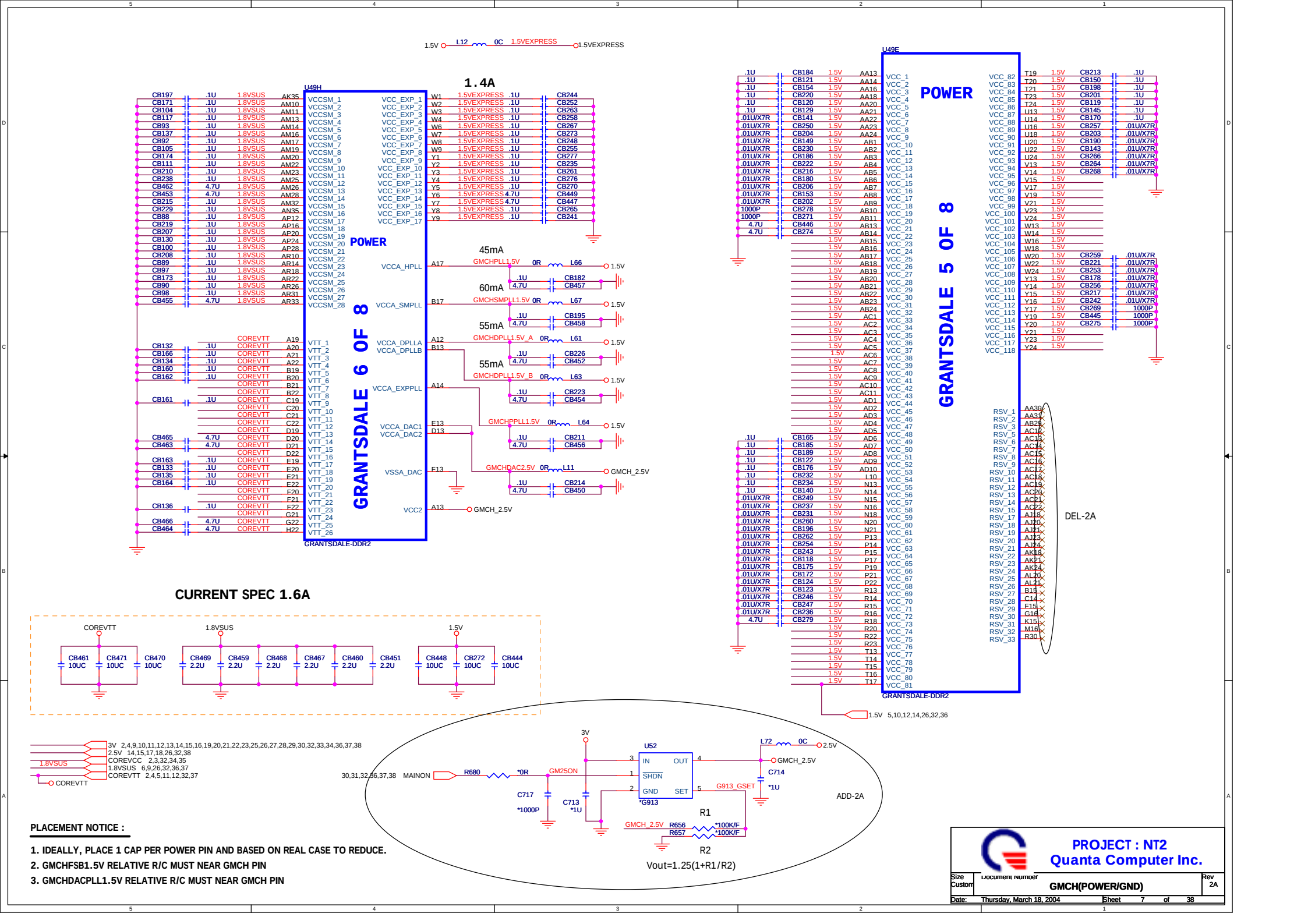
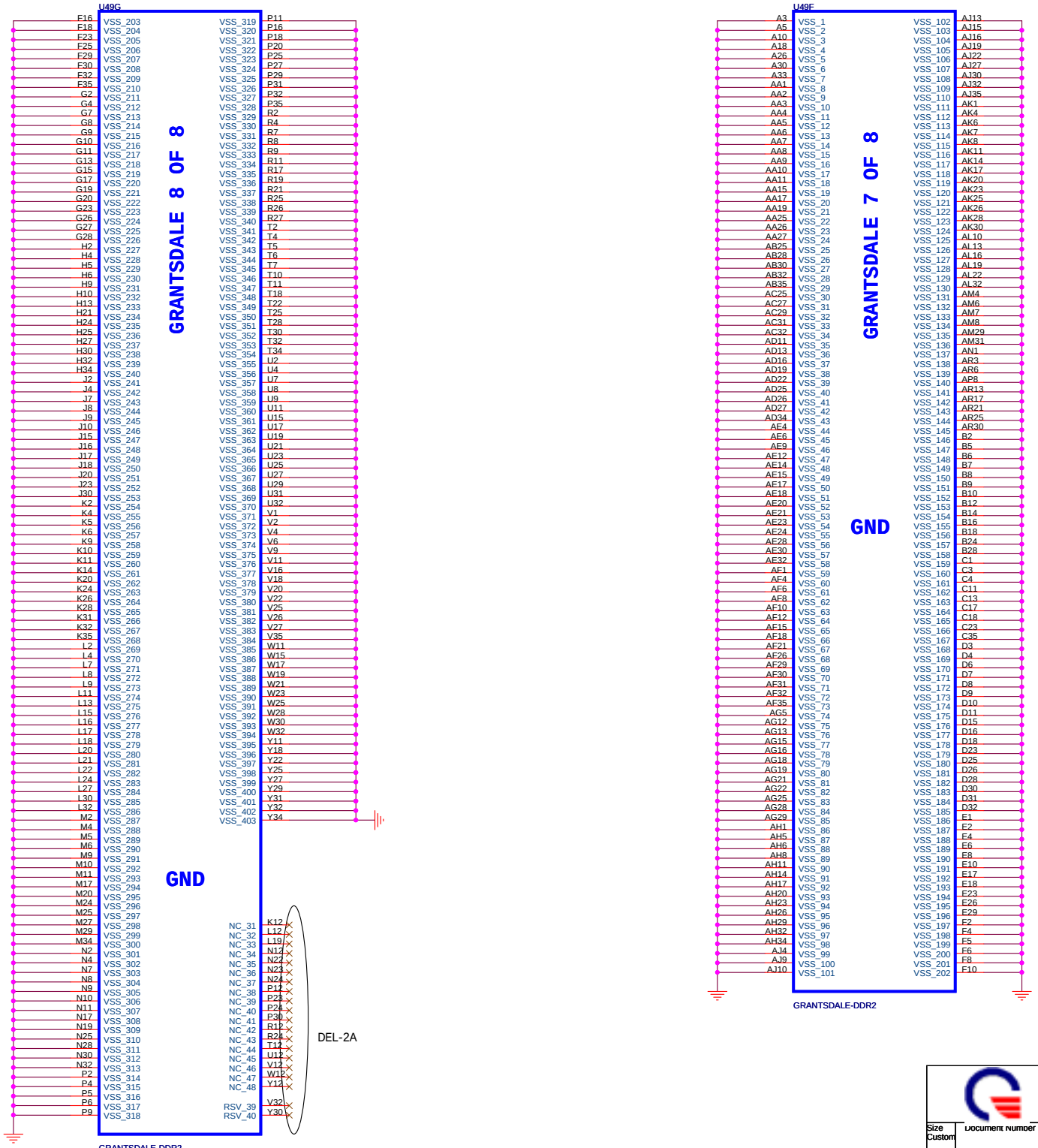

1.4A
45mA
60mA
55mA
55mA
U49H
POWER
GRANTSDALE 6 OF 8
GRANTSDALE-DDR2
U49E
POWER
GRANTSDALE 5 OF 8
GRANTSDALE-DDR2
DEL-2A
CURRENT SPEC 1.6A
COREVTT
1.8VSUS
1.5V
3V 2,4,9,10,11,12,13,14,15,16,19,20,21,22,23,25,26,27,28,29,30,32,33,34,36,37,38
2.5V 14,15,17,18,26,32,38
COREVCC 2,3,32,34,35
1.8VSUS 6,9,26,32,36,37
COREVTT 2,4,5,11,12,32,37
1.5V 5,10,12,14,26,32,36
MAINON
U52
ADD-2A
Vout=1.25(1+R1/R2)
PLACEMENT NOTICE :
1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. GMCHFSB1.5V RELATIVE R/C MUST NEAR GMCH PIN
3. GMCHDACPLL1.5V RELATIVE R/C MUST NEAR GMCH PIN
PROJECT : NT2
Quanta Computer Inc.
GMCH(POWER/GND)
Size Custom
Rev 2A
Date: Thursday, March 18, 2004
Sheet 7 of 38


U49G
GRANTSDALE 8 OF 8
GND
VSS_203 VSS_204 VSS_205 VSS_206 VSS_207 VSS_208 VSS_209 VSS_210 VSS_211 VSS_212 VSS_213 VSS_214 VSS_215 VSS_216 VSS_217 VSS_218 VSS_219 VSS_220 VSS_221 VSS_222 VSS_223 VSS_224 VSS_225 VSS_226 VSS_227 VSS_228 VSS_229 VSS_230 VSS_231 VSS_232 VSS_233 VSS_234 VSS_235 VSS_236 VSS_237 VSS_238 VSS_239 VSS_240 VSS_241 VSS_242 VSS_243 VSS_244 VSS_245 VSS_246 VSS_247 VSS_248 VSS_249 VSS_250 VSS_251 VSS_252 VSS_253 VSS_254 VSS_255 VSS_256 VSS_257 VSS_258 VSS_259 VSS_260 VSS_261 VSS_262 VSS_263 VSS_264 VSS_265 VSS_266 VSS_267 VSS_268 VSS_269 VSS_270 VSS_271 VSS_272 VSS_273 VSS_274 VSS_275 VSS_276 VSS_277 VSS_278 VSS_279 VSS_280 VSS_281 VSS_282 VSS_283 VSS_284 VSS_285 VSS_286 VSS_287 VSS_288 VSS_289 VSS_290 VSS_291 VSS_292 VSS_293 VSS_294 VSS_295 VSS_296 VSS_297 VSS_298 VSS_299 VSS_300 VSS_301 VSS_302 VSS_303 VSS_304 VSS_305 VSS_306 VSS_307 VSS_308 VSS_309 VSS_310 VSS_311 VSS_312 VSS_313 VSS_314 VSS_315 VSS_316 VSS_317 VSS_318
F16 F18 F23 F25 F29 F30 F32 F35 G2 G4 G7 G8 G9 G10 G11 G13 G15 G17 G19 G20 G23 G26 G27 G28 H2 H4 H5 H6 H9 H10 H13 H21 H24 H25 H27 H30 H32 H34 J2 J4 J7 J8 J9 J10 J15 J16 J17 J18 J20 J23 J30 K2 K4 K5 K6 K9 K10 K11 K14 K20 K24 K26 K28 K31 K32 K35 L2 L4 L7 L8 L9 L11 L13 L15 L16 L17 L18 L20 L21 L22 L24 L27 L30 L32 M2 M4 M5 M6 M9 M10 M11 M17 M20 M24 M25 M27 M29 M34 N2 N4 N7 N8 N9 N10 N11 N17 N19 N25 N28 N30 N32 P2 P4 P5 P6 P9
VSS_319 VSS_320 VSS_321 VSS_322 VSS_323 VSS_324 VSS_325 VSS_326 VSS_327 VSS_328 VSS_329 VSS_330 VSS_331 VSS_332 VSS_333 VSS_334 VSS_335 VSS_336 VSS_337 VSS_338 VSS_339 VSS_340 VSS_341 VSS_342 VSS_343 VSS_344 VSS_345 VSS_346 VSS_347 VSS_348 VSS_349 VSS_350 VSS_351 VSS_352 VSS_353 VSS_354 VSS_355 VSS_356 VSS_357 VSS_358 VSS_359 VSS_360 VSS_361 VSS_362 VSS_363 VSS_364 VSS_365 VSS_366 VSS_367 VSS_368 VSS_369 VSS_370 VSS_371 VSS_372 VSS_373 VSS_374 VSS_375 VSS_376 VSS_377 VSS_378 VSS_379 VSS_380 VSS_381 VSS_382 VSS_383 VSS_384 VSS_385 VSS_386 VSS_387 VSS_388 VSS_389 VSS_390 VSS_391 VSS_392 VSS_393 VSS_394 VSS_395 VSS_396 VSS_397 VSS_398 VSS_399 VSS_400 VSS_401 VSS_402 VSS_403
P11 P16 P18 P20 P25 P27 P29 P31 P32 P35 R2 R4 R7 R8 R9 R11 R17 R19 R21 R25 R26 R27 T2 T4 T5 T6 T7 T10 T11 T18 T22 T25 T28 T30 T32 T34 U2 U4 U7 U8 U9 U11 U15 U17 U19 U21 U23 U25 U27 U29 U31 U32 V1 V2 V4 V6 V9 V11 V16 V18 V20 V22 V25 V26 V27 V35 W11 W15 W17 W19 W21 W23 W25 W28 W30 W32 Y11 Y18 Y22 Y25 Y27 Y29 Y31 Y32 Y34
NC_31 NC_32 NC_33 NC_34 NC_35 NC_36 NC_37 NC_38 NC_39 NC_40 NC_41 NC_42 NC_43 NC_44 NC_45 NC_46 NC_47 NC_48
K12 L12 L19 N12 N21 N23 N24 P12 P23 P24 P30 R12 R24 T12 U12 V12 W12 Y12
RSV_39 RSV_40
V32 Y30
DEL-2A
GRANTSDALE-DDR2
U49F
GRANTSDALE 7 OF 8
GND
VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_32 VSS_33 VSS_34 VSS_35 VSS_36 VSS_37 VSS_38 VSS_39 VSS_40 VSS_41 VSS_42 VSS_43 VSS_44 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59 VSS_60 VSS_61 VSS_62 VSS_63 VSS_64 VSS_65 VSS_66 VSS_67 VSS_68 VSS_69 VSS_70 VSS_71 VSS_72 VSS_73 VSS_74 VSS_75 VSS_76 VSS_77 VSS_78 VSS_79 VSS_80 VSS_81 VSS_82 VSS_83 VSS_84 VSS_85 VSS_86 VSS_87 VSS_88 VSS_89 VSS_90 VSS_91 VSS_92 VSS_93 VSS_94 VSS_95 VSS_96 VSS_97 VSS_98 VSS_99 VSS_100 VSS_101
A3 A5 A10 A18 A26 A30 A33 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8 AA10 AA11 AA15 AA17 AA19 AA25 AA26 AA27 AB25 AB28 AB30 AB32 AB35 AC25 AC27 AC29 AC31 AC32 AD11 AD13 AD16 AD19 AD22 AD25 AD26 AD27 AD34 AE4 AE6 AE9 AE12 AE14 AE15 AE17 AE18 AE20 AE21 AE23 AE24 AE28 AE30 AE32 AF1 AF4 AF6 AF8 AF10 AF12 AF15 AF18 AF21 AF26 AF29 AF30 AF31 AF32 AF35 AG5 AG12 AG13 AG15 AG16 AG18 AG19 AG21 AG22 AG25 AG28 AG29 AH1 AH5 AH6 AH8 AH11 AH14 AH17 AH20 AH23 AH26 AH29 AH32 AH34 AJ4 AJ9 AJ10
VSS_102 VSS_103 VSS_104 VSS_105 VSS_106 VSS_107 VSS_108 VSS_109 VSS_110 VSS_111 VSS_112 VSS_113 VSS_114 VSS_115 VSS_116 VSS_117 VSS_118 VSS_119 VSS_120 VSS_121 VSS_122 VSS_123 VSS_124 VSS_125 VSS_126 VSS_127 VSS_128 VSS_129 VSS_130 VSS_131 VSS_132 VSS_133 VSS_134 VSS_135 VSS_136 VSS_137 VSS_138 VSS_139 VSS_140 VSS_141 VSS_142 VSS_143 VSS_144 VSS_145 VSS_146 VSS_147 VSS_148 VSS_149 VSS_150 VSS_151 VSS_152 VSS_153 VSS_154 VSS_155 VSS_156 VSS_157 VSS_158 VSS_159 VSS_160 VSS_161 VSS_162 VSS_163 VSS_164 VSS_165 VSS_166 VSS_167 VSS_168 VSS_169 VSS_170 VSS_171 VSS_172 VSS_173 VSS_174 VSS_175 VSS_176 VSS_177 VSS_178 VSS_179 VSS_180 VSS_181 VSS_182 VSS_183 VSS_184 VSS_185 VSS_186 VSS_187 VSS_188 VSS_189 VSS_190 VSS_191 VSS_192 VSS_193 VSS_194 VSS_195 VSS_196 VSS_197 VSS_198 VSS_199 VSS_200 VSS_201 VSS_202
AJ13 AJ15 AJ16 AJ19 AJ22 AJ27 AJ30 AJ32 AJ35 AK1 AK4 AK6 AK7 AK8 AK11 AK14 AK17 AK20 AK23 AK25 AK26 AK28 AK30 AL10 AL13 AL16 AL19 AL22 AL32 AM4 AM6 AM7 AM8 AM29 AM31 AN1 AR3 AR6 AP8 AR13 AR17 AR21 AR25 AR30 B2 B5 B6 B7 B8 B9 B10 B12 B14 B16 B18 B24 B28 C1 C3 C4 C11 C13 C17 C18 C23 C35 D3 D4 D6 D7 D8 D9 D10 D11 D15 D16 D18 D23 D25 D26 D28 D30 D31 D32 E1 E2 E4 E6 E8 E10 E17 E18 E23 E26 E29 F2 F4 F5 F6 F8 F10
GRANTSDALE-DDR2
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
GMCH(POWER/GND)-2
Rev 2A
Date: Thursday, March 18, 2004
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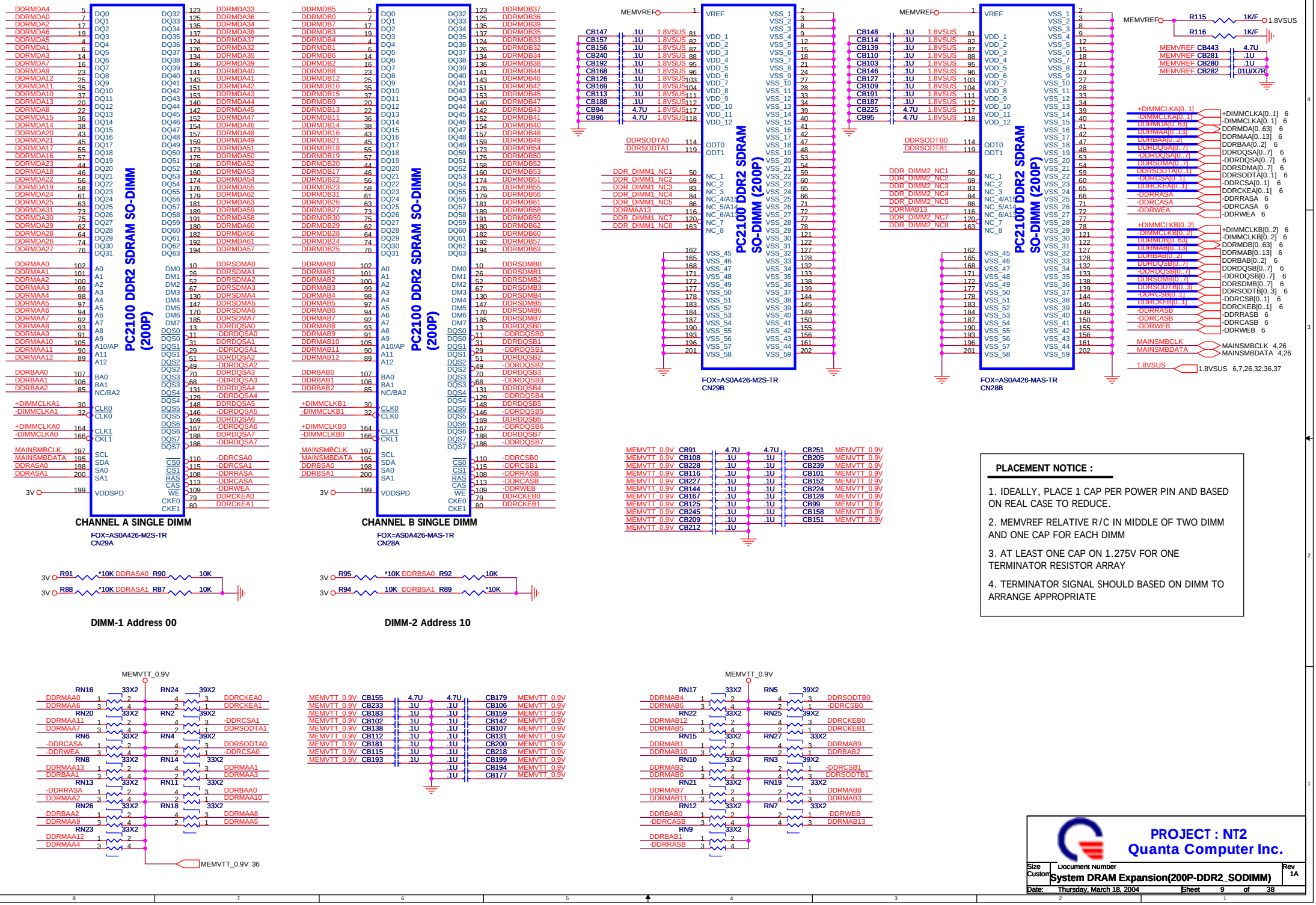
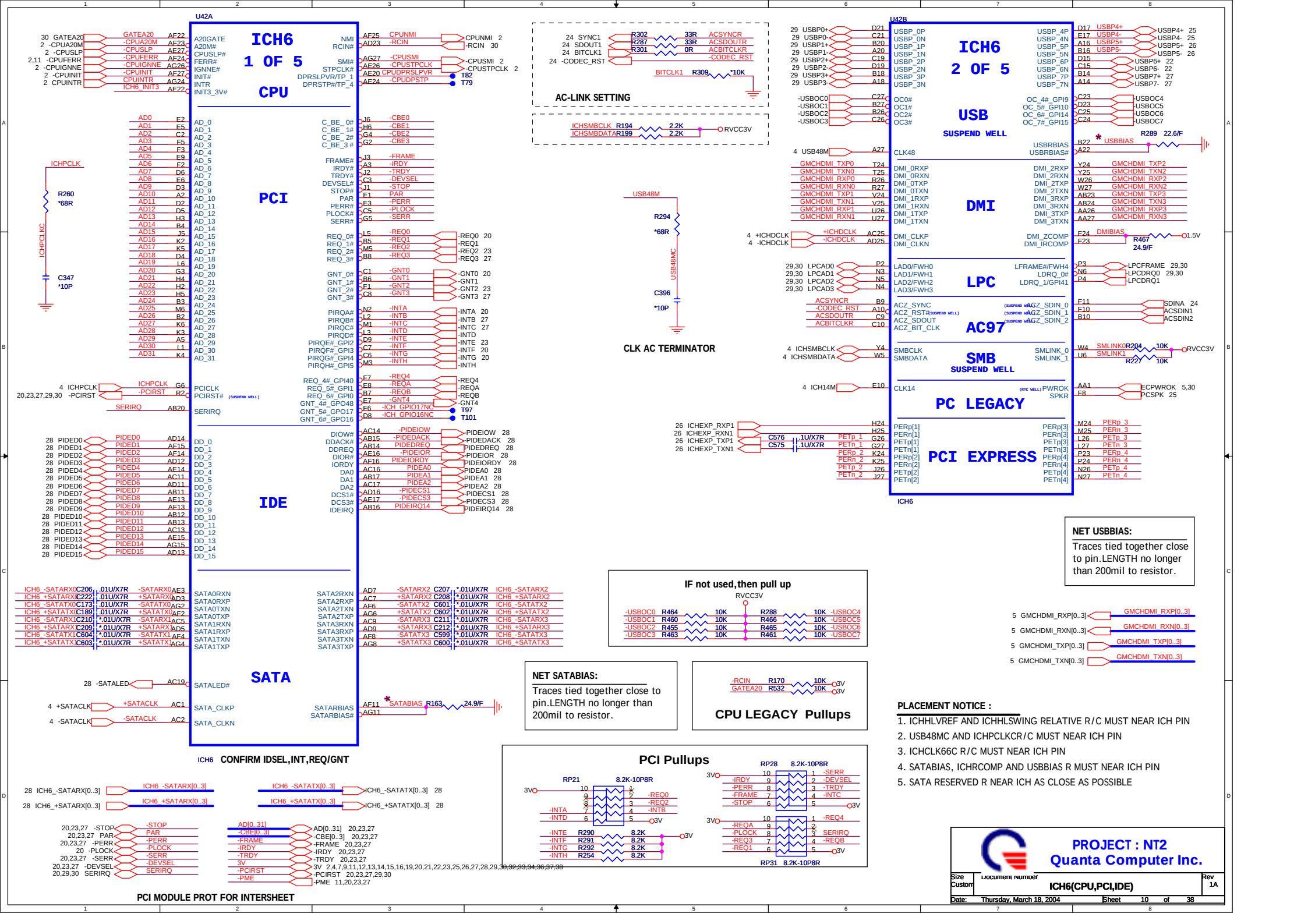

CHANNEL A SINGLE DIMM
FOX=AS0A426-M2S-TR
CN29A
CHANNEL B SINGLE DIMM
FOX=AS0A426-MAS-TR
CN28A
PC2100 DDR2 SDRAM SO-DIMM (200P)
FOX=AS0A426-M2S-TR
CN29B
FOX=AS0A426-MAS-TR
CN28B
DIMM-1 Address 00
DIMM-2 Address 10
PLACEMENT NOTICE :
1. IDEALLY, PLACE 1 CAP PER POWER PIN AND BASED ON REAL CASE TO REDUCE.
2. MEMVREF RELATIVE R/C IN MIDDLE OF TWO DIMM AND ONE CAP FOR EACH DIMM
3. AT LEAST ONE CAP ON 1.275V FOR ONE TERMINATOR RESISTOR ARRAY
4. TERMINATOR SIGNAL SHOULD BASED ON DIMM TO ARRANGE APPROPRIATE
PROJECT : NT2
Quanta Computer Inc.
System DRAM Expansion(200P-DDR2_SODIMM)
Thursday, March 18, 2004

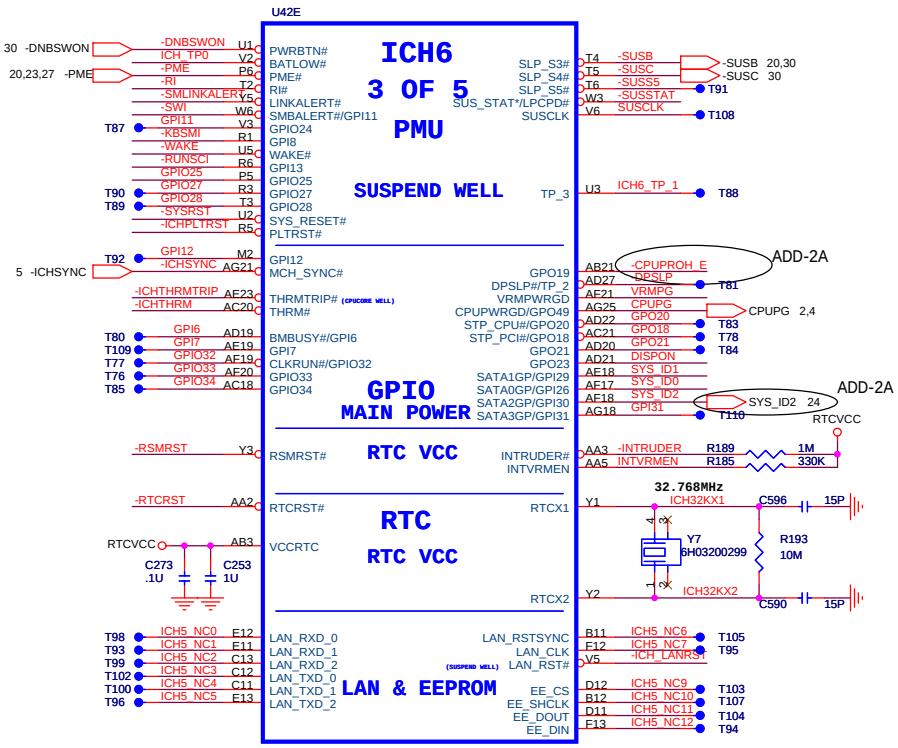

ICH6 1 OF 5 CPU
PCI
IDE
SATA
ICH6 2 OF 5
USB
SUSPEND WELL
DMI
LPC
AC97
SMB
SUSPEND WELL
PC LEGACY
PCI EXPRESS
ICH6
AC-LINK SETTING
CLK AC TERMINATOR
IF not used,then pull up
RVCC3V
NET USBBIAS:
Traces tied together close to pin.LENGTH no longer than 200mil to resistor.
NET SATABIAS:
Traces tied together close to pin.LENGTH no longer than 200mil to resistor.
CPU LEGACY Pullups
PCI Pullups
RP21 8.2K-10P8R
RP28 8.2K-10P8R
RP31 8.2K-10P8R
ICH6 CONFIRM IDSEL,INT,REQ/GNT
PCI MODULE PROT FOR INTERSHEET
PLACEMENT NOTICE :
1. ICHHLVREF AND ICHHLSWING RELATIVE R/C MUST NEAR ICH PIN
2. USB48MC AND ICHPCLKCR/C MUST NEAR ICH PIN
3. ICHCLK66C R/C MUST NEAR ICH PIN
4. SATABIAS, ICHRCOMP AND USBBIAS R MUST NEAR ICH PIN
5. SATA RESERVED R NEAR ICH AS CLOSE AS POSSIBLE
PROJECT : NT2
Quanta Computer Inc.
ICH6(CPU,PCI,IDE)
Size: Custom
Rev: 1A
Date: Thursday, March 18, 2004
Sheet 10 of 38

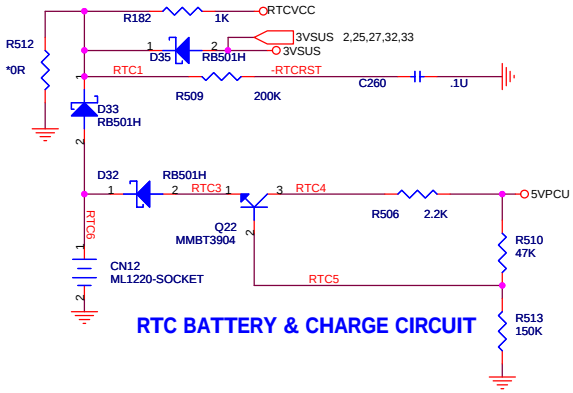
GPIO PIN DEFINE

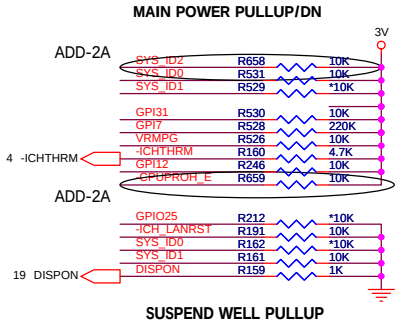
GPI6		
GPI7		PULL UP
GPI8	-KBSMI	PULL UP
GPI11	-SWI	PULL UP
GPI12		PULL UP
GPI13	-RUNSCI	PULL UP
GPI26	SYS_ID0	PULL UP
GPI29	SYS_ID1	PULL LO
GPI30		PULL UP
GPI31		PULL UP
GPO18		SET OUTPUT
GPO19		SET OUTPUT
GPO20		SET OUTPUT
GPO21		SET OUTPUT
GPO23	DISPON	SET OUTPUT
GPIO24		SET OUTPUT
GPO49	CPUPG	SET OUTPUT
GPIO25		SET OUTPUT
GPIO27		SET OUTPUT
GPIO28		SET OUTPUT
GPIO32		SET OUTPUT
GPIO33		SET OUTPUT
GPIO34		SET OUTPUT

Functional Straps

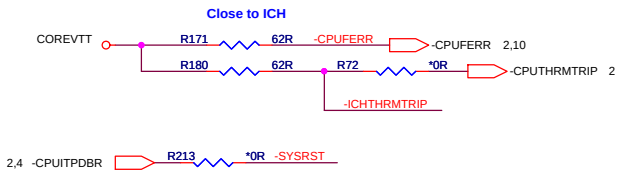
GNT[6]#/ GPO[16]	**Top-Block Swap Override**
	Pull-Low : "top-block swap" mode
LINKALERT#	**Reserved**
	Requires an external pull-up resistor.
SPKR	**No Reboot**
	Pull-up : "No Reboot" mode
INTVRMEN	**Integrated VccSus1.5 VRM enable/disable**
	Pull-up : Enable integrated VccSus1.5V VRM
GPIO[25]	**Integrated Vcc2.5 VRM enable/disable**
	Pull-Low : Enable inegrated Vcc2.5 VRM
EE_CS	**Reserved**
	iternal pull-down & should not be pull-high
GNT[5]#/ GPO[17]	**Boot BIOS Desination Selection**
	This functionality for debug/testing only
EE_DOUT	**Reserved**
	iternal pull-up & should not be pull-low
ACZ_SDOUT	**XOR chain Entrance / PCI Express port config bit1**
	Pull-low : allows entrance to XOR Chain testing
ACZ_SYNC	**PCI Express Port Config bit 0**
	This signal has a weak internal pull-down
TP[1]	iternal pull-down & should not be pull-high
STATLED#	iternal pull-up & should not be pull-low
REQ[4:1]	**XOR Chain Selection / See Chapter 8**
TP[3]	**XOR Chain Entrance / See Chapter 8** This signal should not be Pull-low unless using XOR Chain testing

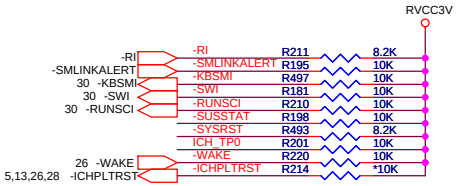


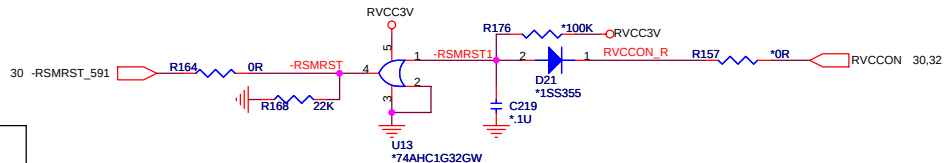


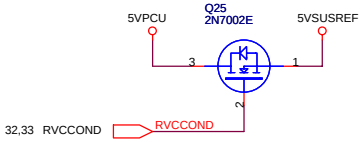


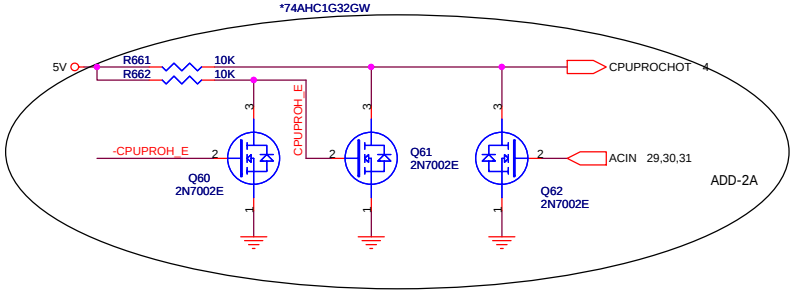
ASSUME S5 SUPPORT











DESIGN CHECK LIST :

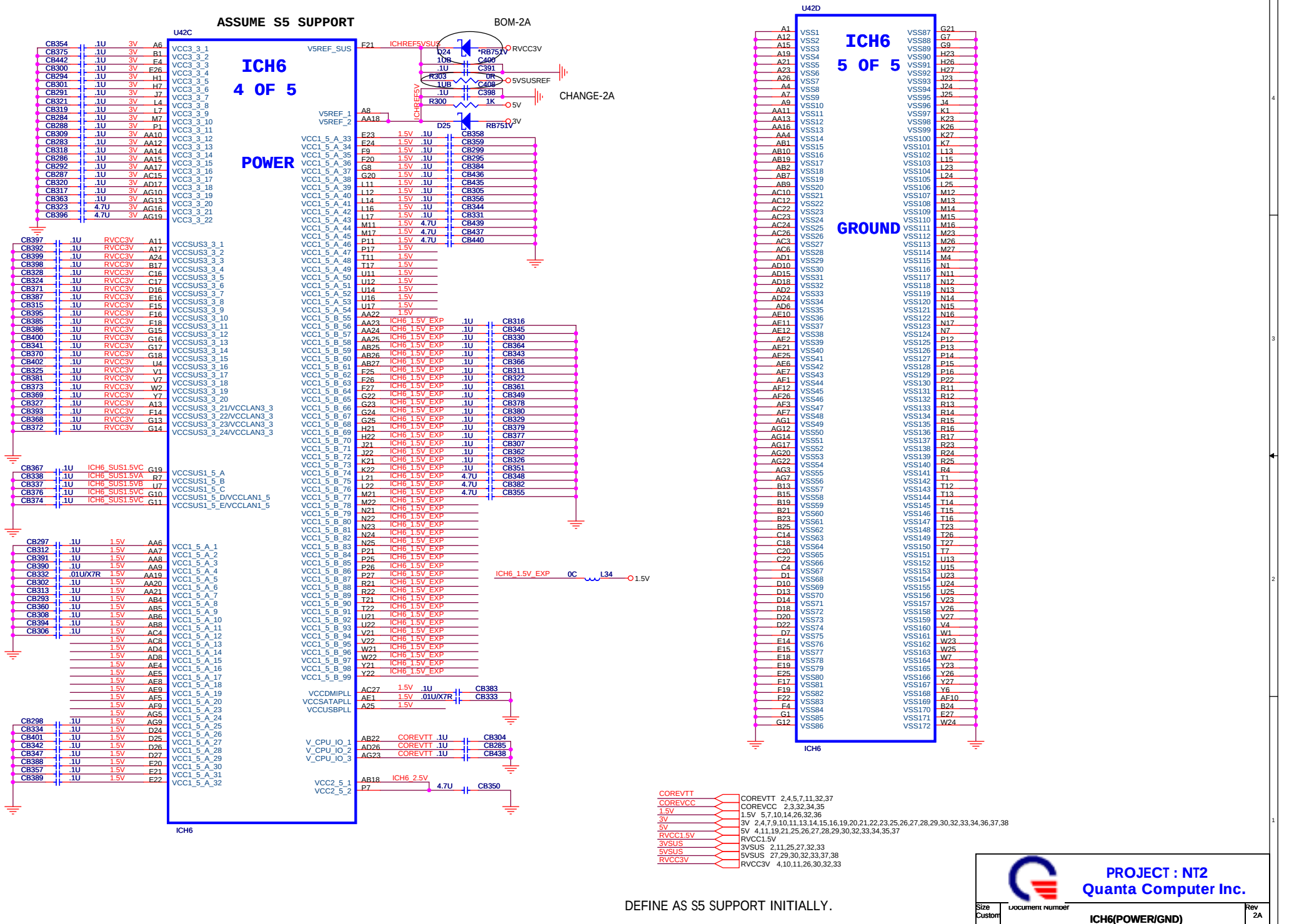
1. CLASSIFY THE POWER PLANE FOR PMU AND GPIO PIN
2. CLASSIFY GPI AND GPO PIN
3. COMMON PIN FOR PMU INPUT: -PME, BATLOW, -RI, -WAKESCI, RUNSCI, KBSMI AND -DNBSWON
4. USUALLY USED GPIO PIN : DISPON, CRTSENSE, SPKOFF
5. USUALLY USED CLK CONTRL PIN : -CPUSTP, -PCISTP, -SUSA AND -SUSSTAT
6. AGP PMU PIN : -AGPBUSY AND -STPAGP
7. CHECK -PCIRST BUFFERAND PWROK SIGNAL
8. CHECK -RSMRST CIRCUI

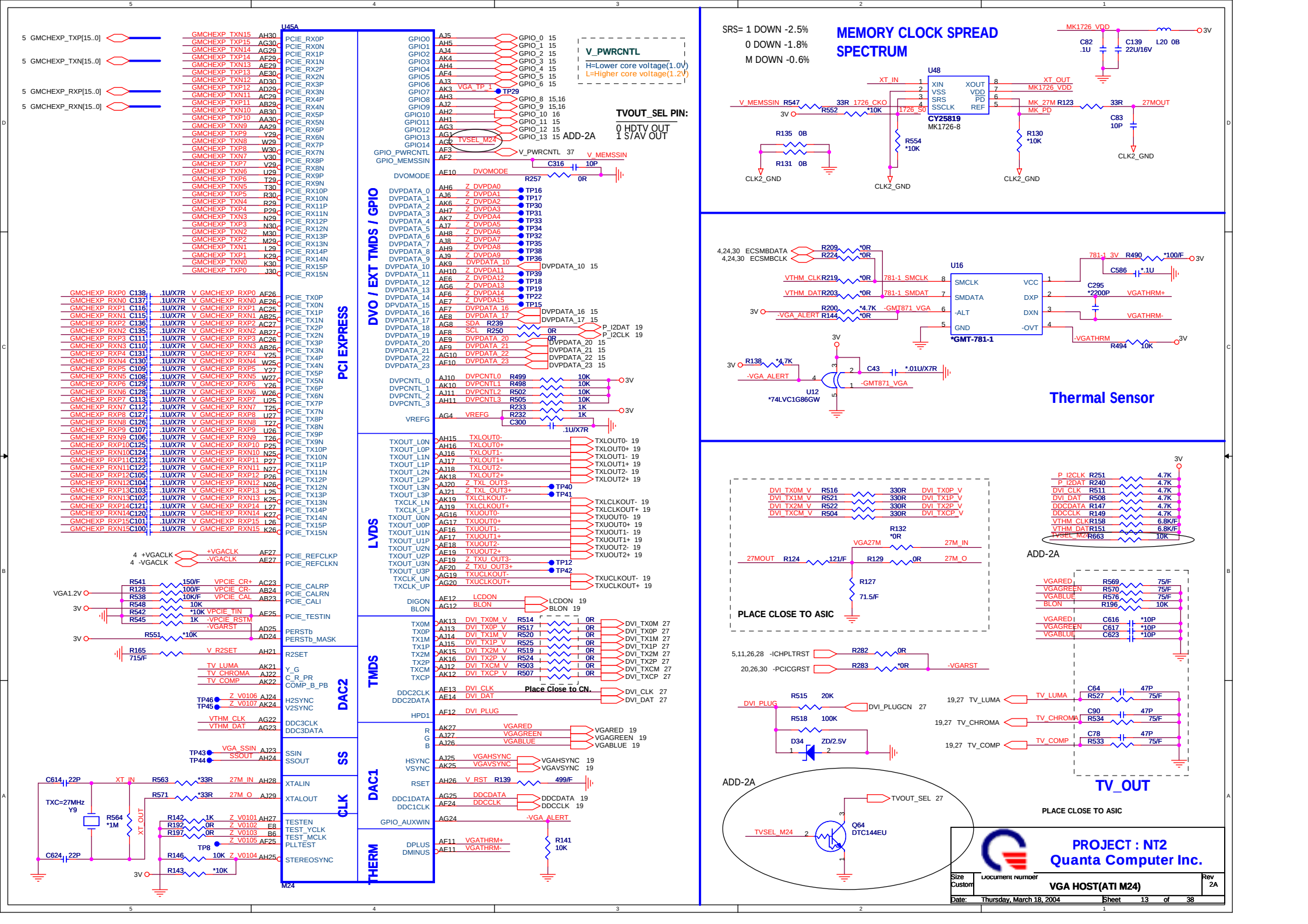
PLACEMENT NOTICE :

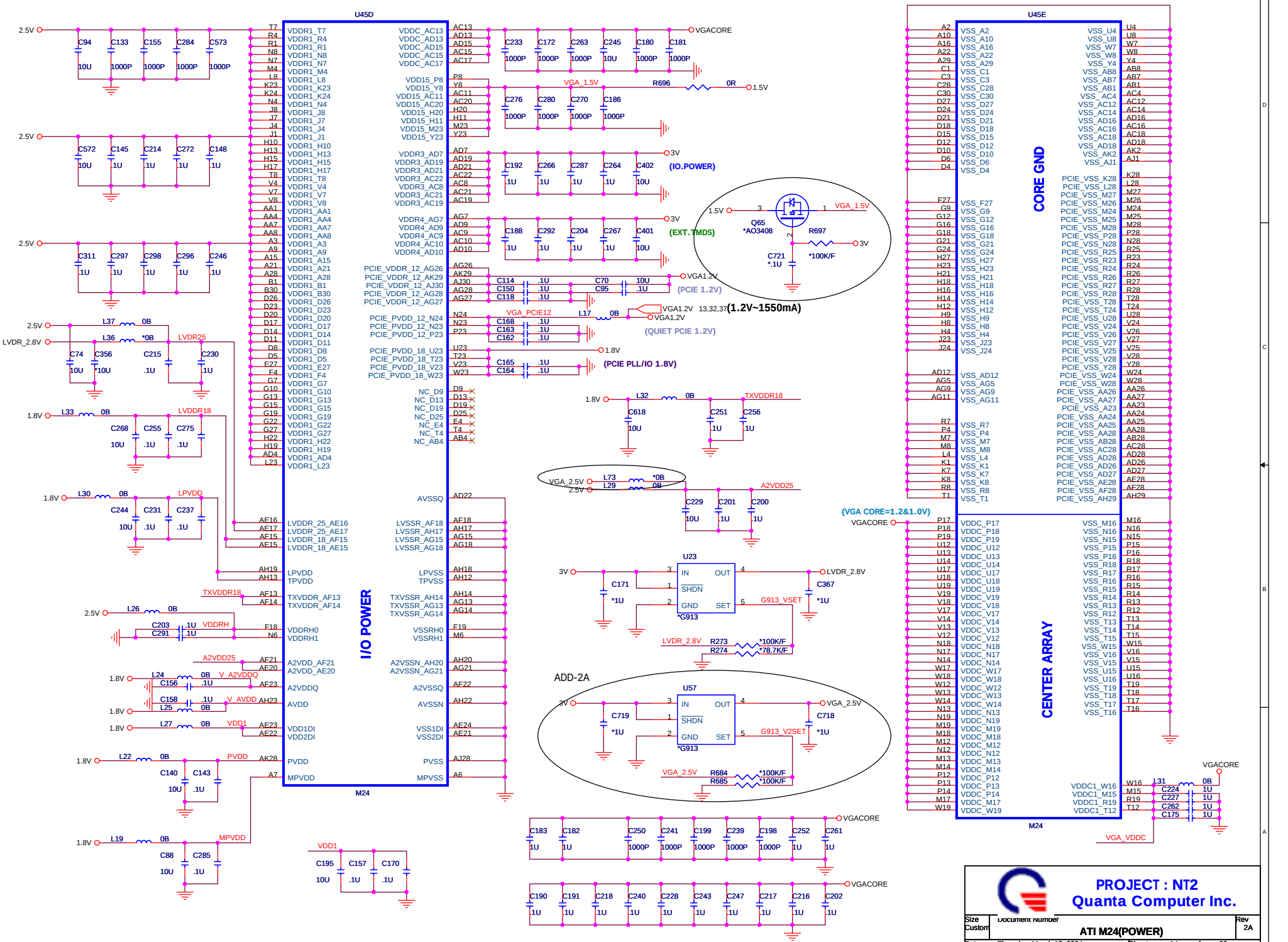
1. ONE BYPASS CAP FOR EACH ICH PIN IF POSSIBLE
2. RTC XTAL MUST NEAR ICH
3. PUT RTC BAT CIRCUIT AS A GROUP
4. REF5VSUS AND REF5V R/C/D NEAR ICH PIN

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH6(GPIO/MISC)	2A
Date: Thursday, March 18, 2004	Sheet 11 of 38	


ASSUME S5 SUPPORT
BOM-2A
U42C
ICH6
4 OF 5
POWER
ICH6
CHANGE-2A
U42D
ICH6
5 OF 5
GROUND
ICH6
DEFINE AS S5 SUPPORT INITIALLY.
PROJECT : NT2
Quanta Computer Inc.
ICH6(POWER/GND)
Thursday, March 18, 2004
Sheet 12 of 38


U45A
PCI EXPRESS
DVO / EXT TMDS / GPIO
LVDS
TMDS
DAC1
DAC2
SS
CLK
THERM
M24
V_PWRCNTL
H=Lower core voltage(1.0V)
L=Higher core voltage(1.2V)
TVOUT_SEL PIN:
0 HDTV OUT
1 S/AV OUT
ADD-2A
Place Close to CN.
SRS= 1 DOWN -2.5%
0 DOWN -1.8%
M DOWN -0.6%
MEMORY CLOCK SPREAD SPECTRUM
U48
CY25819
MK1726-8
Thermal Sensor
*GMT-781-1
PLACE CLOSE TO ASIC
TV_OUT
PROJECT : NT2
Quanta Computer Inc.
VGA HOST(ATI M24)
Thursday, March 18, 2004
Sheet 13 of 38


U45D
I/O POWER
M24
U45E
CORE GND
CENTER ARRAY
M24
(1.2V~1550mA)
(IO.POWER)
(EXT.TMDS)
(PCIE 1.2V)
(QUIET PCIE 1.2V)
(PCIE PLL/IO 1.8V)
(VGA CORE=1.2&1.0V)
ADD-2A
PROJECT : NT2
Quanta Computer Inc.
ATI M24(POWER)
Thursday, March 18, 2004
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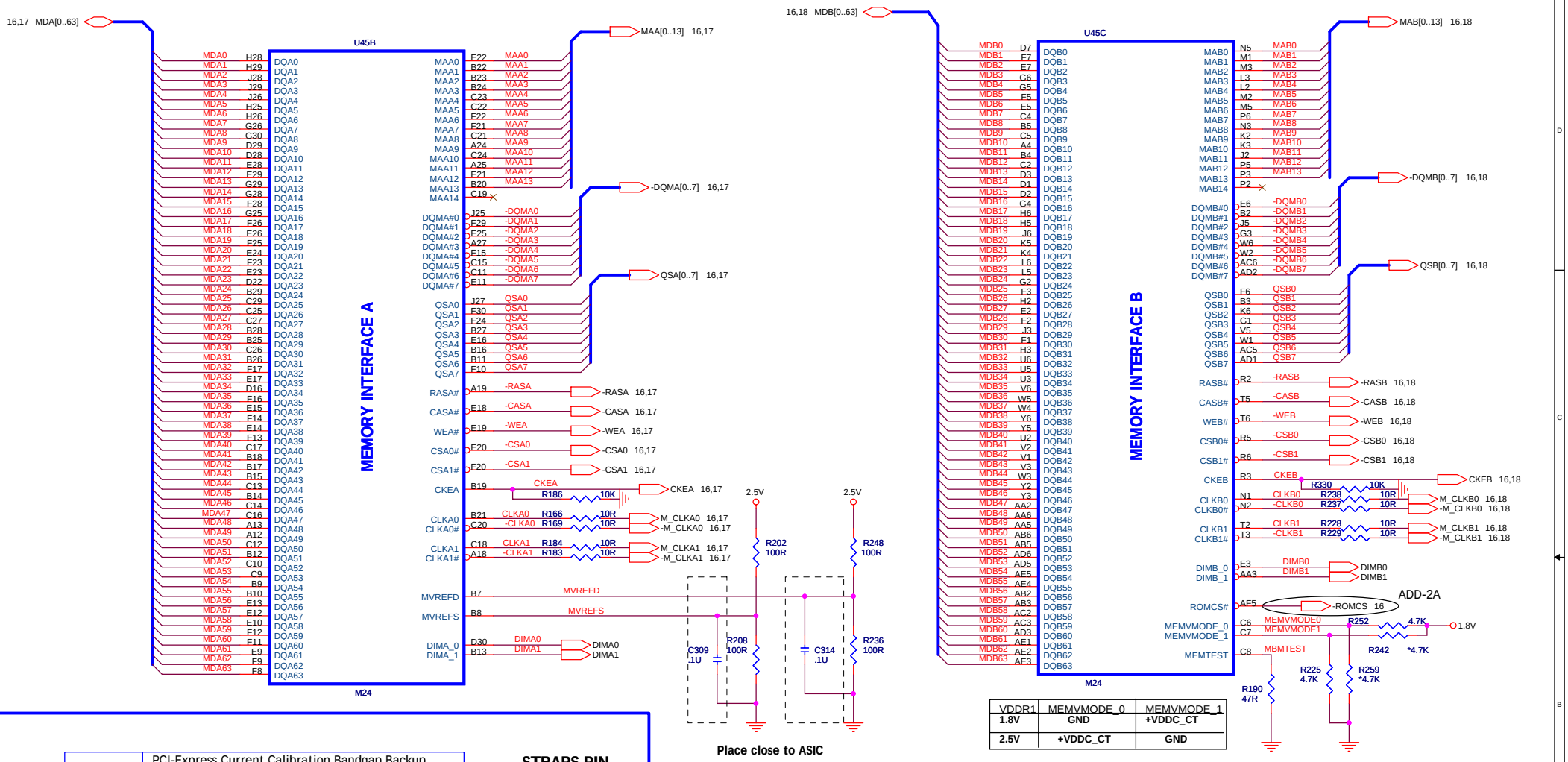
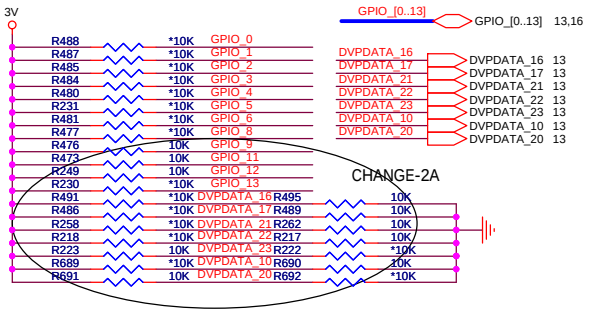


VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND

STRAPS PIN

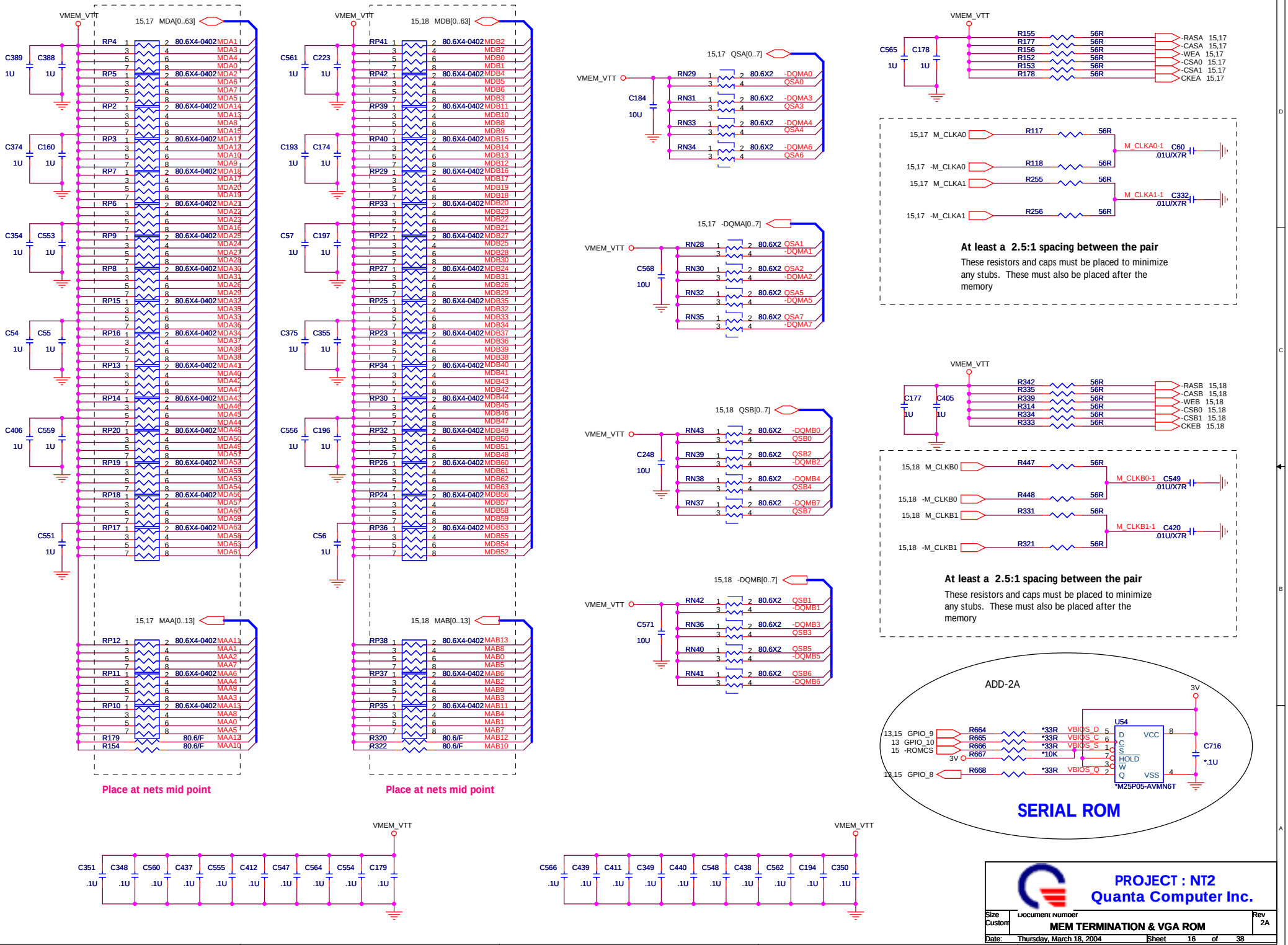
GPIO_0	PCI-Express Current Calibration Bandgap Backup **0: use reference voltage from Bandgap** 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable **0: Disable PLL force calibration** 1: Enable PLL force calibration
GPIO_(3,2)	**00: PCI Express 1.0 mode** 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration **0: enable** 1: disable
GPIO_5	Bypass PCI-Express PLL
GPIO_6	PCI-Express transmitter current compensation **0: Normal** 1: Inject extra current for output buffer switching

GPIO_8	Strap to set the debug muxes to bting out DEBUG signals even if registers are inaccessible
GPIO(9,13:11) INT P/D	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 **1011 - Serial M25P10 ROM (ST), chip IDis from ROM** 1100 - Serial M25P05 ROM (ST), chip IDis from ROM
DVPDATA_15, 20,21,23	DATA23 Vendor; DATA22 Voltage; DATA21 CS; DATA20 MEM SIZE; DATA10 MEM TYPE 0 0 0 0 0 4MX32 0 0 0 0 1 8MX32 MEM TYPE 0 0 0 0 X 128M(M22), 256M(M24) 0 0 0 1 X 64M(M22),128M(M24) 0 0 0 X X CS x1 0 0 1 X X CS x2 0 0 X X X 1.8V 0 1 X X X 2.5V 0 X X X X Hynix 1 X X X X Samsung



PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI M24 MEM/STRAPS PIN	2A
Date: Thursday, March 18, 2004	Sheet 15 of 38	


VMEM_VTT
15,17 MDA[0..63]
RP4 80.6X4-0402 MDA1 MDA3 MDA4 MDA0
RP5 80.6X4-0402 MDA2 MDA6 MDA7 MDA5
RP2 80.6X4-0402 MDA14 MDA13 MDA8 MDA15
RP3 80.6X4-0402 MDA11 MDA12 MDA10 MDA9
RP7 80.6X4-0402 MDA17 MDA20 MDA19
RP6 80.6X4-0402 MDA21 MDA22 MDA23 MDA16
RP9 80.6X4-0402 MDA28 MDA24 MDA27 MDA26
RP8 80.6X4-0402 MDA30 MDA31 MDA32 MDA29
RP15 80.6X4-0402 MDA33 MDA35 MDA36 MDA34
RP16 80.6X4-0402 MDA37 MDA39 MDA38 MDA41
RP13 80.6X4-0402 MDA40 MDA42 MDA47 MDA43
RP14 80.6X4-0402 MDA46 MDA45 MDA44 MDA48
RP20 80.6X4-0402 MDA49 MDA50 MDA51 MDA52
RP19 80.6X4-0402 MDA53 MDA54 MDA55 MDA56
RP18 80.6X4-0402 MDA57 MDA60 MDA59 MDA62
RP17 80.6X4-0402 MDA58 MDA63 MDA61
C389 C388 C374 C160 C354 C553 C54 C55 C406 C559 C551
1U
15,17 MAA[0..13]
RP12 80.6X4-0402 MAA11 MAA1 MAA2 MAA7
RP11 80.6X4-0402 MAA6 MAA4 MAA9 MAA3
RP10 80.6X4-0402 MAA13 MAA8 MAA0 MAA5
R179 80.6/F MAA12
R154 80.6/F MAA10
Place at nets mid point
VMEM_VTT
15,18 MDB[0..63]
RP41 80.6X4-0402 MDB2 MDB7 MDB0 MDB1
RP42 80.6X4-0402 MDB4 MDB5 MDB6 MDB3
RP39 80.6X4-0402 MDB11 MDB10 MDB8 MDB9
RP40 80.6X4-0402 MDB15 MDB14 MDB13 MDB12
RP29 80.6X4-0402 MDB16 MDB17 MDB19 MDB18
RP33 80.6X4-0402 MDB20 MDB23 MDB22 MDB21
RP22 80.6X4-0402 MDB27 MDB25 MDB28 MDB30
RP27 80.6X4-0402 MDB24 MDB31 MDB26 MDB29
RP25 80.6X4-0402 MDB35 MDB32 MDB33 MDB34
RP23 80.6X4-0402 MDB37 MDB36 MDB39 MDB38
RP34 80.6X4-0402 MDB40 MDB41 MDB43 MDB42
RP30 80.6X4-0402 MDB44 MDB45 MDB46 MDB47
RP32 80.6X4-0402 MDB49 MDB50 MDB51 MDB48
RP26 80.6X4-0402 MDB60 MDB61 MDB62 MDB63
RP24 80.6X4-0402 MDB56 MDB57 MDB58 MDB59
RP36 80.6X4-0402 MDB53 MDB55 MDB54 MDB52
C561 C223 C193 C174 C57 C197 C375 C355 C556 C196 C56
1U
15,18 MAB[0..13]
RP38 80.6X4-0402 MAB13 MAB8 MAB0 MAB5
RP37 80.6X4-0402 MAB6 MAB2 MAB9 MAB3
RP35 80.6X4-0402 MAB11 MAB4 MAB1 MAB7
R320 80.6/F MAB12
R322 80.6/F MAB10
Place at nets mid point
15,17 QSA[0..7]
RN29 RN31 RN33 RN34 80.6X2 QSA0 QSA3 QSA4 QSA6 -DQMA0 -DQMA3 -DQMA4 -DQMA6
C184 10U
15,17 -DQMA[0..7]
RN28 RN30 RN32 RN35 80.6X2 QSA1 QSA2 QSA5 QSA7 -DQMA1 -DQMA2 -DQMA5 -DQMA7
C568 10U
15,18 QSB[0..7]
RN43 RN39 RN38 RN37 80.6X2 QSB0 QSB2 QSB4 QSB7 -DQMB0 -DQMB2 -DQMB4 -DQMB7
C248 10U
15,18 -DQMB[0..7]
RN42 RN36 RN40 RN41 80.6X2 QSB1 QSB3 QSB5 QSB6 -DQMB1 -DQMB3 -DQMB5 -DQMB6
C571 10U
C565 C178 1U
R155 R177 R156 R152 R153 R178 56R
-RASA 15,17
-CASA 15,17
-WEA 15,17
-CSA0 15,17
-CSA1 15,17
CKEA 15,17
15,17 M_CLKA0 R117 56R M_CLKA0-1 C60 .01U/X7R
15,17 -M_CLKA0 R118 56R
15,17 M_CLKA1 R255 56R M_CLKA1-1 C332 .01U/X7R
15,17 -M_CLKA1 R256 56R
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory
C177 C405 1U
R342 R335 R339 R314 R334 R333 56R
-RASB 15,18
-CASB 15,18
-WEB 15,18
-CSB0 15,18
-CSB1 15,18
CKEB 15,18
15,18 M_CLKB0 R447 56R M_CLKB0-1 C549 .01U/X7R
15,18 -M_CLKB0 R448 56R
15,18 M_CLKB1 R331 56R M_CLKB1-1 C420 .01U/X7R
15,18 -M_CLKB1 R321 56R
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory
ADD-2A
3V
13,15 GPIO_9
13 GPIO_10
15 -ROMCS
3V
13,15 GPIO_8
R664 R665 R666 R667 *33R *10K
R668 *33R
VBIOS_D VBIOS_C VBIOS_S VBIOS_Q
U54
D C S HOLD W Q VCC VSS
*M25P05-AVMN6T
C716 *.1U
SERIAL ROM
C351 C348 C560 C437 C555 C412 C547 C564 C554 C179 .1U
C566 C439 C411 C349 C440 C548 C438 C562 C194 C350 .1U
PROJECT : NT2
Quanta Computer Inc.
Size Custom
Document Number
MEM TERMINATION & VGA ROM
Rev 2A
Date: Thursday, March 18, 2004
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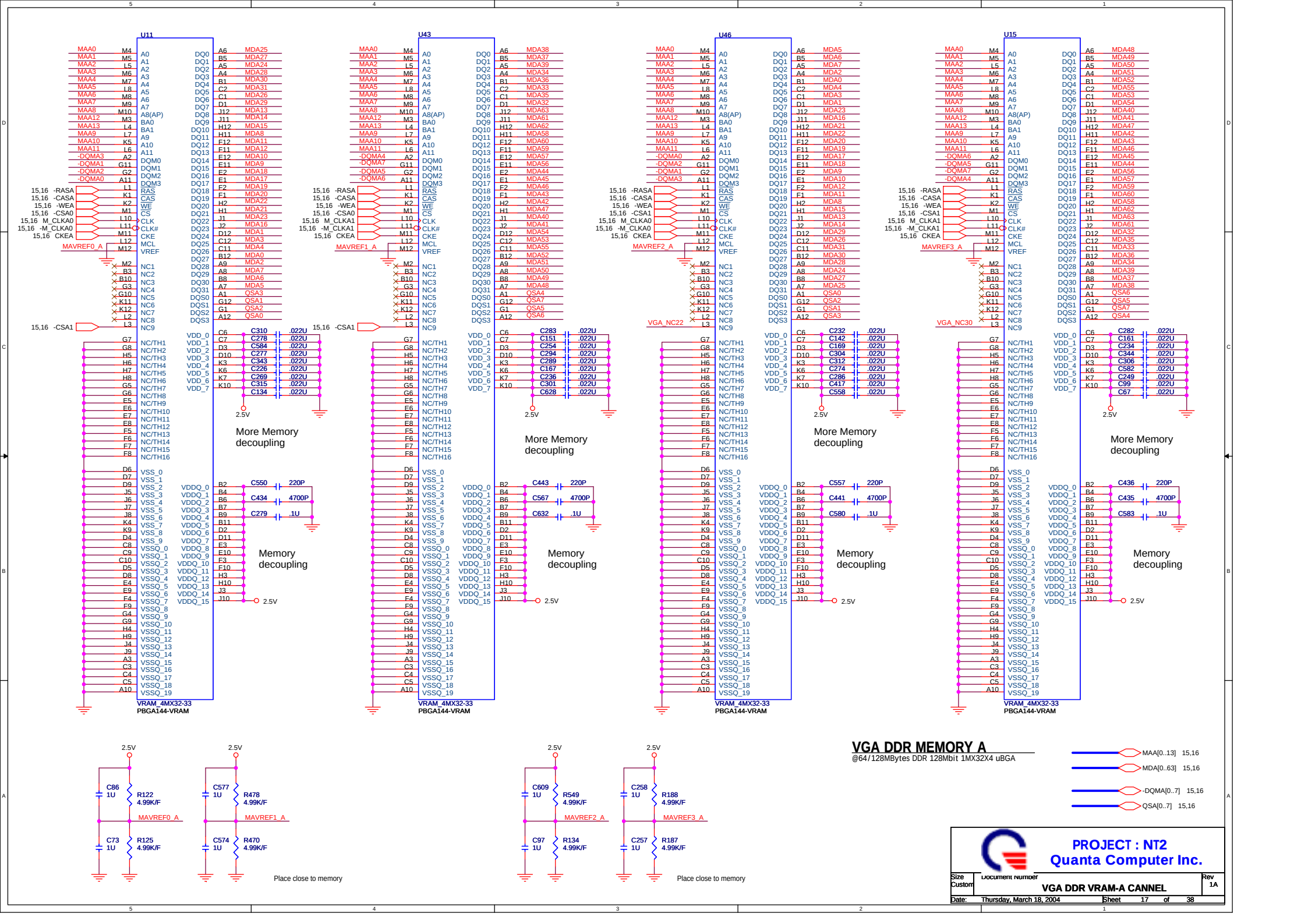
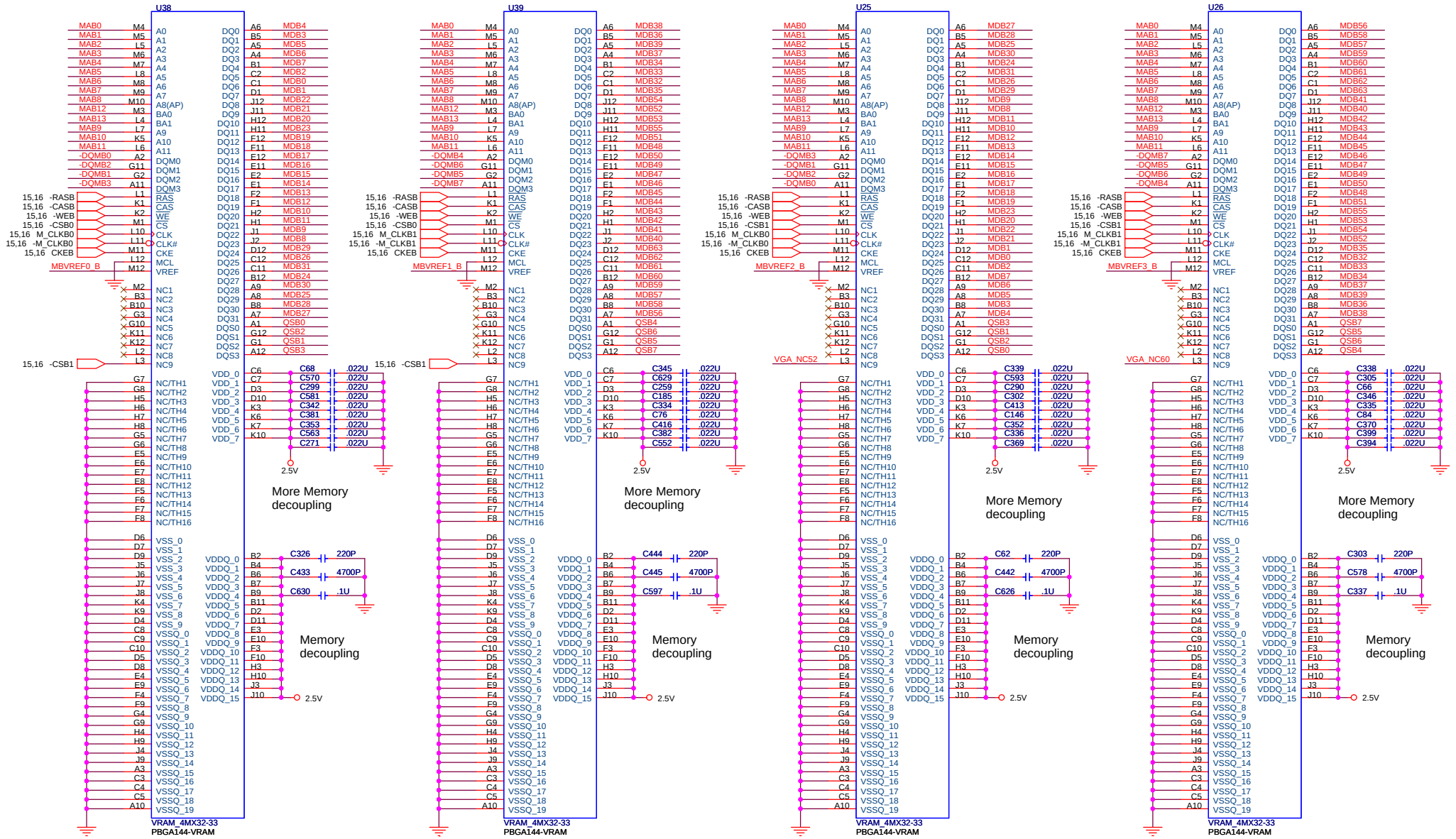

U11
U43
U46
U15
VRAM_4MX32-33
PBGA144-VRAM
More Memory decoupling
Memory decoupling
2.5V
VGA DDR MEMORY A
@64/128MBytes DDR 128Mbit 1MX32X4 uBGA
MAA[0..13] 15,16
MDA[0..63] 15,16
-DQMA[0..7] 15,16
QSA[0..7] 15,16
Place close to memory
PROJECT : NT2
Quanta Computer Inc.
VGA DDR VRAM-A CANNEL
Size Custom
Document Number
Rev 1A
Date: Thursday, March 18, 2004
Sheet 17 of 38



VGA DDR MEMORY B

@64/128MBytes DDR 128Mbit 1MX32X4 uBGA

PROJECT : NT2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA DDR VRAM-B CANNEL	1A
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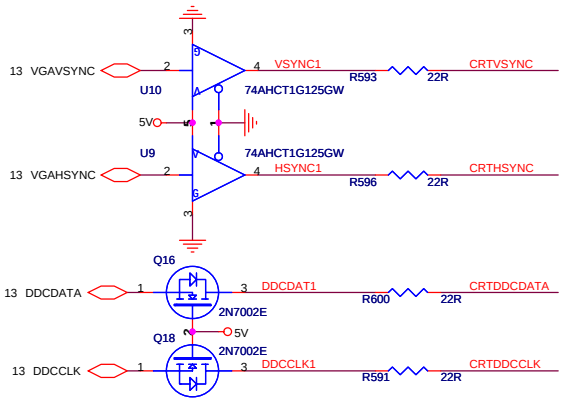
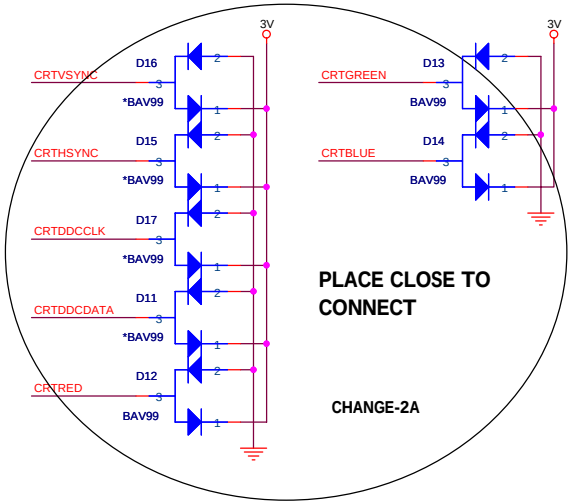
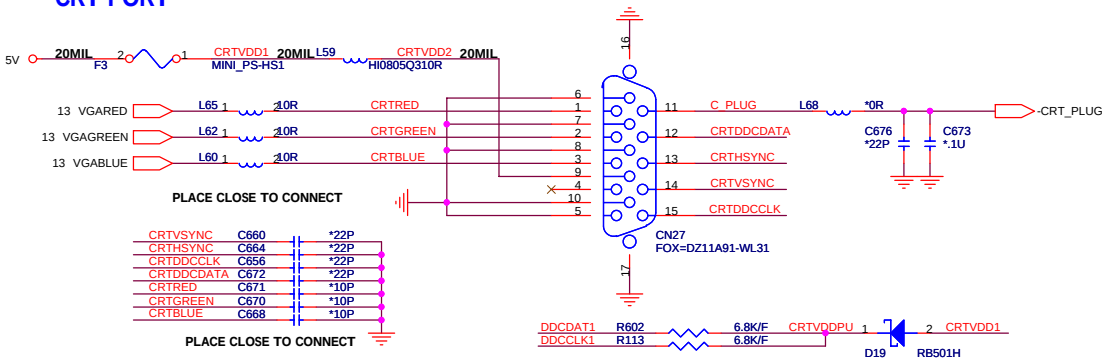
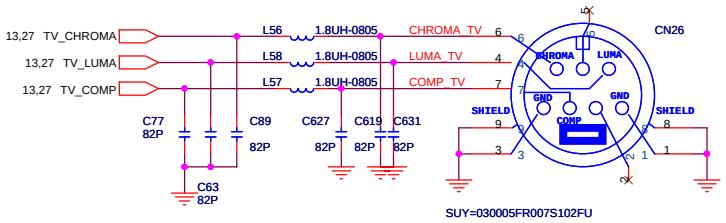




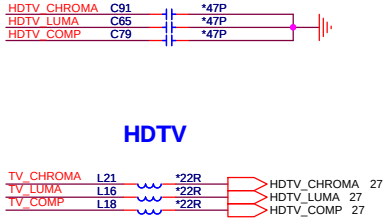
CRT PORT

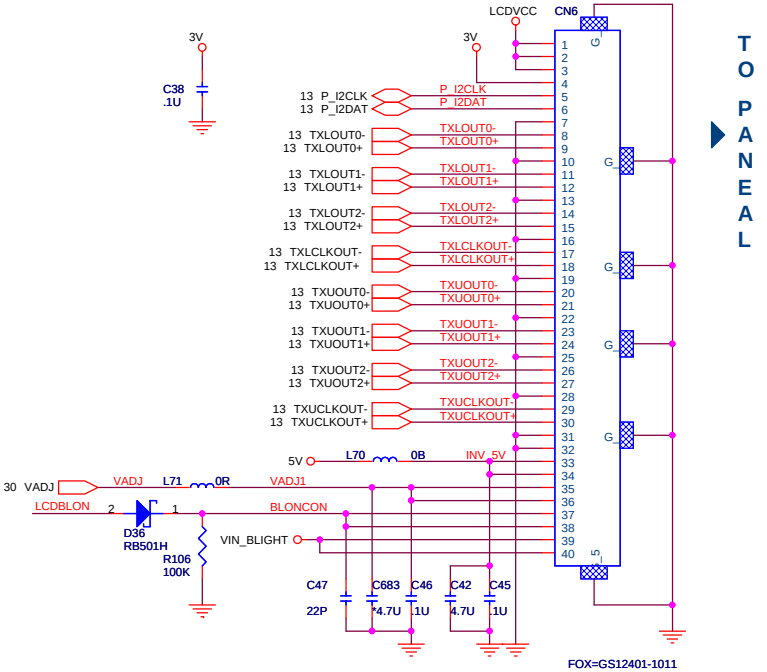


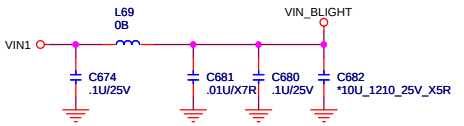
TV_OUT

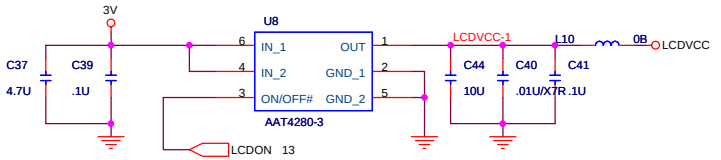


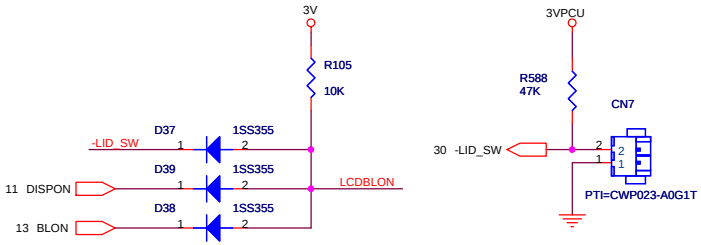
HDTV











BACKLIGHT CONTROL

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SVIDEO/CRT/PANLE/HDTV	2A
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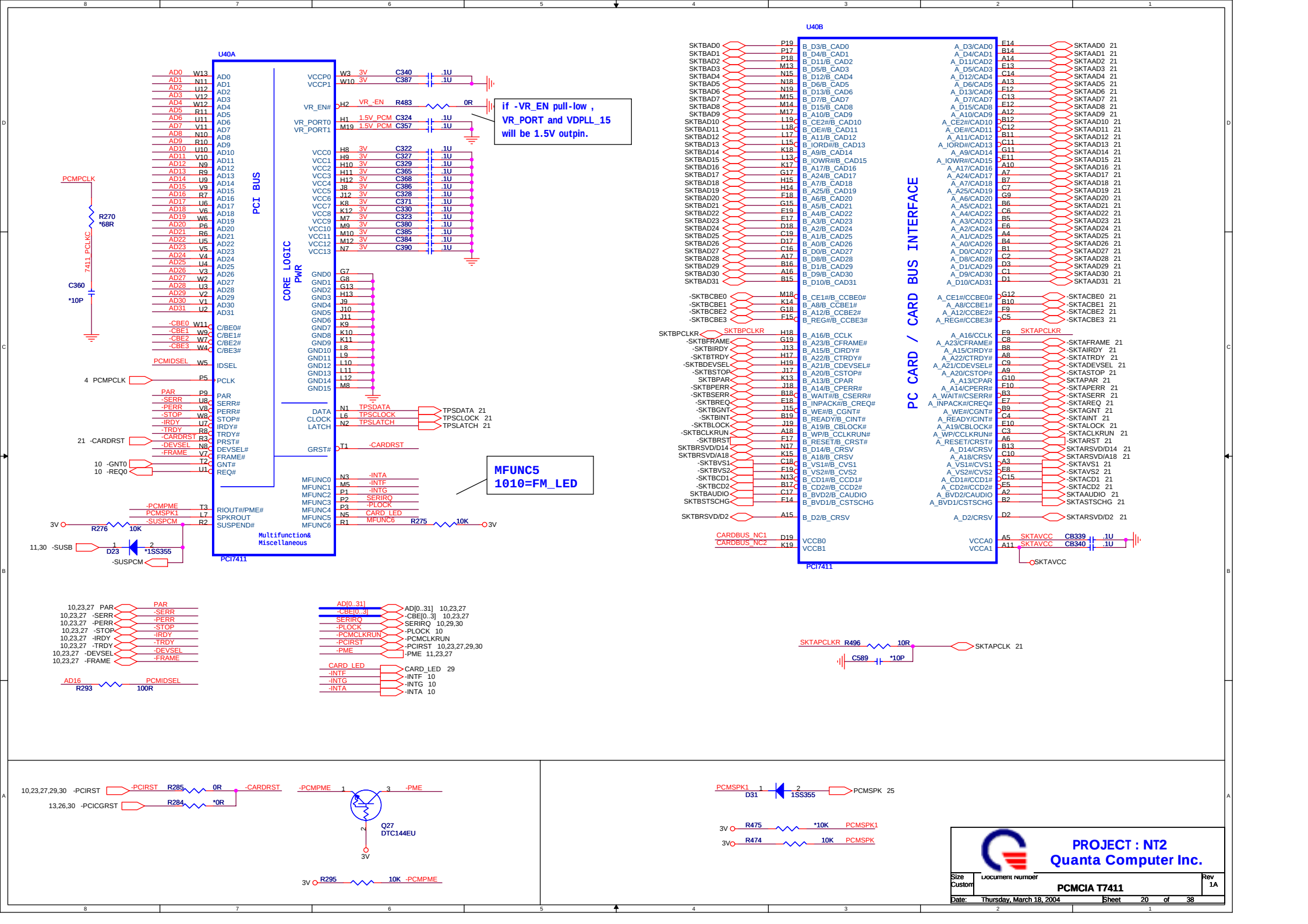
U40A
PCI BUS
CORE LOGIC
PWR
PCI7411
Multifunction&
Miscellaneous
U40B
PC CARD / CARD BUS INTERFACE
PCI7411
if -VR_EN pull-low ,
VR_PORT and VDPLL_15
will be 1.5V outpin.
MFUNC5
1010=FM_LED
PCMPCLK
R270
*68R
7411 PCLKC
C360
*10P
4 PCMPCLK
21 -CARDRST
10 -GNT0
10 -REQ0
3V
R276
10K
11,30 -SUSB
D23
*1SS355
-SUSPCM
R275
10K
TPSDATA 21
TPSCLOCK 21
TPSLATCH 21
SKTAPCLKR
R496
10R
SKTAPCLK 21
C589
*10P
PCMSPK1
D31
1SS355
PCMSPK 25
R475
*10K
R474
10K
PCMSPK1
PCMSPK
R293
100R
AD16
R285
0R
R284
*0R
-PCIRST
-CARDRST
Q27
DTC144EU
R295
10K
-PCMPME
PROJECT : NT2
Quanta Computer Inc.
PCMCIA T7411
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Custom
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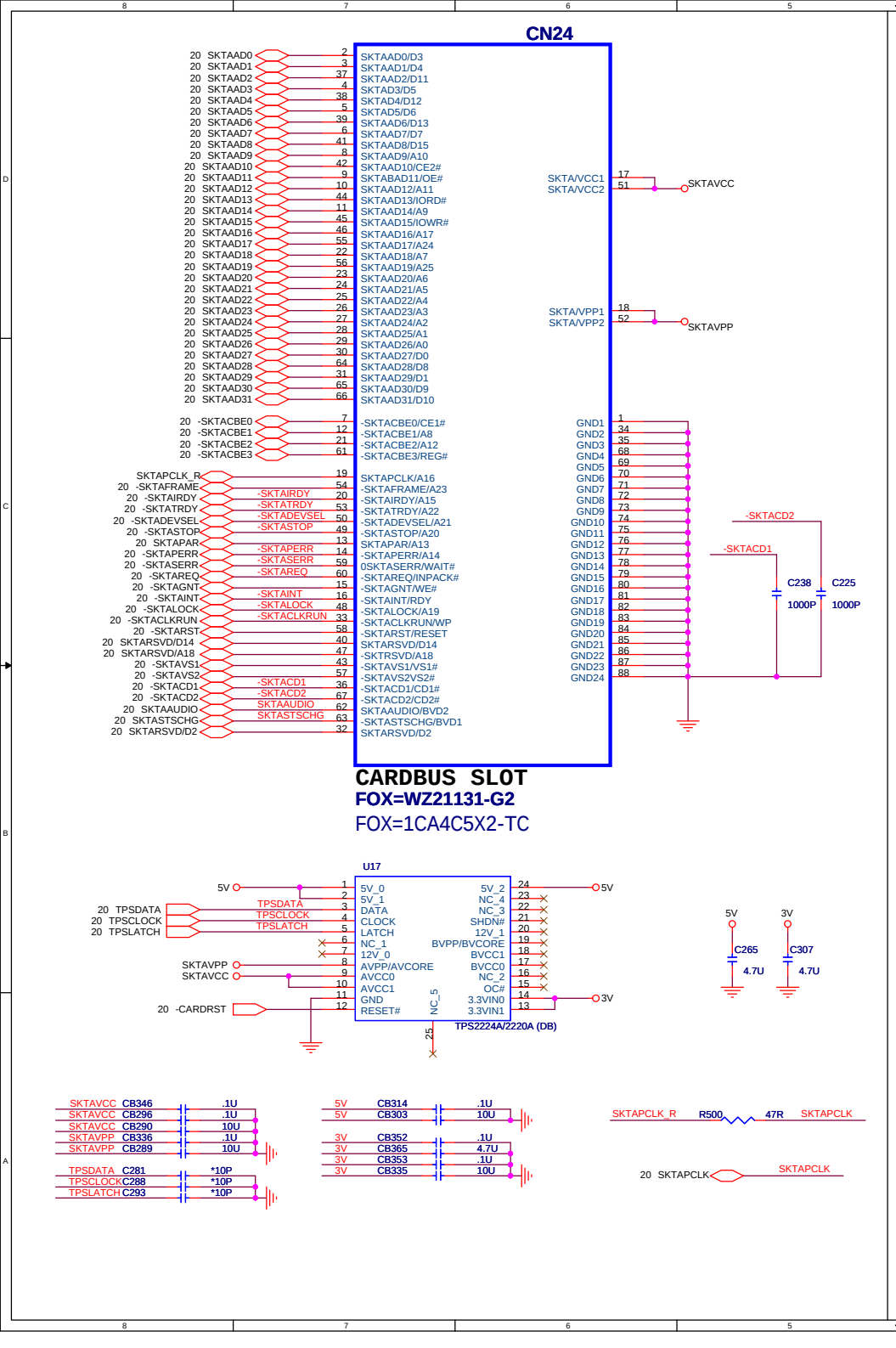
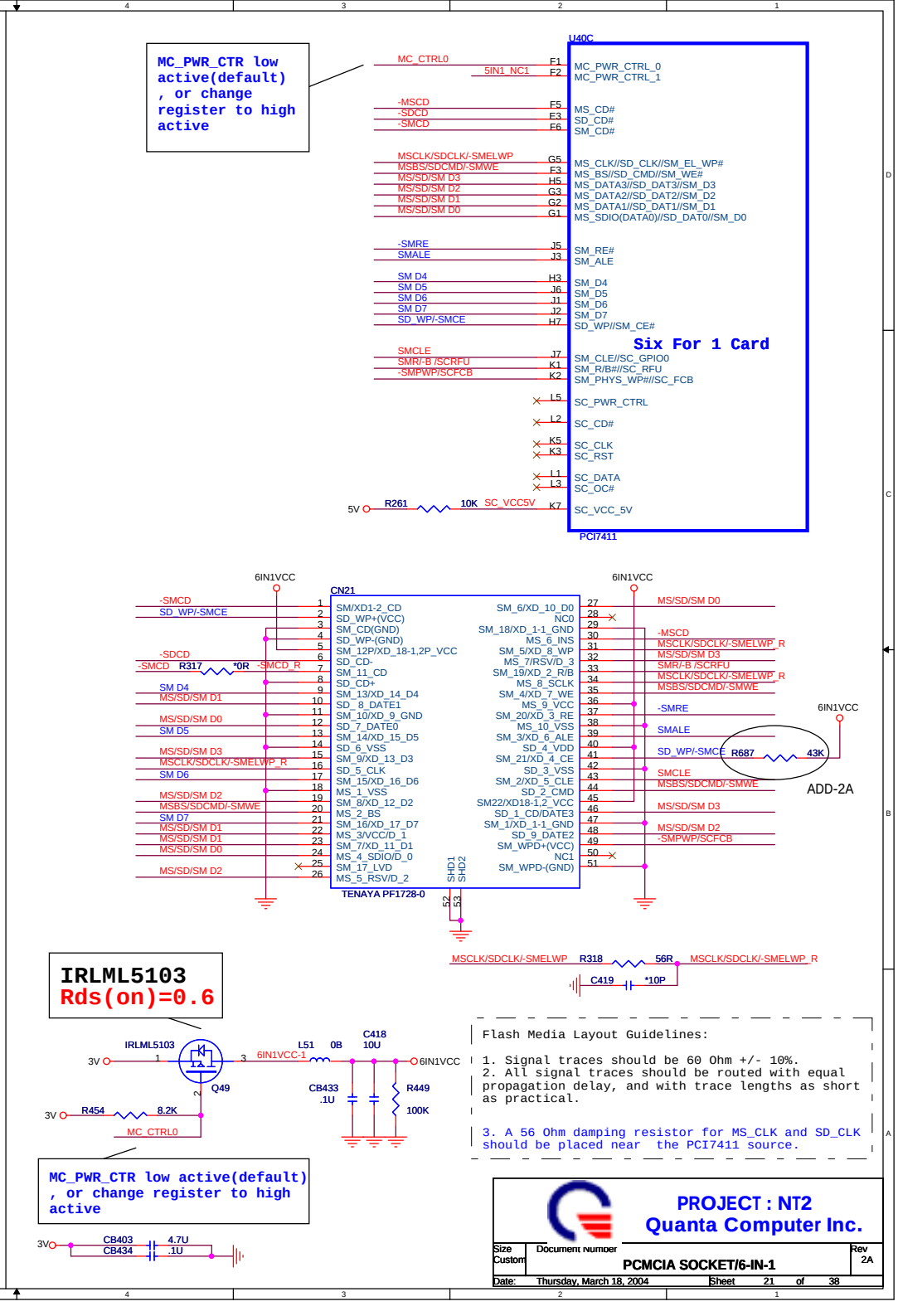

CN24
SKTAAD0/D3
SKTAAD1/D4
SKTAAD2/D11
SKTAD3/D5
SKTAD4/D12
SKTAD5/D6
SKTAAD6/D13
SKTAAD7/D7
SKTAAD8/D15
SKTAAD9/A10
SKTAAD10/CE2#
SKTABAD11/OE#
SKTAAD12/A11
SKTAAD13/IORD#
SKTAAD14/A9
SKTAAD15/IOWR#
SKTAAD16/A17
SKTAAD17/A24
SKTAAD18/A7
SKTAAD19/A25
SKTAAD20/A6
SKTAAD21/A5
SKTAAD22/A4
SKTAAD23/A3
SKTAAD24/A2
SKTAAD25/A1
SKTAAD26/A0
SKTAAD27/D0
SKTAAD28/D8
SKTAAD29/D1
SKTAAD30/D9
SKTAAD31/D10
-SKTACBE0/CE1#
-SKTACBE1/A8
-SKTACBE2/A12
-SKTACBE3/REG#
SKTAPCLK/A16
-SKTAFRAME/A23
-SKTAIRDY/A15
-SKTATRDY/A22
-SKTADEVSEL/A21
-SKTASTOP/A20
SKTAPAR/A13
-SKTAPERR/A14
0SKTASERR/WAIT#
-SKTAREQ/INPACK#
-SKTAGNT/WE#
-SKTAINT/RDY
-SKTALOCK/A19
-SKTACLKRUN/WP
-SKTARST/RESET
SKTARSVD/D14
SKTRSVD/A18
-SKTAVS1/VS1#
-SKTAVS2/VS2#
-SKTACD1/CD1#
-SKTACD2/CD2#
SKTAAUDIO/BVD2
-SKTASTSCHG/BVD1
SKTARSVD/D2
SKTA/VCC1
SKTA/VCC2
SKTAVCC
SKTA/VPP1
SKTA/VPP2
SKTAVPP
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
GND18
GND19
GND20
GND21
GND22
GND23
GND24
-SKTACD2
-SKTACD1
C238
1000P
C225
1000P
CARDBUS SLOT
FOX=WZ21131-G2
FOX=1CA4C5X2-TC
U17
5V_0
5V_1
DATA
CLOCK
LATCH
NC_1
12V_0
AVPP/AVCORE
AVCC0
AVCC1
GND
RESET#
5V_2
NC_4
NC_3
SHDN#
12V_1
BVPP/BVCORE
BVCC1
BVCC0
NC_2
OC#
3.3VIN0
3.3VIN1
NC_5
TPS2224A/2220A (DB)
TPSDATA
TPSCLOCK
TPSLATCH
SKTAVPP
SKTAVCC
-CARDRST
C265
4.7U
C307
4.7U
SKTAVCC CB346 .1U
SKTAVCC CB296 .1U
SKTAVCC CB290 10U
SKTAVPP CB336 .1U
SKTAVPP CB289 10U
TPSDATA C281 *10P
TPSCLOCK C288 *10P
TPSLATCH C293 *10P
5V CB314 .1U
5V CB303 10U
3V CB352 .1U
3V CB365 4.7U
3V CB353 .1U
3V CB335 10U
SKTAPCLK_R R500 47R SKTAPCLK
SKTAPCLK


MC_PWR_CTR low active(default), or change register to high active
U40C
MC_CTRL0
5IN1_NC1
MC_PWR_CTRL_0
MC_PWR_CTRL_1
-MSCD
-SDCD
-SMCD
MS_CD#
SD_CD#
SM_CD#
MSCLK/SDCLK/-SMELWP
MSBS/SDCMD/-SMWE
MS/SD/SM D3
MS/SD/SM D2
MS/SD/SM D1
MS/SD/SM D0
MS_CLK//SD_CLK//SM_EL_WP#
MS_BS//SD_CMD//SM_WE#
MS_DATA3//SD_DAT3//SM_D3
MS_DATA2//SD_DAT2//SM_D2
MS_DATA1//SD_DAT1//SM_D1
MS_SDIO(DATA0)//SD_DAT0//SM_D0
-SMRE
SMALE
SM_RE#
SM_ALE
SM D4
SM D5
SM D6
SM D7
SD_WP/-SMCE
SM_D4
SM_D5
SM_D6
SM_D7
SD_WP//SM_CE#
Six For 1 Card
SMCLE
SMR/-B /SCRFU
-SMPWP/SCFCB
SM_CLE//SC_GPIO0
SM_R/B#//SC_RFU
SM_PHYS_WP#//SC_FCB
SC_PWR_CTRL
SC_CD#
SC_CLK
SC_RST
SC_DATA
SC_OC#
5V
R261
10K
SC_VCC5V
SC_VCC_5V
PCI7411
6IN1VCC
CN21
-SMCD
SD_WP/-SMCE
-SDCD
R317
*0R
SM D4
MS/SD/SM D1
MS/SD/SM D0
SM D5
MS/SD/SM D3
MSCLK/SDCLK/-SMELWP_R
SM D6
MS/SD/SM D2
MSBS/SDCMD/-SMWE
SM D7
MS/SD/SM D1
MS/SD/SM D1
MS/SD/SM D0
MS/SD/SM D2
SM/XD1-2_CD
SD_WP+(VCC)
SM_CD(GND)
SD_WP-(GND)
SM_12P/XD_18-1,2P_VCC
SD_CD-
SM_11_CD
SD_CD+
SM_13/XD_14_D4
SD_8_DATE1
SM_10/XD_9_GND
SD_7_DATE0
SM_14/XD_15_D5
SD_6_VSS
SM_9/XD_13_D3
SD_5_CLK
SM_15/XD_16_D6
MS_1_VSS
SM_8/XD_12_D2
MS_2_BS
SM_16/XD_17_D7
MS_3/VCC/D_1
SM_7/XD_11_D1
MS_4_SDIO/D_0
SM_17_LVD
MS_5_RSV/D_2
SM_6/XD_10_D0
NC0
SM_18/XD_1-1_GND
MS_6_INS
SM_5/XD_8_WP
MS_7/RSV/D_3
SM_19/XD_2_R/B
MS_8_SCLK
SM_4/XD_7_WE
MS_9_VCC
SM_20/XD_3_RE
MS_10_VSS
SM_3/XD_6_ALE
SD_4_VDD
SM_21/XD_4_CE
SD_3_VSS
SM_2/XD_5_CLE
SD_2_CMD
SM22/XD18-1,2_VCC
SD_1_CD/DATE3
SM_1/XD_1-1_GND
SD_9_DATE2
SM_WPD+(VCC)
NC1
SM_WPD-(GND)
SHD1
SHD2
TENAYA PF1728-0
MS/SD/SM D0
-SMRE
SMALE
SD_WP/-SMCE
R687
43K
SMCLE
MSBS/SDCMD/-SMWE
MS/SD/SM D3
MS/SD/SM D2
-SMPWP/SCFCB
ADD-2A
MSCLK/SDCLK/-SMELWP
R318
56R
C419
*10P
IRLML5103
Rds(on)=0.6
IRLML5103
Q49
6IN1VCC-1
L51
0B
C418
10U
CB433
.1U
R449
100K
R454
8.2K
MC_CTRL0
MC_PWR_CTR low active(default), or change register to high active
CB403
4.7U
CB434
.1U
Flash Media Layout Guidelines:
1. Signal traces should be 60 Ohm +/- 10%.
2. All signal traces should be routed with equal propagation delay, and with trace lengths as short as practical.
3. A 56 Ohm damping resistor for MS_CLK and SD_CLK should be placed near the PCI7411 source.
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Quanta Computer Inc.
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Custom
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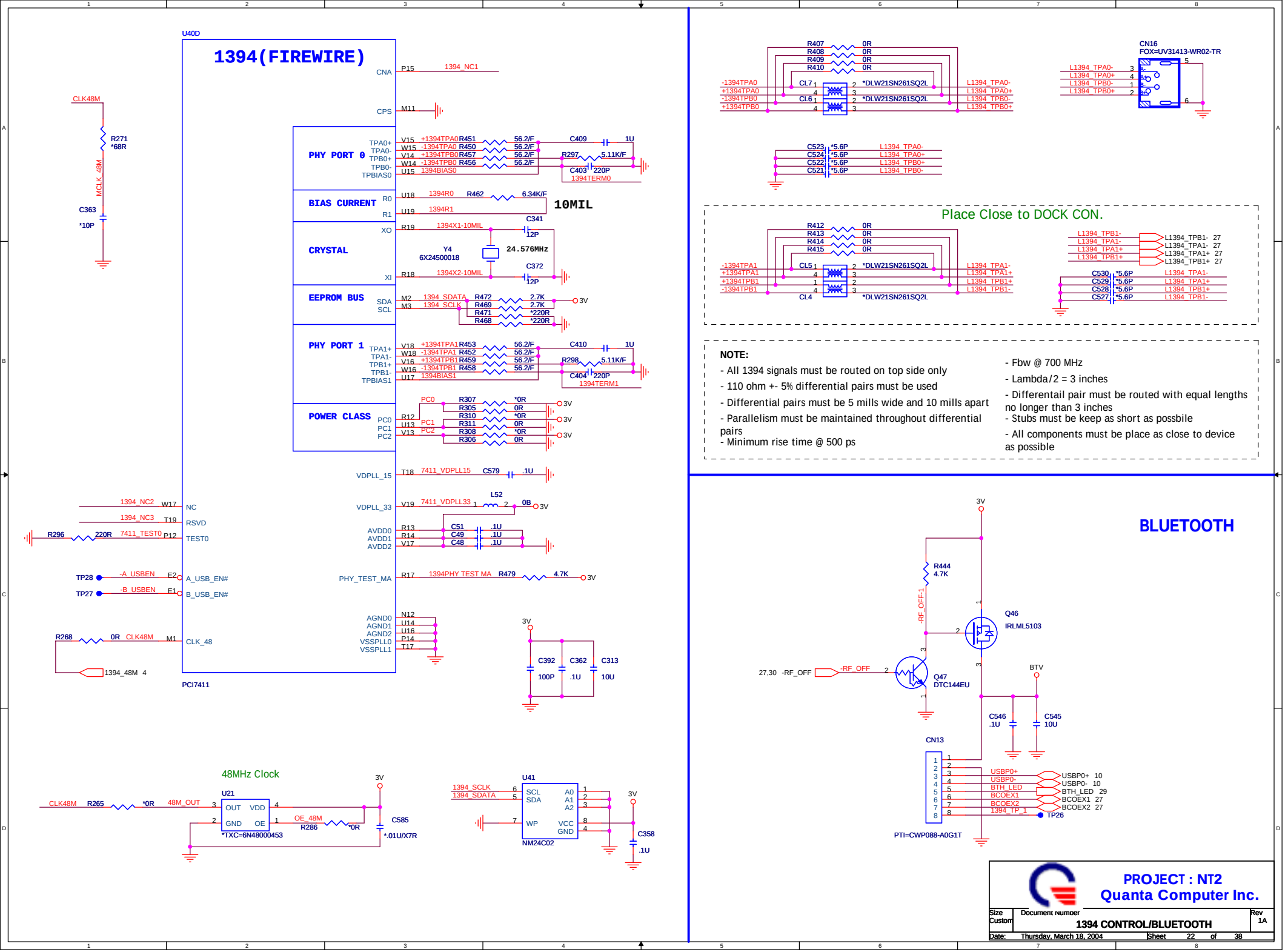
1394(FIREWIRE)
U40D
PCI7411
PHY PORT 0
PHY PORT 1
BIAS CURRENT
CRYSTAL
EEPROM BUS
POWER CLASS
10MIL
Place Close to DOCK CON.
NOTE:
- All 1394 signals must be routed on top side only
- 110 ohm +- 5% differential pairs must be used
- Differential pairs must be 5 mills wide and 10 mills apart
- Parallelism must be maintained throughout differential pairs
- Minimum rise time @ 500 ps
- Fbw @ 700 MHz
- Lambda/2 = 3 inches
- Differentail pair must be routed with equal lengths no longer than 3 inches
- Stubs must be keep as short as possbile
- All components must be place as close to device as possible
BLUETOOTH
48MHz Clock
PROJECT : NT2
Quanta Computer Inc.
1394 CONTROL/BLUETOOTH
Thursday, March 18, 2004

U29

RTL8100C/8110SBL

FOR RTL8100C

FOR RTL8110S(B)

	RTL 8100C	RTL 8110S(B)
LAN_DVDD25/12	2.5V	1.2V
LAN_AVDD33/25	3.3V Analog	2.5V Analog
LAN_AVDD33	none	3.3V Analog
LAN_V12P	2.5V Analog	none(3.3V Ana.)

LAN_DVDD25/12-->1A
LAN_AVDD33/25-->300mA

Placed closely to the RTL8110SB/8100C

FOR RTL8110S(B) ONLY

ADD-2A

FOR RTL8110S(B) ONLY

ADD-2A

LAN CON

CN17
AMP=1470620-5

CN15
SUYIN=127039MH002G200Z0

MODEM CON

U37
*NS680016

FOR RTL8110S(B) ONLY

FOR RTL8110S(B)=2.49K/F
Placed near to ASIC

Placed near to RJ45 connector

U55
H0013

PLACEMENT CAREFULLY

U27
93LC46B/SN

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Size: Custom	Document Number: LAN interface RTL8100C/8110SB
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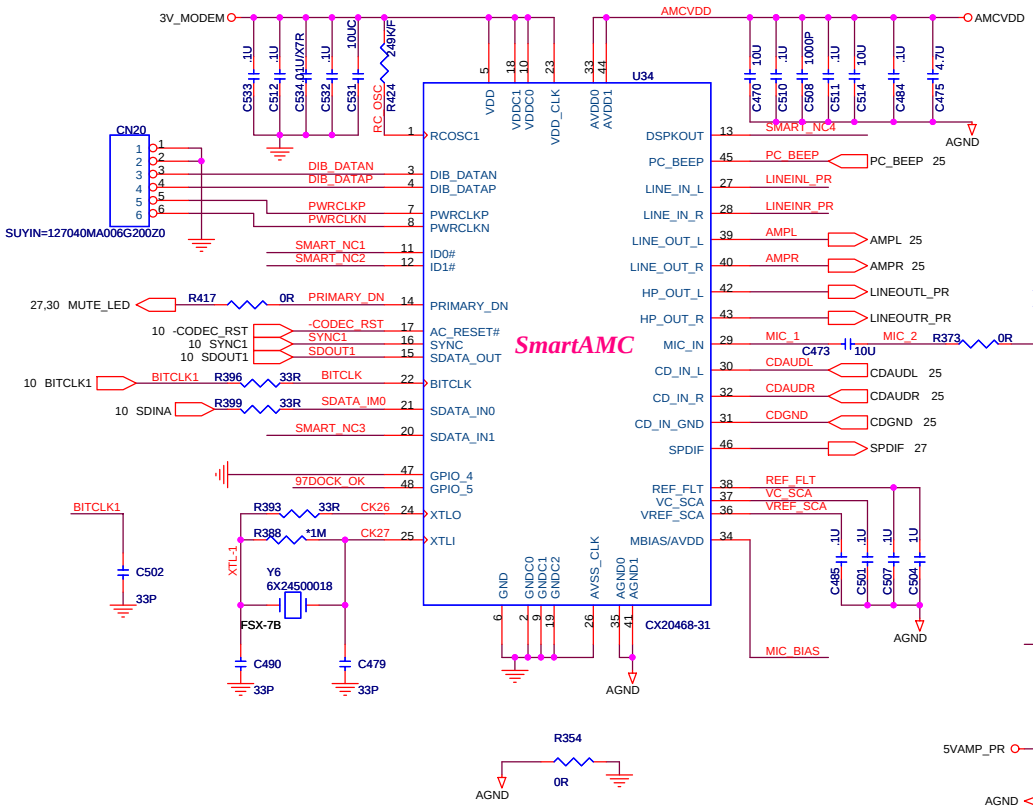

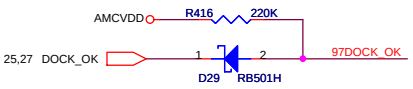

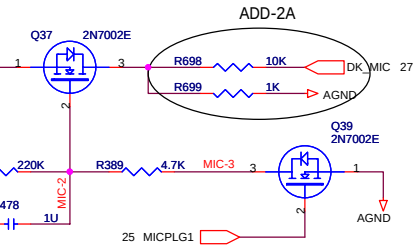

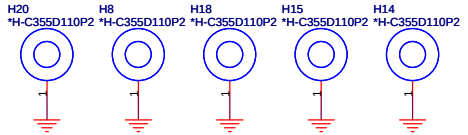

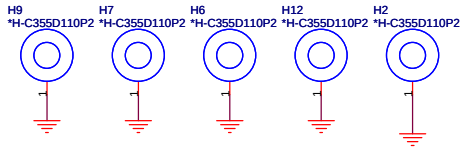

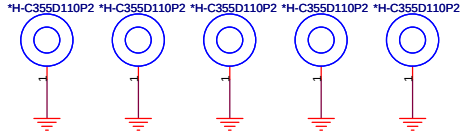

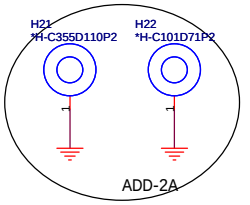

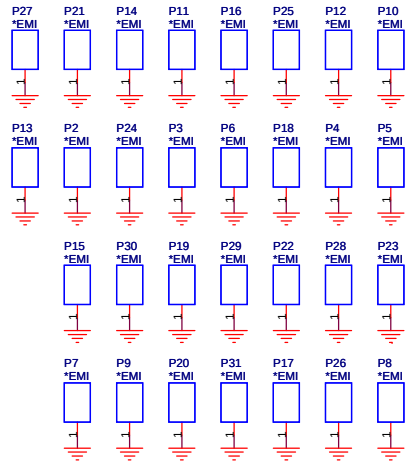

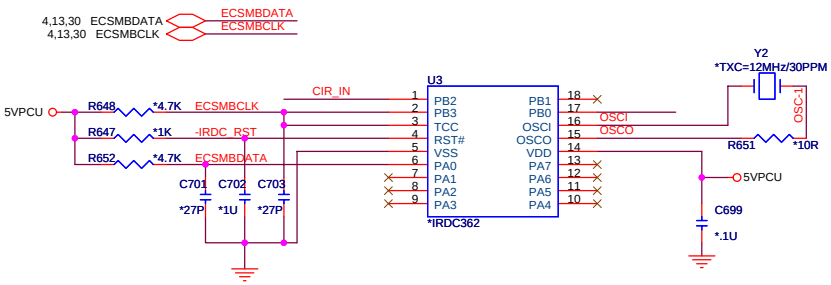

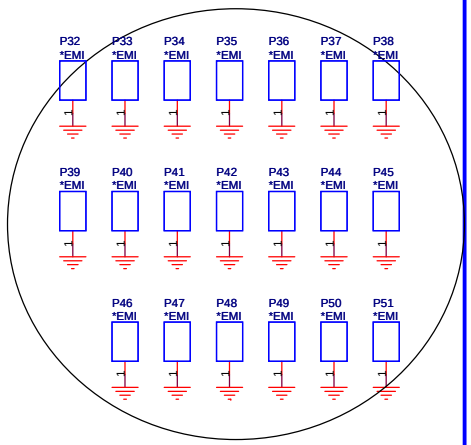

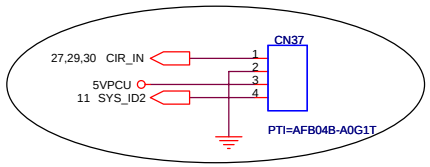

PROJECT : NT2
Quanta Computer Inc.

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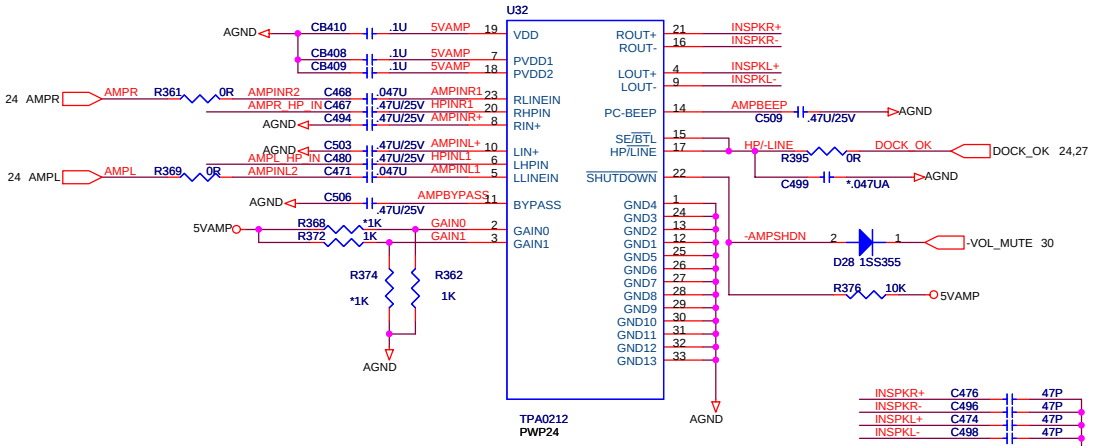
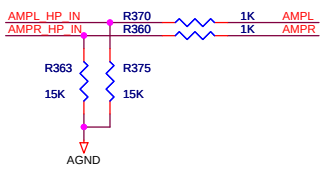
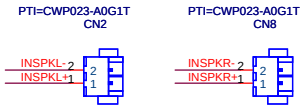
AUDIO AMPLIFIER

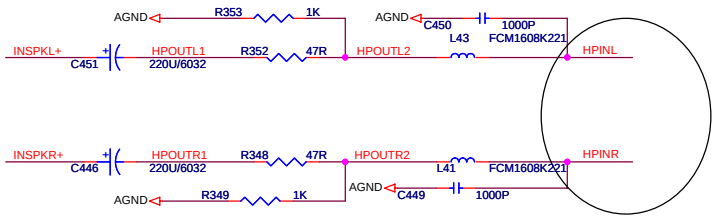


GAIN0	GAIN1	Av
0	0	6dB
0	1	15.6dB
1	0	21.6dB
1	1	27.6dB

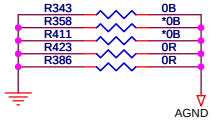


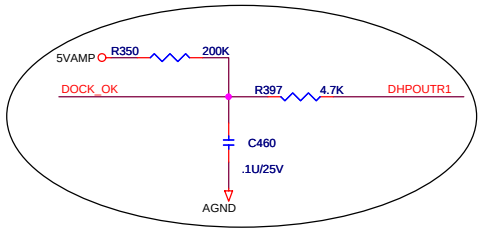
INT. SPEAKER





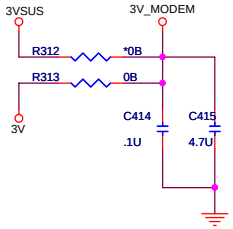
CHANGE-2A

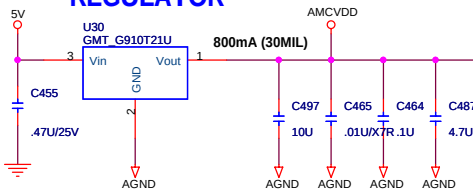




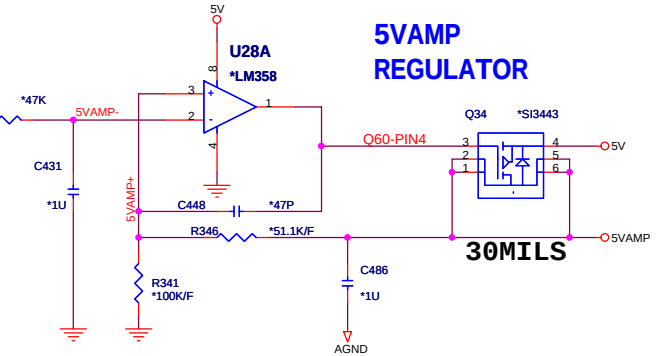
CD/PHONE INPUT & MONOOUT

3VAUD REGULATOR

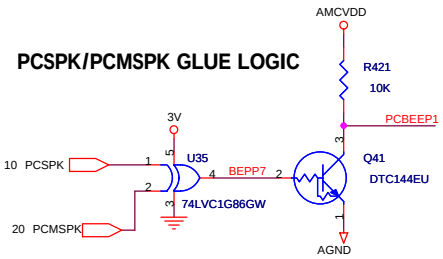


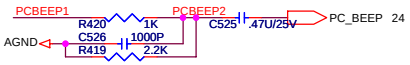


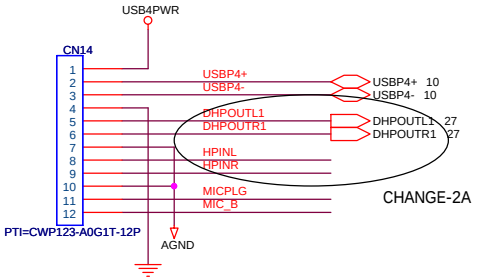
5VAMP REGULATOR



PCSPK/PCMSPK GLUE LOGIC

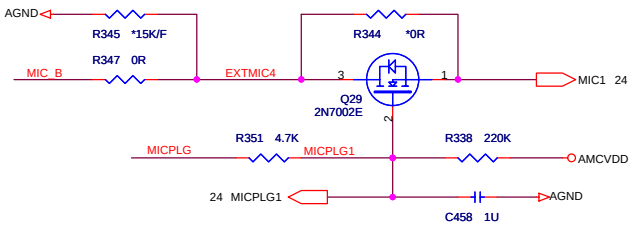






CHANGE-2A

EXT MIC



PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO AMP, HEADPHONE&SPEAKER	1A
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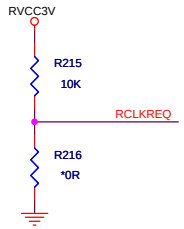
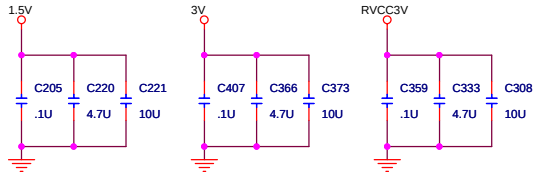
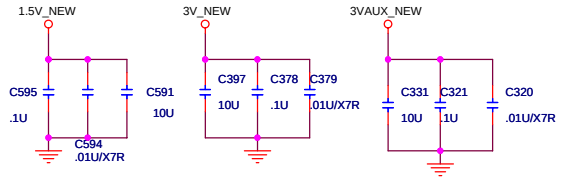
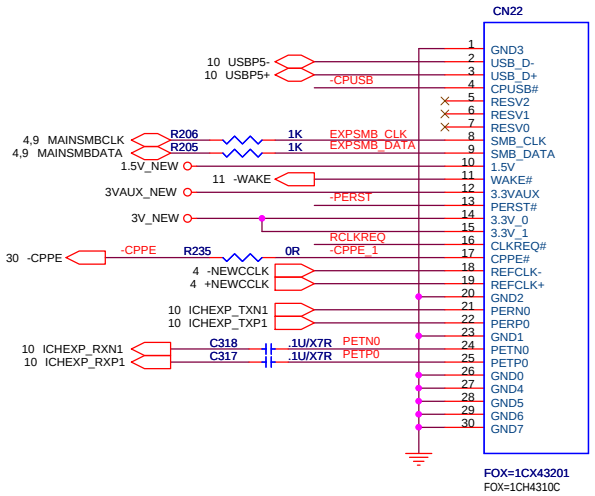
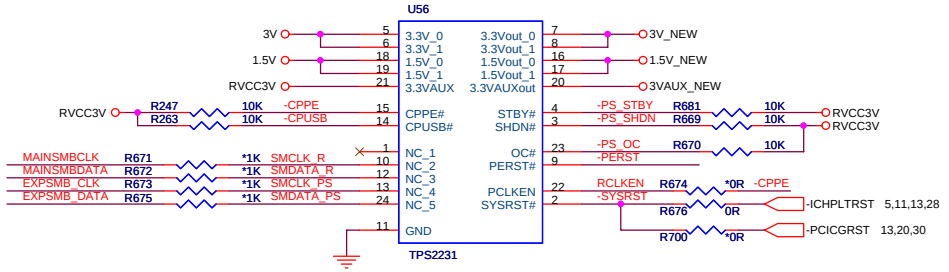


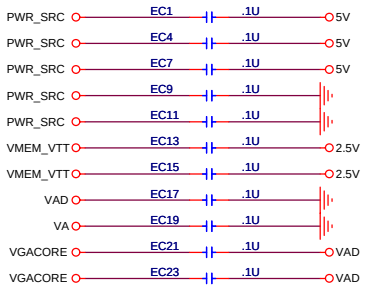


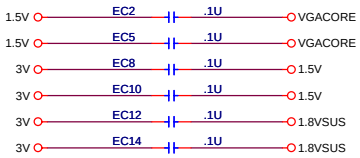


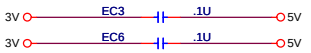


CHANGE-2A









EMI

ADD-2A

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Quanta Computer Inc.

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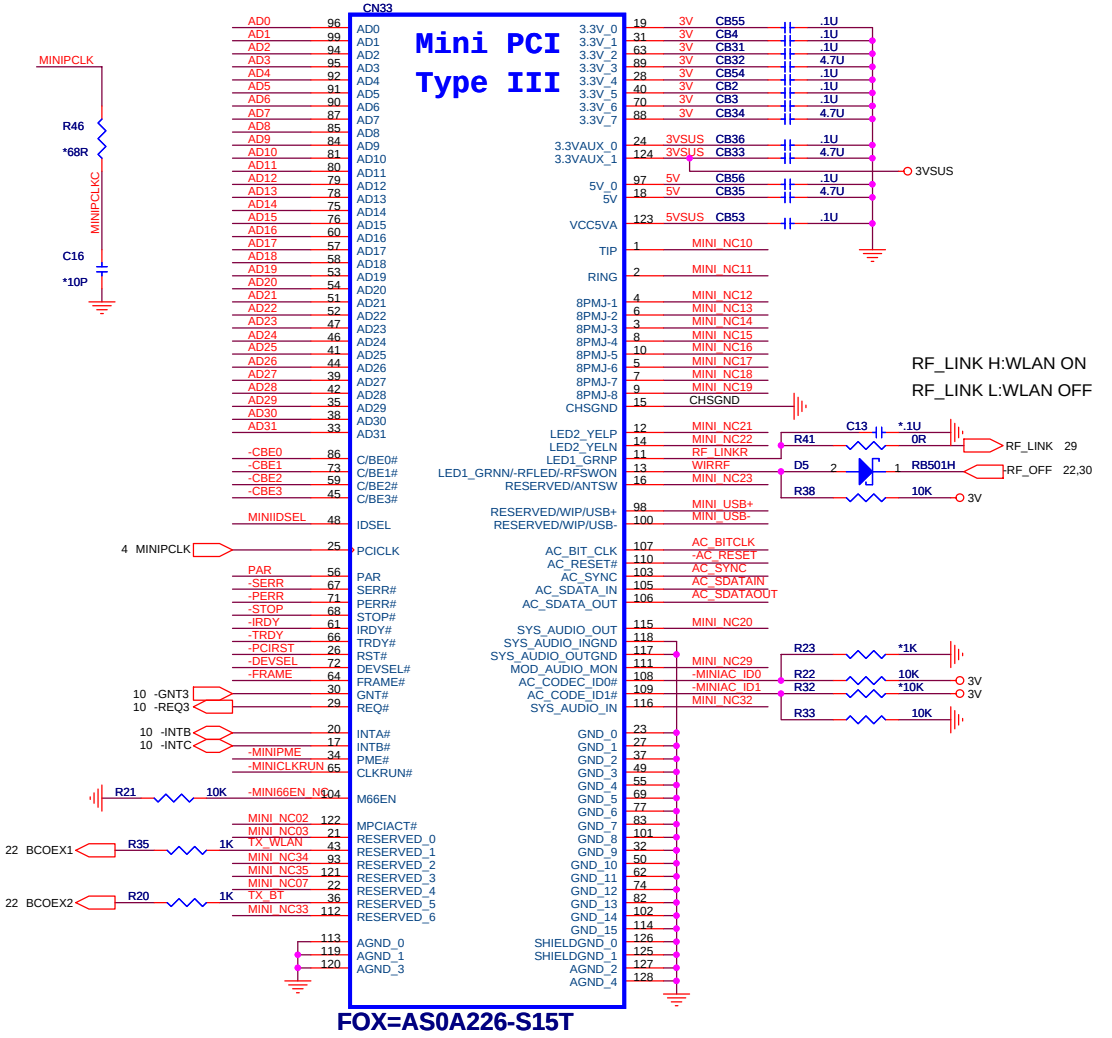
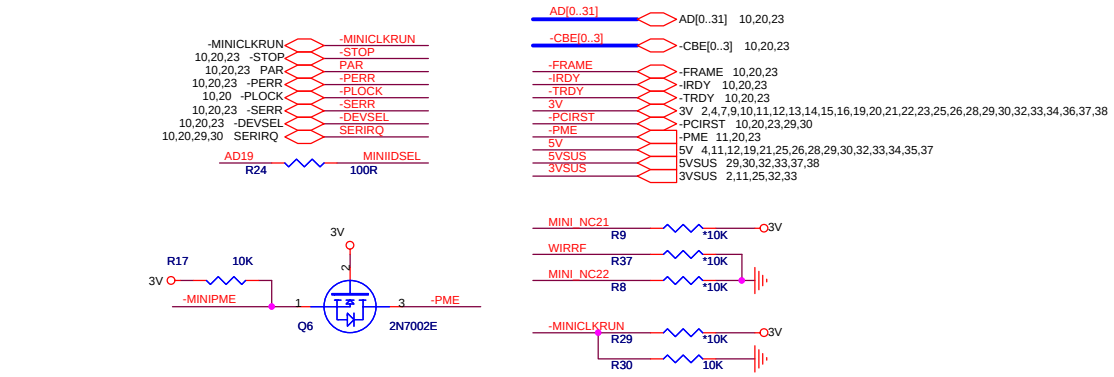
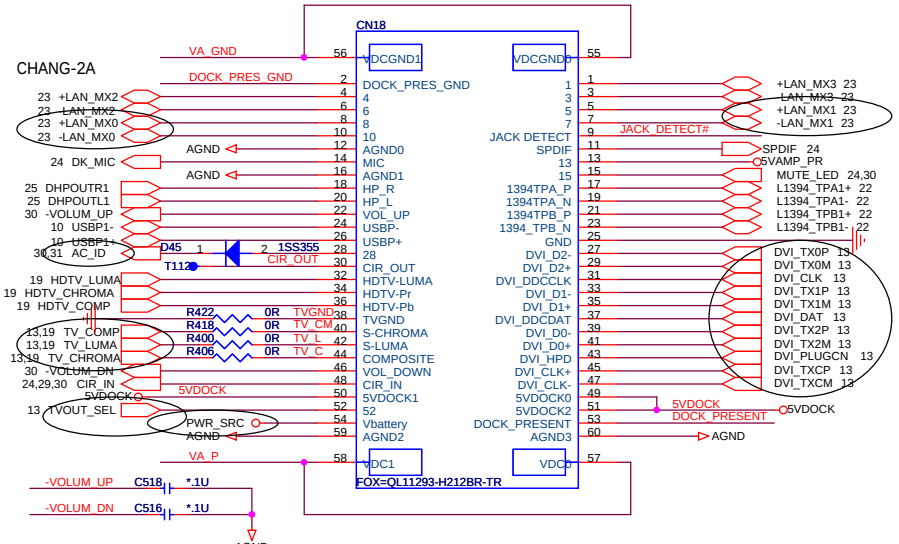
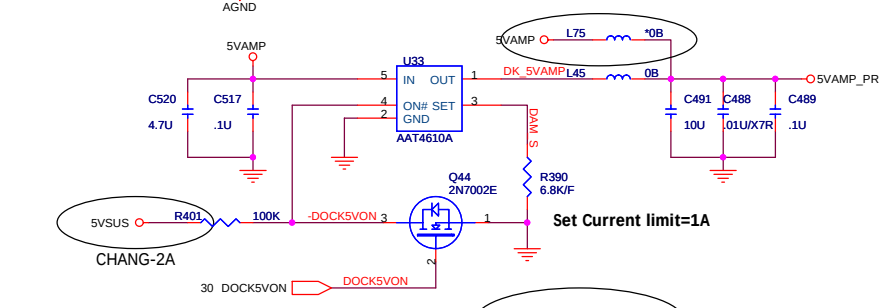
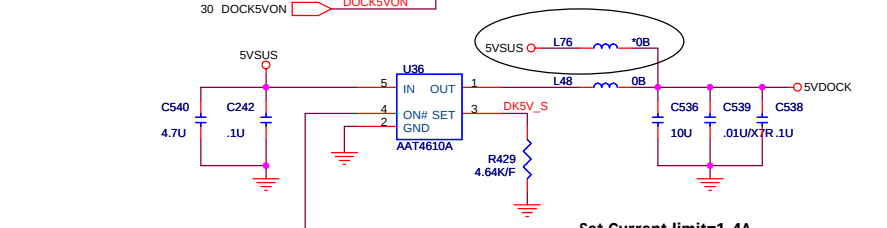
(Don't support AC-LINK)

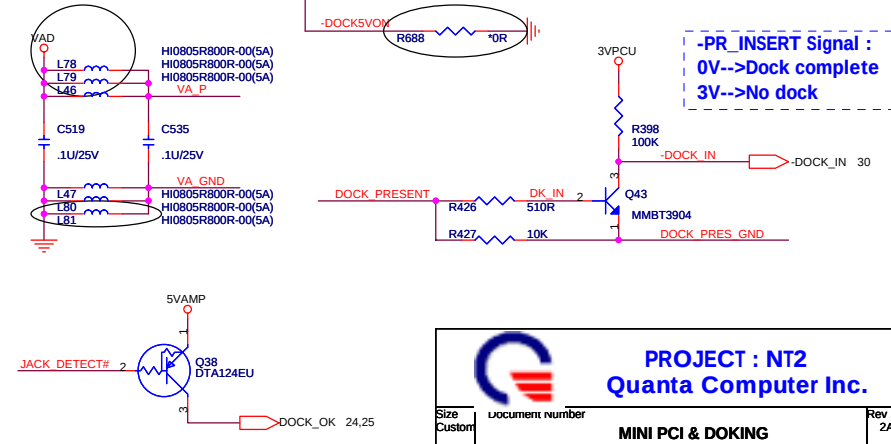




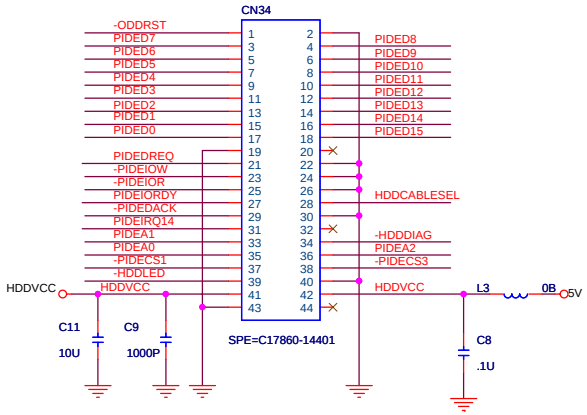




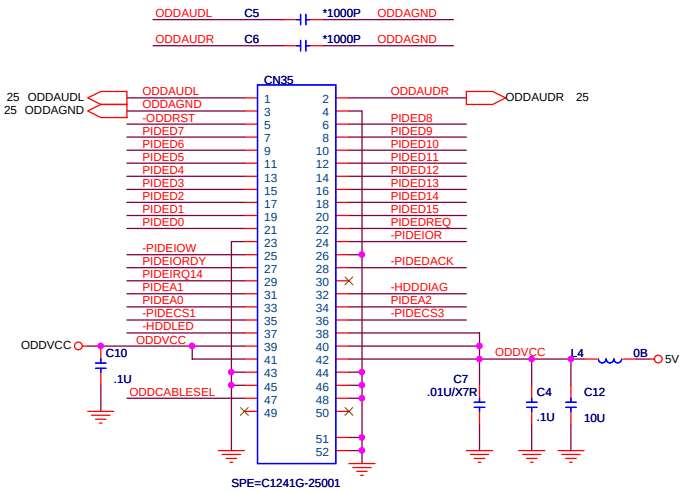


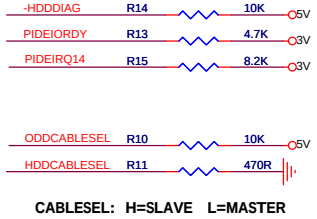


HDD CONNECTOR

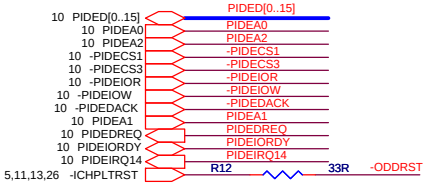


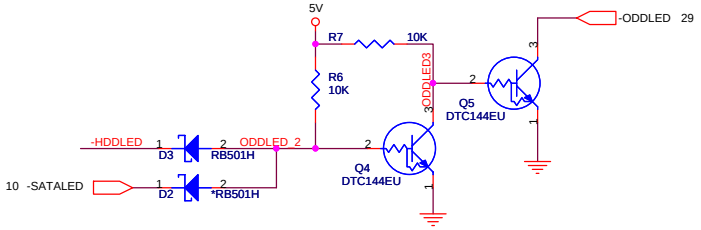
ODD CONNECTOR





CABLESEL: H=SLAVE L=MASTER

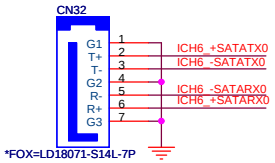


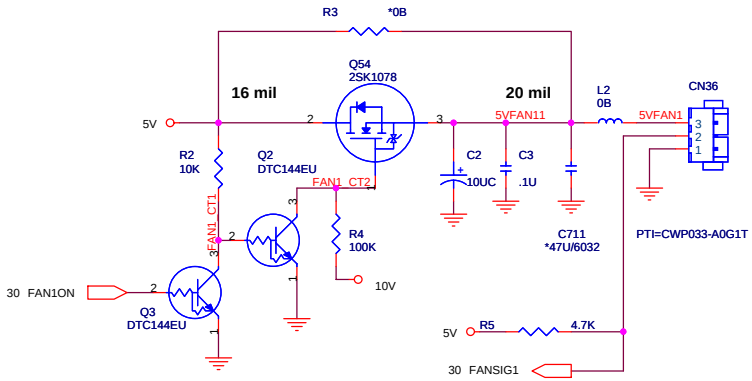


PLACEMENT NOTICE :

1. PUT THE BYPASS CAP AND INDUCTOR NEAR THE HDD AND ODD CONNECTOR
2. ALL DAMPING RESISTORS SHOULD NEAR ODD AND HDD CONNECOTR RESPECTIVELY
3. ALL PULLUP AND PULLDN SHOULD NEAR THE CONNECTOR
4. ALL IDE TRACE SHOULD KEEP 5:15 ID POSSIBLE AND 5:10 IS MINIMUM REQUIREMENT

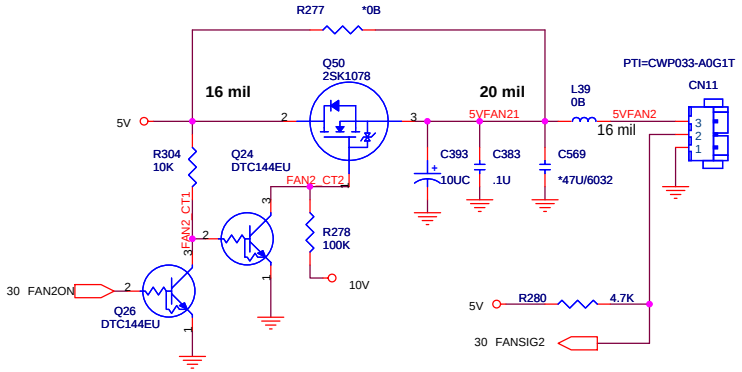
SATA HDD CONNECTOR

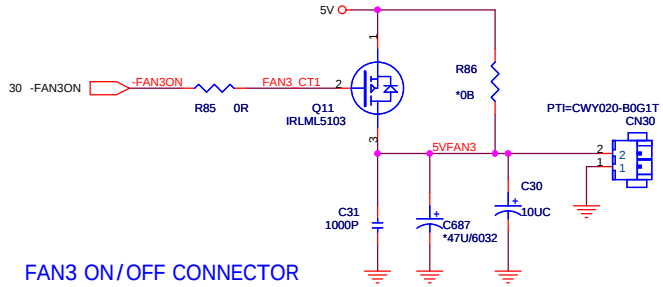




FAN1 PWM CONNECTOR

FAN2 PWM CONNECTOR





FAN3 ON/OFF CONNECTOR

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Quanta Computer Inc.

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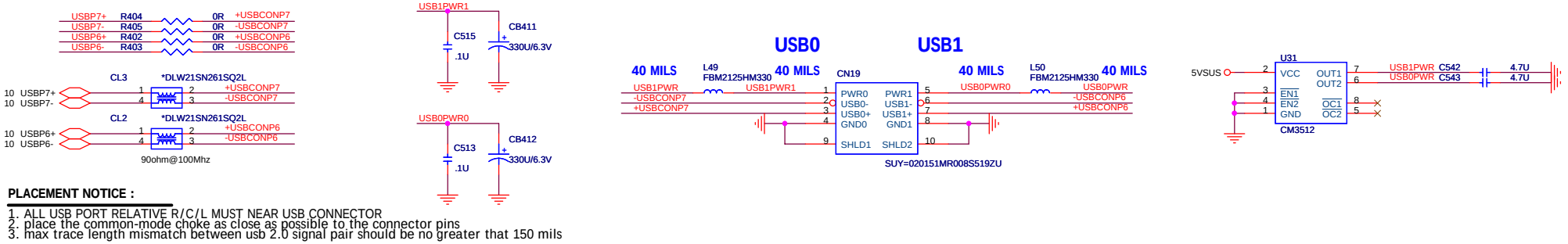
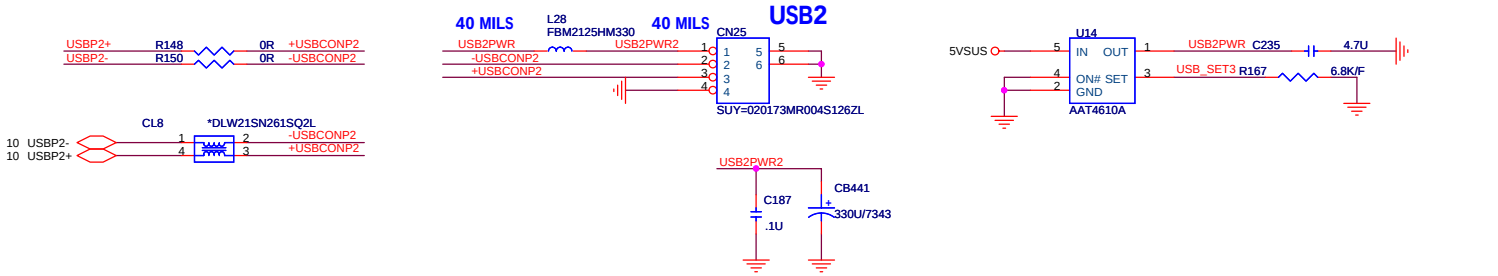
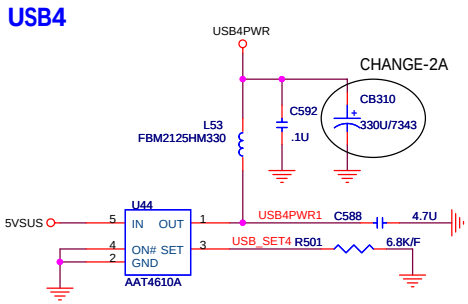
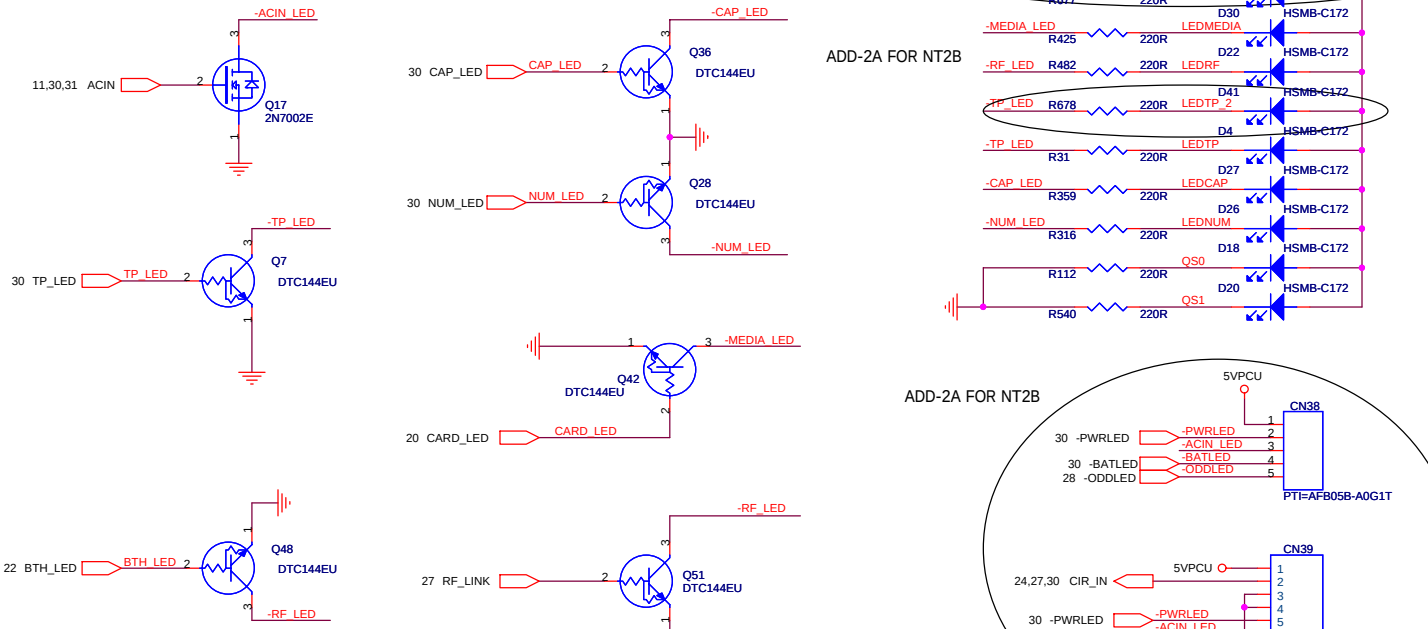


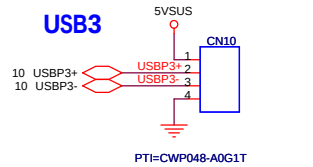
PLACEMENT NOTICE :

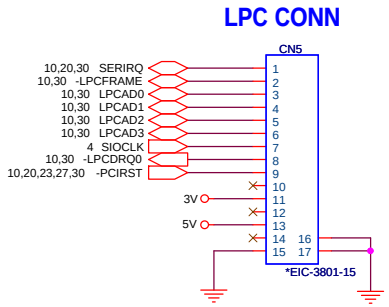
1. ALL USB PORT RELATIVE R/C/L MUST NEAR USB CONNECTOR
2. place the common-mode choke as close as possible to the connector pins
3. max trace length mismatch between usb 2.0 signal pair should be no greater that 150 mils











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Quanta Computer Inc.

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Custom	USB PORT/LED	2A
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KBC-NS87591L

-LDRQ(pin 8) internal is no use

PIN	NS PC87591		ENE KB3910	
11	NC		TEST_TP	High: Clock Test Mode. Low: 32KHz clock in normal running. (Recommend)
12	NC		DPLL_TP	High: Test mode, set KSO [0:15] and KSO16 to become internal output. Low : Normal operation. (Recommend)
105	TINT#		ISP_TP	High: Normal operation. (Recommend) Low: Enable ISP mode.
124	ENV0	Internal pull-down to GND. Set the Enviroment to OBD which is used for debugging the PC87591 firmware while it is mounted on its final production board.	A0	
125	ENV1	External pull-up to 3VPCU by 10k. Set the Enviroment to OBD which is used for debugging the PC87591 firmware while it is mounted on its final production board.	XIOP_TP	High: Enable the internal pull-up resistor on XIOCS [F:0] pins. Low: Disable the internal pull-up resistor on XIOCS [F:0] pins.
126	BADDR0	Internal pull-down to GND. To set Super I/O configuration Base Address.	A2	
127	BADDR1	Internal pull-down to GND. To set Super I/O configuration Base Address.	A3	
128	TRIS	Internal pull-down to GND. Normal operation.	DMRP_TP	High: Disable Memory Remapping Process. (Recommend) Low : Enable Memory Remapping Process.
131	SHBM	External pull-up to 3VPCU by 10k. Enable shared memory with host BIOS.	EMWB_TP	High: Enable Memory while Boot. (Recommand for shared BIOS application) Low: Disable Memory while Boot.

I/O Address

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

EEPROM

BIOS ROM

AKE248RKK09 FOR BIOS ROM

KEYBOARD PULL-UP

TOUCH PAD

PC87591VPC

Pin 103 internal is "A19",Can't use to GPIO

Pin 24 if no pull-high, will can't reboot.

Package Change-2A

BOM-2A

VOLUME DOWN	/ MX5-MY15
VOLUME UP	/ MX4-MY15
TOUCH PAD	/ MX1-MY15
MUTE	/ MX0-MY15

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Quanta Computer Inc.

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C	KBC PCU-87591	2A

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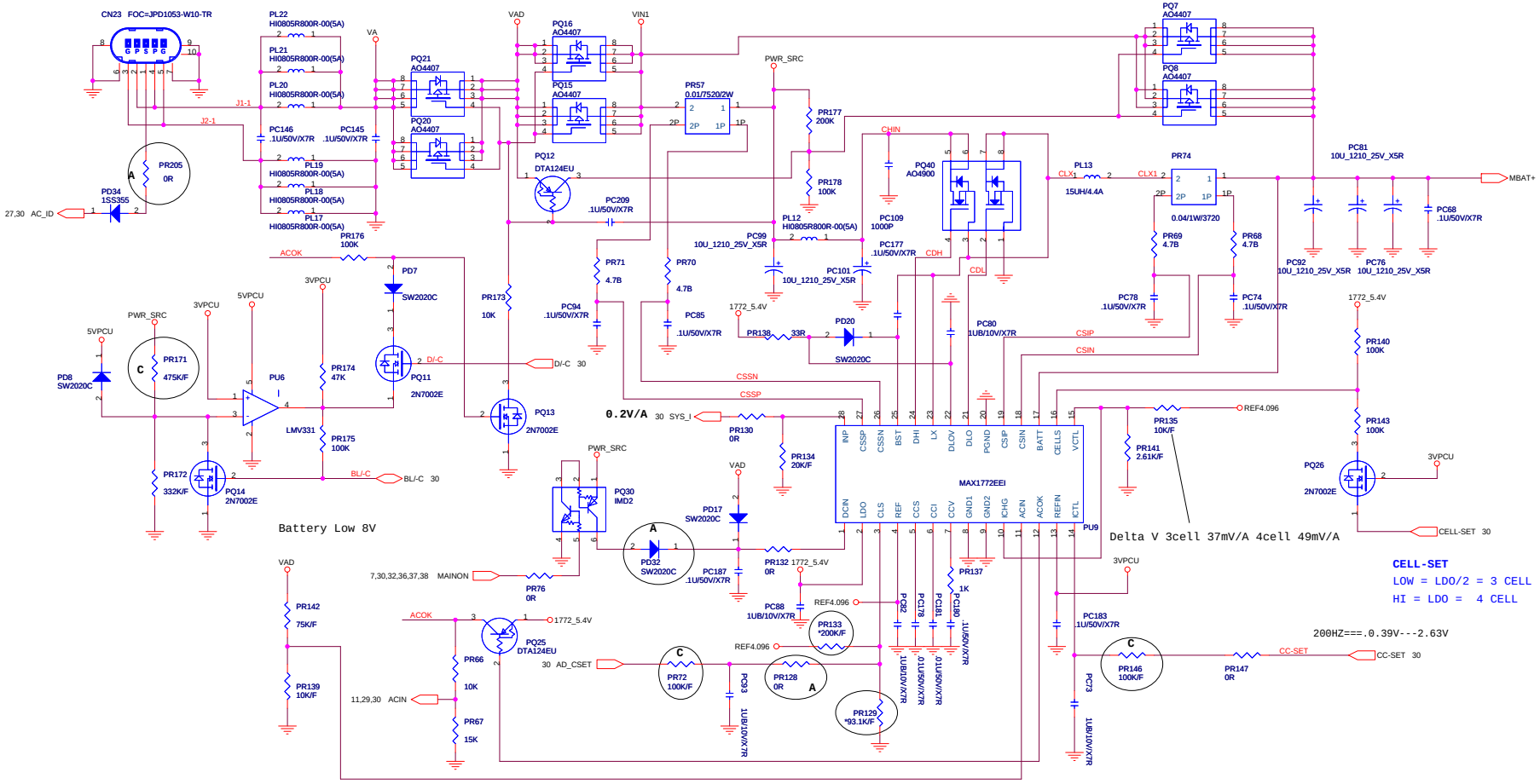
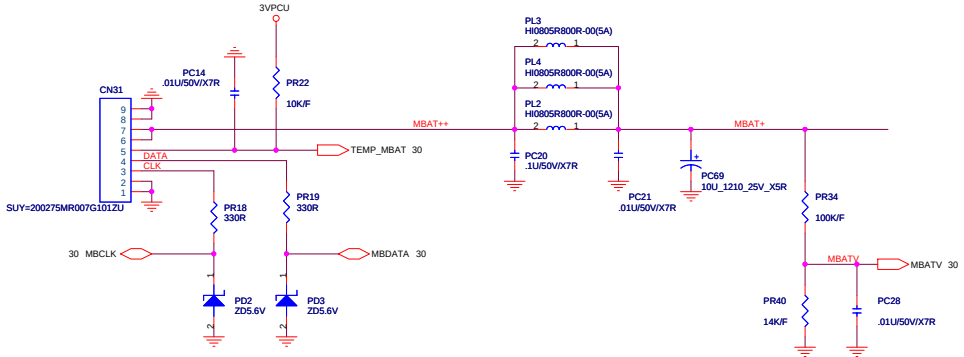
BATTERY CHARGER





AD SET

120W	1.26V
135W	1.42V
160W	1.73V
180W	1.89V
200W	2.10V
220W	2.31V

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
C	BATTERY CHARGER 1772	2A
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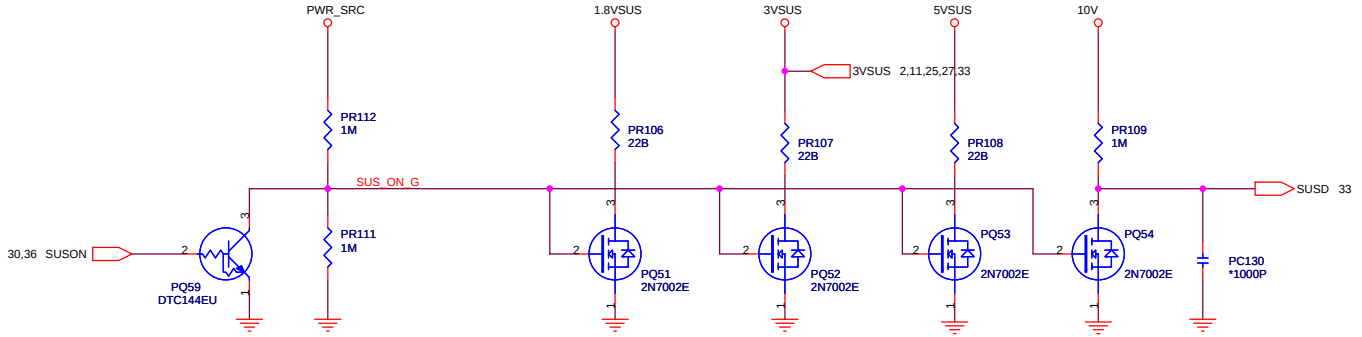

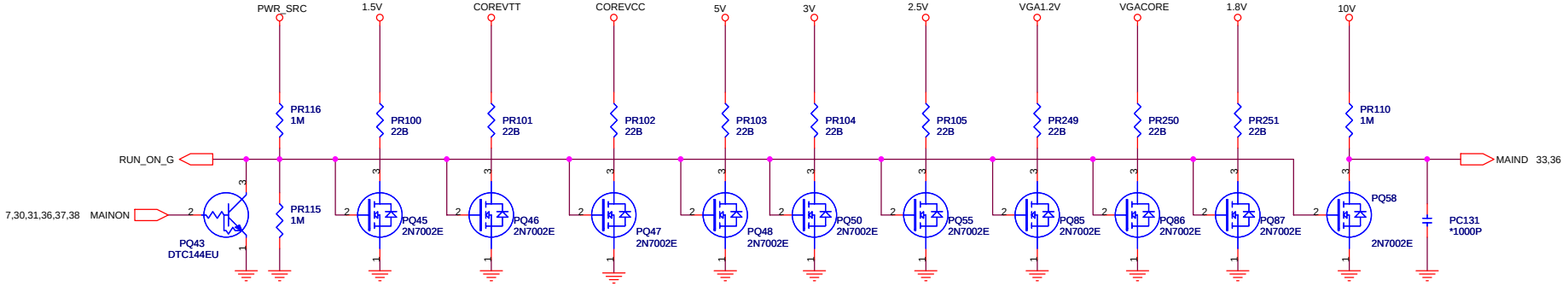

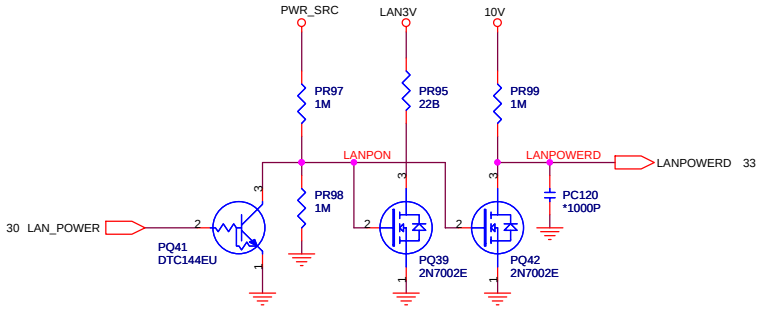

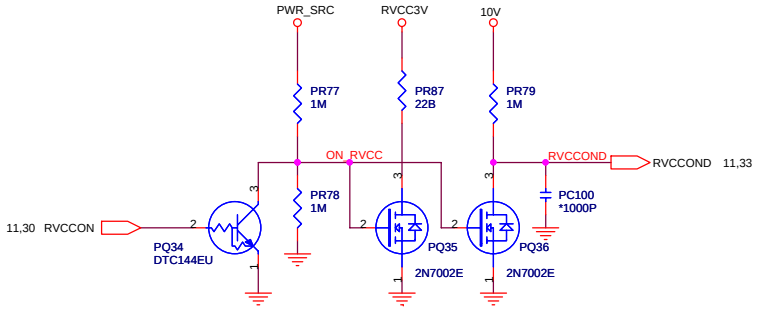

PROJECT : NT2
Quanta Computer Inc.

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Custom	DISCHARGE CIRCUIT	2A
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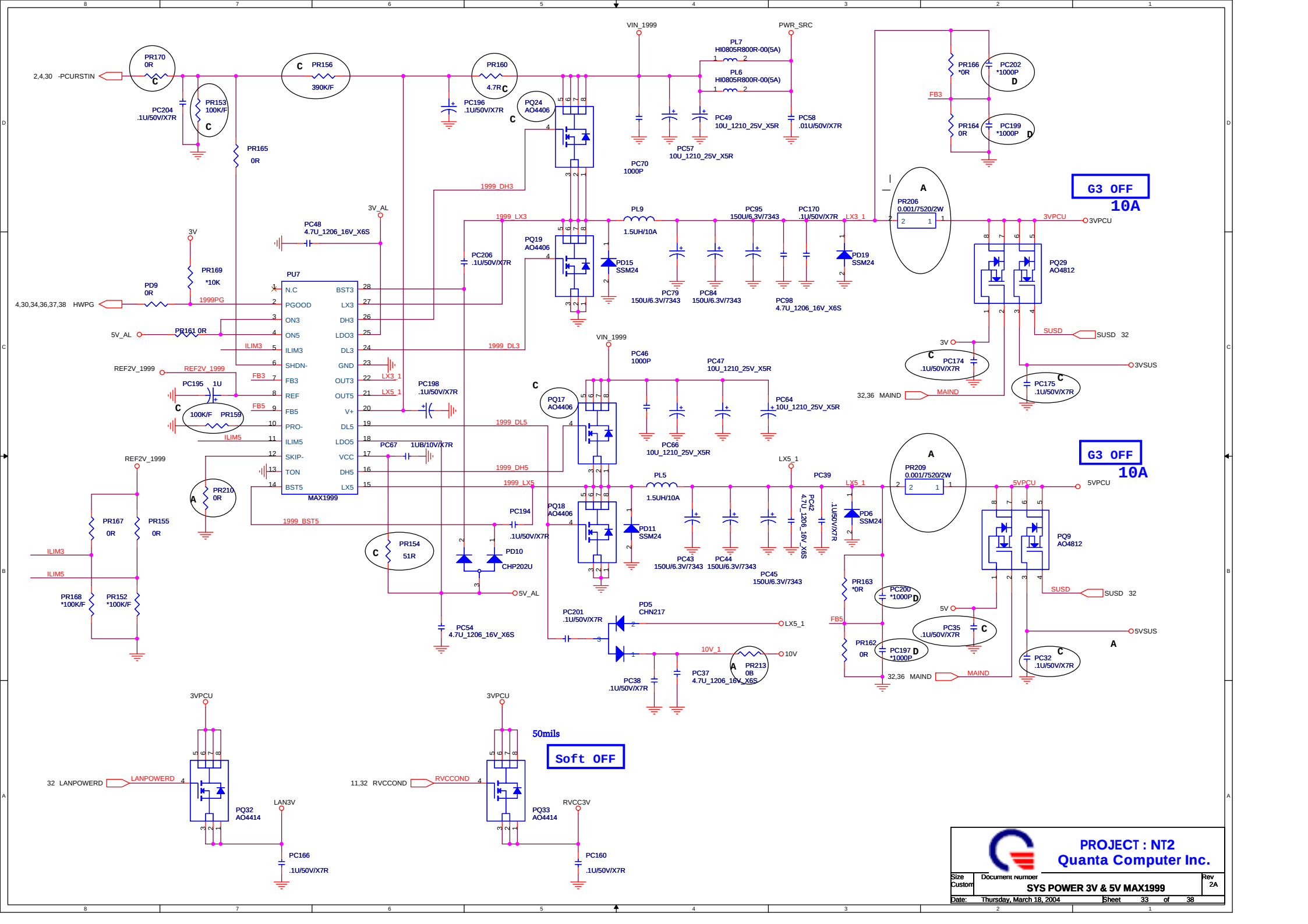
G3 OFF
10A
G3 OFF
10A
Soft OFF
50mils
MAX1999
PU7
PROJECT : NT2
Quanta Computer Inc.
SYS POWER 3V & 5V MAX1999
Size: Custom
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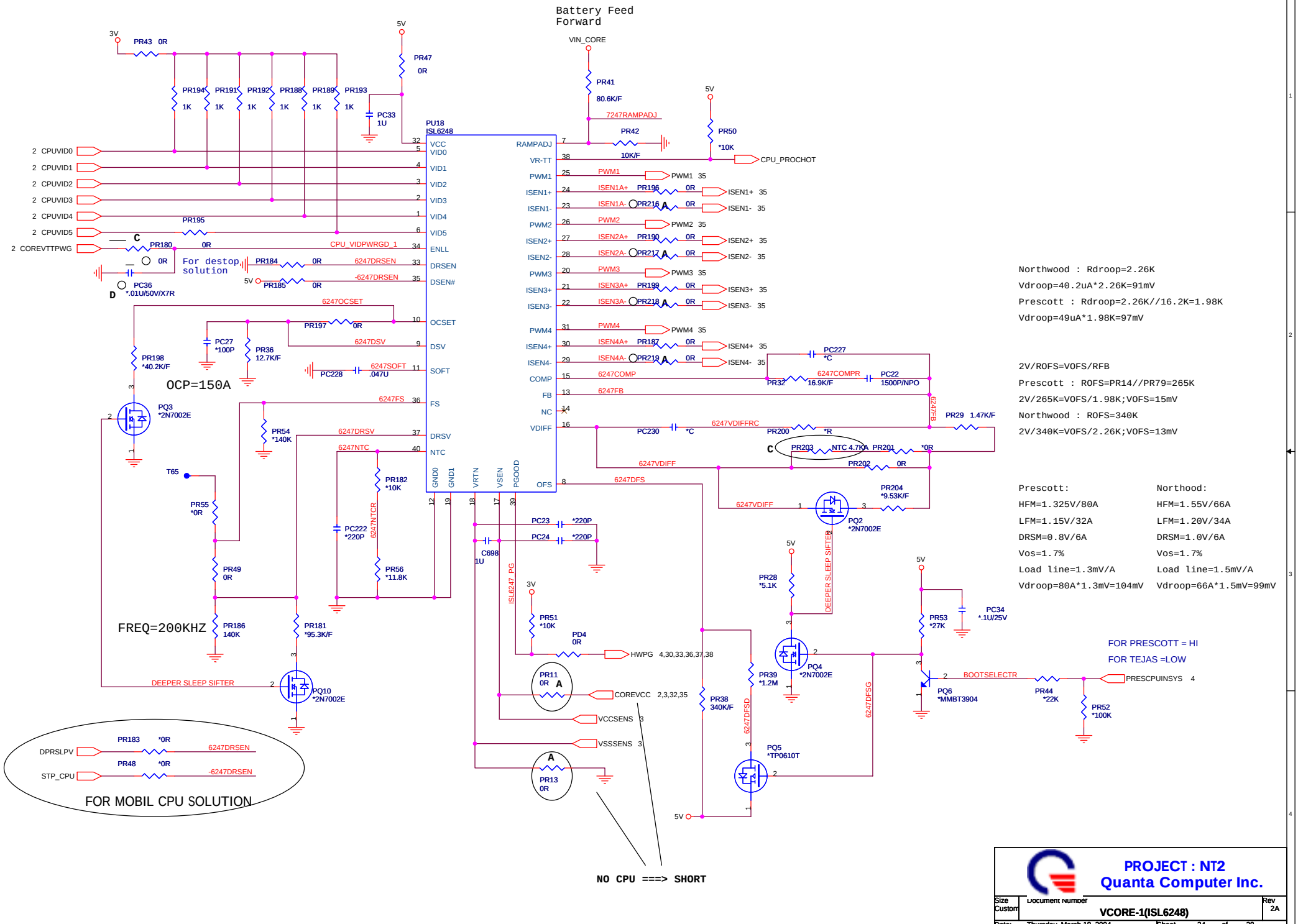

Northwood : Rdroop=2.26K
Vdroop=40.2uA*2.26K=91mV
Prescott : Rdroop=2.26K//16.2K=1.98K
Vdroop=49uA*1.98K=97mV

2V/ROFS=VOFS/RFB
Prescott : ROFS=PR14//PR79=265K
2V/265K=VOFS/1.98K;VOFS=15mV
Northwood : ROFS=340K
2V/340K=VOFS/2.26K;VOFS=13mV

Prescott:	Northood:
HFM=1.325V/80A	HFM=1.55V/66A
LFM=1.15V/32A	LFM=1.20V/34A
DRSM=0.8V/6A	DRSM=1.0V/6A
Vos=1.7%	Vos=1.7%
Load line=1.3mV/A	Load line=1.5mV/A
Vdroop=80A*1.3mV=104mV	Vdroop=66A*1.5mV=99mV

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VCORE-1(ISL6248)	2A
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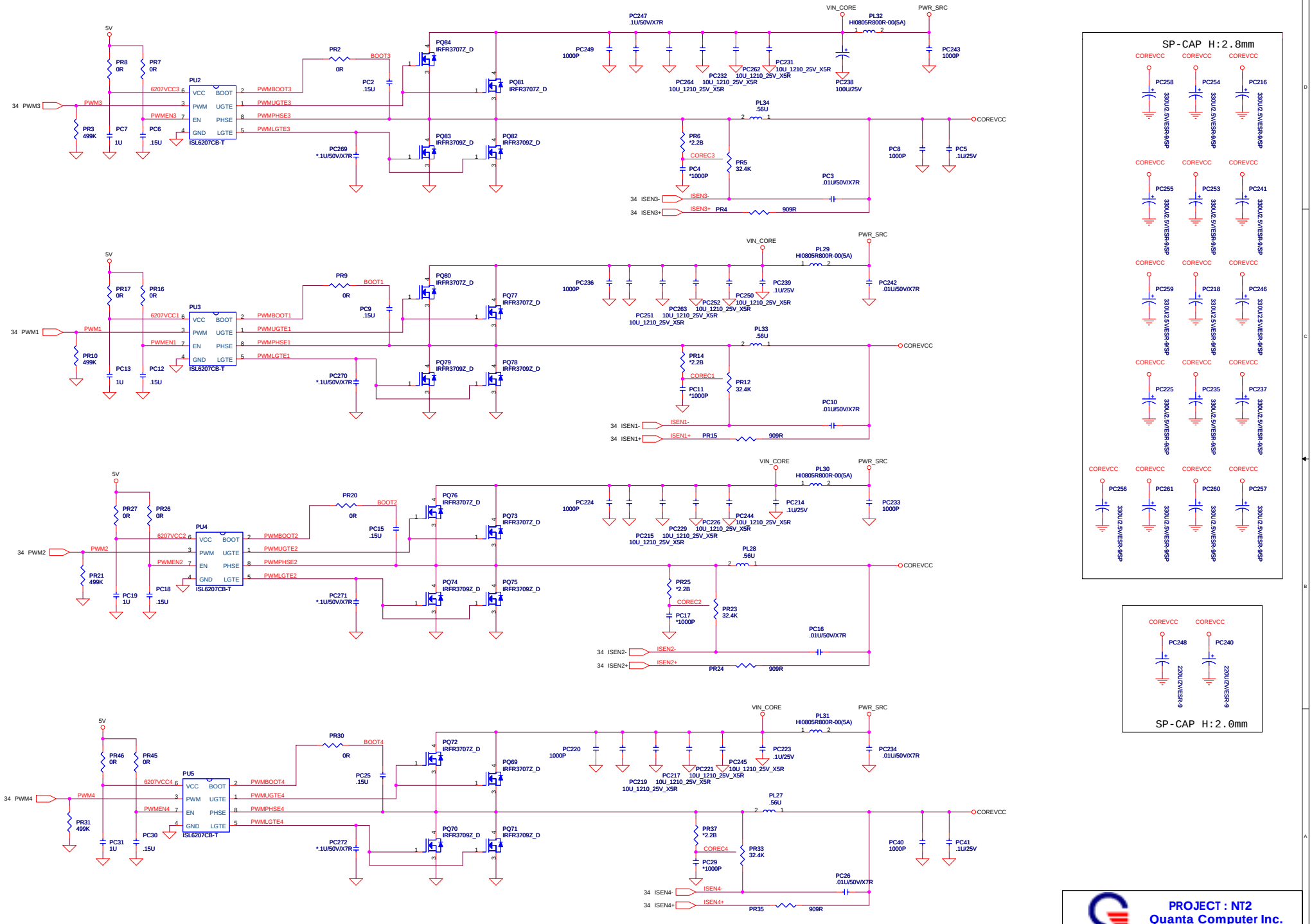

PROJECT : NT2
Quanta Computer Inc.

Size	Document Number	Rev
C	COREVCC (Power train)	2A

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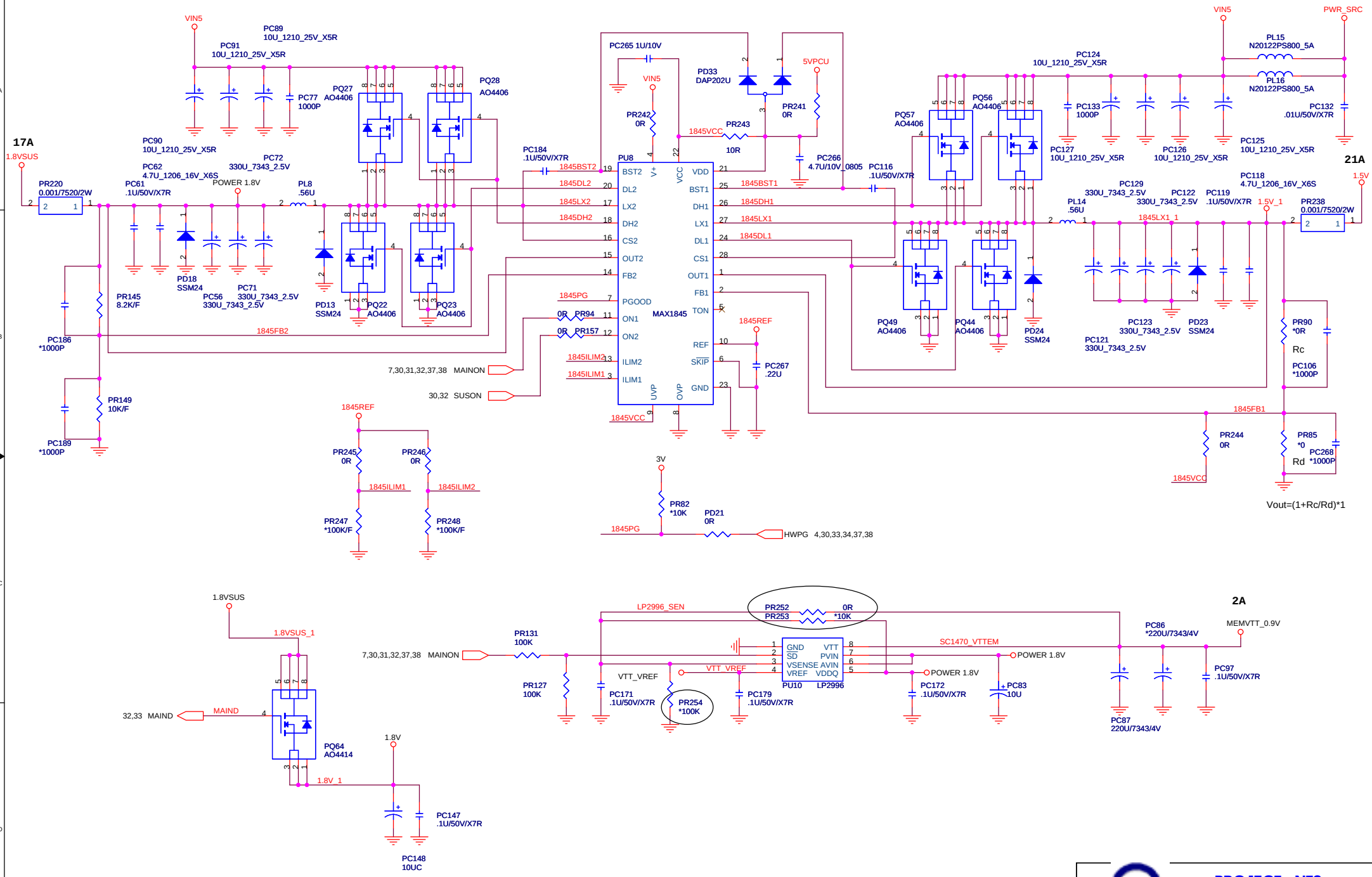
MAX1845



PROJECT : NT2 Quanta Computer Inc.			
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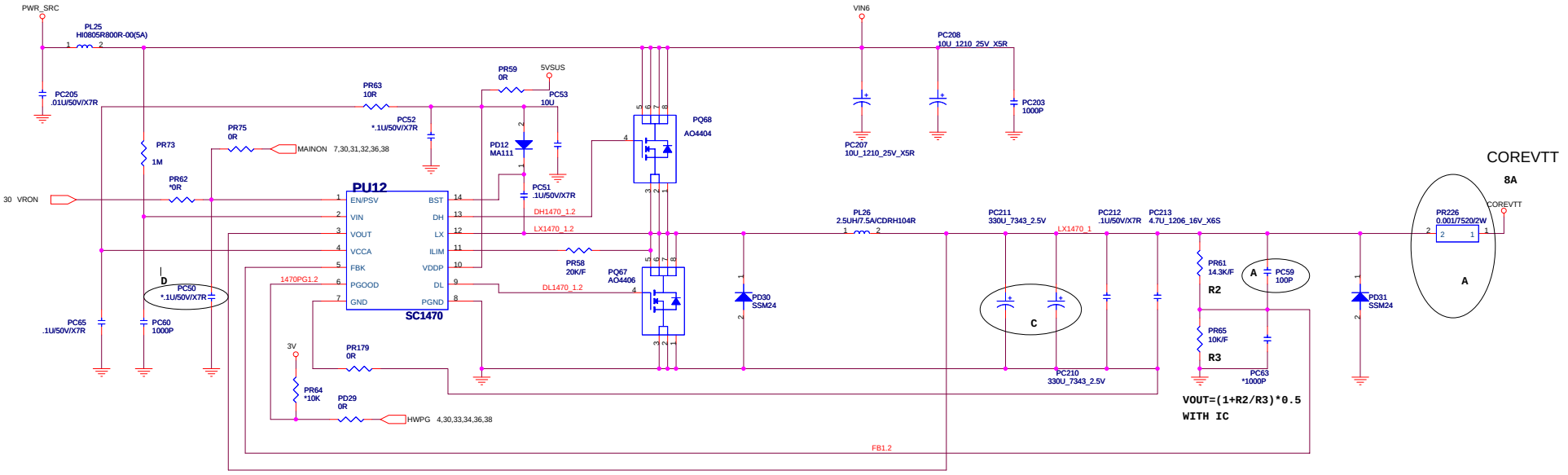

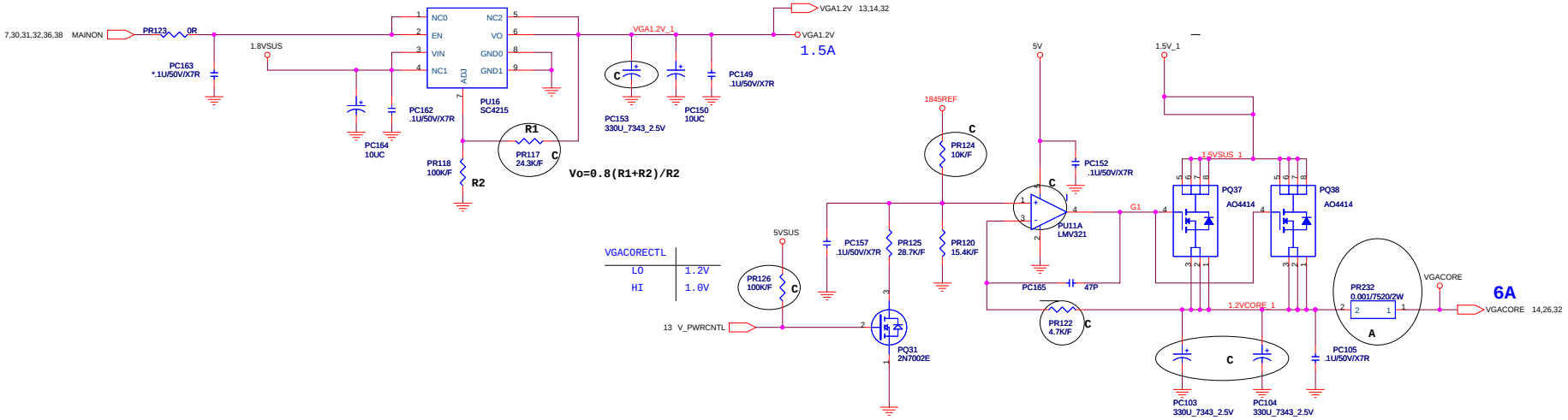

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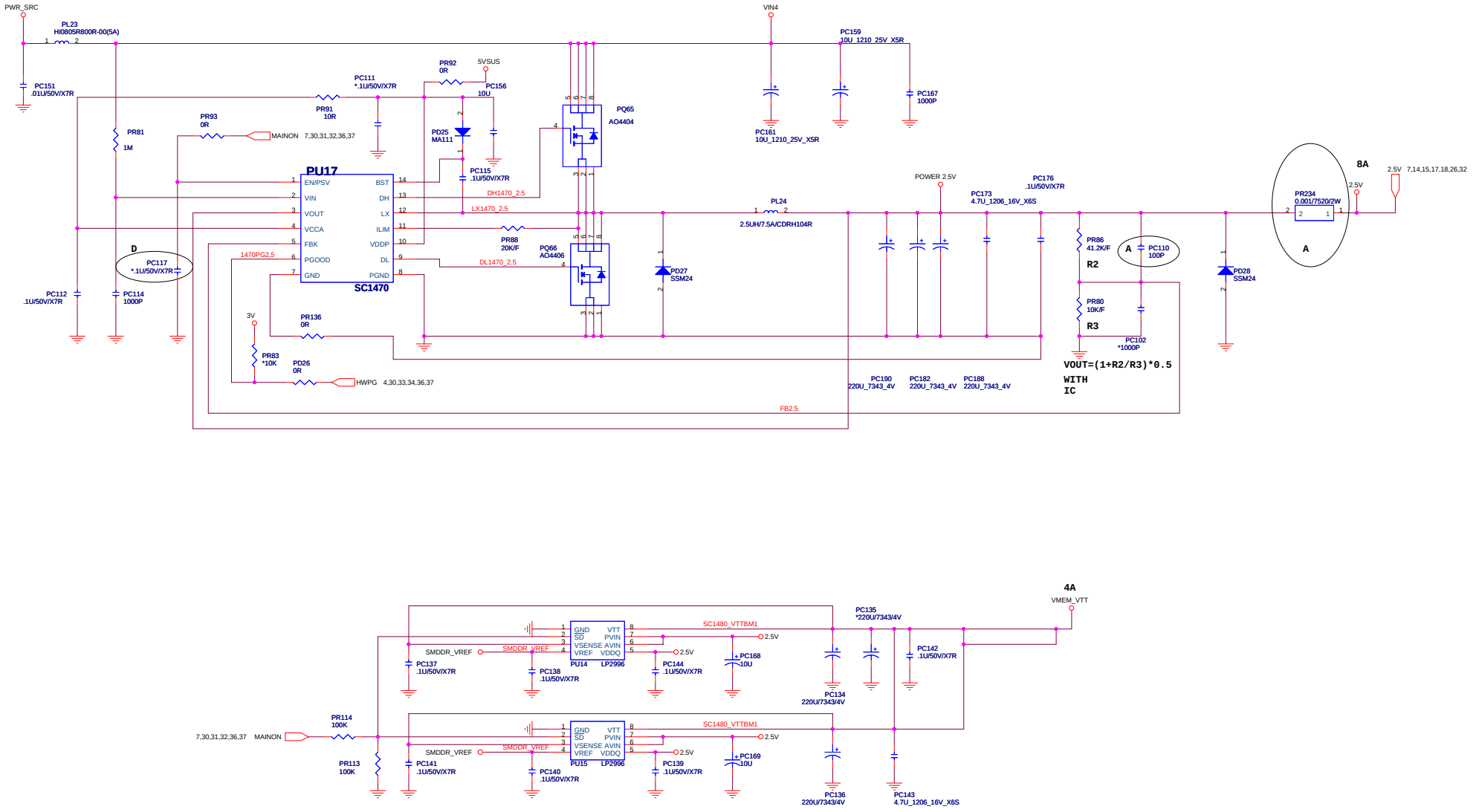

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