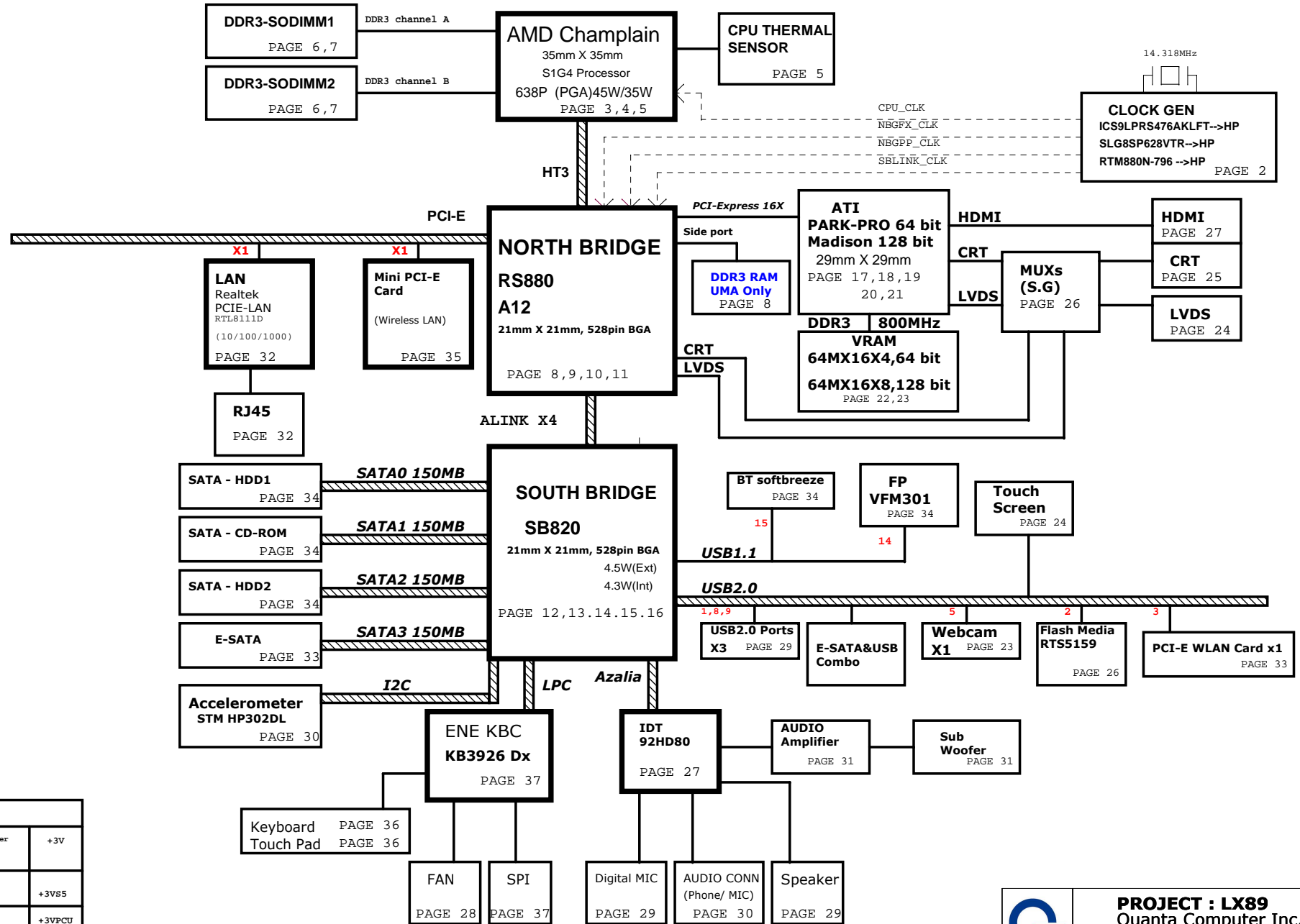


LAYER 1 : TOP
 LAYER 2 : GND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : VCC
 LAYER 6 : BOT

LX89 SYSTEM DIAGRAM

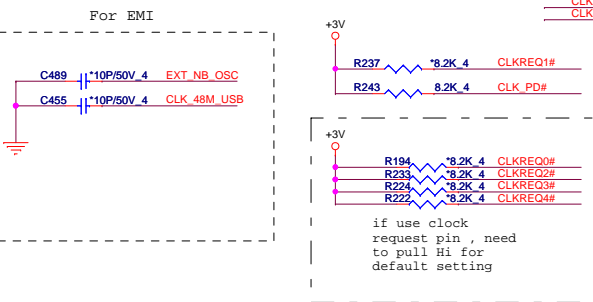
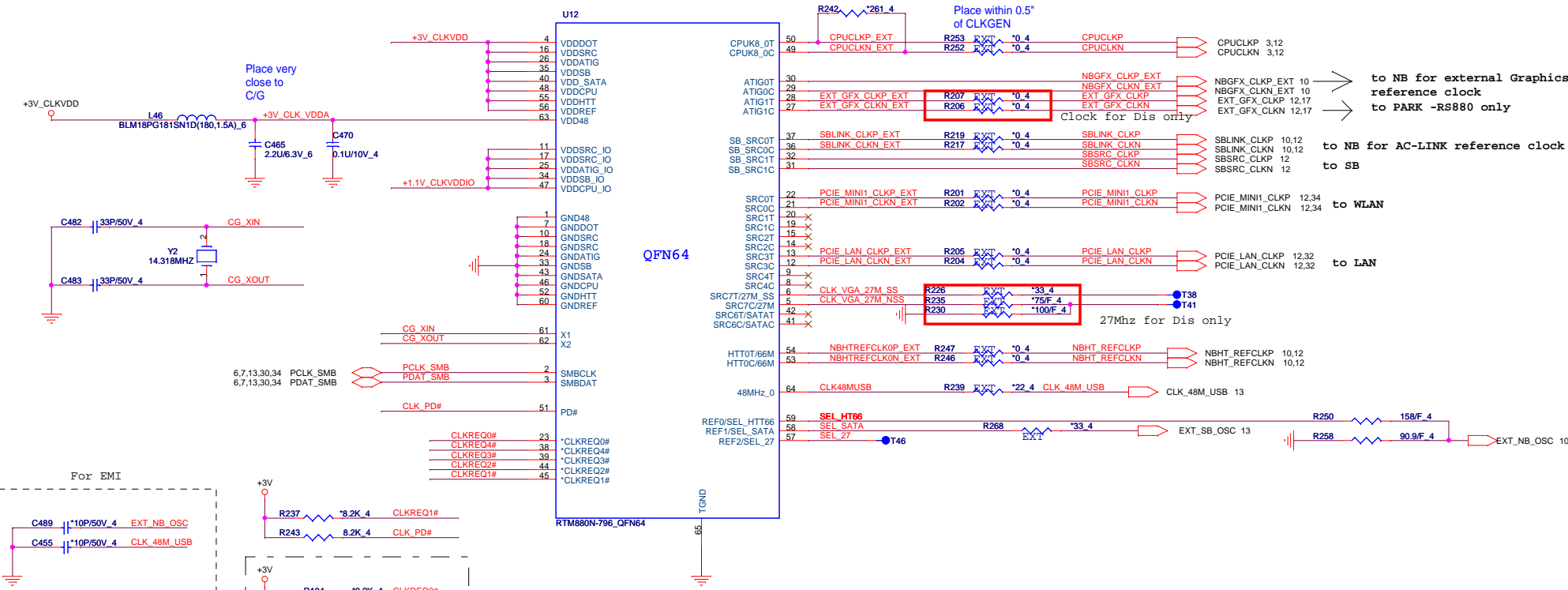
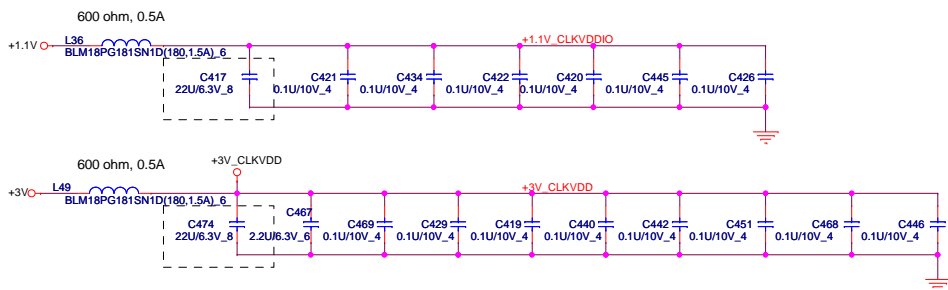


- SYSTEM CHARGER(ISL6251) PAGE 40
- SYSTEM POWER ISL6237 PAGE 34
- DDR II SMD DR_VTERM 1.8V/1.8VSUS(RT8207) PAGE 37
- VCCP +1.1V AND +1.2V(RT8204) PAGE 35
- VGACORE(1.1V~1.2V)Oz8118 PAGE 38
- CPU CORE ISL6265HRTZ-T PAGE 36

SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/FV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	epress card	
	Wlan Card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

PROJECT : LX89
 Quanta Computer Inc.

Size Custom	Document Number	Rev
	Block Diagram	1A
Date: Monday, September 28, 2009 Sheet 1 of 46		

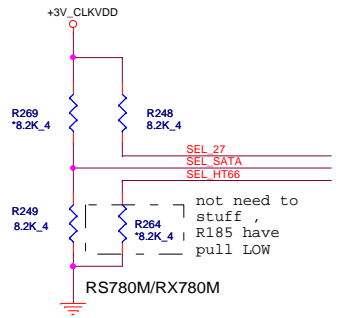


SLG
RTL

SLG8SP628VTR--AL8SP628000
RTM880N-796--AL000880001

* default

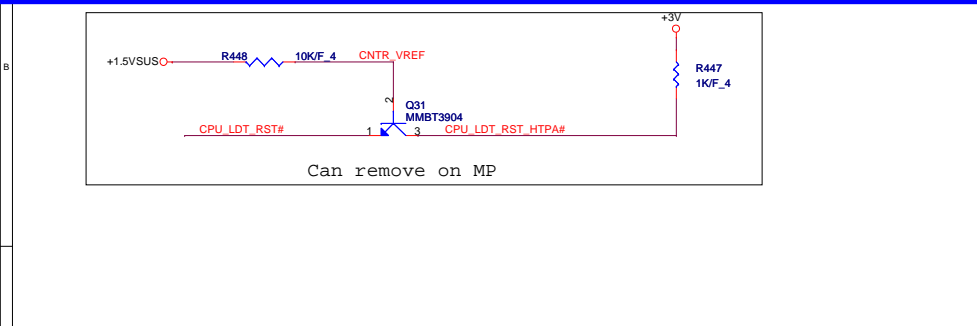
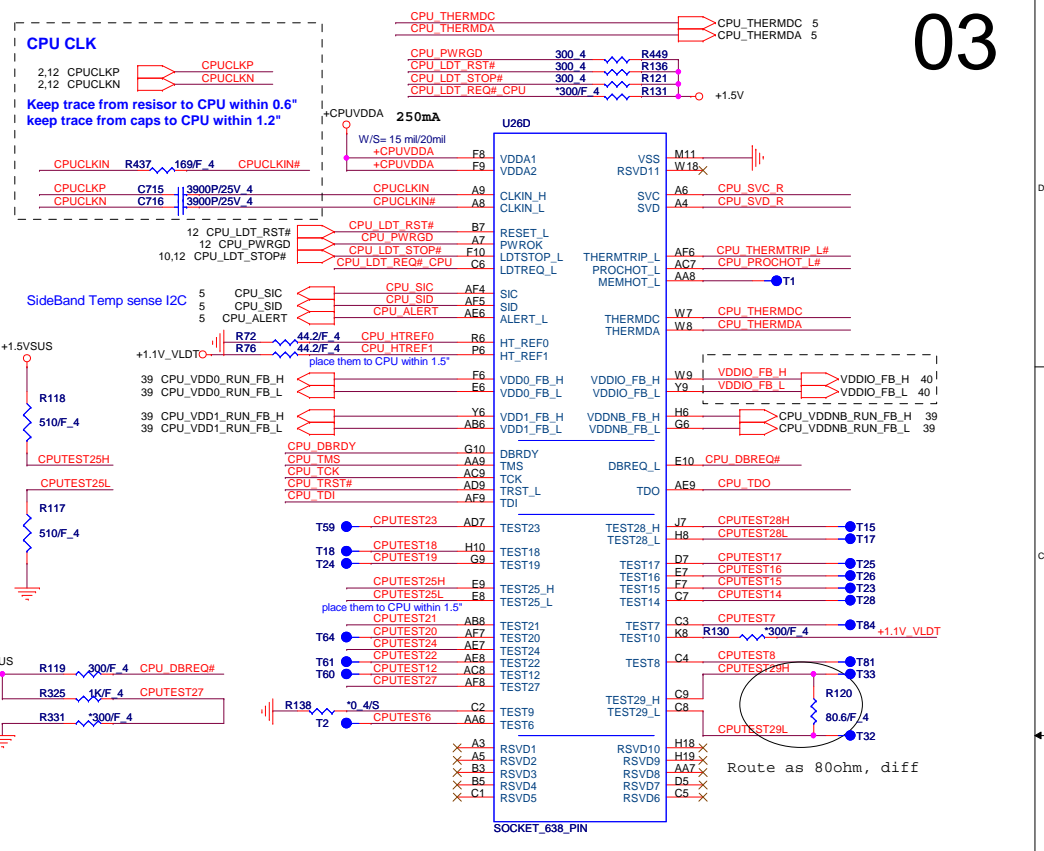
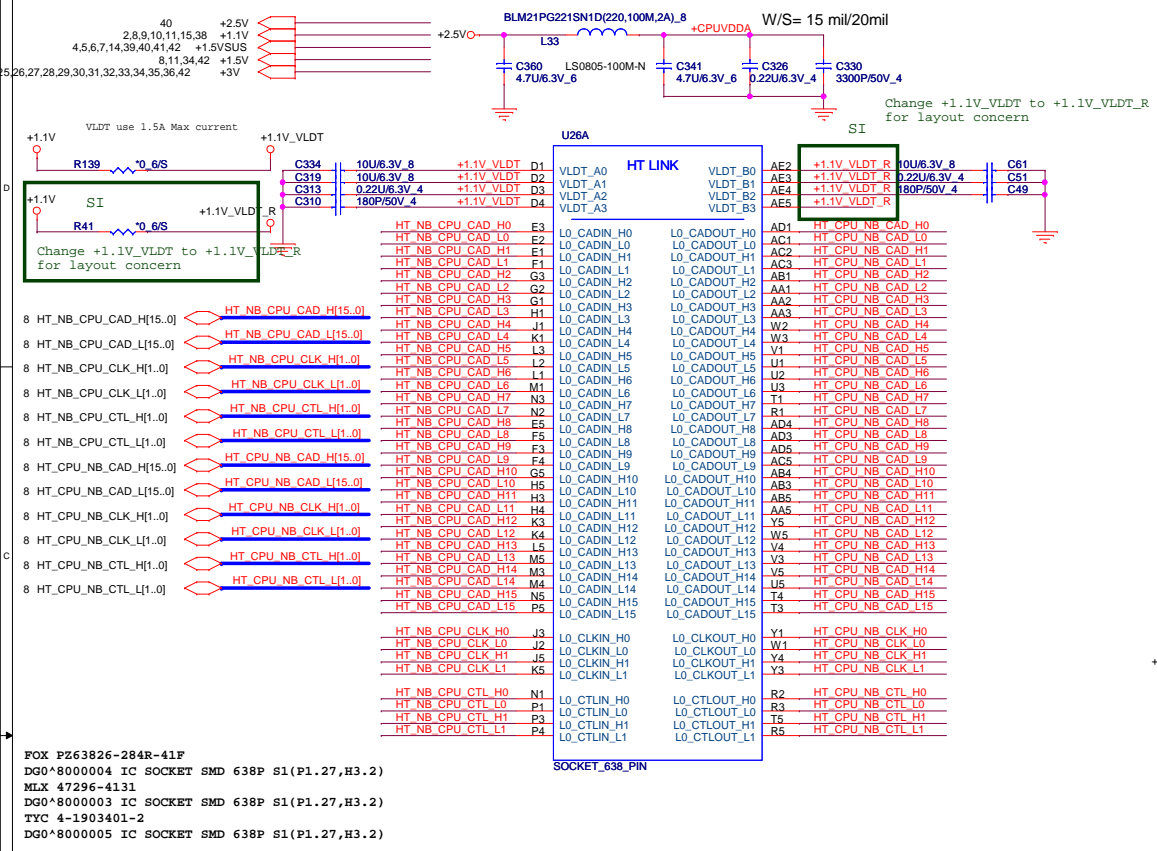
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
SEL_HTT66	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
SEL_SATA	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
SEL_27	0	100 MHz spreading differential SRC clock



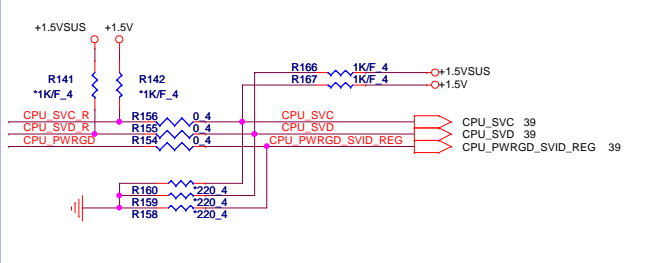
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number Clock Generator	Rev 1A
Date: Monday, September 28, 2009 Sheet 2 of 46		

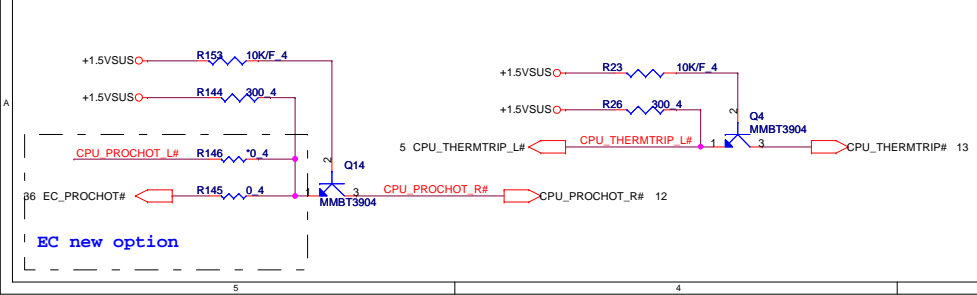


Serial VID

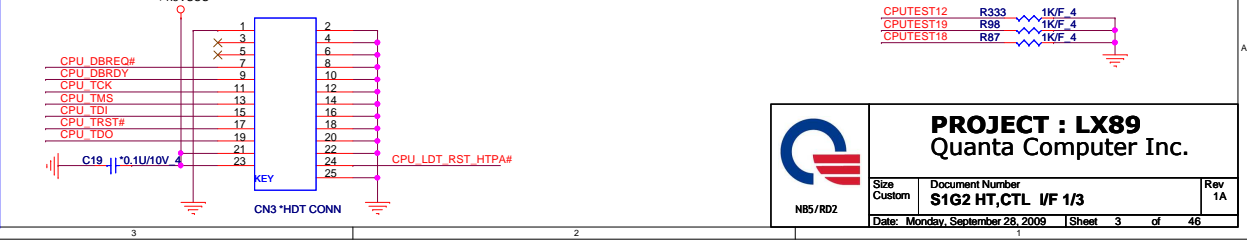


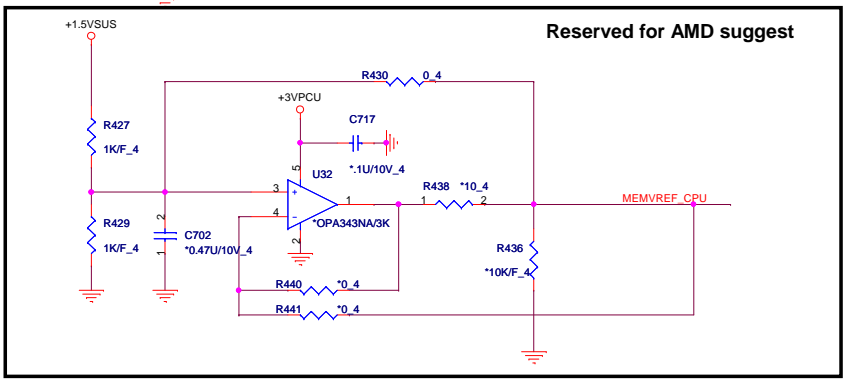
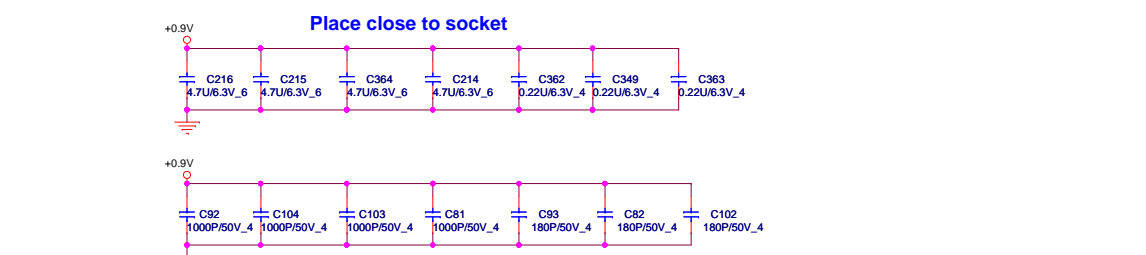
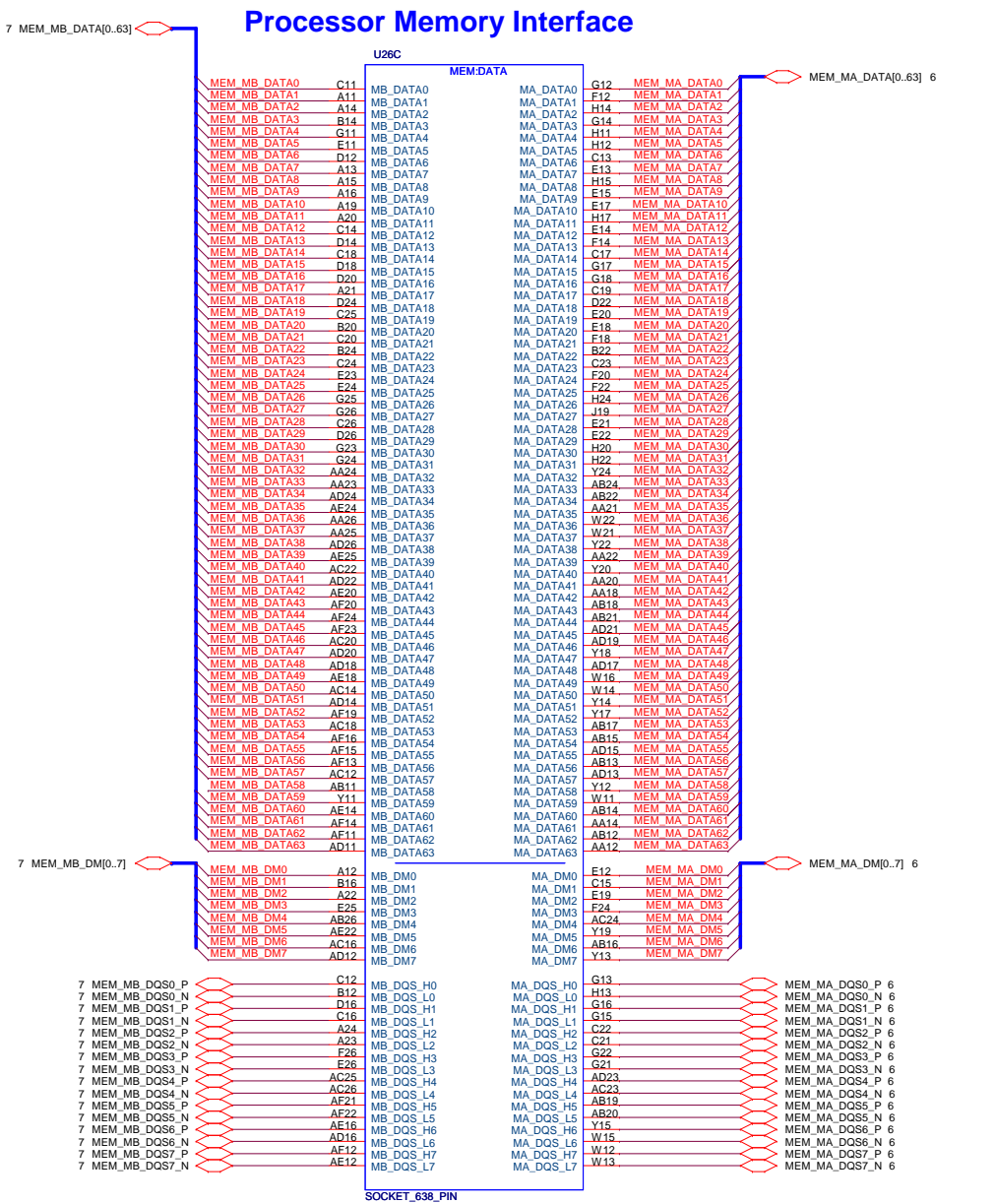
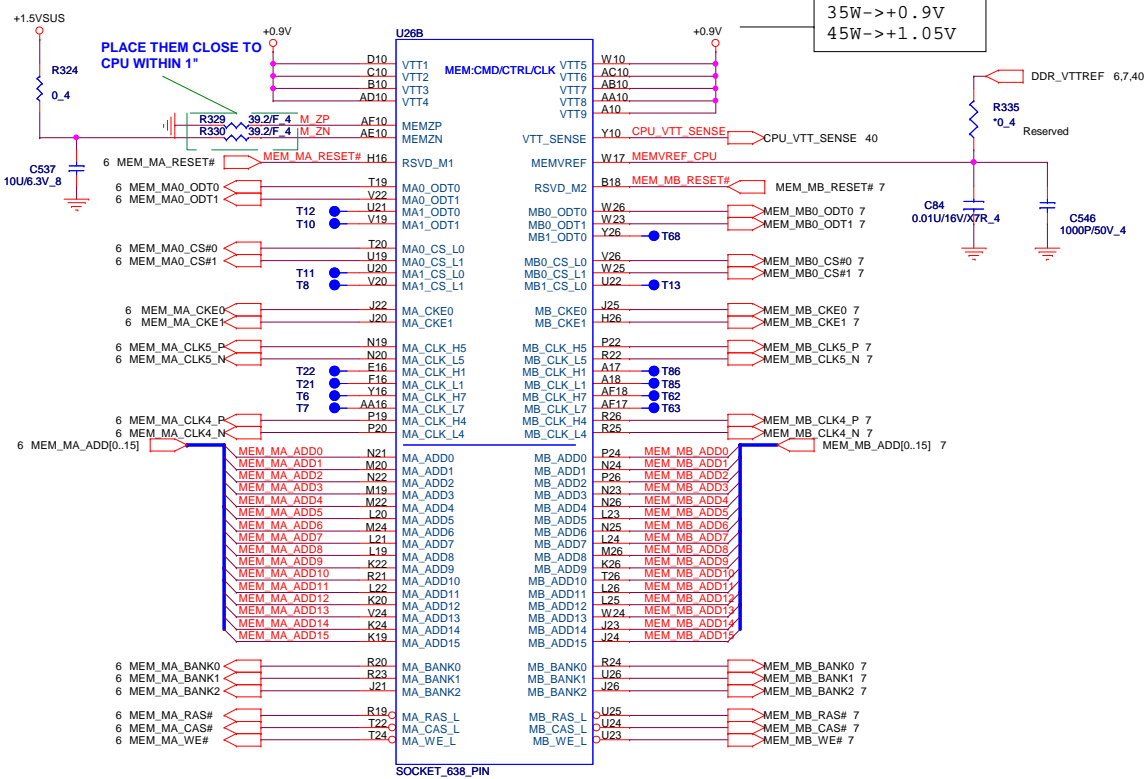
VFIX MODE VID Override table (VDD)

SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V



HDT Connector



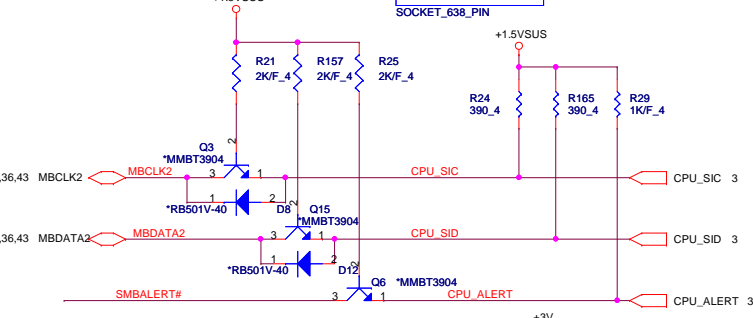
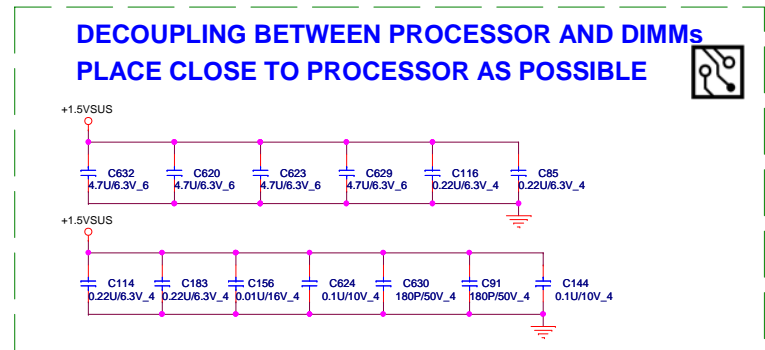
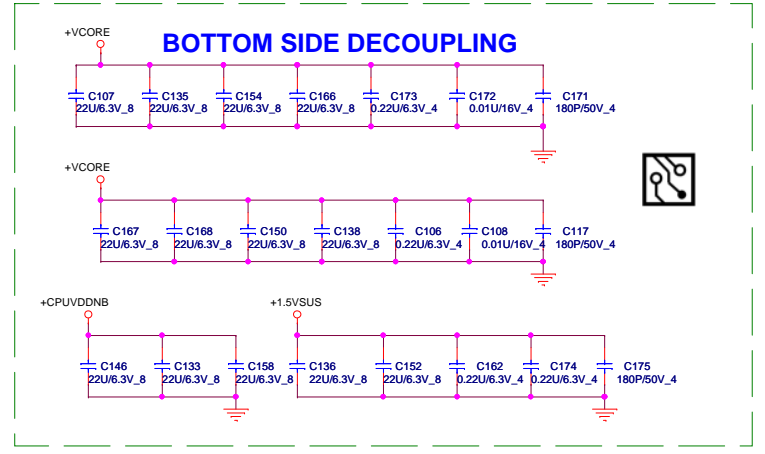
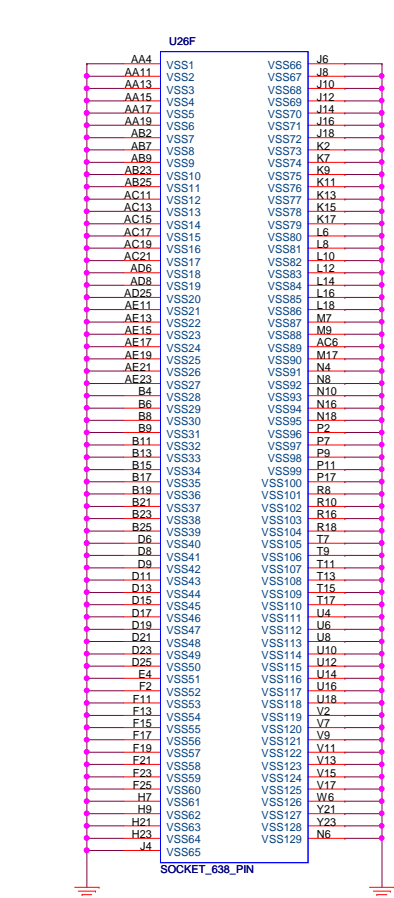
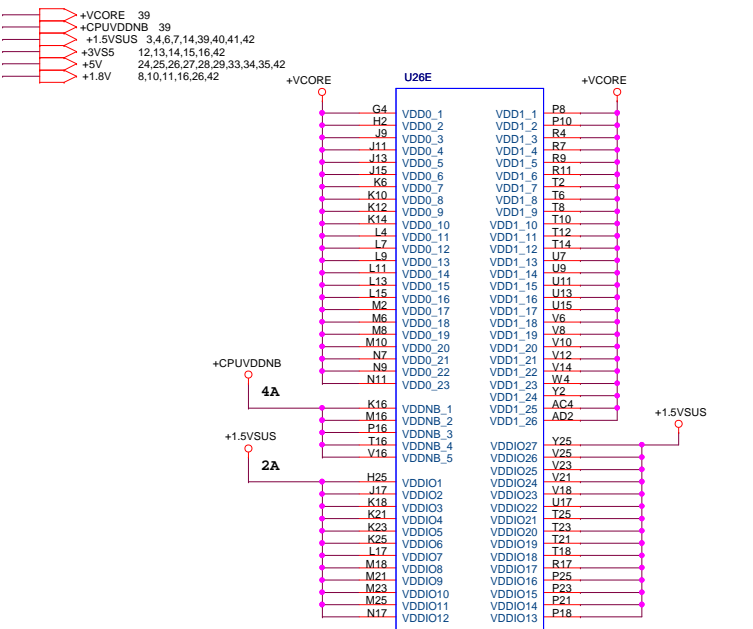


PROJECT : LX89
Quanta Computer Inc.

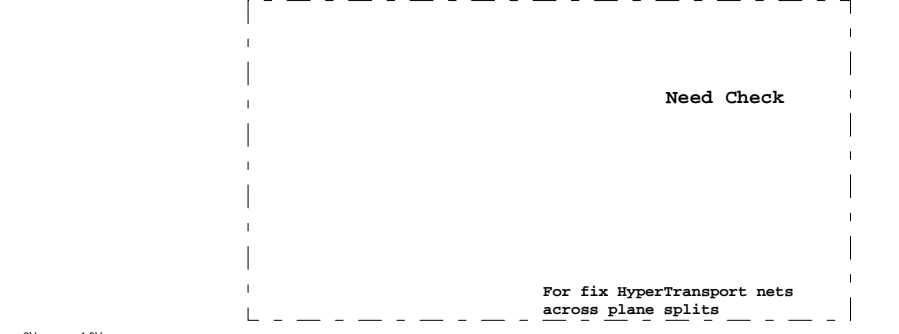
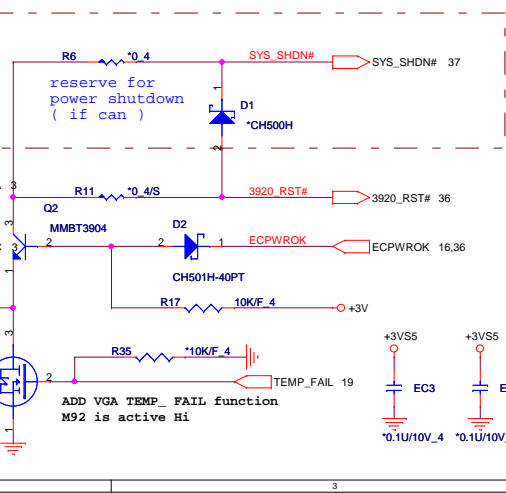
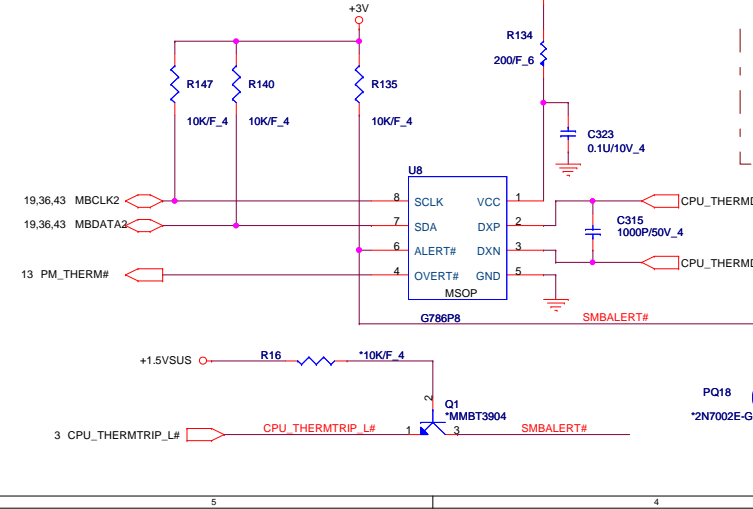
Size Custom Document Number **\$1G2 DDRII MEMORY U/F 2/3** Rev 1A

Date: Monday, September 28, 2009 Sheet 4 of 46

NBS/RD2

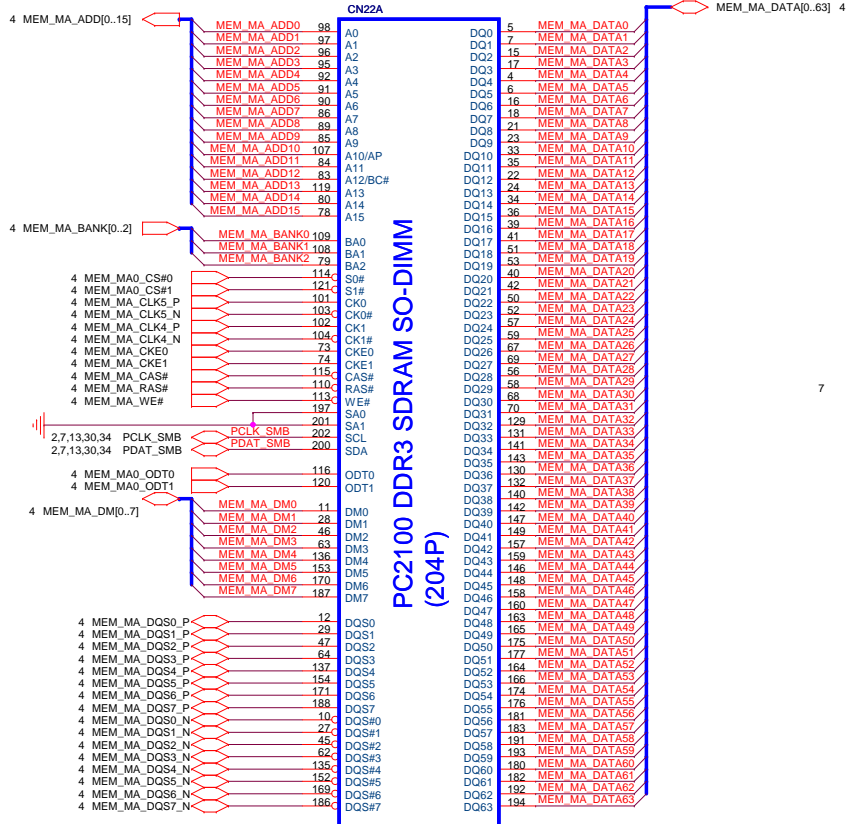


PROCESSOR POWER AND GROUND



	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number S1G2 PWR & GND 3/3	
Date: Monday, September 28, 2009		Sheet 5 of 46	

+1.5VSUS 3,4,5,7,14,39,40,41,42
+3V 2,3,5,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+0.75V_DDR_VTT 7,40

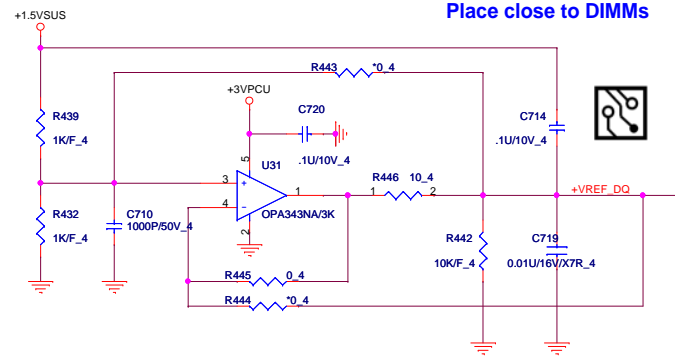
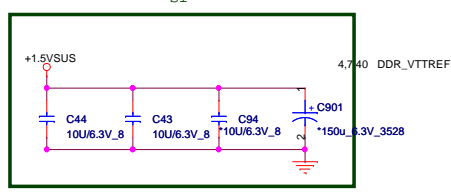
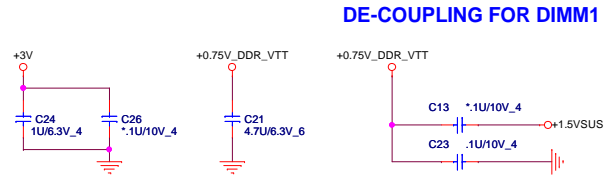
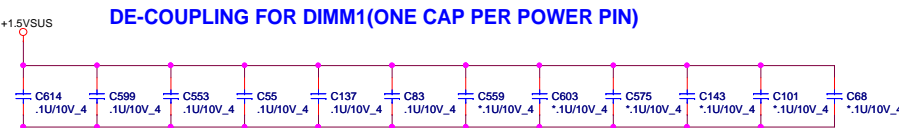


PC2100 DDR3 SDRAM SO-DIMM (204P)

PC2100 DDR3 SDRAM SO-DIMM (204P)

H=5.2 Footprint: "ddr-c-2013289-204p" DGMK4000059

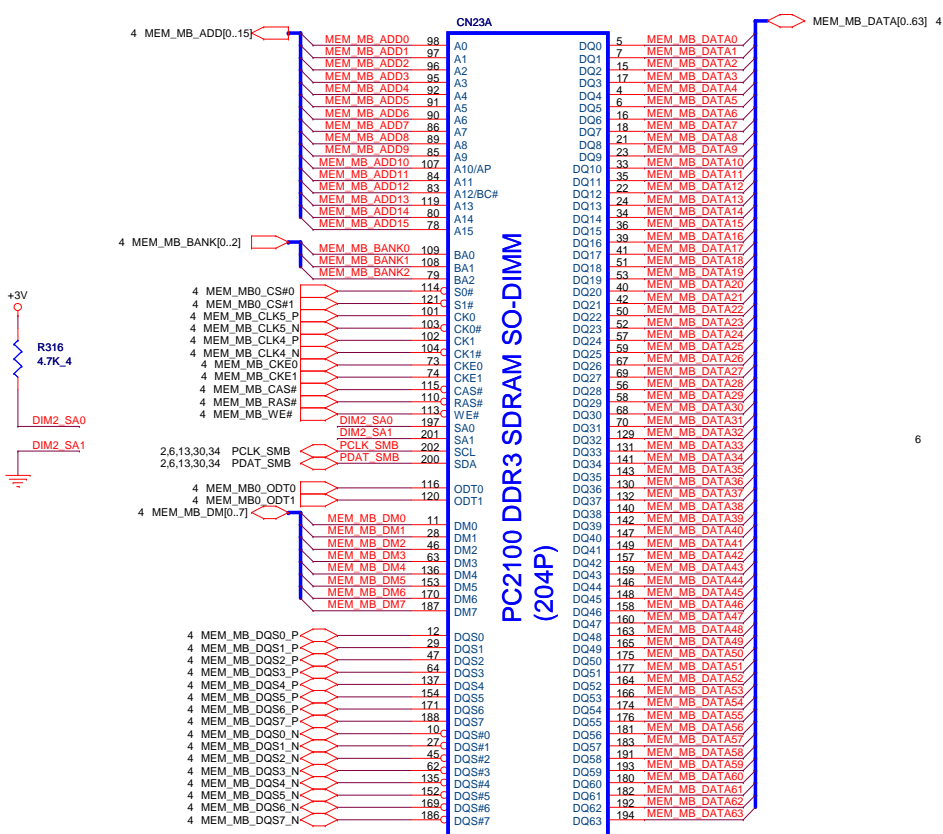
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.



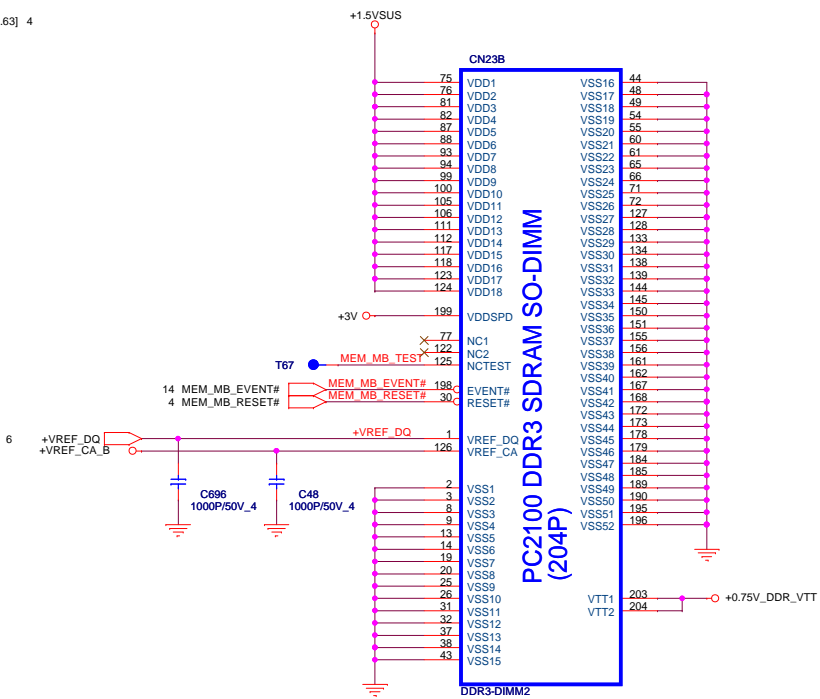
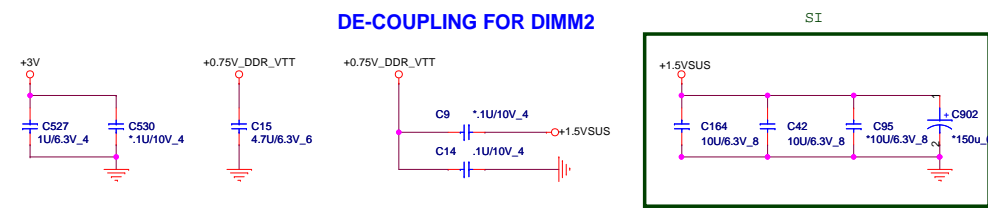
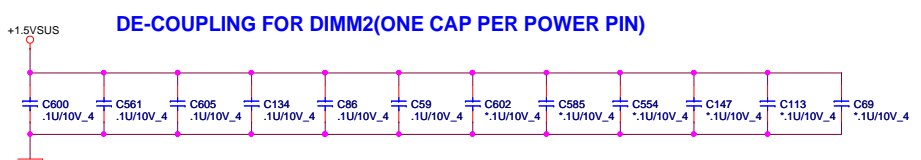
Place close to DIMMs

	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number	
Date: Monday, September 28, 2009		Sheet 6 of 46	

- +1.5VSUS 3,4,5,6,14,39,40,41,42
- +3V 2,3,5,6,10,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
- +0.75V_DDR_VTT 6,40



SO-DIMM BYPASS PLACEMENT :
 Place these Caps near So-Dimm1.
 No Vias Between the Trace of PIN to CAP.



H=9.2 footprint: "ddr-c-2013310-204p-1"
 DGMK4000058



PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
DDR3 SODIMMS TERMINATIONS		
Date: Monday, September 28, 2009	Sheet 7	of 46

+1.5V 3,11,34,42
+1.8V 5,10,11,16,26,42
+1.1V 2,3,9,10,11,15,38

- HT_CPU_NB_CAD_H[15..0] HT_CPU_NB_CAD_H[15..0] 3
- HT_CPU_NB_CAD_L[15..0] HT_CPU_NB_CAD_L[15..0] 3
- HT_CPU_NB_CLK_H[1..0] HT_CPU_NB_CLK_H[1..0] 3
- HT_CPU_NB_CLK_L[1..0] HT_CPU_NB_CLK_L[1..0] 3
- HT_CPU_NB_CTL_H[1..0] HT_CPU_NB_CTL_H[1..0] 3
- HT_CPU_NB_CTL_L[1..0] HT_CPU_NB_CTL_L[1..0] 3
- HT_NB_CPU_CAD_H[15..0] HT_NB_CPU_CAD_H[15..0] 3
- HT_NB_CPU_CAD_L[15..0] HT_NB_CPU_CAD_L[15..0] 3
- HT_NB_CPU_CLK_H[1..0] HT_NB_CPU_CLK_H[1..0] 3
- HT_NB_CPU_CLK_L[1..0] HT_NB_CPU_CLK_L[1..0] 3
- HT_NB_CPU_CTL_H[1..0] HT_NB_CPU_CTL_H[1..0] 3
- HT_NB_CPU_CTL_L[1..0] HT_NB_CPU_CTL_L[1..0] 3

- HT_CPU_NB_CAD_H0 Y25
- HT_CPU_NB_CAD_L0 Y24
- HT_CPU_NB_CAD_H1 V22
- HT_CPU_NB_CAD_L1 V23
- HT_CPU_NB_CAD_H2 V26
- HT_CPU_NB_CAD_L2 V24
- HT_CPU_NB_CAD_H3 U24
- HT_CPU_NB_CAD_L3 U25
- HT_CPU_NB_CAD_H4 T25
- HT_CPU_NB_CAD_L4 T24
- HT_CPU_NB_CAD_H5 P22
- HT_CPU_NB_CAD_L5 P23
- HT_CPU_NB_CAD_H6 P25
- HT_CPU_NB_CAD_L6 P24
- HT_CPU_NB_CAD_H7 N24
- HT_CPU_NB_CAD_L7 N25
- HT_CPU_NB_CAD_H8 AC24
- HT_CPU_NB_CAD_L8 AC25
- HT_CPU_NB_CAD_H9 AB25
- HT_CPU_NB_CAD_L9 AB24
- HT_CPU_NB_CAD_H10 AA24
- HT_CPU_NB_CAD_L10 AA25
- HT_CPU_NB_CAD_H11 Y22
- HT_CPU_NB_CAD_L11 Y23
- HT_CPU_NB_CAD_H12 W21
- HT_CPU_NB_CAD_L12 W20
- HT_CPU_NB_CAD_H13 V21
- HT_CPU_NB_CAD_L13 V20
- HT_CPU_NB_CAD_H14 U20
- HT_CPU_NB_CAD_L14 U21
- HT_CPU_NB_CAD_H15 U19
- HT_CPU_NB_CAD_L15 U18
- HT_CPU_NB_CLK_H0 T22
- HT_CPU_NB_CLK_L0 T23
- HT_CPU_NB_CLK_H1 AB23
- HT_CPU_NB_CLK_L1 AA22
- HT_CPU_NB_CTL_H0 M22
- HT_CPU_NB_CTL_L0 M23
- HT_CPU_NB_CTL_H1 R21
- HT_CPU_NB_CTL_L1 R20

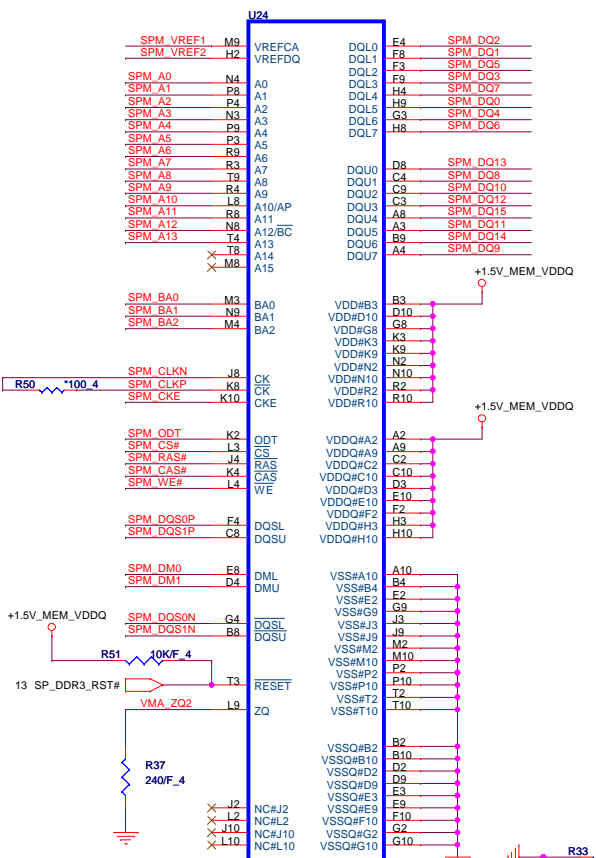
- HT_RXCAD0P
- HT_RXCAD0N
- HT_RXCAD1P
- HT_RXCAD1N
- HT_RXCAD2P
- HT_RXCAD2N
- HT_RXCAD3P
- HT_RXCAD3N
- HT_RXCAD4P
- HT_RXCAD4N
- HT_RXCAD5P
- HT_RXCAD5N
- HT_RXCAD6P
- HT_RXCAD6N
- HT_RXCAD7P
- HT_RXCAD7N
- HT_RXCAD8P
- HT_RXCAD8N
- HT_RXCAD9P
- HT_RXCAD9N
- HT_RXCAD10P
- HT_RXCAD10N
- HT_RXCAD11P
- HT_RXCAD11N
- HT_RXCAD12P
- HT_RXCAD12N
- HT_RXCAD13P
- HT_RXCAD13N
- HT_RXCAD14P
- HT_RXCAD14N
- HT_RXCAD15P
- HT_RXCAD15N

PART 1 OF 6

HYPER TRANSPORT CPU I/F

- HT_NB_CPU_CAD_H0 D24
- HT_NB_CPU_CAD_L0 D25
- HT_NB_CPU_CAD_H1 E24
- HT_NB_CPU_CAD_L1 E25
- HT_NB_CPU_CAD_H2 F24
- HT_NB_CPU_CAD_L2 F25
- HT_NB_CPU_CAD_H3 F23
- HT_NB_CPU_CAD_L3 F22
- HT_NB_CPU_CAD_H4 H23
- HT_NB_CPU_CAD_L4 H22
- HT_NB_CPU_CAD_H5 J25
- HT_NB_CPU_CAD_L5 J24
- HT_NB_CPU_CAD_H6 K24
- HT_NB_CPU_CAD_L6 K23
- HT_NB_CPU_CAD_H7 K22
- HT_NB_CPU_CAD_L7 K22
- HT_NB_CPU_CAD_H8 G21
- HT_NB_CPU_CAD_L8 G20
- HT_NB_CPU_CAD_H9 H21
- HT_NB_CPU_CAD_L9 H20
- HT_NB_CPU_CAD_H10 J20
- HT_NB_CPU_CAD_L10 J18
- HT_NB_CPU_CAD_H11 K17
- HT_NB_CPU_CAD_L11 L19
- HT_NB_CPU_CAD_H12 J19
- HT_NB_CPU_CAD_L12 M19
- HT_NB_CPU_CAD_H13 L18
- HT_NB_CPU_CAD_L13 M21
- HT_NB_CPU_CAD_H14 P21
- HT_NB_CPU_CAD_L14 P18
- HT_NB_CPU_CAD_H15 M18
- HT_NB_CPU_CAD_L15 M18
- HT_NB_CPU_CLK_H0 H24
- HT_NB_CPU_CLK_L0 H25
- HT_NB_CPU_CLK_H1 L21
- HT_NB_CPU_CLK_L1 L20
- HT_NB_CPU_CTL_H0 M24
- HT_NB_CPU_CTL_L0 M25
- HT_NB_CPU_CTL_H1 P19
- HT_NB_CPU_CTL_L1 R18
- HT_RXCALP R418
- HT_RXCALN B25

signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

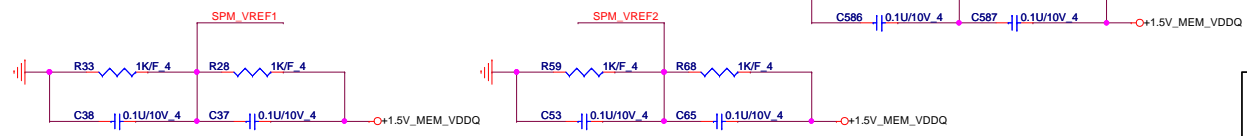
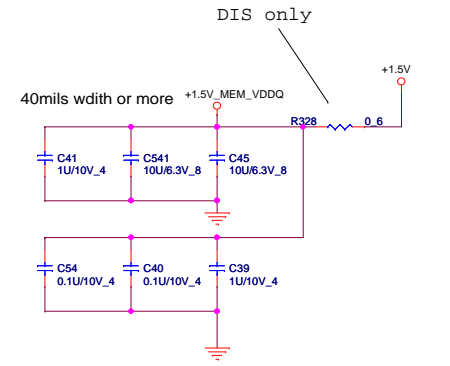


This block is for UMA only , DIS can remove all component

- SPM_A0 M9, AB12, SPM_A1 N4, AB16, SPM_A2 P8, V11, SPM_A3 N3, AE15, SPM_A4 P9, AA12, SPM_A5 R9, AB14, SPM_A6 R3, AD14, SPM_A7 R3, AD13, SPM_A8 T9, AD15, SPM_A9 R4, AC16, SPM_A10 L8, AE13, SPM_A11 R8, AC14, SPM_A12 N8, Y14, SPM_A13 T4, Y14
- SPM_BA0 AD16, MEM_BA0(NC), SPM_BA1 N9, AE17, MEM_BA1(NC), SPM_BA2 M4, AD17, MEM_BA2(NC)
- SPM_RAS# W12, MEM_RAS(NC), SPM_CAS# J4, Y12, MEM_CAS(NC), SPM_WE# AD18, MEM_WE(NC), SPM_CKE K10, AB13, MEM_CKE(NC), SPM_ODT T4, V14, MEM_ODT(NC)
- SPM_CLKP V15, MEM_CLKP(NC), SPM_CLKN W14, MEM_CLKN(NC)
- R371 40.2F_4, SPM_COMP P, R368 40.2F_4, SPM_COMP N
- RS880M

PAR 4 OF 6

- MEM_D00(DVO_VSYNC(NC)) AA18, SPM_DQ0
- MEM_D01(DVO_HSYNC(NC)) AA20, SPM_DQ1
- MEM_D02(DVO_DE(NC)) AA19, SPM_DQ2
- MEM_D03(DVO_D0(NC)) Y19, SPM_DQ3
- MEM_D04(NC) V17, SPM_DQ4
- MEM_D05(DVO_D1(NC)) AA17, SPM_DQ5
- MEM_D06(DVO_D2(NC)) Y15, SPM_DQ7
- MEM_D07(DVO_D4(NC)) AC20, SPM_DQ9
- MEM_D08(DVO_D3(NC)) AD19, SPM_DQ8
- MEM_D09(DVO_D5(NC)) AE22, SPM_DQ10
- MEM_D010(DVO_D6(NC)) AC18, SPM_DQ11
- MEM_D011(DVO_D7(NC)) AB20, SPM_DQ12
- MEM_D012(NC) AD22, SPM_DQ13
- MEM_D013(DVO_D9(NC)) AC22, SPM_DQ14
- MEM_D014(DVO_D10(NC)) AD21, SPM_DQ15
- MEM_D015(DVO_D11(NC)) Y17, SPM_DQS0P
- MEM_DQS0P(DVO_IDCKN(NC)) W18, SPM_DQS0N
- MEM_DQS1P(NC) AD20, SPM_DQS1P
- MEM_DQS1N(NC) AE21, SPM_DQS1N
- MEM_DM0(NC) W17, SPM_DM0
- MEM_DM1(DVO_D8(NC)) AE19, SPM_DM1
- AE23 +1.8V IOPLLVD18, BLM18PG181SN1D(180.15A) 6, L61 +0.1.8V
- AE24 +1.1V IOPLLVD18, BLM18PG181SN1D(180.15A) 6, L56 +0.1.1V
- AD23, AD20, AE18 SPM_VREF, C573, C558, 2.2U/6.3V_6, 2.2U/6.3V_6
- C586 0.1U/10V_4, C587 0.1U/10V_4



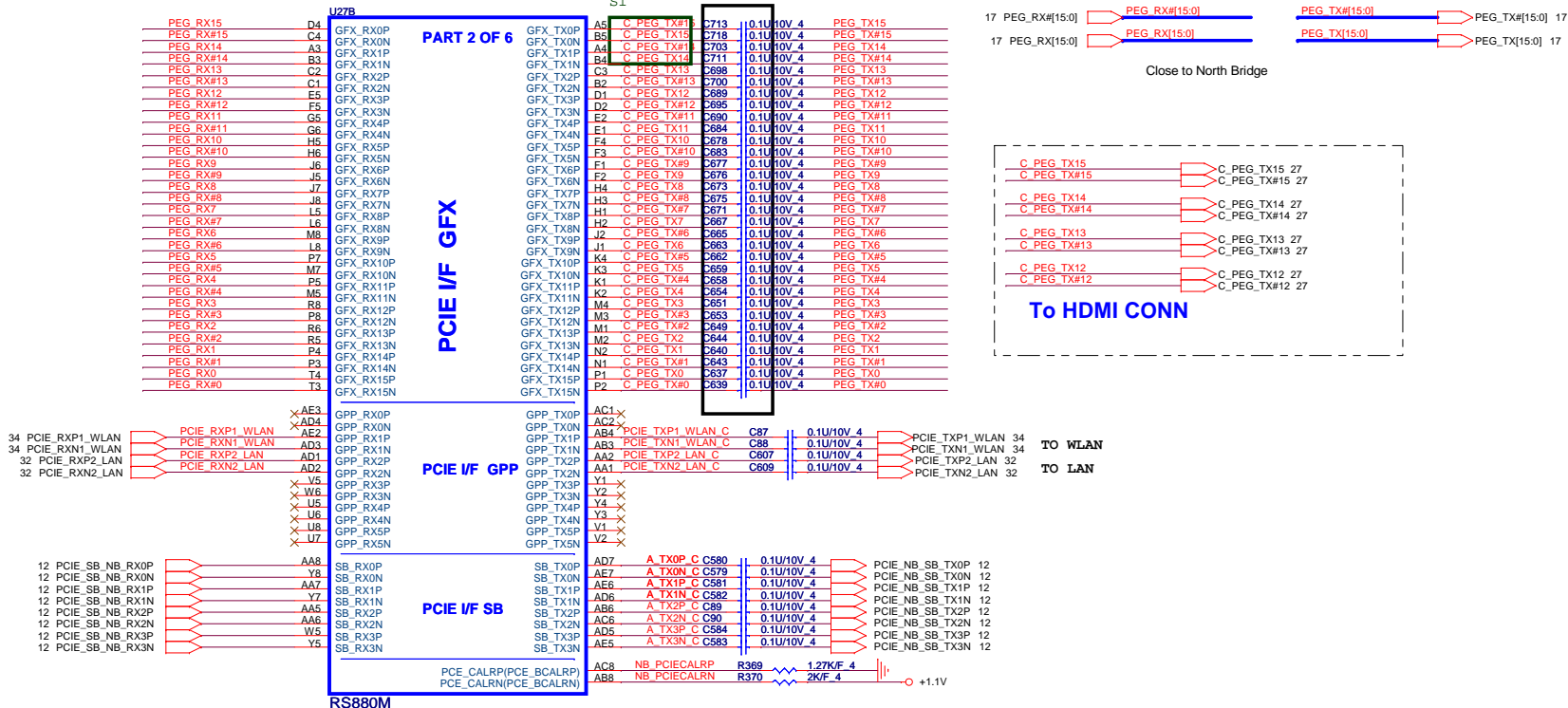
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number RS880-HT LINK I/F 1/5	Rev 1A
Date: Monday, September 28, 2009 Sheet 8 of 46		

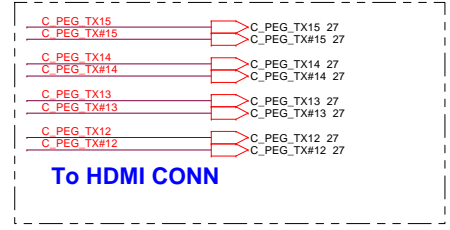
NBS/RD2

UMA Remove All Cap

Swap pin for Layout



Close to North Bridge



RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

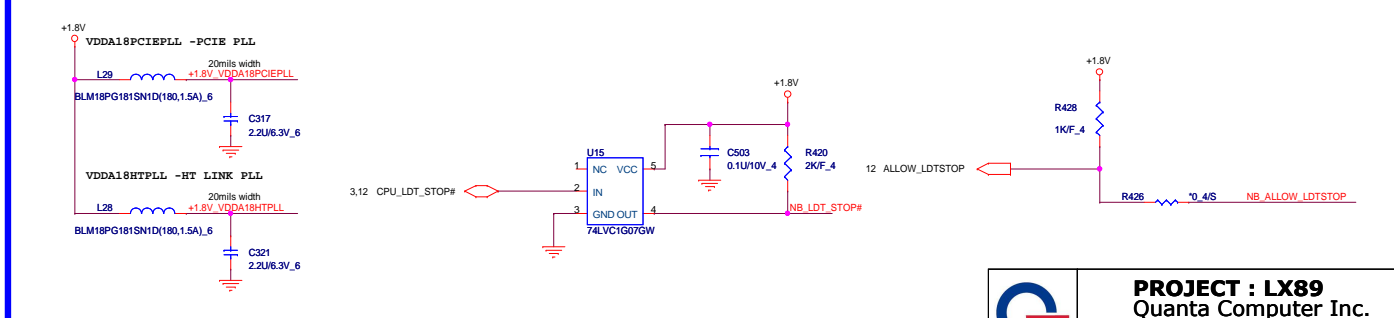
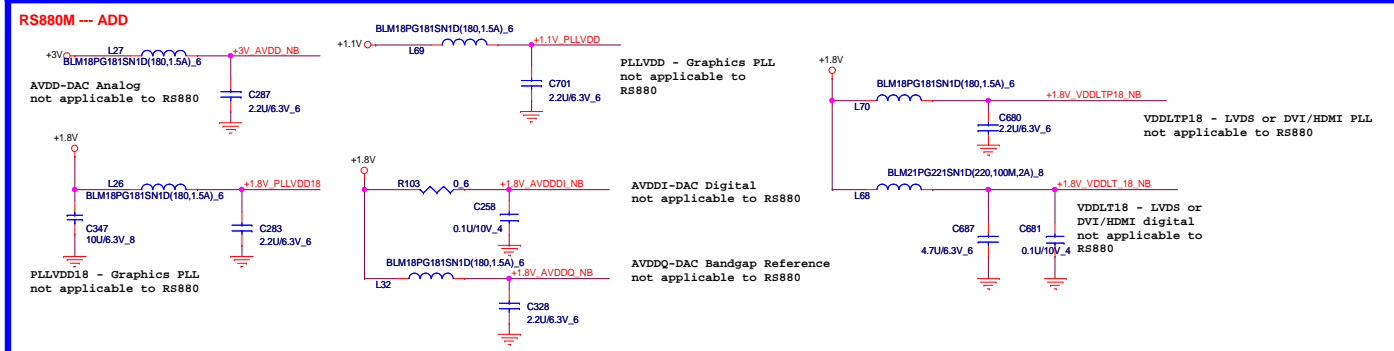
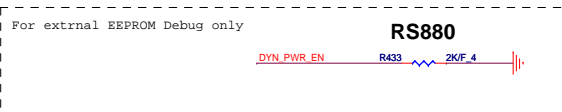
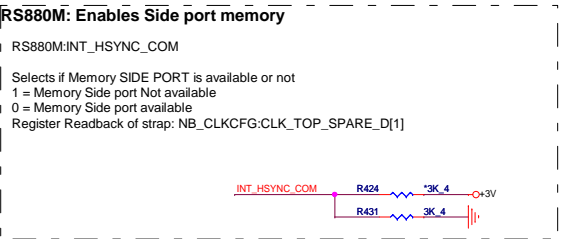
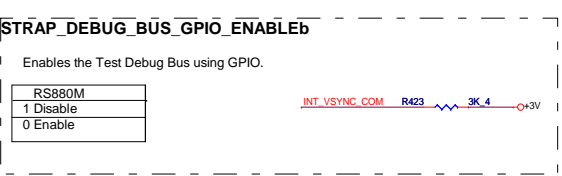
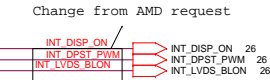
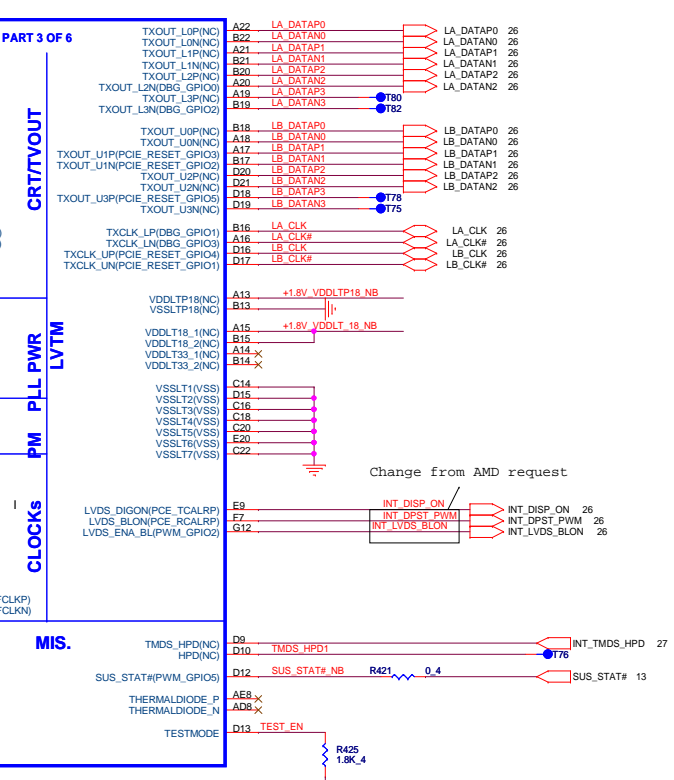
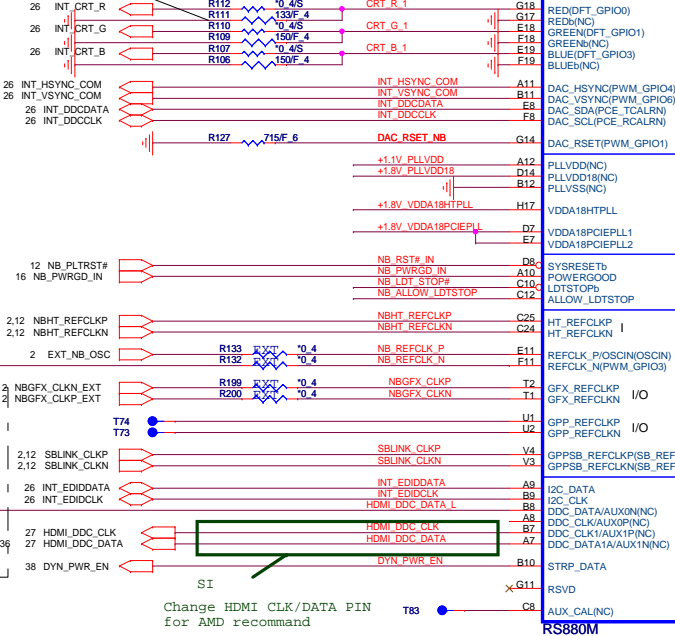
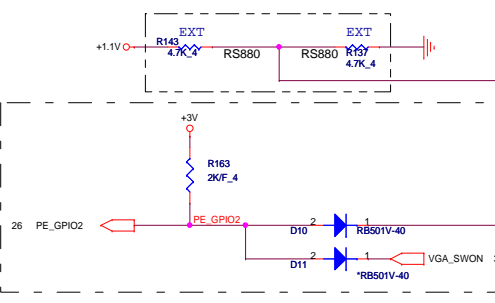
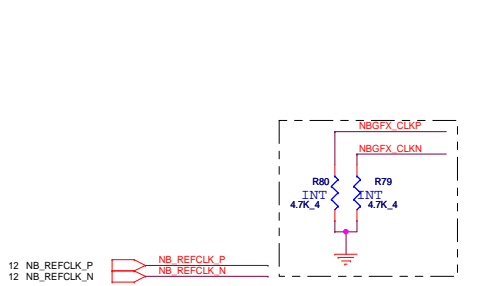


<p>NB5/RD2</p>	<p>PROJECT : LX89 Quanta Computer Inc.</p>		Rev 1A
	Size Custom	Document Number RS880-PCIE I/F 2/5	
	Date: Monday, September 28, 2009	Sheet 9 of 46	

+3V	2,3,5,6,7,11,12,13,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+1.8V	5,8,11,16,26,42
+1.1V	2,3,8,9,11,15,38
+1.5V	3,8,11,34,42

R111 for UMA use 140 ohm
for DIS+PowerExpress use 133 ohm (AMD)

133ohm CS11332FB19
140ohm CS11402FB19



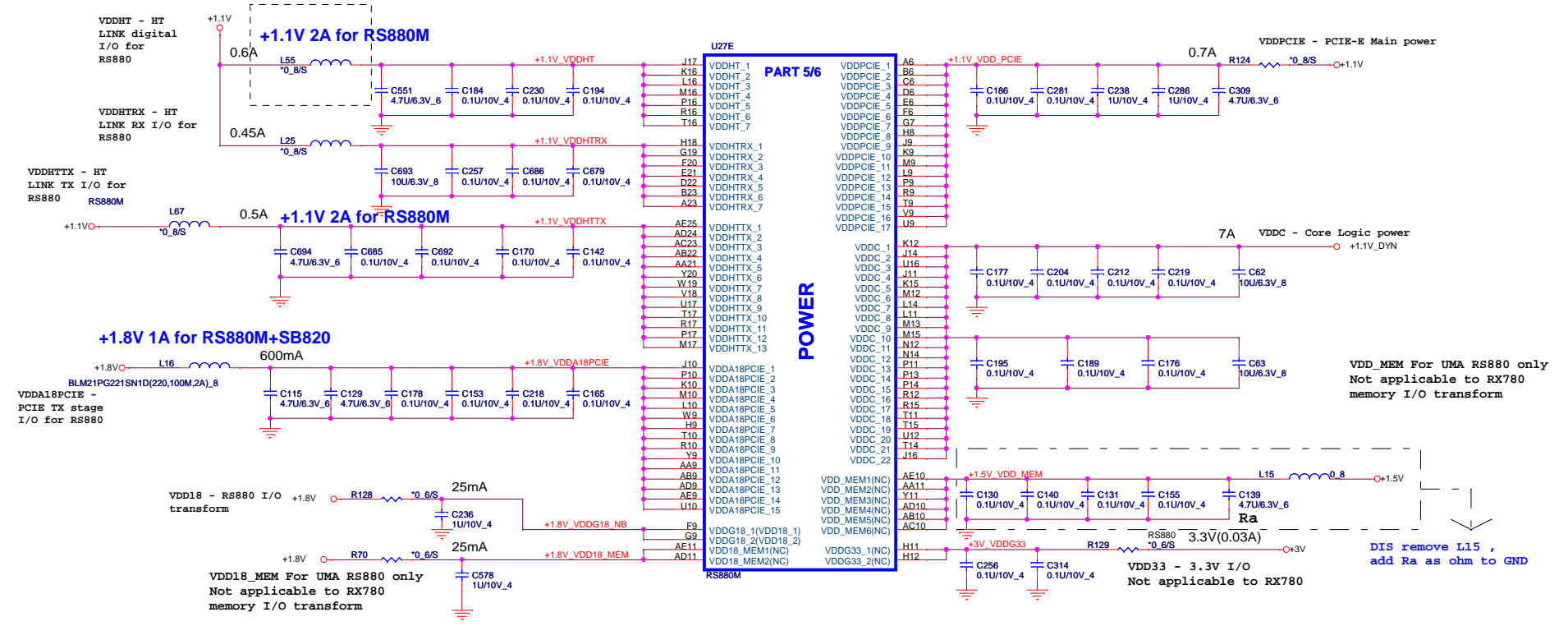
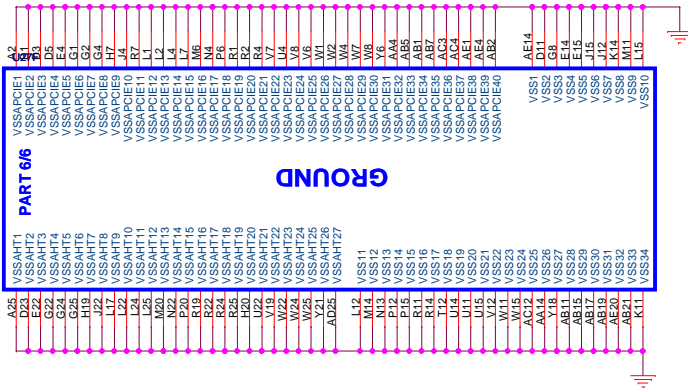
PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number
RS880-SYSTEM I/F 3/5

NBS/RDZ Date: Monday, September 28, 2009 Sheet 10 of 46

RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC



PART 5/6 POWER

VDD_MEM For UMA RS880 only Not applicable to RX780 memory I/O transform

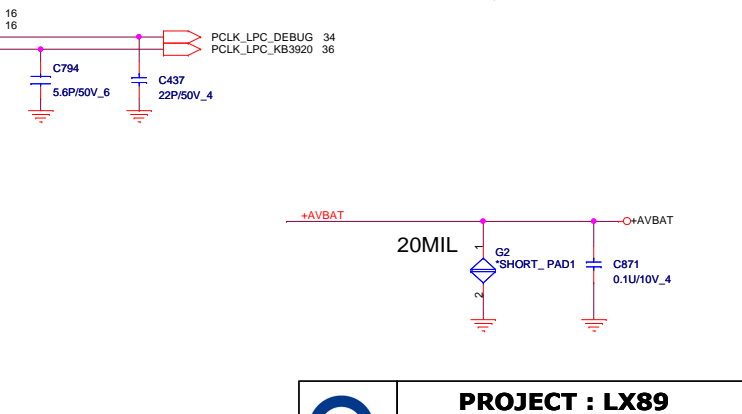
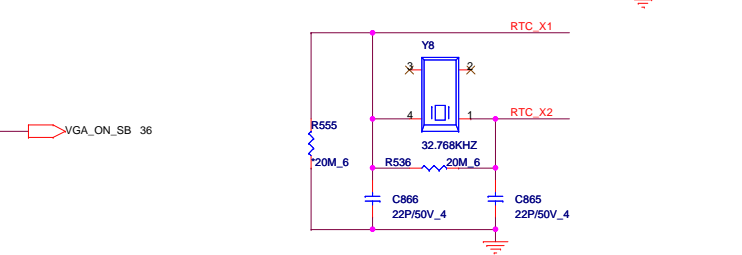
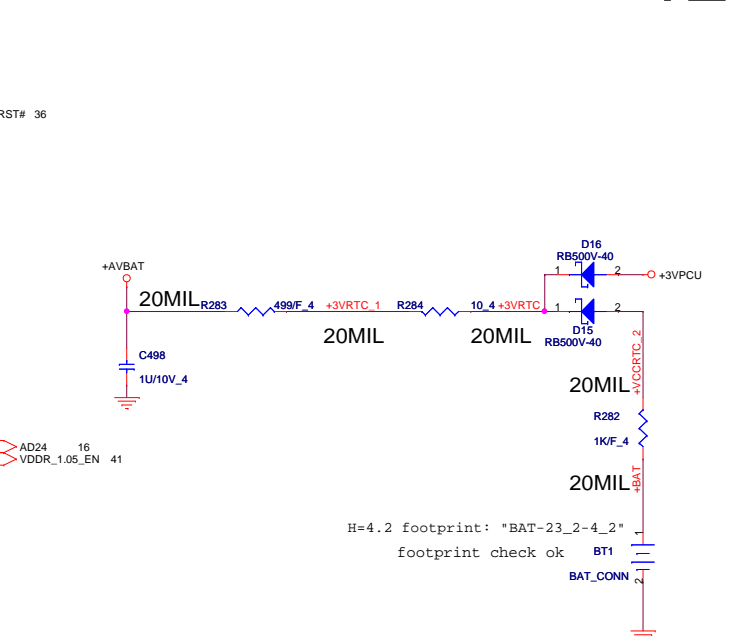
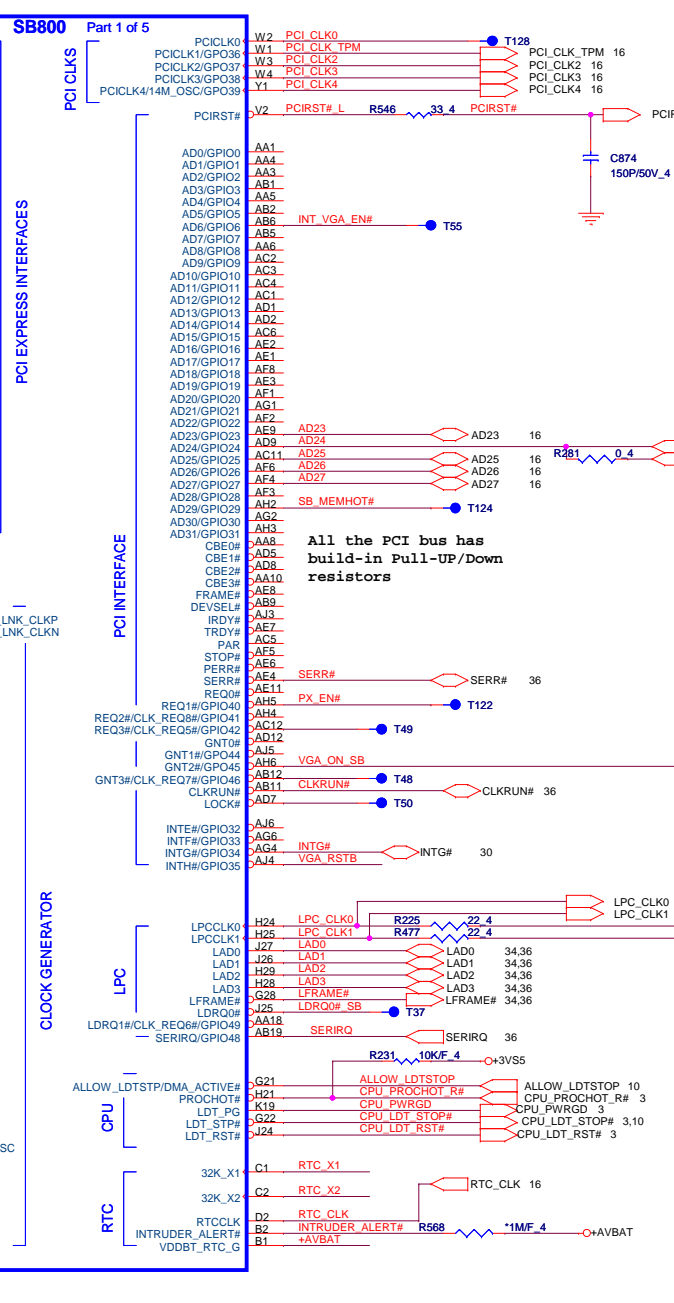
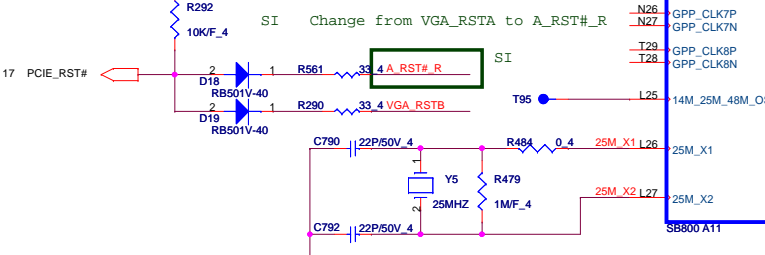
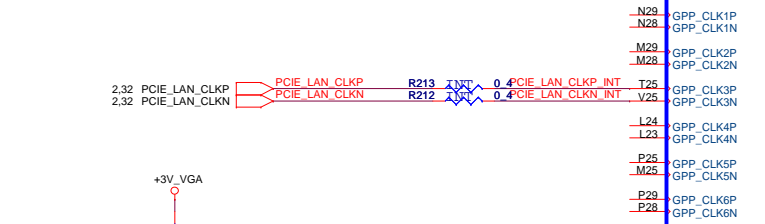
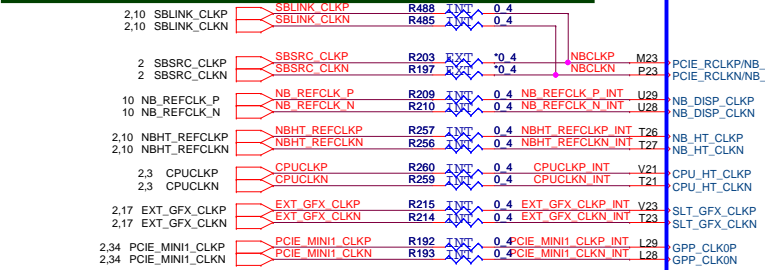
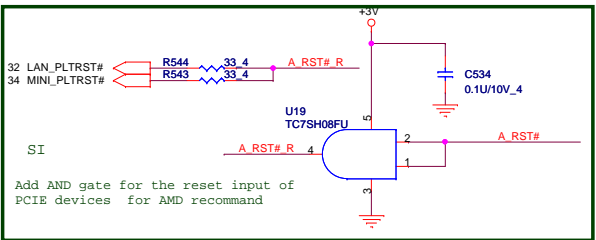
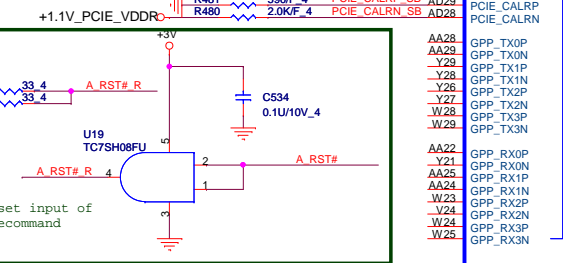
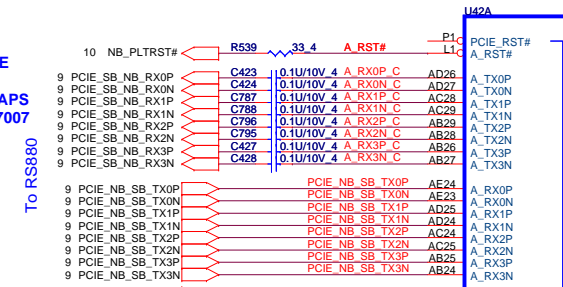
DIS remove L15, add Ra as ohm to GND

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number RS880-POWER5/5	Rev 1A
Date: Monday, September 28, 2009		Sheet 11 of 46

+1.1V_PCIE_VDDR 15
+3V_VGA 21,41
+3VS5 5,13,14,15,16,42
+3VPCU 4,6,24,33,35,36,37,38,39,40,41,42,43

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U7007

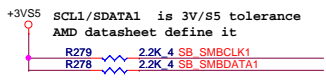
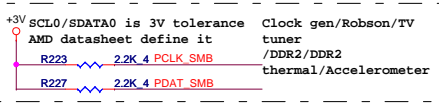
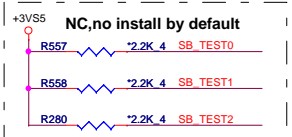


INTRUDER_ALERT# Left not connected (southbridge has 50-kohm internal pull-up to VBAT).

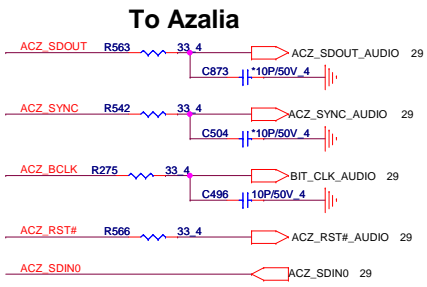
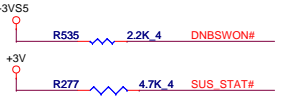
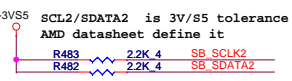
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SB820-PCIE/PCICPU/LPC 1/4	Rev 1A
Date: Monday, September 28, 2009	Sheet 12 of 46	

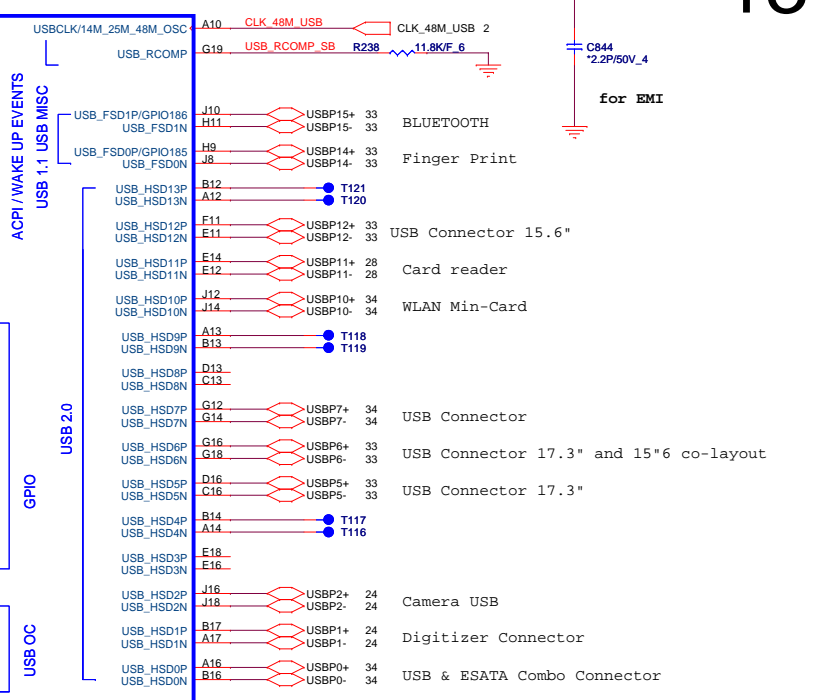
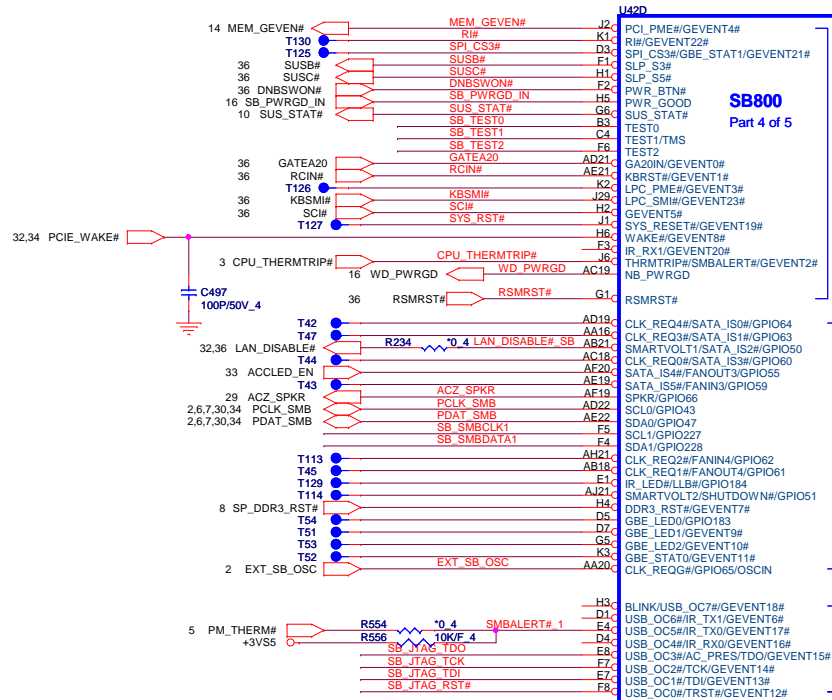
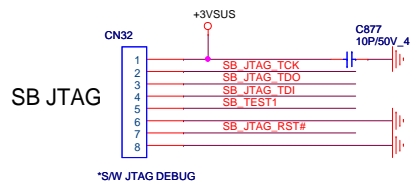
NBS/RD2



remove pull hi
 (chip internal
 have pull hi)



- +3VSUS 28,33,34,35,41,42
- +3V 2,3,5,6,7,10,11,12,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
- +3VS5 5,12,14,15,16,42



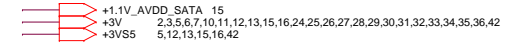
SB800 A11

			PROJECT : LX89 Quanta Computer Inc.	
Size Custom	Document Number	SB820-ACPI/USB 2/J4		Rev 1A
Date: Monday, September 28, 2009	Sheet 13	of 46		

SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

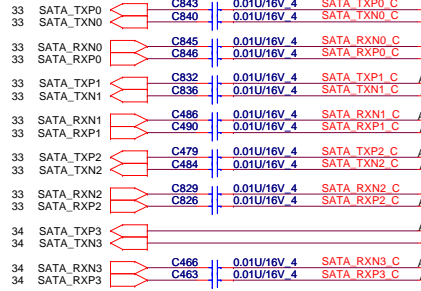


SATA1 HDD

SATA ODD

SATA2 HDD

E-SATA



XTLVDD_SATA-- SATA
crystal power

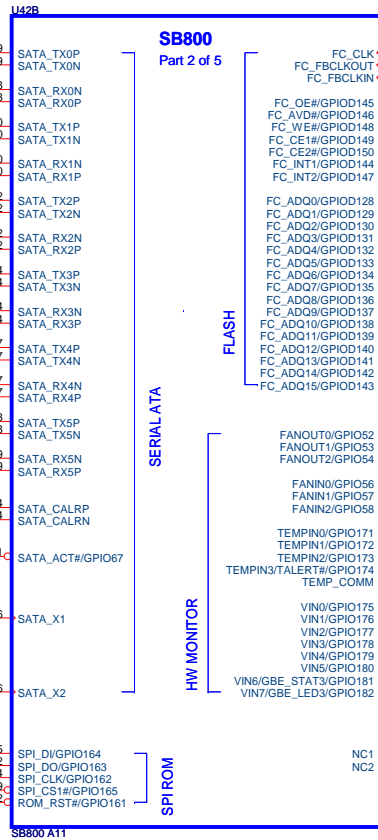
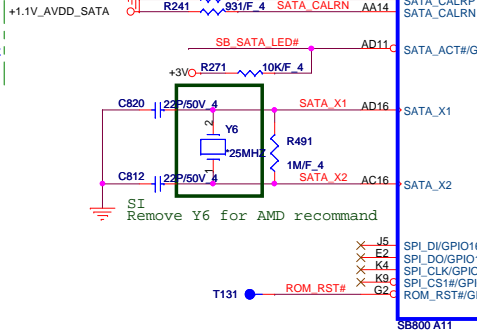
PLVDD_SATA--
SATA PLL
POWER



PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

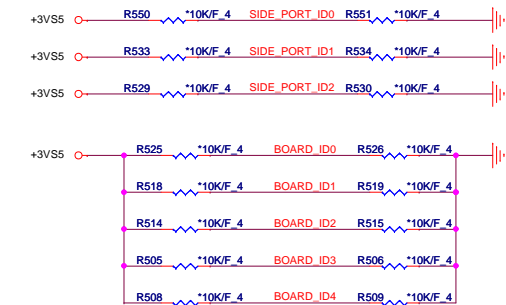
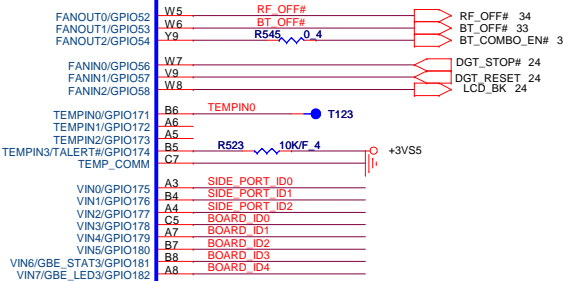
NOTE:

R361 IS 1K 1% FOR 25MHz
XTAL. 4.99K 1% FOR 100MHz
INTERNAL CLOCK

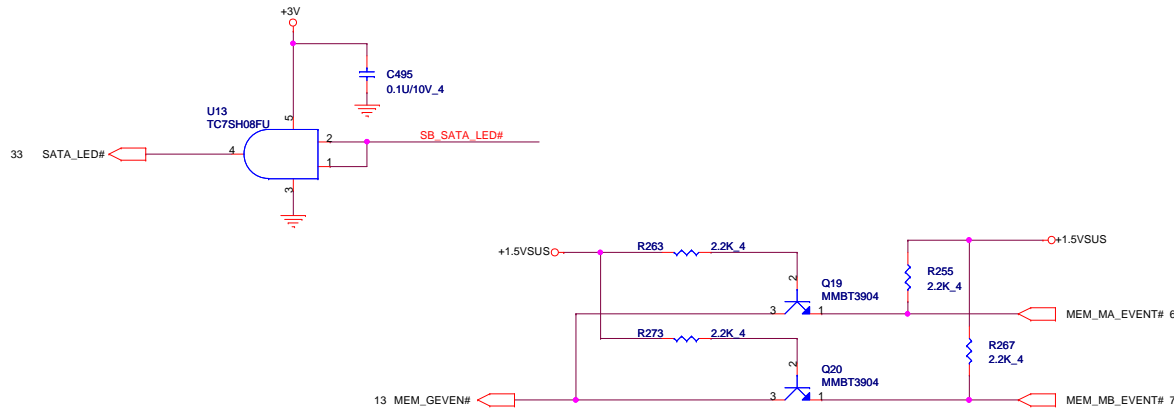


IF USE, power need ready

SIDE_PORT_ID2	SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	0	Samsung
0	0	1	Hynix
0	1	0	NC
0	1	1	no supprot side port



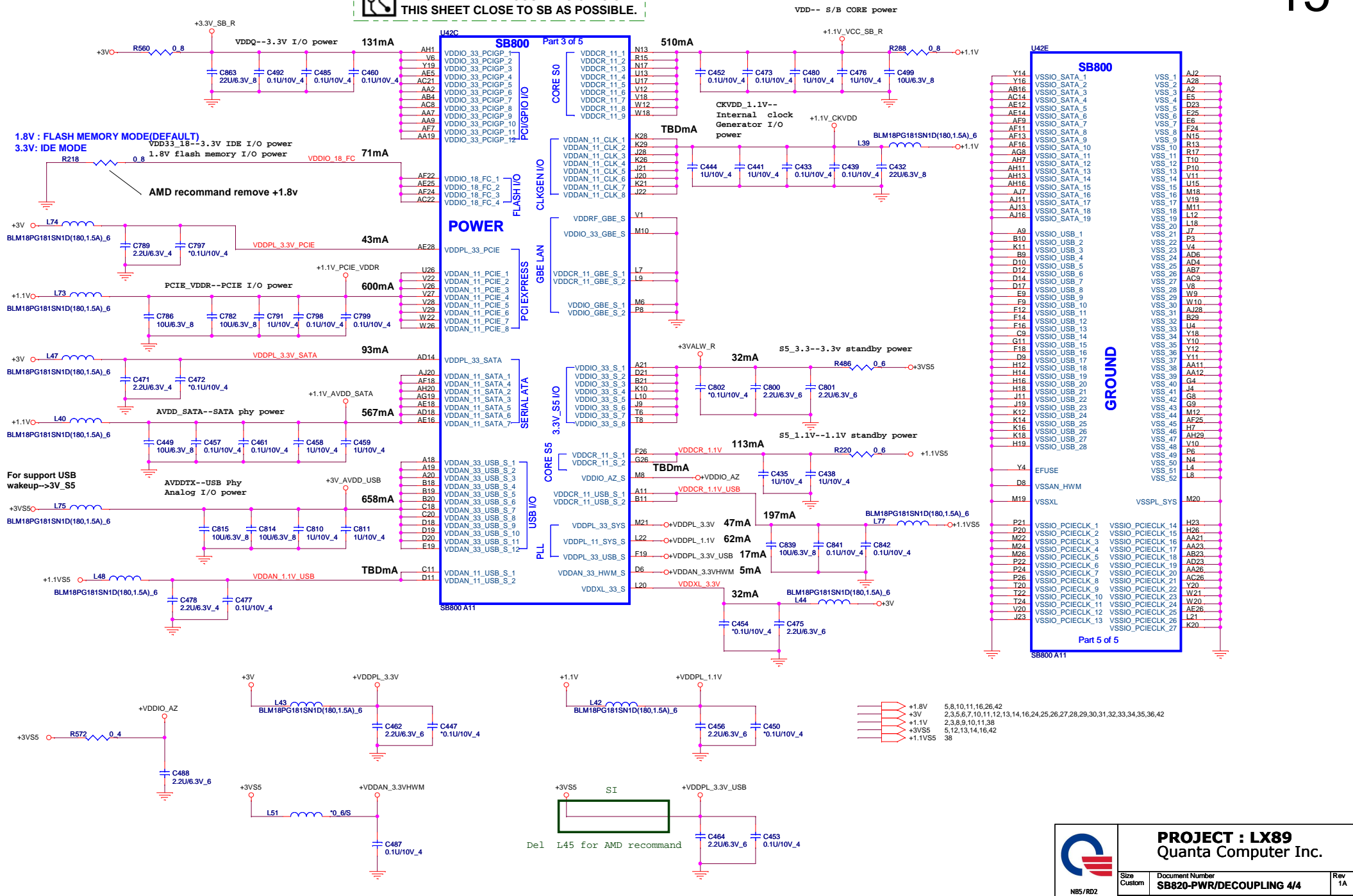
ID4	ID3	ID2	ID1	ID0	
0	0	0	0	0	LX8 UMA
0	0	0	0	1	LX9 UMA
0	0	0	1	0	LX8 Madison
0	0	0	1	1	LX8 Park
0	0	1	0	0	LX9 Park
0	0	1	0	1	
0	0	1	1	0	
0	0	1	1	1	



PROJECT : LX89
Quanta Computer Inc.

Size Custom Document Number SB820-ACPI/GPIO/USB 2J4 Rev 1A
Date: Monday, September 28, 2009 Sheet 14 of 46

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number SB820-PWR/DECOUPLING 4/4	Rev 1A
Date: Monday, September 28, 2009 Sheet 15 of 46		

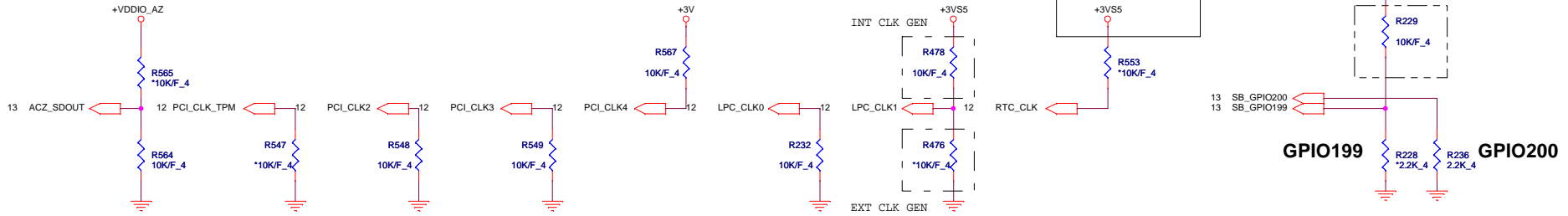
NBS/RDZ

+1.8V	5,8,10,11,16,26,42
+3V	2,3,5,6,7,10,11,12,13,14,16,24,25,26,27,28,29,30,31,32,33,34,35,36,42
+1.1V	2,3,8,9,10,11,38
+3VSS	5,12,13,14,16,42
+1.1VSS	38

Del L45 for AMD recommand

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



It must ready before RSMRST#

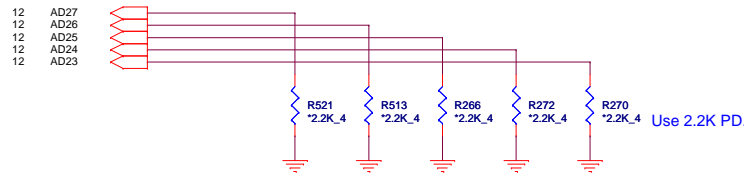
REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

TYPE	GPIO199	GPIO200
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

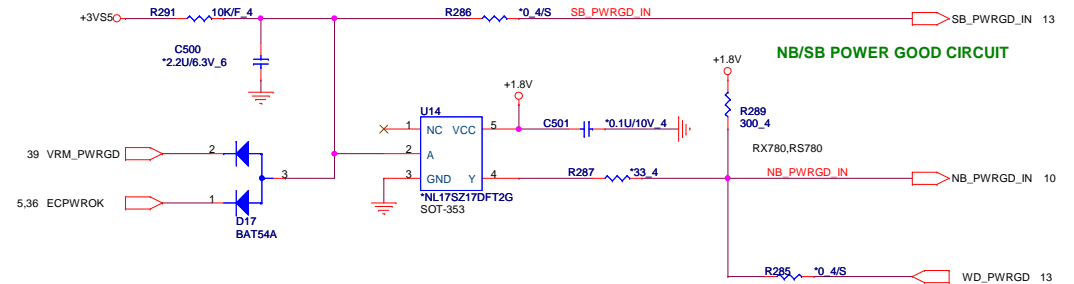
DEBUG STRAPS

SB820 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



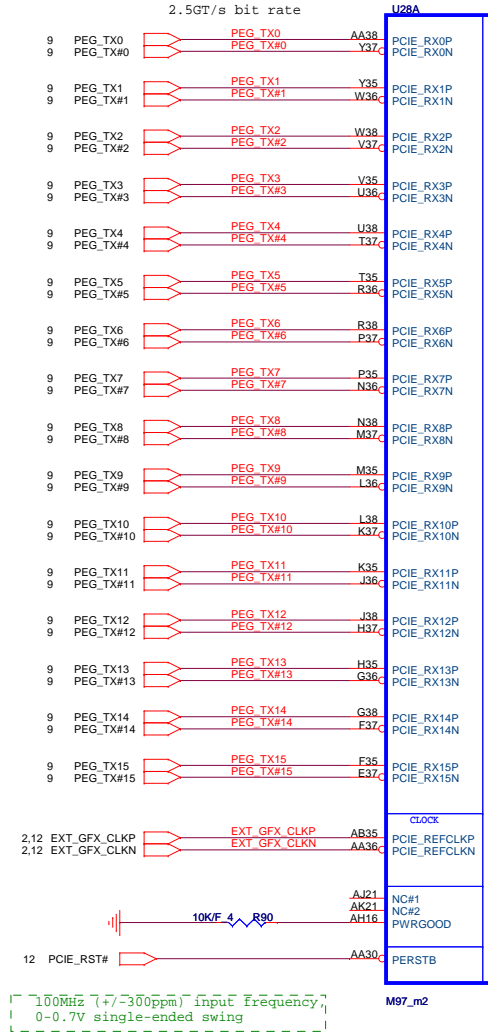
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)

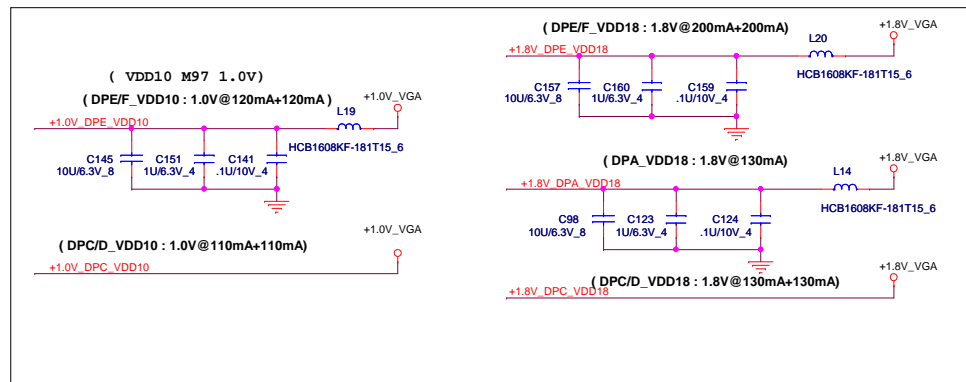
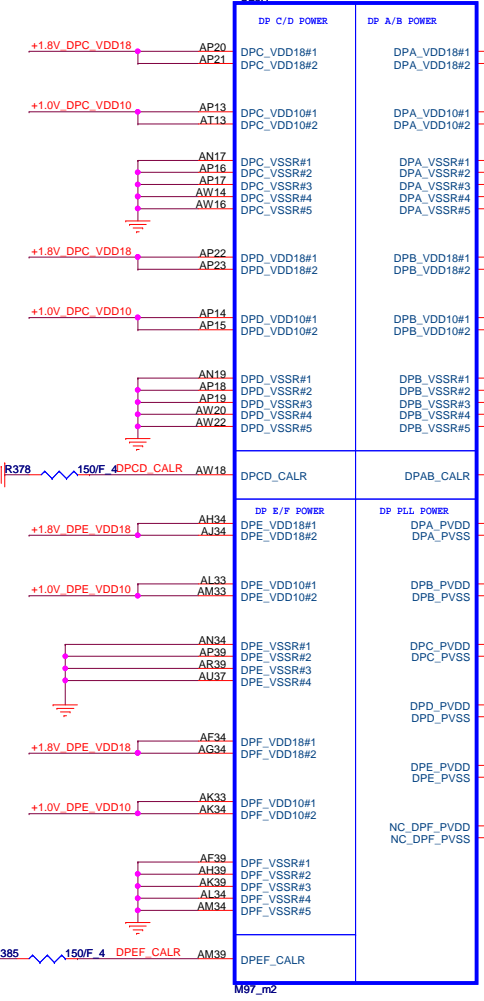
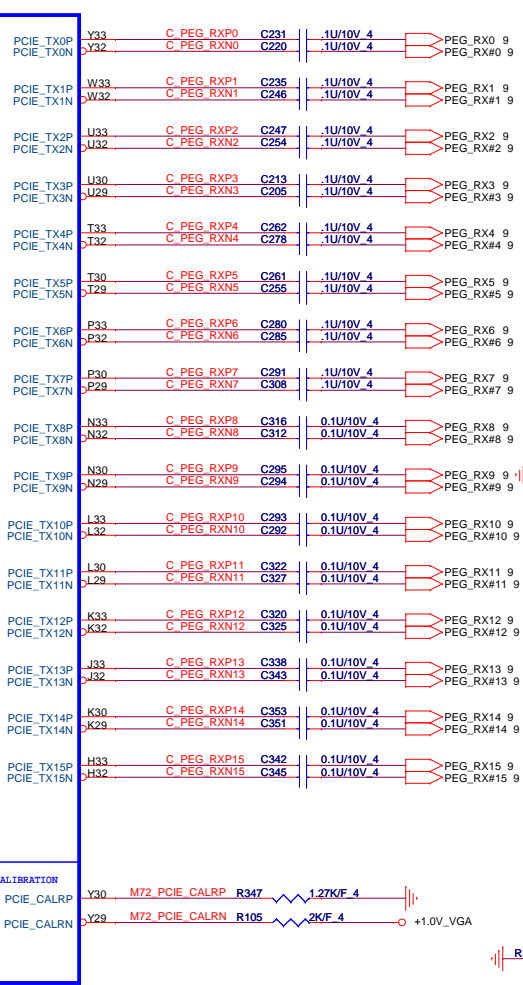


AL17S217000 IC(5P) NL17S217DFT2G(SOT-353) SOT-353
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

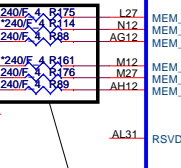
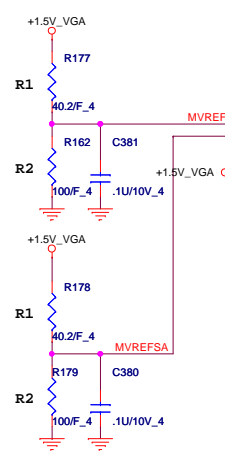
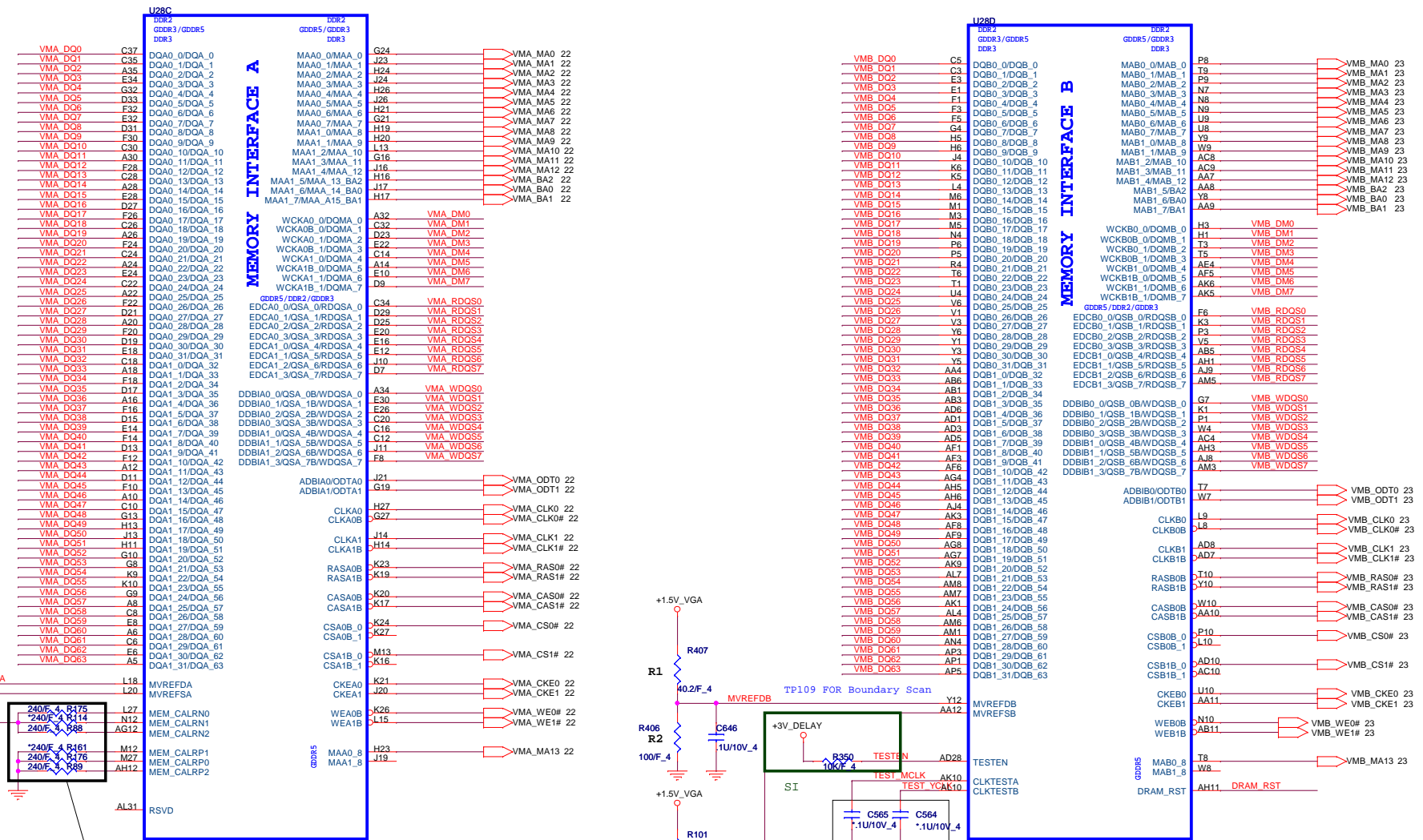
	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number SB820-STRAPS	
NB5/RD2	Date: Monday, September 28, 2009	Sheet 16 of 46	



PCI EXPRESS INTERFACE



	PROJECT : LX89		Rev
	Quanta Computer Inc.		1A
Size Custom	Document Number	ATI Park/Madison (PCIe I/F) 1/5	
NB5/RDZ	Date: Monday, September 28, 2009	Sheet	17 of 46

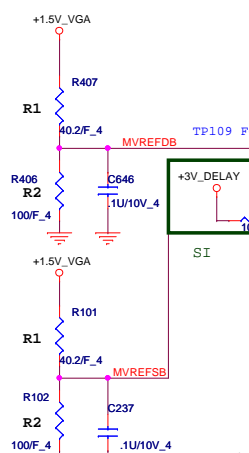


	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

DDR3/GDDR3 Memory Stuff Option

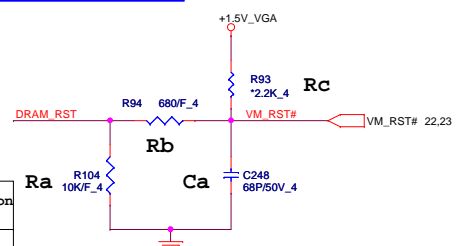
	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
R1	40.2R	40.2R	40.2R
R2	100R	100R	100R

- 22 VMA_DQ[63..0]
- 22 VMA_DM[7..0]
- 22 VMA_WDQS[7..0]
- 22 VMA_RDQS[7..0]
- 23 VMB_DQ[63..0]
- 23 VMB_DM[7..0]
- 23 VMB_WDQS[7..0]
- 23 VMB_RDQS[7..0]
- 21,22,23,40 +1.5V_VGA

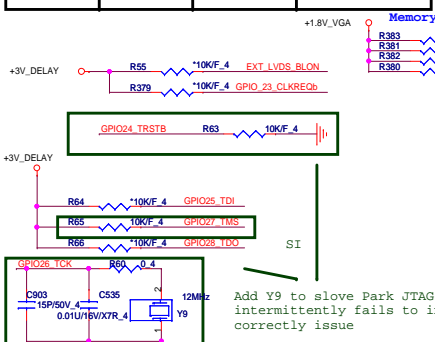


route 50ohms single-ended/100ohms diff and keep short Debug only, for clock observation, if not needed, DNI

Designator	For M97-M2	For Manhattan
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF



MEM_ID[3:0], Vendor, Type, Vendor P/N table listing Samsung and Hynix memory modules.



NC on PARK

NC on PARK

NC on PARK

Generic/G is NC on PARK

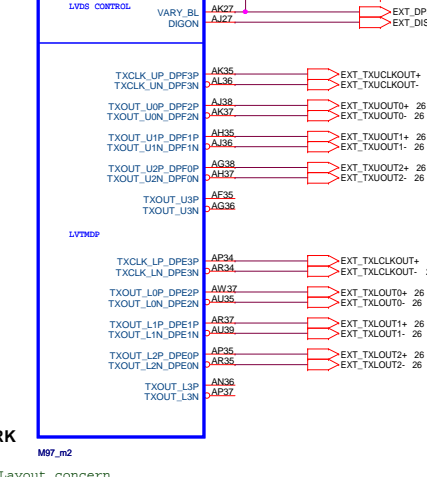
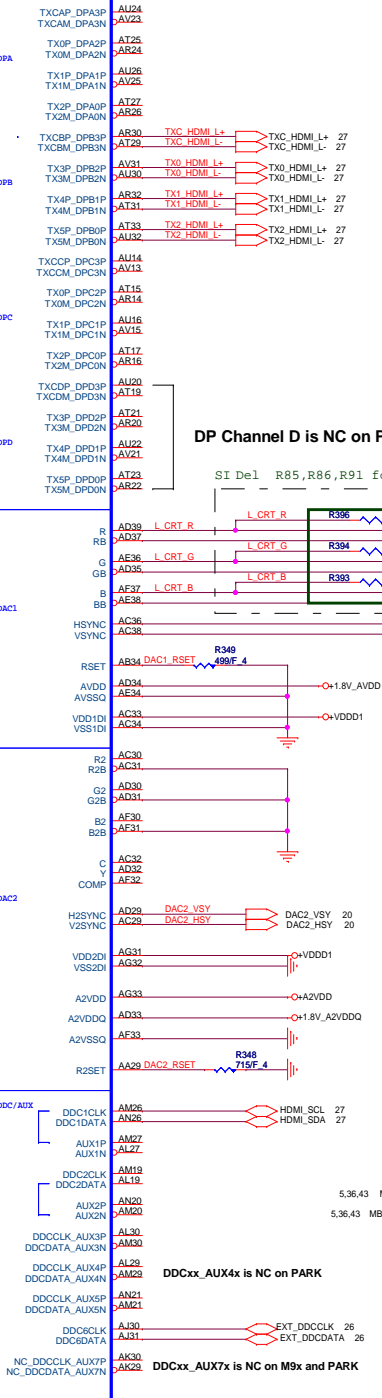
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Remove GND

Remove GND

Remove GND

- U288 MT71 GFX, U286 LVDS CONTROL, U286 LVTSNDP, U286 DIS, U286 SI Del R85, R86, R91 for Layout concern

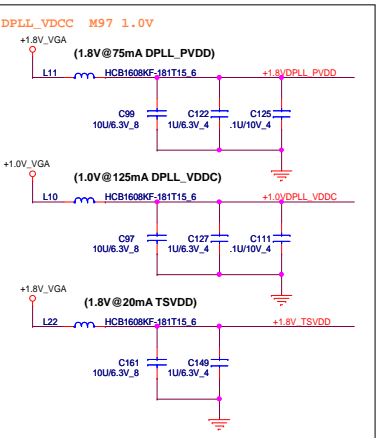
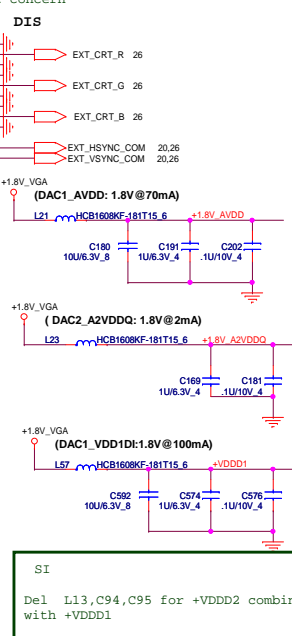


DisplayPort F Configuration

DisplayPort E Configuration For Single-link panel

DP Channel D is NC on PARK

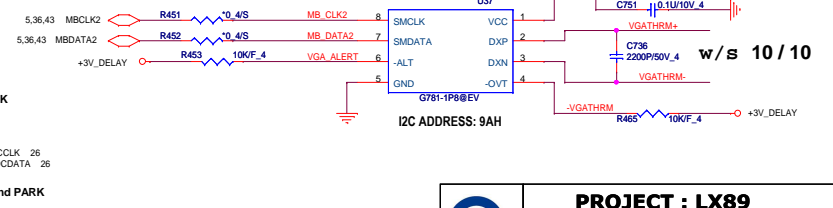
SI Del R85, R86, R91 for Layout concern



Del L9 A2VDD can be powered by VDDR3 directly without filter

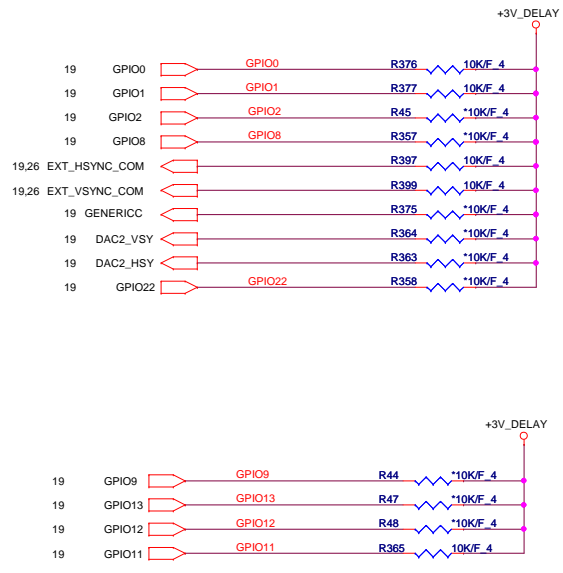
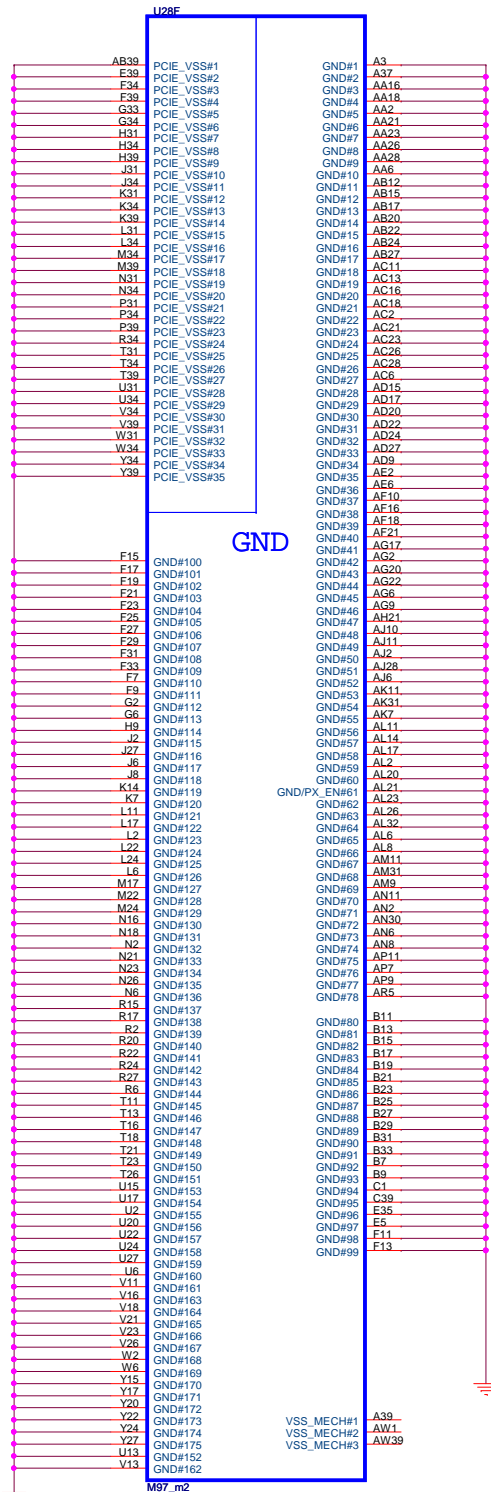
Del L13, C94, C95 for +VDDDD2 combine with +VDDDD1

Thermal Sensor



DDCxx_AUX4x is NC on PARK

DDCxx_AUX7x is NC on M9x and PARK



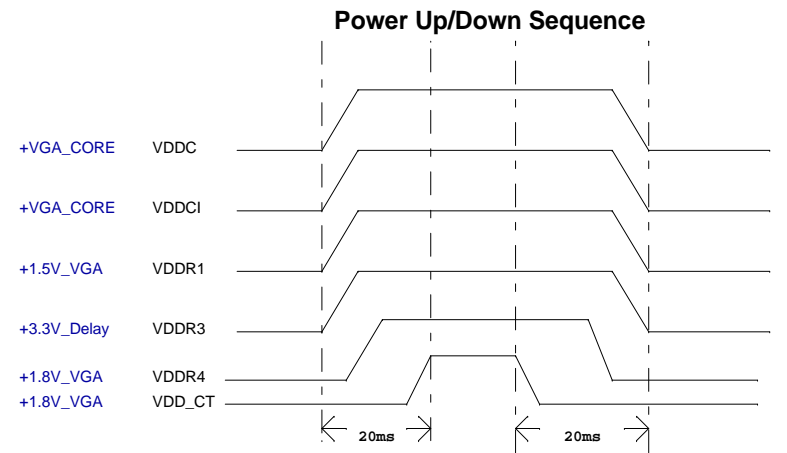
Memory Aperture size fix 256M

GPIO9		GPIO13	GPIO12	GPIO11
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

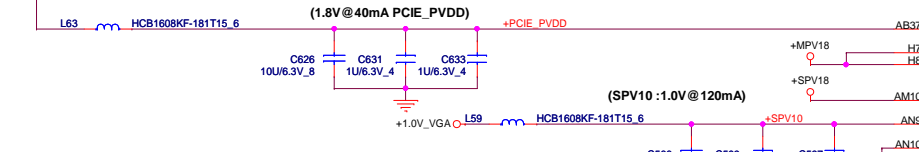
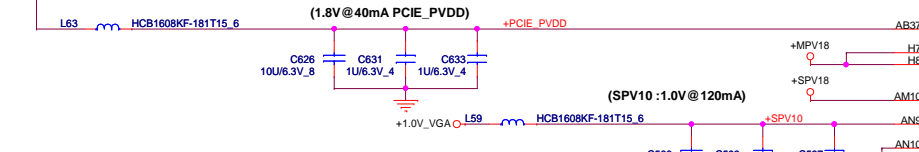
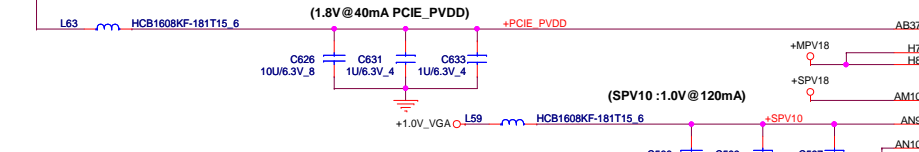
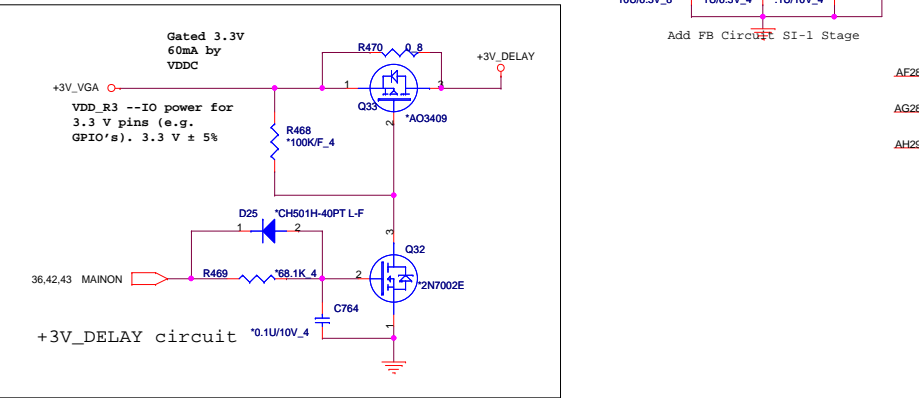
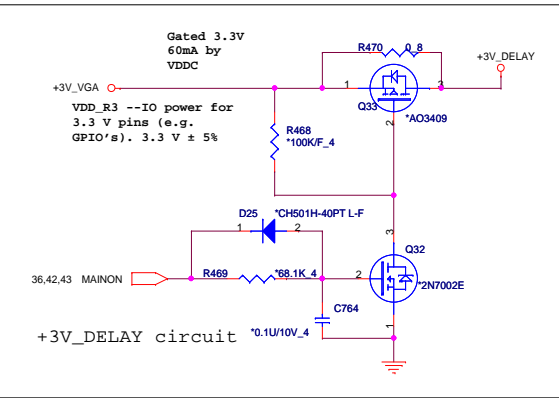
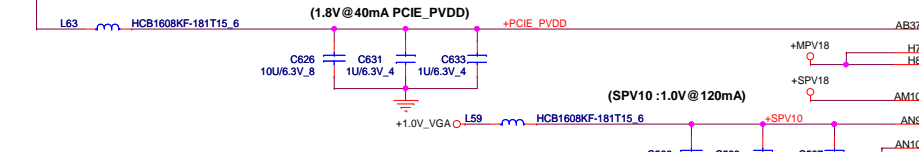
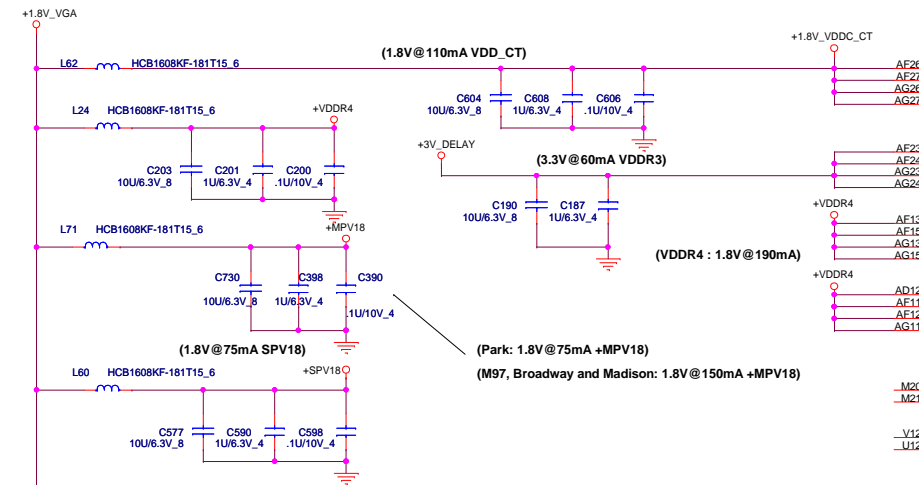
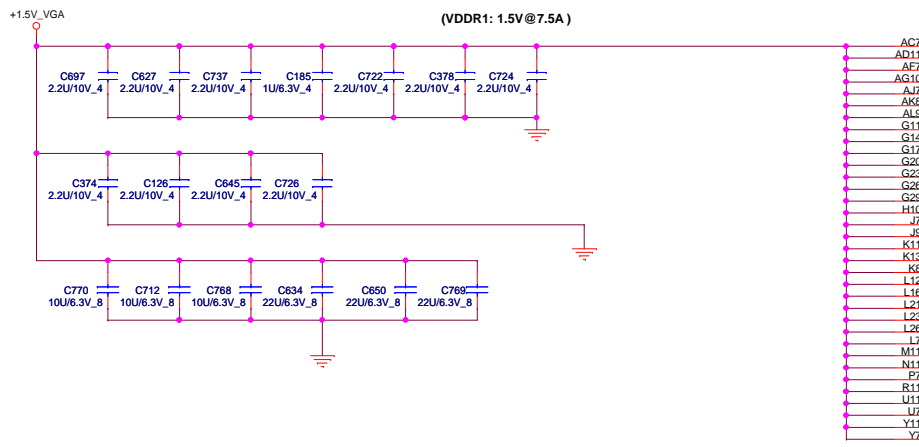
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS			RECOMMENDED SETTINGS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO{13:11}	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	



	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	Date: Monday, September 28, 2009	
NB5/RDZ	ATI Park/Madison(GND&Str&Ther)4/5	Sheet	20 of 46



M87 I/O

AC7	VDDR1#1
AD11	VDDR1#2
AF7	VDDR1#3
AG10	VDDR1#4
AJ7	VDDR1#5
AK8	VDDR1#6
AL9	VDDR1#7
G11	VDDR1#8
G14	VDDR1#9
G17	VDDR1#10
G20	VDDR1#11
G23	VDDR1#12
G26	VDDR1#13
G29	VDDR1#14
H10	VDDR1#15
J7	VDDR1#16
J9	VDDR1#17
K11	VDDR1#18
K13	VDDR1#19
K8	VDDR1#20
L12	VDDR1#21
L16	VDDR1#22
L21	VDDR1#23
L23	VDDR1#24
L26	VDDR1#25
L7	VDDR1#26
M11	VDDR1#27
N11	VDDR1#28
P7	VDDR1#29
R11	VDDR1#30
U11	VDDR1#31
U7	VDDR1#32
Y11	VDDR1#33
Y7	VDDR1#34

LEVEL TRANSLATION

AF26	VDD_CT#1
AF27	VDD_CT#2
AG26	VDD_CT#3
AG27	VDD_CT#4

I/O

AF23	VDDR3#1
AF24	VDDR3#2
AG23	VDDR3#3
AG24	VDDR3#4

VDDR4#1-4

AF13	VDDR4#4
AF15	VDDR4#5
AG13	VDDR4#7
AG15	VDDR4#8

VDDR4#1-4

AD12	VDDR4#1
AF11	VDDR4#2
AF12	VDDR4#3
AG11	VDDR4#6

NC_VDDRHA, NC_VSSRHA, NC_VDDRHB, NC_VSSRHB

PCIE_PVDD

AB37	PCIE_PVDD
------	-----------

MPV18#1, MPV18#2

AM10	MPV18#1
AM10	MPV18#2

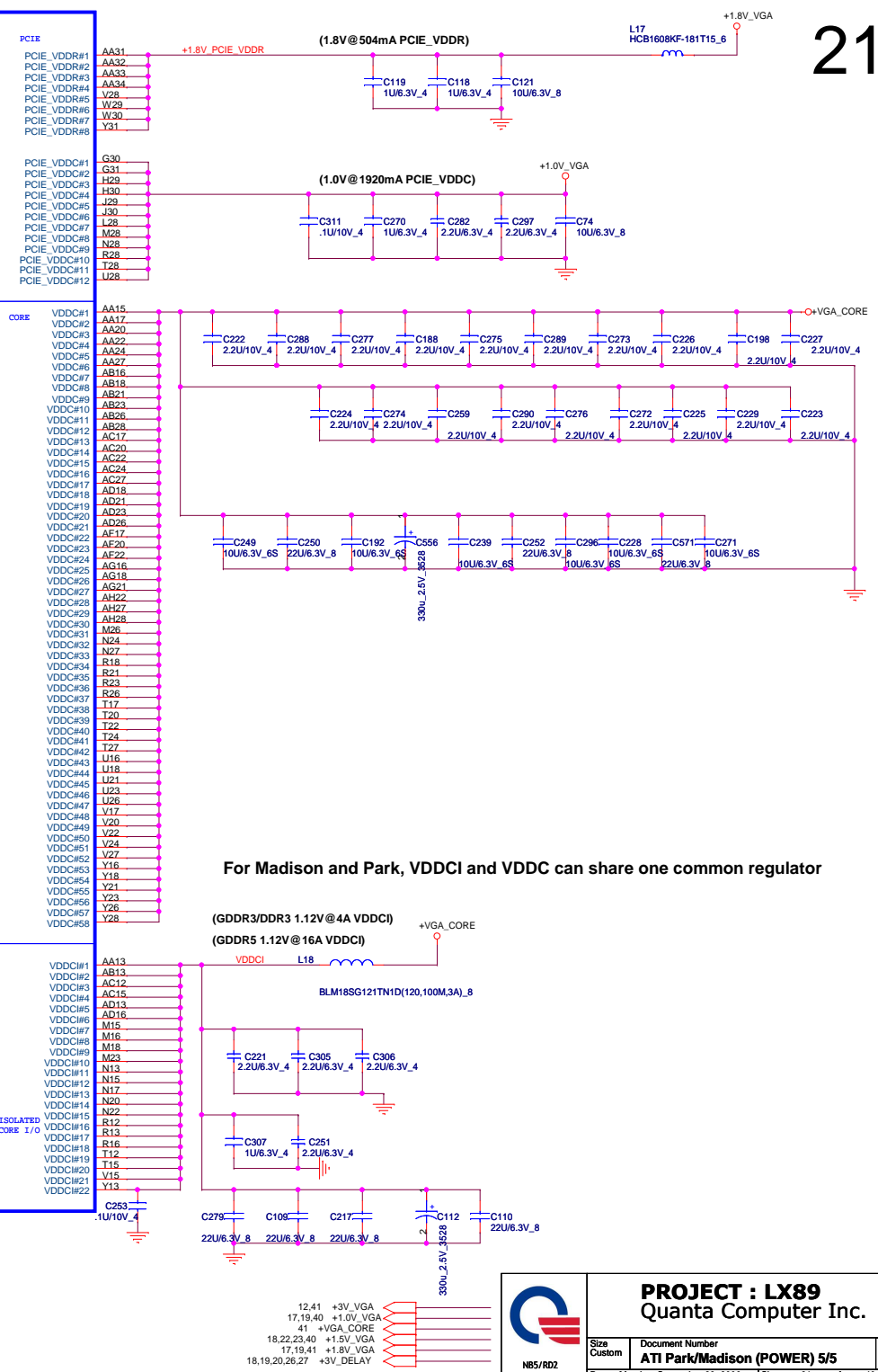
SPV18, SPV10, SPVSS

VOLTAGE SENSE

AF28	FB_VDDC
AG28	FB_VDDCI
AH29	FB_GND

M87_m2

POWER



For Madison and Park, VDDCI and VDDC can share one common regulator

(GDDR3/DDR3 1.12V@4A VDDCI)

(GDDR5 1.2V@16A VDDCI)

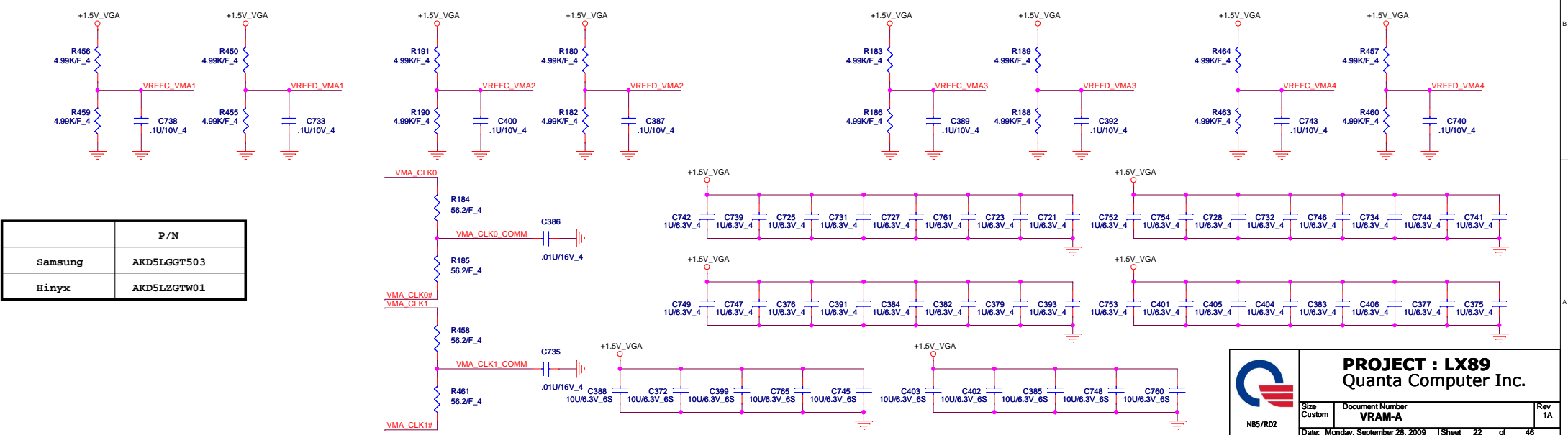
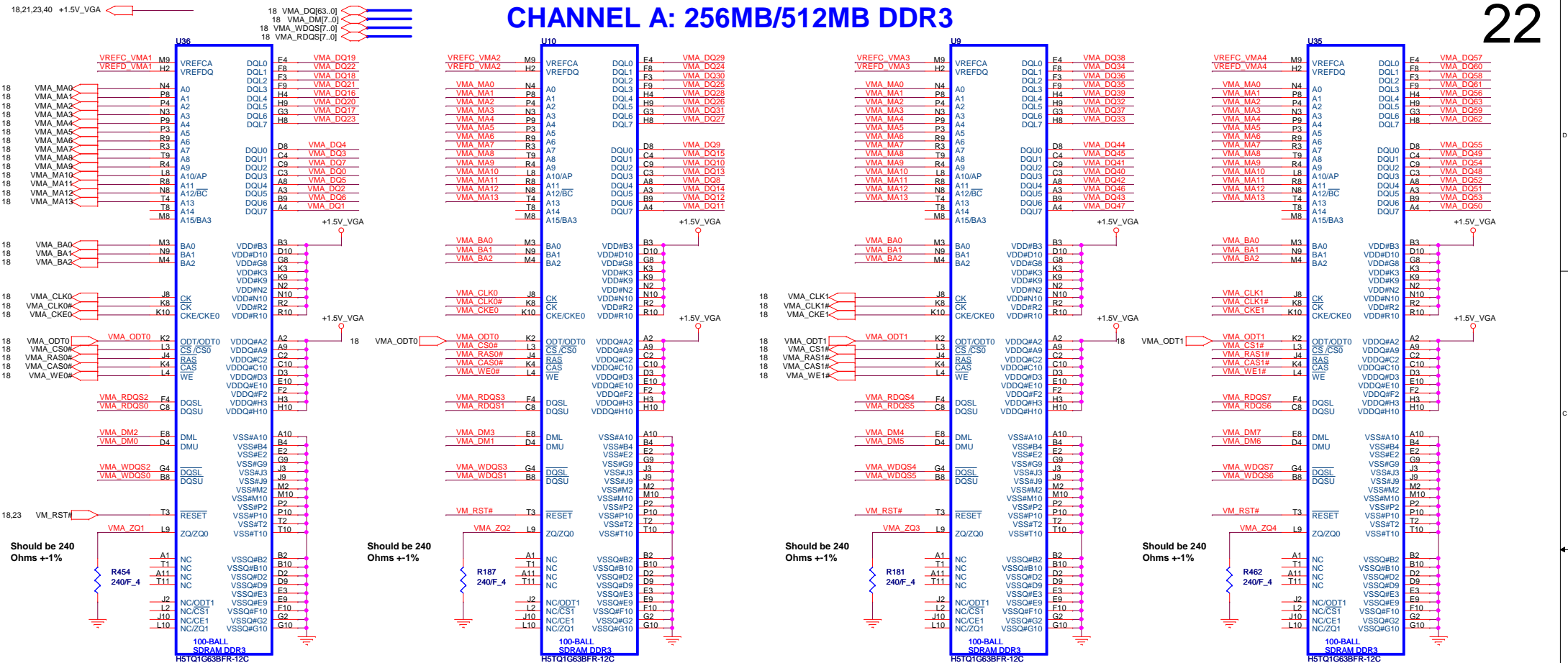
12.41	+3V_VGA
17.19,40	+1.0V_VGA
41	+VGA_CORE
18,22,23,40	+1.5V_VGA
17,19,41	+1.8V_VGA
18,19,20,26,27	+3V_DELAY

PROJECT : LX89
Quanta Computer Inc.

Size Custom
 Document Number **ATI Park/Madison (POWER) 5/5**
 Date: Monday, September 28, 2009 Sheet 21 of 46

Rev 1A

CHANNEL A: 256MB/512MB DDR3

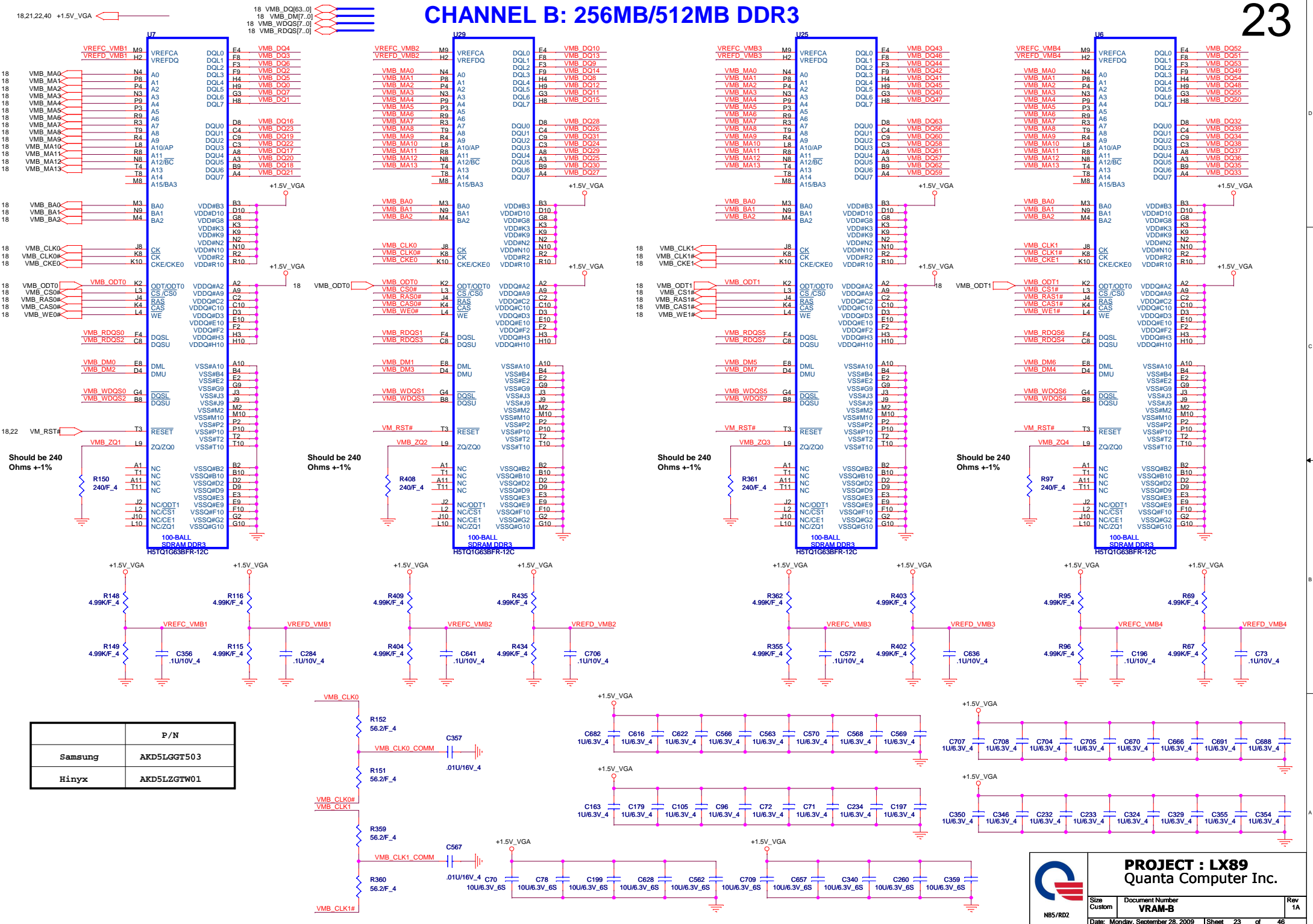


	P/N
Samsung	AKD5LGGT503
Hynix	AKD5LZGTW01

PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number VRAM-A	Rev 1A
Date: Monday, September 28, 2009		
Sheet 22 of 46		

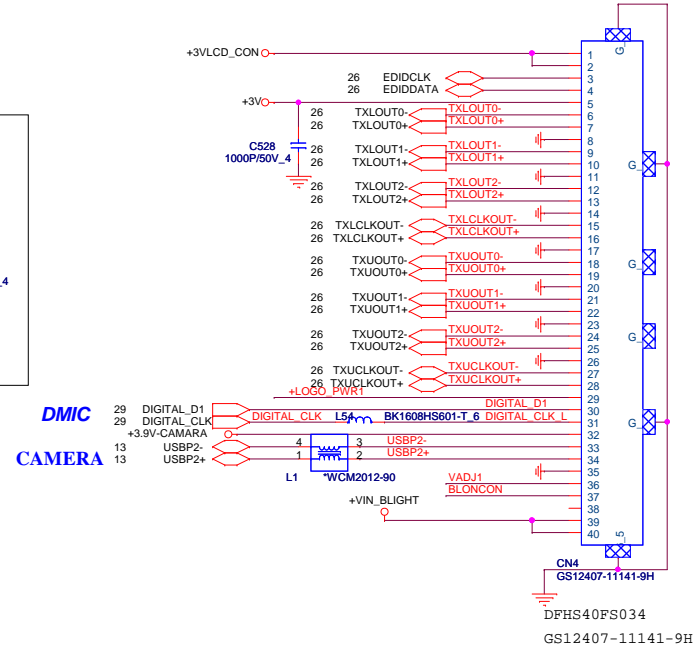
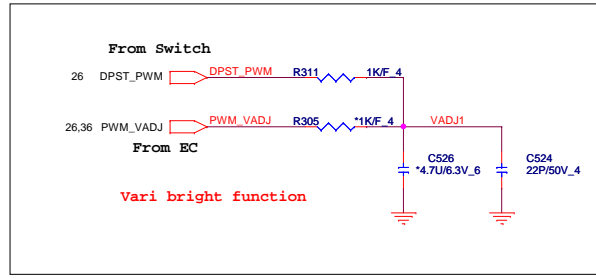
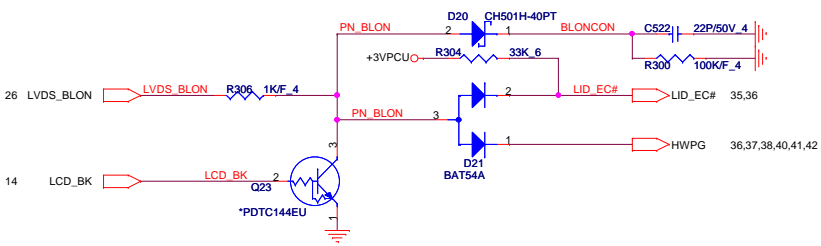
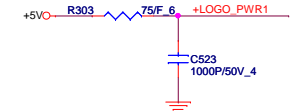
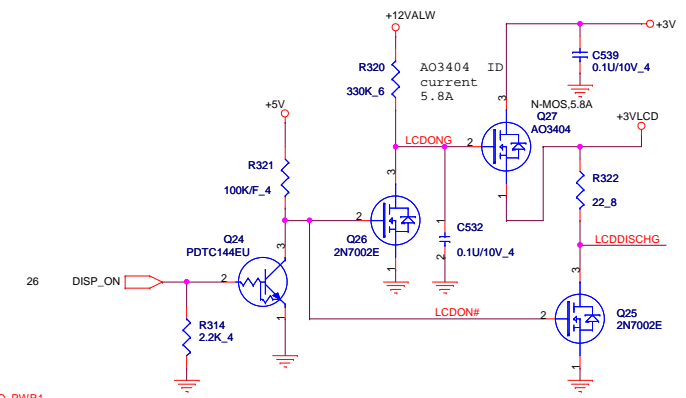
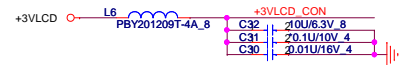
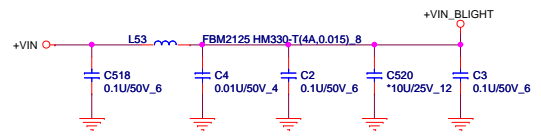
CHANNEL B: 256MB/512MB DDR3



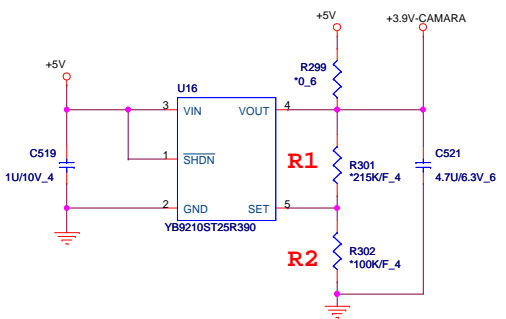
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number VRAM-B	Rev 1A
Date: Monday, September 28, 2009	Sheet 23 of 46	

+VIN	31,37,38,39,40,41,42,43
+12VALW	33,35,40,41,42
+3V	2,3,5,6,7,10,11,12,13,14,15,16,25,26,27,28,29,30,31,32,33,34,35,36,42
+3V_DELAY	18,19,20,21,26,27
+5V	25,26,27,28,29,33,34,35,42

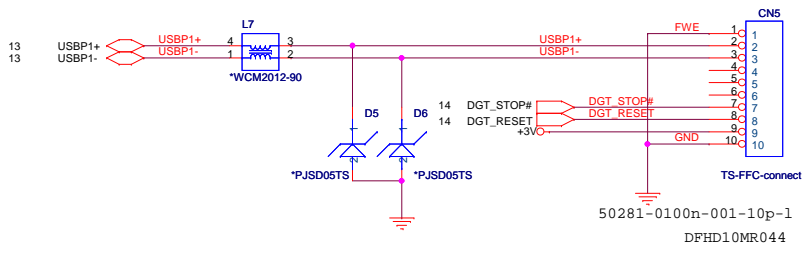


CAMERA POWER



$$V_{out} = 1.25(1 + R1/R2)$$

Digitizer Connector



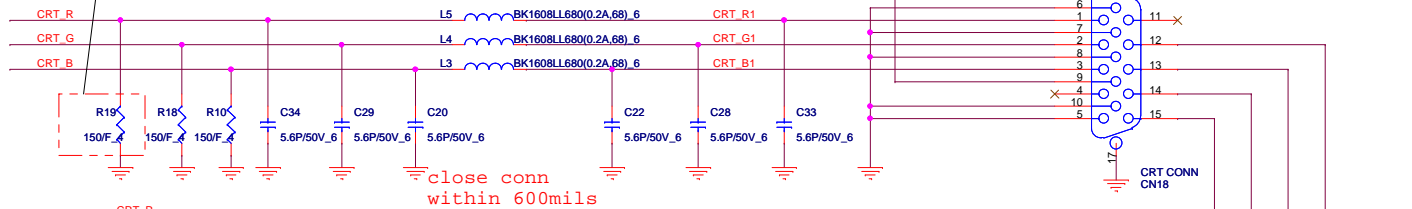
$$V_{out} = 1.25(1 + R1/R2)$$

	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number	LCD CONN	
Date: Monday, September 26, 2009		Sheet 24	of 46

CRT PORT

+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,26,27,28,29,30,31,32,33,34,35,36,42
 +5V 24,26,27,28,29,33,34,35,42
 +3V_DELAY 18,19,20,21,26,27

R19 for UMA use 140 ohm
 for DIS+PowerExpress use 150 ohm (AMD)

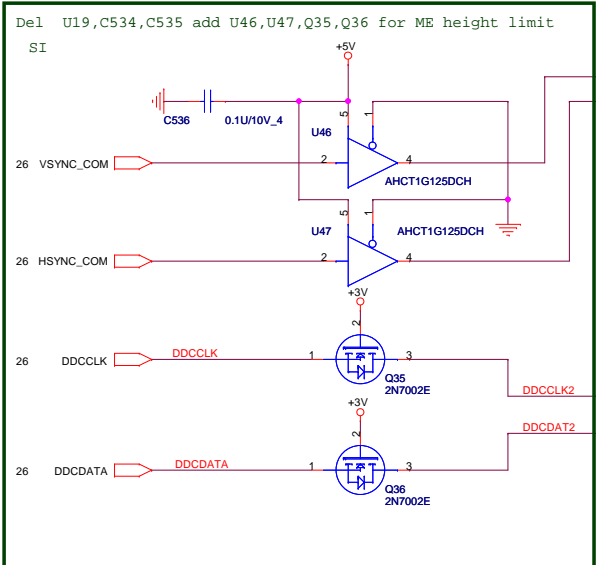


26 CRT_R
 26 CRT_G
 26 CRT_B

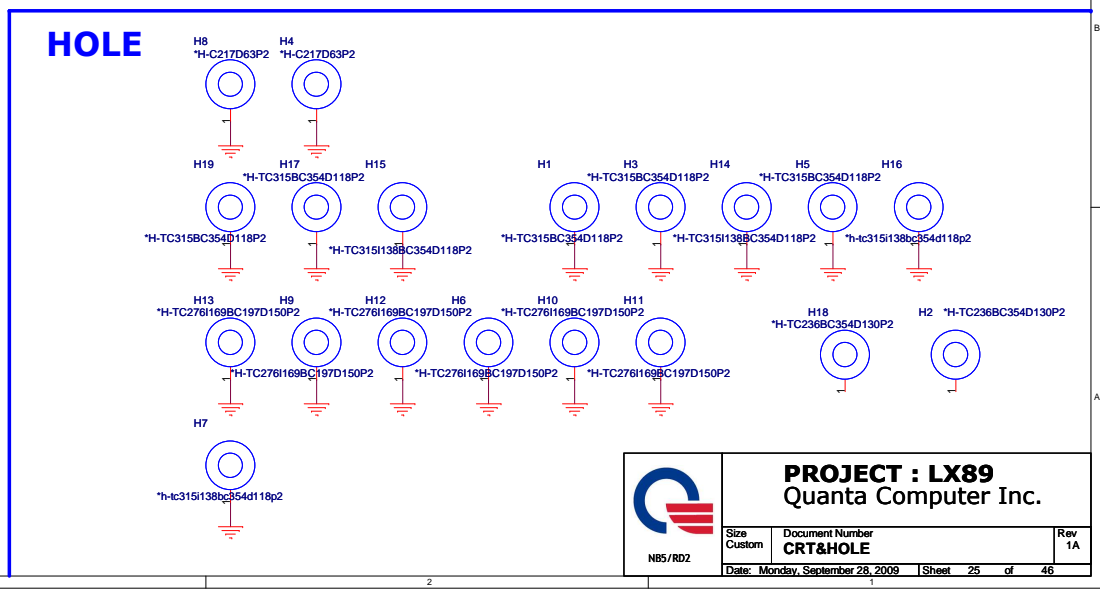
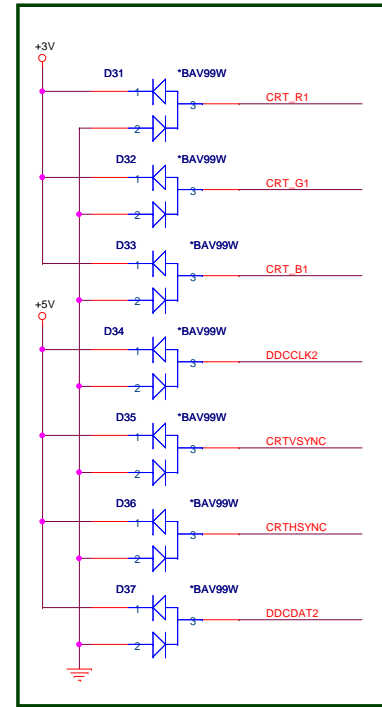
close conn
 within 600mils

DFDS15FR148
 dsusb-070546fr015s22fzr-15p-v

SI Add D31-D37 for ME height limit



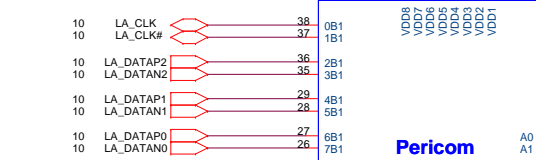
Del U19,C534,C535 add U46,U47,Q35,Q36 for ME height limit
 SI



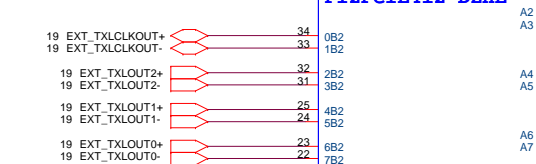
		PROJECT : LX89 Quanta Computer Inc.	
Size Custom	Document Number CRT&HOLE	Rev 1A	
Date: Monday, September 28, 2009	Sheet 25	of 46	

For Single-link panel

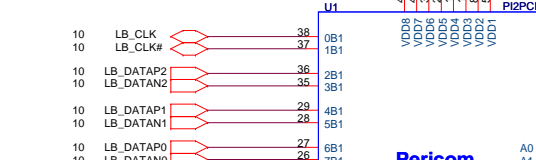
IGPU_Channel-A



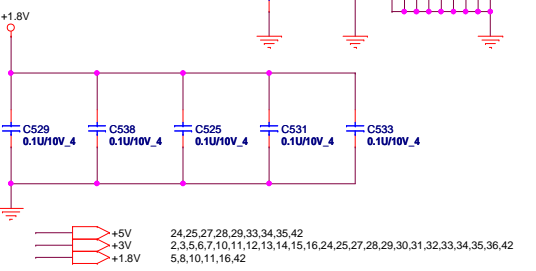
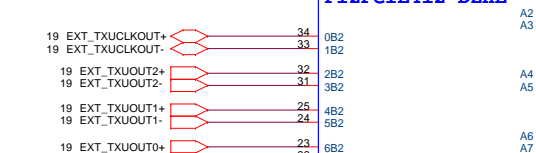
DGPU_Channel-A



IGPU_Channel-B



DGPU_Channel-B

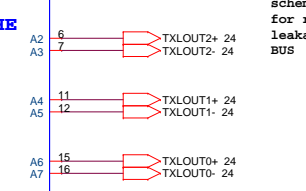


+5V	24,25,27,28,29,33,34,35,42
+3V	2,3,5,6,7,10,11,12,13,14,15,16,24,25,27,28,29,30,31,32,33,34,35,36,42
+1.8V	5,8,10,11,16,42

LVDS Channel Switch

SELx	Ay
HIGH	B2
LOW	B1

follow AMD reference schematic change for reduce leakage to VDDR3 BUS

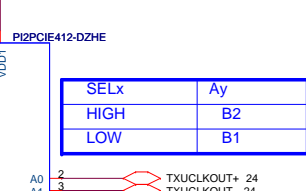


SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

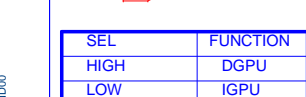
LVDS Channel Switch



SELx	Ay
HIGH	B2
LOW	B1

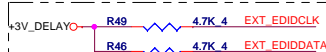


SEL	FUNCTION
HIGH	DGPU
LOW	IGPU

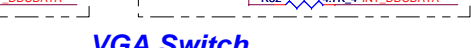
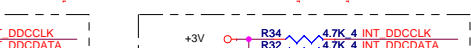
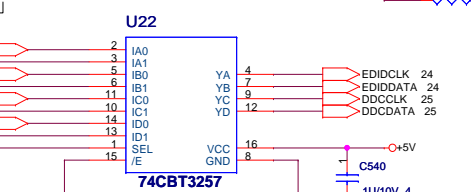
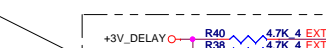
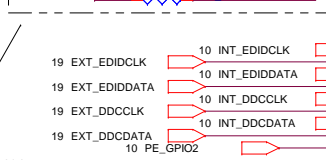


OPTION SIGNAL FROM NB to LVDS for UMA

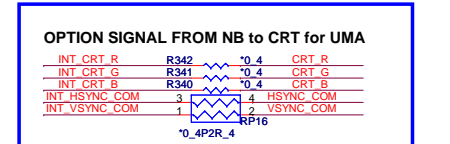
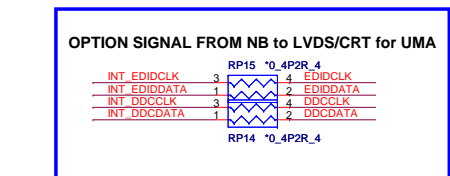
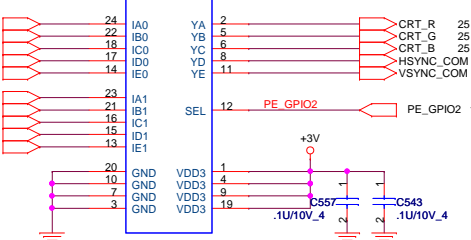
LA_CLK	1	2	TXLCLKOUT+
LA_CLK#	3	2	TXLCLKOUT-
LA_DATAP0	RP10	2	*0_4P2R_4 TXLOUT0+
LA_DATAN0	RP13	2	*0_4P2R_4 TXLOUT0-
LA_DATAP1	RP11	2	*0_4P2R_4 TXLOUT1+
LA_DATAN1	RP12	2	*0_4P2R_4 TXLOUT1-
LA_DATAP2	RP12	2	*0_4P2R_4 TXLOUT2+
LA_DATAN2	RP11	2	*0_4P2R_4 TXLOUT2-
LB_CLK	1	2	TXUCLKOUT+
LB_CLK#	3	2	TXUCLKOUT-
LB_DATAP0	RP6	2	*0_4P2R_4 TXUOUT0+
LB_DATAN0	RP9	2	*0_4P2R_4 TXUOUT0-
LB_DATAP1	RP3	2	*0_4P2R_4 TXUOUT1+
LB_DATAN1	RP8	2	*0_4P2R_4 TXUOUT1-
LB_DATAP2	RP8	2	*0_4P2R_4 TXUOUT2+
LB_DATAN2	RP7	2	*0_4P2R_4 TXUOUT2-



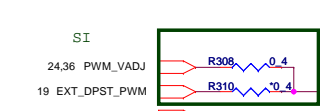
LVDS/CRT DDC Switch



VGA Switch

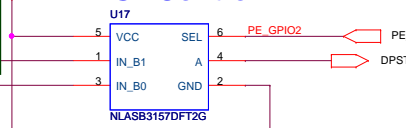


DIS Change Vari bright function from EC control

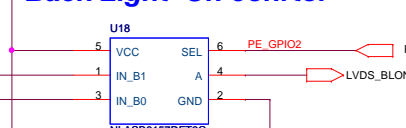
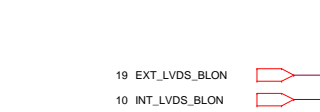


DPST Control

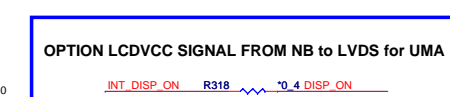
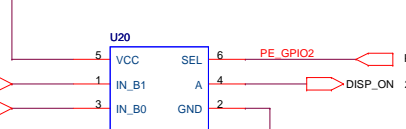
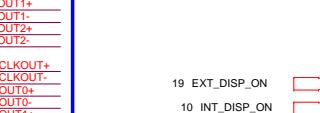
SEL	FUNCTION(COM)
LOW	IN_B0 to A
HIGH	IN_B1 to A



Back Light On control

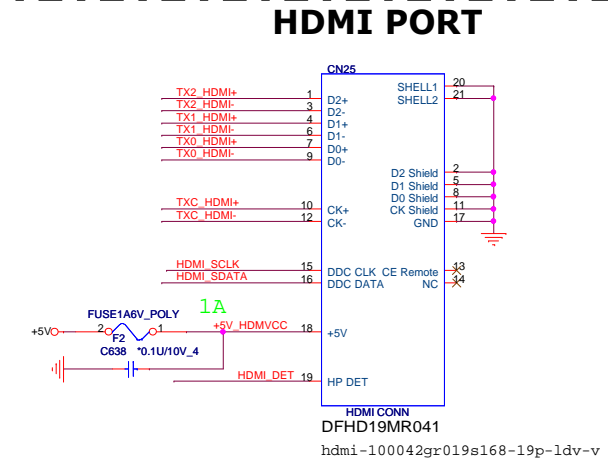
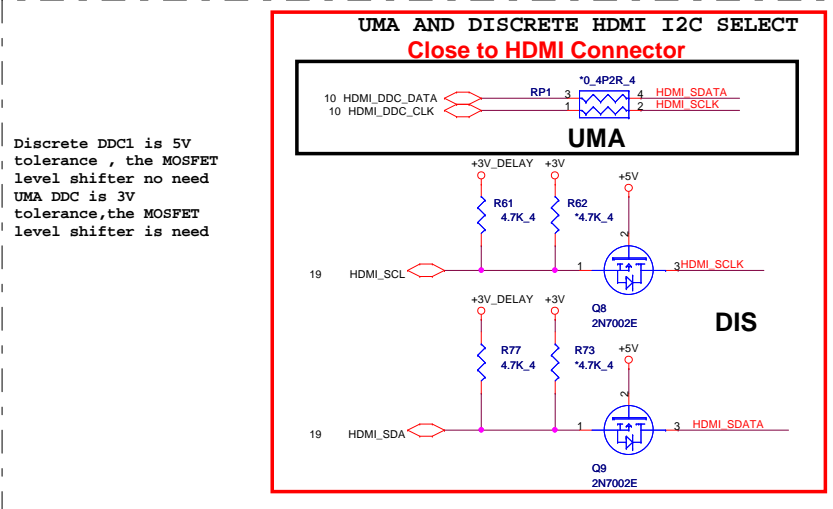
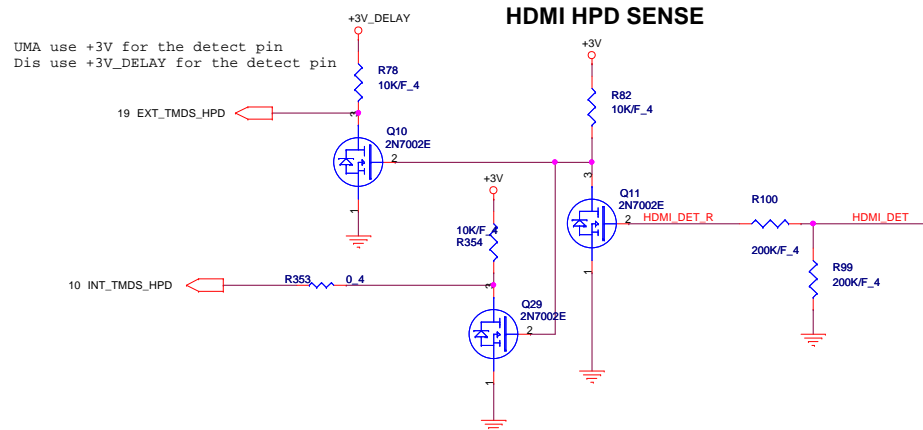
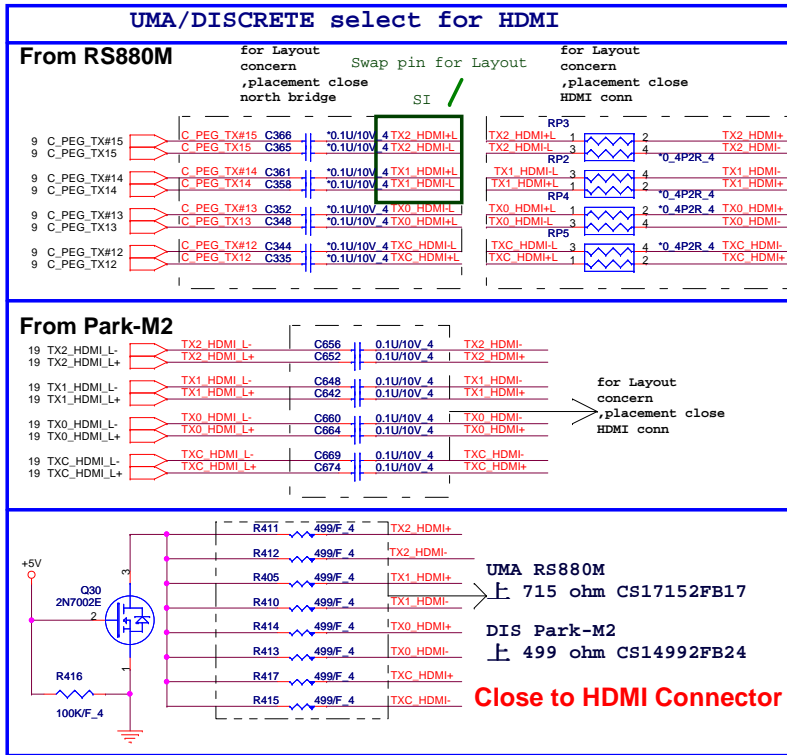


LCDVcc control



PROJECT : LX89
Quanta Computer Inc.

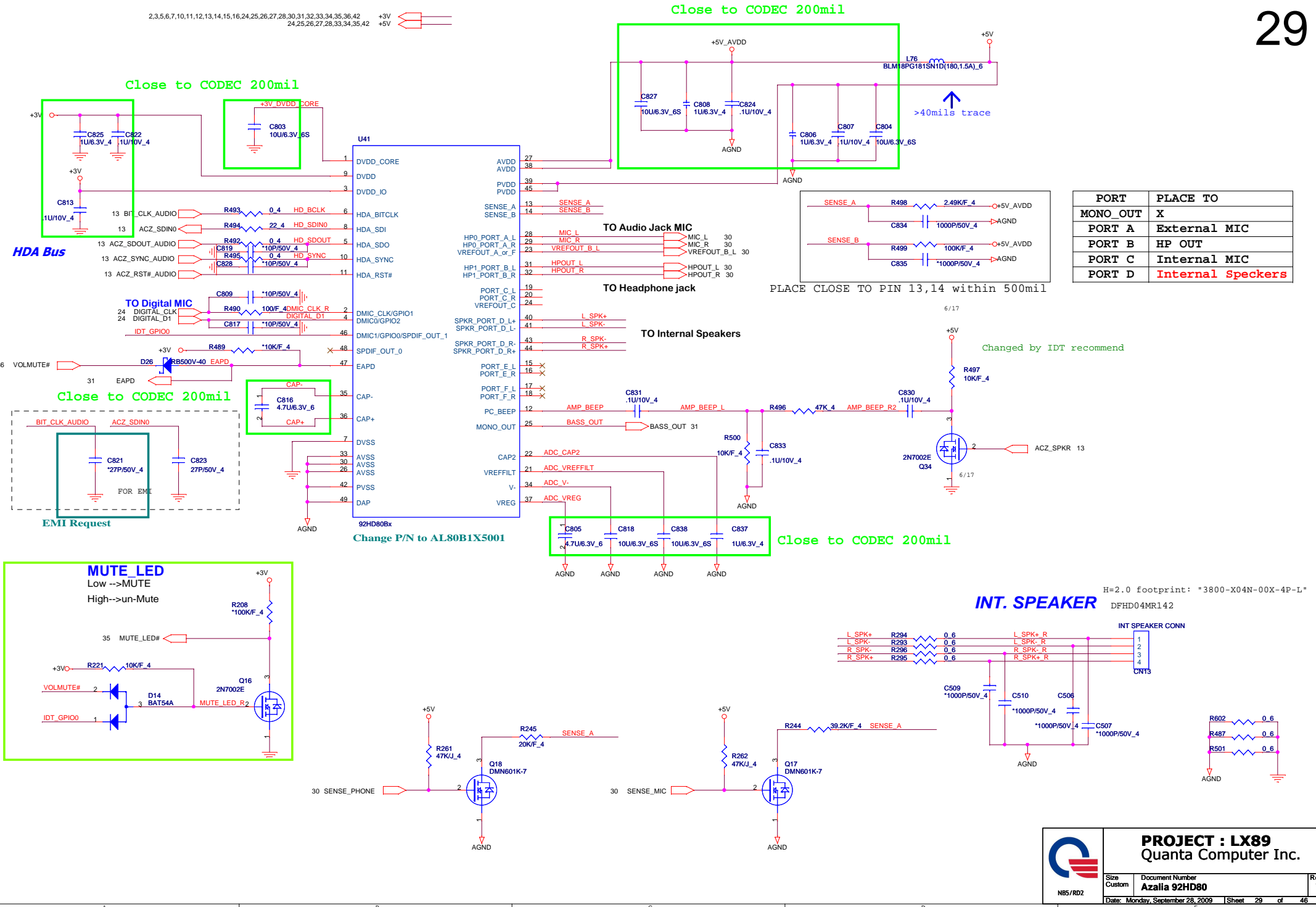
Size Custom	Document Number	Rev 1A
	LVDS/CRT Hyper_switch	
Date: Monday, September 28, 2009		Sheet 26 of 46



+5V 24,25,26,28,29,33,34,35,42
 +3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,28,29,30,31,32,33,34,35,36,42
 +3V_DELAY 18,19,20,21,26

	PROJECT : LX89		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number		
	HDMI		
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2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,30,31,32,33,34,35,36,42
24,25,26,27,28,33,34,35,42



Close to CODEC 200mil

Close to CODEC 200mil

HDA Bus

TO Digital MIC

TO Audio Jack MIC

TO Headphone jack

TO Internal Speakers

Close to CODEC 200mil

EMI Request

MUTE_LED

Low -->MUTE
High-->un-Mute

Close to CODEC 200mil

INT. SPEAKER

PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers

PLACE CLOSE TO PIN 13,14 within 500mil

Changed by IDT recommend

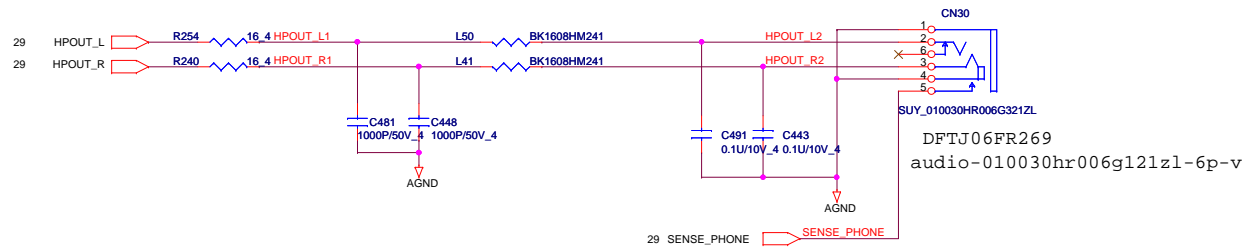
H=2.0 footprint: "3800-X04N-00X-4P-L"
DFHD04MR142

	PROJECT : LX89 Quanta Computer Inc.	
	Size Custom Document Number Azalia 92HD80	Rev 1A
Date: Monday, September 28, 2009		Sheet 29 of 46

Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

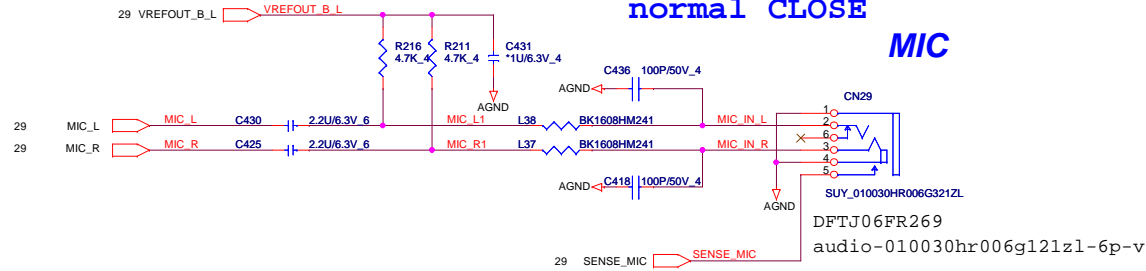
33,34,36,37,38,39,40,41,42,43 +5VPCU
2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,31,32,33,34,35,36,42 +3V

normal CLOSE Line out



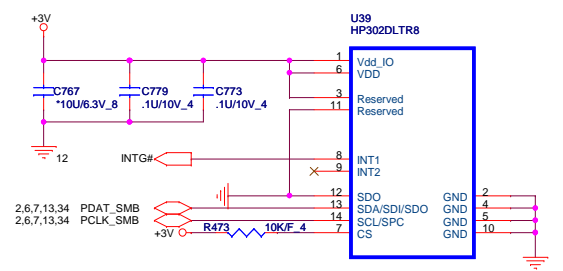
Note: JACK_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.


normal CLOSE MIC



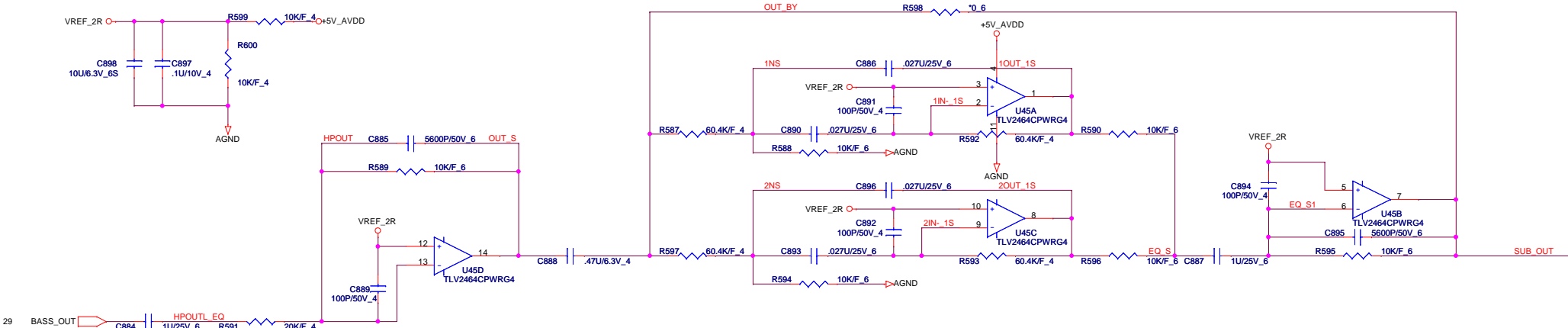
Accelerometer Sensor

SGT-LI9302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



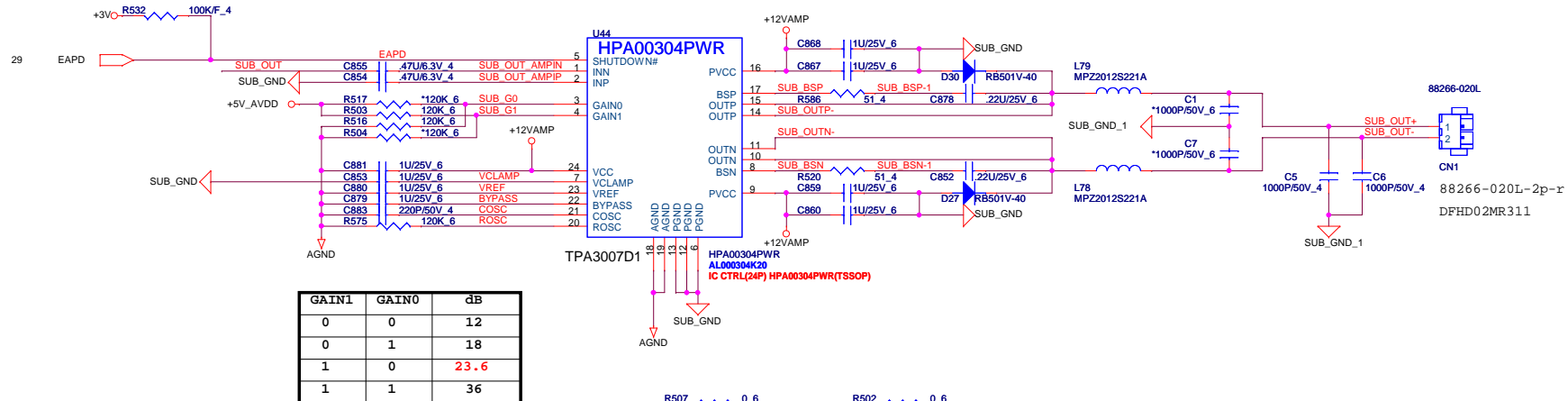
 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number Audio Jack/Accelerometer	

EQ FOR SUBWOOFER



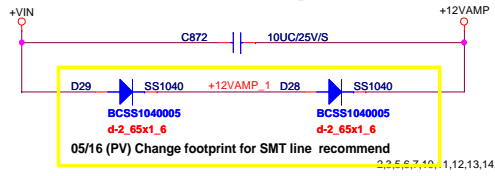
MODEL	UP7
R9402	60.4K/F_6
R9403	60.4K/F_6
R9407	60.4K/F_6
R9408	60.4K/F_6
C5144	0.027U/25V_6
C5146	0.027U/25V_6
C5148	0.027U/25V_6
C5153	0.027U/25V_6

5/27: NA for subwofer function



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

Sub-Woofer power

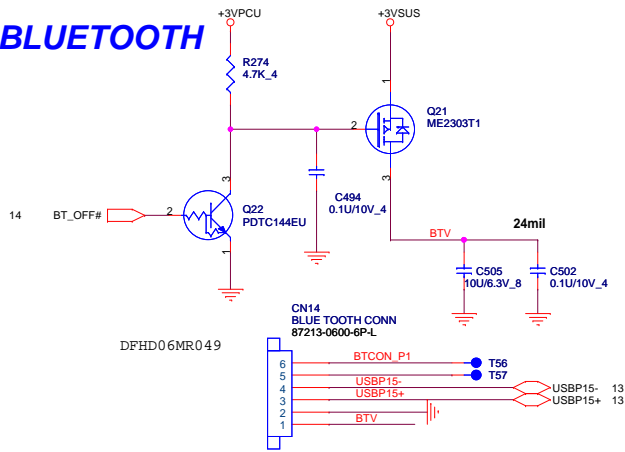


+3V 2,3,5,6,7,10,11,12,13,14,15,16,24,25,26,27,28,29,30,32,33,34,35,36,42
 +5V_AVDD 29
 +VIN 24,37,38,39,40,41,42,43

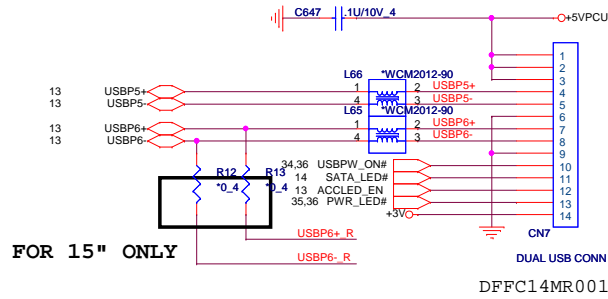
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
SUBWOOFER (EQ & AMP.)		
Date: Monday, September 28, 2009	Sheet 31	of 46

BLUETOOTH

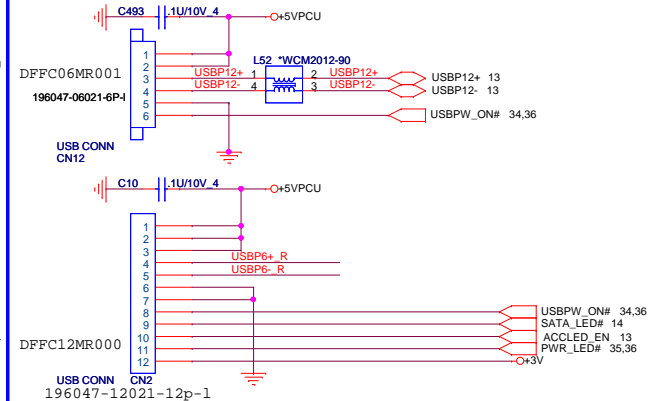


RIGHT SIDE USB2 for 17"



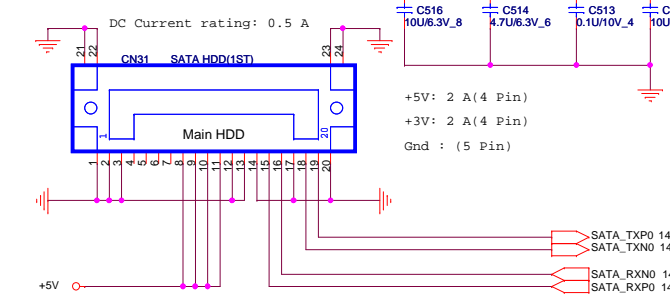
FOR 15" ONLY

RIGHT SIDE USB2 for 15"



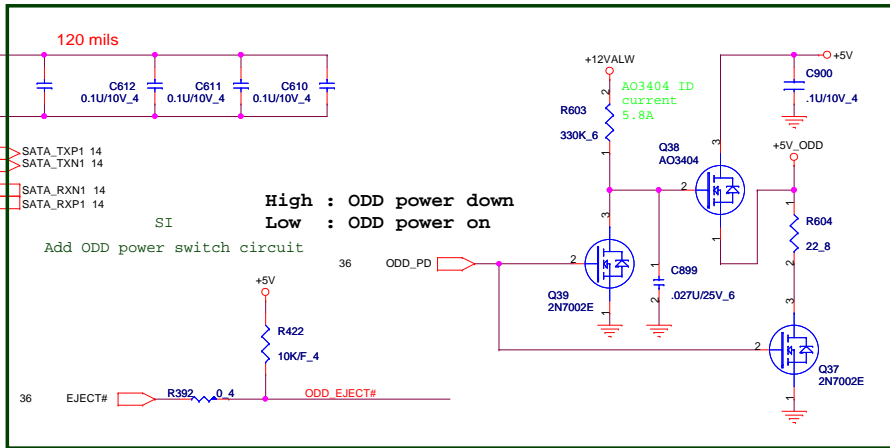
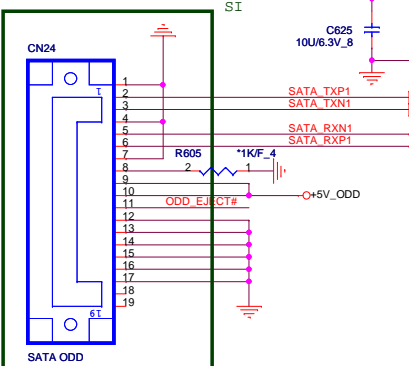
SATA HDD CONNECTOR

H=2.6 Footprint: "GS12201-1011-9F-20P-L"
DFHD20MR023



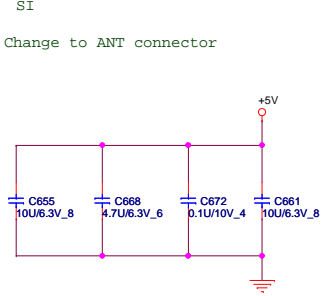
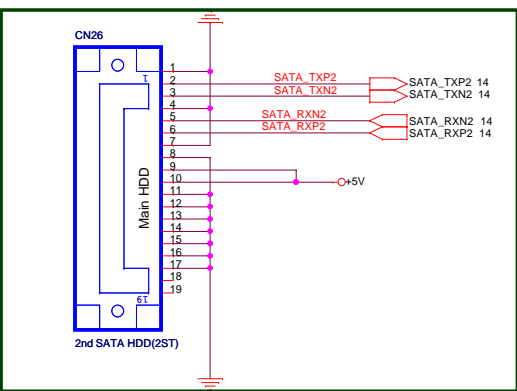
SATA CD-ROM

Change to ANT connector



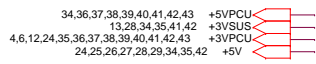
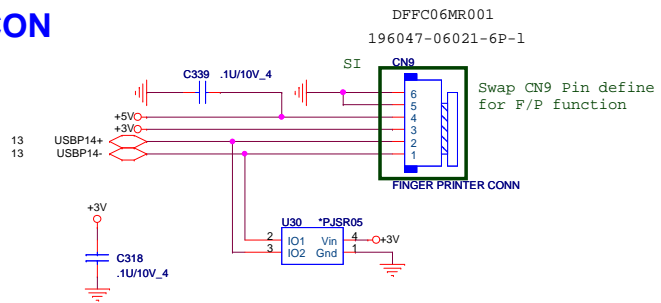
SATA_2 HDD CONNECTOR FOR 17.3"

+5V: 2 A(4 Pin)
Gnd : (5 Pin)



USB Fingerprint CON

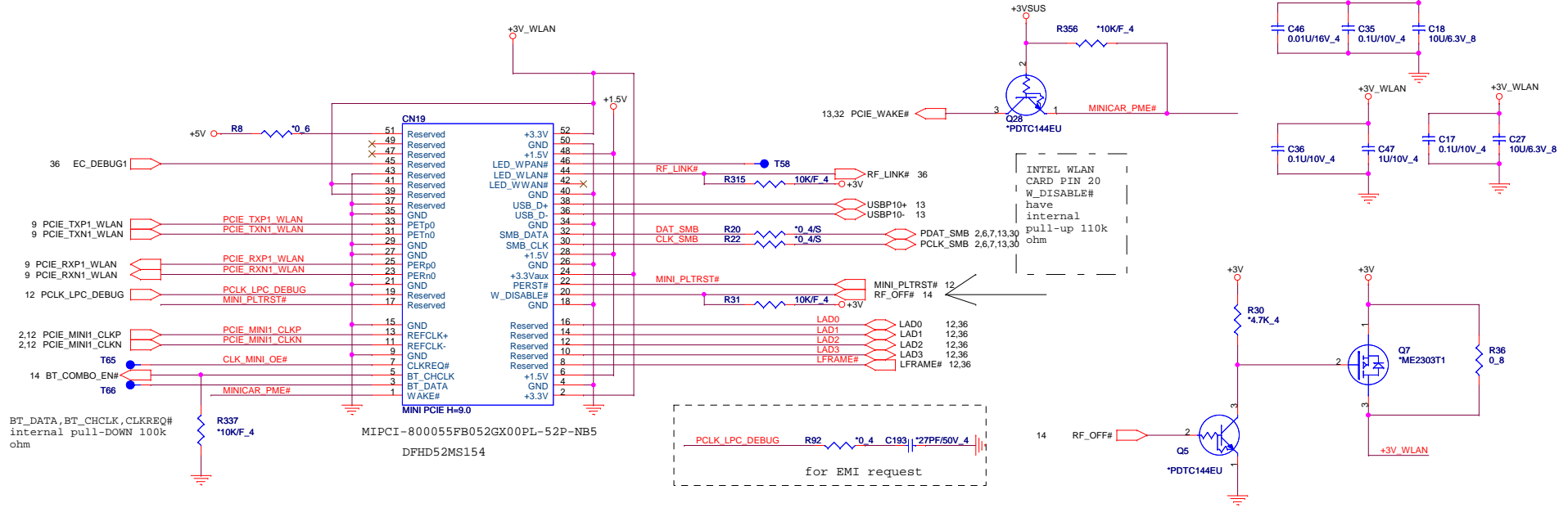
1. SYSTEM GND
2. SYSTEM GND
3. LED PWR(+5V)
4. USB PWR(+3V)
5. USB1.1+
6. USB1.1-



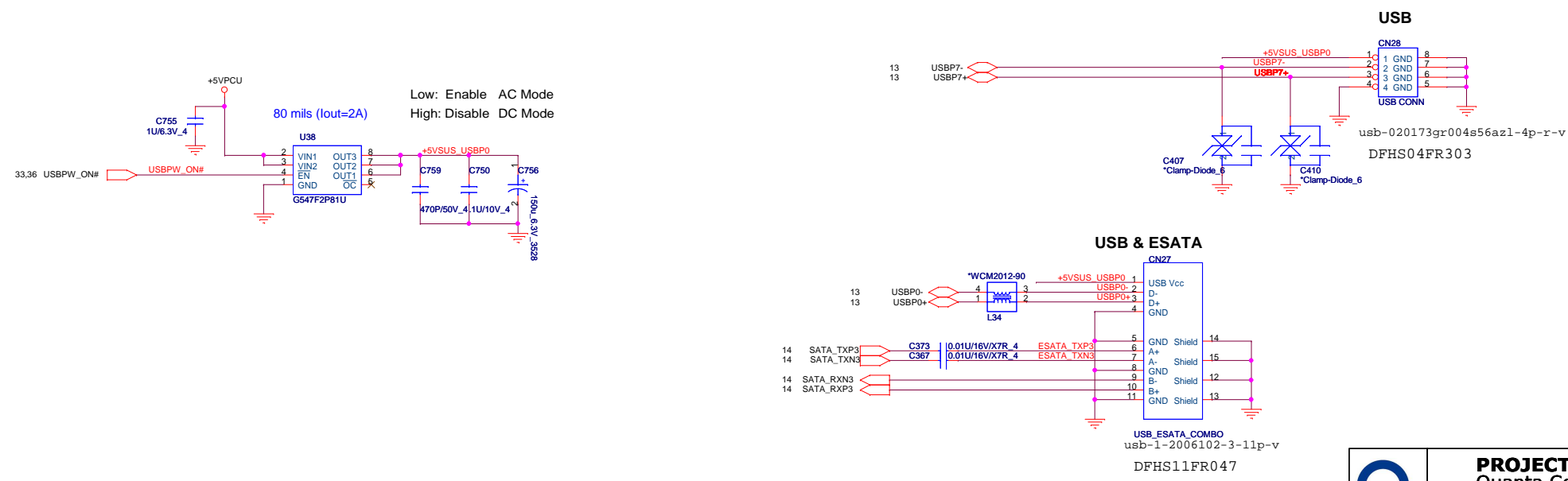
PROJECT : LX89
Quanta Computer Inc.

Size Custom	Document Number BT/FP/USBX2/SATA HDDX2/ODD	Rev 1A
Date: Monday, September 28, 2009	Sheet 33 of 46	

Mini PCI-E Card WLAN

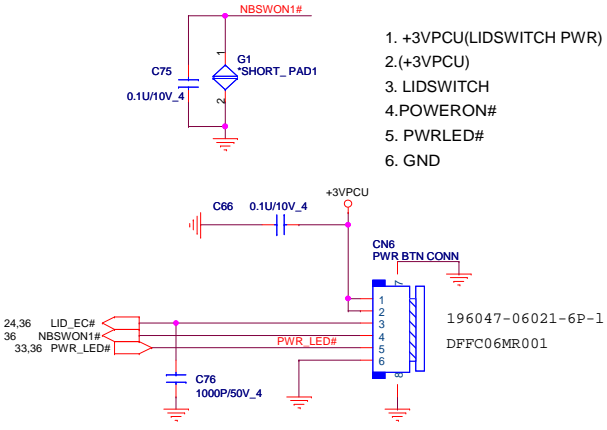


USB2.0 X 1 and E-SATA/USB2.0 COMBO

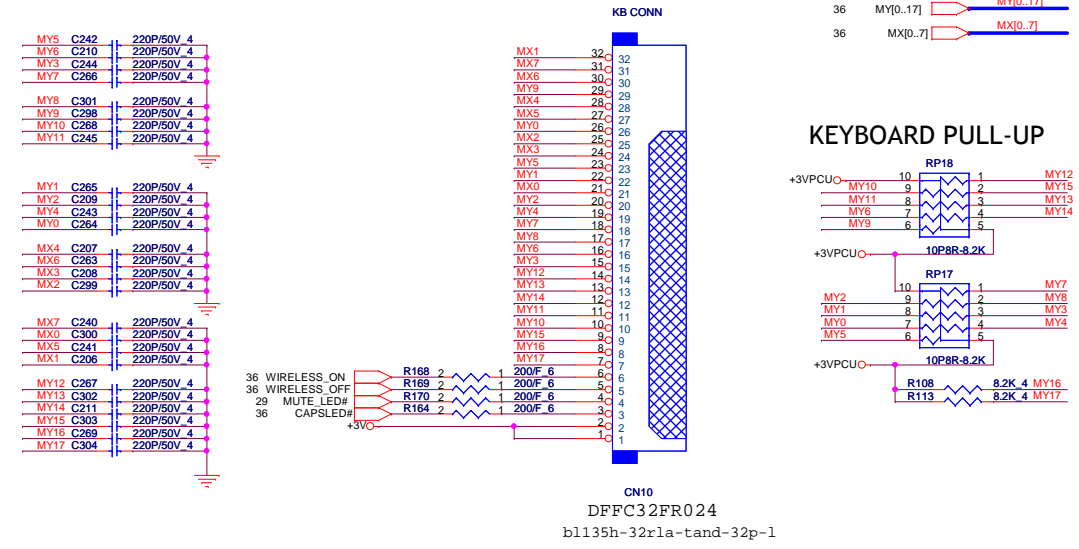


	PROJECT : LX89	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A
Mini CARD		
Date: Monday, September 28, 2009	Sheet 34	of 46

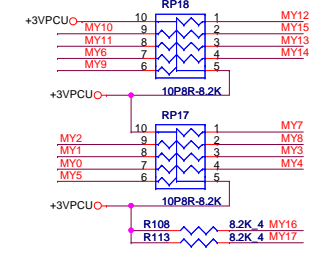
POWER BUTTON CONNECT



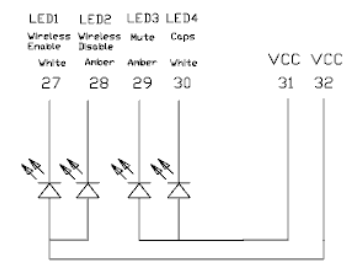
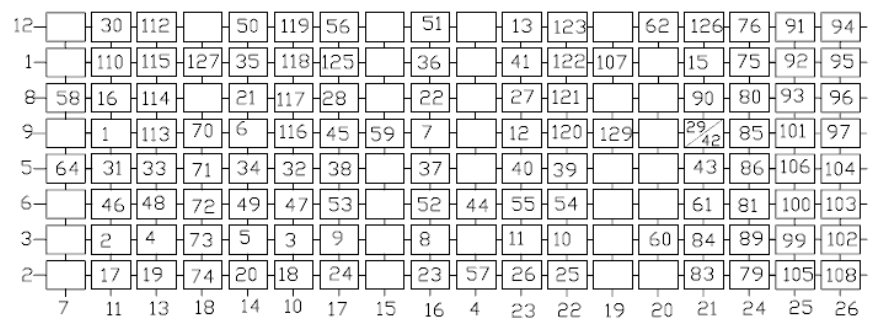
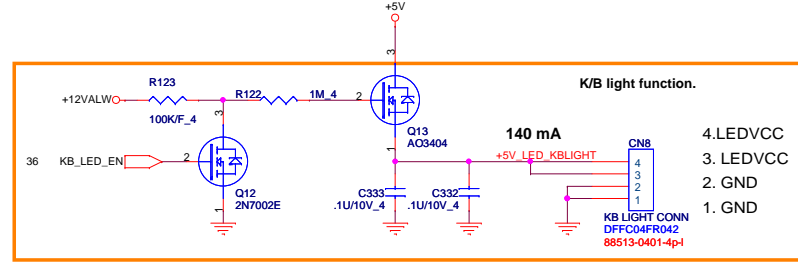
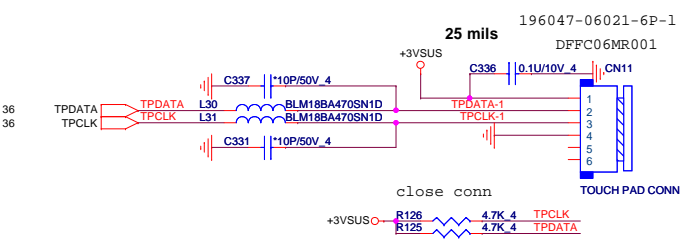
KEYBOARD Con.

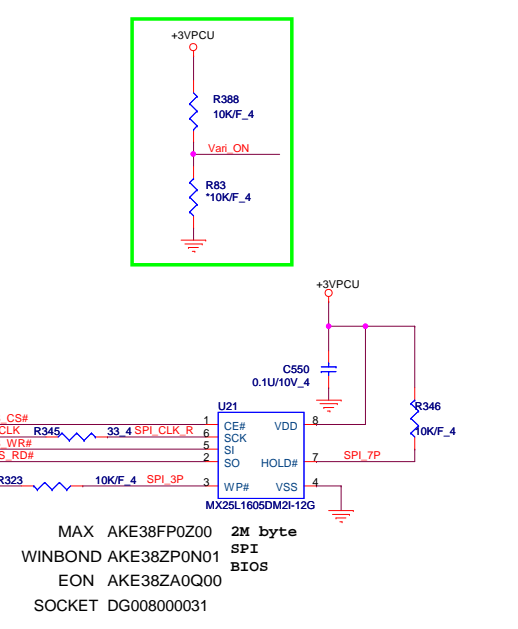
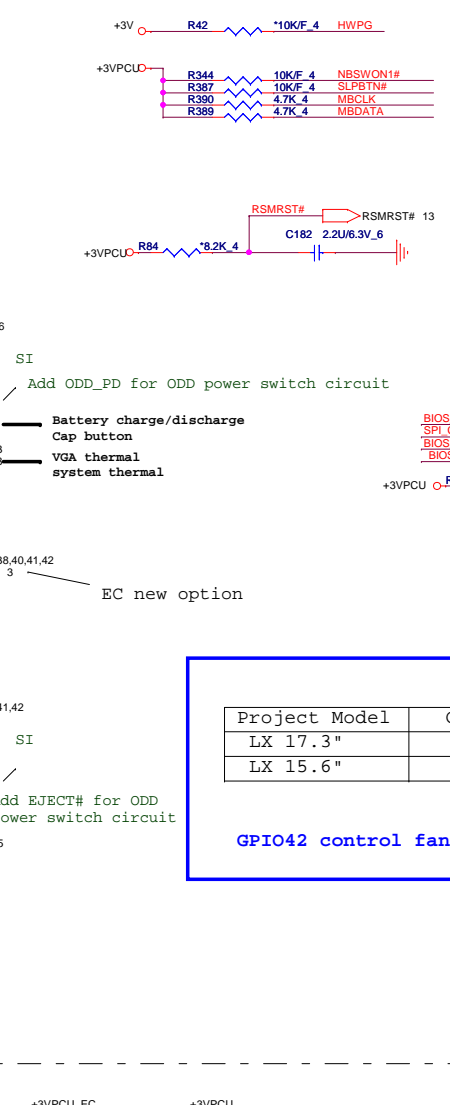
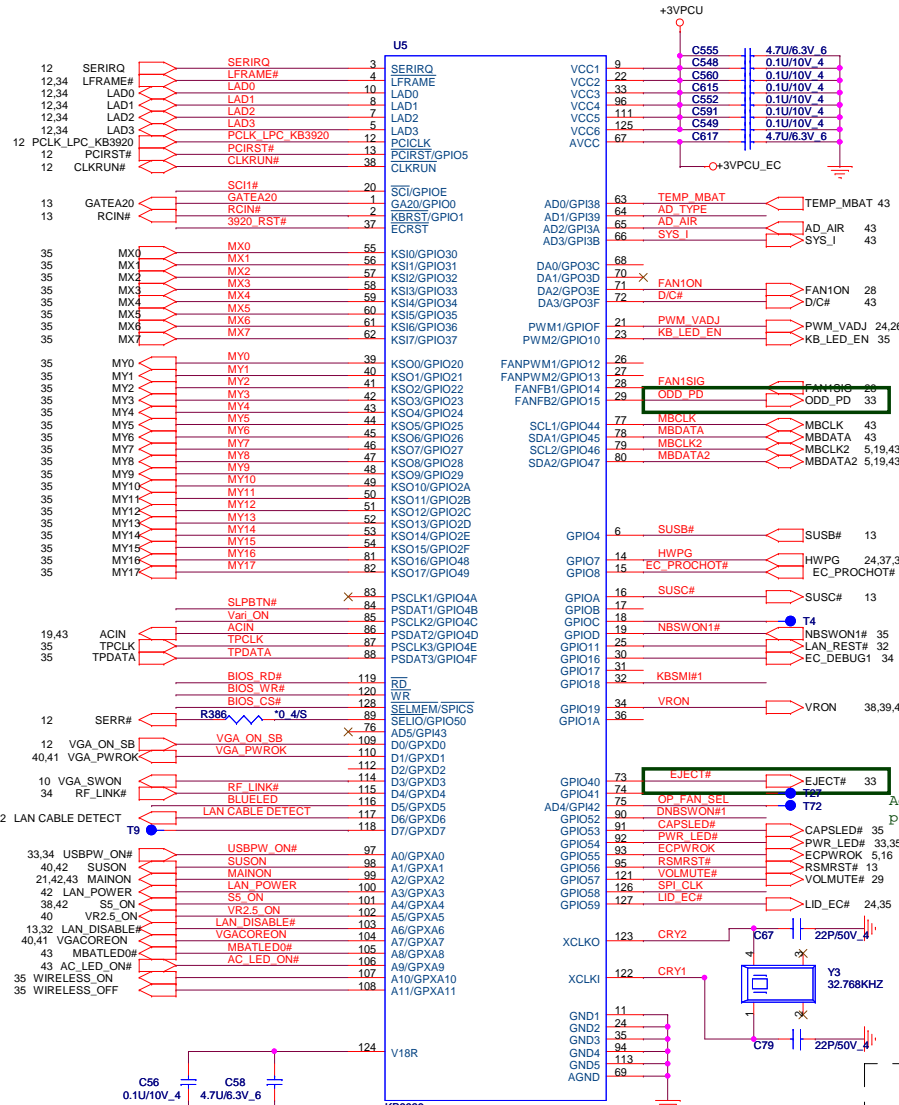


KEYBOARD PULL-UP



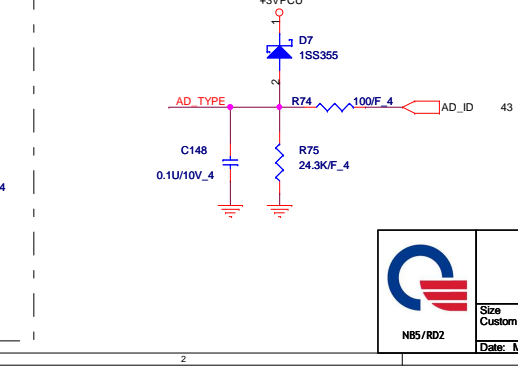
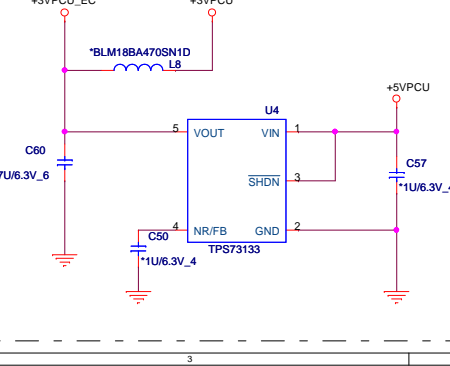
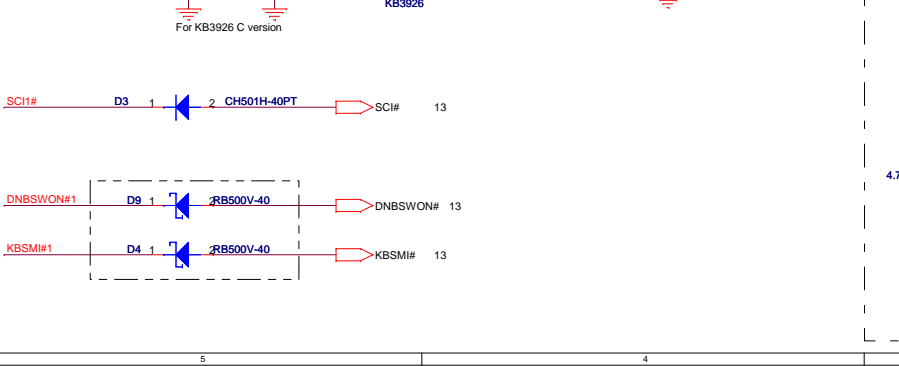
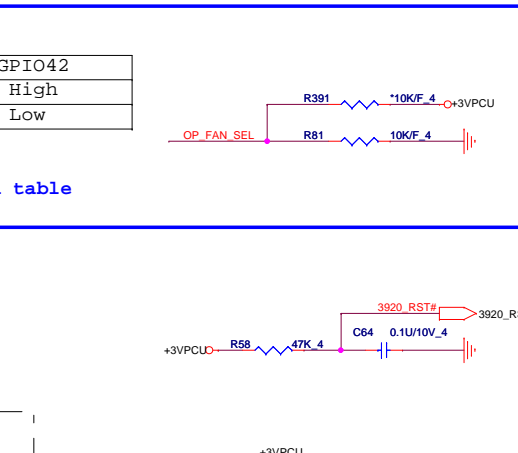
TOUCH PAD CONN





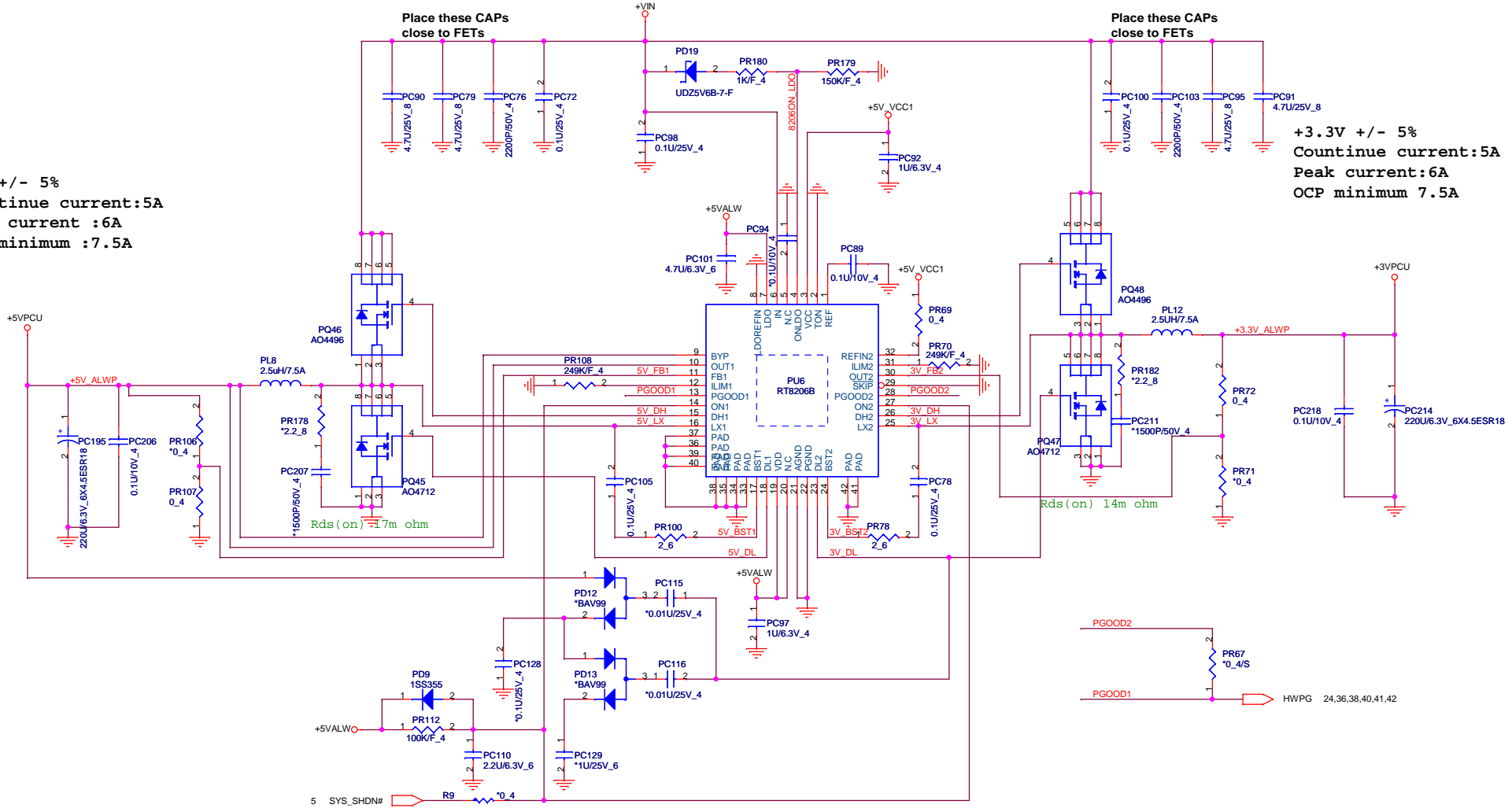
Project Model	GPIO42
LX 17.3"	High
LX 15.6"	Low

GPIO42 control fan table



+5V +/- 5%
 Countinue current:5A
 Peak current :6A
 OCP minimum :7.5A

+3.3V +/- 5%
 Countinue current:5A
 Peak current:6A
 OCP minimum 7.5A



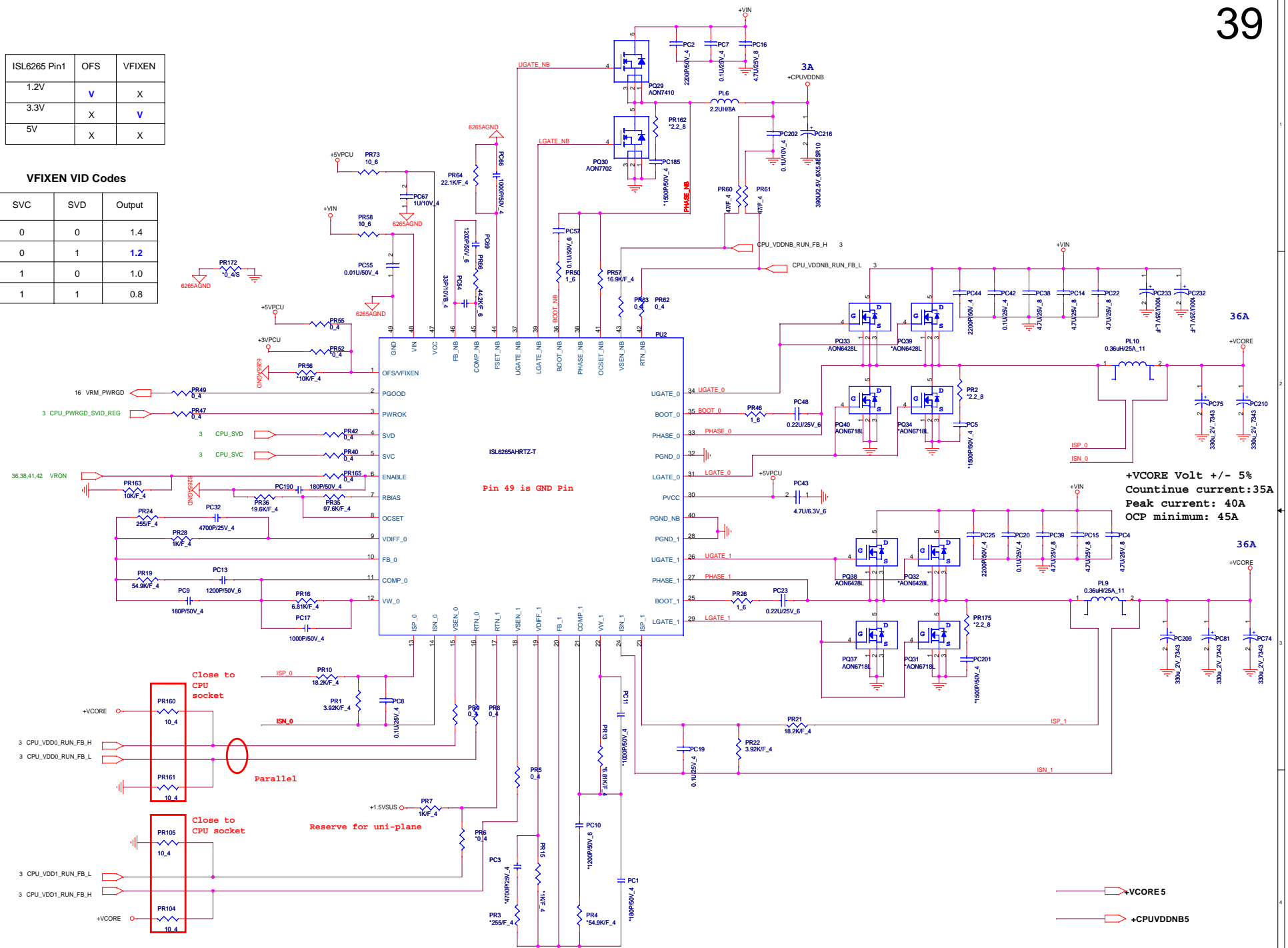
- +VIN 24,31,38,39,40,41,42,43
- +3VPCU 4,6,12,24,33,35,36,38,39,40,41,42,43
- +5VPCU 33,34,36,38,39,40,41,42,43

	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Size Custom	Document Number +5V/+3V (RT8206B)
Date: Monday, September 28, 2009 Sheet 37 of 46		

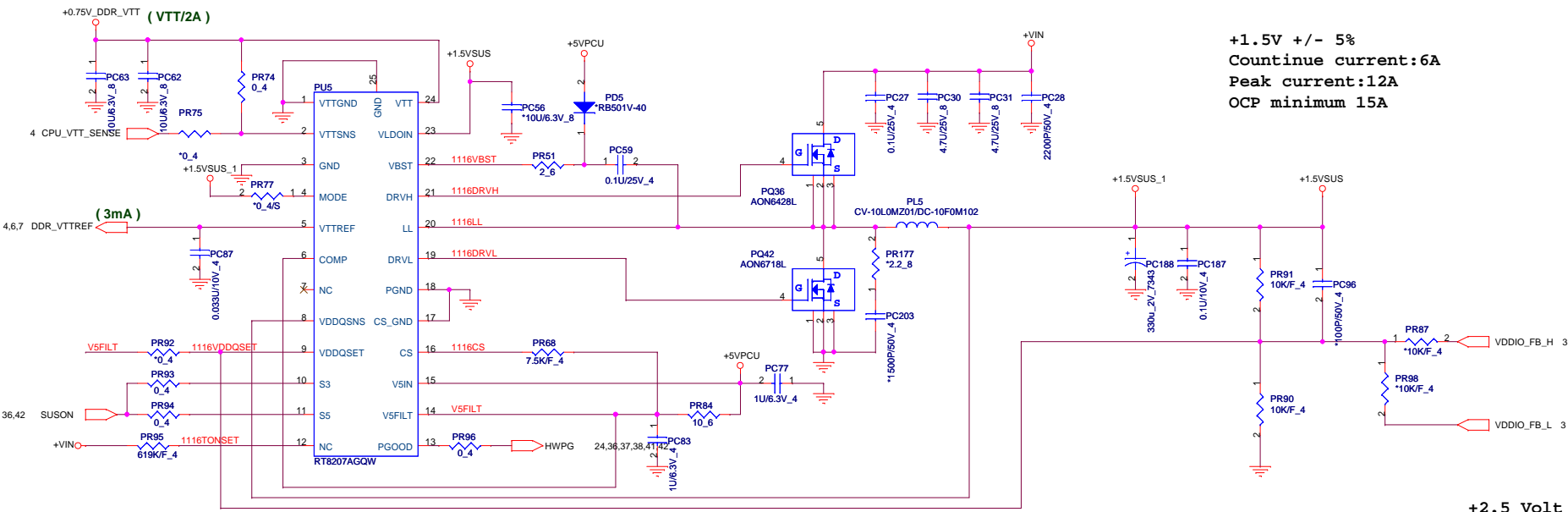
ISL6265 Pin1	OFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

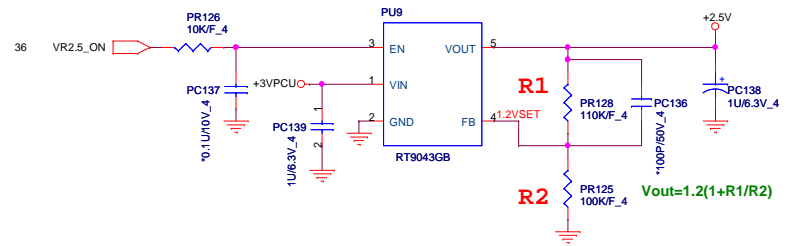


+VCORE Volt +/- 5%
 Countinue current:35A
 Peak current: 40A
 OCP minimum: 45A

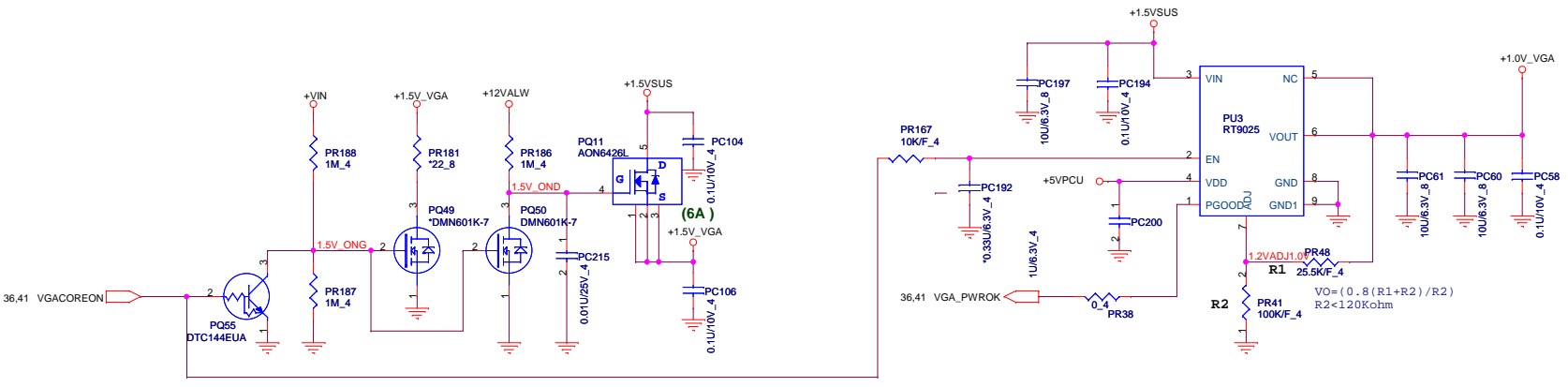


+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A


+2.5 Volt +/- 5%
Countinue current: 200mA
Peak current: 600mA

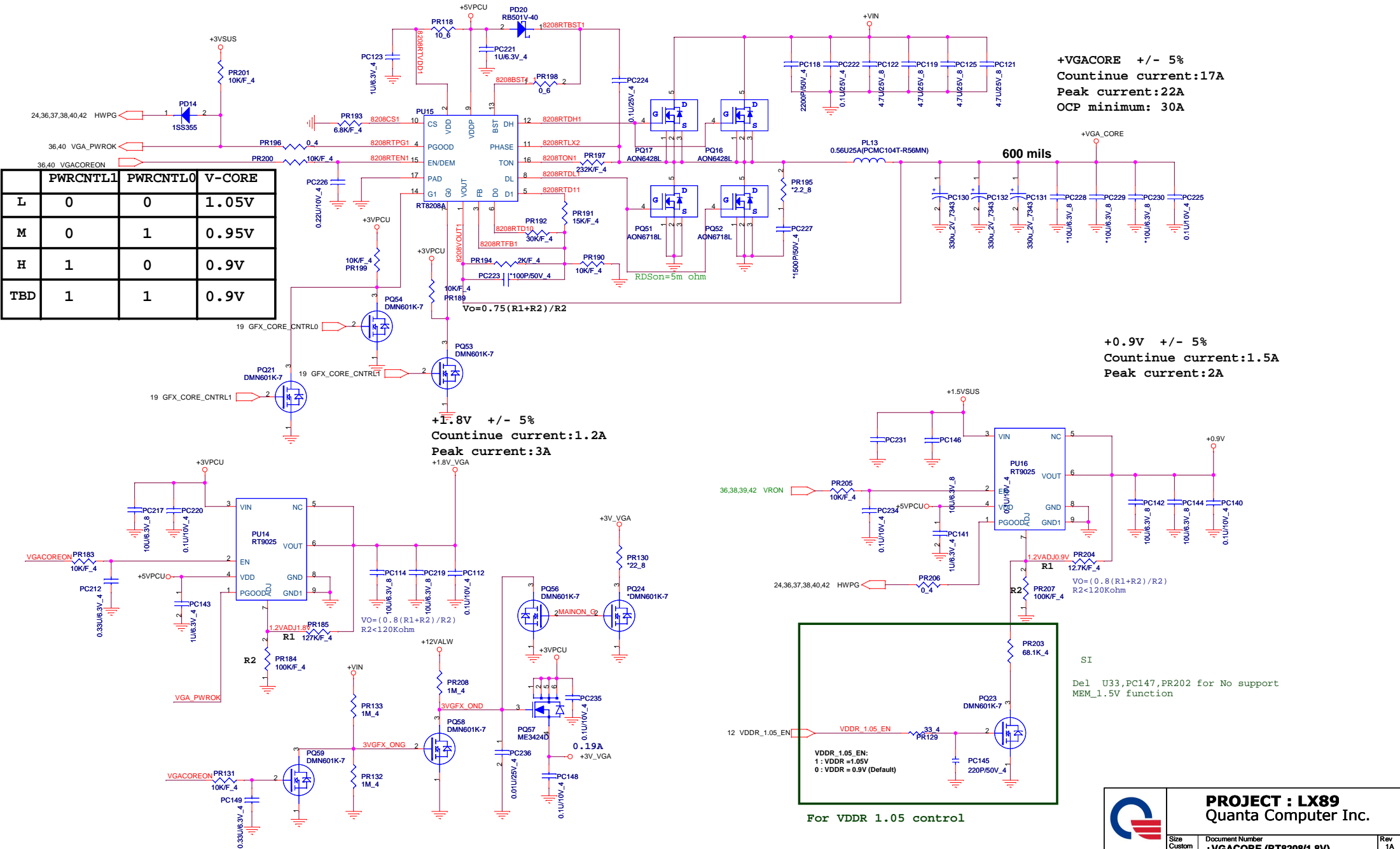


+1.0V +/- 5%
Countinue current:1.5A
Peak current:3A



$V_O = (0.8 \cdot (R1 + R2) / R2)$
 $R2 < 120k\text{ohm}$

 NBS/RD2	PROJECT : LX89 Quanta Computer Inc.	
	Document Number DDR3 (RT8207)	Rev 1A
Date: Monday, September 28, 2009 Sheet 40 of 46		

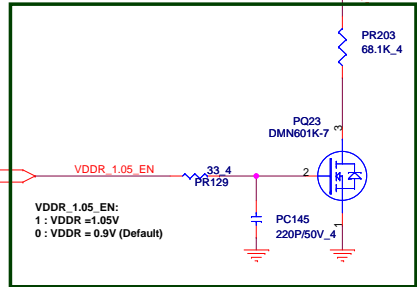


	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	1.05V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.9V

+VGACORE +/- 5%
 Countinue current:17A
 Peak current:22A
 OCP minimum: 30A

+0.9V +/- 5%
 Countinue current:1.5A
 Peak current:2A

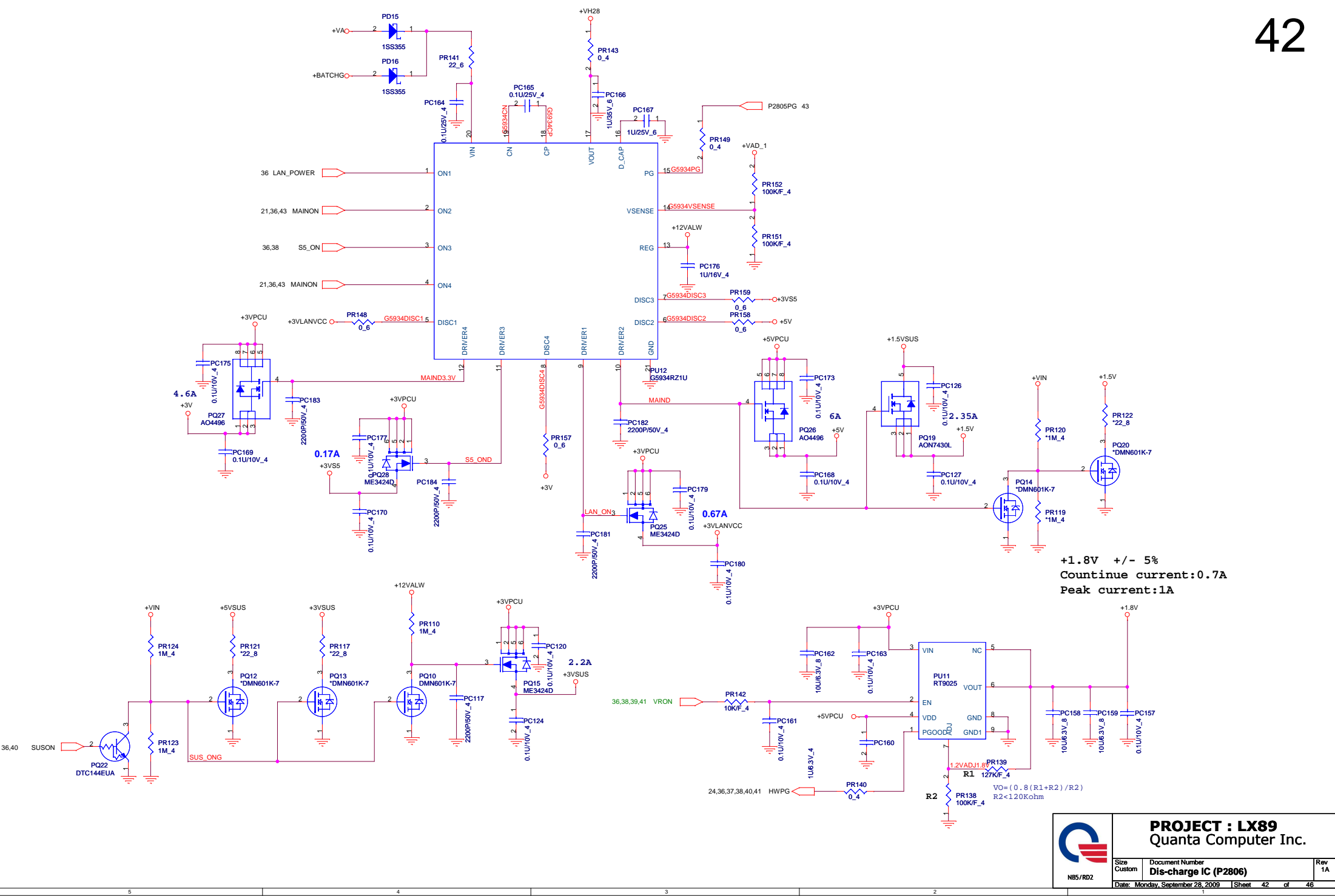
+1.8V +/- 5%
 Countinue current:1.2A
 Peak current:3A




For VDDR 1.05 control

SI
 Del U33,PC147,PR202 for No support
 MEM_1.5V function

	PROJECT : LX89	
	Quanta Computer Inc.	
	Size Custom	Document Number +VGACORE (RT8208/1.8V)
Date: Monday, September 28, 2009 Sheet 41 of 46		

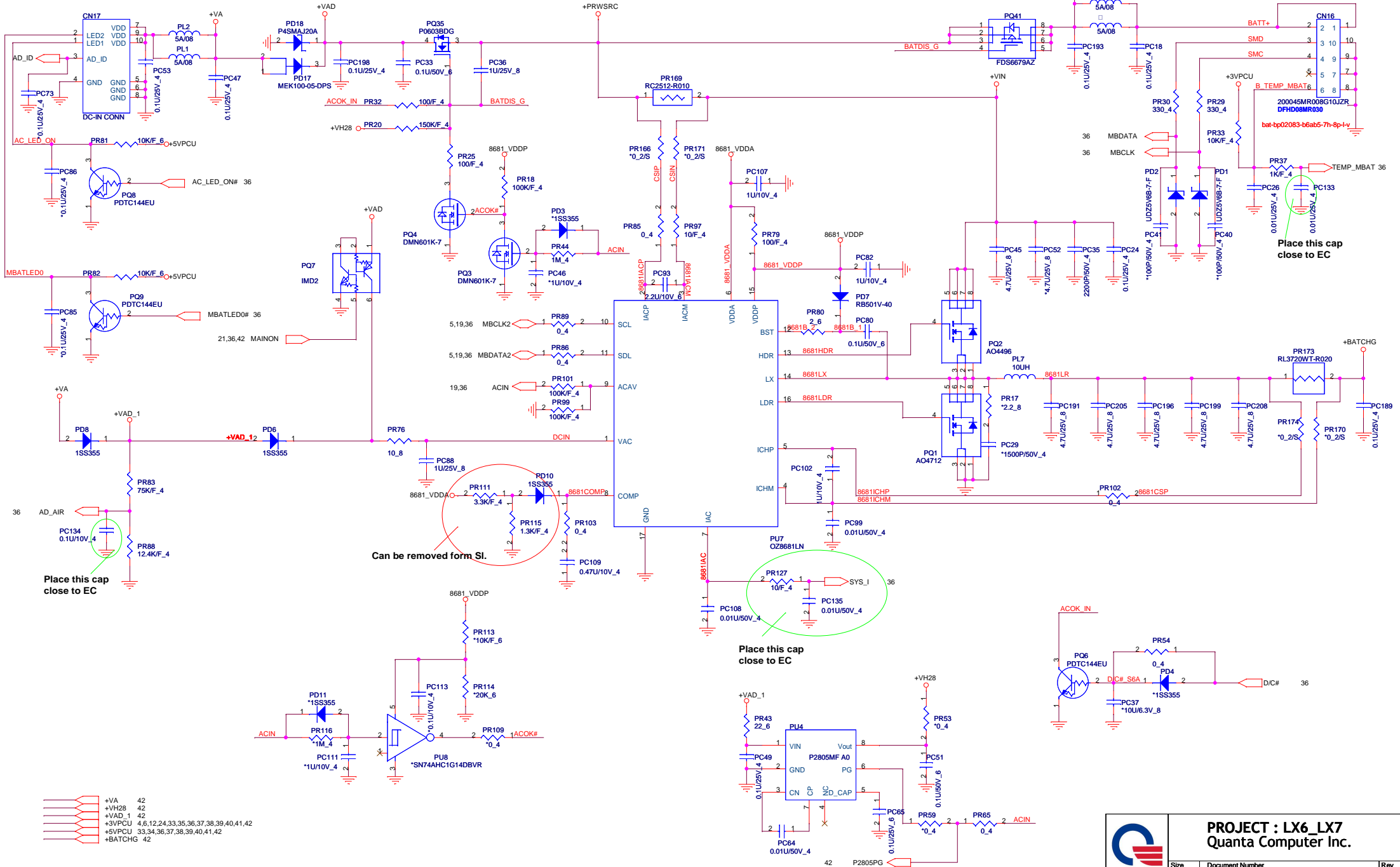


+1.8V +/- 5%
Countinue current:0.7A
Peak current:1A

 PROJECT : LX89 Quanta Computer Inc.		
Size Custom	Document Number Dis-charge IC (P2806)	Rev 1A
Date: Monday, September 28, 2009 Sheet 42 of 46		

TOP DC JACK
65W/90W

20346-100n-1-10p-1dv




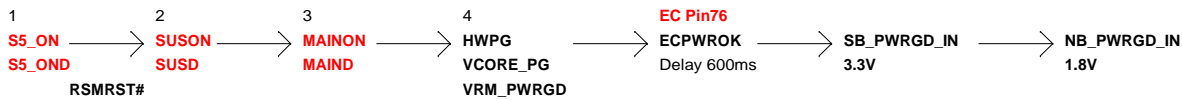
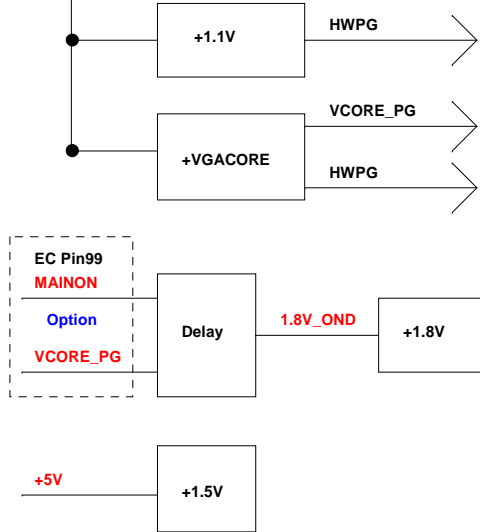
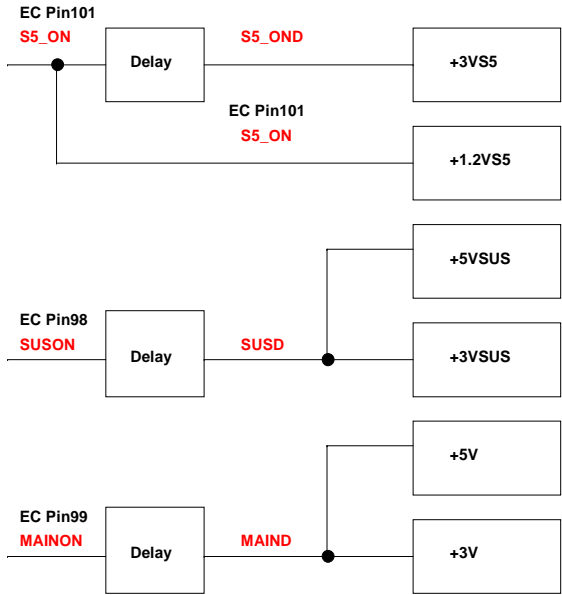
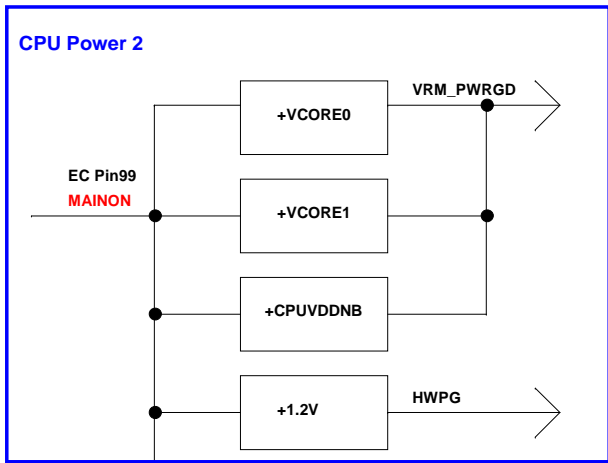
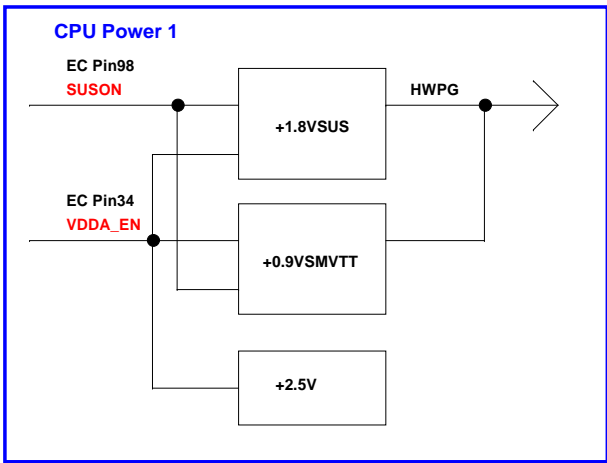
- +VA 42
- +VH28 42
- +VAD_1 42
- +3VPCU 4.6,12,24,33,35,36,37,38,39,40,41,42
- +5VPCU 33,34,36,37,38,39,40,41,42
- +BATCHG 42

Place this cap close to EC

Can be removed from SI.

Place this cap close to EC

 NB5	PROJECT : LX6_LX7		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number Charger (BQ24704)	



Power & Ground

Label	ACTIVE	Description	Control Signal
+VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
+3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+3V	S0		MAINON
+3VSUS	S0, S3		SUSON
+3VS5	S0, S3, S4, S5		S5_ON
+3VLAVCC	S0		LAN_POWER
+5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+5V	S0		MAINON
+5V_VCC1			
+5VALW			
+10VALW			
+15VALW			
+1.8V	S0		+1.5_ON
+1.8VSUS	S0, S3		
+1.5V	S0		MAINON
+1.5VSUS	S0, S3	DDR CORE POWER	SUSON
+1.5VSUS_1			
+1.5V_VGA	S0	VGA , VRAM POWER	+1.5_ON
+1.2V	S0		VRON
+1.2VSUS	S0, S3		SUSON
+1.1V	S0	VDDPCIE - PCIE-E MAIN POWER	VRON
+1.1VS5	S0, S3, S4, S5	STANDBY POWER	S5_ON
+1.1V_DYN	S0	NB VDDC - CORE LOGIC POWER	DYN_PWR_EN
+1.05V	S0	HT POWER (1.05V)	VRON
+1.0V_VGA	S0	PARK DPX_VDD10 POWER	VRON
+2.5V	S0	CPU VDDA POWER	VR2.5_ON
+VCORE0	S0	CPU CORE POWER (?V)	VRON
+VCORE1	S0	CPU CORE POWER (?V)	VRON
+CPUVDDNB	S0	CPU VDDNB POWER	VRON
+0.75_DDR_VTT	S0	DDR COMMAND & CONTROL PULL UP POWER	SUSON
DDR_VTTREF	S0, S3	DDR REFERENCE POWER	SUSON
+VGA_CORE	S0	VGA CORE POWER	MAINON
+AVBAT	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	

SMBUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR		
DDR3		
CPU THERMAL SENSOR		
CHARGER		

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT

www.s-manuals.com