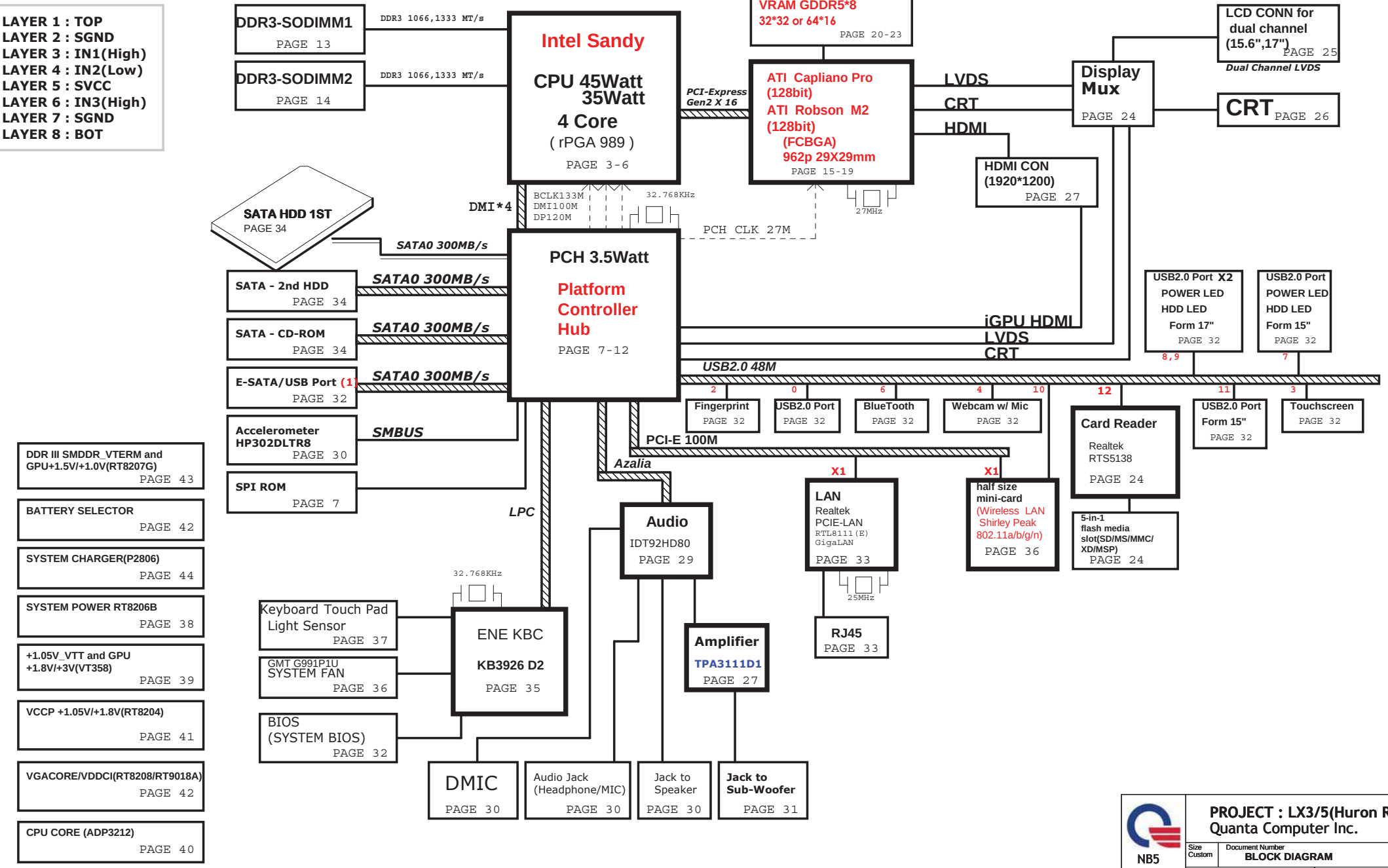
LX3/5 (Huron River) BLOCK DIAGRAM

01

Dis.

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND
LAYER 8 : BOT



PROJECT : LX3/5(Huron River)	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: BLOCK DIAGRAM; Rev: 1A
	Date: Friday, October 01, 2010; Sheet 1 of 47

4/7 DB del for PDC update.

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen(9LRS3197)/HOLES	1A

Date: Friday, October 01, 2010 Sheet 2 of 47

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

03

U31A

DMI

Intel(R) FDI

eDP

PCI EXPRESS* - GRAPHICS

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

SNB_IVB# N.A at SNB EDS #27637 0.7v1

Placement close to EC.

U31B

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

3/26 DB for H/W modify.

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU XDP

3/26 DB del for DG update.

8/16 PV Modify

CPU_RESET#

4/20 DB add.

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

SM_DRAMPWROK Processor Input.

8/6 PV NA.

3/26 DB del for DG update.

6/4 DB2 Modify.

10/13 MV Modify.

DDR3 DRAM RESET

+1.05V_VTT [5,11,39,40]
+1.5V_CPU [5]
+3VS5 [7,8,9,10,11,45]
+3V [7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]

FDI disable (DIS only stuff)

8/17: PV Modify.

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

PEG x16 disable (UMA only remove)

0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

Embedded Display PLL Clock

8/17: PV Modify.

3/26 DB change Part reference.

	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)

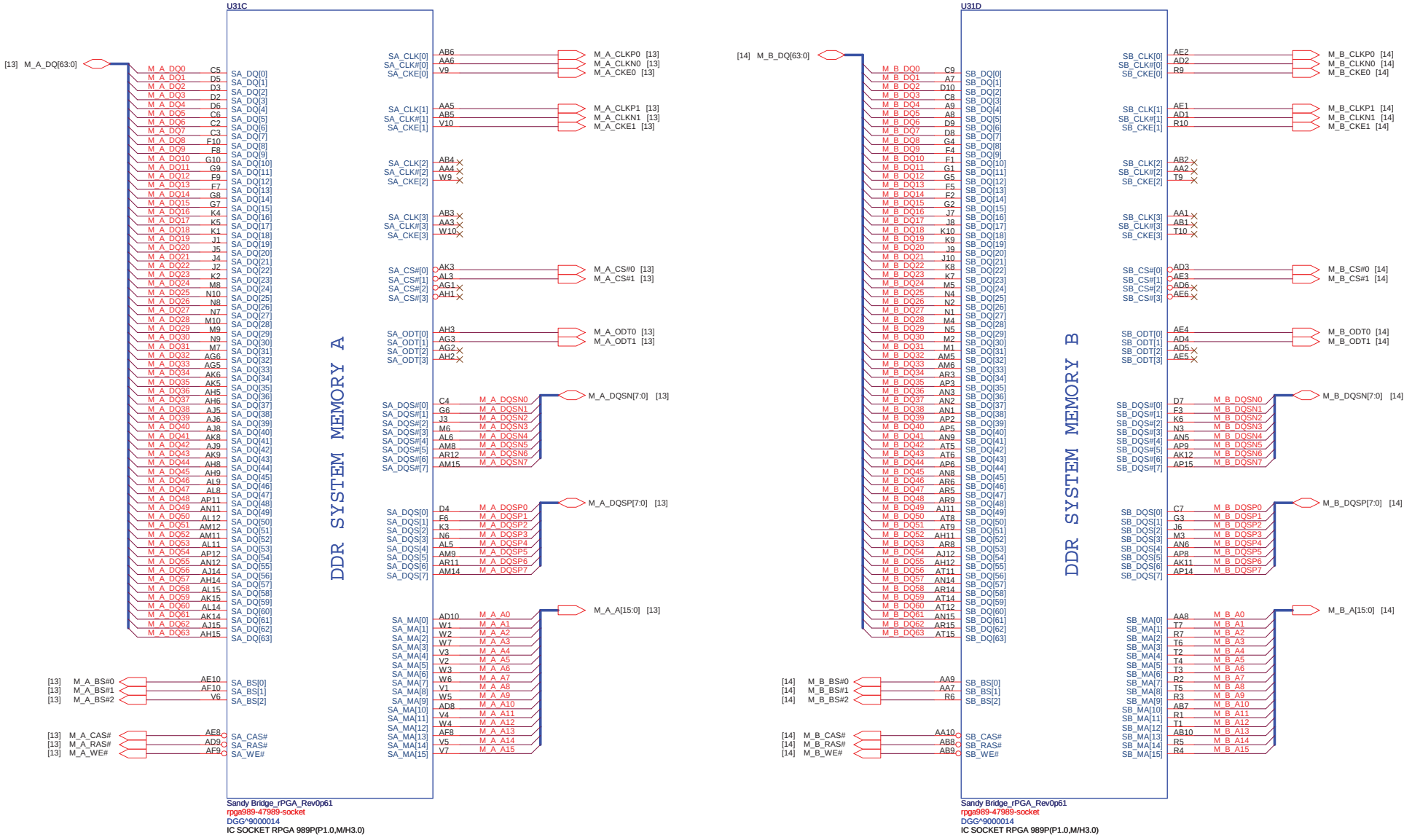
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

Date: Wednesday, October 13, 2010 | Sheet 3 of 47

Sandy Bridge Processor (DDR3)



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

Date: Wednesday, October 13, 2010 Sheet 4 of 47

Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

9/29 MV for Power Modify.

05

SNB: 55A

+VCC_CORE

U31F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SNB: 8.5A

+1.05V_VTT

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

5/4: add C8260/ C8322

8/17: PV Modify

	DIS	SG/UMA
Ra	Stuff	NC

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

3/26 DB change 10U FP to 0805.

3/26 DB Modify.

Trace Route to Power IC area.

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

+VCC_CORE [40]
+VCC_GFX [40]
+VCCSA [41]
+1.05V_VTT [3,11,39,40]
+1.5V_CPU [3]
+1.5V_CPU [3]
+1.5VSUS [3,11,13,14,43,45]

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

9/26: MV Modify

SNB: 21.5A

+VCC_GFX

U31G

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

SNB: 1.5A

+1.8V

330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge.

3/26 DB change 10U FP to 0805.

6/7 DB2 Modify

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGQ^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

3/26 DB Modify.

	DIS	SG/UMA
R130	NC	Stuff

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

5/14 modify

SNB: 5A

+1.5V_CPU

4/27: layout modify

5/23: na

330uF x1, 10uF_8 x6 Socket BOT edge.

3/26 DB change 10U FP to 0805.

SNB: 6A

+VCCSA

330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

3/26 DB change 10U FP to 0805.

5/11: Add for intel CRB

5/13: modify 40mile routing

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

Place PU resistor close to VR

3/26 DB Modify.

SVID DATA

Place PU resistor close to CPU

Place PU resistor close to VR

4/27: layout modify

5/12: modify

Place PU resistor close to CPU

SVID ALERT

10/01: modify

3/26 DB Modify.

+1.5VSUS

JP1 *SOLDERJUMPER-2

Q39 AON7410

3/26 DB add for Intel. Placement close to CPU.

5/6: modify

CPU VDDQ

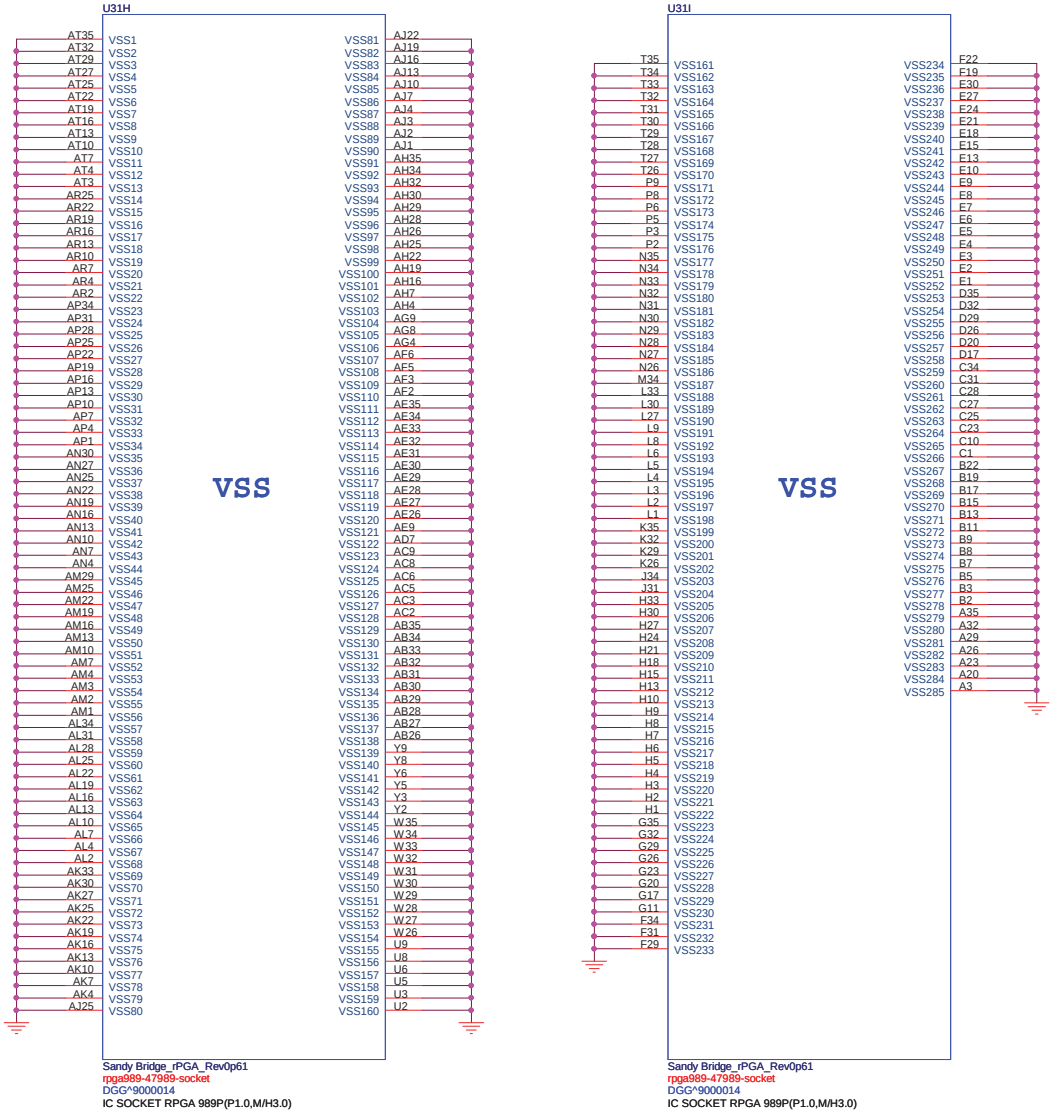
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

NB5

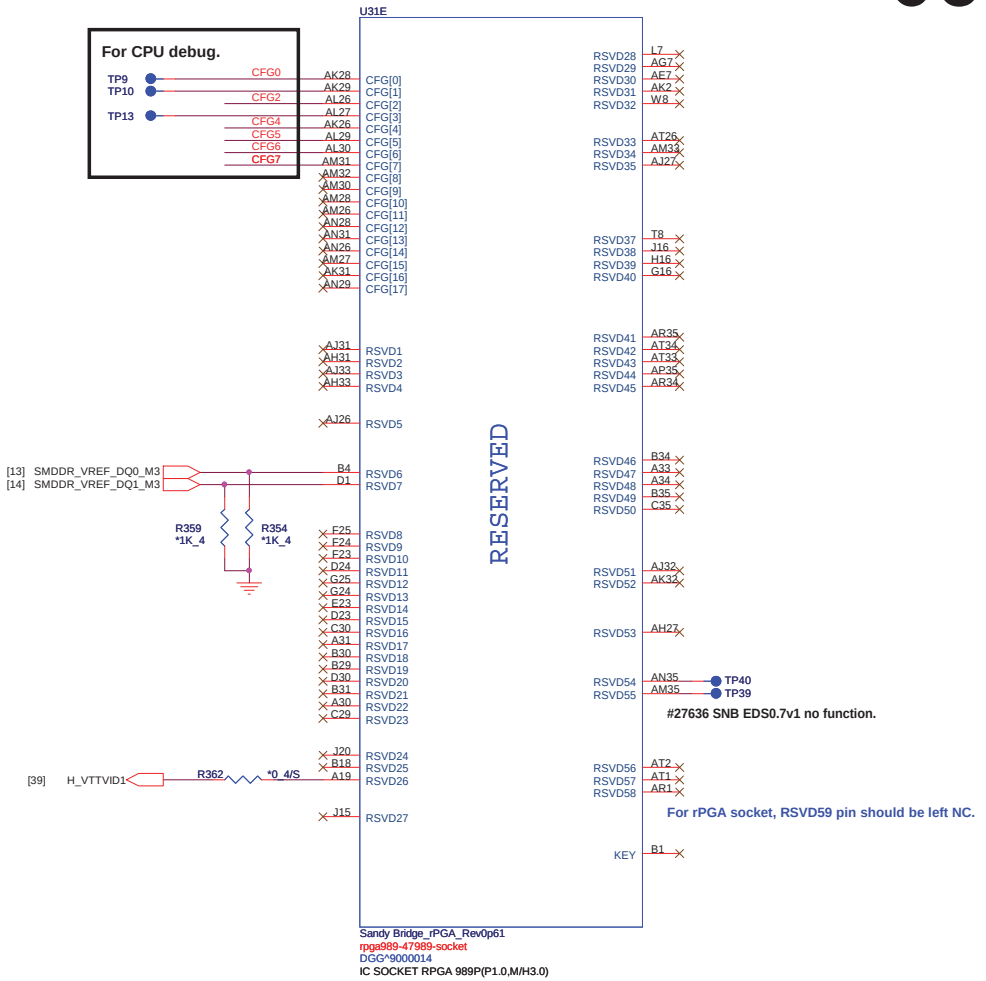
Size	Document Number	Rev
Custom	SNB 3/4 (POWER)	1A

Date: Wednesday, October 13, 2010 Sheet 5 of 47

Sandy Bridge Processor (GND)



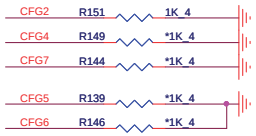
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	1A

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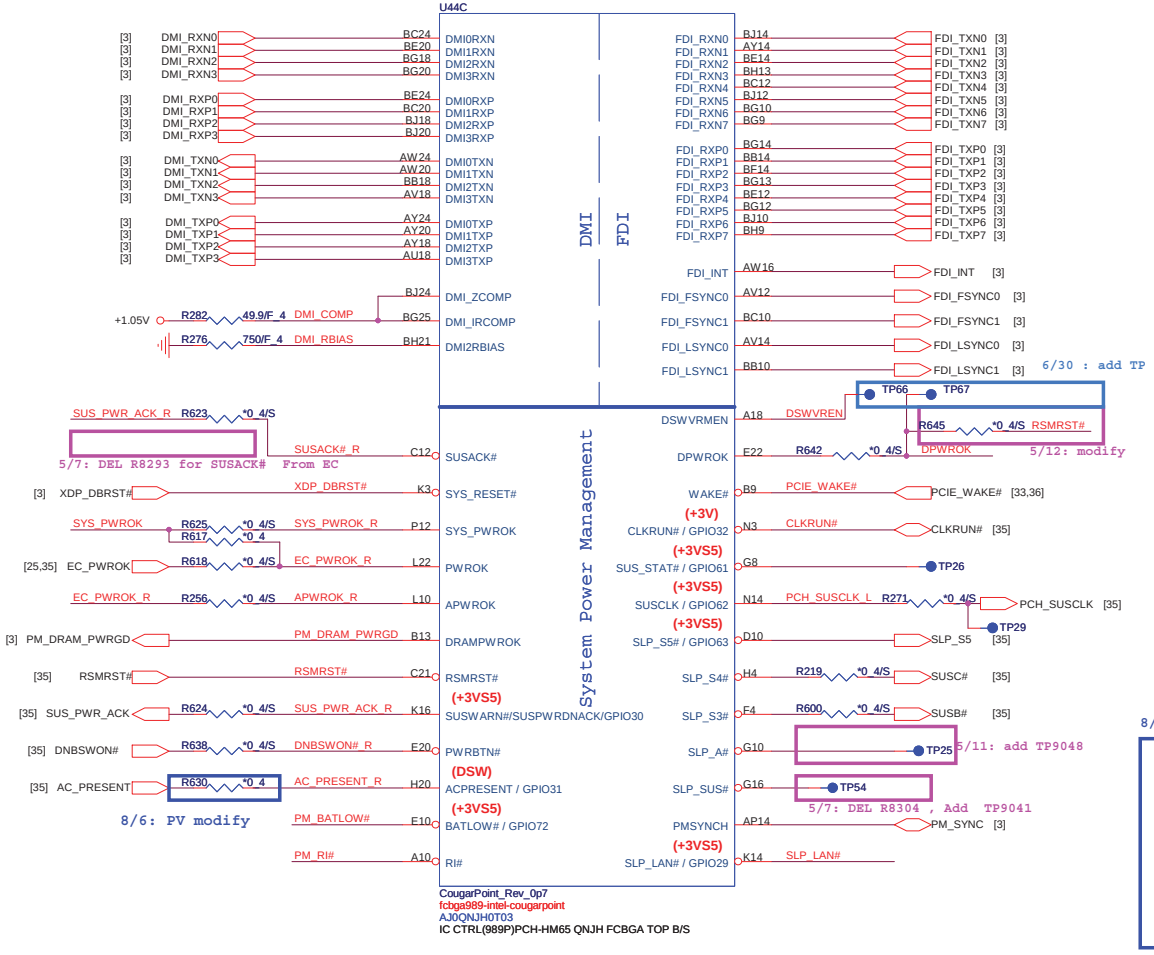
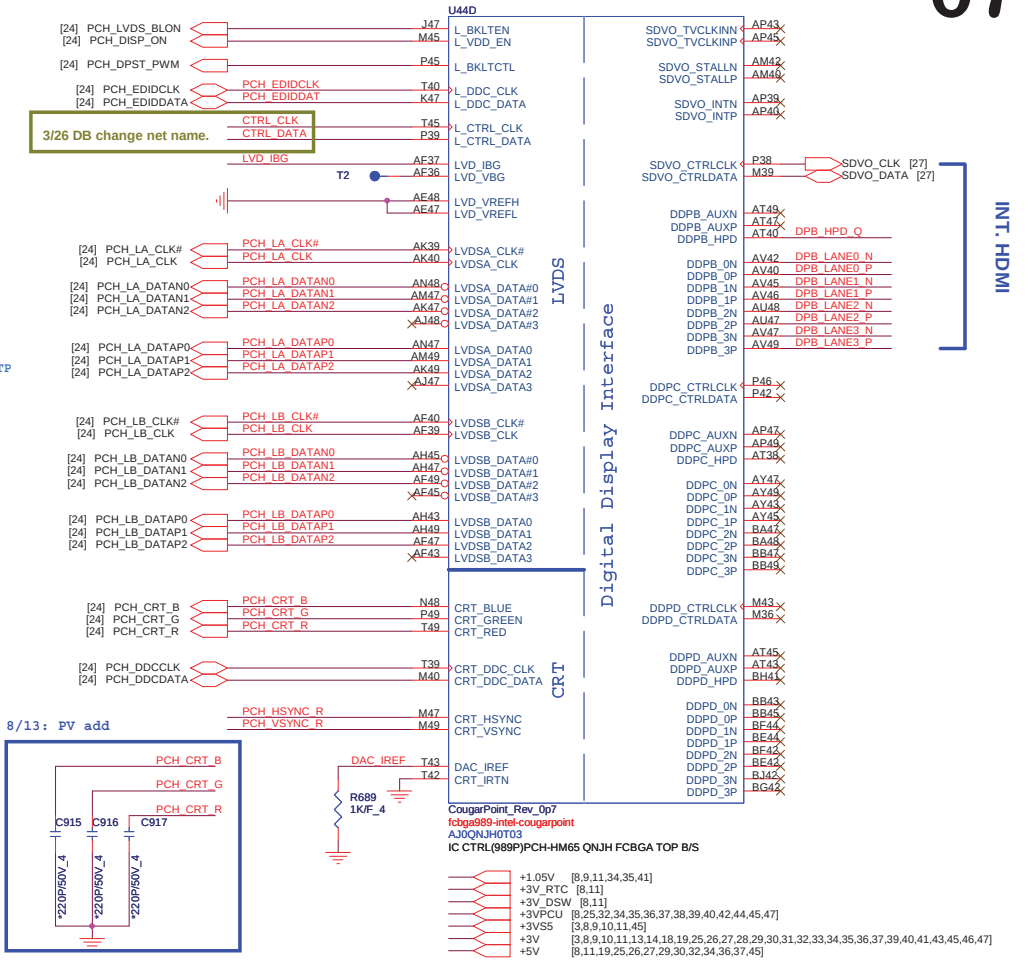
Cougar Point (DMI,FDI,PM)

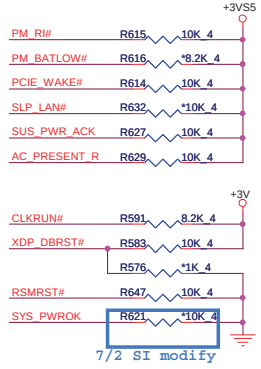


Cougar Point (LVDS,DDI)

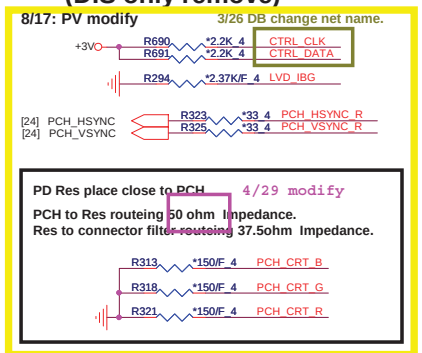


07

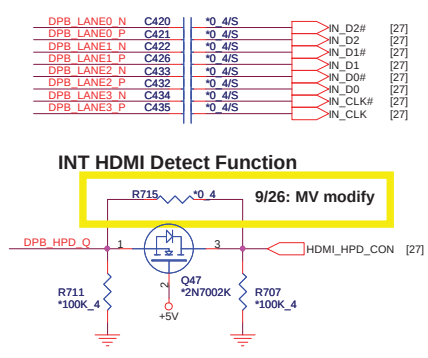
PCH Pull-high/low(CLG)



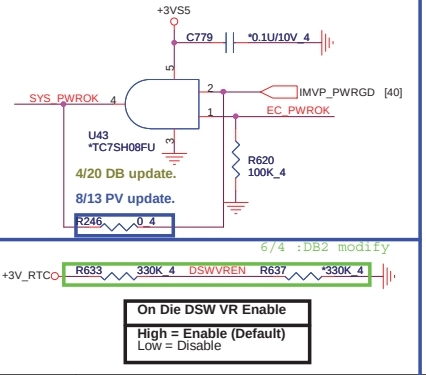
INT LVDS & CRT disable (DIS only remove)



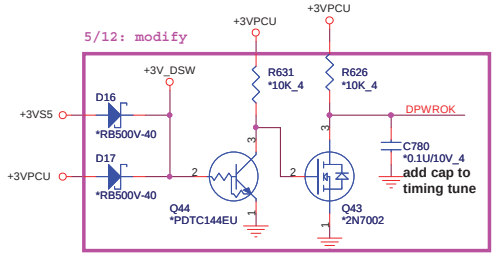
INT HDMI disable (DIS only remove)



System PWR_OK(CLG)



DPWROK FOR DSW

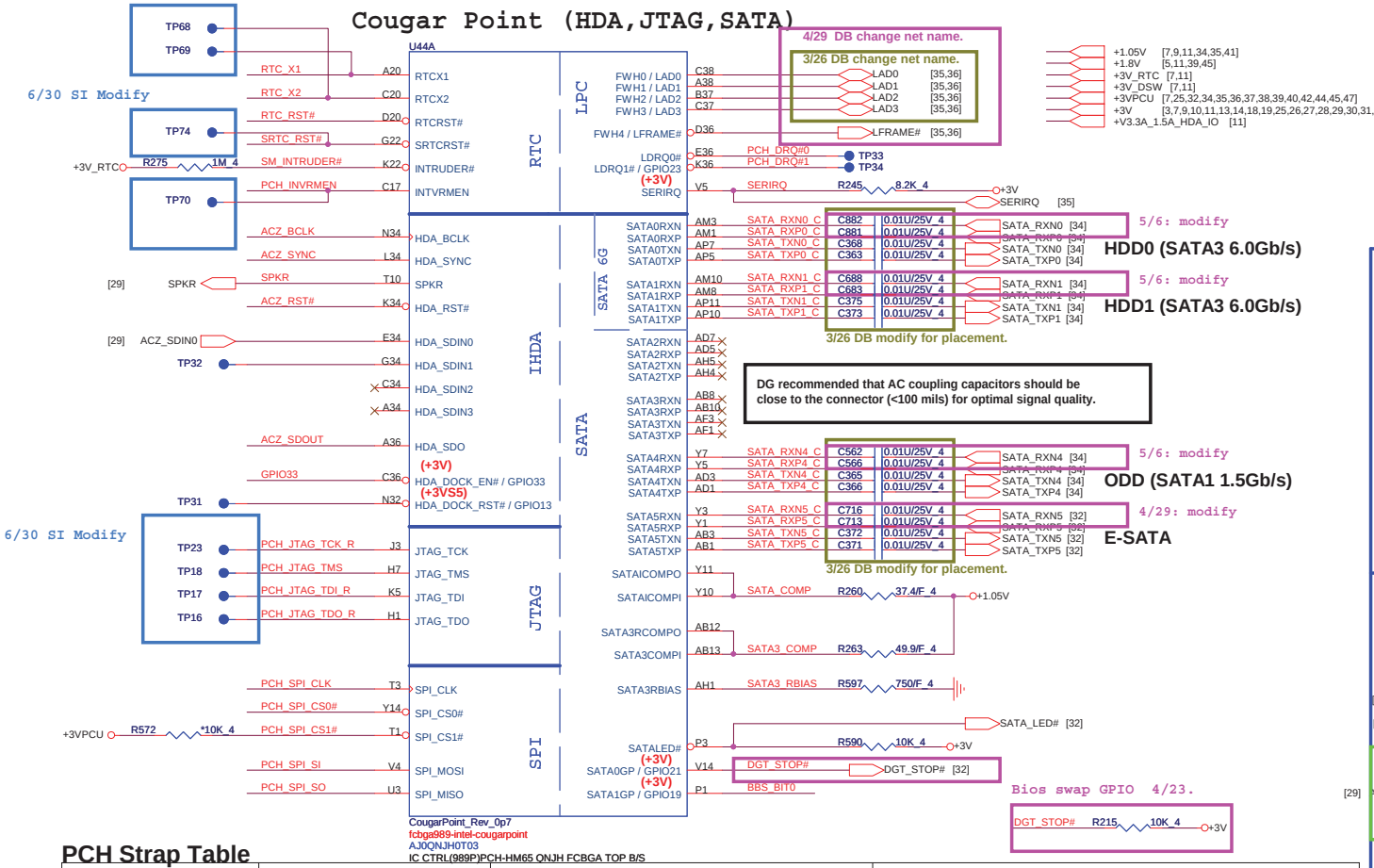


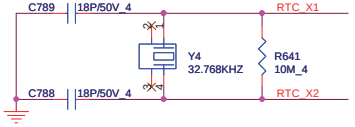
NB5

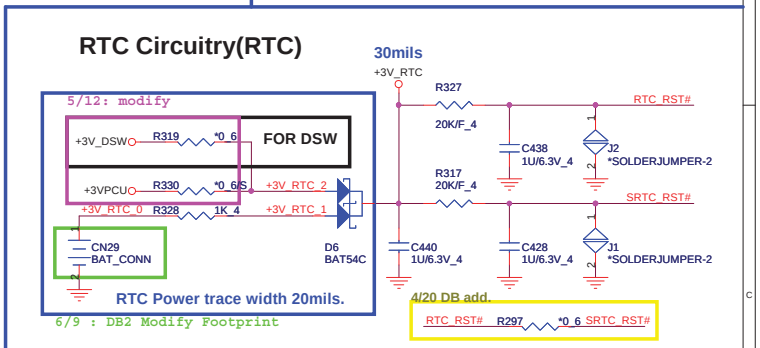
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

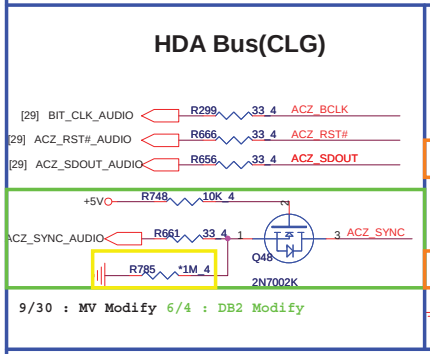
Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Wednesday, October 13, 2010	Sheet 7 of 47	

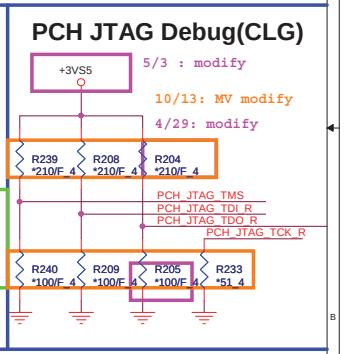
Cougar Point (HDA,JTAG,SATA)

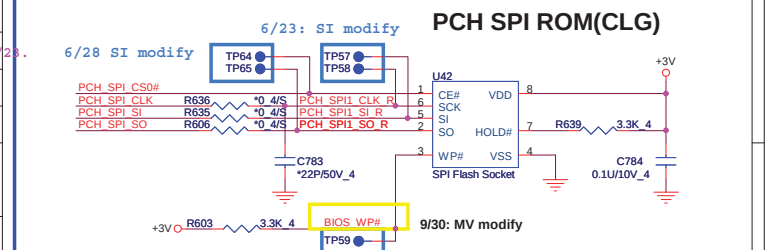












Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R568 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R687 *1K_4, R700 10K_4, PCI_GNT3# [9], Bios request, for can't boot Capella 4/28.
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R640 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R659 0_4 BIOS_WP# 9/30: MV modify
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1, GNT0# 1 → Boot Location SPI	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# 1, GNT0# 0 → Boot Location LPC	R573 *1K_4, R686 *1K_4, BBS_BIT0, BBS_BIT1 [9]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R596 *1K_4 NV_ALE [9]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 modify	+1.8V R595 2.2K_4, R609 4.7K_4, NV_CLE [9], H_SNB_IVB# [3] N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R307 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[35] GPIO33_E ACZ_SDOUT R662 *1K_4 +V3.3A_1.5A_HDA_IO 8/12 PV Modify.
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R619 *1K_4 ICC_EN# [10] 4/29 reserve.
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R608 *1K_4 PLL_ODVR_EN [10]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R634 1K_4 +3V

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNJH0T03
IC CTRL(989P)PCH-HM65 QNJH FCBGA TOP B/S

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A

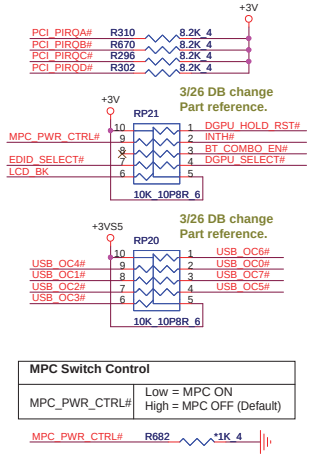
Date: Wednesday, October 13, 2010 | Sheet 8 of 47

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

09

PCI/USBOC# Pull-up(CLG)



MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R682 *1K_4

PCIE

PIRQA# K40
PIRQB# K38
PIRQC# H38
PIRQD# G38
BT_COMBO_EN# C46
DGPU_SELECT# C44
EDID_SELECT# E40
REQ1# / GPIO50 (+3V)
REQ2# / GPIO52 (+3V)
REQ3# / GPIO54 (+3V)
BBS_BIT1 D47
PWM_SELECT# E42
PCI_GNT3# F46
GNT1# / GPIO51 (+3V)
GNT2# / GPIO53 (+3V)
GNT3# / GPIO55 (+3V)
LCD_BK G42
DGPU_HOLD_RST# G40
INTH# C42
PIRQE# / GPIO2 (+3V)
PIRQF# / GPIO3 (+3V)
PIRQG# / GPIO4 (+3V)
PIRQH# / GPIO5 (+3V)
PME# K10
PCI_PLTRST# C6

Bios swap GPIO 4/23.

TP24 PCI_PME#

TP56 CLK_PCI_TPM_R H49
TP36 CLK_PCI_CARD_R H43
CLKOUT_PCI0 J48
CLKOUT_PCI1 K42
CLKOUT_PCI2 H40
CLKOUT_PCI3
CLKOUT_PCI4
CLK_33M_DEBUG R324 22_4
CLK_33M_KBC R316 22_4
CLK_PCI_FB R315 22_4
CLK_PCI_FB_R
CLK_PCI_LPC_R
CLK_PCI_EC_R

USB

USBP0- [32] Left_USB
USBP0+ [32] E-Sata
USBP1- [32] Fingerprin
USBP1+ [32] Touchscreen
USBP2- [32] Webcam
USBP2+ [32]
USBP3- [32]
USBP3+ [32] Right_USB 17"
USBP4- [25] Right_USB 15"
USBP4+ [25] WLAN
USBP8- [32] Right_USB 15"
USBP8+ [32] Card Reaer
USBP9- [32] Blue tooth
USBP9+ [32]
USBP10- [36]
USBP10+ [36]
USBP11- [32]
USBP11+ [32]
USBP5- [28]
USBP5+ [28]
USBP6- [32]
USBP6+ [32]

3/26 DB change from Port5 & Port6 to Port12 & Port13 for DF PCH.

USB_BIAS
R654 22.6/F_4
USBRBIAS#
USBRBIAS

OC0# / GPIO59 (+3V5) USB_OC0#
OC1# / GPIO40 (+3V5) USB_OC1#
OC2# / GPIO41 (+3V5) USB_OC2#
OC3# / GPIO42 (+3V5) USB_OC3#
OC4# / GPIO43 (+3V5) USB_OC4#
OC5# / GPIO9 (+3V5) USB_OC5#
OC6# / GPIO10 (+3V5) USB_OC6#
OC7# / GPIO14 (+3V5) USB_OC7#

NVRAM

NV_CE#0 AY7
NV_CE#1 AV7
NV_CE#2 AU3
NV_CE#3 BG4
NV_DQS0 AT10
NV_DQS1 BC8
NV_DQ0 / NV_IO0 AU2
NV_DQ1 / NV_IO1 AT4
NV_DQ2 / NV_IO2 AT3
NV_DQ3 / NV_IO3 AT1
NV_DQ4 / NV_IO4 AY3
NV_DQ5 / NV_IO5 AT5
NV_DQ6 / NV_IO6 AV3
NV_DQ7 / NV_IO7 AV1
NV_DQ8 / NV_IO8 BB1
NV_DQ9 / NV_IO9 BA3
NV_DQ10 / NV_IO10 BB5
NV_DQ11 / NV_IO11 BB3
NV_DQ12 / NV_IO12 BB7
NV_DQ13 / NV_IO13 BE8
NV_DQ14 / NV_IO14 BD4
NV_DQ15 / NV_IO15 BF6
NV_ALE AV5 NV_ALE [8]
NV_CLE AY1 NV_CLE [8]
NV_RCOMP AV10
NV_RB# AT8
NV_RE#_WRB0 AY5
NV_RE#_WRB1 BA2
NV_WE#_CK0 AT12
NV_WE#_CK1 BF3

RSVD

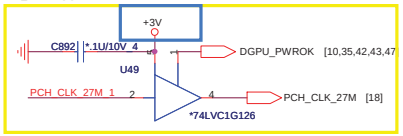
TP1 BG26
TP2 BJ26
TP3 BH25
TP4 BJ16
TP5 BG16
TP6 AH38
TP7 AH37
TP8 AK43
TP9 AK45
TP10 C18
TP11 N30
TP12 C_H3
TP13 AH12
TP14 AM4
TP15 AM5
TP16 Y13
TP17 K24
TP18 L24
TP19 AB46
TP20 AB45
TP21 B21
TP22 M20
TP23 AY16
TP24 BG46
TP25 BE28
TP26 BC30
TP27 BE32
TP28 BJ32
TP29 BC28
TP30 BE30
TP31 BF32
TP32 BG32
TP33 AV26
TP34 BB26
TP35 AU28
TP36 AY30
TP37 AU26
TP38 AY26
TP39 AV28
TP40 AW30

WLAN / LAN

WLAN
[36] PCIE_RXN1 BG34
[36] PCIE_RXP1 BJ34
[36] PCIE_TXN1 C414 0.1U/10V_4 PCIE_TXN1_C AV32
[36] PCIE_TXP1 C410 0.1U/10V_4 PCIE_TXP1_C AU32

LAN
[33] PCIE_RXN2_LAN BE34
[33] PCIE_RXP2_LAN BE34
[33] PCIE_TXN2_LAN C418 0.1U/10V_4 PCIE_TXN2_LAN_C BB32
[33] PCIE_TXP2_LAN C419 0.1U/10V_4 PCIE_TXP2_LAN_C AY32

5/13: add for leakage
7/2 : Modify +3v
9/26: MV modify



PCI-E*

PERN1 BG34
PERP1 BJ34
PETN1 AV32
PETP1 AU32
PERN2 BE34
PERP2 BE34
PETN2 BB32
PETP2 AY32
PERN3 BG36
PERP3 BJ36
PETN3 AV34
PETP3 AU34
PERN4 BE36
PERP4 BE36
PETN4 AY34
PETP4 BB34
PERN5 BG37
PERP5 BH37
PETN5 AY36
PETP5 BB36
PERN6 BJ38
PERP6 BG38
PETN6 AU36
PETP6 AV36
PERN7 BG40
PERP7 BJ40
PETN7 AY40
PETP7 BB40
PERN8 BE38
PERP8 BC38
PETN8 AW38
PETP8 AY38

SMBUS

(+3VS5) SMBALERT# / GPIO11 E12 SMBALERT#
SMBCLK H14 SMB_PCH_CLK
SMBDATA C9 SMB_PCH_DAT
(+3VS5) SML0ALERT# / GPIO60 A12 DRAMRST_CNTRL_PCH DRAMRST_CNTRL_PCH [3]
SML0CLK C8 SMB_ME0_CLK
SML0DATA G12 SMB_ME0_DAT
(+3VS5) SML1ALERT# / PCHHOT# / GPIO74 C13 SML1ALERT# R TP28
(+3VS5) SML1CLK / GPIO58 E14 SMB_ME1_CLK
(+3VS5) SML1DATA / GPIO75 M16 SMB_ME1_DAT

Controller Link

CL_CLK1 M7 CL_CLK_R TP19
CL_DATA1 T11 CL_DAT_R TP21
CL_RST1# P10 CL_RST#_R TP20

CLOCKS

CLK_PCH_SRC0N Y40
CLK_PCH_SRC0P Y39
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLK_PCIE_REQ0# J2
PCIECLKRQ0# / GPIO73
(+3VS5)
CLK_PCH_SRC2N AB49
CLK_PCH_SRC2P AB47
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLK_PCIE_REQ1# M1
PCIECLKRQ1# / GPIO18
(+3V)
CLKOUT_PCIE2N AA48
CLKOUT_PCIE2P AA47
CLK_PCIE_REQ2# V10
PCIECLKRQ2# / GPIO20
(+3V)
CLKOUT_PCIE3N Y37
CLKOUT_PCIE3P Y36
CLK_PCIE_REQ3# A8
PCIECLKRQ3# / GPIO25
(+3VS5)
CLKOUT_PCIE4N Y43
CLKOUT_PCIE4P Y45
CLK_PCIE_REQ4# L12
PCIECLKRQ4# / GPIO26
(+3VS5)
CLKOUT_PCIE5N V45
CLKOUT_PCIE5P V46
PCIECLKRQ5# / GPIO44
(+3VS5)
CLKOUT_PEG_B_N AB42
CLKOUT_PEG_B_P AB40
PEG_B_CLKRQ# / GPIO56
(+3VS5)
CLKOUT_PCIE6N V40
CLKOUT_PCIE6P V42
PCIECLKRQ6# / GPIO45
(+3VS5)
CLKOUT_PCIE7N V38
CLKOUT_PCIE7P V37
PCIECLKRQ7# / GPIO46
(+3VS5)
CLKOUT_ITPXDP_N AK14
CLKOUT_ITPXDP_P AK13

Bios swap GPIO 4/23.
[10] BOARD_ID0 L14
TP22 CLK_PEGB_REQ# E6
[10] BOARD_ID1
[10] BOARD_ID2
TP30
TP27
CLK_PCH_ITPN
CLK_PCH_ITPP

(+3VS5) PEG_A_CLKRQ# / GPIO47 M10 CLK_PEGA_REQ#
CLKOUT_PEG_A_N AB37 CLK_PCH_PEGAN
CLKOUT_PEG_A_P AB38 CLK_PCH_PEGAP
CLKOUT_DMI_N AV22 CLK_CPU_BCLKN [3]
CLKOUT_DMI_P AU22 CLK_CPU_BCLKP [3]
CLKOUT_DP_N AM12 CLK_DPLL_SSCLKN [3]
CLKOUT_DP_P AM13 CLK_DPLL_SSCLKP [3]
CLKIN_DMI_N BF18 CLK_BUF_PCIE_3GPLL#
CLKIN_DMI_P BE18 CLK_BUF_PCIE_3GPLL
CLKIN_GND1_N BJ30 CLK_BUF_BCLK_N
CLKIN_GND1_P BG30 CLK_BUF_BCLK_P
CLKIN_DOT_96N G24 CLK_BUF_DREFCLK#
CLKIN_DOT_96P E24 CLK_BUF_DREFCLK
CLKIN_SATA_N AK7 CLK_BUF_DREFSSCLK#
CLKIN_SATA_P AK5 CLK_BUF_DREFSSCLK
REFCLK14IN K45 CLK_PCH_14M
CLKIN_PCILOOPBACK H45 CLK_PCI_FB

3/26 DB del external clock generator.

TP71
C830 18P/50V_4
Y5 25MHz
C829 18P/50V_4
TP72 +1.05V
XTAL25_IN V47
XTAL25_OUT V49
XCLK_RCOMP Y47 R688 90.9/F_4
CLK_FLEX0 TP35
4/29: remove CLK_27M_VGA
5/13: modify CLK_48M to CLK_FLEX1

FLEX CLOCKS

(+3V) CLKOUTFLEX0 / GPIO64 K43
(+3V) CLKOUTFLEX1 / GPIO65 F47 CLK_FLEX1
(+3V) CLKOUTFLEX2 / GPIO66 H47 CLK_FLEX2
(+3V) CLKOUTFLEX3 / GPIO67 K49 CLK_FLEX3

R304 22_4 CLK_48M_CR [28]
TP55
Rb R692 *22_4 PCH_CLK_27M_1

Remove Ra, Rb for UMA & SG.
27MHz support DIS only.

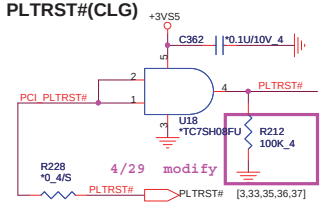
CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNJH0T03
IC CTRL(989P)PCH-HM65 QNJH FCBGA TOP B/S

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNJH0T03
IC CTRL(989P)PCH-HM65 QNJH FCBGA TOP B/S

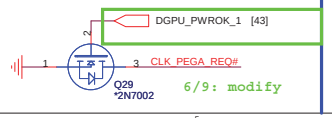
CLK_33M_DEBUG C897 *27P/50V_4 L63 *33nH/600mA_6
CLK_33M_KBC C898 *27P/50V_4 L64 *33nH/600mA_6

6/28: DB2 reserve

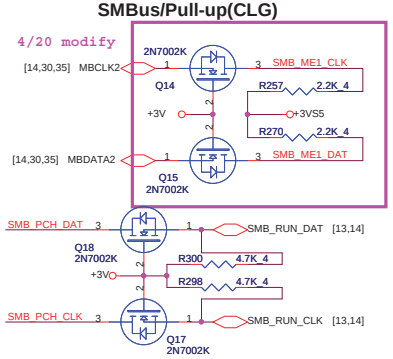
PLTRST#(CLG)



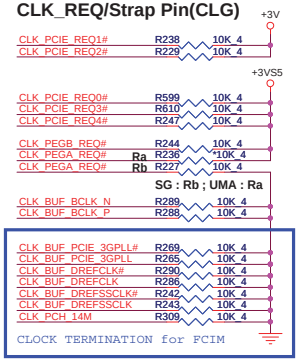
PEG Clock detect (SG only)



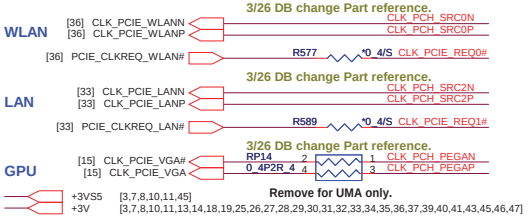
SMBus/Pull-up(CLG)



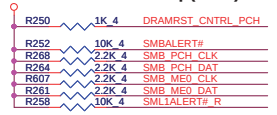
CLK_REQ/Strap Pin(CLG)



PCIE Clock



SMBus/Pull-up(CLG)



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (PCIE/USB/CLK)	1A
Date: Wednesday, October 13, 2010	Sheet 9 of 47	

Cougar Point (GPIO,VSS_NCTF,RSVD)

5/23: stuff for bios

Bios swap GPIO 4/23.

4/29 modify

9/26: MV Modify

Bios swap GPIO 4/23.

5/11 stuff R9144

DG rev0.9 suggest to TS_VSS connect to GND 4/23.

U44F

GPIO

CPU/MISC

NCTF

CougarPoint_Rev_0p7 IC CTRL(989P)PCH-HM65 QNJH FCBGA TOP B/S

fcbga989-intel-cougarpoint

AJ0QNJH0T03

+3VS5 [3,7,8,9,11,45]

+3V [3,7,8,9,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]

Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

MFG-TEST

Bios swap GPIO 4/23.

GPIO Pull-up/Pull-down(CLG)

4/29 modify

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)
High = Enable

BIOS RECOVERY | High = Disable (Default) Low = Enable

SV_SET_UP

High = Strong (Default)

TEST DETECT

Low = Default

DMI TERMINATION VOLTAGE OVERRIDE | Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

FDI TERMINATION VOLTAGE OVERRIDE | LOW - Tx, Rx terminated to same voltage

GFX Present

	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
LX3 UMA	0	0	0	0	0	0
LX5 UMA	0	0	0	0	0	1
LX3 Capilano XT - SG	0	0	0	0	1	0
LX5 Capilano XT - SG	0	0	0	0	1	1
LX3 Capilano XT - SG/Subwoofer	0	0	0	1	0	0
LX5 Capilano XT - SG/Subwoofer	0	0	0	1	0	1
LX3 DISCRETE Subwoofer	0	0	0	1	1	0
LX5 DISCRETE Subwoofer	0	0	0	1	1	1

4/29 modify

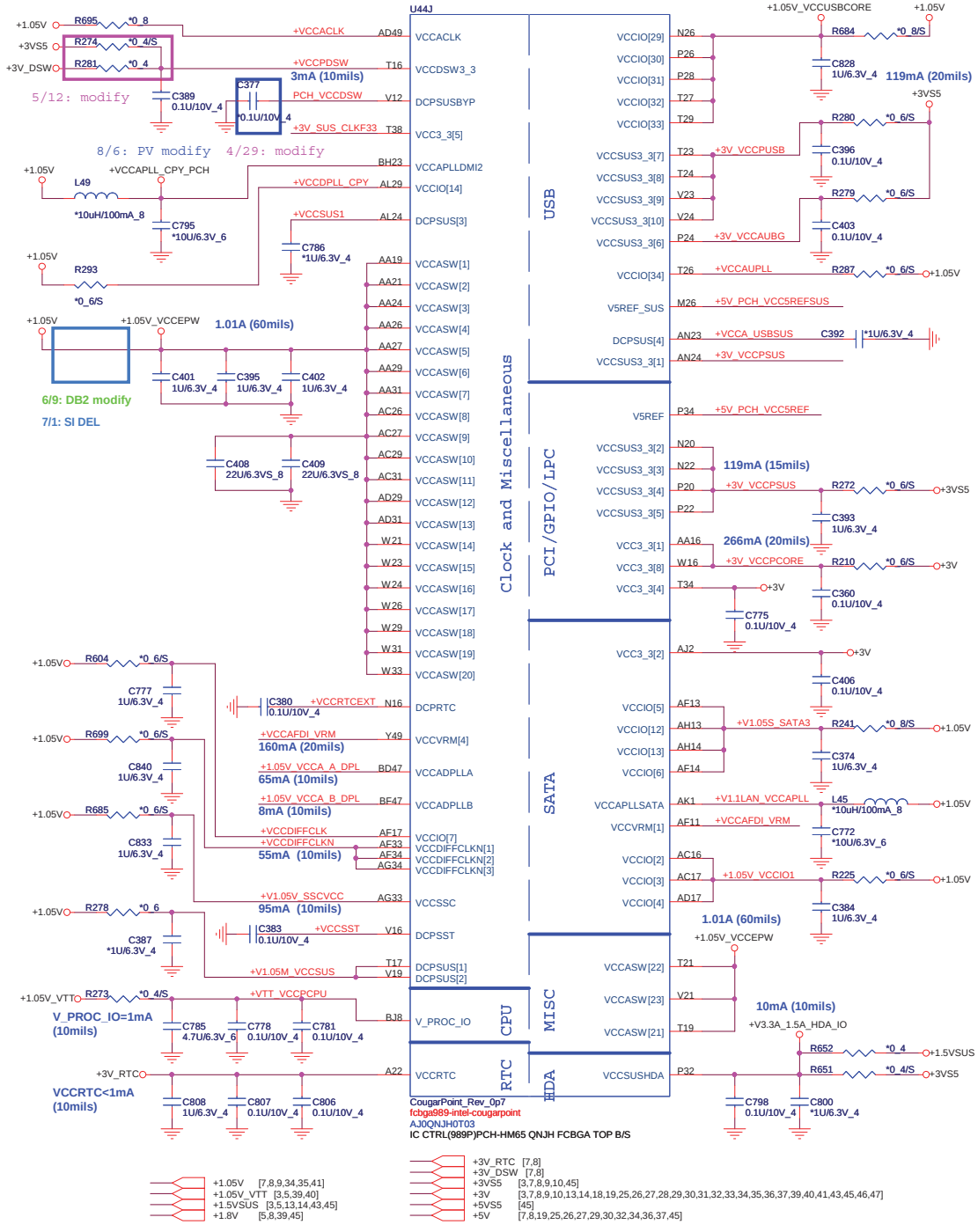
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

NB5

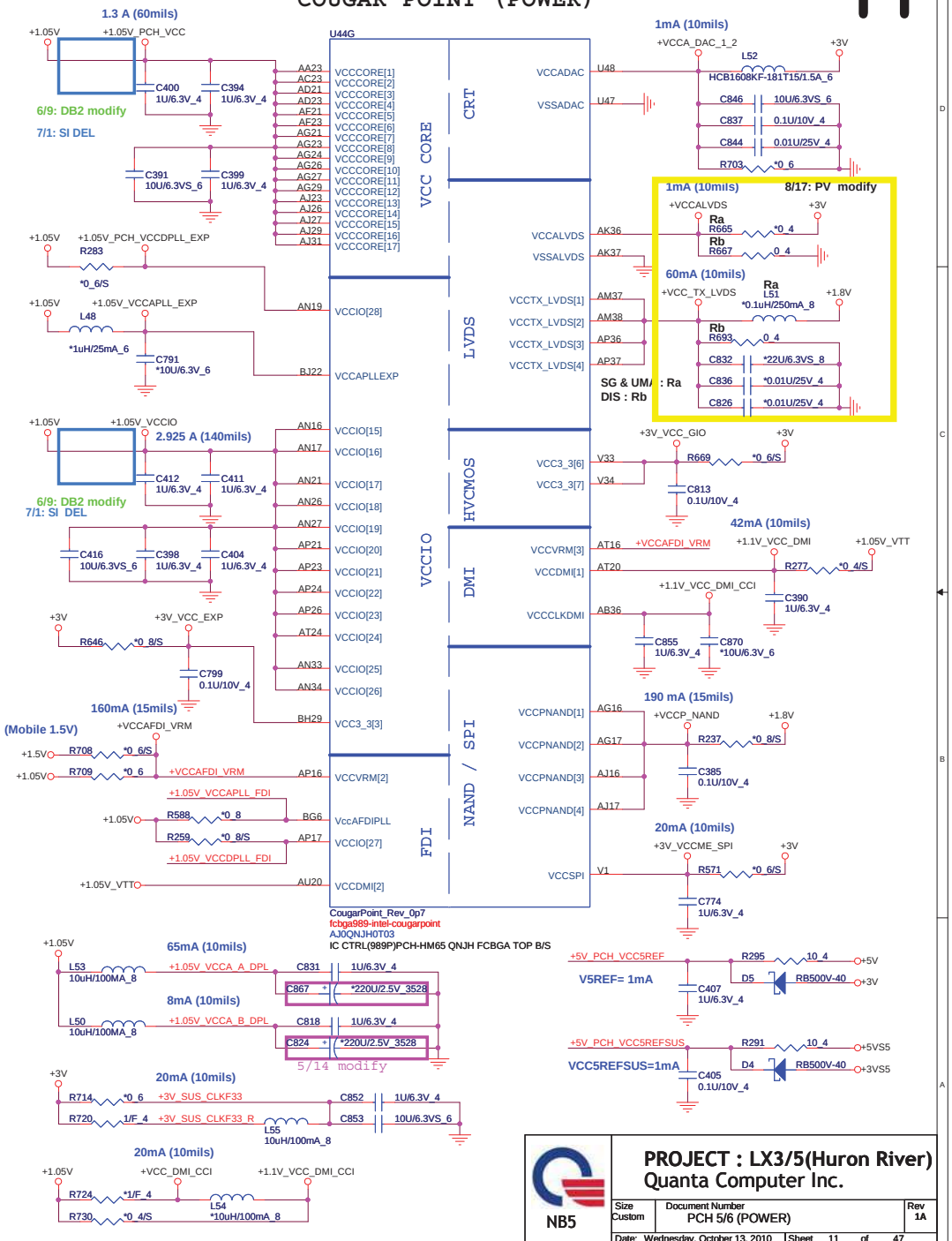
Size: Custom | Document Number: PCH 4/6 (GPIO/MISC) | Rev: 1A

Date: Wednesday, October 13, 2010 | Sheet 10 of 47

Cougar Point-M (POWER)



COUGAR POINT (POWER)



+1.05V [7,8,9,34,35,41]
+1.05V_VTT [3,5,39,40]
+1.5VSUS [3,5,13,14,43,45]
+1.8V [5,8,39,45]

+3V_RTC [7,8]
+3V_DSW [7,8]
+3VS5 [3,7,8,9,10,45]
+3V [3,7,8,9,10,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]
+5VS5 [45]
+5V [7,8,19,25,26,27,29,30,32,34,36,37,45]

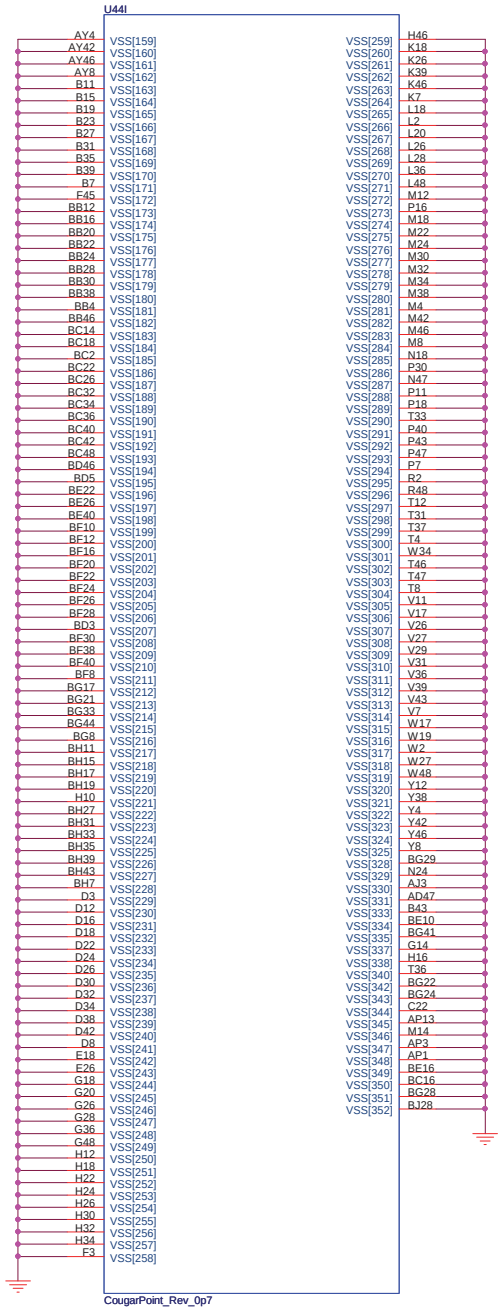
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

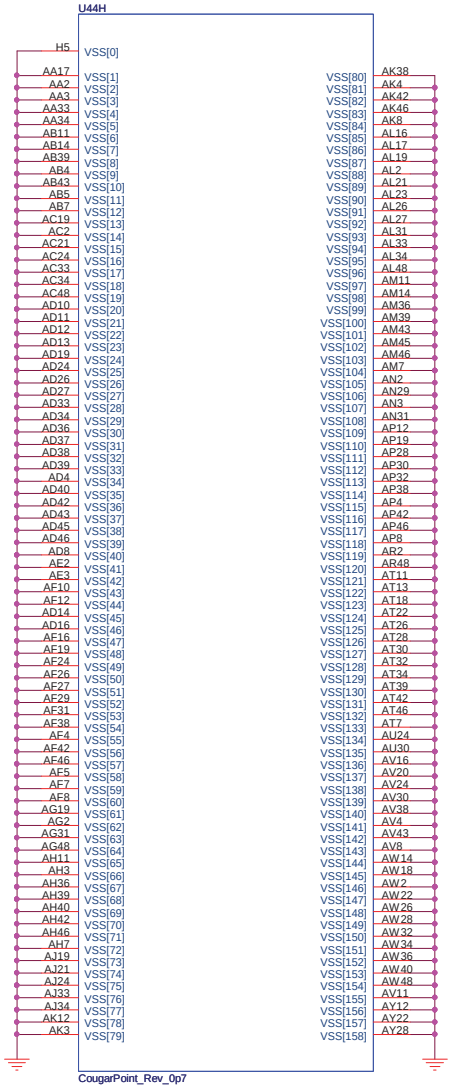
Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A

Date: Wednesday, October 13, 2010 | Sheet 11 of 47

IBEX PEAK-M (GND)



IBEX PEAK-M (GND)

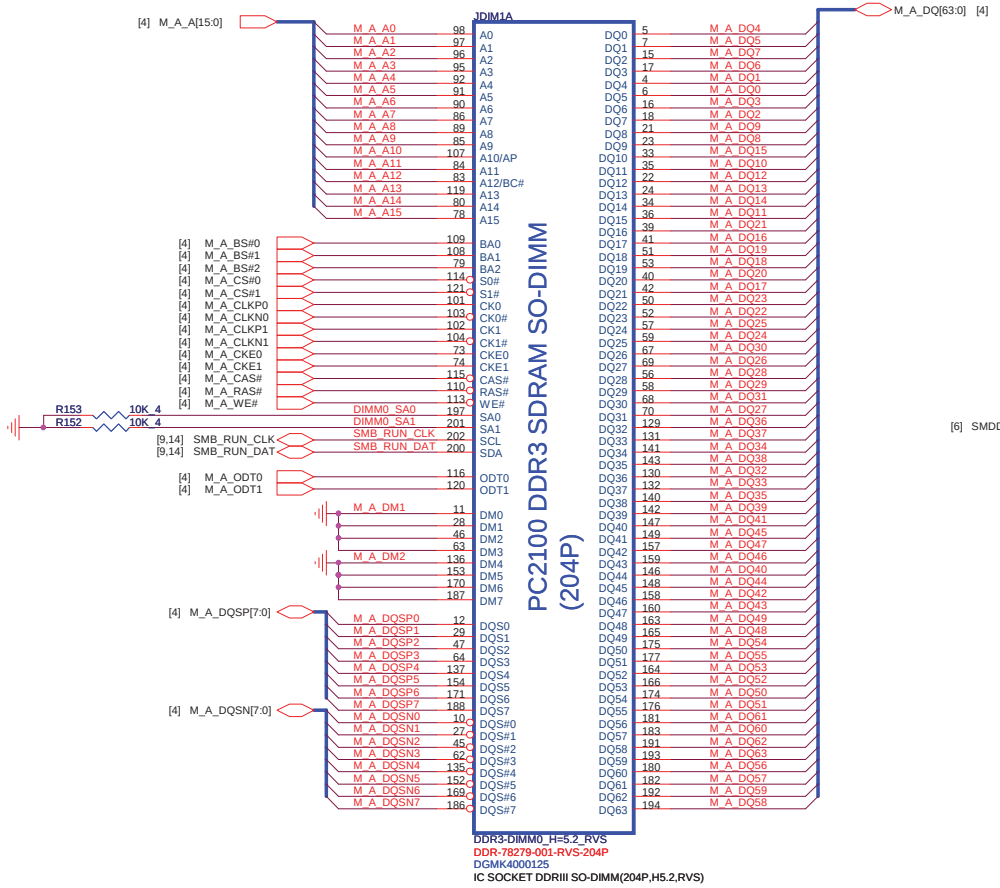


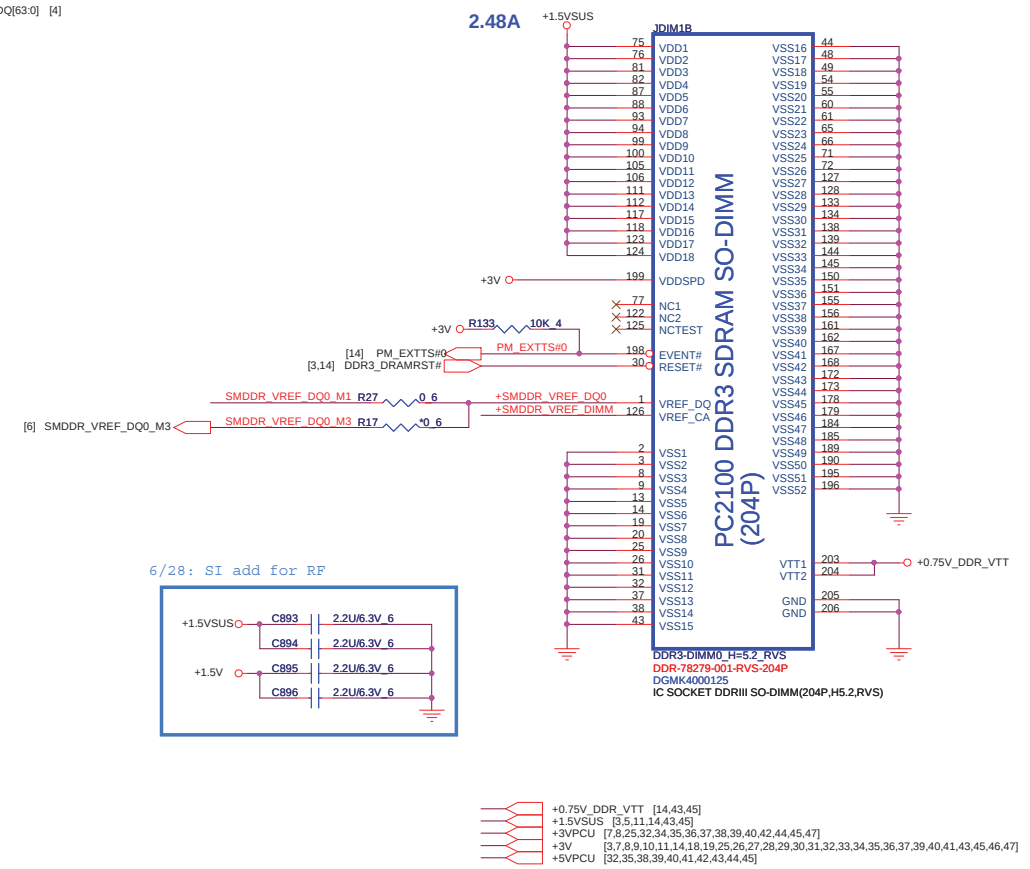
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

Date: Wednesday, October 13, 2010 | Sheet 12 of 47



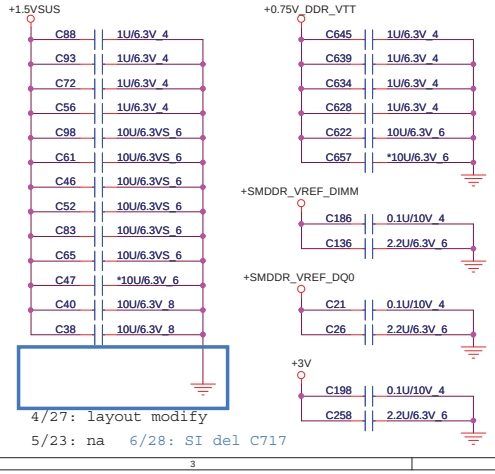


VREF DQ0 M2 Solution

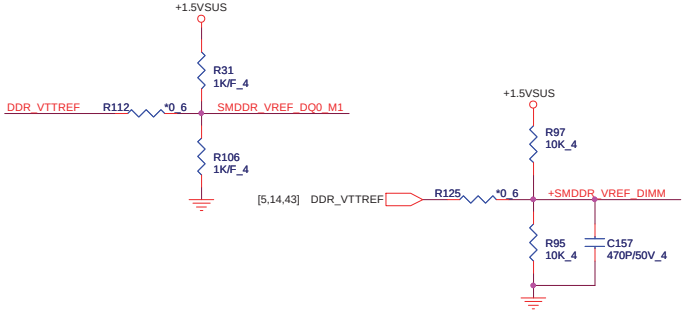
6/23 : Del M2 solution

4/29: reserve M2 solution

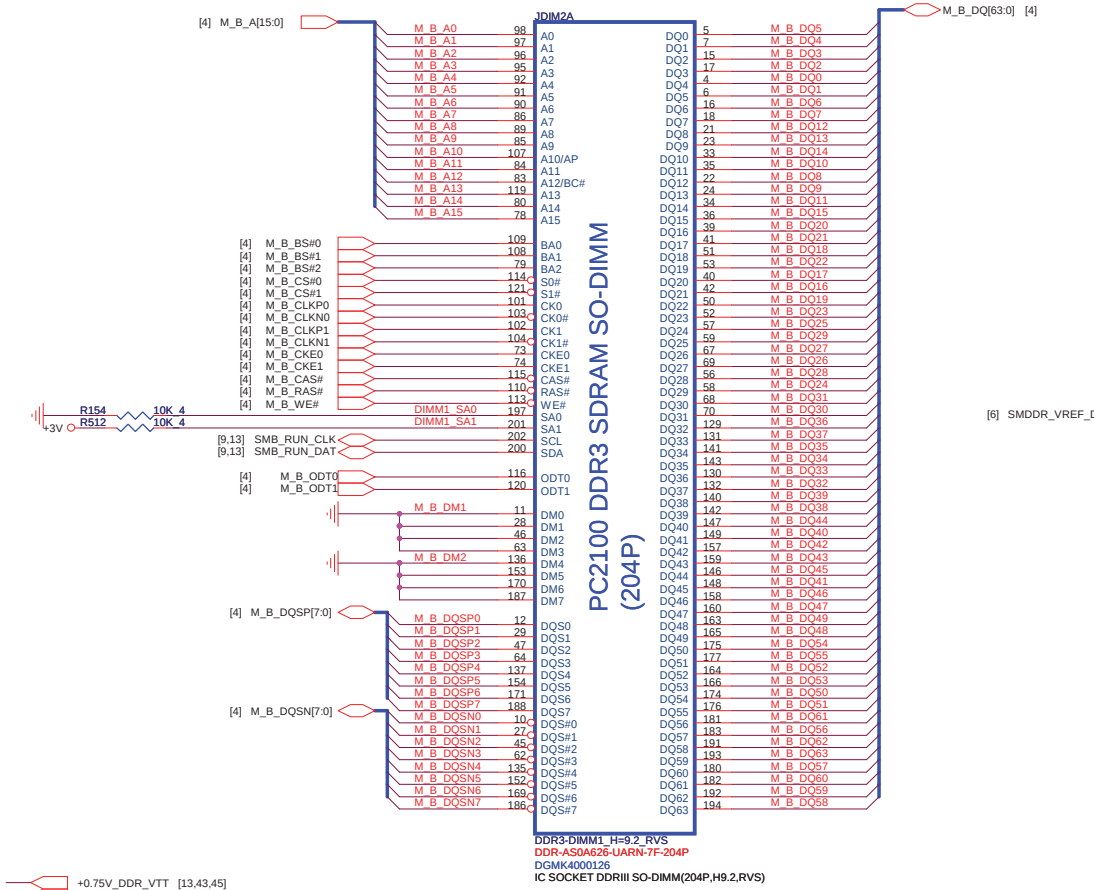
Place these Caps near So-Dimm0.

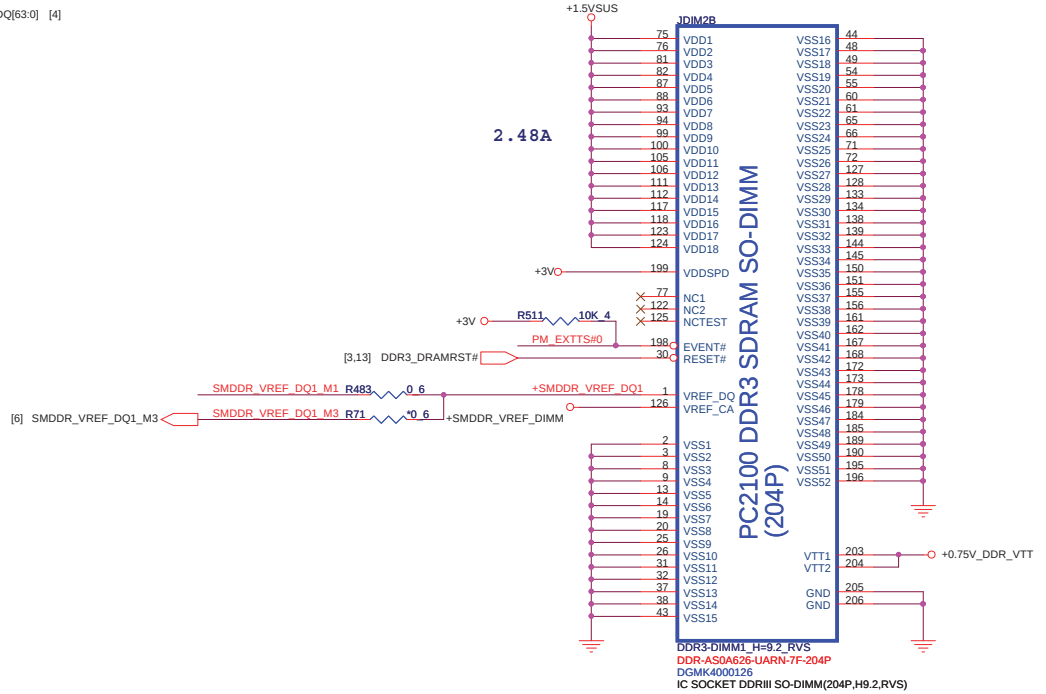


VREF DQ0 M1 Solution

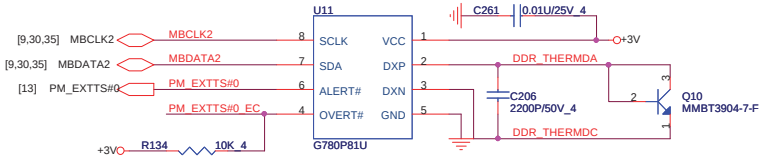


NB5	PROJECT : LX3/5(Huron River) Quanta Computer Inc.
Size: Custom	Document Number: DDR3 DIMM0-RVS (5.2H) — Rev: 1A
Date: Wednesday, October 13, 2010	Sheet 13 of 47





DDR3 Thermal Sensor

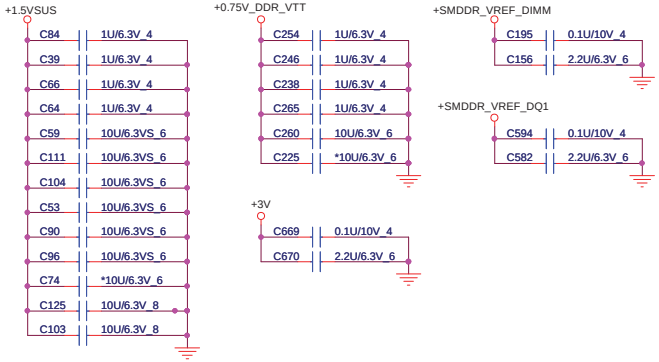


VREF DQ1 M2 Solution

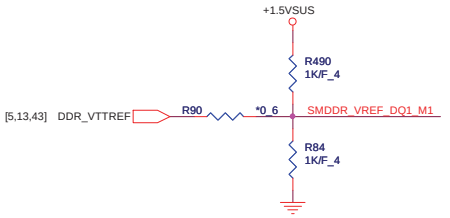
6/23 : Del M2 solution

4/29 reserve M2 solution

Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution

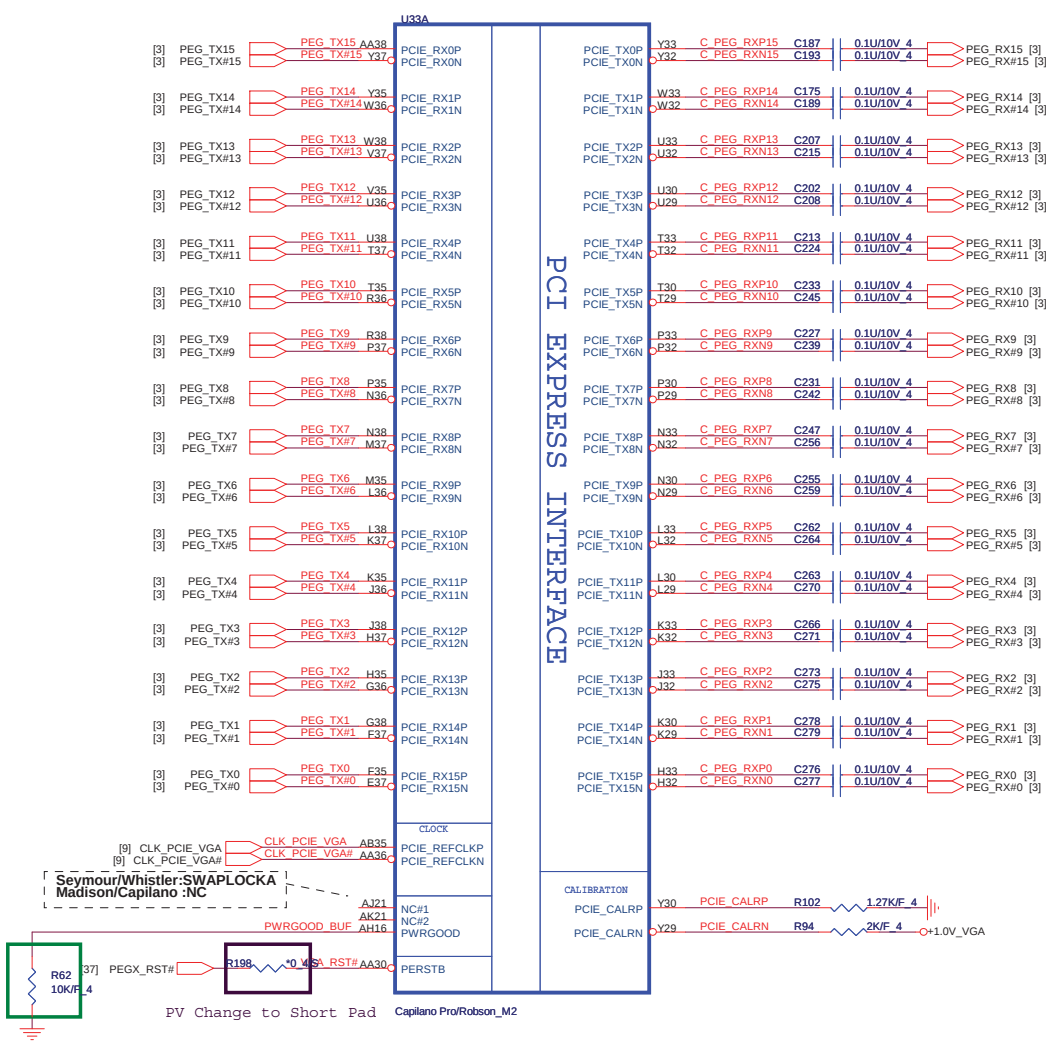


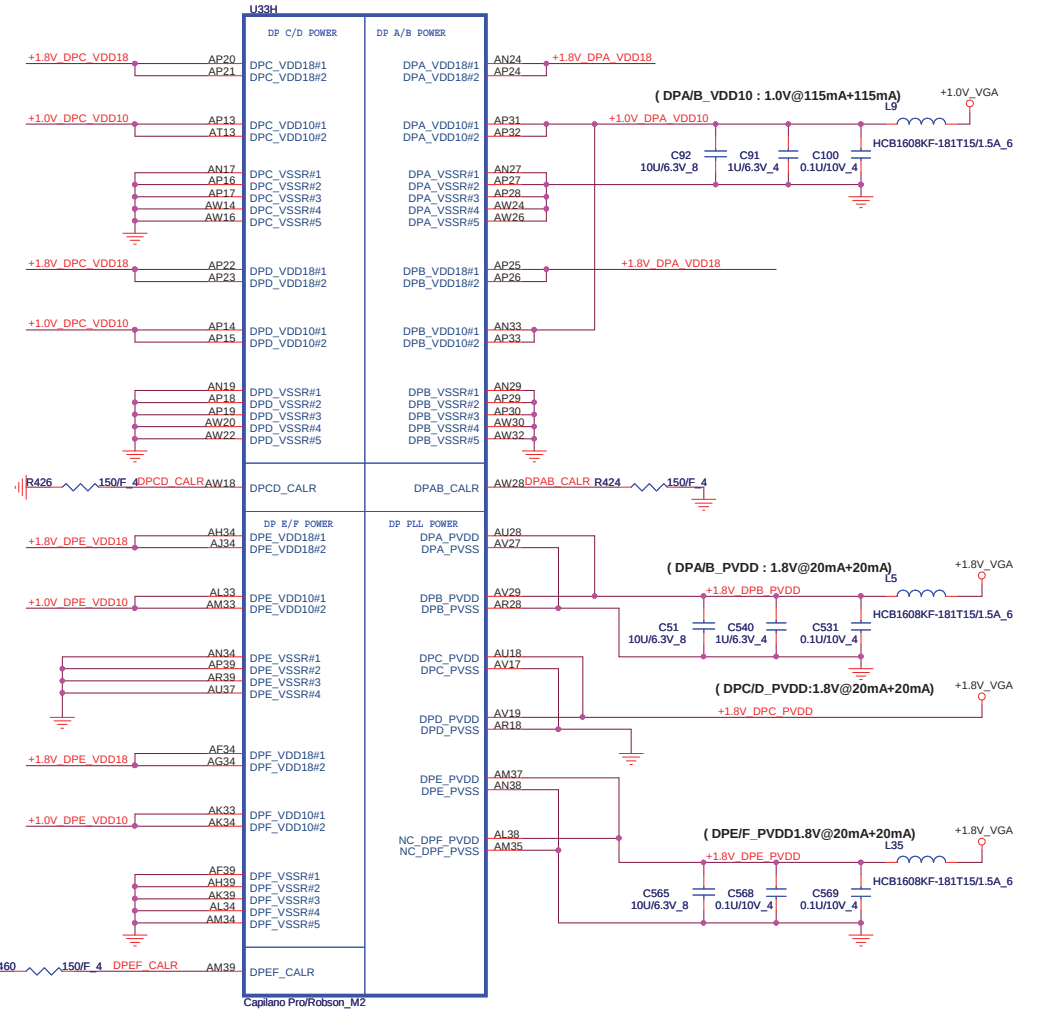
NB5

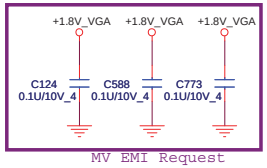
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS (9.2H)	1A

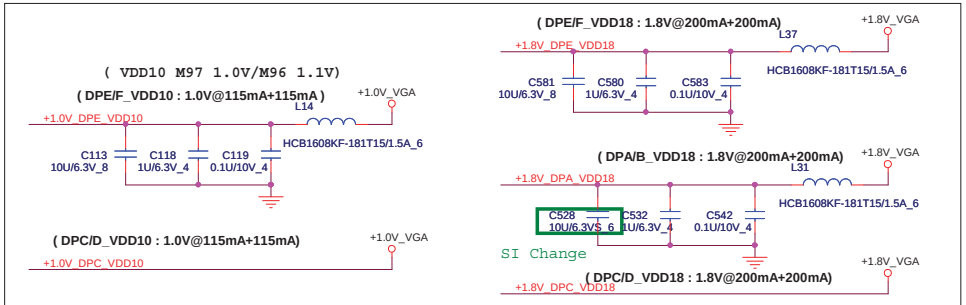
Date: Wednesday, October 13, 2010 Sheet 14 of 47







SI Del R43,R38,C57



+1.0V_VGA [17,19,43]
+1.8V_VGA [17,19,42]

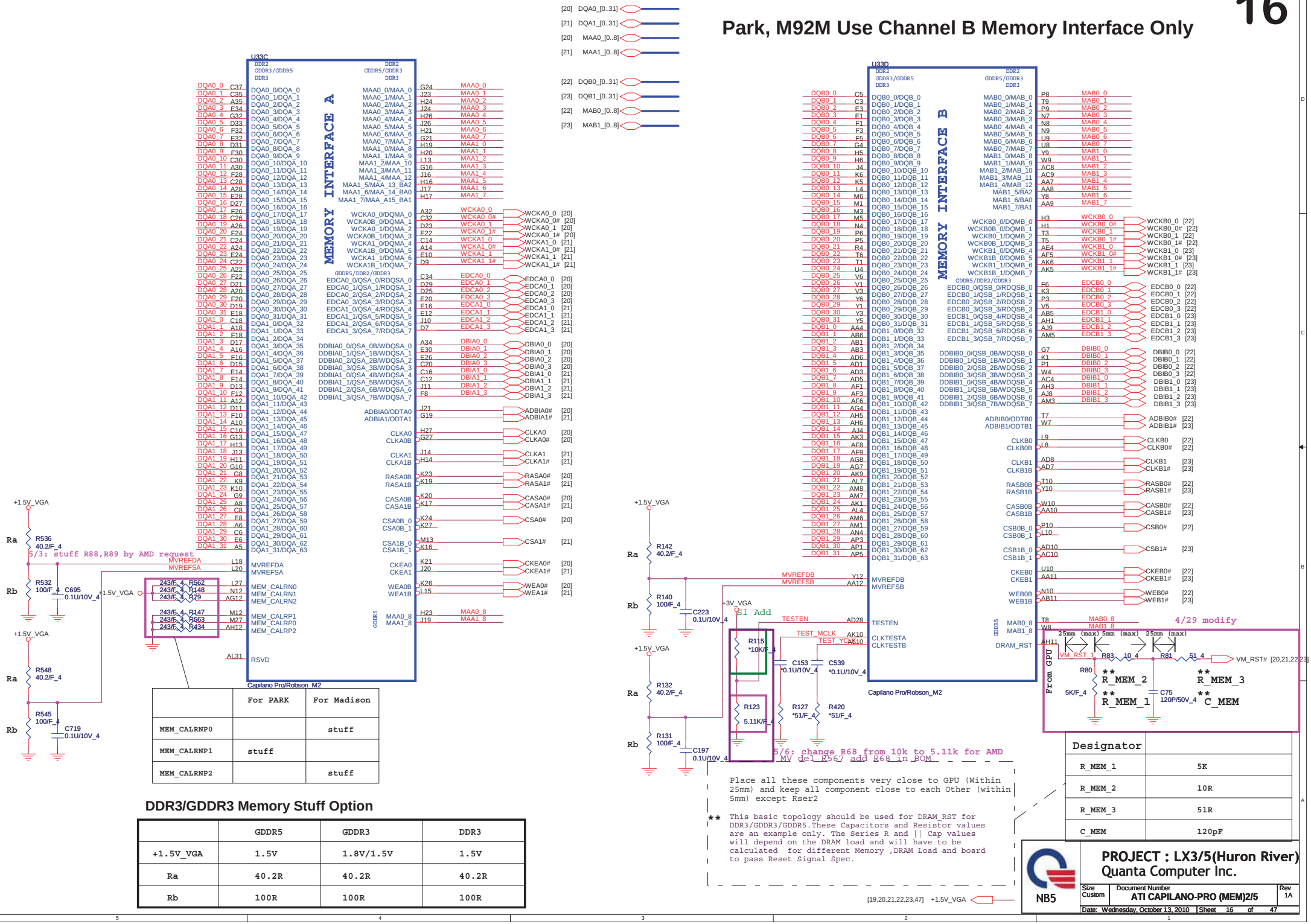
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CATI APILANO-PRO (MEM)1/5	1A

Date: Wednesday, October 13, 2010 | Sheet 15 of 47

Park, M92M Use Channel B Memory Interface Only



	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

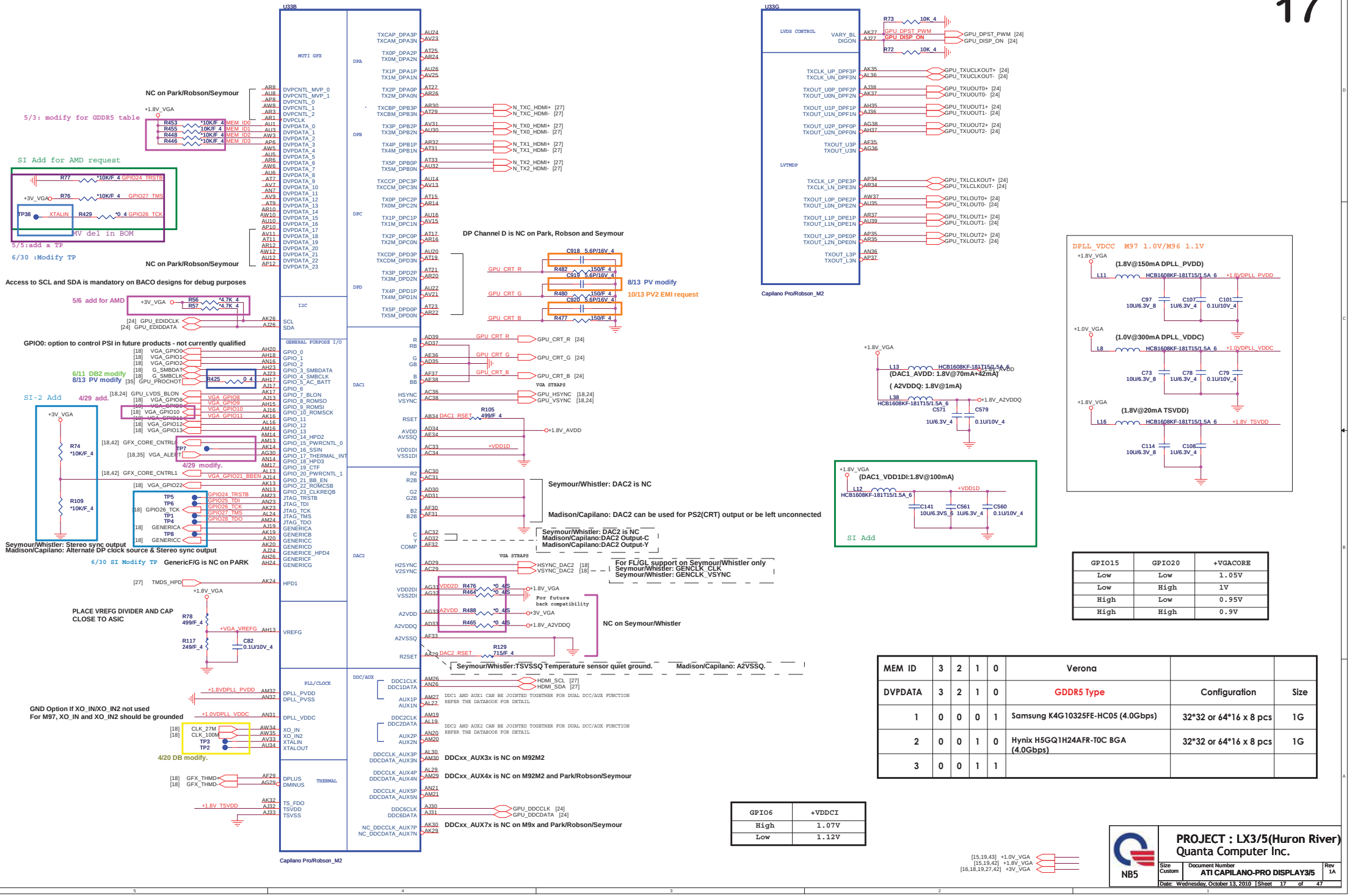
Designator	
R_MEM_1	5K
R_MEM_2	10R
R_MEM_3	51R
C_MEM	120pF

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI CAPILANO-PRO (MEM)2/5	1A

Date: Wednesday, October 13, 2010 Sheet 16 of 47



GPIO15	GPIO20	+VGACORE
Low	Low	1.05V
Low	High	1V
High	Low	0.95V
High	High	0.9V

GPIO6	+VDDCI
High	1.07V
Low	1.12V

MEM ID	3	2	1	0	Verona		
DVPDATA	3	2	1	0	GDDR5 Type	Configuration	Size
1	0	0	0	1	Samsung K4G10325FE-HC05 (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
2	0	0	1	0	Hynix H5GQ1H24AFR-T0C BGA (4.0Gbps)	32*32 or 64*16 x 8 pcs	1G
3	0	0	1	1			

[15,19,43] +1.0V_VGA
[15,19,42] +1.8V_VGA
[16,18,19,27,42] +3V_VGA

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ATI CAPILANO-PRO DISPLAY3/5	1A

Date: Wednesday, October 13, 2010 | Sheet 17 of 47

U33F

Capilano Pro/Robson_M2

GND

STRAPS

5/6: Add pu down for GPIO table

add GPIO10 for EEPROM 4/23.

5/6: Add for Enable EEPROM

5/10 add pu down by AMD request.

Table 3-34 ROM Configurations

Manufacturer	Part Number	Size	CONFIG[2:0]
Atmel	AT25F512	512 kbit	001
	AT25F512A	512 kbit	010
	AT25F1024	1 Mbit	011
	AT25F1024A	1 Mbit	011
	AT25F2048	2 Mbit	011
	AT25F4096	4 Mbit	011
ST Microelectronics	M25P05A	512 kbit	100
	M25P10A	1 Mbit	101
	M25P20	2 Mbit	101
	M25P40	4 Mbit	101
	M25P80	8 Mbit	101
Silicon Storage Technology	SST25VF512	512 kbit	010
	SST25VF010	1 Mbit	011
	SST25VF020	2 Mbit	011
	SST25VF040	4 Mbit	011
Winbond Electronics Corporation	W45B512	512 kbit	110
	W45B012	1 Mbit	111
YMC	Y25LF05	512 kbit	010
	SA25C020	2 Mbit	011
PMC	Pm25LV512	512 kbit	100
	Pm25LV010	1 Mbit	101

Default

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set t 0.

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

27MHz + 100Mhz OSC Option

5/10 modify

4/29 reserve PCH_CLK

6/23: SI modify

SL16010DCT

Reserve for support BACO mode

For PX_EN, refer to the BACO reference schematics for detail

For GDDR5 EEPROM

4/20 DB update

6/23: SI modify

4/19: change only from VGA

Thermal Sensor

*781-1P8@EV

I2C ADDRESS: 9AH

w/s 10 / 10

[16,17,19,27,42] +3V_VGA

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

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(VDDR1: 1.5V@9.1A)

(1.8V@500mA PCIE_VDDR)

(1.0V@2000mA PCIE_VDDC)

(1.8V@136mA VDD_CT)

(3.3V@60mA VDDR3)

VDDR4 for DVPDATA[12..23]

(VDDR4_5 : 1.8V@20/170mA)

VDDR5 for DVPDATA[0..11]

(1.8V@40mA PCIE_PVDD)

(SPV10 :1.0V@120mA)

(For MP7, 1.12V@4A VDDCI).

SI Change BOM

SI MODIFY

SI ADD

SI MODIFY and ADD

SI Del R46

For non-BACO designs, connect BIF_VDDC to VDDC.
For BACO designs - see BACO reference schematics (ref138)

4/20 DB add.

Support BACO Mode

Capilano Pro/Robson_M2

PROJECT :	LX3/5(Huron River)
	Quanta Computer Inc.
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1GB GDDR5 : CHANNEL A-0 (64M x 16)

[16] DQA0_[31..0]
[16] MAA0_[8..0]

U39

MAA0_7 K4
MAA0_6 K5
MAA0_5 K10
MAA0_4 K11
MAA0_3 H10
MAA0_2 H11
MAA0_1 H5
MAA0_0 H4

A8/A7_A10/A0
A11/A6_A9/A1
BA1/A5_BA3/A3
BA2/A4_BA0/A2
BA3/A3_BA1/A5
BA0/A2_BA2/A4
A9/A1_A11/A6
A10/A0_A8/A7

DQ0/DQ24 A4 DQA0_16
DQ1/DQ25 A2 DQA0_18
DQ2/DQ26 B4 DQA0_19
DQ3/DQ27 B2 DQA0_17
DQ4/DQ28 F4 DQA0_20
DQ5/DQ29 E2 DQA0_23
DQ6/DQ30 F4 DQA0_21
DQ7/DQ31 F2 DQA0_22

+1.5V_VGA
[16] DBIA0_2 DBIA0_2 D2
[16] DBIA0_0 DBIA0_0 P13
D13
P2

DBI0#/DBI3#
DBI1#/DBI2#
DBI2#/DBI1#
DBI3#/DBI0#

DQ8/DQ16 A11
DQ9/DQ17 A13
DQ10/DQ18 B11
DQ11/DQ19 B13
DQ12/DQ20 E11
DQ13/DQ21 E13
DQ14/DQ22 F11
DQ15/DQ23 F13

R558 *0_4/S
[16] EDCA0_2 EDCA0_2 C2
[16] EDCA0_0 EDCA0_0 R13
C13
R2

EDC0/EDC3
EDC1/EDC2
EDC2/EDC1
EDC3/EDC0

DQ16/DQ8 U11 DQA0_5
DQ17/DQ9 U13 DQA0_1
DQ18/DQ10 T11 DQA0_4
DQ19/DQ11 T13 DQA0_3
DQ20/DQ12 N11 DQA0_6
DQ21/DQ13 N13 DQA0_2
DQ22/DQ14 M11 DQA0_7
DQ23/DQ15 M13 DQA0_0

[16] RASA0# RASA0# G3
[16] CASA0# CASA0# L3
[16] CSA0# CSA0# G12
[16] WEA0# WEA0# L12
A5

RAS#/CAS#
CAS#/RAS#
CS#/WE#
WE#/CS#

MAA0_8 J5
U5

NC1
NC2
NC3

DQ24/DQ0 U4
DQ25/DQ1 U2
DQ26/DQ2 T4
DQ27/DQ3 T2
DQ28/DQ4 N4
DQ29/DQ5 N2
DQ30/DQ6 M4
DQ31/DQ7 M2

6/29: SI add

R758 0_4 J1
R551 120_4 J13

MF
ZQ

[16,21,22,23] VM_RST# VM_RST# J2
R760 0_4 J10

RESET#
SEN

[16] ADBIA0# ADBIA0# J4

ABI#

WCK01/WCK23 D4 WCKA0_1
WCK01#/WCK23# D5 WCKA0_1# [16]
WCK23/WCK01 P4 WCKA0_0 [16]
WCK23#/WCK01# P5 WCKA0_0# [16]

CK# J11 CLKA0# [16]
CK J12 CLKA0 [16]
CKE# J3 CKEA0# [16]

C728 1U/6.3V_4
R553 5.49K_4
VREFC_VMA1 J14

VREFC

+1.5V_VGA
C738 1U/6.3V_4
R557 2.37K_4
VREFD_VMA1 A10

VREFD#A10

VREFD_VMAU1 U10

VREFD#U10

+1.5V_VGA
C766 1U/6.3V_4
R565 5.49K_4
C765 1U/6.3V_4
+1.5V_VGA R564 2.37K_4

+1.5V_VGA
C318 1U/6.3V_4
R180 5.49K_4
C323 1U/6.3V_4
+1.5V_VGA R183 2.37K_4

VDD#C5 C5
VDD#G1 G1
VDD#G4 G4
VDD#L1 L1
VDD#L4 L4
VDD#R5 R5
VDD#C10 C10
VDD#D11 D11
VDD#G11 G11
VDD#G14 G14
VDD#L11 L11
VDD#L14 L14
VDD#P11 P11
VDD#R10 R10

VSS#B5 B5
VSS#G5 G5
VSS#H1 H1
VSS#K1 K1
VSS#L5 L5
VSS#T5 T5
VSS#B10 B10
VSS#D10 D10
VSS#G10 G10
VSS#H14 H14
VSS#K14 K14
VSS#L10 L10
VSS#P10 P10
VSS#T10 T10

170-BALL
SDRAM GDDR5

VDDQ#B1 B1
VDDQ#B3 B3
VDDQ#D1 D1
VDDQ#D3 D3
VDDQ#E5 E5
VDDQ#F1 F1
VDDQ#F3 F3
VDDQ#G2 G2
VDDQ#H3 H3
VDDQ#K3 K3
VDDQ#L2 L2
VDDQ#M1 M1
VDDQ#M3 M3
VDDQ#N5 N5
VDDQ#P1 P1
VDDQ#P3 P3
VDDQ#T1 T1
VDDQ#T3 T3
VDDQ#B12 B12
VDDQ#B14 B14
VDDQ#D12 D12
VDDQ#D14 D14
VDDQ#E10 E10
VDDQ#F12 F12
VDDQ#F14 F14
VDDQ#G13 G13
VDDQ#H12 H12
VDDQ#K12 K12
VDDQ#L13 L13
VDDQ#M12 M12
VDDQ#M14 M14
VDDQ#N10 N10
VDDQ#P12 P12
VDDQ#P14 P14
VDDQ#T12 T12
VDDQ#T14 T14

VSSQ#A1 A1
VSSQ#A3 A3
VSSQ#C1 C1
VSSQ#C3 C3
VSSQ#C4 C4
VSSQ#E1 E1
VSSQ#E3 E3
VSSQ#F5 F5
VSSQ#H2 H2
VSSQ#K2 K2
VSSQ#M5 M5
VSSQ#N1 N1
VSSQ#N3 N3
VSSQ#R1 R1
VSSQ#R3 R3
VSSQ#R4 R4
VSSQ#U1 U1
VSSQ#U3 U3
VSSQ#A12 A12
VSSQ#A14 A14
VSSQ#C11 C11
VSSQ#C12 C12
VSSQ#C14 C14
VSSQ#E12 E12
VSSQ#E14 E14
VSSQ#F10 F10
VSSQ#H13 H13
VSSQ#K13 K13
VSSQ#M10 M10
VSSQ#N12 N12
VSSQ#N14 N14
VSSQ#R11 R11
VSSQ#R12 R12
VSSQ#R14 R14
VSSQ#U12 U12
VSSQ#U14 U14

K4G52324FG

MF=1 Mirror

U15

MAA0_0 K4
MAA0_1 K5
MAA0_3 K10
MAA0_2 K11
MAA0_5 H10
MAA0_4 H11
MAA0_6 H5
MAA0_7 H4

A8/A7_A10/A0
A11/A6_A9/A1
BA1/A5_BA3/A3
BA2/A4_BA0/A2
BA3/A3_BA1/A5
BA0/A2_BA2/A4
A9/A1_A11/A6
A10/A0_A8/A7

DQ0/DQ24 A4 DQA0_29
DQ1/DQ25 A2 DQA0_30
DQ2/DQ26 B4 DQA0_26
DQ3/DQ27 B2 DQA0_25
DQ4/DQ28 E4 DQA0_27
DQ5/DQ29 E2 DQA0_28
DQ6/DQ30 F4 DQA0_24
DQ7/DQ31 F2 DQA0_31

+1.5V_VGA
[16] DBIA0_3 D2
[16] DBIA0_1 D13
P13
P2

DBI0#/DBI3#
DBI1#/DBI2#
DBI2#/DBI1#
DBI3#/DBI0#

DQ8/DQ16 A11
DQ9/DQ17 A13
DQ10/DQ18 B11
DQ11/DQ19 B13
DQ12/DQ20 E11
DQ13/DQ21 E13
DQ14/DQ22 F11
DQ15/DQ23 F13

R186 *0_4/S
[16] EDCA0_3 C2
[16] EDCA0_1 C13
R13
R2

EDC0/EDC3
EDC1/EDC2
EDC2/EDC1
EDC3/EDC0

DQ16/DQ8 U11 DQA0_12
DQ17/DQ9 U13 DQA0_9
DQ18/DQ10 T11 DQA0_15
DQ19/DQ11 T13 DQA0_8
DQ20/DQ12 N11 DQA0_13
DQ21/DQ13 N13 DQA0_10
DQ22/DQ14 M11 DQA0_14
DQ23/DQ15 M13 DQA0_11

CASA0# G3
RASA0# L3
WEA0# G12
CSA0# L12
A5

RAS#/CAS#
CAS#/RAS#
CS#/WE#
WE#/CS#

MAA0_8 J5
U5

NC1
NC2
NC3

DQ24/DQ0 U4
DQ25/DQ1 U2
DQ26/DQ2 T4
DQ27/DQ3 T2
DQ28/DQ4 N4
DQ29/DQ5 N2
DQ30/DQ6 M4
DQ31/DQ7 M2

6/29: SI add

+1.5V_VGA
R759 0_4 J1
R189 120_4 J13

MF
ZQ

VM_RST# J2
R761 0_4 J10

RESET#
SEN

ADBIA0# J4

ABI#

WCK01/WCK23 D4 WCKA0_1
WCK01#/WCK23# D5 WCKA0_1#
WCK23/WCK01 P4 WCKA0_0
WCK23#/WCK01# P5 WCKA0_0#

CK# J11 CLKA0#
CK J12 CLKA0
CKE# J3 CKEA0#

C332 1U/6.3V_4
R191 5.49K_4
VREFC_VMA2 J14

VREFC

+1.5V_VGA
C336 1U/6.3V_4
R192 2.37K_4
VREFD_VMA2 A10

VREFD#A10

VREFD_VMAU2 U10

VREFD#U10

+1.5V_VGA
C319 1U/6.3V_4
R181 5.49K_4
C324 1U/6.3V_4
+1.5V_VGA R184 2.37K_4

+1.5V_VGA
C353 1U/6.3V_4
R199 5.49K_4
C761 1U/6.3V_4
+1.5V_VGA R200 2.37K_4

VDD#C5 C5
VDD#G1 G1
VDD#G4 G4
VDD#L1 L1
VDD#L4 L4
VDD#R5 R5
VDD#C10 C10
VDD#D11 D11
VDD#G11 G11
VDD#G14 G14
VDD#L11 L11
VDD#L14 L14
VDD#P11 P11
VDD#R10 R10

VSS#B5 B5
VSS#G5 G5
VSS#H1 H1
VSS#K1 K1
VSS#L5 L5
VSS#T5 T5
VSS#B10 B10
VSS#D10 D10
VSS#G10 G10
VSS#H14 H14
VSS#K14 K14
VSS#L10 L10
VSS#P10 P10
VSS#T10 T10

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SDRAM GDDR5

VDDQ#B1 B1
VDDQ#B3 B3
VDDQ#D1 D1
VDDQ#D3 D3
VDDQ#E5 E5
VDDQ#F1 F1
VDDQ#F3 F3
VDDQ#G2 G2
VDDQ#H3 H3
VDDQ#K3 K3
VDDQ#L2 L2
VDDQ#M1 M1
VDDQ#M3 M3
VDDQ#N5 N5
VDDQ#P1 P1
VDDQ#P3 P3
VDDQ#T1 T1
VDDQ#T3 T3
VDDQ#B12 B12
VDDQ#B14 B14
VDDQ#D12 D12
VDDQ#D14 D14
VDDQ#E10 E10
VDDQ#F12 F12
VDDQ#F14 F14
VDDQ#G13 G13
VDDQ#H12 H12
VDDQ#K12 K12
VDDQ#L13 L13
VDDQ#M12 M12
VDDQ#M14 M14
VDDQ#N10 N10
VDDQ#P12 P12
VDDQ#P14 P14
VDDQ#T12 T12
VDDQ#T14 T14

VSSQ#A1 A1
VSSQ#A3 A3
VSSQ#C1 C1
VSSQ#C3 C3
VSSQ#C4 C4
VSSQ#E1 E1
VSSQ#E3 E3
VSSQ#F5 F5
VSSQ#H2 H2
VSSQ#K2 K2
VSSQ#M5 M5
VSSQ#N1 N1
VSSQ#N3 N3
VSSQ#R1 R1
VSSQ#R3 R3
VSSQ#R4 R4
VSSQ#U1 U1
VSSQ#U3 U3
VSSQ#A12 A12
VSSQ#A14 A14
VSSQ#C11 C11
VSSQ#C12 C12
VSSQ#C14 C14
VSSQ#E12 E12
VSSQ#E14 E14
VSSQ#F10 F10
VSSQ#H13 H13
VSSQ#K13 K13
VSSQ#M10 M10
VSSQ#N12 N12
VSSQ#N14 N14
VSSQ#R11 R11
VSSQ#R12 R12
VSSQ#R14 R14
VSSQ#U12 U12
VSSQ#U14 U14

K4G52324FG

CLKA0 R201 60.4_4 +1.5V_VGA
CLKA0# R202 60.4_4

+1.5V_VGA
C764 2.2U/10V_4
C736 2.2U/10V_4
C732 2.2U/10V_4
C740 2.2U/10V_4
C768 1U/6.3V_4
C737 1U/6.3V_4
C767 10U/6.3V_8
C769 10U/6.3V_8

+1.5V_VGA
C751 2.2U/10V_4
C338 2.2U/10V_4
C352 2.2U/10V_4
C351 2.2U/10V_4
C326 1U/6.3V_4
C328 1U/6.3V_4
C346 10U/6.3V_8
C321 10U/6.3V_8

Change 1u to 2.2,for ATI Request 1212

[16,19,21,22,23,47] +1.5V_VGA

NB5

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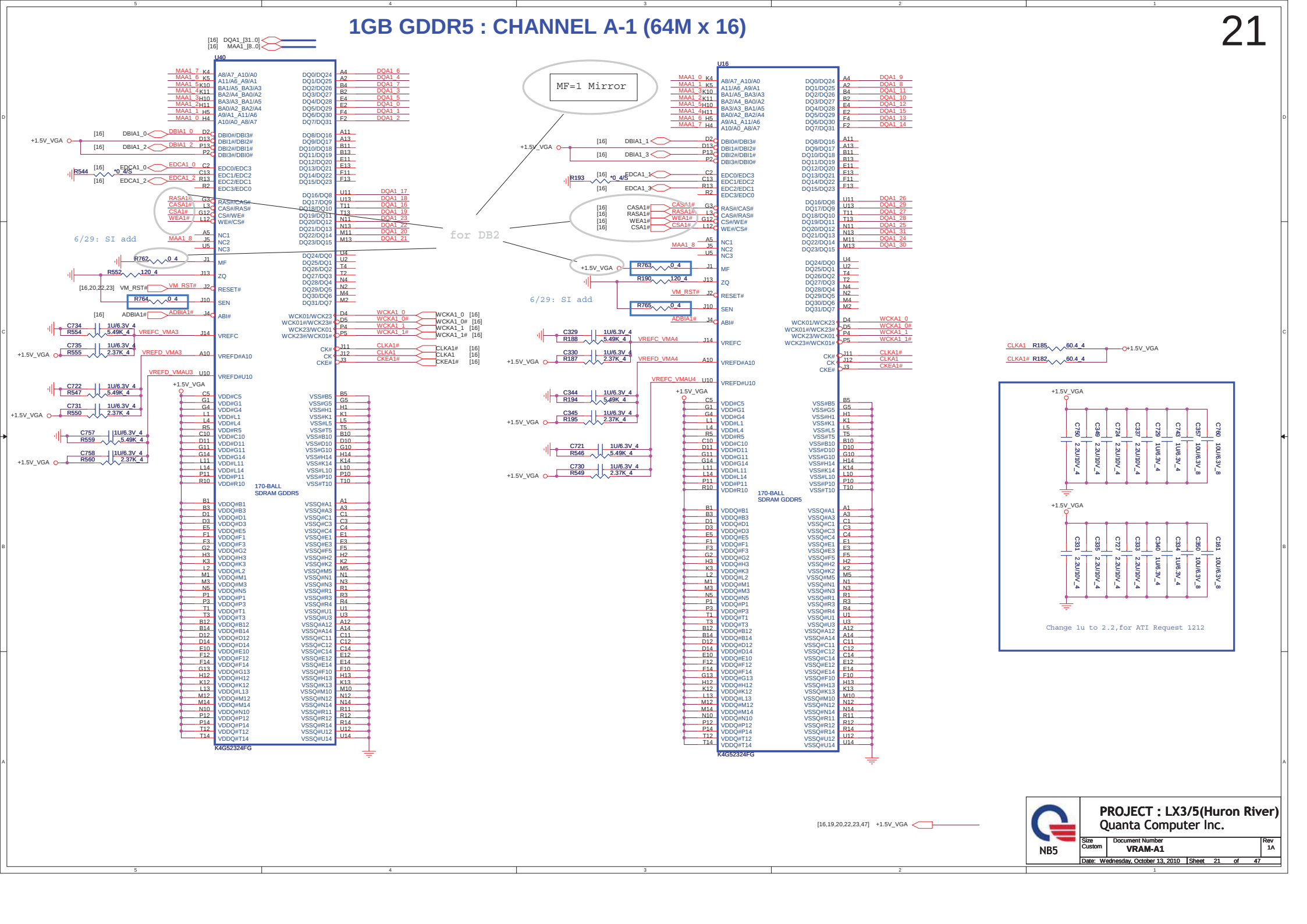
1GB GDDR5 : CHANNEL A-1 (64M x 16)



1GB GDDR5 : CHANNEL B-0 (64M x 16)

[16] DQB0_[0..31]
[16] MAB0_[0..8]

U12

MF=1 Mirror

U36

6/29: SI add

6/29: SI add

170-BALL SDRAM GDDR5

K4G52324FG

Change 1u to 2.2,for ATI Request 1212

+1.5V_VGA [16,19,20,21,23,47]

[16,19,20,21,23,47] +1.5V_VGA

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Quanta Computer Inc.
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Size Custom
Document Number VRAM-B0
Rev 1A
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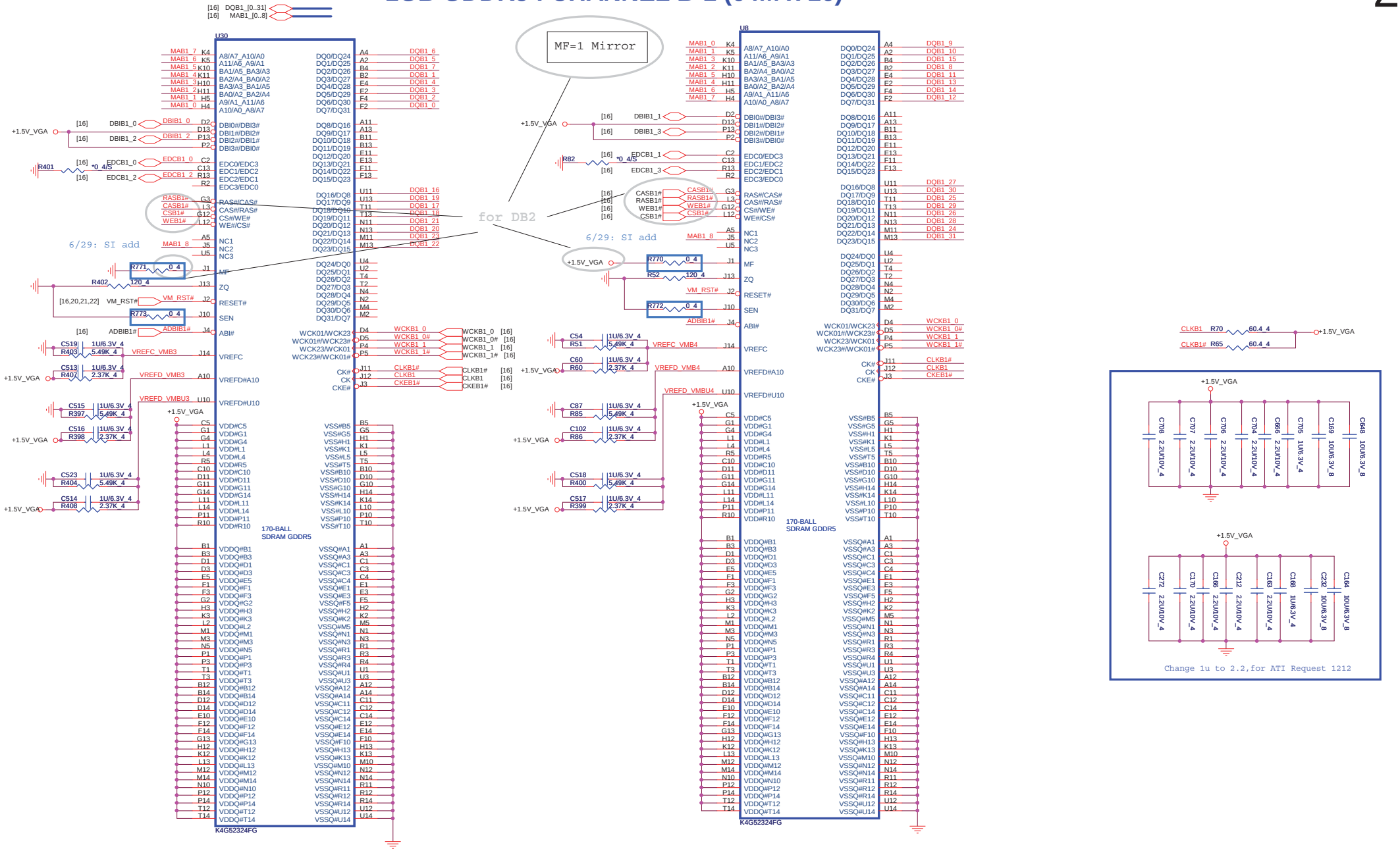
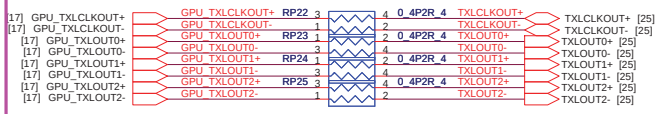
1GB GDDR5 : CHANNEL B-1 (64M x 16)



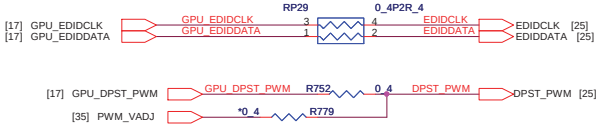
FOR DIS ONLY

OPTION SIGNAL FROM NB to LVDS for DIS



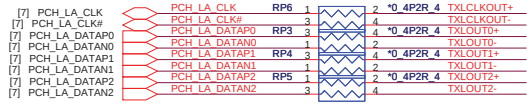
OPTION Back Light SIGNAL FROM NB to LVDS for DIS

OPTION SIGNAL FROM NB to LVDS for DIS

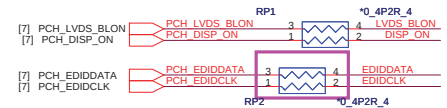


FOR UMA ONLY

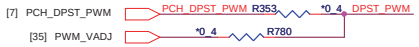
OPTION SIGNAL FROM NB to LVDS for UMA



OPTION Back Light SIGNAL FROM NB to LVDS for UMA

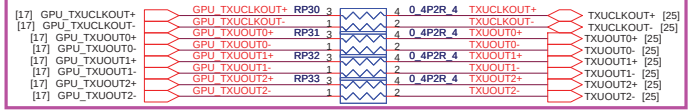


OPTION SIGNAL FROM NB to LVDS for UMA

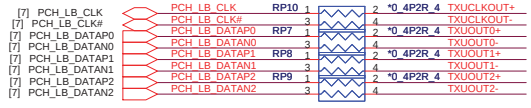


FOR UMA/SG

FOR 17"DIS ONLY

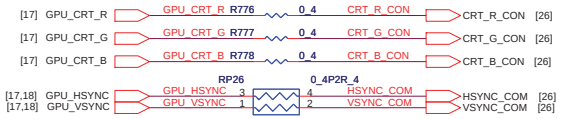


FOR 17"UMA ONLY

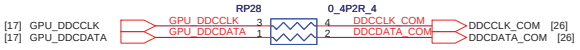


FOR DIS ONLY

OPTION SIGNAL FROM NB to CRT for DIS

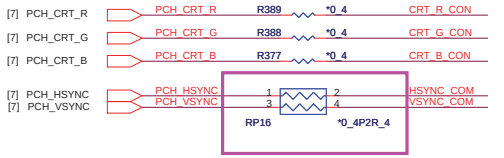


OPTION SIGNAL FROM NB to CRT for DIS



FOR UMA ONLY

OPTION SIGNAL FROM NB to CRT for UMA



5/11:for Layout modify

OPTION SIGNAL FROM NB to CRT for UMA

9/26 :MV Modify

+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,34,36,37,45]
+1.8V [5,8,11,39,45]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

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Custom	SWITCHABLE	1A
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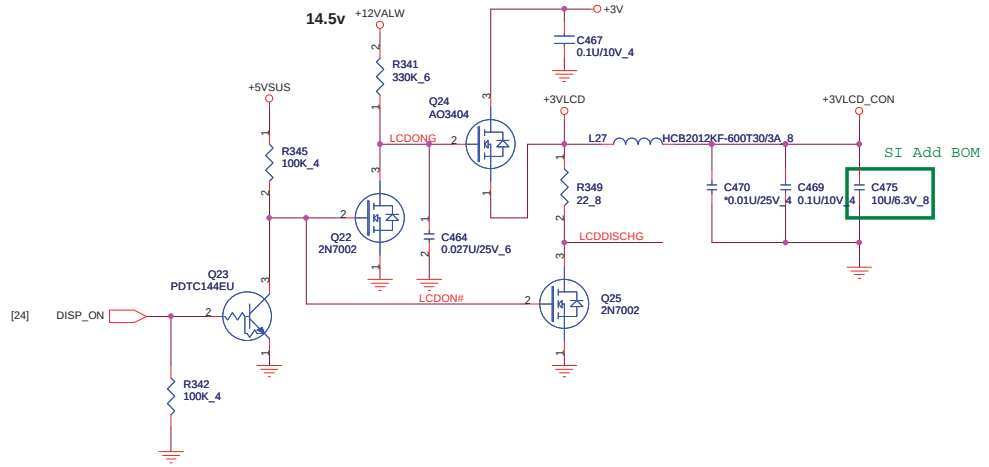
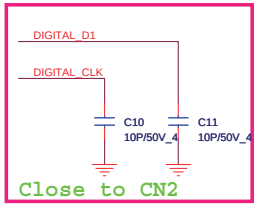
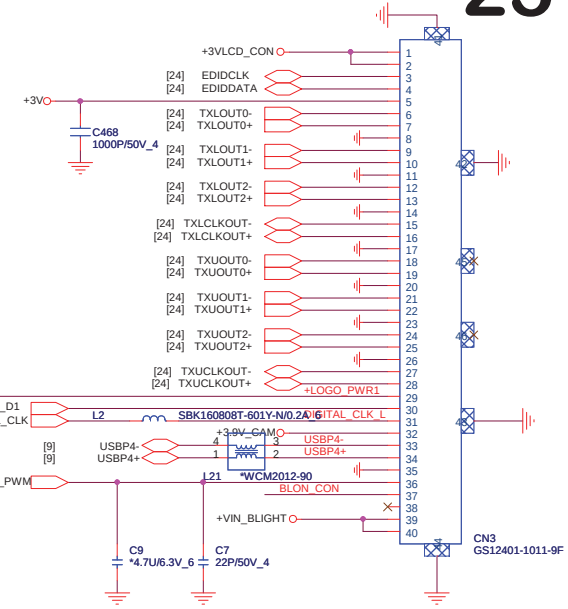
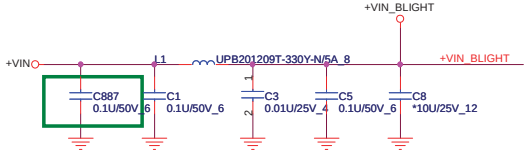
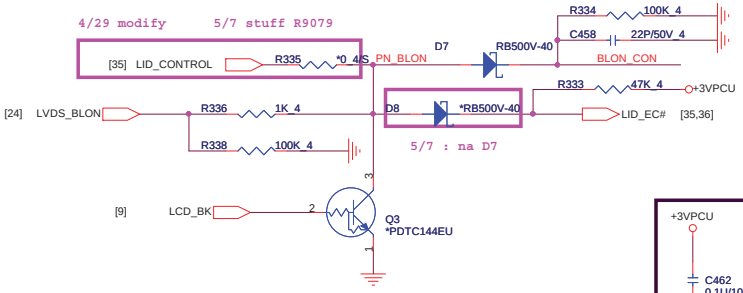
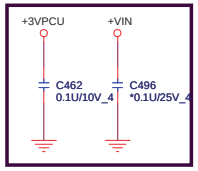


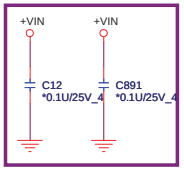


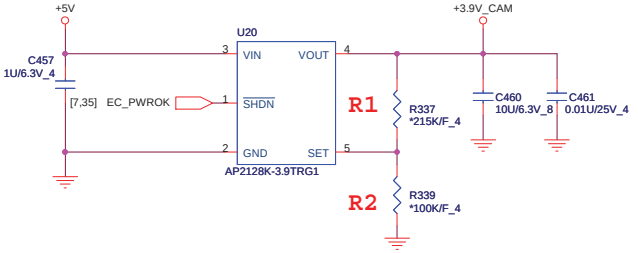












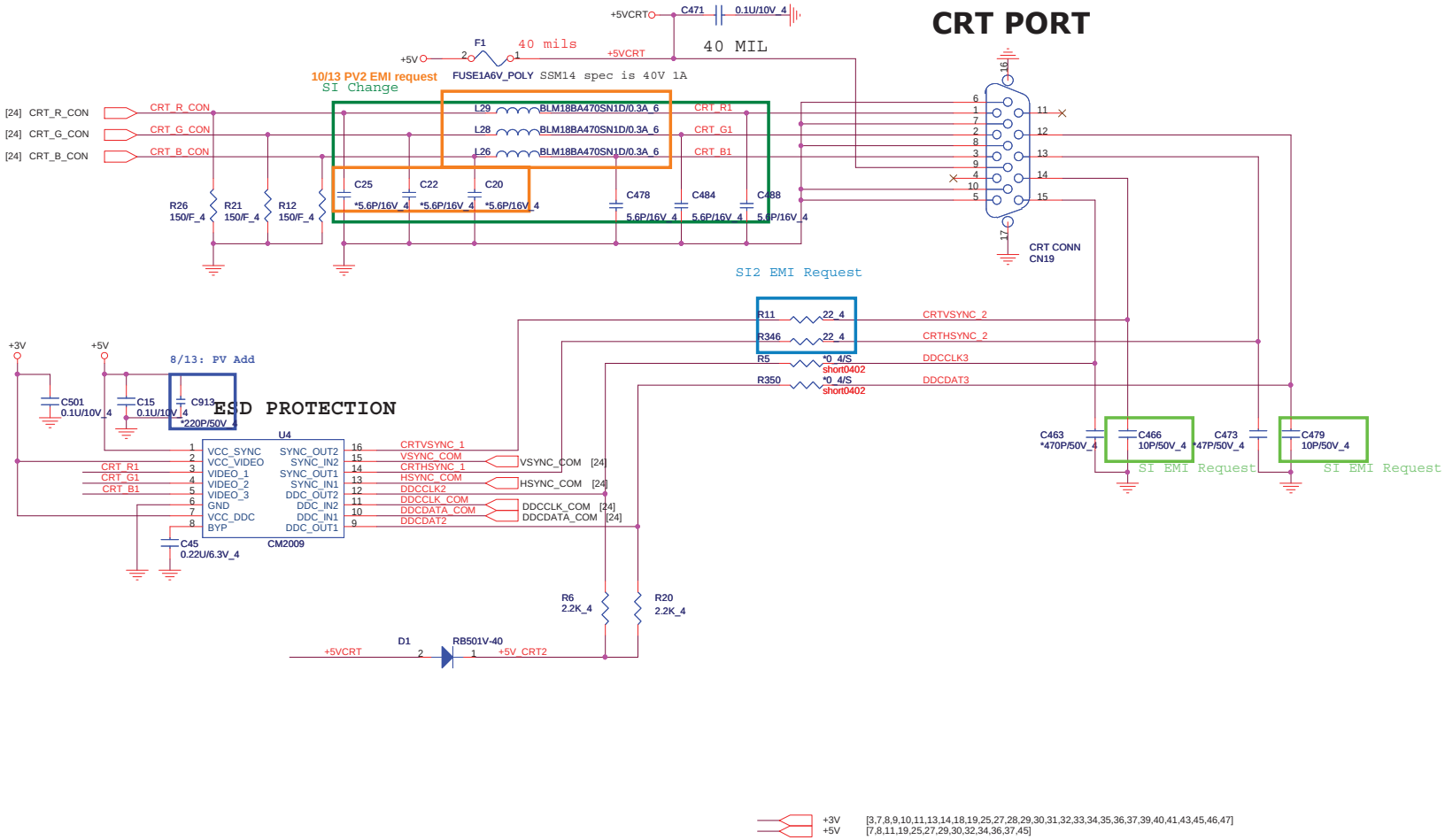
[3,7,8,9,10,11,13,14,18,19,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47] +3V
[7,8,11,19,26,27,29,30,32,34,36,37,45] +5V
[31,38,39,41,42,43,44,45] +VIN
[7,8,32,34,35,36,37,38,39,40,42,44,45,47] +3VPCU
[34,37,42,44,45] +12VALW

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

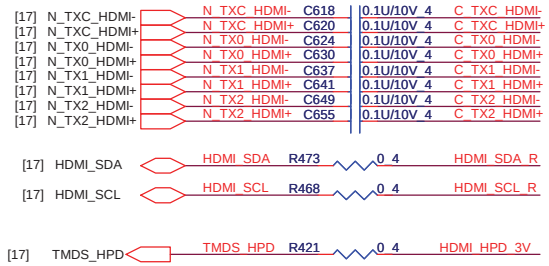
Size	Document Number	Rev
Custom	LCD CONN/LID function	1A
Date: Wednesday, October 13, 2010	Sheet 25 of 47	

CRT PORT

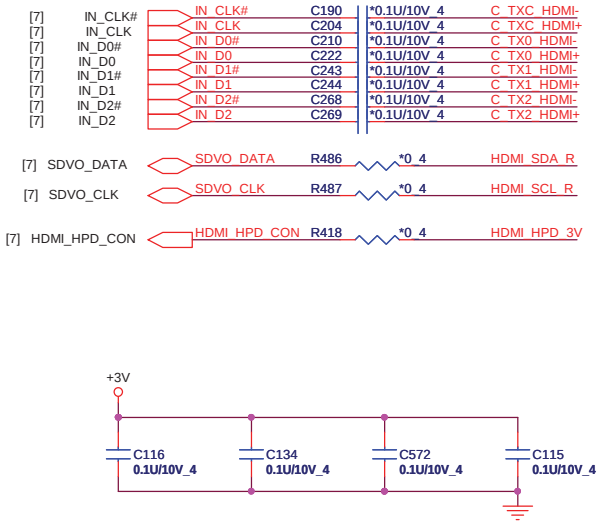


NB5	PROJECT : LX3/5(Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: CRT/HDMI Conn	Rev: 1A
Date: Wednesday, October 13, 2010	Sheet 26 of 47	

DIS/SG HDMI



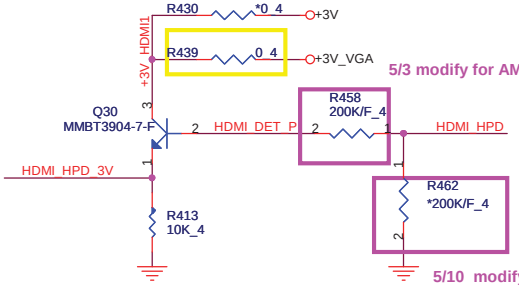
UMA ONLY HDMI

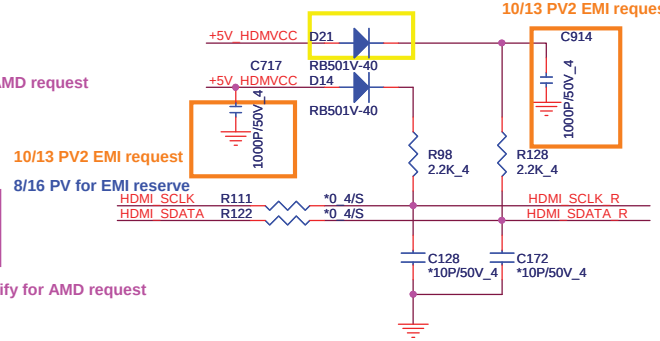


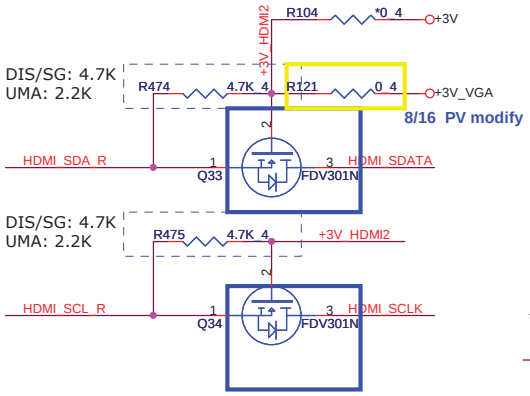
HDMI CON_COM

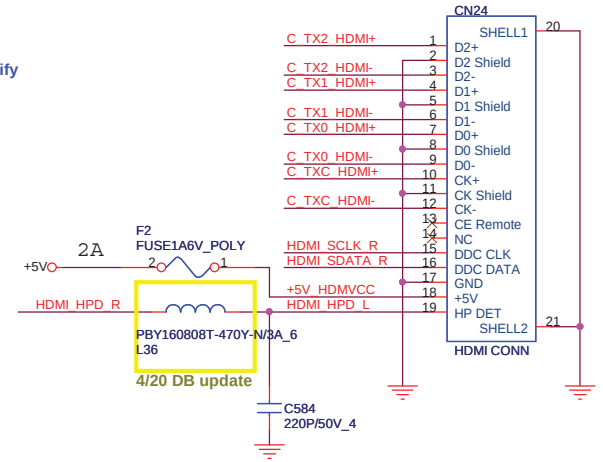
27

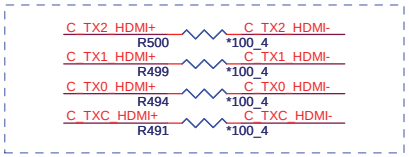
9/26: MV Del C906,C914
9/26: MV Add D21

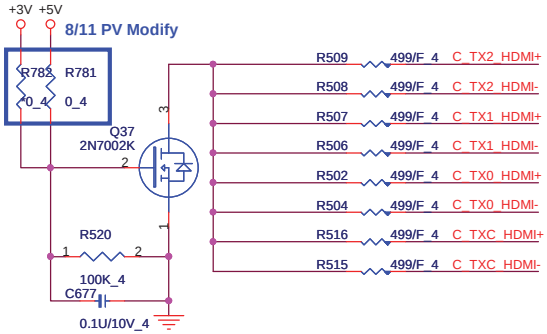


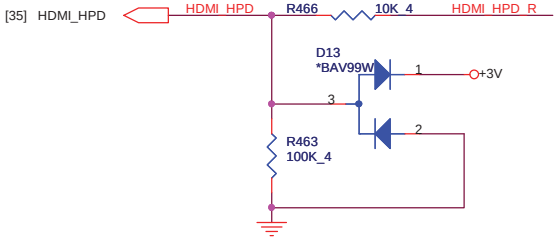










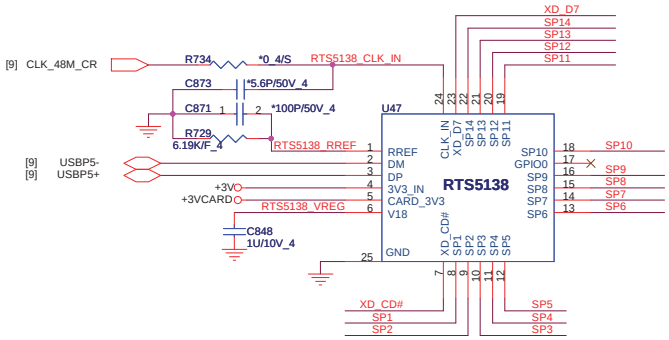


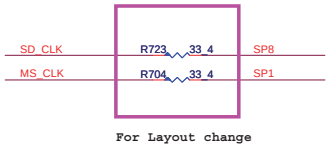
NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/POWER CONN	1A

Date: Wednesday, October 13, 2010 Sheet 27 of 47

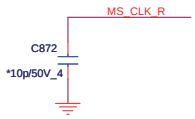




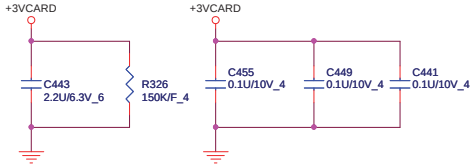
For Layout change

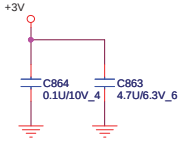
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

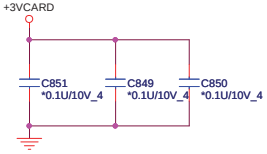
Share Pin



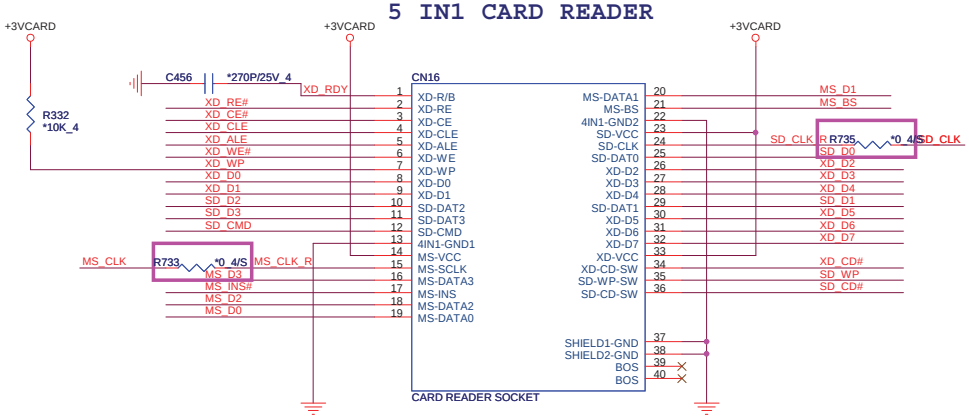
CLOSE CN13







XD,MMC/SD,MS/MSP 5 IN1 CARD READER



5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,29,30,31,32,33,34,35,36,37,39,40,41,43,45,46,47]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5138 & CR SOCKET	1A

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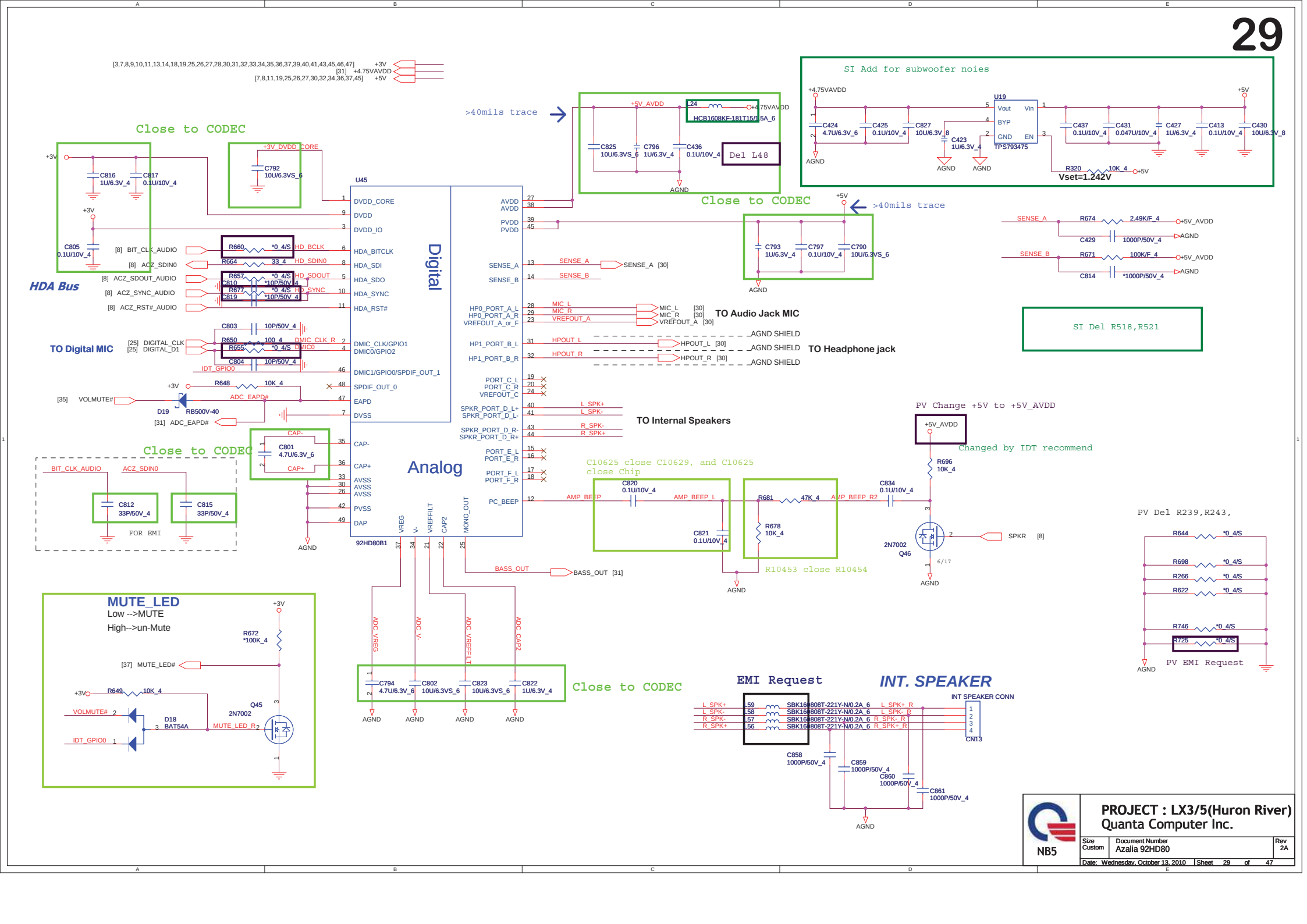

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Azalia 92HD80	2A

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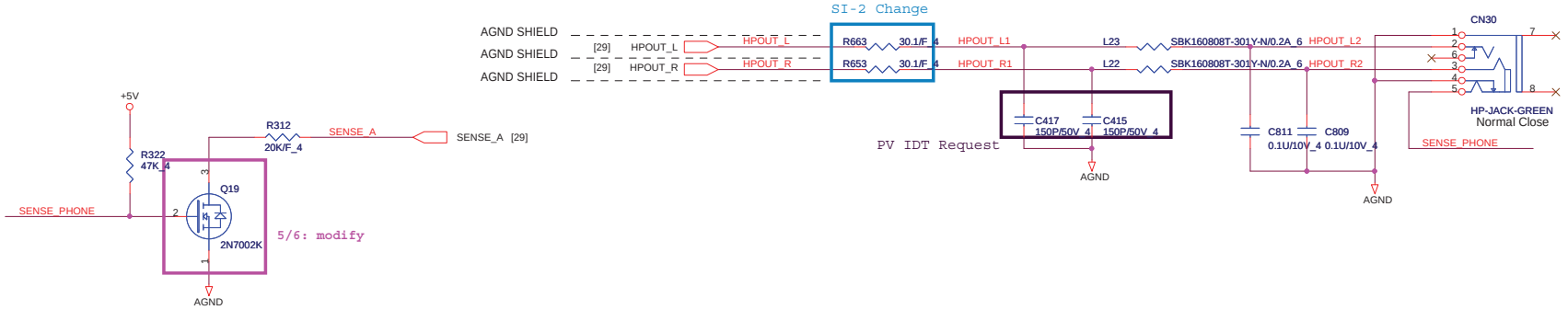
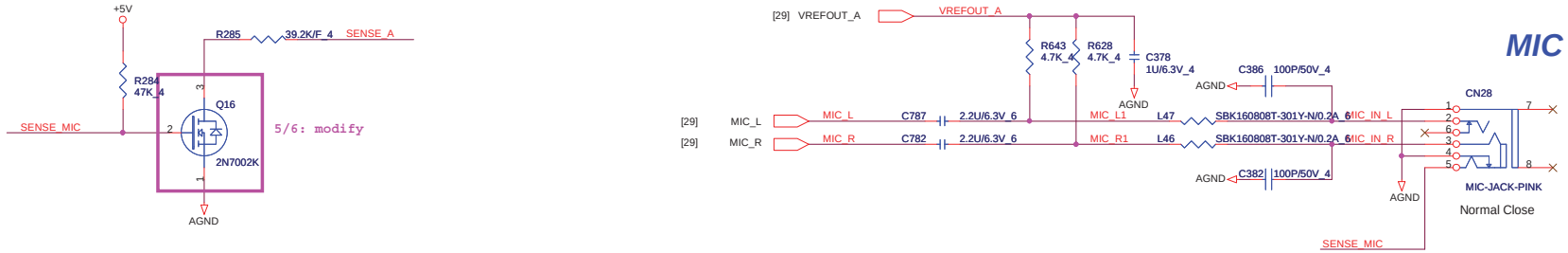
Line out

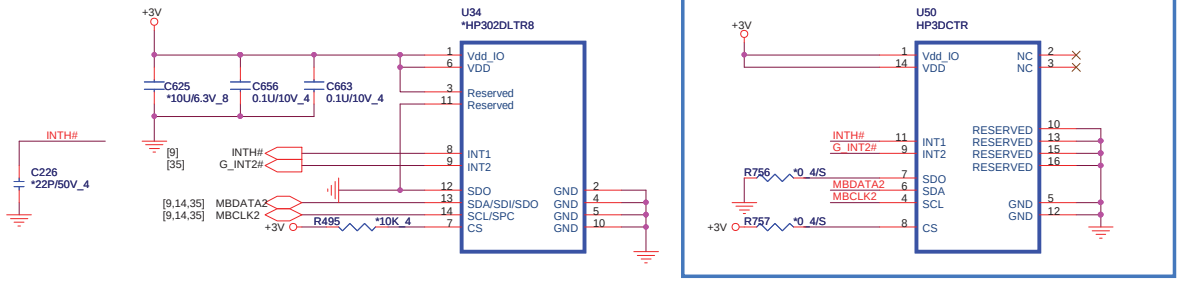


MIC



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

Accelerometer Sensor



Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Audio Jack/Accelerometer	1A

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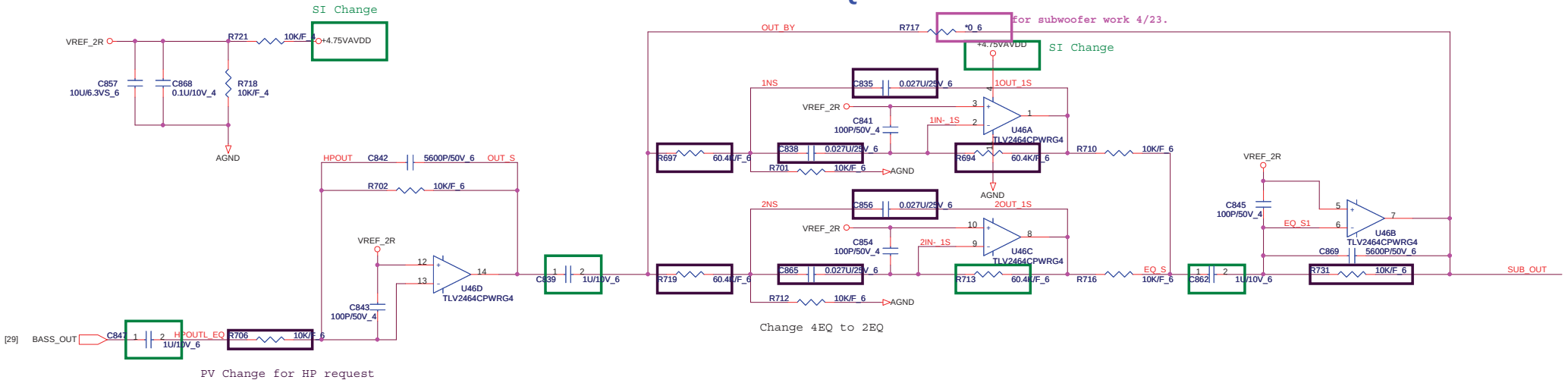
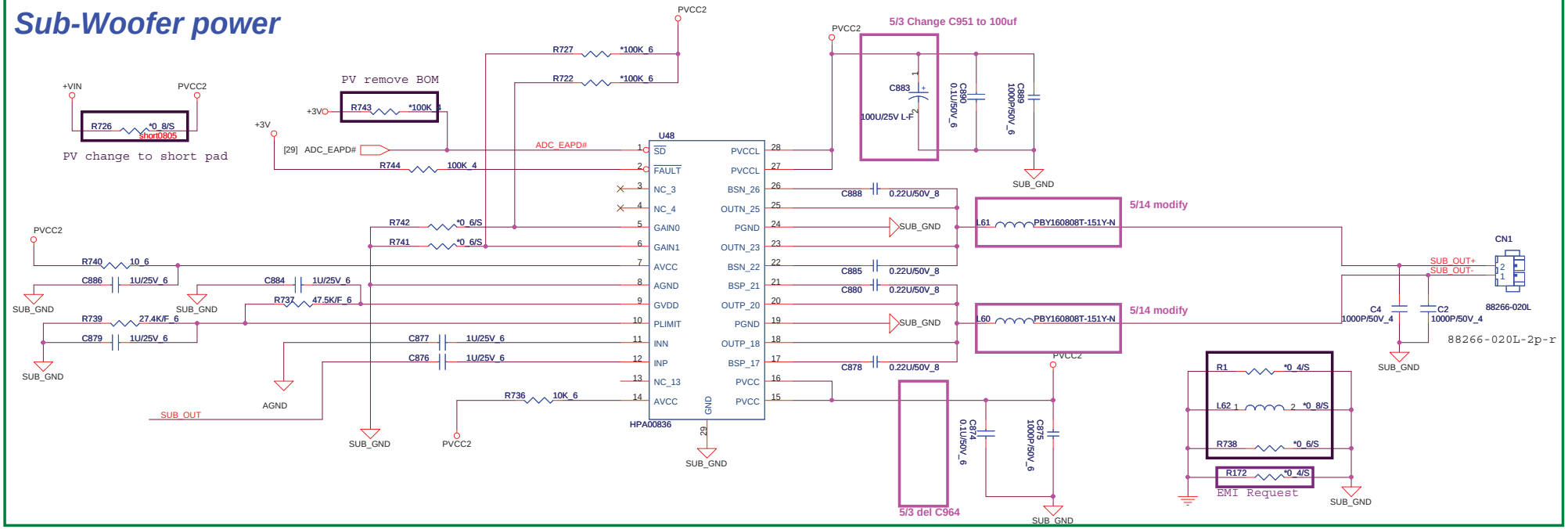
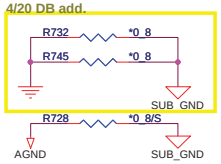
EQ FOR SUBWOOFER



Sub-Woofer power



4/20 DB add.



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

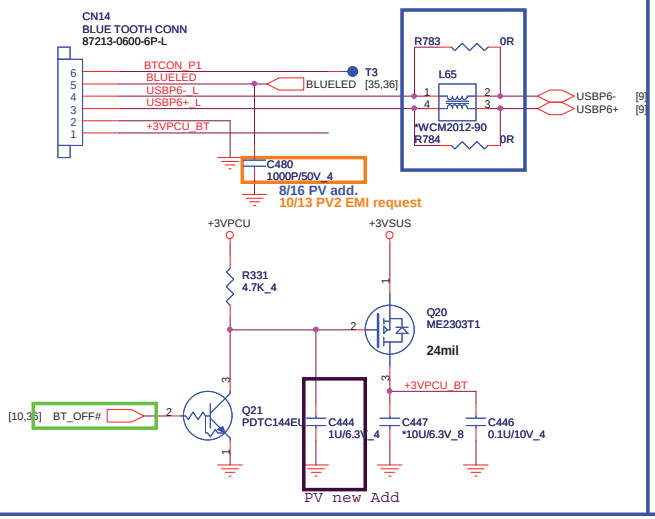
+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,32,33,34,35,36,37,39,40,41,43,44]
+4.75VADD [29]
+VIN [25,38,39,41,42,43,44,45]

NB5

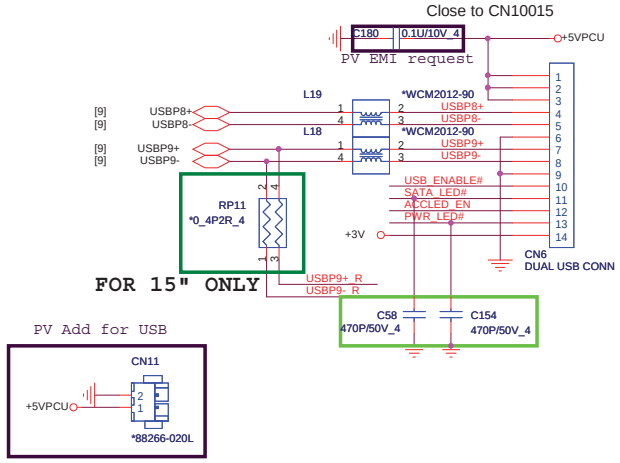
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SUBWOOFER (EQ & AMP.)	1A
Date: Wednesday, October 13, 2010	Sheet 31 of 47	

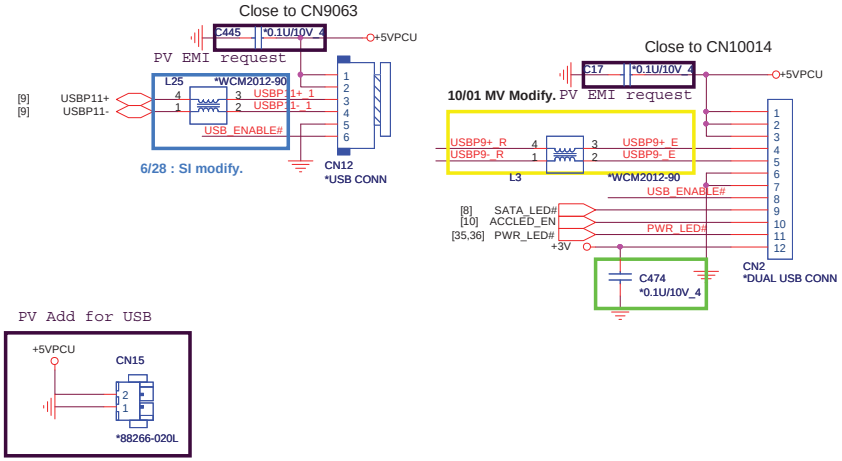
BLUETOOTH



RIGHT SIDE USBX2 for 17"

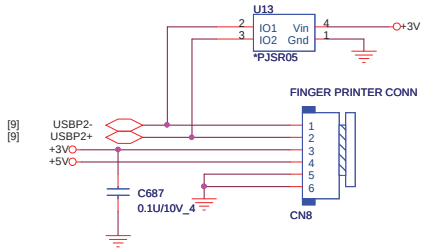


RIGHT SIDE USB for 15"

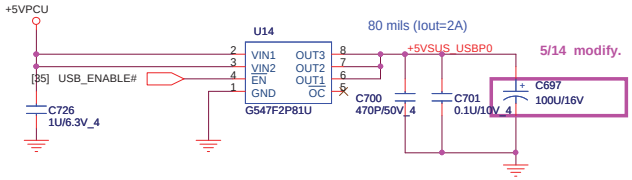


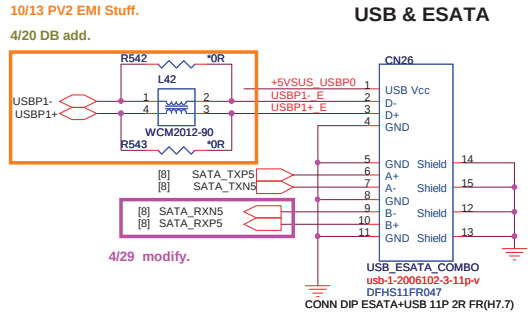
USB fingerprint CON

1. USBP2-
2. USBP2+
3. +3V
4. +5V
5. SYSTEM GND
6. SYSTEM GND

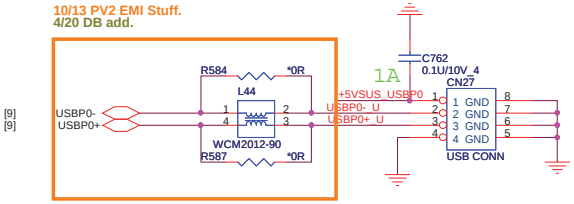


E-SATA

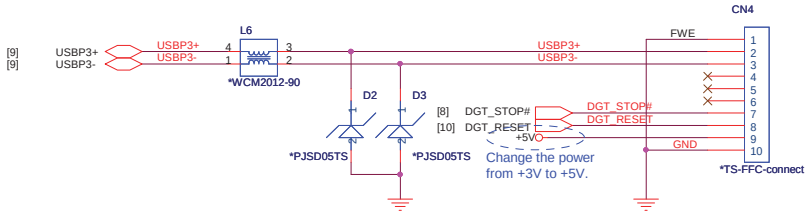




LEFT USB PORT



Touch screen for 15"



NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT/WC/FT/Touchscreen	1A

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For EMI 0 ~ 22 ohm

9/29: Modify footprint

4/23 modify AL08111DB00 RTL8111DL-GR 4/23 modify

4/29 modify

10/13 PV2 EMI Request

GND VIA x 9 Pcs

Close to Pin 35/34

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

Power trace Layout 寬度> 60mil

>60mil

>60mil

Trace<30 mil
Width > 60 mil

Link

4/23 modify

Close to Pin 21

RJ45

4/23 modify

FOR EMI

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	RTL 8111EL/RJ45	1A

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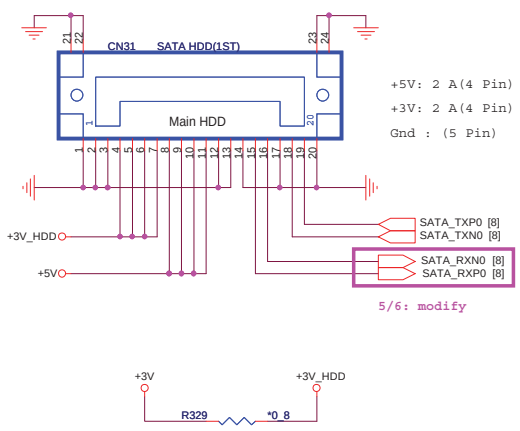
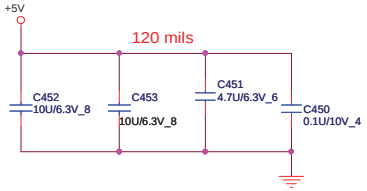
SATA HDD CONNECTOR

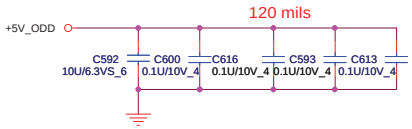
DFHD20MR005

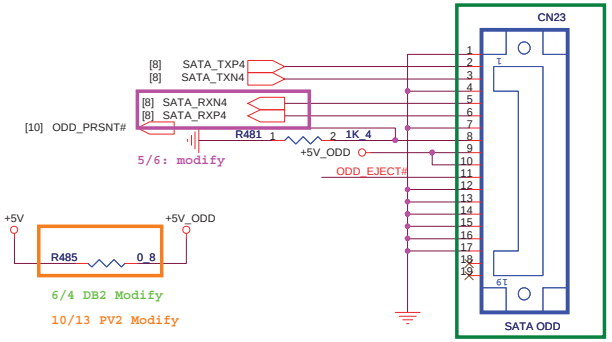
DC Current rating: 0.5 A





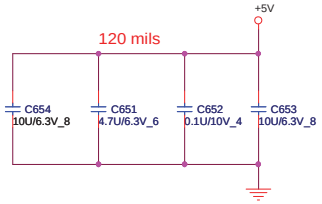
SATA CD-ROM

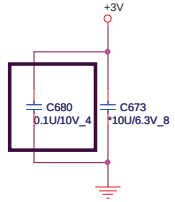




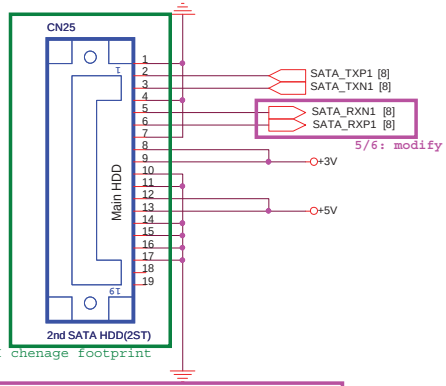
SI chenage footprint

SATA_2 CONNECTOR FOR 17.3"



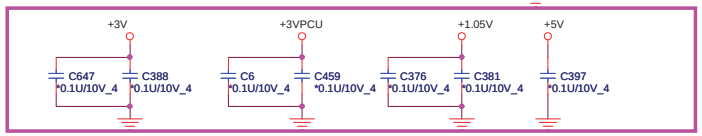


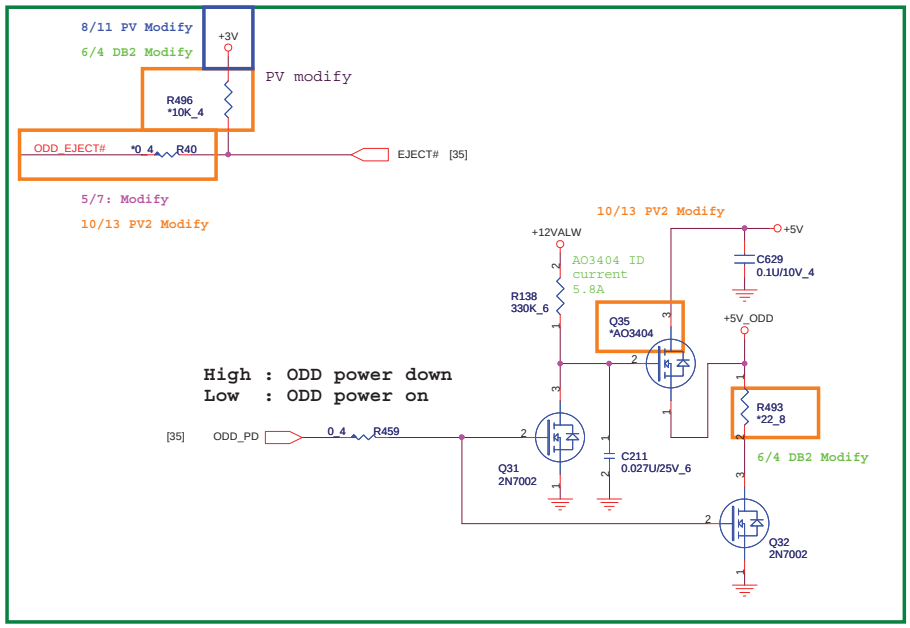
PV EMI request



SI chenage footprint

5/6: EMI request reserve





+3VPCU [7,8,25,32,35,36,37,38,39,40,42,44,45,47]
+1.05V [7,8,9,11,35,41]
+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,35,36,37,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,36,37,45]
+12VALW [25,37,42,44,45]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/ANT	1A

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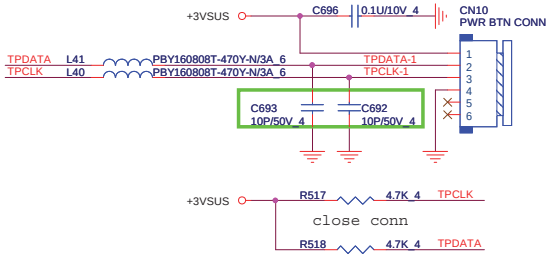
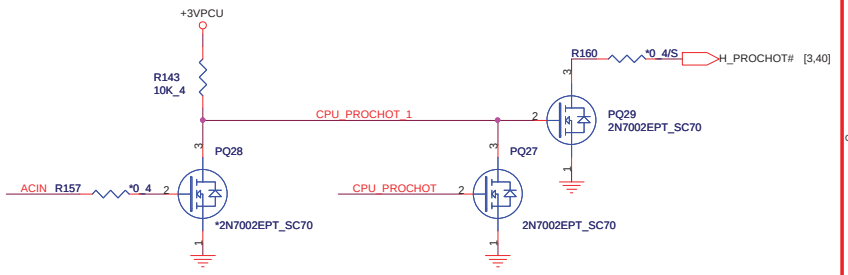
TOUCH PAD CONNECTOR & ON/OFF BOTTOM



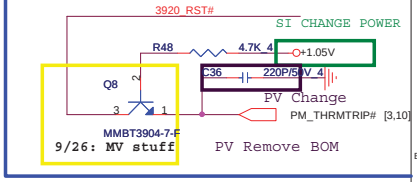
AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high

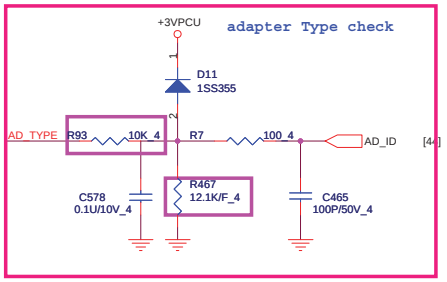
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->high

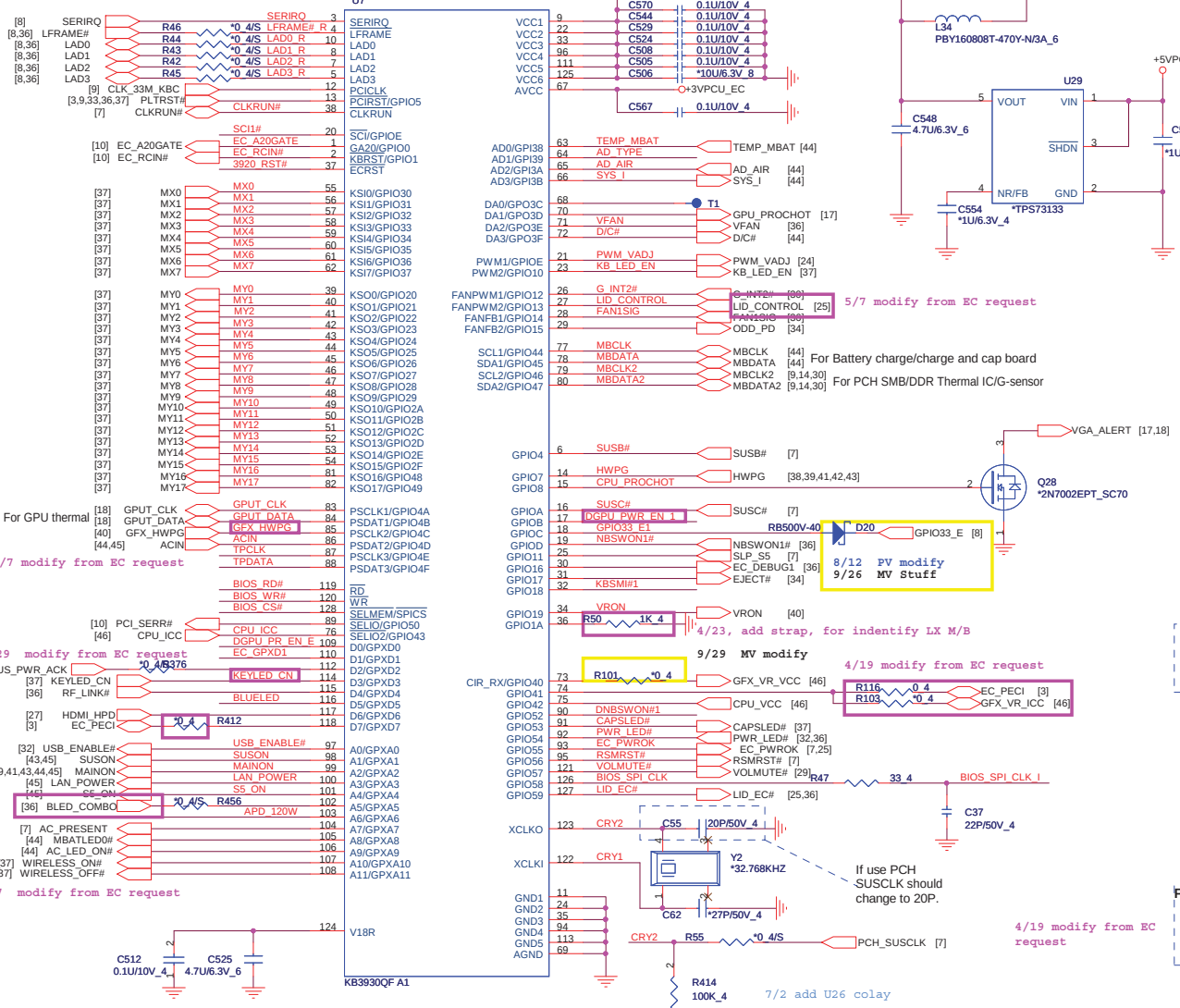
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high

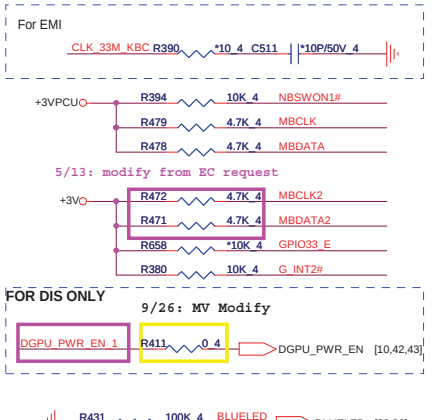


thermal shutdown circuit









	SG/DIS	UMA
R432	10K	NA
R440	NA	10K

PV Change BOM

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

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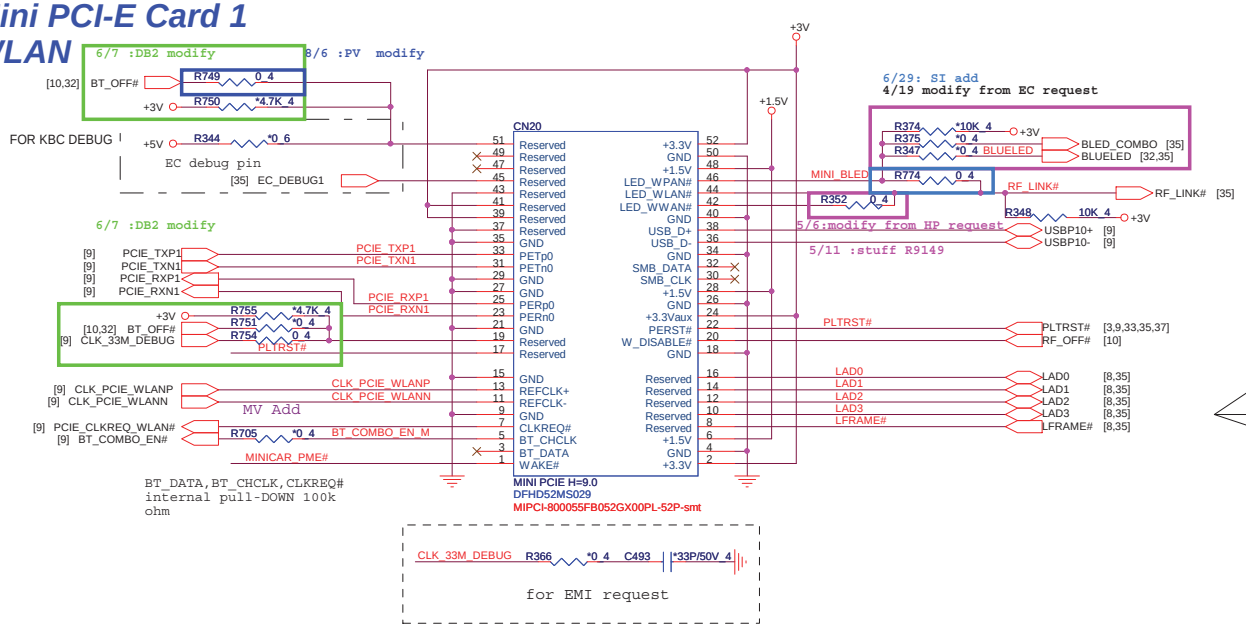
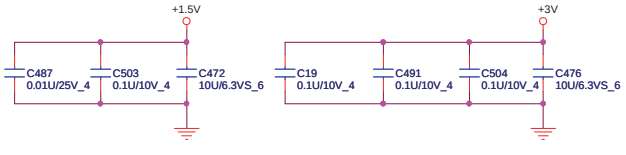
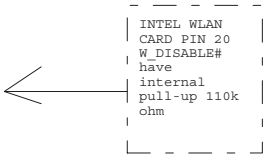
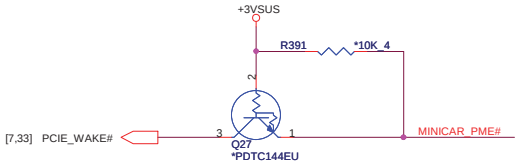
Mini PCI-E Card 1
WLAN



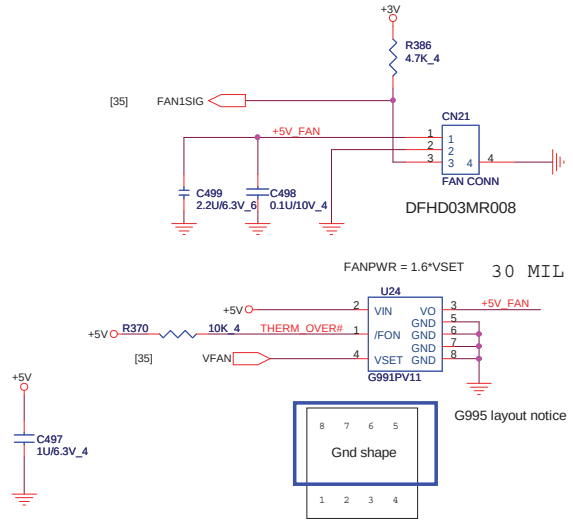




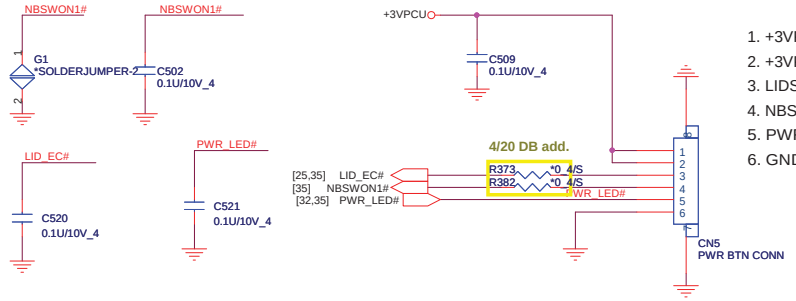


+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,37,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,34,37,45]
+1.5V [5,11,13,45]
+3VPCU [7,8,25,32,34,35,37,38,39,40,42,44,45,47]

CPU FAN



POWER BOTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. NBSWON1#
5. PWRLED#
6. GND

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN/FAN	1A

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KEYBOARD PULL-UP

RP18
10 MY1 9 MY5 8 MY0 7 MY9 6
1 MY2 2 MY4 3 MY7 4 MY8 5
+3VPCU
*8.2K_10P8R_6
8/6: PV del
RP19
10 MY13 9 MY12 8 MY3 7 MY6 6
1 MY14 2 MY11 3 MY10 4 MY15 5
*8.2K_10P8R_6
R470 *8.2K_4 MY16
R469 *8.2K_4 MY17

MY5 C308 220P/50V_4
MY6 C301 220P/50V_4
MY3 C299 220P/50V_4
MY7 C303 220P/50V_4
MY8 C302 220P/50V_4
MY9 C314 220P/50V_4
MY10 C294 220P/50V_4
MY11 C295 220P/50V_4

MY1 C307 220P/50V_4
MY2 C305 220P/50V_4
MY4 C304 220P/50V_4
MY0 C311 220P/50V_4
MX4 C313 220P/50V_4
MX6 C315 220P/50V_4
MX3 C309 220P/50V_4
MX2 C310 220P/50V_4

MX7 C316 220P/50V_4
MX0 C306 220P/50V_4
MX5 C312 220P/50V_4
MX1 C317 220P/50V_4
MY12 C298 220P/50V_4
MY13 C297 220P/50V_4
MY14 C296 220P/50V_4
MY15 C293 220P/50V_4
MY16 C292 220P/50V_4
MY17 C291 220P/50V_4

clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

SI Add

PV Change BOM
+5V
R505 1K_4
R519 *200/F_6
WIRELESS_ON_R
[35] WIRELESS_ON#
Q36 PDTC144EU

PV Change BOM
+5V
R531 1K_4
R525 *200/F_6
WIRELESS_OFF_R
[35] WIRELESS_OFF#
Q38 PDTC144EU

[35] MY[0..17] MY[0..17]
[35] MX[0..7] MX[0..7]

KB CONN
MX1 32 MX7 31 MX6 30 MY9 29 MX4 28 MX5 27 MY0 26 MX2 25 MX3 24 MY5 23 MY1 22 MX0 21 MY2 20 MY4 19 MY7 18 MY8 17 MY6 16 MY3 15 MY12 14 MY13 13 MY14 12 MY11 11 MY10 10 MY15 9 MY16 8 MY17 7
WIRELESS_ON_R 6
WIRELESS_OFF_R 5
[29] MUTE_LED# R533 200/F_4 4
[35] CAPSLED# R528 200/F_4 3
+3V 2
[35] KEYLED_CN R415 1K_4 KEYLED_CN_R 1
R416 100K_4
C300 0.1U/10V_4
CN9
MV Add

KB backlight for 15"

+5V
+12VALW R164 *100K_4
R161 *1M_4
C274 *0.01U/25V_4
[35] KB_LED_EN
Q11 *2N7002K
Q12 *AO3404
140 mA
+5V_LED_KBLIGHT
C679 *0.1U/10V_4
C678 *0.1U/10V_4
CN7
*KB LIGHT CONN
DFFC04FR042
88513-0401-4p-l-smt
4.LEDVCC
3. LEDVCC
2. GND
1. GND

12: 30 112 50 119 56 51 13 123 62 126 76 91 94
1: 110 115 127 35 118 125 36 41 122 107 15 75 92 95
8: 58 16 114 21 117 28 22 27 121 90 80 93 96
9: 1 113 70 6 116 45 59 7 12 120 129 29/42 85 101 97
5: 64 31 33 71 34 32 38 37 40 39 43 86 106 104
6: 46 48 72 49 47 53 52 44 55 54 61 81 100 103
3: 2 4 73 5 3 9 8 11 10 60 84 89 99 102
2: 17 19 74 20 18 24 23 57 26 25 83 79 105 108
7 11 13 18 14 10 17 15 16 4 23 22 19 20 21 24 25 26

LED1 Wireless Enable White 27
LED2 Wireless Disable Amber 28
LED3 Mute Amber 29
LED4 Caps White 30
VCC 31 VCC 32

H17 H-C217D126P2
H16 H-C217D126P2
H14 *H-TC315BC354D118P2
H13 *H-TC315BC354D118P2
H11 *H-TC315I138BC354D118P2
H3 *H-TC315BC354D118P2
H15 *H-TC236BC354D130P2
H2 *H-TC236BC354D130P2
H1 *H-TC315BC354D118P2
H10 *H-TC315I138BC354D118P2
H4 *H-TC315BC354D118P2
H12 *H-TC315I138BC354D118P2
H5 *H-TC315I138BC354D118P2

HOLE

5/10: del H6,H7,H11,H12

GPU
H9 *H-TC276I169BC217D150P2
H6 *H-TC276I169BC217D150P2
H8 *H-TC276I169BC217D150P2
CPU

H7 *INTEL-CPU-BRACKET

5/4: add for PDC request

PAD1 *SPAD-RE118X197NP SPAD-RE118X197NP
PAD2 *SPAD-RE118X197NP SPAD-RE118X197NP

FOR SG ONLY

+3V
U41 *MC74VHC1G08DFT2G
C770 *0.1U/10V_4
[3,9,33,35,36] PLTRST#
[9] DGPU_HOLD_RST# R569 *330_4 DGPU_HIN_RST#
PEGX_RST# [15]
R570 *100K_4
6/7 :DB2 Modify

8/6 :PV Modify

FOR DIS ONLY

[3,9,33,35,36] PLTRST# PLTRST# R753 0_4 PEGX_RST# PEGX_RST# [15]

+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,39,40,41,43,45,46,47]
+5V [7,8,11,19,25,26,27,29,30,32,34,36,45]
+3VPCU [7,8,25,32,34,35,36,38,39,40,42,44,45,47]
+3V_VGA [16,17,18,19,27,42]
+12VALW [25,34,42,44,45]
+1.0V_VGA [15,17,19,43]
+1.5V_VGA [16,19,20,21,22,23,47]
+1.8V_VGA [15,17,19,42]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB	1A

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DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

5VPCU setting			
	PR123		PQ16/PQ13
	Value	P/N	
35W CPU	133k	CS41332FB06	No POP
45W CPU	130k	CS41302FB00	POP

	PL13		PC38
	Value	P/N	
35W CPU	2.2uH	DC-22C0M000	No POP
45W CPU	1.5uH	DC-15G0M000	POP

+5V +/- 5% 35W/45W CPU
Countinue current:9A/12A
Peak current :12A/15A
OCP minimum :15A/20A

DB Change
Place these CAPs close to FETs
DB Change 35W CPU NA
PV change
Rds(on) 5m ohm
Rds(on) 14m ohm
NTC need place under CPU Socket
CPU Thermal protection at 90 +/-3 degrreC

+3.3V +/- 5%
Countinue current:6A
Peak current:7.5A
OCP minimum 9A

PU5 RT8206B
PU17
PQ16 RJK03B9D
PQ47 RJK03B9D
PQ13 RJK03D3D
PQ46 RJK03D3D
PQ49 AON7410
PQ48 AON7702
PD8 UDZ5V6B-7-F
PD11 BAS316/DG

+VIN [25,31,39,41,42,43,44,45]
+3VPCU [7,8,25,32,34,35,36,37,39,40,42,44,45,47]
+5VPCU [32,35,39,40,41,42,43,44,45]

MAINON [35,39,41,43,44,45]
HWPG [35,39,41,42,43]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

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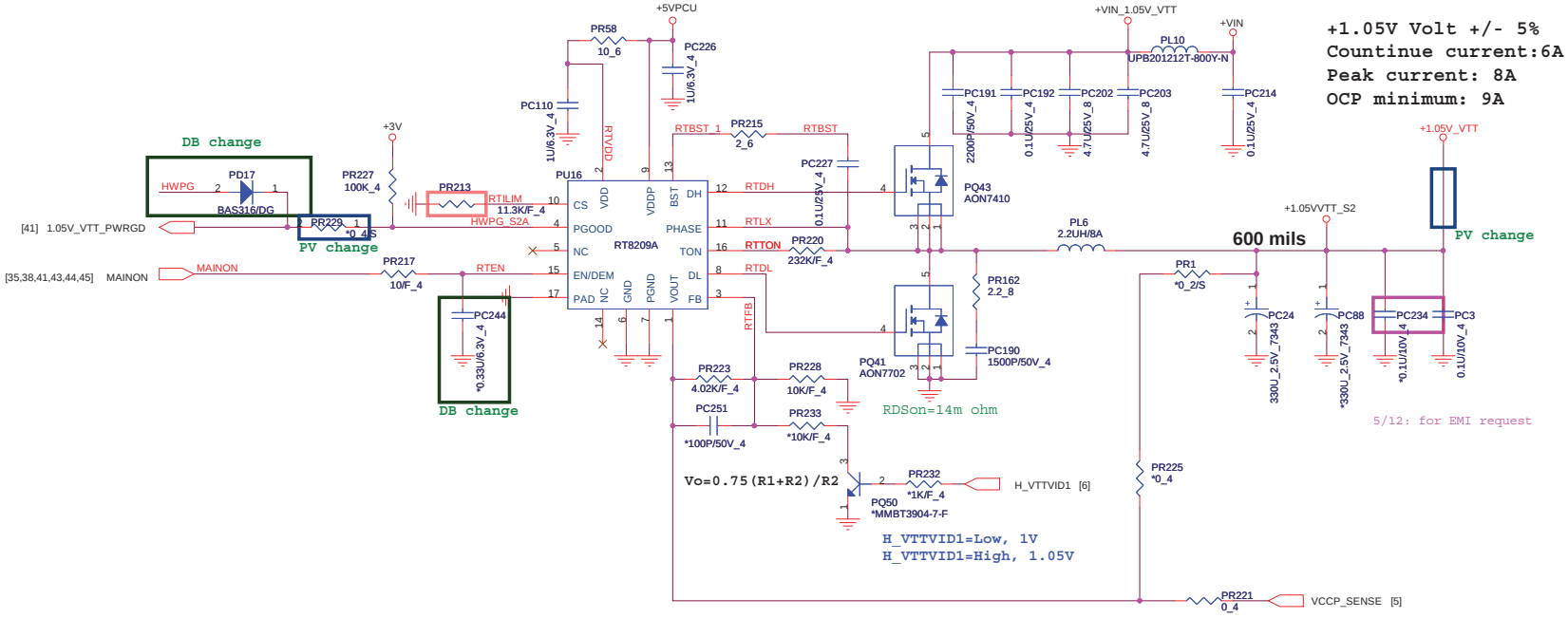

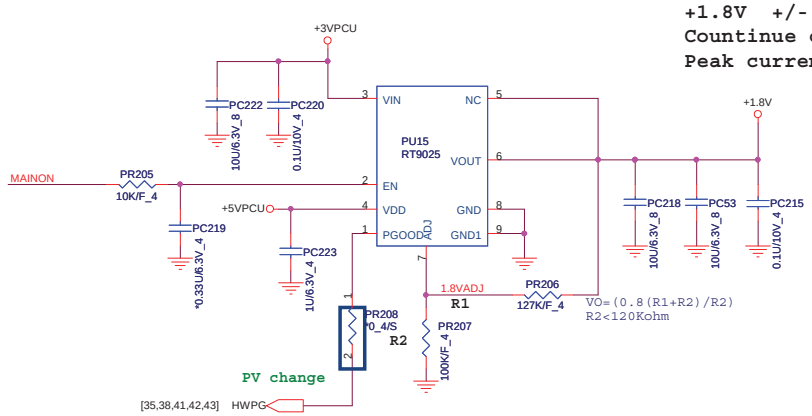

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V/+1.8V (RT8204C)	1A

NB5

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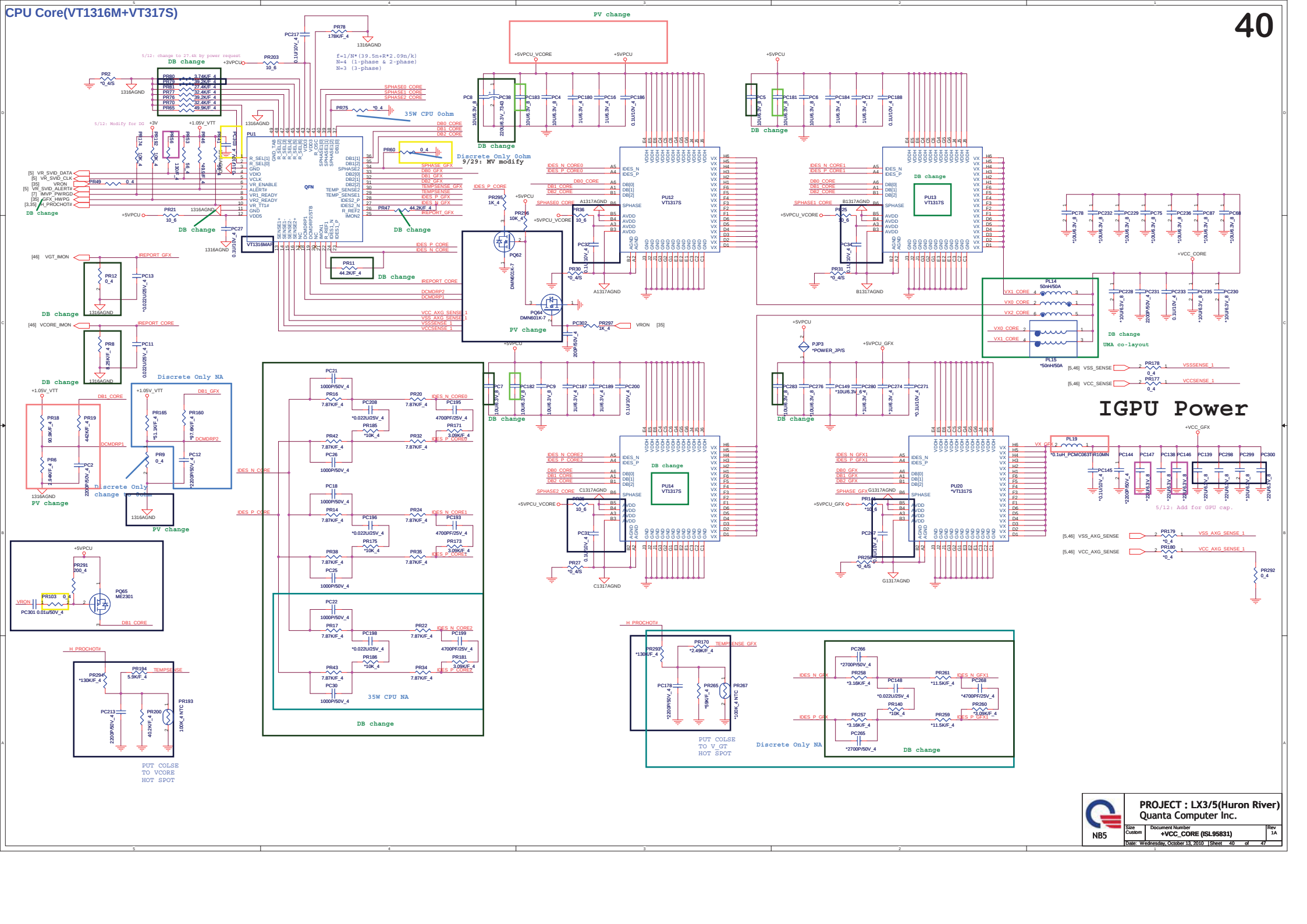
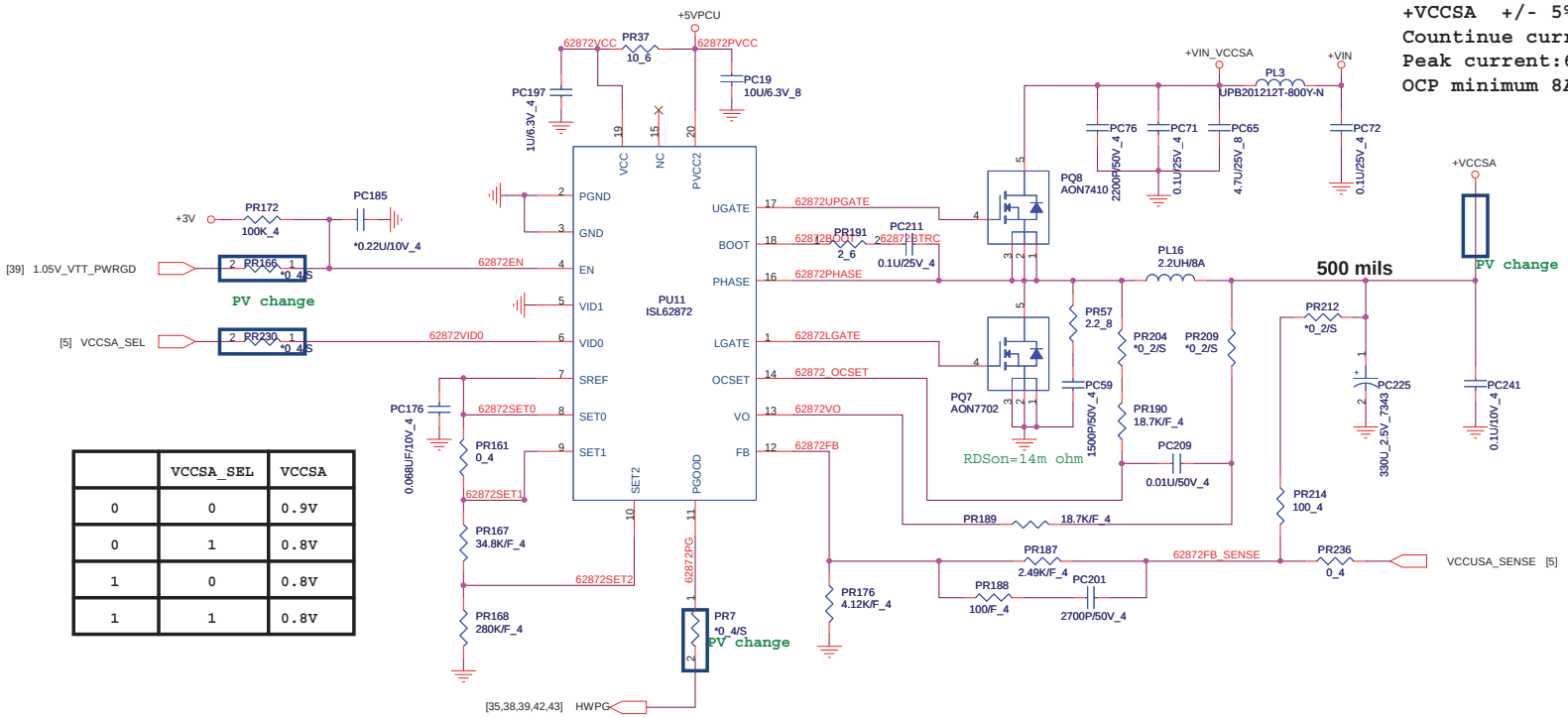
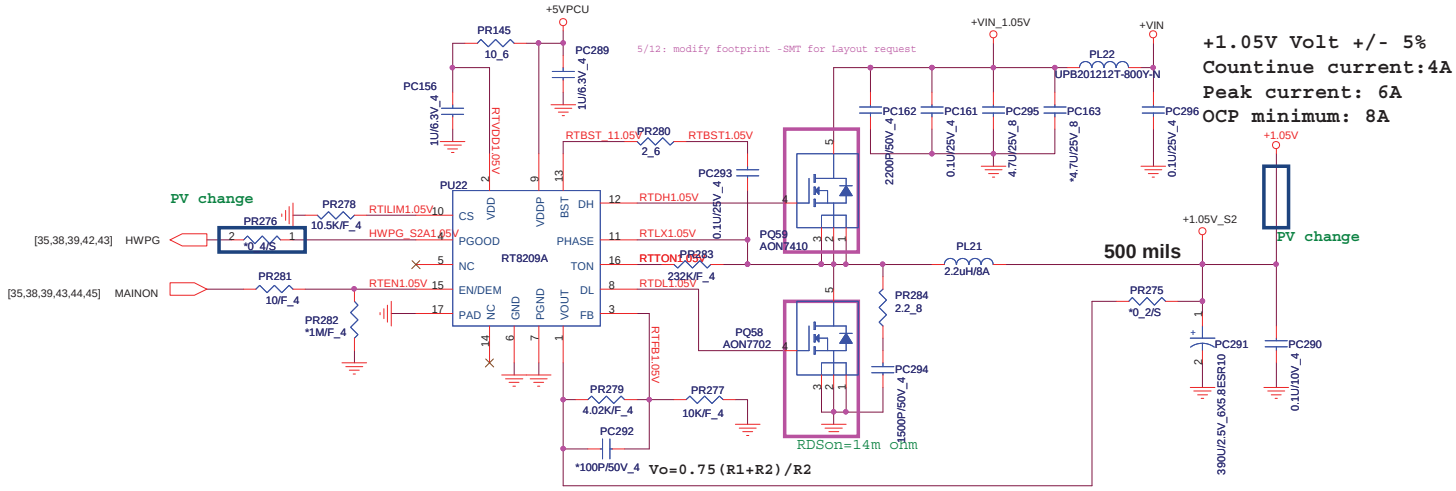

PV change
DB change
35W CPU 0ohm
Discrete Only 0ohm
9/29: MV modify
Discrete Only NA
35W CPU NA
PUT COLSE TO VCORE HOT SPOT
PUT COLSE TO V_GT HOT SPOT
IGPU Power
PROJECT : LX3/5(Huron River)
Quanta Computer Inc.
+VCC_CORE (ISL95831)
NB5

+VCCSA +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum 8A

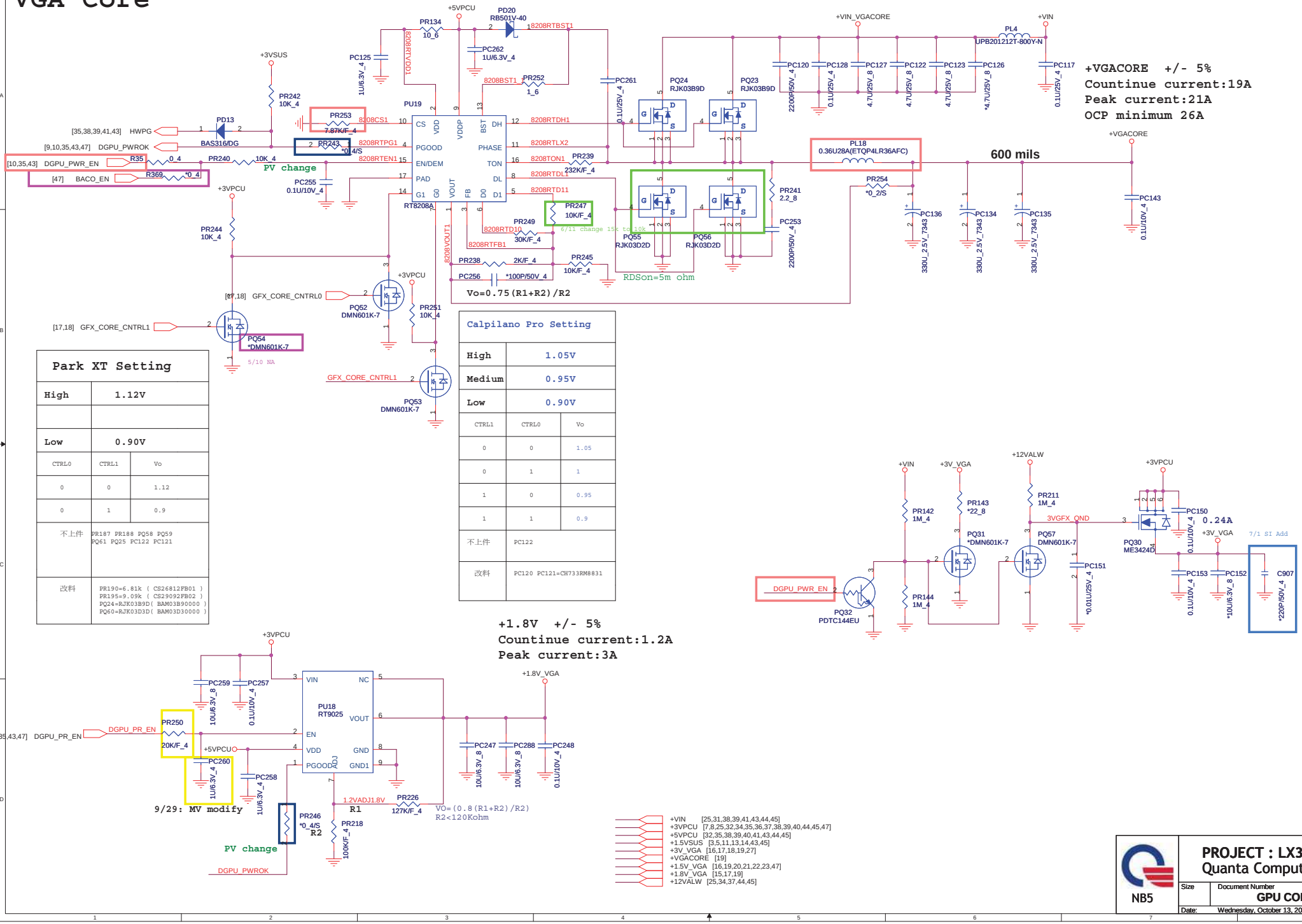
	VCCSA_SEL	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.8V
1	1	0.8V



+1.05V Volt +/- 5%
Countinue current:4A
Peak current: 6A
OCP minimum: 8A



VGA Core



Park XT Setting

High	1.12V	
Low	0.90V	
CTRL0	CTRL1	Vo
0	0	1.12
0	1	0.9
不上件	PR187 PR188 PQ58 PQ59 PQ61 PQ25 PC122 PC121	
改料	PR190=6.81k (CS26812FB01) PR195=9.09k (CS29092FB02) PQ24=RJK03B9D(BAM03B90000) PQ60=RJK03D3D(BAM03D30000)	

Calpilano Pro Setting

High	1.05V	
Medium	0.95V	
Low	0.90V	
CTRL1	CTRL0	Vo
0	0	1.05
0	1	1
1	0	0.95
1	1	0.9
不上件	PC122	
改料	PC120 PC121=CH733RM8831	

+VIN [25,31,38,39,41,43,44,45]
+3VPCU [7,8,25,32,34,35,36,37,38,39,40,44,45,47]
+5VPCU [32,35,38,39,40,41,43,44,45]
+1.5VSUS [3,5,11,13,14,43,45]
+3V_VGA [16,17,18,19,27]
+VGACORE [19]
+1.5V_VGA [16,19,20,21,22,23,47]
+1.8V_VGA [15,17,19]
+12VALW [25,34,37,44,45]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
	GPU CORE(ISL6264)	1A
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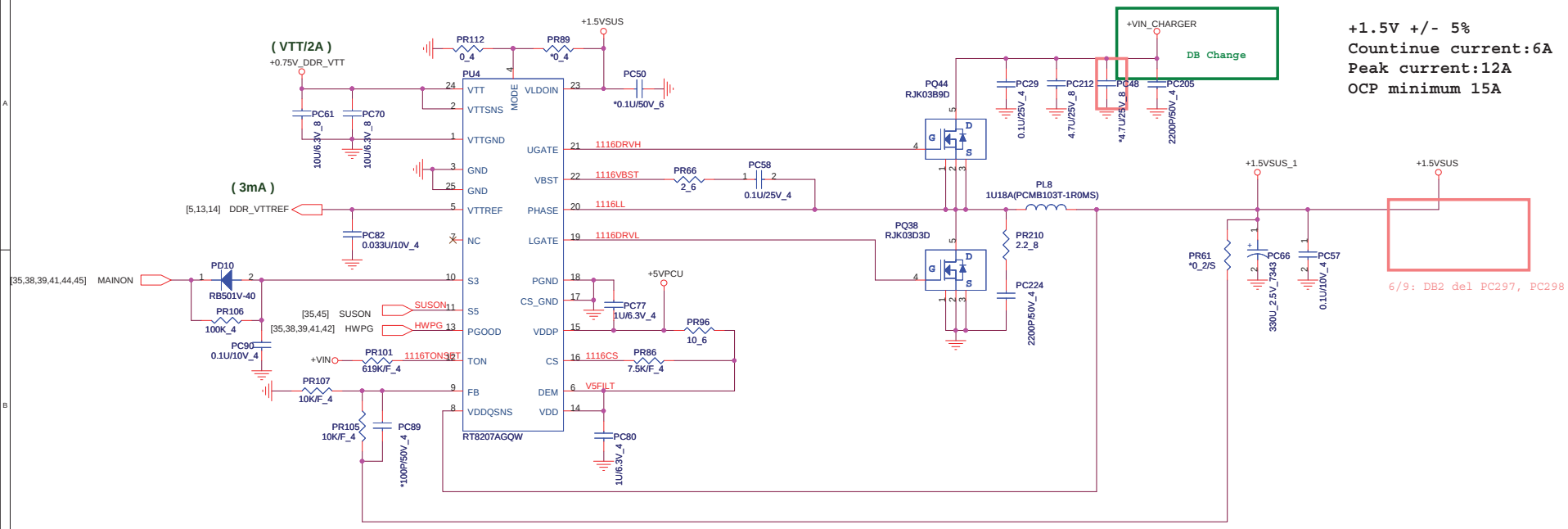
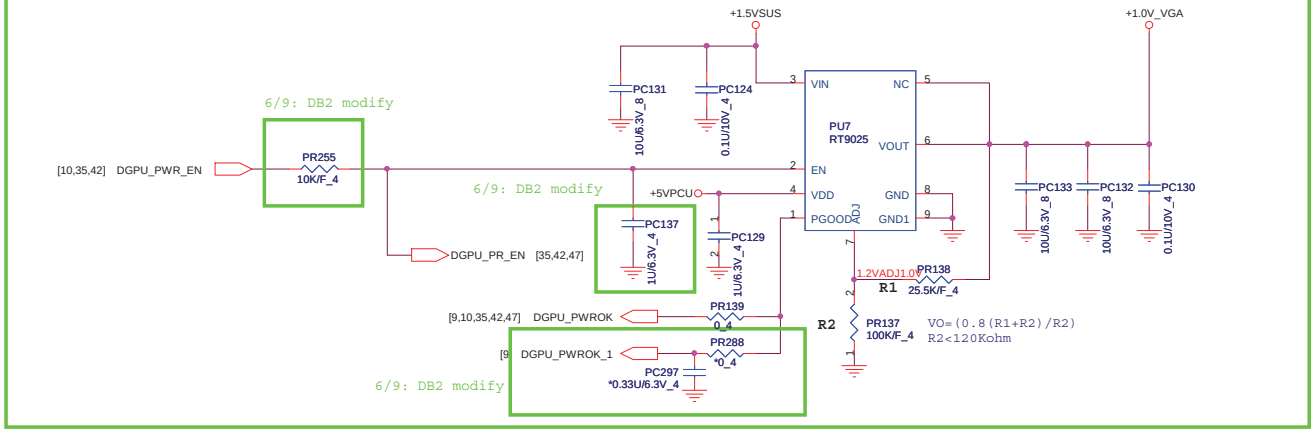
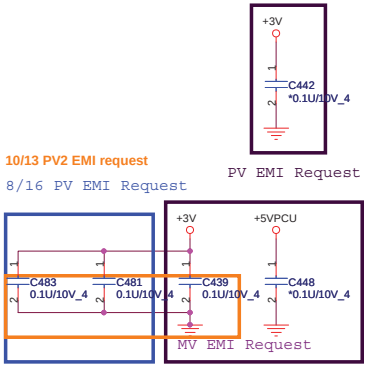


SG & Discrete Only

+1.0V +/- 5%
Countinue current:1.7A
Peak current:3A





+3V [3,7,8,9,10,11,13,14,18,19,25,26,27,28,29,30,31,32,33,34,35,36,37,39,40,41,45,46,47]
+VIN [25,31,38,39,41,42,44,45]
+5VPCU [32,35,38,39,40,41,42,44,45]
+1.5VSUS [3,5,11,13,14,45]
+1.0V_VGA [15,17,19]
+0.75V_DDR_VTT [13,14,45]

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

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TOP DC_JACK
65W/90W

6/28: SI modify footprint

5/12: Mpdify footprint -SMT for layout request

6/30:SI Add

Do Not add test pad on BATDIS_G signal

PV change

15.6" DFHD08MR094
17.3" DFHD08MR096

CN18
DC-IN CONN

PU6
OZ8681

6/11: DB2 modify for power request

6/9: DB2 modify footprint

Place this cap close to EC

Place this cap close to EC

+VA [45]
+VH28 [45]
+VAD_1 [45]
+3VPCU [7,8,25,32,34,35,36,37,38,39,40,42,45,47]
+5VPCU [32,35,38,39,40,41,42,43,45]
+BATCHG [45]

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Charger (BQ24704)	1A

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+VA [44]
+5V [7,8,11,19,25,26,27,29,30,32,34,36,37]
+VIN [25,31,38,39,41,42,43,44]
+1.5V [5,11,13,36]
+1.8V [5,8,11,39]
+3VS5 [3,7,8,9,10,11]
+5VS5 [11]
+VH28 [44]
+VAD_1 [44]
+3VSUS [32,35,36,42]
+5VSUS [25,38]
+3VPCU [7,8,25,32,34,35,36,37,38,39,40,42,44,47]
+5VPCU [32,35,38,39,40,41,42,43,44]
+12VALW [25,34,37,42,44]
+BATCHG [44]
+1.5VSUS [3,5,11,13,14,43]
+3VLANVCC [33]
+0.75V_DDR_VTT [13,14,43]

PD14 *RB501V-40
PD15 *RB501V-40
PR148 *22_6
PR146 22_6
PC160 0.1U/25V_4
PC164 0.1U/25V_4
PR151 *0_4/S
PC167 1U/35V_6
PC168 0.47u/25V_6
PR153 *0_4/S
PR154 750K/F_4
PR155 100K/F_4
PC174 1U/16V_4
PR150 *0_6/S
PR149 *0_6/S
PR147 *0_6/S
PR152 *0_6/S
PV change

PU8 P2806
VIN CN CP VOUT D_CAP PG VSENSE REG DISC3 DISC2 DISC1 ON1 ON2 ON3 ON4 DRIVER4 DRIVER3 DISC4 DRIVER1 DRIVER2 GND

[35] LAN_POWER
[35,38,39,41,43,44] MAINON
[35,43] SUSON
MAINON
ACIN [35,44]
G5934PG
G5934VSENSE
G5934DISC3
G5934DISC2
G5934DISC1
G5934DISC4
G5934CN
G5934CP

PQ35 AON7410
PC158 0.1U/10V_4
PC165 *10U/6.3V_8
PC159 0.1U/10V_4
PC173 2200P/50V_4
MAIND3.3V
4.6A

PQ33 ME3424D
PC154 0.1U/10V_4
PC249 *10U/6.3V_8
PC155 0.1U/10V_4
PC175 2200P/50V_4
SUSD
0.24A

PQ22 ME3424D
PC116 0.1U/10V_4
PC121 *10U/6.3V_8
PC119 0.1U/10V_4
0.1A

PQ25 *DMN601K-7
PQ26 *DMN601K-7
PR132 *22_8
PR135 *1M_4
PR136 *1M_4

PQ36 AON7410
PC170 0.1U/10V_4
PC169 2200P/50V_4
MAIND
6A

PQ34 ME3424D
PC142 0.1U/10_4
PC166 2200P/50V_4
LAN_ON
0.67A

PC172 0.1U/10V_4
PC171 *10U/6.3V_8
PC157 0.1U/10V_4
PC263 *10U/6.3V_8

PV EMI Request
4/20 Del C982,C992 for dummy net
C454 *0.1U/10V_4
C14 *0.1U/10V_4
C13 *0.1U/10V_4

5/13: reserve
PQ12 *ME3424D
PC60 *0.1U/10V_4
PC64 *0.1U/10V_4
PC74 *10U/6.3V_8
0.5A
MAIND [5]

PR84 1M_4
PR83 1M_4
PQ10 DMN601K-7
PQ4 *DMN601K-7
PQ11 *DMN601K-7
PQ51 DMN601K-7
PR67 *22_8
PR69 *22_8
PR248 22_8
MAIN_ONG
MAIN_ONG [3,5]

6/29: SI add for EMI
C899 *0.1U/50V_6
C900 *0.1U/10V_4
C901 *0.1U/10V_4
C902 *0.1U/10V_4
C903 *1500P/50V_4
C904 *100P/50V_4

7/1 : SI add for EMI
C912 *220P/50V_4
C908 *0.1U/10V_4
C910 *220P/50V_4
C909 *220P/50V_4
C911 *220P/50V_4

8/16 : PV add for EMI

PR122 1M_4
PR54 22_8
PR127 22_8
PQ9 DMN601K-7
PQ20 DMN601K-7
PR128 1M_4
PQ21 PDTC144EU
[35] S5_ON
S5_ONG

PR73 1M_4
PQ6 DMN601K-7
S5_OND
PC52 2200P/50V_4

PQ3 DMN601K-7
PC49 0.1U/10V_4
PC37 0.1U/10V_4
PC42 *10U/6.3V_8
10mA

PQ17 ME3424D
PC101 0.1U/10V_4
PC109 0.1U/10V_4
PC113 *10U/6.3V_8
0.17A

5/3: modify for leakage

NB5

PROJECT : LX3/5(Huron River)
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (P2806)	1A
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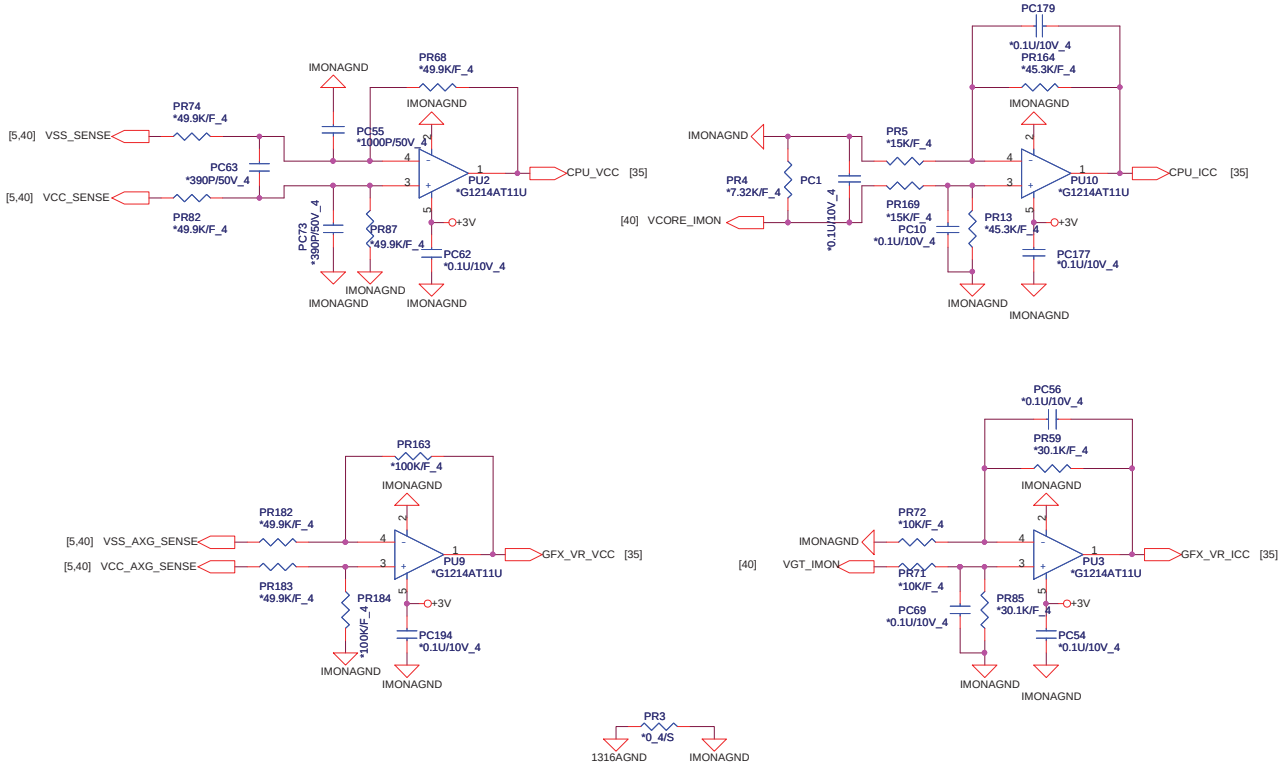

Vender	Size	P/N
EON	128KB	
	512KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031

NB5

PROJECT : LX3/5(Huron River)
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Custom	IMON	1A

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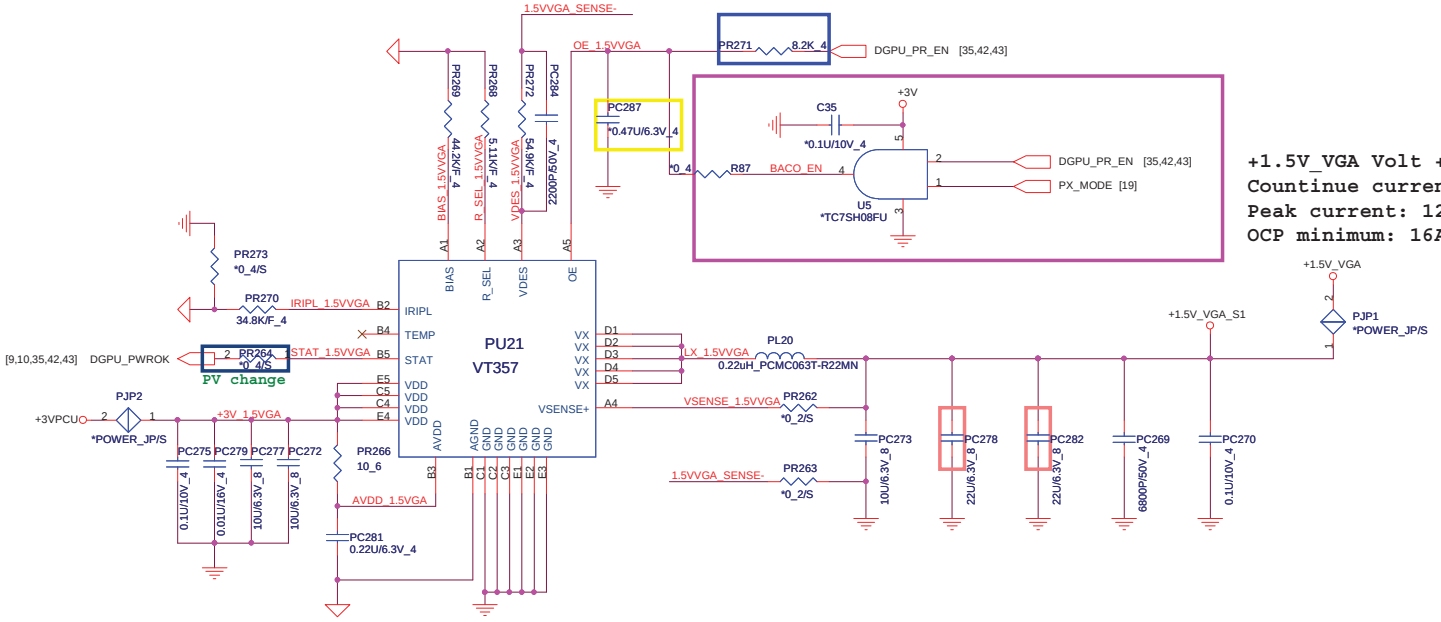
BACO_EN [42]
+1.5V_VGA [16,19,20,21,22,23]
+3VPCU [7,8,25,32,34,35,36,37,38,39,40,42,44,45]

9/29: MV modify



+1.5V_VGA Volt +/- 5%
Countinue current:8A
Peak current: 12A
OCP minimum: 16A

NB5	PROJECT : LX3/5(Huron River) Quanta Computer Inc.	
Size: Custom	Document Number: +1.5V_VGA	Rev: 1A
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