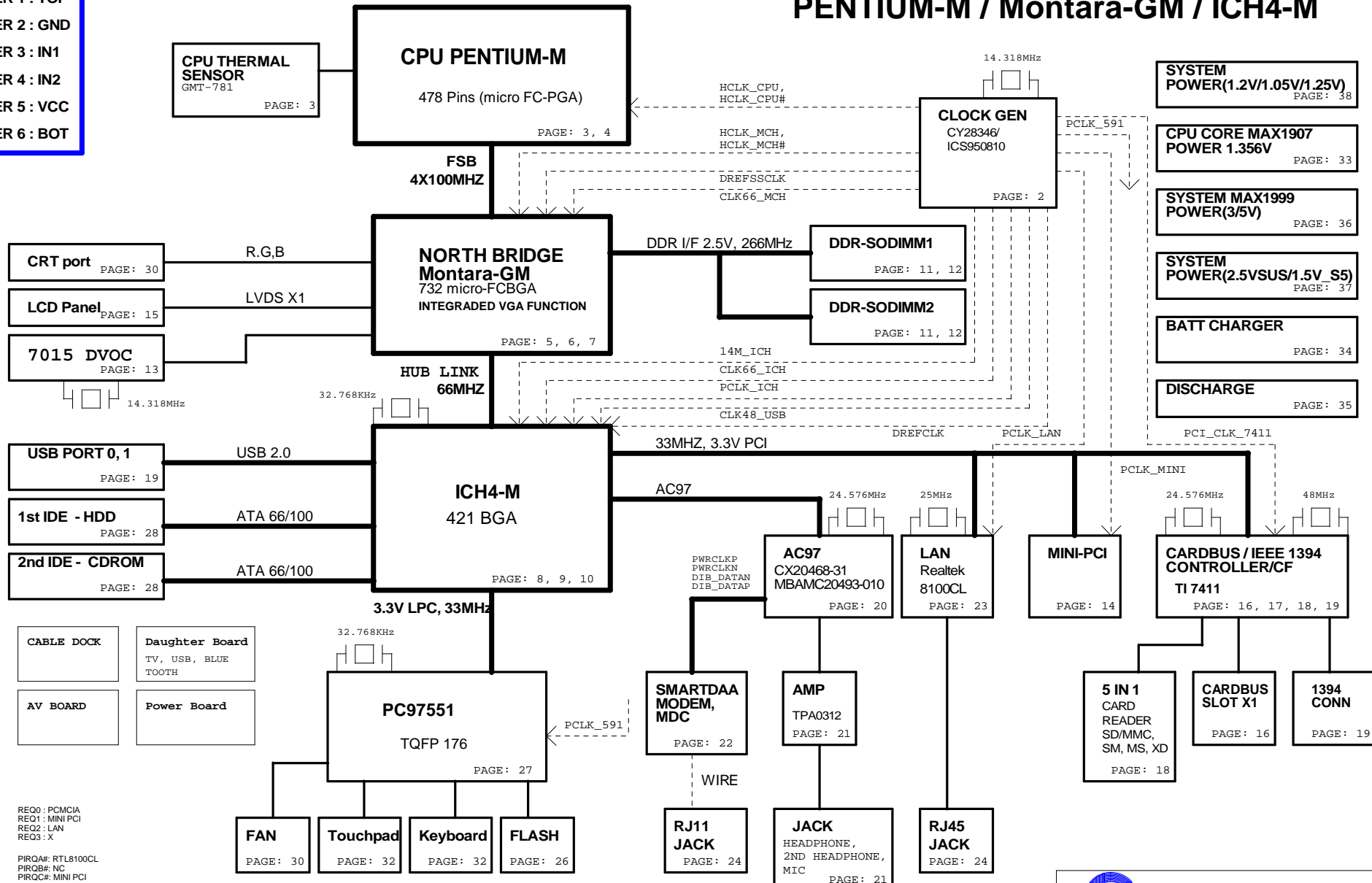


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CT1 BLOCK DIAGRAM

PENTIUM-M / Montara-GM / ICH4-M



REQ0 : PCMCIA
 REQ1 : MINI PCI
 REQ2 : LAN
 REQ3 : X

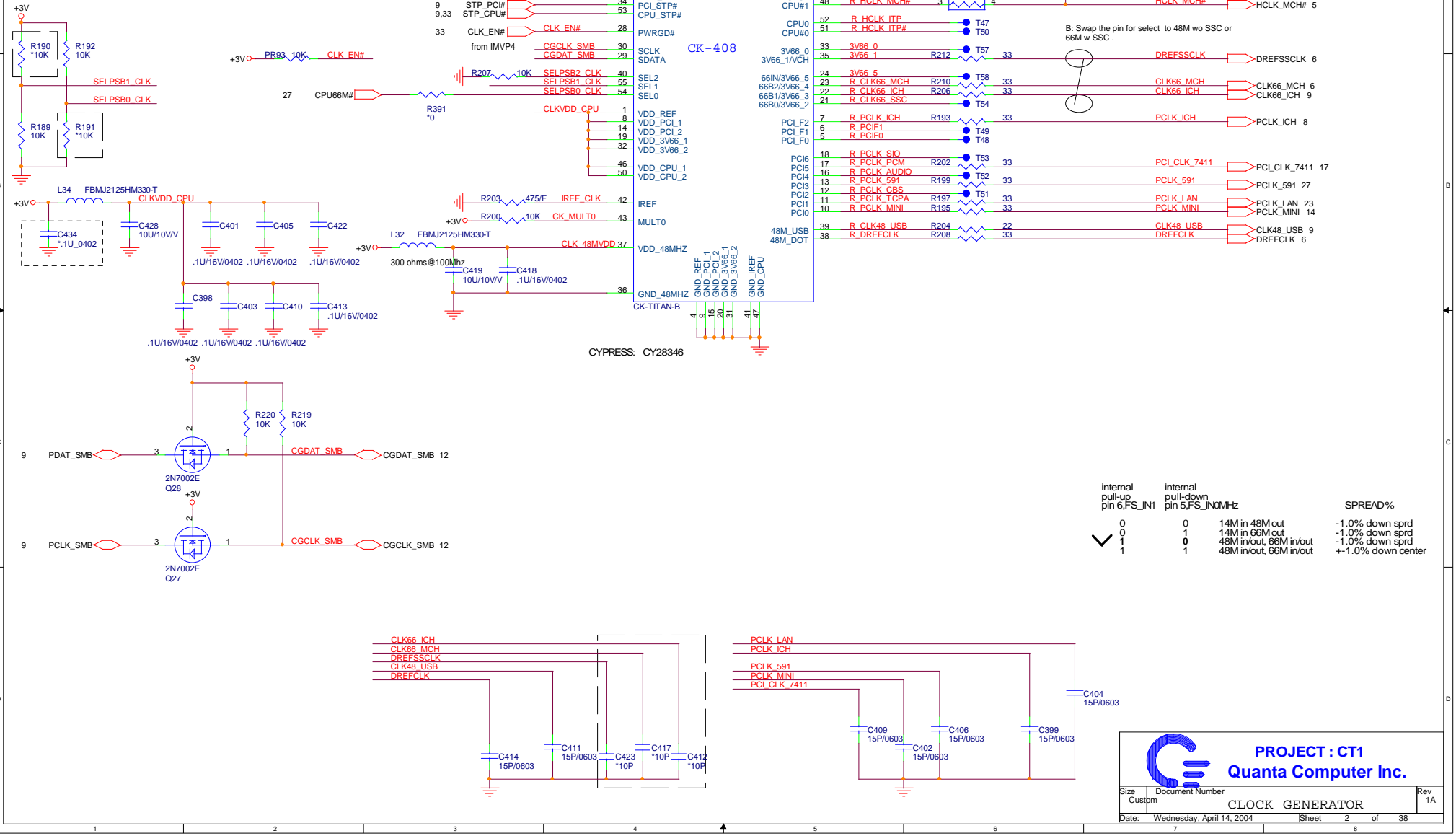
PIRQA# : RTL8100CL
 PIRQB# : NC
 PIRQC# : MINI PCI
 PIRQD# : MINI PCI
 PIRQE# : 7411
 PIRQF# : 7411
 PIRQG# : 7411
 PIRQH# : Internal USB

PROJECT : CT1
Quanta Computer Inc.

Size Custpm	Document Number BLOCK DIAGRAM	Rev 1A
Date: Wednesday, April 14, 2004	Sheet 1 of 38	

CLK GEN

S2	S1	S0	CPU	3V66[0..4]	3V66_5/66IN
1	0	0	66	66IN	66 Input
1	0	1	100	66IN	66 Input
1	1	0	200	66IN	66 Input
1	1	1	133	66IN	66 Input
0	0	0	66	66	66 Input
0	0	1	100	66	66 Input
0	1	0	200	66	66 Input
0	1	1	133	66	66 Input



B: Swap the pin for select to 48M wo SSC or 66M w SSC.

internal pull-up pin 6,FS_IN1	internal pull-down pin 5,FS_IN0MHz		SPREAD%
0	0	14M in 48M out	-1.0% down sprd
0	1	14M in 66M out	-1.0% down sprd
1	0	48M in/out, 66M in/out	-1.0% down sprd
1	1	48M in/out, 66M in/out	+1.0% down center

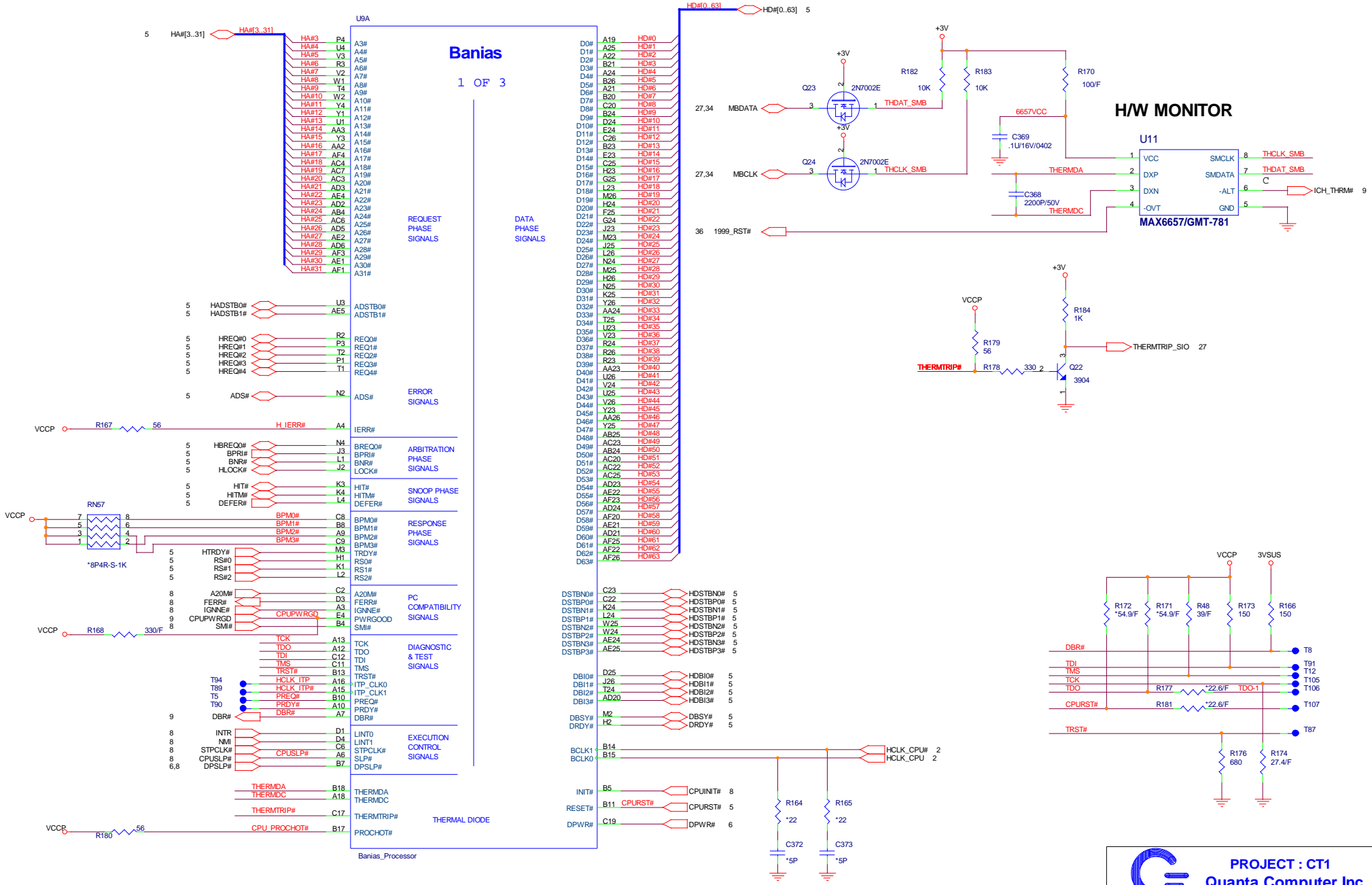
PROJECT : CT1
Quanta Computer Inc.

Size	Document Number	Rev
Custm	CLOCK GENERATOR	1A
Date:	Wednesday, April 14, 2004	Sheet 2 of 38

BANIAS CPU 1 of 2 (HOST BUS)

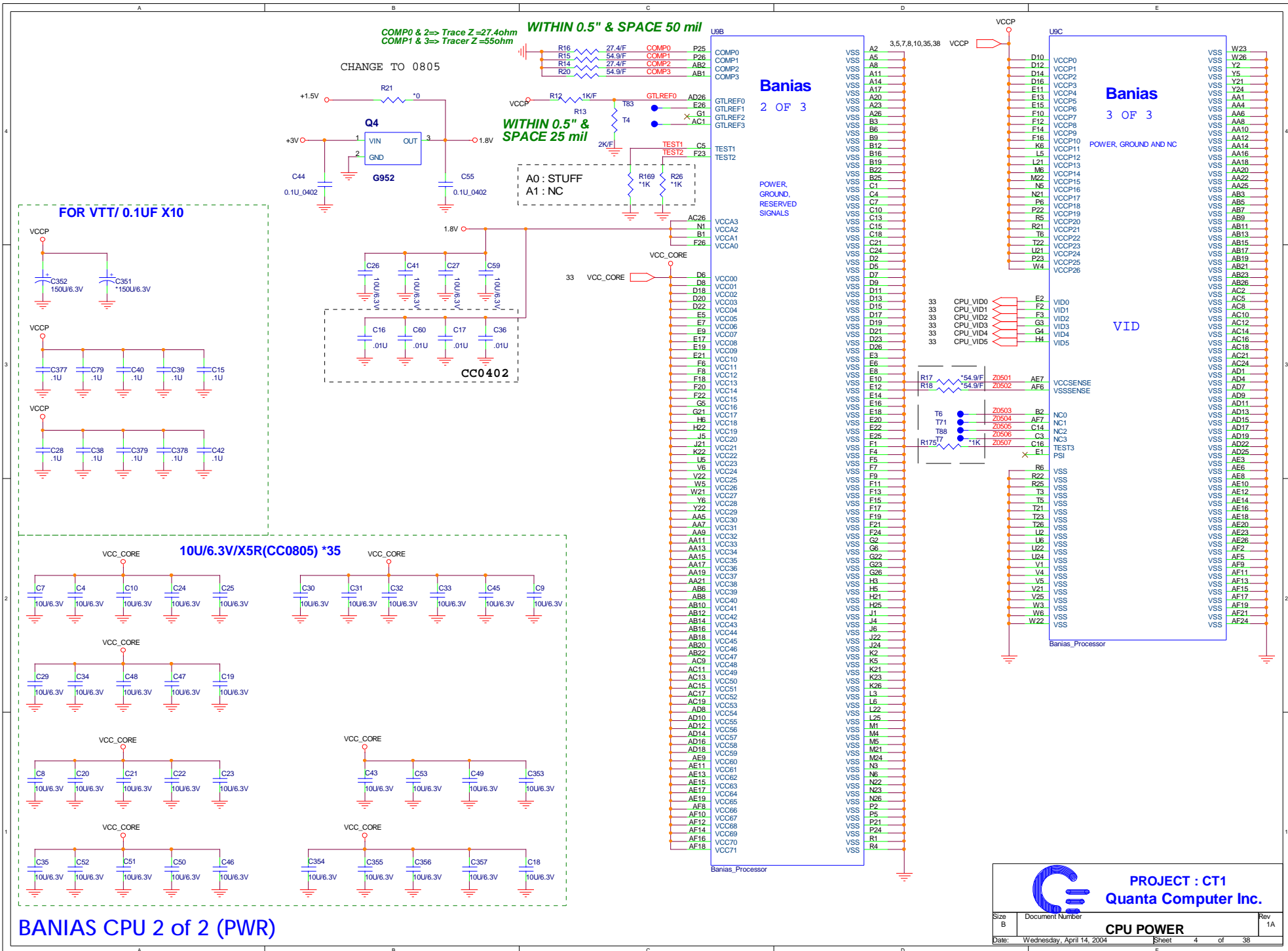
Banias
1 OF 3

Banias_Processor



PROJECT : CT1
Quanta Computer Inc.

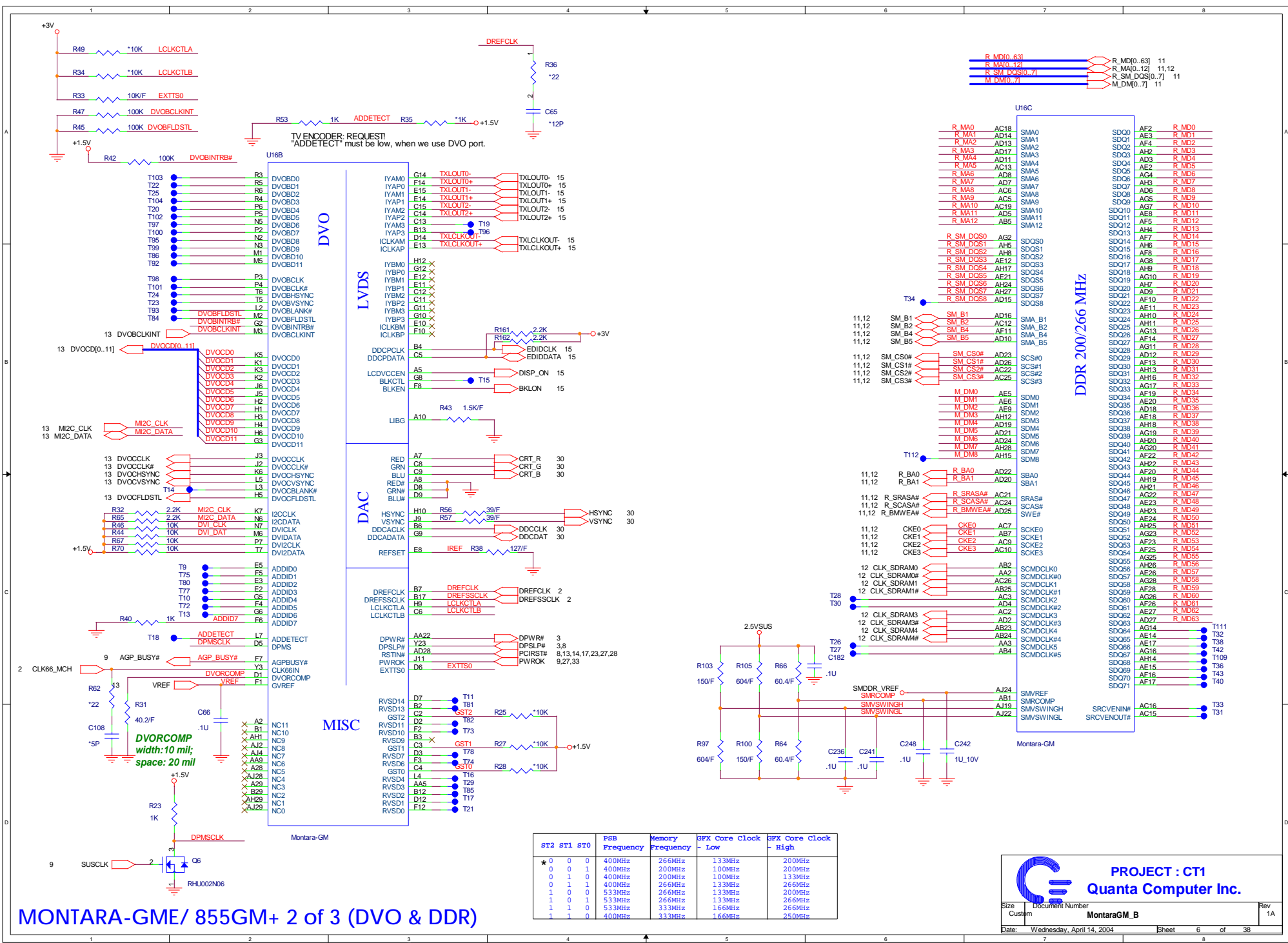
Size	Document Number	Rev
Custom		1A
Date:	Wednesday, April 14, 2004	Sheet 3 of 38



BANIAS CPU 2 of 2 (PWR)

PROJECT : CT1
Quanta Computer Inc.

Size B	Document Number	Rev
	CPU POWER	1A
Date:	Wednesday, April 14, 2004	Sheet 4 of 38



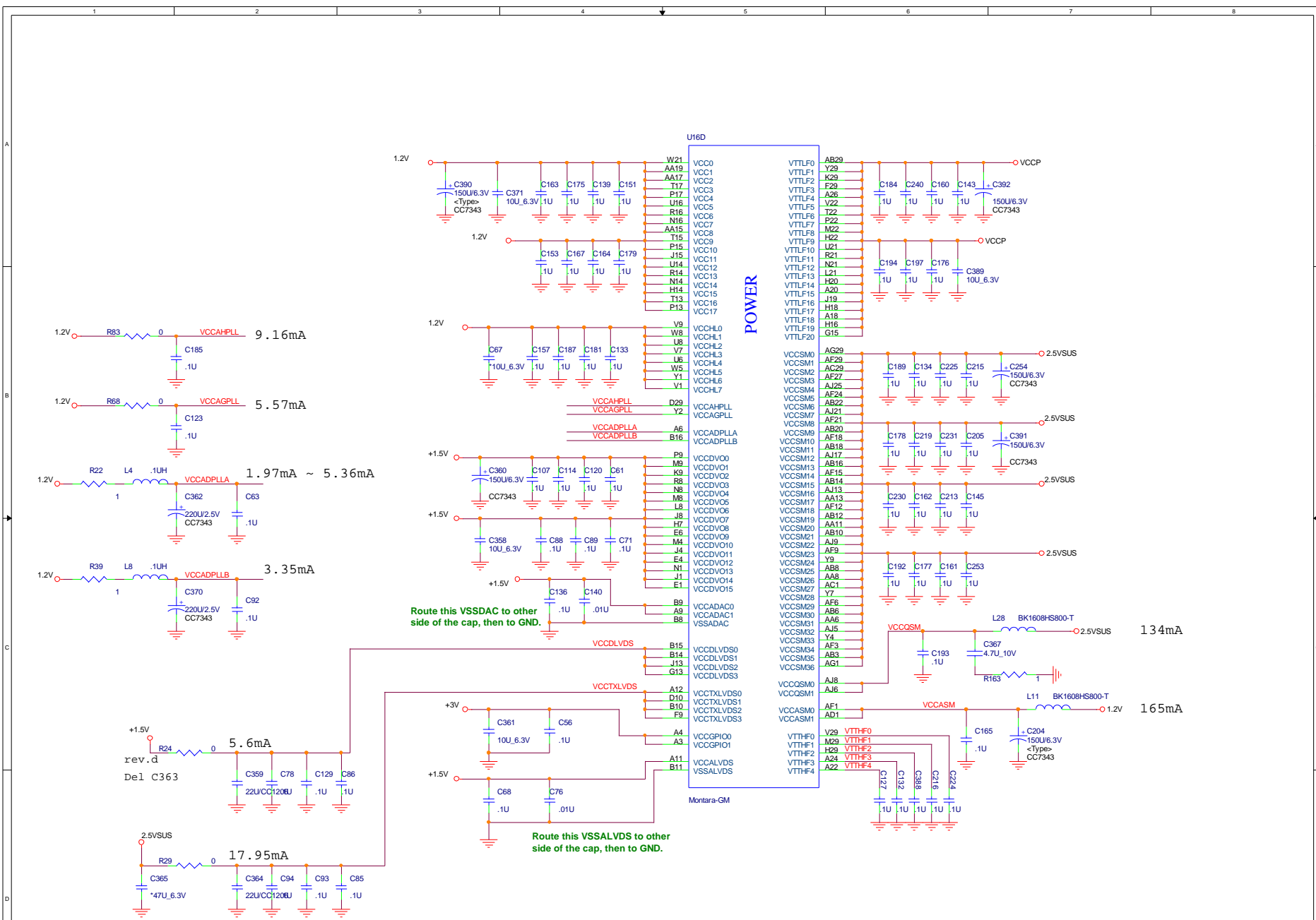
ST2	ST1	ST0	PSB Frequency	Memory Frequency	GFX Core Clock - Low	GFX Core Clock - High
*	0	0	400MHz	266MHz	1.33MHz	200MHz
0	0	1	400MHz	200MHz	1.00MHz	200MHz
0	1	0	400MHz	266MHz	1.33MHz	266MHz
0	1	1	400MHz	266MHz	1.33MHz	266MHz
1	0	0	533MHz	266MHz	1.33MHz	200MHz
1	0	1	533MHz	266MHz	1.33MHz	266MHz
1	1	0	533MHz	333MHz	1.66MHz	266MHz
1	1	1	400MHz	333MHz	1.66MHz	250MHz

PROJECT : CT1
Quanta Computer Inc.

Size: Custom Document Number: **MontaraGM_B** Rev: 1A


Date: Wednesday, April 14, 2004 Sheet: 6 of 38

MONTARA-GME/855GM+ 2 of 3 (DVO & DDR)

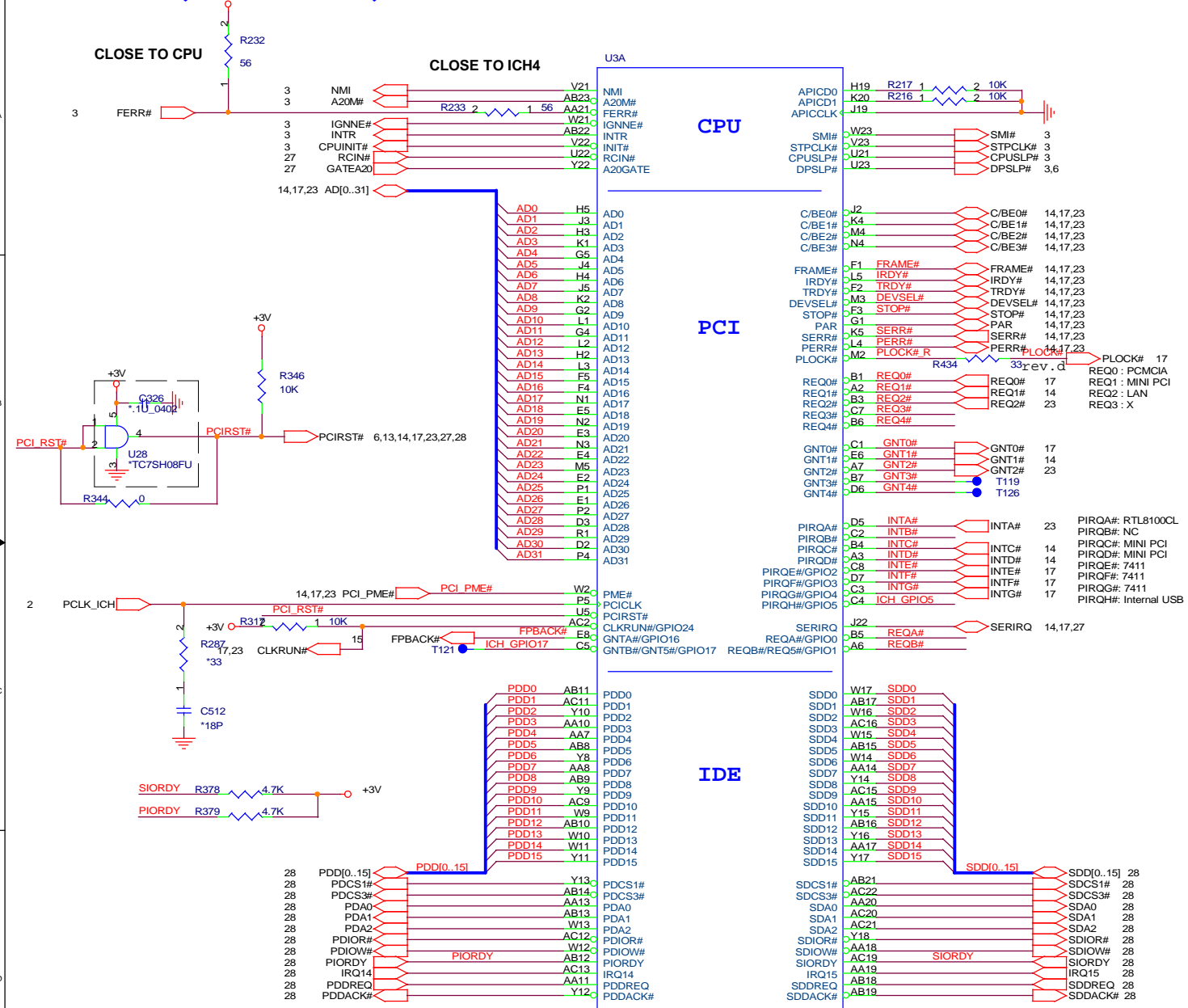


change +2.5v to 2.5vsus

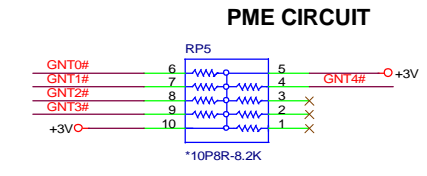
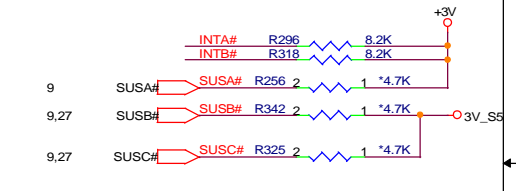
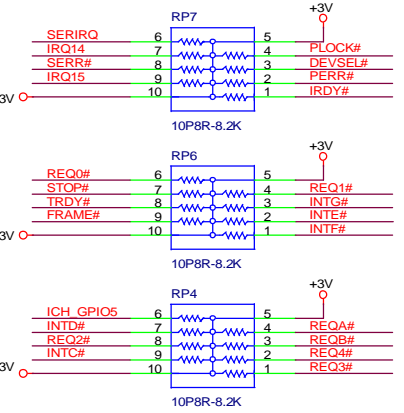
MONTARA-GME/ 855GM+ 3 of 3 (POWER & CAP.)


		PROJECT : CT1 Quanta Computer Inc.	
Size	Document Number	MontaraGM_C	Rev
Custom			1A
Date:	Wednesday, April 14, 2004	Sheet	7 of 38

ICH4-M 1/3 (CPU, PCI, IDE)



PCI Bus pull high resistor



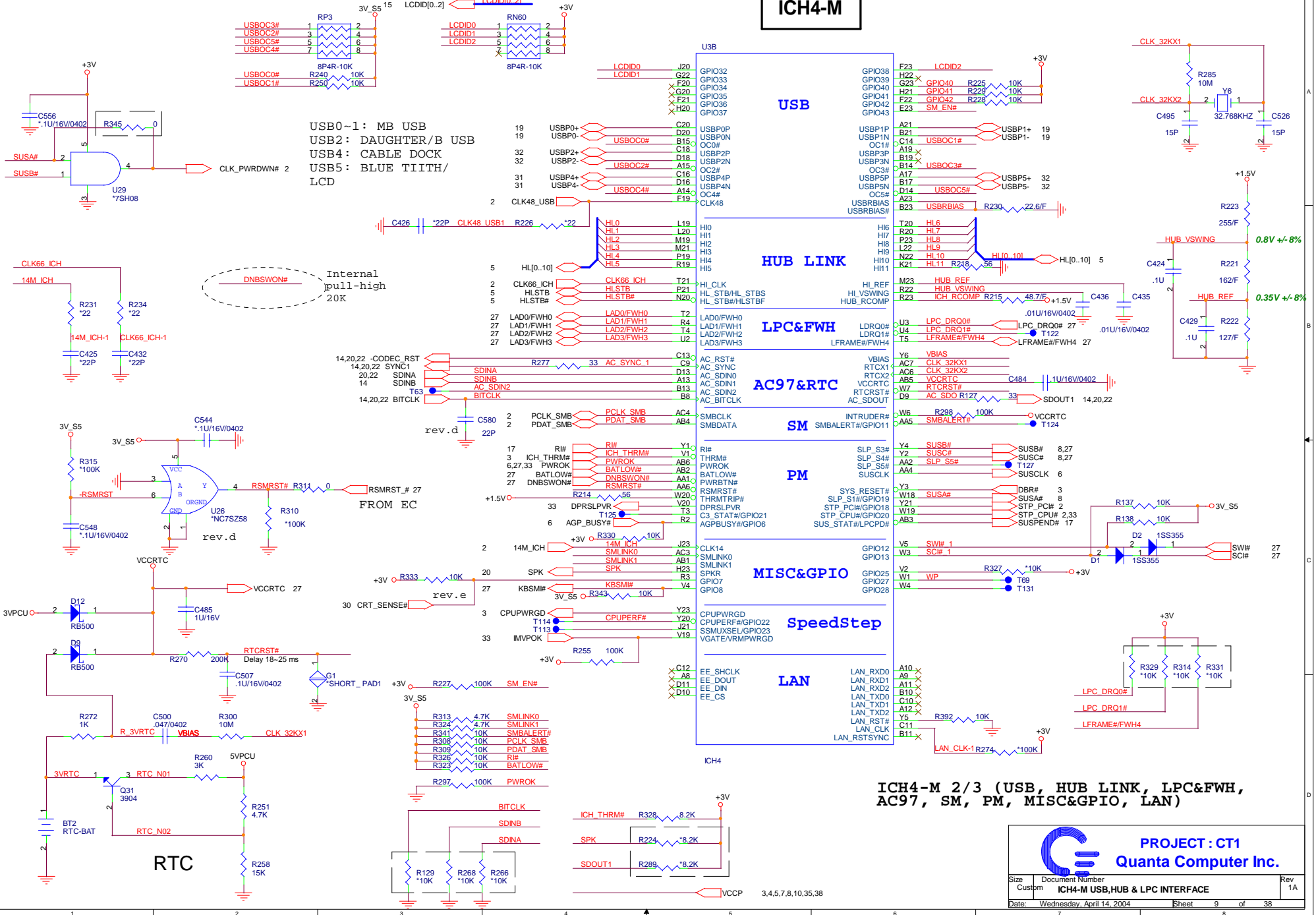


PROJECT : CT1
Quanta Computer Inc.

Size	Document Number	Rev
Custbrn	ICH4-M (CPU,PCI,IDE)	1A
Date:	Wednesday, April 14, 2004	Sheet 8 of 38

ICH4-M

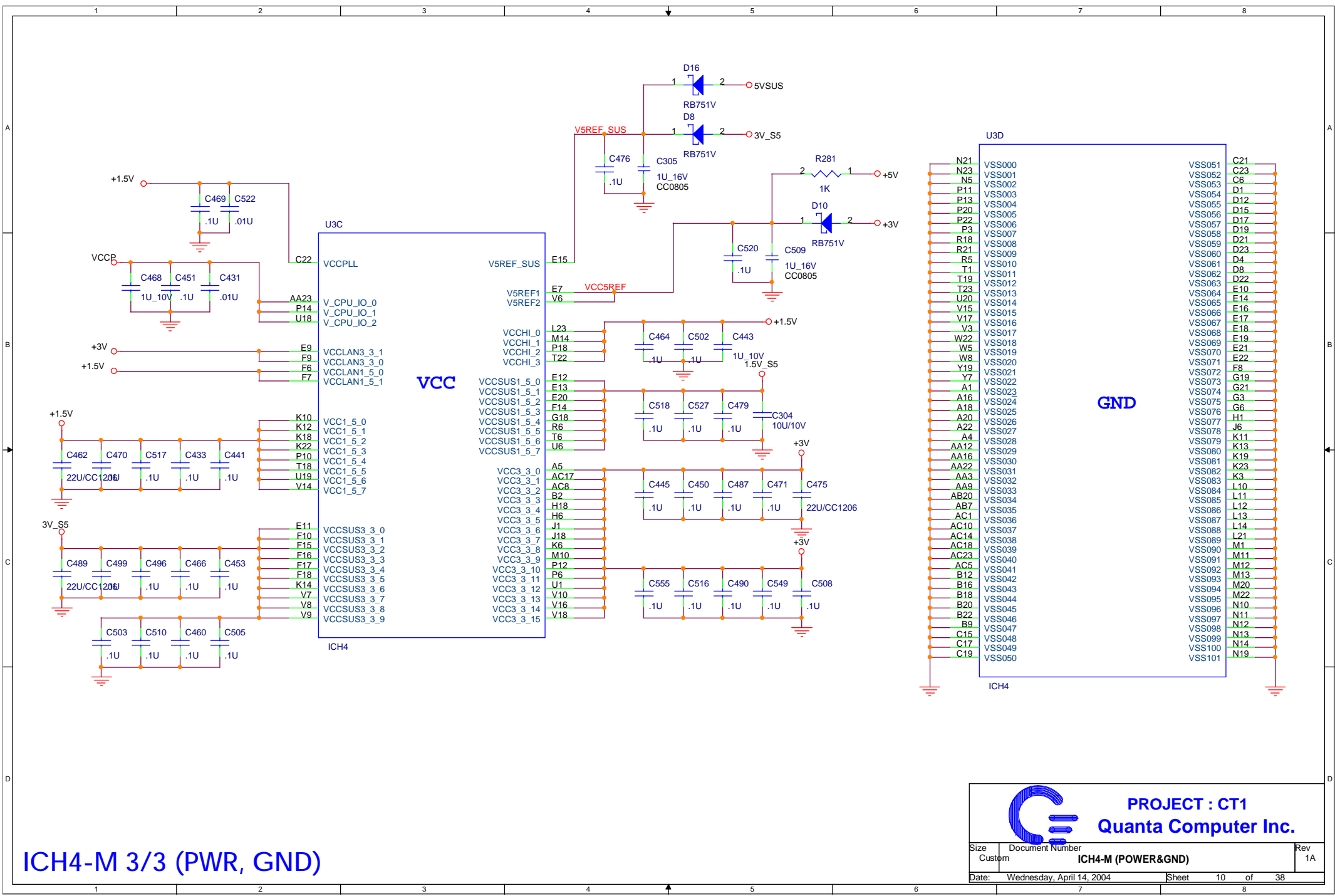
ICH4-M




ICH4-M 2/3 (USB, HUB LINK, LPC&FWH, AC97, SM, PM, MISC&GPIO, LAN)

PROJECT : CT1
Quanta Computer Inc.

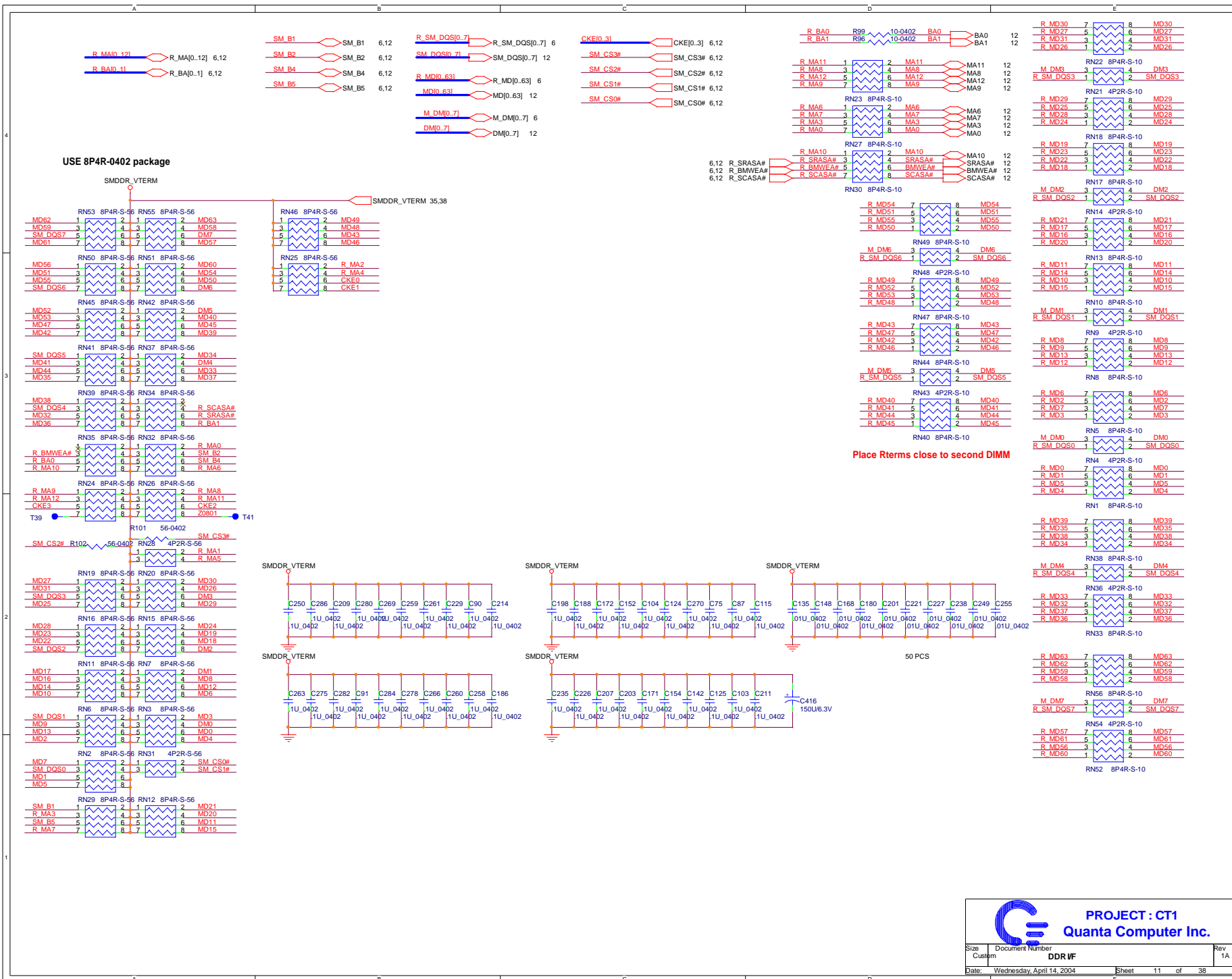
Size	Document Number	Rev
Custpm	ICH4-M USB,HUB & LPC INTERFACE	1A
Date:	Wednesday, April 14, 2004	Sheet 9 of 38

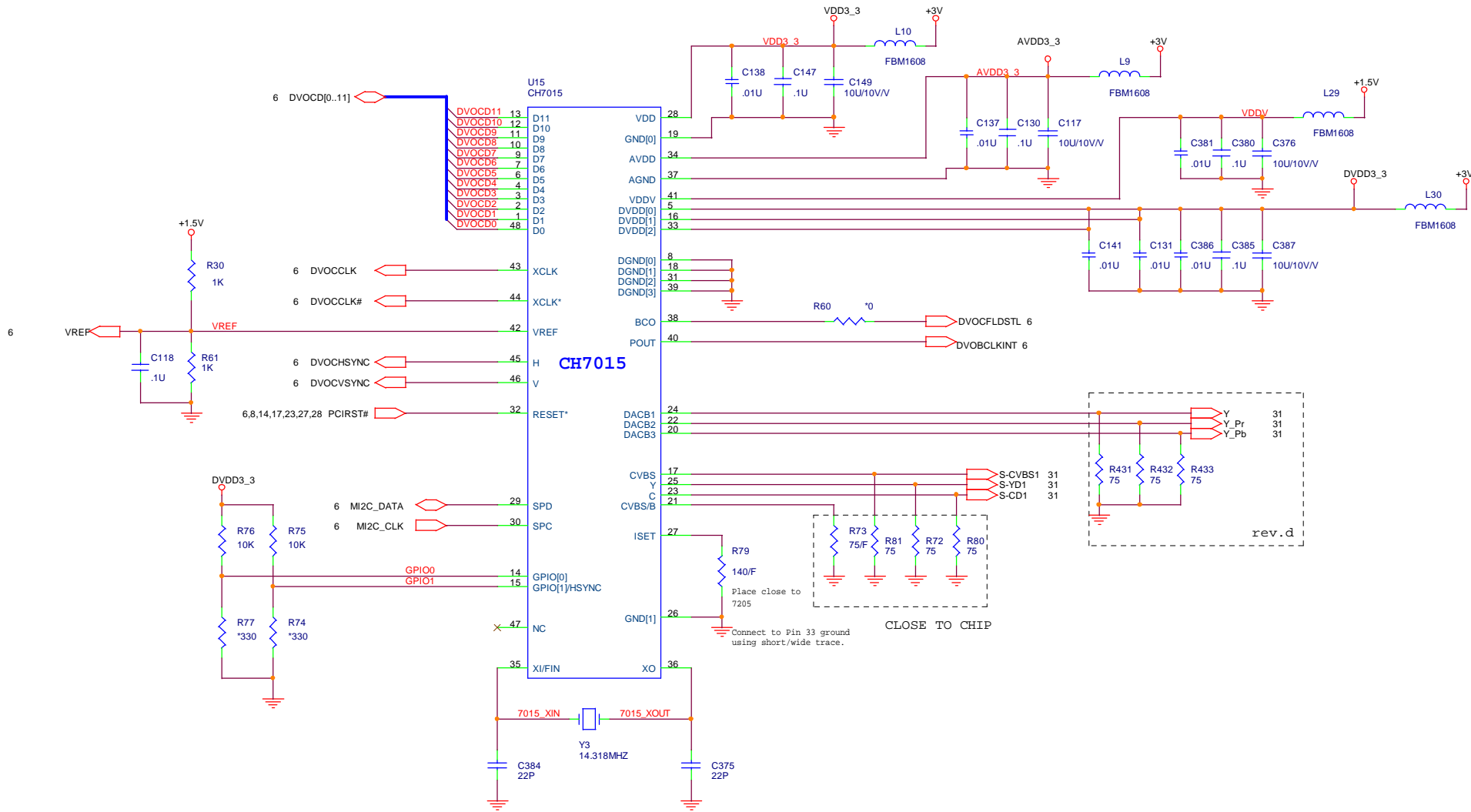


ICH4-M 3/3 (PWR, GND)



PROJECT : CT1
Quanta Computer Inc.

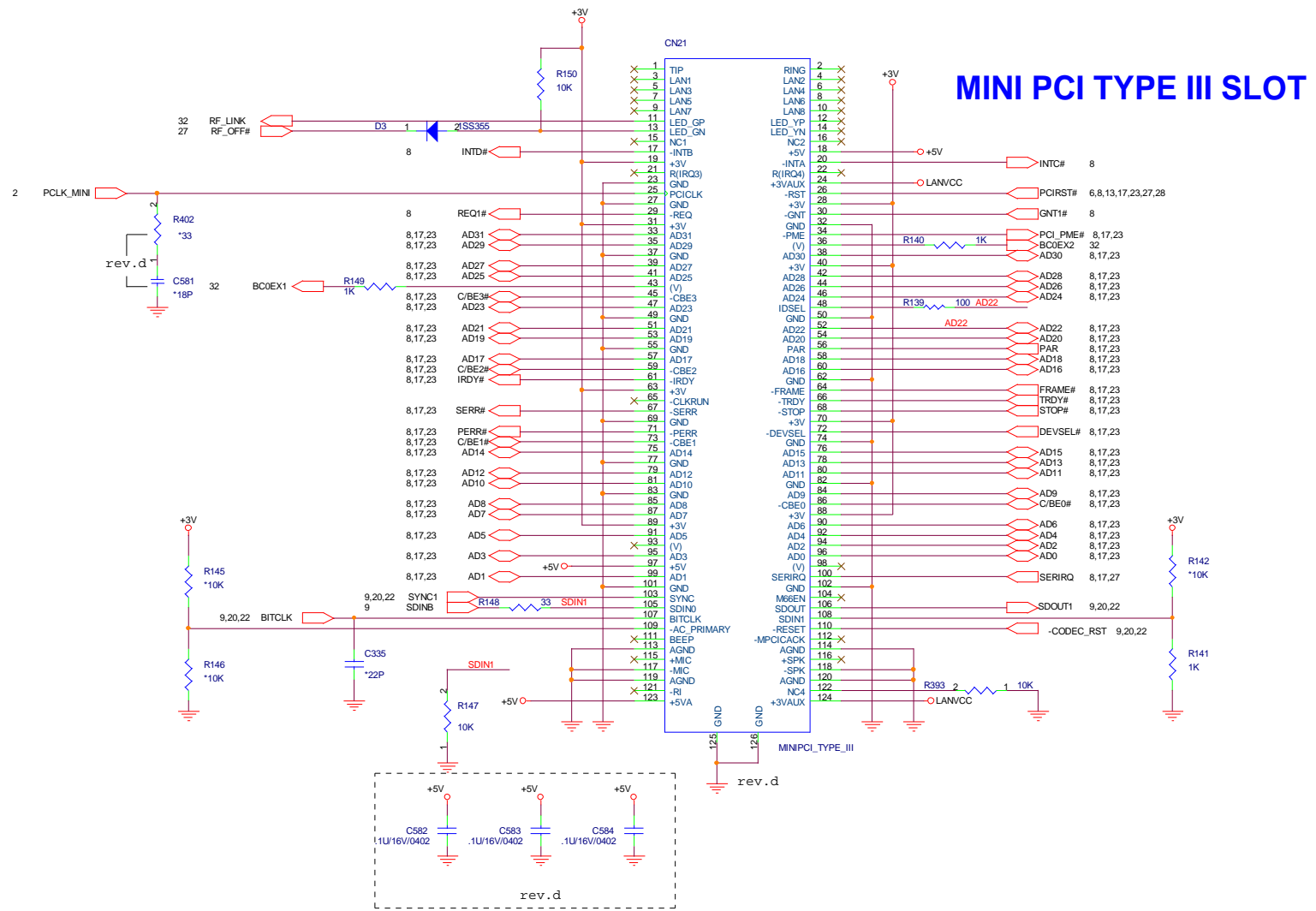
Size	Document Number	Rev
Custom	ICH4-M (POWER&GND)	1A
Date:	Wednesday, April 14, 2004	Sheet 10 of 38






GPIO[1:0] Pull Up and Pull Down
TV output option will be
defined later by SW group.

 PROJECT : CT1 Quanta Computer Inc.		Rev
		1A
Size	Document Number	Date: Wednesday, April 14, 2004
Custom		
Date: Wednesday, April 14, 2004		Sheet 13 of 38



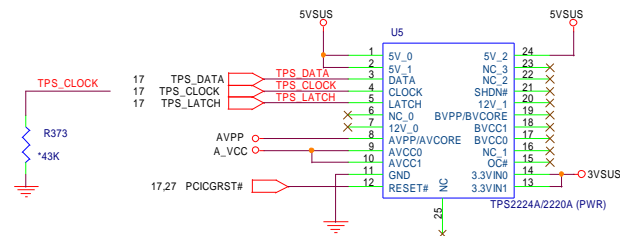
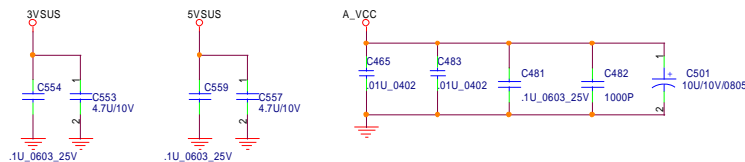
MINI PCI TYPE III SLOT



PROJECT : CT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom		1A
Date:	Wednesday, April 14, 2004	Sheet 14 of 38

CardBus Connector

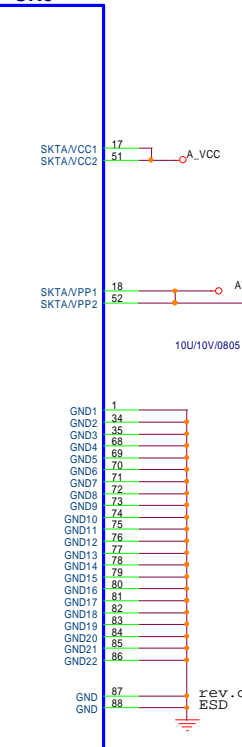


U21-3	VCCB	D19	X
	VCCB	K19	X
B_CAD31/B_D10	B15	X	
B_CAD30/B_D9	A16	X	
B_CAD29/B_D1	B16	X	
B_CAD28/B_D8	C17	X	
B_CAD27/B_D0	D17	X	
B_CAD26/A_0	C18	X	
B_CAD25/A_1	C19	X	
B_CAD24/A_2	D18	X	
B_CAD23/A_3	E17	X	
B_CAD22/A_4	G15	X	
B_CAD21/A_5	H14	X	
B_CAD20/A_6	H14	X	
B_CAD19/A_25	H15	X	
B_CAD18/A_7	G17	X	
B_CAD17/A_A24	K17	X	
B_CAD16/A_17	L13	X	
B_CAD15/B_IOWR	K18	X	
B_CAD14/B_A8	L15	X	
B_CAD13/B_IORD	L18	X	
B_CAD12/B_A11	L18	X	
B_CAD11/B_OE	L19	X	
B_CAD10/A_CE2	M17	X	
B_CAD9/B_A10	M14	X	
B_CAD8/B_D15	M15	X	
B_CAD7/B_D7	N19	X	
B_CAD6/B_D13	N18	X	
B_CAD5/B_D6	N15	X	
B_CAD4/A_D12	M13	X	
B_CAD3/B_D5	P18	X	
B_CAD2/B_D11	P17	X	
B_CAD1/B_D4	P19	X	
B_CAD0/B_D3	P19	X	
B_CCBE3/B_REG	F15	X	
B_CCBE2/B_A12	G18	X	
B_CCBE1/B_A8	K14	X	
B_CCBE0/B_CE1	M18	X	
B_CPAR/B_A13	K13	X	
B_CFRAME/B_A23	G19	X	
B_CTRDY/B_A22	H17	X	
B_CIRDY/B_A15	J13	X	
B_CSTOP/B_A20	J17	X	
B_CDEVSLE/B_A21	H19	X	
B_CBLOCK/B_A19	J19	X	
B_CPEERR/B_A14	J18	X	
B_CSERR/B_WAIT	B18	X	
B_CREQ/B_INPACK	F18	X	
B_CGNT/B_WE	J15	X	
B_CSTSCHG/B_BVD1(STSCHGR)	F14	X	
B_CCLKRUN/B_WP(OIS16)	A18	X	
B_CCLK/B_A16	H18	X	
B_CINT/B_READY(IREQ)	B19	X	
B_CRST/B_RESET	F17	X	
B_CAUDIO/B_BVD2(SPKR)	C17	X	
B_CCD1/B_CD1	N13	X	
B_CCD2/B_CD2	B17	X	
B_CVS1/B_VS1	C18	X	
B_CVS2/B_VS2	F19	X	
B_RSVD/B_D14	N17	X	
B_RSVD/B_D2	A15	X	
B_RSVD/B_A18	K15	X	

U21-2	VCCA	A5	X
	VCCA	A11	X
A_CAD31/A_D10	D1	A_D10	
A_CAD30/A_D9	C1	A_D9	
A_CAD29/A_D1	D3	A_D1	
A_CAD28/A_D8	C2	A_D8	
A_CAD27/A_D0	B4	A_D0	
A_CAD26/A_0	A4	A_A0	
A_CAD25/A_1	E6	A_A2	
A_CAD24/A_2	B5	A_A3	
A_CAD23/A_3	C6	A_A4	
A_CAD22/A_4	A6	A_A5	
A_CAD21/A_5	G9	A_A6	
A_CAD20/A_6	C7	A_A25	
A_CAD19/A_25	B7	A_A7	
A_CAD18/A_7	A7	A_A24	
A_CAD17/A_A24	A10	A_A17	
A_CAD16/A_17	E11	A_IOWR#	
A_CAD15/A_IOWR	G11	A_A9	
A_CAD14/A_A8	C11	A_IORD#	
A_CAD13/A_IORD	L17	A_A11	
A_CAD12/A_A11	C12	A_OE#	
A_CAD11/A_OE	B12	A_CE2#	
A_CAD10/A_CE2	A12	A_A10	
A_CAD9/A_10	E12	A_D15	
A_CAD8/A_D15	C13	A_D7	
A_CAD7/A_D7	F12	A_D13	
A_CAD6/A_D13	A13	A_D6	
A_CAD5/A_D6	A14	A_D12	
A_CAD4/A_D12	A11	A_D5	
A_CAD3/A_D5	A14	A_D11	
A_CAD2/A_D11	B14	A_D4	
A_CAD1/A_D4	E14	A_D3	
A_CAD0/A_D3	E14	A_D3	
A_CCBE3/A_REG	C5	A_REG#	
A_CCBE2/A_A12	F9	A_A12	
A_CCBE1/A_A8	B10	A_A8	
A_CCBE0/A_CE1	G12	A_CE1#	
A_CPAR/A_A13	G10	A_A13	
A_CFRAME/A_A23	C8	A_A23	
A_CTRDY/A_A22	A8	A_A22	
A_CIRDY/A_A15	B8	A_A15	
A_CSTOP/A_A20	A9	A_A20	
A_CDEVSLE/A_A21	C9	A_A21	
A_CBLOCK/A_A19	E10	A_A19	
A_CPEERR/A_A14	F10	A_A14	
A_CSERR/A_WAIT	B3	A_WAIT#	
A_CREQ/A_INPACK	E7	A_INPACK#	
A_CGNT/A_WE	B9	A_WER#	
A_CSTSCHG/A_BVD1(STSCHGR)	B2	A_STSCHG_P	
A_CCLKRUN/A_WP(OIS16)	C3	A_IOIS16#	
A_CCLK/A_A16	E9	A_A16	
A_CINT/A_READY(IREQ)	C4	A_IREQ#	
A_CRST/A_RESET	A6	A_RESET	
A_CAUDIO/A_BVD2(SPKR)	A2	A_SPKR_P	
A_CCD1/A_CD1	C15	A_CD1#	
A_CCD2/A_CD2	E5	A_CD2#	
A_CVS1/A_VS1	A3	A_VS1#	
A_CVS2/A_VS2	E8	A_VS2#	
A_RSVD/A_D14	B13	A_D14	
A_RSVD/A_D2	D2	A_D2	
A_RSVD/A_A18	C10	A_A18	


A_D3	2	SKTAA0/D3
A_D4	3	SKTAA1/D4
A_D11	37	SKTAA2/D11
A_D5	4	SKTAD3/D5
A_D12	38	SKTAD4/D12
A_D6	5	SKTAD5/D6
A_D13	39	SKTAA6/D13
A_D7	6	SKTAA7/D7
A_D15	41	SKTAA8/D15
A_A0	1	SKTAA9/A10
A_CE2#	42	SKTAA10/CE2#
A_OE#	9	SKTAA11/OE#
A_A11	10	SKTAA12/A11
A_IORD#	11	SKTAA13/IORD#
A_A9	13	SKTAA14/A9
A_IOWR#	45	SKTAA15/IOWR#
A_A17	46	SKTAA16/A17
A_A24	55	SKTAA17/A24
A_A7	56	SKTAA18/A7
A_A25	56	SKTAA19/A25
A_A6	23	SKTAA20/A6
A_D15	23	SKTAA21/A5
A_A4	24	SKTAA22/A4
A_A3	26	SKTAA23/A3
A_A2	27	SKTAA24/A2
A_D12	28	SKTAA25/A1
A_A0	28	SKTAA26/A0
A_D11	30	SKTAA27/D11
A_D8	64	SKTAA28/D8
A_D1	31	SKTAA29/D1
A_D9	65	SKTAA30/D9
A_D10	66	SKTAA31/D10
A_CE1#	7	-SKTACBE0/CE1#
A_A8	12	-SKTACBE1/A8
A_A12	21	-SKTACBE2/A12
A_REG#	61	-SKTACBE3/REG#
A_A23	19	SKTAPCLK/A16
A_A15	20	SKTAFRAME/A23
A_A22	53	SKTAIRDY/A15
A_A21	50	SKTATRDY/A22
A_A20	49	SKTADVSEL/A21
A_A13	13	SKTASTOP/A20
A_A14	14	SKTAPARA/A13
A_WAIT#	14	-SKTAPERR/A14
A_INPACK#	60	SKTASERR/WAIT#
A_WER#	16	SKTAREQ/INPACK#
A_WE#	15	SKTAGNT/WE#
A_I19	48	SKTAINTRDY
A_IOIS16#	33	SKTALOCK/A19
A_RESET	58	SKTACLKRUN/WP
A_A16	40	SKTARST/RESET
A_A18	47	SKTARSDV/D14
A_VS1#	43	SKTARSDV/A18
A_VS2#	57	SKTAVS1/VS1#
A_CD1#	39	SKTAVS2/VS2#
A_RD2#	69	SKTACD1/CD1#
A_SPKR_P	62	SKTACD2/CD2#
A_STSCHG_P	63	SKTAAUDIO/BVD2
A_D2	32	SKTASTSCHG/BVD1
		SKTARSDV/D2

CN6



CARDBUS SLOT

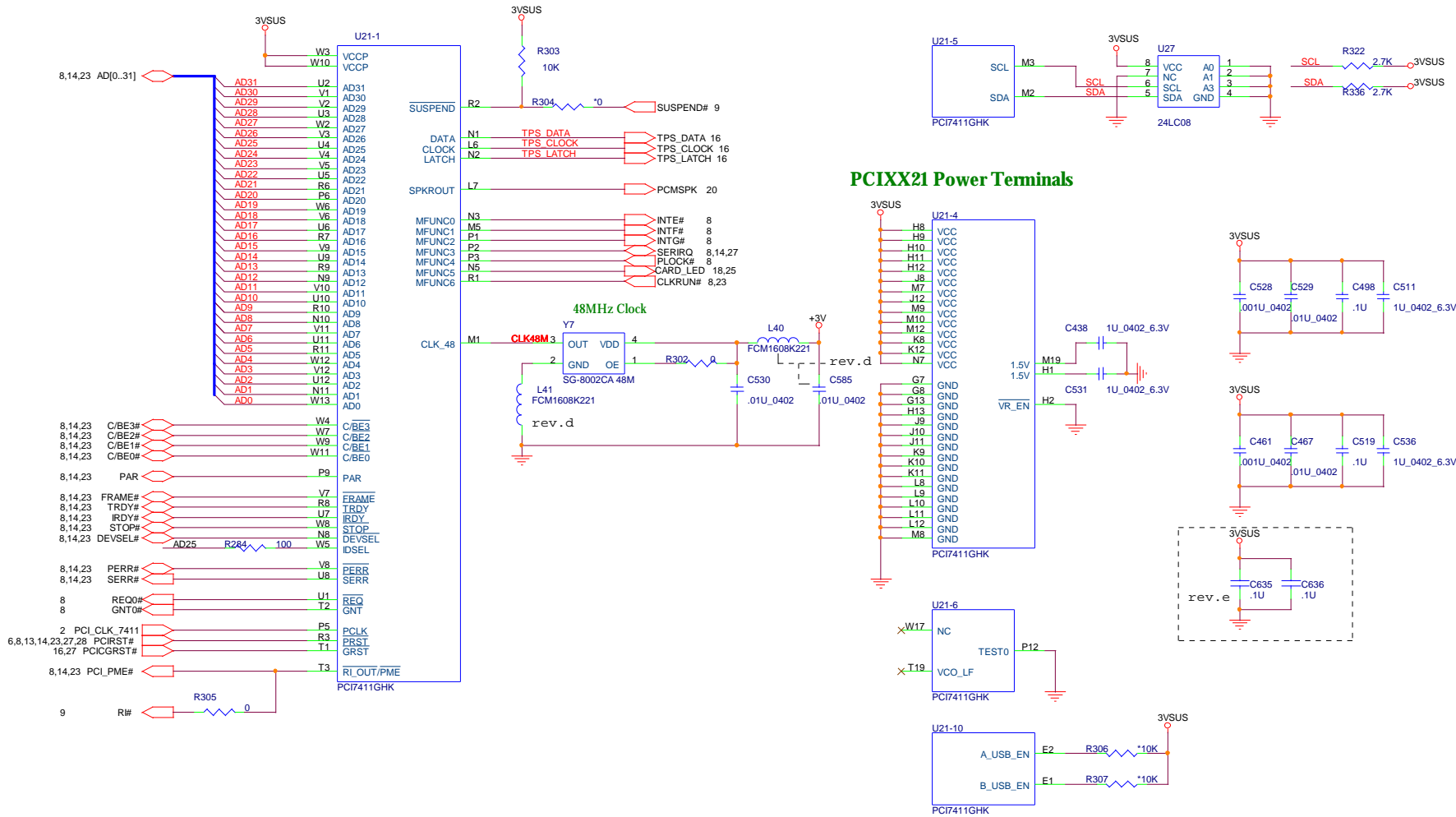
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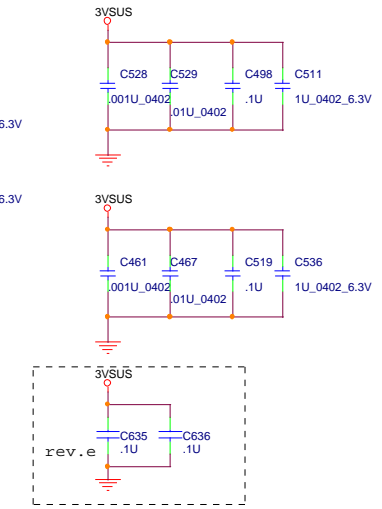
PROJECT : CT1
Quanta Computer Inc.

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Date:	Wednesday, April 14, 2004	Sheet 16 of 38

CardBus



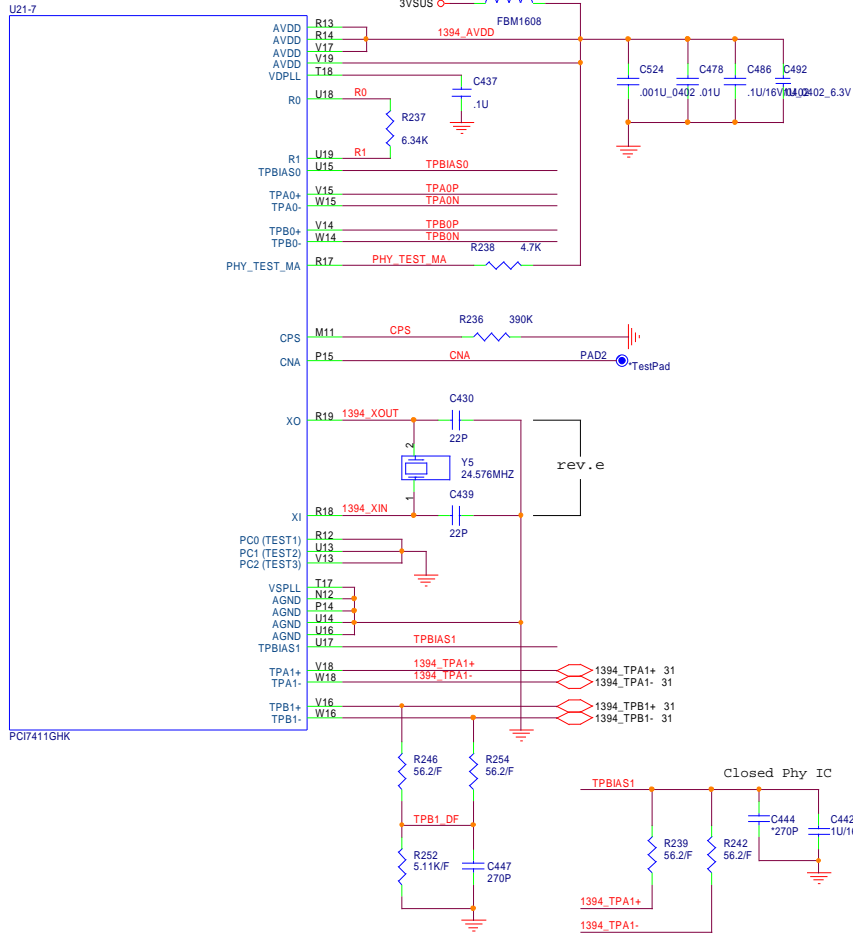
PCIXX21 Power Terminals



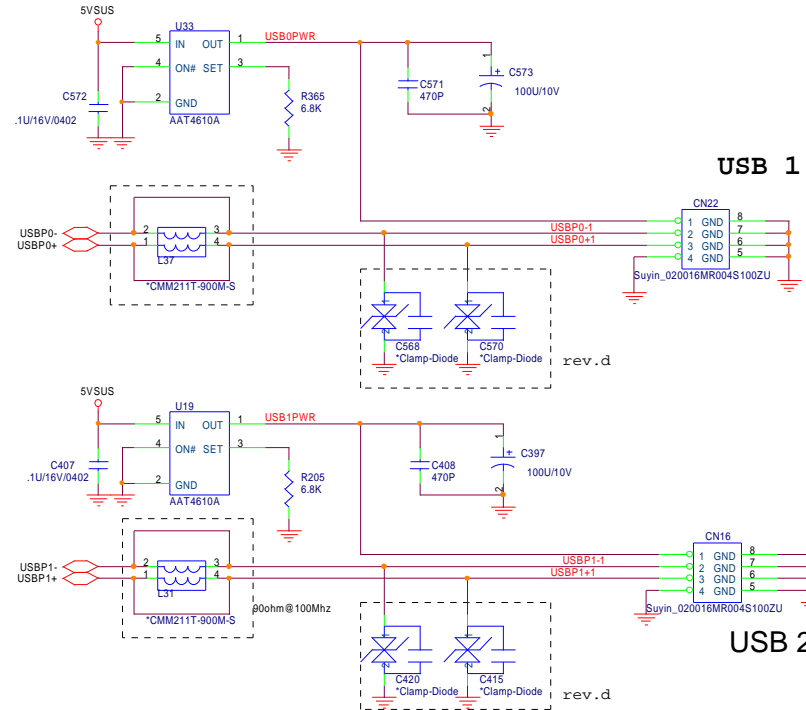
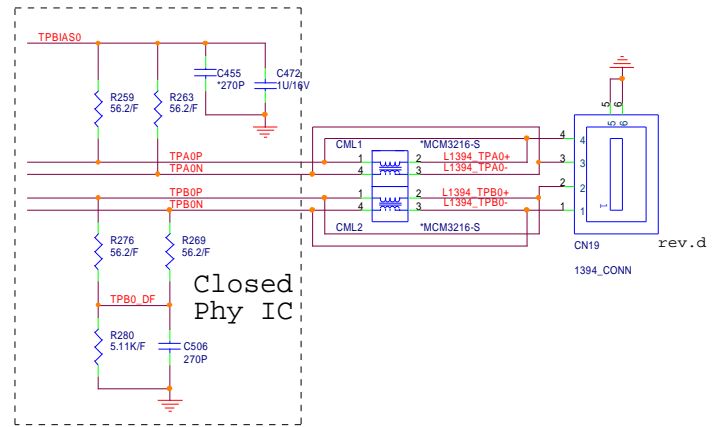
PROJECT : CT1
Quanta Computer Inc.


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Custom		1A
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IEEE 1394a



IEEE 1394 CONNECTOR

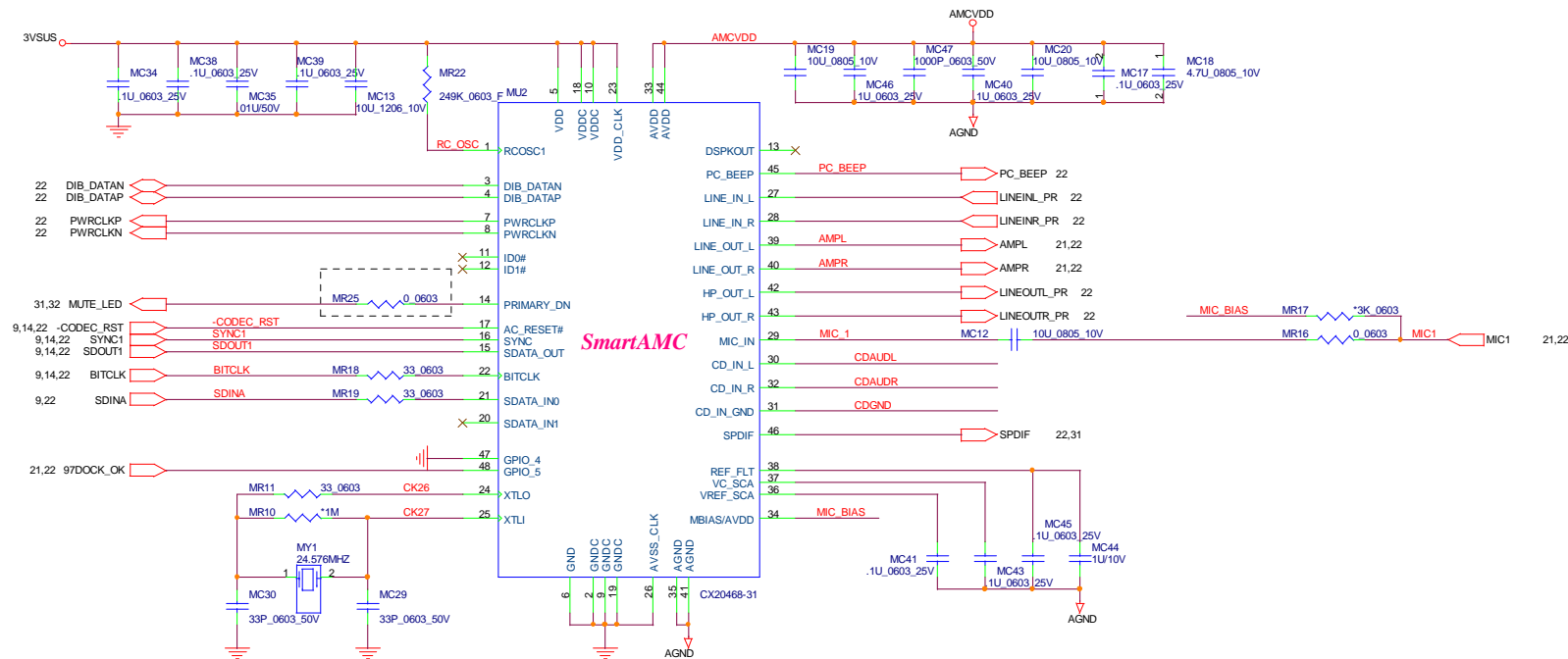




PROJECT : CT1
Quanta Computer Inc.

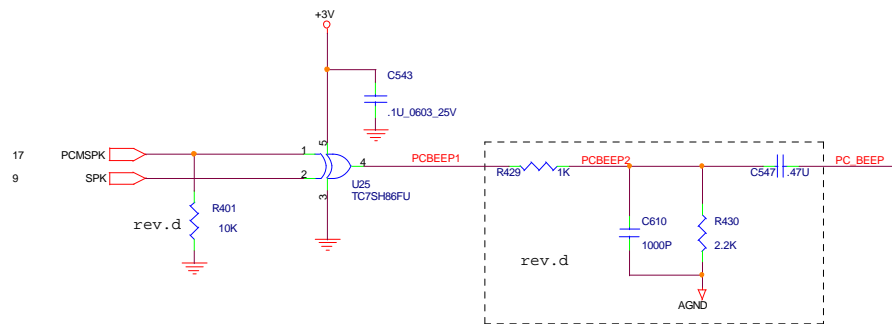
Size	Document Number	Rev
Custom		1A
Date:	Wednesday, April 14, 2004	Sheet 19 of 38

The AMC20493-001 modem is used for mother board family MBAMC20493-010.

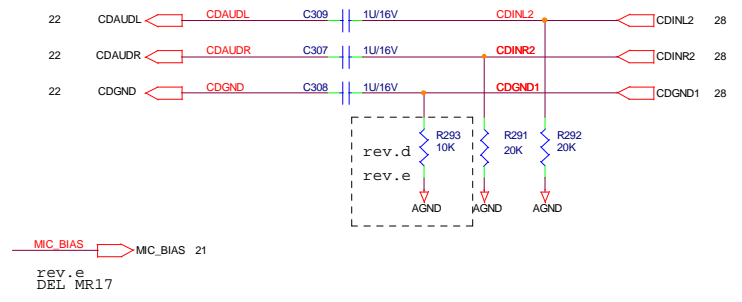


SmartAMC

PC SPEAKER



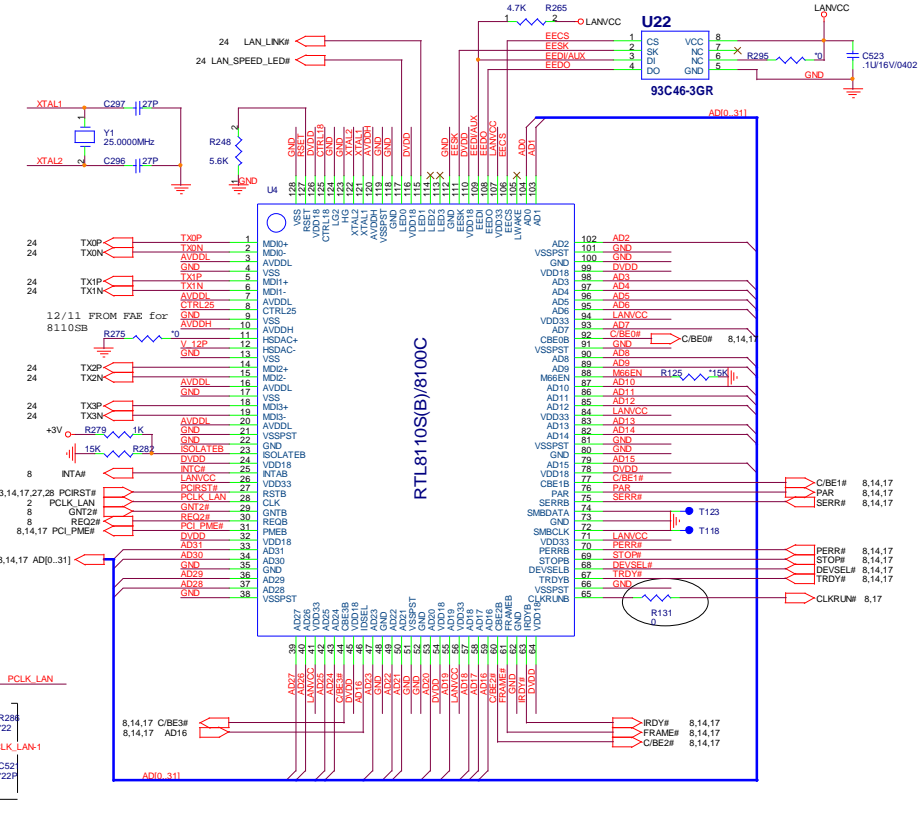
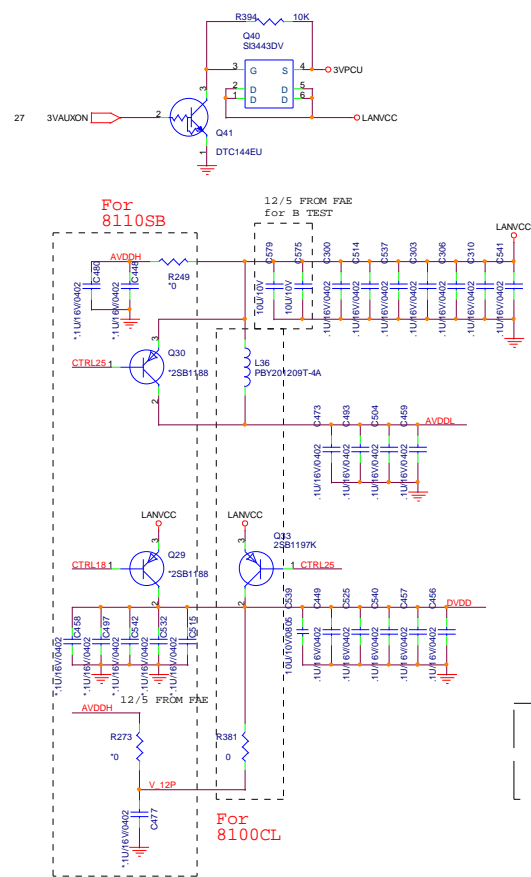
FROM CD-ROM

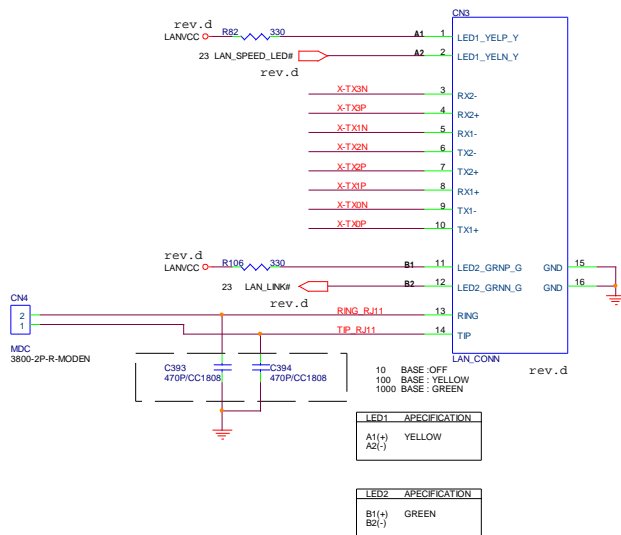
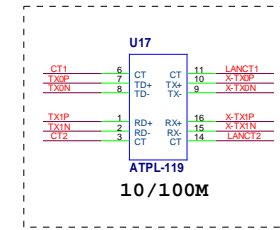
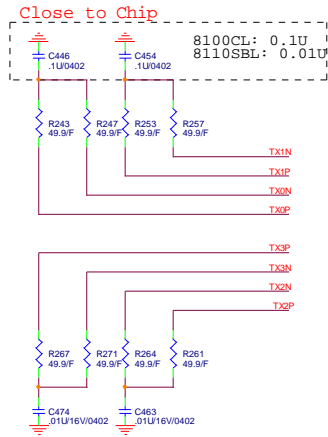
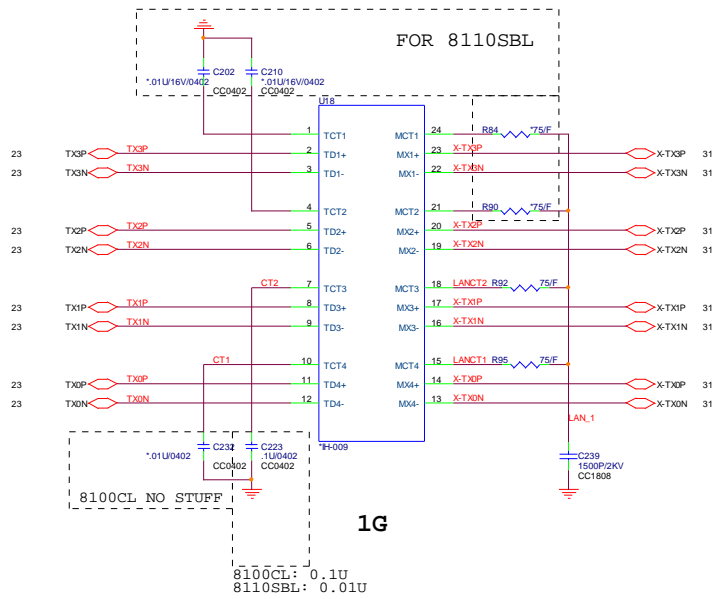


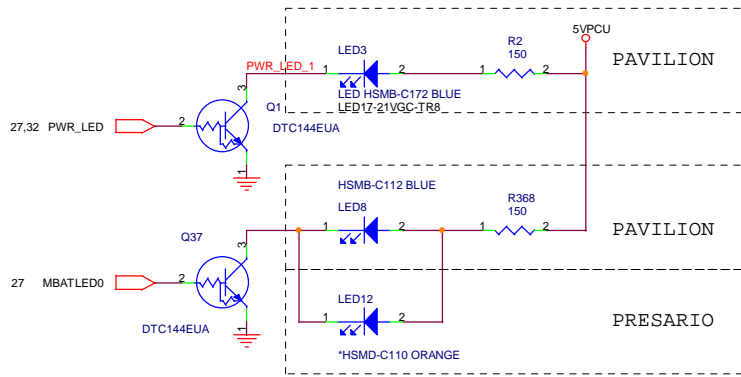
PROJECT : CT1
Quanta Computer Inc.

Size: Document Number
AMC97 CODEC
 Date: Wednesday, April 14, 2004 Sheet 20 of 38 Rev 1A

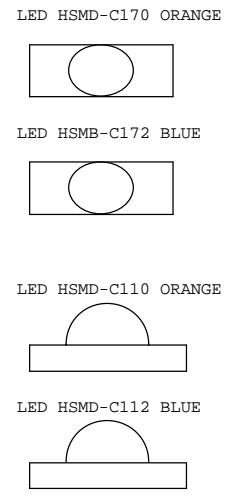
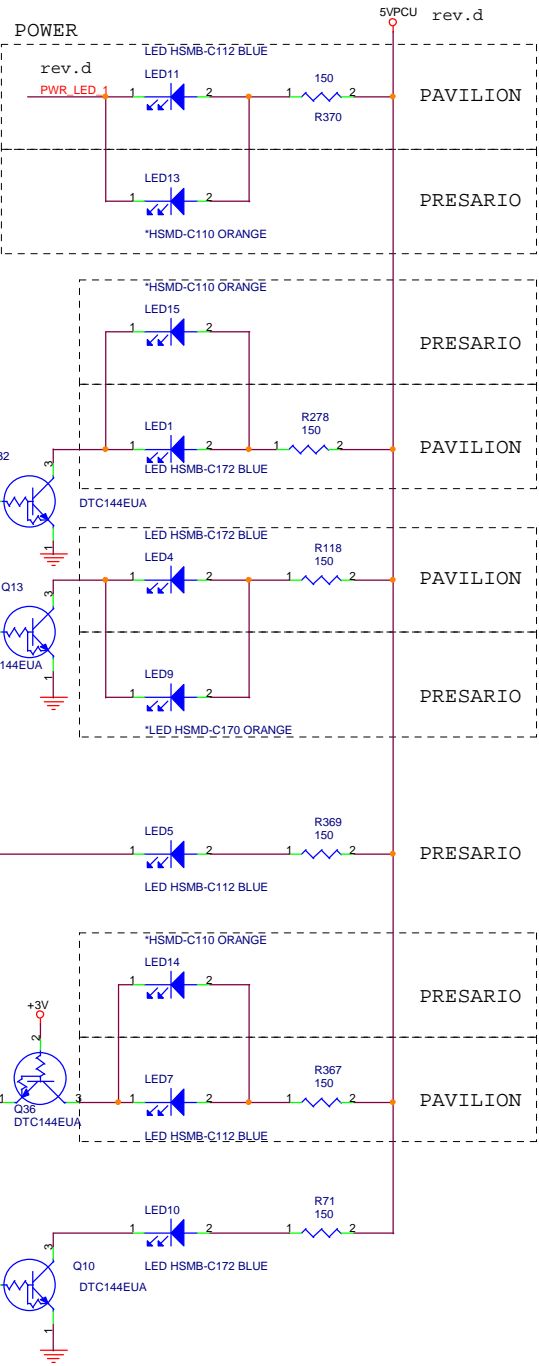
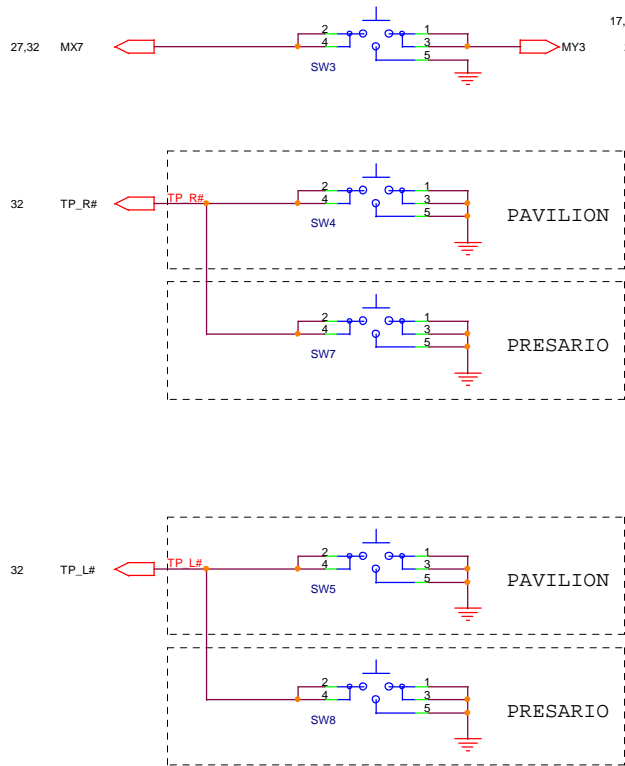
	8100CL(10/100M)	8110SB(1G)
DVDD33	3.3VD 26,41,56,71,84,94,107	3.3VD 26,41,56,71,84,94,107
AVDDL	3.3VA 3,7,20	2.5VA 3,7,20,16
DVDD	2.5VD 32,54,78,99	1.8VD 32,54,78,99,24,45,64,110,116,125
AVDD25	2.5VA 12	NC
AVDDH	NC	3.3VA 10,120








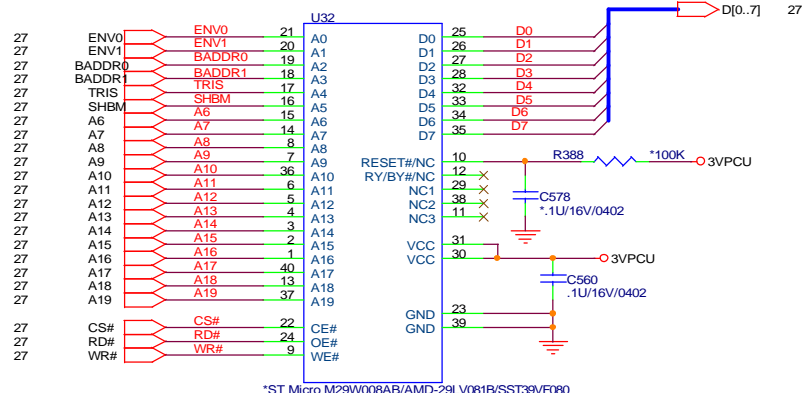
Touchpad control



REV.B: LED7 AND LED8 SWAP

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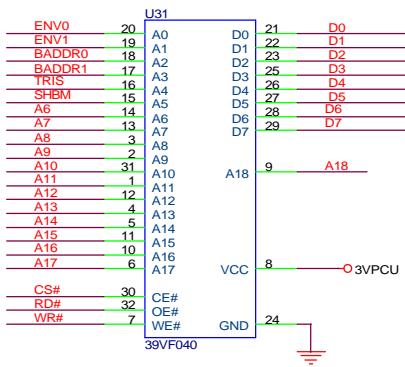
8Mbit (1M Byte), TSSOP40



AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
 SST :Pin10,12 are NC

- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

4Mbit (512k Byte), TSSOP32

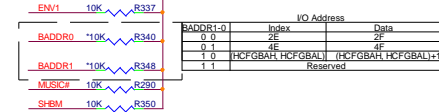
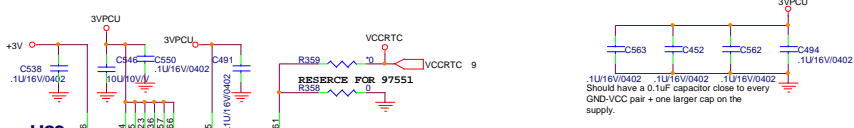
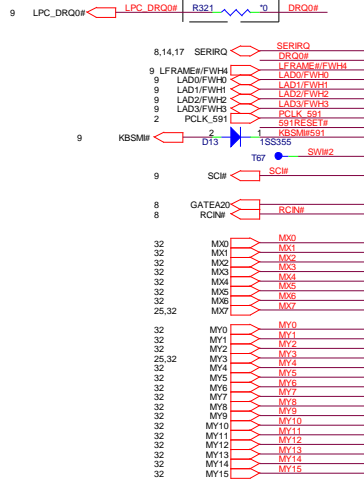


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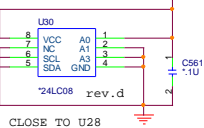
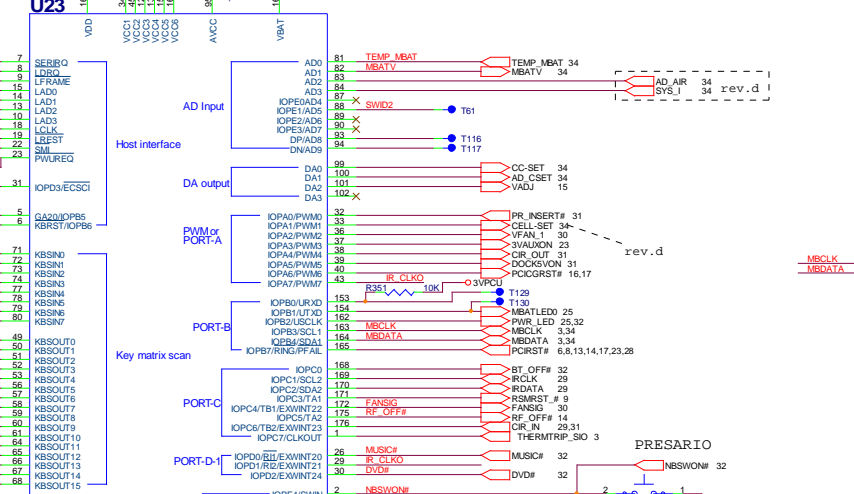
KBC-NS87551L

LDRQ#(pin 8) internal is no use



IO Address	Index	Digita
BADDR1-0	1	2E
0-1	2E	4E
1-0	4E	4F
1-1	4F	Reserved

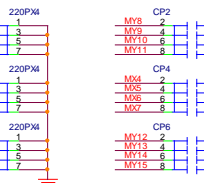
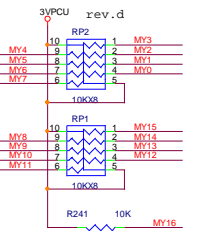
SHBM=1: Enable shared memory with host BIOS



CLOSE TO U28



Pin 24 if no pull-high, will can't reboot.



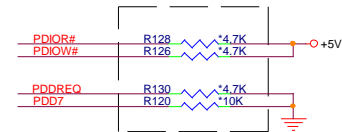
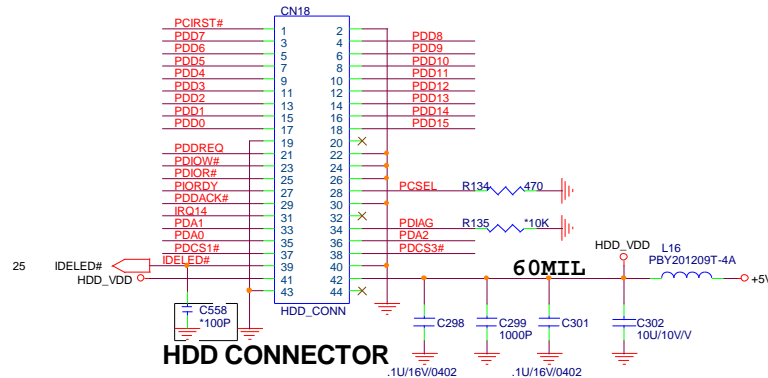
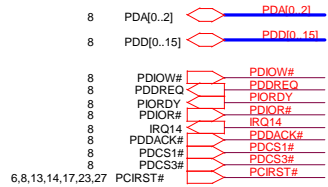
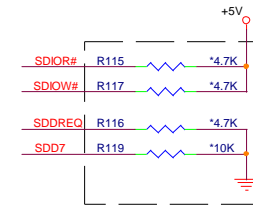
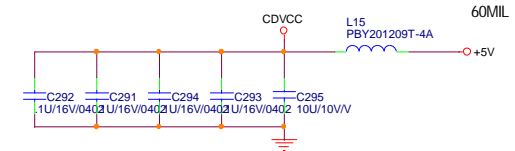
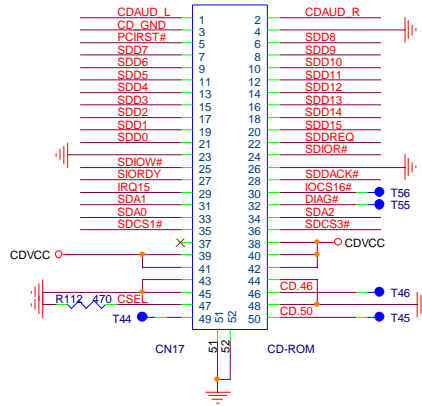
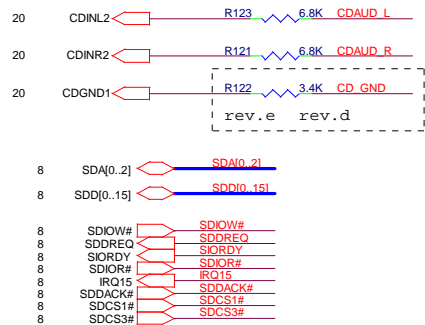
Pin 103 internal is "A19", Can't use to GPIO

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2		0.2

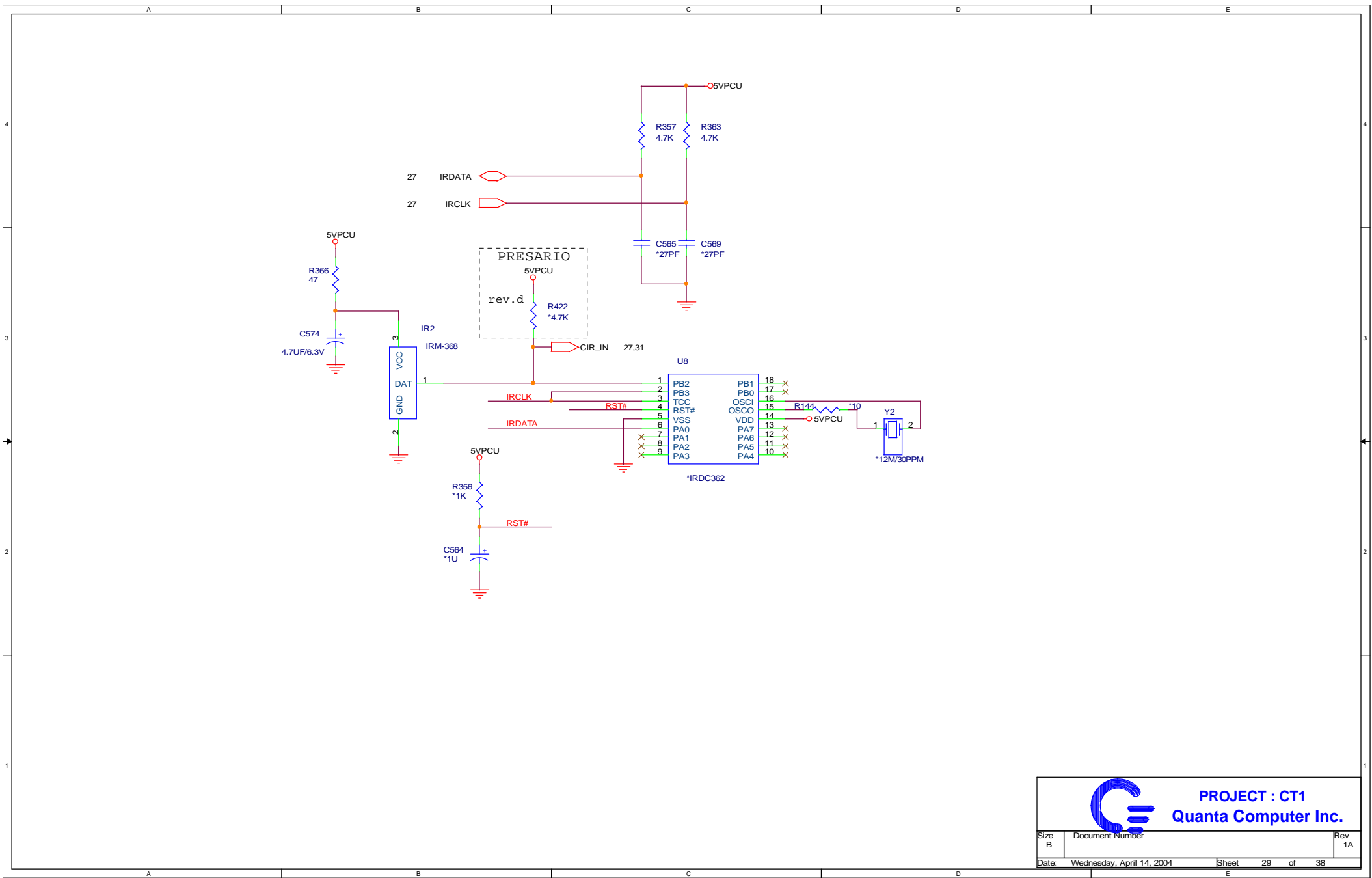
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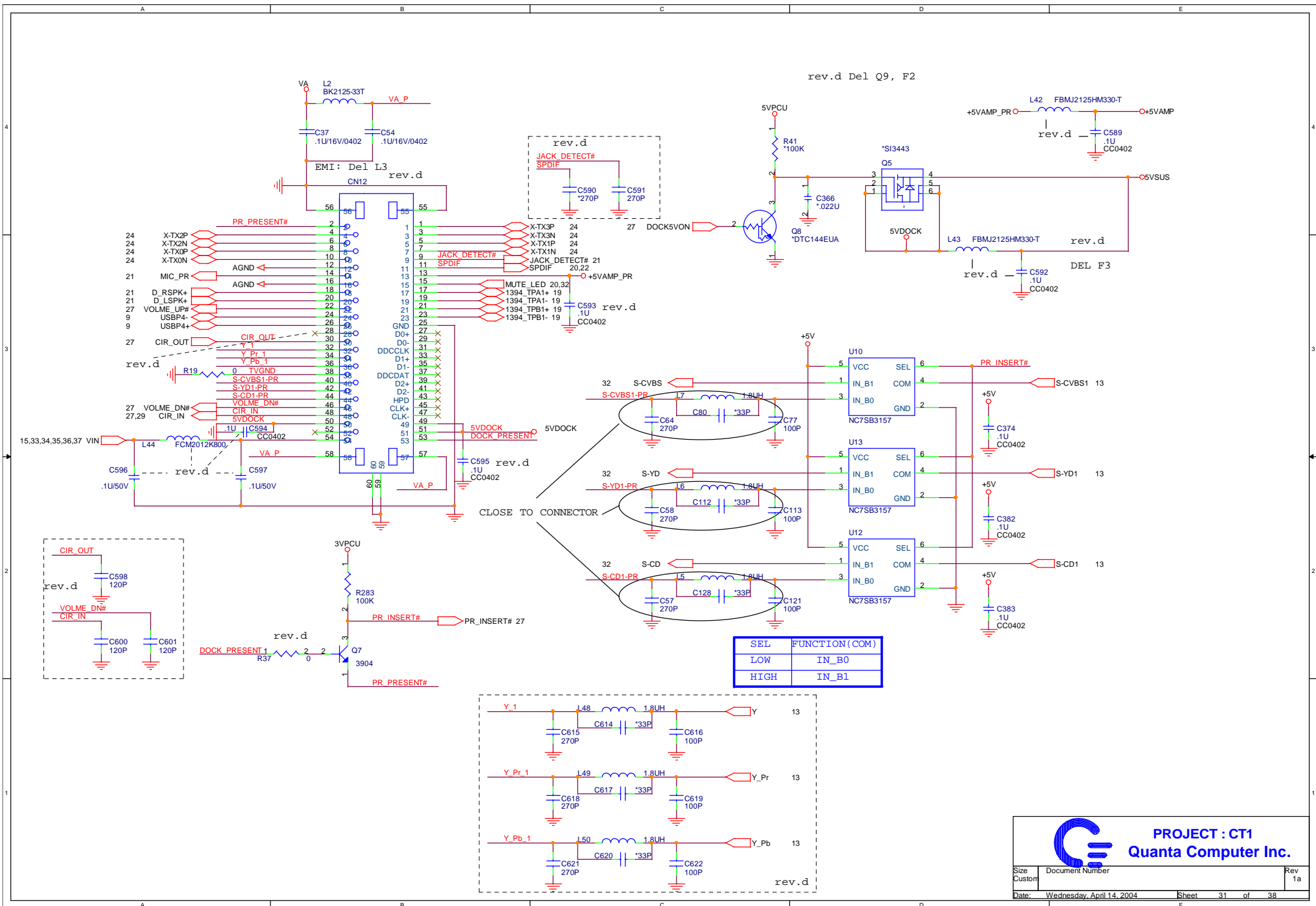
CD-ROM



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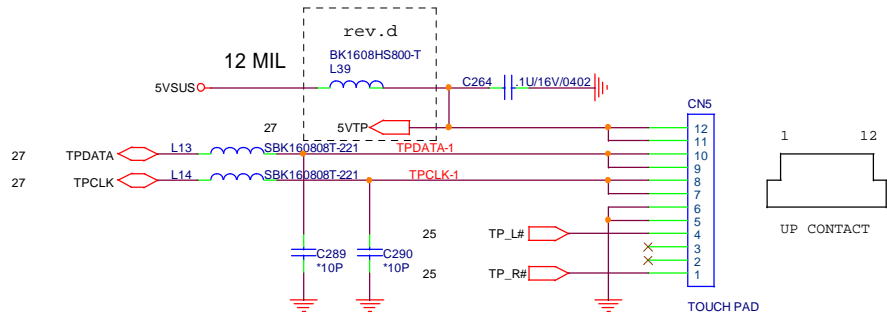




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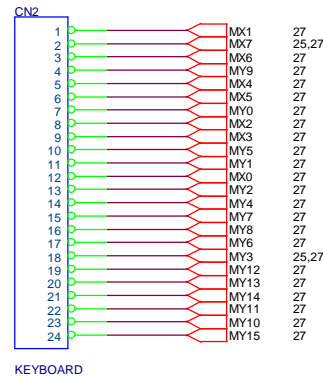
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TOUCH PAD CONNECTOR

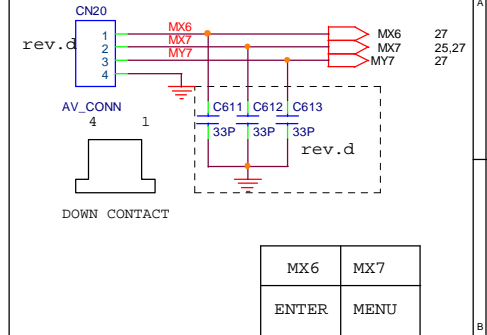


CHECK PIN DEFINE

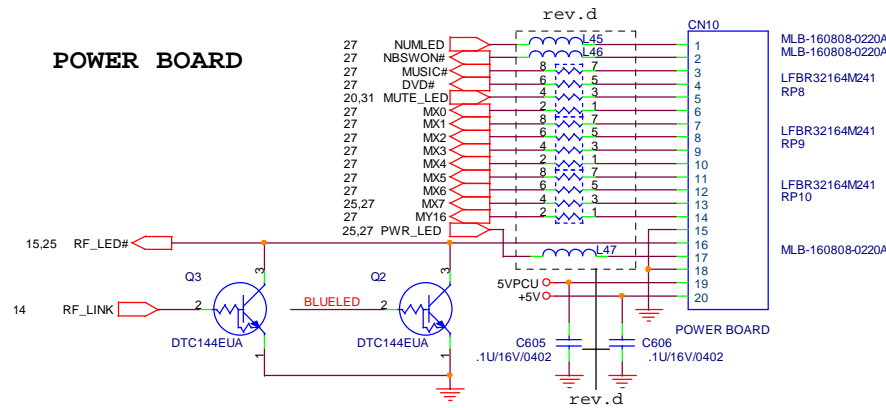
KEYBOARD CONNECTOR



AV BOARD

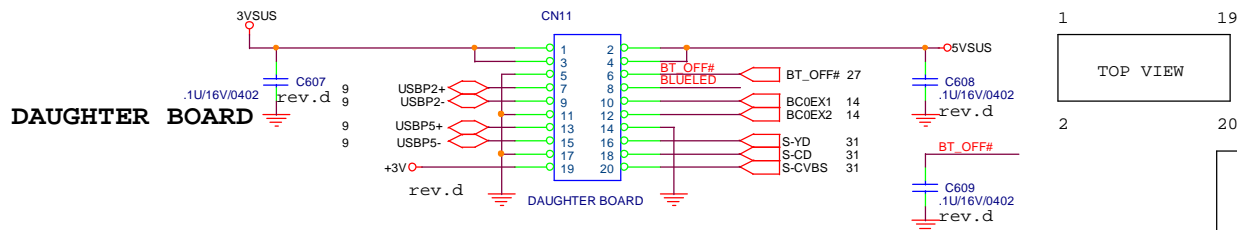


POWER BOARD

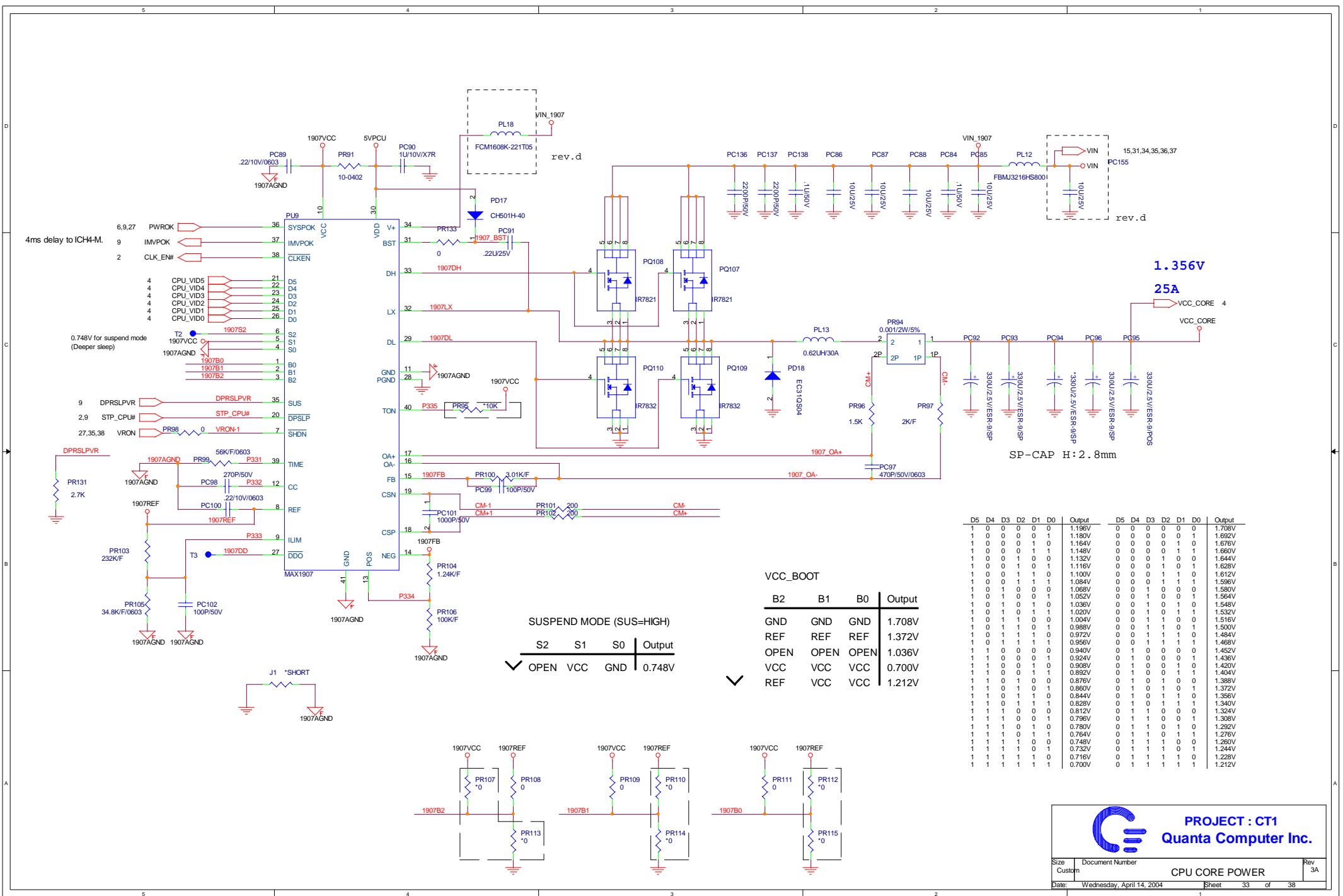


MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD



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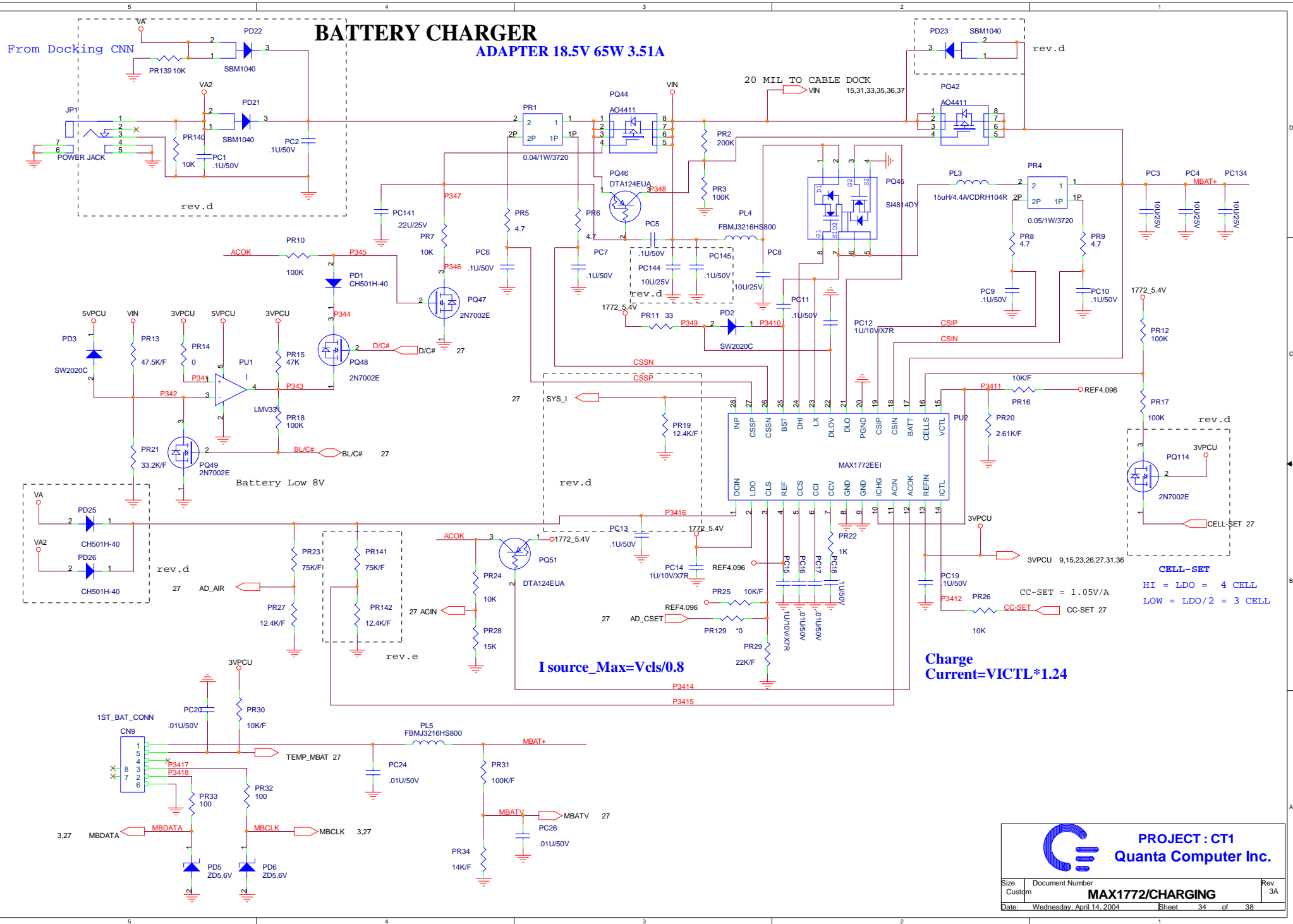


D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	0	1	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

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BATTERY CHARGER ADAPTER 18.5V 65W 3.51A

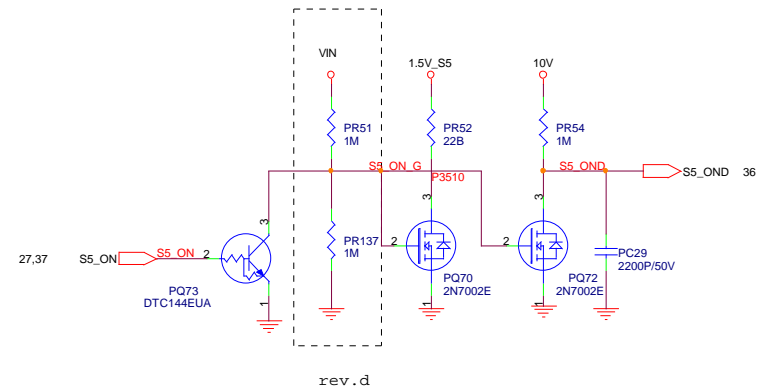
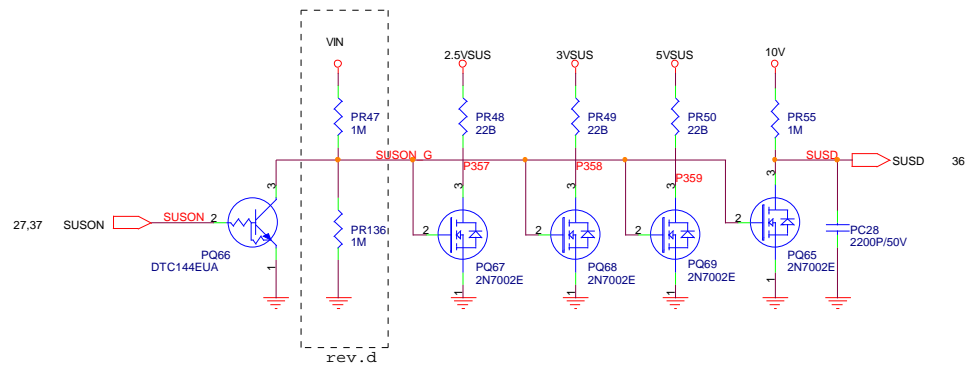
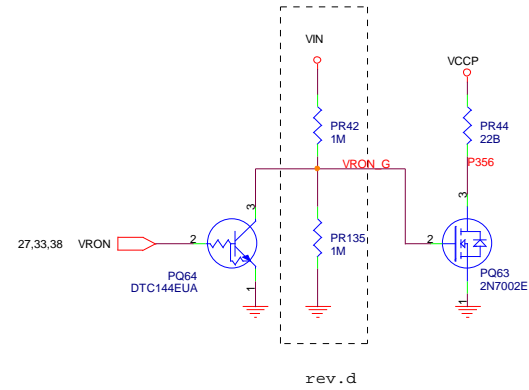
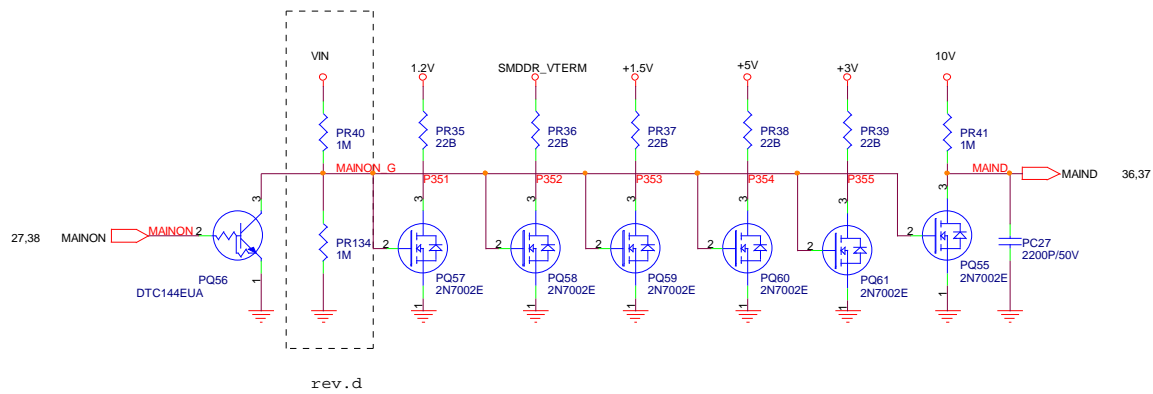


$I_{source_Max} = V_{cls}/0.8$

Charge Current = $VICTL * 1.24$

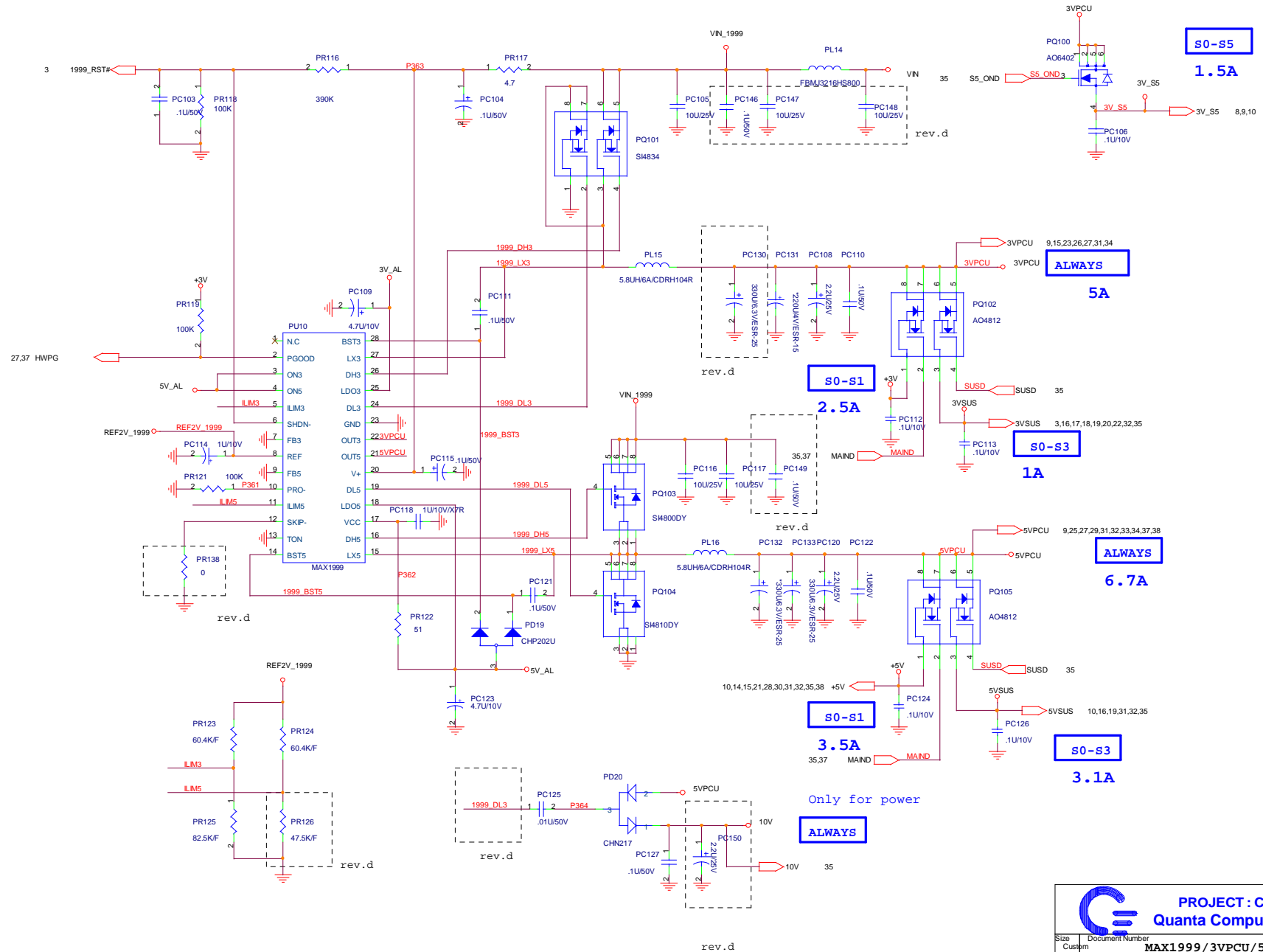
CELL-SET
 HI = LDO = 4 CELL
 LOW = LDO/2 = 3 CELL

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		3A
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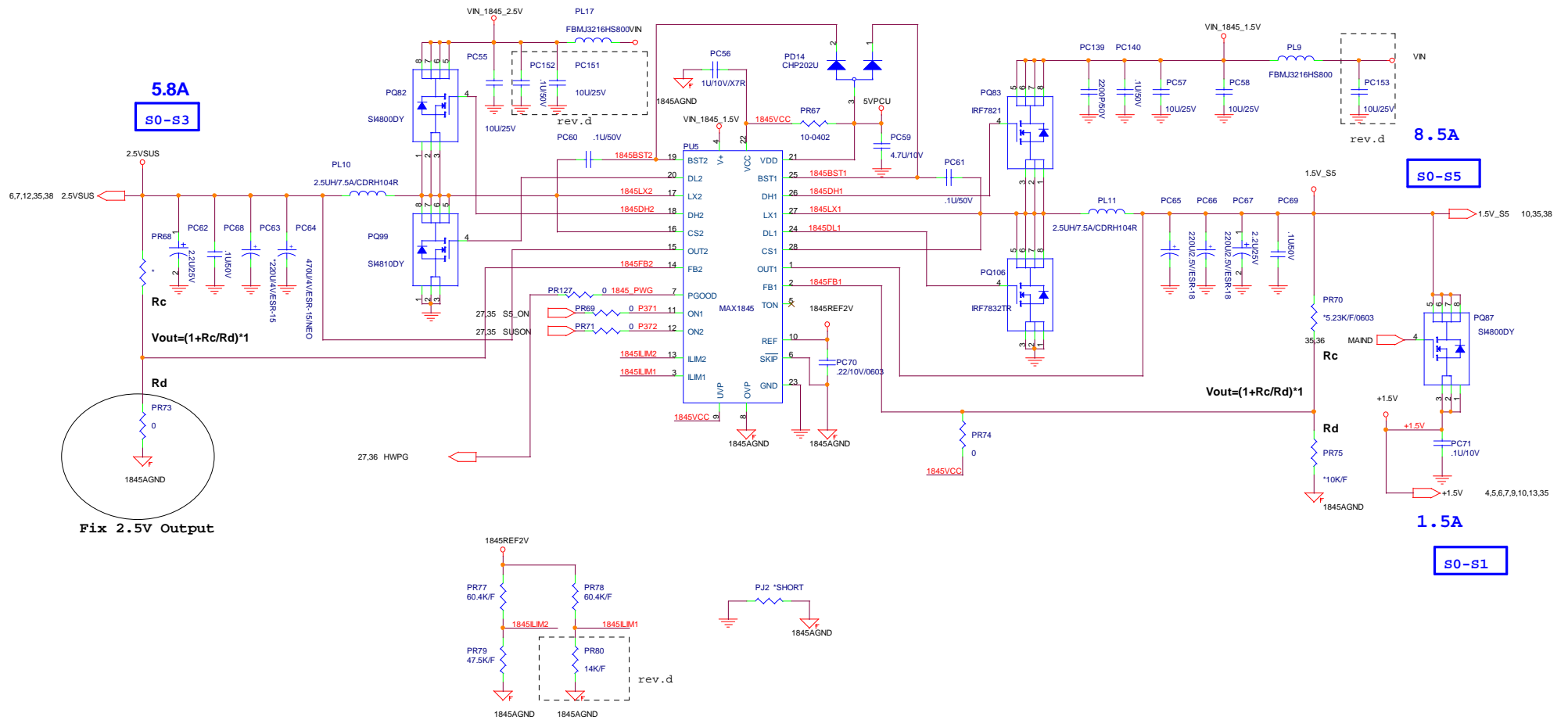
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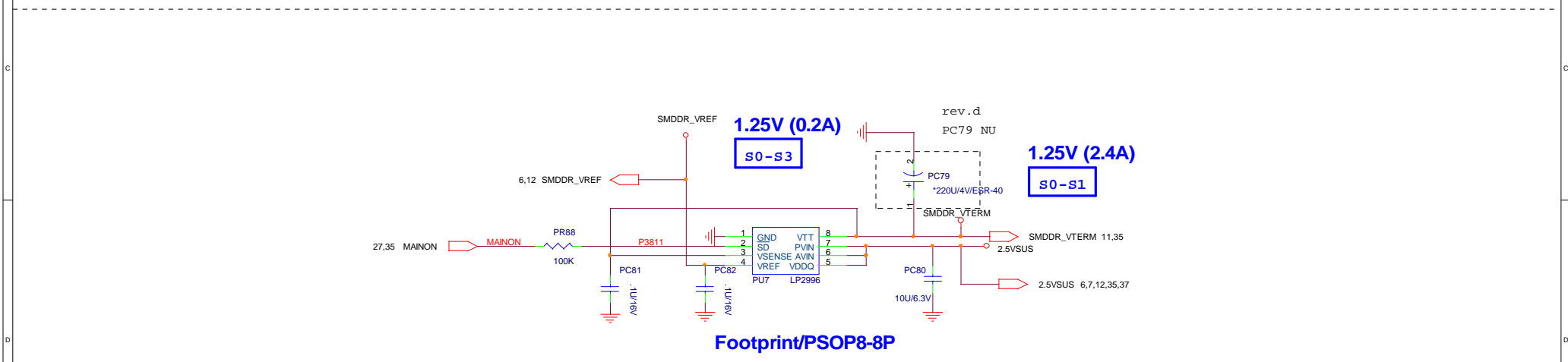
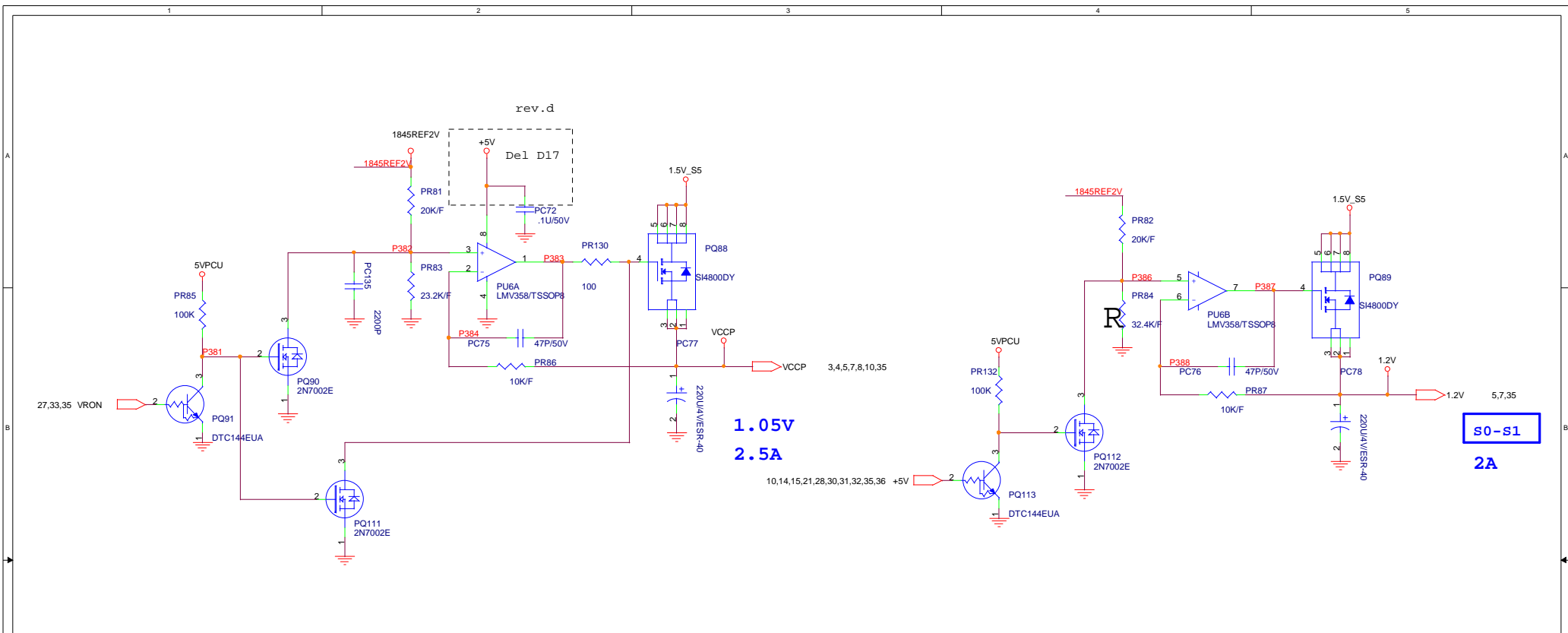
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Fix 2.5V Output

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		1A
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