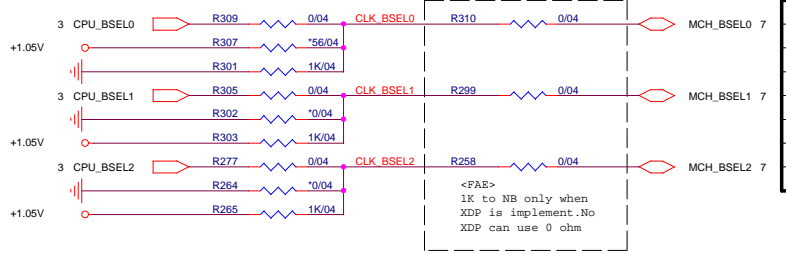


CPU Clock select



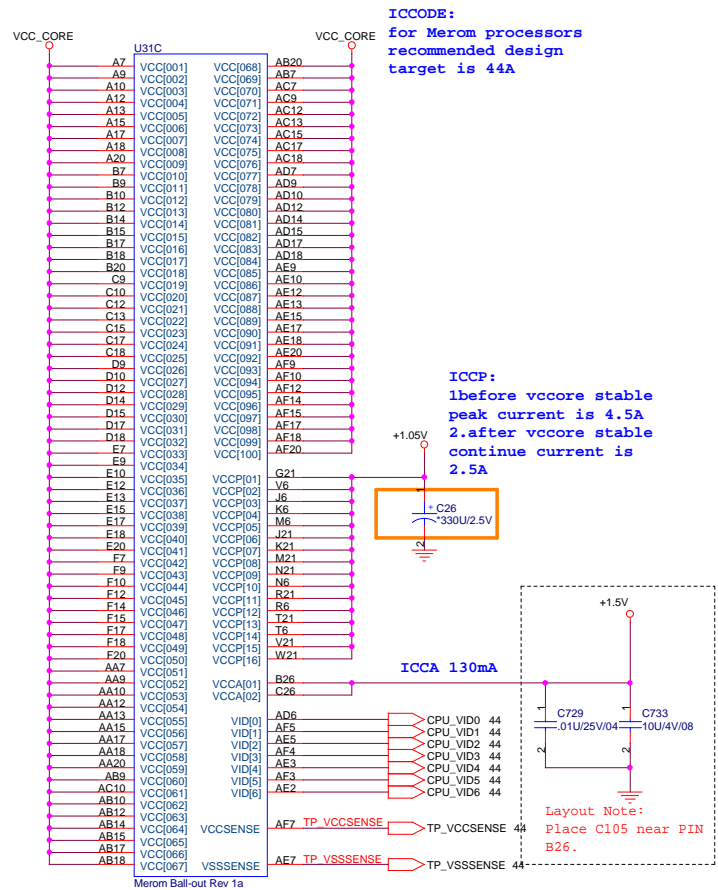
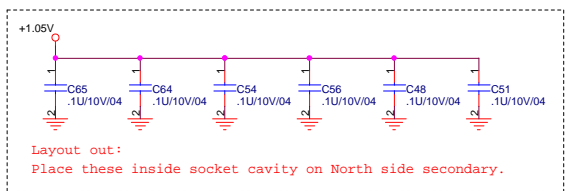
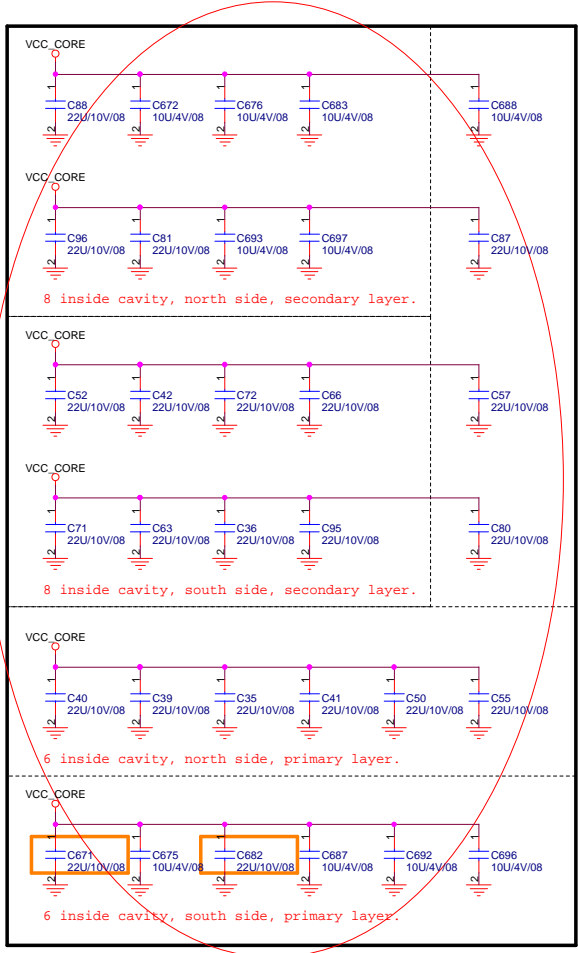
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

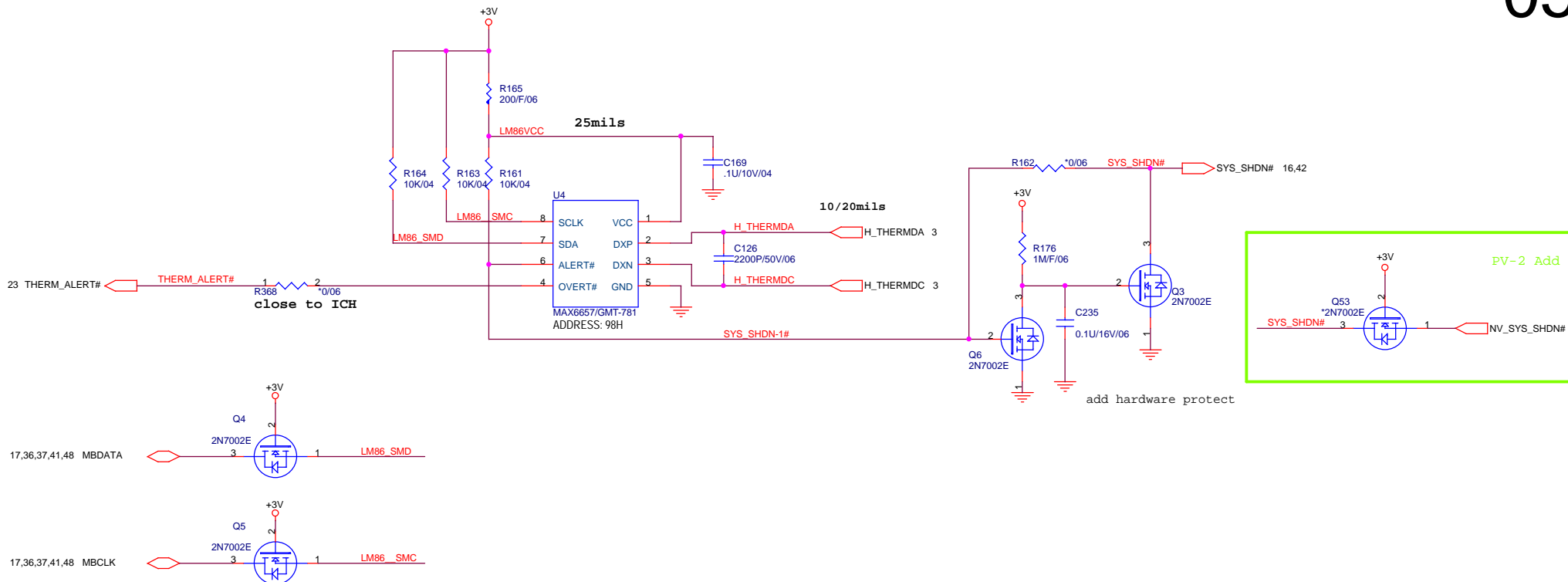
GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS



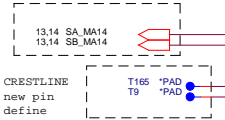
PROJECT : AT5
Quanta Computer Inc.



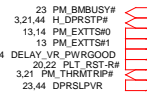
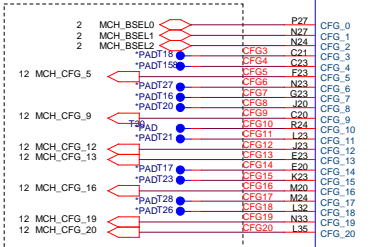


<p>NBS/RD1/HW2</p>	<p>PROJECT : AT5 Quanta Computer Inc.</p>		
	<p>Size B</p>	<p>Document Number THERMAL LM86</p>	<p>Rev 1A</p>
	<p>Date: Monday, March 19, 2007</p>		<p>Sheet 5 of 48</p>

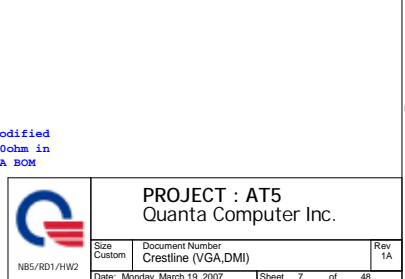
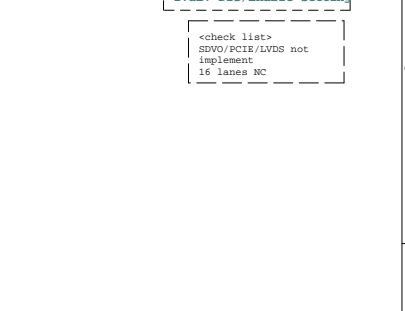
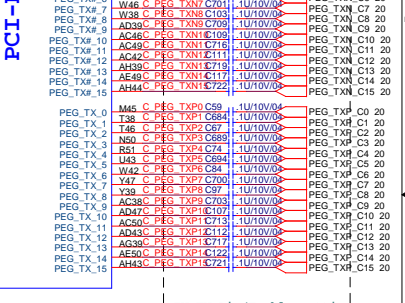
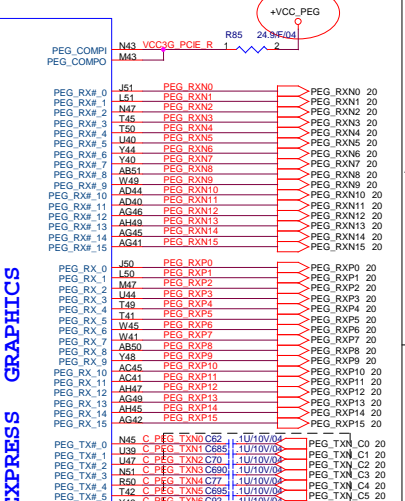
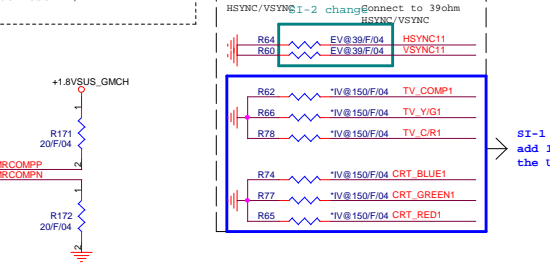
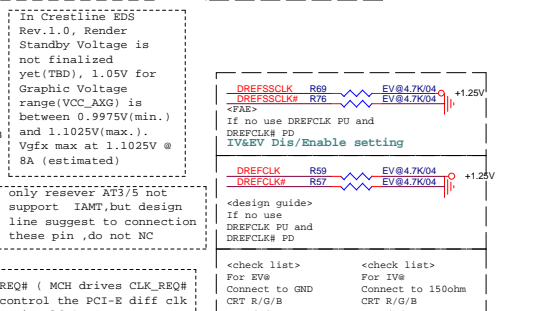
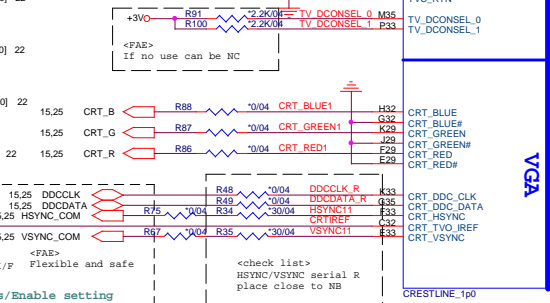
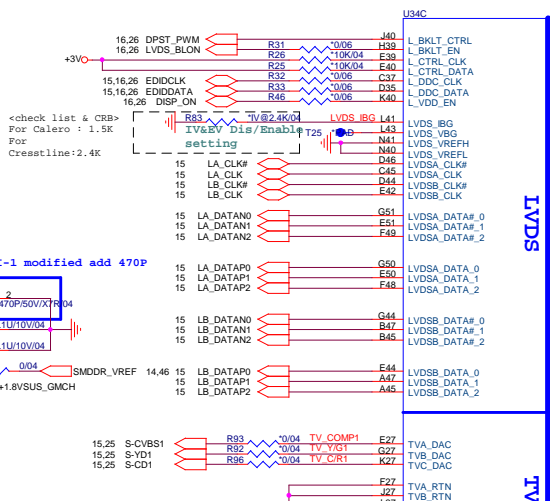
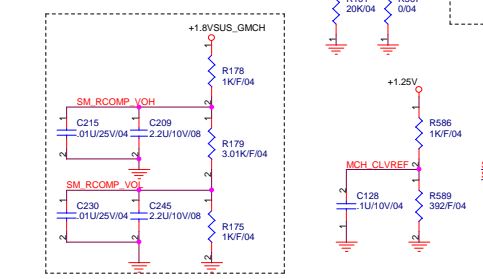
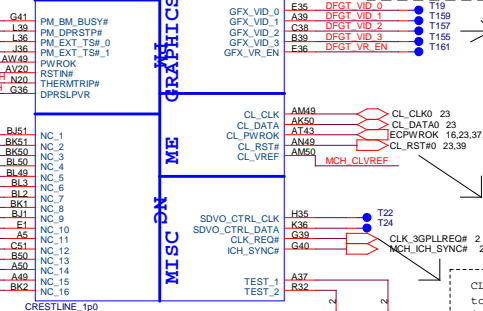
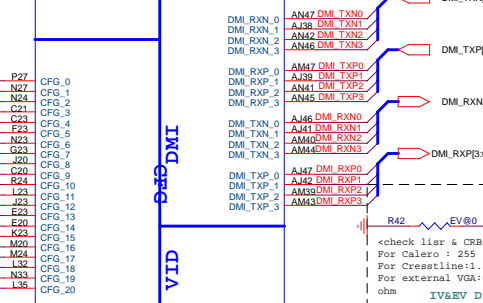
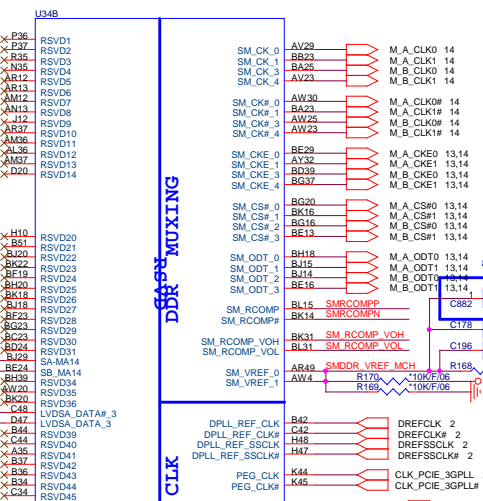
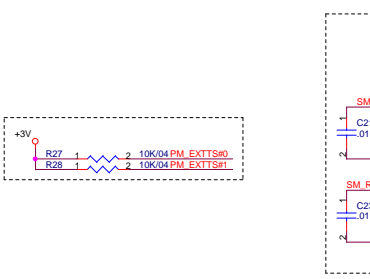
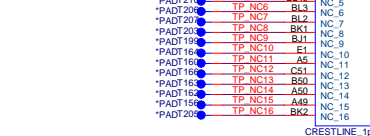
W22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs

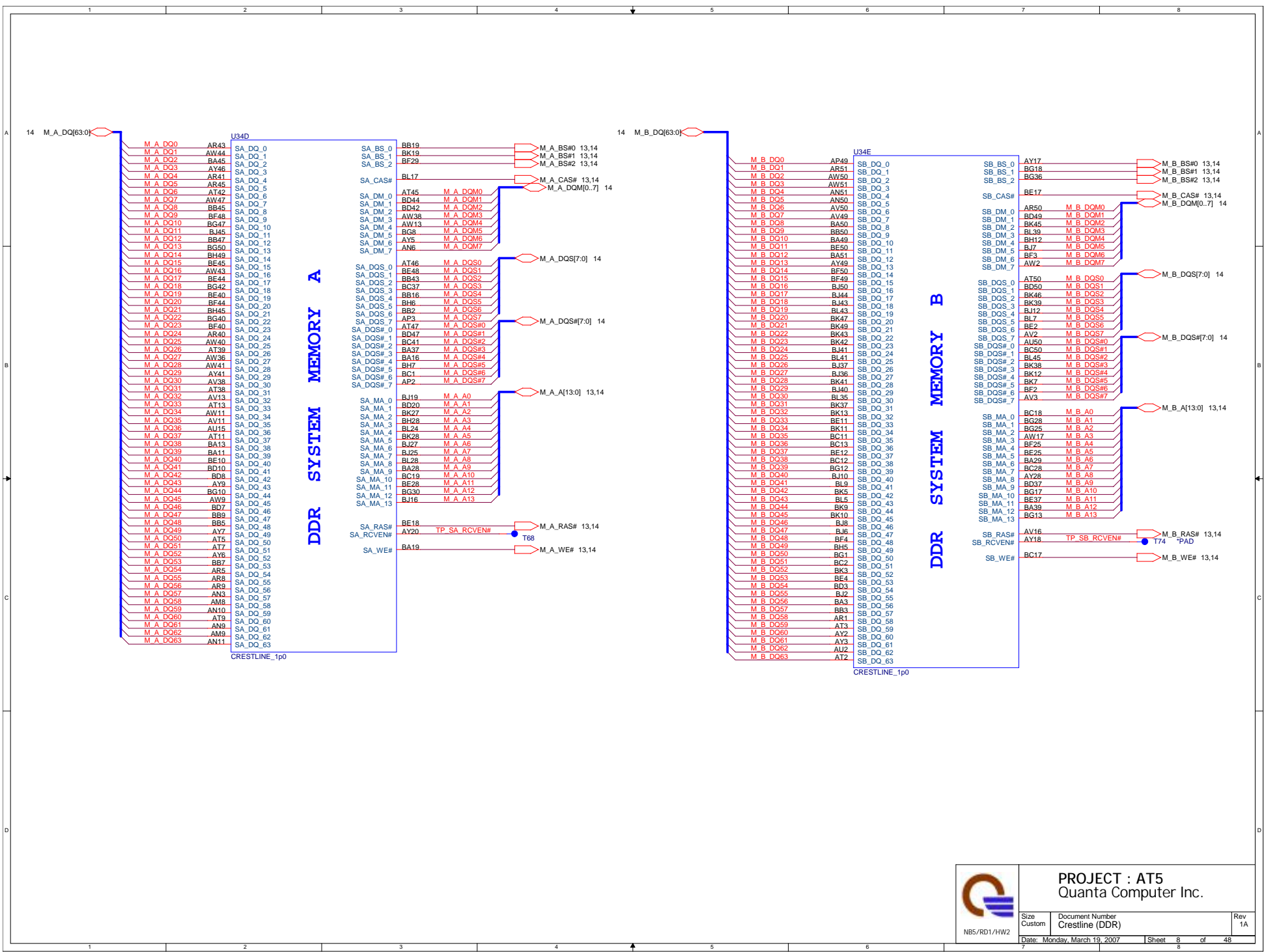


Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.



GMCH pwrack is 3.3v tolerant

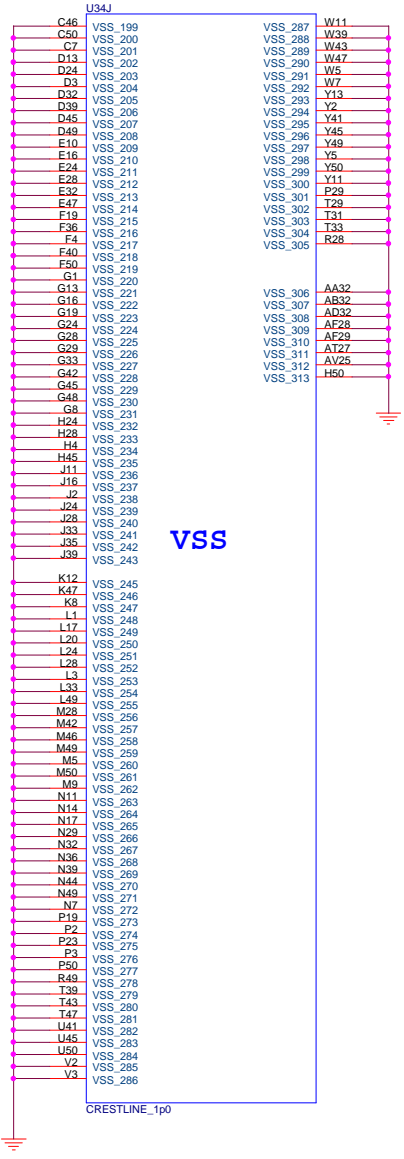
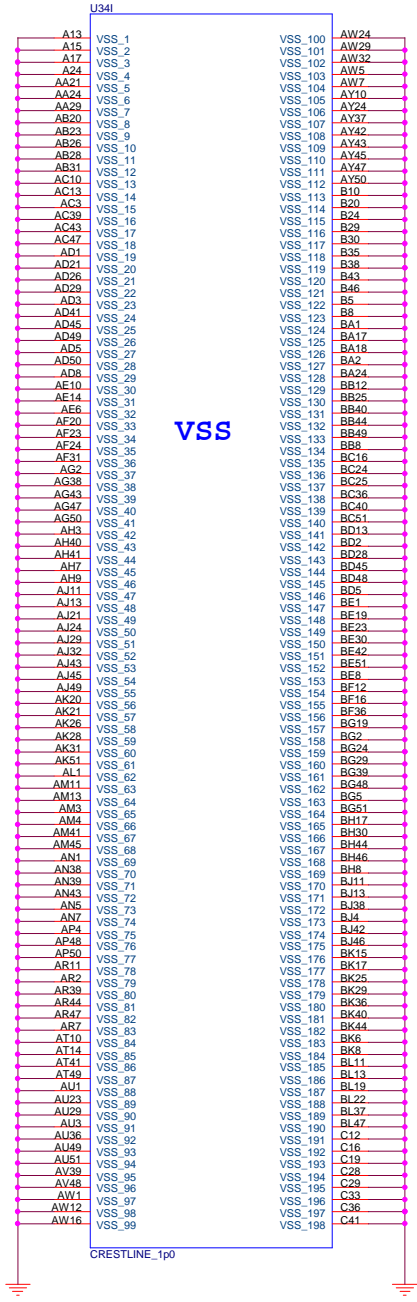




PROJECT : AT5
Quanta Computer Inc.

Size Custom	Document Number Crestline (DDR)	Rev 1A
Date: Monday, March 19, 2007		Sheet 8 of 48

NB5/RD1/HW2



PROJECT : AT5
 Quanta Computer Inc.

Size Custom	Document Number Crestline (VSS)	Rev 1A
Date: Monday, March 19, 2007		Sheet 11 of 48

Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
 CFG[17:3] Have internal Pull-up
 CFG[18:19] Have internal Pull-down
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMI X4(Default)
-----------	--

DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--

XOR /ALLz /Clock Un-gating

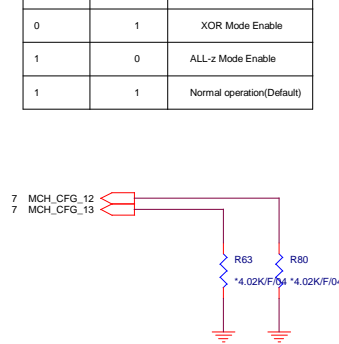
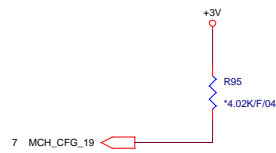
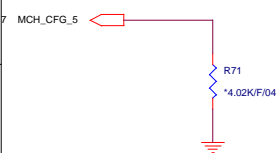
MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

SDVO Present

Strap define at External DVI control page

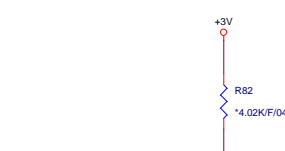
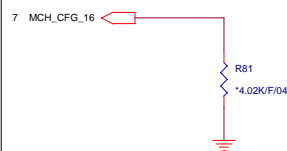


FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---

SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO and PCIE X1 are operating simultaneously via the PEG port
------------	---

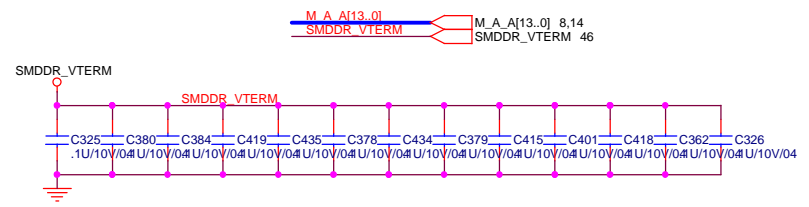


PROJECT : AT5
Quanta Computer Inc.

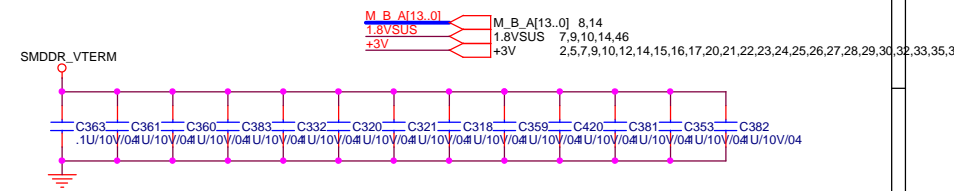
Size Custom	Document Number 10 - GMCH STRAP-3(6 of 6)	Rev 1A
Date: Monday, March 19, 2007		Sheet 12 of 48

DDRII DUAL CHANNEL A,B.

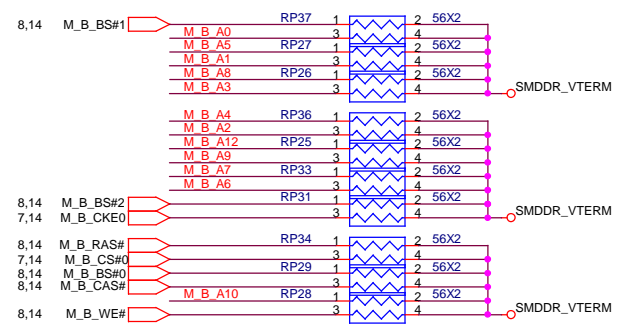
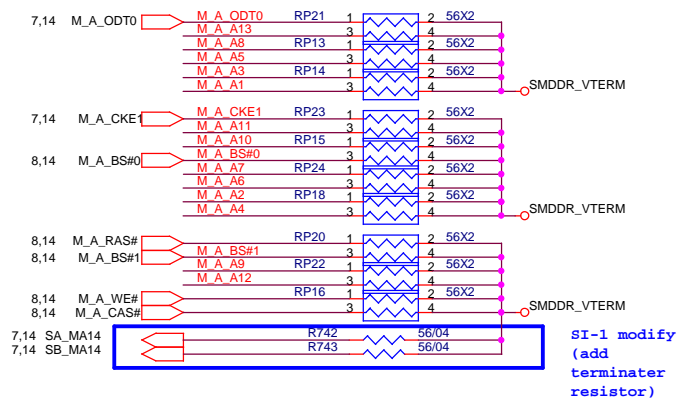
DDRII A CHANNEL



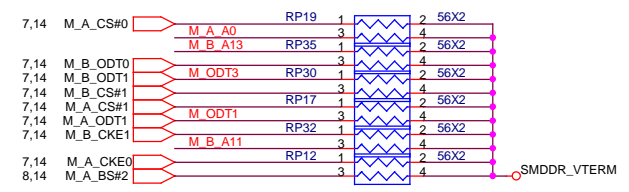
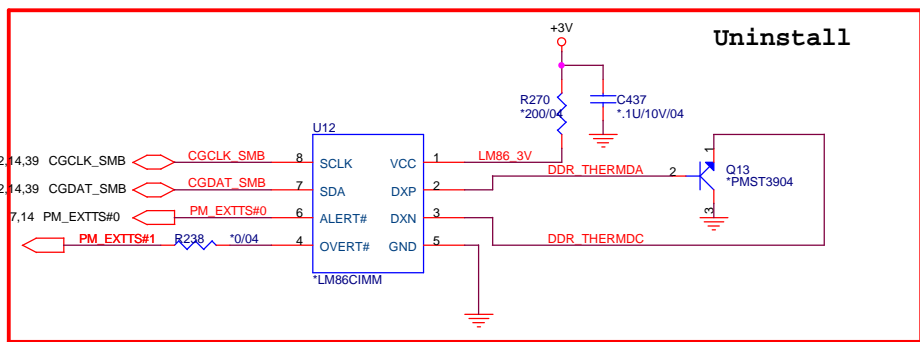
DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



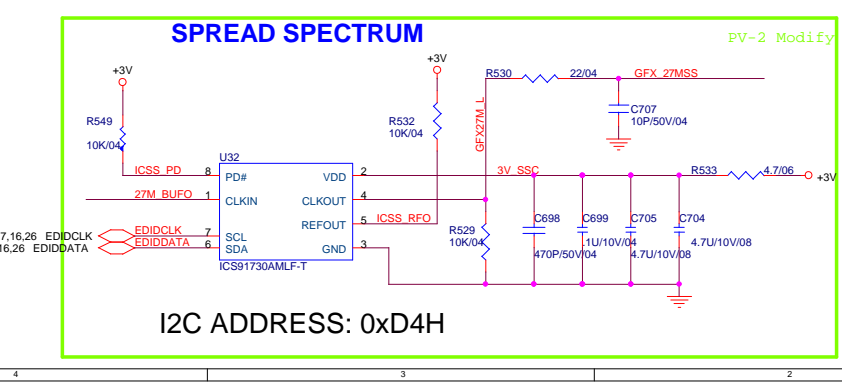
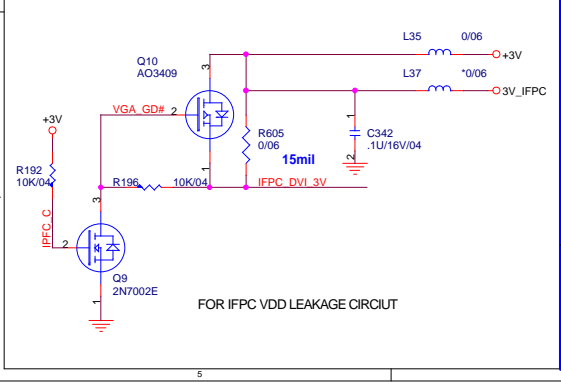
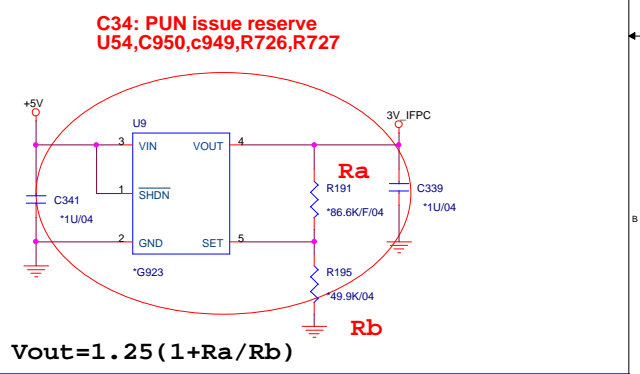
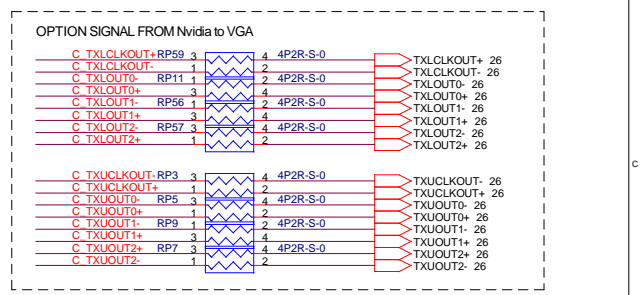
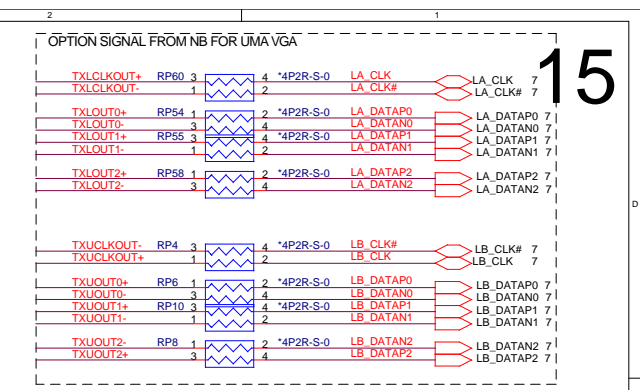
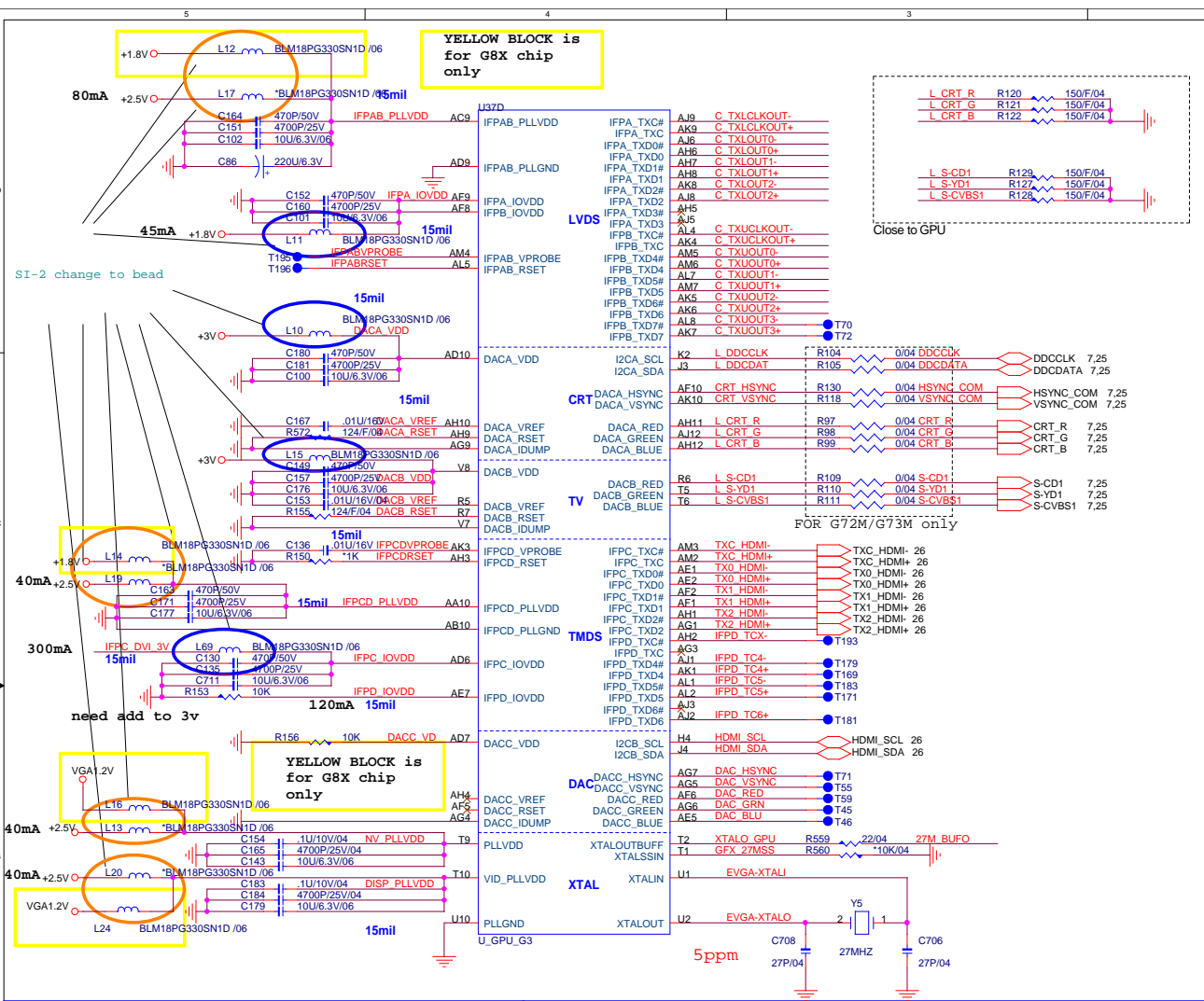
SI-1 modify
(add terminator resistor)



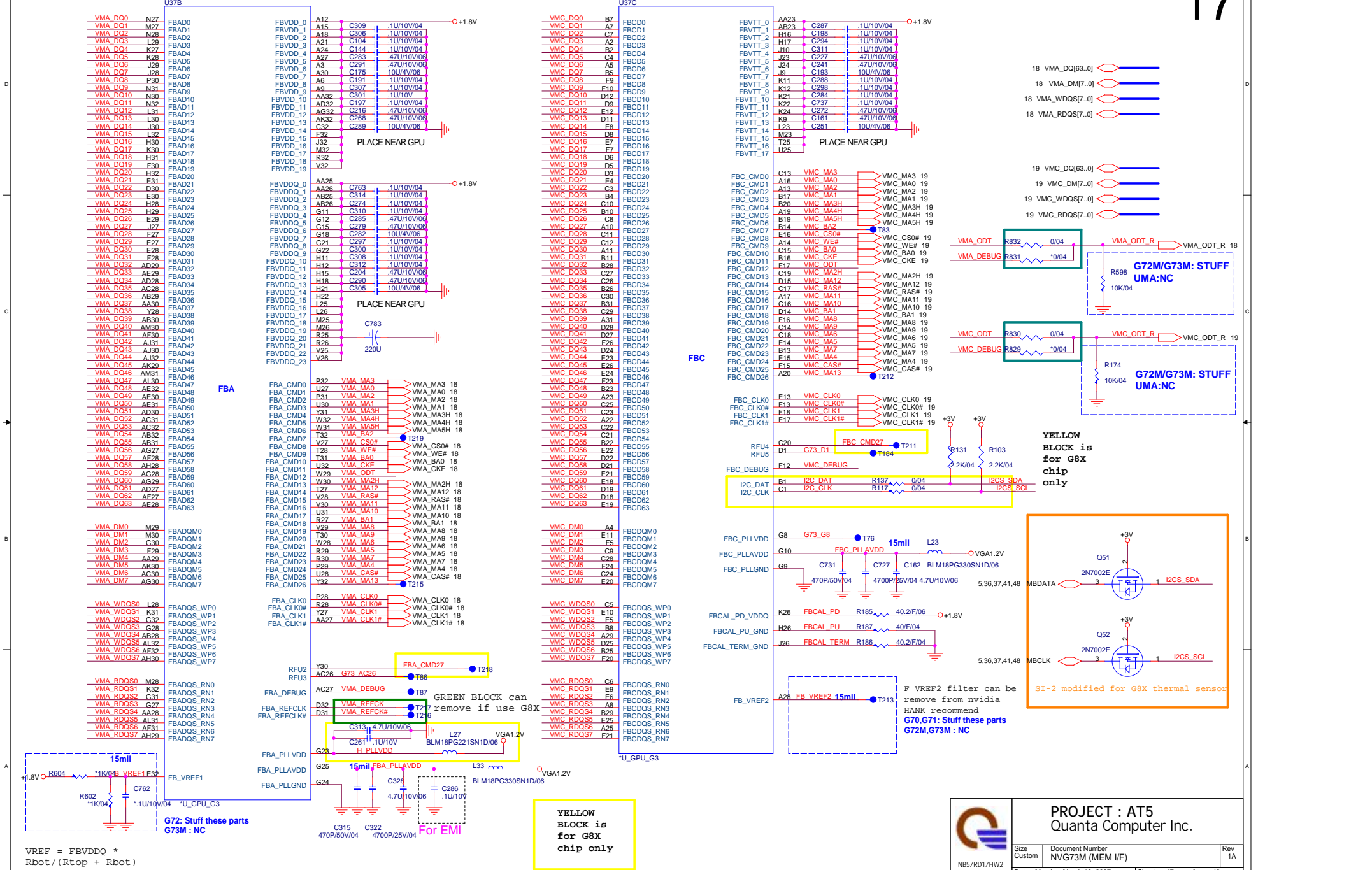
PROJECT : AT5
Quanta Computer Inc.

Size B	Document Number DDRII RES.ARRAY	Rev 1A
Date: Monday, March 19, 2007 Sheet 13 of 48		

NBS/RD1/HW2



Channel C is available on G73M only



VREF = FBVDDQ * Rbot / (Rtop + Rbot)

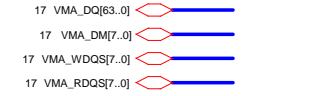
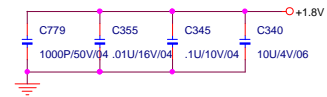
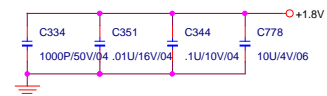
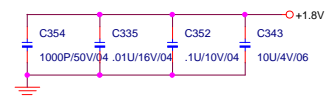
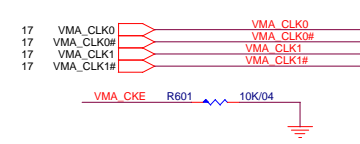
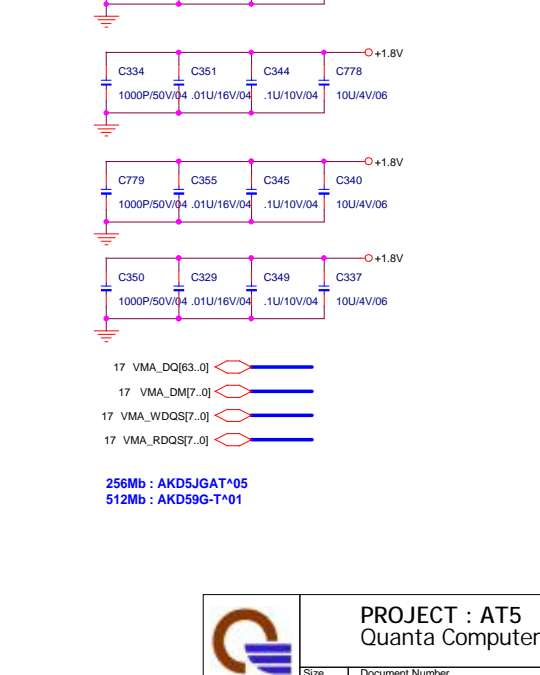
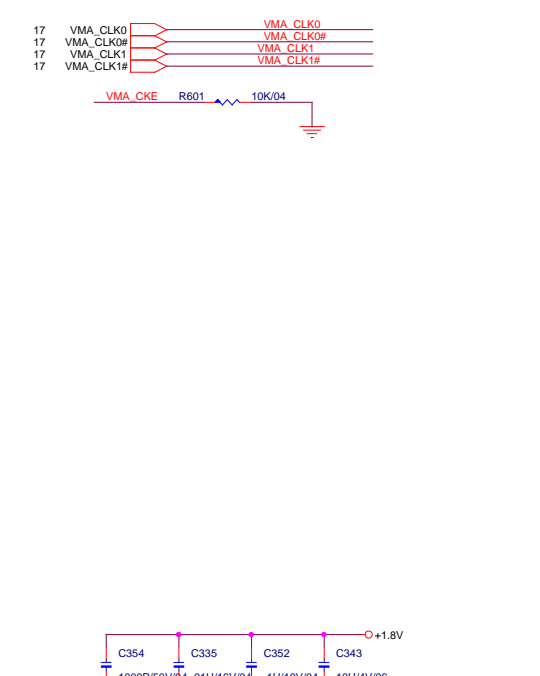
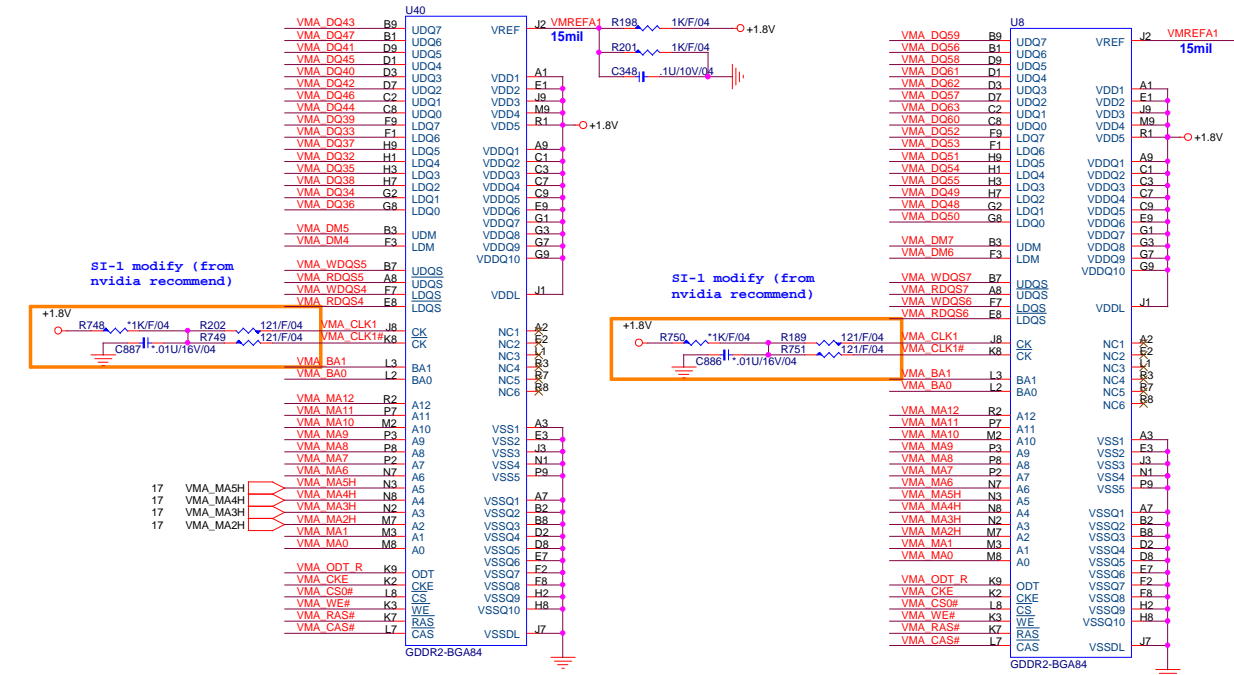
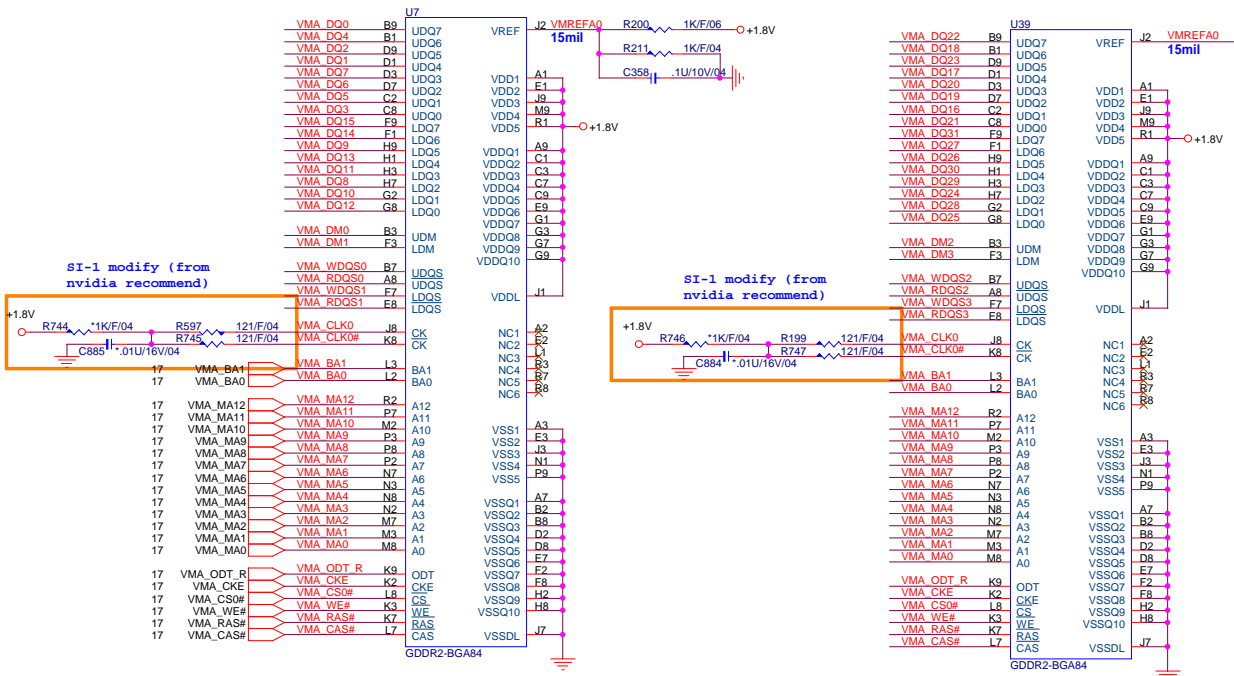
YELLOW BLOCK is for G8X chip only

YELLOW BLOCK is for G8X chip only

F_VREF2 filter can be remove from nvidia HANK recommend G70,G71: Stuff these parts G72M,G73M : NC



PROJECT : AT5
Quanta Computer Inc.

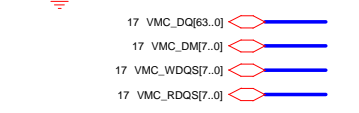
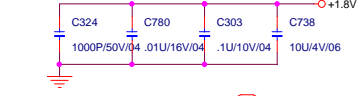
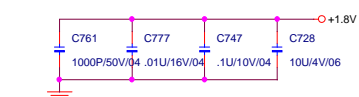
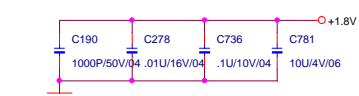
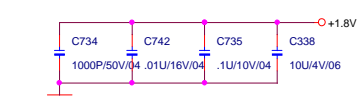
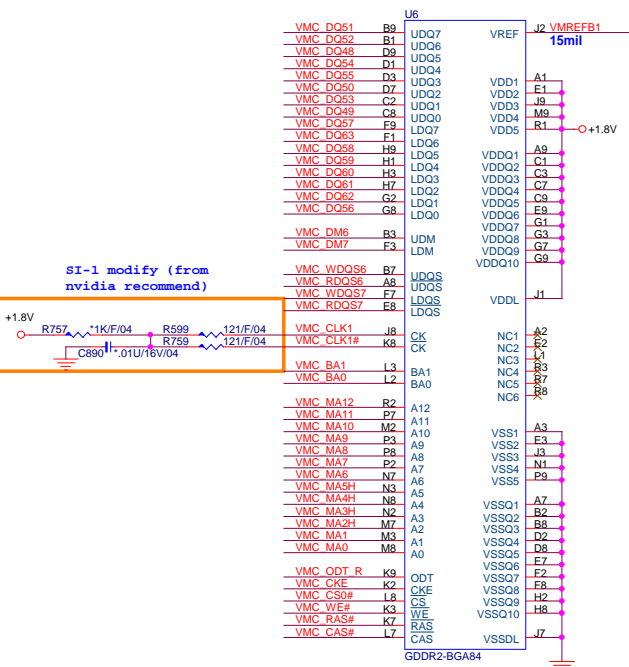
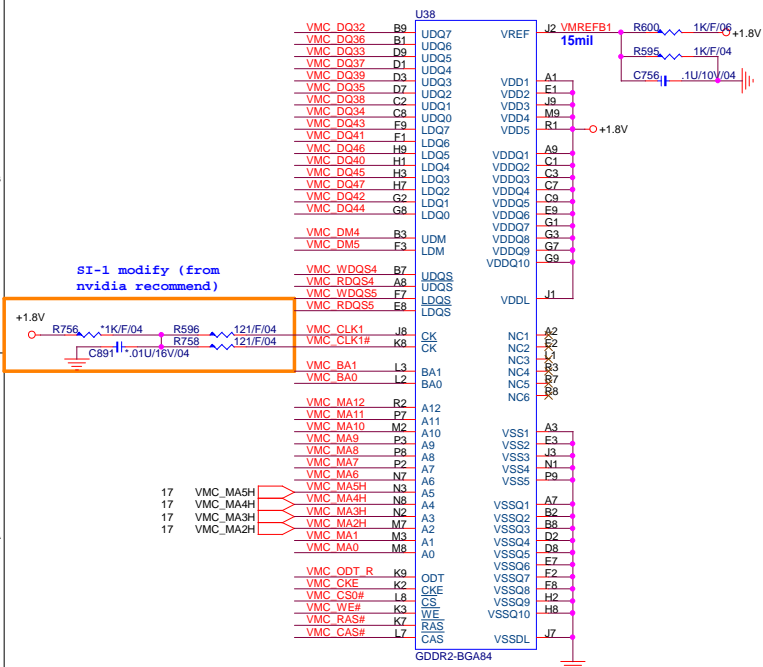
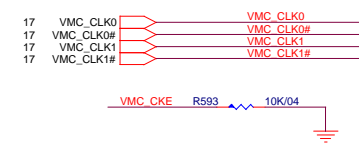
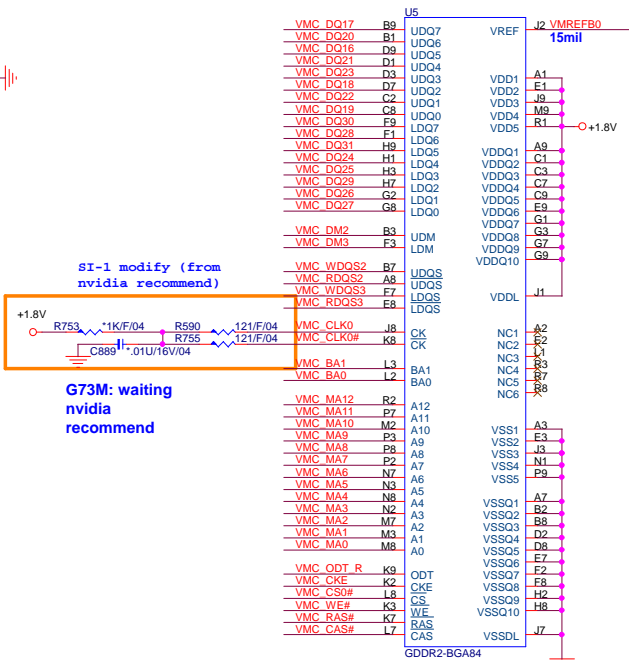
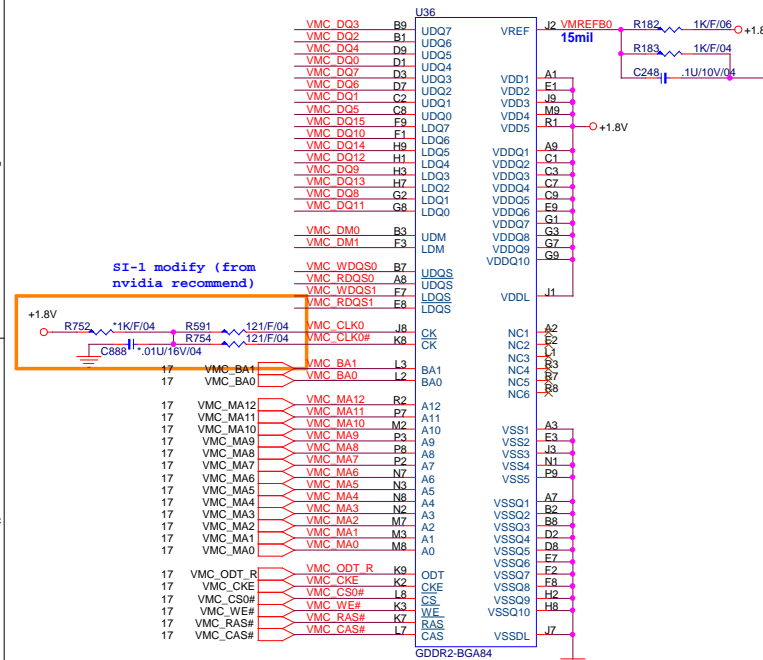


256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01

PROJECT : AT5
Quanta Computer Inc.

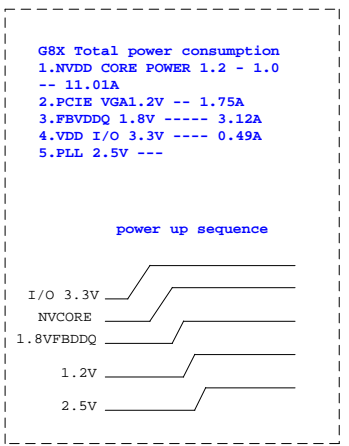
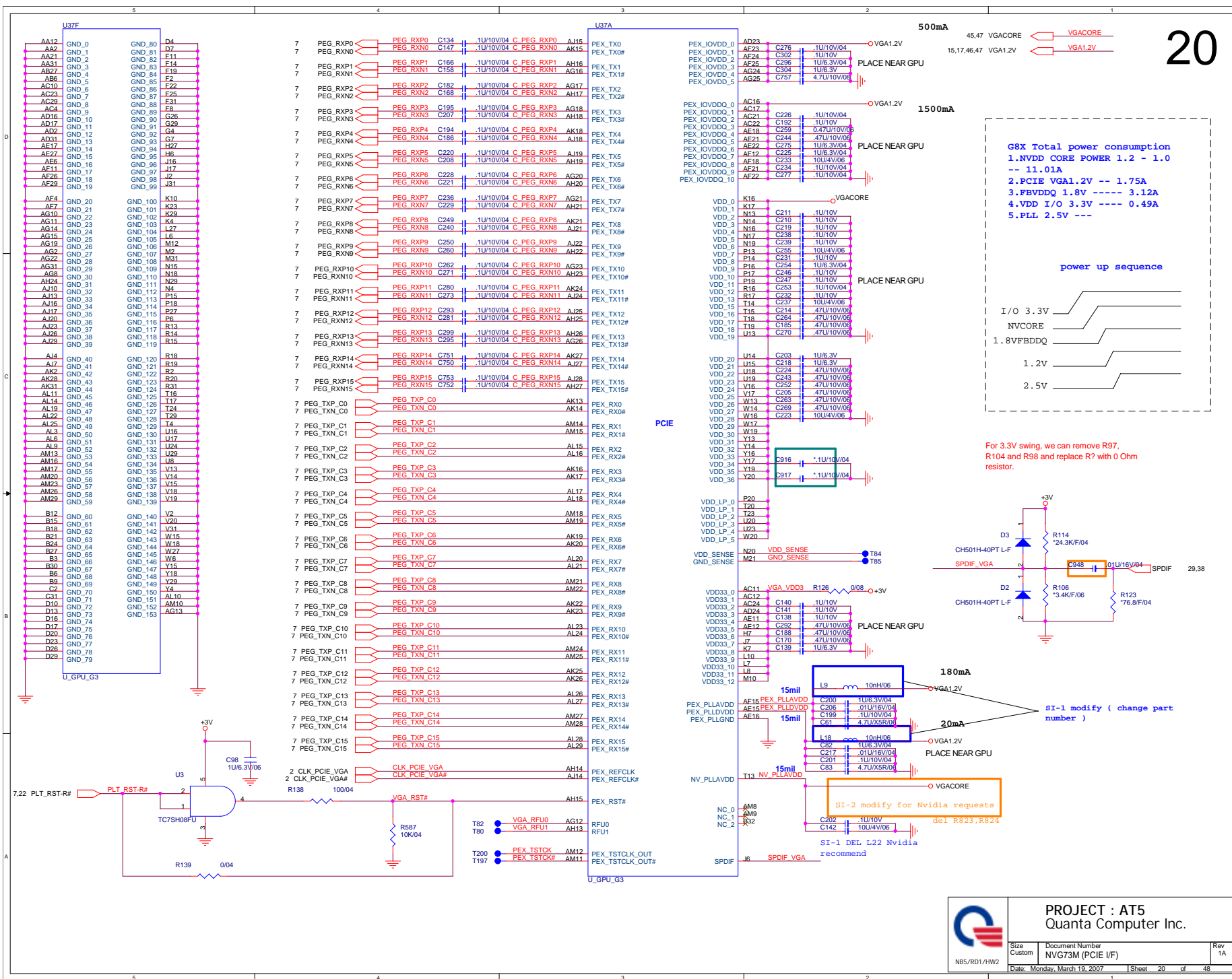
Size Custom	Document Number NVG73M VRAN-1(GDDR2 BGA84)	Rev 1A
Date: Monday, March 19, 2007		Sheet 18 of 48



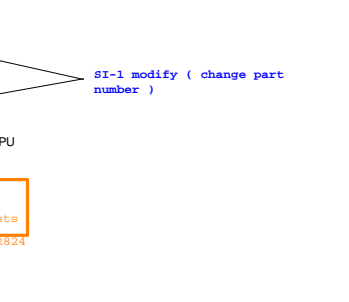
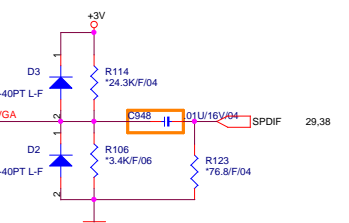


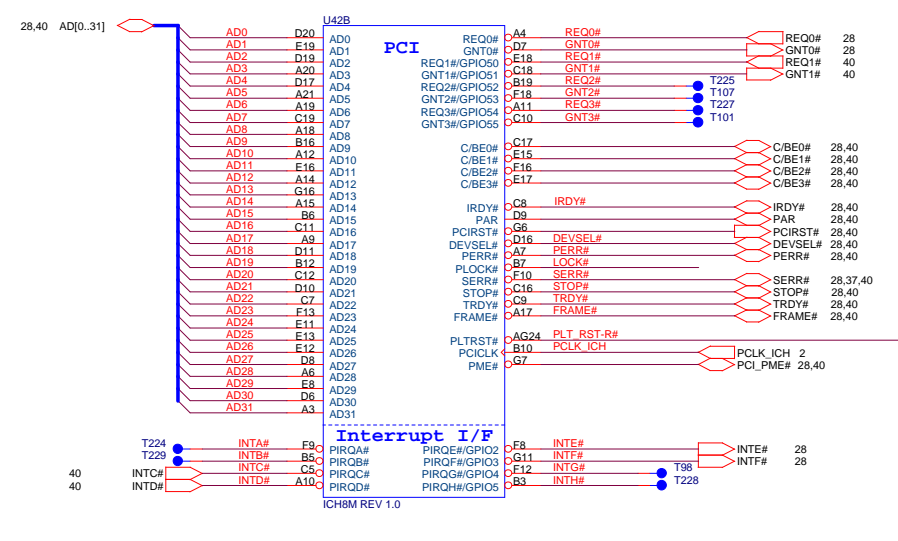
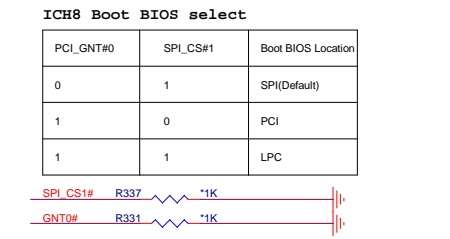
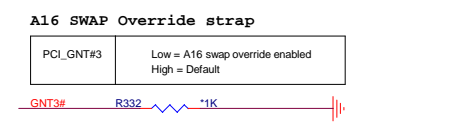
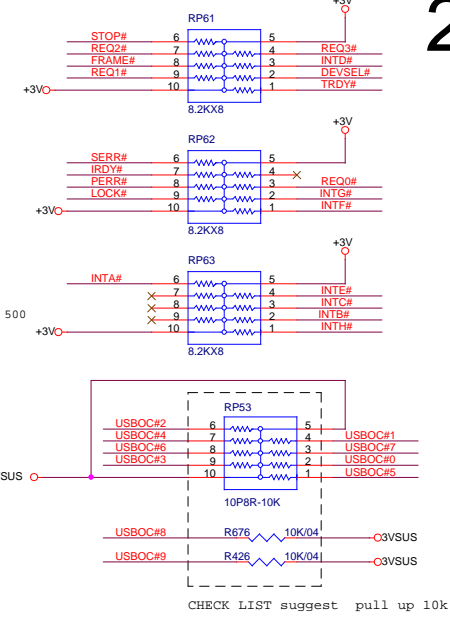
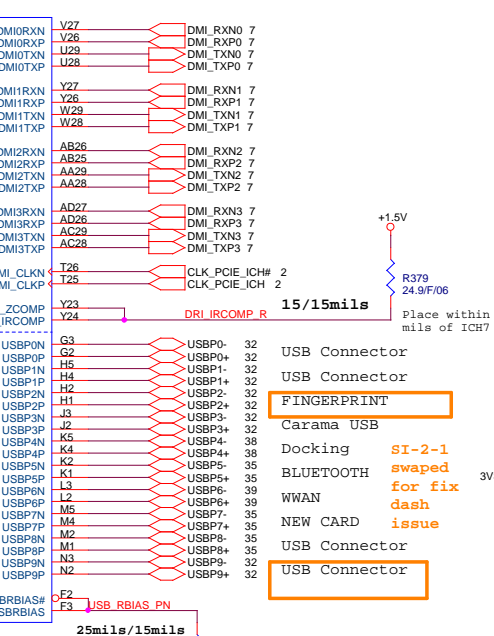
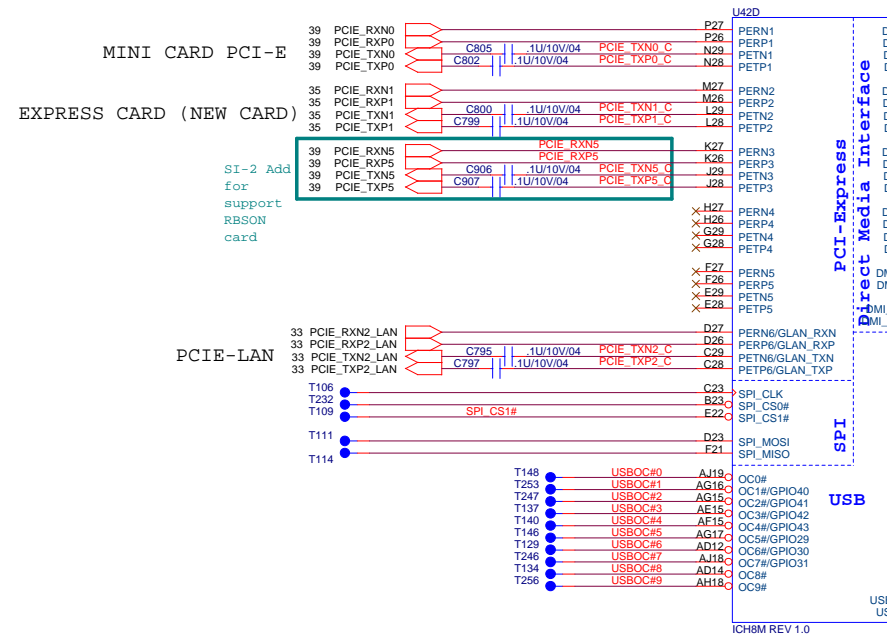
256Mb : AKD5JGAT*05
512Mb : AKD59G-T*01

		PROJECT : AT5 Quanta Computer Inc.	
		Size Custom Document Number NVG73M VREM-2(GDDR2 BGA84) Date: Monday, March 19, 2007	Rev 1A Sheet 19 of 48

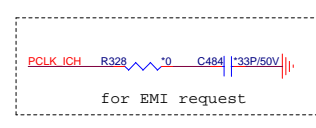
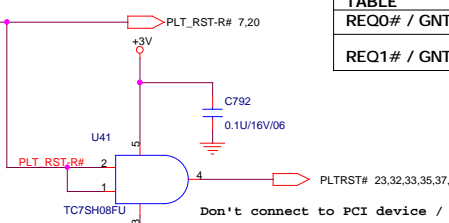


For 3.3V swing, we can remove R97, R104 and R98 and replace R7 with 0 Ohm resistor.





PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

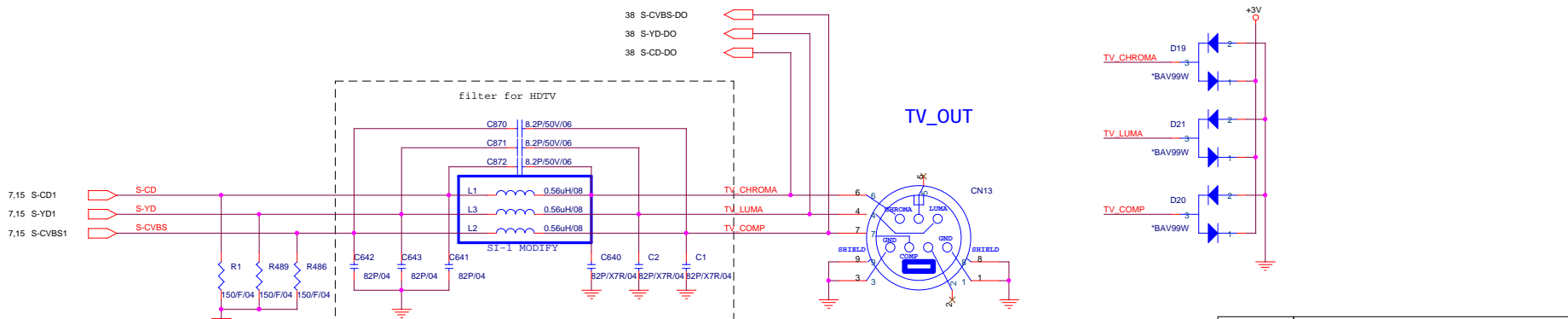
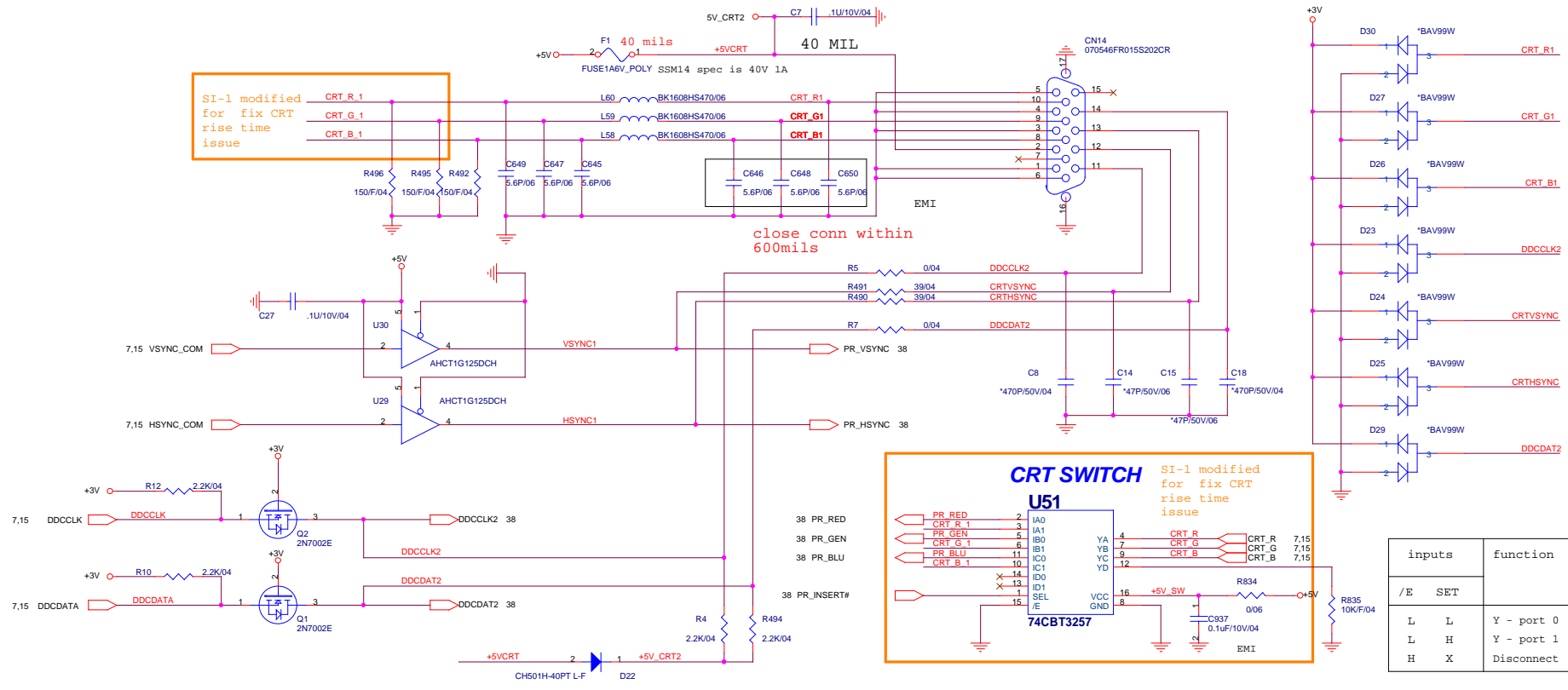



PROJECT : AT5
Quanta Computer Inc.

Size Custom Document Number ICH7-M M PCI E(2/4) Rev 1A

Date: Monday, March 19, 2007 Sheet 22 of 48

CRT PORT

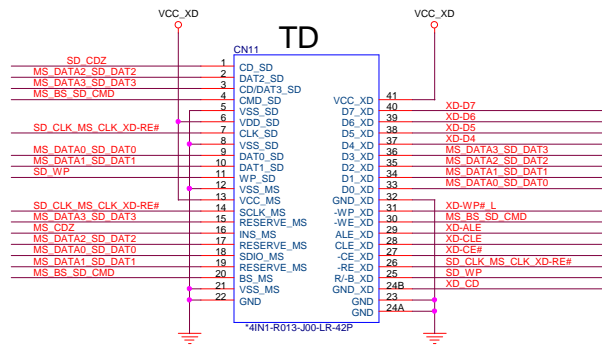
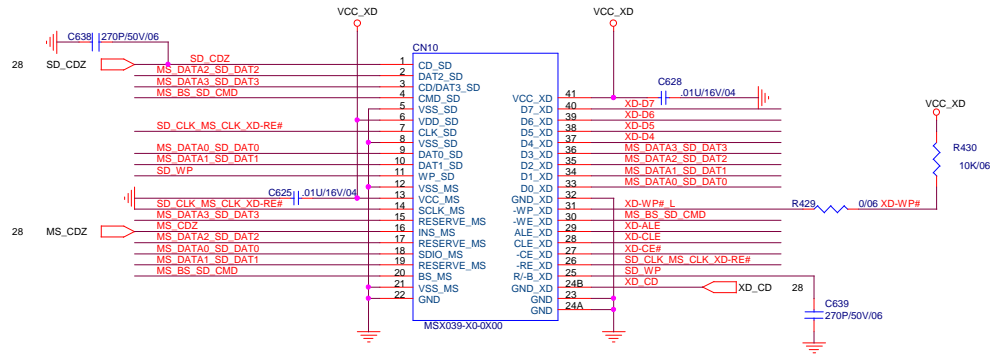




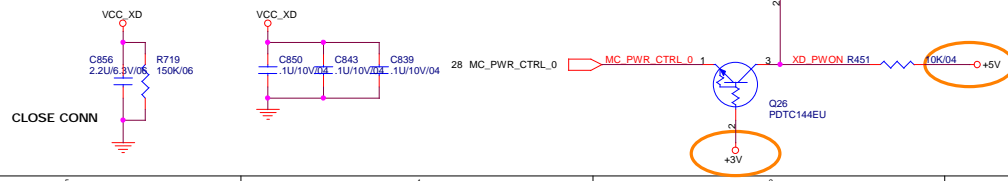
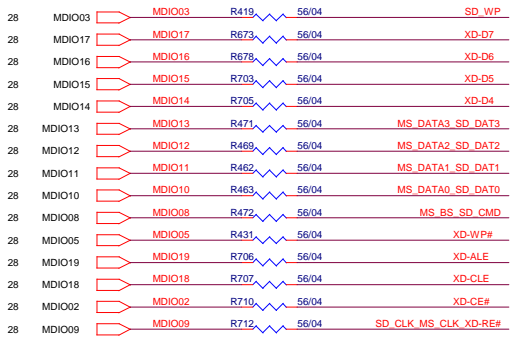
PROJECT : AT5
Quanta Computer Inc.

Size Custom	Document Number CRT/TV_OUT	Rev 1A
Date: Monday, March 19, 2007		Sheet 25 of 48

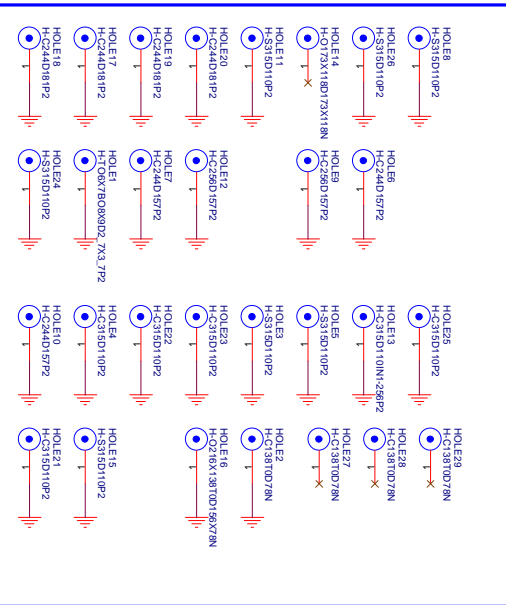
5 IN1 CARD READER
XD, MMC / SD, MS / MSP



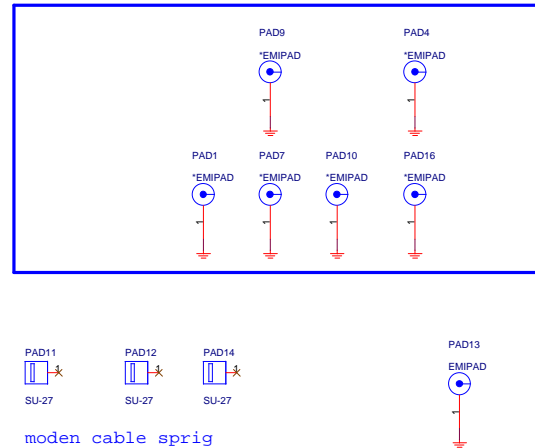
bom create 2'nd source



SCREW HOLE



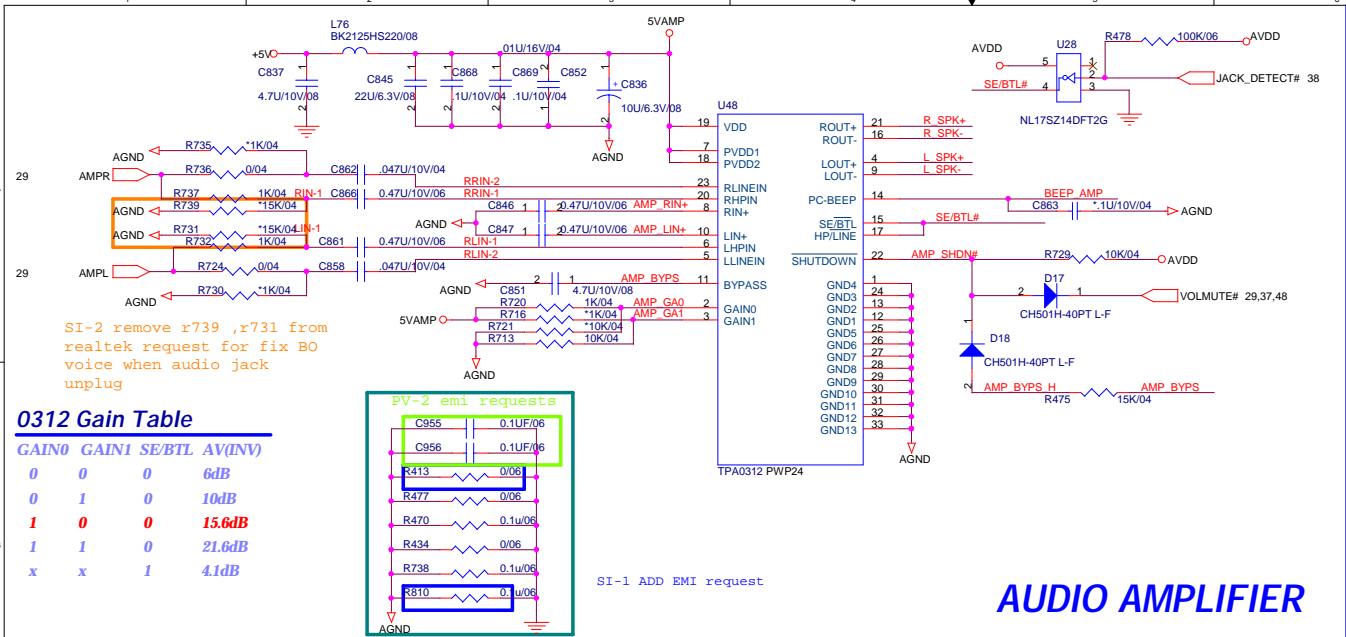
EMI PAD



PROJECT : AT5
Quanta Computer Inc.

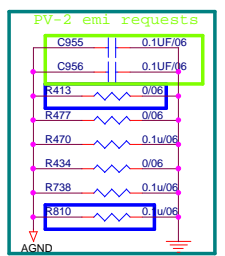
Size Custom	Document Number CARD READER/HOLE	Rev 1A
Date: Monday, March 19, 2007		Sheet 27 of 48

NBS/RD1/HW2



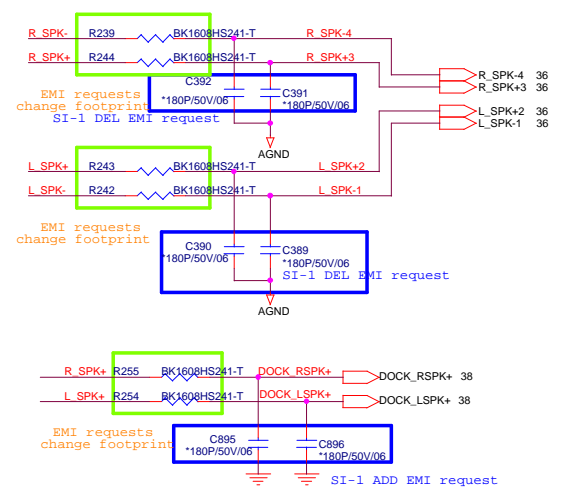
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

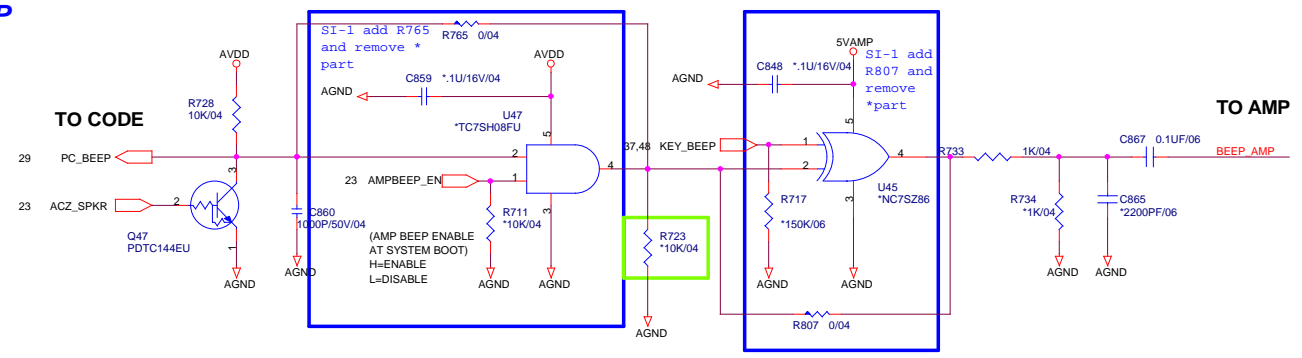


AUDIO AMPLIFIER

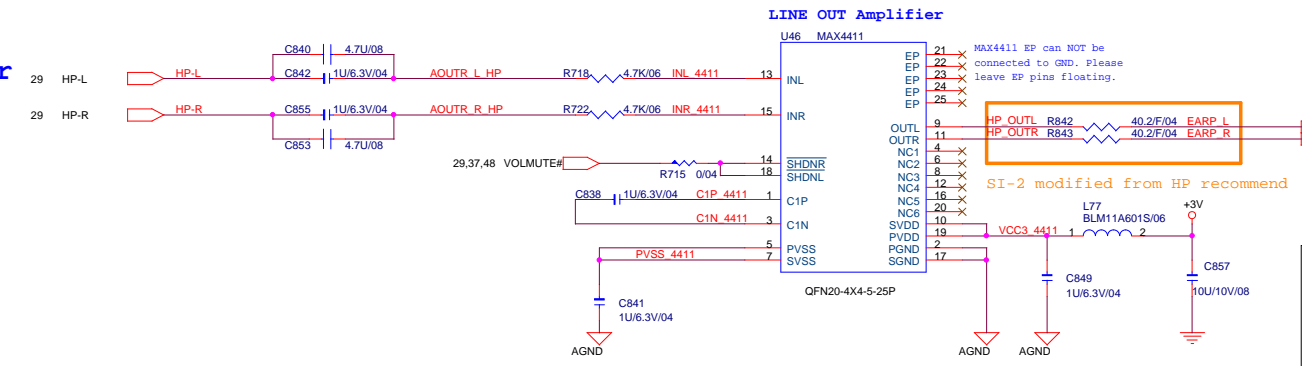
INT. SPEAKER



PCSPK BEEP



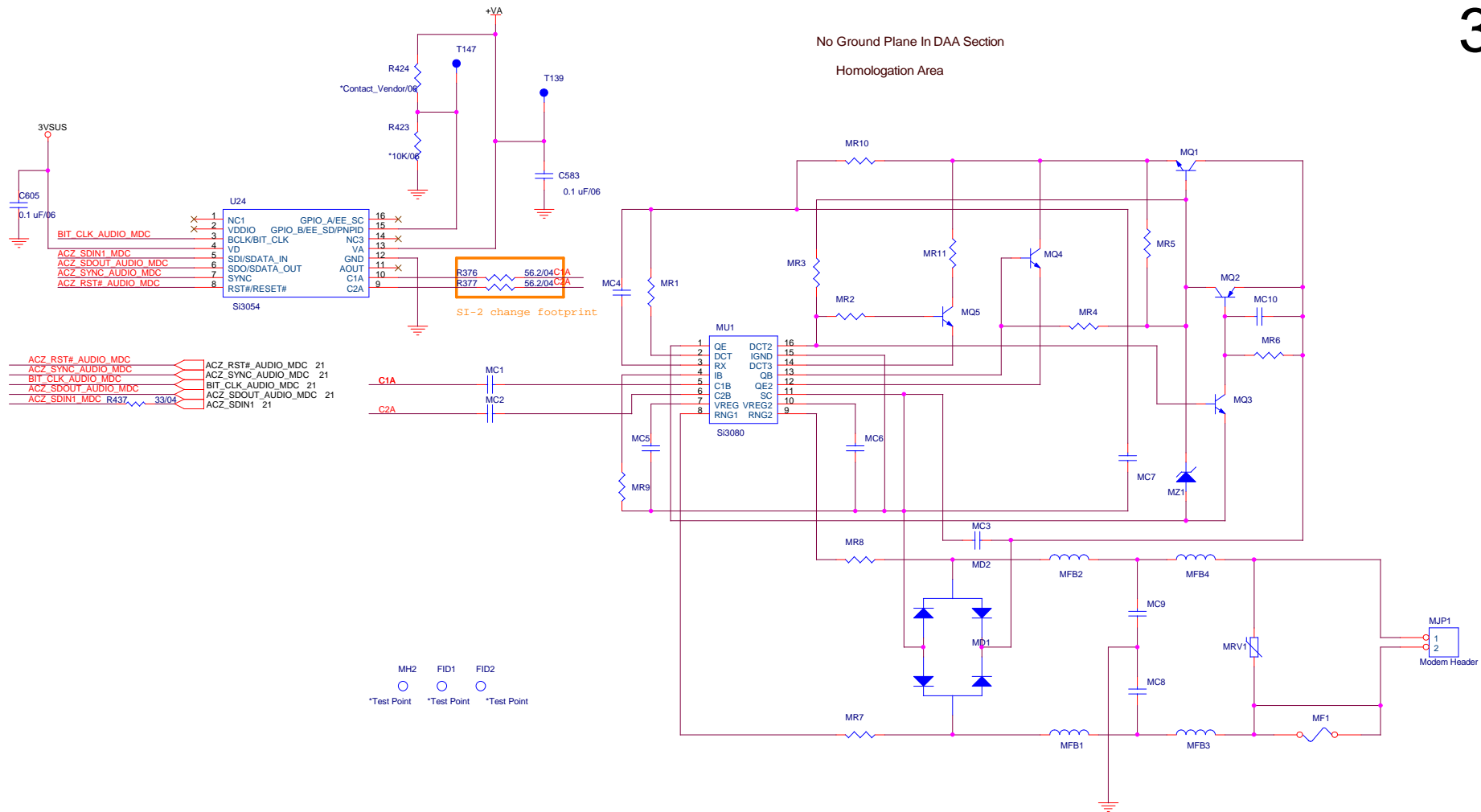
LINE OUT Amplifier



PROJECT : AT5
Quanta Computer Inc.


Size Custom	Document Number JACK/AMP_TAP0312	Rev 1A
Date: Monday, March 19, 2007		Sheet 30 of 48

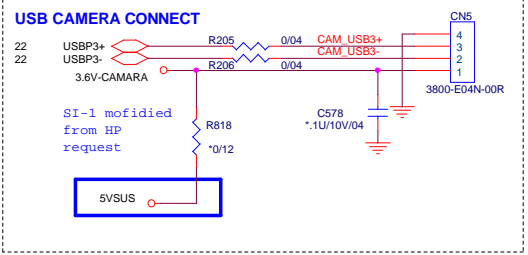
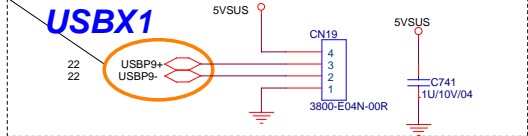
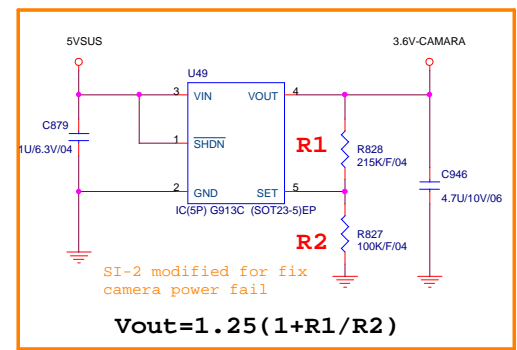
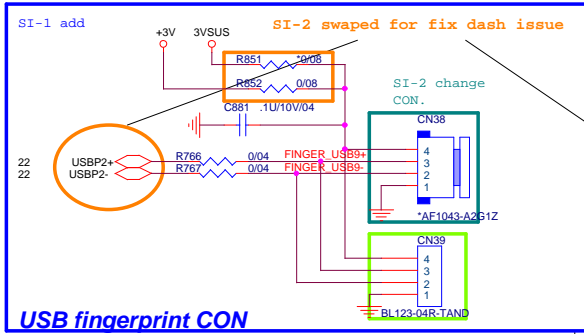
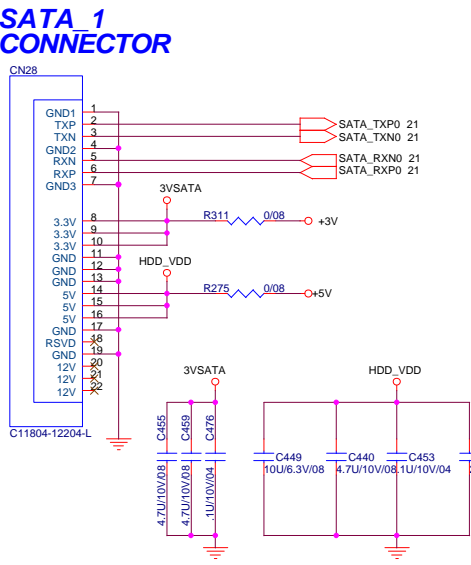
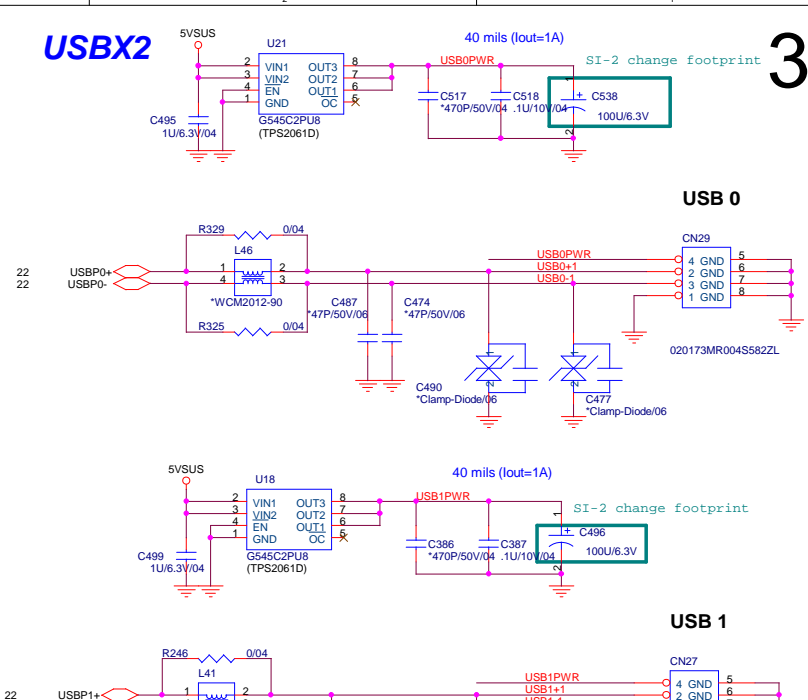
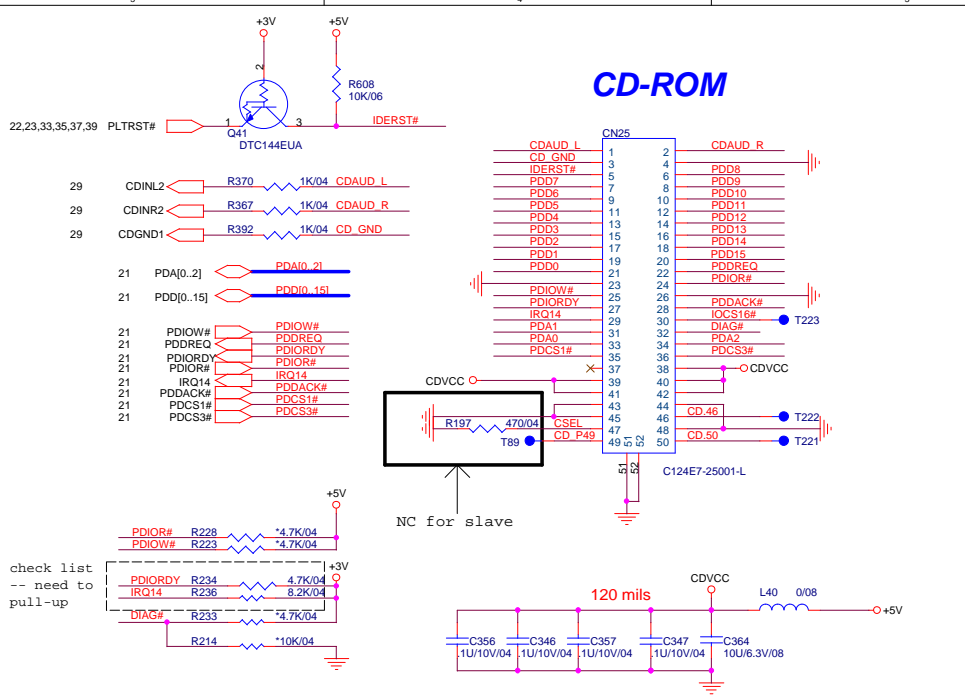
No Ground Plane In DAA Section
Homologation Area



DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL

		PROJECT : AT5 Quanta Computer Inc.	
		Size Custom	Document Number MODEM(DAA)
NB5/RD1/HW2		Date: Monday, March 19, 2007	Sheet 31 of 48



PROJECT : AT5
Quanta Computer Inc.

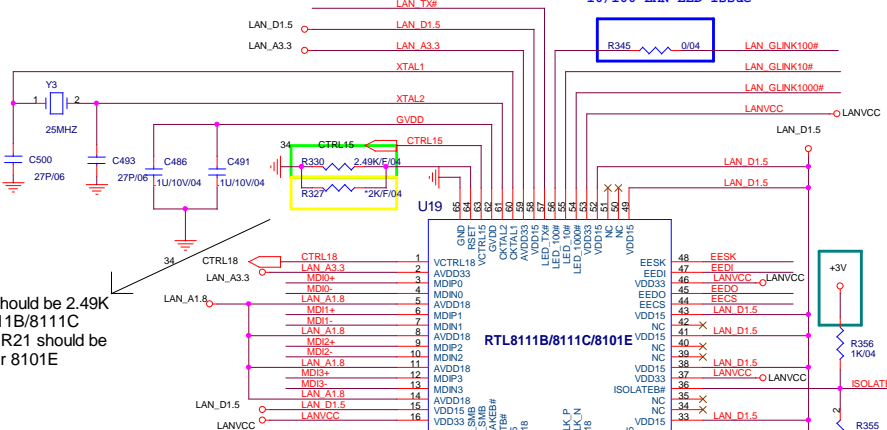
Size Custom	Document Number SATA HDD/CD-ROM/USBX3	Rev 1A
Date: Monday, March 19, 2007		Sheet 32 of 48

T : Stuffed for RTL8111B(10/100/1000)

giga LAN part number AJ081110006

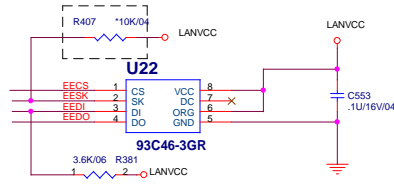
E : Stuffed for 8101E(10/100)

SI-1 BOM add to fix 10/100 LAN LED issue

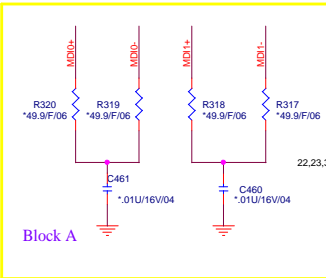


R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

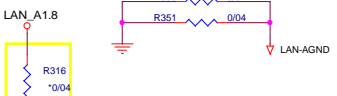
for 93C56 used. NC if 93C46 is used.



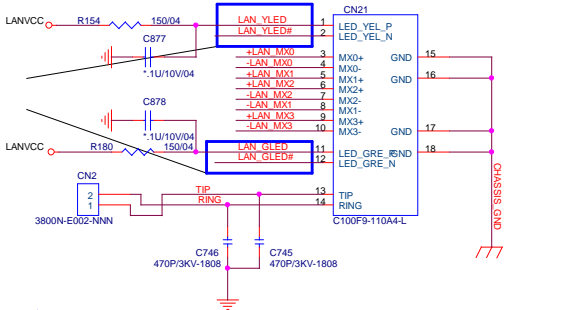
BLOCK A is only for RTL8101E application.



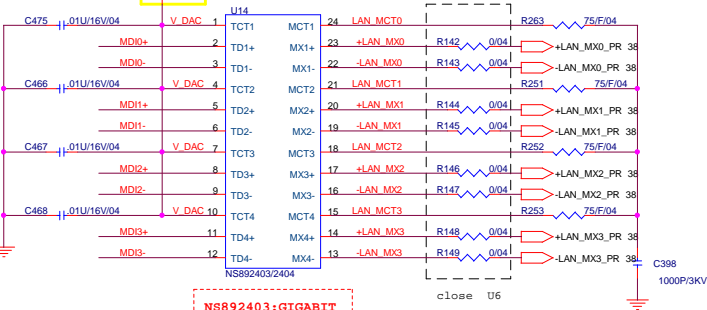
Remove R70 for 8111B and 8111C



RJ45



SI-1 modified to fix giga LAN LED issue

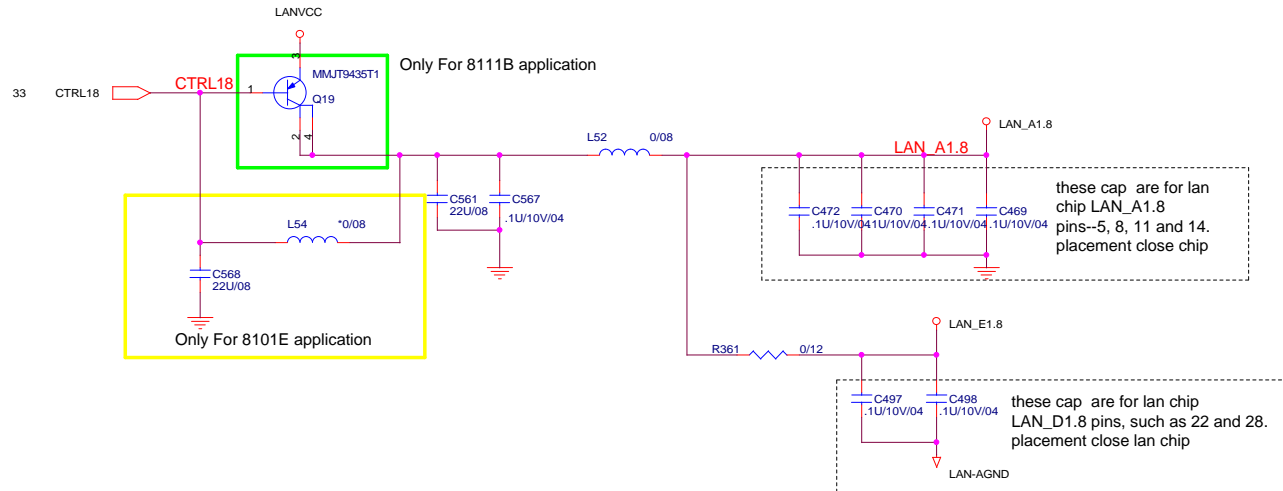
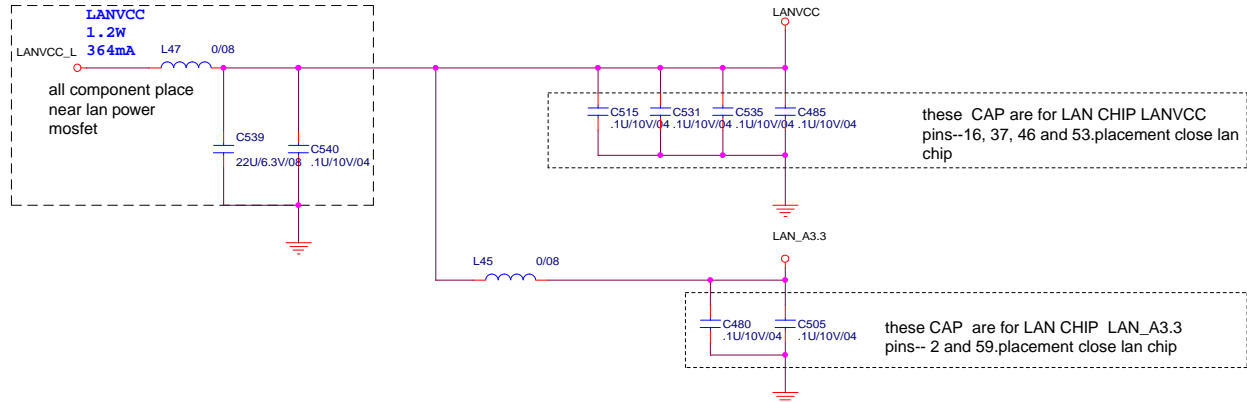


NS892403:GIGABIT NS892405:10/100

	PROJECT : AT5	
	Quanta Computer Inc.	
Size Custom	Document Number	Rev 1A
RTL8111B/8111C/8101E		
Date: Monday, March 19, 2007	Sheet 33 of 48	

T : Stuffed for RTL8111B(10/100/1000)

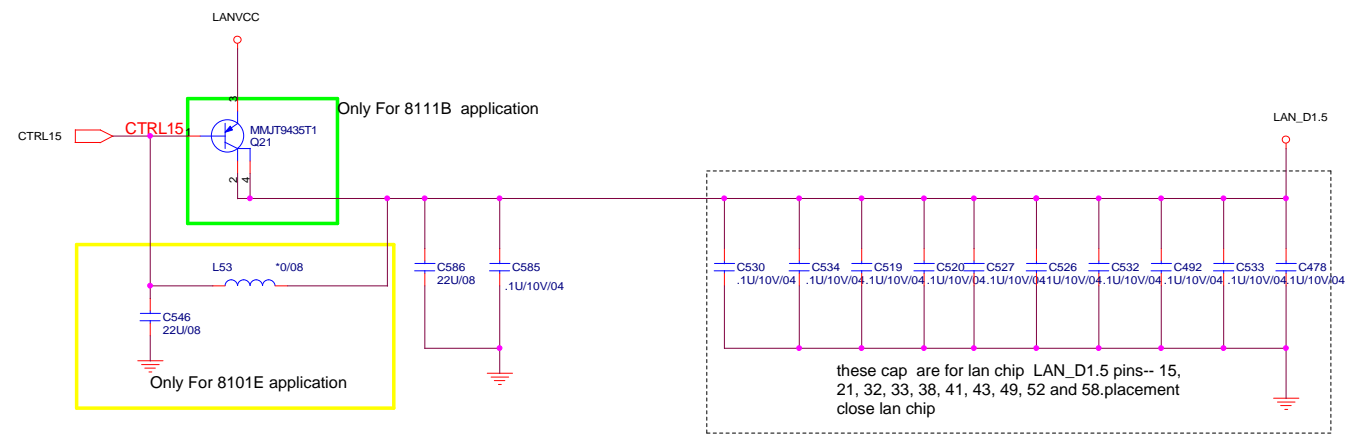
E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B/ RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

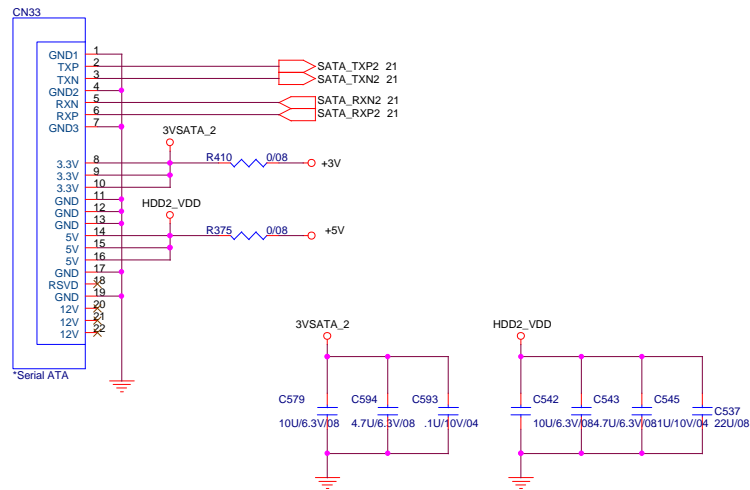
	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A



PROJECT : AT5
Quanta Computer Inc.

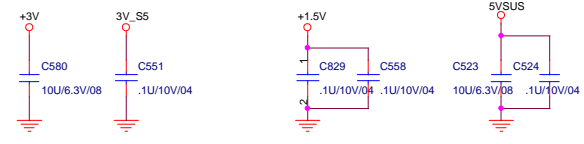
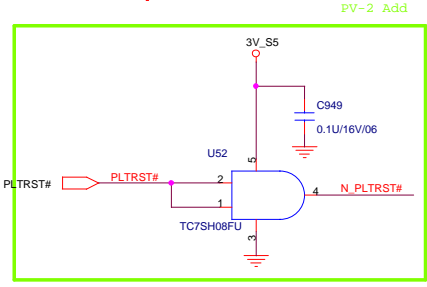
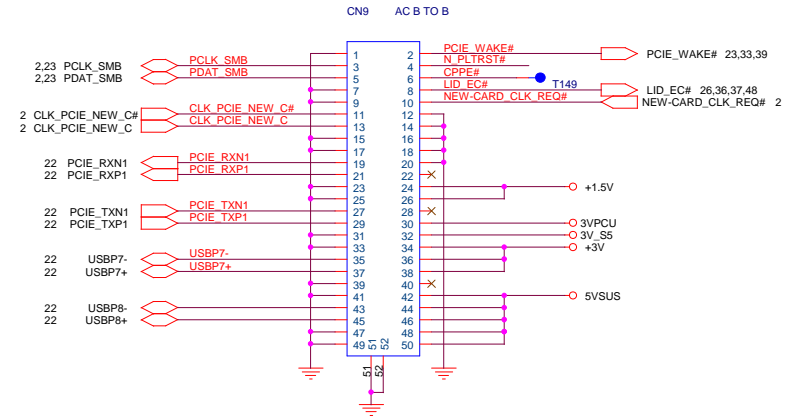
Size A3	Document Number LAN POWER	Rev 1A
Date: Monday, March 19, 2007		
Sheet 34 of 48		

SATA_2 CONNECTOR For 17"W Second HDD

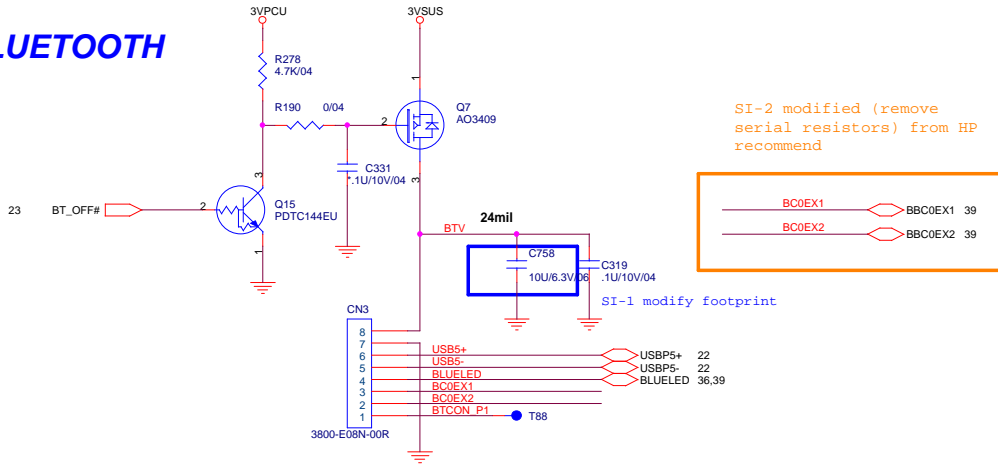


NEWCARD

35

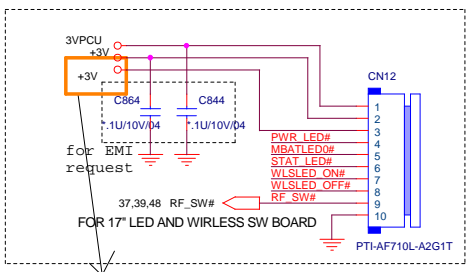


BLUETOOTH

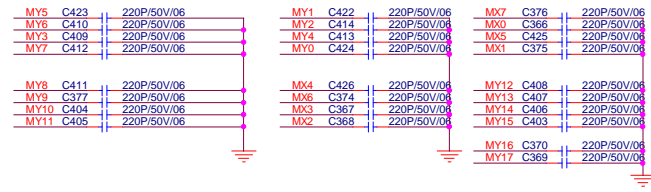
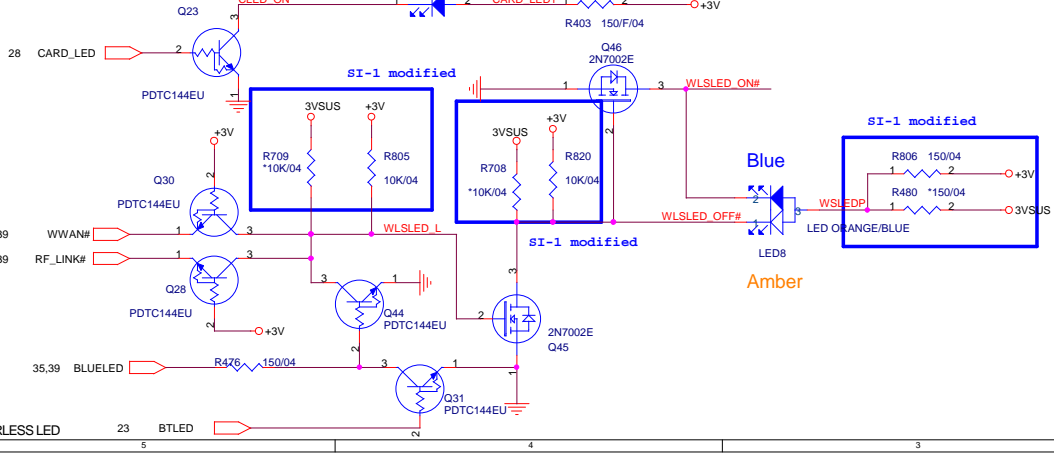
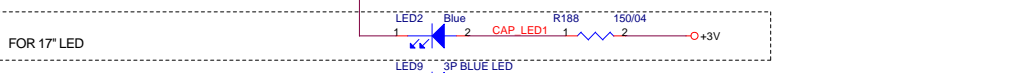
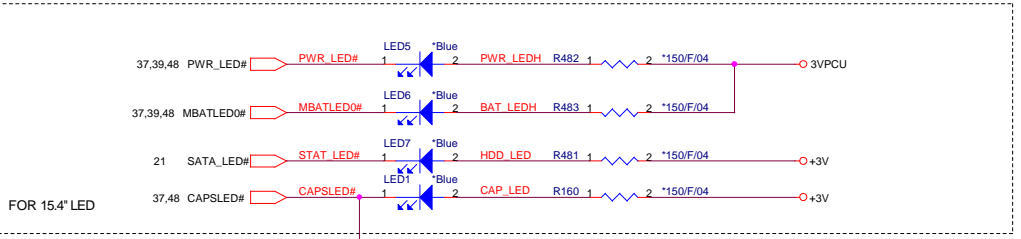
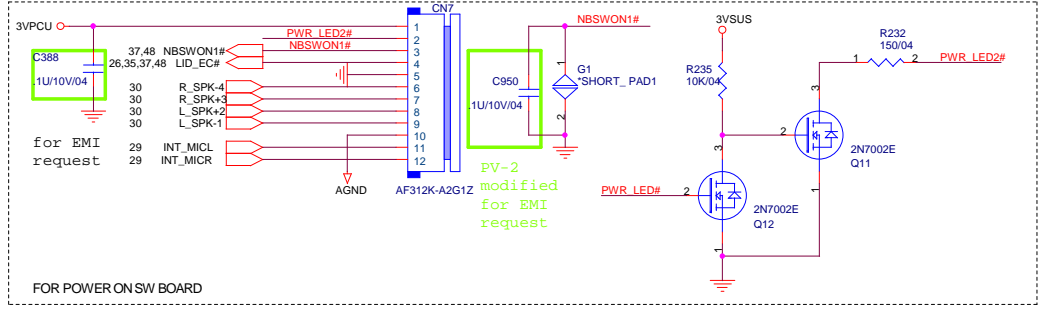
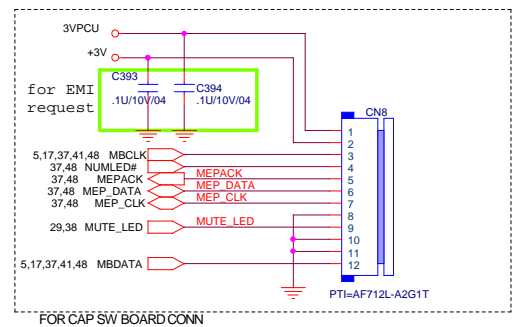


PROJECT : AT5
Quanta Computer Inc.

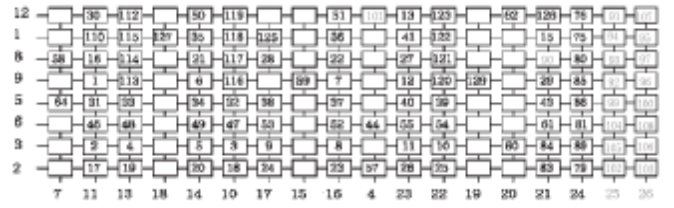
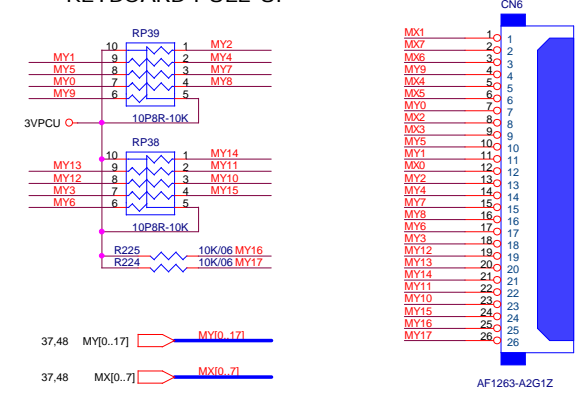
Size Custom	Document Number NEW CARD/BT	Rev 1A
Date: Monday, March 19, 2007 Sheet 35 of 48		



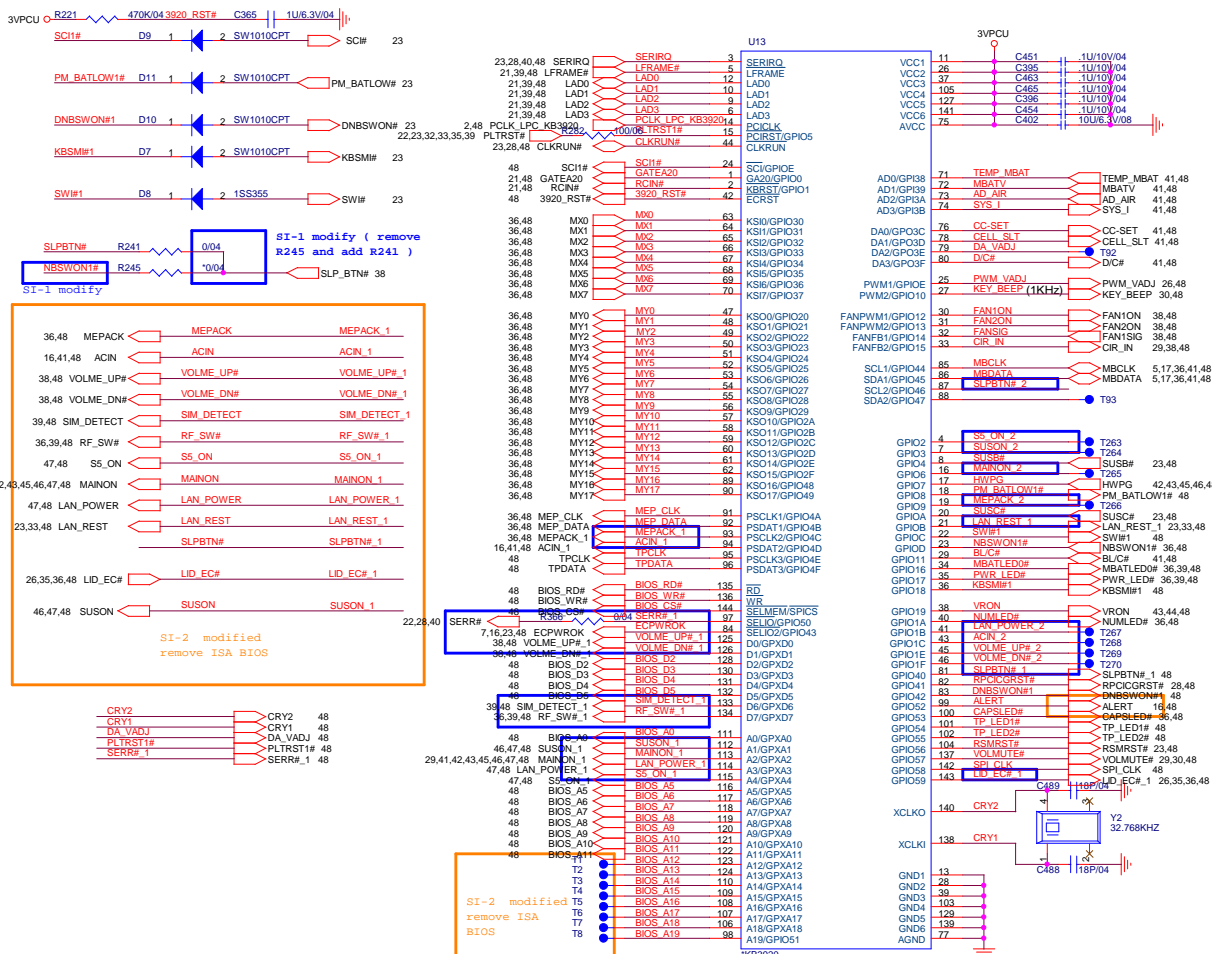
SI-2 modified for fix s3 not support wireless LED



KEYBOARD PULL-UP

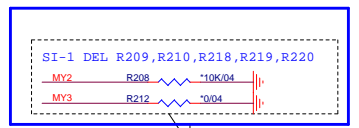


		PROJECT : AT5 Quanta Computer Inc.	
		Size Custom	Document Number LED/KEYBOARD/SW
NB5/RD1/HW2		Date: Monday, March 19, 2007	Sheet 36 of 48



STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



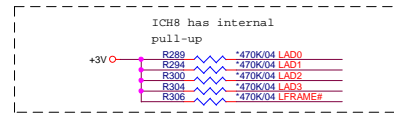
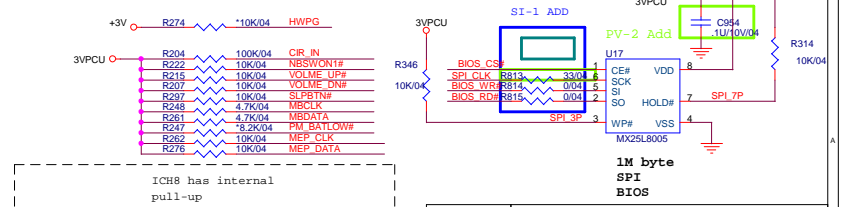
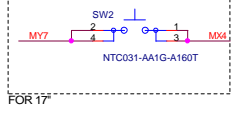
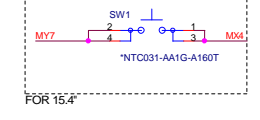
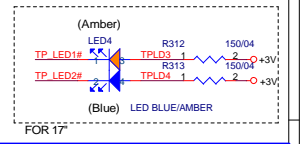
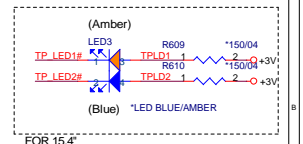
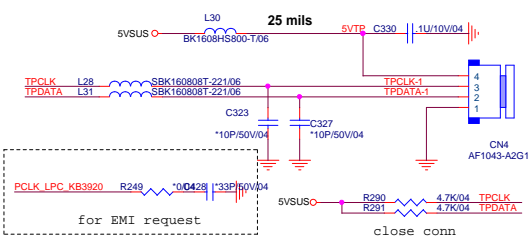
All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

SELECT KBC TPE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified
remove ISA BIOS

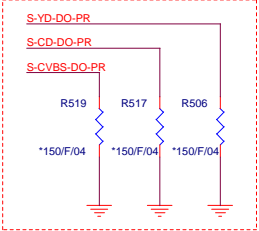
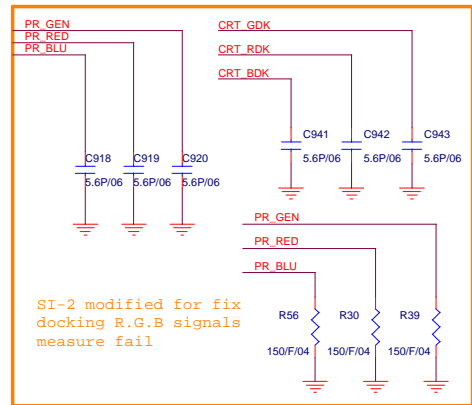
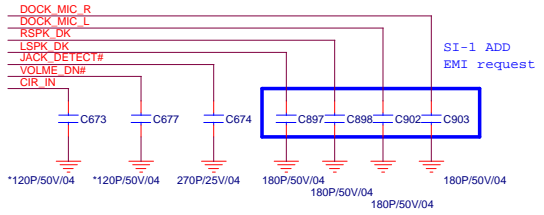
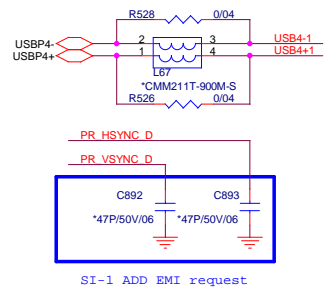
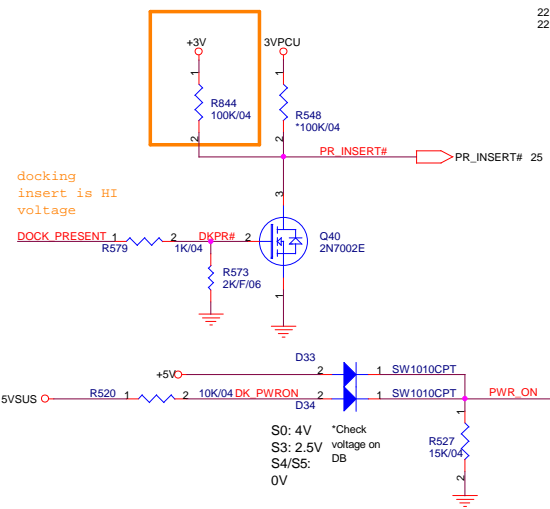
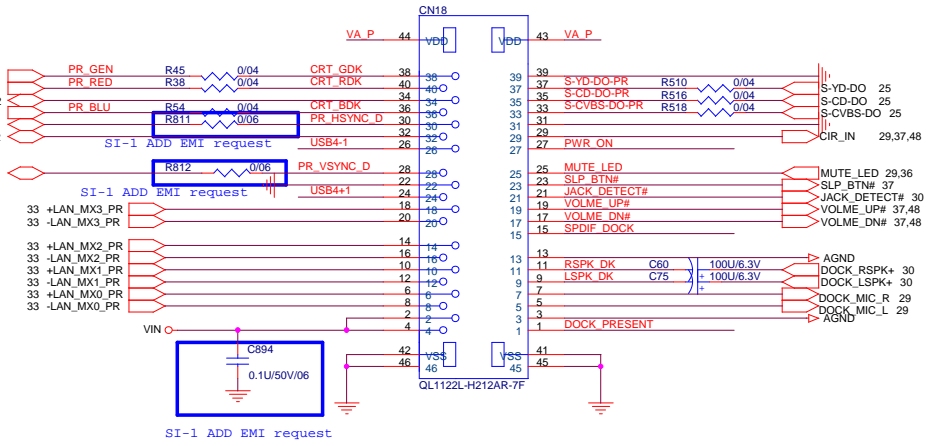
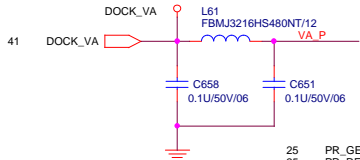
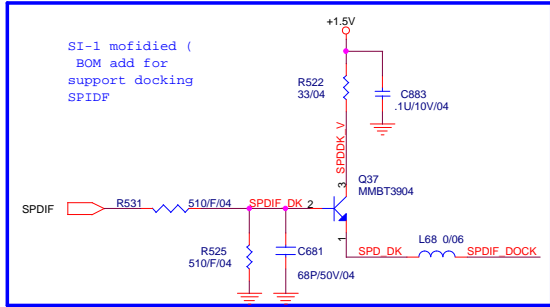
TOUCH PAD CONNECTOR



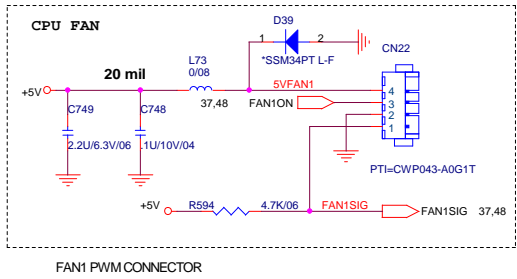
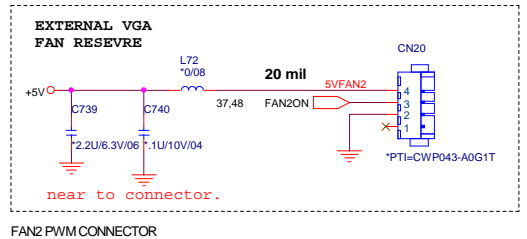
PROJECT : AT5
Quanta Computer Inc.

Size Custom	Document Number KB3920/ROM/TP	Rev 1A
Date: Monday, March 19, 2007		Sheet 37 of 48

support 6A 200mils
CX000480005

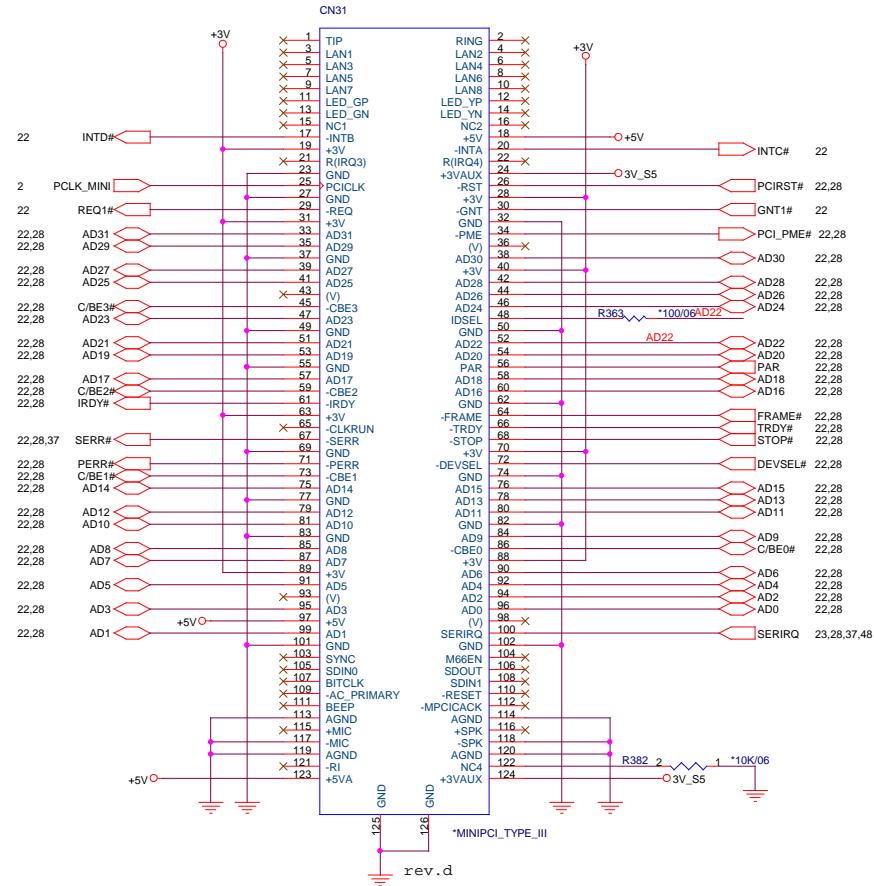


FAN

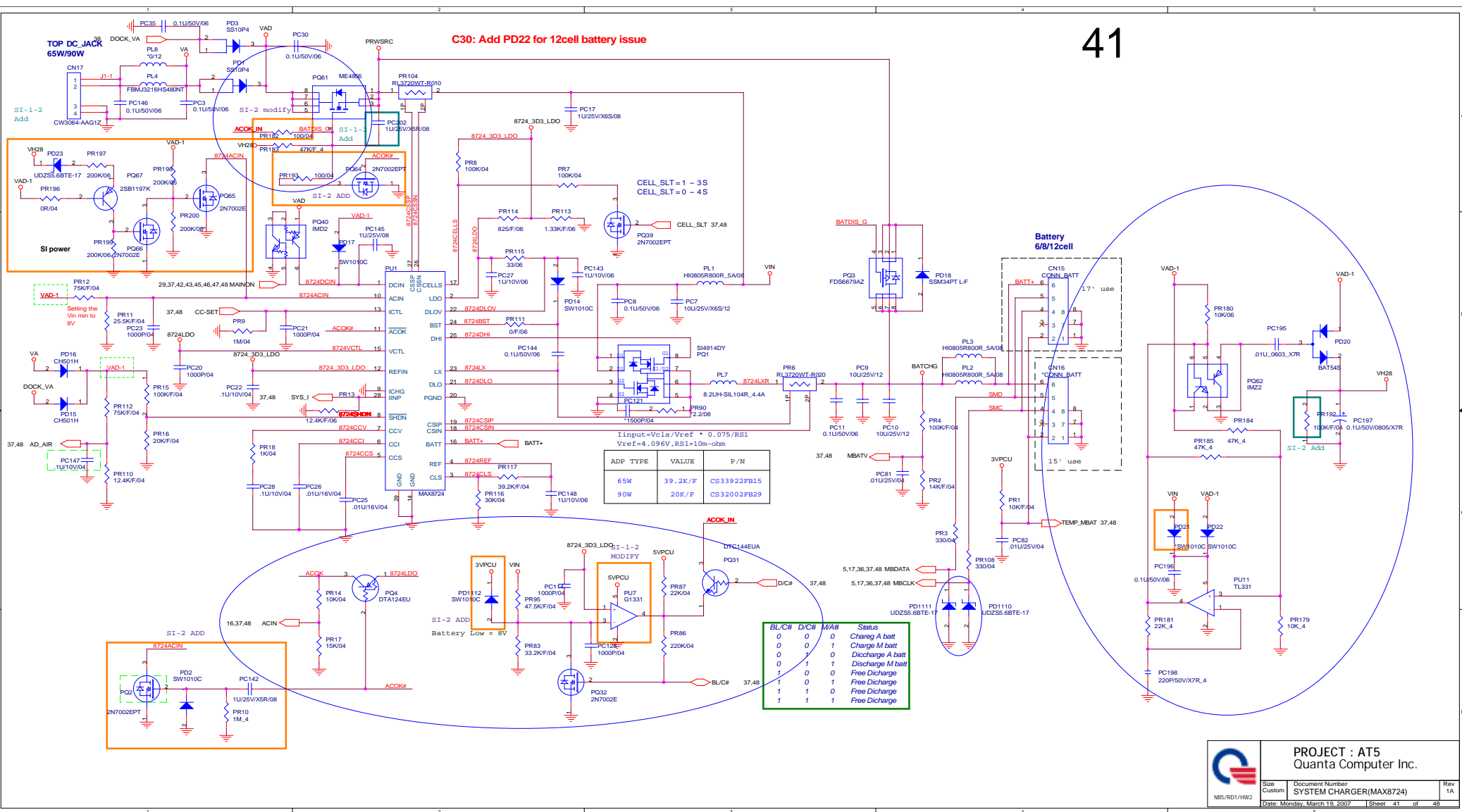


MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22

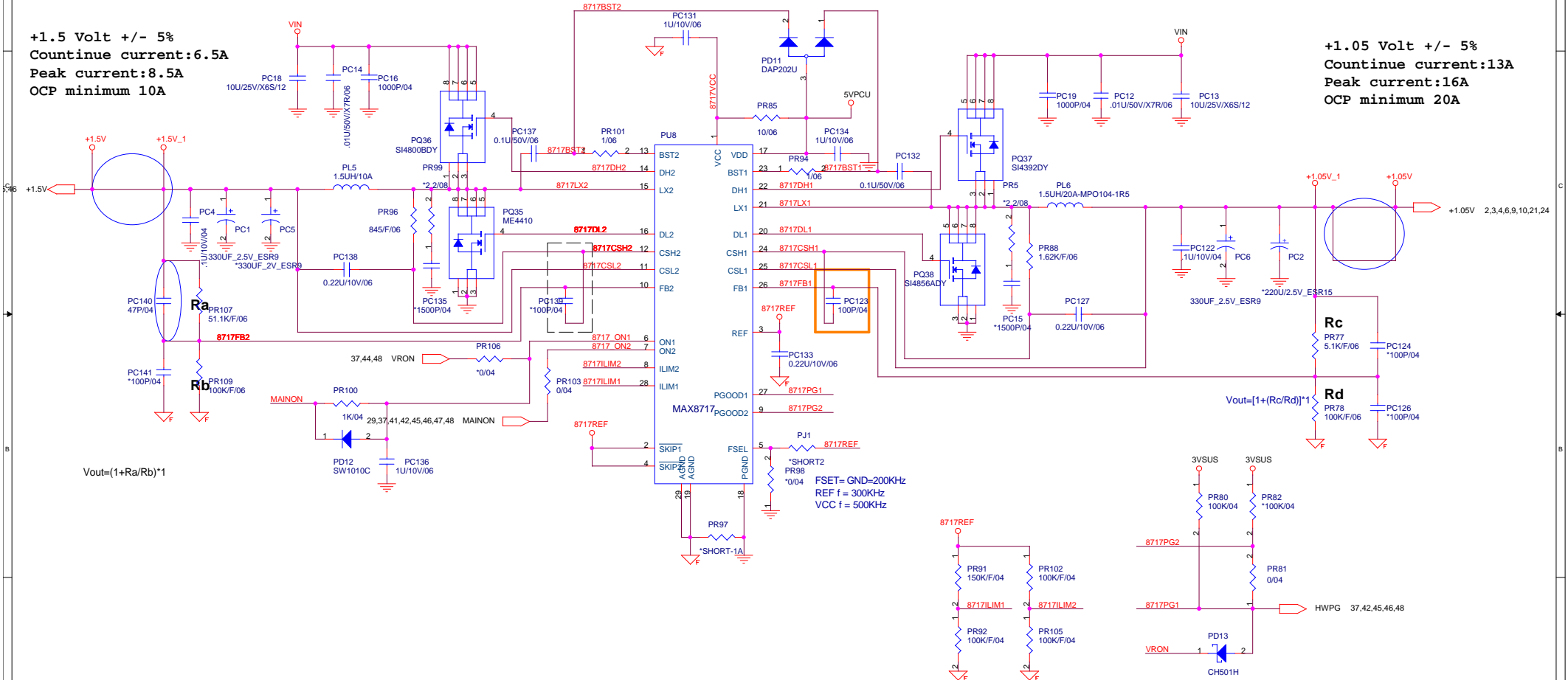


C30: Add PD22 for 12cell battery issue




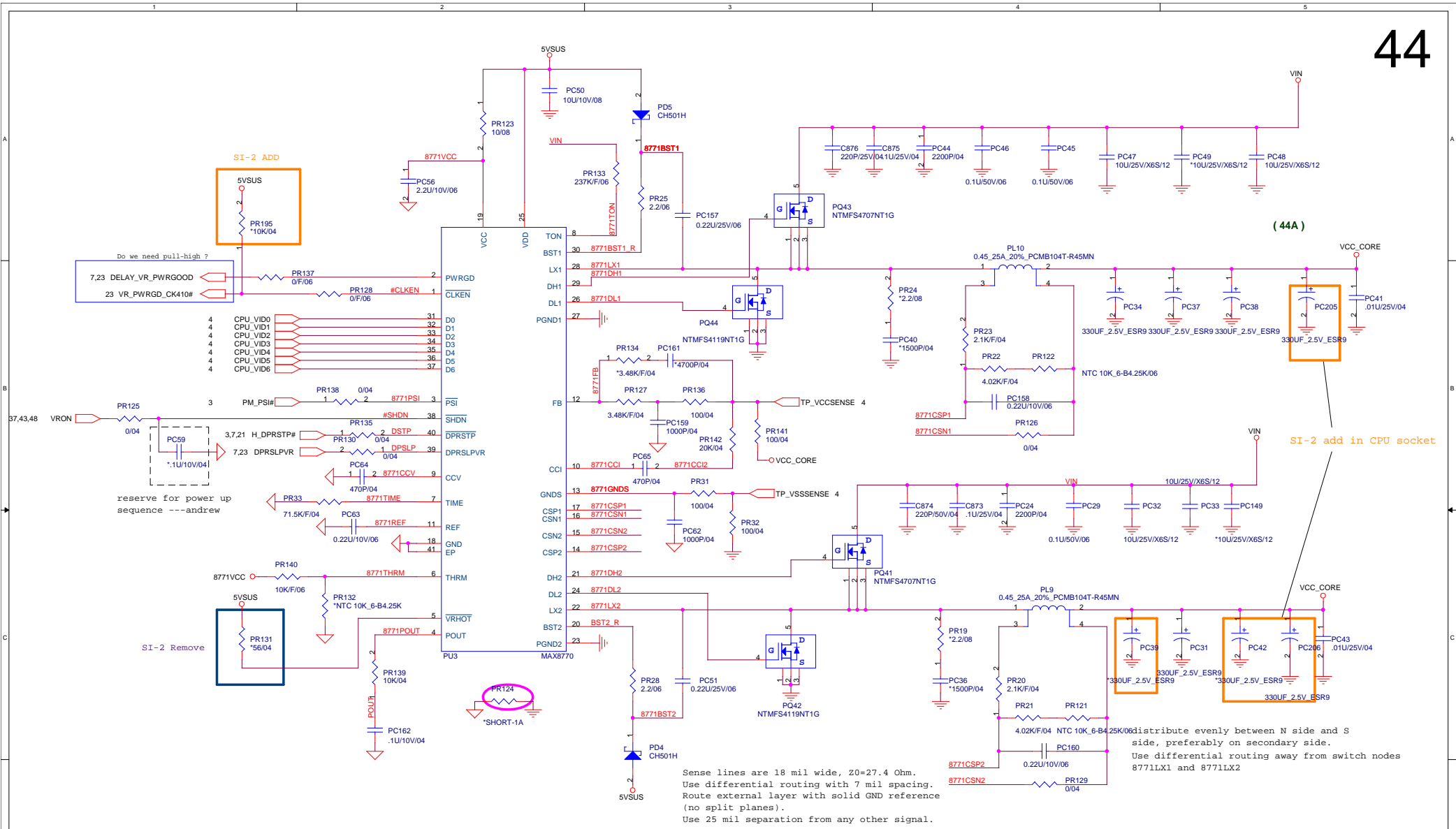
+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



$$V_{out} = (1 + R_a/R_b) * 1$$

 NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.		
	Size Custom	Document Number +1.5V & VCCP+1.05V(MAX8743)	Rev 1A
	Date: Monday, March 19, 2007		Sheet 43 of 48




(44A)

SI-2 add in CPU socket

distribute evenly between N side and S side, preferably on secondary side. Use differential routing away from switch nodes 8771LX1 and 8771LX2

Sense lines are 18 mil wide, Z0=27.4 Ohm. Use differential routing with 7 mil spacing. Route external layer with solid GND reference (no split planes). Use 25 mil separation from any other signal.

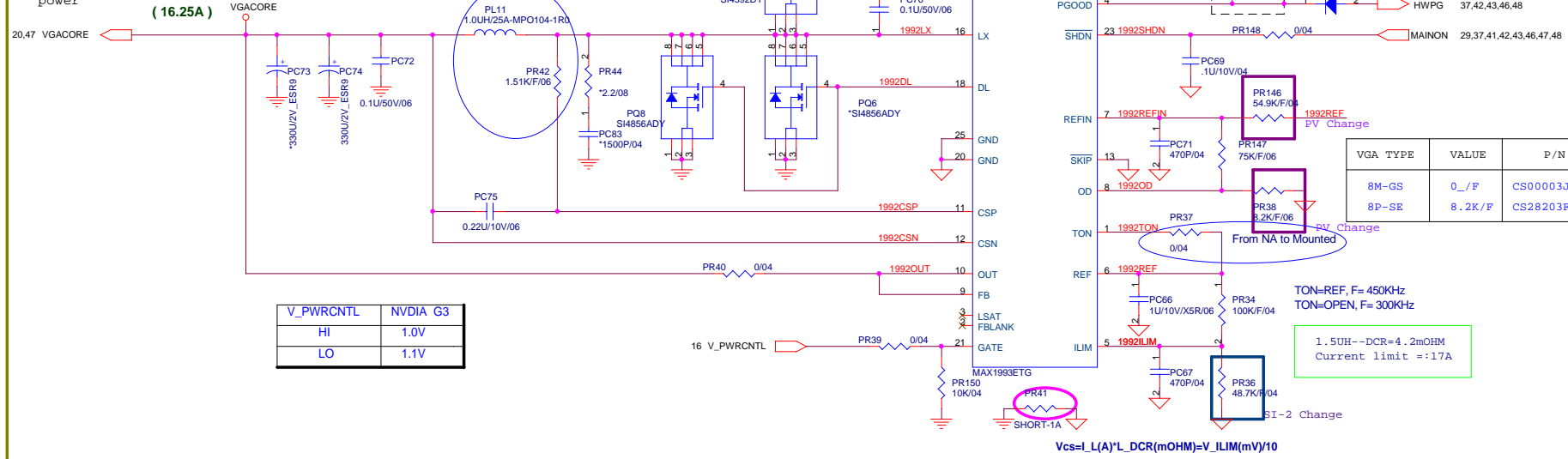
Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

		PROJECT : AT5 Quanta Computer Inc.	
		Size Custom Document Number CPU_CORE(MAX8771) Date: Monday, March 19, 2007	Rev 1A Sheet 44 of 48

For Discrete Only

1.1 Volt +/- 5%
 Countinue current:11A
 Peak current:13.5A
 OCP minimum 17A

to external
 VGA core
 power



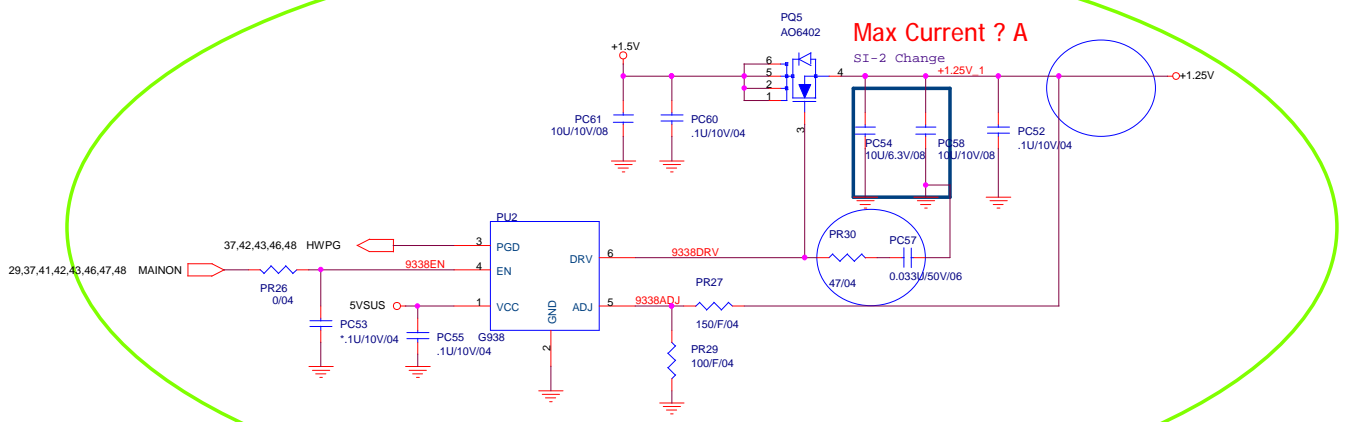
V_PWRCNTL	NVIDIA G3
HI	1.0V
LO	1.1V

VGA TYPE	VALUE	P/N
8M-GS	0_/F	CS00003J951
8P-SE	8.2K/F	CS28203P919

TON=REF, F= 450KHz
 TON=OPEN, F= 300KHz
 1.5UH--DCR=4.2mOHM
 Current limit =:17A

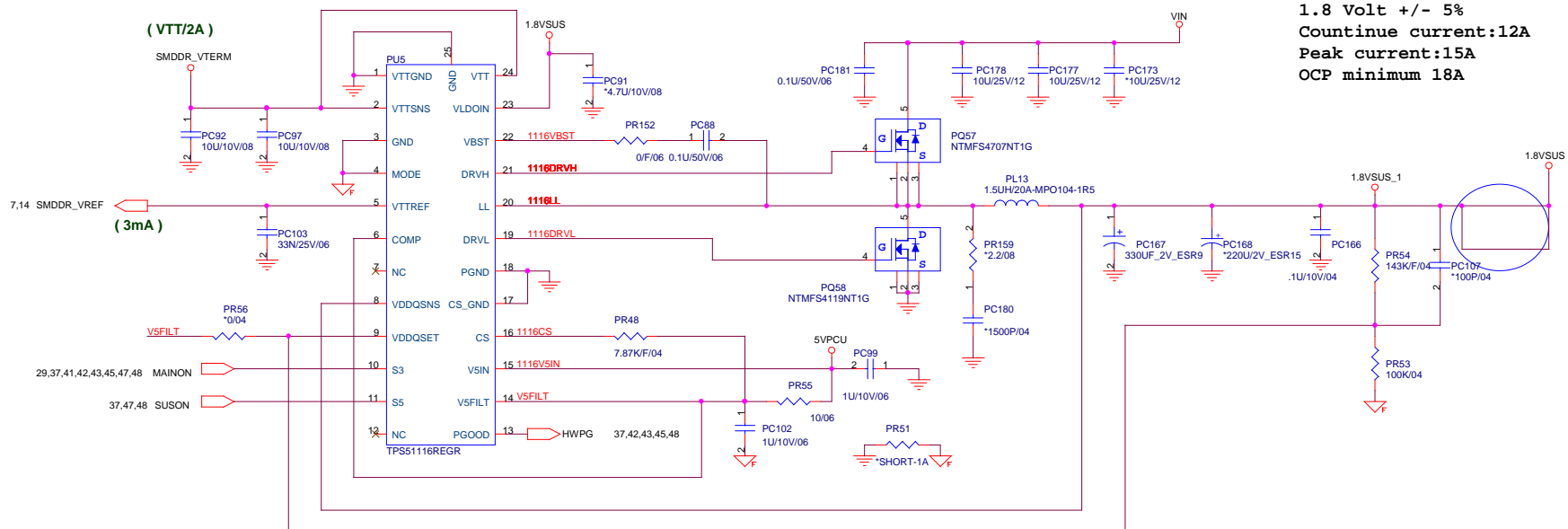
$V_{cs} = L(A) * L_DCR(mOHM) = V_ILIM(mV) / 10$

Max Current ? A

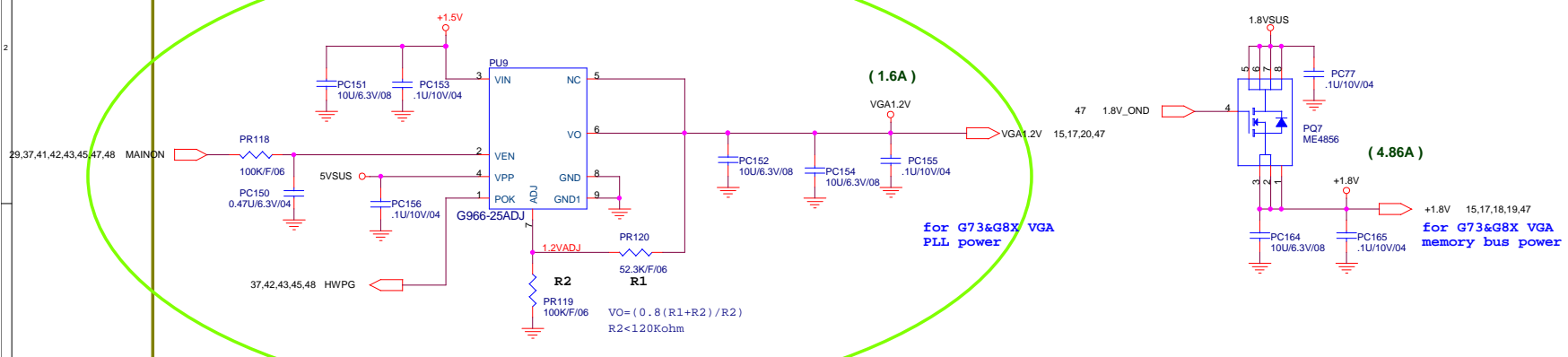


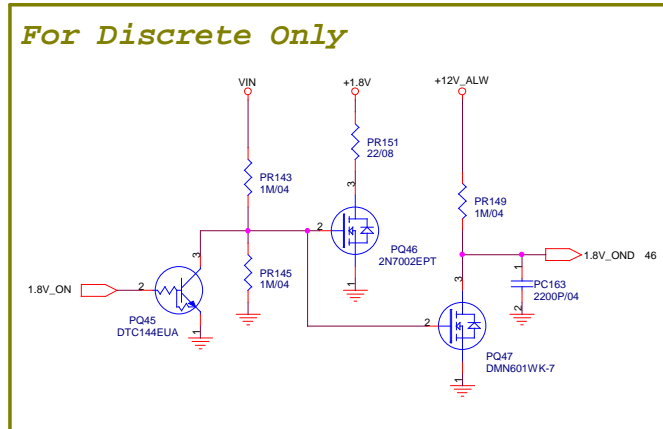
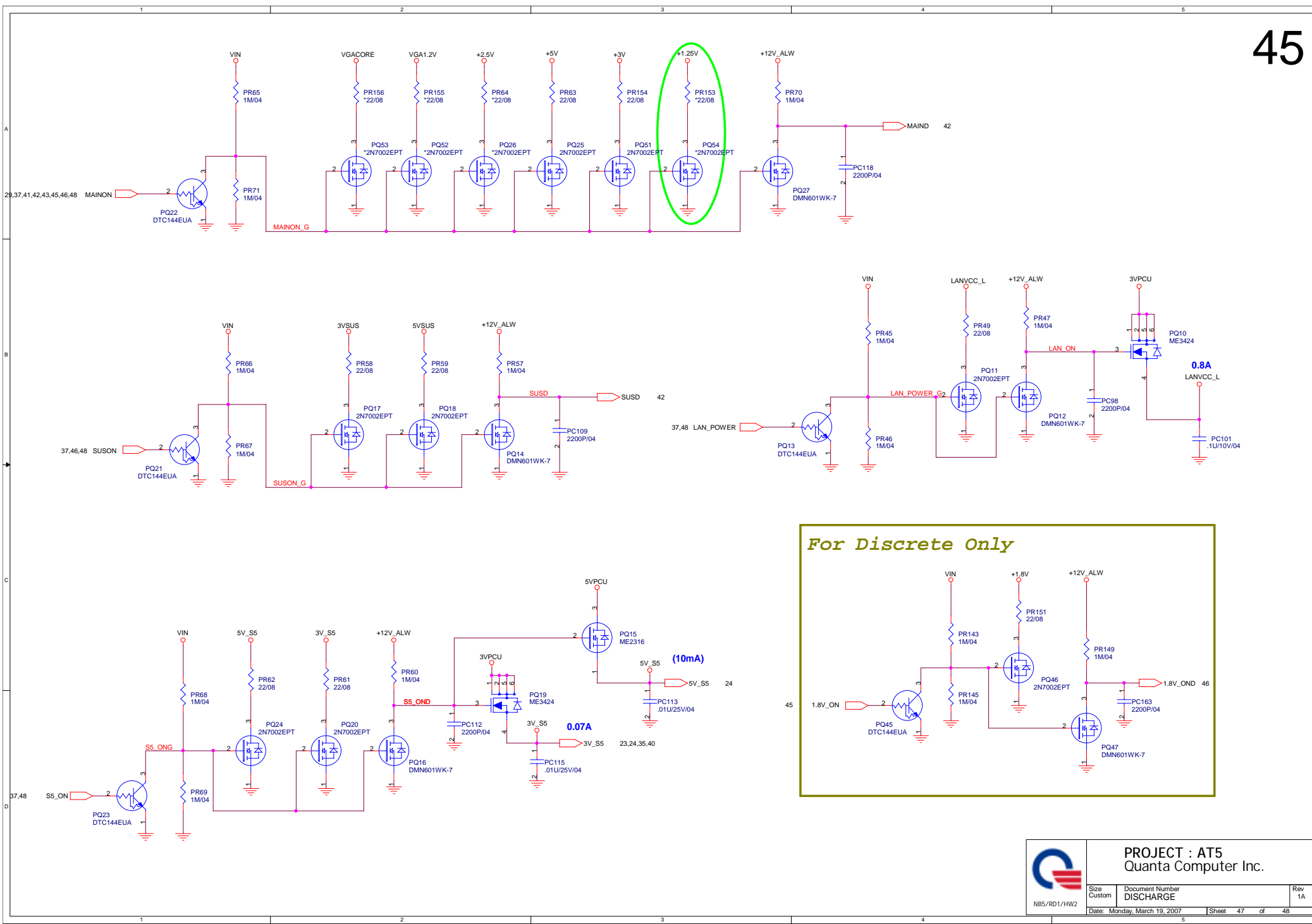
$V_{out1} = (1 + R1/R2) * 0.5$

	PROJECT : AT5 VGACORE (MAX1993)	
	Size Custom	Document Number VGACORE (MAX1993)
	Date: Monday, March 19, 2007	Sheet 45 of 48

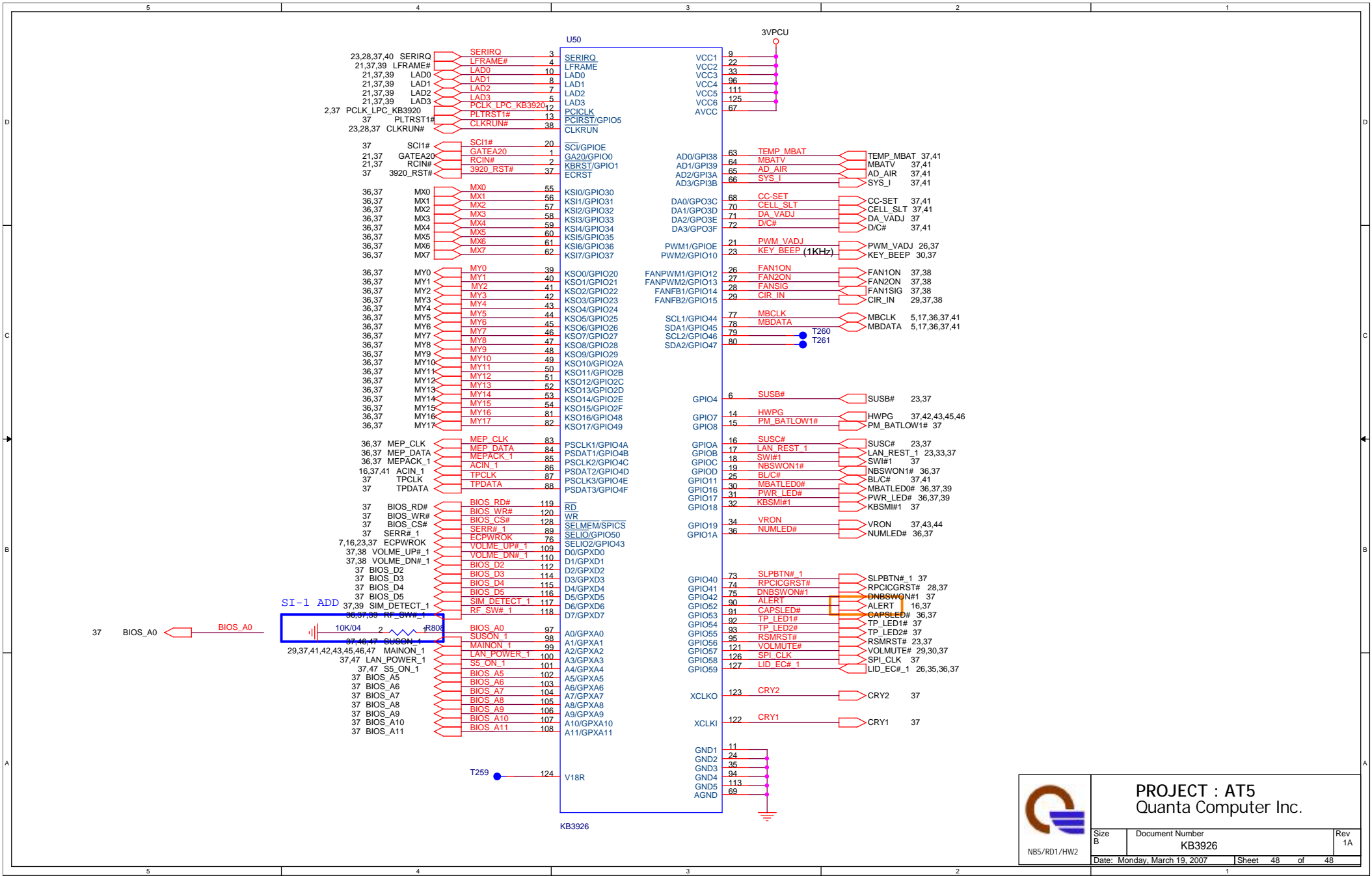


For Discrete Only





	PROJECT : AT5 Quanta Computer Inc.	
	Size Custom	Document Number DISCHARGE
	Date: Monday, March 19, 2007	Sheet 47 of 48



PROJECT : AT5
Quanta Computer Inc.

Size B	Document Number KB3926	Rev 1A
Date: Monday, March 19, 2007 Sheet 48 of 48		

www.s-manuals.com