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**Project Code & Schematics Subject:** M850 Main Board 8L

<b>PCB P/N:</b>	1P-0094J00-8011(IRIS) 1P-0094500-8011(HANNSTAR)
<b>A+U/B P/N:</b>	1P-1094J01-8011(IRIS) 1P-1094501-8011(HANNSTAR)
<b>P/B P/N:</b>	1P-1094J00-8011(IRIS) 1P-1094500-8011(HANNSTAR)

P. Leader	Check by	Design by
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>Index Page</b>		
Size Custom	Document Number M850-1-01	Rev 1.0
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7 H\_A#[3..35]

7 H\_ADSTB#0  
7 H\_REQ#[4..0]

7 H\_ADSTB#1

28 H\_A20M#

28 H\_FERR#

28 H\_IGNNE#

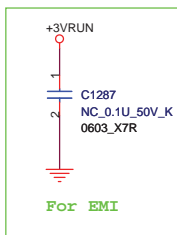
28 H\_STPCLK#

28 H\_INTR#

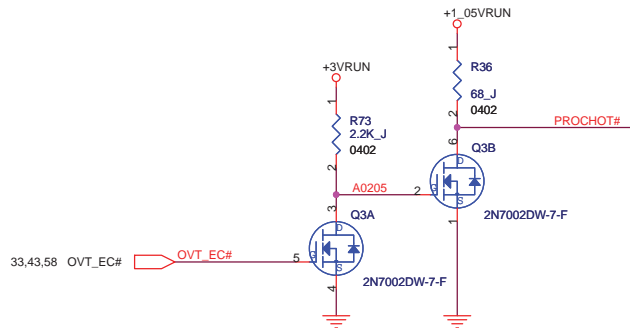
28 H\_NMI#

28 H\_SM#

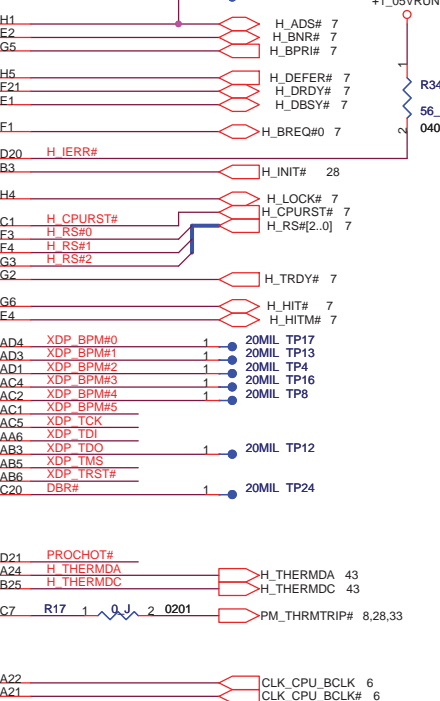
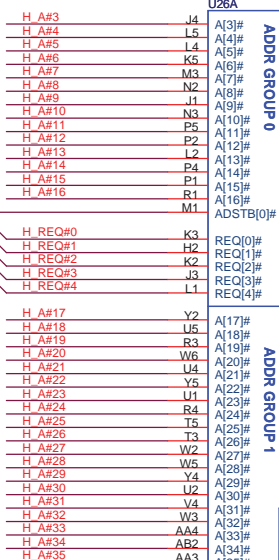
- TP15 20MIL -1 TP CPU RSVD01 M4
- TP18 20MIL -1 TP CPU RSVD02 N5
- TP7 20MIL -1 TP CPU RSVD03 T2
- TP11 20MIL -1 TP CPU RSVD04 V3
- TP5 20MIL -1 TP CPU RSVD05 B2
- TP14 20MIL -1 CPU TEST7 C3
- TP6 20MIL -1 TP CPU RSVD07 D2
- TP25 20MIL -1 TP CPU RSVD08 D22
- TP10 20MIL -1 TP CPU RSVD09 D3
- TP19 20MIL -1 TP CPU RSVD10 F6



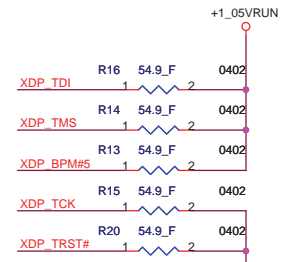
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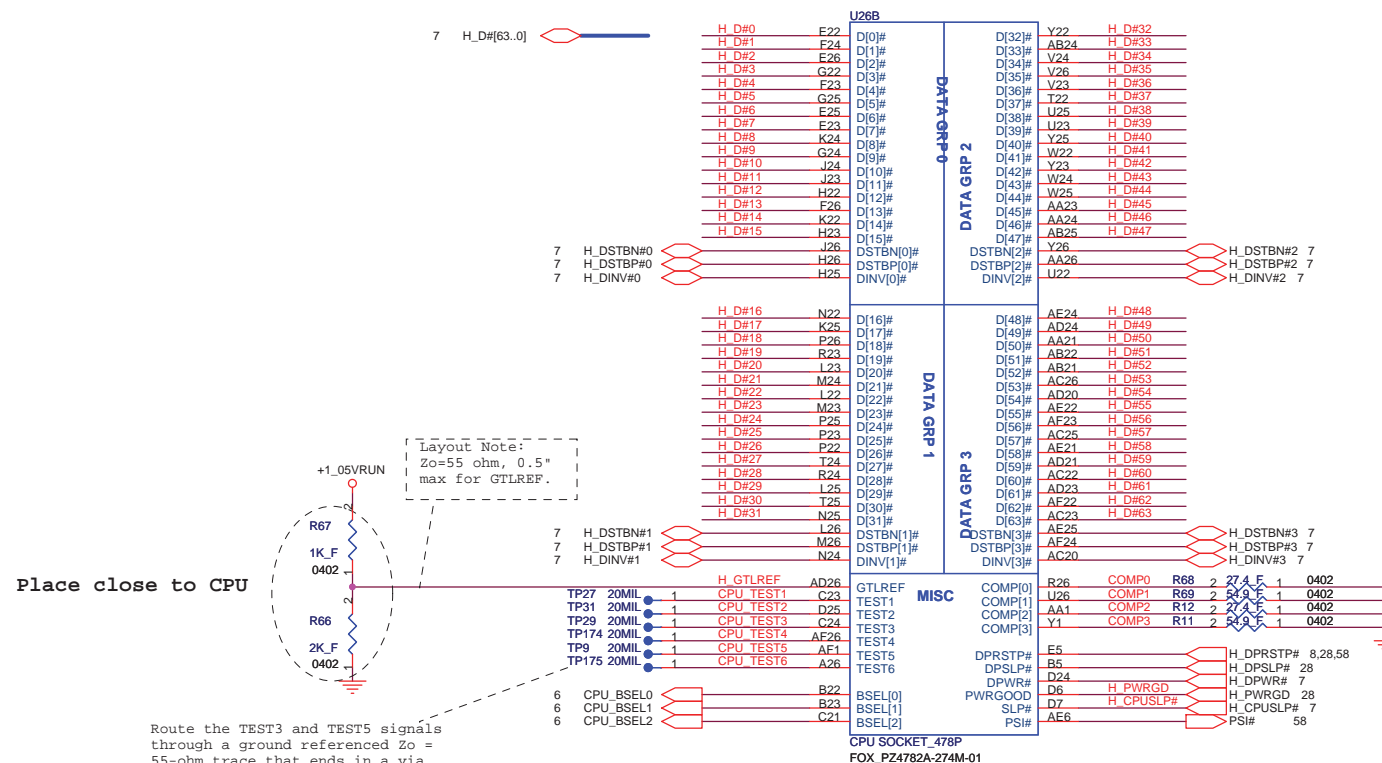


CPU SOCKET\_478P  
FOX\_PZ4782A-274M-01



H\_CPURST# 1 20MIL TP2

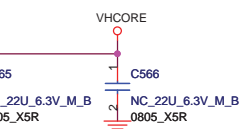
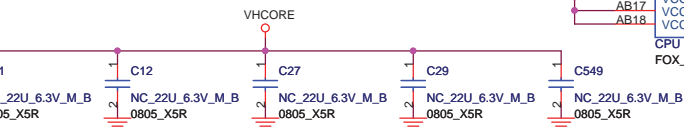
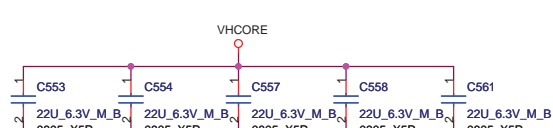
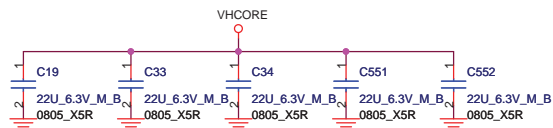
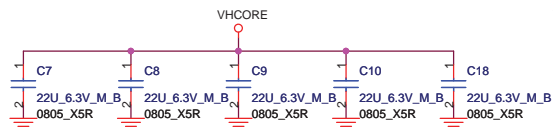




Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=18mil(MS)  
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

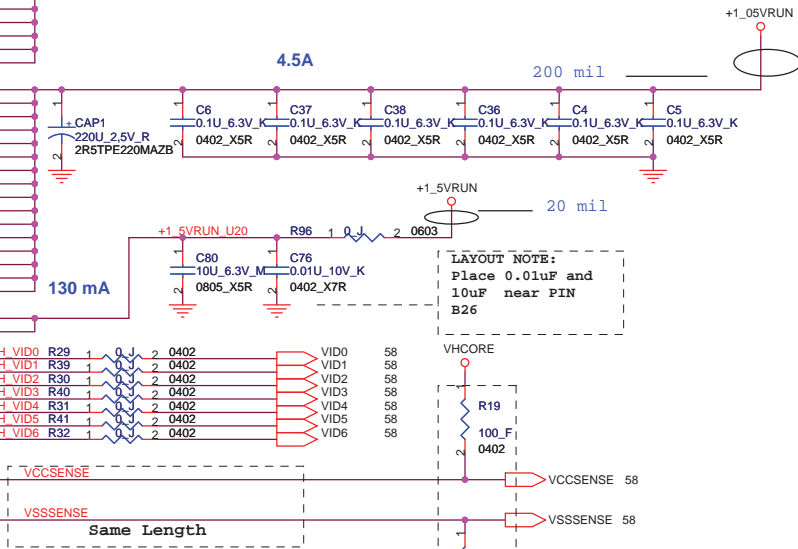
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U26C	VCC	VCC	AB
A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	B13
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AE9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
F10	VCC[035]	VCCP[01]	G21
F12	VCC[036]	VCCP[02]	J6
F13	VCC[037]	VCCP[03]	K6
F15	VCC[038]	VCCP[04]	IM6
F17	VCC[039]	VCCP[05]	J21
F18	VCC[040]	VCCP[06]	K21
F20	VCC[041]	VCCP[07]	M21
F7	VCC[042]	VCCP[08]	N21
F9	VCC[043]	VCCP[09]	R6
F10	VCC[044]	VCCP[10]	T21
F12	VCC[045]	VCCP[11]	T6
F13	VCC[046]	VCCP[12]	V21
F15	VCC[047]	VCCP[13]	W21
F17	VCC[048]	VCCP[14]	
F18	VCC[049]	VCCP[15]	
F20	VCC[050]	VCCP[16]	
AA7	VCC[051]	VCCA[01]	B26
AA9	VCC[052]	VCCA[02]	C26
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]		
AA15	VCC[056]		
AA17	VCC[057]		
AA18	VCC[058]		
AA20	VCC[059]		
AB9	VCC[060]		
AC10	VCC[061]		
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]		

CPU\_VCCA---->0.13A  
 CPU\_VCCP---->4.5A  
 CPU\_VCC---->47A

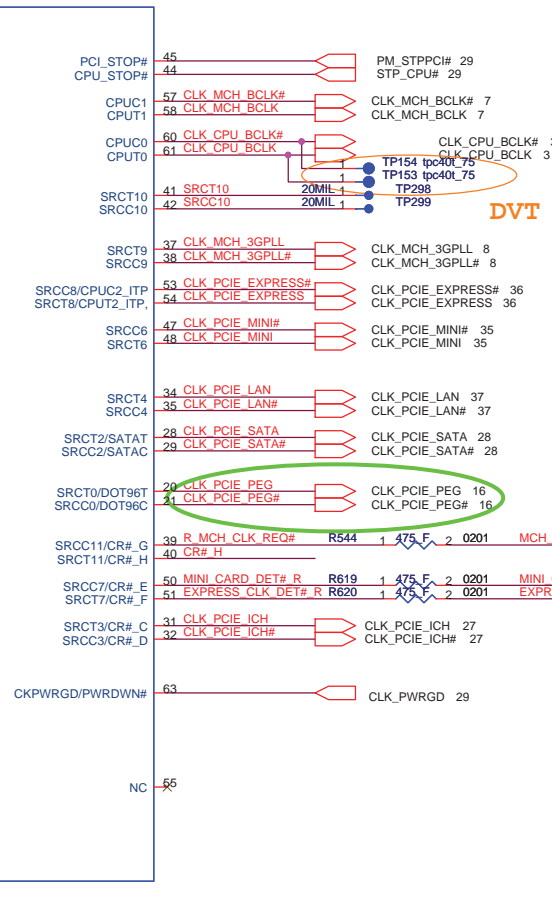
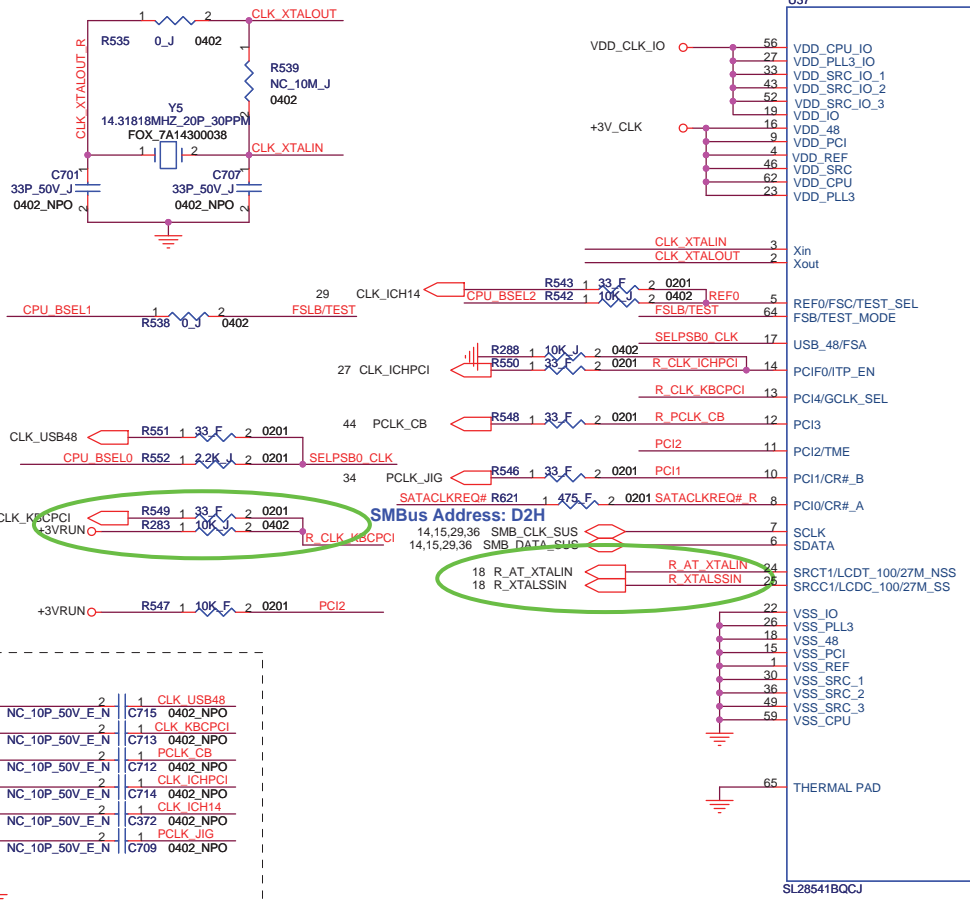
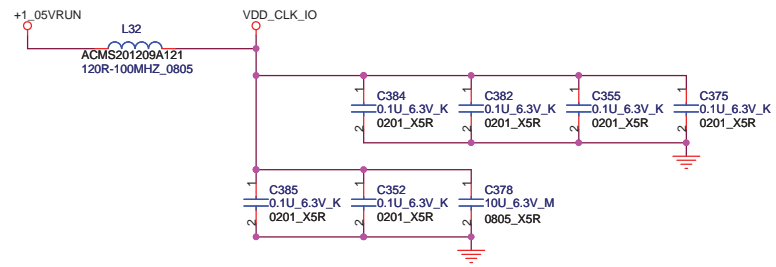
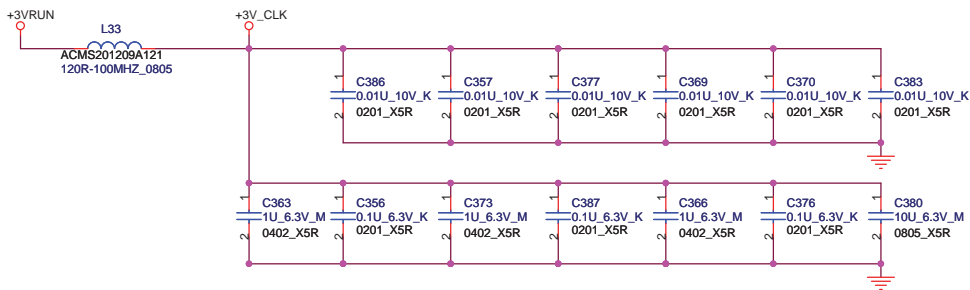
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Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 1 inch of CPU.

Outer width=18 mil spacing=7 mil  
 Inner width=14 mil spacing=7 mil  
 Length match < 25 mil

U26D	VSS	VSS	P
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C14	VSS[019]	VSS[100]	W1
C16	VSS[020]	VSS[101]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	V3
C25	VSS[025]	VSS[106]	V6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[033]	VSS[114]	AA11
D19	VSS[034]	VSS[115]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[035]	VSS[116]	AA19
E3	VSS[036]	VSS[117]	AA22
E6	VSS[037]	VSS[118]	AA25
E8	VSS[038]	VSS[119]	AB1
E11	VSS[039]	VSS[120]	AB4
E14	VSS[040]	VSS[121]	AB8
E16	VSS[041]	VSS[122]	AB11
E19	VSS[042]	VSS[123]	AB13
E21	VSS[043]	VSS[124]	AB16
E24	VSS[044]	VSS[125]	AB19
F5	VSS[045]	VSS[126]	AB23
F8	VSS[046]	VSS[127]	AB26
F11	VSS[047]	VSS[128]	AC3
F13	VSS[048]	VSS[129]	AC6
F16	VSS[049]	VSS[130]	AC8
F19	VSS[050]	VSS[131]	AC11
F2	VSS[051]	VSS[132]	AC14
F22	VSS[052]	VSS[133]	AC16
F25	VSS[053]	VSS[134]	AC19
G4	VSS[054]	VSS[135]	AC21
G1	VSS[055]	VSS[136]	AC24
G23	VSS[056]	VSS[137]	AD2
G26	VSS[057]	VSS[138]	AD5
H3	VSS[058]	VSS[139]	AD8
H6	VSS[059]	VSS[140]	AD11
H21	VSS[060]	VSS[141]	AD13
H24	VSS[061]	VSS[142]	AD16
J2	VSS[062]	VSS[143]	AD19
J5	VSS[063]	VSS[144]	AD22
J22	VSS[064]	VSS[145]	AD25
J25	VSS[065]	VSS[146]	AE1
K1	VSS[066]	VSS[147]	AE4
K4	VSS[067]	VSS[148]	AE8
K23	VSS[068]	VSS[149]	AE11
K26	VSS[069]	VSS[150]	AE14
L3	VSS[070]	VSS[151]	AE16
L6	VSS[071]	VSS[152]	AE19
L21	VSS[072]	VSS[153]	AE23
L24	VSS[073]	VSS[154]	AE26
M2	VSS[074]	VSS[155]	A2
M5	VSS[075]	VSS[156]	AF6
M22	VSS[076]	VSS[157]	AF8
M25	VSS[077]	VSS[158]	AF11
N1	VSS[078]	VSS[159]	AF13
N4	VSS[079]	VSS[160]	AF16
N23	VSS[080]	VSS[161]	AF19
N26	VSS[081]	VSS[162]	AF21
P3	VSS[082]	VSS[163]	A25
			AF25



Clock Request	Clock Request Function
CR#A	SATACLKREQ#
CR#B	NC
CR#C	NC
CR#D	NC
CR#E	MINI_CARD_DET#
CR#F	EXPRESS_CLK_DET#
CR#G	MCH_CLK_REQ#
CR#H	NC

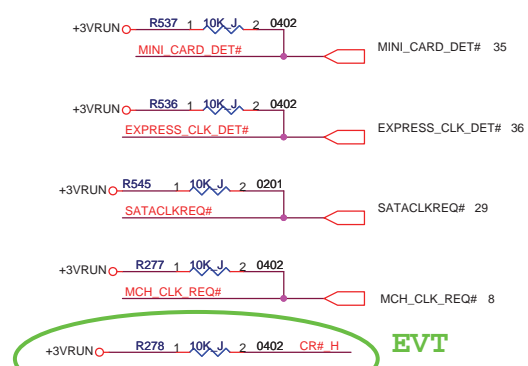
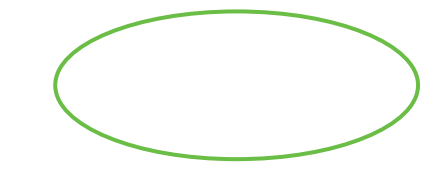
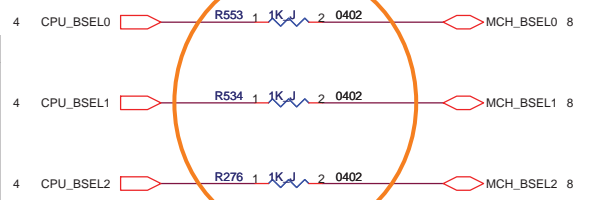
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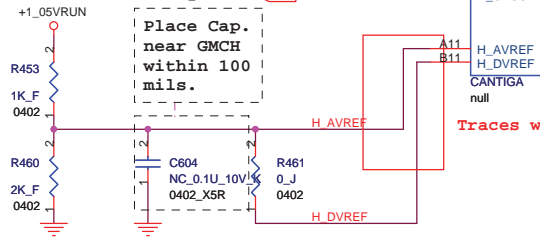
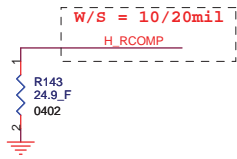
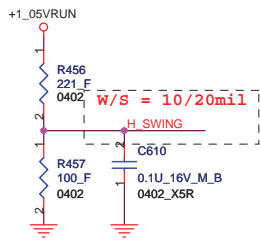
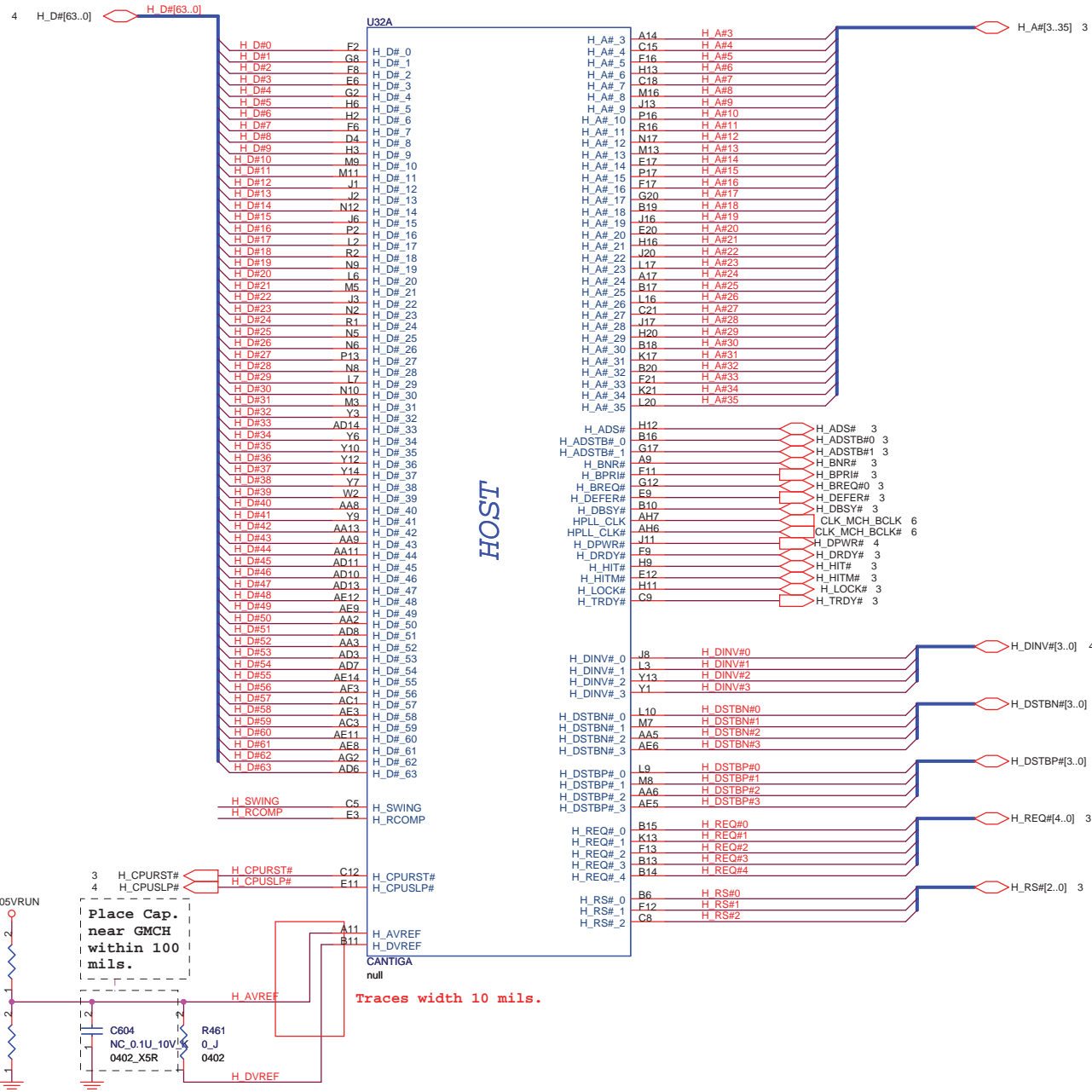
close to clk gen (For EMI)

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**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33







MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low = The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation (default)
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

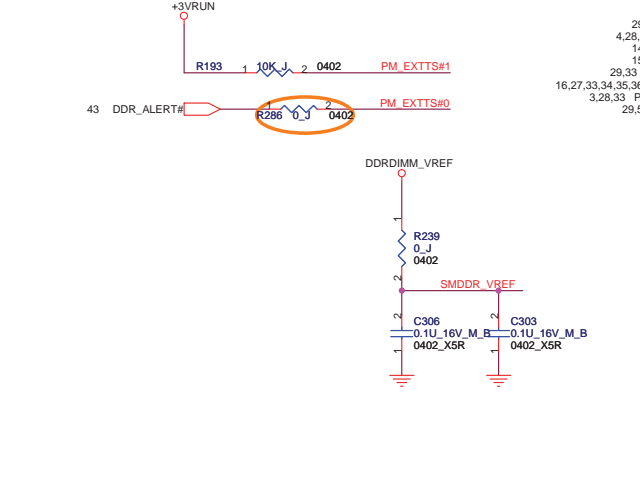
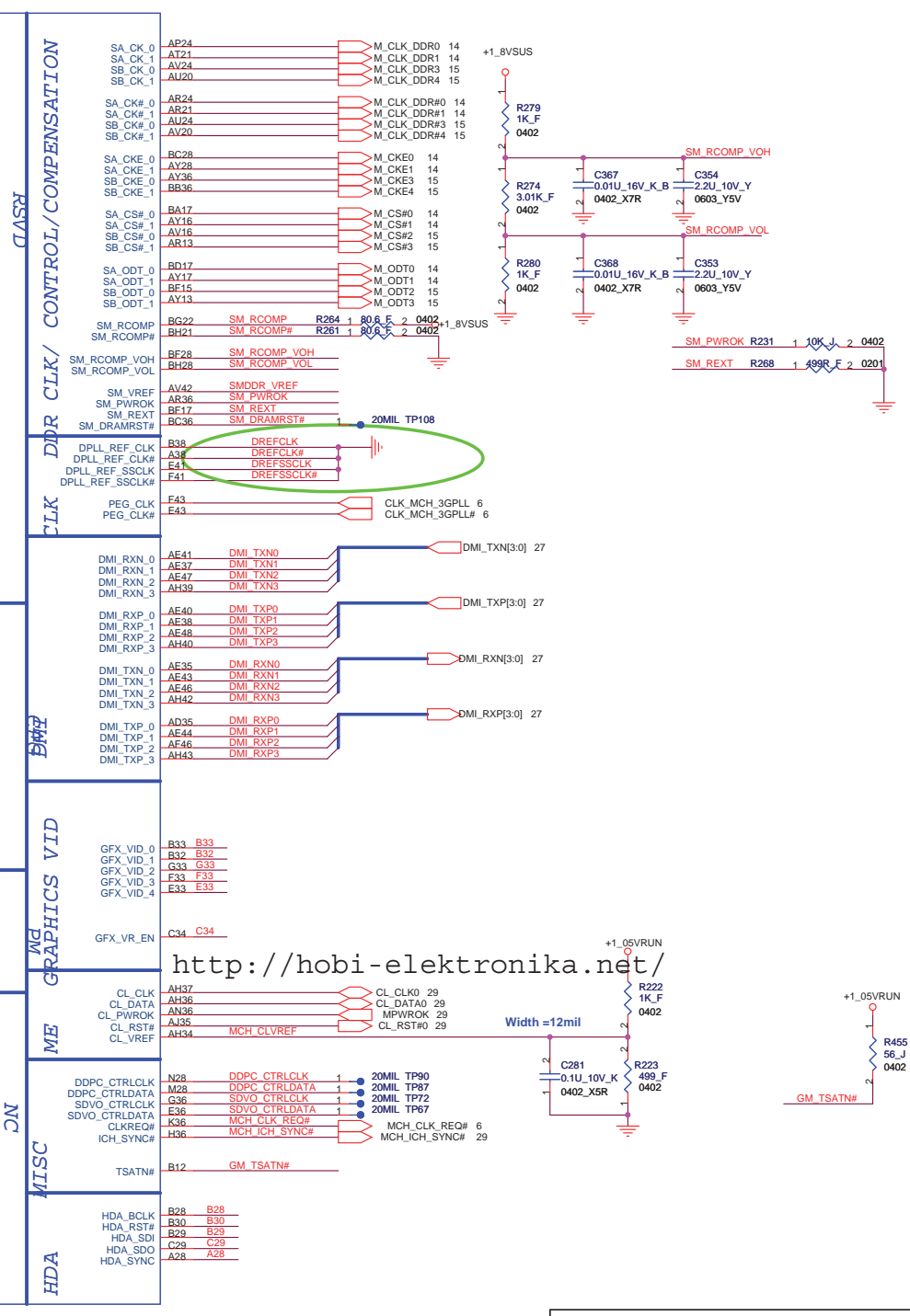
- U32B**
- M36 M36
  - N36 N36
  - R33 R33
  - T33 T33
  - AH9 AH9
  - AH10 AH10
  - AH12 AH12
  - AH13 AH13
  - K12 K12
  - AL34 AL34
  - AK34 AK34
  - AN35 AN35
  - AM35 AM35
  - T24 T24
  - B31 B31
  - B2 B2
  - M1 M1
  - AY21 AY21
  - BG23 BG23
  - BF23 BF23
  - BH18 BH18
  - BF18 BF18

- RSVD1
- RSVD2
- RSVD3
- RSVD4
- RSVD5
- RSVD6
- RSVD7
- RSVD8
- RSVD9
- RSVD10
- RSVD11
- RSVD12
- RSVD13
- RSVD14
- RSVD15
- RSVD16
- RSVD17
- RSVD20
- RSVD22
- RSVD23
- RSVD24
- RSVD25

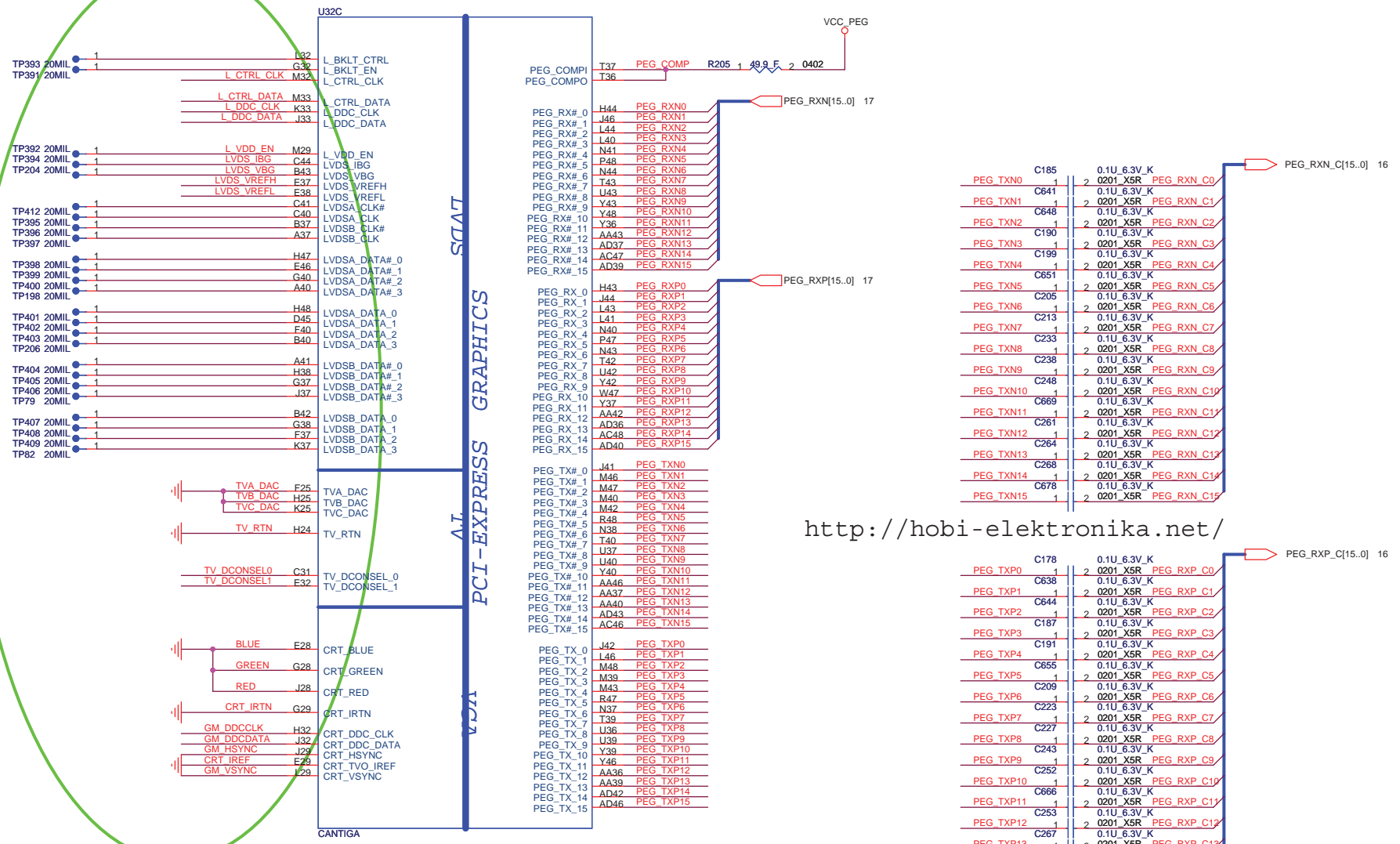
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- CFG\_1
- CFG\_2
- CFG\_3
- CFG\_4
- CFG\_5
- CFG\_6
- CFG\_7
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- CFG\_9
- CFG\_10
- CFG\_11
- CFG\_12
- CFG\_13
- CFG\_14
- CFG\_15
- CFG\_16
- CFG\_17
- CFG\_18
- CFG\_19
- CFG\_20

- NC\_1
- NC\_2
- NC\_3
- NC\_4
- NC\_5
- NC\_6
- NC\_7
- NC\_8
- NC\_9
- NC\_10
- NC\_11
- NC\_12
- NC\_13
- NC\_14
- NC\_15
- NC\_16
- NC\_17
- NC\_18
- NC\_19
- NC\_20
- NC\_21
- NC\_22
- NC\_23
- NC\_24
- NC\_25
- NC\_26

CANTIGA







<http://hobi-elektronika.net/>

EVT

14 M\_A\_DQ[63.0]

M_A_DQ0	AJ38	SA_DQ_0
M_A_DQ1	AJ41	SA_DQ_1
M_A_DQ2	AN38	SA_DQ_2
M_A_DQ3	AM38	SA_DQ_3
M_A_DQ4	AJ36	SA_DQ_4
M_A_DQ5	AJ40	SA_DQ_5
M_A_DQ6	AM44	SA_DQ_6
M_A_DQ7	AM42	SA_DQ_7
M_A_DQ8	AN43	SA_DQ_8
M_A_DQ9	AN44	SA_DQ_9
M_A_DQ10	AL40	SA_DQ_10
M_A_DQ11	AT38	SA_DQ_11
M_A_DQ12	AN41	SA_DQ_12
M_A_DQ13	AN39	SA_DQ_13
M_A_DQ14	AL44	SA_DQ_14
M_A_DQ15	AL42	SA_DQ_15
M_A_DQ16	AV39	SA_DQ_16
M_A_DQ17	AY44	SA_DQ_17
M_A_DQ18	BA40	SA_DQ_18
M_A_DQ19	BD43	SA_DQ_19
M_A_DQ20	AV41	SA_DQ_20
M_A_DQ21	AY43	SA_DQ_21
M_A_DQ22	BA43	SA_DQ_22
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M_A_DQ42	AL10	SA_DQ_42
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M_A_DQ45	BD9	SA_DQ_45
M_A_DQ46	AY8	SA_DQ_46
M_A_DQ47	BA6	SA_DQ_47
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M_A_DQ52	AU5	SA_DQ_52
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M_A_DQ61	AM13	SA_DQ_61
M_A_DQ62	AJ11	SA_DQ_62
M_A_DQ63	AJ12	SA_DQ_63

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DDR SYSTEM MEMORY A

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SA_BS_1	BG18	M_A_BS1	14
SA_BS_2	AT25	M_A_BS2	14
SA_RAS#	BB20	M_A_RAS#	14
SA_CAS#	BD20	M_A_CAS#	14
SA_WE#	AY20	M_A_WE#	14
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SA_DM_1	AT41	M_A_DM1	14
SA_DM_2	AY41	M_A_DM2	14
SA_DM_3	AU39	M_A_DM3	14
SA_DM_4	BB12	M_A_DM4	14
SA_DM_5	AY6	M_A_DM5	14
SA_DM_6	AT7	M_A_DM6	14
SA_DM_7	AJ5	M_A_DM7	14
SA_DQS_0	AJ44	M_A_DQS0	14
SA_DQS_1	BA43	M_A_DQS1	14
SA_DQS_2	BC37	M_A_DQS2	14
SA_DQS_3	AW12	M_A_DQS3	14
SA_DQS_4	BC8	M_A_DQS4	14
SA_DQS_5	AU8	M_A_DQS5	14
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SA_MA_4	BG25	M_A_A4	14
SA_MA_5	BA24	M_A_A5	14
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SA_MA_10	BC21	M_A_A10	14
SA_MA_11	BG26	M_A_A11	14
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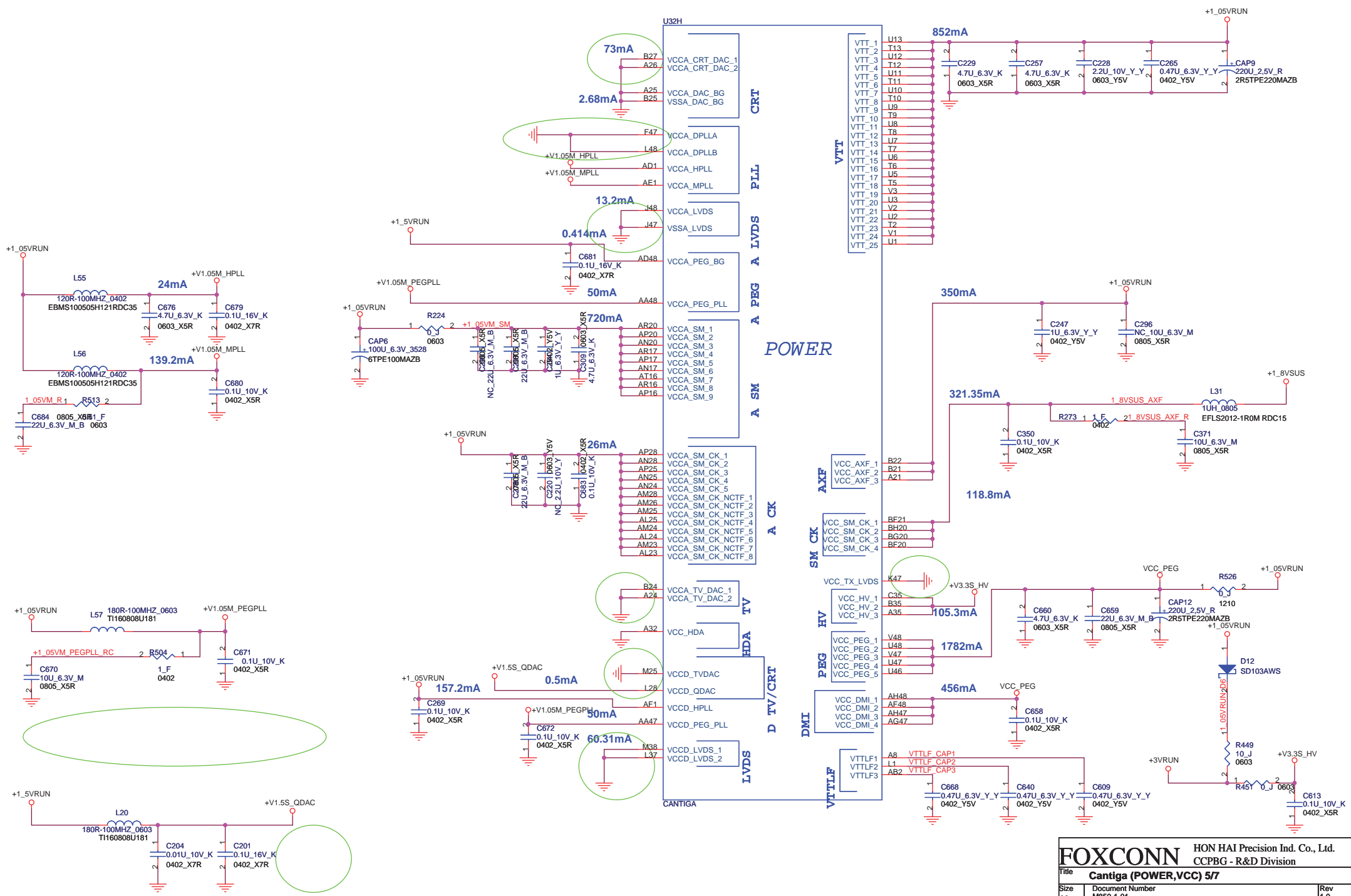
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M_B_DQ35	BG8	SB_DQ_35
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M_B_DQ46	BA1	SB_DQ_46
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M_B_DQ57	AL2	SB_DQ_57
M_B_DQ58	AJ1	SB_DQ_58
M_B_DQ59	AH1	SB_DQ_59
M_B_DQ60	AM2	SB_DQ_60
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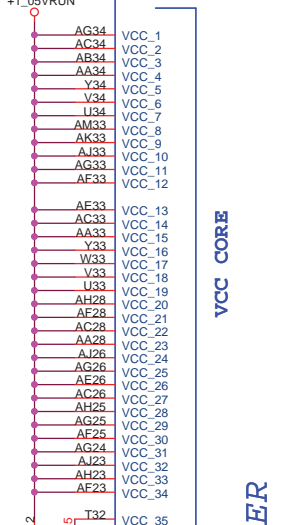
CANTIGA

DDR SYSTEM MEMORY B

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SB_CAS#	BG16	M_B_CAS#	15
SB_WE#	BF14	M_B_WE#	15
SB_DM_0	AM47	M_B_DM0	15
SB_DM_1	AY47	M_B_DM1	15
SB_DM_2	BD40	M_B_DM2	15
SB_DM_3	BF35	M_B_DM3	15
SB_DM_4	BG11	M_B_DM4	15
SB_DM_5	BA3	M_B_DM5	15
SB_DM_6	AP1	M_B_DM6	15
SB_DM_7	AK2	M_B_DM7	15
SB_DQS_0	AL47	M_B_DQS0	15
SB_DQS_1	AV48	M_B_DQS1	15
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SB_DQS_4	BH9	M_B_DQS4	15
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SB_DQS#_2	BH41	M_B_DQS#2	15
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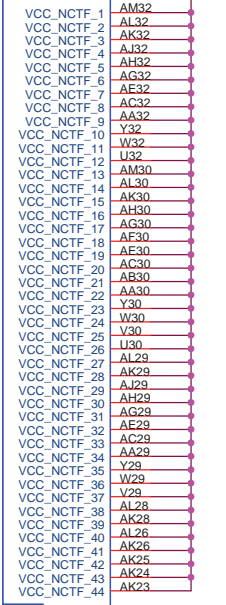
3.06A



VCC CORE

POWER

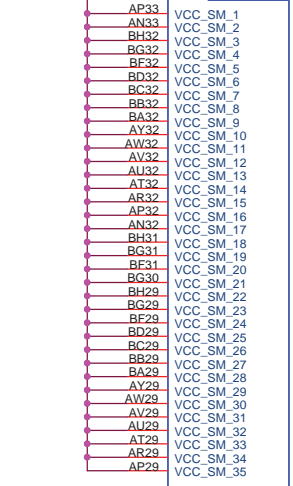
VCC NCTF



+1\_05VRUN



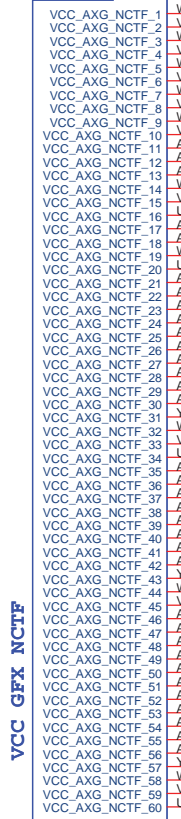
3A +1\_8VSUS



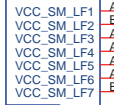
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VCC GFX NCTF

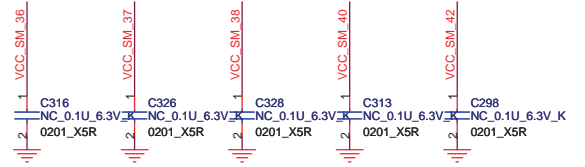
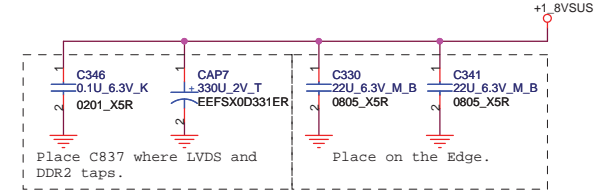
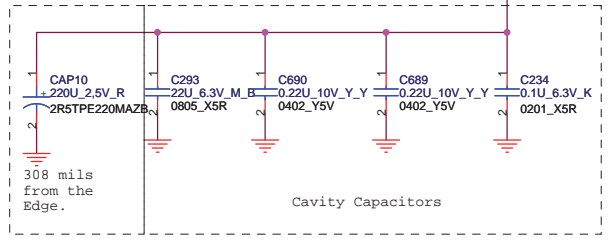
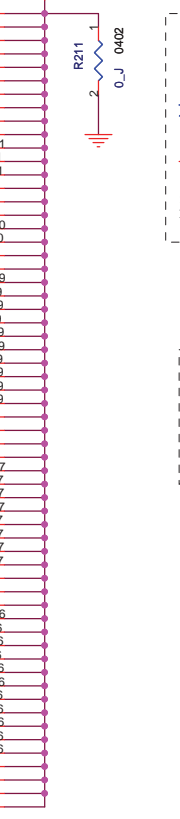
VCC GFX



VCC SM L.F

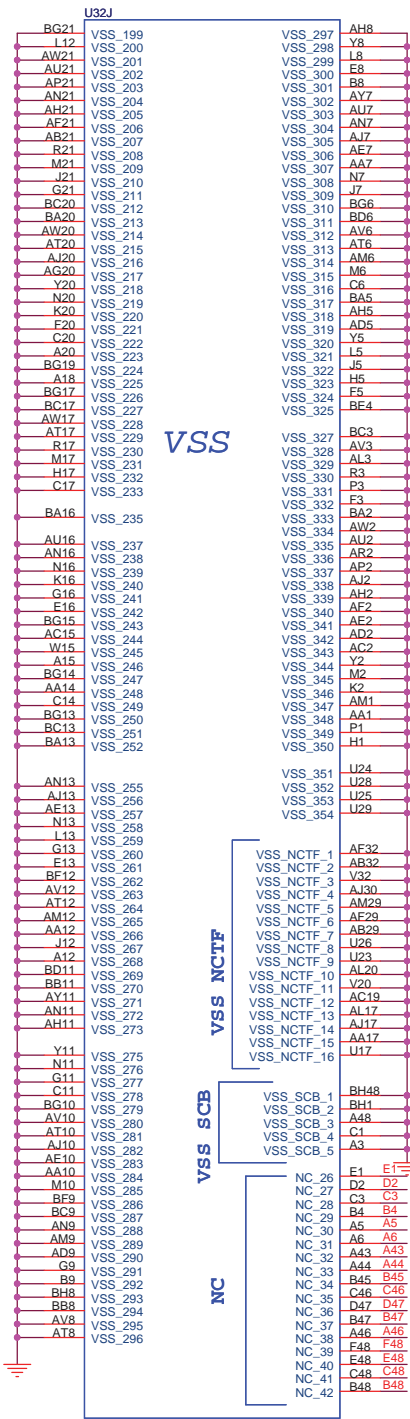
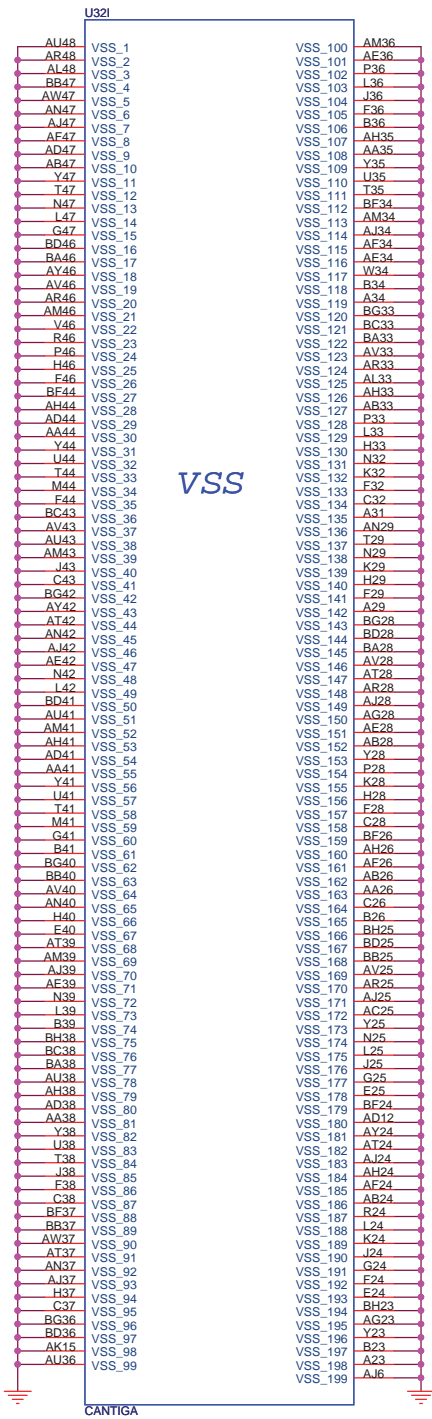


+VGF\_X\_CORE 8.7A



**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title <b>Cantiga (VCC CORE) 6/7</b>		
Size A3	Document Number M850-1-01	Rev 1.0
Date: Thursday, July 09, 2009	Sheet 12	of 69



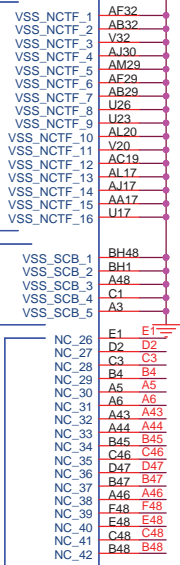
VSS

VSS

VSS NCTF

VSS SCB

NC

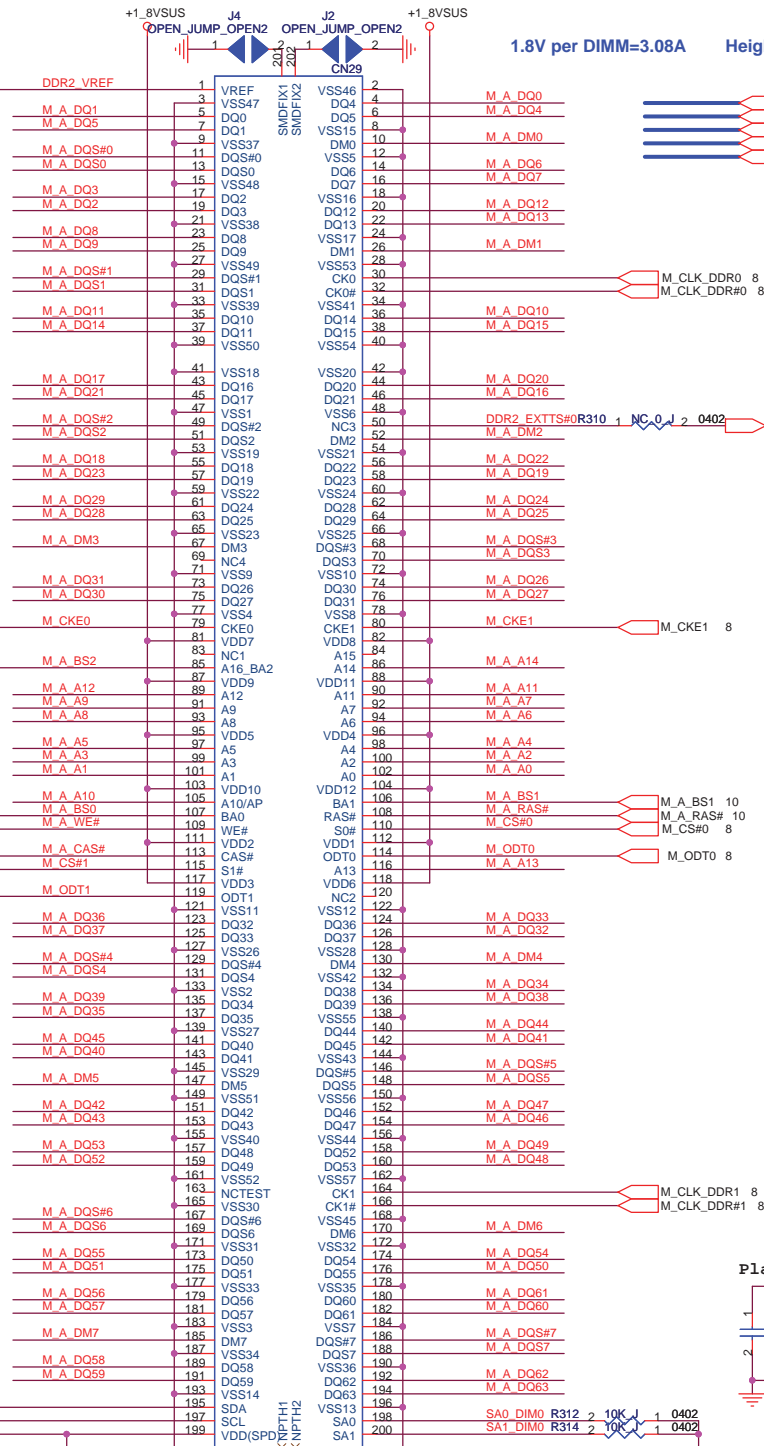
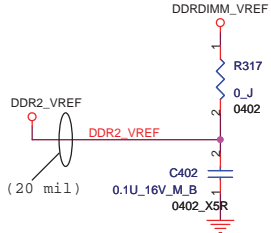
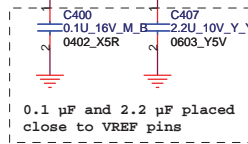


**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **Cantiga (VSS) 7/7**

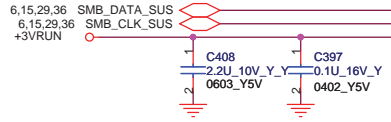
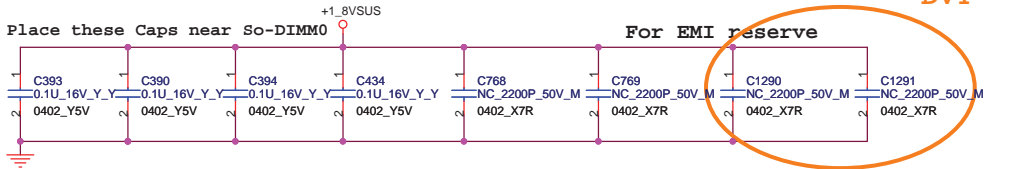
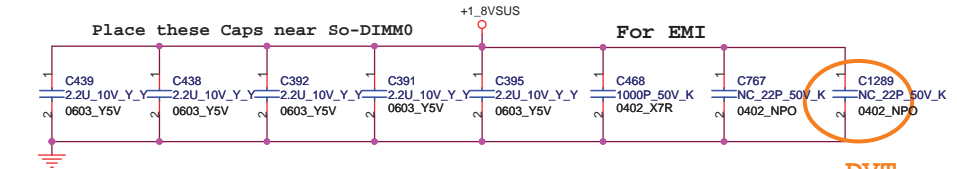
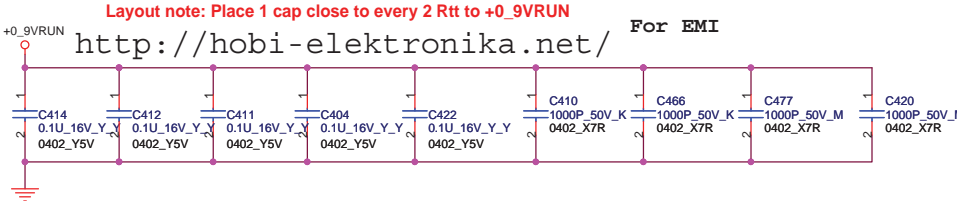
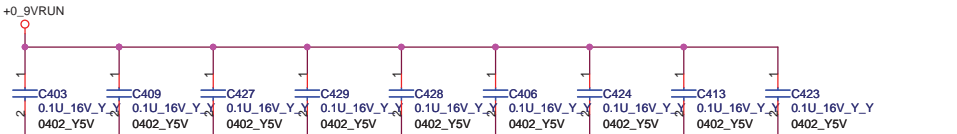
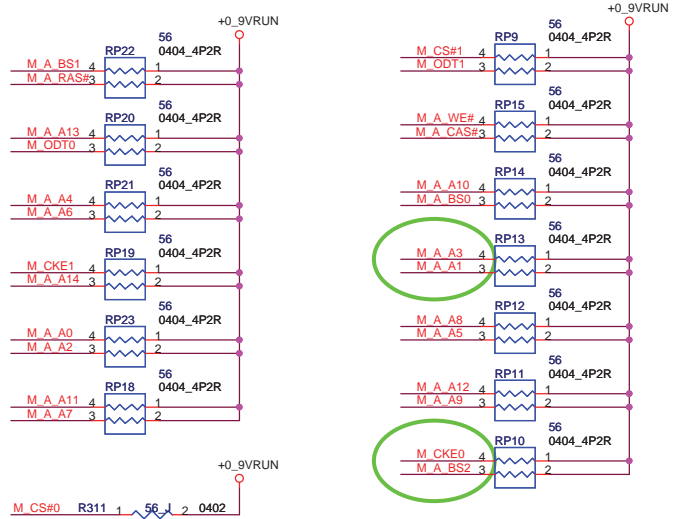
Size: A3	Document Number: M850-1-01	Rev: 1.0
Date: Thursday, February 26, 2009	Sheet: 13	of: 69





SMBus Address: A0H(W)/A1H(R)

Place DIMM\_0 near GMCH



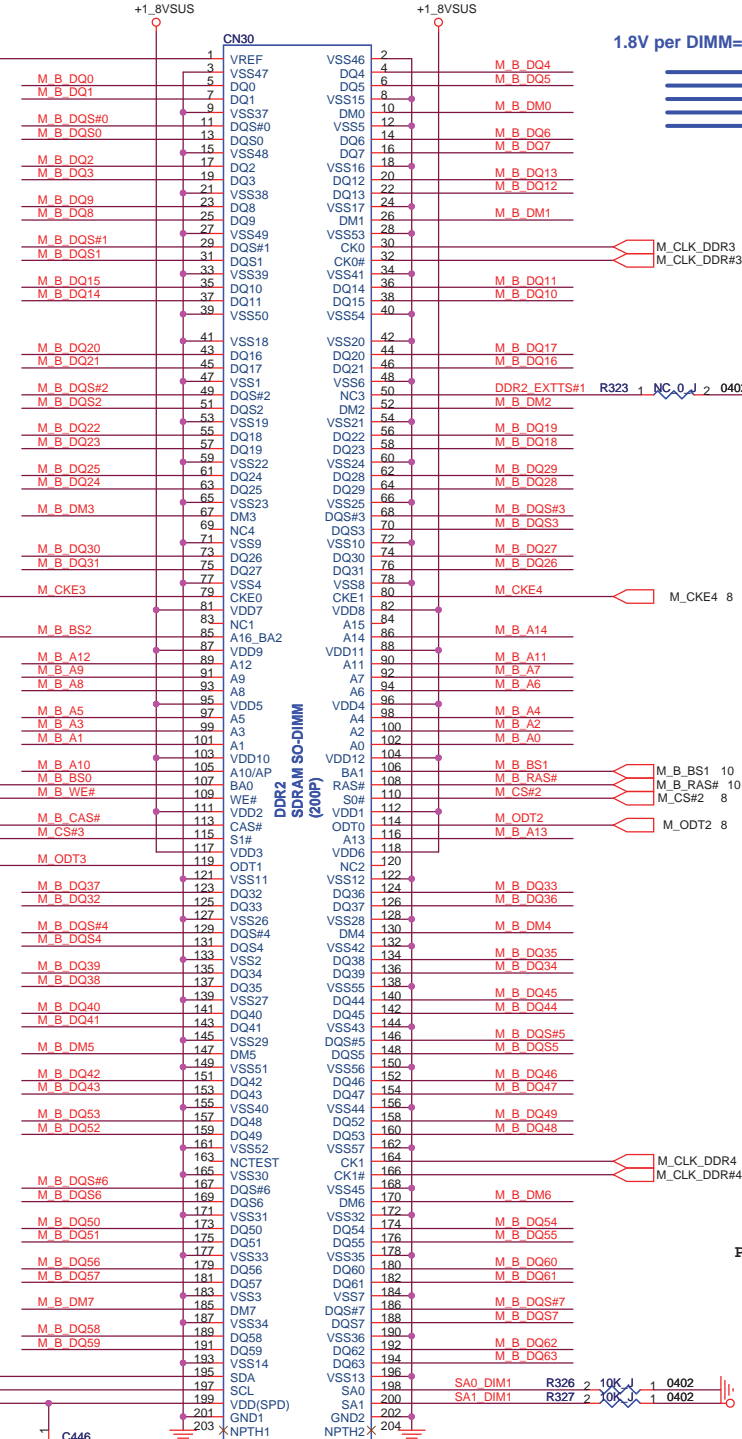
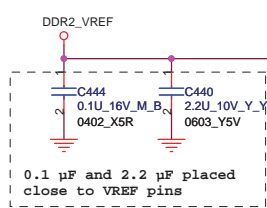
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

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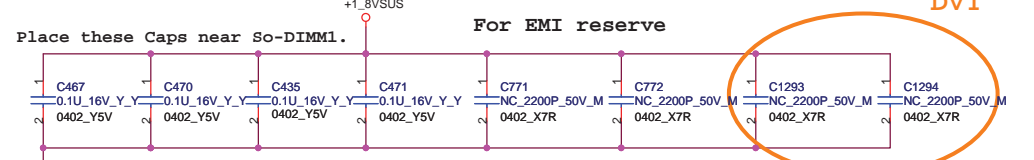
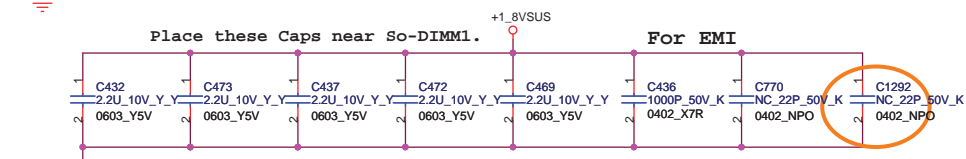
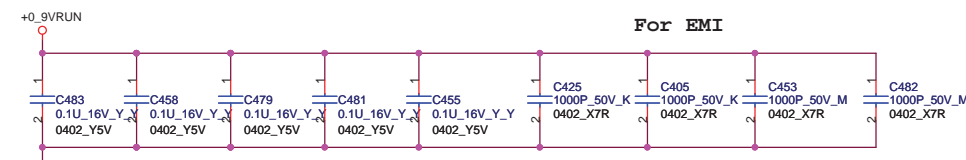
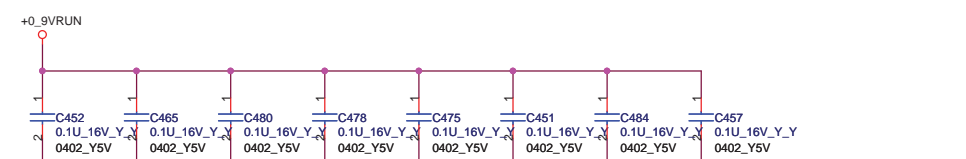
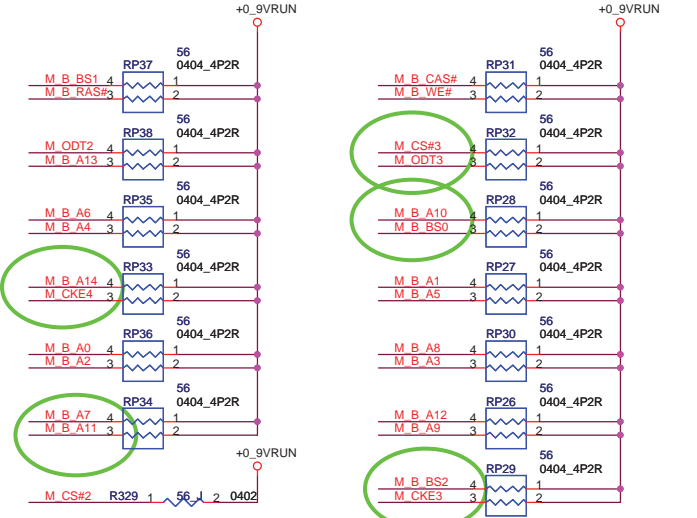
Size A3	Document Number M850-1-01	Rev 1.0
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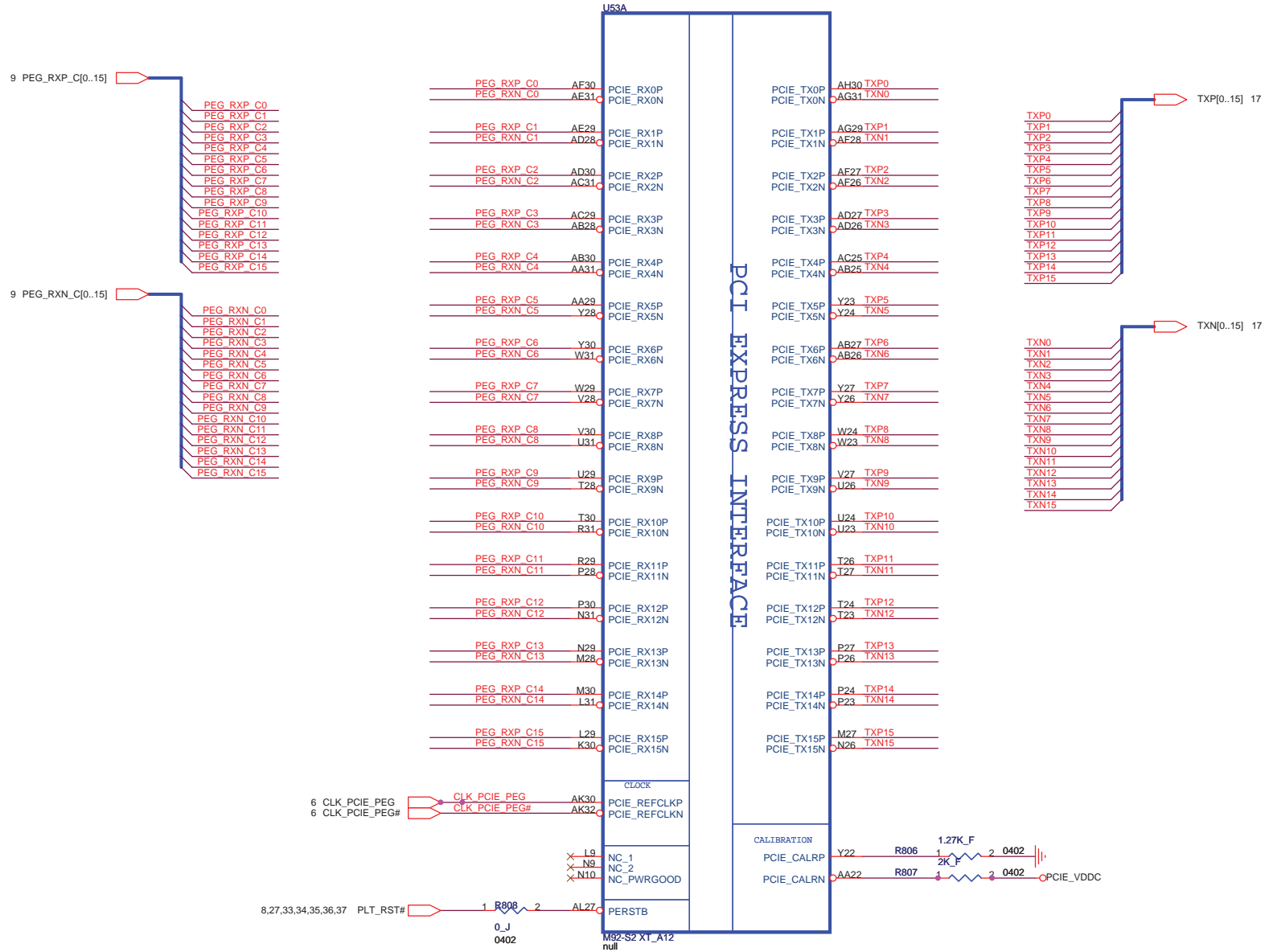
Date: Wednesday, April 01, 2009 Sheet 14 of 69





1.8V per DIMM=3.08A Height = 9.2 mm

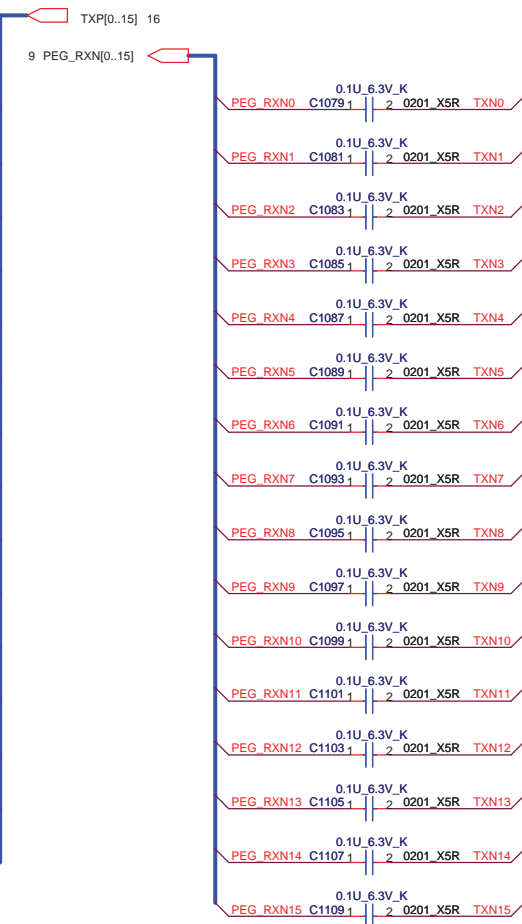
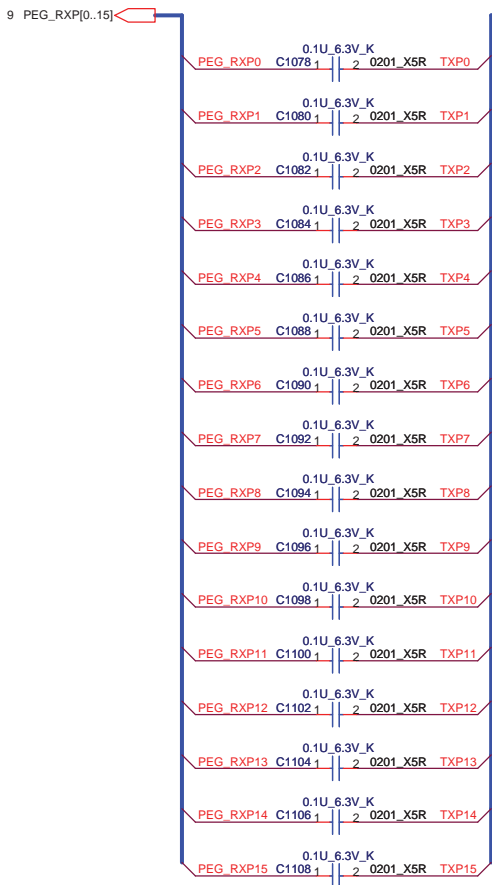




	Mount	NC
Hynix-256MB H5RS1H23MFR-11C	R812,R809	R910,R911, R811,R810
Hynix-512MB H5RS1H23MFR-11C	R910 R812,R809	R911 R811,R810

	Mount	NC
Samsung-256MB K4J10324QD-HC12	R812,R810	R910,R911, R811,R809
Qimonda-256MB HYB18H1G321A2F-10	R811,R810	R910,R911, R812,R809

	Mount	NC
Samsung-512MB K4J10324QD-HC12	R910 R812,R810	R911 R811,R809
Qimonda-512MB HYB18H1G321A2F-10	R910 R811,R810	R911 R812,R809



### DVT

### DVT

Strap for GDDR3-136ball  
ATL\_DVPDATA[1:0:21:20]

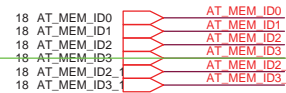
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 0011 32Mx32 Samsung-256MB  
 0101 32Mx32 Qimonda-512MB  
 0110 32Mx32 Hynix-512MB  
 0111 32Mx32 Samsung-512MB

If no ROM attached, GPIO[13:12:11] ;  
 CONFIG(2:0)  
 controls the memory aperture size.  
 64MB 010  
 128MB 000  
 256MB 001  
 512MB 001

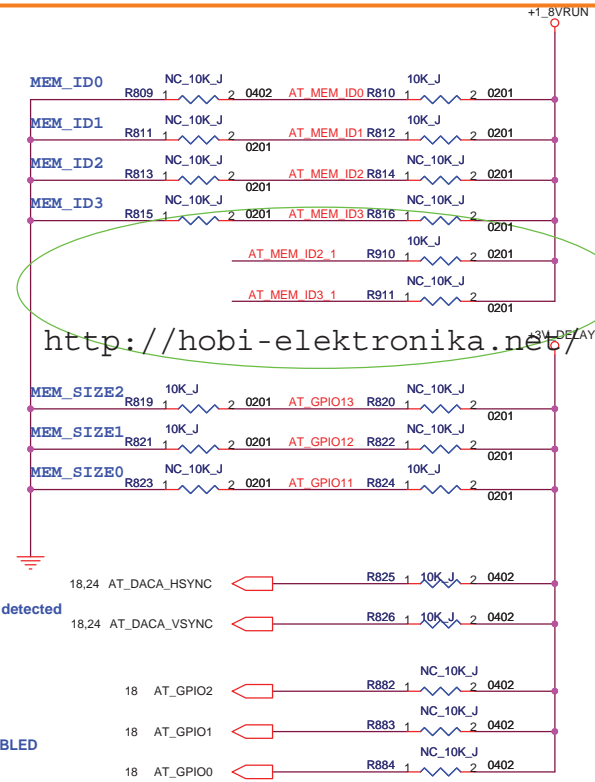
HSYNC , VSYNC  
 AUD[1] , AUD[0]

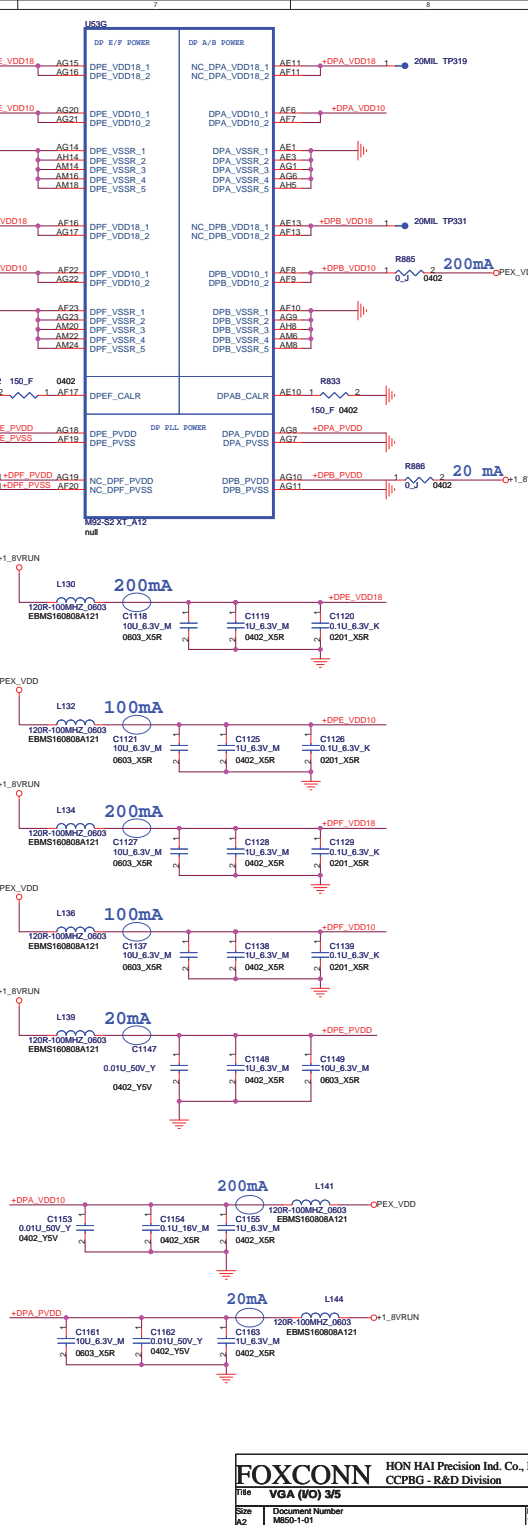
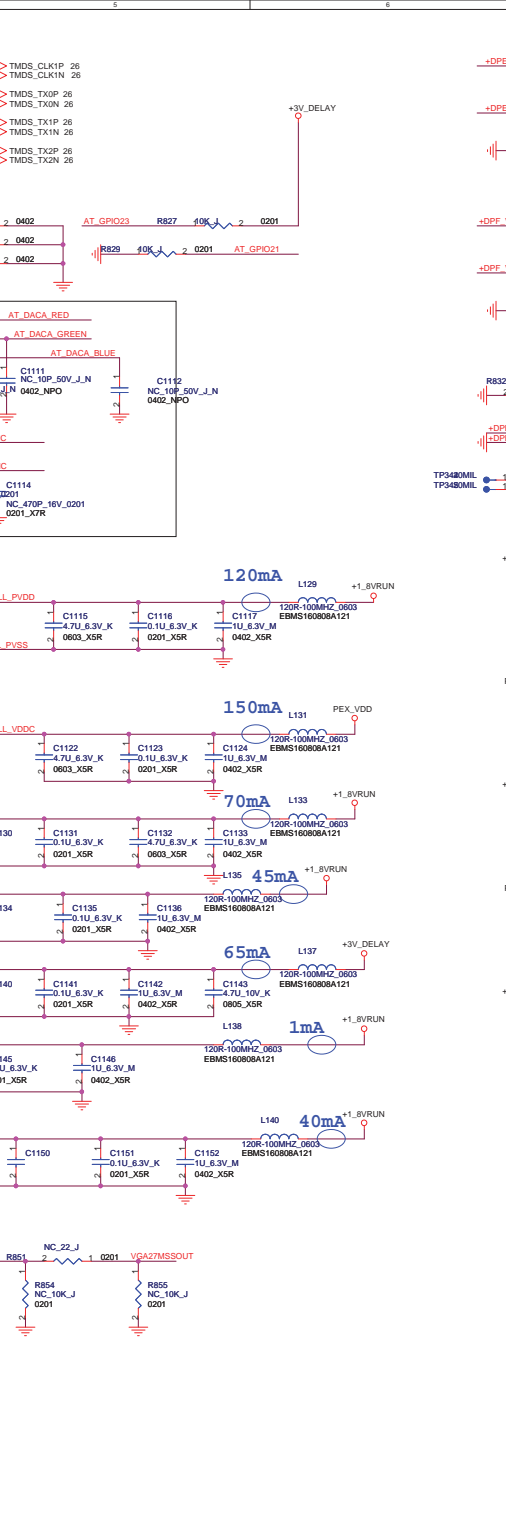
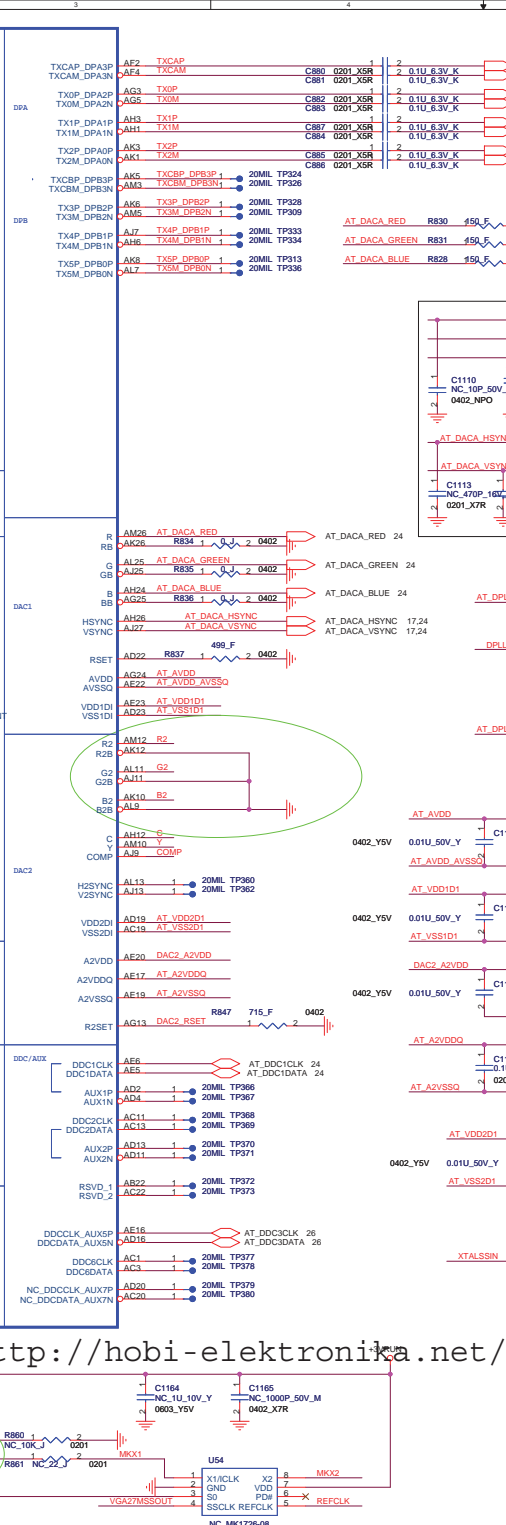
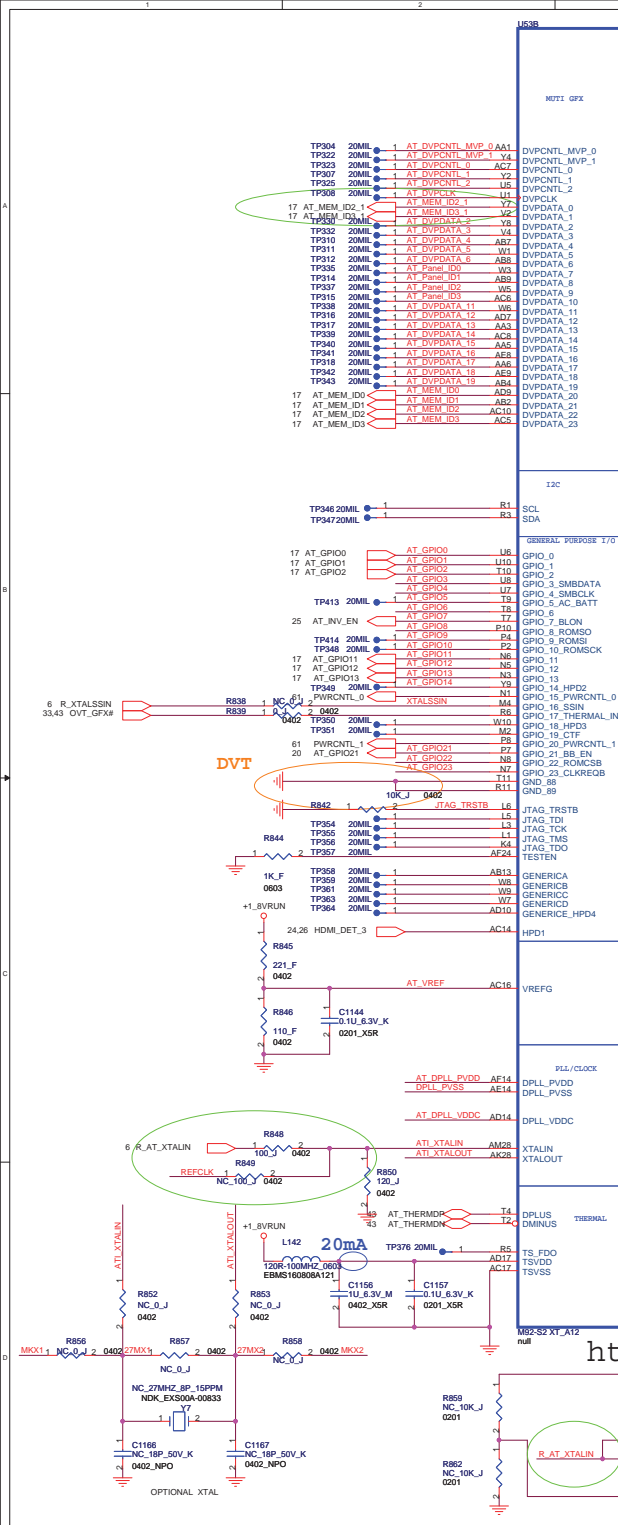
0,0 No audio function  
 0,1 Audio for DisplayPort and HDMI if dongle is detected  
 1,0 Audio for DisplayPort only  
 1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING  
 GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED  
 GPIO 2 : PCIE GEN2 ENABLED

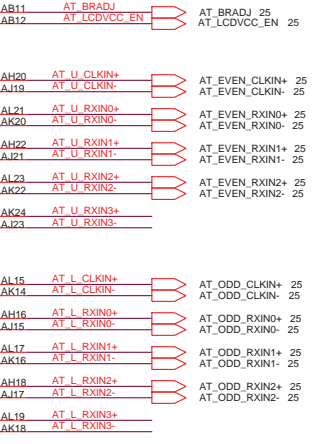
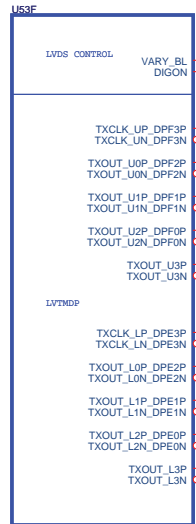


For AMD verification

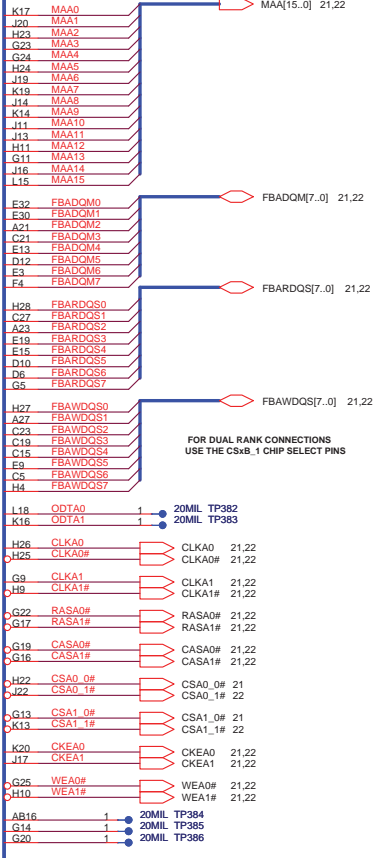
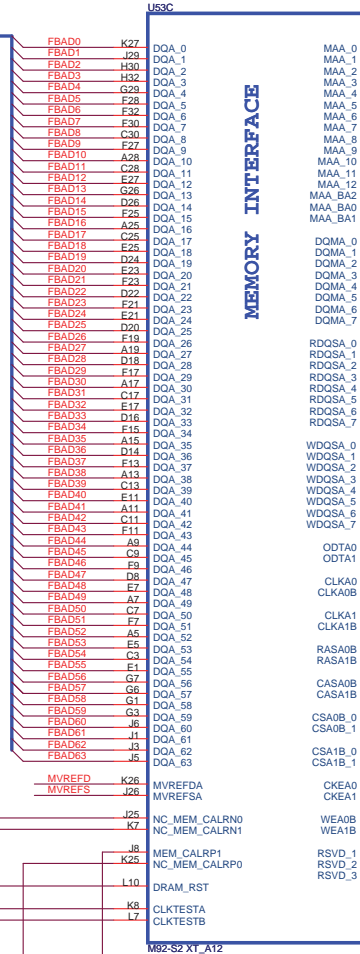
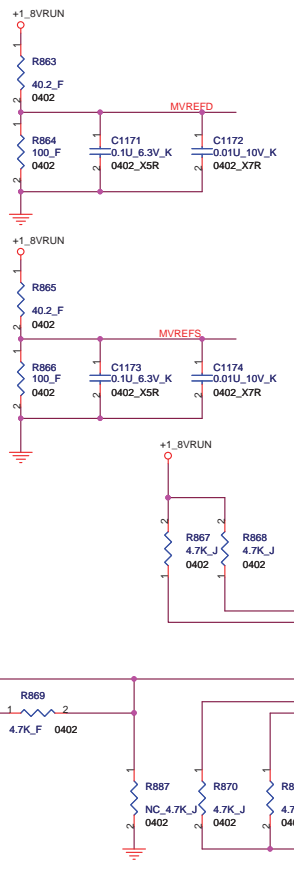




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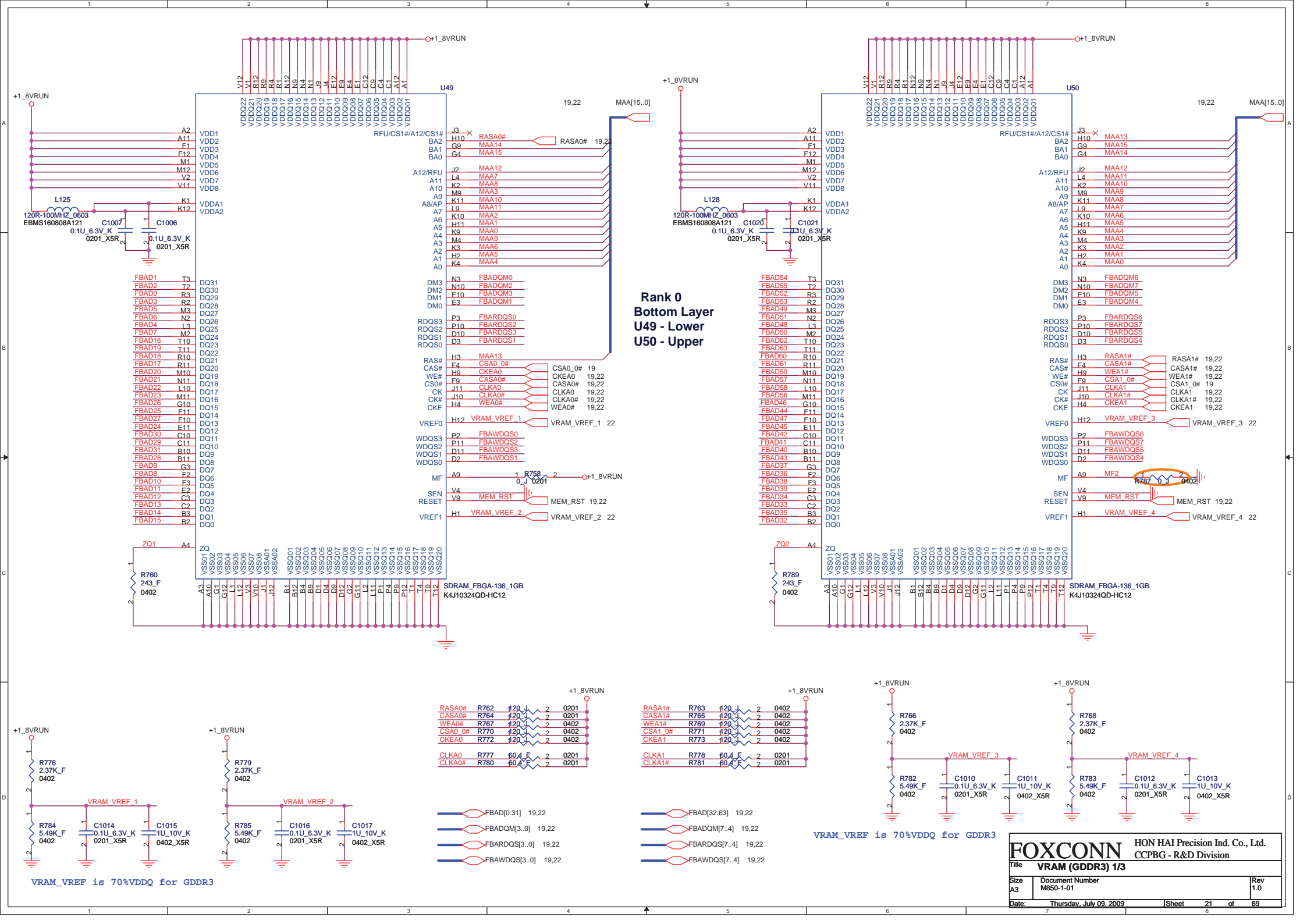


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC





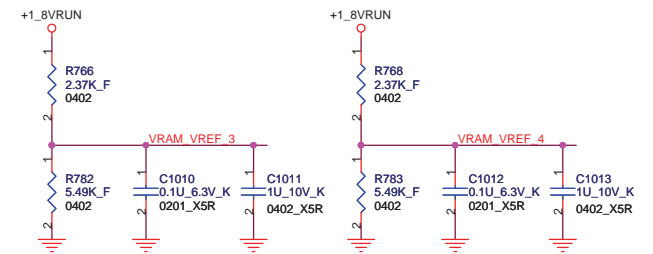
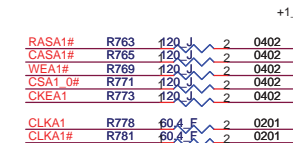
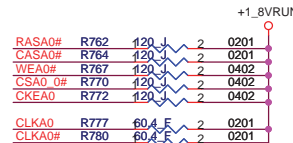
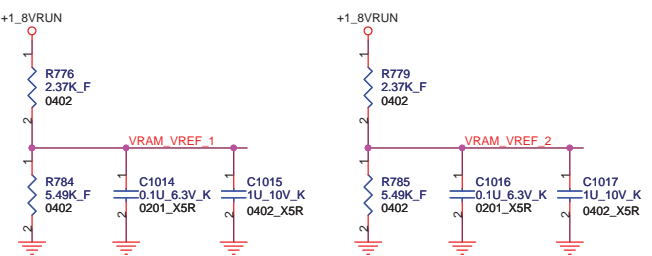
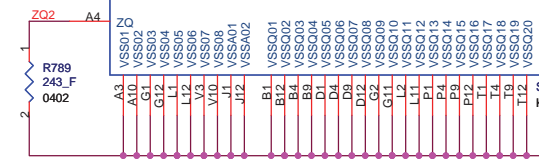
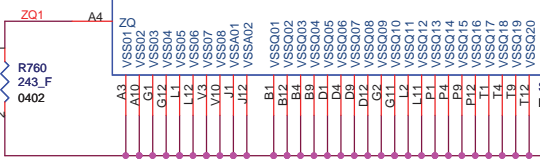




**Rank 0  
Bottom Layer  
U49 - Lower  
U50 - Upper**

- FBAD1 T3 DQ31
- FBAD2 T2 DQ30
- FBAD0 R3 DQ29
- FBAD3 R2 DQ28
- FBAD5 M3 DQ27
- FBAD6 N2 DQ26
- FBAD4 L3 DQ25
- FBAD7 M2 DQ24
- FBAD16 M2 DQ23
- FBAD19 T11 DQ22
- FBAD18 R10 DQ21
- FBAD17 R11 DQ20
- FBAD20 M10 DQ19
- FBAD21 N11 DQ18
- FBAD22 L10 DQ17
- FBAD23 M11 DQ16
- FBAD26 G11 DQ15
- FBAD25 F11 DQ14
- FBAD27 F10 DQ13
- FBAD24 E11 DQ12
- FBAD30 C10 DQ11
- FBAD29 C11 DQ10
- FBAD31 B10 DQ9
- FBAD28 B11 DQ8
- FBAD9 G3 DQ7
- FBAD8 F2 DQ6
- FBAD10 F3 DQ5
- FBAD11 E2 DQ4
- FBAD12 C3 DQ3
- FBAD13 C2 DQ2
- FBAD14 B3 DQ1
- FBAD15 B2 DQ0

- FBAD54 T3 DQ31
- FBAD55 T2 DQ30
- FBAD52 R3 DQ29
- FBAD53 R2 DQ28
- FBAD49 M3 DQ27
- FBAD51 N2 DQ26
- FBAD48 L3 DQ25
- FBAD50 M2 DQ24
- FBAD62 M2 DQ23
- FBAD63 T10 DQ22
- FBAD60 R10 DQ21
- FBAD61 R11 DQ20
- FBAD59 M10 DQ19
- FBAD57 N11 DQ18
- FBAD58 L10 DQ17
- FBAD56 M11 DQ16
- FBAD46 G11 DQ15
- FBAD44 F11 DQ14
- FBAD47 F10 DQ13
- FBAD45 E11 DQ12
- FBAD42 C10 DQ11
- FBAD41 C11 DQ10
- FBAD40 B10 DQ9
- FBAD43 B11 DQ8
- FBAD37 G3 DQ7
- FBAD36 F2 DQ6
- FBAD38 F3 DQ5
- FBAD39 E2 DQ4
- FBAD34 C3 DQ3
- FBAD35 C2 DQ2
- FBAD32 B2 DQ1



VRAM\_VREF is 70%VDDQ for GDDR3

VRAM\_VREF is 70%VDDQ for GDDR3

- FBAD[0:31] 19,22
- FBADQM[3:0] 19,22
- FBARDQS[3:0] 19,22
- FBAWDQS[3:0] 19,22

- FBAD[32:63] 19,22
- FBADQM[7:4] 19,22
- FBARDQS[7:4] 19,22
- FBAWDQS[7:4] 19,22

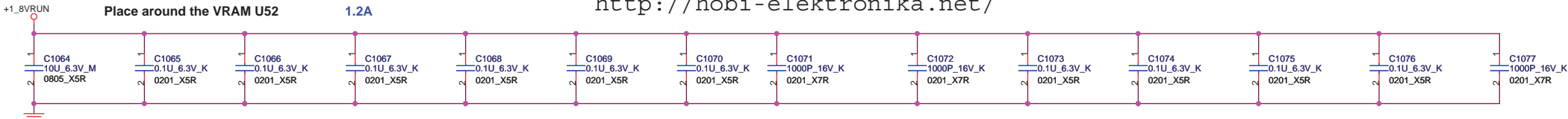
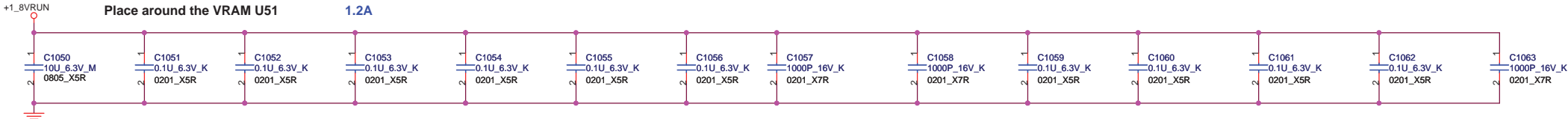
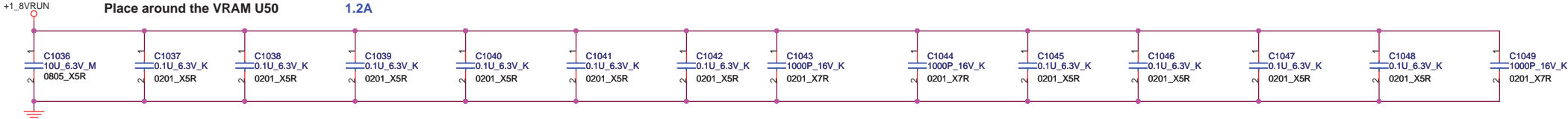
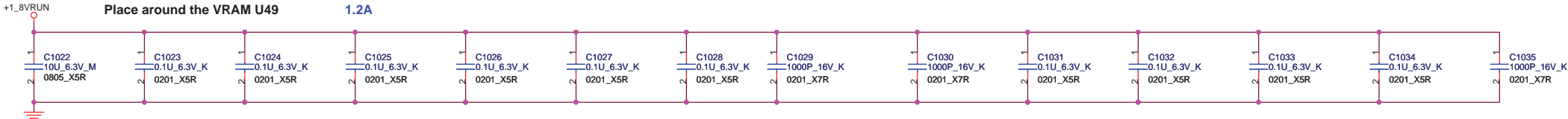
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CCPBG - R&D Division

Title **VRAM (GDDR3) 1/3**

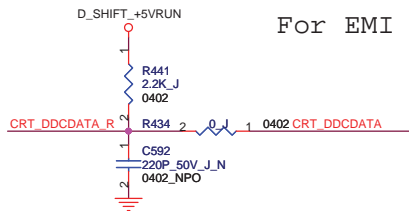
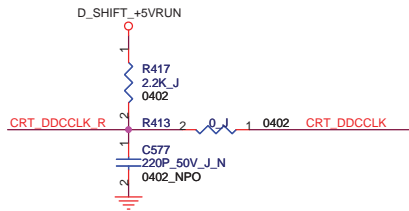
Size A3	Document Number M950-1-01	Rev 1.0
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Date: Thursday, July 09, 2009 Sheet 21 of 69

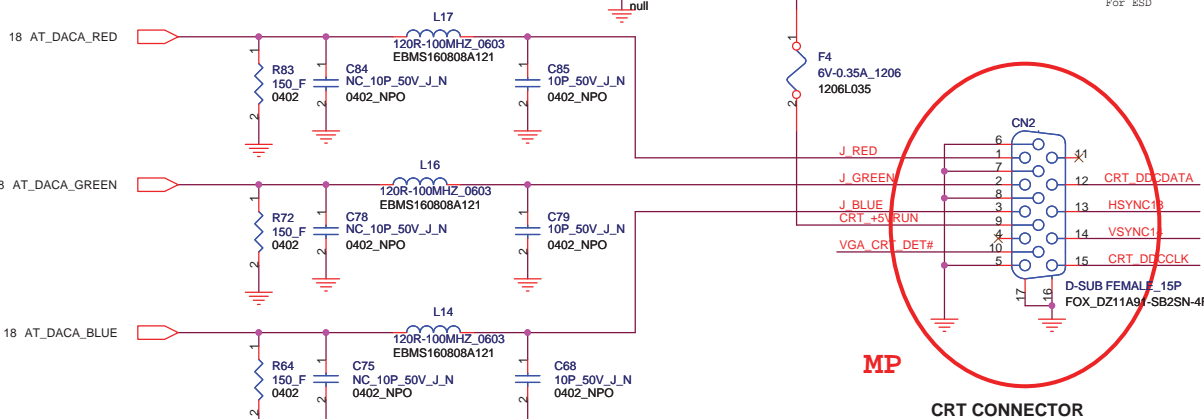
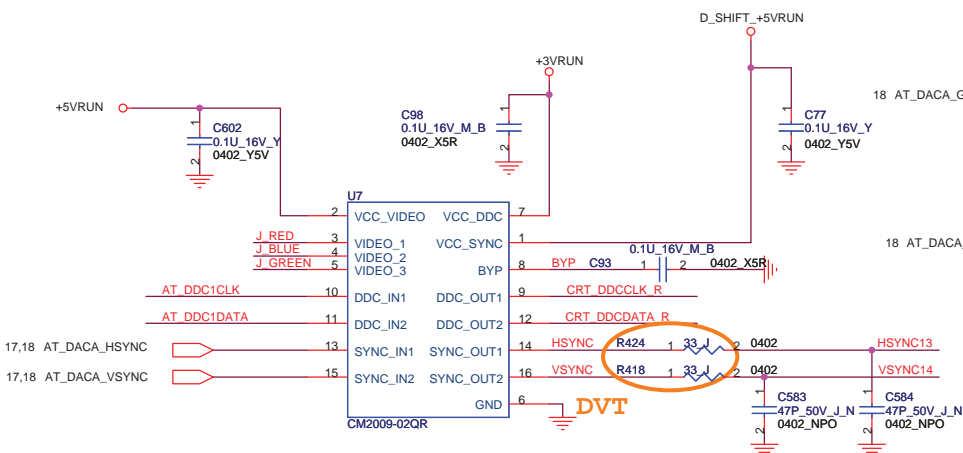
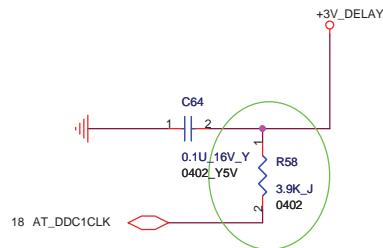
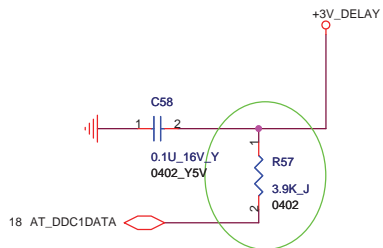




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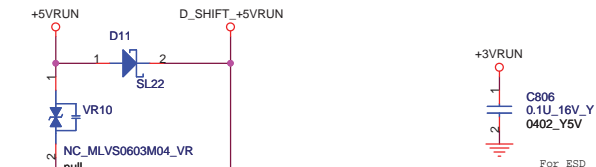
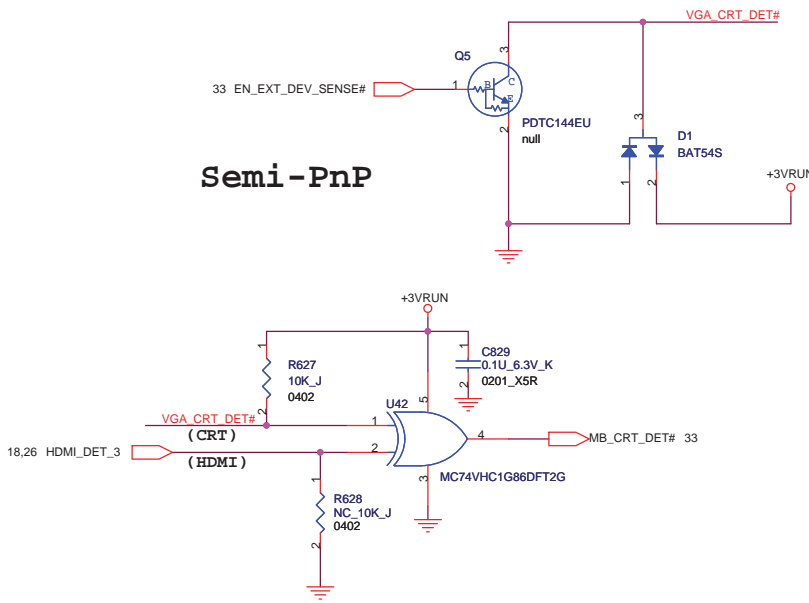


For EMI



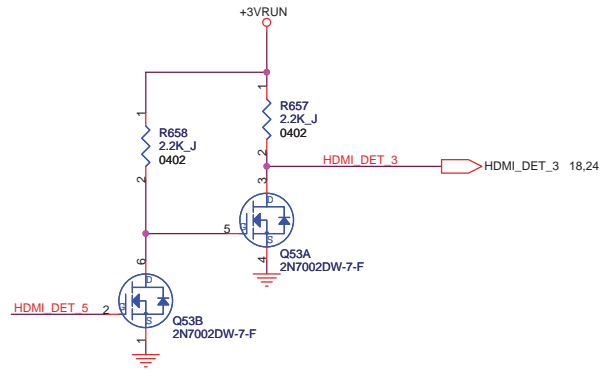
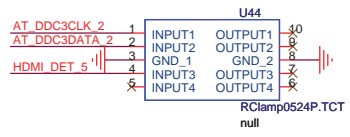
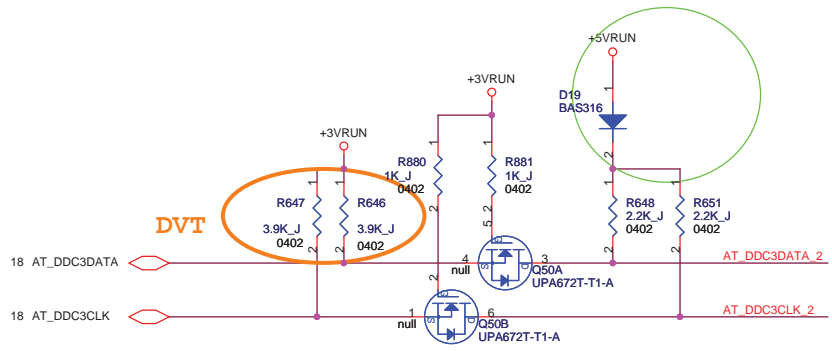
**MP**  
CRT CONNECTOR

Semi-PnP

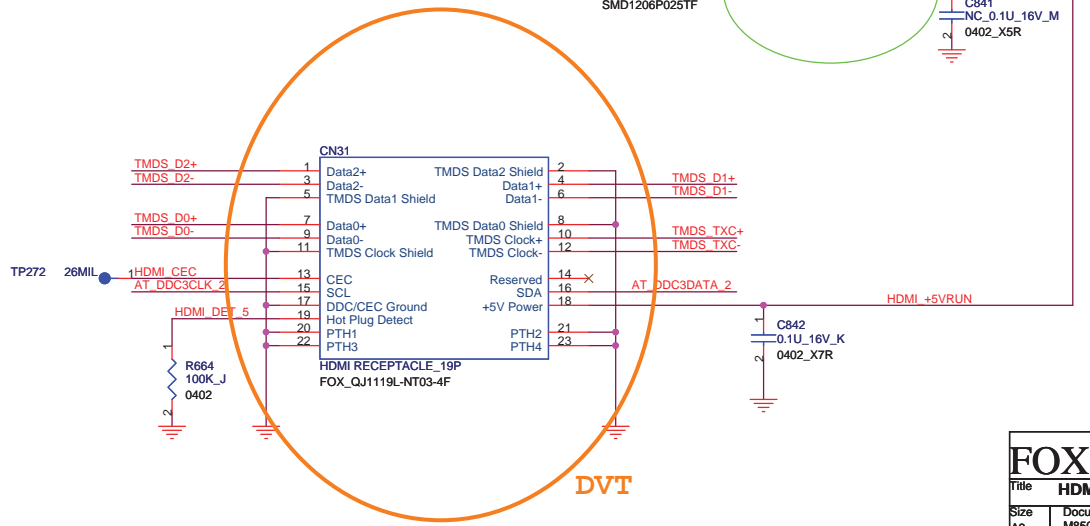
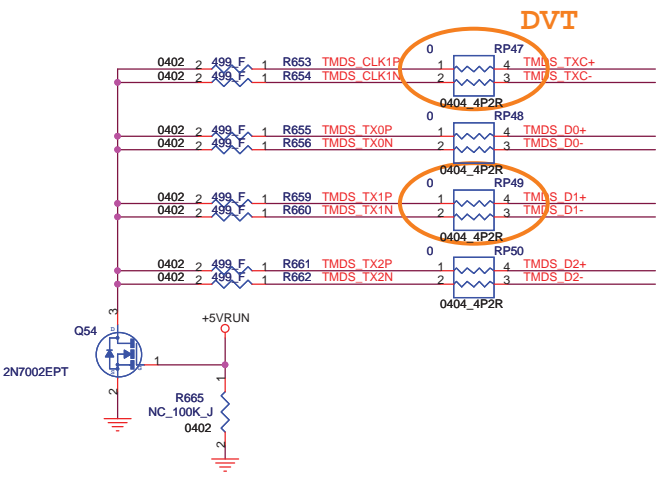
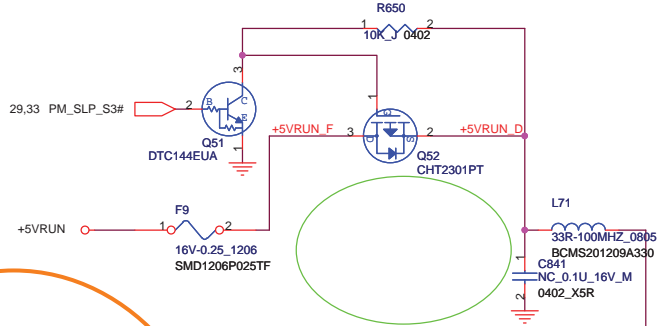


For ESD

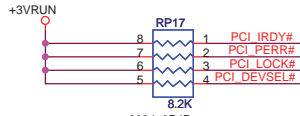
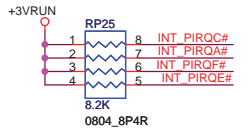
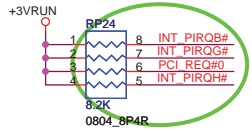
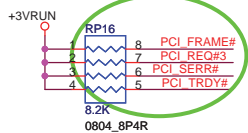
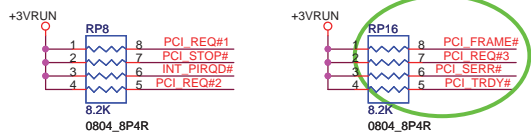




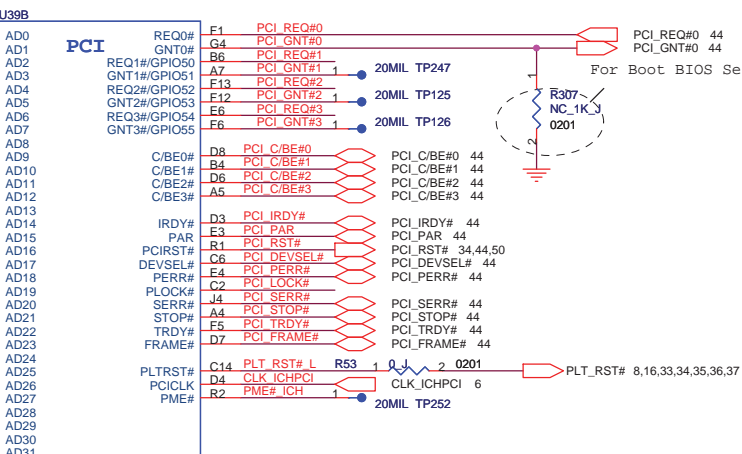
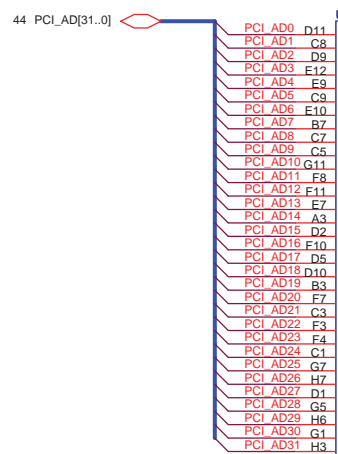
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- 18 TMDS\_CLK1P
- 18 TMDS\_TX0N
- 18 TMDS\_TX0P
- 18 TMDS\_TX1N
- 18 TMDS\_TX1P
- 18 TMDS\_TX2N
- 18 TMDS\_TX2P





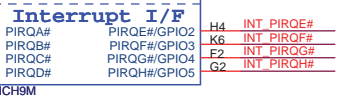


PCI Pullups



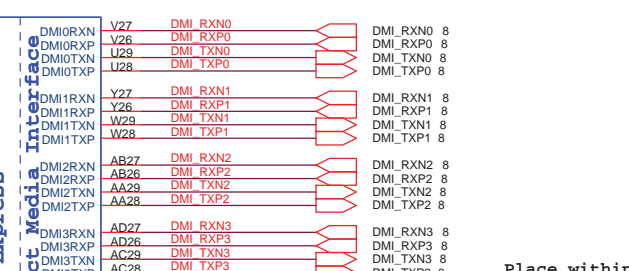
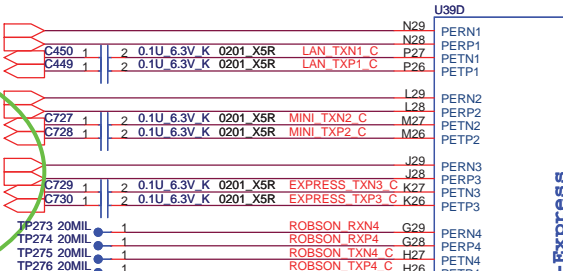
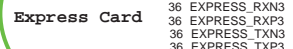
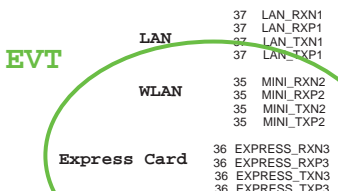
**Strap for Boot-BIOS**

	GNT#	SPI_CS1#
LPC(Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI



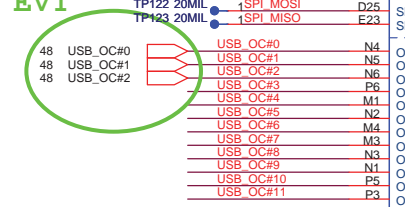
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EVT

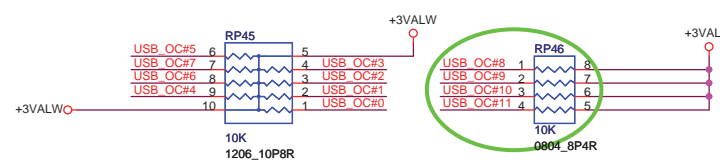


USB PORT	Function
PORT-0	Ext. Port
PORT-1	Ext. Port
PORT-2	Ext. Port
PORT-3	
PORT-4	Bluetooth
PORT-5	EXPRESS CARD
PORT-6	
PORT-7	Camera
PORT-8	Felica
PORT-9	
PORT-10	Wi-MAX
PORT-11	

EVT



Place within 500 mils of ICH and don't routing next to high speed signals

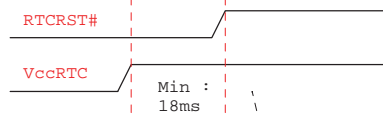


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Title: **ICH9-M(PCI/DMI/USB/PCIE) 1/5**

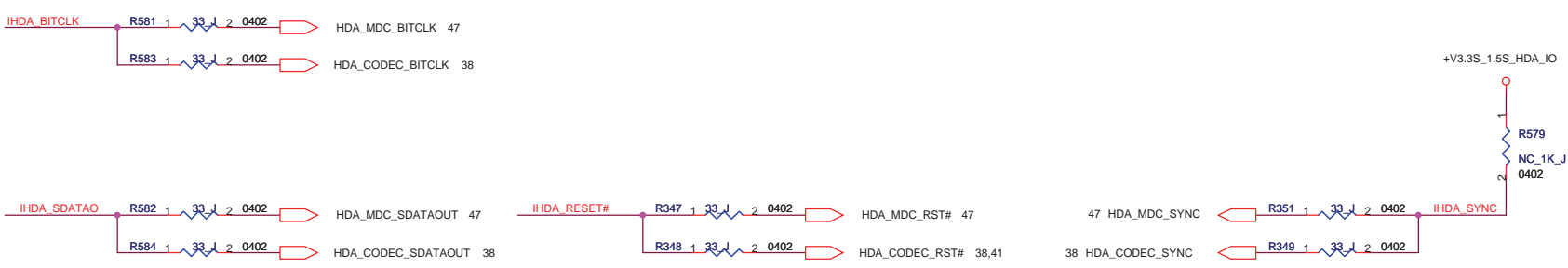
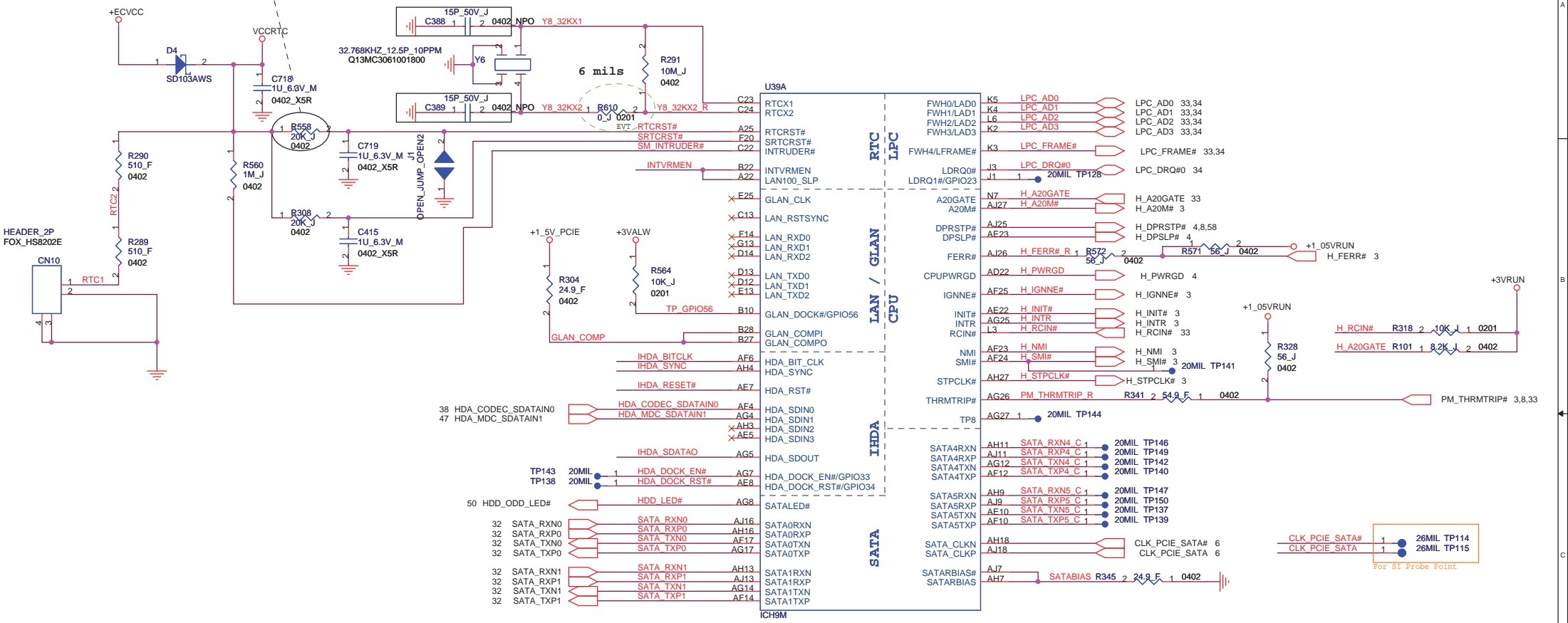
Size A3	Document Number M850-1-01	Rev 1.0
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Date: Wednesday, April 01, 2009 | Sheet 27 of 69

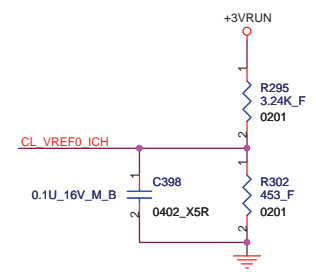
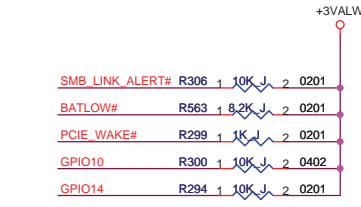
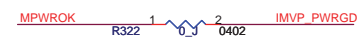
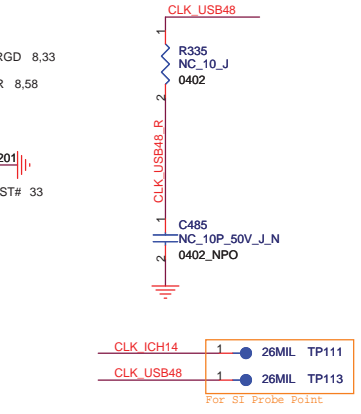
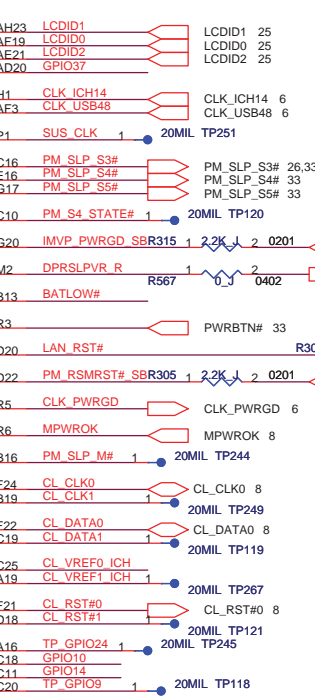
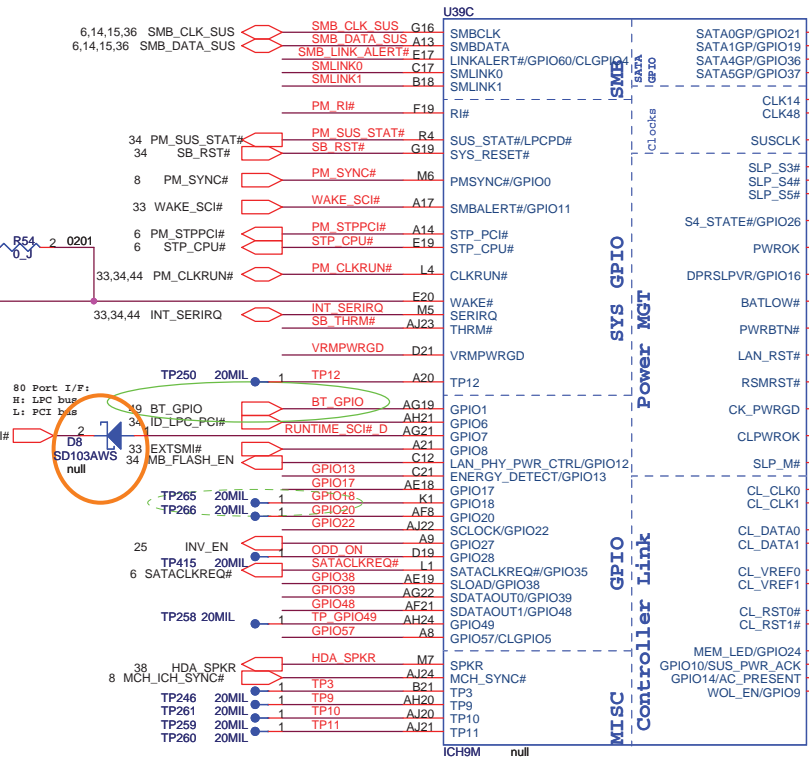
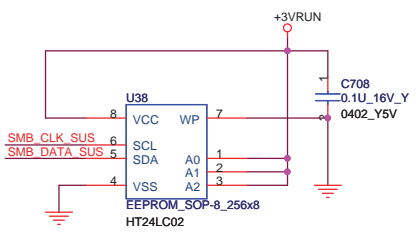
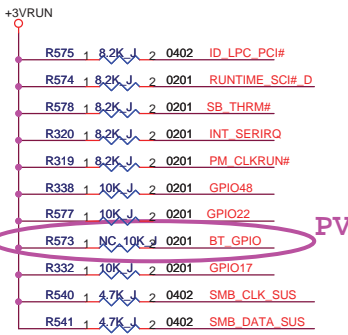
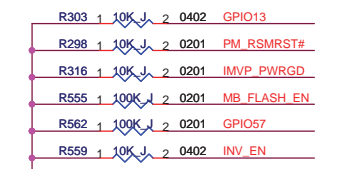
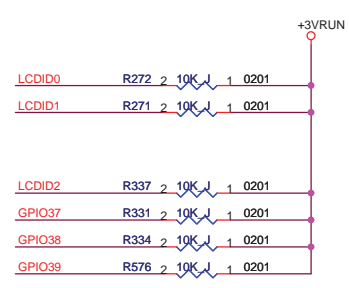
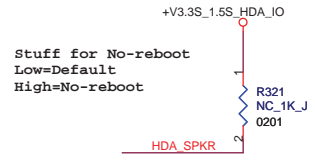
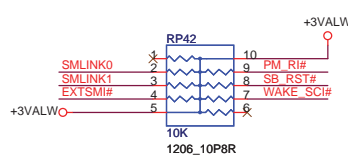


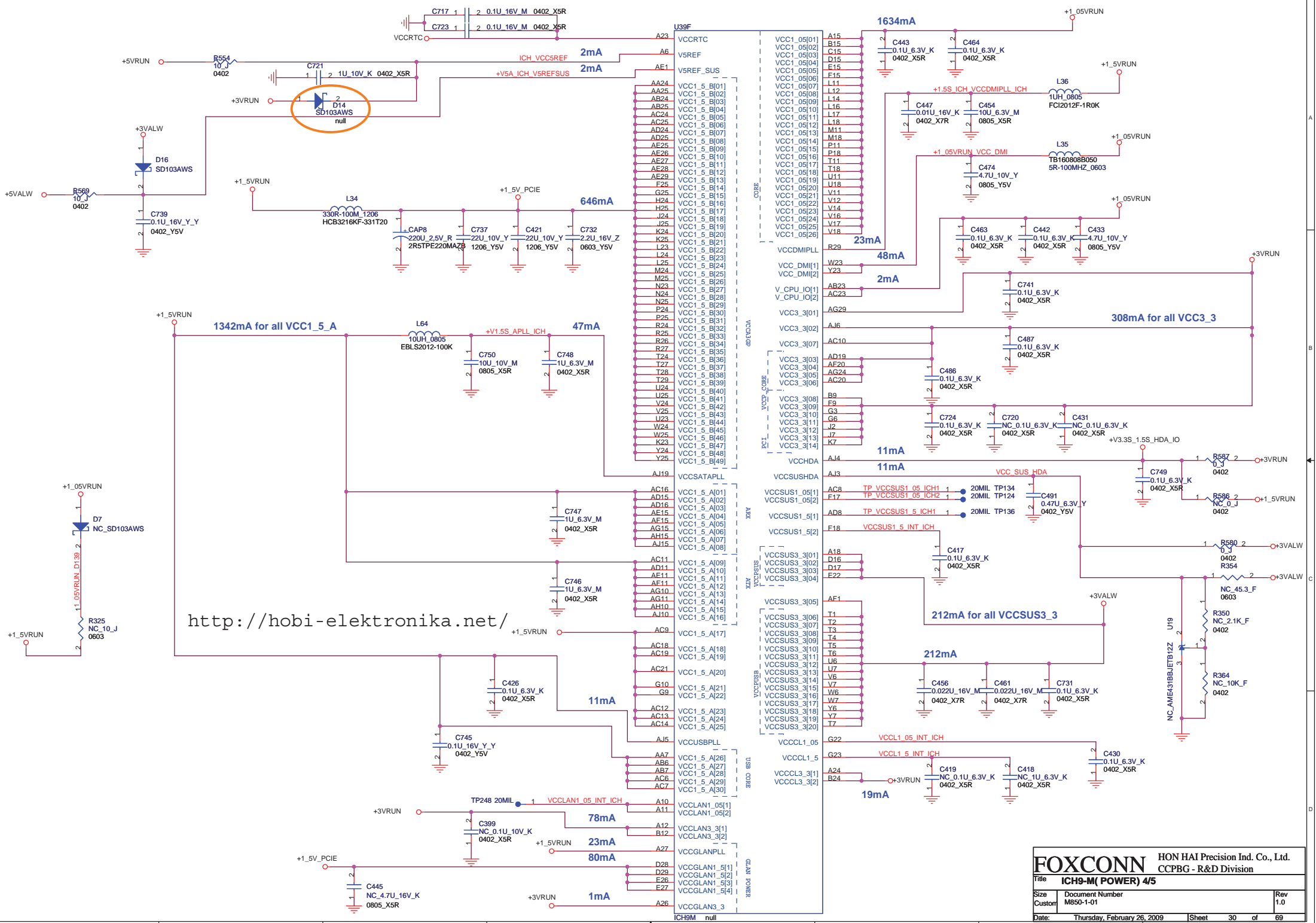
The traces inside this block should be wider.

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCl1_5, VccLAN1_05 and VccCl1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)



FWH0/LAD0	K5	LPC_ADO	LPC_ADO	33,34
FWH1/LAD1	K4	LPC_AD1	LPC_AD1	33,34
FWH2/LAD2	L6	LPC_AD2	LPC_AD2	33,34
FWH3/LAD3	K2	LPC_AD3	LPC_AD3	33,34
FWH4/LFRAME#	K3	LPC_FRAME#	LPC_FRAME#	33,34
LDRQ0#	J3	LPC_DRQ#0	LPC_DRQ#0	34
LDRQ1#/GPIO23	J1	20MIL TP128		
A20GATE	N7	H_A20GATE	H_A20GATE	33
A20M#	AJ27	H_A20M#	H_A20M#	3
DPRSTP#	AJ25	H_DPRSTP#	H_DPRSTP#	4,8,58
DPPLP#	AE23	H_DPPLP#	H_DPPLP#	4
FERR#	AJ26	H_FERR# R	H_FERR#	3
CPUPWRGD	AD22	H_PWRGD	H_PWRGD	4
IGNNE#	AE25	H_IGNNE#	H_IGNNE#	3
INIT#	AE22	H_INIT#	H_INIT#	3
INTR	AG25	H_INTR	H_INTR	3
RCIN#	L3	H_RCIN#	H_RCIN#	33
NMI	AE23	H_NMI	H_NMI	3
SMI#	AE24	H_SMI#	H_SMI#	3
STPCLK#	AH27	H_STPCLK#	H_STPCLK#	3
THRMTRIP#	AG26	PM_THRMTRIP# R	PM_THRMTRIP#	3,8,33
TP8	AG27	1	20MIL TP144	
SATA4RXN	AH11	SATA_RXN4 C	20MIL TP146	
SATA4RXP	AJ11	SATA_RXP4 C	20MIL TP149	
SATA4TXN	AG12	SATA_TXN4 C	20MIL TP142	
SATA4TXP	AE12	SATA_TXP4 C	20MIL TP140	
SATA5RXN	AH9	SATA_RXN5 C	20MIL TP147	
SATA5RXP	AJ9	SATA_RXP5 C	20MIL TP150	
SATA5TXN	AE10	SATA_TXN5 C	20MIL TP137	
SATA5TXP	AE10	SATA_TXP5 C	20MIL TP139	
SATA_CLKN	AH18	CLK_PCIE_SATA#	26MIL TP114	
SATA_CLKP	AJ18	CLK_PCIE_SATA	26MIL TP115	
SATARBIAS#	AJ7	SATARBIAS		
SATARBIAS	AH7	SATARBIAS R345	24.9 F	1 0402





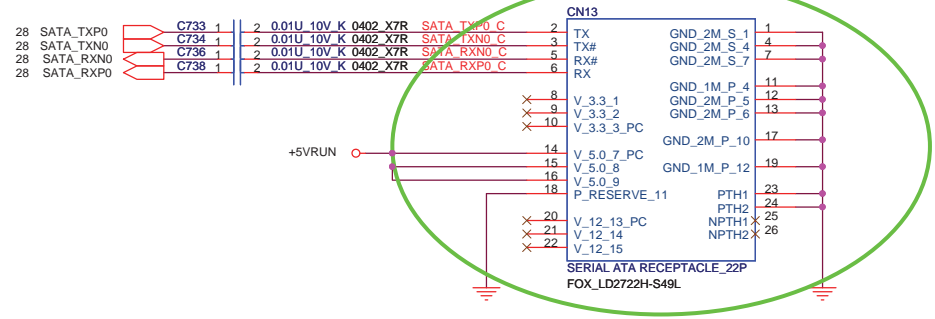
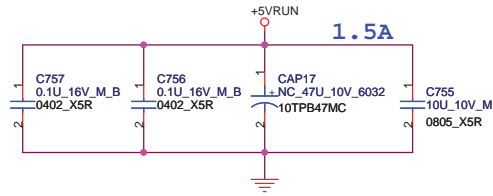
<http://hobi-elektronika.net/>

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		ICH9-M(POWER) 4/5	
Size	Document Number	Rev	
Custor	M850-1-01	1.0	
Date:	Thursday, February 26, 2009	Sheet	30 of 69

U39E		H5	
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	J26
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AA23	VSS[006]	VSS[112]	K29
AB28	VSS[007]	VSS[113]	L13
AB29	VSS[008]	VSS[114]	L15
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L5
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD5	VSS[026]	VSS[132]	N14
AD6	VSS[027]	VSS[133]	N15
AD7	VSS[028]	VSS[134]	N16
AD9	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE2	VSS[035]	VSS[141]	P14
AE20	VSS[036]	VSS[142]	P15
AE24	VSS[037]	VSS[143]	P16
AE3	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P23
AE9	VSS[041]	VSS[147]	P28
AF13	VSS[042]	VSS[148]	P29
AF16	VSS[043]	VSS[149]	P4
AF18	VSS[044]	VSS[150]	P7
AF22	VSS[045]	VSS[151]	R11
AH26	VSS[046]	VSS[152]	R12
AF26	VSS[047]	VSS[153]	R13
AF27	VSS[048]	VSS[154]	R14
AF5	VSS[049]	VSS[155]	R15
AF7	VSS[050]	VSS[156]	R16
AF9	VSS[051]	VSS[157]	R17
AG13	VSS[052]	VSS[158]	R19
AG18	VSS[053]	VSS[159]	R28
AG20	VSS[054]	VSS[160]	T12
AG23	VSS[055]	VSS[161]	T13
AG3	VSS[056]	VSS[162]	T14
AG6	VSS[057]	VSS[163]	T15
AG9	VSS[058]	VSS[164]	T16
AH12	VSS[059]	VSS[165]	T17
AH14	VSS[060]	VSS[166]	T23
AH17	VSS[061]	VSS[167]	B26
AH19	VSS[062]	VSS[168]	U12
AH2	VSS[063]	VSS[169]	U13
AH22	VSS[064]	VSS[170]	U14
AH25	VSS[065]	VSS[171]	U15
AH28	VSS[066]	VSS[172]	U16
AH5	VSS[067]	VSS[173]	U17
AH8	VSS[068]	VSS[174]	AD23
AJ12	VSS[069]	VSS[175]	U26
AJ14	VSS[070]	VSS[176]	U27
AJ17	VSS[071]	VSS[177]	U3
AJ8	VSS[072]	VSS[178]	V1
B11	VSS[073]	VSS[179]	V13
B14	VSS[074]	VSS[180]	V15
B17	VSS[075]	VSS[181]	V23
B2	VSS[076]	VSS[182]	V28
B20	VSS[077]	VSS[183]	V29
B23	VSS[078]	VSS[184]	V4
B5	VSS[079]	VSS[185]	V5
B8	VSS[080]	VSS[186]	W26
C26	VSS[081]	VSS[187]	W27
C27	VSS[082]	VSS[188]	W3
E11	VSS[083]	VSS[189]	Y1
E14	VSS[084]	VSS[190]	Y28
E18	VSS[085]	VSS[191]	Y29
E2	VSS[086]	VSS[192]	Y4
E21	VSS[087]	VSS[193]	Y5
E24	VSS[088]	VSS[194]	AG28
E5	VSS[089]	VSS[195]	AH6
E8	VSS[090]	VSS[196]	AF2
F18	VSS[091]	VSS[197]	B25
F28	VSS[092]	VSS[198]	
F29	VSS[093]		A1
G12	VSS[094]	VSS_NCTF[01]	A2
G14	VSS[095]	VSS_NCTF[02]	A28
G18	VSS[096]	VSS_NCTF[03]	A29
G21	VSS[097]	VSS_NCTF[04]	AH1
G24	VSS[098]	VSS_NCTF[05]	AH29
G26	VSS[099]	VSS_NCTF[06]	AJ1
G27	VSS[100]	VSS_NCTF[07]	AJ2
G8	VSS[101]	VSS_NCTF[08]	AJ28
H2	VSS[102]	VSS_NCTF[09]	AJ29
H23	VSS[103]	VSS_NCTF[10]	B1
H28	VSS[104]	VSS_NCTF[11]	B29
H29	VSS[105]	VSS_NCTF[12]	
	VSS[106]		

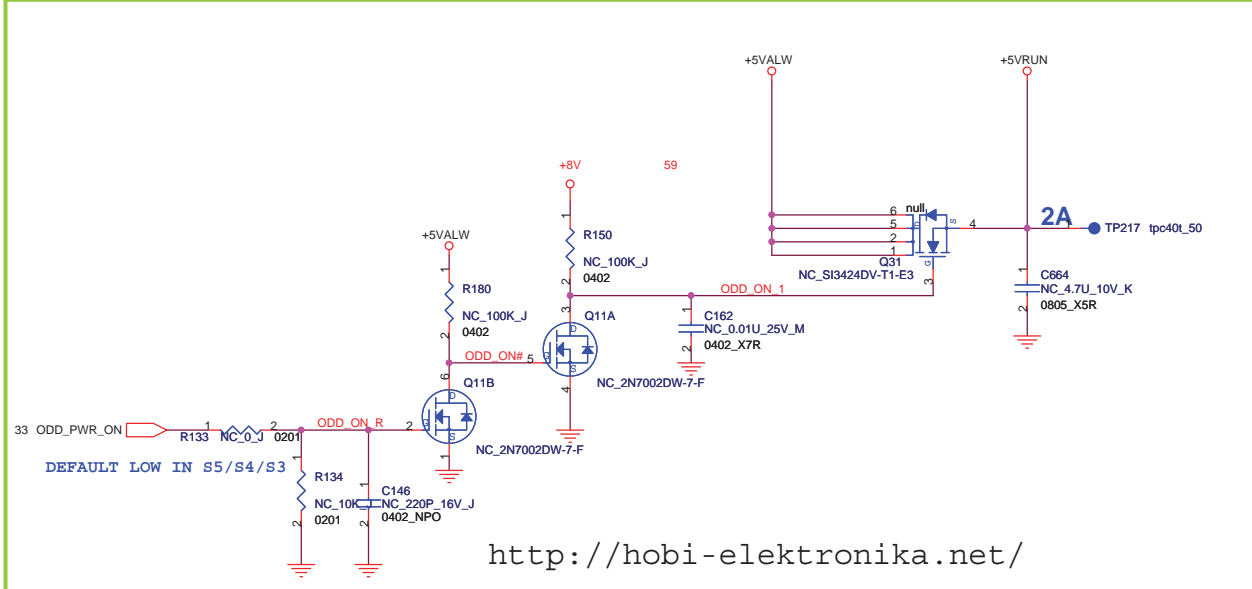
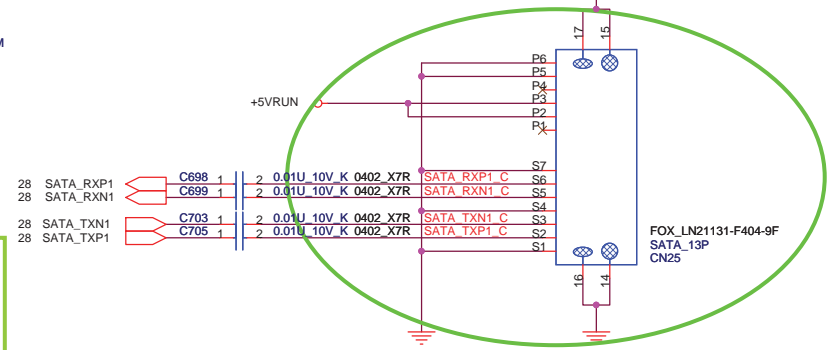
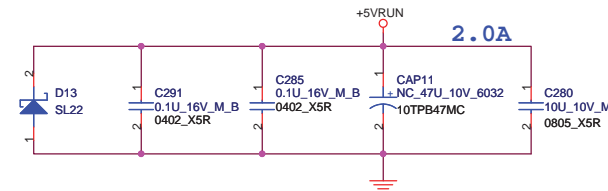
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>ICH9-M( GND) 5/5</b>			
Size	Document Number	Rev	
A3	M850-1-01	1.0	
Date:	Thursday, February 26, 2009	Sheet	31 of 69

# SATA HDD CONN



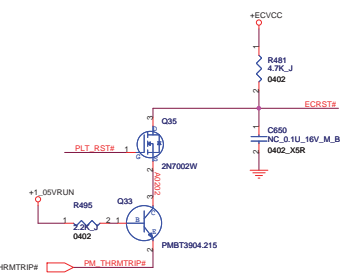
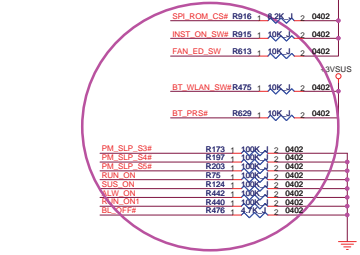
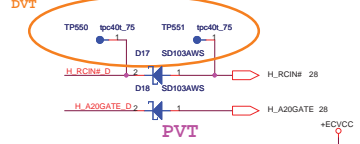
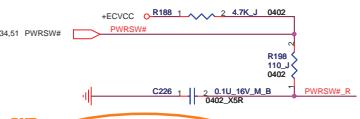
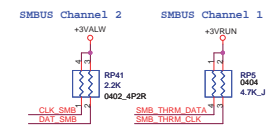
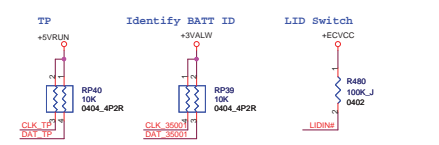
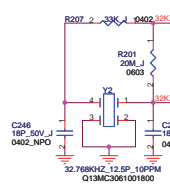
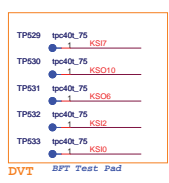
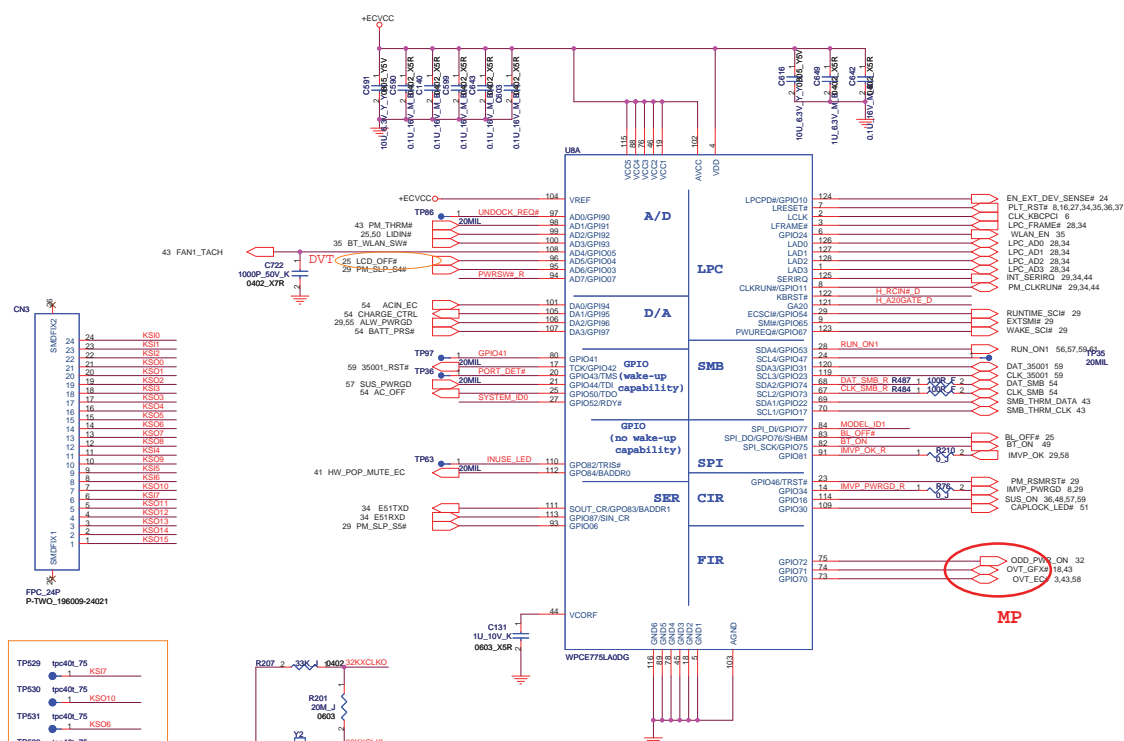
EVT

# SATA ODD CONN



<http://hobi-elektronika.net/>

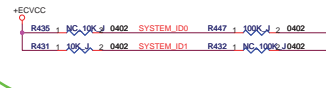
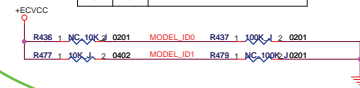


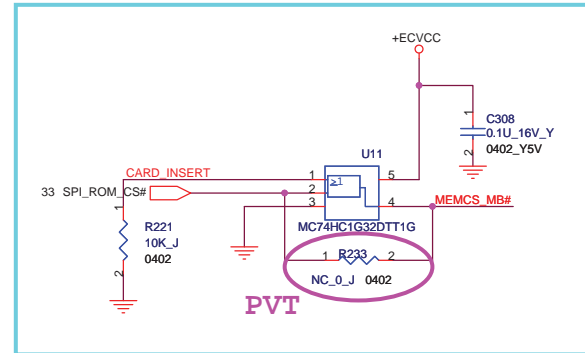
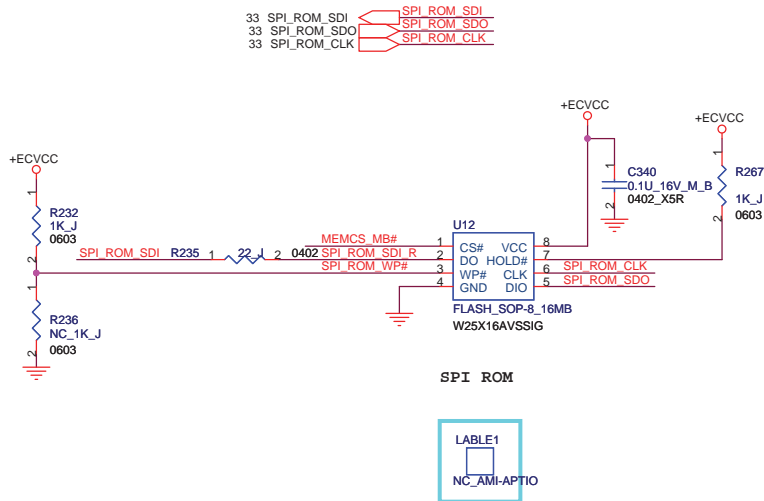


**M851 DVT2**

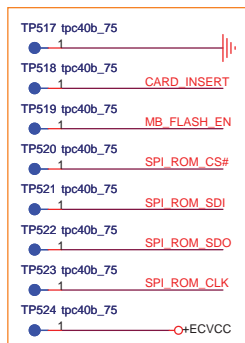
ID1	ID0	Model
1	0	H (PM45+Ext GEX)
1	1	M (GM45+Ext GEX)
0	1	M (GM45+Int GEX)
0	0	L (GL40)

ID1	ID0	System
1	0	M851_DDR2
0	1	M851_DDR3

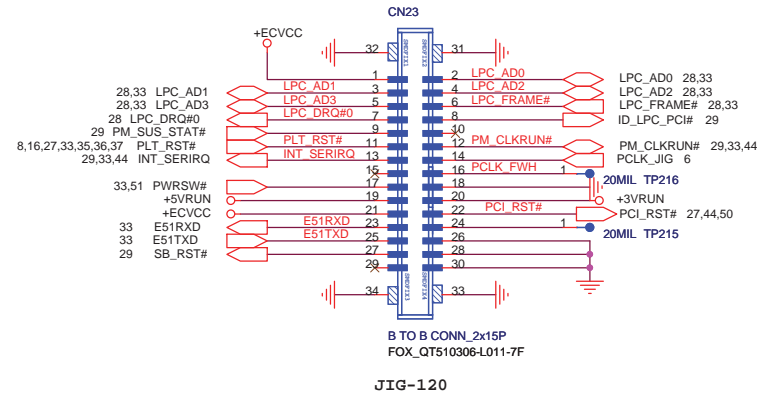
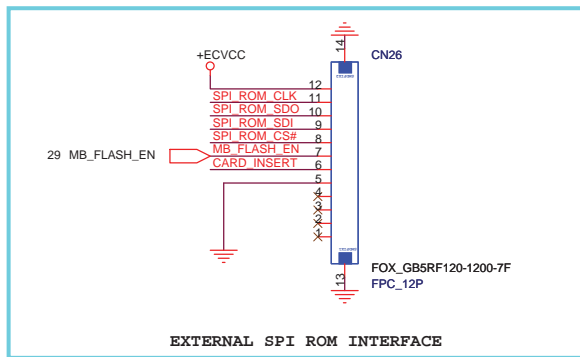


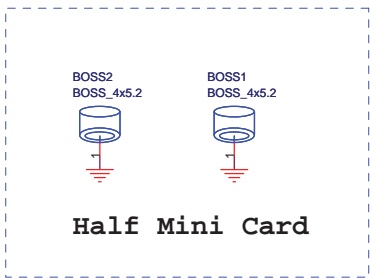


<http://hobi-elektronika.net/>



DVT BFT Test Pad

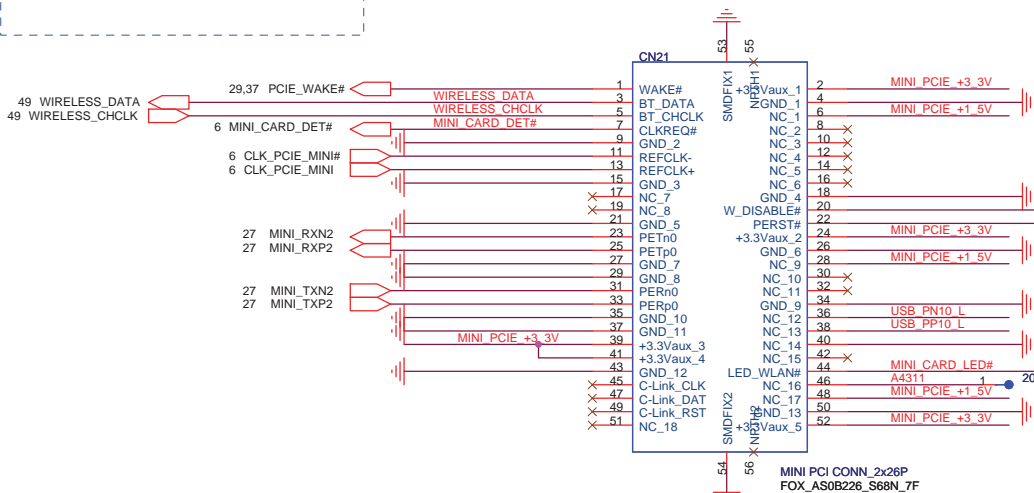
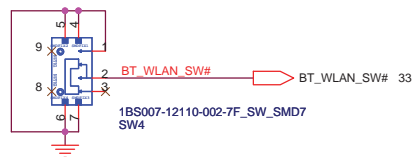




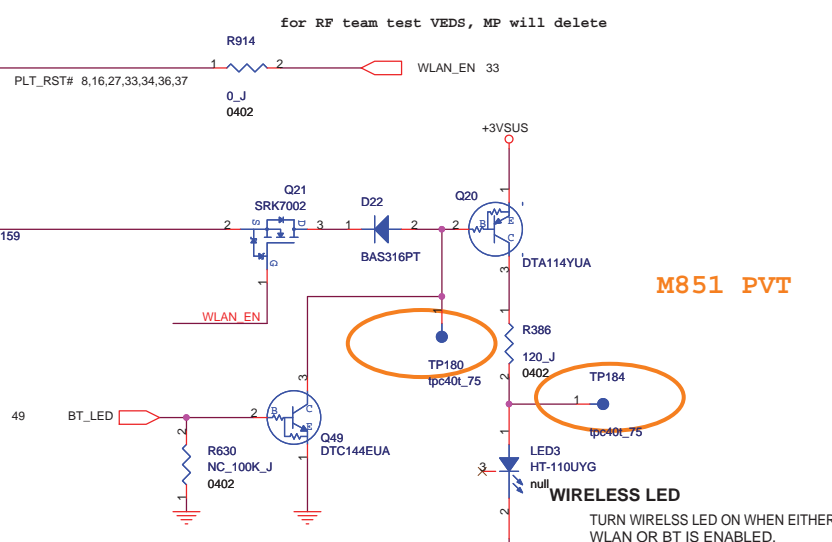
Half Mini Card

+1\_5V=>0.5A Peak/0.375A Normal  
 +3\_3VAux=>2.75A Peak/1.1A Normal

WLAN ON/OFF Switch



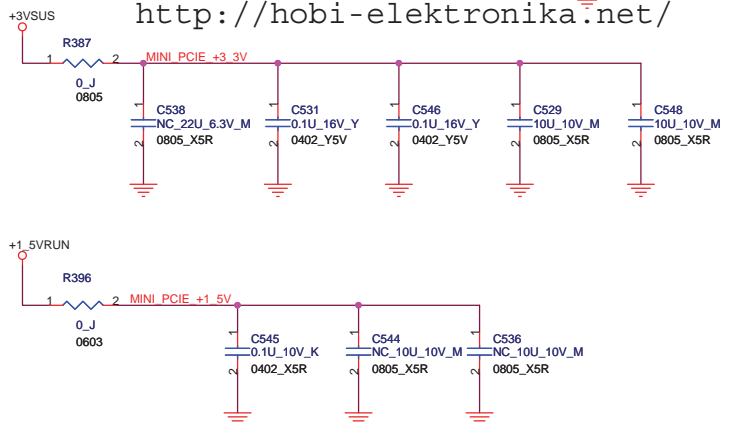
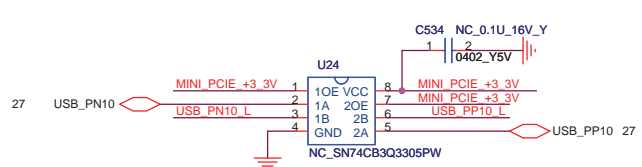
Half Mini Card  
WLAN



M851 PVT

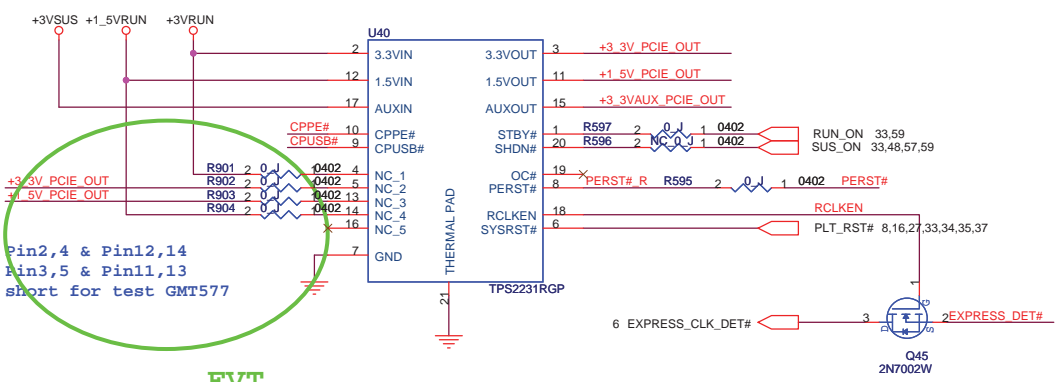
WIRELESS LED  
 TURN WIRELESS LED ON WHEN EITHER  
 WLAN OR BT IS ENABLED.

<http://hobi-elektronika.net/>

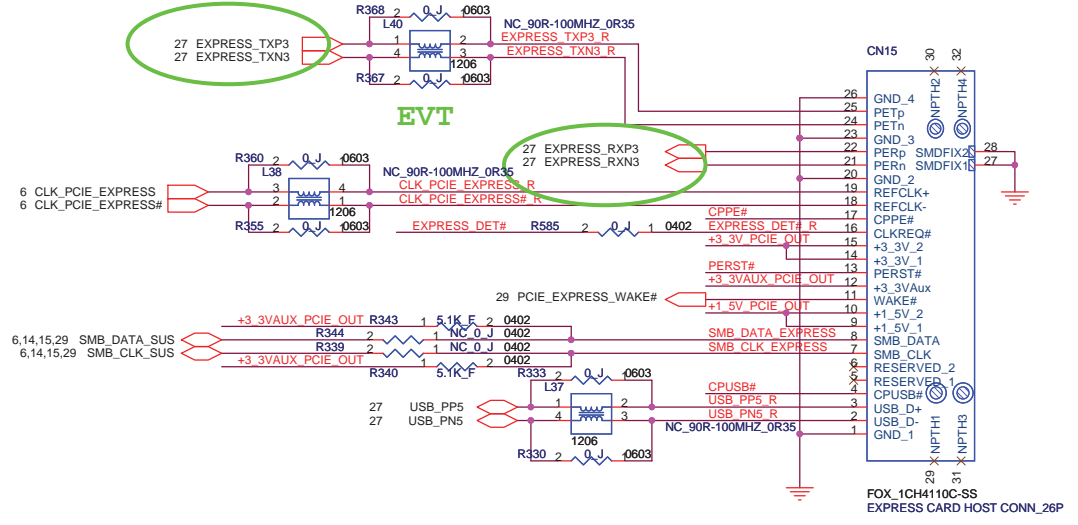


+1\_5V=>1.3A  
 +3\_3VAux=>0.6A  
 +3\_3V=>2.5A

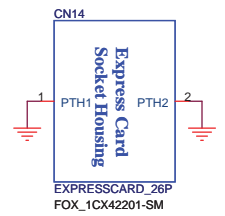
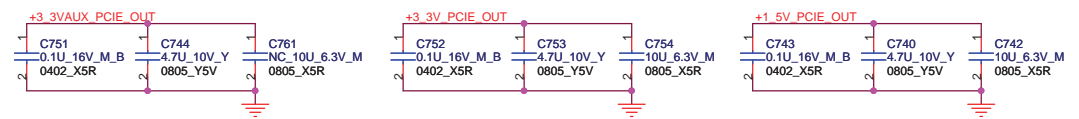
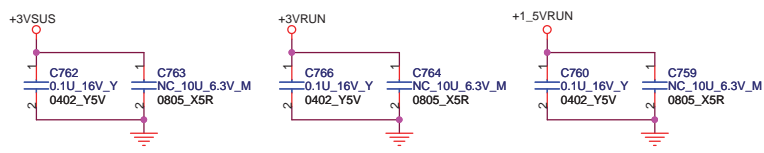
Express Card Power Switch

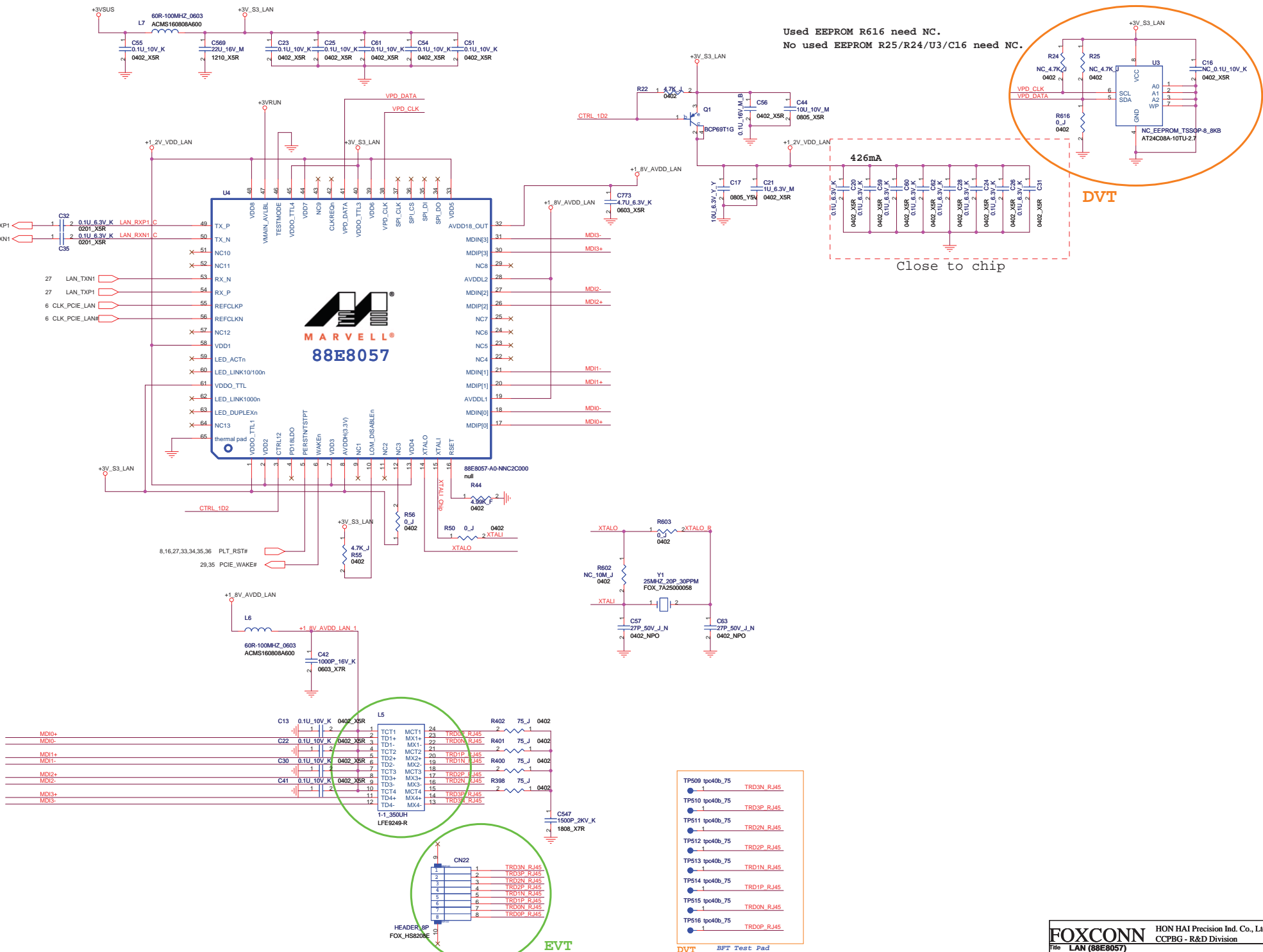


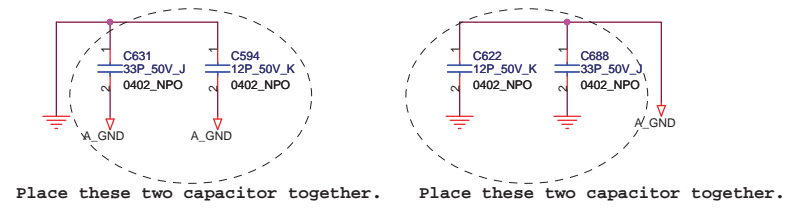
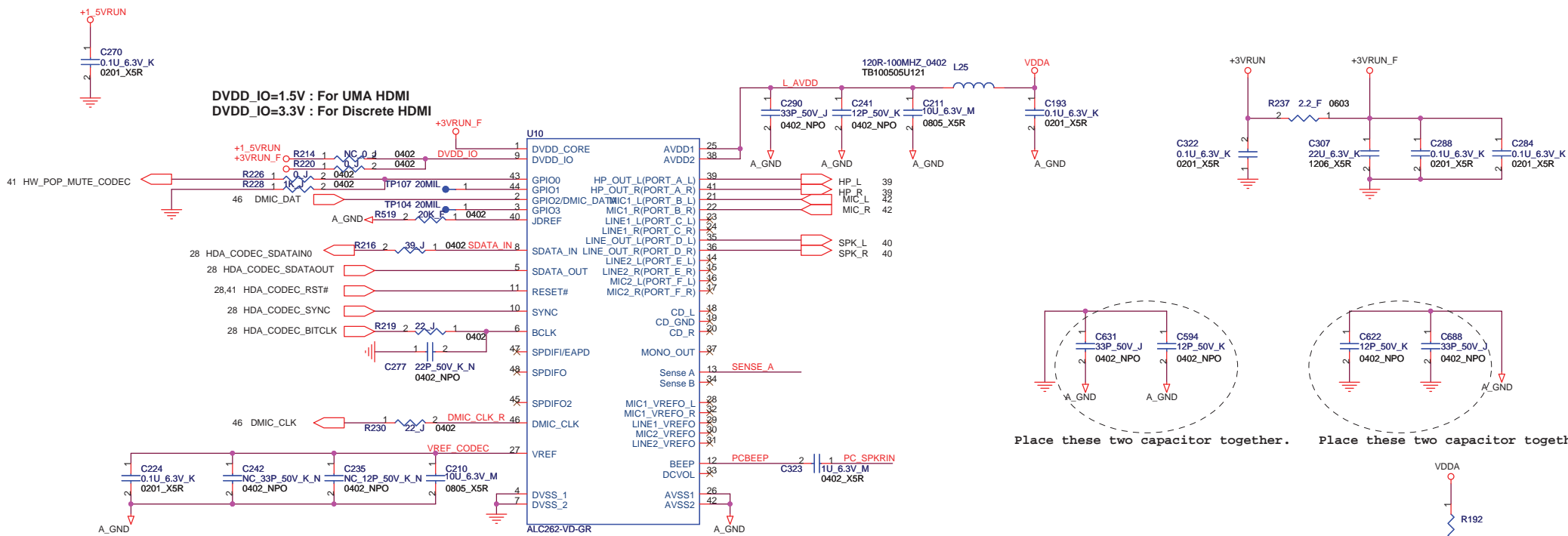
EVT



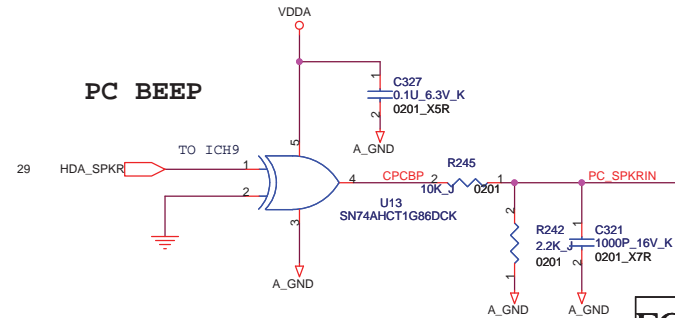
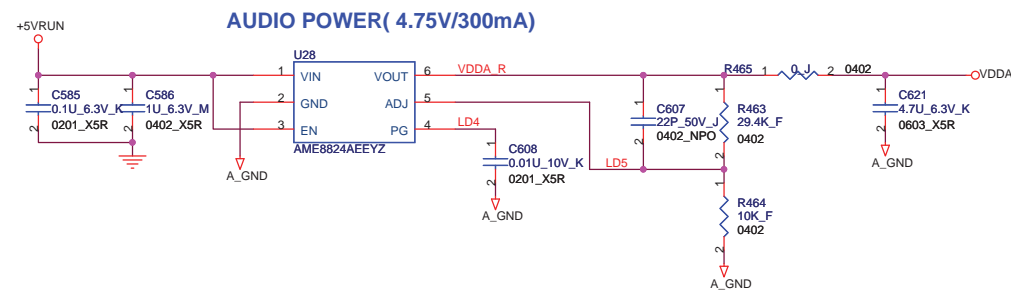
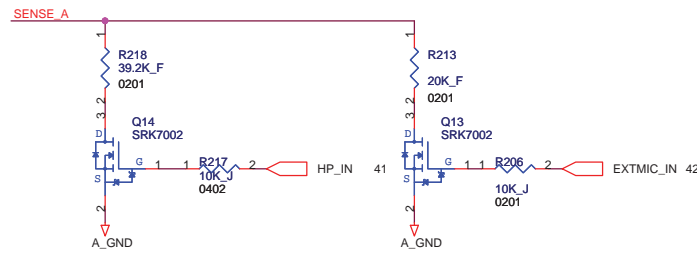
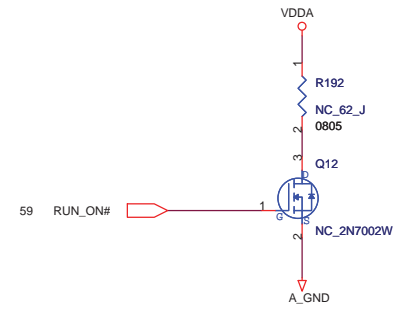
Express Card Slot.



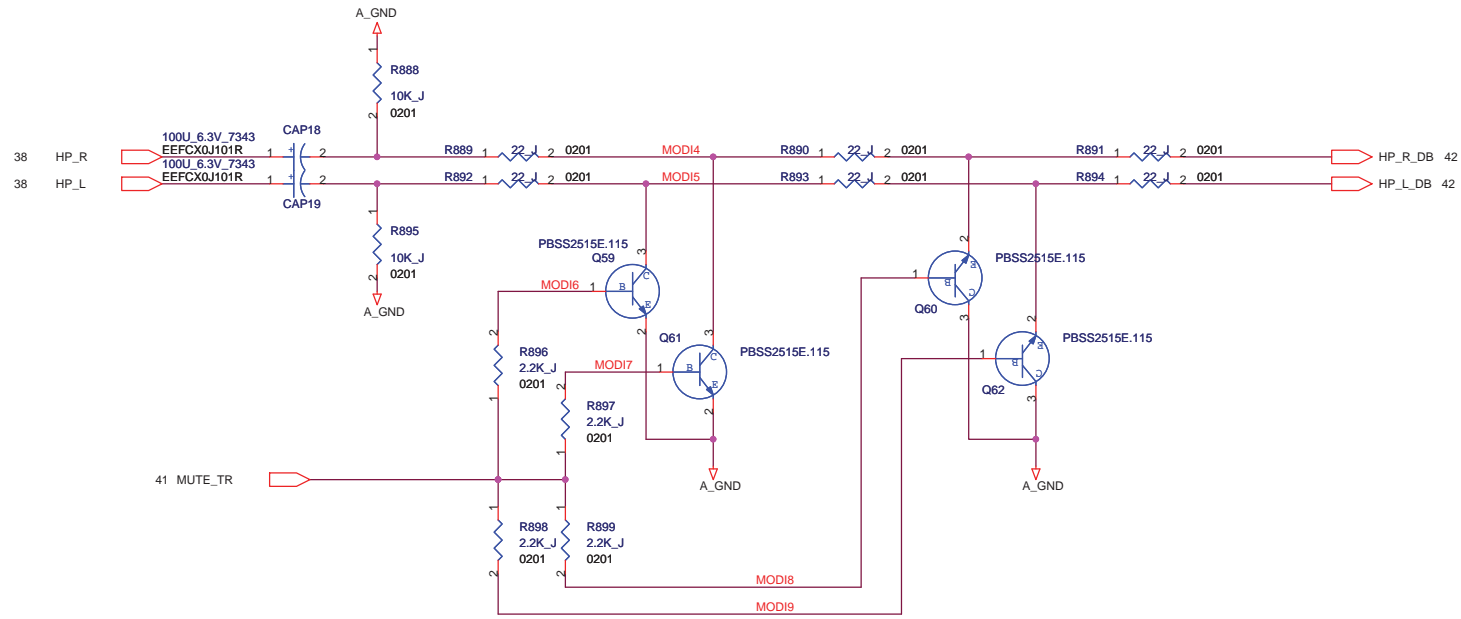


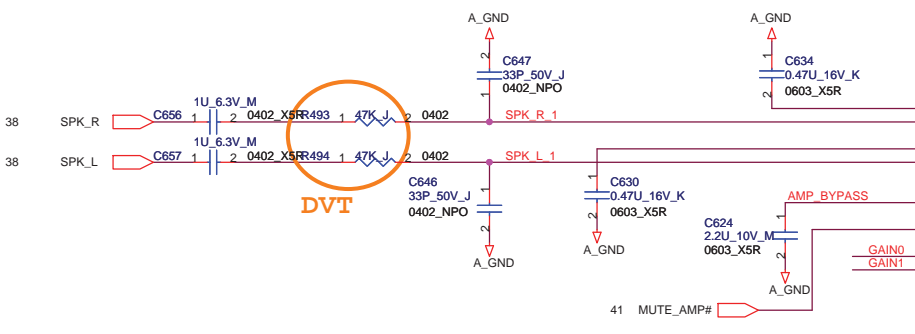
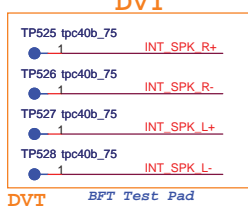
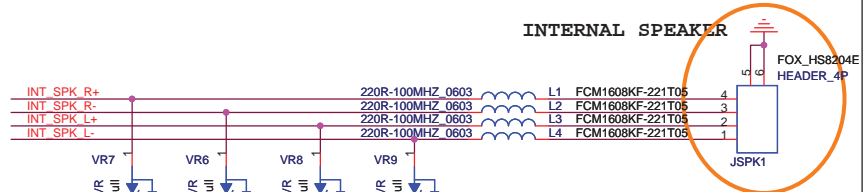
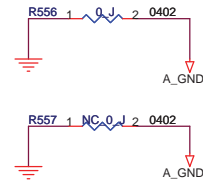
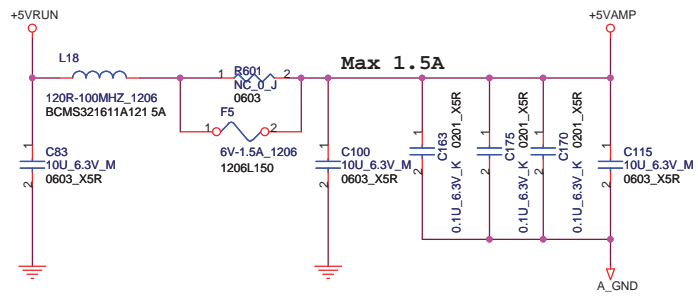


<http://hobi-elektronika.net/>

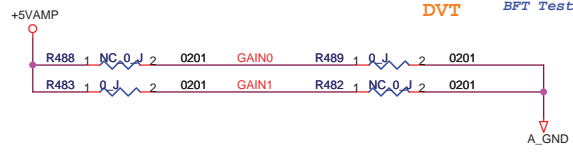
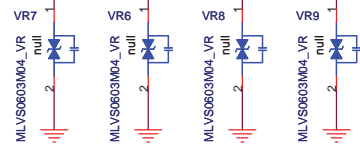
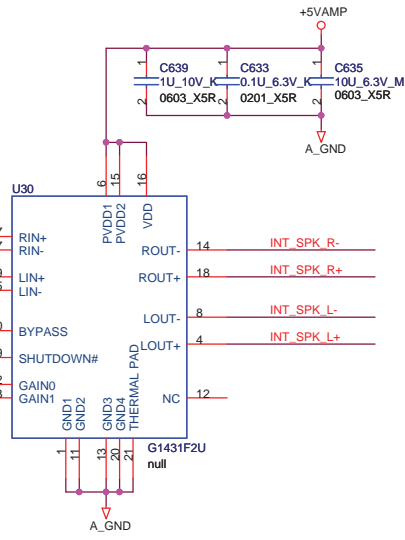






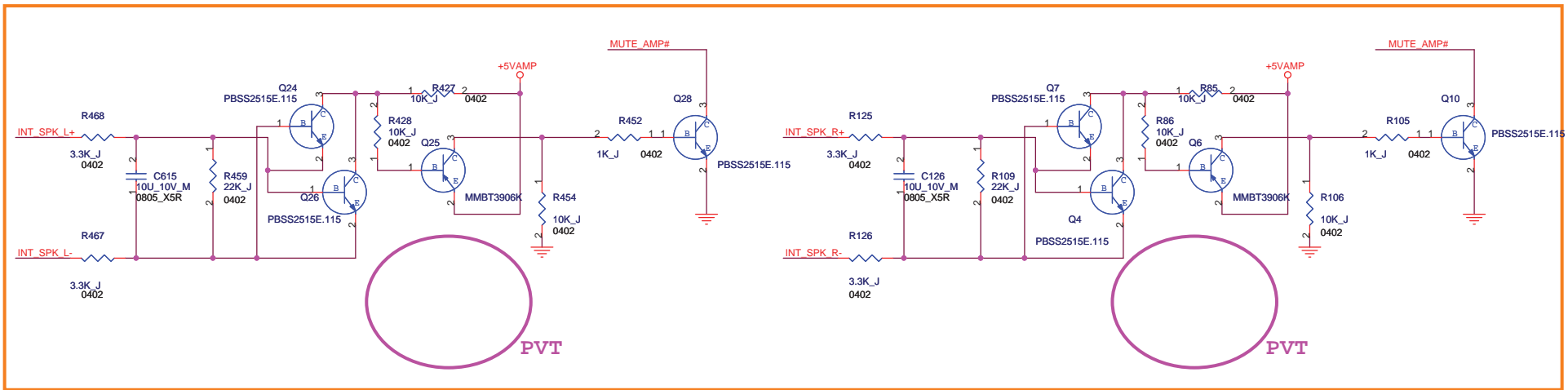


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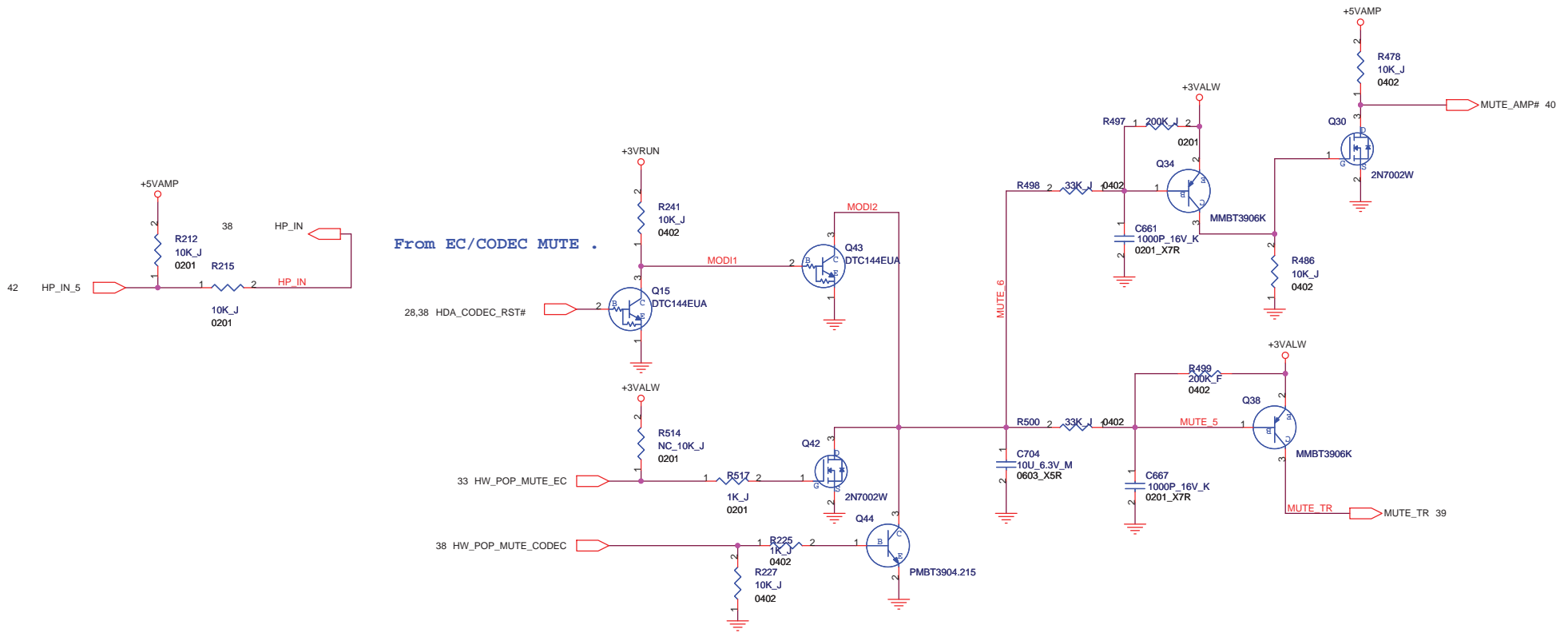


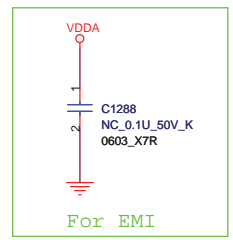
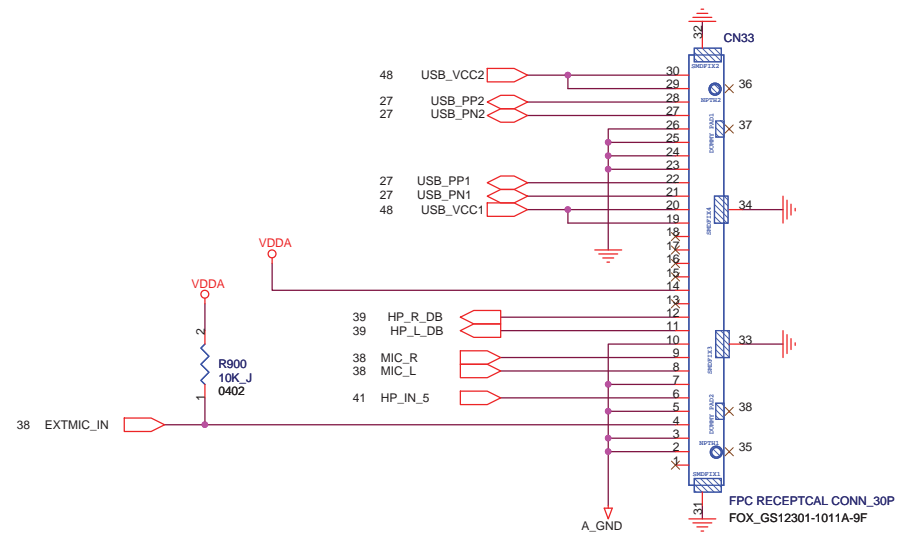
**SPEAKER AMP**

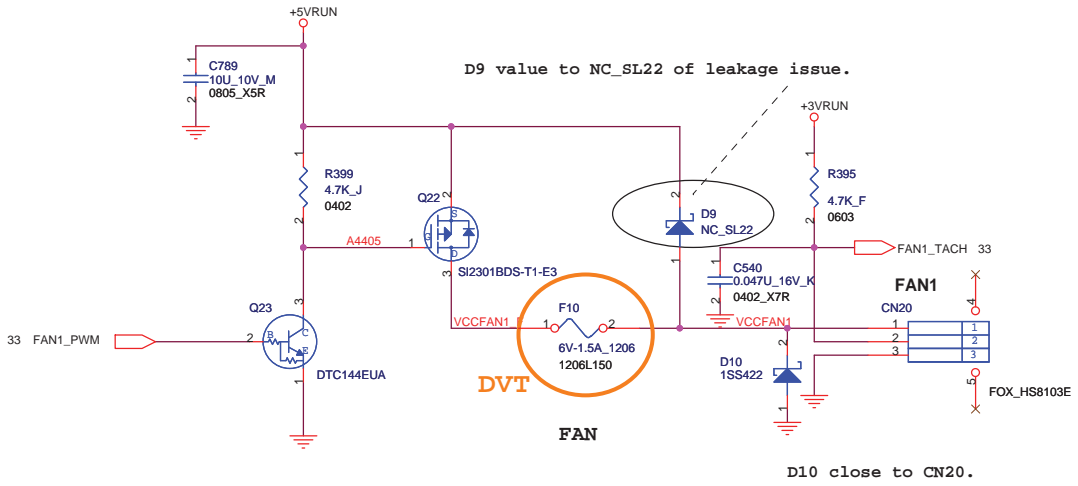
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10 dB	0	1
15.6 dB	1	0
21.6 dB	1	1



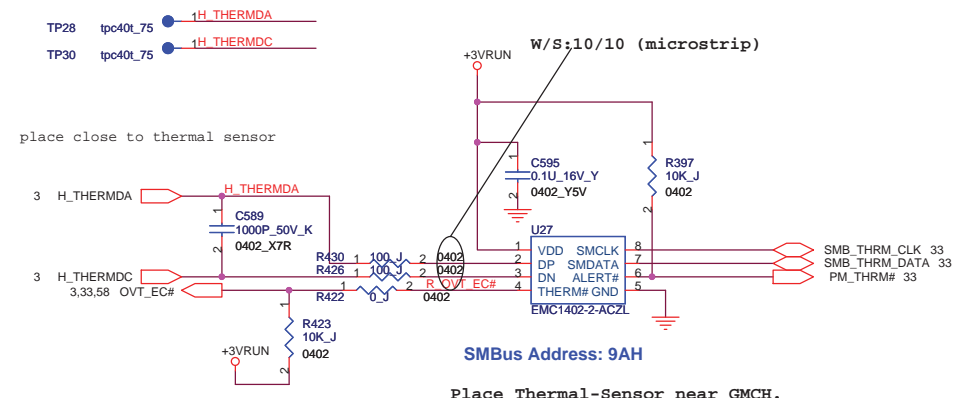
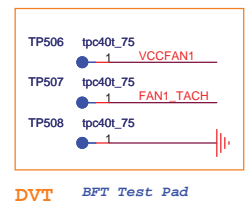
For Mor request, add the speaker cable short protection circuit



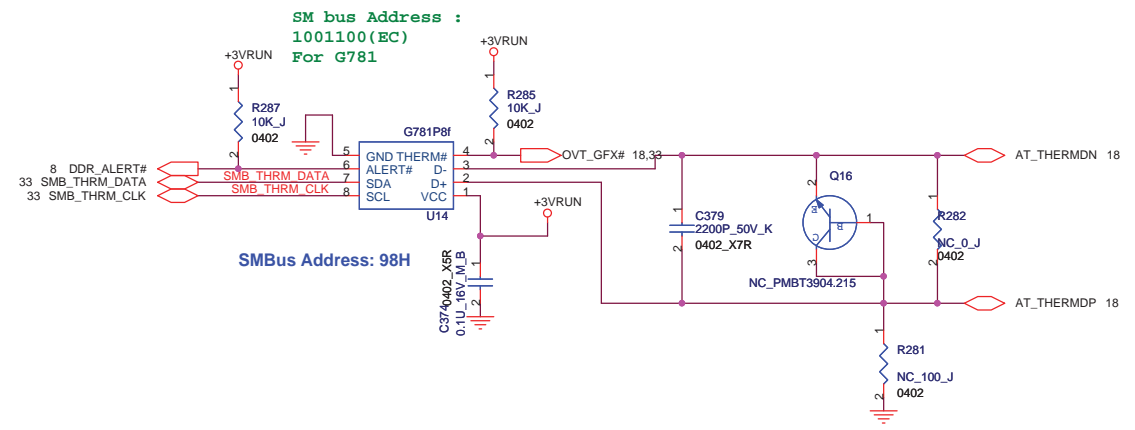


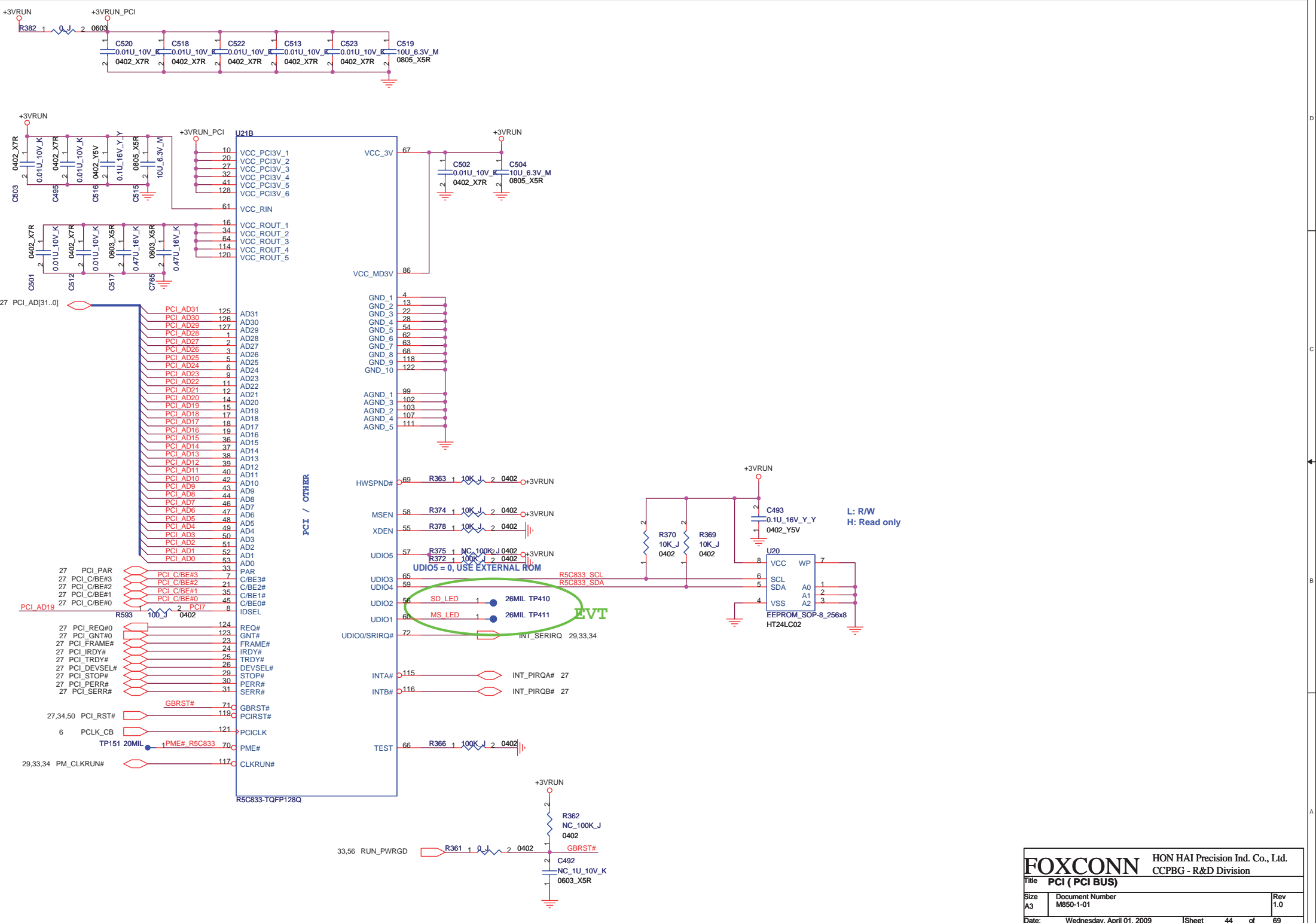


**DVT**  
6V-1.5A\_1206  
1206L150



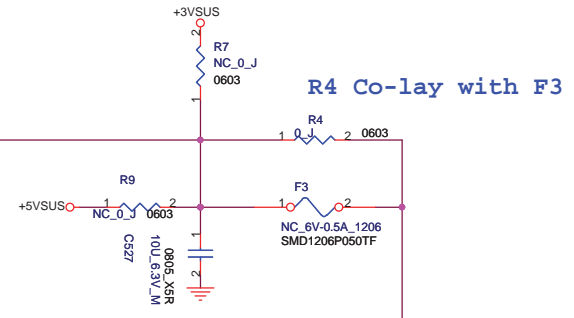
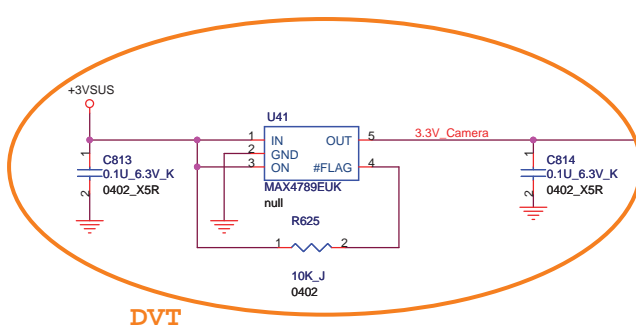
**CPU Thermal-Sensor**



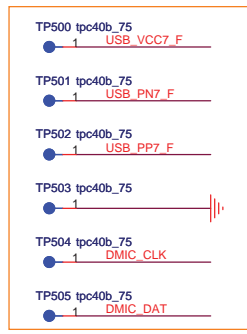
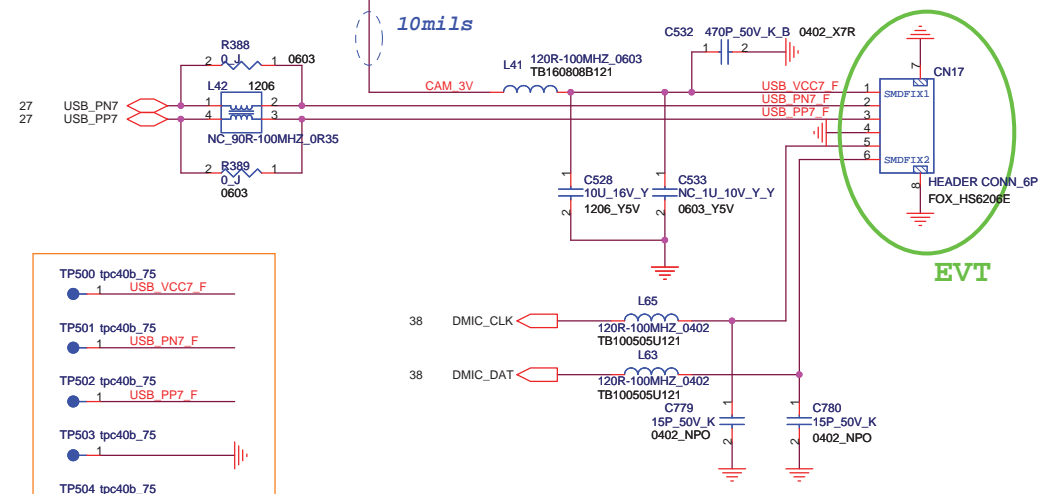




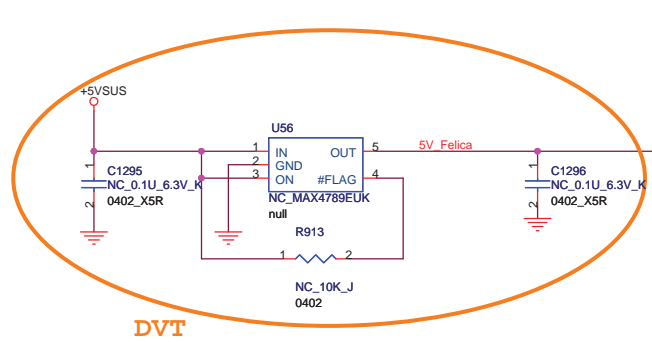




### CAMERA Connector



### Int MIC Connector



DVT

+5VSUS

R912  
0\_J  
0603

R622  
NC\_0\_J  
0603

F6  
10V-0.125A\_1206  
1206L012

PVT

10mils

L27  
120R-100MHZ\_0603  
TB160808B121

28 USB\_PN8  
27 USB\_PP8

R527 2  
R528 2

0603  
0603

C279  
22U\_10V\_Y\_Y  
1206\_Y5V

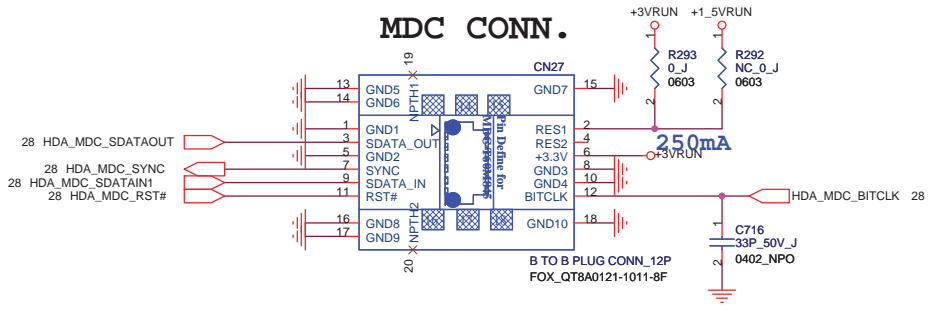
C282  
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0603\_Y5V

USB\_VCC8\_F  
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Felica CONN.

DVT

CN6  
FFC\_6P  
FOX\_GB5RF060-1200-7F



MDC CONN.

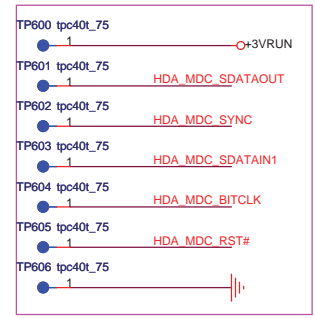
+3VRUN +1\_5VRUN

R293 0\_J  
R292 0\_J  
0603 0603

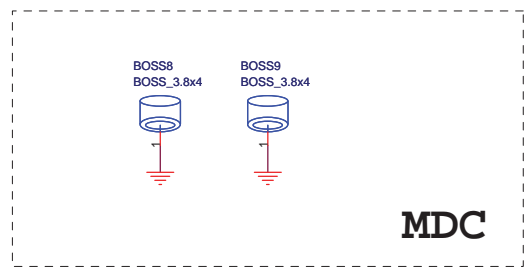
250mA

C716  
33P\_50V\_J  
0402\_NPO

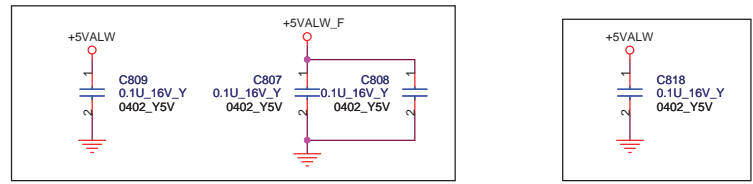
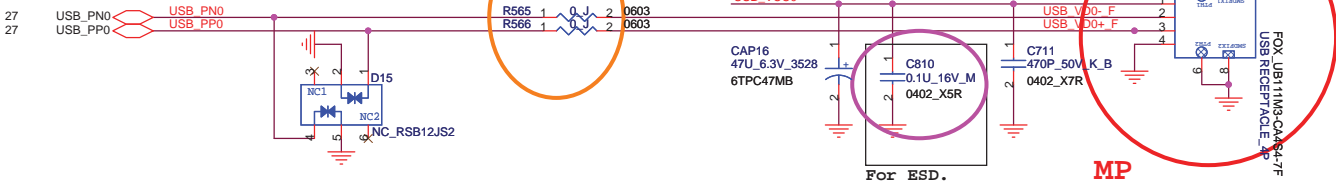
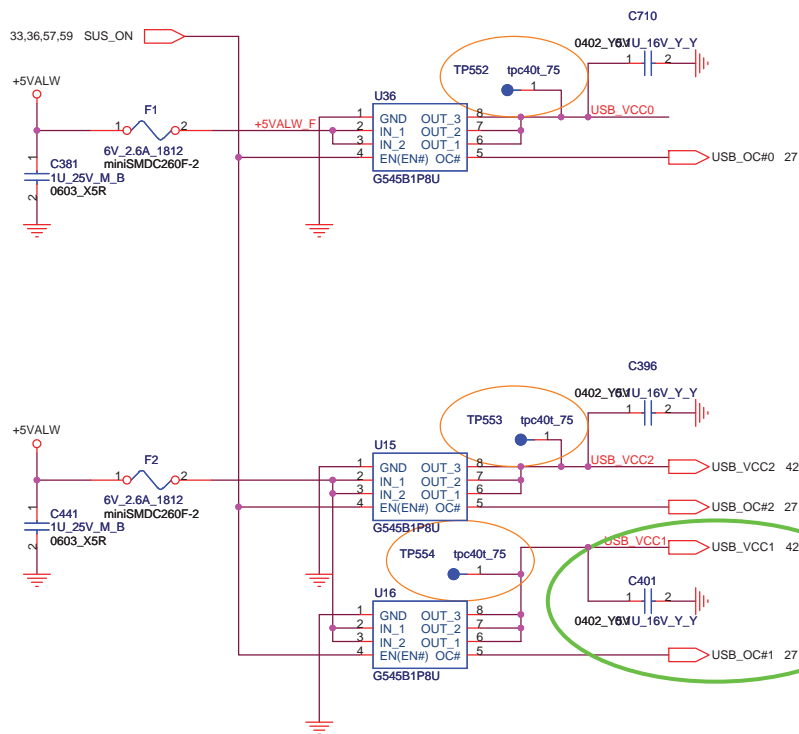
B TO B PLUG CONN\_12P  
FOX\_QT8A0121-1011-8F



PVT BFT Test Pad



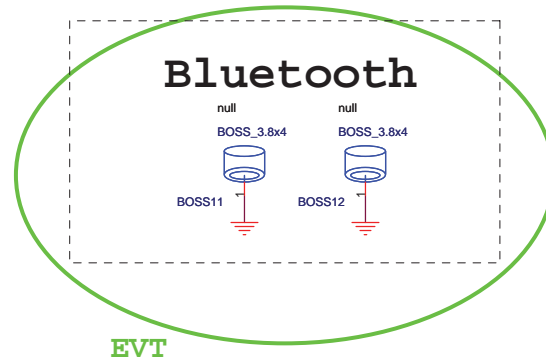
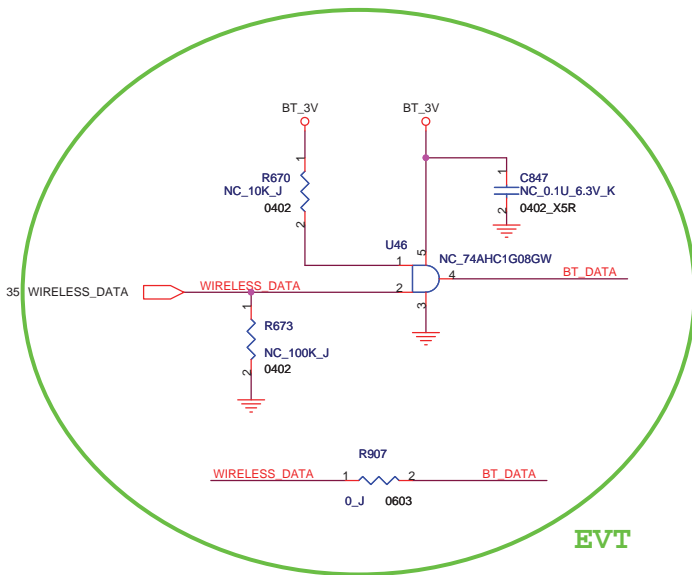
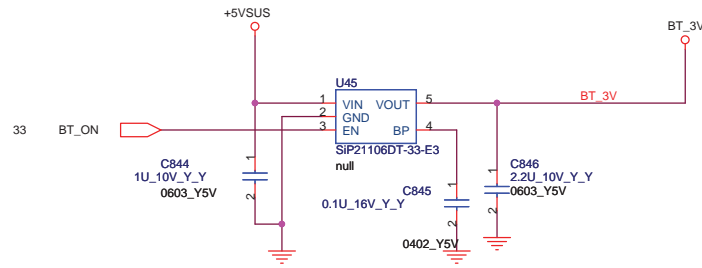
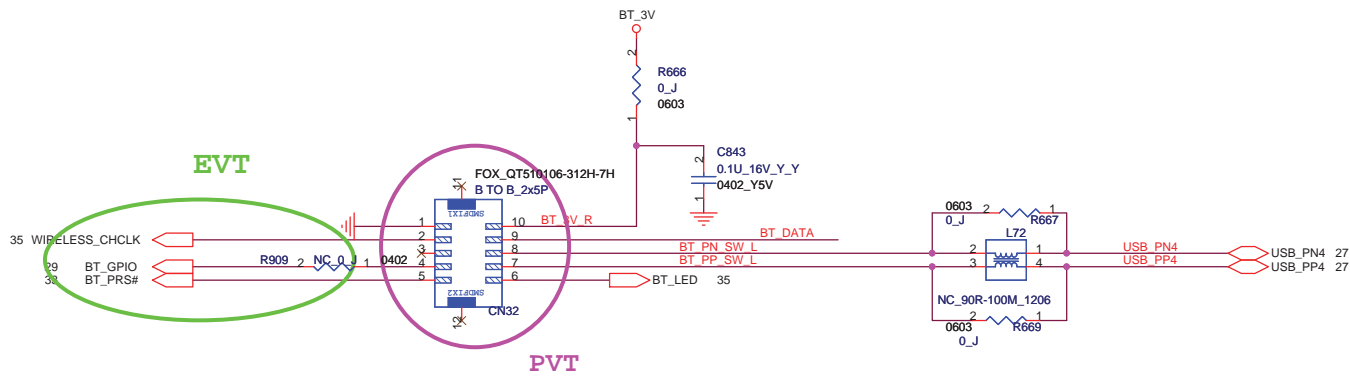
MDC

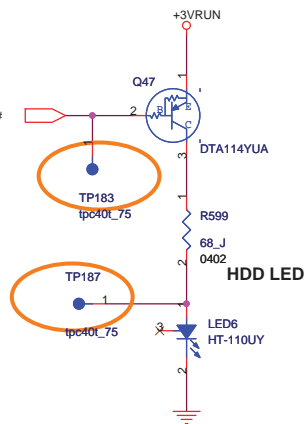
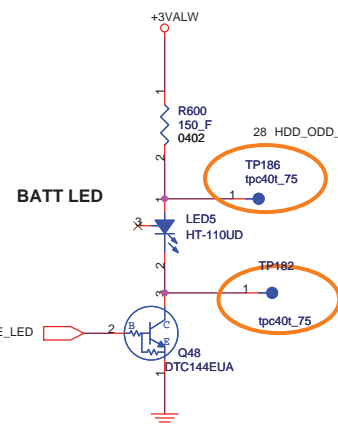
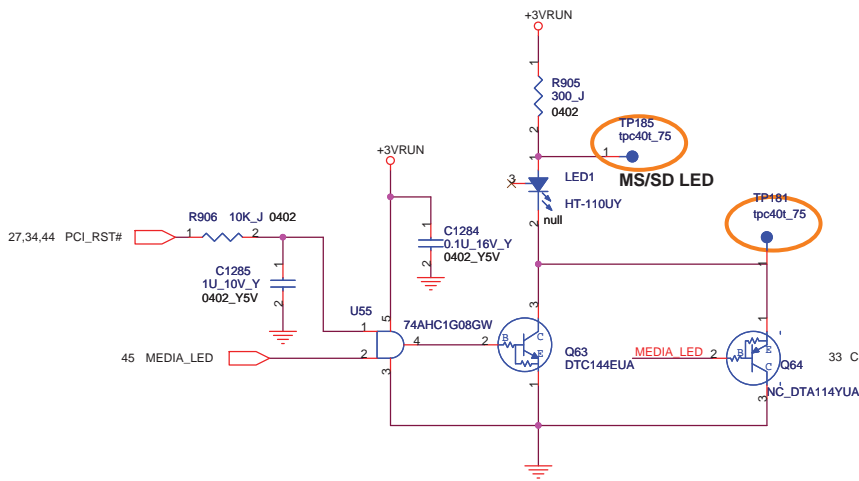


For ESD.

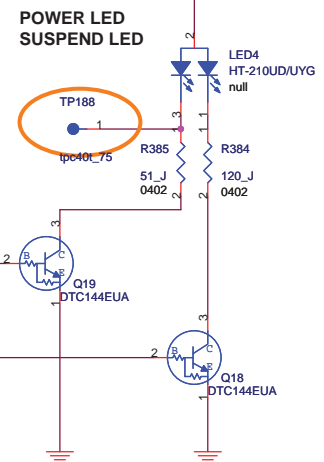
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>USB2.0</b>		CCPBG - R&D Division	
Size A3	Document Number M850-1-01	Rev 1.0	
Date: Wednesday, April 08, 2009	Sheet 48	of 69	

# Bluetooth connector



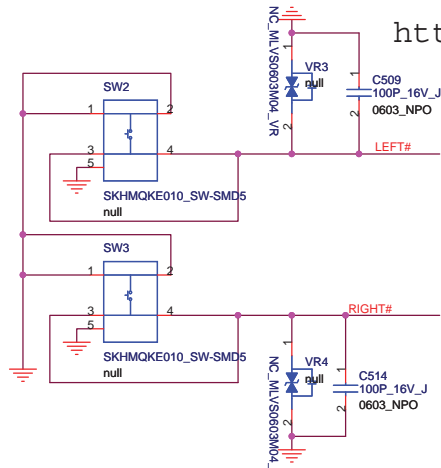


**M851 PVT**

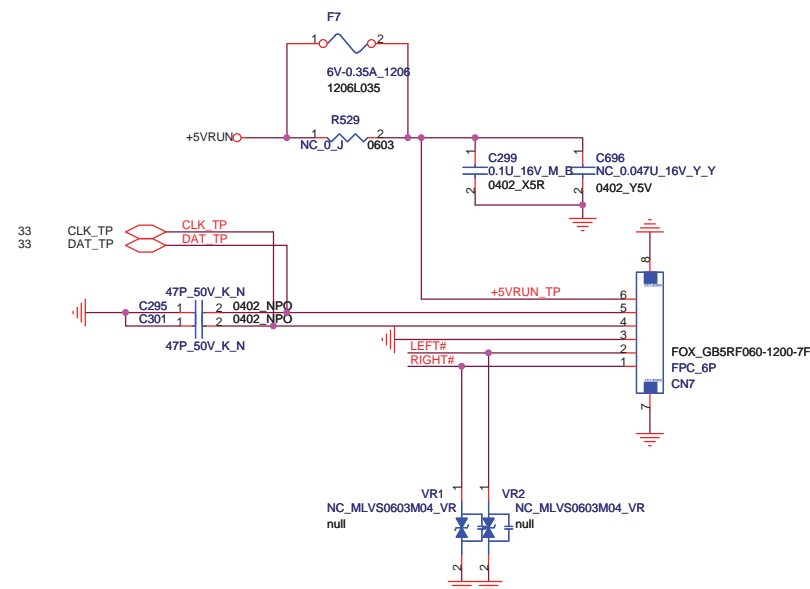


**TP\_LEFT Button**

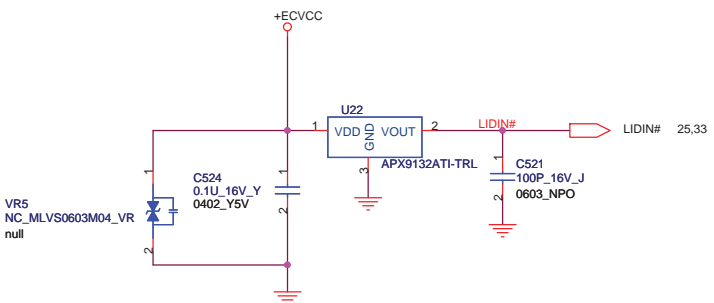
<http://hobi-elektronika.net/>



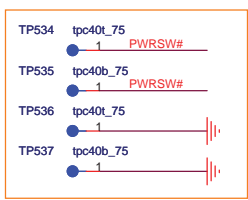
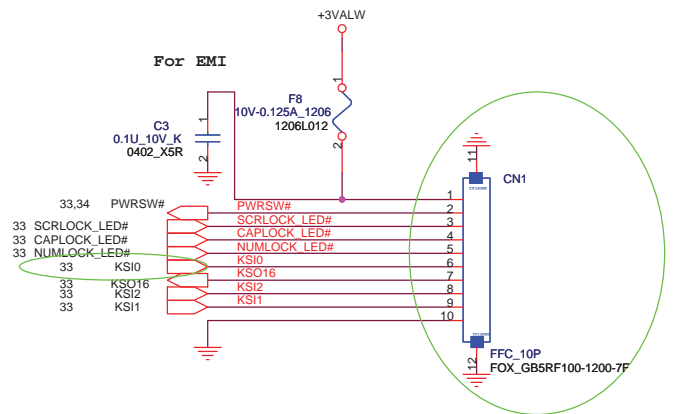
**TP\_Right Button**



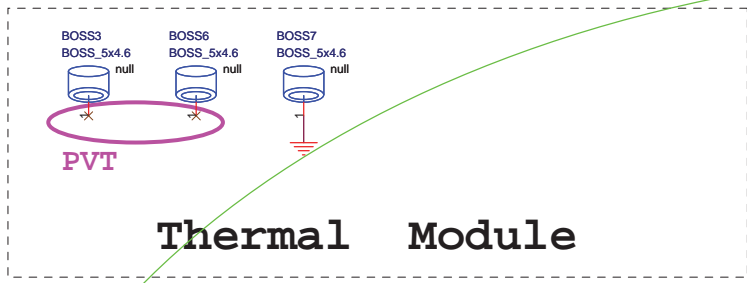
**LID Switch**



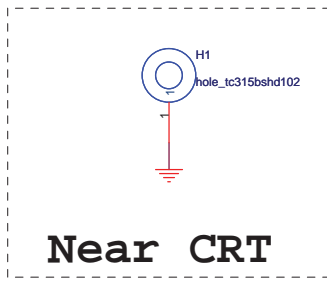




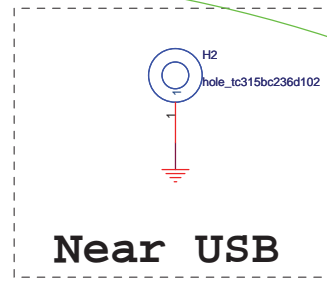
DVT BFT Test Pad



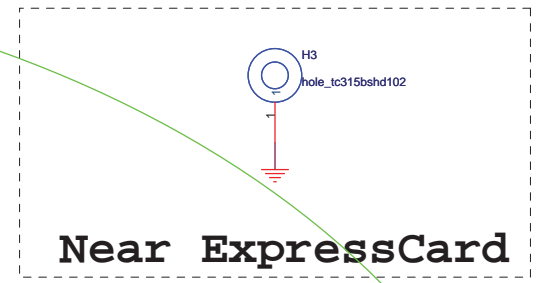
**Thermal Module**



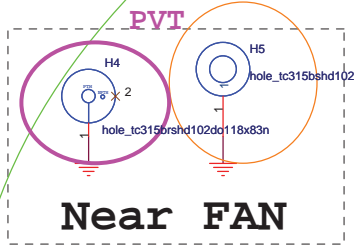
**Near CRT**



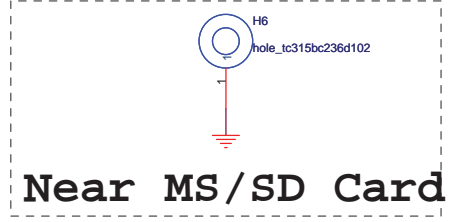
**Near USB**



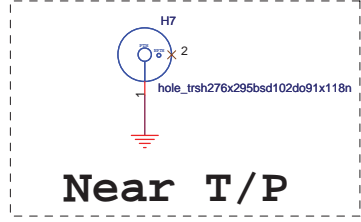
**Near ExpressCard**



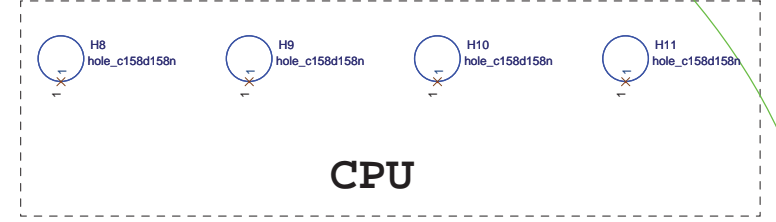
**Near FAN**



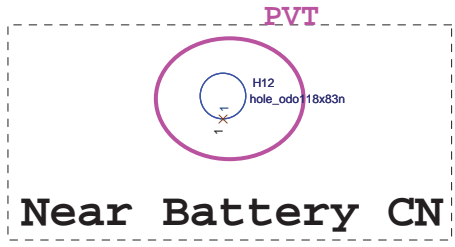
**Near MS/SD Card**



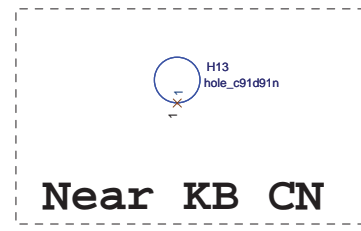
**Near T/P**



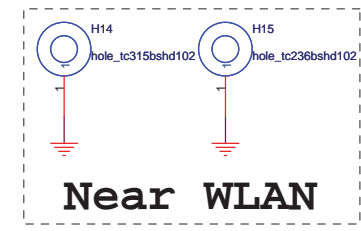
**CPU**



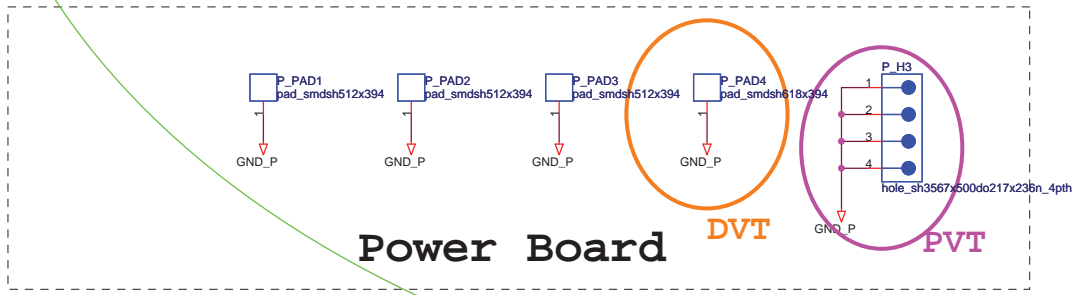
**Near Battery CN**



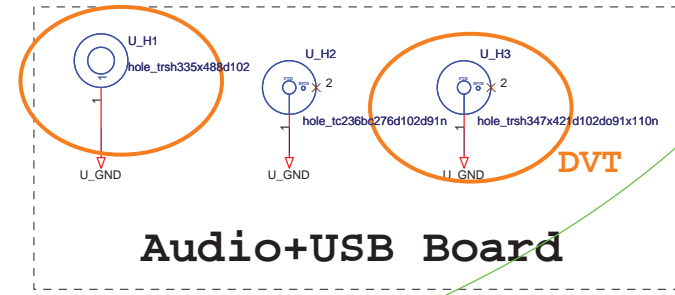
**Near KB CN**



**Near WLAN**



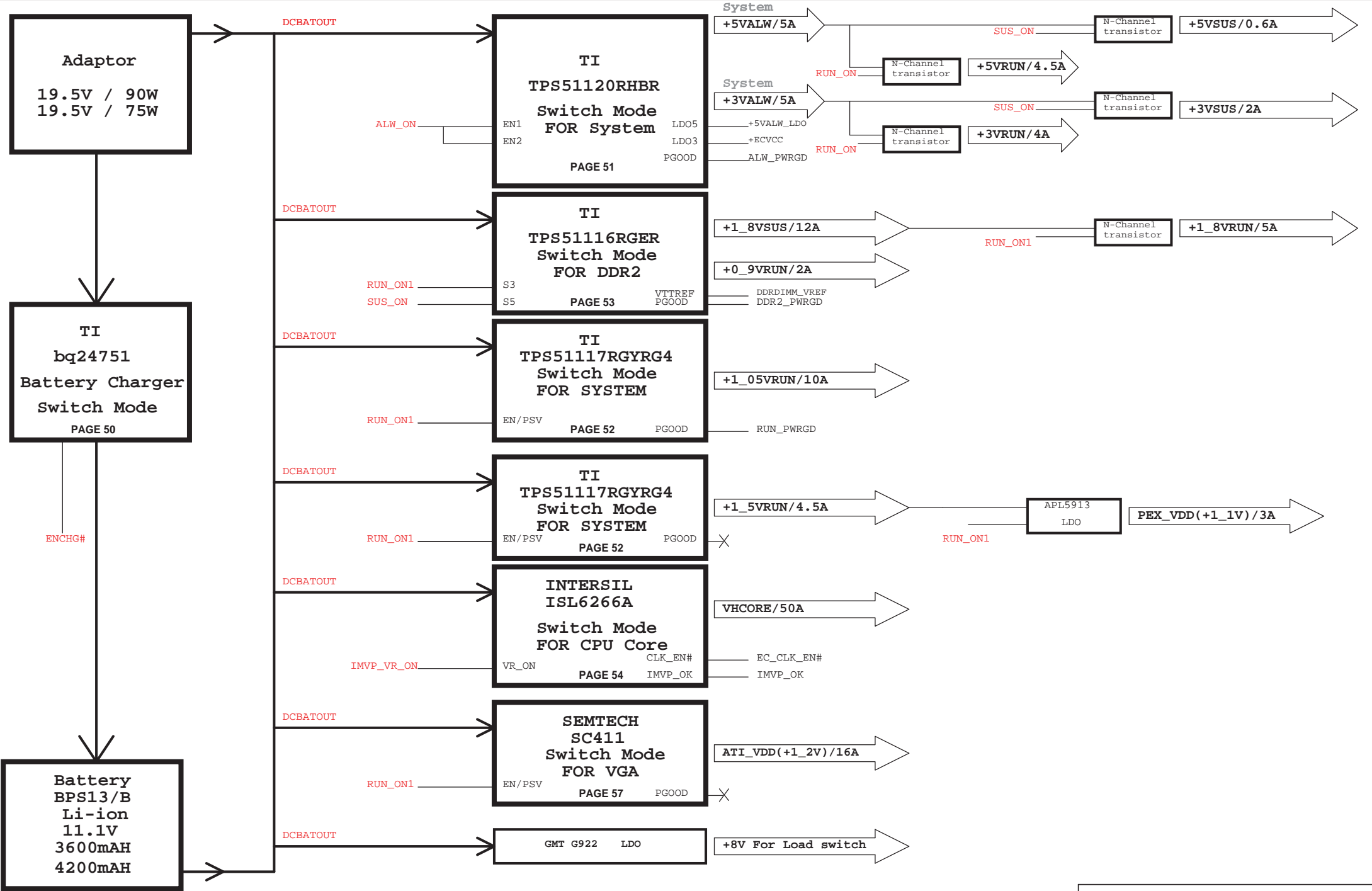
**Power Board**

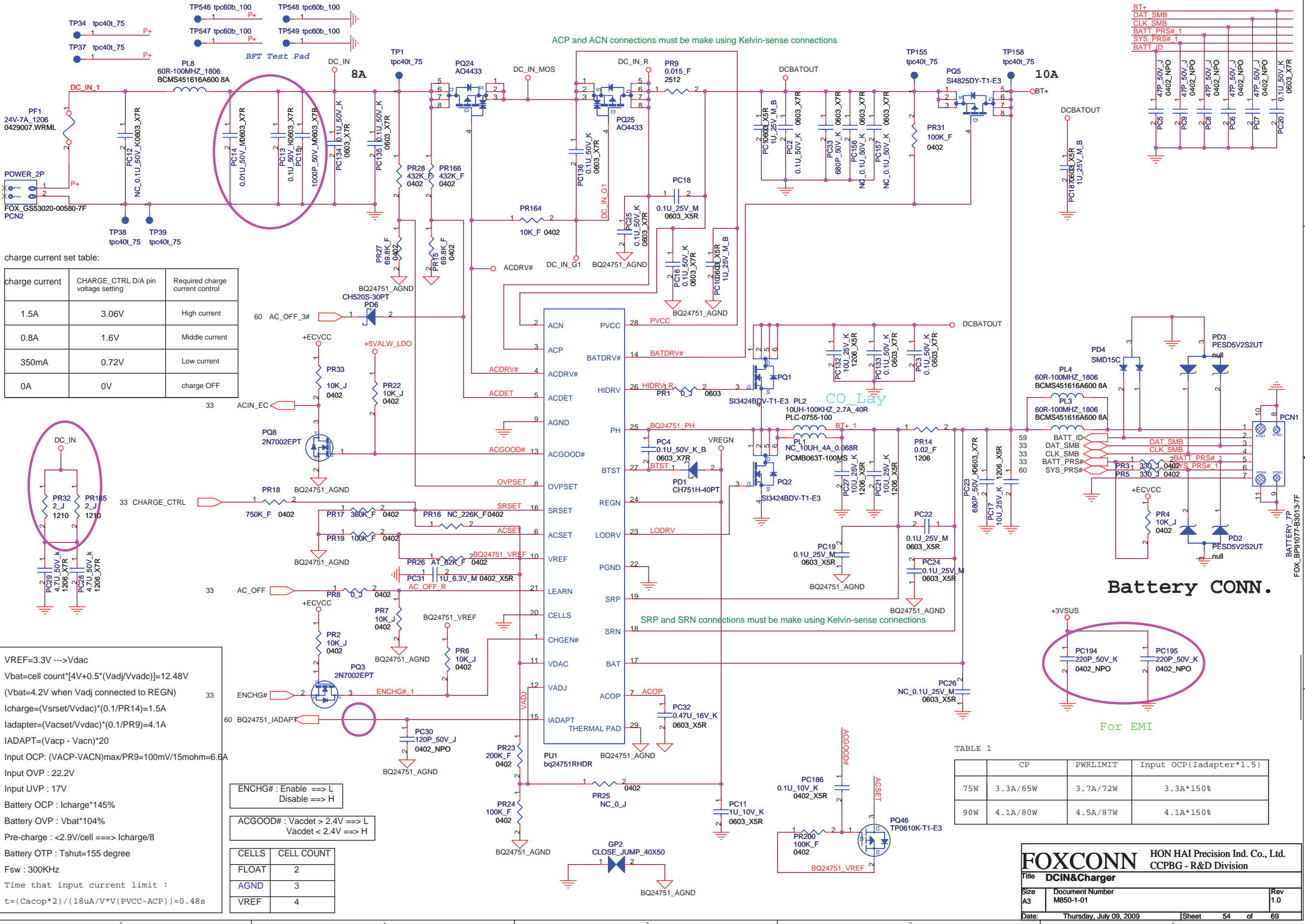


**Audio+USB Board**

EVT

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>HOLE</b>		CCPBG - R&D Division	
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ACP and ACN connections must be make using Kelvin-sense connections

SRP and SRN connections must be make using Kelvin-sense connections

### Battery CONN.

For EMI

charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V --->Vdac  
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdc})] = 12.48V$   
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to } REGN)$   
 $I_{charge} = (V_{rsrset} / V_{vdc}) * (0.1 / PR14) = 1.5A$   
 $I_{adapter} = (V_{acset} / V_{vdc}) * (0.1 / PR9) = 4.1A$   
 $IADAPT = (V_{acp} - V_{vacn}) * 20$   
 Input OCP:  $(V_{acp} - V_{vacn})_{max} / PR9 = 100mV / 15m\Omega = 6.6A$   
 Input OVP: 22.2V  
 Input UVP: 17V  
 Battery OCP:  $I_{charge} * 145\%$   
 Battery OVP:  $V_{bat} * 104\%$   
 Pre-charge :  $< 2.9V / \text{cell} ==> I_{charge} / 8$   
 Battery OTP :  $T_{shut} = 155 \text{ degree}$   
 $F_{sw} = 300KHz$   
 Time that input current limit :  
 $t = (C_{acop} * 2) / (18\mu A / V * V * (PVCC - ACCP)) = 0.48s$

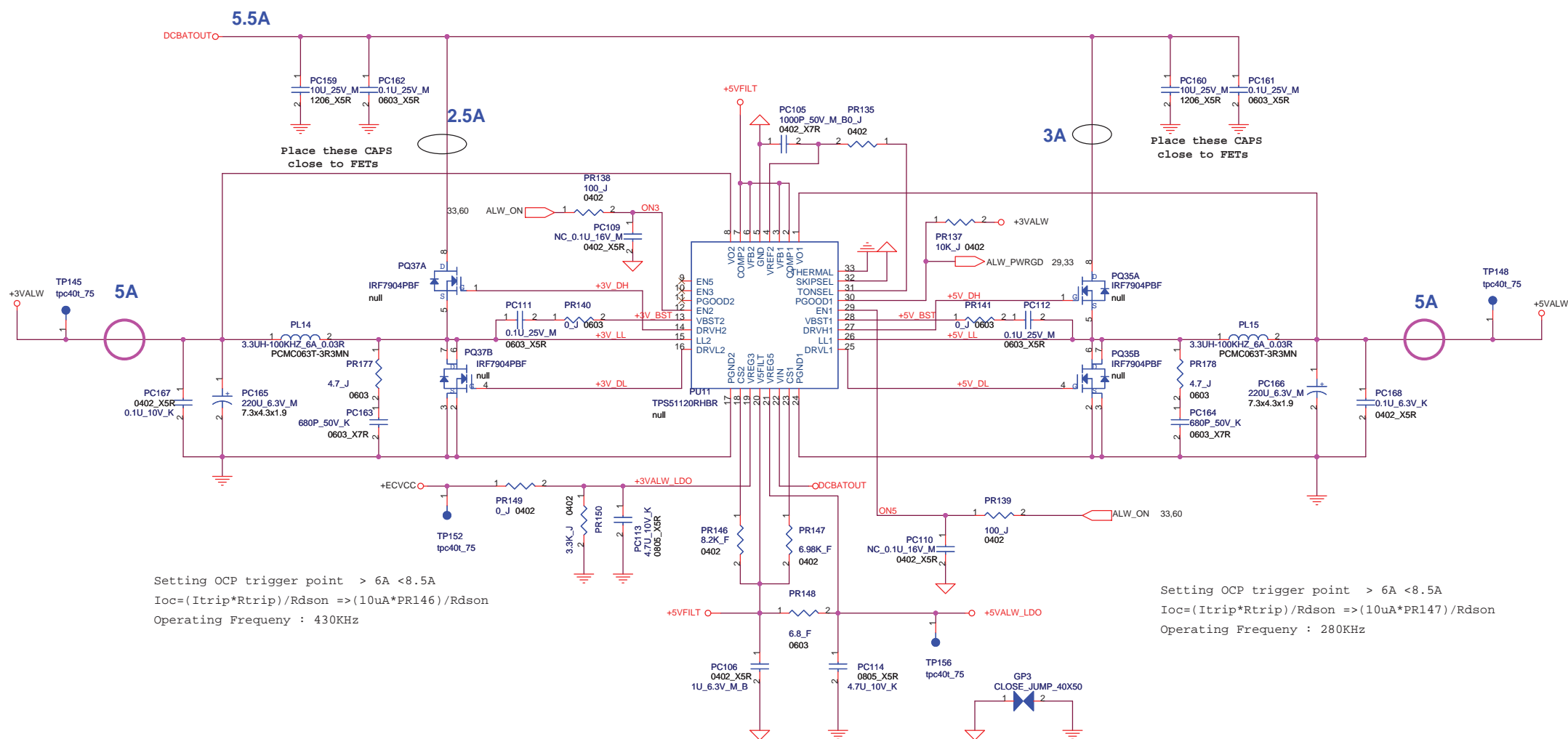
ENCHG# : Enable ==> L  
 Disable ==> H

ACGOOD# :  $V_{vacdet} > 2.4V ==> L$   
 $V_{vacdet} < 2.4V ==> H$

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

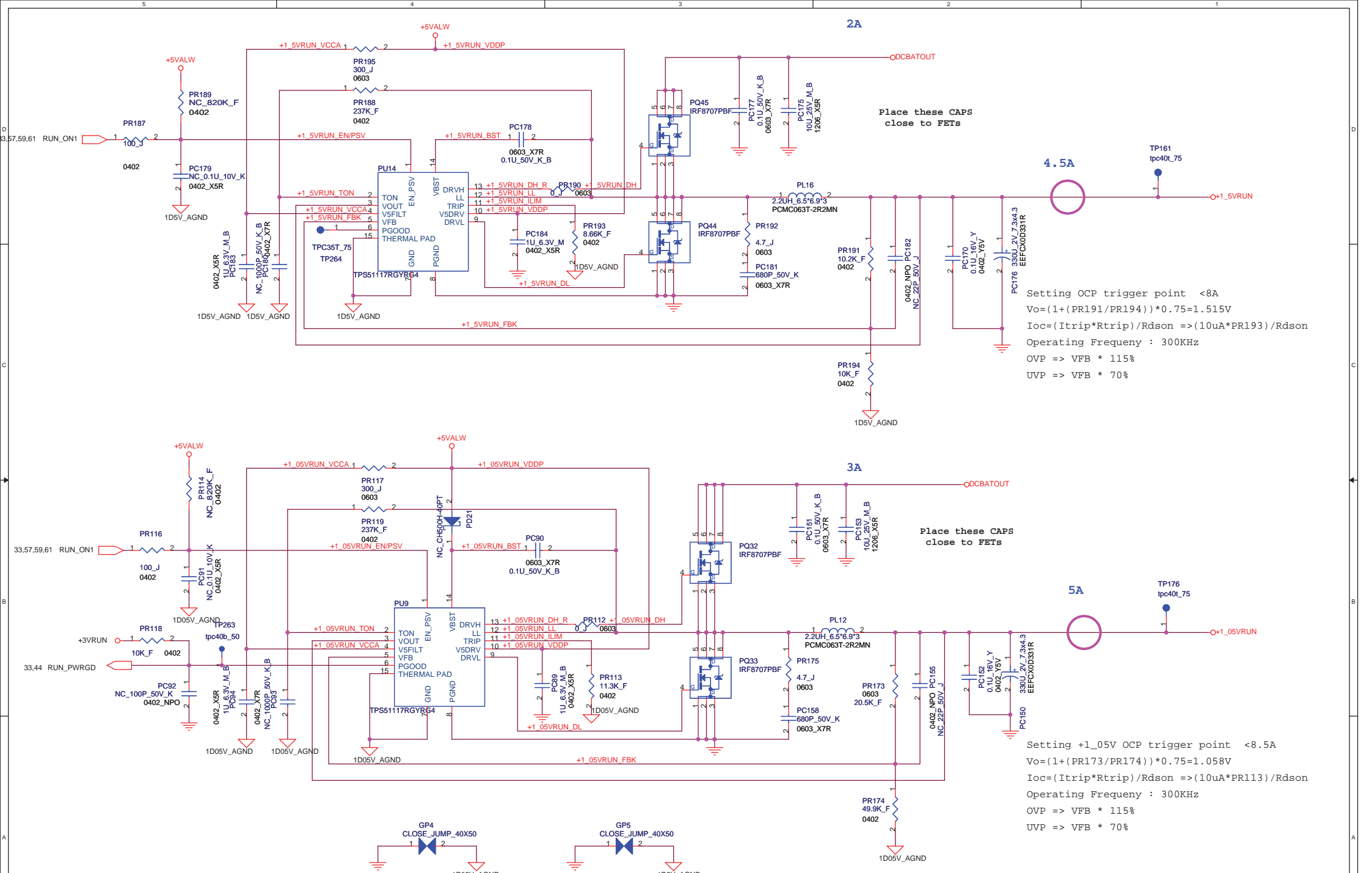
TABLE 1

CP	PWRLIMIT	Input OCP (Iadapter*1.5)	
75W	3.3A/65W	3.7A/72W	3.3A*150%
90W	4.1A/80W	4.5A/87W	4.1A*150%



Setting OCP trigger point > 6A < 8.5A  
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR146) / R_{dson}$   
 Operating Frequency : 430KHz

Setting OCP trigger point > 6A < 8.5A  
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR147) / R_{dson}$   
 Operating Frequency : 280KHz



Place these CAPS close to FETs

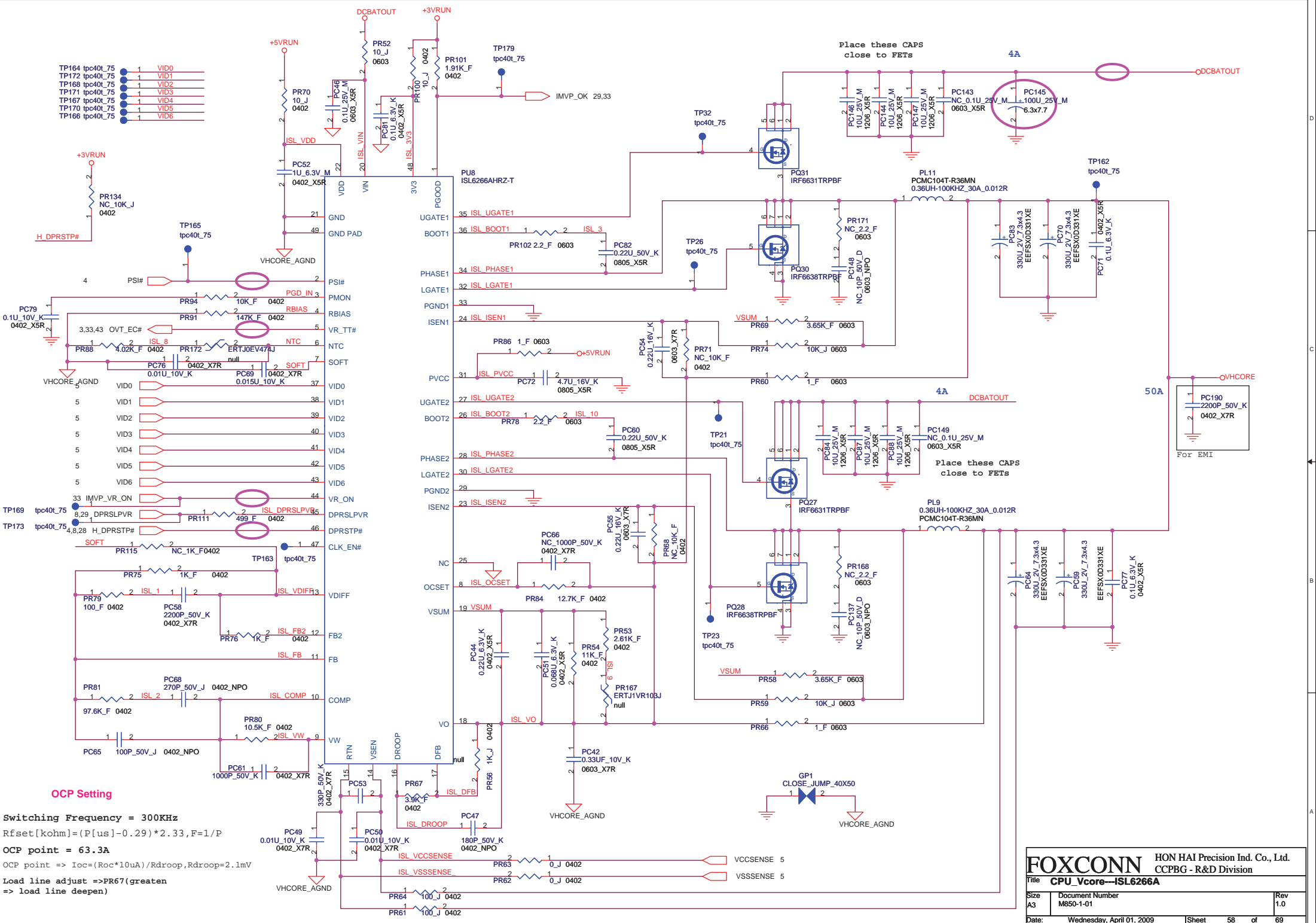
Setting OCP trigger point <8A  
 $V_o = (1 + (PR191/PR194)) * 0.75 = 1.515V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR193) / R_{dson}$   
 Operating Frequency : 300KHz  
 OVP => VFB \* 115%  
 UVP => VFB \* 70%

Place these CAPS close to FETs

Setting +1\_05V OCP trigger point <8.5A  
 $V_o = (1 + (PR173/PR174)) * 0.75 = 1.058V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR113) / R_{dson}$   
 Operating Frequency : 300KHz  
 OVP => VFB \* 115%  
 UVP => VFB \* 70%



- TP164 tpc40L\_75 1 VID0
- TP172 tpc40L\_75 1 VID1
- TP168 tpc40L\_75 1 VID2
- TP171 tpc40L\_75 1 VID3
- TP167 tpc40L\_75 1 VID4
- TP170 tpc40L\_75 1 VID5
- TP166 tpc40L\_75 1 VID6



Place these CAPS close to FETs

4A

Place these CAPS close to FETs

4A

50A

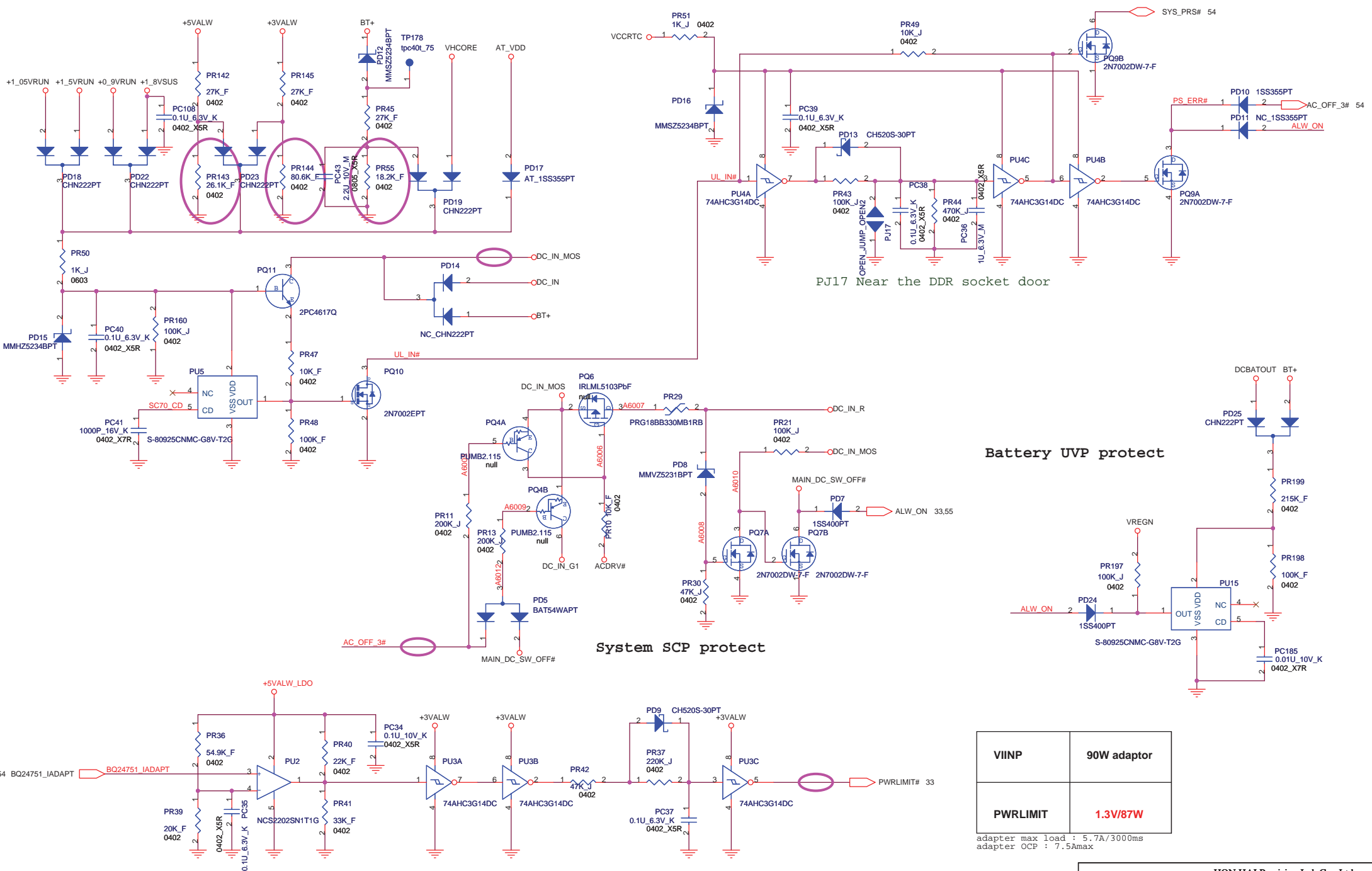
**OCP Setting**

Switching Frequency = 300KHz  
 $Rfset[kohm] = (P[us] - 0.29) * 2.33, F=1/P$   
 OCP point = 63.3A  
 OCP point =>  $Ioc = (Roc * 10uA) / Rdroop, Rdroop = 2.1mV$   
 Load line adjust => PR67(greaten => load line deepen)

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>CPU_Vcore-ISL6266A</b>		CCPBG - R&D Division	
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PJ17 Near the DDR socket door

Battery UVP protect

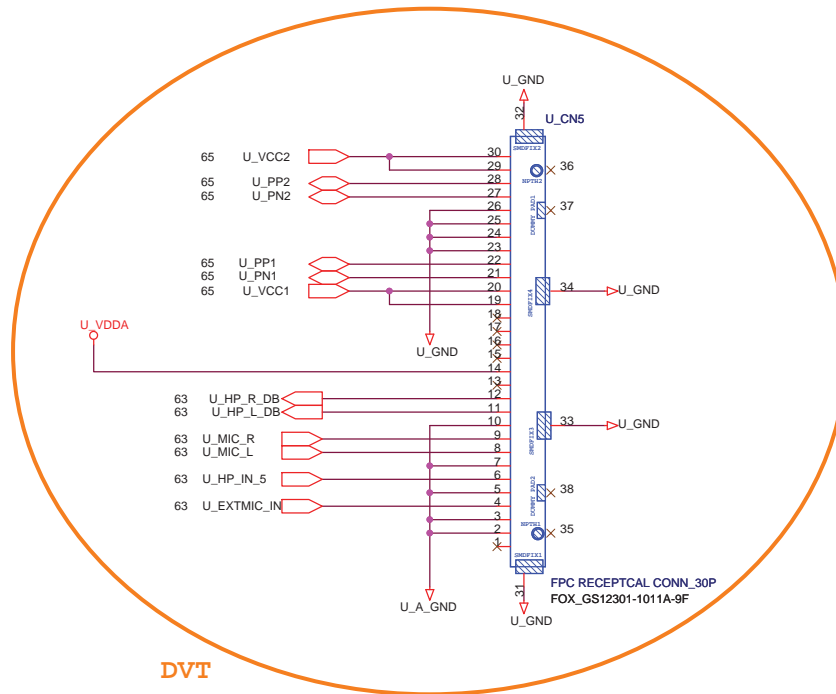
System SCP protect

PWRLIMIT Protect

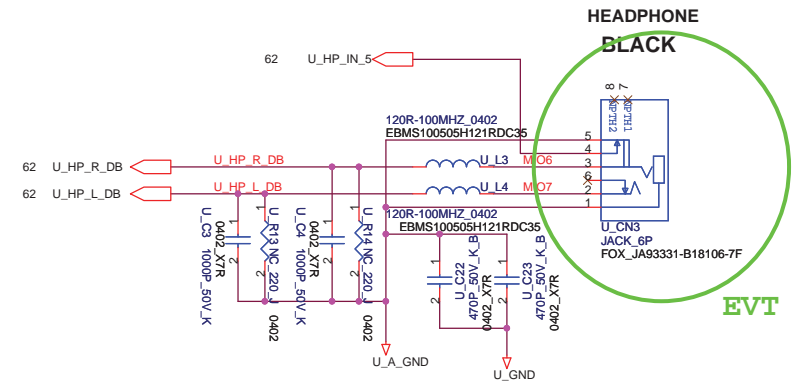
VIINP	90W adaptor
PWRLIMIT	1.3V/87W

adaptor max load : 5.7A/3000ms  
adaptor OCP : 7.5Amax



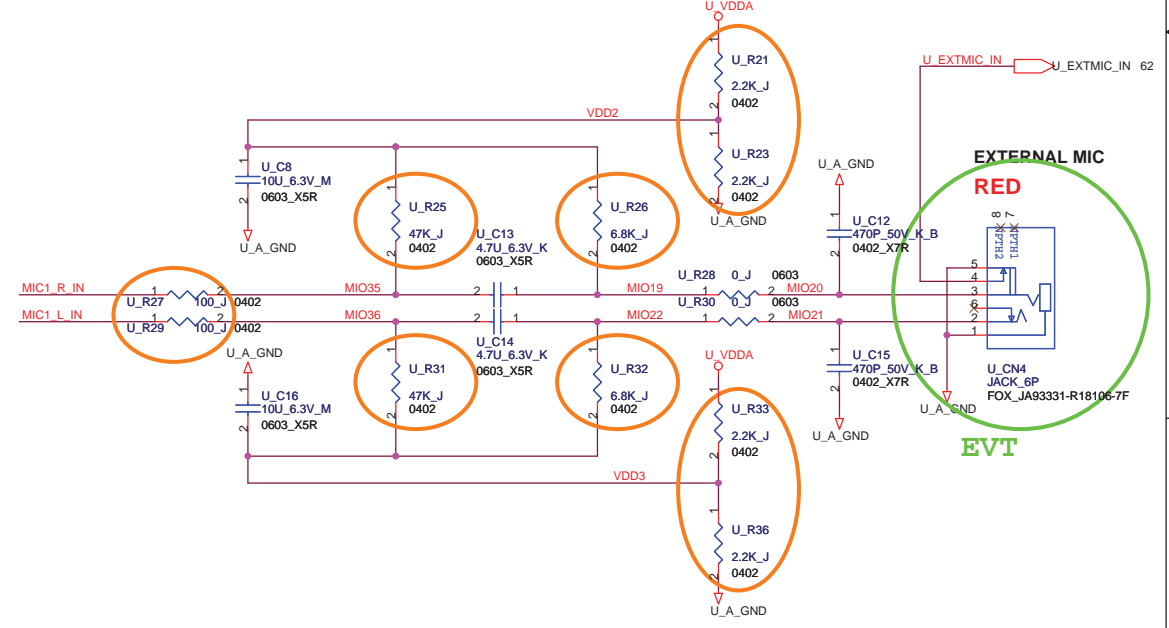
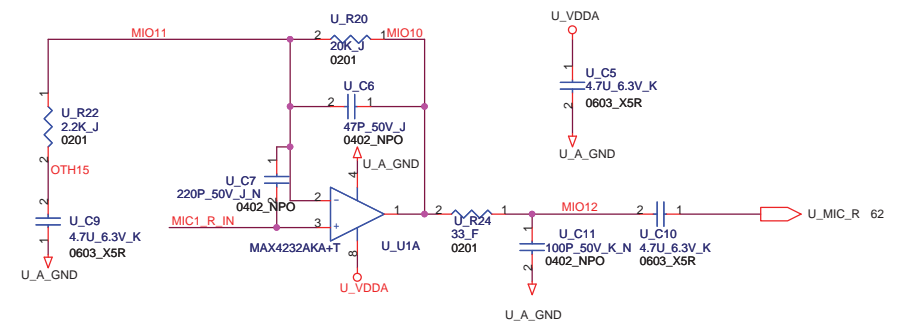


DVT



HEADPHONE  
BLACK

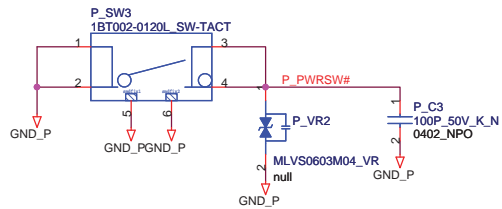
EVT



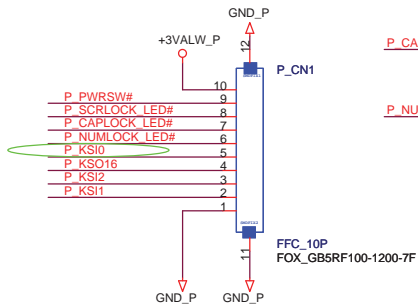
EXTERNAL MIC  
RED

EVT

**POWER BUTTON**



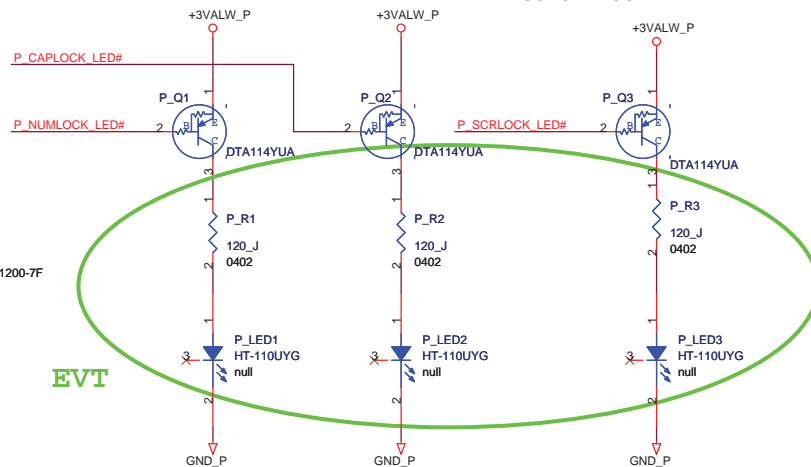
**Power Button Board**



**NUM LOCK LED**

**CAP LED**

**SCROLL LOCK LED**



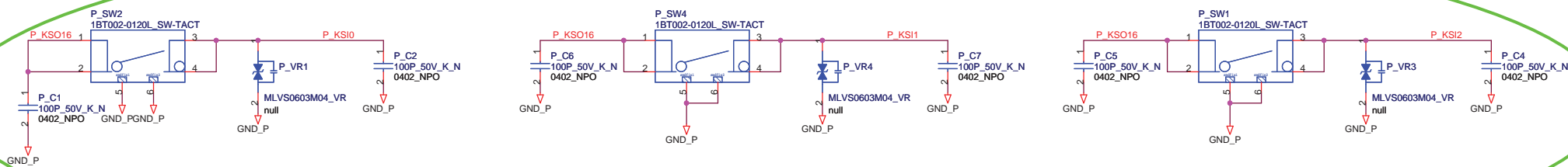
**EVT**

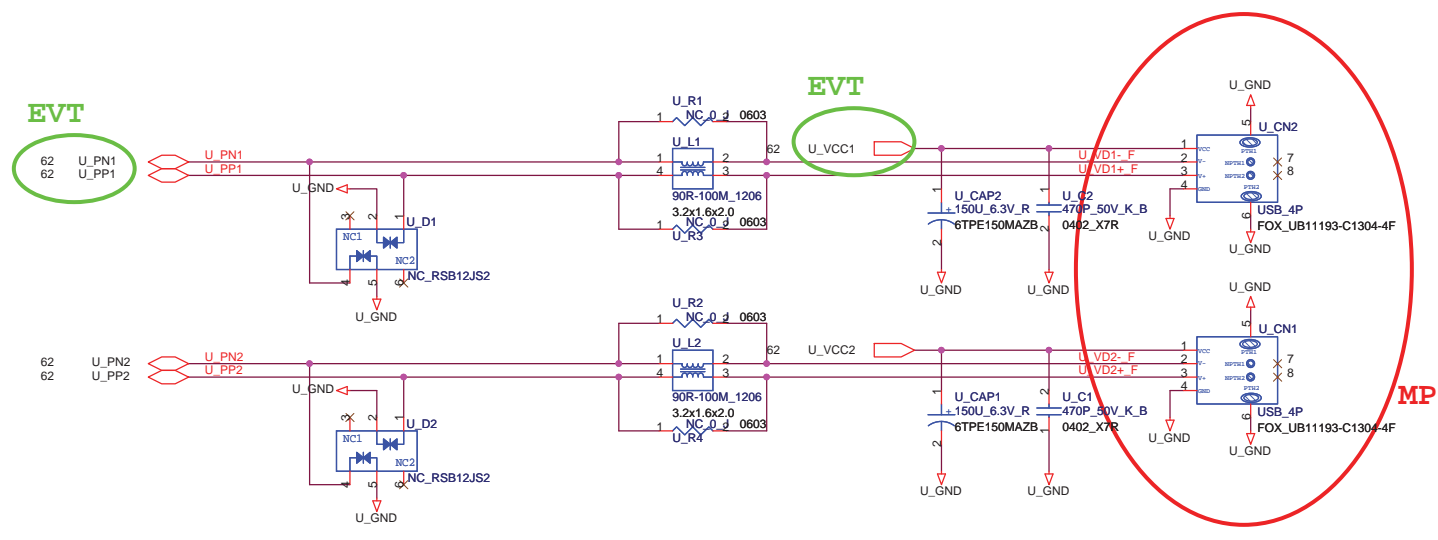
**Instant ON**

**Mute**

**Display OFF**

**EVT**





## M850 EVT

### (2008/08/29)

- P.45 Change CN16 from WK21923-S6P-7F to WK21923-R6S-7F for ME request.
- P.32 Change CN25 from LN27131-A403-4F to LN21131-F404-9F for ME request.
- P.32 Change CN13 from LD2722F-SR6L to LD2722H-S49L for ME request.
- P.25 Change CN18 from HT1310F to GS12201-1011-9F for ME request.
- P.46 Change CN17 from HS6106E to HS6206E for ME request.
- P.37 Change CN22 from HS6108E to HS8208E for ME request.
- P.33 Change CN3 from GB21240-0002-7F to 196009-24021 for ME request.
- P.49 Change CN32 from QT510106-111H-7F to QT510106-311H-7F for ME request.
- P.35 Change SW4 from 1BS007-12120-002-7F to 1BS007-12110-002-7F for ME request.
- P.39 Change U\_CN4 from JA9333L-R5S7-7F to JA93331-R18106-7F for ME request.
- P.39 Change U\_CN3 from JA9333L-B5S7-7F to JA93331-B18106-7F for ME request.
- P.51 Change U\_CN1 and U\_CN2 from UB11193-C1314-4F to UB11193-C1308-4F for ME request.
- P.52 Add BOSS11 and BOSS12 for ME request.

### (2008/08/29)

- P.45 Change CN11 form UV31413-GR56P-7F to UV31413-WZ03P-7F for ME request.
- P.24 Change CN2 from DZ11A91-MA2SY-4F to DZ11A91-SB281-4F for ME request.
- P.26 Change CN31 from QJ5119L-NT03-4F to QJ5119L-NK03-4F for ME request.
- P.48 Change CN9 from UB11193-C1314-4F to UB1112C-CA501-7F for ME request.

### (2008/09/01)

- P.55 Change PR146 from 6.98K\_F to 8.2K\_F for OCP setting.
- P.55 Change PR147 from 6.19K\_F to 6.98K\_F for OCP setting.
- P.56 Change PR193 from 5.49K\_F to 8.66K\_F for OCP setting.
- P.56 Change PR113 from 8.66K\_F to 11.3K\_F for OCP setting.
- P.61 Change PR87 from 6.8K\_F to 8.2K\_F for OCP setting.
- P.61 Change PR99 from 8.2K\_F to 6.98K\_F for AT\_VDD voltage setting to 1.2V.

### (2008/09/02)

- P.25 Change CN18 from GS12201-1011-9F to GS12301-1011A-9F for support Dual-LVDS.
- P.25 Add RP51,RP52,RP53 and RP54 for support Dual-LVDS.

### (2008/09/19)

- P.35 Delete R611&R612 for MOR's requested
- P.35 Add D22 for MOR's requested
- P.27,42,48,51 Change external USB port from USBP3N/USBP3P to USBP1N/USBP1P for MOR's requested
- P.27,35,36 Change PCIE port from Express Card #2, WLAN #3 to WLAN #2, Express Card #3 for MOR's requested
- P.54 Change PCN1 from BP91077-B2013-7F to BP91077-B3013-7F for ME's requested
- P.37 Change U4 from 88E8055 to 88E8057 for MOR's requested
- P.49 Delete R668,674,672,671 for MOR's requested
- P.35 Change C538,C544,C536 to NC for MOR's requested

### (2008/09/22)

- P.45 Change CN11 from UV31413-WZ03P-7F to UV31413-RU81P-7F for ME's requested

### (2008/09/24)

- P.48 Change CN9 from UB1112C-CA501-7F to UB1112C-CA207-7F for ME's requested

### (2008/09/26)

- P.65 [Power board DB button] Add P\_SW4,P\_C6,P\_C7,P\_VR4 for add mute button
- P.25 [Inverter CONN] Change CN19 from HS6106E to HS6108E for support LED backlight function
- P.25 [Panel ID Switch] Change SW1 from HDS404-E to FHDS-04-T-V-T/R for shortage issue

### (2008/10/02)

- P.36 [ExpressCard] Add R901,R902,R903,R904 for test GMT577 ExpressCard power switch
- P.37 [GLAN]Change L5 from NS682403P to LFE9249-R for PUR's suggestion
- P.26 [HDMI] Change CN31 from QJ5119L-NK03-4F to QJ5119L-NT03-4F for ME's ID concern
- P.52 [Thermal Module Nut] Change BOSS3,BOSS6,BOSS7 form F50M20-501130BS to EMI\_F50M20\_351130BS for ME's concern
- P.21,22 [VRAM] Change U49,U50,U51,U52 from K4J10324QD-HC14 to K4J10324QD-HC12 for support 800MHz
- P.50 [TouchPad] Change CN7 from GB5RF120-1200-7F to GB5RF060-1200-7F for change to 6-pin solution
- P.60 [OVP protection]Delete PR35 CA\_69.8K\_F for 8L version unnecessary resister.
- P.50 [MS/SD LED] Combine MS/SD LED for MOR's requested
- P.65 [Caps/Num/Scroll lock LED] Change from HT-150YG to HT-110UYG for ME's ID concern
- P.14 [DDR2] Swap RP13,RP10 pin assignment for layout convenient
- P.15 [DDR2] Swap RP33,RP34,RP32,RP28,RP29 pin assignment for layout convenient
- P.25 [LVDS] Change L98 from EBMS160808A121(400mA) to HCB1608KF-121T10(1A) for Panel max current is 500mA

### (2008/10/06)

- P.27 [ICH9] Swap RP46,RP24,RP16 pin assignment for layout convenient
- P.50 [TP] Reserved 12pin TP solution in EVT

### (2008/10/07)

- P.49 [BT]NC U46,R673,R670,C847 and add R907 for BT module has internal protection schematics for BT\_DATA pin.
- P.35 [WLAN]Change Q49 from FET to transistor for a little cost down.
- P.54 [DCIN&Charger]Delete PR34 for 8L version unnecessary resister.
- P.52 [HOLE]Update HOLE for ME's requested.
- P.11 [Cantiga] Delete R121,R151 for 8L version unnecessary resister.

### (2008/10/08)

- P.11 [Cantiga]Delete C202,C225 for VCCD\_TVDC can be connected to GND form Intel DG mention.
- P.18 [VGA]REFCLK jumper R849.2pin should be connected to R848.1pin side not R848.2pin side. In case if you use REFCLK, It's voltage should be devided also.
- P.18 [VGA]Delete R840,R841,R843 and connect R2B,G2B,B2B to GND directly.
- P.24 [CRT]Change DDC 3V pull-up R57,R58 from 2.2k to 3.9k to meet E-DDC spec.
- P.25 [LVDS]Add R908 for AT\_LCDVCC\_EN need 10k pull-down as AMD Check list 8-1 mention.
- P.26 [HDMI]Delete R649 for HDMI DDC need back drive protection so cannot use R649.
- P.26 [HDMI]Delete D21 and R652 for if using diode, HDMI\_+5VRUN voltage cannot meet spec. And HDMI\_+5VRUN need back drive protection.
- P.25 [LVDS]Change R393 from 10k to 100k to meet desing guide.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
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## M850 EVT

### (2008/10/09)

- P.21 [VRAM]Change R770,R771 from 82.5ohm to 120ohm for AMD suggestion
- P.33,51,64 [Button]Delte KSO15 and add KSI0 control signal for SW request
- P.49 [BT]Add R909(NC) for new BT module reserved
- P.11 [Cantiga>Delete R116 for useless
- P.33 [EC]Change R477,R437 to mount and R479,R436 to NC for H model ID change to "10"
- P.25 [LVDS]Change back R393 from 100k to 10k to meet AMD check list 8-8.

### (2008/10/10)

- P.62 [Audio+USB CONN]Swap pin assignment for cable routing smooth.
- P.03 [Penryn]Add C1287(NC) for EMI verification.
- P.33 [EC]Add R910~R933 for EMI verification.
- P.51 [Power Board CONN]Add C1288~C1295(NC) for EMI verification.
- P.17 [VGA>Delete R817,R818 for GPIO9 is VGA\_DIS strap.

### (2008/10/11)

- P.52 [HOLE]Update all holes for ME's requested

### (2008/10/13)

- P.33 [EC>Delete R910~R933 for layout space not enough
- P.51 [Power Board CONN>Delete C1288~C1295 for layout space not enough.
- P.48 [USB]Change CN9 from UB1112C-CA207-7F to UB11123-CA301-7F for ME's concerned.
- P.54 [DCIN&Charger]Add PC194,PC195(NC) for EMI verification

### (2008/10/14)

- P.52 [HOLE>Delete H16,H17,H18 for ME's requested.
- P.17 [VGA]Add R910,R911 for AMD confirm pin DVPPDATA\_22 and DVPPDATA\_23 function
- P.29 [ICH9>Delete R301 for needless
- P.48 [USB]Change CN9 from UB11123-CA301-7F to UB111M3-CA4S4-7F for ME's requested

### (2008/10/15)

- P.16 [VGA]Change R849 from 0ohm to 100ohm and Net for R861.1&R860.1 changed to R\_AT\_XTALIN for MOR's comment
- P.42 [Audio]Add C1288(NC) for EMI verification

### (2008/10/16)

- P.50 [T/P]Reverse CONN for ME's requested

## M850 DVT

### (2008/11/13)

- P.40 [Audio]Reverse JSPK1 pin definiens for ME's cable routing concern
- P.62 [Audio+USB DB]Reverse U\_CN5 pin definiens for ME's cable routing concern
- P.47 [Felica]Reverse CN6 pin definiens for ME's cable routing concern
- P.50 [T/P]Reverse CN7 pin definiens for ME's cable routing concern
- P.18 [VGA]Connect U53.T11&R11 to GND for ATI updated
- P.17 [VGA]Change R815,R814 to NC and R910 to mount for ATI DVPPDATA[23,22] failure issue

### (2008/11/15)

- P.50 [T/P>Delete CN34,R530,R531 for cancel 12pin T/P solution

### (2008/11/17)

- P.26 [HDMI]Change CN31 from QJ5119L-NT03-4F to QJ1119L-NT03-4F(Dip type) for CONN issue

### (2008/11/19)

- P.26 [HDMI]Swap RP47 and RP49 for layout convenient
- P.52 [HOLE]Change U\_H3 size for ME's requested
- P.52 [HOLE>Delete P\_PAD5 and add P\_H3 for ME's requested
- P.52 [HOLE]Change P\_PAD4 size for ME's requested
- P.52 [HOLE>Delete P\_H1 and P\_H2 for ME's requested

### (2008/11/24)

- P.55 [SYS Power (+3\_3V/+5V)] Add test point TP152, TP156
- P.56 [SYS Power(+1\_5V/+1\_05V))] Add test point TP161, TP176
- P.58 [CPU\_Vcore---ISL6266A] Add test point TP179
- P.59 [Others power plane] Add test point TP132, TP133, TP157, TP160, TP177
- P.60 [OVP protection] Add test point TP178

### (2008/12/01)

- P.54 [DCIN&Charger] Add test point TP34, TP37, TP38, TP39
- P.54 [DCIN&Charger] Change PQ5 from AO4433 to SI4825DY-T1-E3 for EMI Issue
- P.58 [CPU\_Vcore---ISL6266A] Add PJ11 for power test

### (2008/12/02)

- P.62 Change U\_CN5 pin33 and Pin34 to connect U\_GND
- P.06 [Clock Gen] Change test point type of TP153,TP154 for L6 requested
- P.63 [Audio]Change U\_R21,U\_R23,U\_R33,U\_R36,U\_R27,U\_R29,U\_R25,U\_R26,U\_R31 and U\_R32 from 0201 to 0402 for L6 requested
- P.33 [EC,LVDS] Add LED\_OFF#(GPIO04) signal to U6.1 and U23.1 for Display Off issue.
- P.25 [LVDS] Change SW1 from 8pin to 12pin for add Instant ON function

### (2008/12/04)

- P.50 [T/P Buttom] Change SW2 and SW3 from 1BT001-1420L-001(160g) to 1BT001-1410L-001(100g) for ME's requested
- P.26 [HDMI] Swap RP47 and RP49 for layout convenience

### (2008/12/05)

- P.52 [HOLE] Change U\_H3 from 1X-HOLE000-0935 to 1X-HOLE000-0959 for ME's requested
- P.52 [HOLE] Change U\_H1 from 1X-HOLE000-0905 to 1X-HOLE000-0958 for ME's requested
- P.52 [HOLE] Change P\_H3 from 1X-HOLE000-0936 to 1X-HOLE000-0960 for ME's requested

### (2008/12/10)

- P.33,34,37,40,43,46,51,54 [Test Pad] Add TP500~TP549 for BFT test pad
- P.54 [DCIN] Delete PL6 for safety concern
- P.37 [GLAN]NC R24,R25,U3,C16 and mount R616 for using M8057 internal EEPROM.
- P.17 [VGA]Update VRAM strp for add Hynix VRAM
- P.33 [EC]Add TP550,TP551 for detect D17 reverse from L6's suggestion
- P.48 [USB]Add TP552~TP554 for detect USB power switch leakage from L6's suggestion

### (2008/12/12)

- P.59 [Other power plane]Change PQ40,PQ41 from SI2316DS-T1-E3 to SI7326DN-T1-E3 for overload test issue.
- P.26 [HDMI]Change R647 and R646 to 3.9k ohm for meet E-DDC spec.
- P.49 [BT]Change CN32 from QT510106-311H-7F to QT510106-312H-7F for ME's requested.

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## M850 DVT

(2008/12/15)

- P.54 [DCIN&Charger] Change PC194, PC195 from NC\_0.1U\_50V\_K 0603 to 220P\_50V\_K 0603 for EMI request
- P.61 [VGA Power] Change PR99 from 6.98K\_F 0402 to 11K\_F 0402 for AMD M92 Power-Play function
- P.61 [VGA Power] Change PR110 from NC\_49.9K\_F 0402 to 19.6K\_F 0402 for AMD M92 Power-Play function
- P.61 [VGA Power] Change PQ12 from NC to mount for AMD M92 Power-Play function
- P.61 [VGA Power] Change PC85 from NC to mount for AMD M92 Power-Play function
- P.61 [VGA Power] Change PR103 from 0\_J 0402 to 1K\_J 0402 for AMD M92 Power-Play function

(2008/12/18)

- P.54 [DCIN&Charger] Change PC28, PC29 from 4.7U\_25V\_K 0805 to 4.7U\_50V\_K 1206 for reducing DC\_IN inrush voltage.
- P.54 [DCIN&Charger] Parallel PR32 and PR165 for reducing DC\_IN inrush voltage.
- P.54 [DCIN&Charger] Change PL1 from SPD8D43PT100M to PCMB063T-100MS for 2nd source implement.
- P.50 [LED] Change R385 from 33ohm to 51ohm for LED brightness issue

(2008/12/19)

- P.60 [OVP Protection] Add PR160 100K\_J 0402 for MOR request.
- P.46 [CAM]Change U41 to MAX4789EUK and delete C815,C816,R626 for VEDS current limit requested.
- P.43 [FAN]Add F10 for prevent FAN sorot issue of MOR requested
- P.24 [CRT]Change R418 and R424 from 22ohm to 33ohm for improve VEDS AGRB issue.
- P.24 [CRT]Change CN2 from DZ11A91-SB281-4F to DZ11A91-SB2SN-4F for ME's requested.

(2008/12/20)

- P14,15 [DDR2]Add C1289,C1290,C1291,C1292,C1293,C1294 (NC) for EMI concern and MOR requested
- P.50 [TP]Change F7 from 0.5A to 0.35A for MOR's requested
- P.47 [Felica]Change F6 from 0.5A to 0.35A for MOR's requested
- P.47 [Felica]Add U56,C1295,C1296,R913 (NC) and R912 for reserve power switch for MOR's requested
- P.40 [Audio]Change R493,R494 from 1k to 47k for Pi-Pi noise issue

(2008/12/22)

- P.35 [Half Mini Card]Add R914 for RF team test VEDS,MP will delete it.
- P.54 [DCIN&Charger]Change TP546-TP549 from 40mil to 60mil for BFT side requested.
- P.23,33 [EC]Change signal name "LED\_OFF#" to "LCD\_OFF#" for MOR's suggestion.
- P.60 [OVP]Change PC41 from 0.01uF to 1nF for Power\_Abnormal\_Conditions issue.
- P.47 [Felica]Delete L60 for needless and SMT requested
- P.48 [USB]Delete L61 for needless and SMT requested

(2008/12/23)

- P.37 [Marvell GLAN]Delete TP538-TP545 for layout space concern
- P.45 [PCI]Change C496 from 27p to 22p for improve crytal accuracy
- P.29 [ICH9]Change footprint of D8 for SMT requested
- P.30 [ICH9]Change footprint of D14 for SMT requested

(2008/12/24)

- P.52 [HOLE]Change H5 from 1X-HOLE000-0925 to 1X-HOLE000-0913 for ME's requested

## M850 PVT

(2008/12/26)

- P.33 [EC] Add R915 for updating Instand On function.

(2009/02/09)

- P.50 [T/P]Update the connection of SW2 and SW3 to correct T/P function
- P.35 [WLAN]Update the connection of WLAN Switch to meet ME's requested

(2009/02/10)

- P.54 [DCIN&Charger] Change PR32, PR165 from 1\_J 1210 to 2\_J 1210 for reducing DC\_IN inrush voltage.
- P.54 [DCIN&Charger] Change PC194, PC195 from 220P\_50V\_K 0603\_NPO to 220P\_50V\_K 0402\_NPO for PUR convenient.
- P.54 [DCIN&Charger] Delete PR12 for unnecessary.
- P.55 [SYS Power(+3\_3V/+5V)] Delete PJ1, PJ2 for unnecessary.
- P.56 [SYS Power(+1\_5V/+1\_05V)] Delete PJ3, PJ4 for unnecessary.
- P.57 [DDR2 Power(+1\_8V/+0\_9V)] Delete PJ5, PJ8 for unnecessary.
- P.58 [CPU\_Vcore---ISL6266A] Delete PR20, PR38, PR46, PR65, PJ11 for unnecessary.
- P.58 [CPU\_Vcore---ISL6266A] Change PC145 from MATSUSHITA, EEEFK1E101XP to CHEMI-CON, EMVE250ADA101MF80G for MOR request.
- P.59 [Others power plane] Delete PR72, PR77, PR89 for unnecessary.
- P.60 [OVP protection] Delete PR97, PR105, PR108 for unnecessary.
- P.61 [VGA Power(ATI VDD)] Delete PJ7, PJ9, PJ10 for unnecessary.

(2009/02/13)

- P.29 [ICH9]Change R573 from mount to NC because BT\_GPIO is not used for M850.
- P.25 [LVDS]Change signal name "INST\_ON\_SW" to "INST\_ON\_SW#" because it's low active.
- P.33 [EC]Change signal name "INST\_ON\_SW" to "INST\_ON\_SW#" because it's low active.

(2009/02/19)

- P.50 [LED]Change R600 from 120ohm to 150ohm to satisfy brightness requested.
- P.47 [Felica]Change F6 from 0.35A to 0.25A for felica module heated concern.
- P.33 [EC]Add R916 for SPI ROM datasheet updated.
- P.52 [HOLE]Change H4 from 1X-HOLE000-0926 to 1X-HOLE000-1052 for ME's requested.
- P.52 [HOLE]Change H12 from 1X-HOLE000-0915 to 1X-HOLE000-1051 for ME's requested.
- P.65 [USB]Change U\_CN1 and U\_CN2 form UB11193-C1308-4F to UB111S3-C1GS6-4H for ME's requested.

(2009/02/20)

- P.59 [Others power plane] Change PQ16 from IRF8714PBF to IRF8736PBF for +1\_8VRUN voltage drop issue.
- P.60 [OVP protection] Change PR55 from 14.7K\_F 0402 to 18.2K\_F 0402 for BT+ OVP setting.
- P.60 [OVP protection] Change PR143 from 20K\_F 0402 to 26.1K\_F 0402 for +5VALW OVP setting.
- P.60 [OVP protection] Change PR144 from 47K\_F 0402 to 80.6K\_F 0402 for +3VALW OVP setting.
- P.24 [CRT] Change CN2 from DZ11A91-SB2SN-4F to DZ11A91-SA2SN-4H for ME's requested.
- P.47 [Felica]Change F6 from 0.25A to 0.125A for felica module heated concern.

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### (2009/02/23)

- P.50 [TP]Change SW2 and SW3 from 19-1BT0011-1003 to 19-SKHM0KE-1000 for ME's requested.
- P.54 [DCIN]Move PC13,PC14,PC15 to the another side of PL8 for improving EMC.
- P.52 [HOLE]Change BOSS3,BOSS6 from connect to GND to NC for improving EMC.
- P.49 [BT]Change CN32 from QT510106-312H-7F to QT510106-312H-7H for ME's requested.
- P.45 [ILINK]Change CN11 from UV31413-RU81P-7F to UV31413-RU82P-7H for ME's requested.
- P.20 [VGA]Add C1297~C1308 for MOR's requested to check PEG signal.

### (2009/02/24)

- P.48 [USB]Change CN9 from UB111M3-CA4S4-7F to UB111M3-CAGS4-7H for MOR's requested.

### (2009/02/25)

- P.52 [HOLE]Change P\_H3 from 1X-HOLE000-0960 to 1X-HOLE000-1054 for EMC's requested.
  - P.33 [EC]Change R915,R613,R475,R629,R435,R431(10K) from 0201 to 0402 for SMT's requested.
- P.33 [EC]Change R173,R197,R203,R75,R124,R442,R440,R447,R432(100K) from 0201 to 0402 for SMT's requested.
- P.33 [EC]Change R476(4.7K) from 0201 to 0402 for SMT's requested.
- P.34 [Flash ROM]Change R233(0) from 0201 to 0402 for SMT's requested.

### (2009/02/25b)

- P.47 [Modem]Add TP600~TP606 for BFT test requested.

### (2009/02/26)

- P.48 [USB]Change C810 from Y5V to X5R for MOR VEDS requested.
- P.40 [Audio>Delete Q27,R450,R614,Q8,R98,R615 for unnecessary to improve BFT test point.

## M850 MP

### (2009/04/01)

- P.33 [EC]Signal symbol "OVT\_GFX#" change to two-way type for avoiding confusion from SW's suggestion.

### (2009/04/08)

- P.24 [CRT]Change CN2 from FOX\_DZ11A91-SA2SN-4H to FOX\_DZ11A91-SB2SN-4F (same as DVT used) for CONN discoloration issue.
- P.48 [USB2.0]Change CN9 from FOX\_UB111M3-CAGS4-7H to FOX\_UB111M3-CA4S4-7F (same as DVT used) for CONN discoloration issue.
- P.65 [USB DB]Change U\_CN1 and U\_CN2 from FOX\_UB111S3-C1GS6-4H to FOX\_UB11193-C1304-4F for CONN discoloration issue.

### (2009/04/09)

- P.45 [ILINK]Change CN11 from UV31413-RU82P-7H to UV31413-WU82P-7F for CONN discoloration issue.

## M851 PVT

### (2009/07/08)

- P.35 [Half Mini Card]Add TP180,TP184 for LED test in L6.
- P.50 [LED&T/P&LID]Add TP181,TP182,TP183 TP185,TP186,TP187,TP188 for LED test in L6.

### (2009/07/09)

- P.06 [Half Mini Card]Change R542,R276,R283,R288,R553,R277,R278,R536,R537,R538,R534 from 0201 to 0402 for SMT's request.
  - P.08 [Cantiga (DMI) ]Change R286,R231,R193,R195 from 0201 to 0402 for SMT's request.
  - P.12 [Cantiga (VCC CORE)]Change R208 from 0201 to 0402 for SMT's request.
  - P.17 [VGA (Strap)]Change R809,R825,R826 from 0201 to 0402 for SMT's request.
  - P.18 [VGA (I/O)]Change R830,R831,R828 from 0201 to 0402 for SMT's request.
  - P.21 [VRAM (GDDR3)]Change R787,R763,R769,R765,R773,R771,RR772,R767,R770 from 0201 to 0402 for SMT's request.
  - P.22 [VRAM (GDDR3)]Change R801,R786,R800 from 0201 to 0402 for SMT's request.
  - P.28 [ICH9-M (LPC,IDE,SATA)]Change R101 from 0201 to 0402 for SMT's request.
  - P.29 [ICH9-M (GPIO)]Change R541,R540,R567, R322,R575,R300,R297,R303 from 0201 to 0402 for SMT's request.
  - P.33 [EC+KBC (WPCE775L)]Change R444,R477 from 0201 to 0402 for SMT's request.
  - P.38 [Audio (CODEC & POWER)]Change R230,R217 from 0201 to 0402 for SMT's request.
  - P.39 [Audio (HP)]Change R893,R894 from 0201 to 0402 for SMT's request.
  - P.41 [Audio (MUTE)]Change R241,R499,R227,R225,R486,R498,R500,R478 from 0201 to 0402 for SMT's request.
- ### (2009/07/13)
- P.39 [Audio (HP)]Change R893,R894 to 0201 again for avoiding side effect.

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