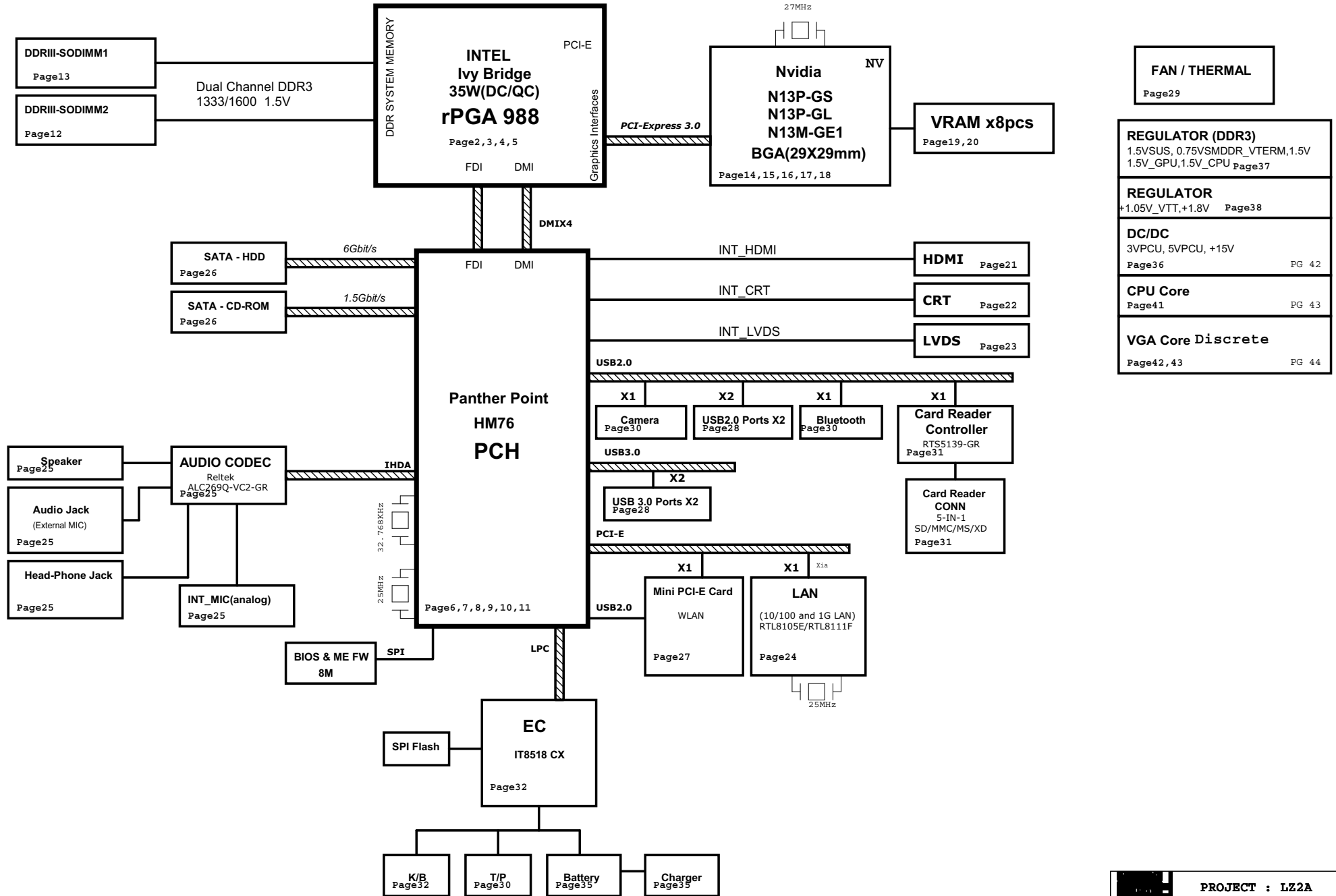


LZ2/LZ2A (Z480) Intel Chief River Platform (Optimus) Block Diagram

01

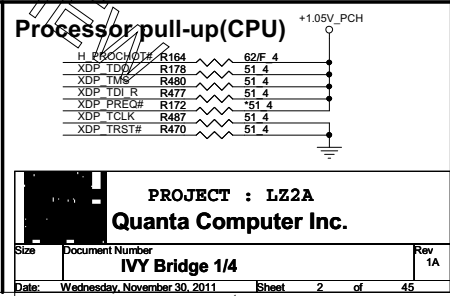
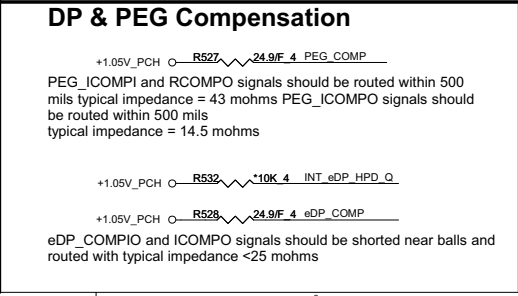
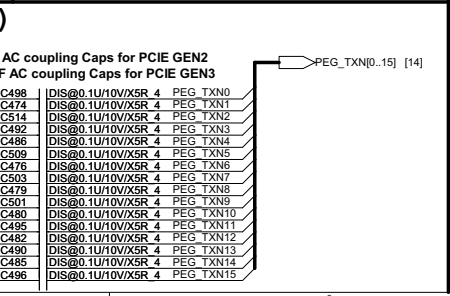
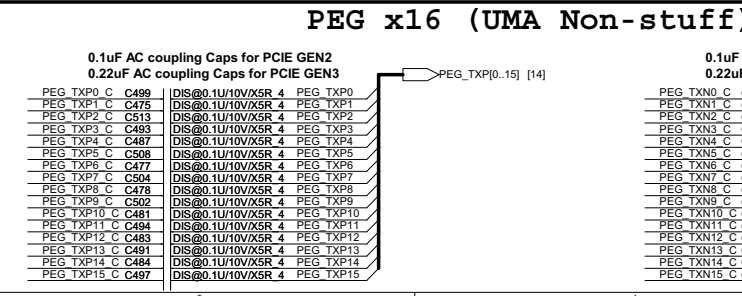
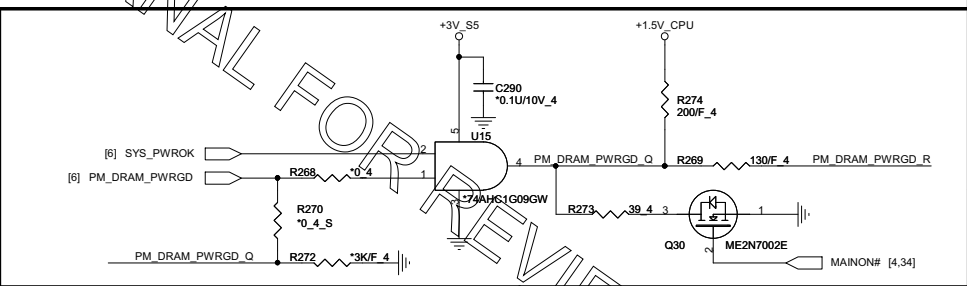
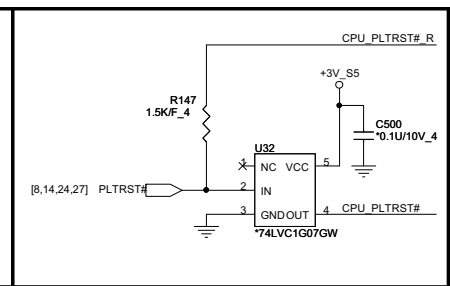
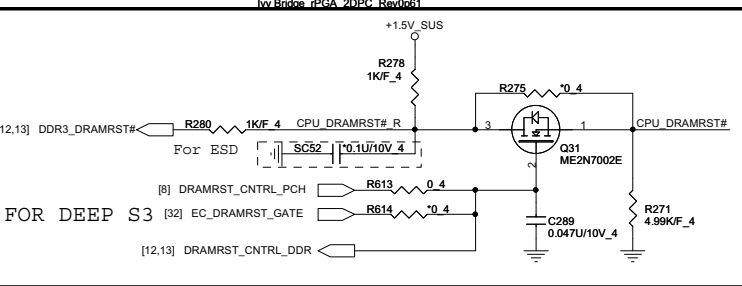
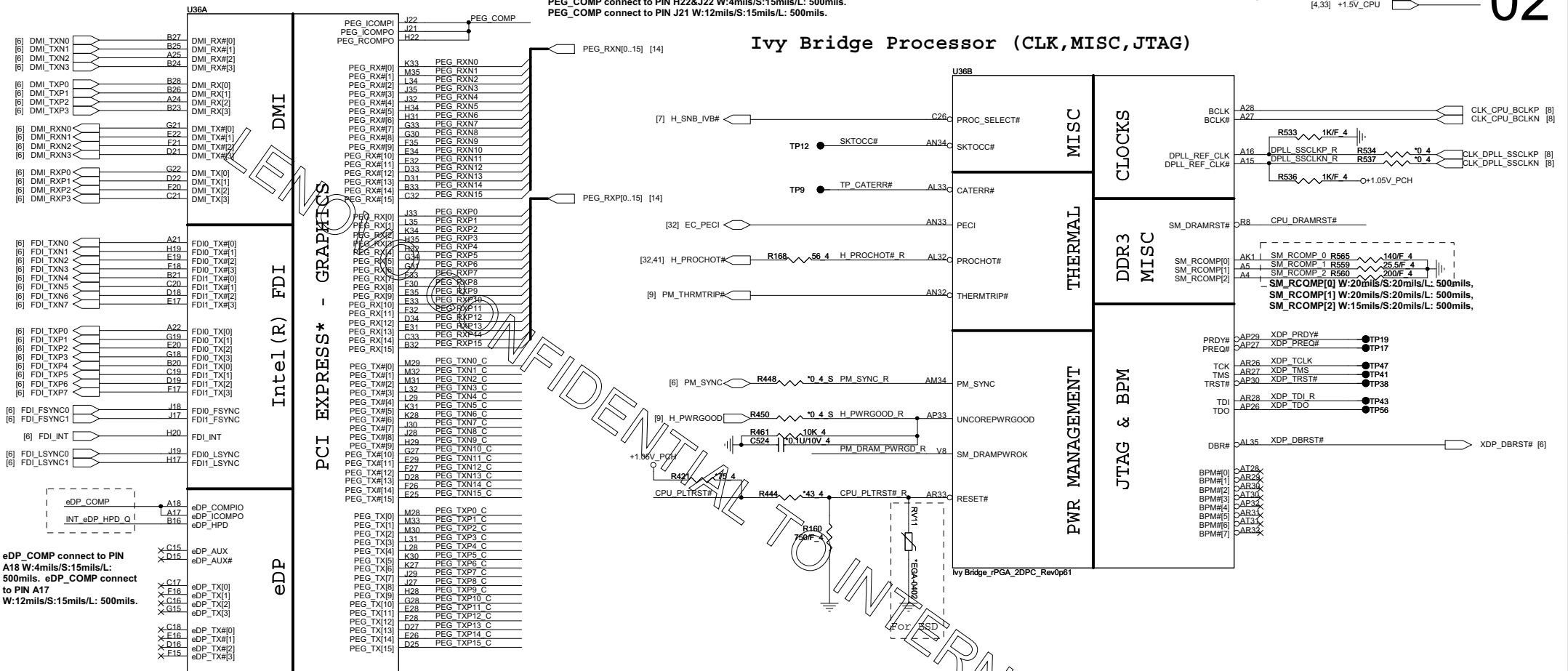


FAN / THERMAL	
Page29	
REGULATOR (DDR3)	
1.5VSUS, 0.75VSMDR_VTERM,1.5V 1.5V_GPU,1.5V_CPU Page37	
REGULATOR	
+1.05V_VTT,+1.8V Page38	
DC/DC	
3VPCU, 5VPCU, +15V Page36 PG 42	
CPU Core	
Page41 PG 43	
VGA Core Discrete	
Page42, 43 PG 44	

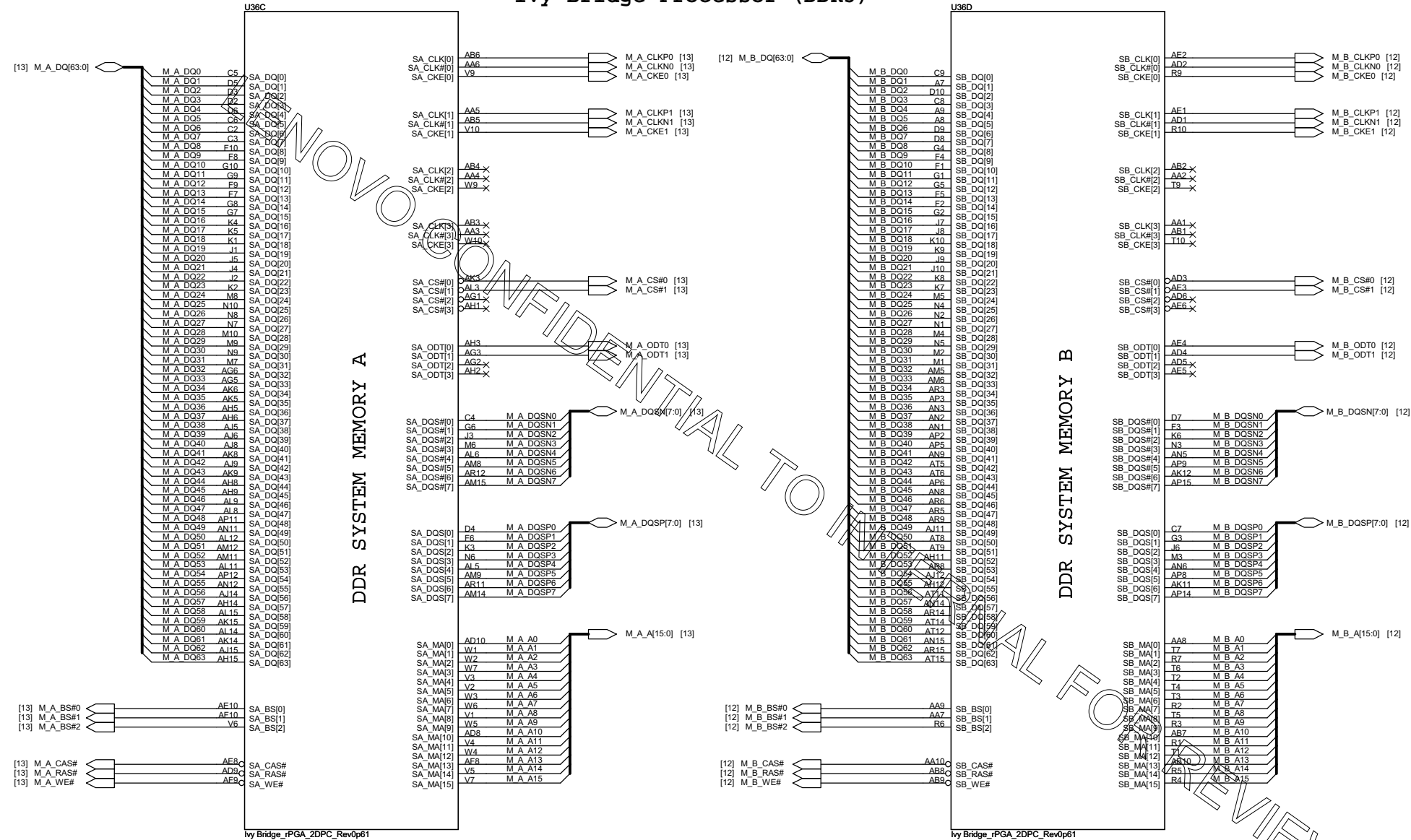
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
 PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

[4,6,7,8,10,33,34,38,43] +1.05V_PCH
 [4,10,12,13,33,34,37,43] +1.5V_SUS
 [6,7,8,9,10,27,31,34] +3V_S5
 [4,33] +1.5V_CPU

Ivy Bridge Processor (CLK, MISC, JTAG)



Ivy Bridge Processor (DDR3)



CONFIDENTIAL TO MICROSOFT FOR REVIEW

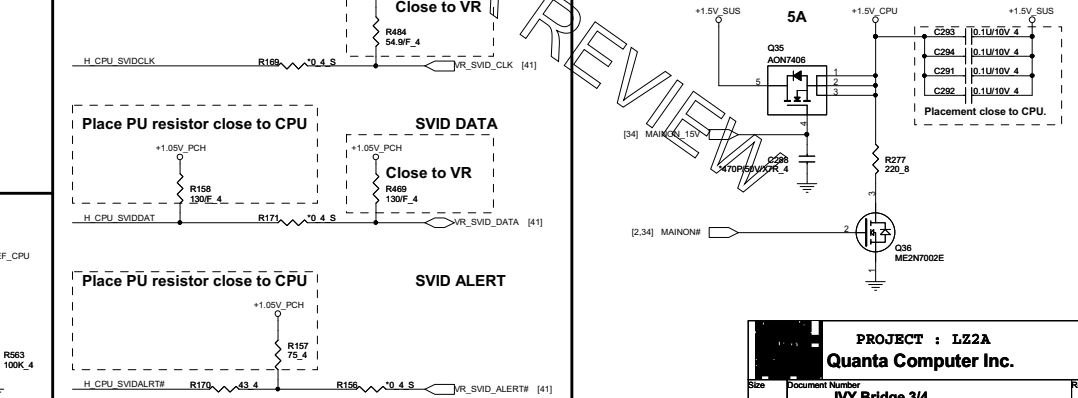
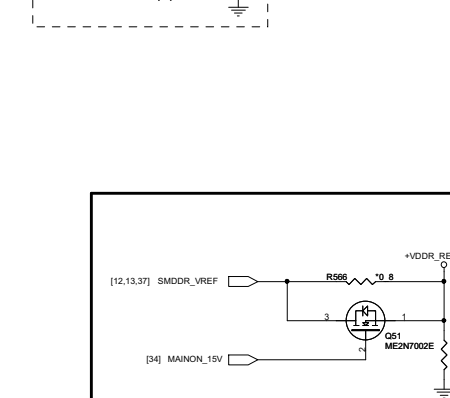
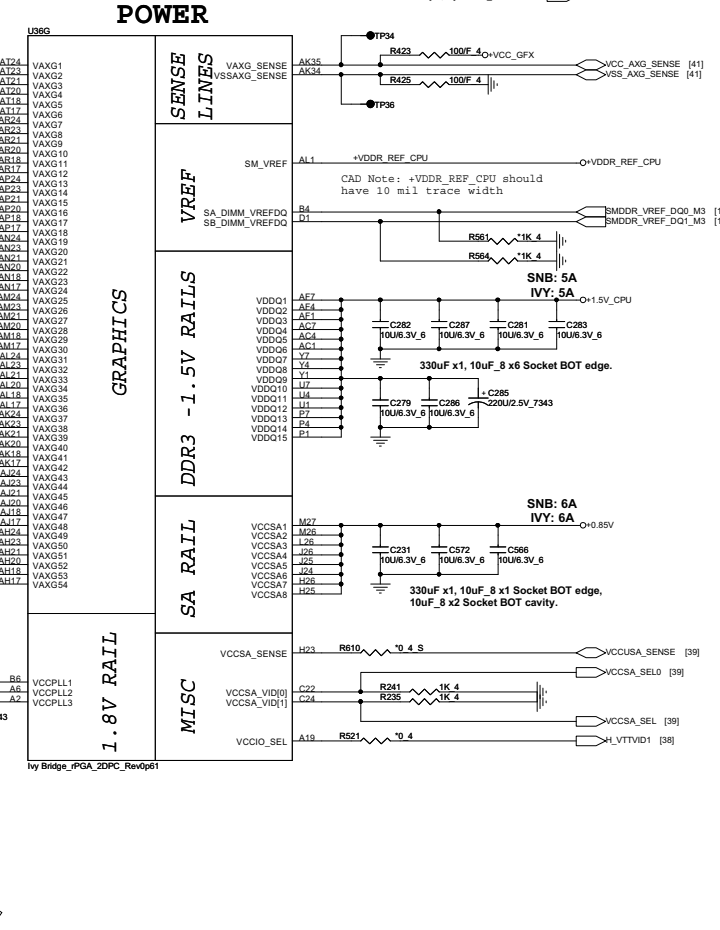
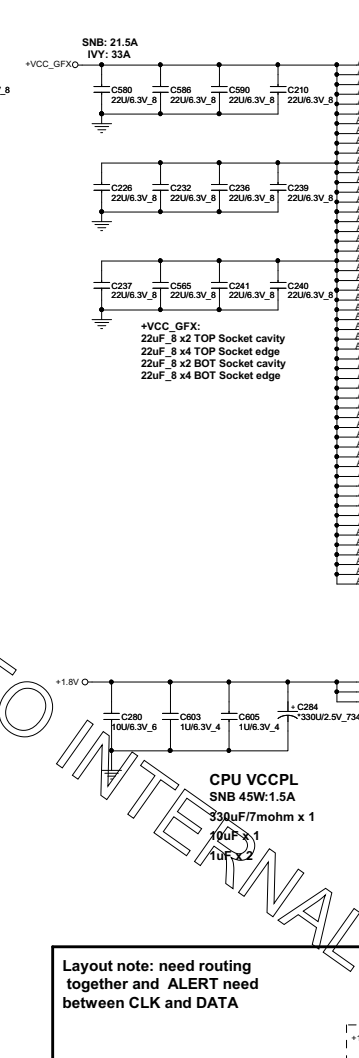
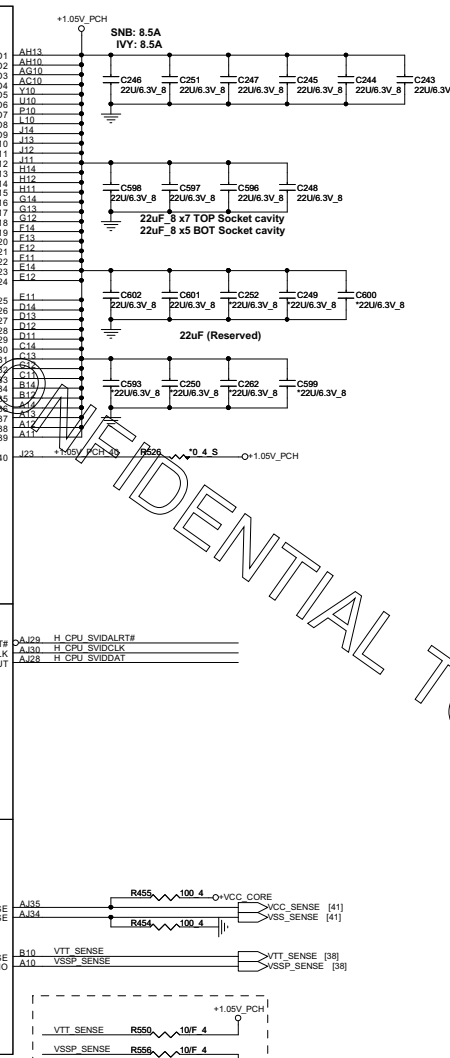
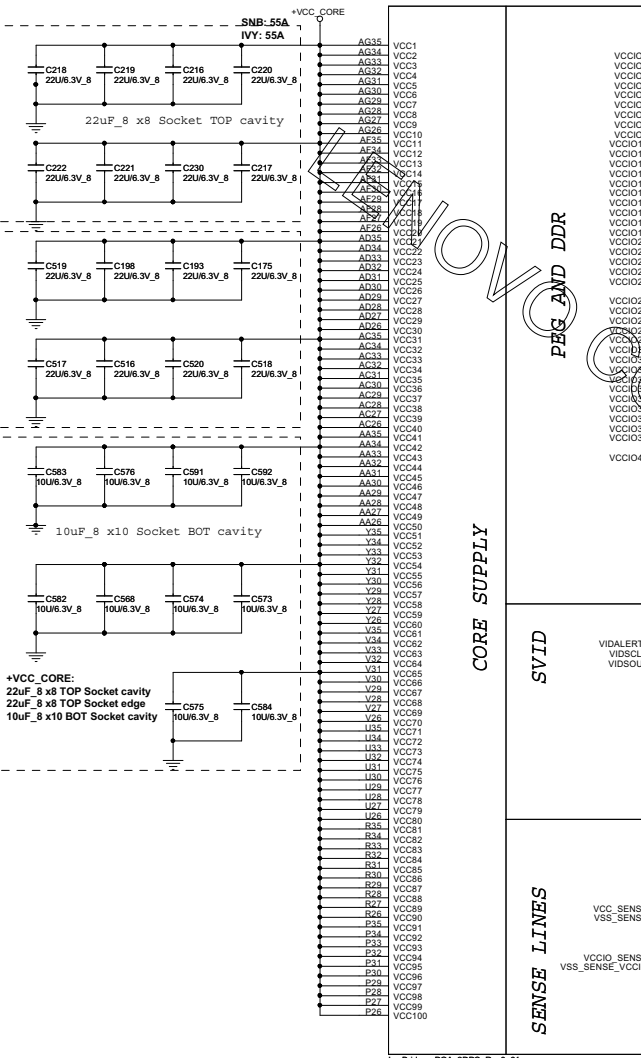
Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge Processor (GRAPHIC POWER)

POWER

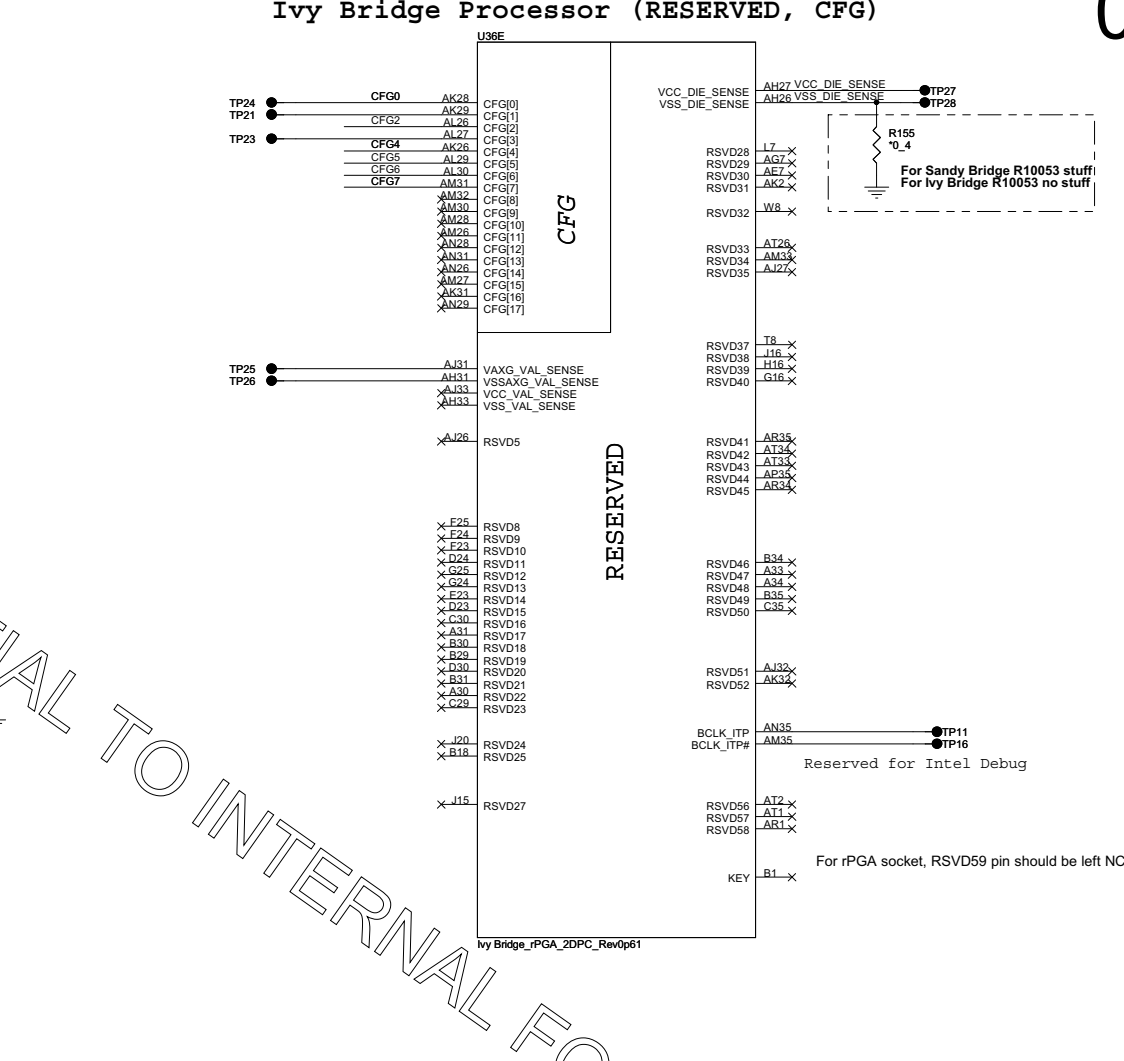
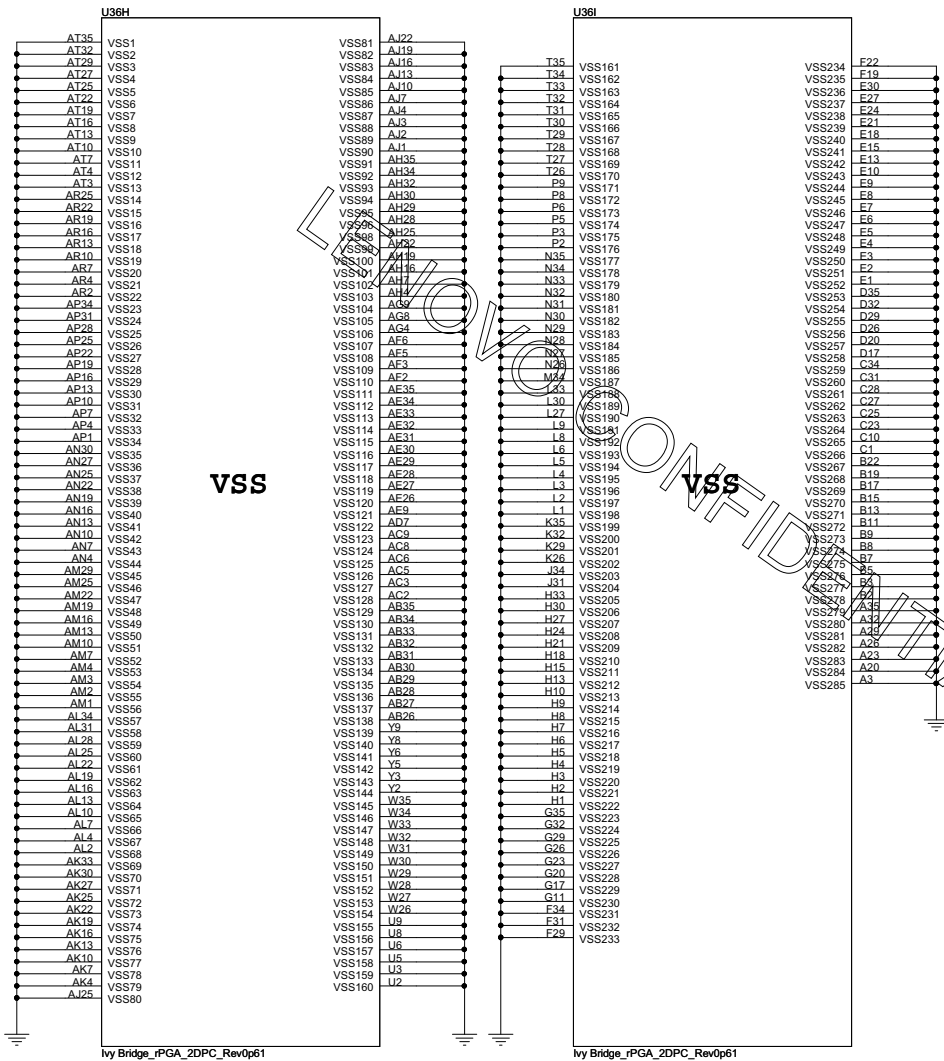
POWER



- Pin list and voltage specifications for various pads including +VCC_CORE, +1.05V_PCH, MAINON_15V, etc.

UNLAWFUL TO REPRODUCE OR TRANSMIT IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM. UNLAWFUL TO REPRODUCE OR TRANSMIT IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM.

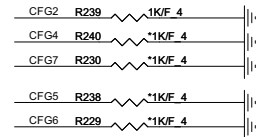
Layout note: need routing together and ALERT need between CLK and DATA. Place PU resistor close to CPU. SVID CLK, SVID DATA, SVID ALERT, CPU VCCPL. PROJECT : L22A - Quantum Computer Inc.



Processor Strapping

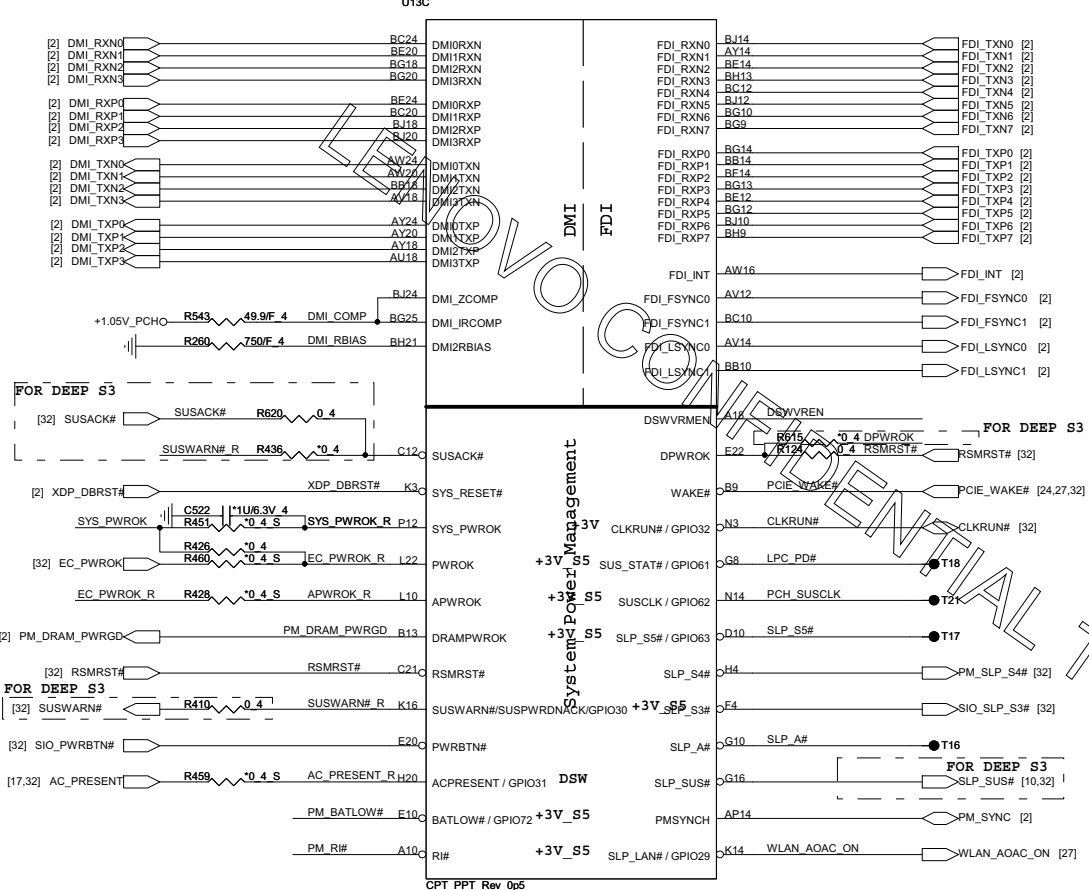
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

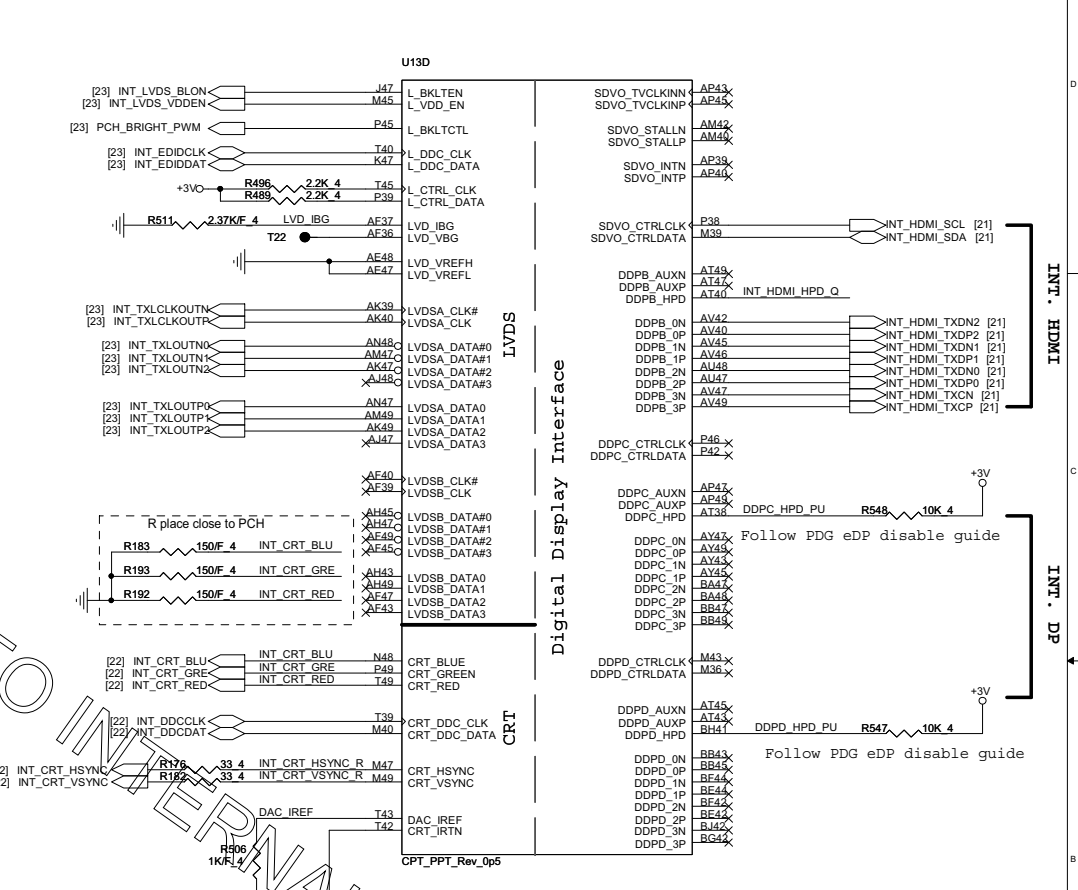


CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

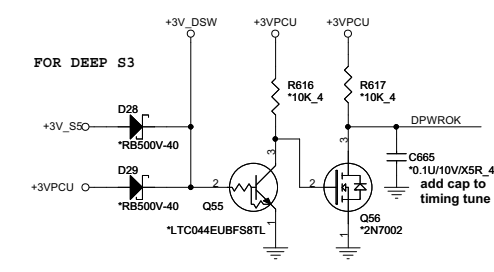
Cougar Point/Panther Point (DMI, FDI, PM)



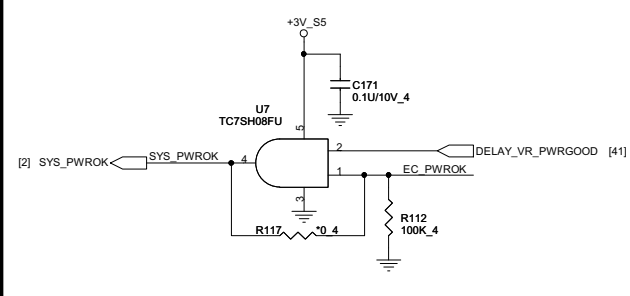
Cougar Point/Panther Point (LVDS, DDI)



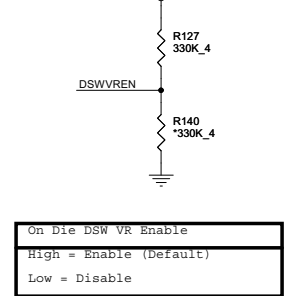
DPWROK FOR DSW (DEEP S3)



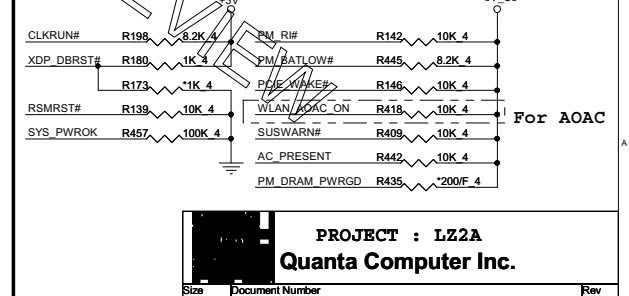
System PWR_OK(CLG)

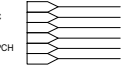


+3V_RTC

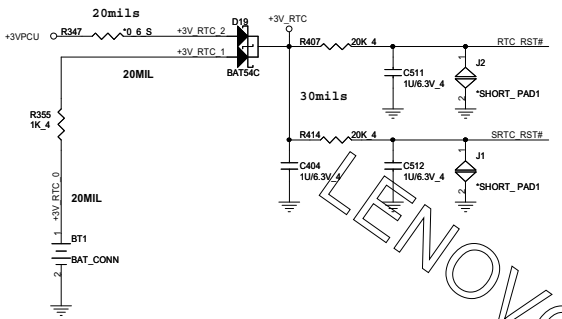


PCH Pull-high/low(CLG)

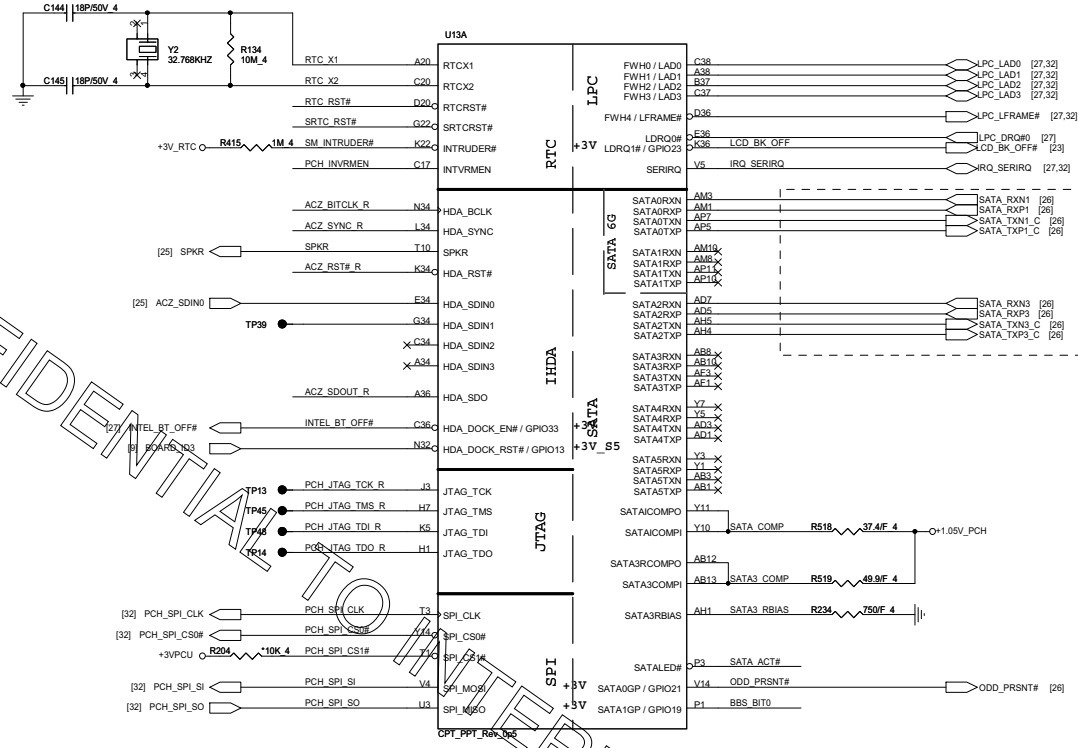




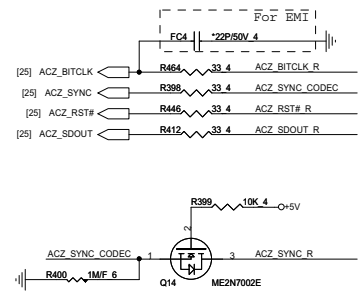
RTC Circuitry(RTC)



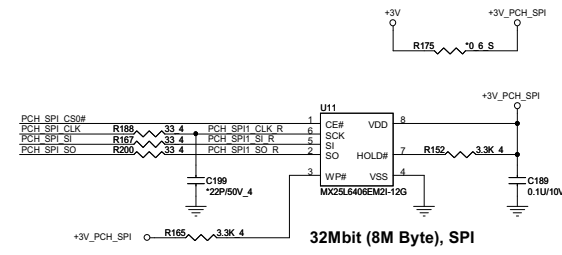
Cougar Point/Panther Point (HDA,JTAG,SATA)



HDA Bus(CLG)

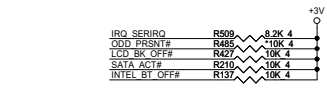


PCH Dual SPI (CLG)



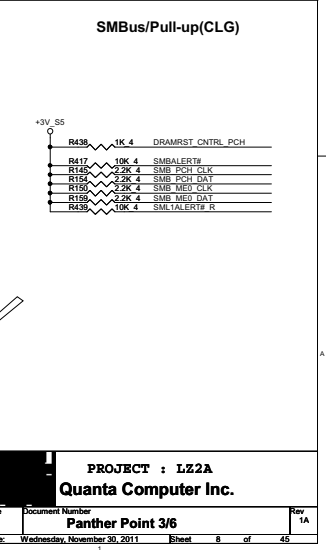
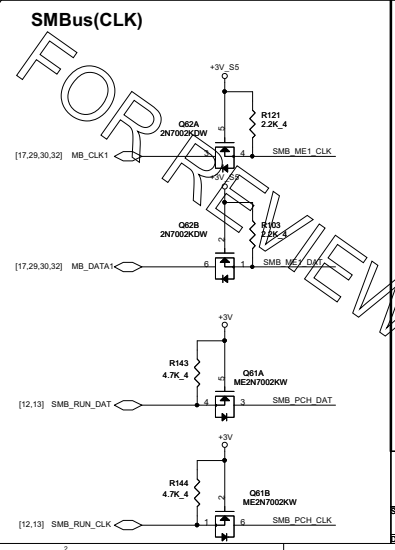
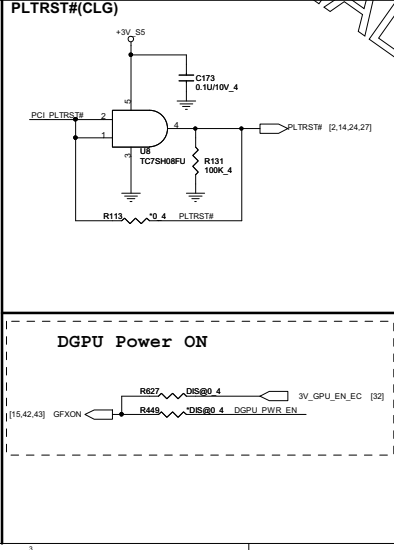
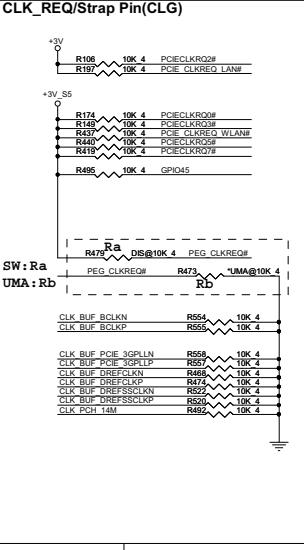
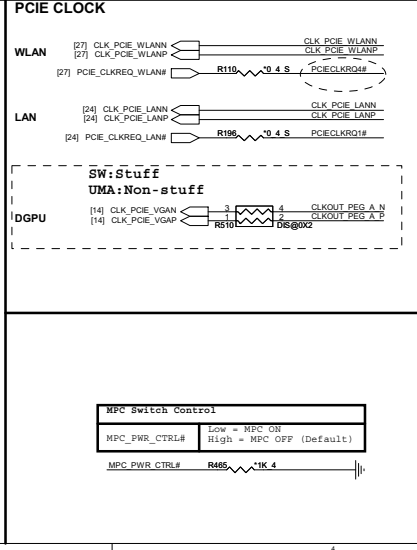
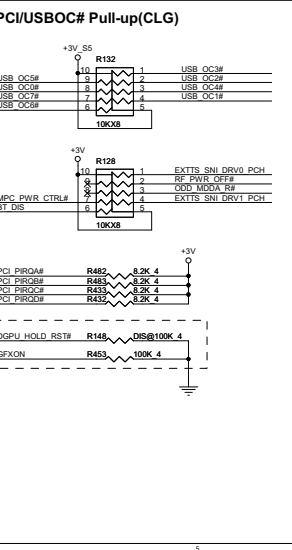
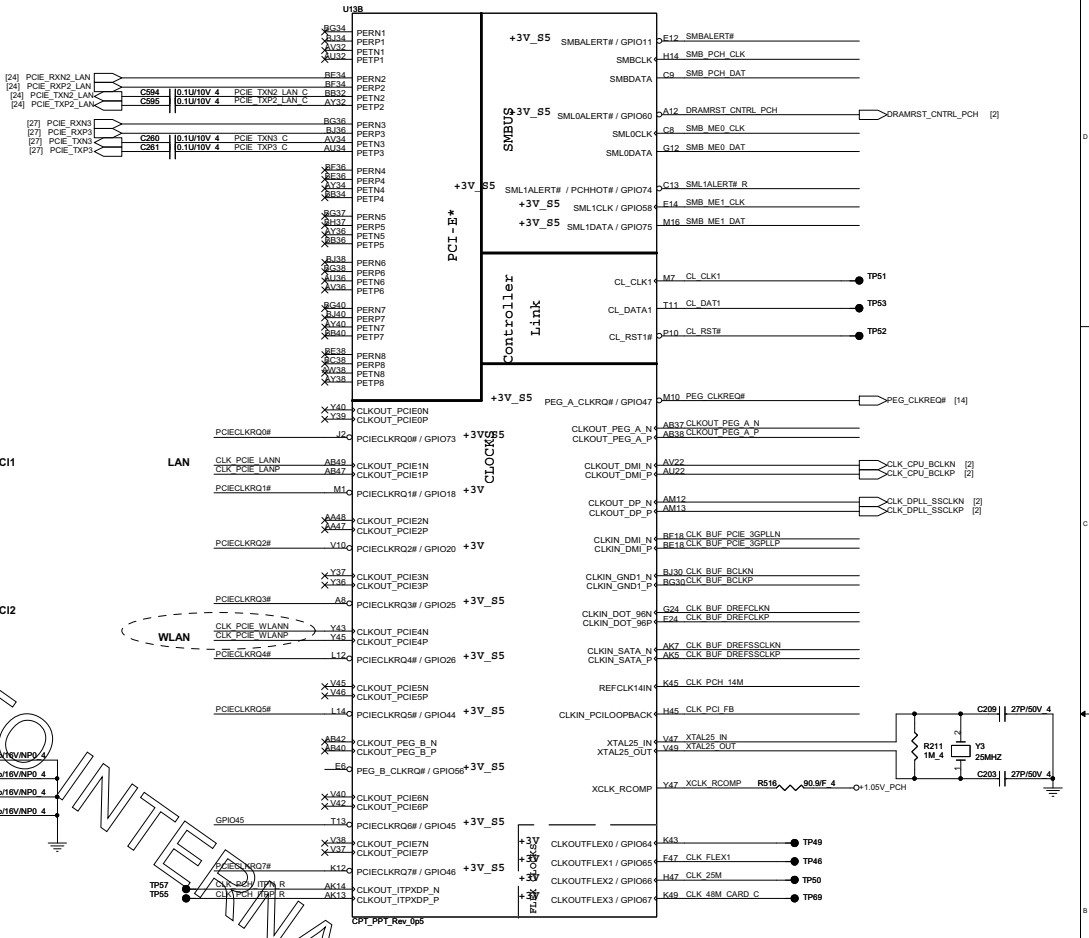
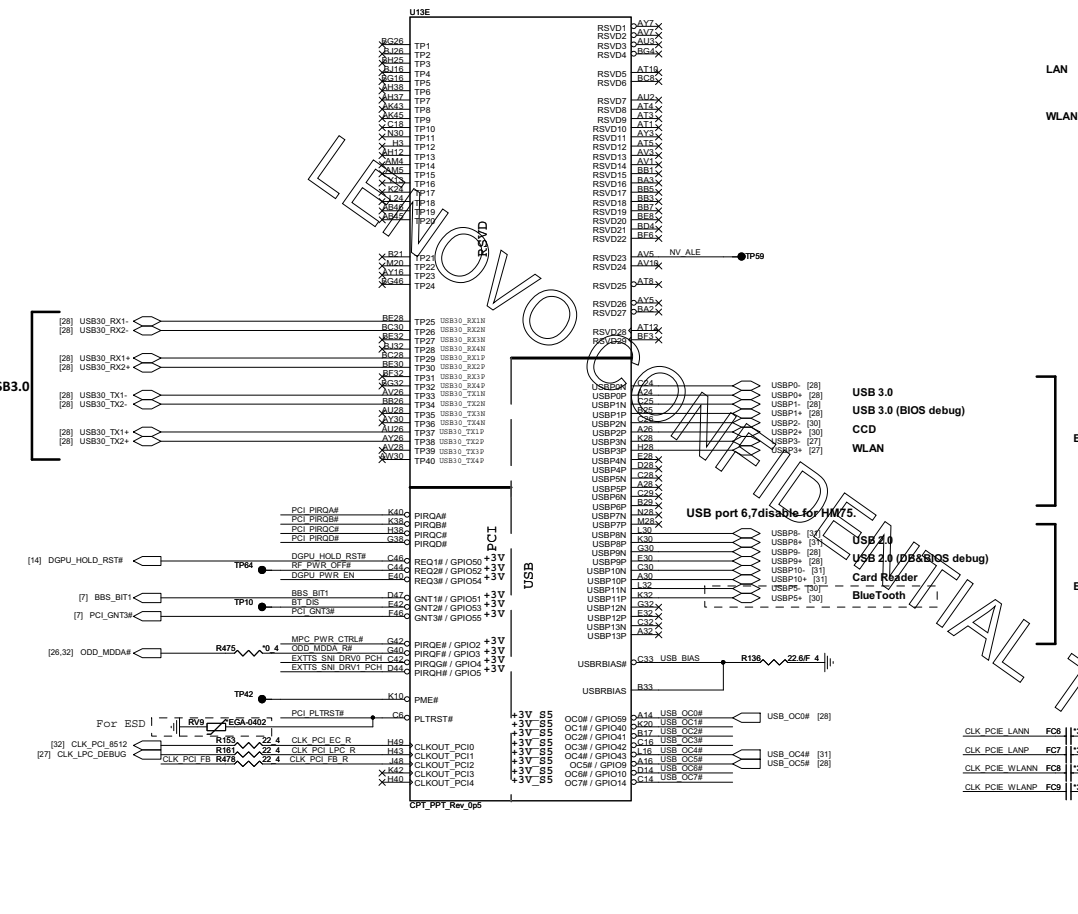
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V0 R515 *1K 4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R472 *1K 4 PCH_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R114 *330K 4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]	R471 *1K 4 BBS_BIT1 [8]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWR0K		R203 *1K 4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 R411 *1K 4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWR0K	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R254 2.2K 4 O+1.8V R255 1K 4 DF_TVS [9] H_SNB_IVB# [2]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R490 *1K 4 PLL_ODDR_EN [9]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R413 *1K 4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWR0K	0 = Default (weak pull-down 20K) 1 = Enable	+3V0 R181 *1K 4 PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWR0K	0 = Disable (Internal pull-down 20kohm)	



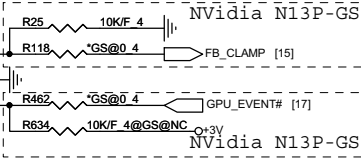
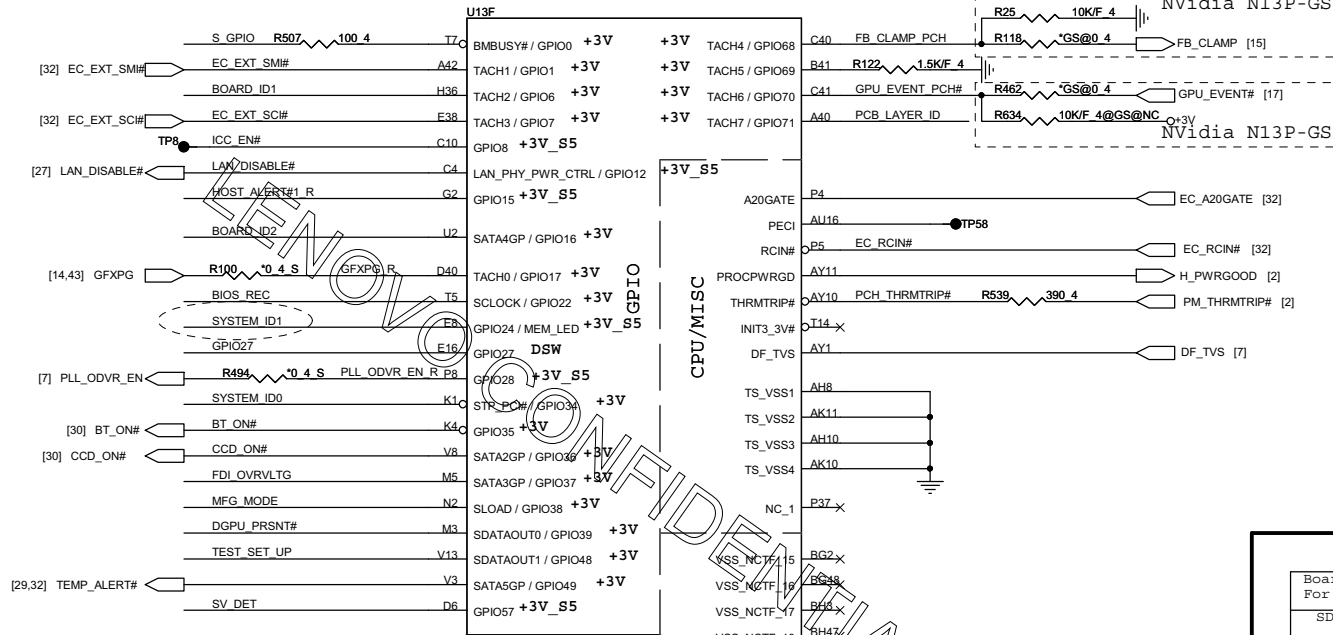
Cougar Point-M/Panther Point (PCI,USB,NVRAM)

Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



Cougar Point/Panther Point (GPIO, VSS_NCTF, RSVD)

[6,7,8,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42,43] +3V_S5 +3V



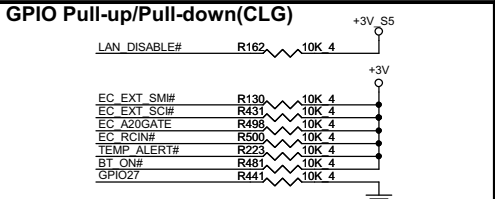
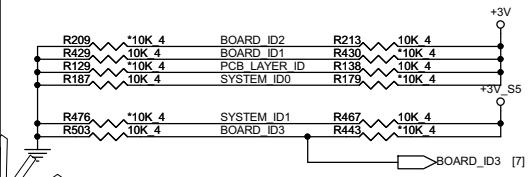
Signal	Pin	Configuration
VSS_NCTF_1	A4	X
VSS_NCTF_2	A44	X
VSS_NCTF_3	A45	X
VSS_NCTF_4	A46	X
VSS_NCTF_5	A5	X
VSS_NCTF_6	A6	X
VSS_NCTF_7	B3	X
VSS_NCTF_8	B47	X
VSS_NCTF_9	BD1	X
VSS_NCTF_10	BD49	X
VSS_NCTF_11	BE1	X
VSS_NCTF_12	BE49	X
VSS_NCTF_13	BE1	X
VSS_NCTF_14	BE49	X
VSS_NCTF_15	BG2	X
VSS_NCTF_16	BG49	X
VSS_NCTF_17	BH4	X
VSS_NCTF_18	BH47	X
VSS_NCTF_19	BJ4	X
VSS_NCTF_20	BJ44	X
VSS_NCTF_21	BJ45	X
VSS_NCTF_22	BJ46	X
VSS_NCTF_23	BJ5	X
VSS_NCTF_24	BJ6	X
VSS_NCTF_25	C2	X
VSS_NCTF_26	C48	X
VSS_NCTF_27	D1	X
VSS_NCTF_28	D49	X
VSS_NCTF_29	E1	X
VSS_NCTF_30	E49	X
VSS_NCTF_31	F1	X
VSS_NCTF_32	F49	X

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV	0	0	0
SIV	0	0	1
SIT	0	1	0
SVT			
SOVP			

Board ID use below GPIO:
BOARD ID1
BOARD ID2
BOARD ID3

PCB_LAYER_ID:
0-->6 layer
1-->8 layer

System ID[0], ID[1]:
-->LZ1 [0,0]
-->LZ2 [0,1]
-->LZ3 [1,0]



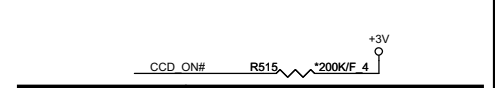
SATA2GP/GPIO26 Reserved

Rising edge of PWRACK

This signal has a weak internal pull-down.

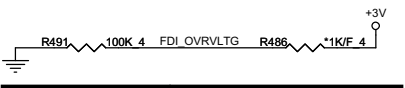
NOTES:

- The internal pull-down is disabled after PLINTR# descends.
- This signal should not be pulled high when strap is



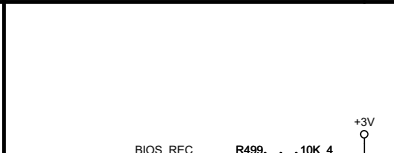
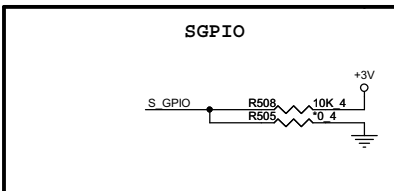
DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



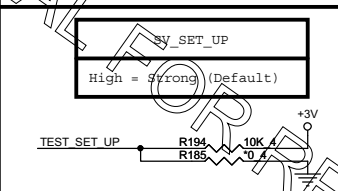
FDI TERMINATION VOLTAGE OVERRIDE

LOW - Tx, Rx terminated to same voltage



BIOS RECOVERY

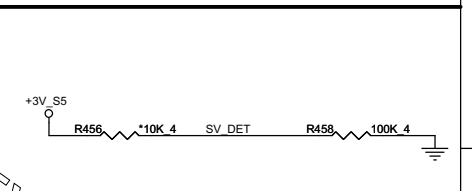
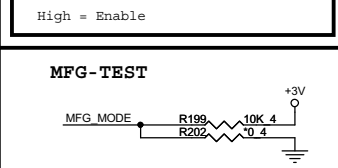
High = Disable (Default)
Low = Enable



HOST ALERT#1_R R466 1K 4

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)
High = Enable



Signal	SWITCHABLE	UMA
Stuff	R186	R195
Stuff	R195	R186

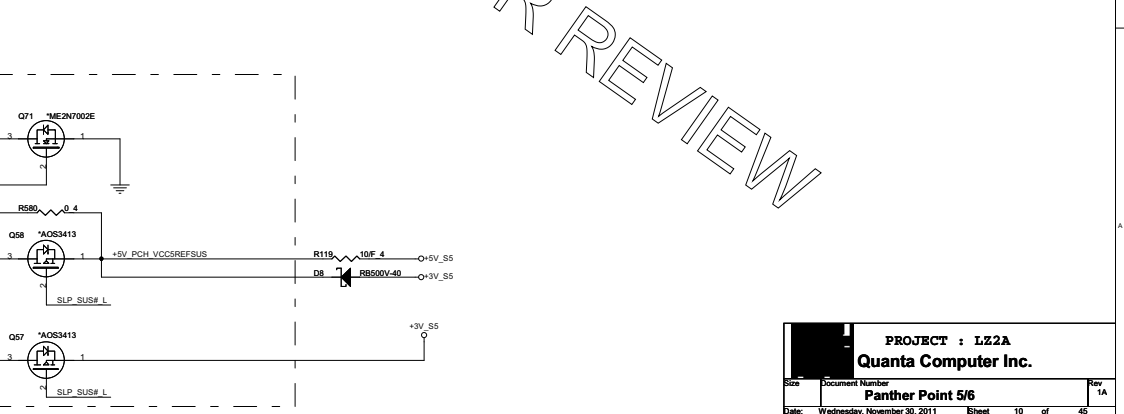
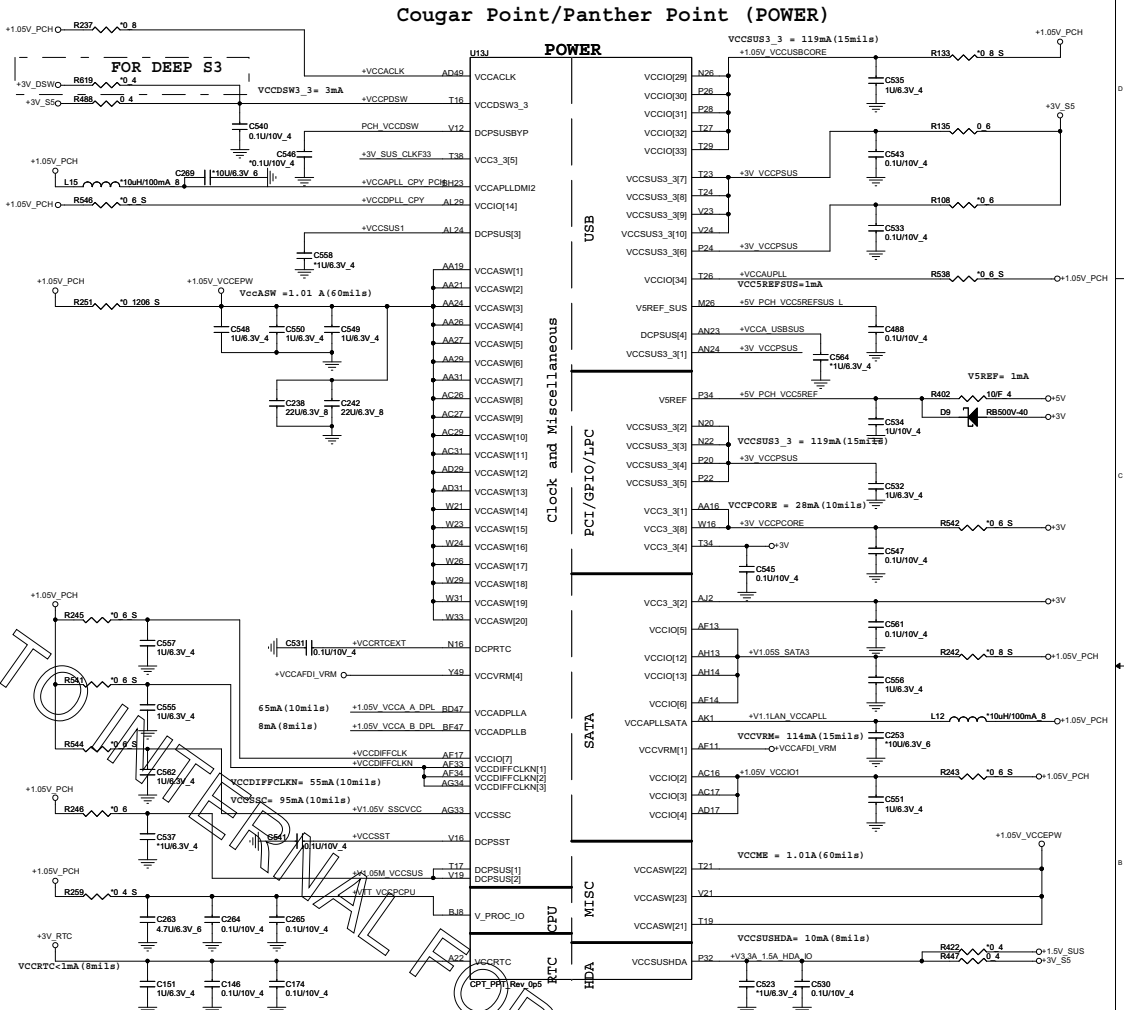
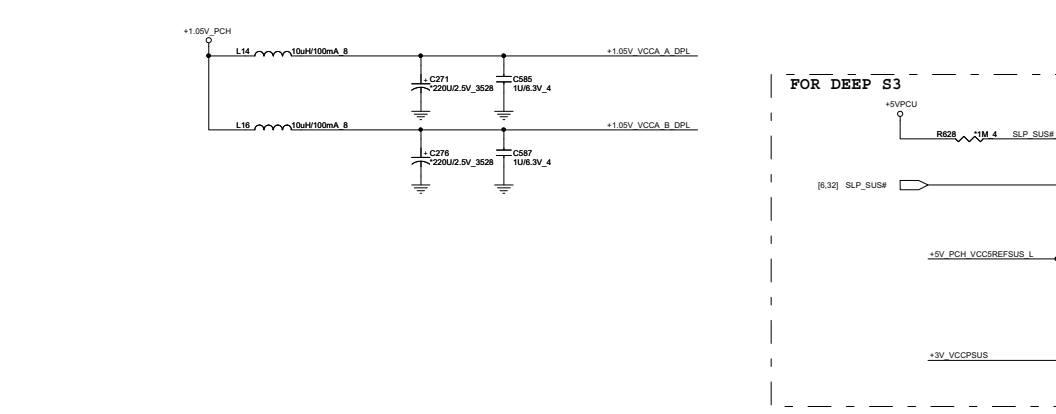
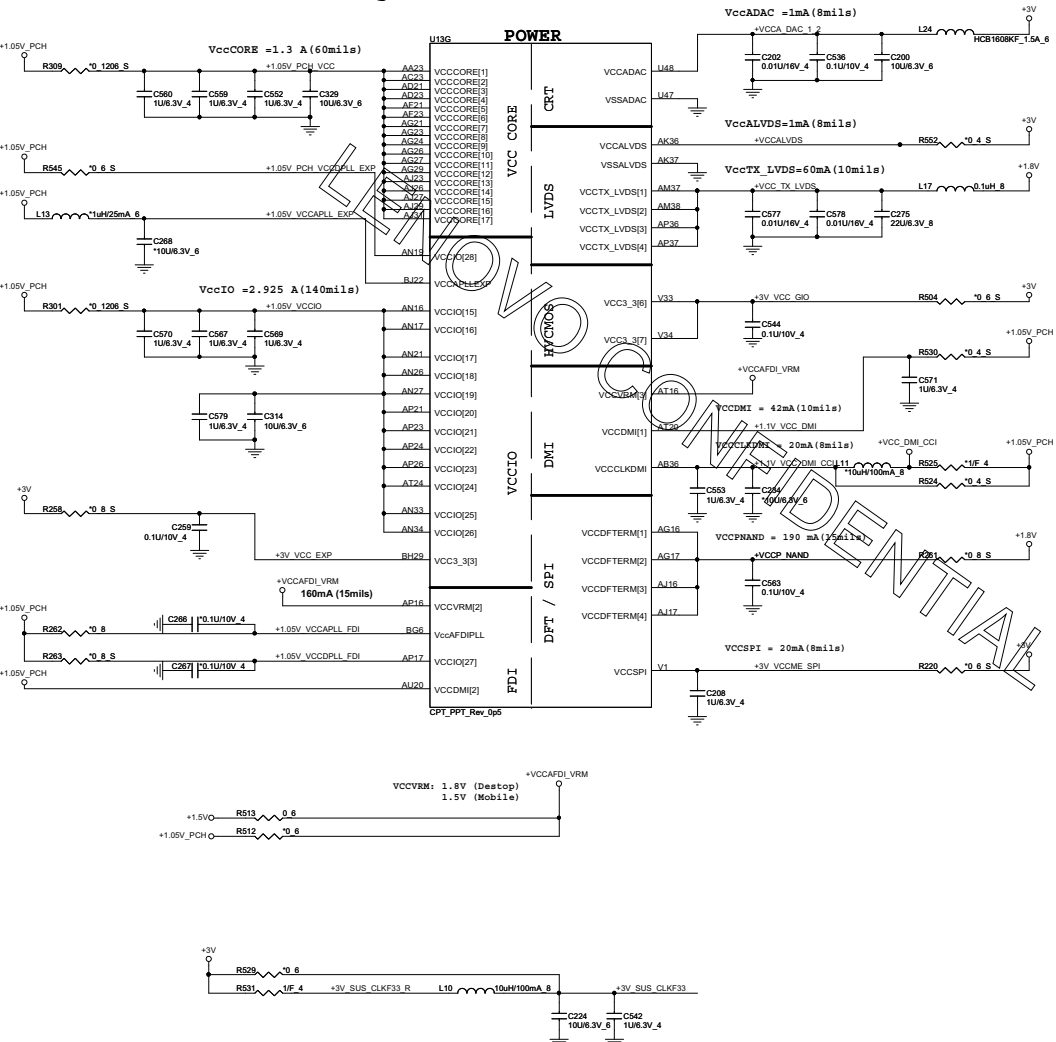
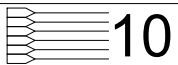
PROJECT : LZ2A
Quanta Computer Inc.

Size Document Number
Panther Point 4/6

Date: Wednesday, November 30, 2011 Sheet 9 of 45 Rev 1A

Cougar Point/Panther Point (POWER)

[2,4,7,8,33,34,38,43]	+1.05V_PCH
[6,7,32]	+3V_RTC
[2,6,7,8,9,27,31,34]	+3V_S5
[23,26,28,31,33,34]	+5V_S5
[7,21,22,25,26,29,30,33,34]	+5V



Cougar Point/Panther Point (GND)

U13H		H5	
VSS[0]		VSS[0]	
VSS[1]		VSS[1]	
VSS[2]		VSS[2]	
VSS[3]		VSS[3]	
VSS[4]		VSS[4]	
VSS[5]		VSS[5]	
VSS[6]		VSS[6]	
VSS[7]		VSS[7]	
VSS[8]		VSS[8]	
VSS[9]		VSS[9]	
VSS[10]		VSS[10]	
VSS[11]		VSS[11]	
VSS[12]		VSS[12]	
VSS[13]		VSS[13]	
VSS[14]		VSS[14]	
VSS[15]		VSS[15]	
VSS[16]		VSS[16]	
VSS[17]		VSS[17]	
VSS[18]		VSS[18]	
VSS[19]		VSS[19]	
VSS[20]		VSS[20]	
VSS[21]		VSS[21]	
VSS[22]		VSS[22]	
VSS[23]		VSS[23]	
VSS[24]		VSS[24]	
VSS[25]		VSS[25]	
VSS[26]		VSS[26]	
VSS[27]		VSS[27]	
VSS[28]		VSS[28]	
VSS[29]		VSS[29]	
VSS[30]		VSS[30]	
VSS[31]		VSS[31]	
VSS[32]		VSS[32]	
VSS[33]		VSS[33]	
VSS[34]		VSS[34]	
VSS[35]		VSS[35]	
VSS[36]		VSS[36]	
VSS[37]		VSS[37]	
VSS[38]		VSS[38]	
VSS[39]		VSS[39]	
VSS[40]		VSS[40]	
VSS[41]		VSS[41]	
VSS[42]		VSS[42]	
VSS[43]		VSS[43]	
VSS[44]		VSS[44]	
VSS[45]		VSS[45]	
VSS[46]		VSS[46]	
VSS[47]		VSS[47]	
VSS[48]		VSS[48]	
VSS[49]		VSS[49]	
VSS[50]		VSS[50]	
VSS[51]		VSS[51]	
VSS[52]		VSS[52]	
VSS[53]		VSS[53]	
VSS[54]		VSS[54]	
VSS[55]		VSS[55]	
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VSS[62]		VSS[62]	
VSS[63]		VSS[63]	
VSS[64]		VSS[64]	
VSS[65]		VSS[65]	
VSS[66]		VSS[66]	
VSS[67]		VSS[67]	
VSS[68]		VSS[68]	
VSS[69]		VSS[69]	
VSS[70]		VSS[70]	
VSS[71]		VSS[71]	
VSS[72]		VSS[72]	
VSS[73]		VSS[73]	
VSS[74]		VSS[74]	
VSS[75]		VSS[75]	
VSS[76]		VSS[76]	
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VSS[79]		VSS[79]	

CPT_PPT_Rev_0p5

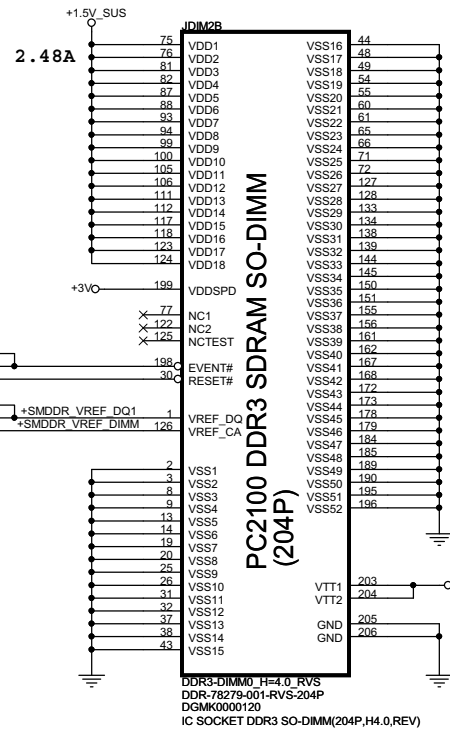
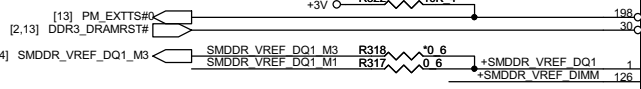
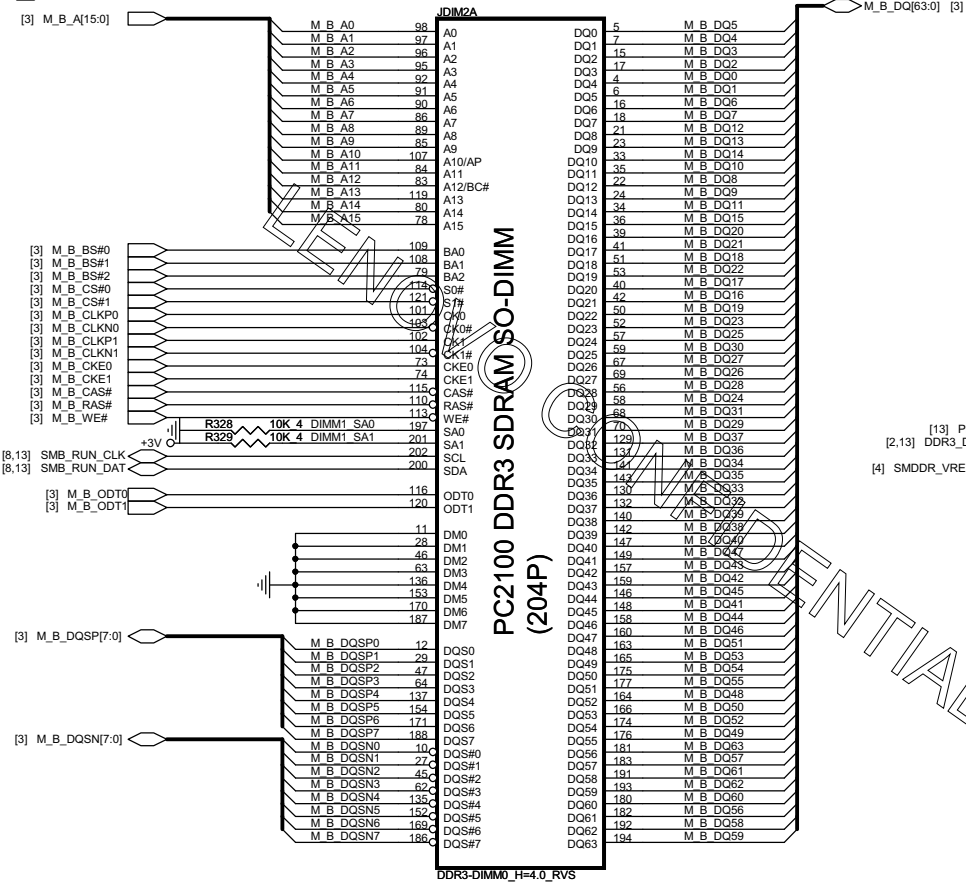
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VSS[164]		VSS[264]	
VSS[165]		VSS[265]	
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VSS[175]		VSS[275]	
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VSS[177]		VSS[277]	
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VSS[186]		VSS[286]	
VSS[187]		VSS[287]	
VSS[188]		VSS[288]	
VSS[189]		VSS[289]	
VSS[190]		VSS[290]	
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VSS[246]		VSS[346]	
VSS[247]		VSS[347]	
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VSS[251]		VSS[351]	
VSS[252]		VSS[352]	
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VSS[257]			
VSS[258]			

CPT_PPT_Rev_0p5

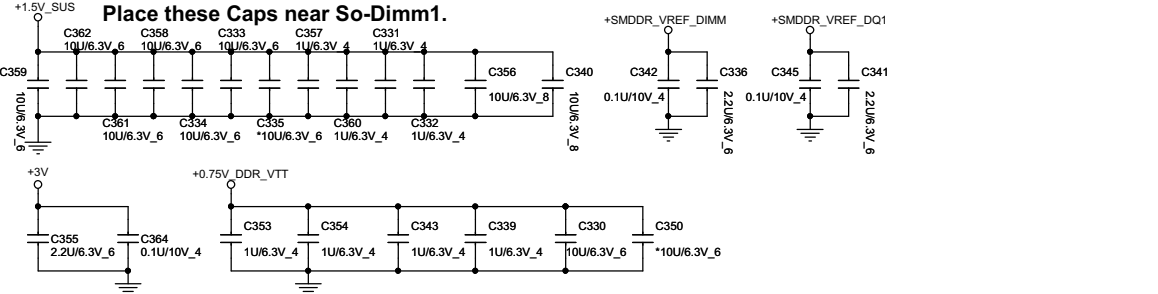
LENVOV CONFIDENTIAL TO INTERNAL FOR REVIEW

PROJECT : LZ2A
Quanta Computer Inc.

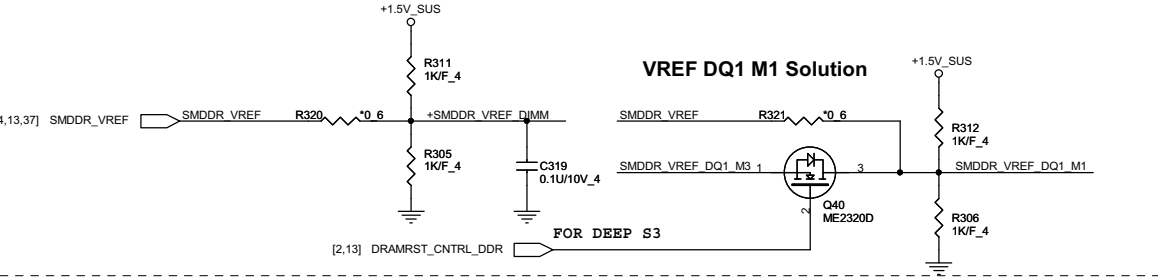
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Date:	Wednesday, November 30, 2011	Sheet 11 of 45

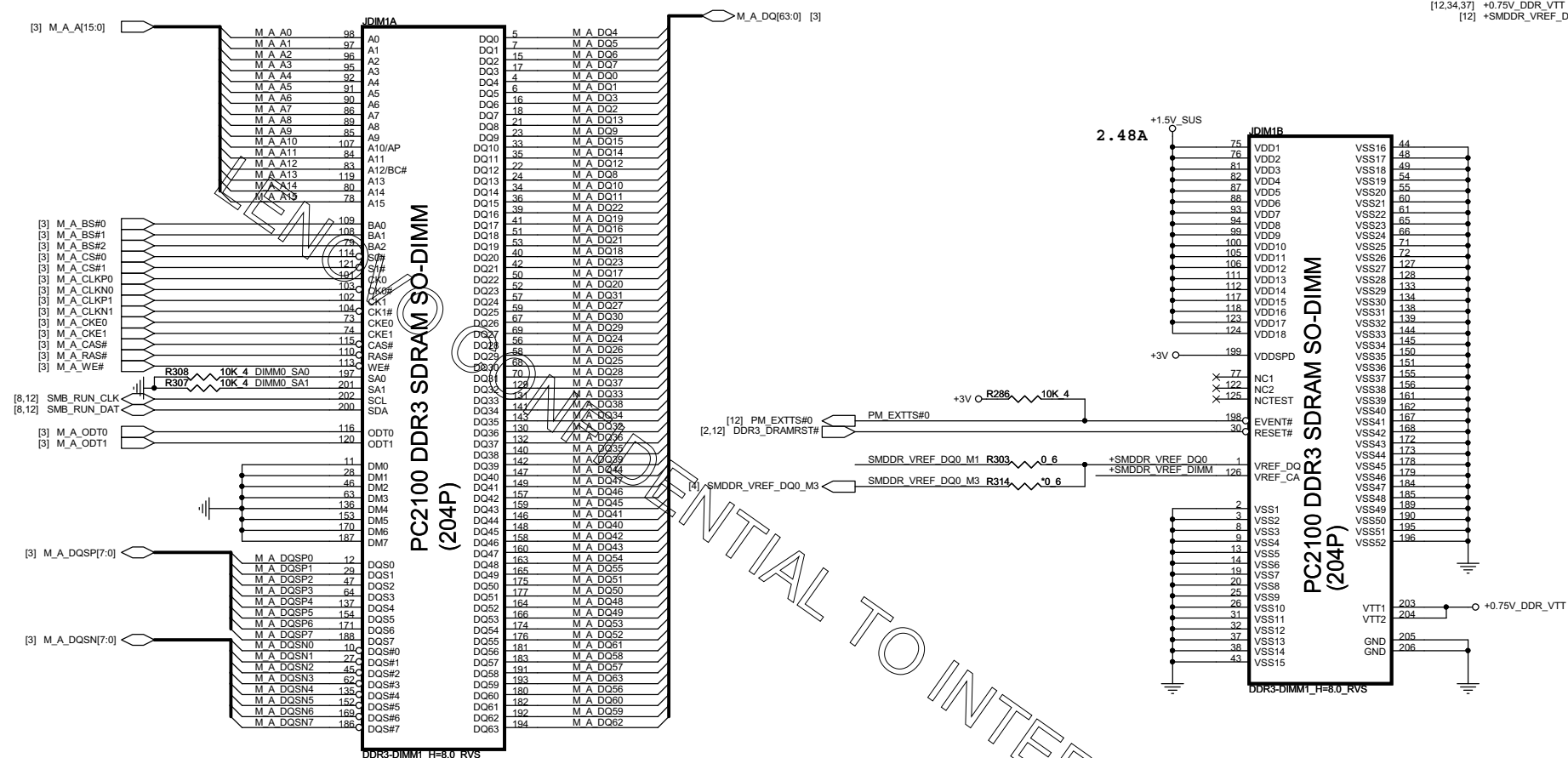


Place these Caps near So-Dimm1.

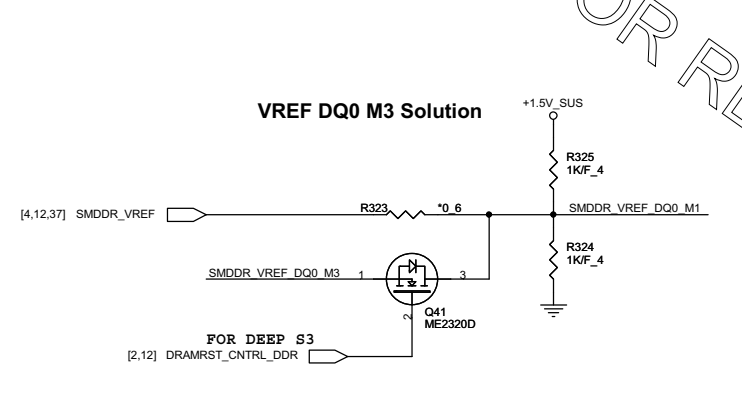
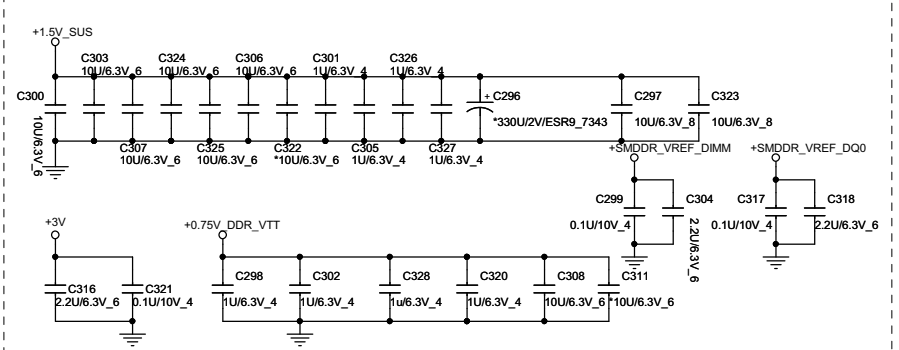


VREF DQ1 M1 Solution



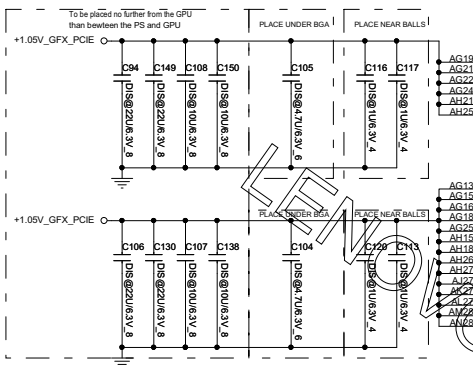


Place these Caps near So-Dimm0.

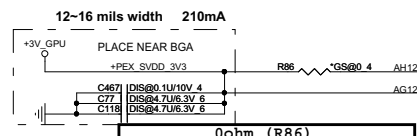


CONFIDENTIAL TO INTERNAL FOR REVIEW

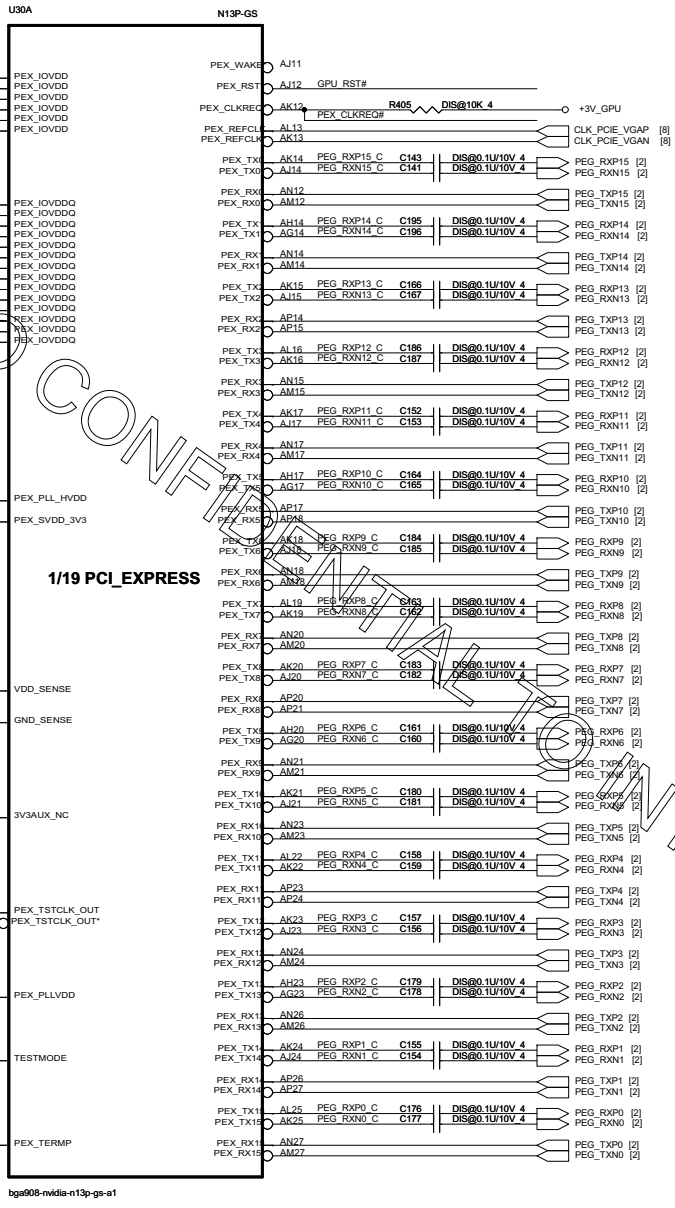
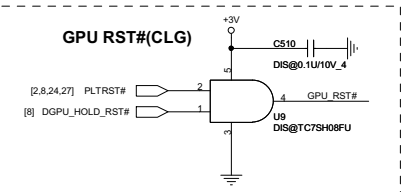
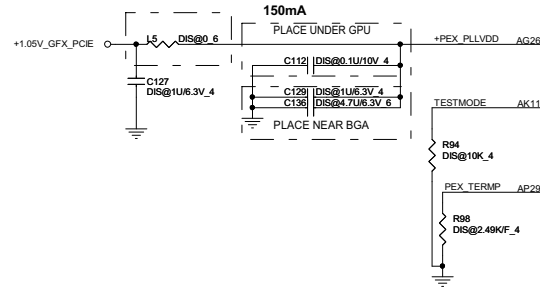
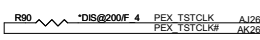
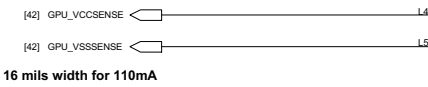
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >3.45A



CAP CLOSE TO BGA



0ohm (R86)	
N13P-GS (GK107)	Stuff
N13P-GL (GF108)	unstuff
N13M-GEL (GF119)	unstuff



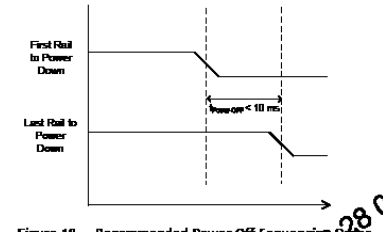
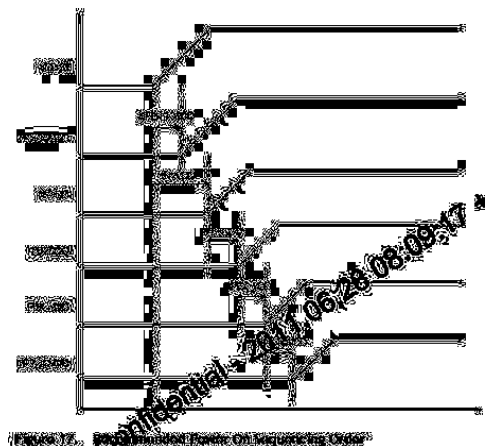
1/19 PCI_EXPRESS

PEG Capacitance	
N13P-GS (GK107)	CH4222K9B04: CAP CHIP 0.22U 10V (+-10%, X5R, 0402)
N13P-GL (GF108)	CH41002KB93: CAP CHIP 0.1U 10V (+-10%, X5R, 0402)
N13M-GEL (GF119)	CH41002KB93: CAP CHIP 0.1U 10V (+-10%, X5R, 0402)

All GPU power rails must ramp up after VDD3. The following conditions must be met:

- ▶ INVDD > 0
- ▶ IPEXIOVDD > 0
- ▶ PEX_VDD > 0
- ▶ IPEXIOVDD > 0

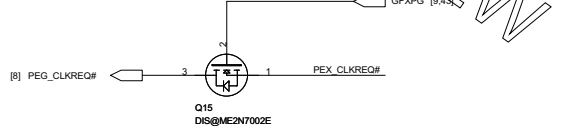
▶ The ramp time for any rail must be more than 40 ns.

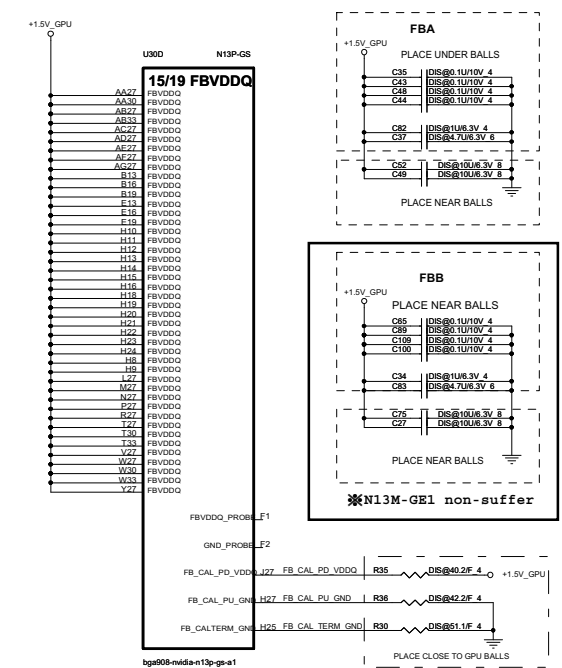
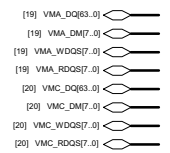
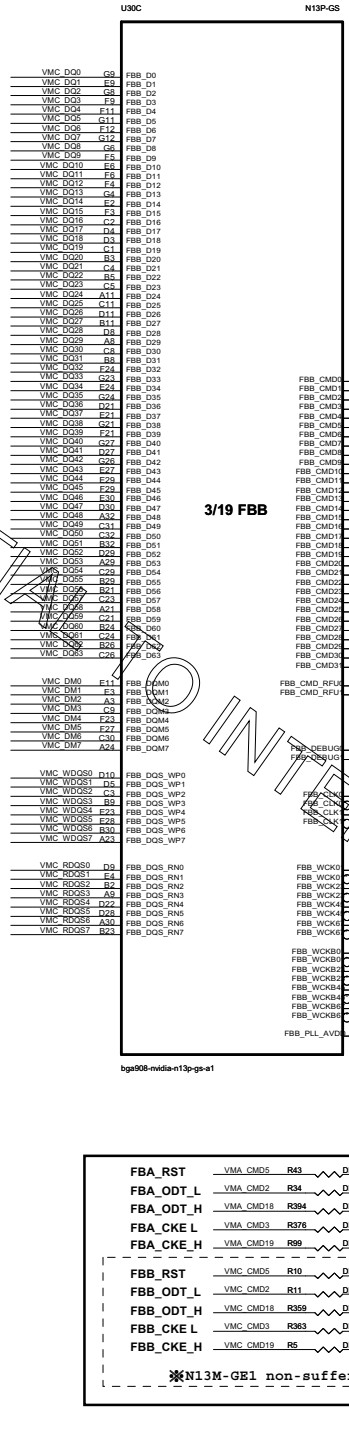
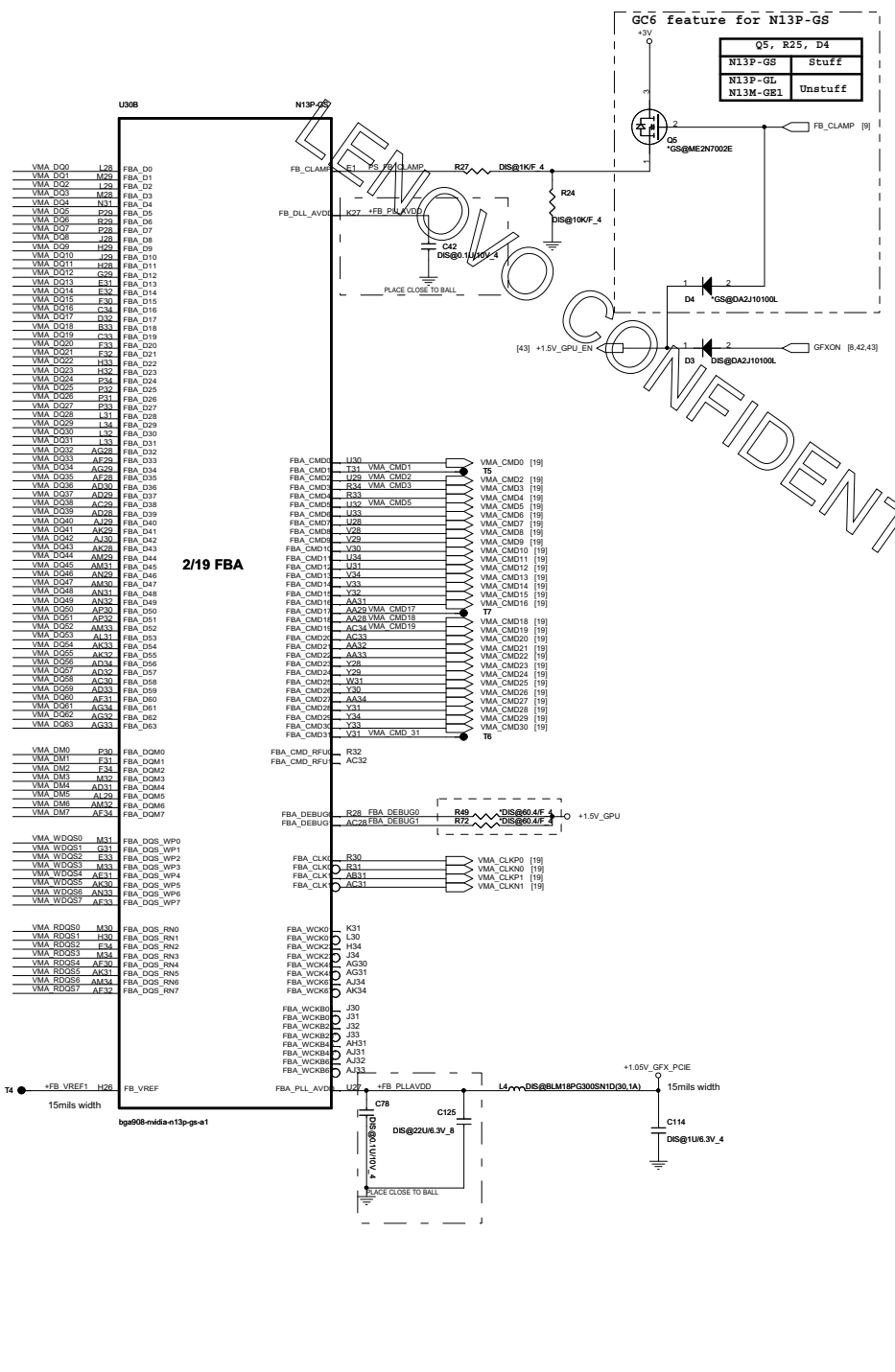


For power-down sequence



PEG CLK detect

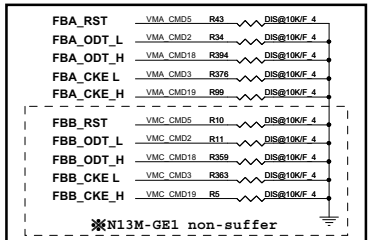


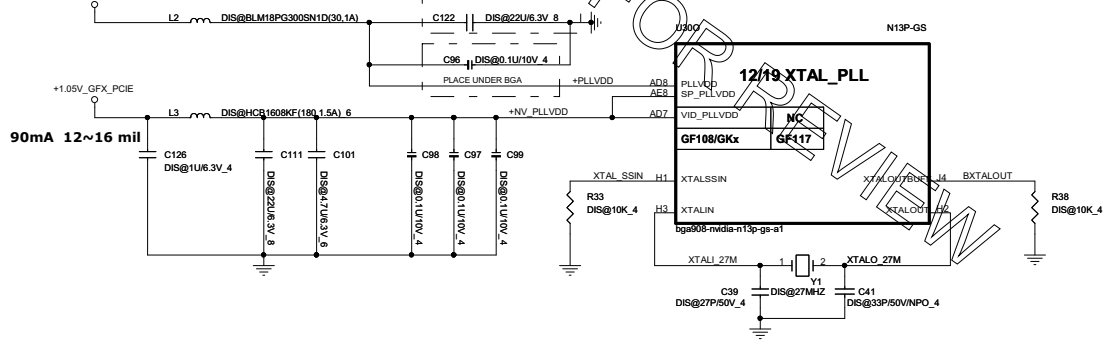
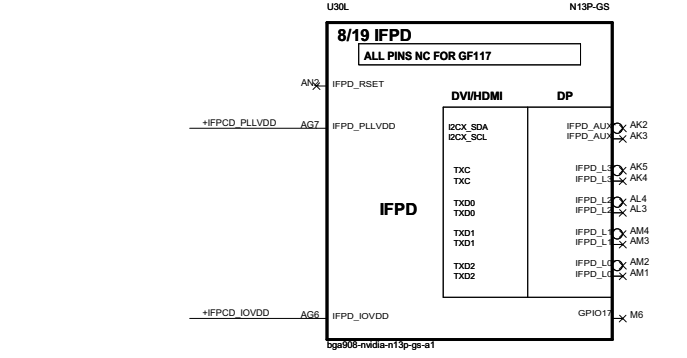
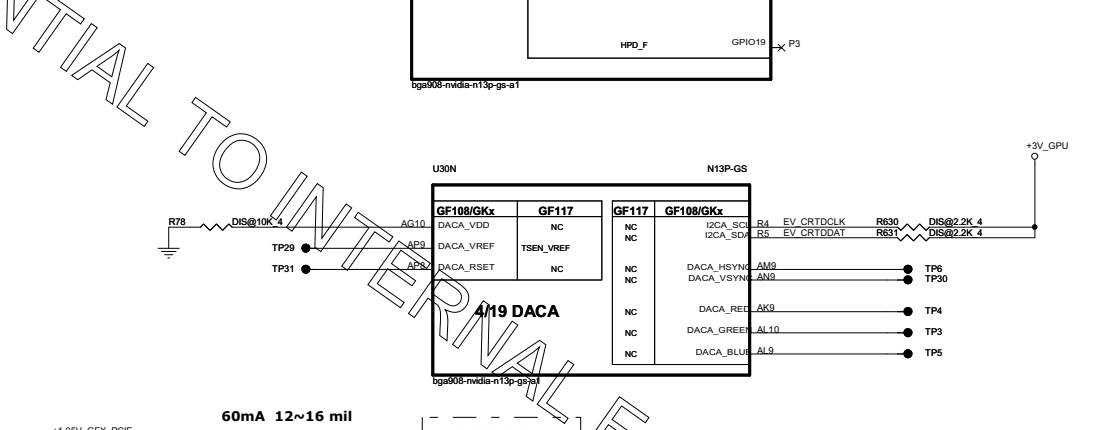
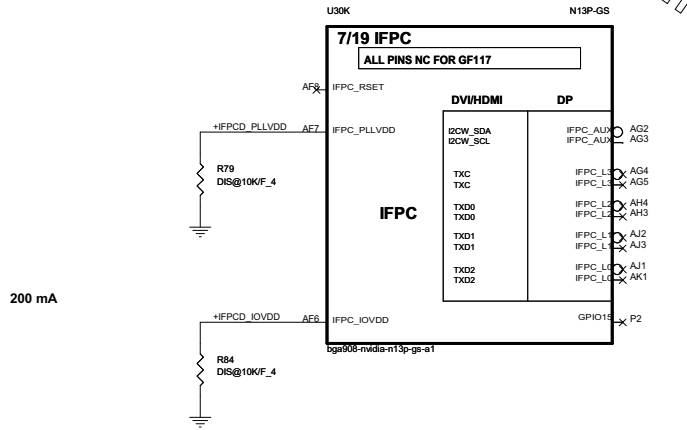
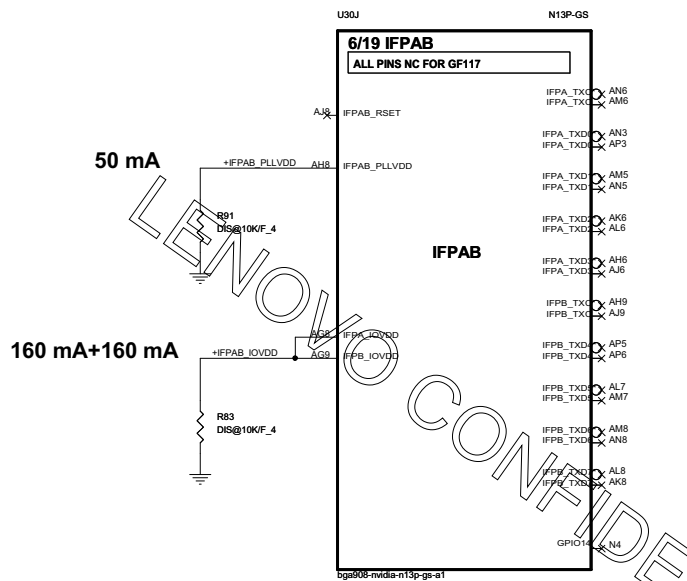


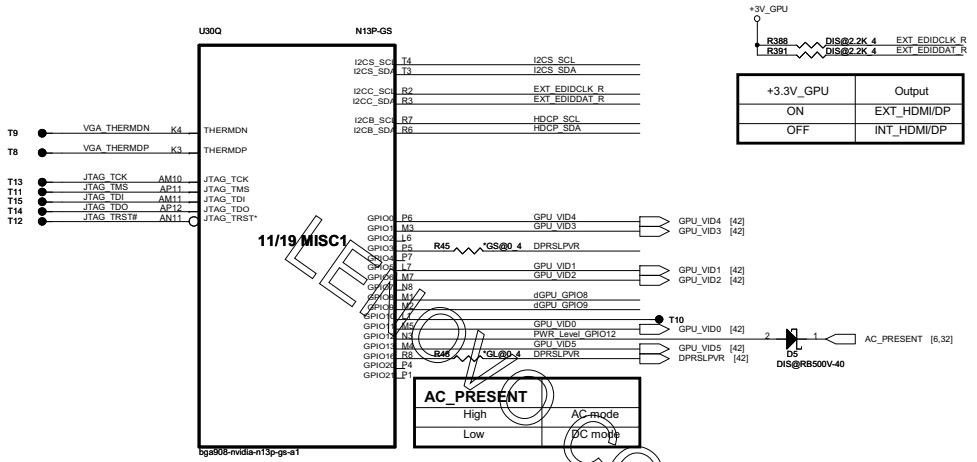
CALIBRATION PIN		DDR3
FB_CALX_PD_VDDQ	R29	40.2
FB_CALX_PD_GND	R30	42.2
FB_CALX_TERM_GND	R31	51.1

Table 1-1 Default GPU Drive Calibration for DDR3

DDR3	1.5V	42.20	40.20	51.10







Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0] XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0] 1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0] 0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0] XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED 0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V XXXX

Resistance	Quanta PN	DESCRIPTION
4.99K/F_4	CS24992FB26	RES CHIP 4.99K 1/16W +1%(0402)
10K/F_4	CS31002FB26	RES CHIP 10K 1/16W +1% (0402)
15K/F_4	CS31502FB24	RES CHIP 15K 1/16W +1% (0402)
20K/F_4	CS32002FB29	RES CHIP 20K 1/16W +1%(0402)
24.9K/F_4	CS32492FB16	RES CHIP 24.9K 1/16W +1%(0402)
30K/F_4	CS33002FB13	RES CHIP 30K 1/16W +1%(0402)
34.8K/F_4	CS33482FB22	RES CHIP 34.8K 1/16W +1%(0402)
45.3K/F_4	CS34532FB18	RES CHIP 45.3K 1/16W +1% (0402)

VRAM Configure	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN	RAMCFG [3:0]	ROM_SI
900MHz 2GB(128M*16) Samsung	AKDSMGWT500		K4W2G1646C-HC11	0x7(0111)	R87 (45.3K ohm)
900MHz 2GB(128M*16) Hynix	AKDSMGWTW00		H5TQ2G63BFR-11C	0x6(0110)	R87 (34.8K ohm)
900MHz 1GB(64M*16) Samsung	AKDEGGT500		K4W1G1646C-BC11	0x3(0011)	R87 (20K ohm)
900MHz 1GB(64M*16) Hynix	AKDSLZWTW02		H5TQ1G63DR-11C	0x2(0010)	R87 (15K ohm)

Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU Model Strap Table

GPU Model	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1-A1 (GF119)	R73 (30K ohm) PD	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R47 (4.99K ohm) PU	R52 (4.99K ohm) PD	R56 (10K ohm) PD
N13P-GL-A1 (GF108)	R73 (10K ohm) PD	R76 (15K ohm) PD	R383 (45.3K ohm) PU	R41 (45.3K ohm) PD	R47 (10K ohm) PU	NA	NA
N13P-GS-A2 (GK107)	R69 (10K ohm) PU	R77 (4.99K ohm) PU	R383 (45.3K ohm) PU	R41 (34.8K ohm) PD	R42 (15K ohm) PD	R52 (4.99K ohm) PD	R56 (10K ohm) PD

Using internal thermal sensor

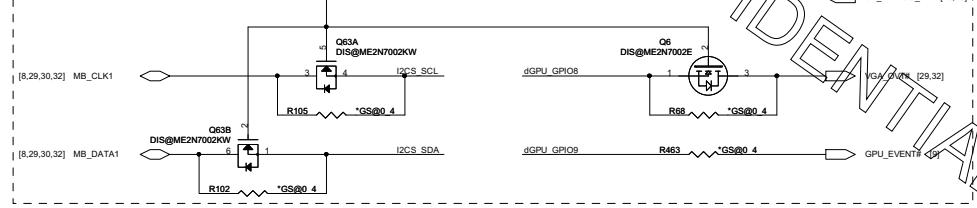
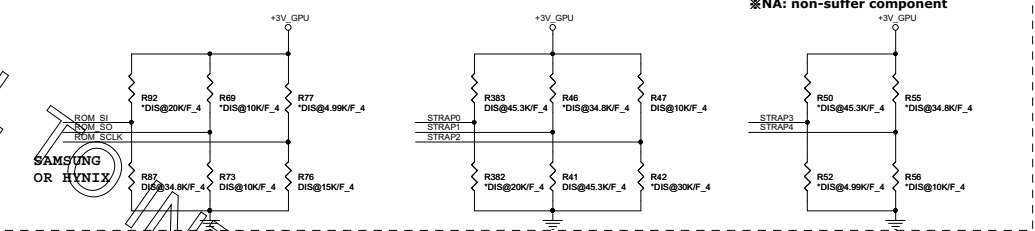


Table 5. Stuffing Options

Model	DC and GPIO	Options
N13M-GE1/GS/4P, N13P-Q1-Q3	DC and GPIO	No stuff FET Stuff IO bypass resistor
	JVMISC	Stuff FET No stuff IO bypass resistor
Other N13P and N13M	DC and GPIO	Stuff FET No stuff IO bypass resistor
	JVMISC	No stuff FET Stuff IO bypass resistor

	Q6, Q63, R81, R104	R68, R102, R105, R463
N13P-GS	Unstuff	Stuff
N13P-GL	Stuff	Unstuff
N13M-GE1	Stuff	Unstuff



GPU Model	N13M-GE1-A1 (GF119)		N13P-GL-A1 (GF108)		N13P-GS-A1 (GK107)	
	GPU_VID0	GPU_VID1	GPU_VID2	GPU_VID3	GPU_VID4	GPU_VID5
	0 (R66)	0 (R62)	0 (R58)	0 (R57)	1 (R71)	1 (R385)
	0 (R62)	0 (R62)	1 (R59)	1 (R54)	0 (R40)	1 (R385)
	0 (R58)	0 (R58)	0 (R58)	0 (R57)	0 (R40)	1 (R385)
	0 (R57)	0 (R57)	1 (R54)	1 (R54)	0 (R40)	1 (R385)
	1 (R71)	1 (R71)	0 (R40)	0 (R40)	1 (R71)	1 (R385)
	1 (R385)	1 (R385)	1 (R385)	1 (R385)	1 (R385)	1 (R385)

GPIO ASSIGNMENTS

GPIO	GPU_VID#	Function
GPIO0	GPU_VID4	GPU Core VDD VID4
GPIO1	GPU_VID3	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	Panel Backlight PWM brightness control
GPIO3	LCD_VCC or PS1	Panel Power Enable or PS1 Enable
GPIO4	LCD_BLEN	Panel Backlight Enable
GPIO5	GPU_VID1	GPU Core VDD VID1
GPIO6	GPU_VID2	GPU Core VDD VID2
GPIO7	3D Vision	3D Motion/3D Right signal
GPIO8	OVERT	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	Memory VREF Control
GPIO11	GPU_VID0	GPU Core VDD VID0
GPIO12	PWR_LED	AC power detect or power supply overdraw input
GPIO13	GPU_VID5	GPU Core VDD VID5
GPIO14	HPD_AB	Hot Plug Detect for ITPAB
GPIO15	HPD_C	Hot Plug Detect for ITPC
GPIO16	HPD_D or MEM_VDD_CTL	Phase Sheddling or Memory VDD VID
GPIO17	HPD_D	Hot Plug Detect for ITPD
GPIO18	HPD_E	Hot Plug Detect for ITPE
GPIO19	HPD_F	Hot Plug Detect for ITPF
GPIO20	Reserved	
GPIO21	Reserved	

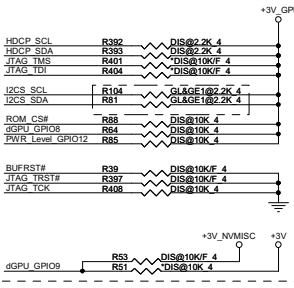
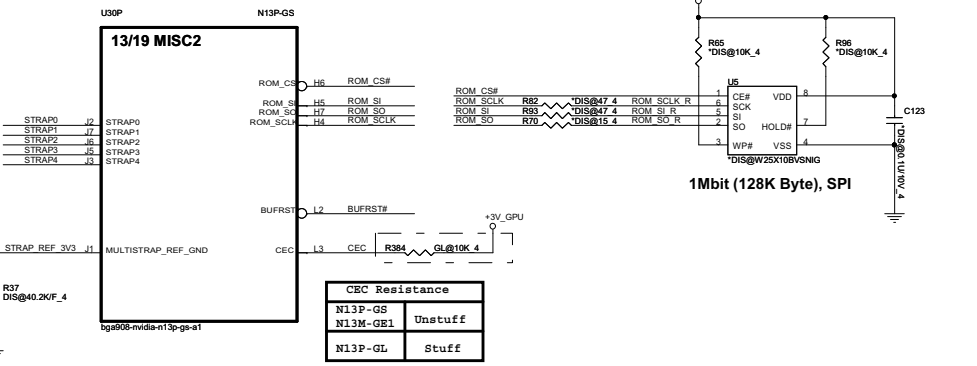


Table 2. GB4-128 Ballout Compatibility

L3	CEC	NC	NC	NC	NC
					Place a 10k pull-up to 3V3 on N13P-PE57-GL1-N61.

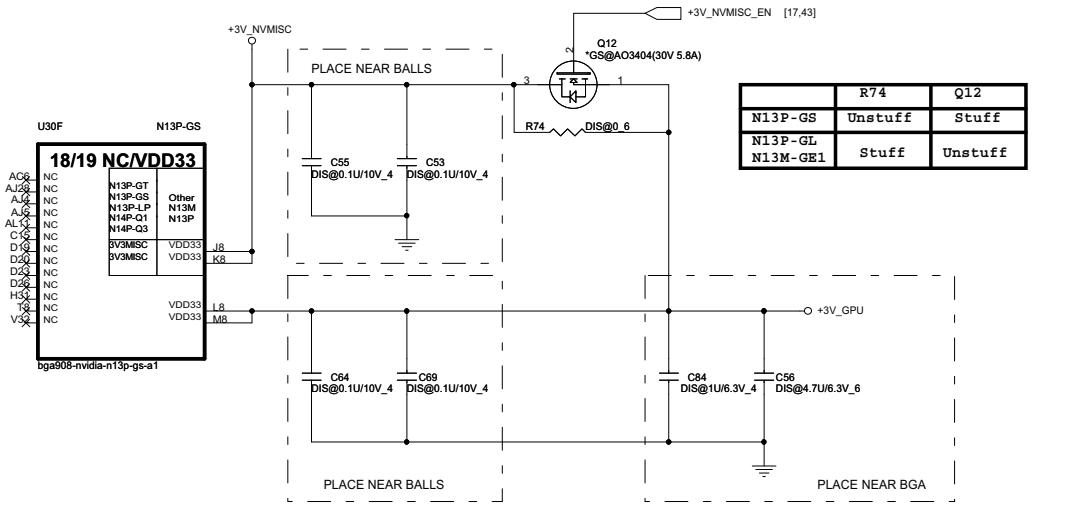
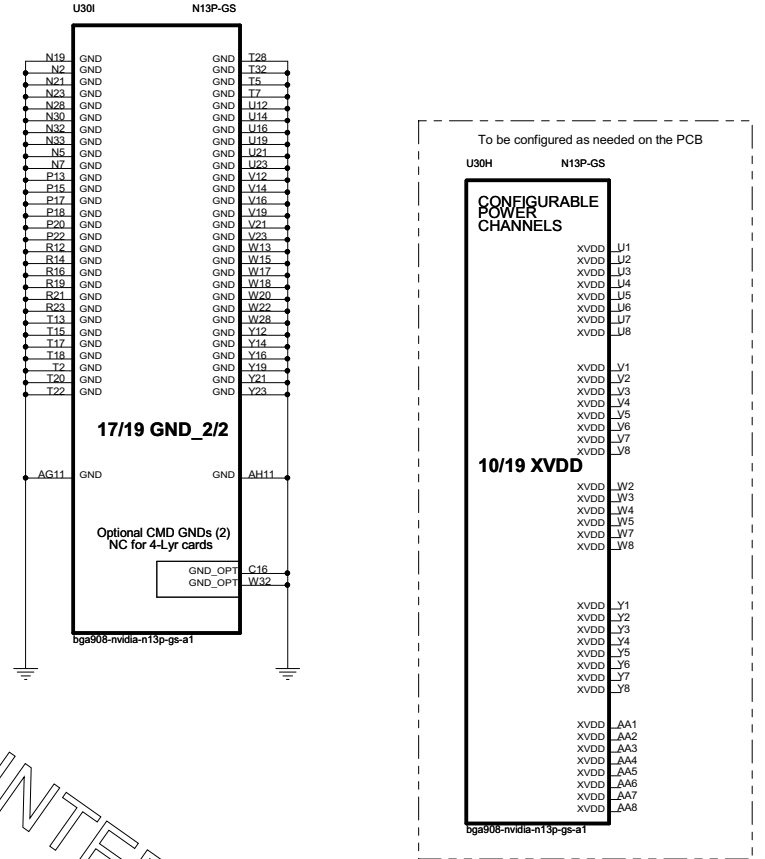
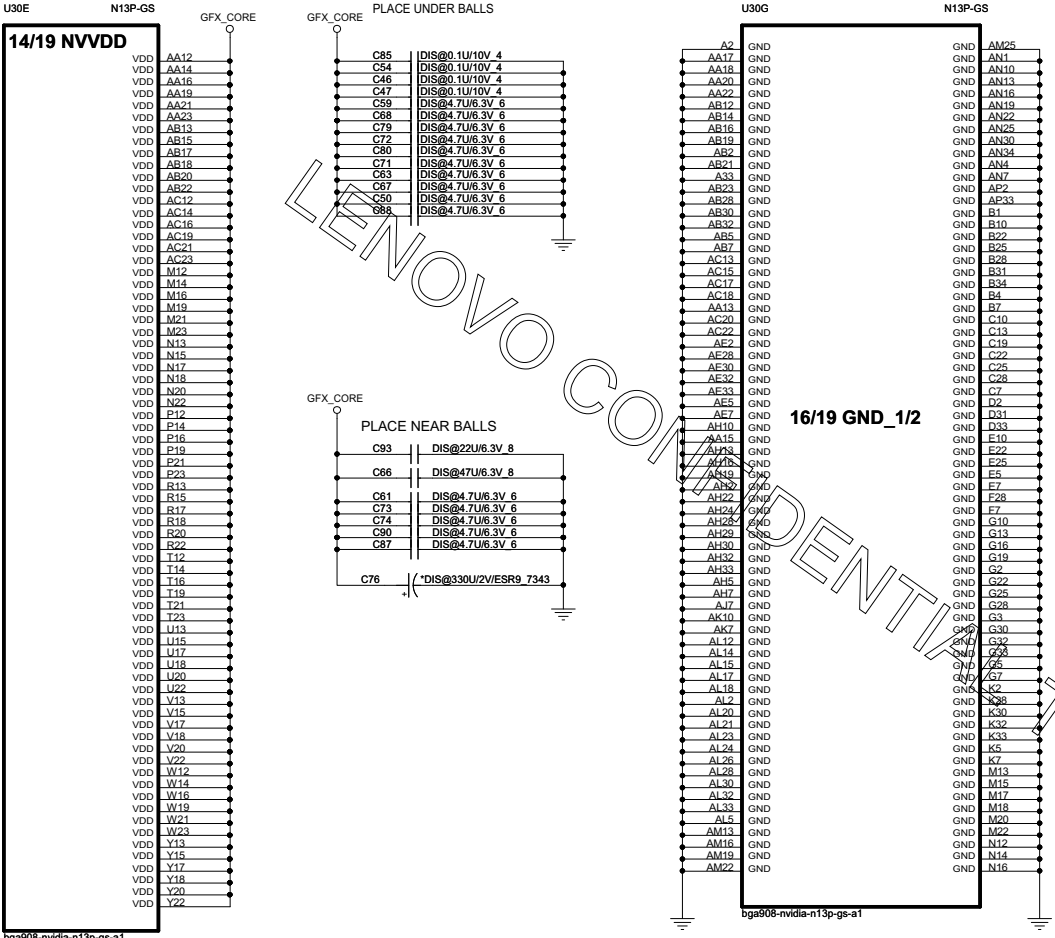


Table 5. Stuffing Options

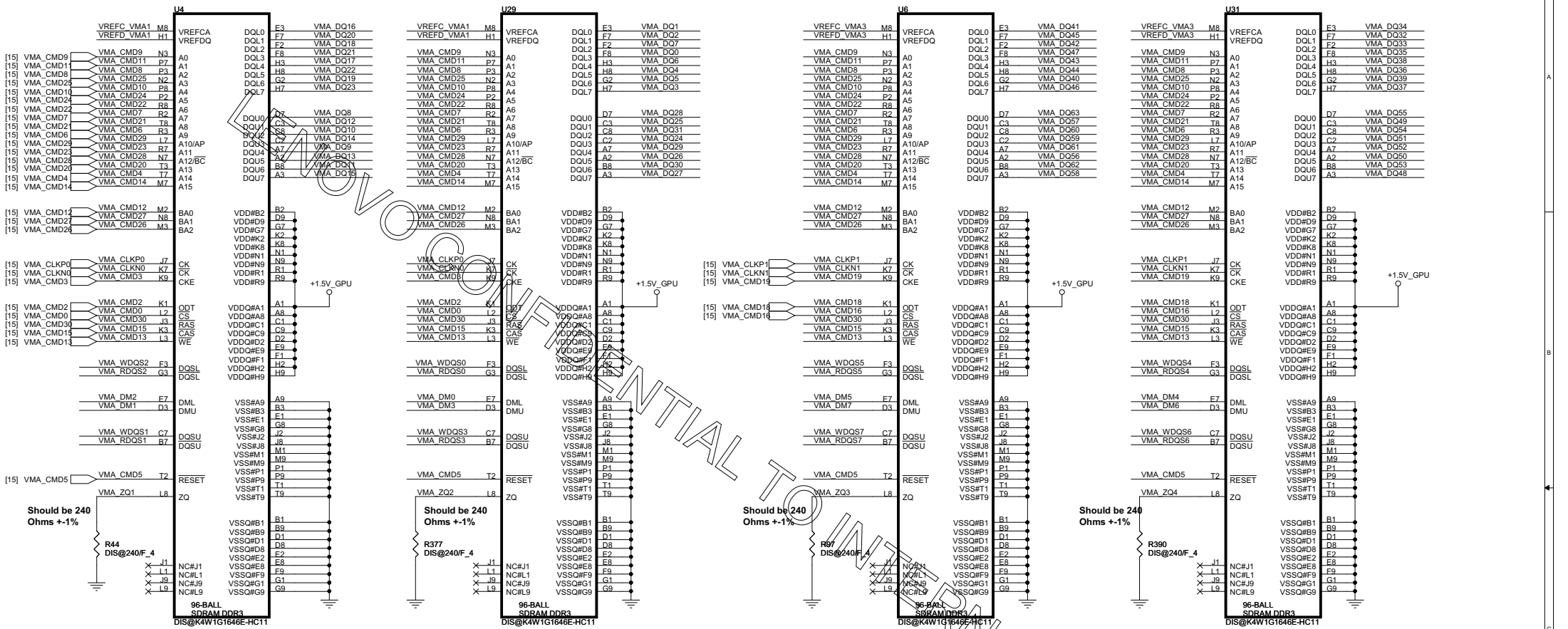
N13P-GT/-GS/-LP, N14P-Q1/-Q3	I2C and GPIO	
	3V3MISC	No stuff FET Stuff OQ bypass resistor
Other N13P and N13M	I2C and GPIO	Stuff FET No stuff OQ bypass resistor
	3V3MISC	No stuff FET Stuff OQ bypass resistor

	R74	Q12
N13P-GS	Unstuff	Stuff
N13P-GL N13M-GE1	Stuff	Unstuff

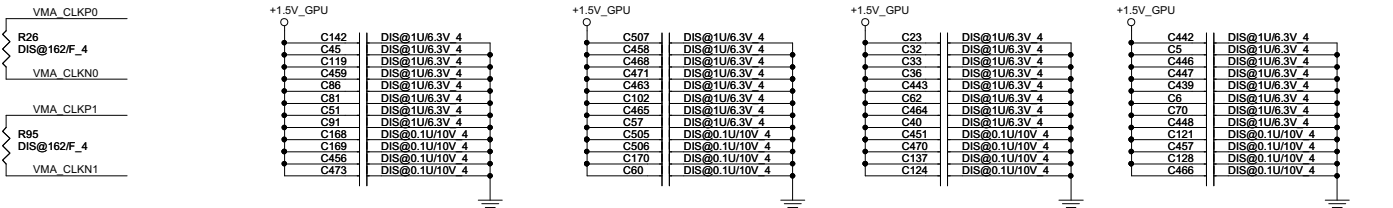
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3

[14,15,20,33,43] +1.5V_GPU



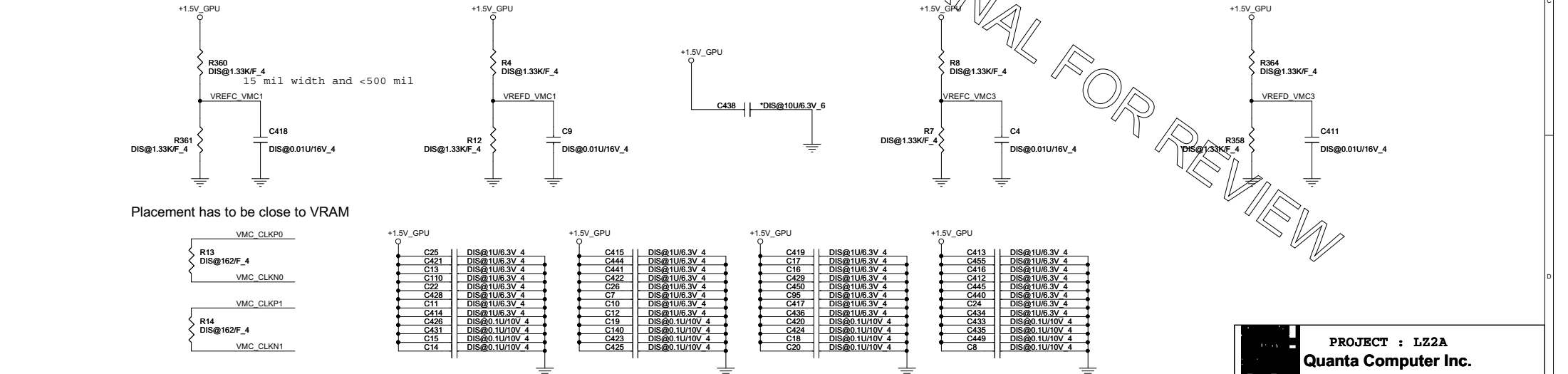
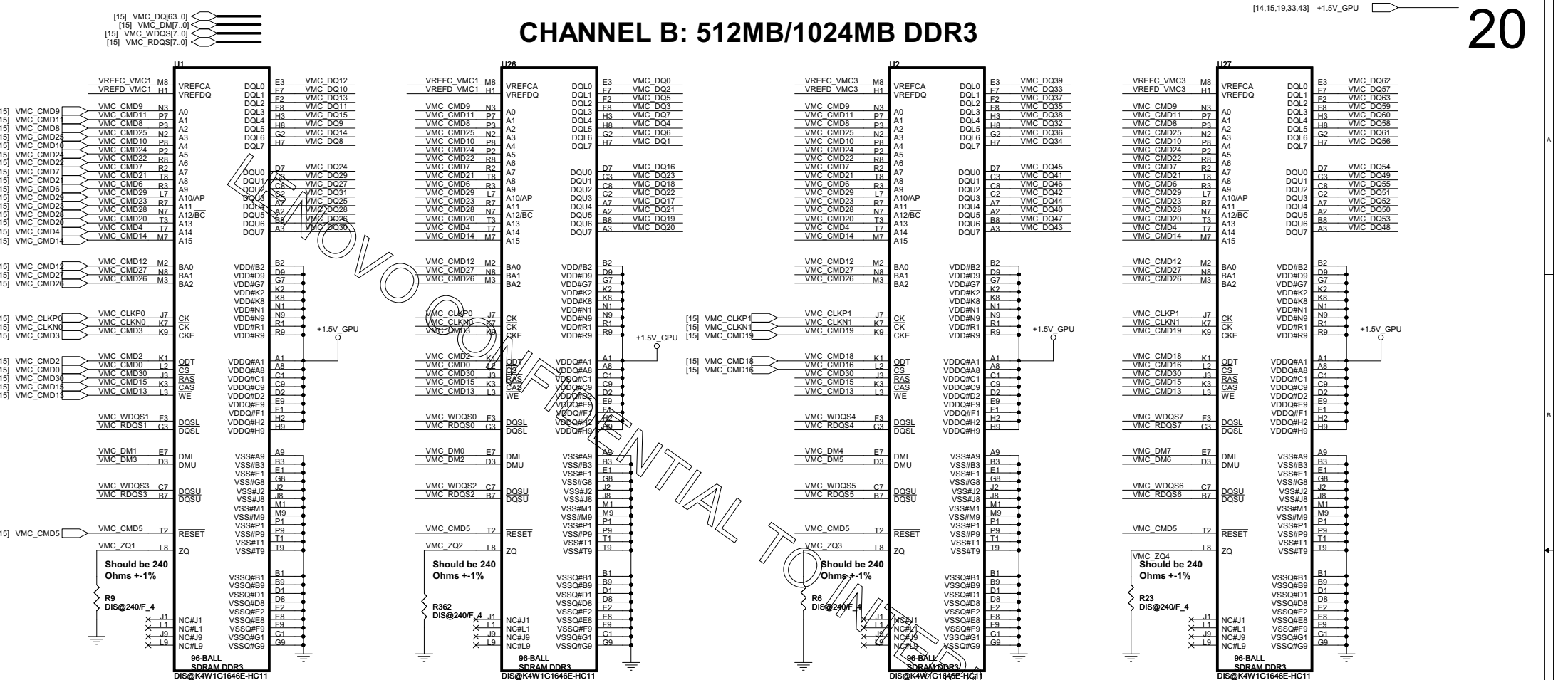
Placement has to be close to VRAM



PROJECT : L2Z2A
Quanta Computer Inc.

CHANNEL B: 512MB/1024MB DDR3

[14,15,19,33,43] +1.5V_GPU



PROJECT : LZ2A
Quanta Computer Inc.

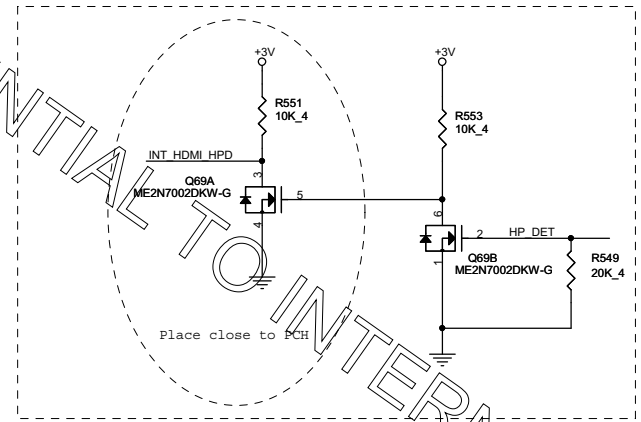
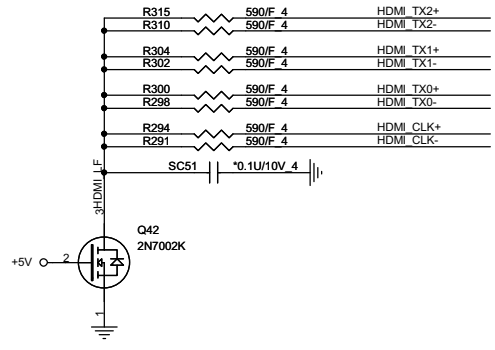
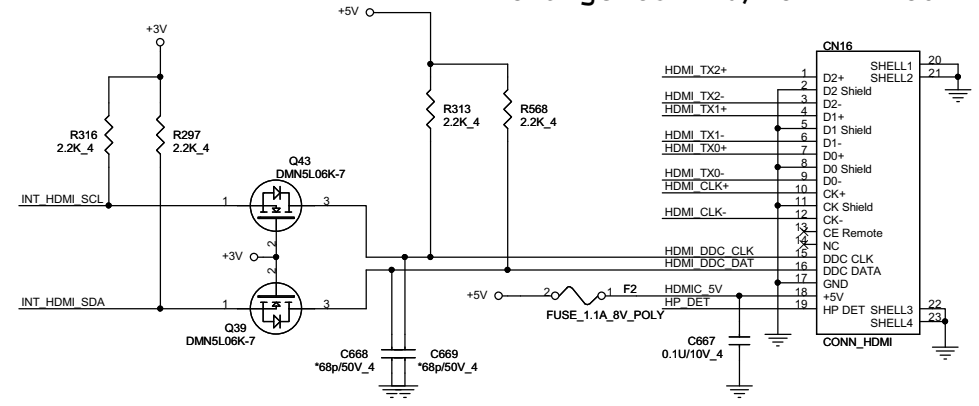
Size Document Number
Nvidia-N13P GB4-128(VRAM-2)

Date: Wednesday, November 30, 2011 Sheet 20 of 45

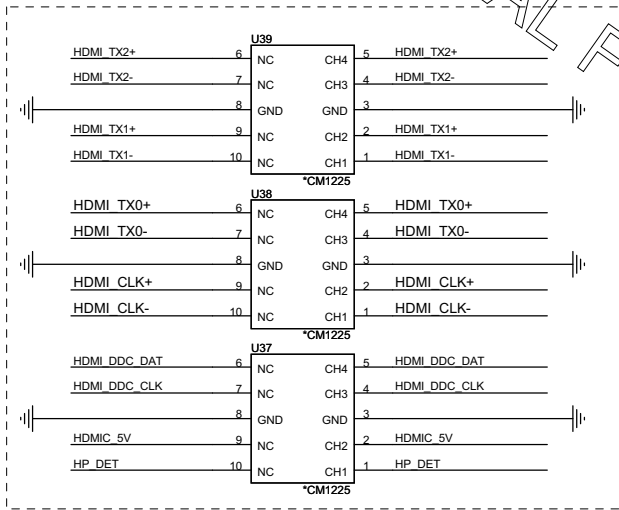
[6] INT_HDMI_TXDP2	C620	0.1U/10V_4	HDMI TX2+
[6] INT_HDMI_TXDN2	C619	0.1U/10V_4	HDMI TX2-
[6] INT_HDMI_TXDP1	C818	0.1U/10V_4	HDMI TX1+
[6] INT_HDMI_TXDN1	C817	0.1U/10V_4	HDMI TX1-
[6] INT_HDMI_TXDP0	C816	0.1U/10V_4	HDMI TX0+
[6] INT_HDMI_TXDN0	C815	0.1U/10V_4	HDMI TX0-
[6] INT_HDMI_TXCP	C813	0.1U/10V_4	HDMI CLK+
[6] INT_HDMI_TXCN	C811	0.1U/10V_4	HDMI CLK-

[6] INT_HDMI_SCL	INT_HDMI_SCL
[6] INT_HDMI_SDA	INT_HDMI_SDA
[6] INT_HDMI_HPD	INT_HDMI_HPD

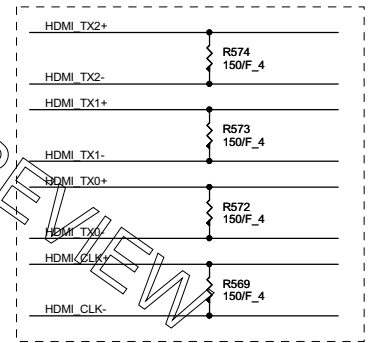
Change to KL6/BC HDMI CONN



For ESD



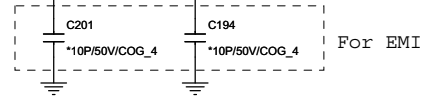
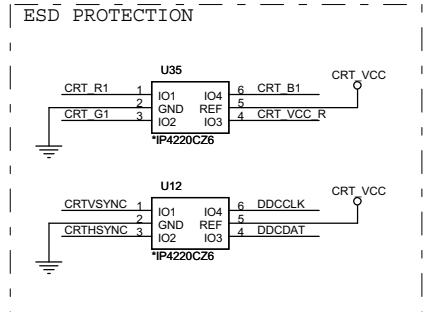
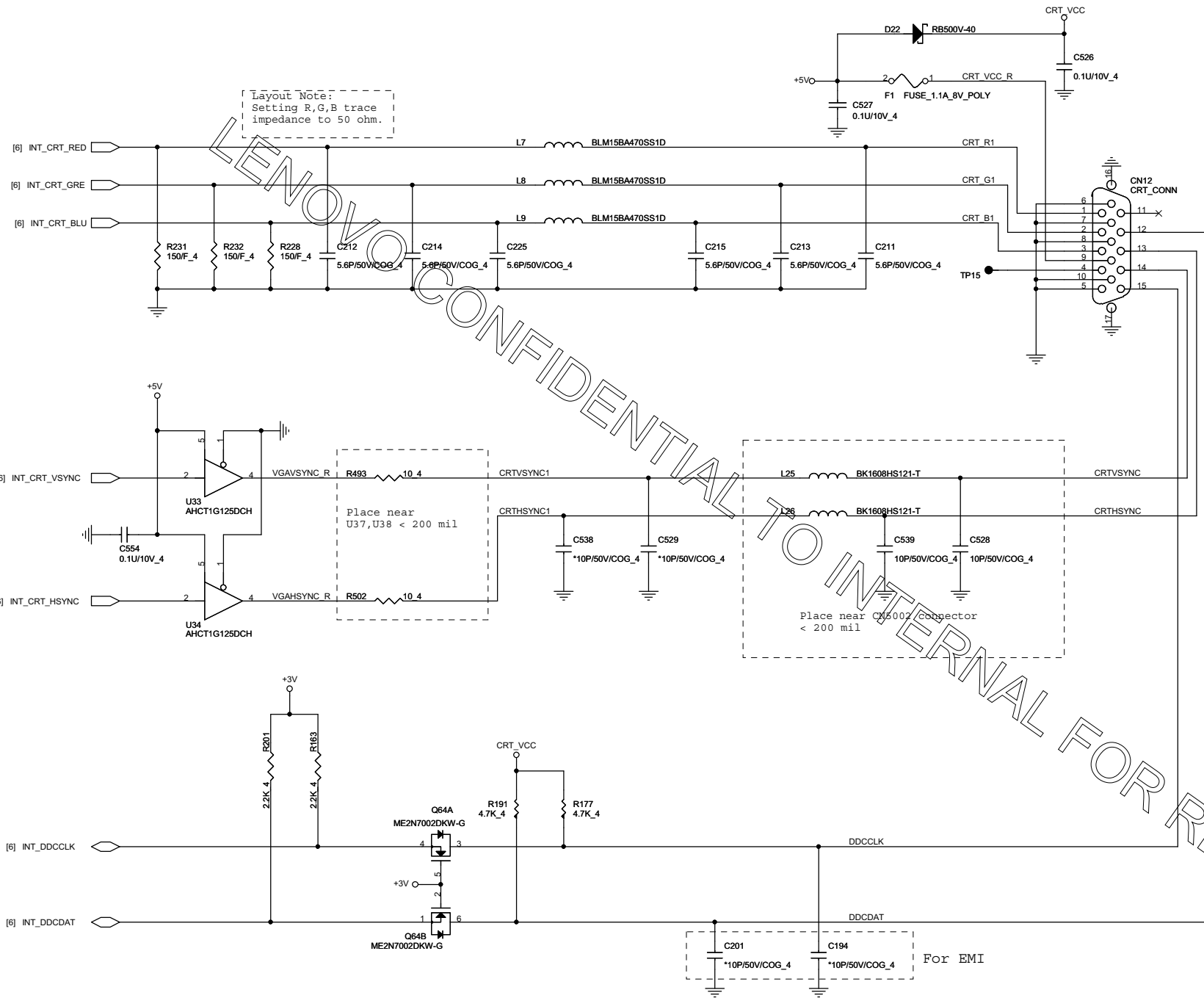
For EMI



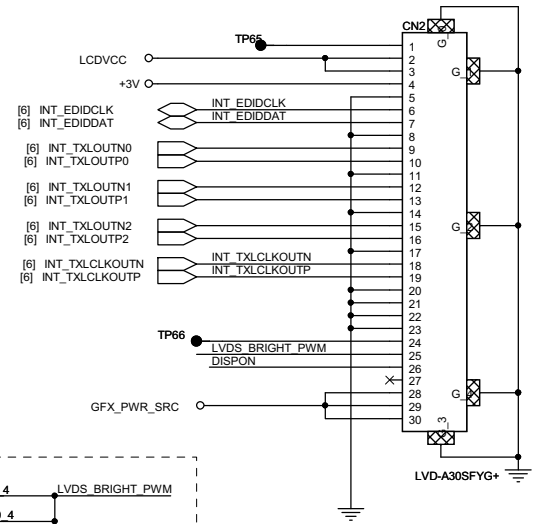
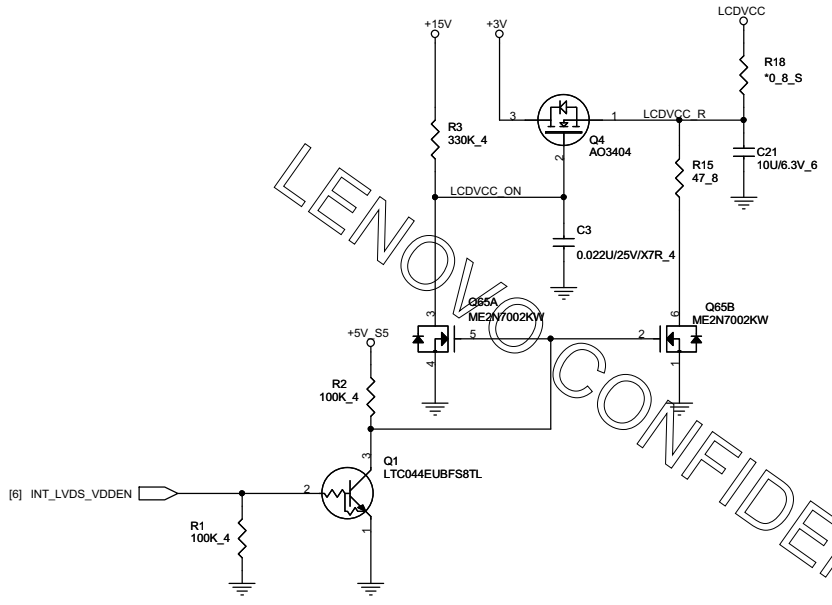
PROJECT : LZ2A
Quanta Computer Inc.

Size Custom Document Number Madison_LVDS/HDMI/CRT switchable Rev 1A
 Date: Wednesday, November 30, 2011 Sheet 21 of 45

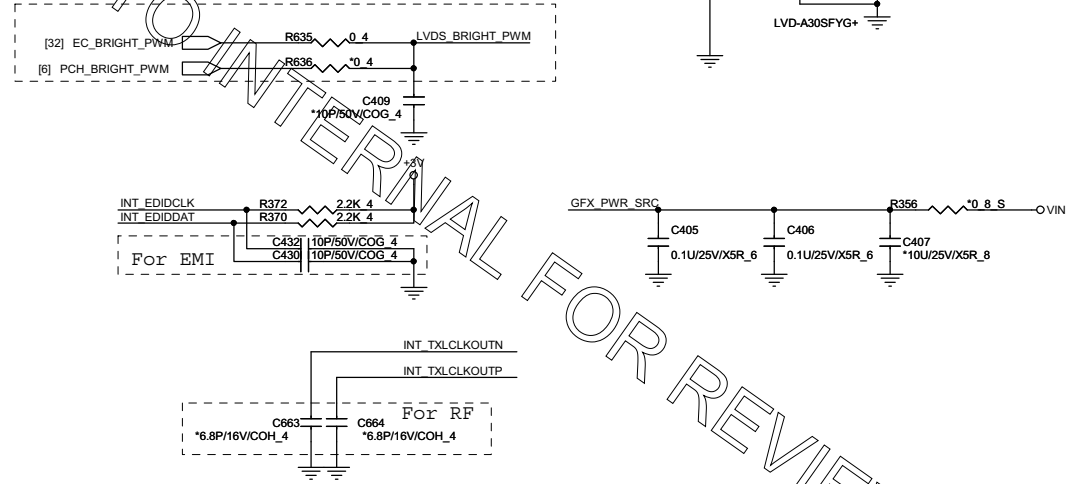
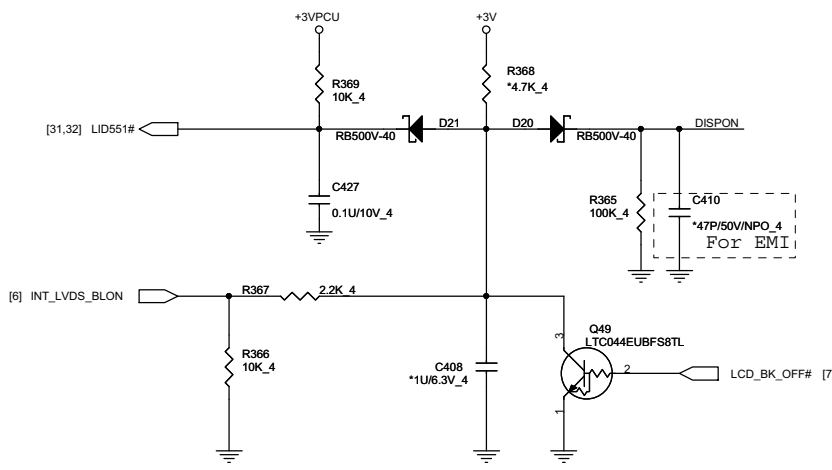
Layout Note:
Setting R,G,B trace
impedance to 50 ohm.

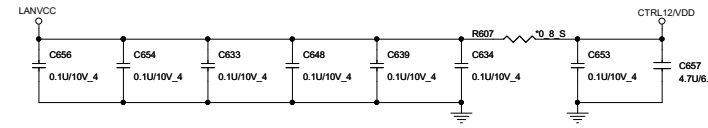
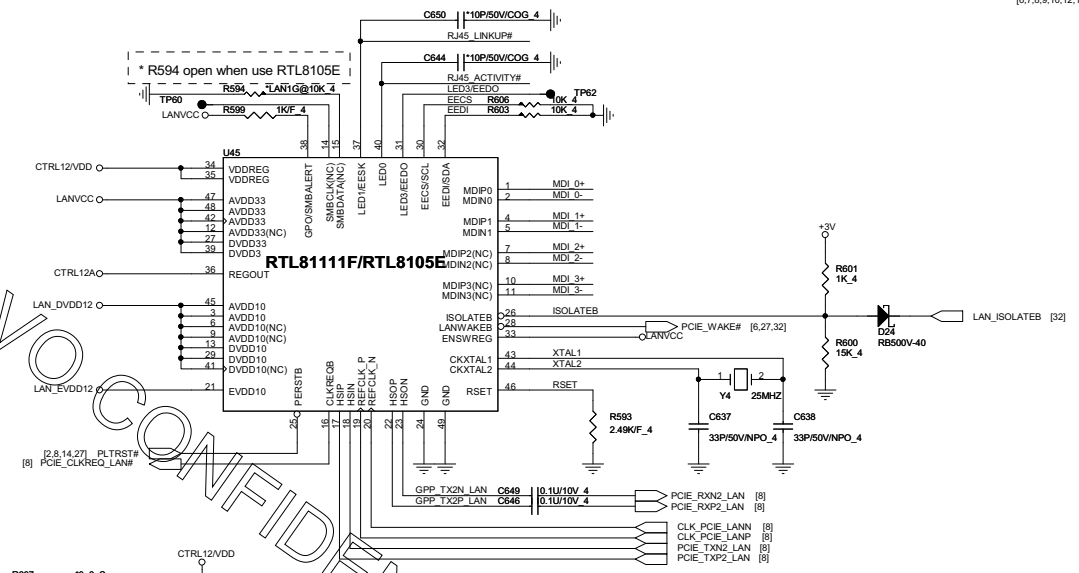
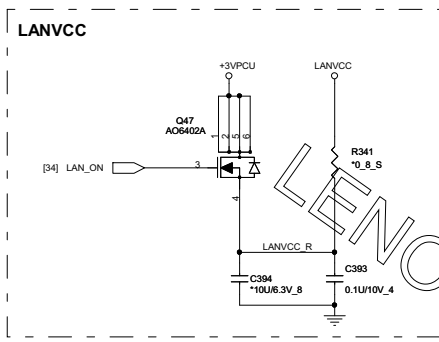
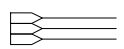


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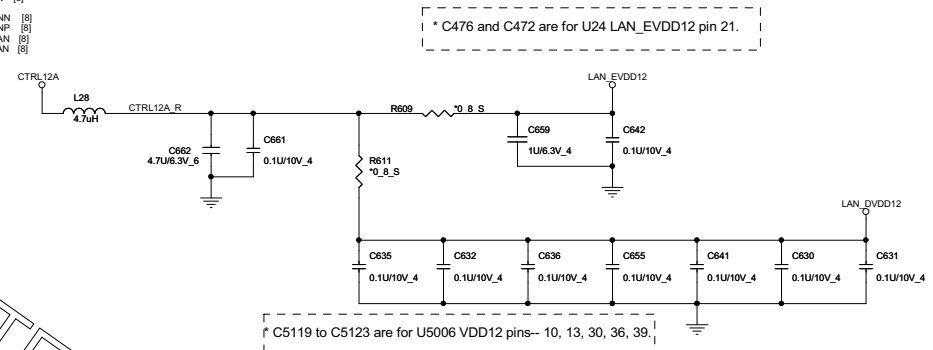


Back Light



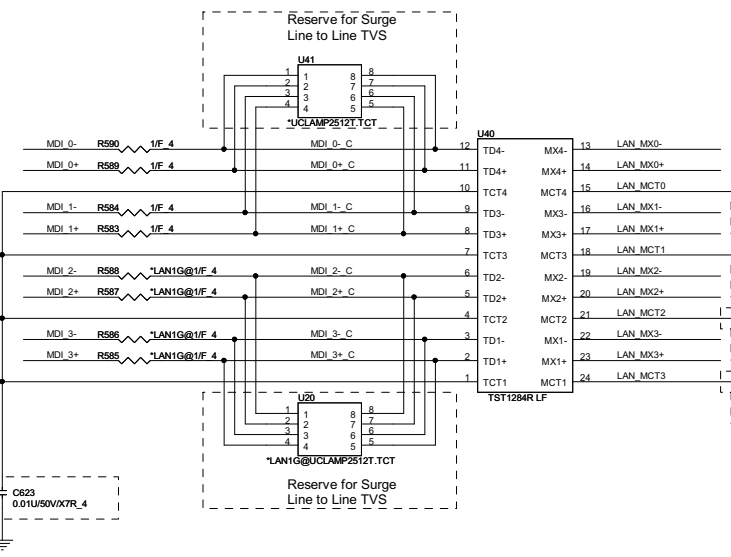
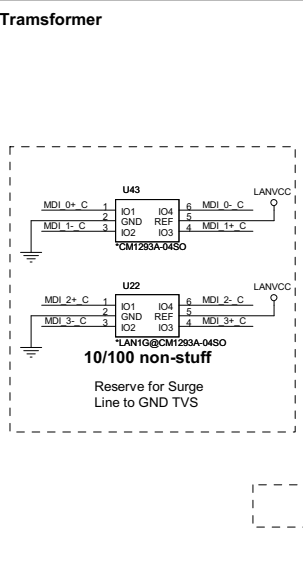


* C5110 to C5113 are for U5006 VDD33 pins-- 1, 29, 37 and 40. Place C5113, C5094 closed to U5006 pins44,45, and 40.

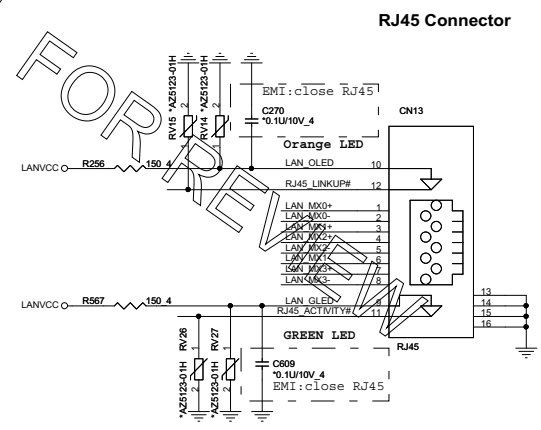


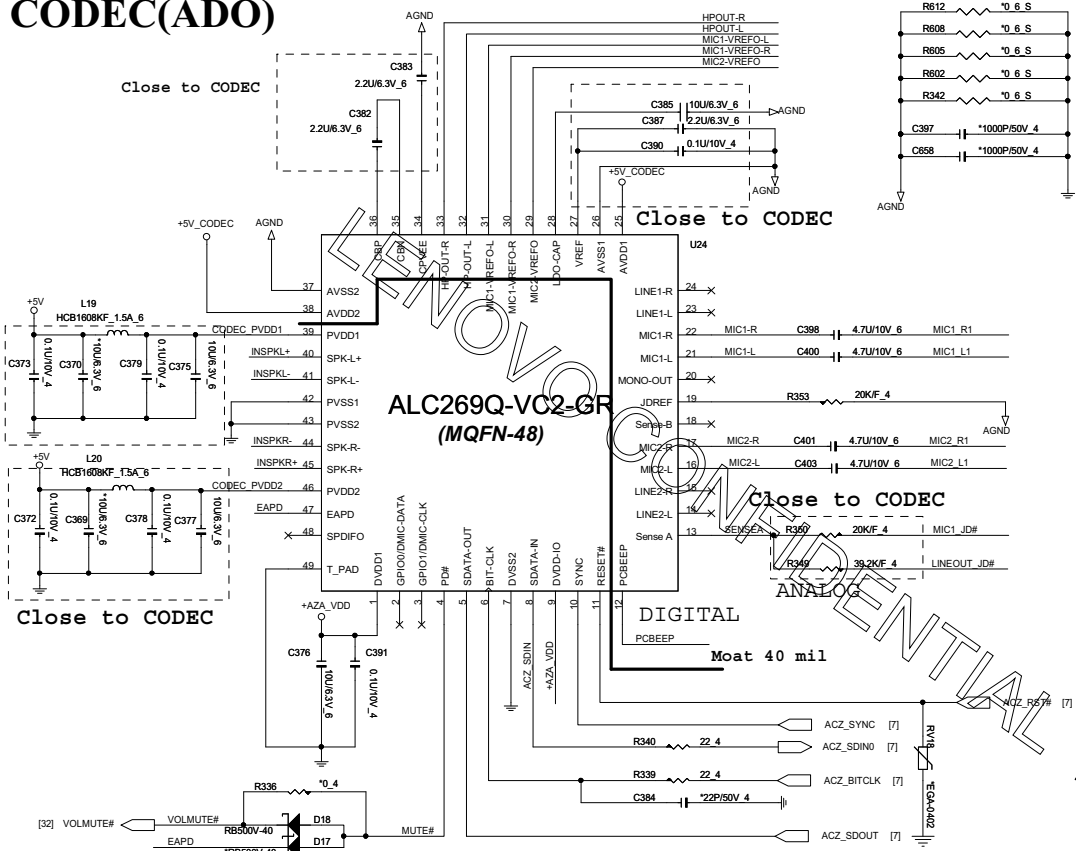
* C5119 to C5123 are for U5006 VDD12 pins-- 10, 13, 30, 36, 39.

* C476 and C472 are for U24 LAN_EVDD12 pin 21.

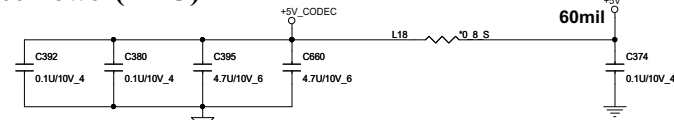


Layout: All termination signal should have 30 mil trace

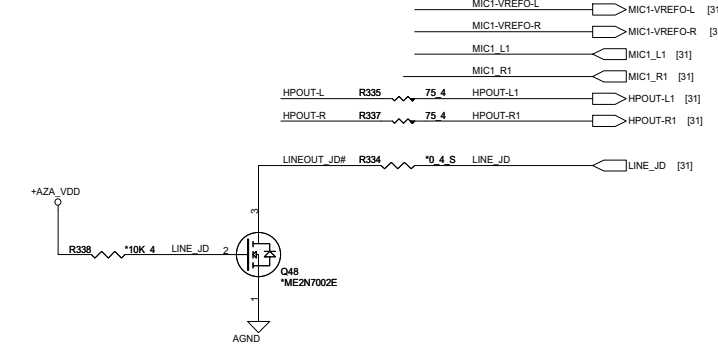




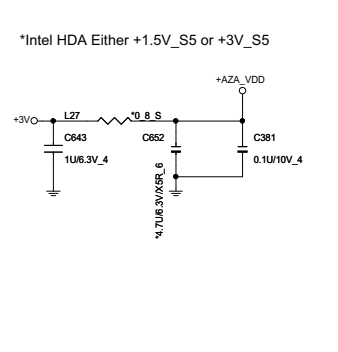
Codec Power(ADO)



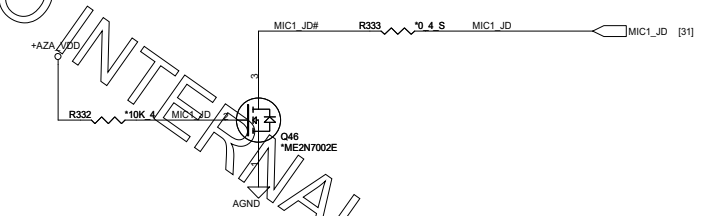
Earphone(AMP)



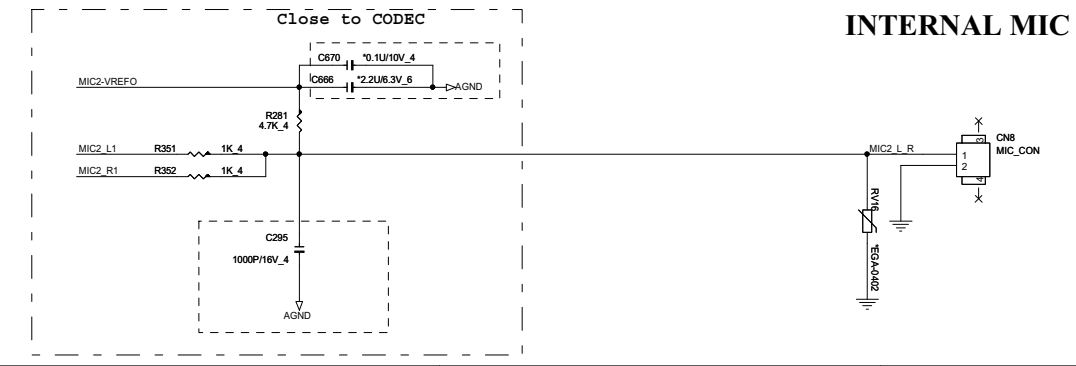
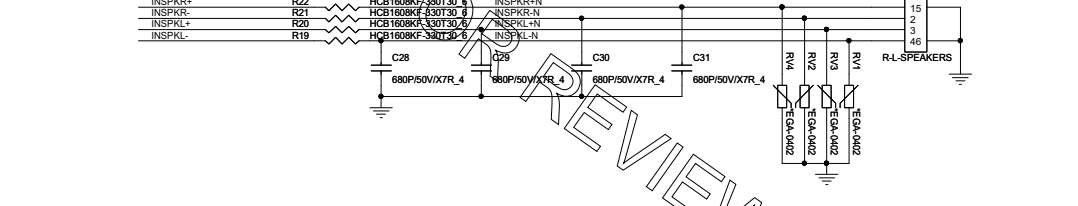
HDA Power(ADO)



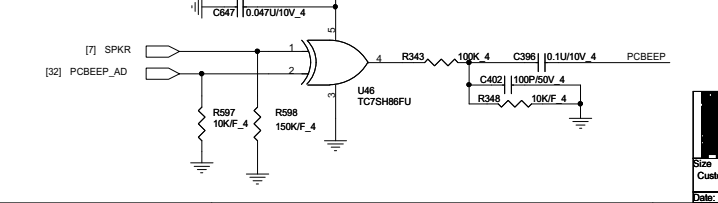
System MIC(AMP)



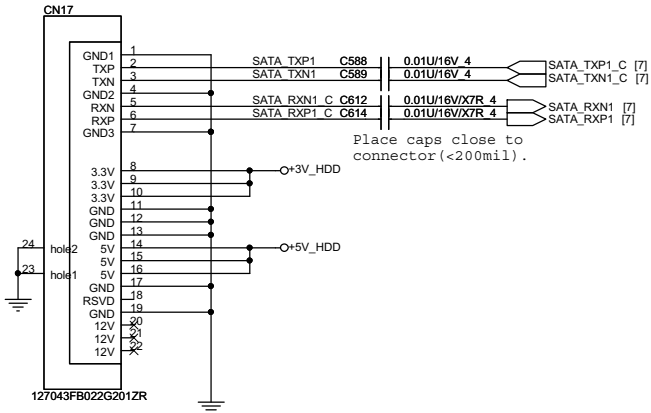
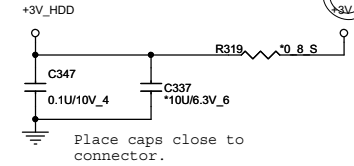
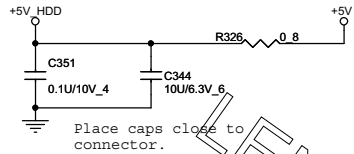
Speaker(AMP)



PC BEEP

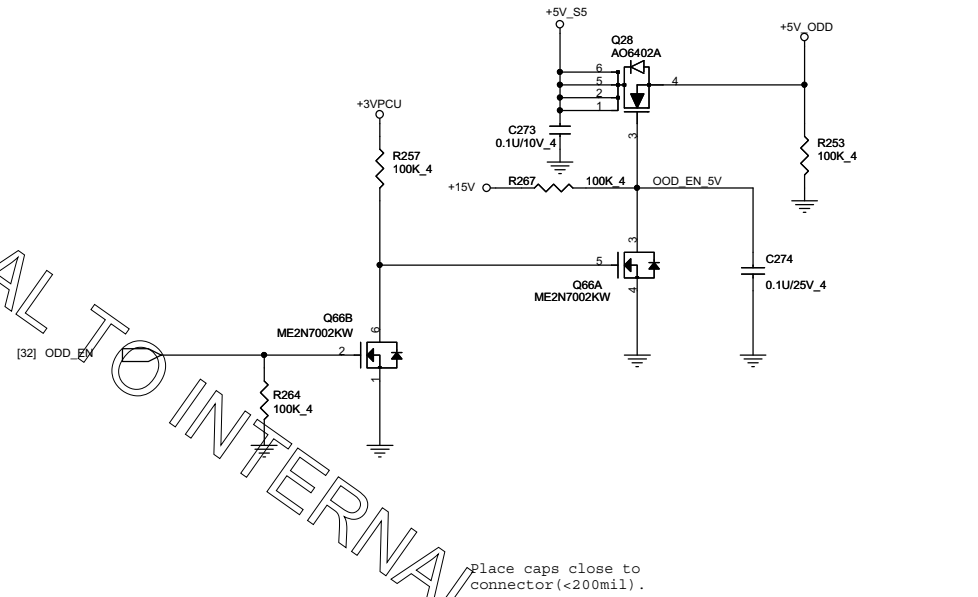
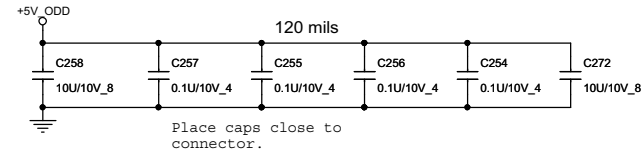


SATA HDD Connector.

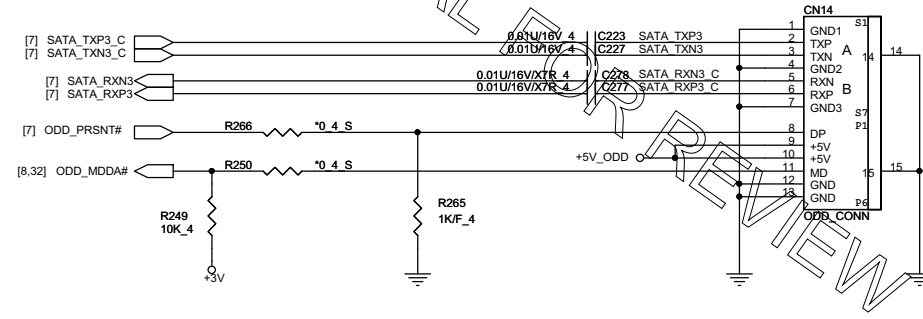


Place caps close to connector (<200mil).

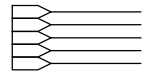
SATA ODD Connector.

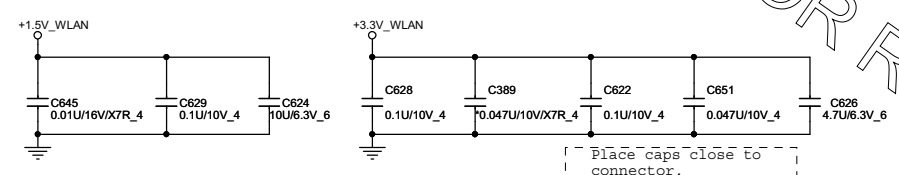
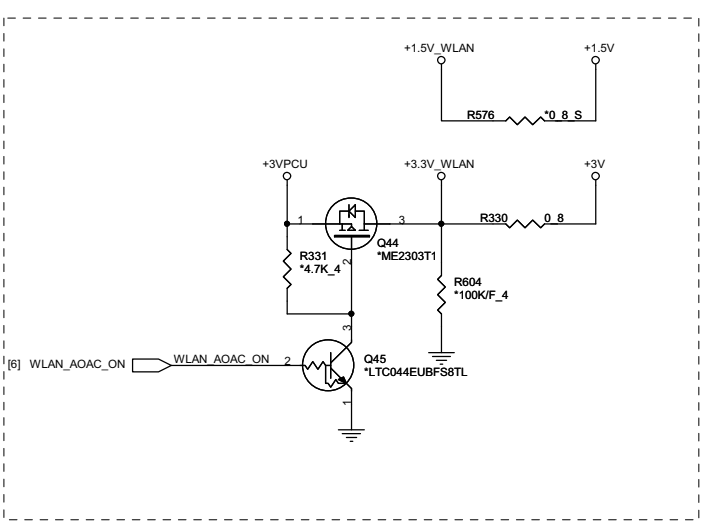
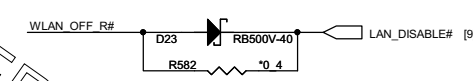
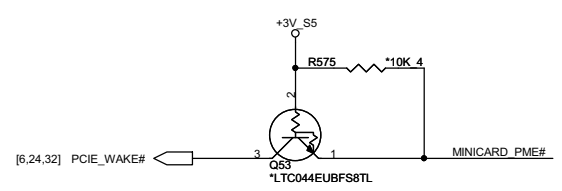
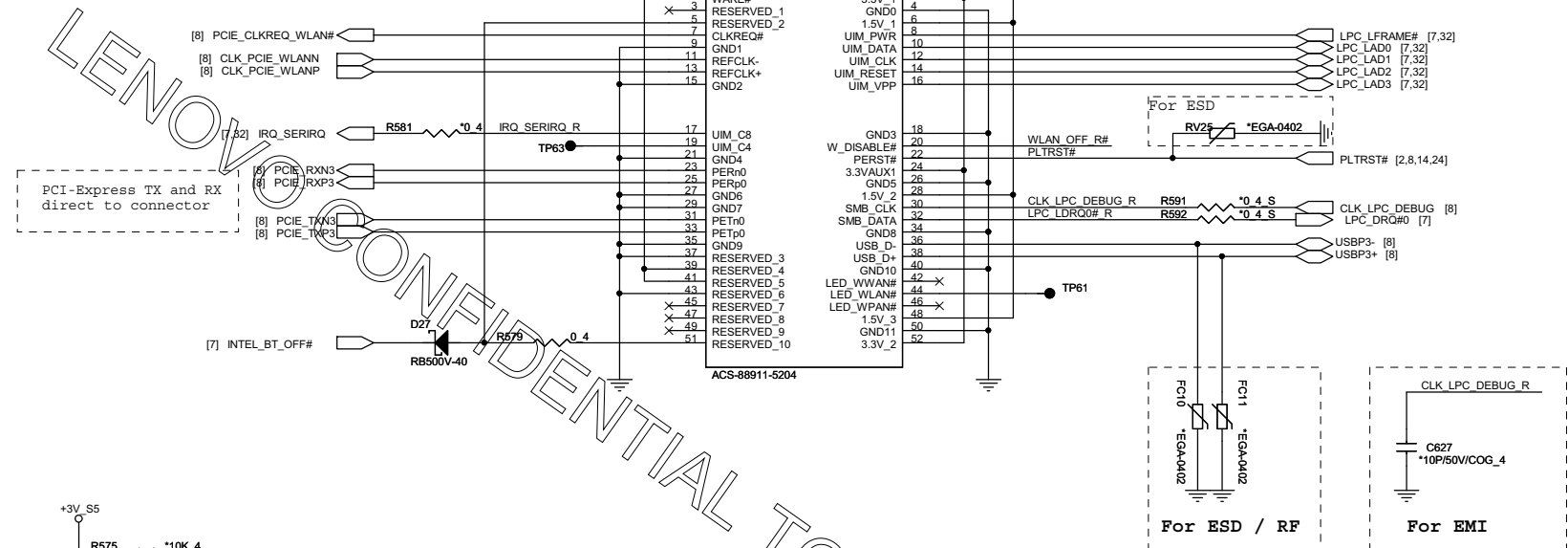


Place caps close to connector (<200mil).

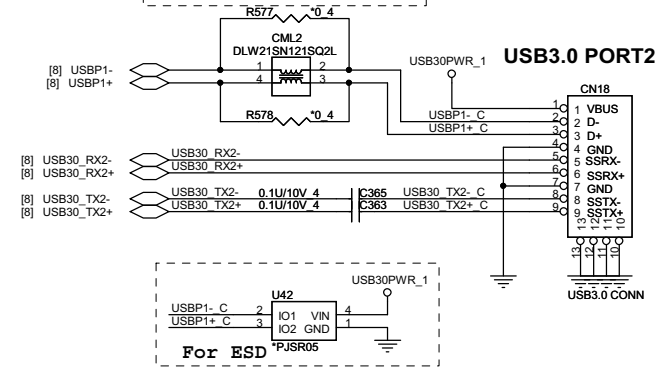
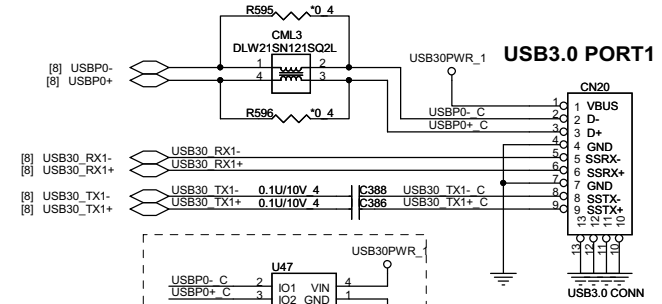
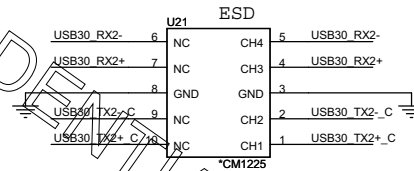
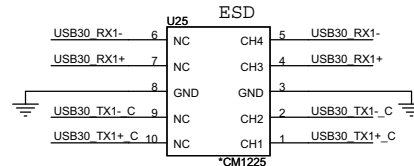
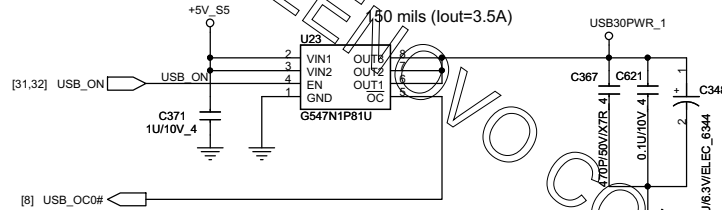


[7,10,21,22,25,29,30,33,34] +5V
 [6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,27,29,30,31,32,33,34,37,38,41,42,43] +3V
 [10,34,35,36,37,38,39,40,41,42,43] +5VPCU
 [6,7,23,24,27,31,32,34,35,36,40] +3VPCU
 [23,30,34,36,43] +15V

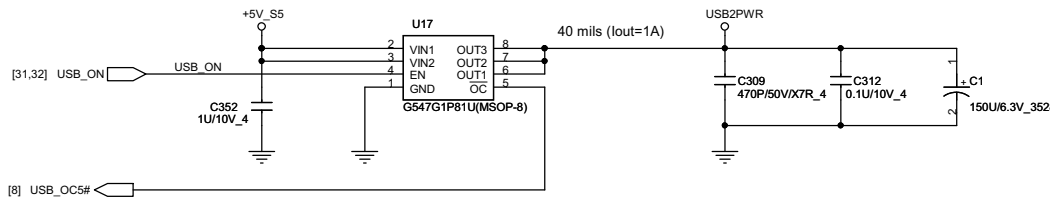




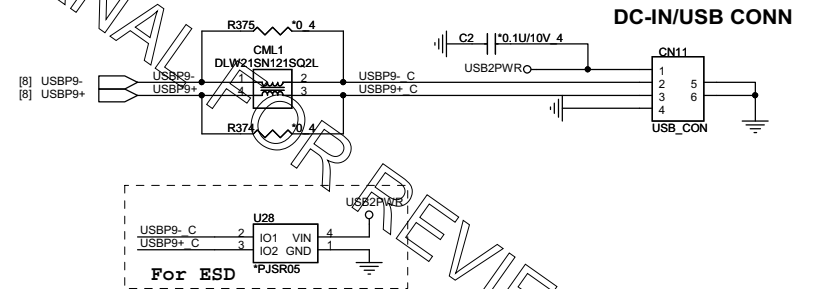
LENOVO CONFIDENTIAL TO INTERNAL FOR REVIEW



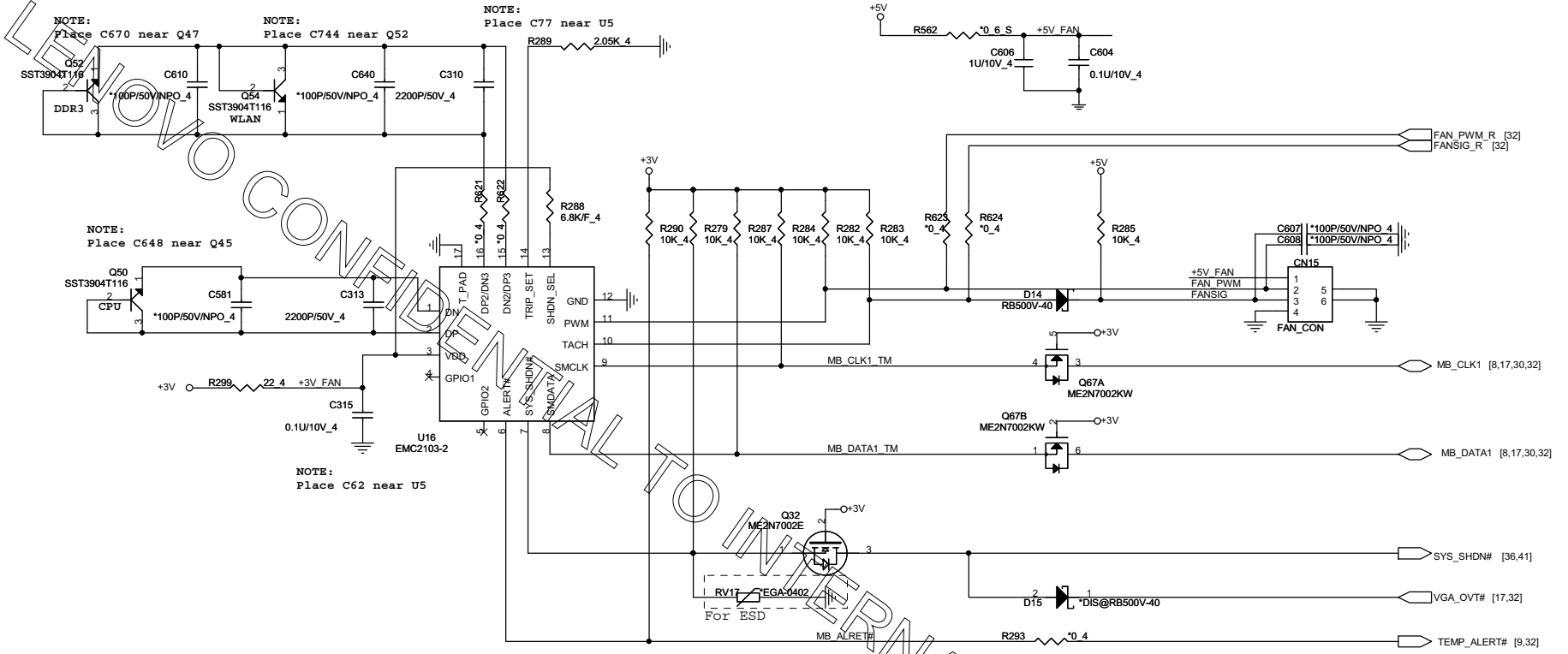
USB2.0*1



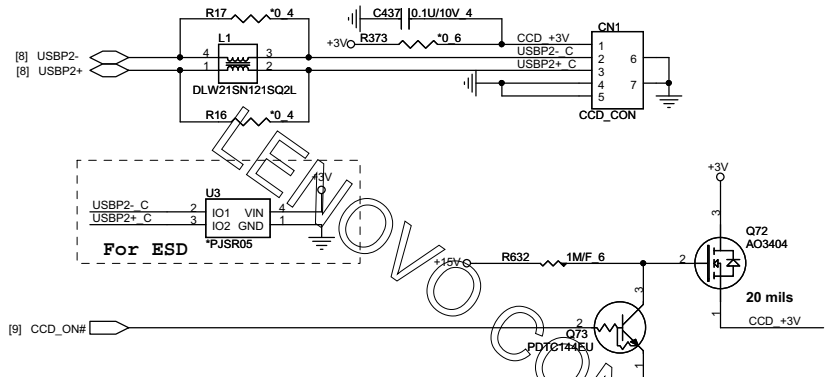
DC-IN Board



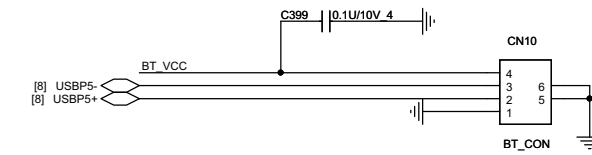
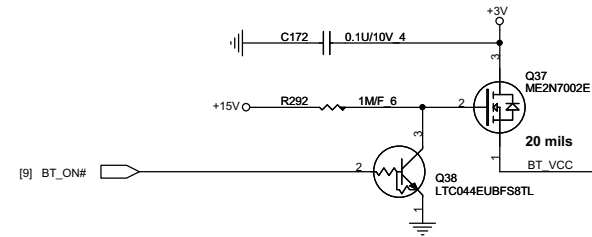
FAN CONTROL



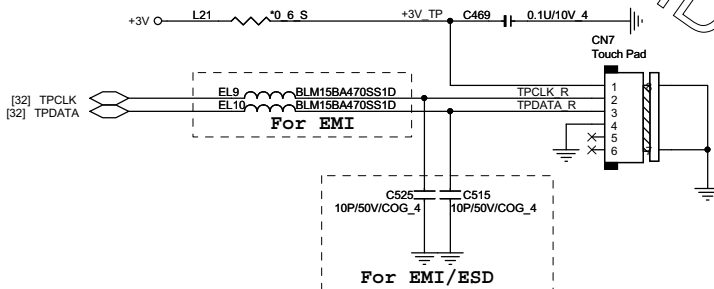
INTERNAL FOR REVIEW



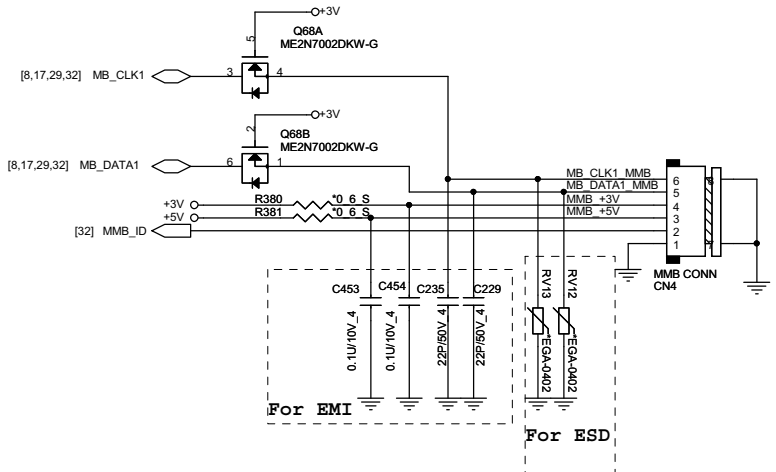
BLUETOOTH



Touch pad



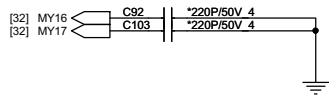
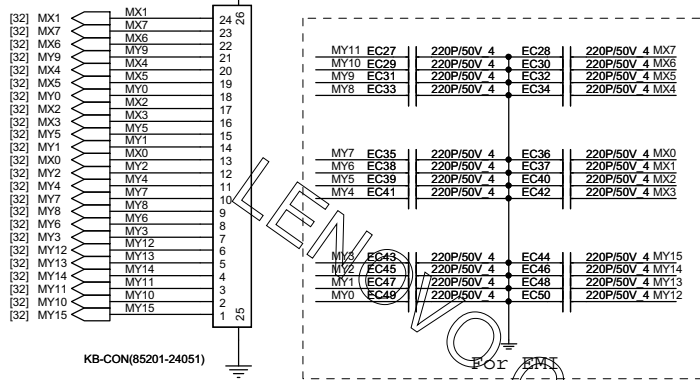
MMB



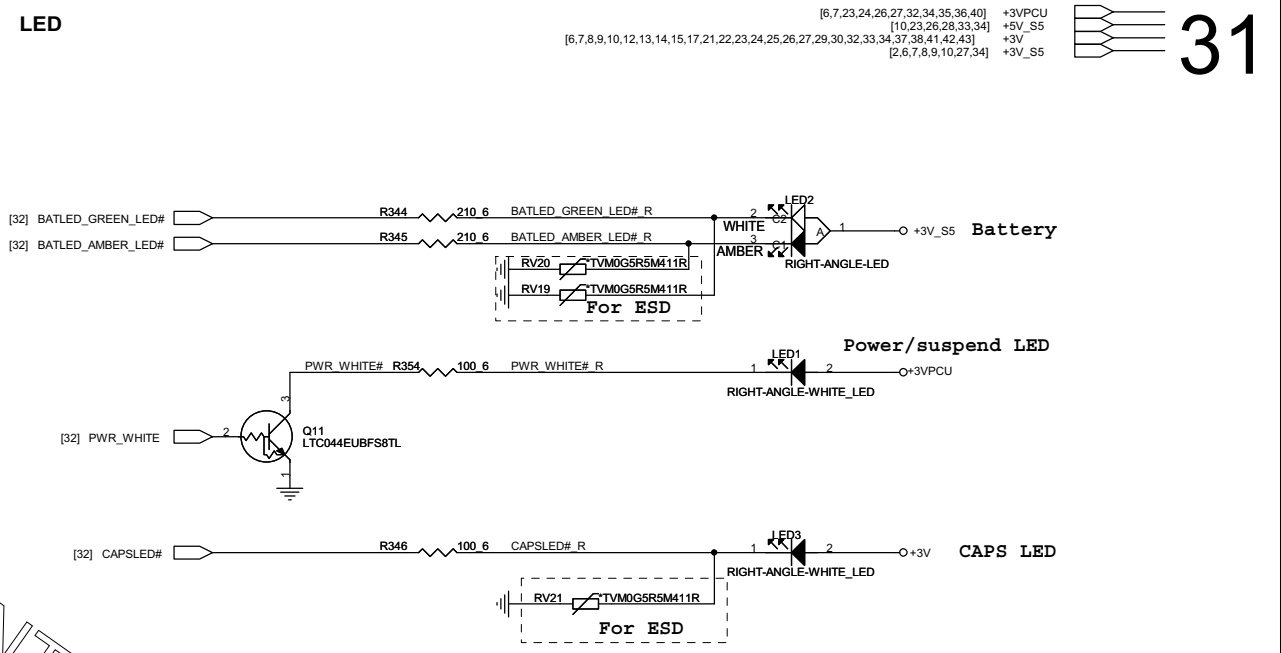
PROJECT : LZ2A
Quanta Computer Inc.

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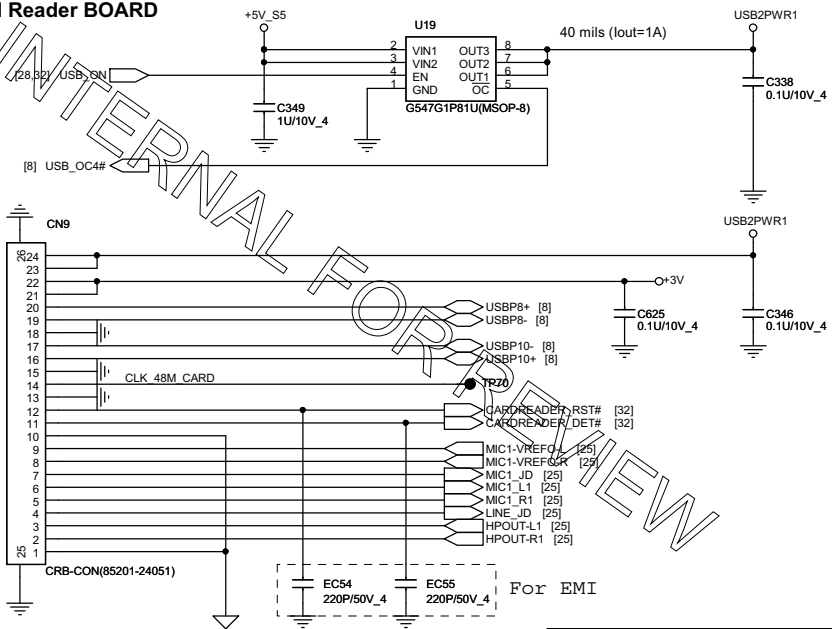
KEYBOARD



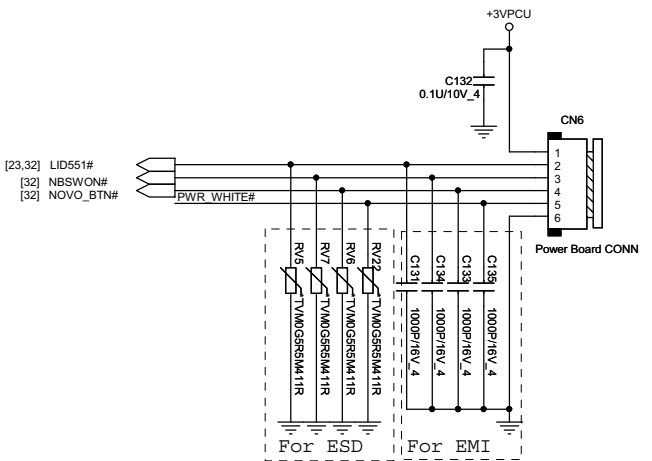
LED

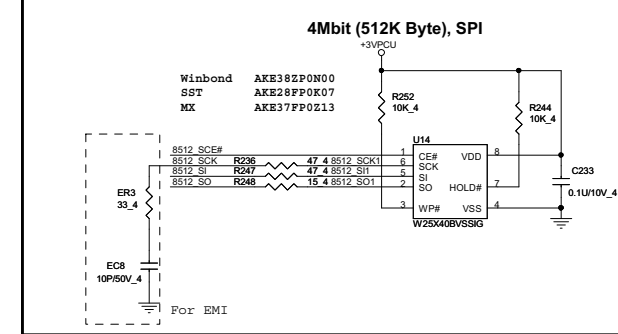
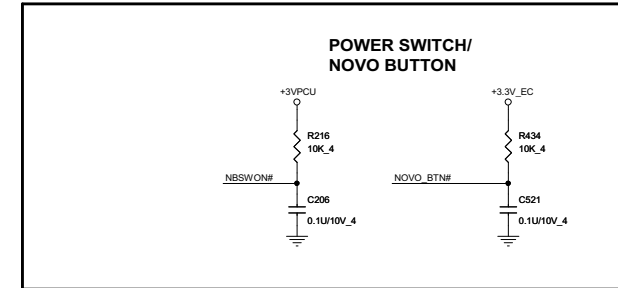
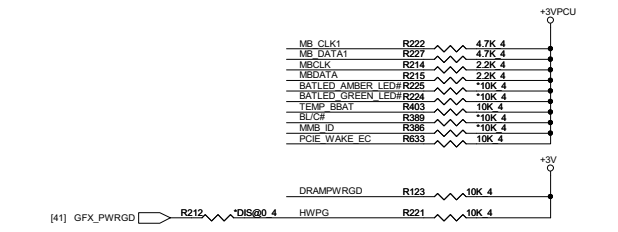
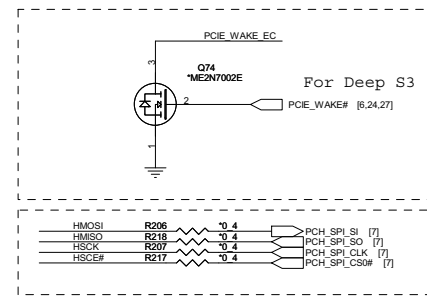
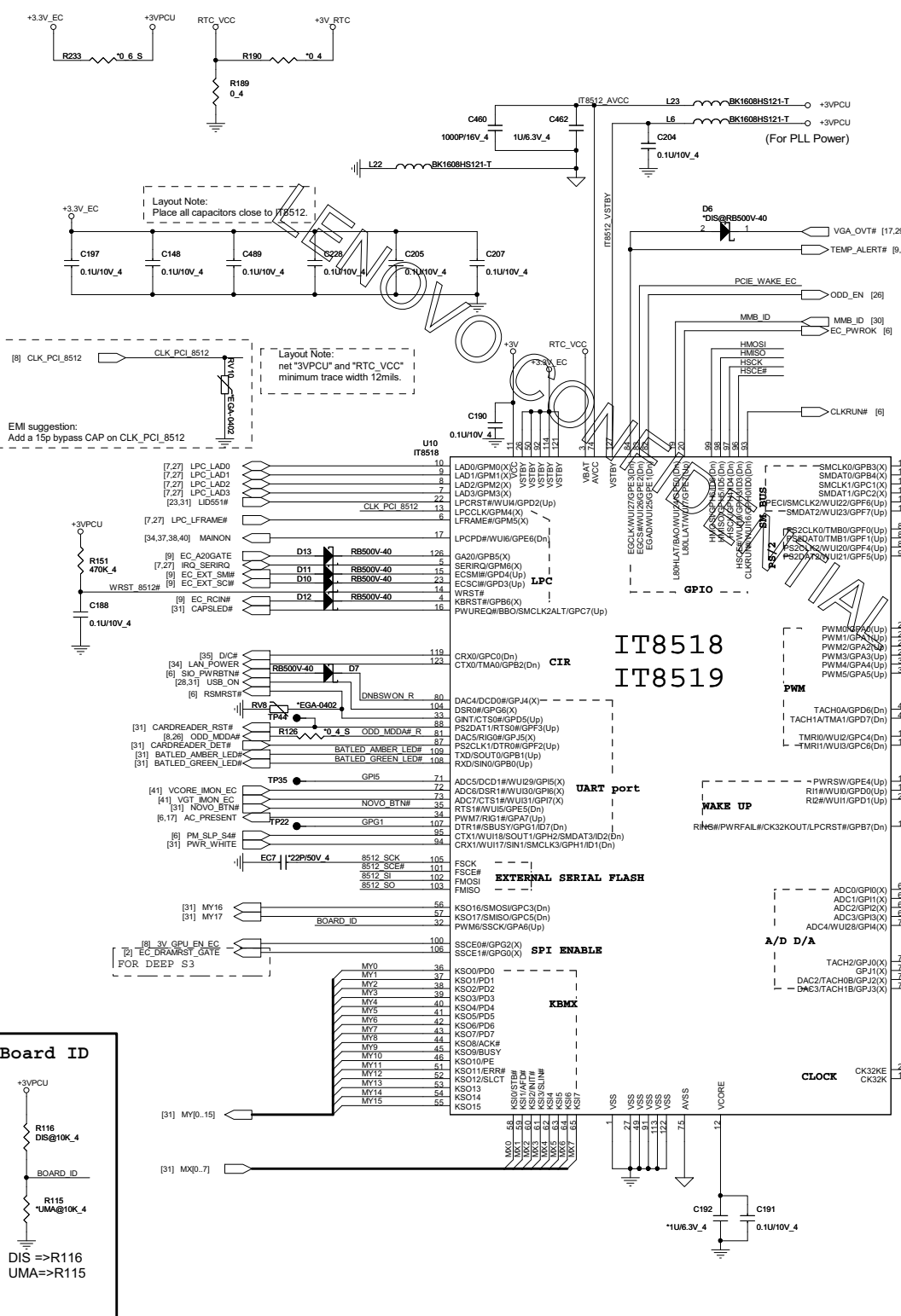


Card Reader BOARD

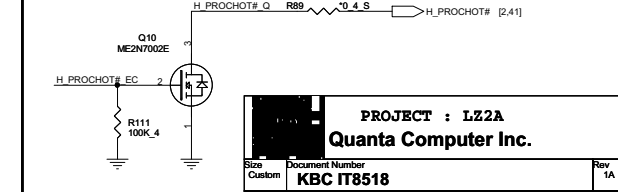


POWER BOARD

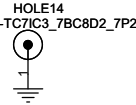
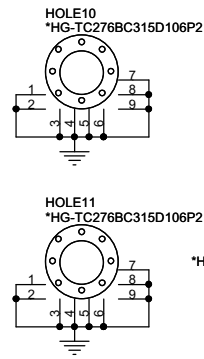
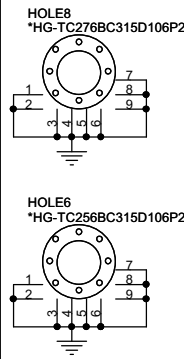
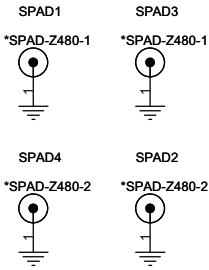
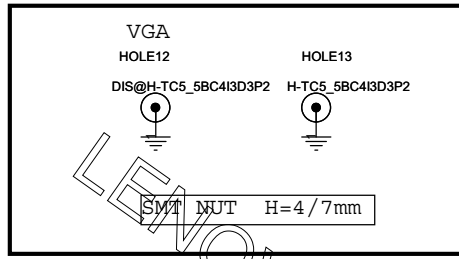




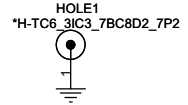
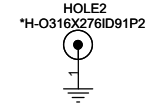
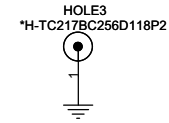
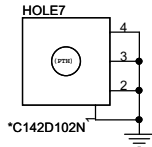
Project	PU/PD
Z380 (LZ1) - INTEL	PU
Z480 (LZ2) - INTEL	PU
Z485 (LZ2) - AMD	PU
Z580 (LZ3) - INTEL	PD
Z585 (LZ3) - AMD	PD



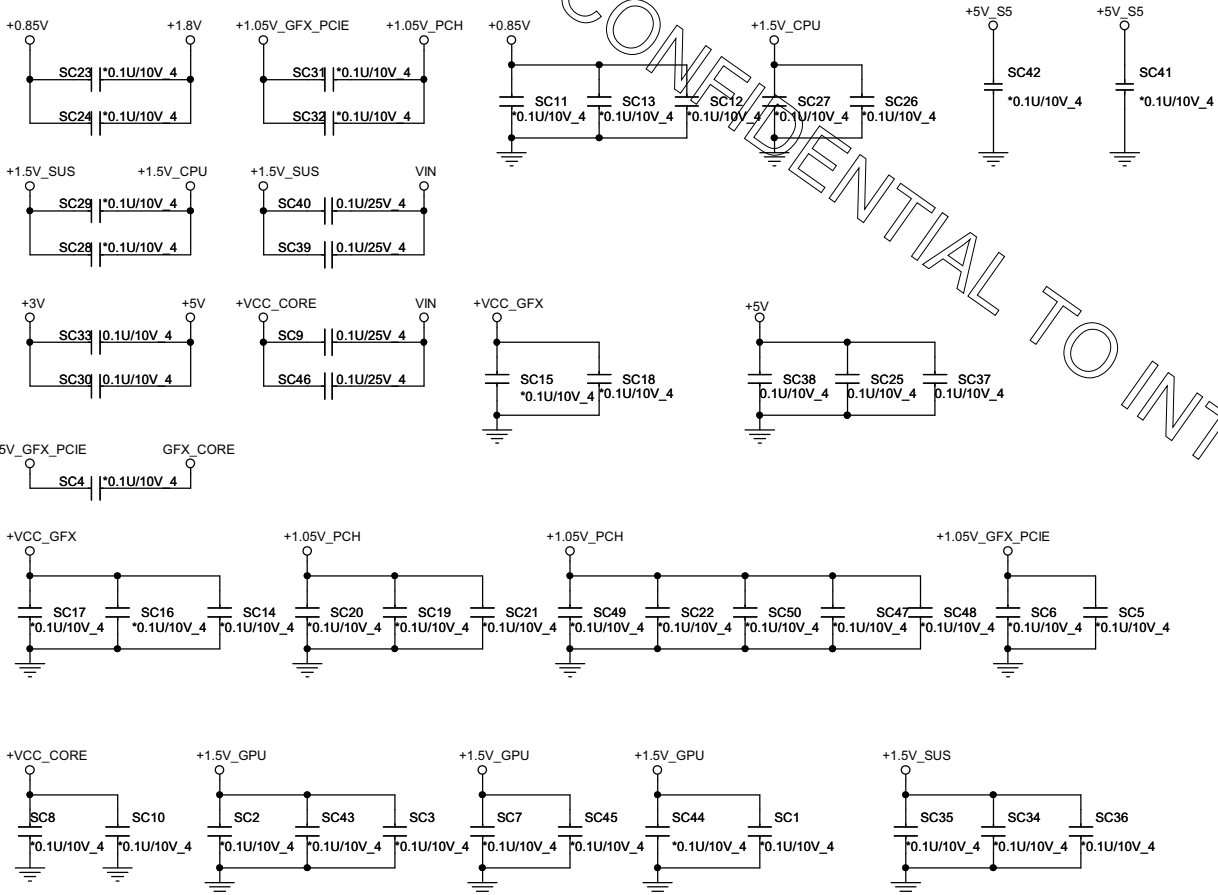
Screw for ME



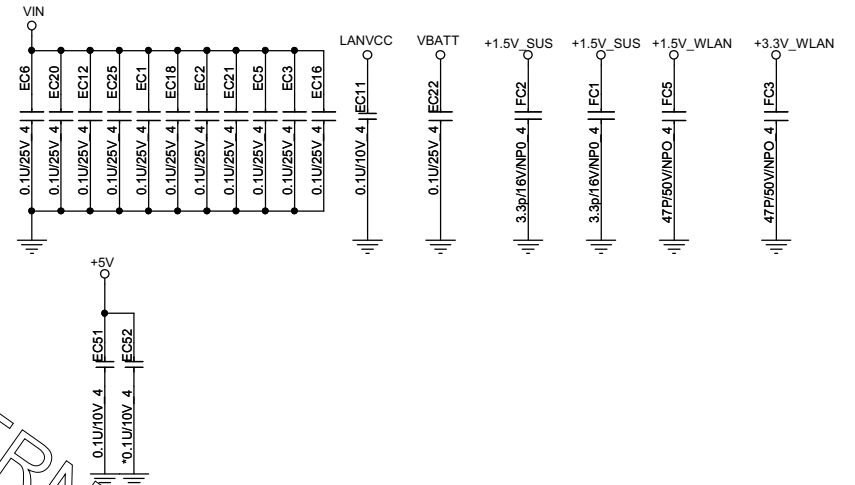
CPU BKT



For ESD



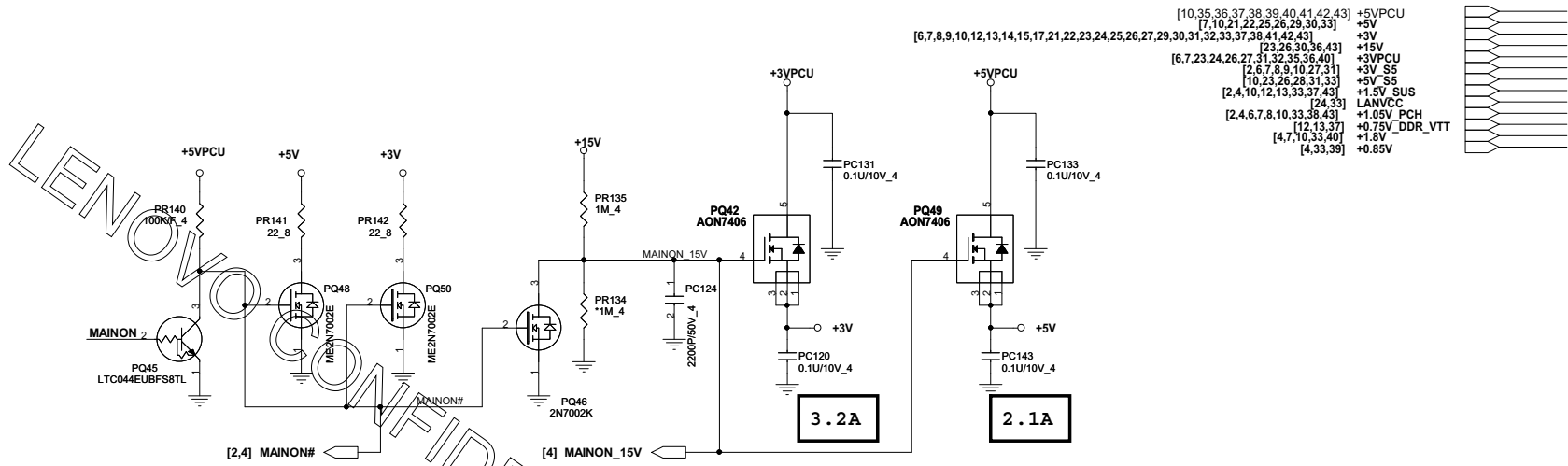
For EMI



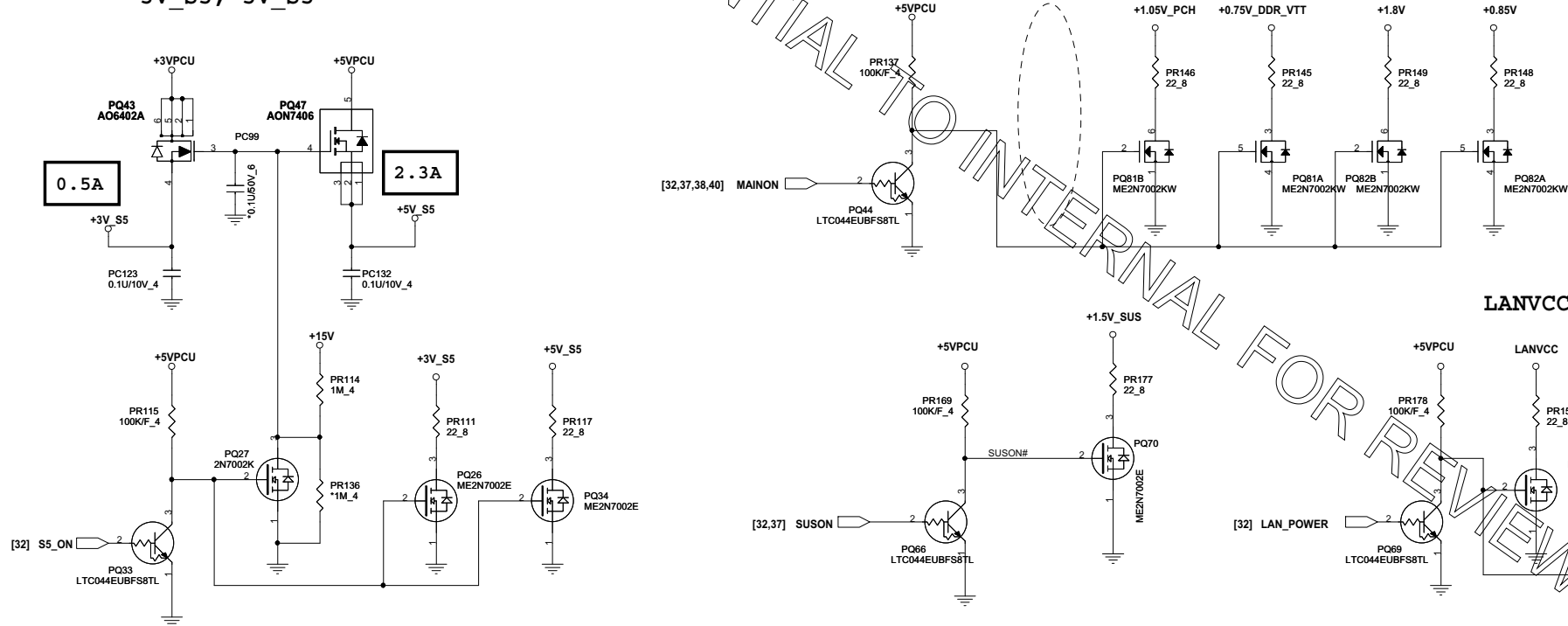
PROJECT : LZ2A
Quanta Computer Inc.

Size	Document Number	Rev
B	HOLD/SKEW/ESD/EMI	1A
Date:	Wednesday, November 30, 2011	Sheet 33 of 45

+3V, +5V

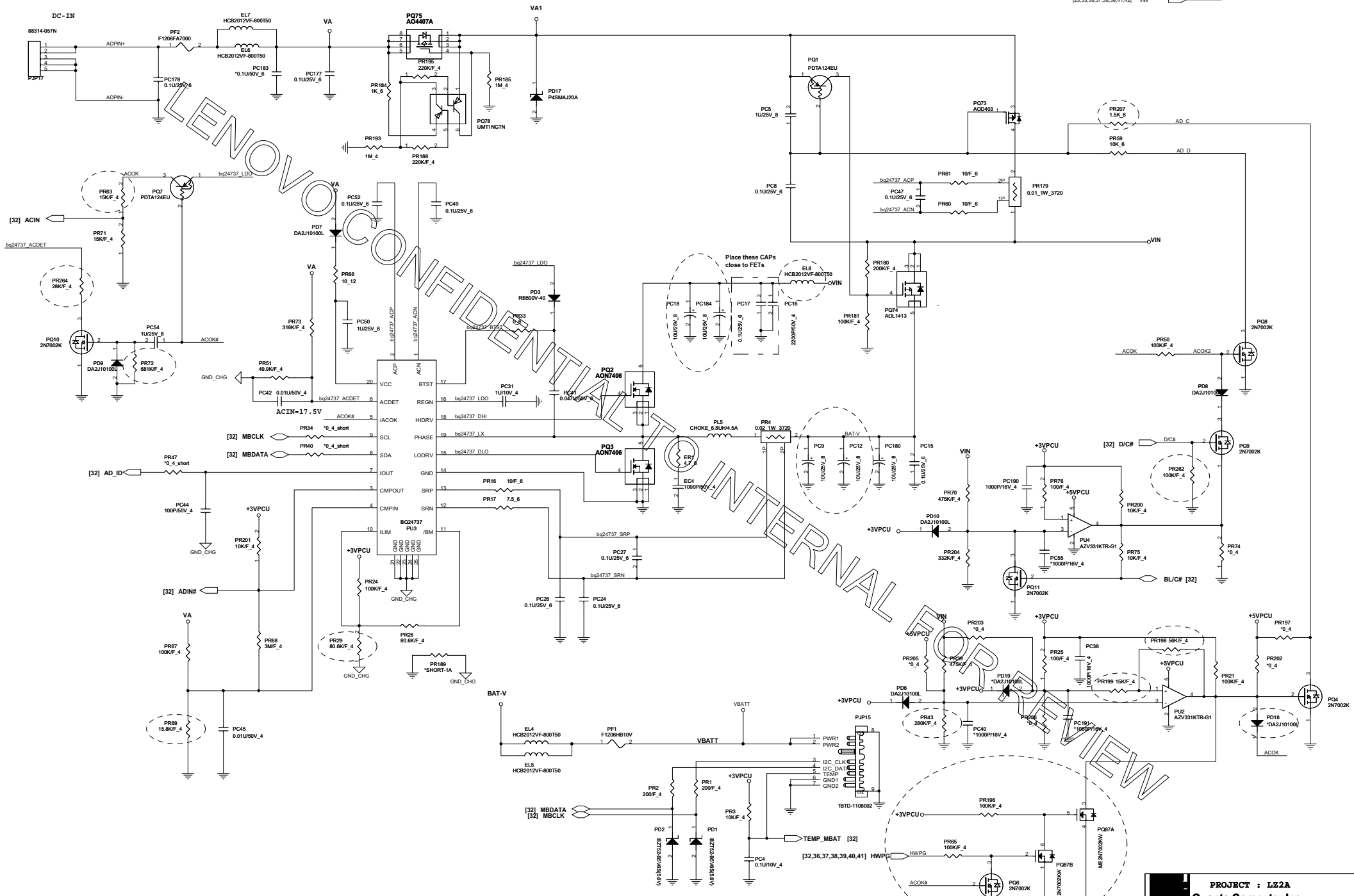


3V_S5, 5V_S5



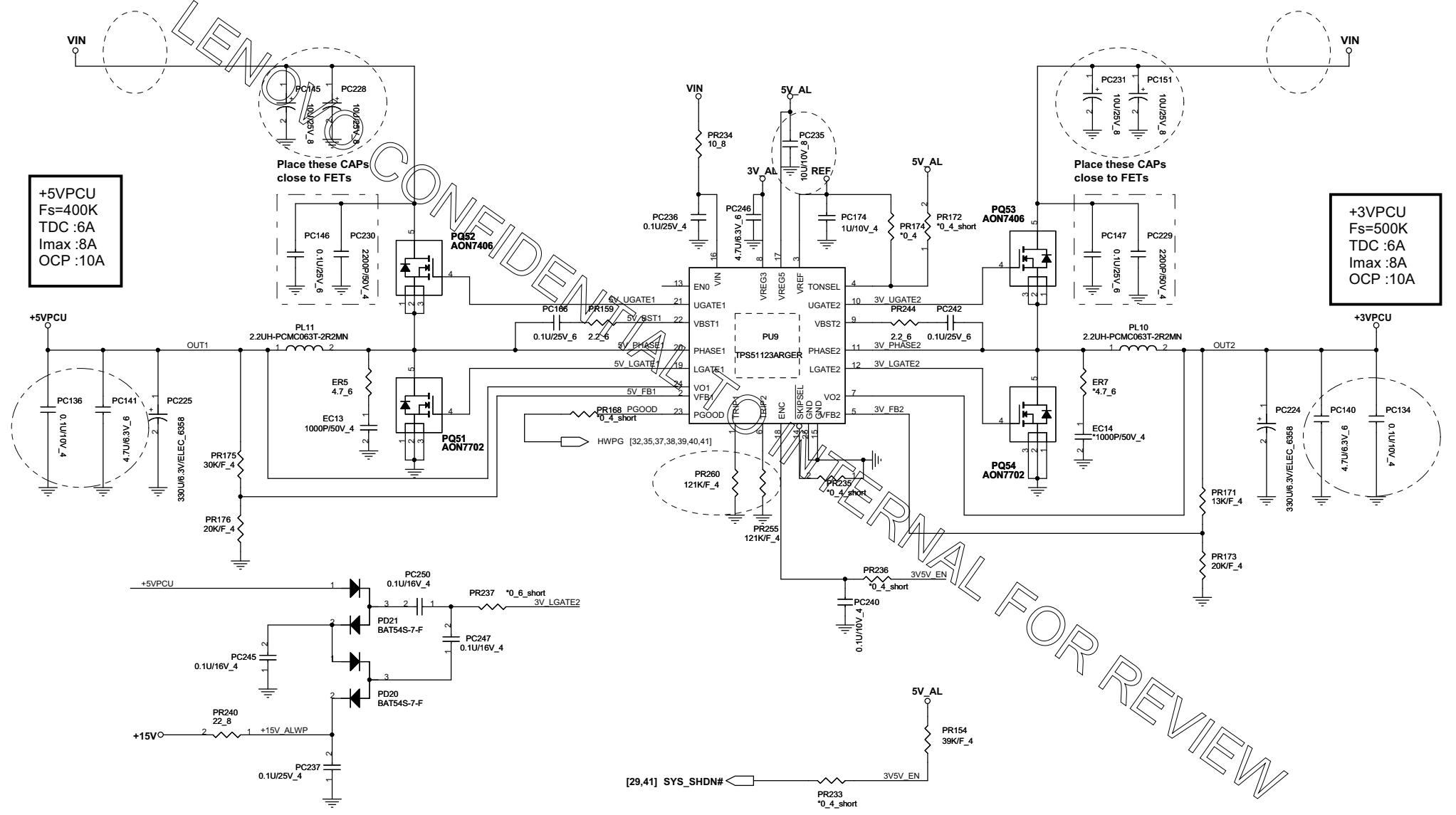
LANVCC

[8,7,23,24,26,27,31,32,34,36,40] +3VPCU
[33] VBATT
[23,33,36,37,38,39,41,42] VIN



CONFIDENTIAL / INTERNAL

[23,33,35,37,38,39,41,42]	VIN
	5V_AL
	3V_AL
	REF
[10,34,35,37,38,39,40,41,42,43]	+5VPCU
[23,26,30,34,43]	+15V
[6,7,23,24,26,27,31,32,34,35,40]	+3VPCU



+5VPCU
 Fs=400K
 TDC :6A
 I_{max} :8A
 OCP :10A

+3VPCU
 Fs=500K
 TDC :6A
 I_{max} :8A
 OCP :10A

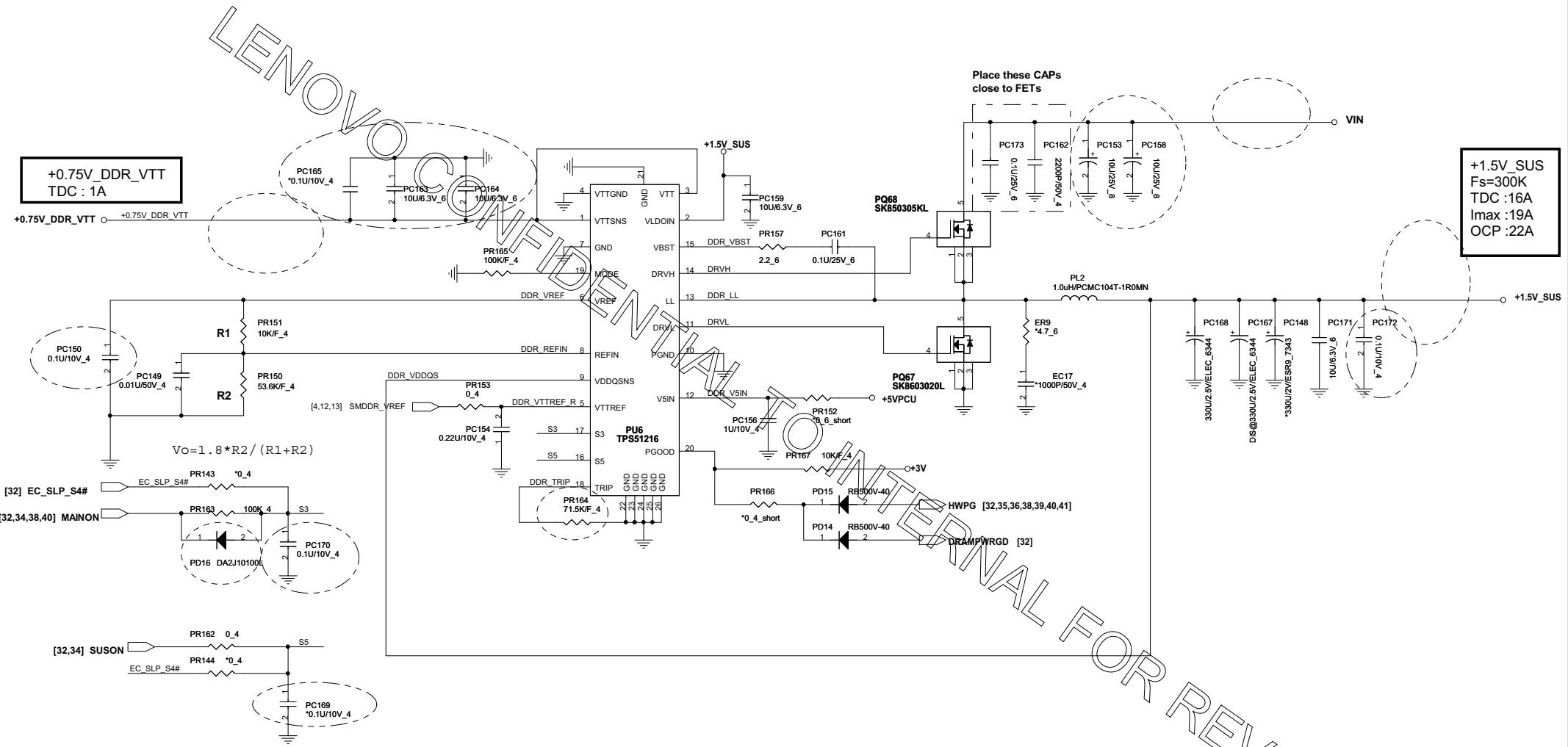
[12,13,34] +0.75V_DDR_VTT

[23,33,35,36,38,39,41,42] VIN

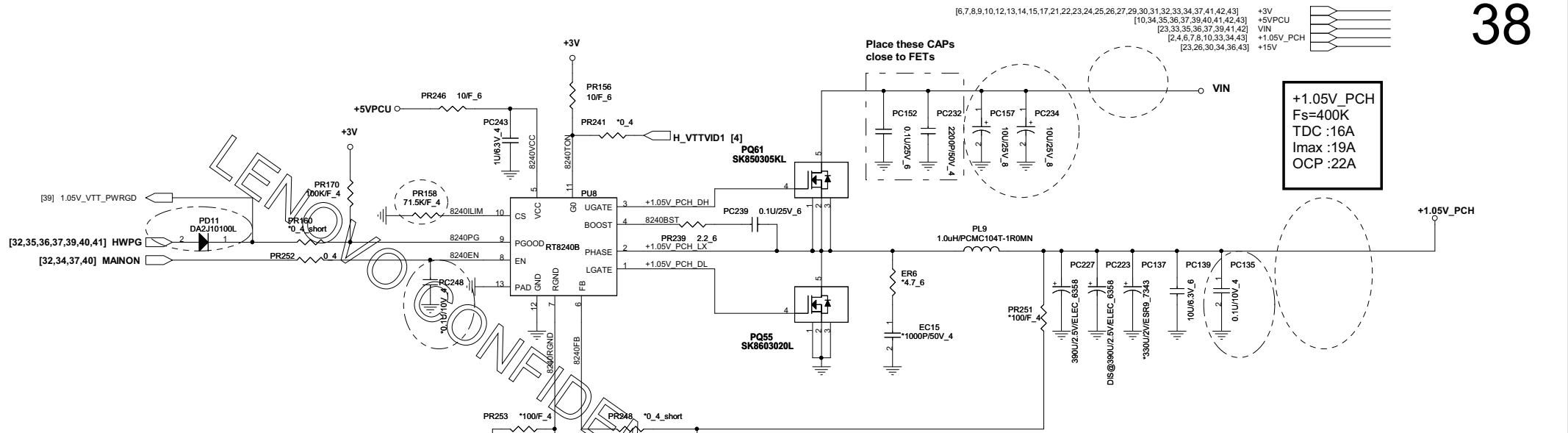
[2,4,10,12,13,33,34,43] +1.5V_SUS

+0.75V_DDR_VTT
TDC : 1A

+1.5V_SUS
Fs=300K
TDC :16A
Imax :19A
OCP :22A



INTERNAL FOR REVIEW

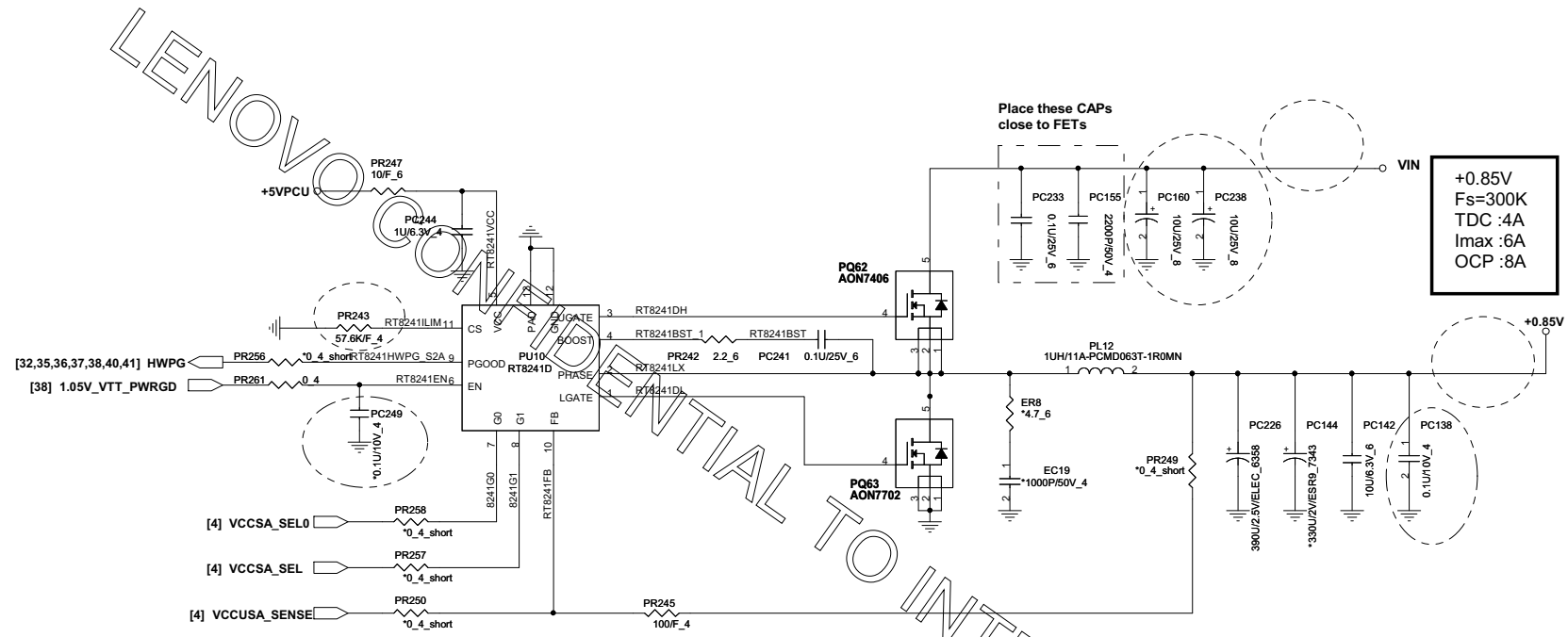


Place these CAPS close to FETs

+1.05V_PCH
 Fs=400K
 TDC :16A
 Imax :19A
 OCP :22A

CONFIDENTIAL TO INTERNAL FOR REVIEW

[10,34,35,36,37,38,40,41,42,43] +5VPCU
 [23,33,35,36,37,38,41,42] VIN
 [4,33,34] +0.85V



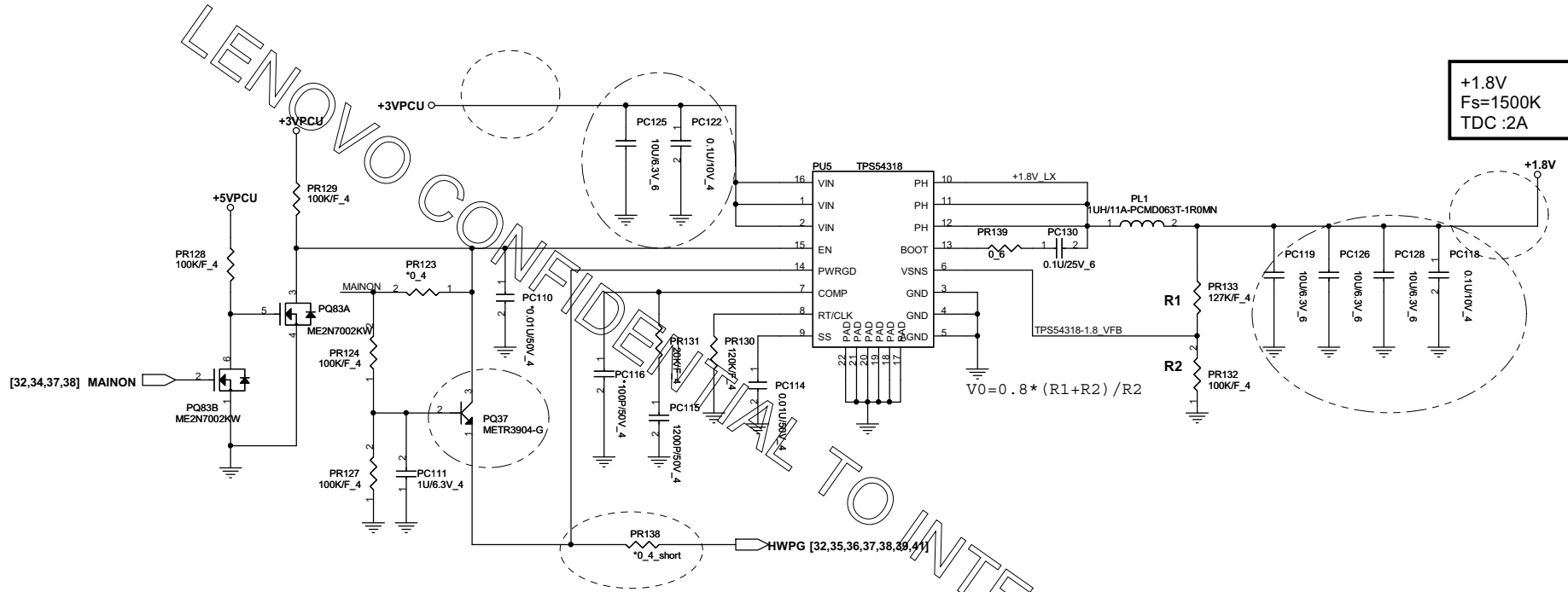
+0.85V
 Fs=300K
 TDC :4A
 Imax :6A
 OCP :8A

G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V

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[10,34,35,36,37,38,39,41,42,43] +5VPCU
[6,7,23,24,26,27,31,32,34,35,36] +3VPCU
[4,7,10,33,34] +1.8V

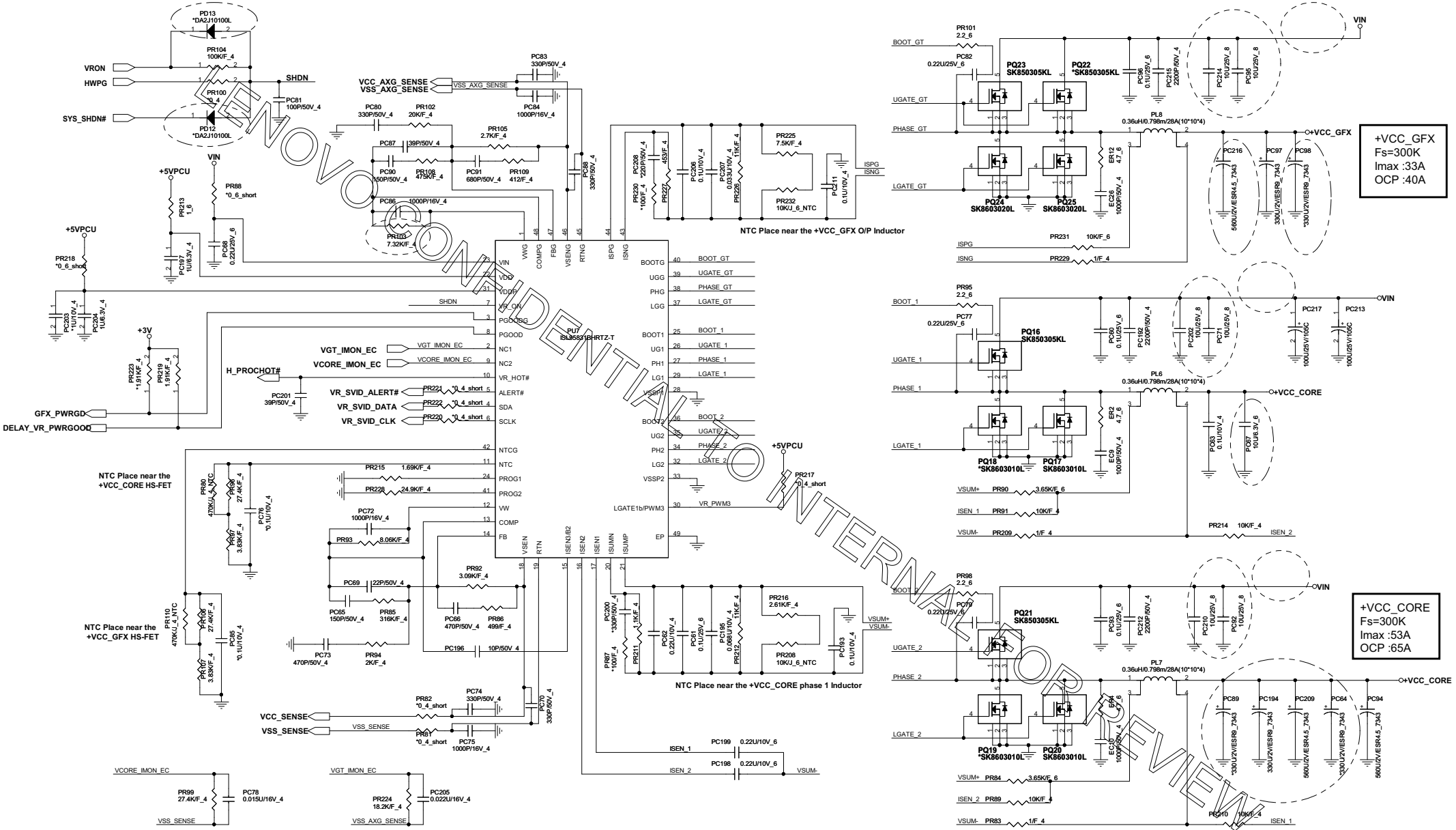


+1.8V
Fs=1500K
TDC :2A

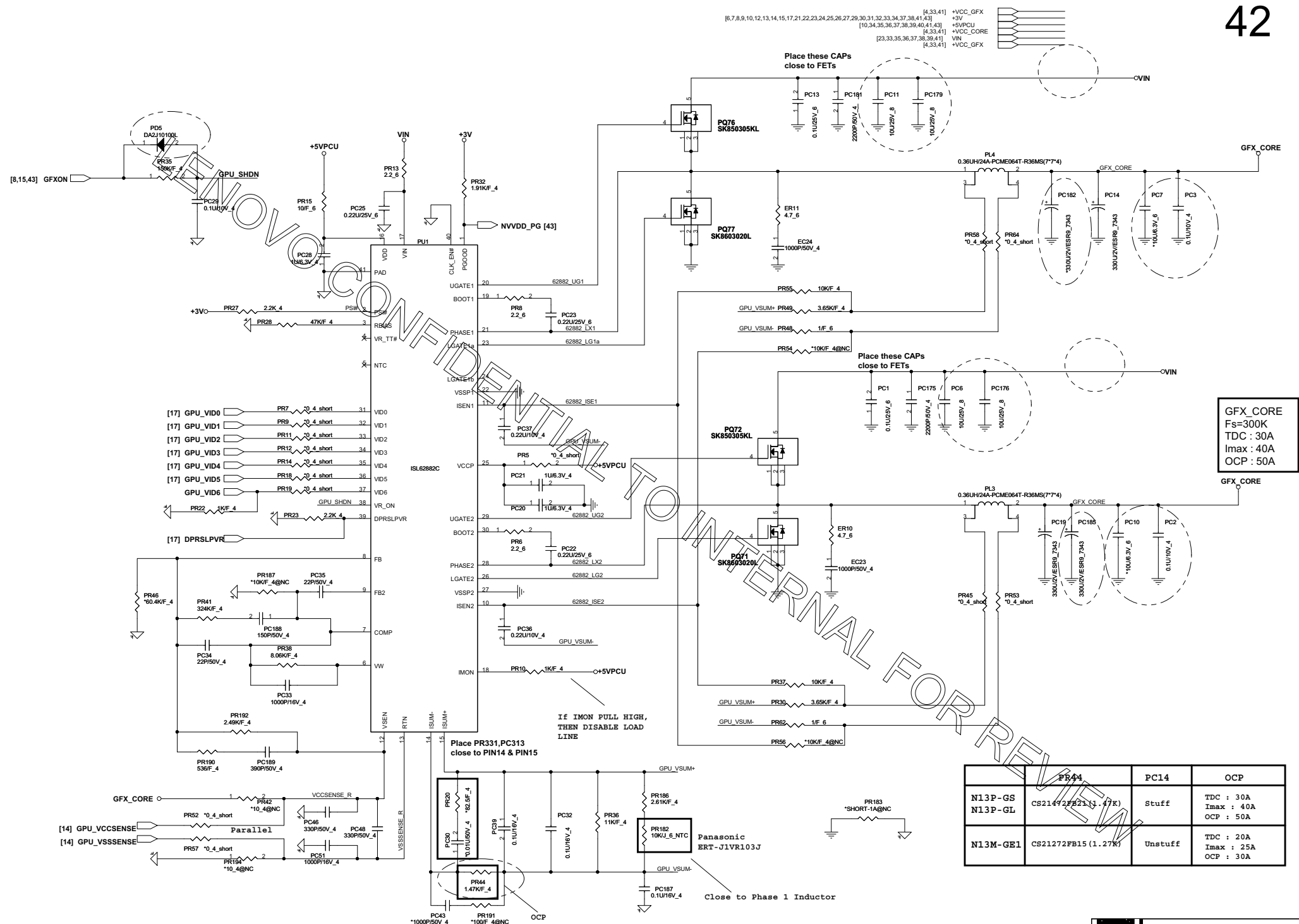
$$V0 = 0.8 * (R1 + R2) / R2$$

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+VCC_GFX
+3V
+5VPCU
+VCC_CORE
VIN
+VCC_GFX



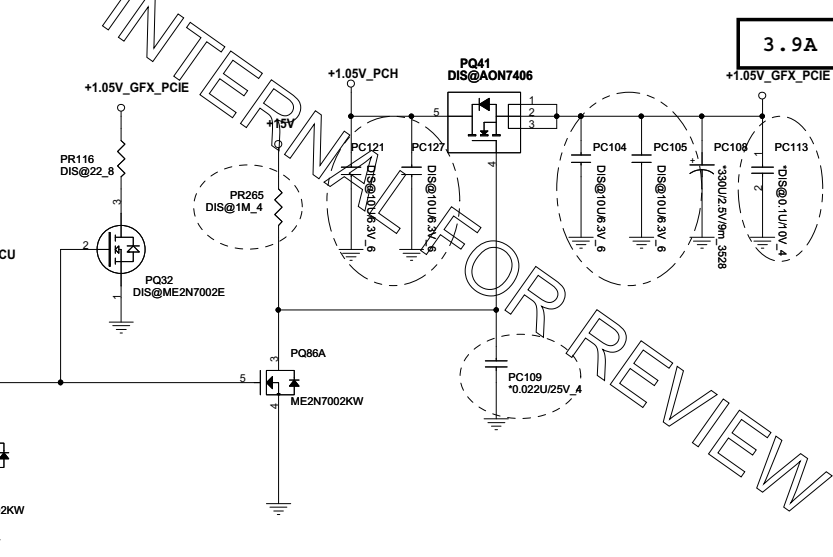
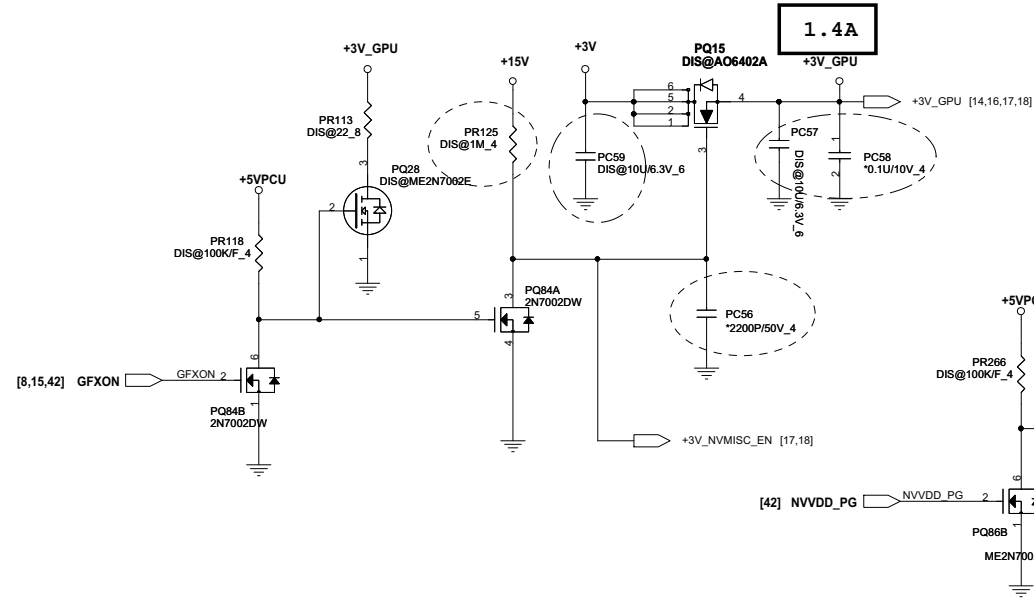
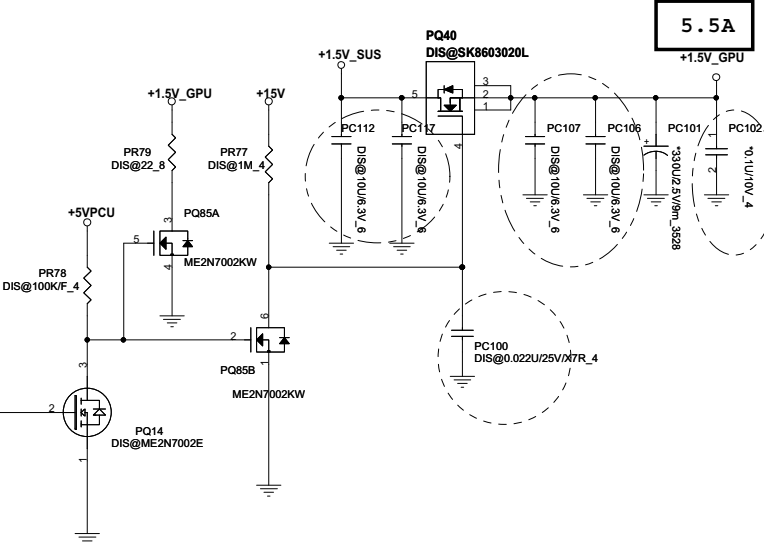
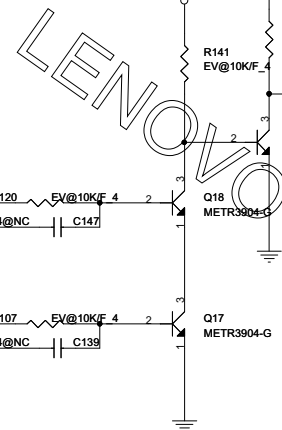
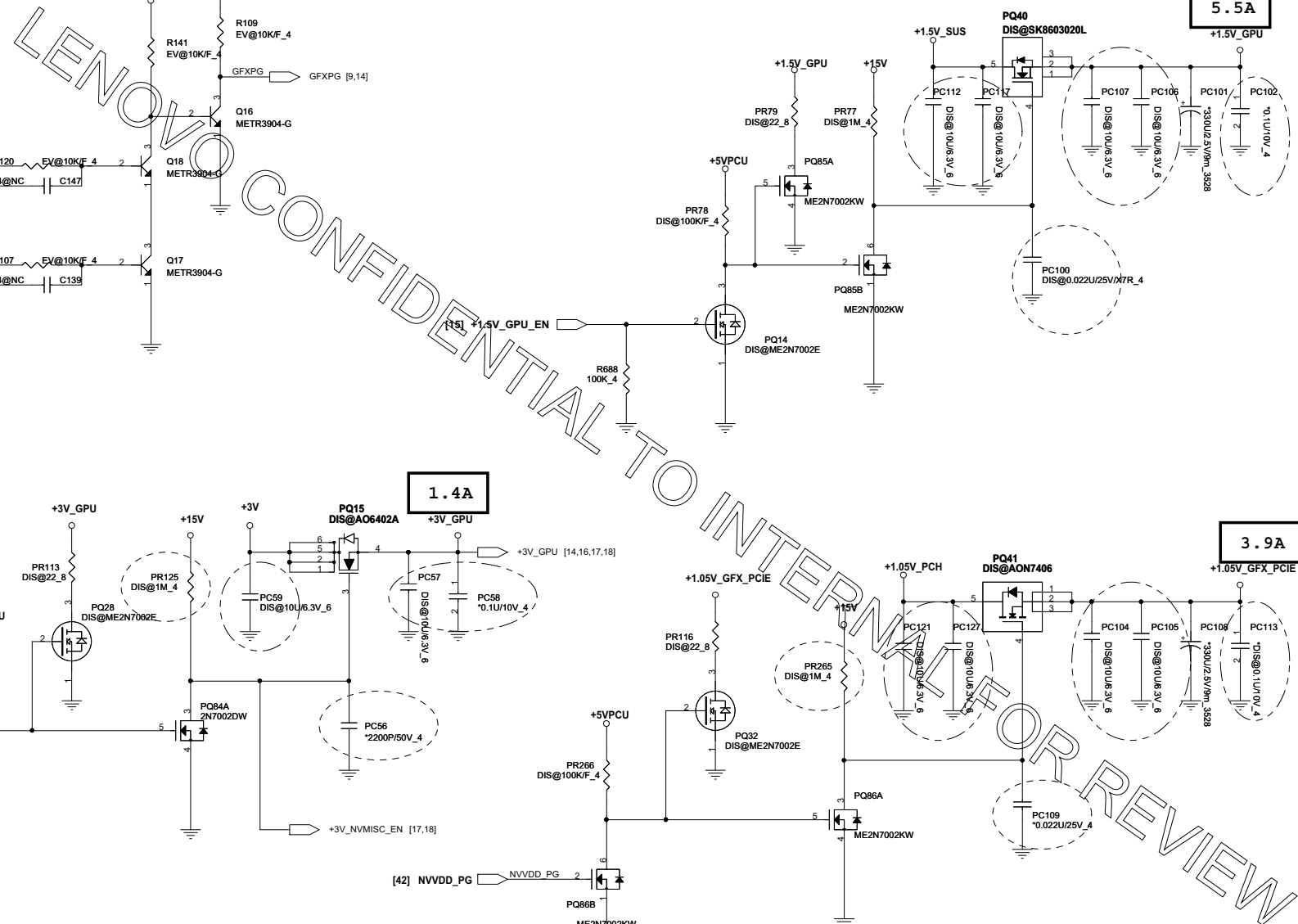
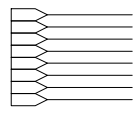
[4,33,41] +VCC_GFX
 [4,33,41] +3V
 [10,34,35,36,37,38,39,40,41,43] +5VPCU
 [4,33,41] +VCC_CORE
 [23,33,35,36,37,38,39,41] VIN
 [4,33,41] +VCC_GFX



GFX_CORE
 Fs=300K
 TDC : 30A
 I_{max} : 40A
 OCP : 50A

	PR44	PC14	OCP
N13P-GS	CS21492FB21(1.47K)	Stuff	TDC : 30A
N13P-GL		Stuff	I _{max} : 40A
			OCP : 50A
N13M-GE1	CS21272FB15(1.27K)	Unstuff	TDC : 20A
			I _{max} : 25A
			OCP : 30A

[6,7,8,9,10,12,13,14,15,17,21,22,23,24,25,26,27,29,30,31,32,33,34,37,38,41,42]	+3V
[14,16,17,18]	+3V_GPU
[10,34,35,36,37,38,39,40,41,42]	+5VPCU
[14,15,19,20,33]	+1.5V_GPU
[23,28,30,34,36]	+15V
[2,4,10,12,13,33,34,37]	+1.5V_SUS
[14,15,16,33]	+1.05V_GFX_PCIE
[2,4,6,7,8,10,33,34,38]	+1.05V_PCH



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