

Compal Confidential

DCL55 Schematics Document

Banias ICP uFCBGA/uFCPGA Package with Montara-GM Core Logic

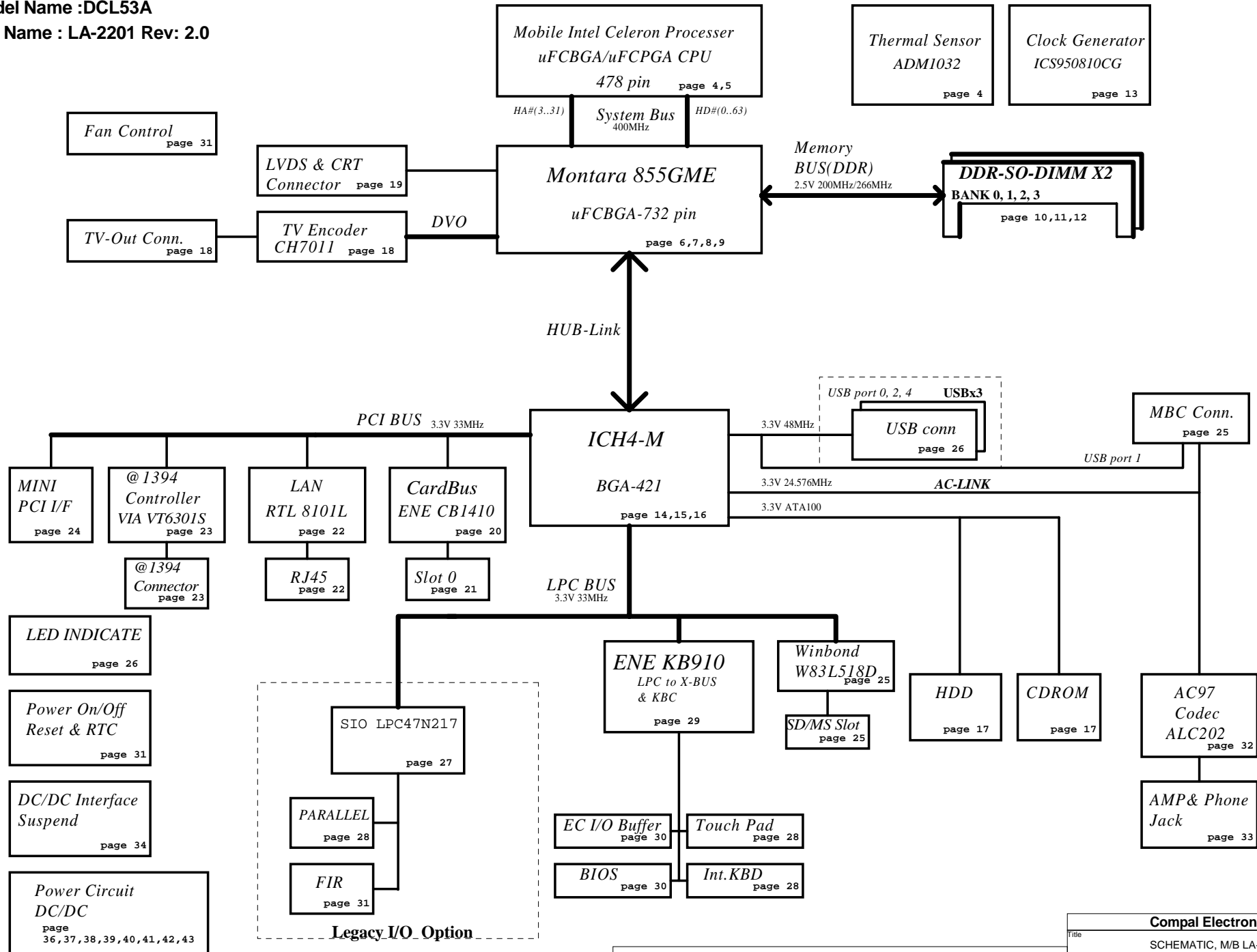
2005-05-23

REV: 3.0

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Model Name :DCL53A
File Name : LA-2201 Rev: 2.0



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
R368	100K +/- 5%			
Board ID	R361	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

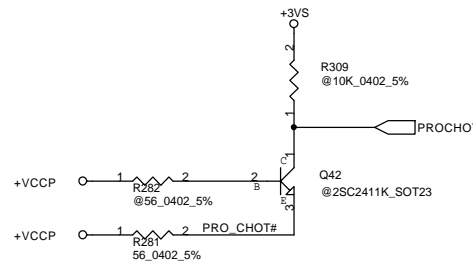
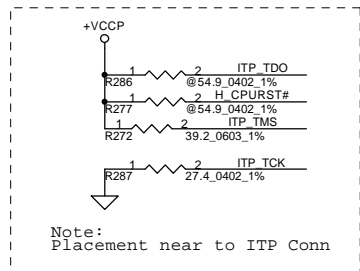
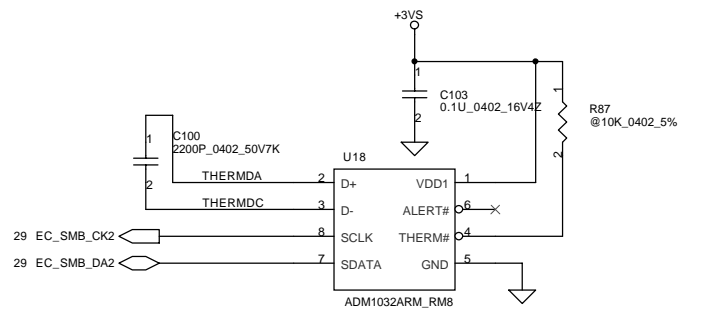
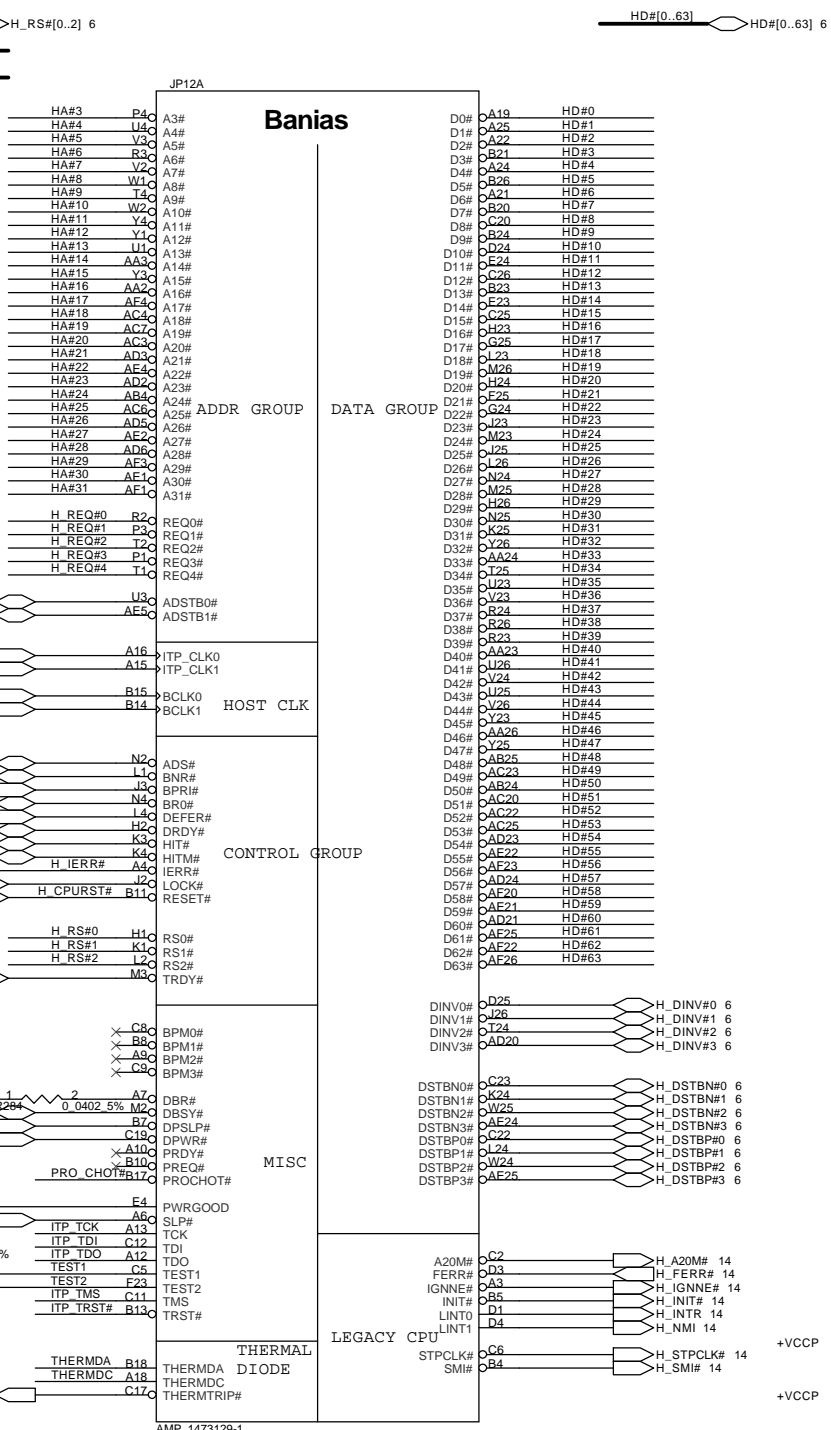
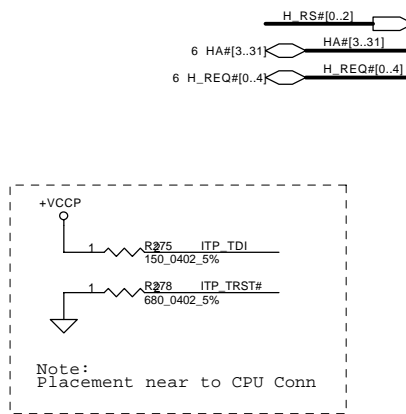
Board ID	PCB Revision
0	
1	0.1
2	0.2
3	1.0
4	
5	
6	
7	

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

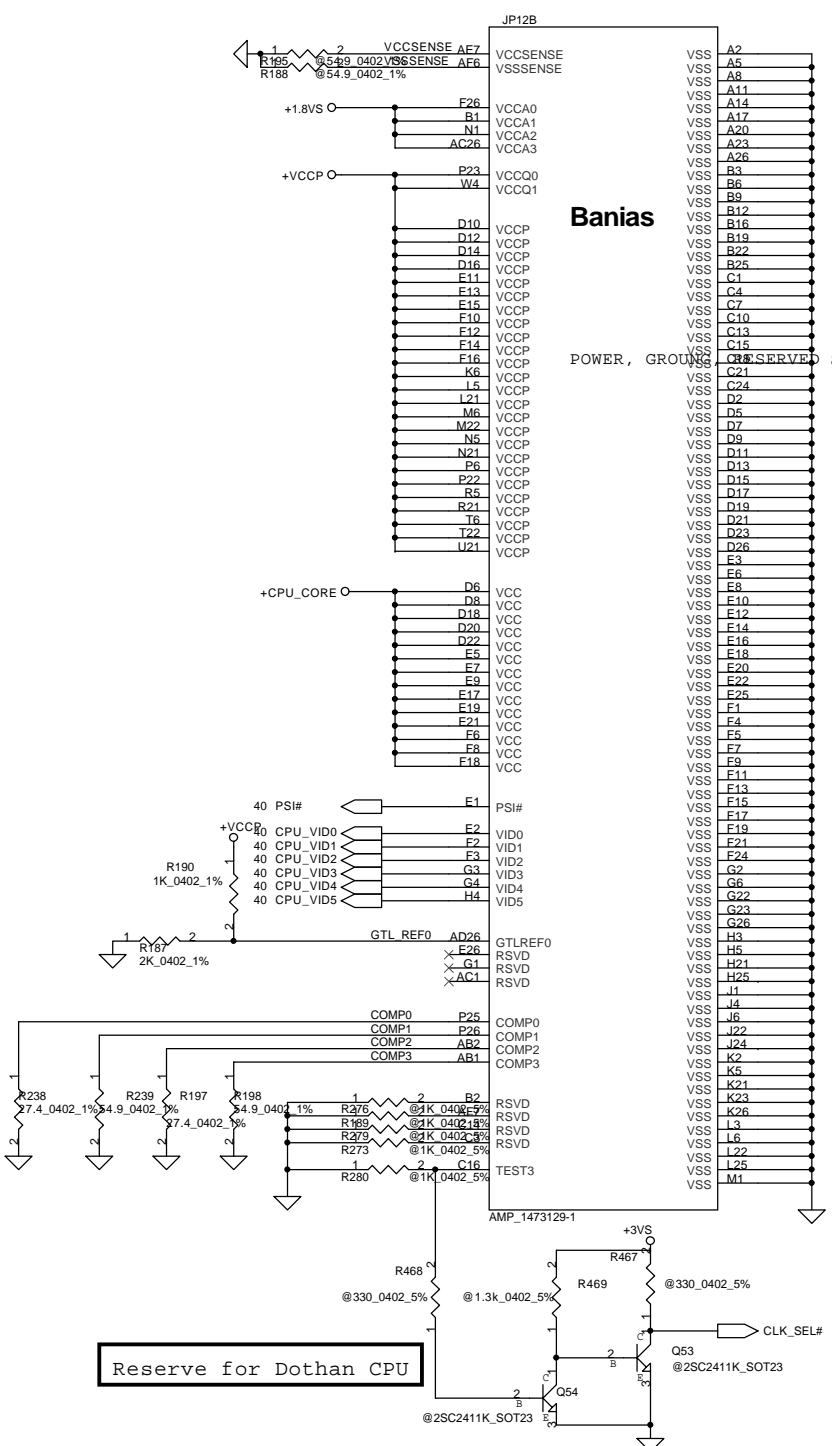
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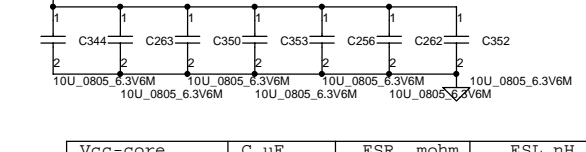
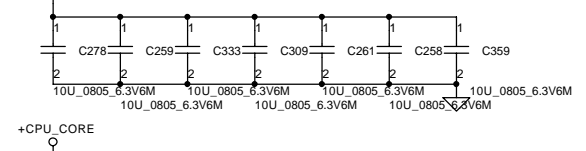
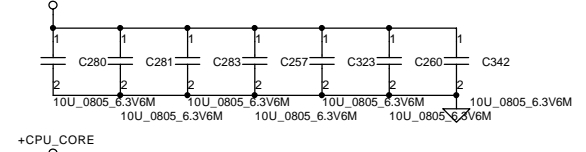
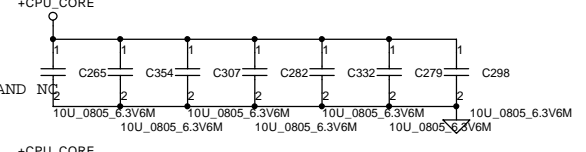
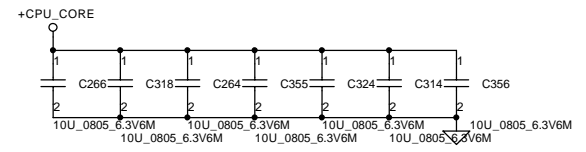
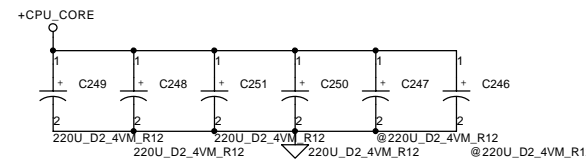
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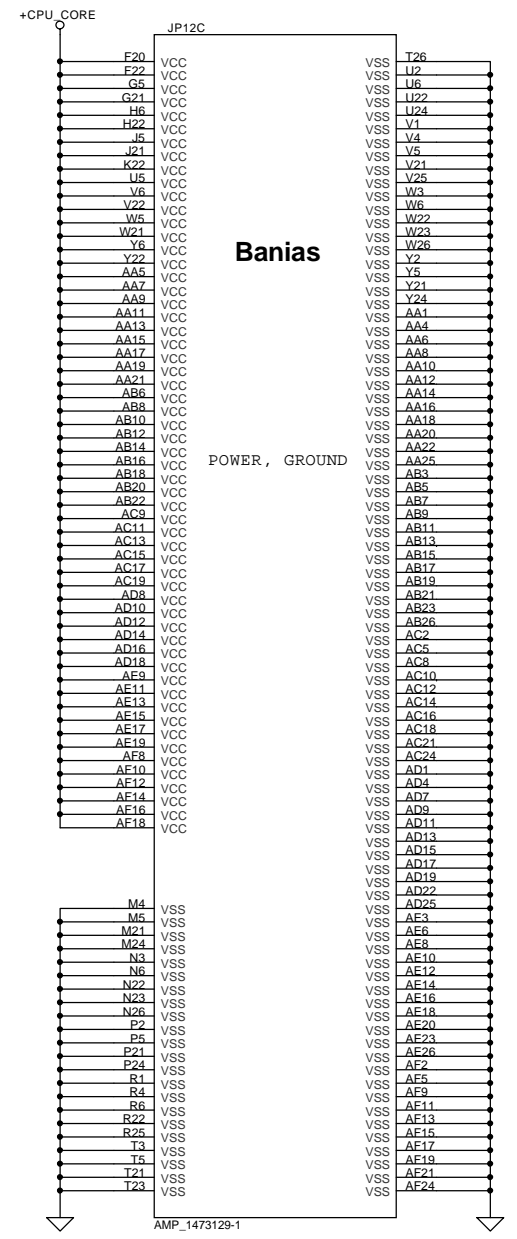
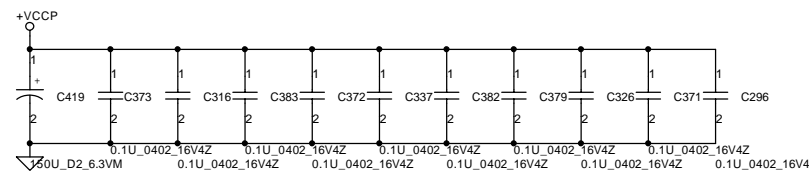
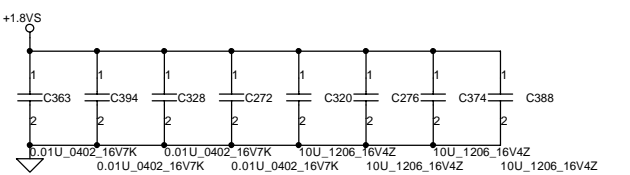


Banias

POWER, GROUND RESERVED SIGNALS AND NC



Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35



Banias

POWER, GROUND

Reserve for Dothan CPU

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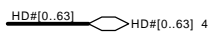
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Montara-GM(L)

HA#3	P23	HA#3	K22	HD#0
HA#4	T25	HA#4	H27	HD#1
HA#5	T28	HA#5	K25	HD#2
HA#6	R27	HA#6	L24	HD#3
HA#7	U23	HA#7	O27	HD#4
HA#8	U24	HA#8	G28	HD#5
HA#9	R24	HA#9	L27	HD#6
HA#10	U28	HA#10	L23	HD#7
HA#11	V28	HA#11	L25	HD#8
HA#12	U27	HA#12	J24	HD#9
HA#13	T27	HA#13	K23	HD#10
HA#14	V27	HA#14	G27	HD#11
HA#15	U25	HA#15	J23	HD#12
HA#16	V26	HA#16	H26	HD#13
HA#17	Y24	HA#17	E26	HD#14
HA#18	V25	HA#18	E25	HD#15
HA#19	V23	HA#19	H26	HD#16
HA#20	W25	HA#20	E26	HD#17
HA#21	Y25	HA#21	B27	HD#18
HA#22	AA27	HA#22	H23	HD#19
HA#23	W24	HA#23	E27	HD#20
HA#24	W23	HA#24	G25	HD#21
HA#25	W27	HA#25	E28	HD#22
HA#26	Y27	HA#26	O27	HD#23
HA#27	AA28	HA#27	G24	HD#24
HA#28	W28	HA#28	C28	HD#25
HA#29	AB27	HA#29	B26	HD#26
HA#30	Y26	HA#30	G22	HD#27
HA#31	AB26	HA#31	C26	HD#28



H_REQ#0	R28	HREQ#0
H_REQ#1	P25	HREQ#1
H_REQ#2	R23	HREQ#2
H_REQ#3	R25	HREQ#3
H_REQ#4	T23	HREQ#4
H_ADSTB#0	T26	HADSTB#0
H_ADSTB#1	AA26	HADSTB#1

HOST

AD29	BCLK#
AE29	BCLK
K28	HYSWING
B18	HXSWING
H28	HYRCOMP
B20	HXRCOMP

K21	HVREF0
J21	HVREF1
J17	HVREF2
Y28	HCCVREF
Y22	HAVREF

H_DSTBN#0	J28	HDSTBN#0
H_DSTBN#1	C27	HDSTBN#1
H_DSTBN#2	E22	HDSTBN#2
H_DSTBN#3	D18	HDSTBN#3
H_DSTBP#0	K27	HDSTBP#0
H_DSTBP#1	D26	HDSTBP#1
H_DSTBP#2	E21	HDSTBP#2
H_DSTBP#3	E18	HDSTBP#3
H_DINV#0	J25	DINV#0
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H_DINV#2	B25	DINV#2
H_DINV#3	G19	DINV#3

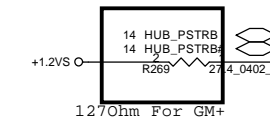
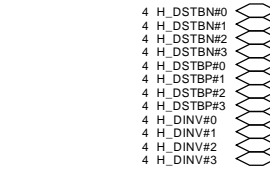
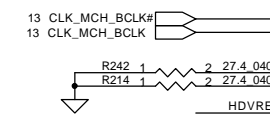
CPURST#	F15	CPURST#
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HUB_PD0	U17	HL_0
HUB_PD1	U4	HL_1
HUB_PD2	U3	HL_2
HUB_PD3	V3	HL_3
HUB_PD4	W2	HL_4
HUB_PD5	W6	HL_5
HUB_PD6	V6	HL_6
HUB_PD7	W7	HL_7
HUB_PD8	T3	HL_8
HUB_PD9	V5	HL_9
HUB_PD10	V4	HL_10
HI_PSTRB	W3	HLSTB
HI_PSTRB#	V2	HLSTB#
HUB_VSWING	T2	HLRCOMP
HUB_VREF	U2	PSWING
	W1	HLVREF

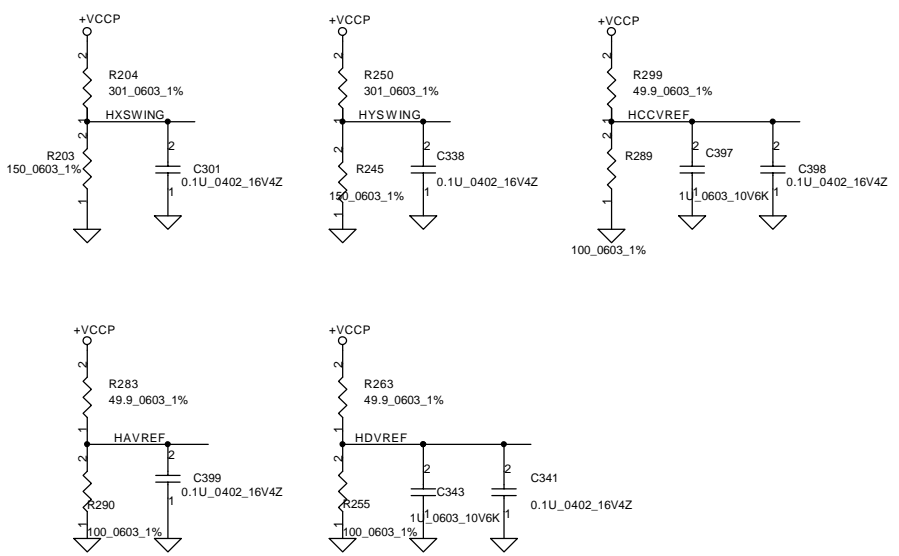
HUB I/F

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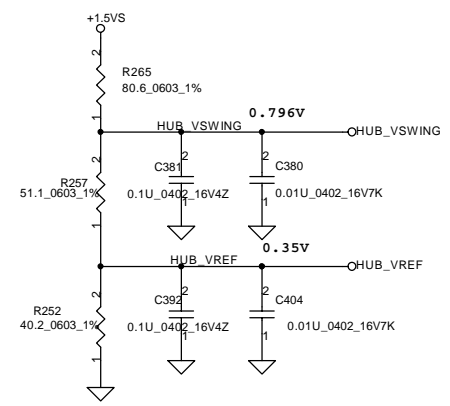
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M25	H_TRDY#	4
M24	H_DRDY#	4
M28	H_DEFER#	4
N28	H_HIT#	4
N27	H_HIT#	4
M23	H_LOCK#	4
M25	H_BR0#	4
E28	H_BNR#	4
M26	H_BPR#	4
N23	H_DBSY#	4
P26	H_RS#0	4
M27	H_RS#1	4
M27	H_RS#2	4



HOST REF VOLTAGE



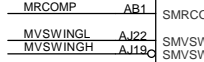
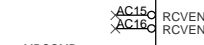
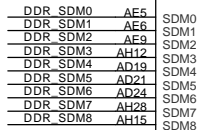
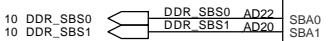
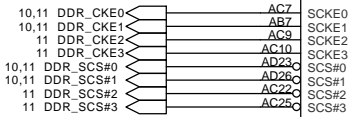
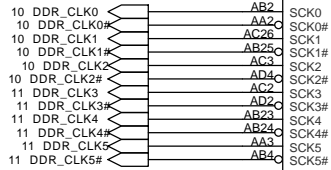
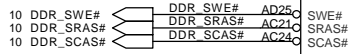
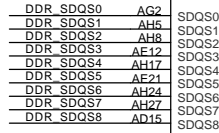
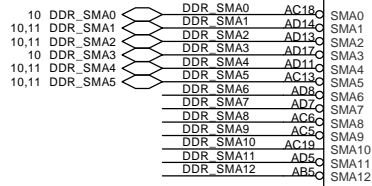
HUB I/F REF VOLTAGE



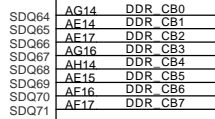
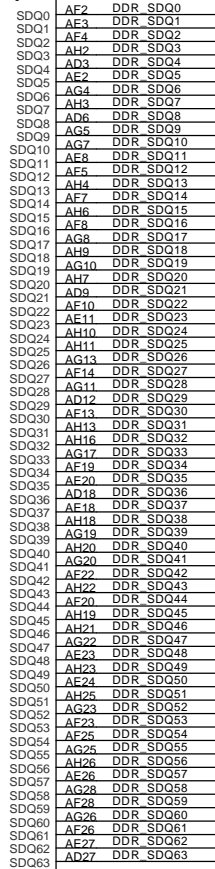
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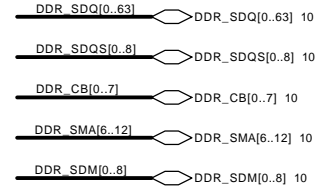
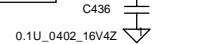
Montara-GM(L)



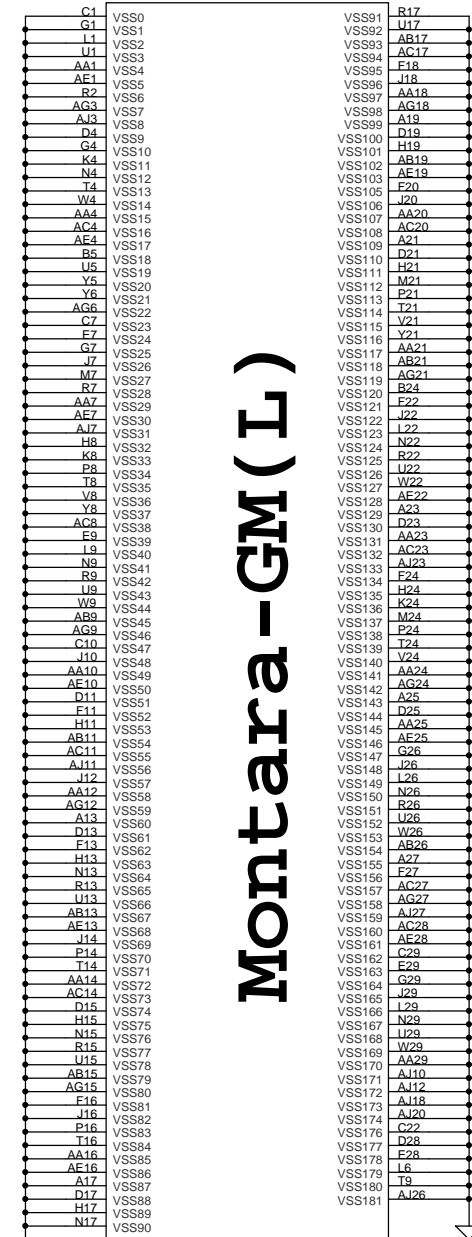
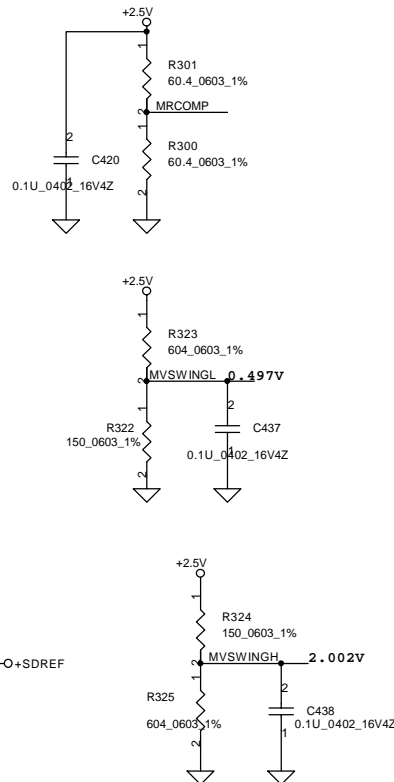
MEMORY



RG82G4350M_uFCBGA732



DDR REF & SWING VOLTAGE



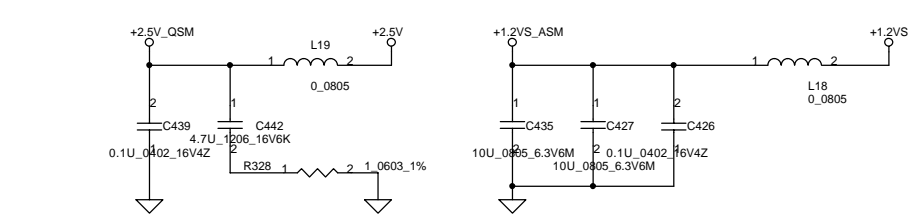
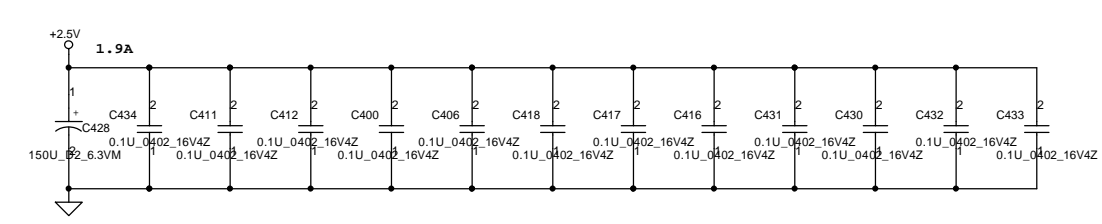
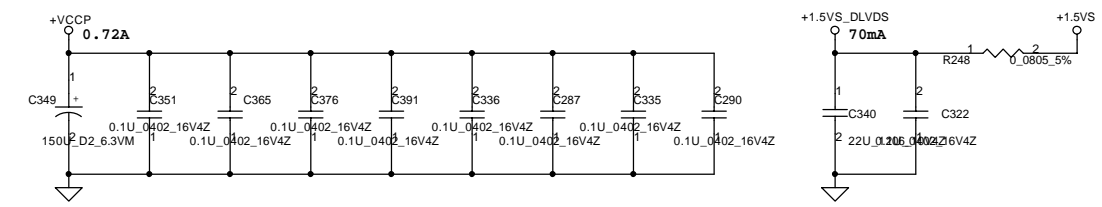
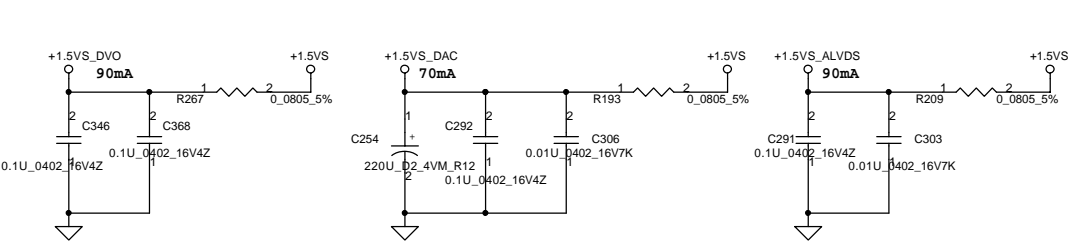
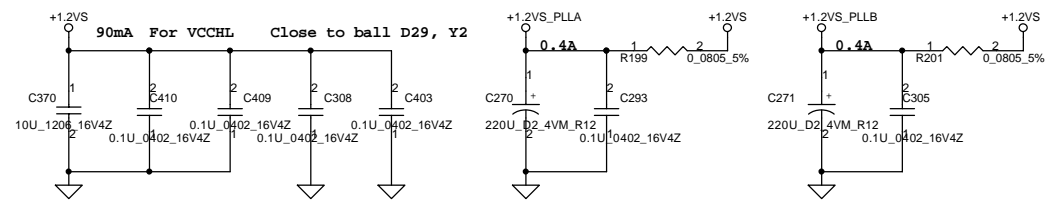
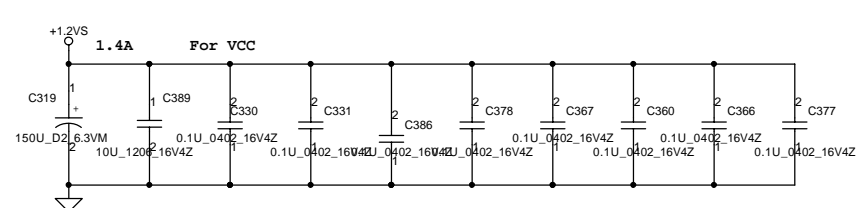
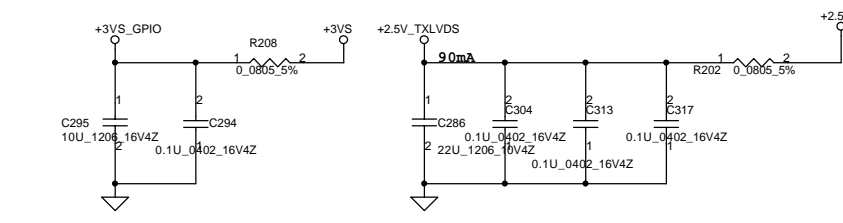
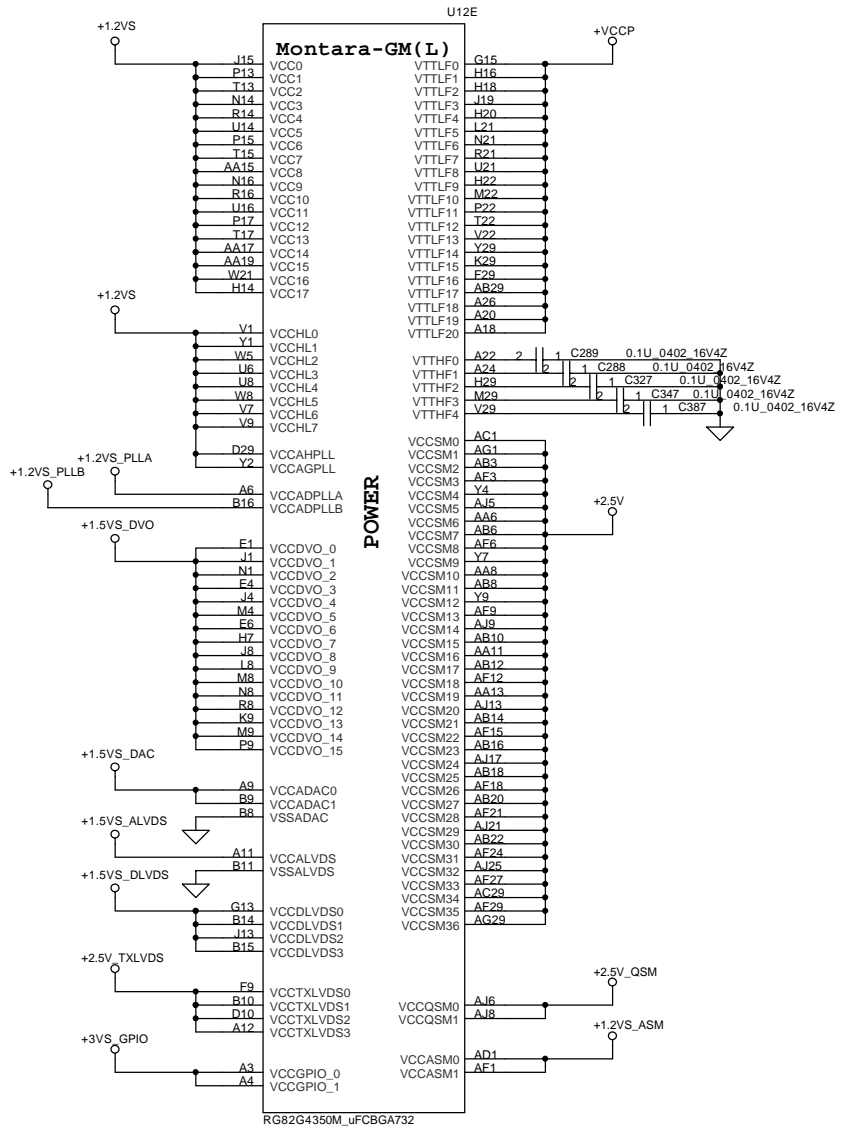
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Montara-GM(L)

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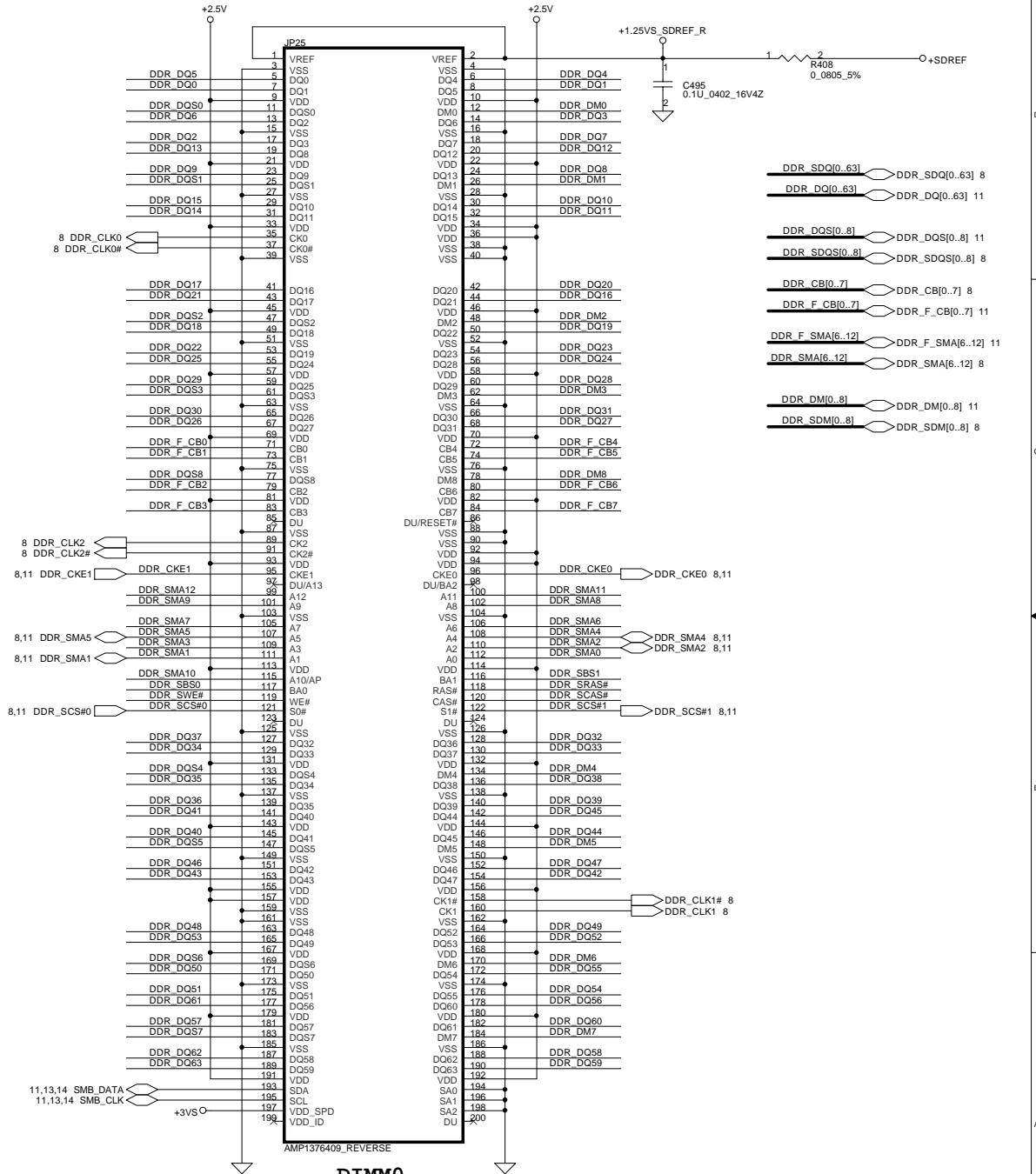
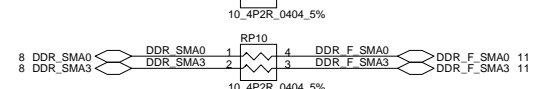
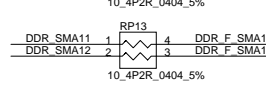
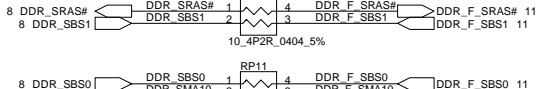
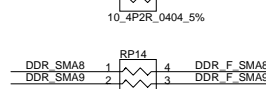
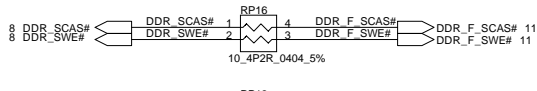
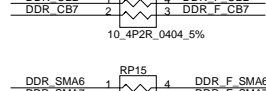
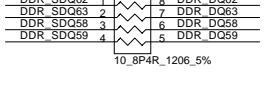
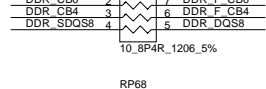
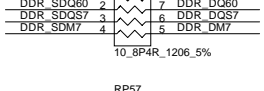
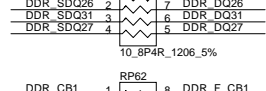
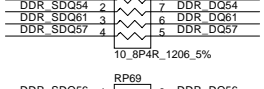
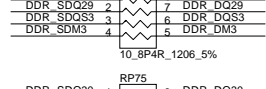
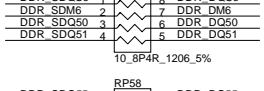
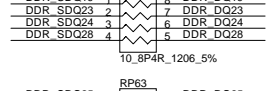
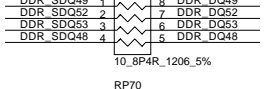
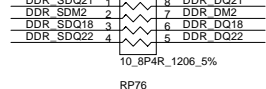
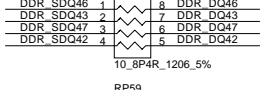
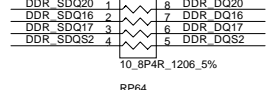
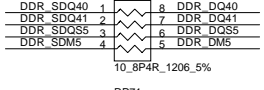
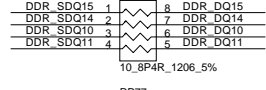
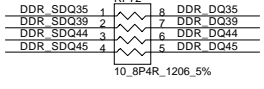
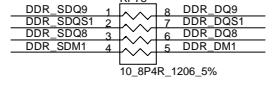
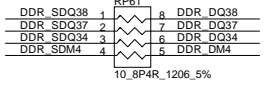
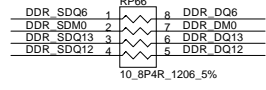
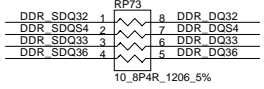
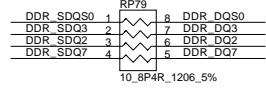
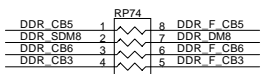
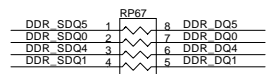
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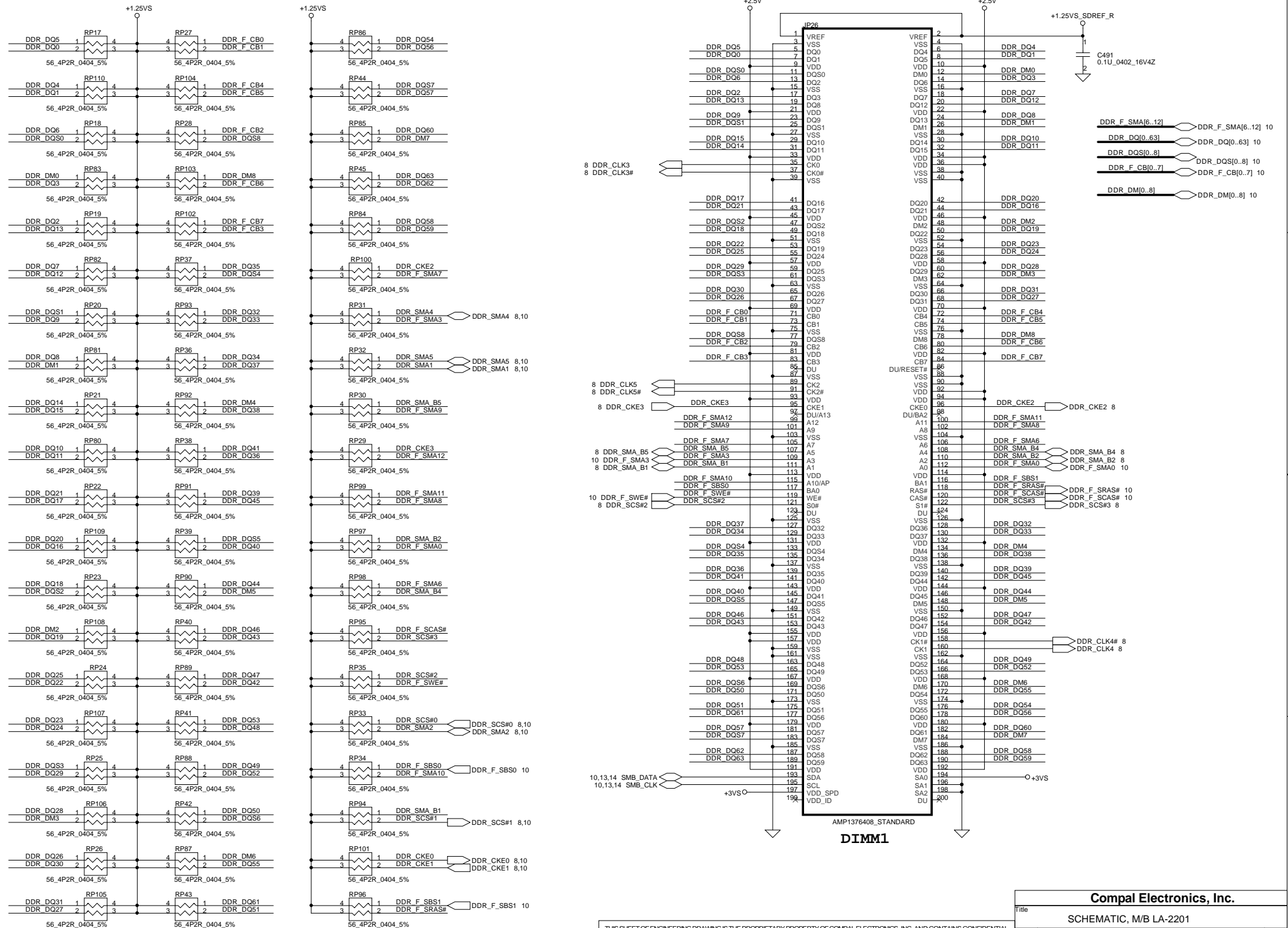
- DDR DQ0[0..63] 8
- DDR DQ1[0..63] 11
- DDR DQ5[0..8] 11
- DDR DQ5[0..8] 8
- DDR CB[0..7] 8
- DDR F CB[0..7] 11
- DDR F SMA[6..12] 11
- DDR SMA[6..12] 8
- DDR DM[0..8] 11
- DDR SDM[0..8] 8

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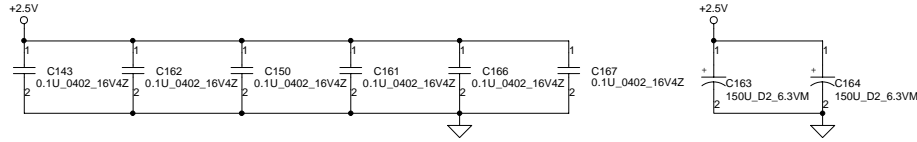
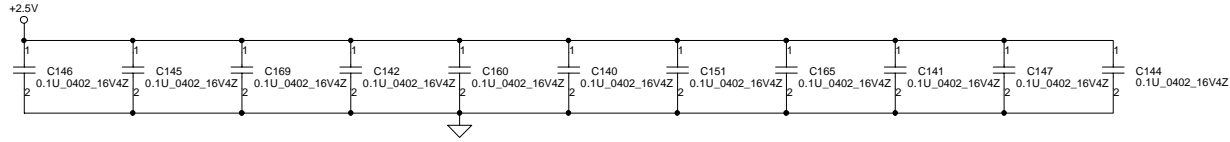


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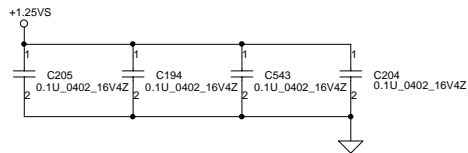
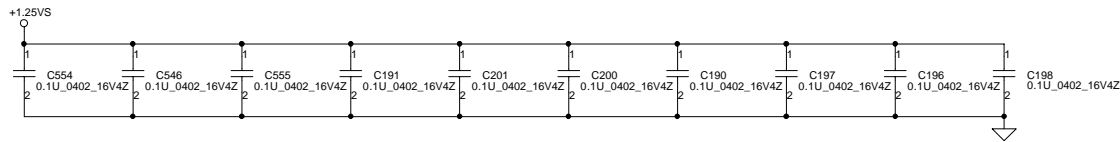
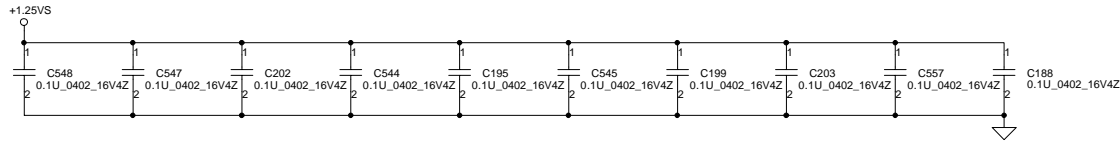
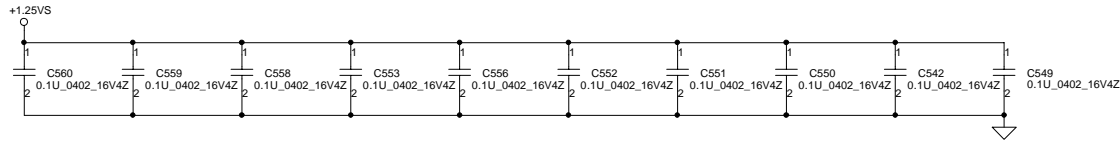
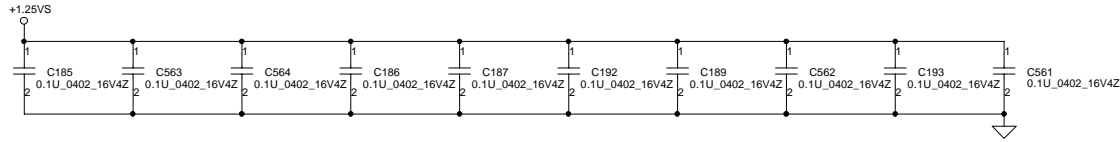
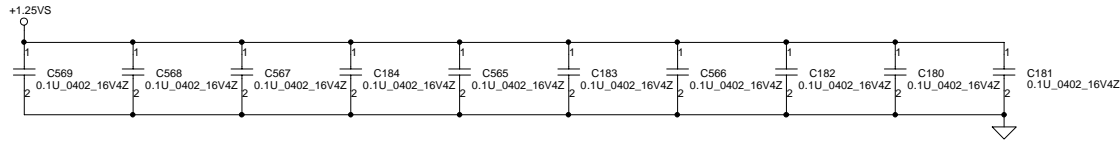
Layout note :

Distribute as close as possible to DDR-SODIMM.



Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25V



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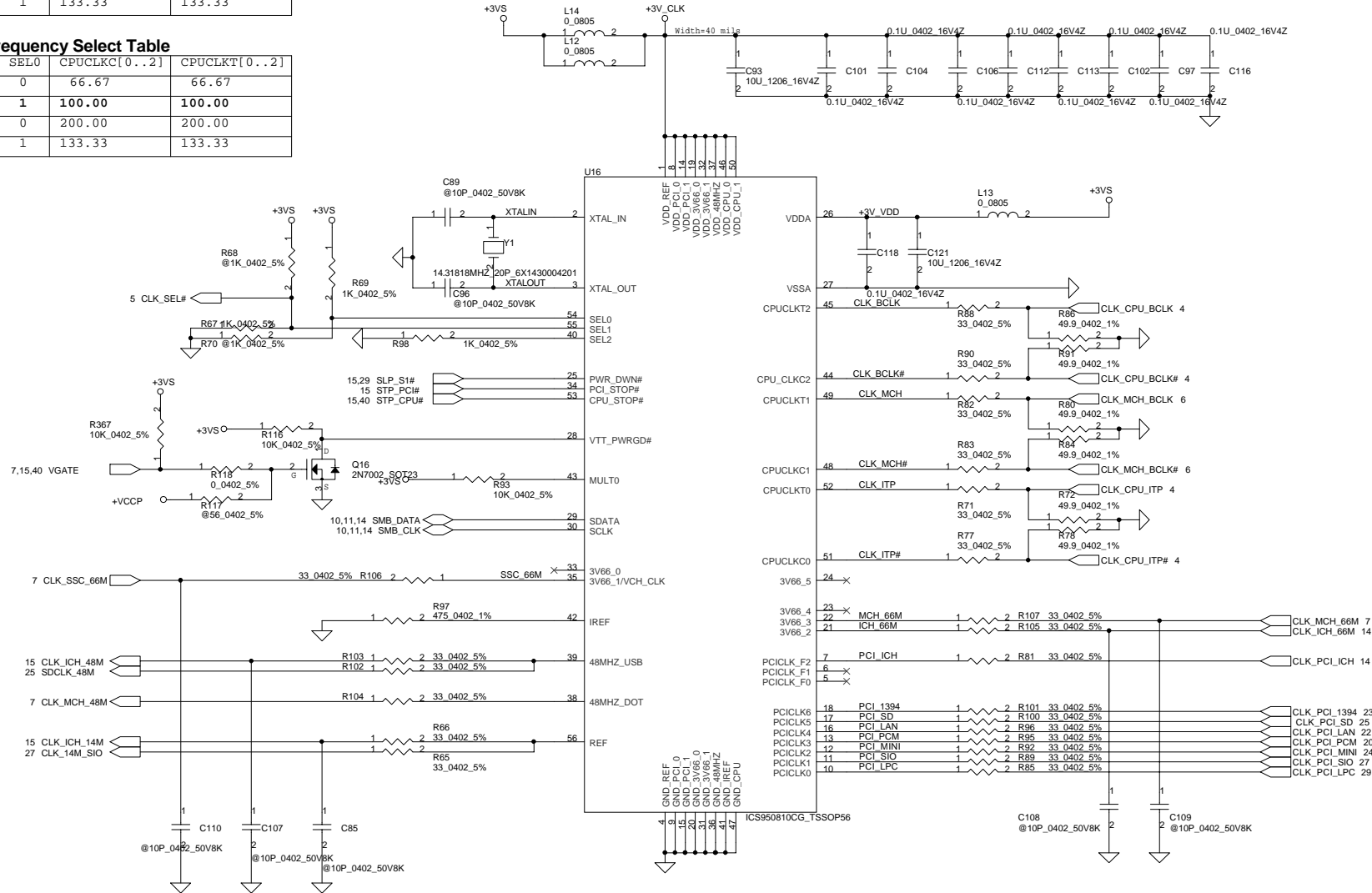
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ICS950810 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

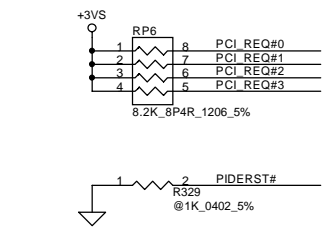
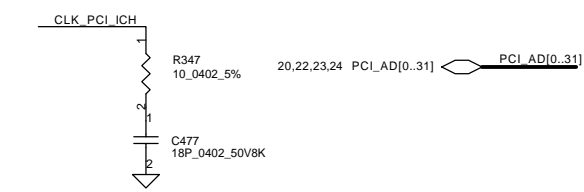
CY28346-2 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

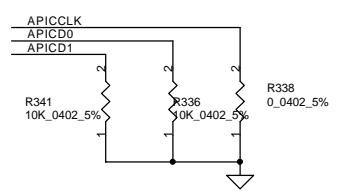
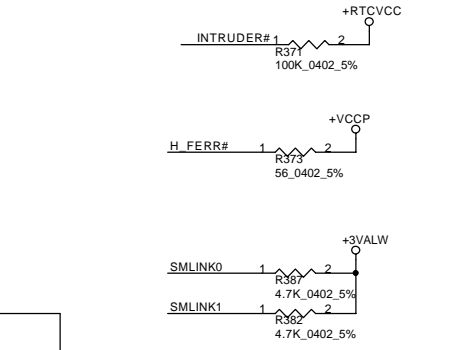
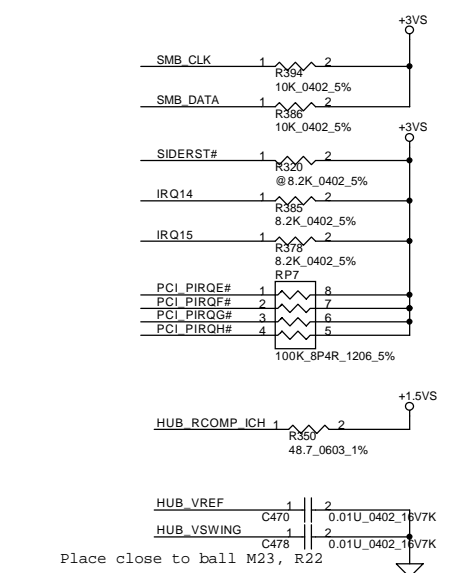
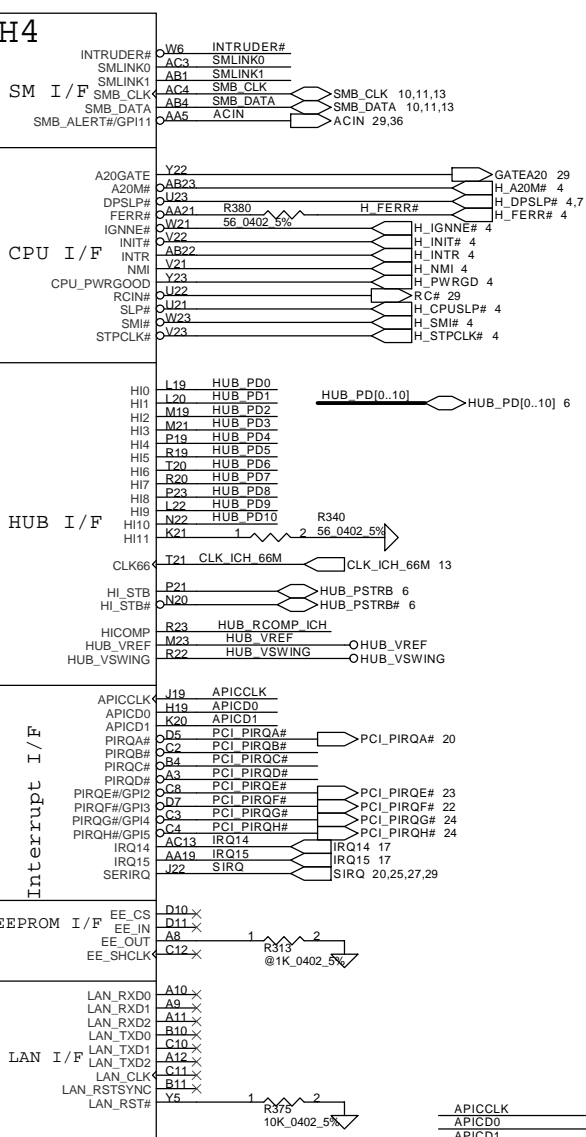
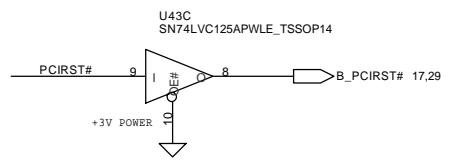
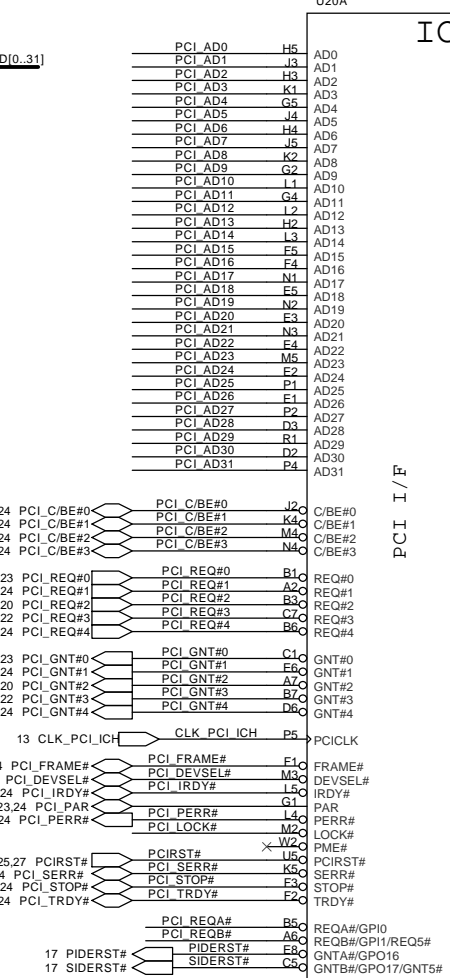
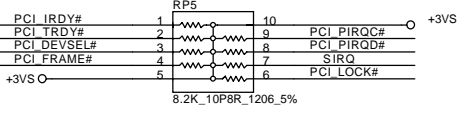
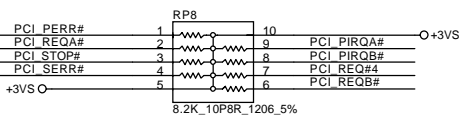


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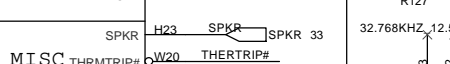
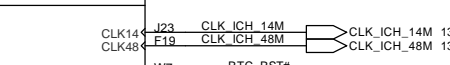
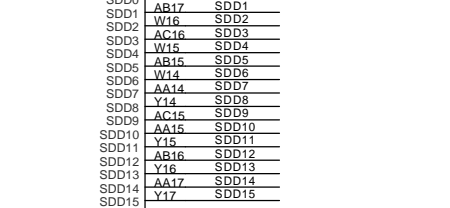
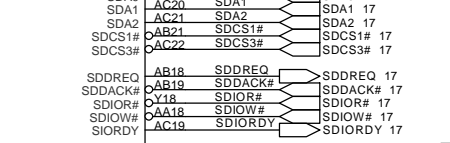
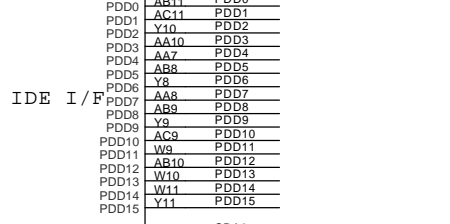
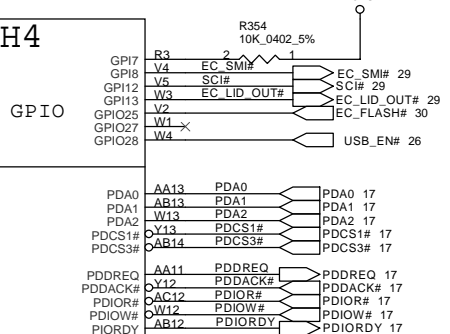
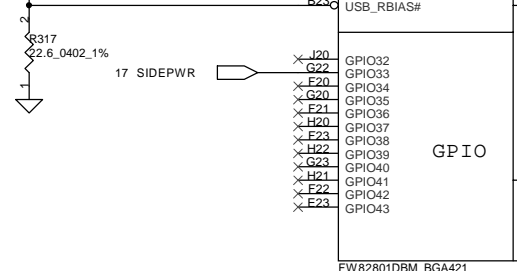
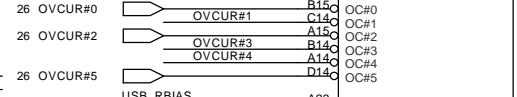
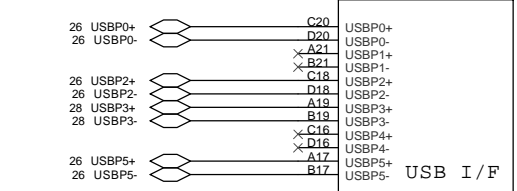
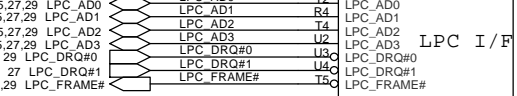
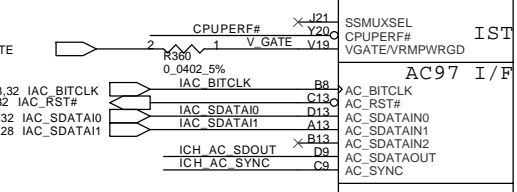
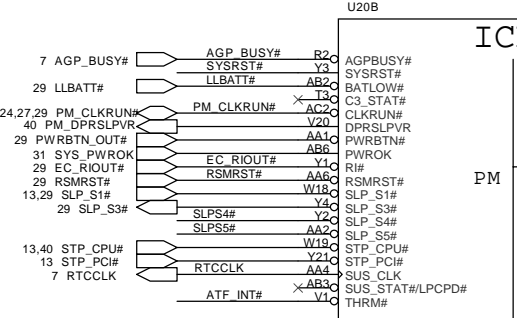
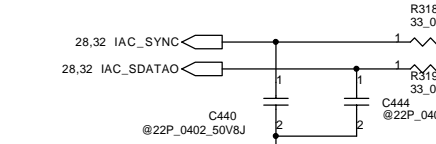
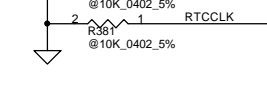
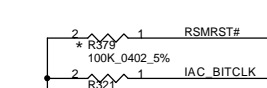
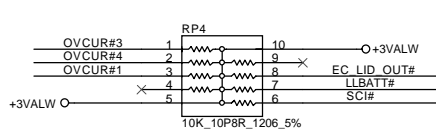
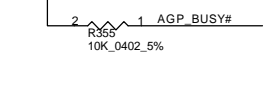
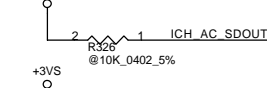
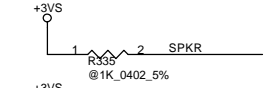
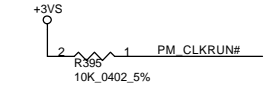
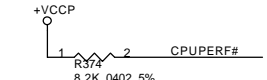
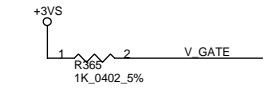
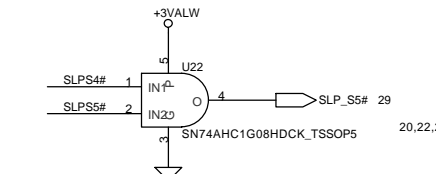


PCI Pullups

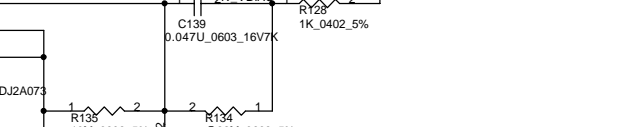
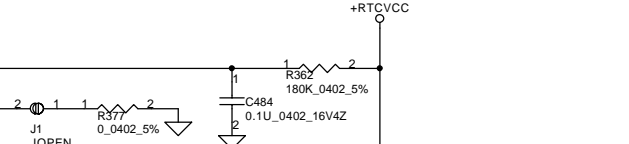
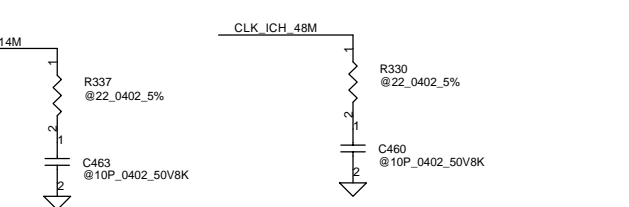
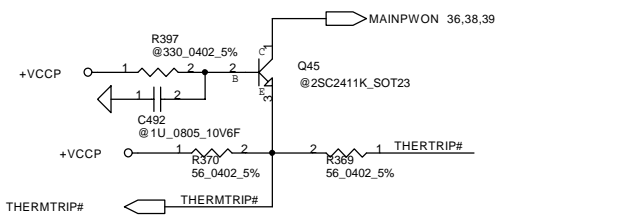
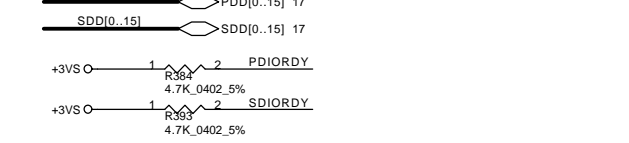
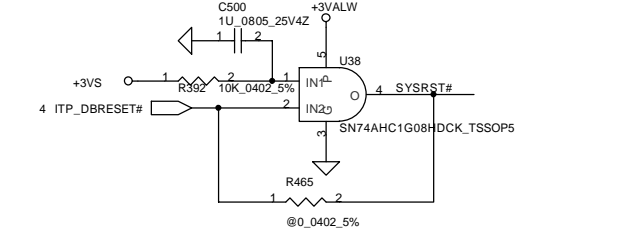
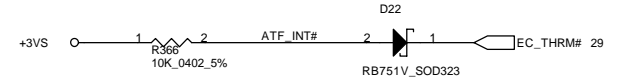


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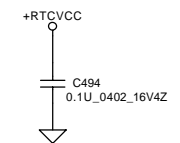
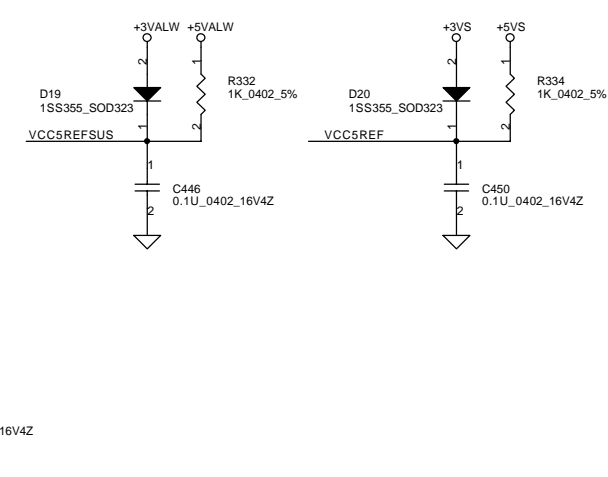
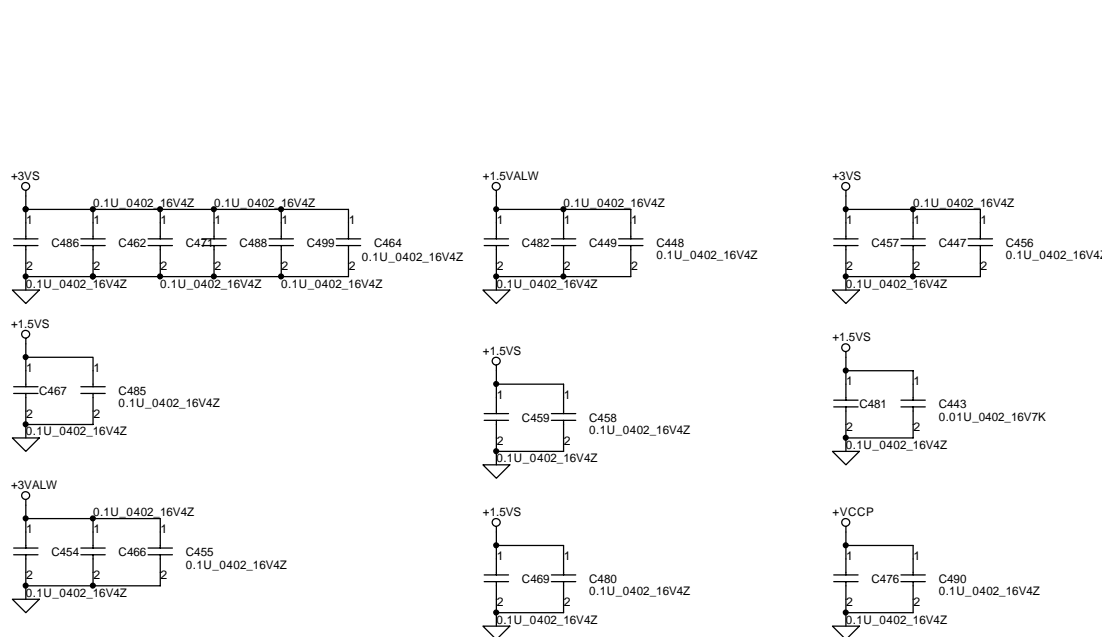
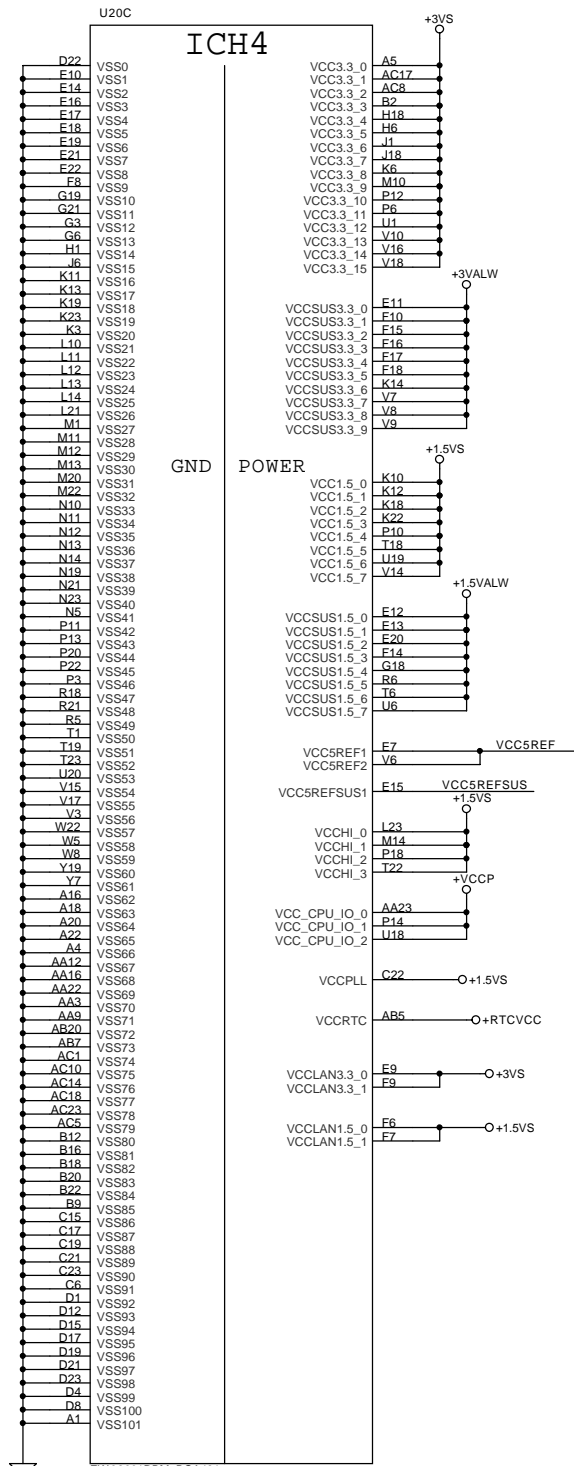


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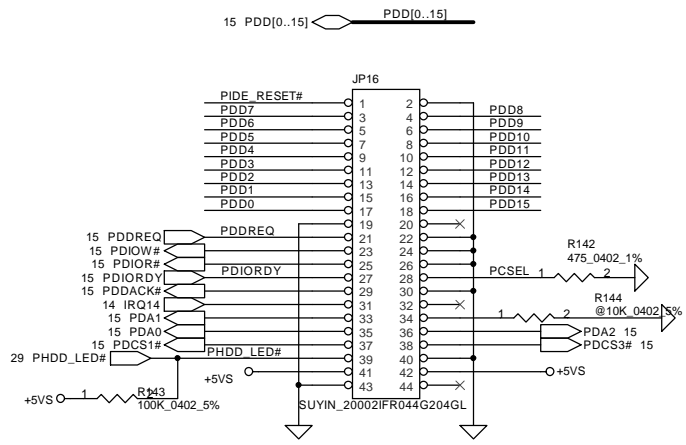


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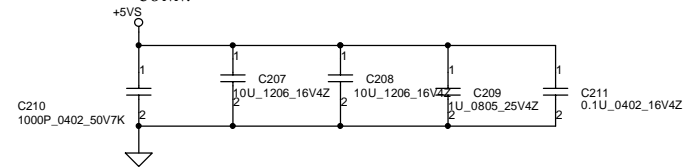
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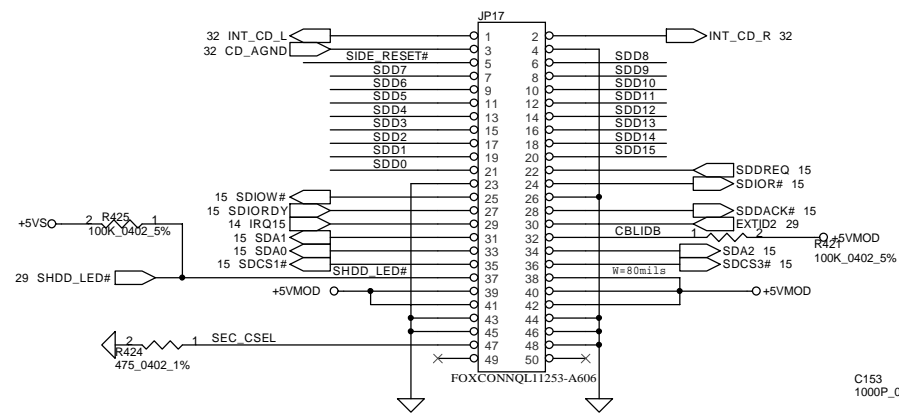
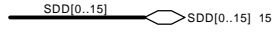
HDD Connector



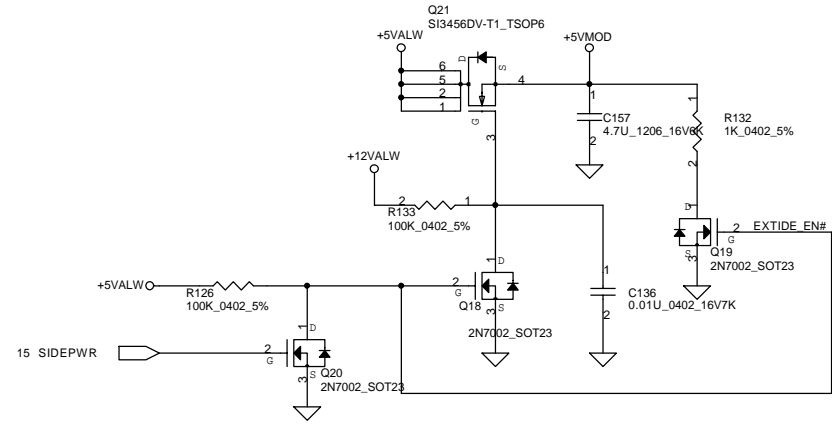
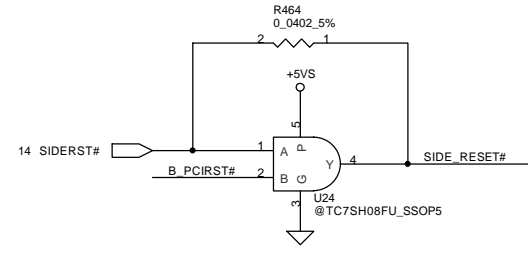
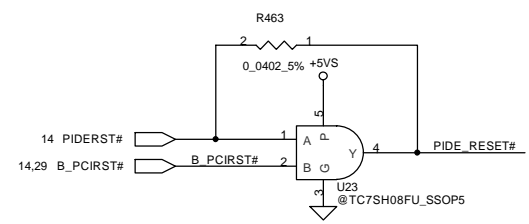
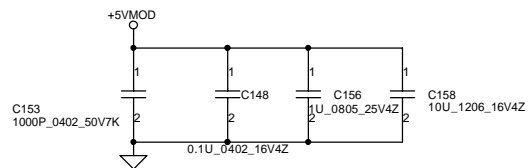
Placea caps. near HDD CONN.



CD-ROM Connector



Placea caps. near CDROM CONN.



SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

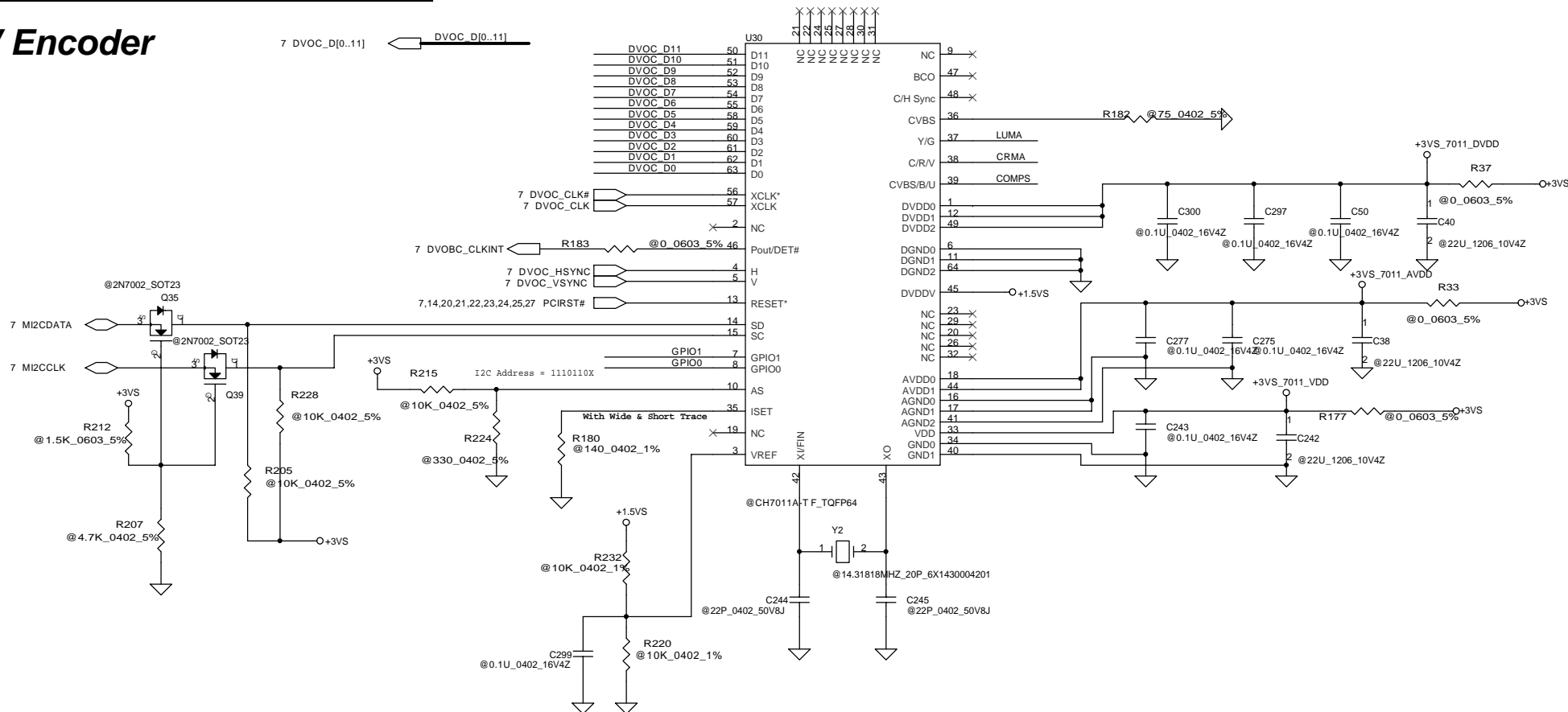
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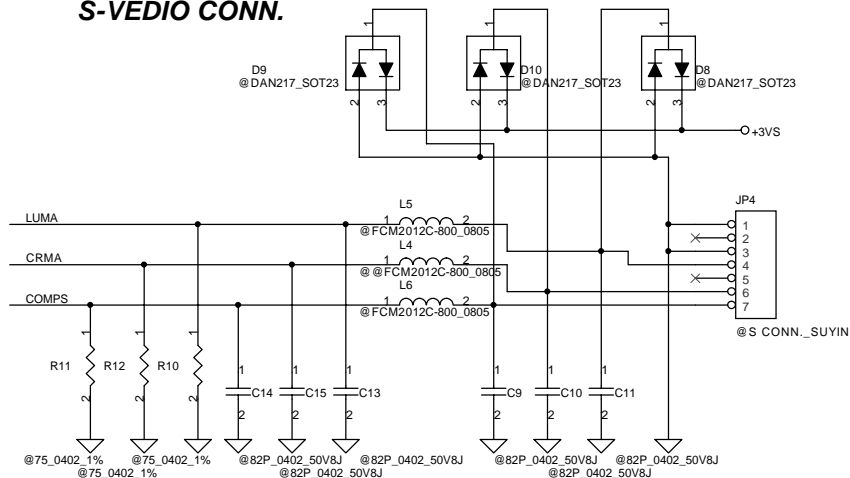
For ABO without TV_out:all this page component unmount

TV Encoder

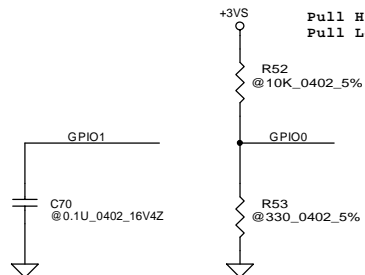
7 DVOC_D[0..11] ← DVOC_D[0..11]



S-VEDIO CONN.



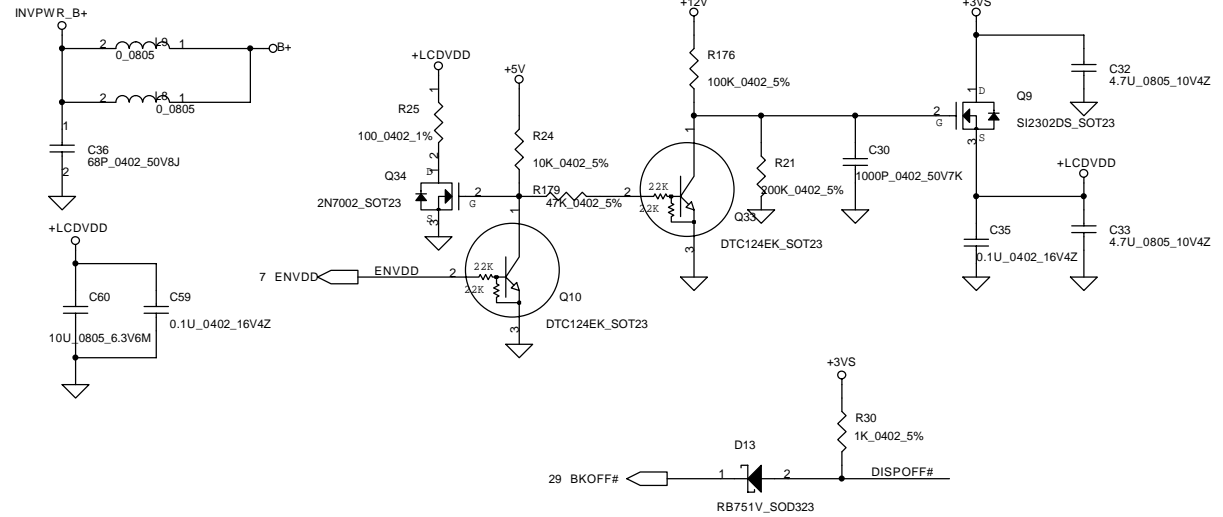
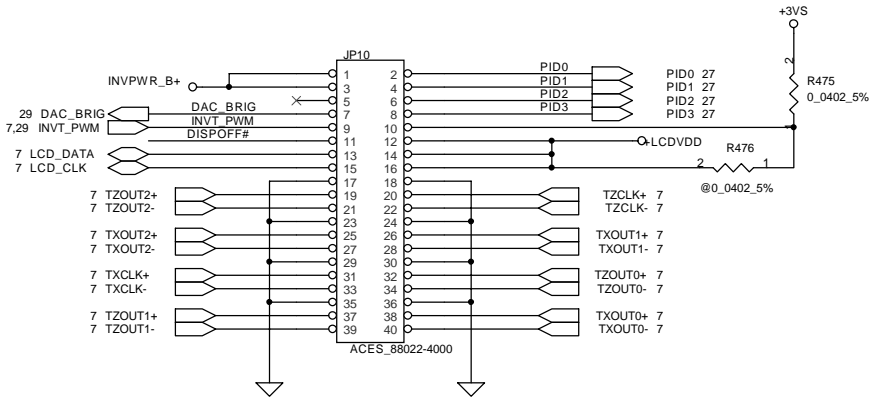
Pull High: Default PAL
Pull Low: Default NTSC



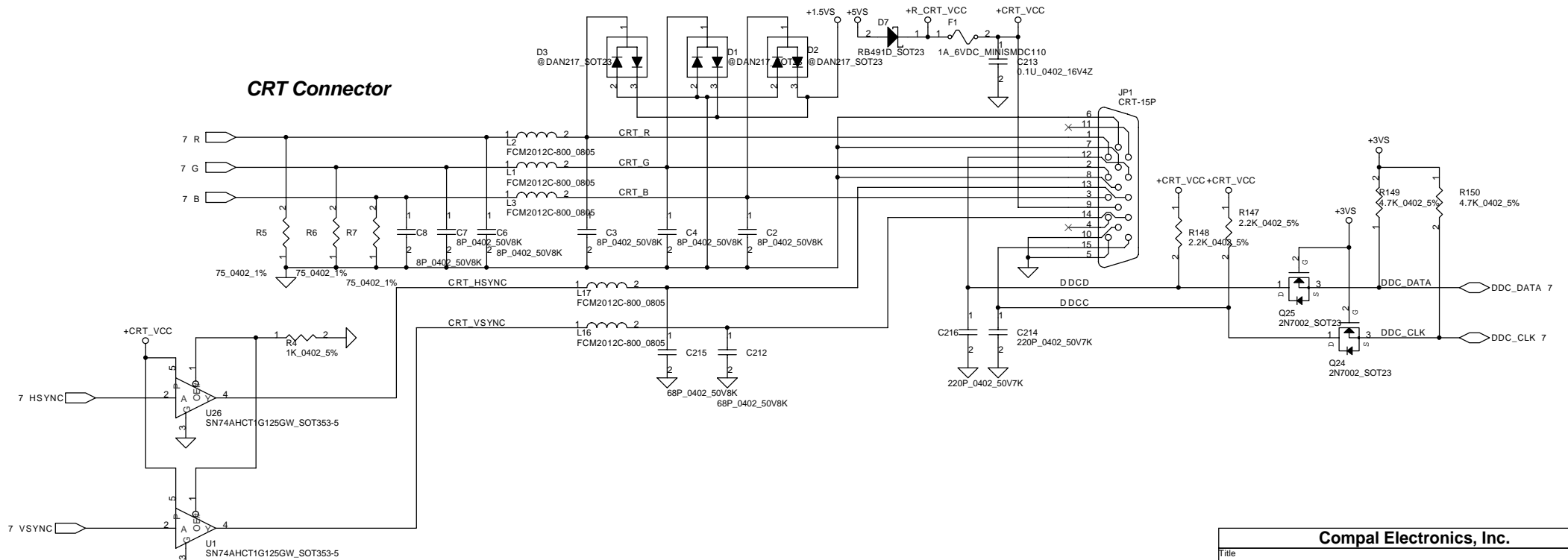
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LVDS Connector



CRT Connector



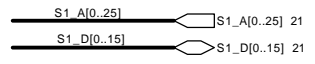
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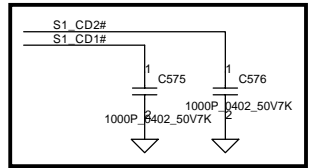
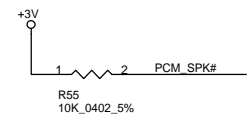
14,22,23,24 PCI_AD[0..31] PCI_AD[0..31]

PCI_AD31	3	AD31	CAD31/D10	144	S1 D10
PCI_AD30	4	AD30	CAD30/D9	142	S1 D9
PCI_AD29	5	AD29	CAD29/D1	141	S1 D1
PCI_AD28	7	AD28	CAD28/D8	140	S1 D8
PCI_AD27	8	AD27	CAD27/D0	139	S1 D0
PCI_AD26	9	AD26	CAD26/A0	129	S1 A0
PCI_AD25	11	AD25	CAD25/A1	128	S1 A1
PCI_AD24	10	AD24	CAD24/A2	127	S1 A2
PCI_AD23	15	AD24	CAD24/A2	124	S1 A3
PCI_AD22	16	AD23	CAD23/A3	121	S1 A4
PCI_AD21	17	AD21	CAD22/A4	120	S1 A5
PCI_AD20	19	AD20	CAD21/A5	120	S1 A5
PCI_AD19	23	AD19	CAD20/A6	118	S1 A6
PCI_AD18	25	AD19	CAD19/A25	116	S1 A25
PCI_AD17	24	AD18	CAD18/A7	115	S1 A7
PCI_AD16	26	AD17	CAD17/A24	113	S1 A24
PCI_AD15	38	AD16	CAD16/A17	98	S1 A17
PCI_AD14	39	AD15	CAD15/IOVR#	96	S1 IOVR#
PCI_AD13	40	AD14	CAD14/A9	97	S1 A9
PCI_AD12	41	AD13	CAD13/IORD#	93	S1 IORD#
PCI_AD11	42	AD12	CAD12/A11	95	S1 A11
PCI_AD10	43	AD11	CAD11/OE#	92	S1 OE#
PCI_AD9	46	AD10	CAD10/CE2#	94	S1 CE2#
PCI_AD8	47	AD9	CAD9/A10	89	S1 A10
PCI_AD7	49	AD8	CAD8/D15	87	S1 D15
PCI_AD6	51	AD7	CAD7/D7	85	S1 D7
PCI_AD5	52	AD6	CAD6/D13	82	S1 D13
PCI_AD4	53	AD5	CAD5/D6	83	S1 D6
PCI_AD3	54	AD4	CAD4/D12	80	S1 D12
PCI_AD2	55	AD3	CAD3/D5	81	S1 D5
PCI_AD1	56	AD2	CAD2/D11	77	S1 D11
PCI_AD0	57	AD1	CAD1/D4	79	S1 D4
		AD0	CAD0/D3	76	S1 D3

PQFP 144
22.2 X 22.2 X 1.60



14,22,23,24 PCI_C/BE#3	12	C/BE3#	CC/BE3#/REG#	125	S1 REG#
14,22,23,24 PCI_C/BE#2	27	C/BE2#	CC/BE2#/A12	112	S1 A12
14,22,23,24 PCI_C/BE#1	37	C/BE1#	CC/BE1#/A8	99	S1 A8
14,22,23,24 PCI_C/BE#0	48	C/BE0#	CC/BE0#/CE1#	88	S1 CE1#
7,14,18,21,22,23,24,25,27 PCIRST#	20	RST#	CRST#/RESET	119	S1 RST
14,22,23,24 PCI_FRAME#	28	FRAME#	CFRAME#/A23	111	S1 A23
14,22,23,24 PCI_IRDY#	29	IRDY#	CIRDY#/A15	110	S1 A15
14,22,23,24 PCI_TRDY#	31	TRDY#	CTRDY#/A22	109	S1 A22
14,22,23,24 PCI_DEVSEL#	32	DEVSEL#	CDEVSEL#/A21	107	S1 A21
14,22,23,24 PCI_STOP#	33	STOP#	CSTOP#/A20	105	S1 A20
14,22,23,24 PCI_PERR#	34	PERR#	CPERR#/A14	104	S1 A14
14,22,24 PCI_SERR#	35	SERR#	CSERR#/WAIT#	133	S1 WAIT#
14,22,23,24 PCI_PAR	36	PAR	CPAR/A13	101	S1 A13
14 PCI_REQ#2	1	REQ#	CREQ#/INPACK#	106	S1 INPACK#
14 PCI_GNT#2	2	GNT#	CGNT#/WE#	108	S1 WE#
13 CLK_PCI_PCM	21	CLK	CCLK/A16	108	A16 CLK
29,30,34,39,42 SUSP#	58	RI_OUT#/PME#	CSTSCHG/BVD1	135	S1 BVD1
	70	SUSPEND#	CLKRUN#/WP	136	S1 WP
PCI_AD20	13	IDSEL	CBLOCK#/A19	103	S1 A19
PCI_PIRQA#	60	MFUNC0	CINT#/READY	132	S1 RDY#
	61	MFUNC1	SPKOUT	62	PCM_SPK#
29 PCM_RI#	64	MFUNC2	CAUDIO/BVD2	134	S1 BVD2
14,25,27,29 SIRQ	65	MFUNC3			
	67	MFUNC4			
15,22,24,27,29 PM_CLKRUN#	68	MFUNC5			
	69	MFUNC6			
21 CBRST#	66	VCC/GRST#			



Reserve for CB1410 B0 Version

Compal Electronics, Inc.

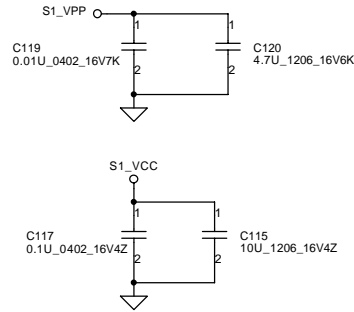
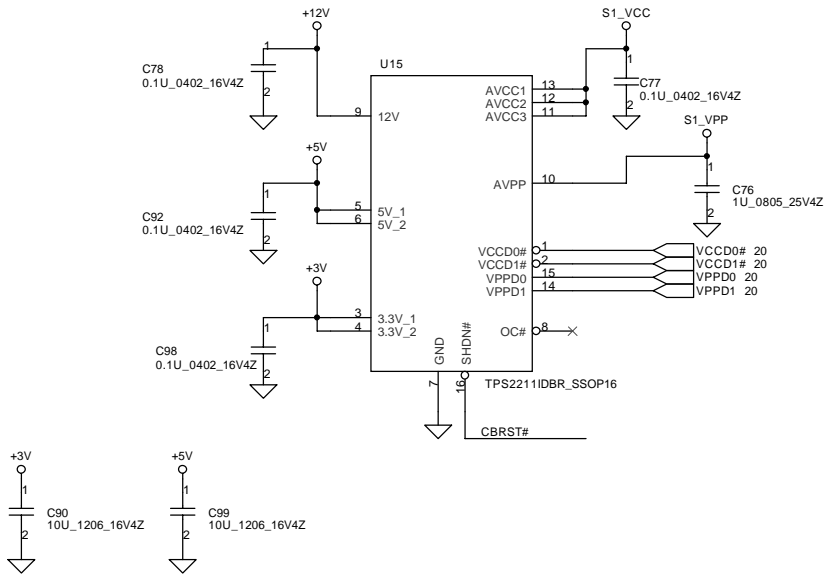
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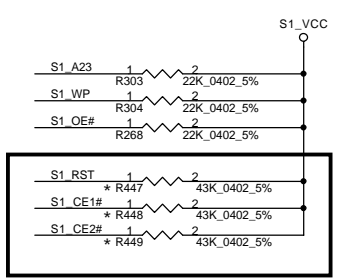
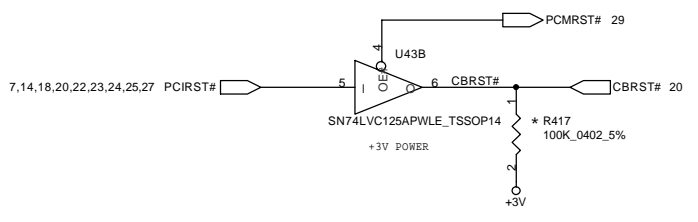
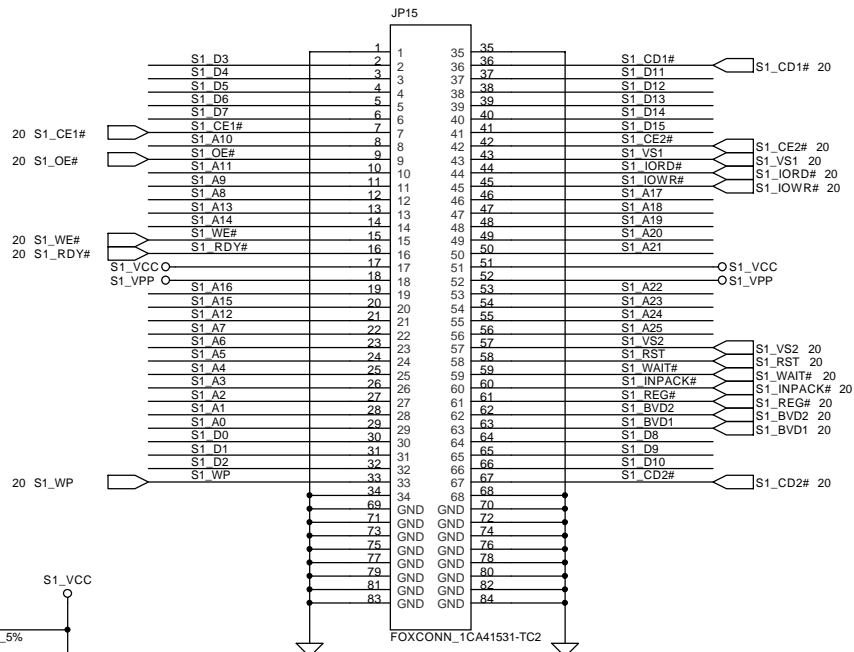
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PCMCIA Power Controller



CardBus Socket



Reserve for CB1410 B0 Version

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14,20,23,24 PCI_AD[0..31]

PCI AD0	47	AD0
PCI AD1	46	AD1
PCI AD2	45	AD2
PCI AD3	43	AD3
PCI AD4	42	AD4
PCI AD5	41	AD5
PCI AD6	40	AD6
PCI AD7	39	AD7
PCI AD8	36	AD8
PCI AD9	35	AD9
PCI AD10	34	AD10
PCI AD11	33	AD11
PCI AD12	32	AD12
PCI AD13	30	AD13
PCI AD14	29	AD14
PCI AD15	28	AD15
PCI AD16	15	AD16
PCI AD17	14	AD17
PCI AD18	13	AD18
PCI AD19	12	AD19
PCI AD20	11	AD19
PCI AD21	10	AD20
PCI AD22	9	AD21
PCI AD23	8	AD22
PCI AD24	96	AD23
PCI AD25	93	AD24
PCI AD26	92	AD25
PCI AD27	91	AD26
PCI AD28	89	AD27
PCI AD29	87	AD28
PCI AD30	86	AD29
PCI AD31	85	AD30

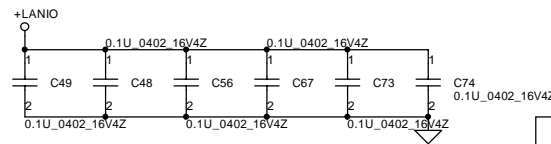
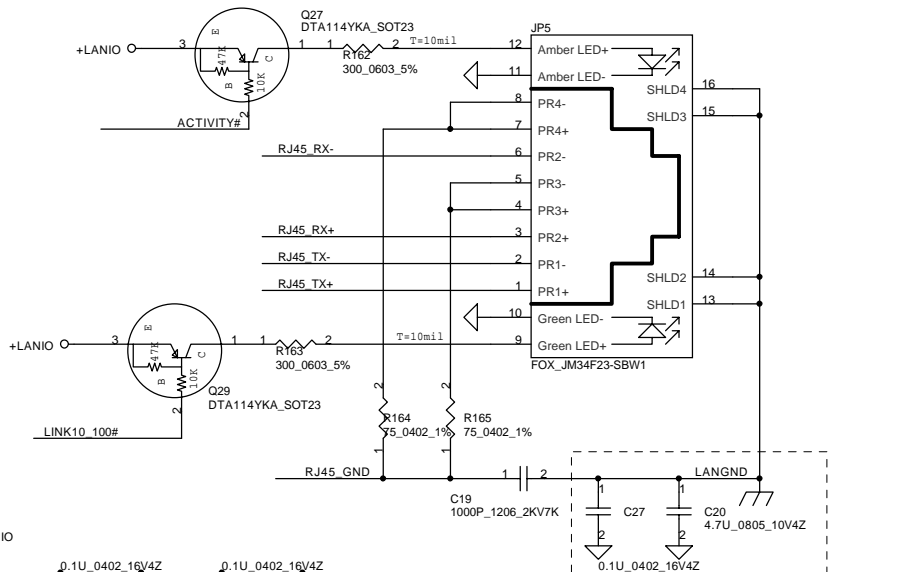
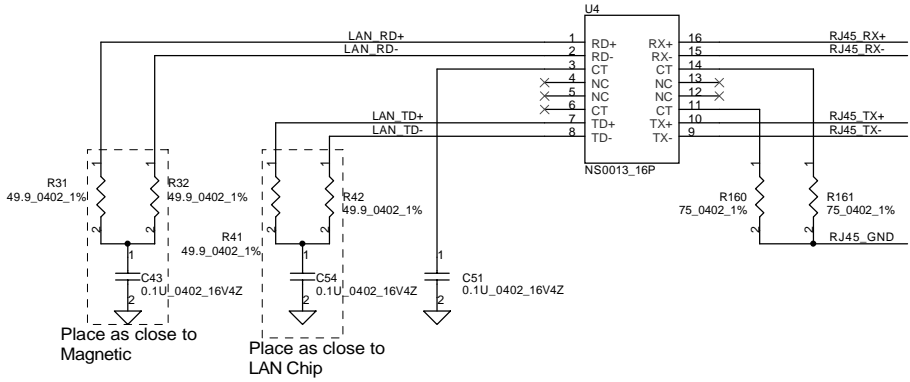
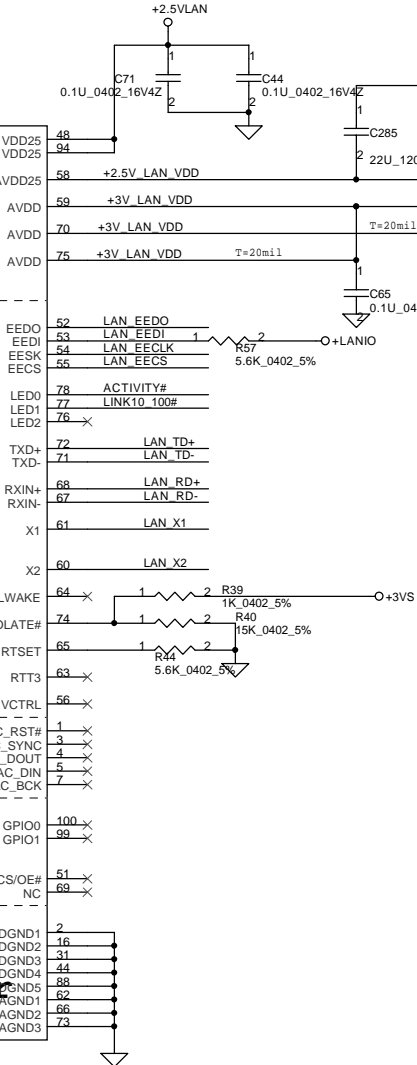
Power

PCI I/F

LAN I/F

AC-Link

Power



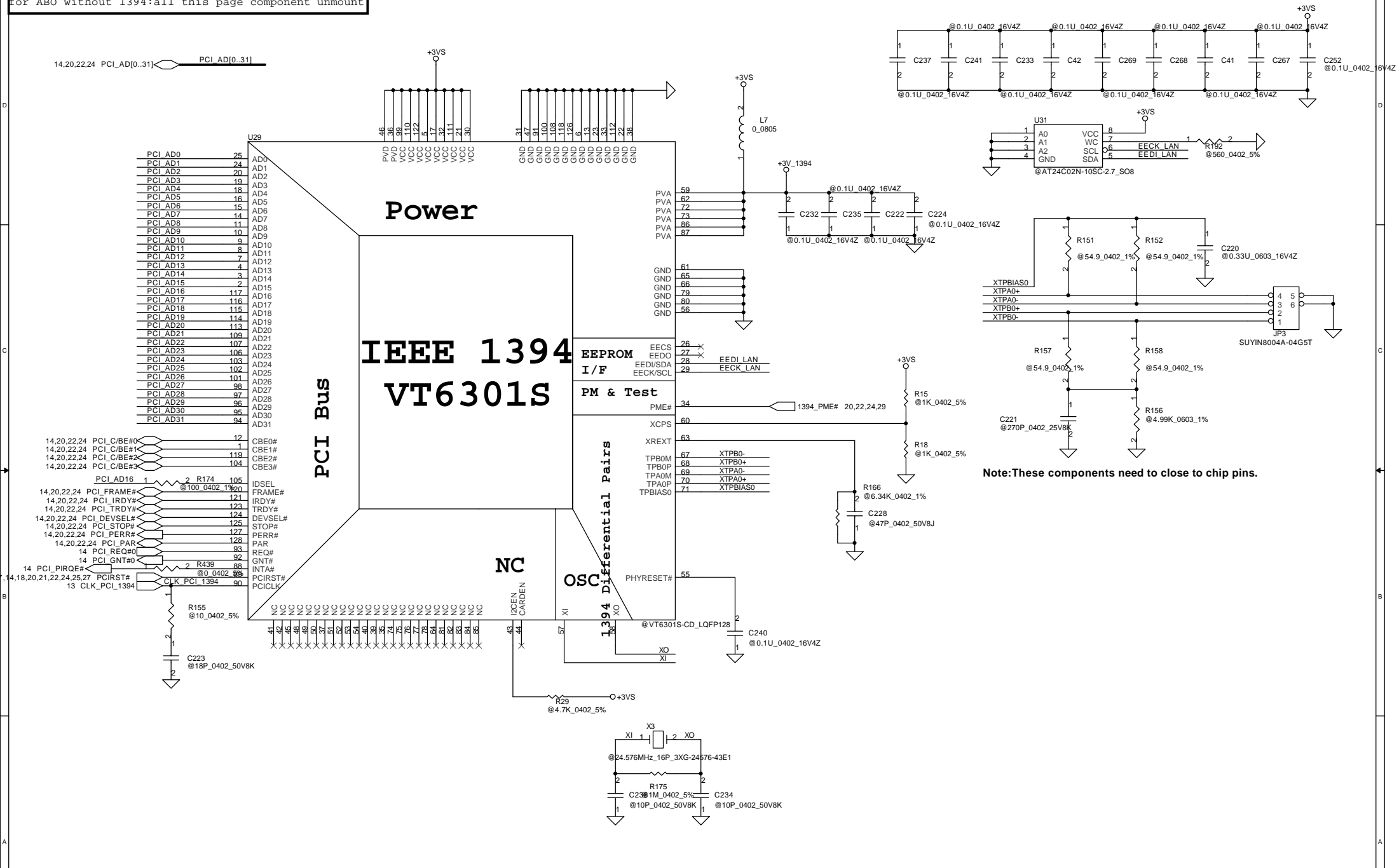
Termination plane should be copied to chassis ground and also depends on safety concern

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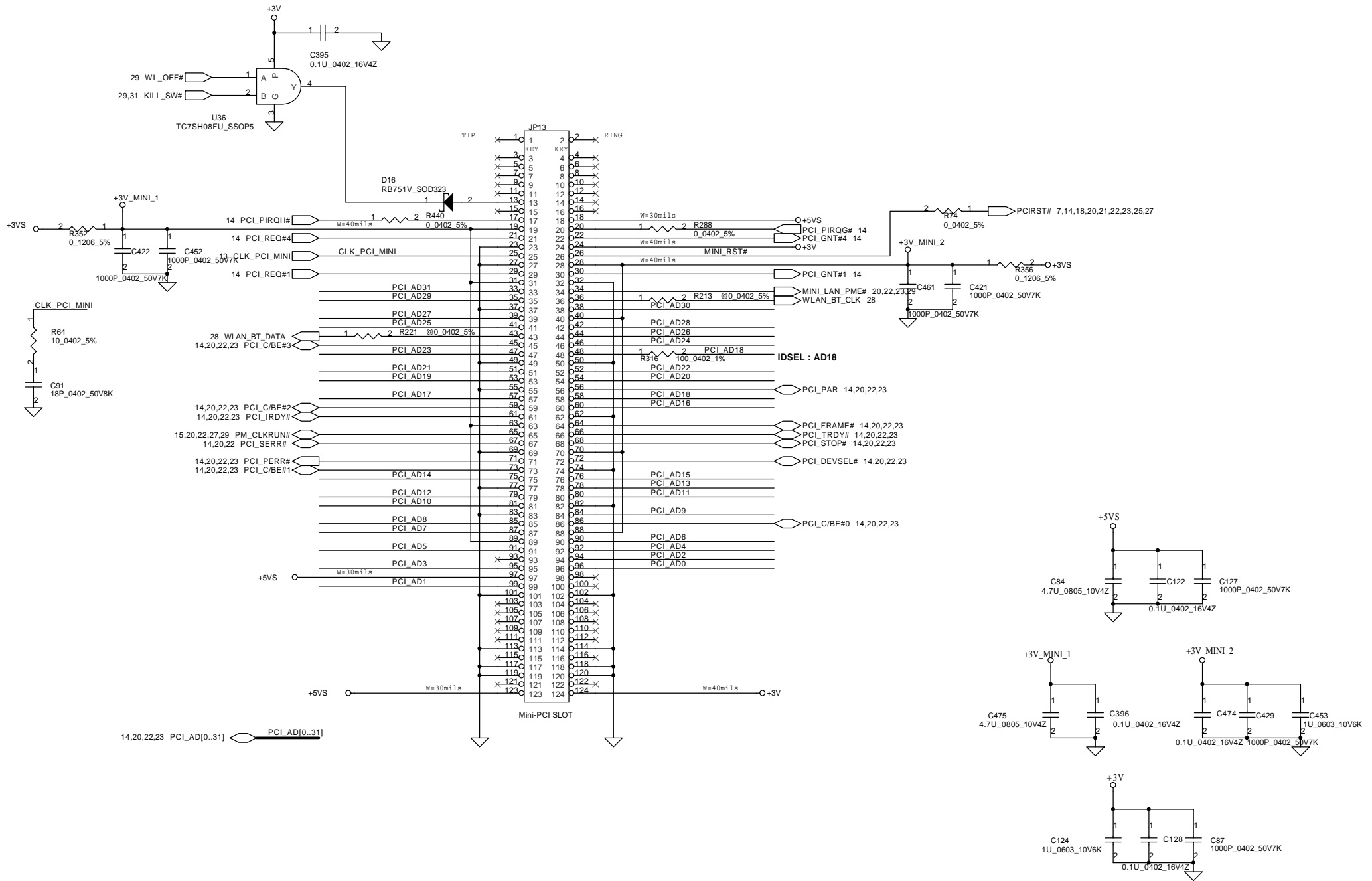
For ABO without 1394:all this page component unmount



Note: These components need to close to chip pins.

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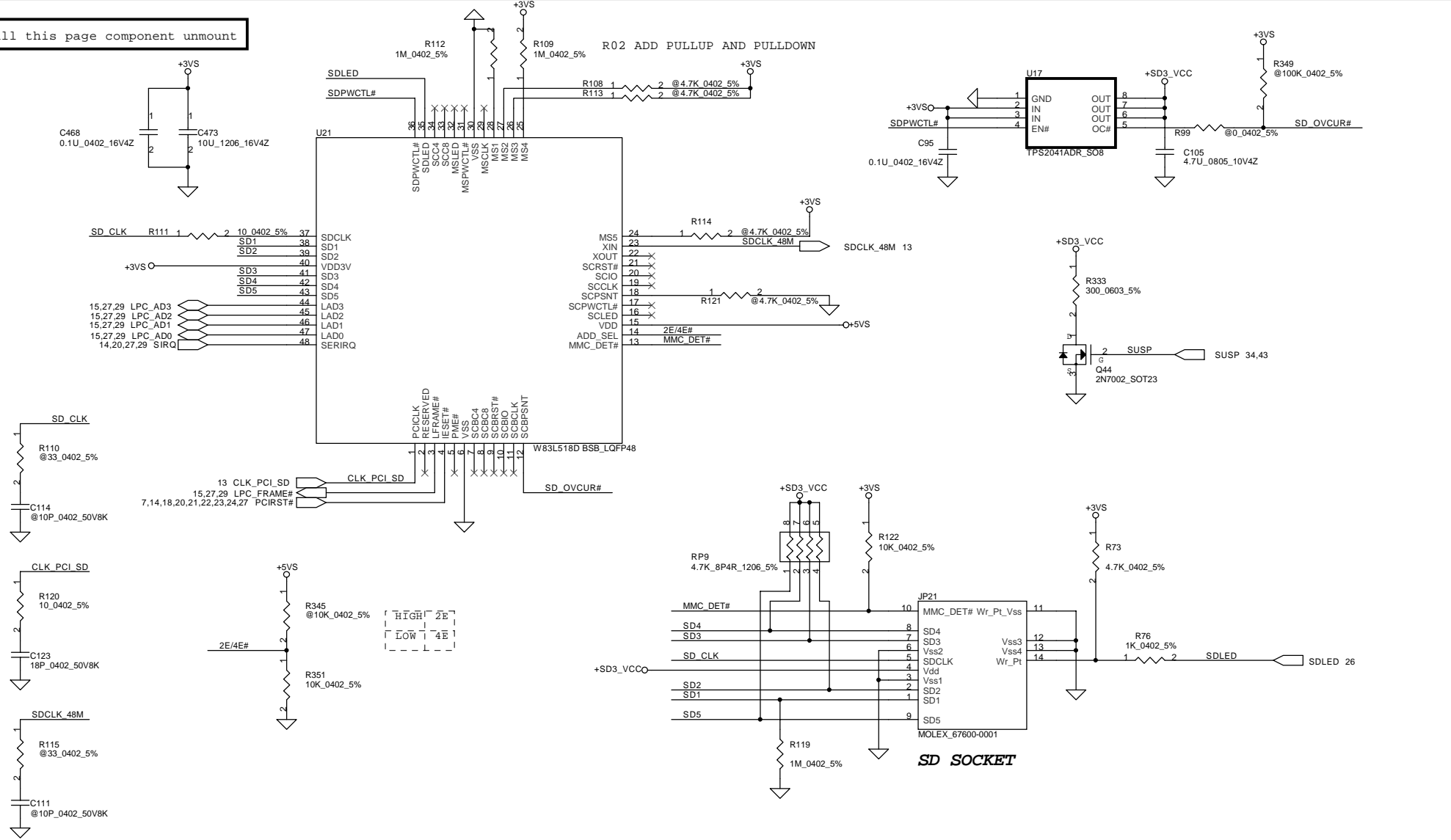
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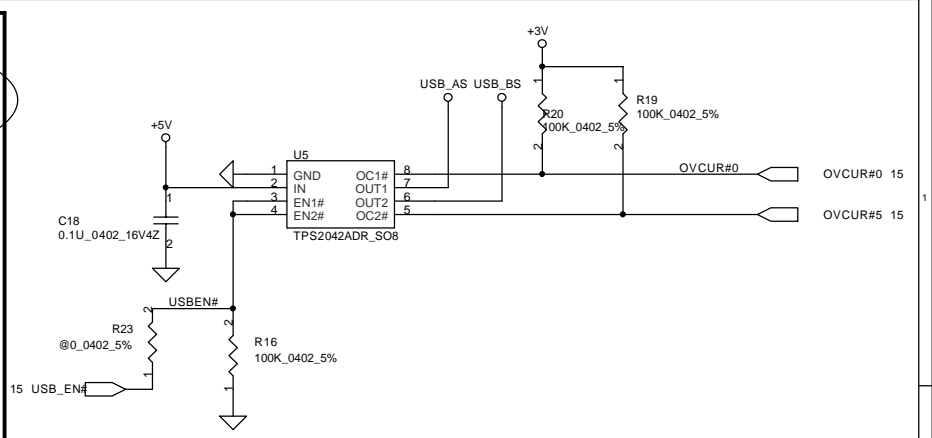
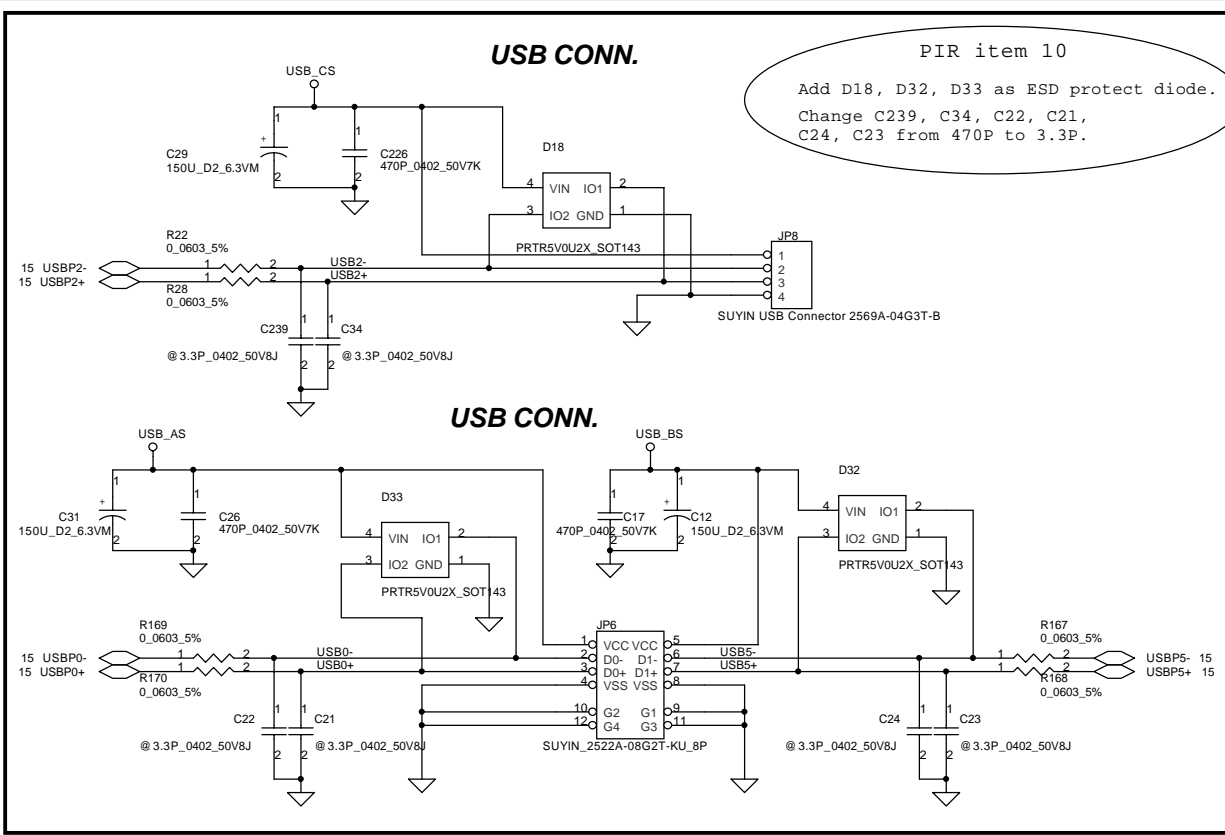
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FOR ABO: all this page component unmount

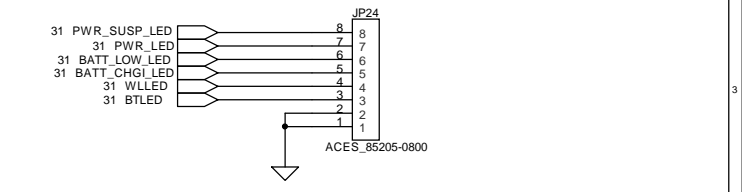
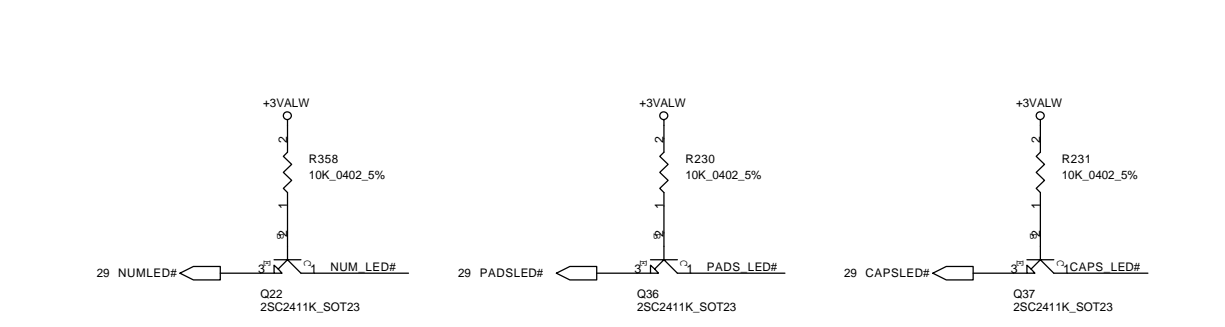
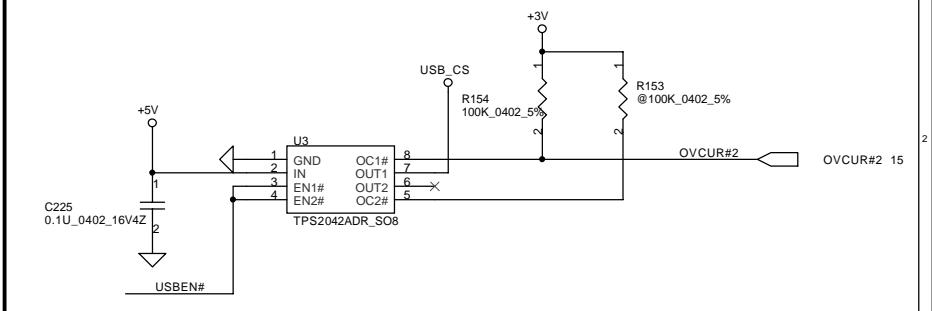


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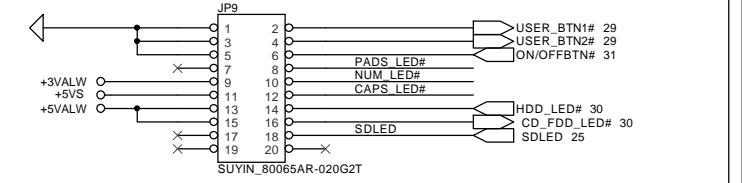
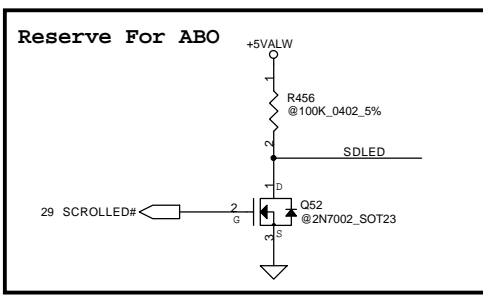
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LED/B CONN.



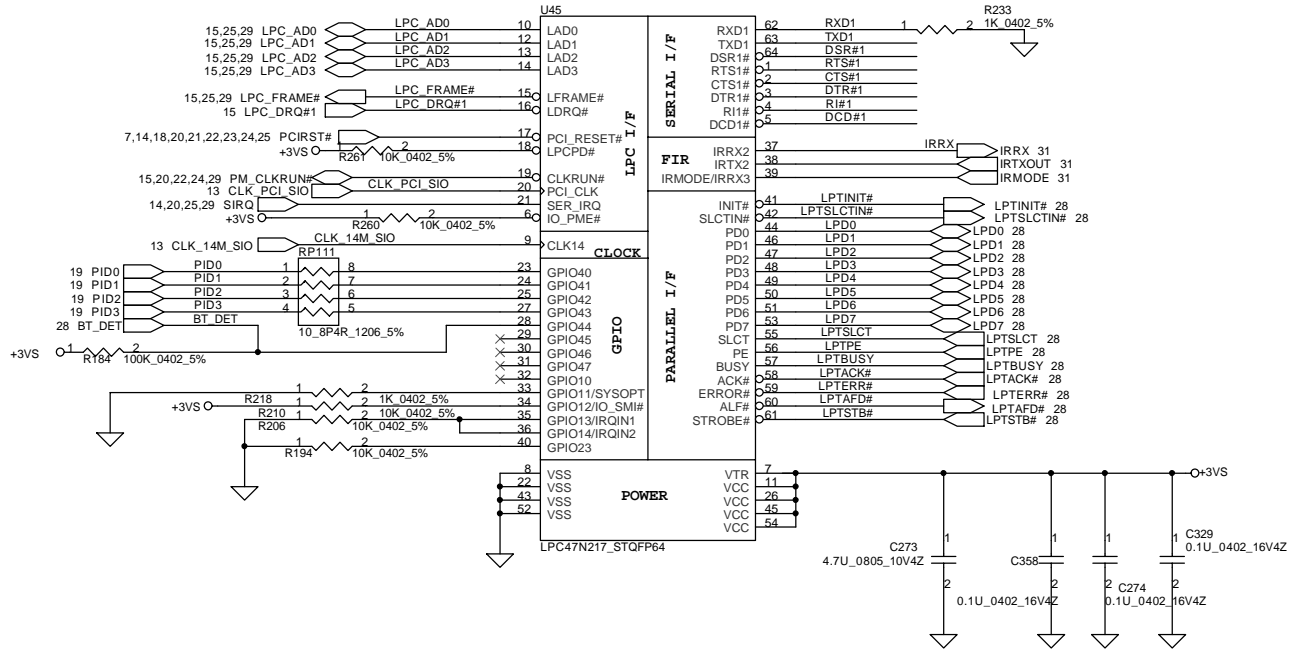
POWER/B CONN.



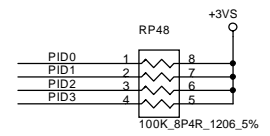
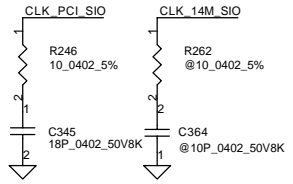
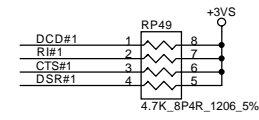
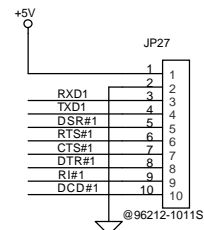
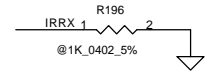
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SUPER I/O SMC FDC47N227



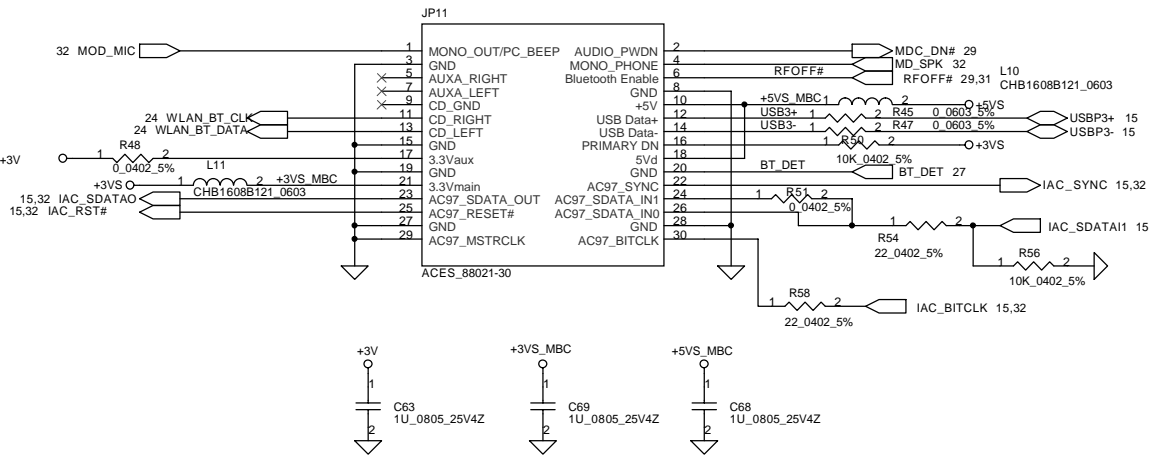
Base I/O Address
 * 0 = 02Eh
 1 = 04Eh



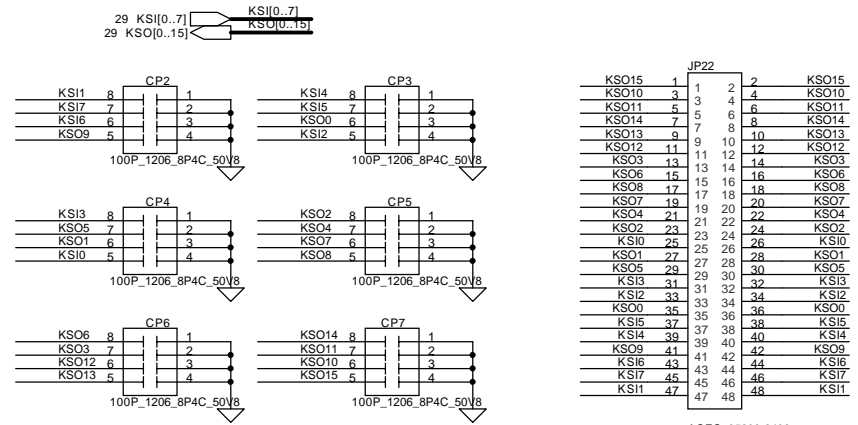
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MBC CONN.

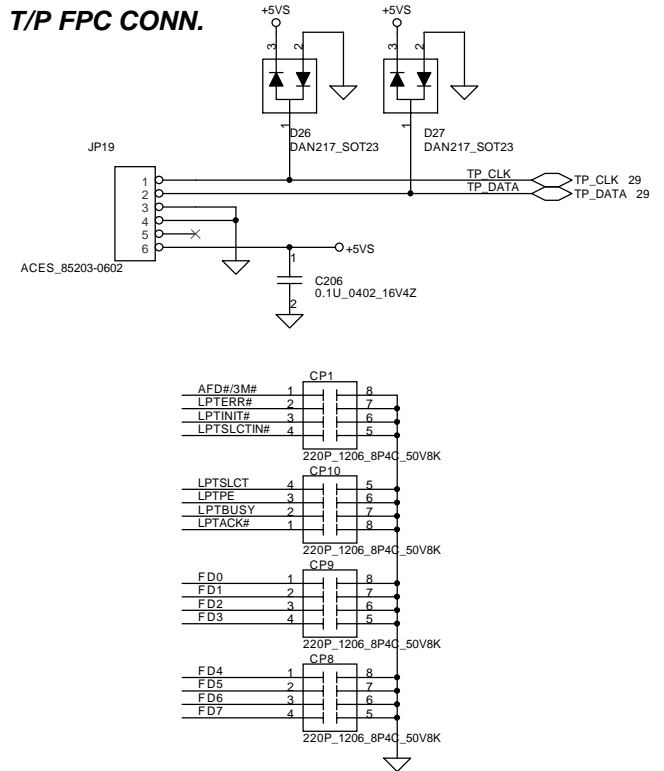


INT_KBD CONN.

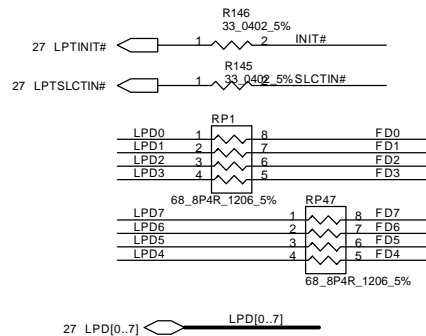
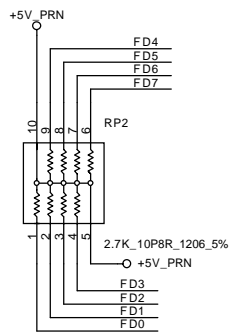
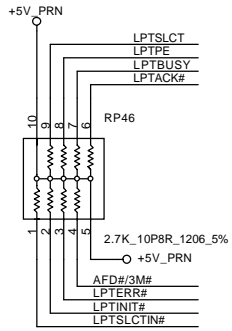
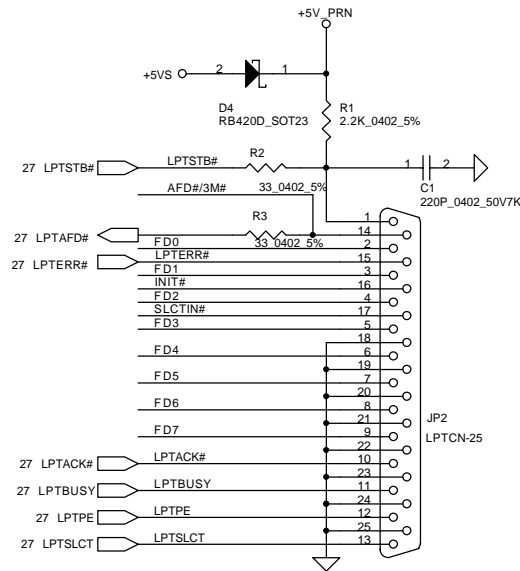


As close as possible to K/B connector

T/P FPC CONN.



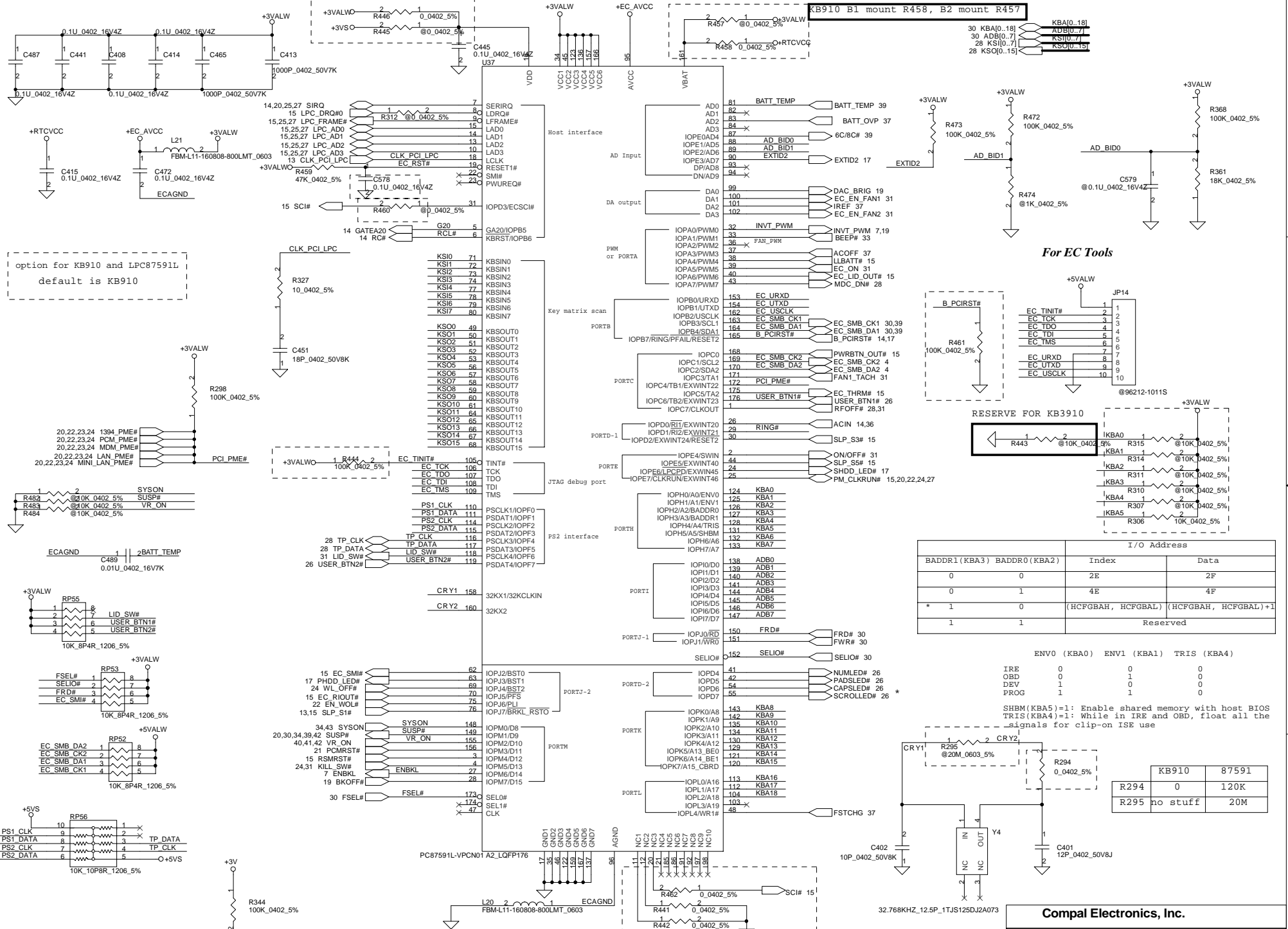
PARALLEL PORT



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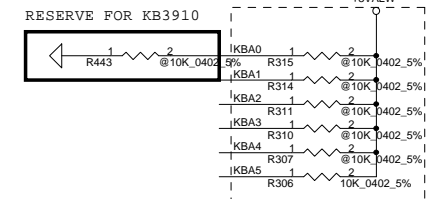
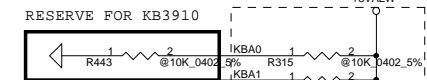
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option for KB910 and LPC87591L
default is KB910

For EC Tools



I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
1	1	Reserved	

ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE 0	NUMLED# 26	0
OBD 0	PADSLED# 26	1
DEV 1	CAPSLED# 26	0
PROG 1	SCROLLED# 26	1

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

	KB910	87591
R294	0	120K
R295	no stuff	20M

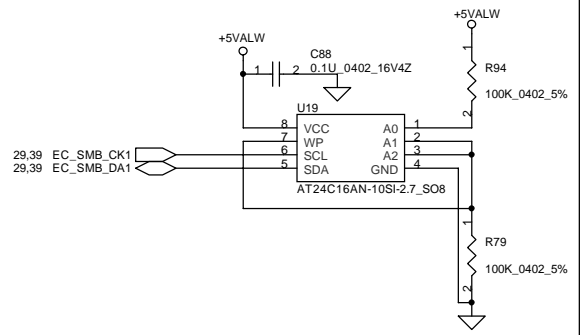
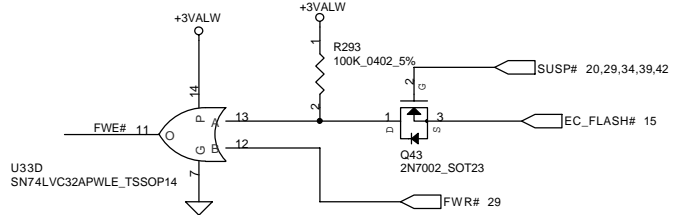
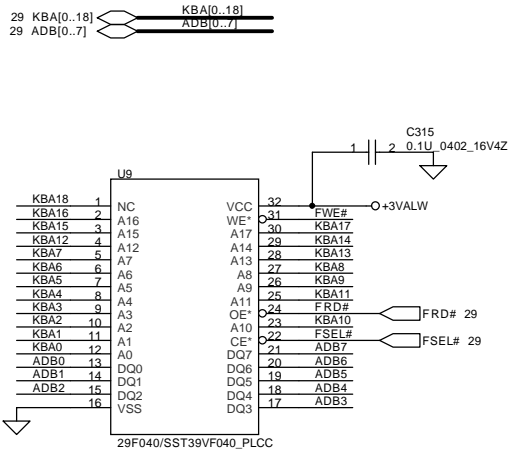
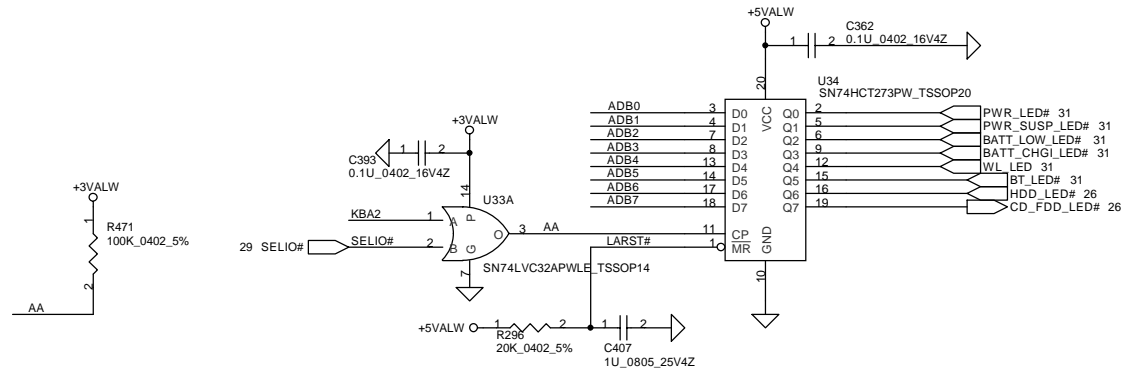
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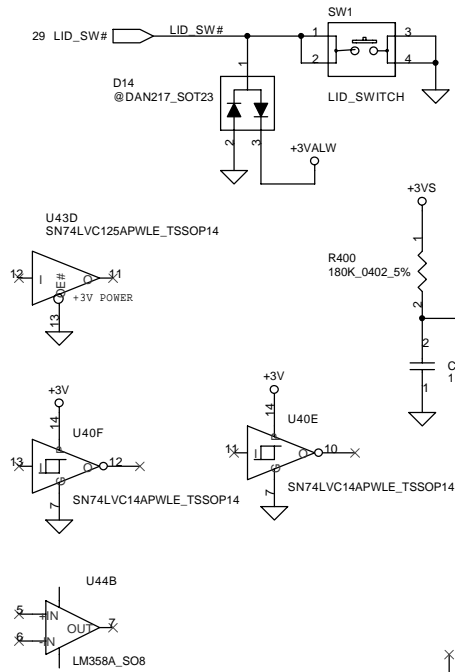
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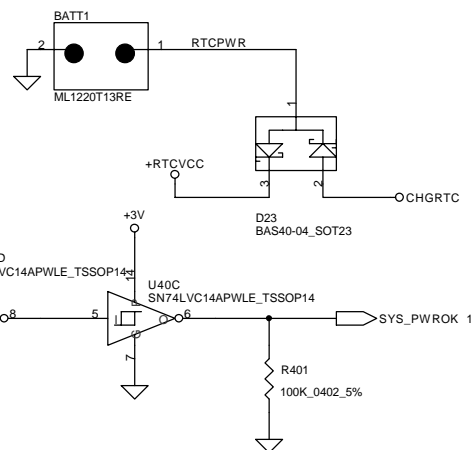
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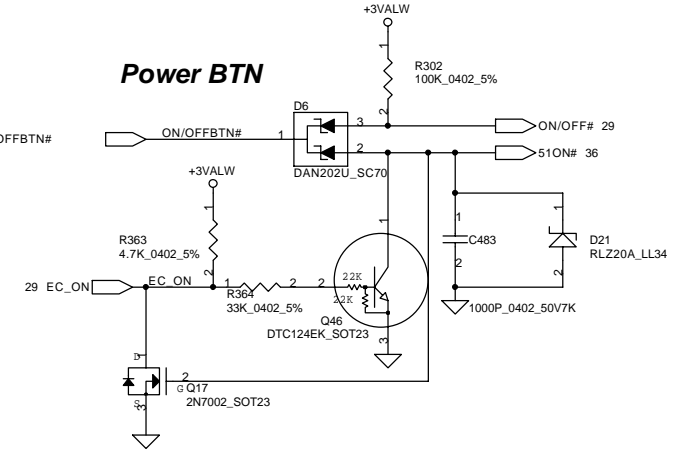
Power ON Circuit



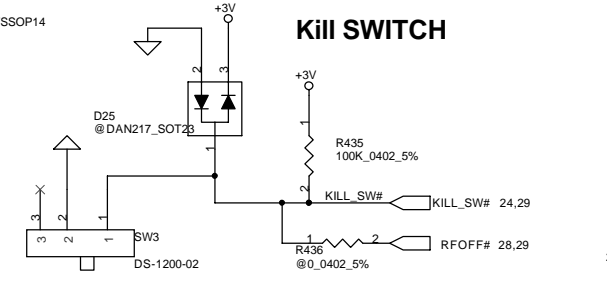
RTC Battery



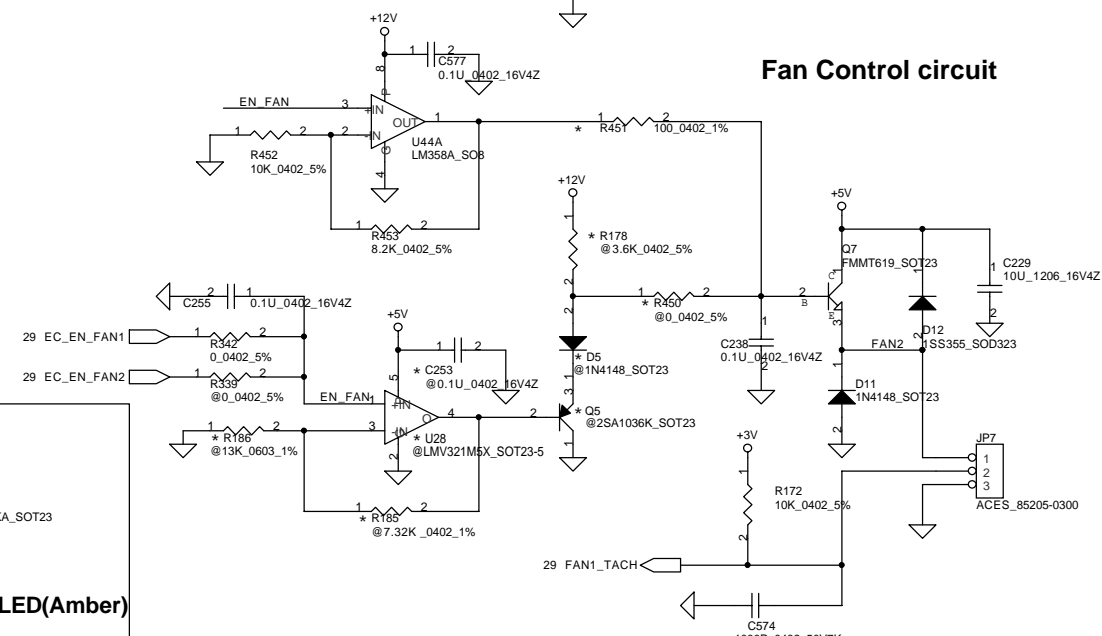
Power BTN



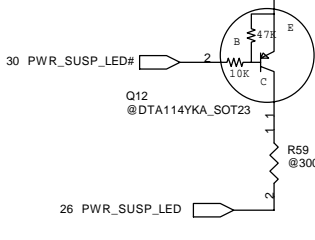
Kill SWITCH



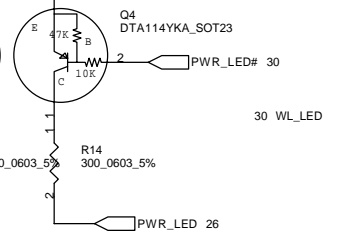
Fan Control circuit



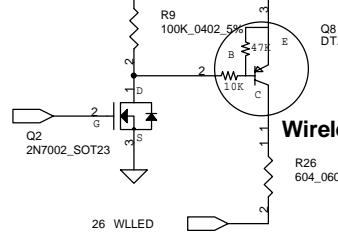
Suspend LED(Amber)



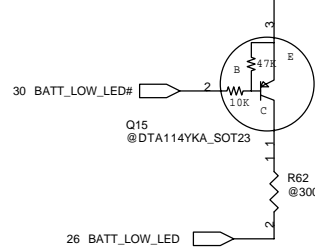
Power LED(Blue)



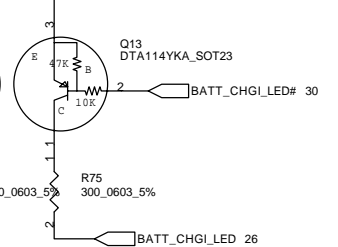
Wireless LED(Amber)



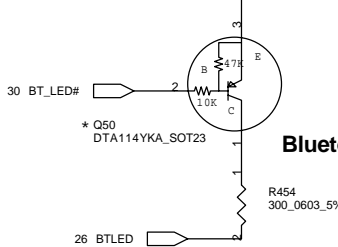
BATT Low LED(Amber)



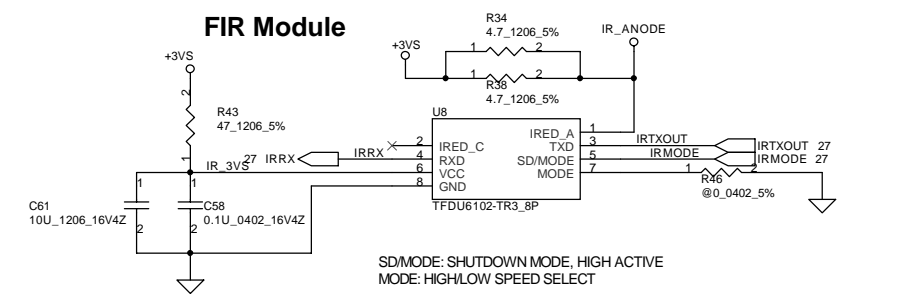
BATT Charge LED(Blue)



Bluetooth LED(Blue)



FIR Module

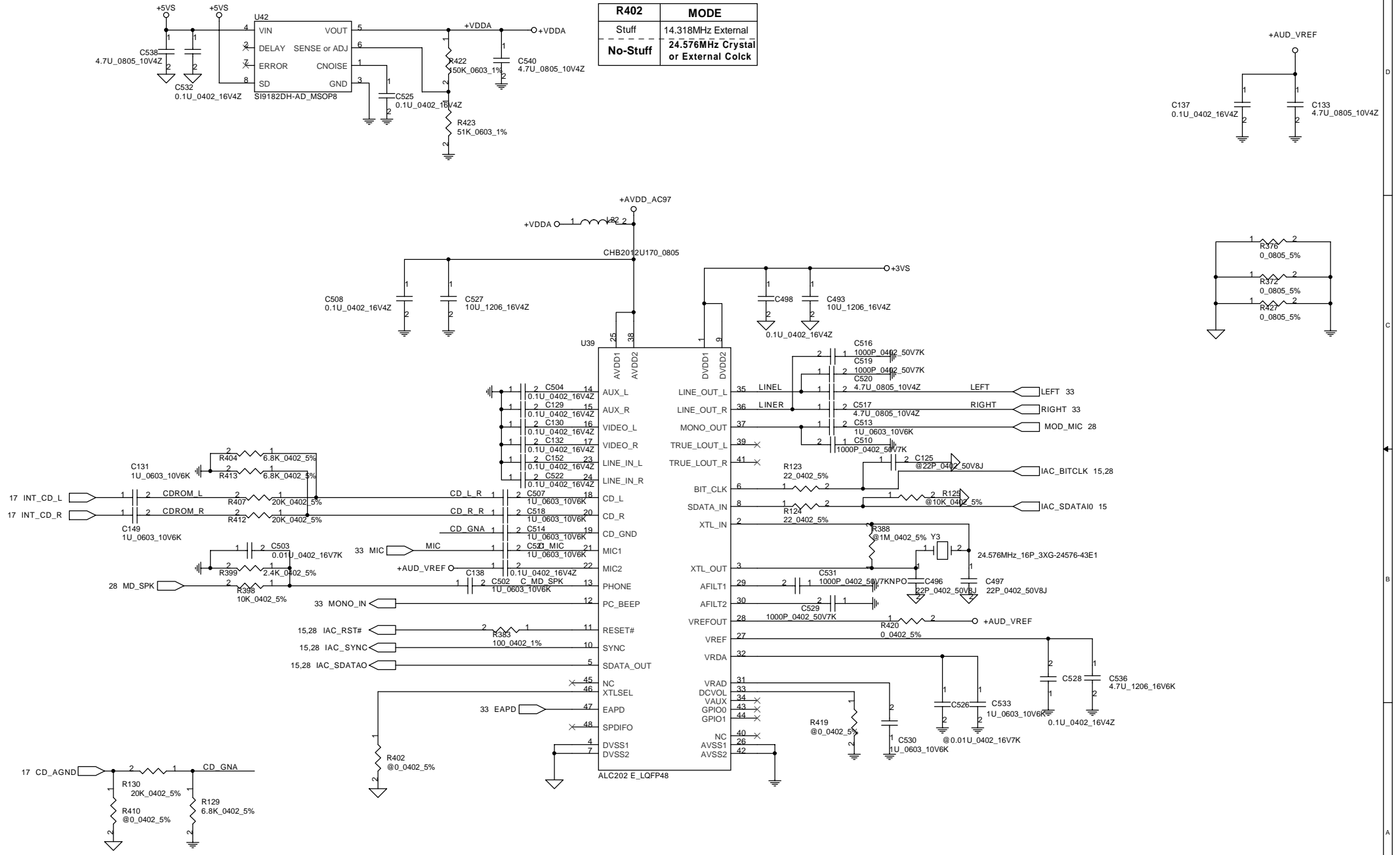


SD/MODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT

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AC97 Codec



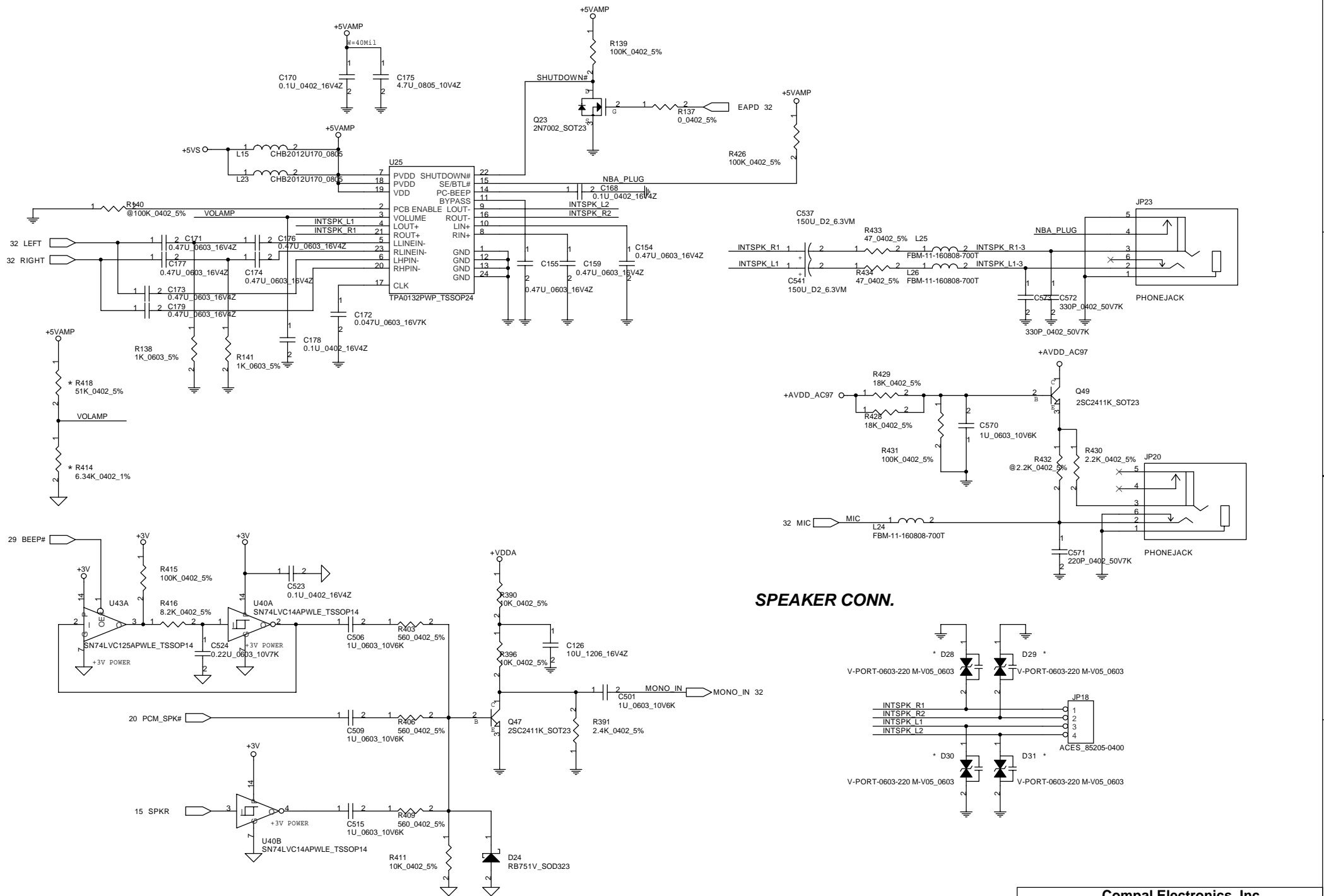
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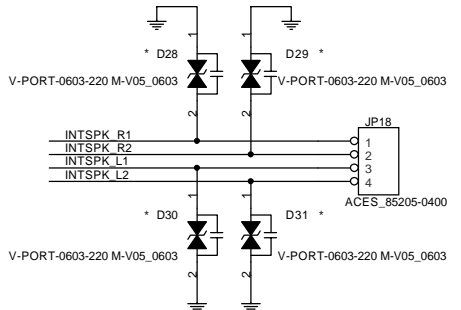
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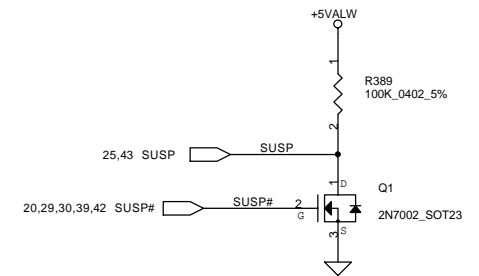
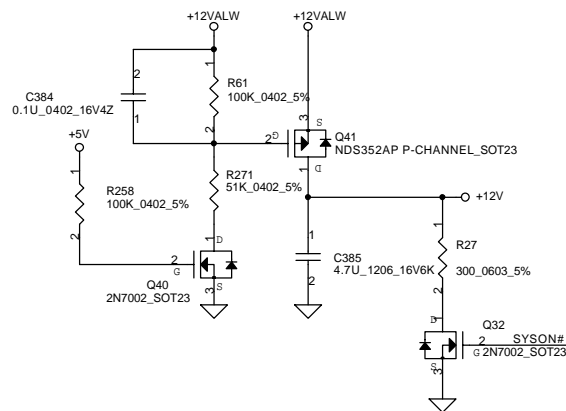
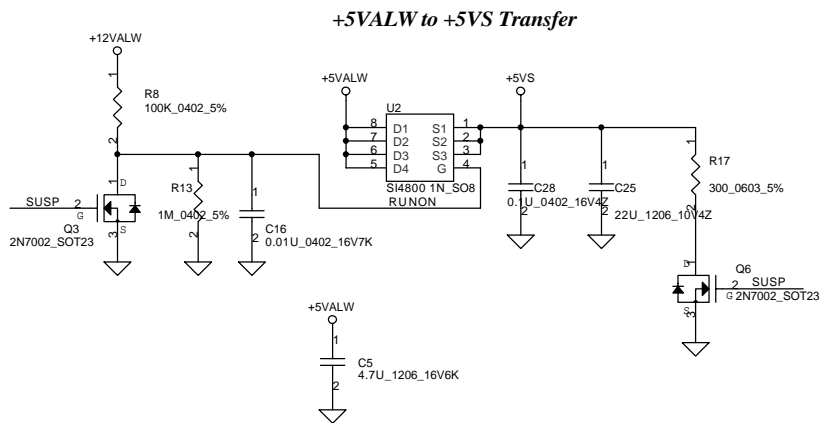
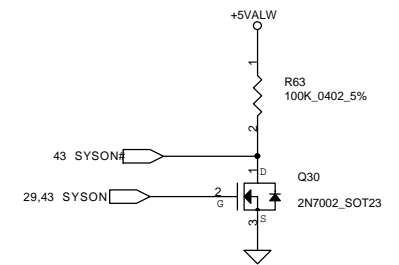
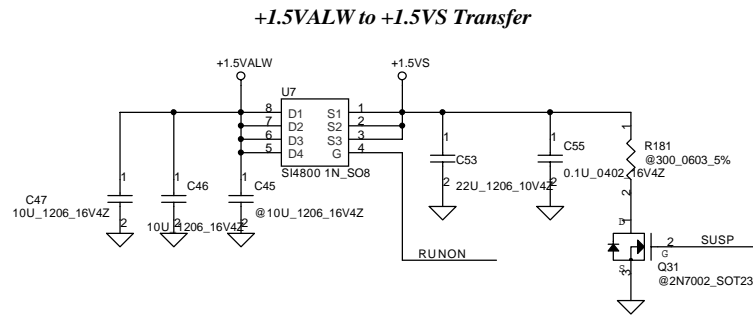
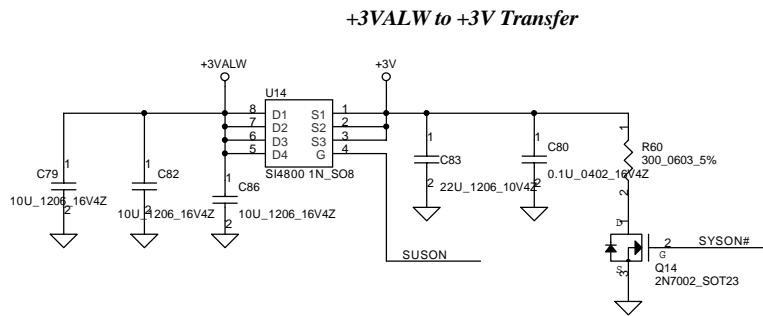
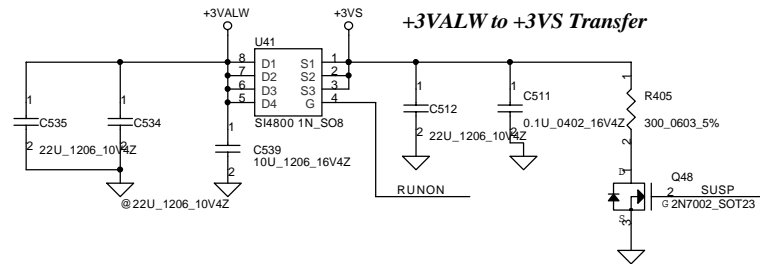
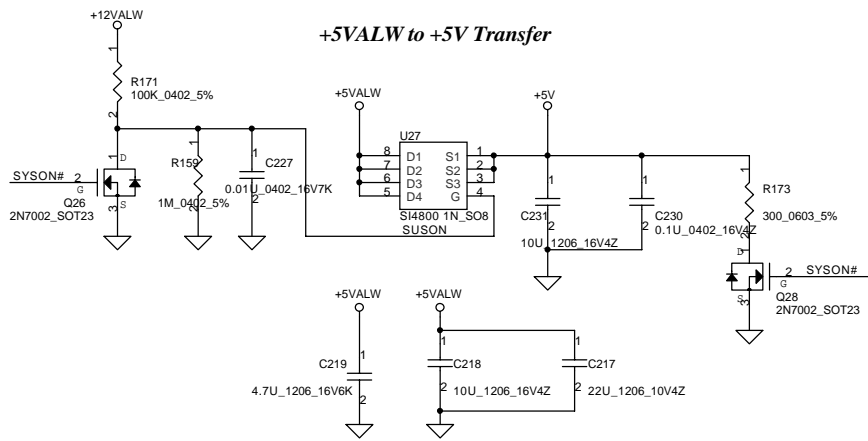


SPEAKER CONN.



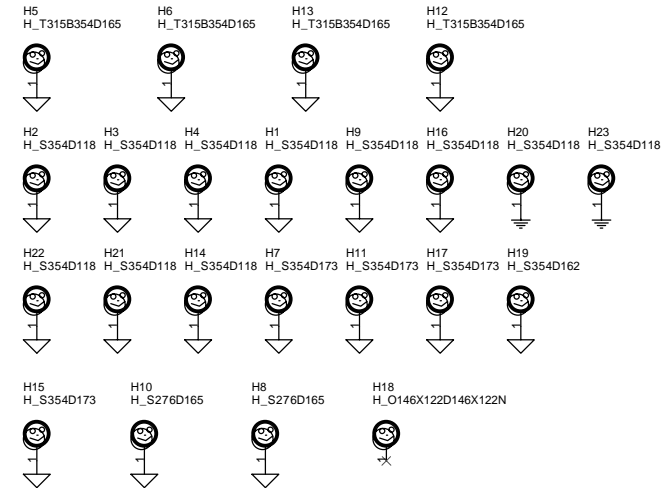
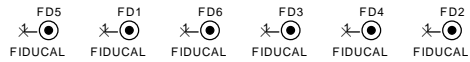
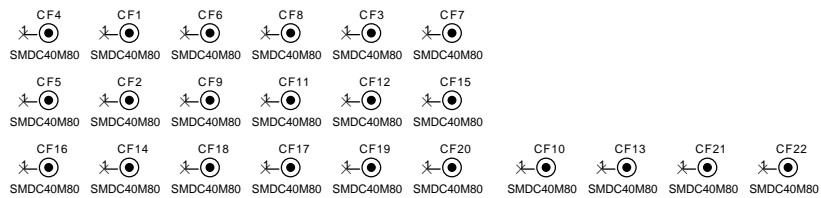
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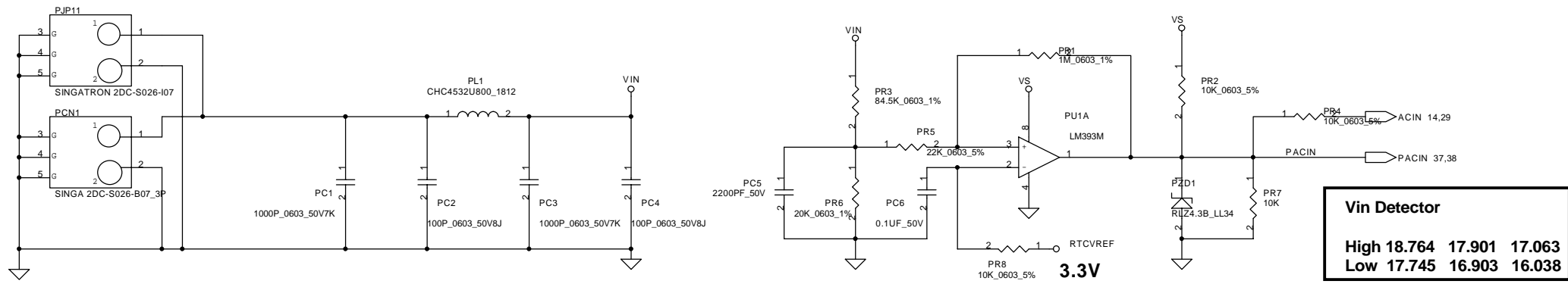
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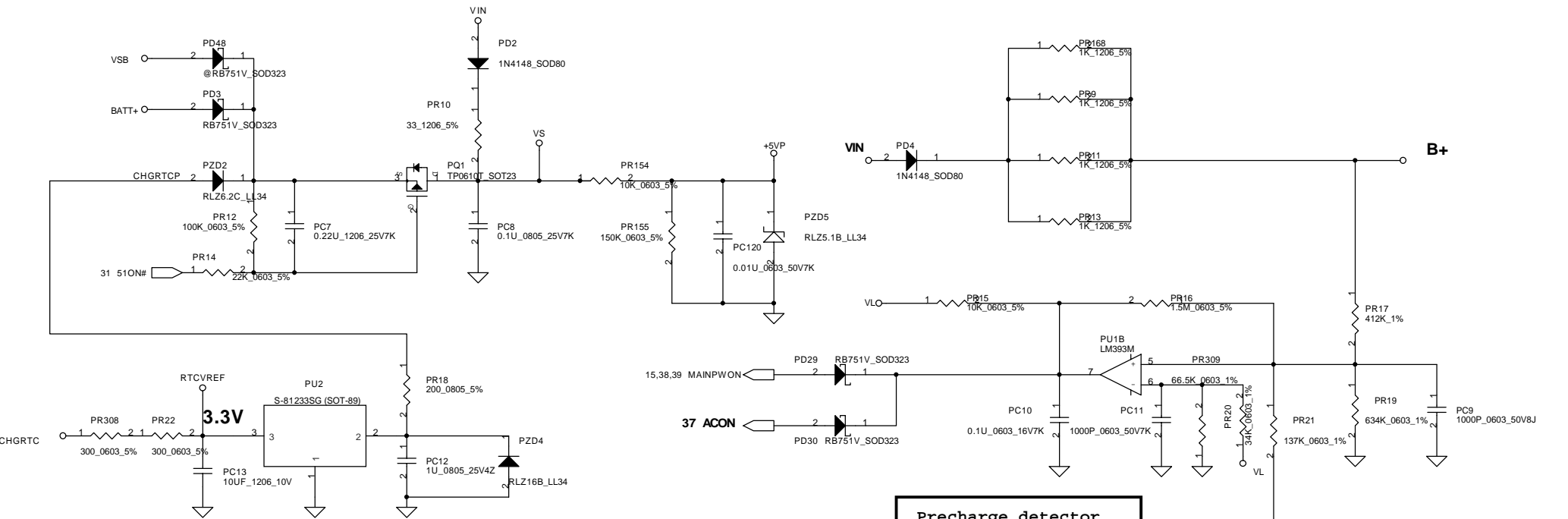


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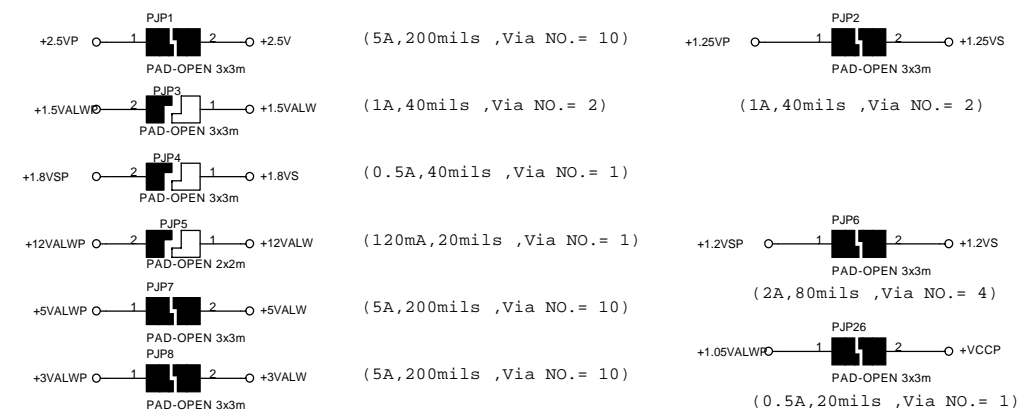


Vin Detector		
High	18.764	17.901
Low	17.745	16.903
	17.063	16.038

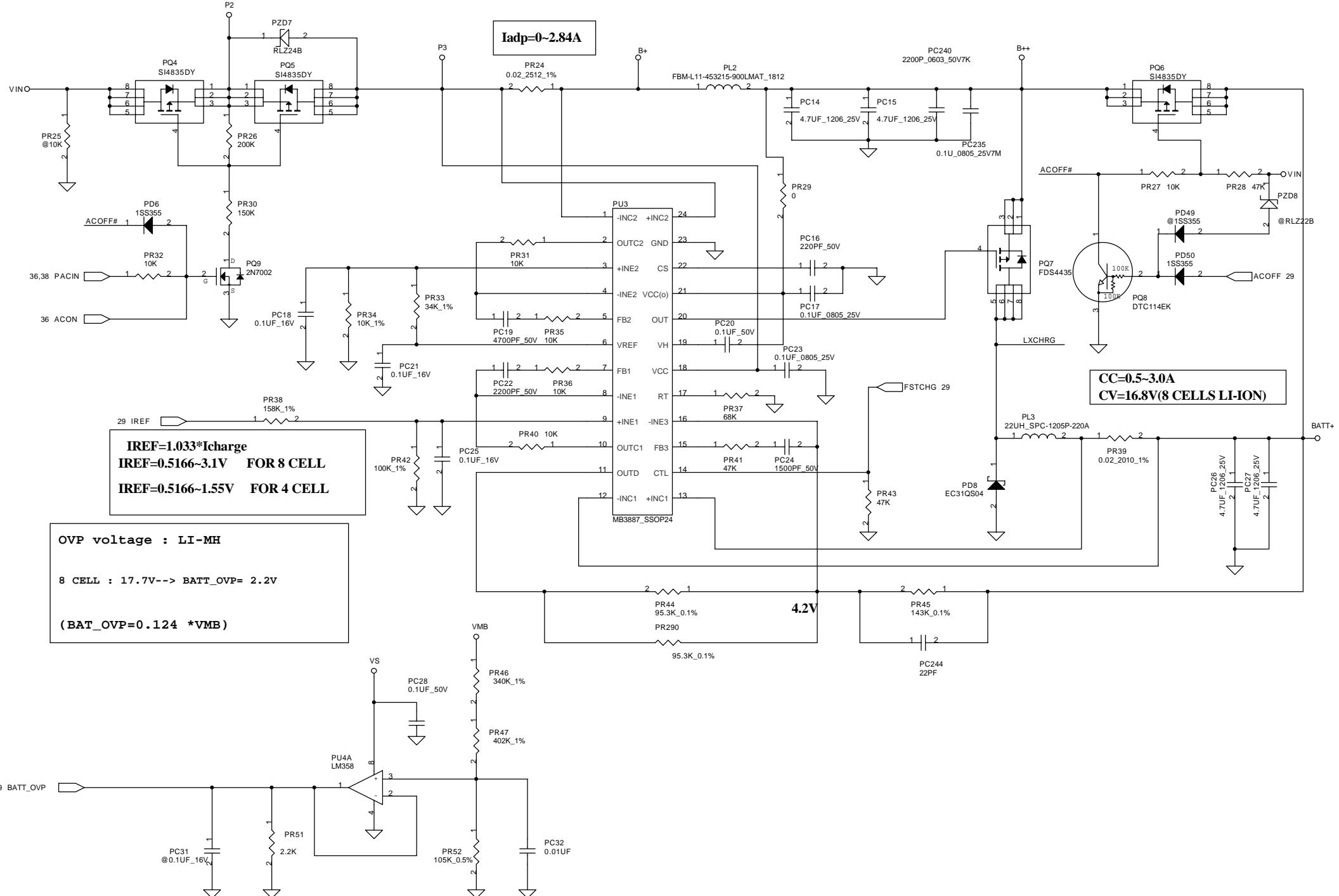


Precharge detector AC ADAPTOR		
	16.69	16.05
	15.6	15.02
	14.35	14.35

Precharge detector AC ADAPTOR		
	6.33	6.12
	5.227	5.09
	4.85	4.85

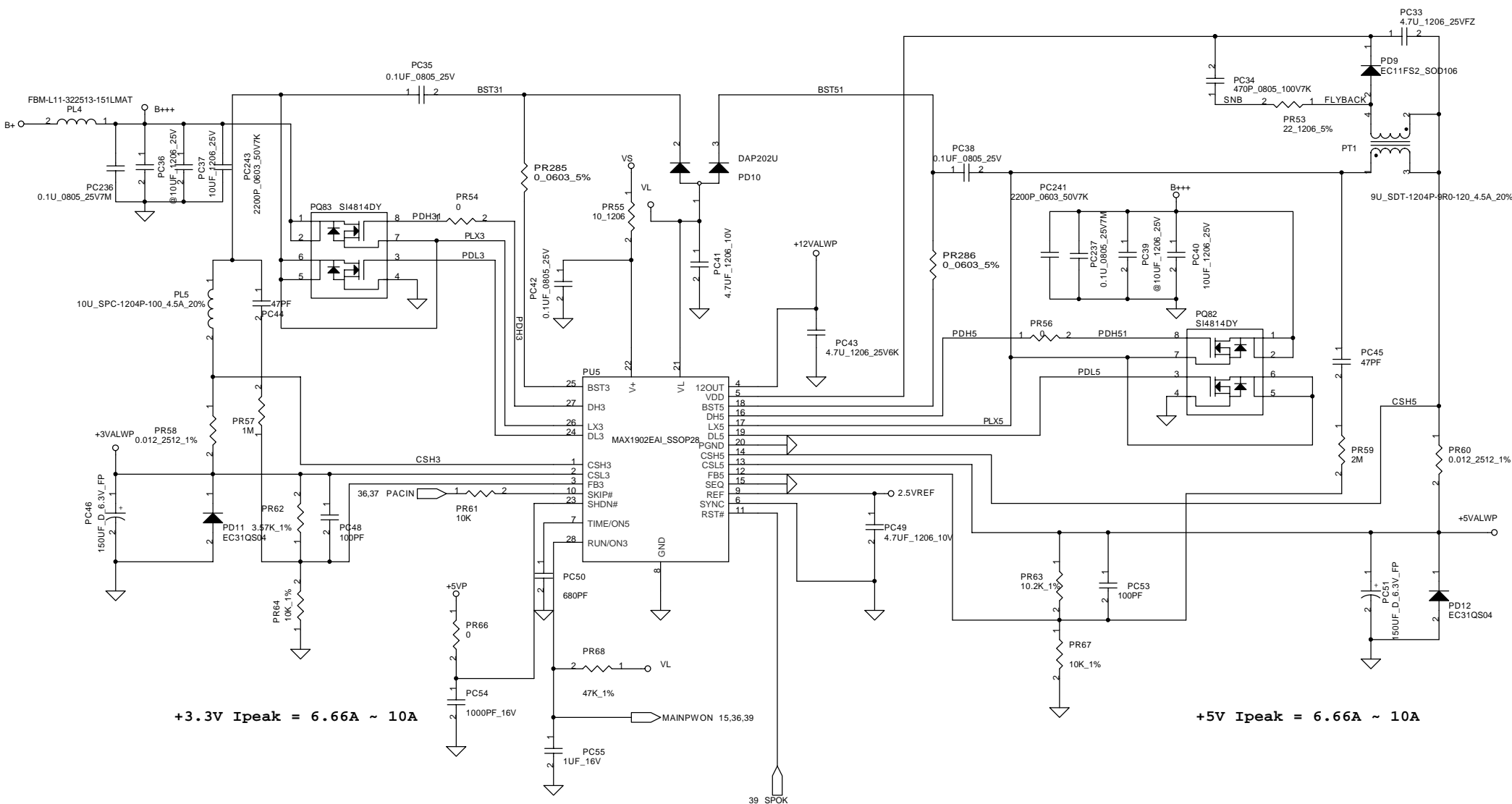


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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

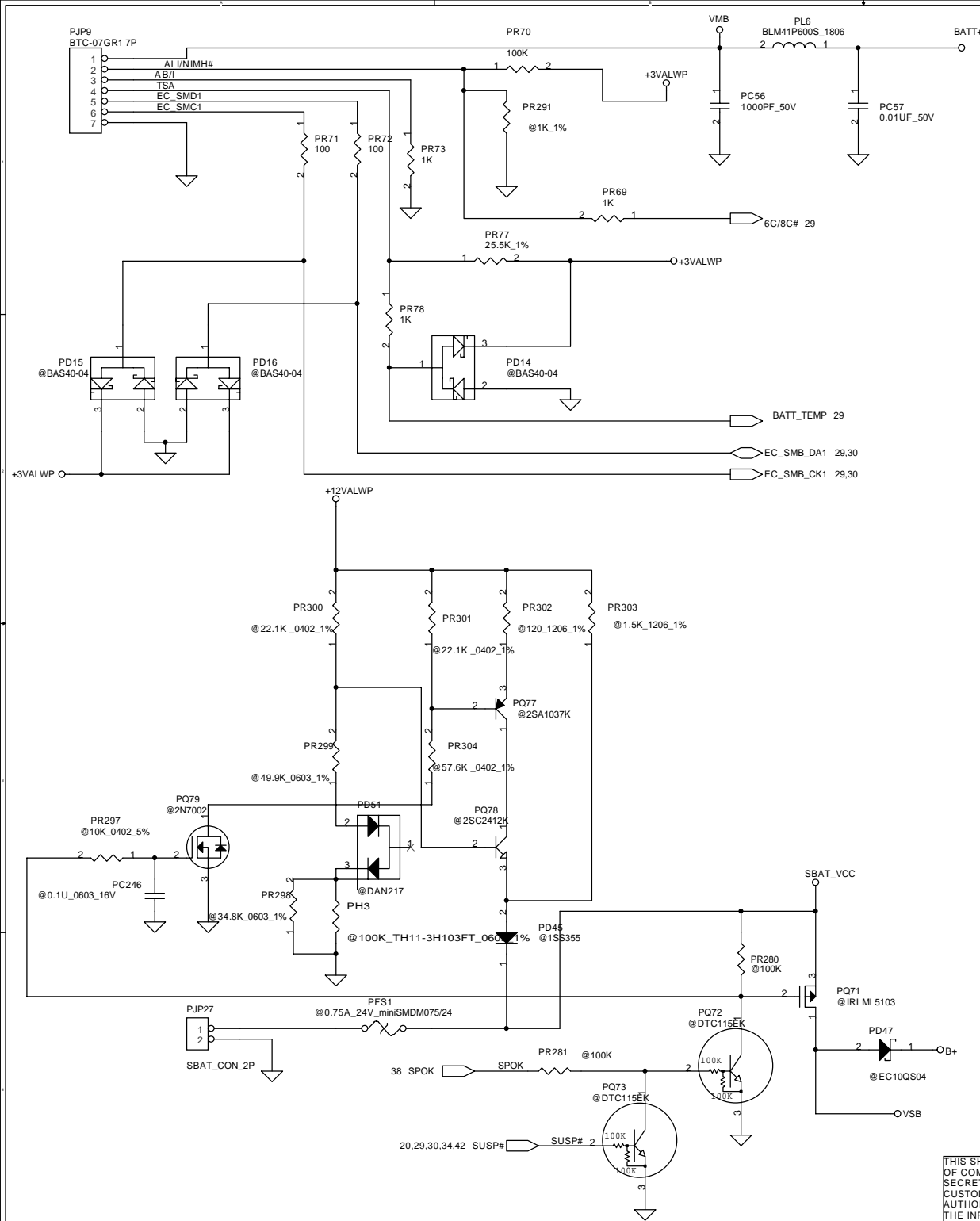
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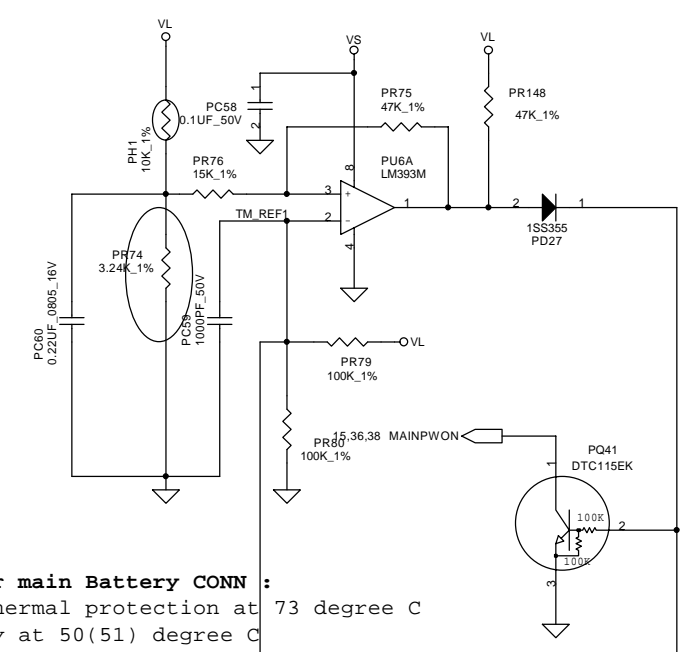
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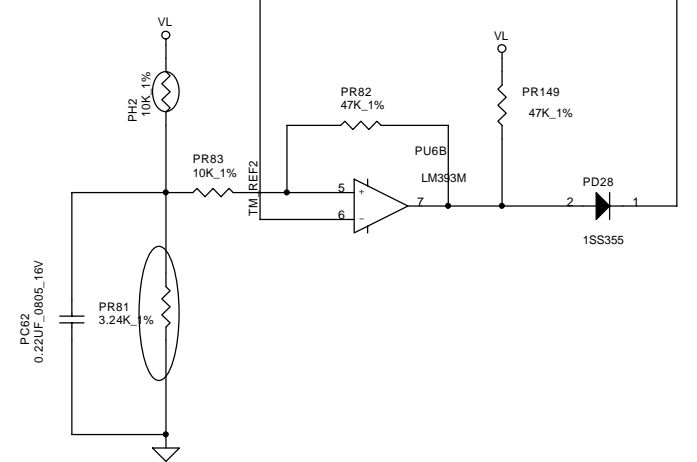
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PH1 under CPU bottom side :
 CPU thermal protection at 82 degree C
 Recovery at 48 degree C



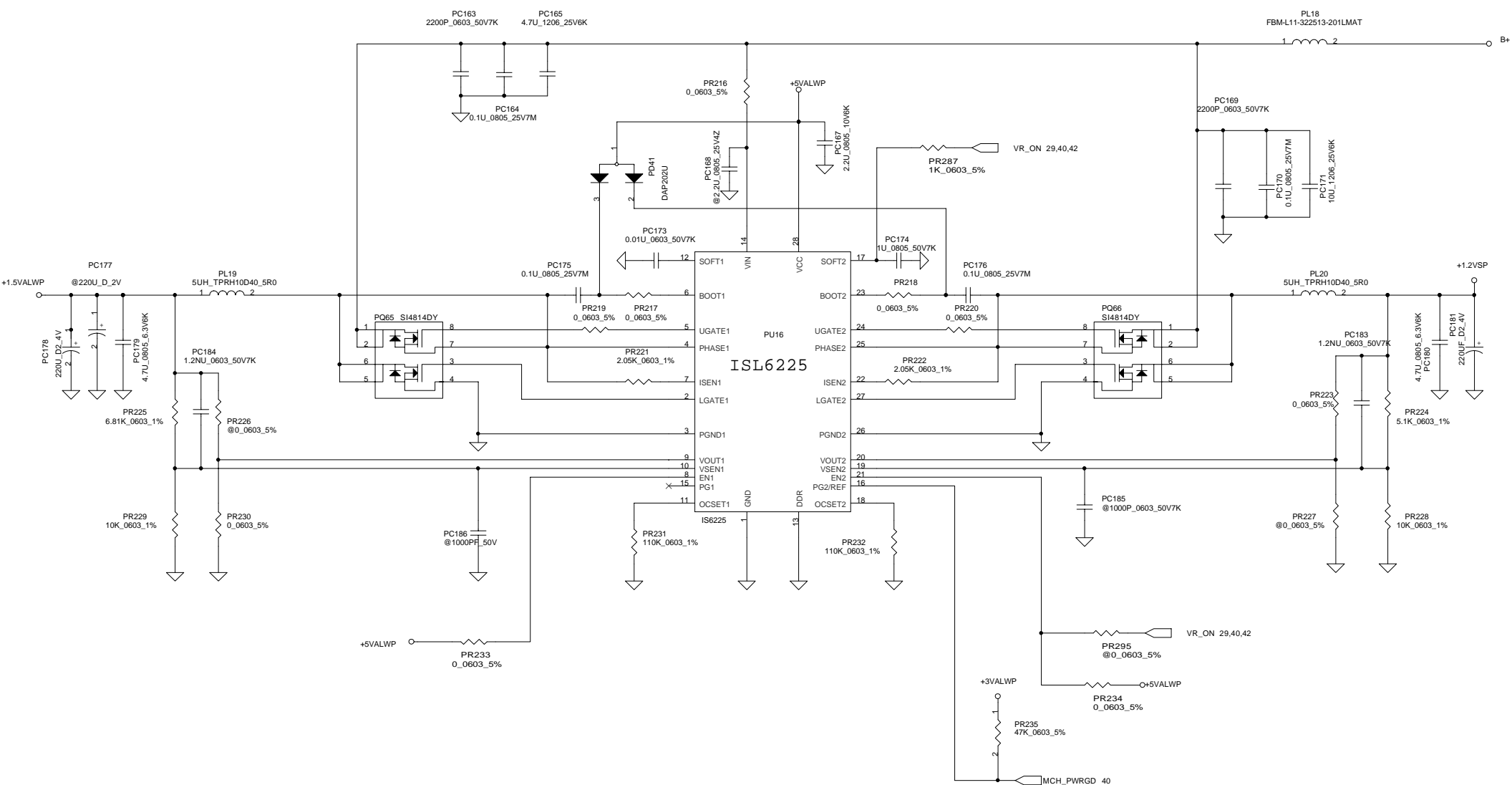
PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50(51) degree C



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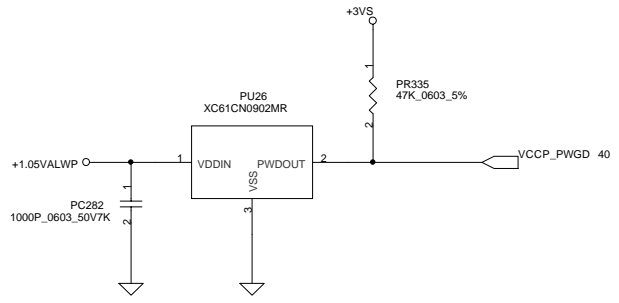
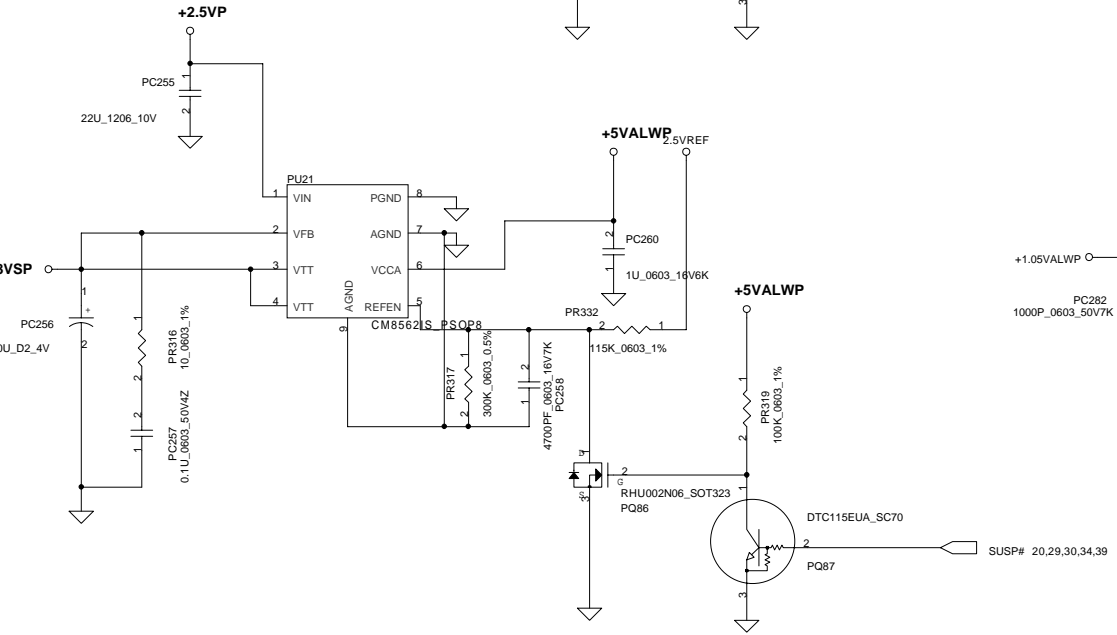
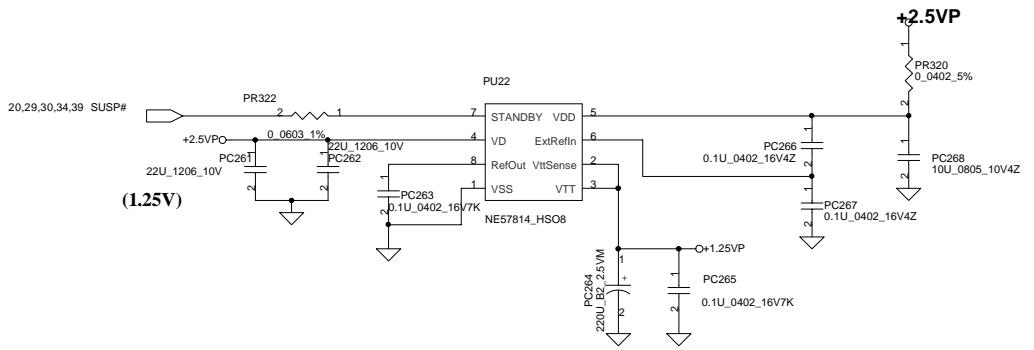
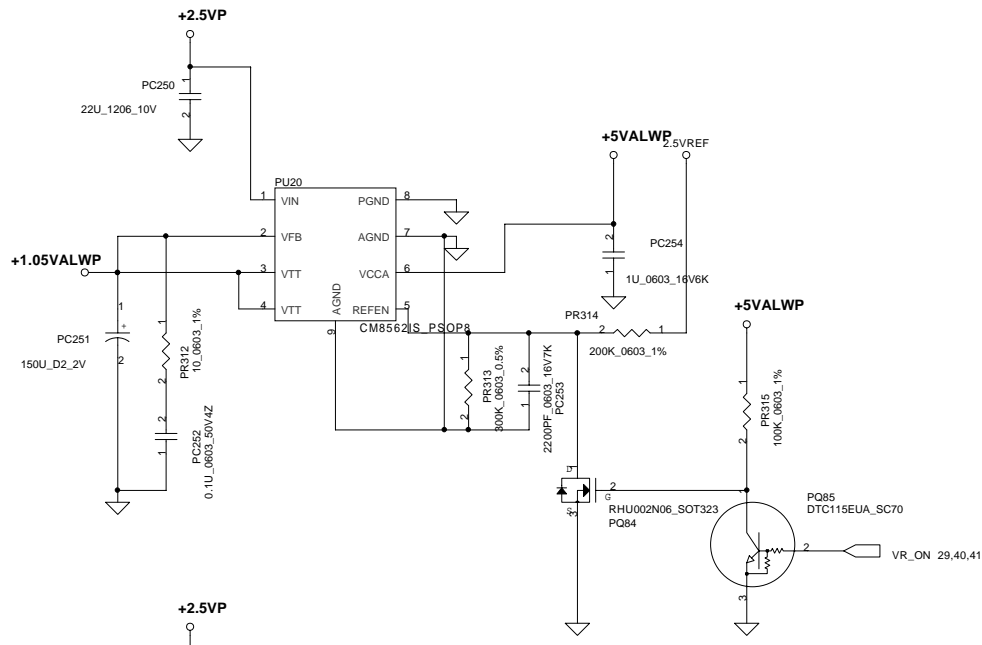
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+1.5VALWPV/+1.2VSP



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		Set c4 mode controlled by bios based difference CPU		40	DELETE PR311:100K ; ADD PR277:0		DVT
2		Modify 1.05VP voltage level		42	1. change PR314 to 200k		DVT
3		modify 1.05VP,1.8VP soft start time		42	add PC253, PC258 to be 0.1U		DVT
4		add +SDREF signal circuit		43	add PR339:0; PQ89: 2N7002; PC283,PC284 :0.1U 16V;PR336,PR337:100K;PC285:10U 1206		PVT
5		Add one set power good:VCCP_PWGD		42,41	ADD LDO PU26 :XC61CN;PR335:47K;PC282:1000P 50V,PCHANGE R235 FROM 10K TO 47K		PVT
6		modify 1.05VP,1.8VP soft start time		42	CHANGE PC253 from 0.1u to 2200PF, PC258 from 0.1U to 4700PF		PVT
7		CHANGE PU5 from MAX1631 to MAX1902 (BECAUSE MAX1631 shortage)		38	CHANGE PT1 from 10u_1205P to 9u_sdt-1204p-9r0-120;delete PU19;CHANGE p15 FROM 10U_SPC-1205P-100 to 10u_1204p-100_4.5A;change PC39 from 180PF to 470PF;DELETE PZD6;change PU5 from max1631 to max1902		MP
8		FOR CL53A ; To change 1.2VSP to 1.35 VSP		37,41	CHANGE PR224 from 3.48K to 5.1K, delete PD49,DELETE PZD8		
9							

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		reserve +SDREF signal circuit		8	reserve R477,R479		PVT
2		reserve +SDREF signal circuit		10	reserve R480,R481		PVT
3		EMI performance		8	change C420_net from MRCOMP to +2.5V		PVT
4		reserve syson,susp#,vr_on pull low resister		29	reserve R482,R483,R484		PVT
5		cost down			change L18,L19,L14,L13,L12,L8,L9,L7 to 0 ohm del C534,C45		PVT
6		board version update		29	change R361 from 8.2k to 18k		PVT
7		for customer request			del TV_out , 1394 funtion		PVT
8		solove leakage			del D15		preMP
9		board version update		29	change R361 from 8.2k to 33k		preMP
10	USB port will be damaged by ESD, add ESD protect diode.	Per Lenovo request, add USB ESD protect diode	Rev3.0	26	Add D18, D32, D33. Change C239, C34, C22, C21, C24, C23 from 470P to 3.3P.		MP

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