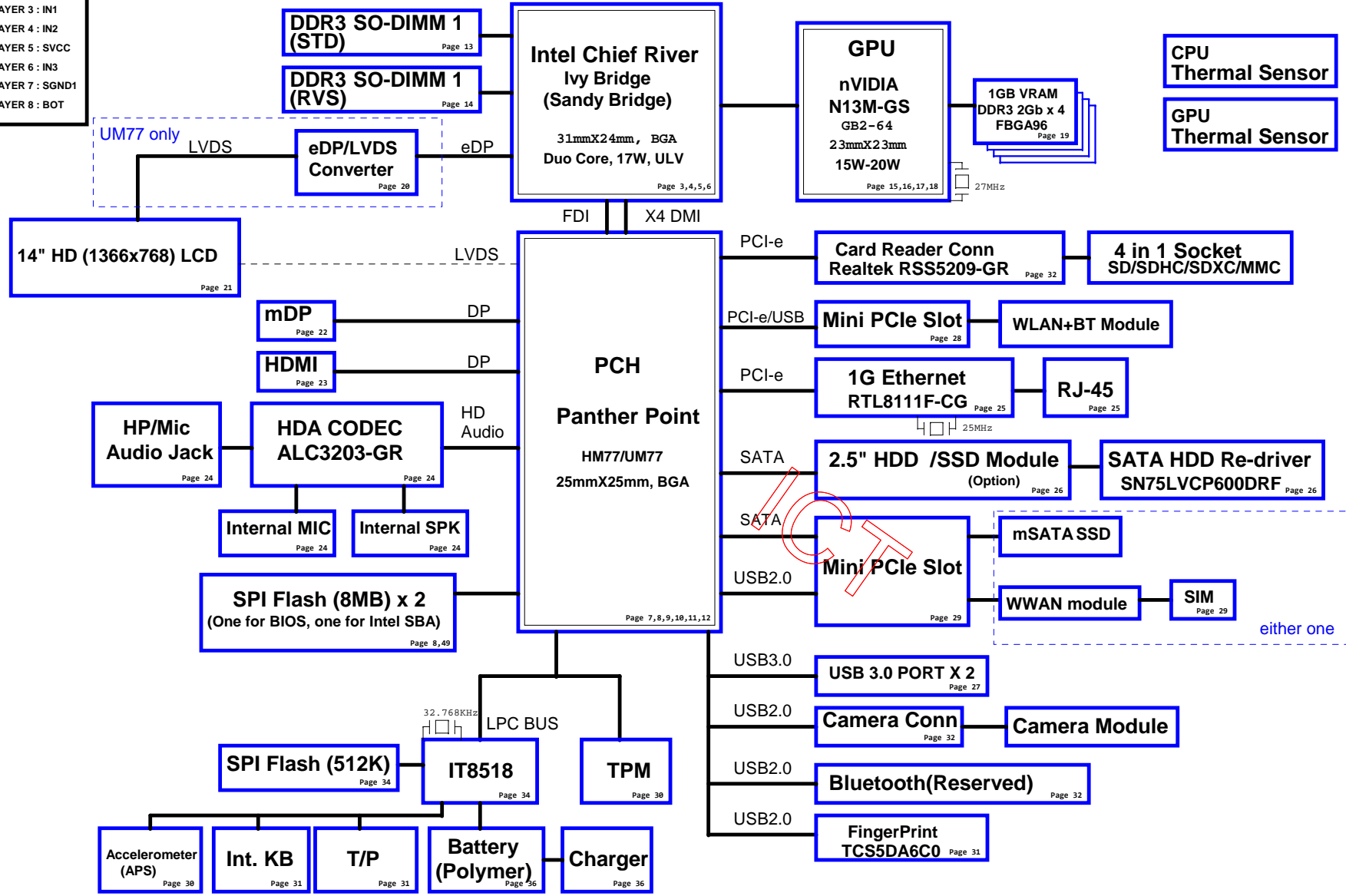


LV3D-14" Block Diagram -- Intel Chief River ULV

PCB STACK UP 8L

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1
 LAYER 4 : IN2
 LAYER 5 : SVCC
 LAYER 6 : IN3
 LAYER 7 : SGND1
 LAYER 8 : BOT



POWER

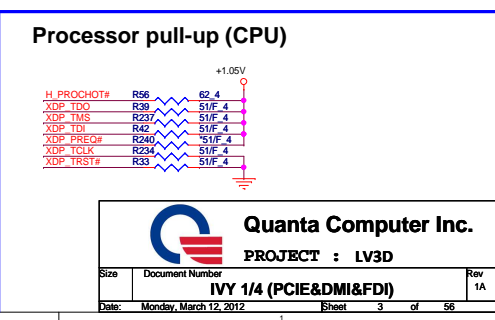
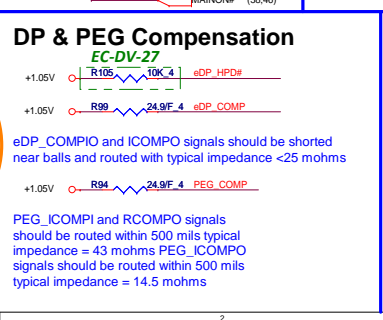
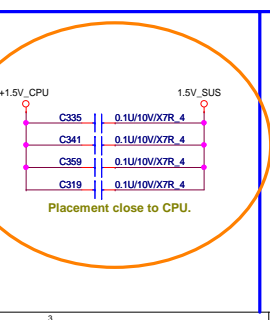
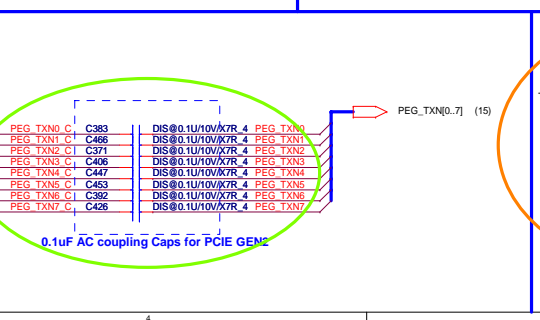
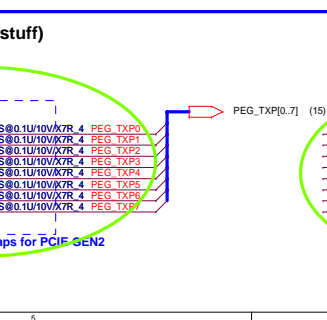
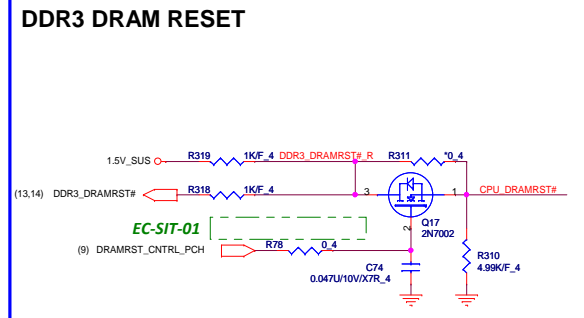
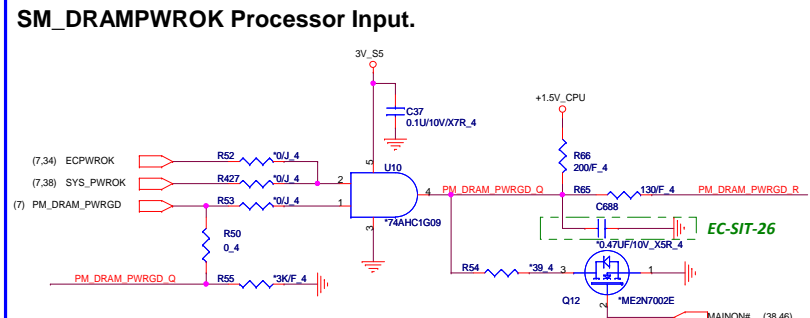
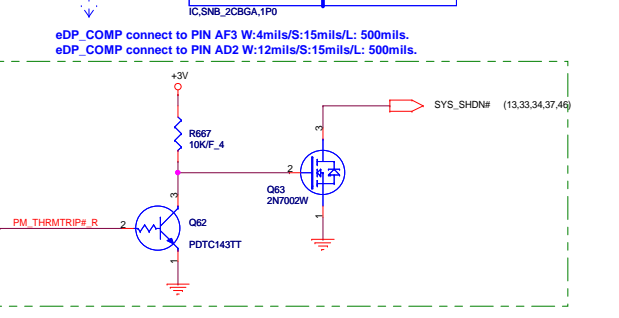
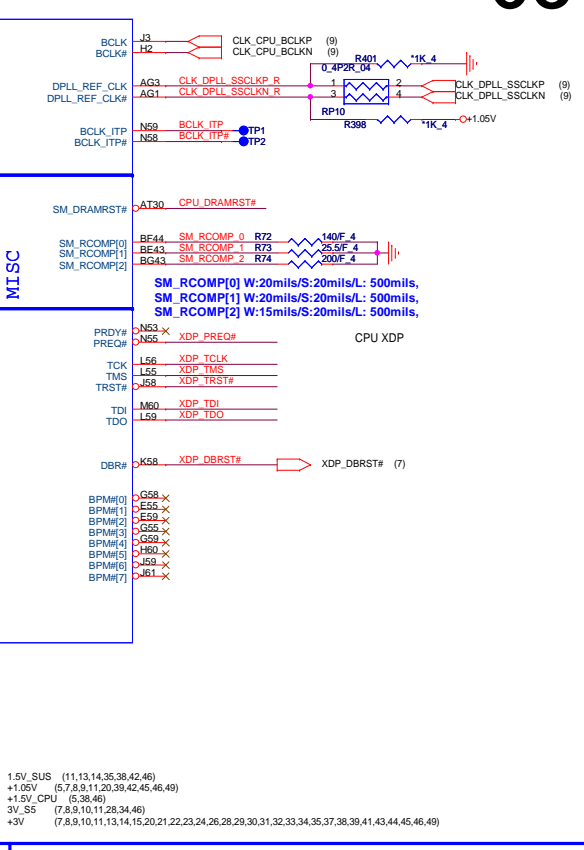
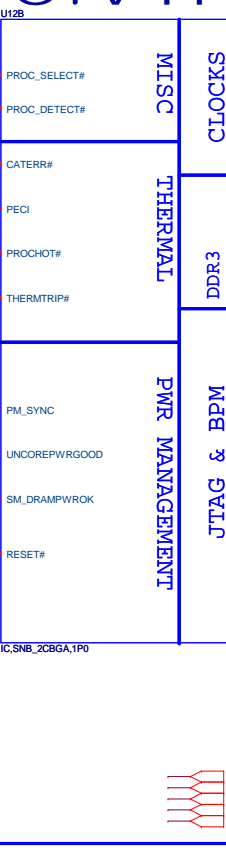
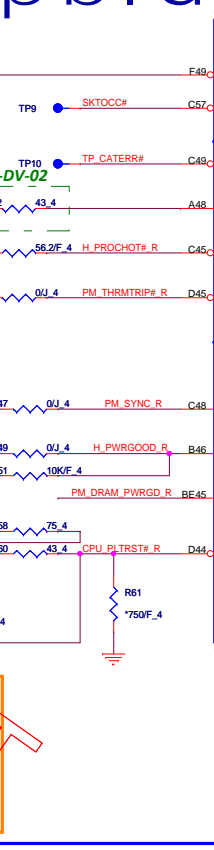
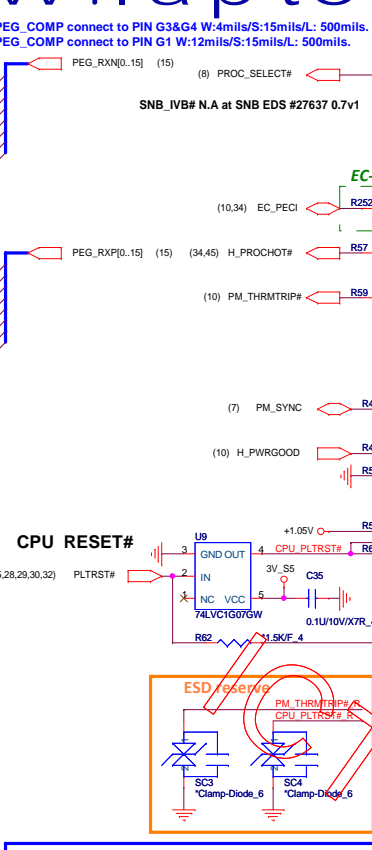
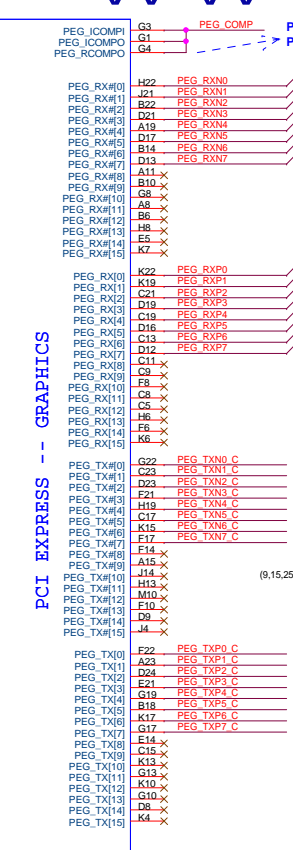
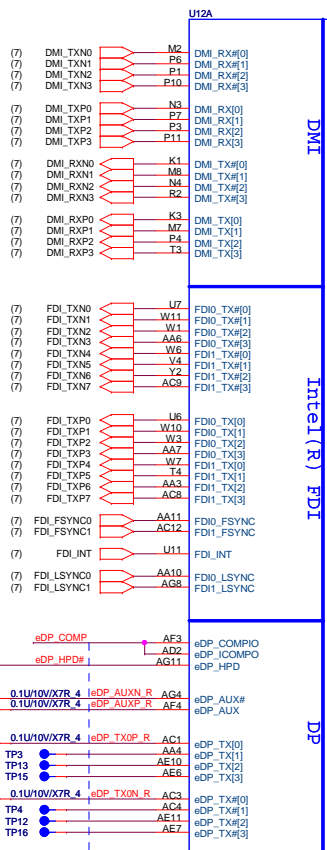
DC/DC 3VPCU, 5VPCU, +15V	Page 37
REGULATOR (DDR3) 1.5VSUS, +0.75V_DDR_VTT	Page 38
REGULATOR +1.05V&+1.8V	Page 39,40
REGULATOR +VCCSA	Page 41
CPU Core +VCC_CORE & +VCC_GFX	Page 45
Charger VIN	Page 36
RUN POWER SW/Discharge 3VSUS,5VSUS, 3V_S5, 5V_S5, +3V, +5V	Page 46
dGPU Core GFX_CORE	Page 44

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20	PS8622 LVDS converter
21	LCD CONN
22	Mlni DisPlay Port
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24	AUDIO (ALC3202-VC3-GR)
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41	VCCSA (RT8241DZQW)
42	+1.5VGPU/+1.05V_GPU
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45	VCC_CORE (ISL95837)
46	POWER_Discharge
47	SBA Block
48	SBA M3 Power(RT8068A)
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50	

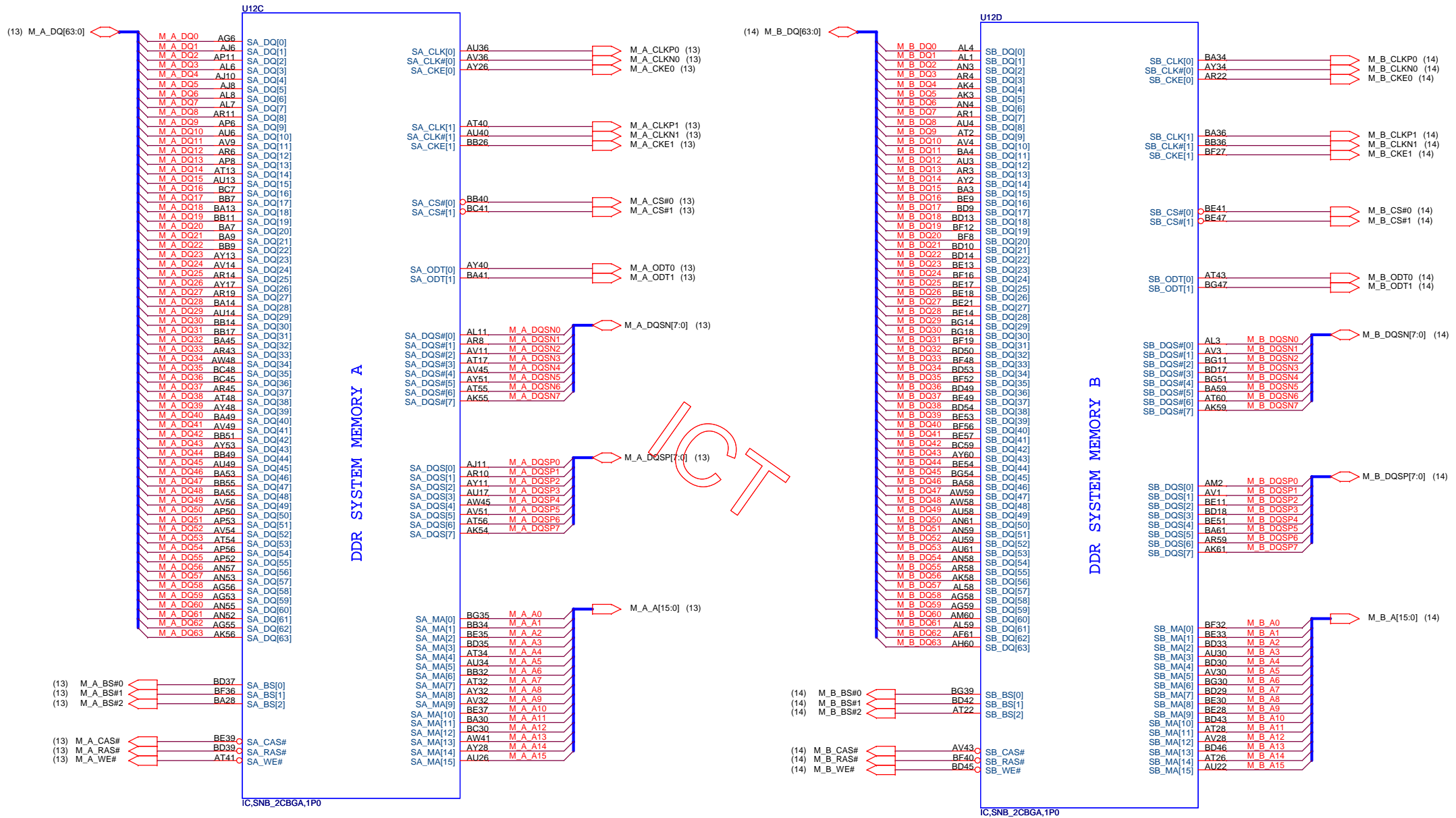
Power States


POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	21,36,37,38,39,41,44,45,46	MAIN POWER		S0-S5
+3V_RTC	+3.0V~+3.3V	7,8,11,34	RTC		S0-S5
3VPCU	+3.3V	7,8,21,25,28,32,34,36,37,39,40,46,48,49	IT8518/19 POWER	3V5V_EN	S0-S5
5VPCU	+5V	21,36,37,38,39,40,41,42,43,44,46,48	DC/DC POWER IC SOURCE	3V5V_EN	S0-S5
+15V	+15V	21,30,32,37,38,42,43,46,48	LARGE POWER	3V5V_EN	S0-S5
LANVCC	+3.3V	25,46	LAN POWER	LAN_ON	
5V_S5	+5V	11,27,46	PCH SUS POWER	S5_ON(AC only)	S0-S3
3V_S5	+3.3V	3,7,8,9,10,11,28,30,32,34,46	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON(AC only)	S0-S3
1.5V_SUS	+1.5V	3,11,13,14,38,42,46	DDR3 SODIMM POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	13,14,38,46	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,21,22,23,24,26,31,32,33,45,46	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,20,21,22,23,24,25,26,28,29,30,31,32,33,34,37,38,39,41,43,45,46,49	SLP_S3# CTRLD POWER	MAINON	S0
VCC_GFX	+0.65V~+1.25V	5,45,46	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5,41,46	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,40,46	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,20,39,42,45,46,49	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
VCC_CORE		5,6,45,46	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	21	LCD Power	ENVDD	S0
+3V_HDD	+3V	26	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	26	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	36	MAIN BATTERY	CHG_PBATT	S0-S5
+1.5V_CPU	+1.5V	3,5,38,46	DDR3 1.5V Rails	PS_S3CNTRL	S0

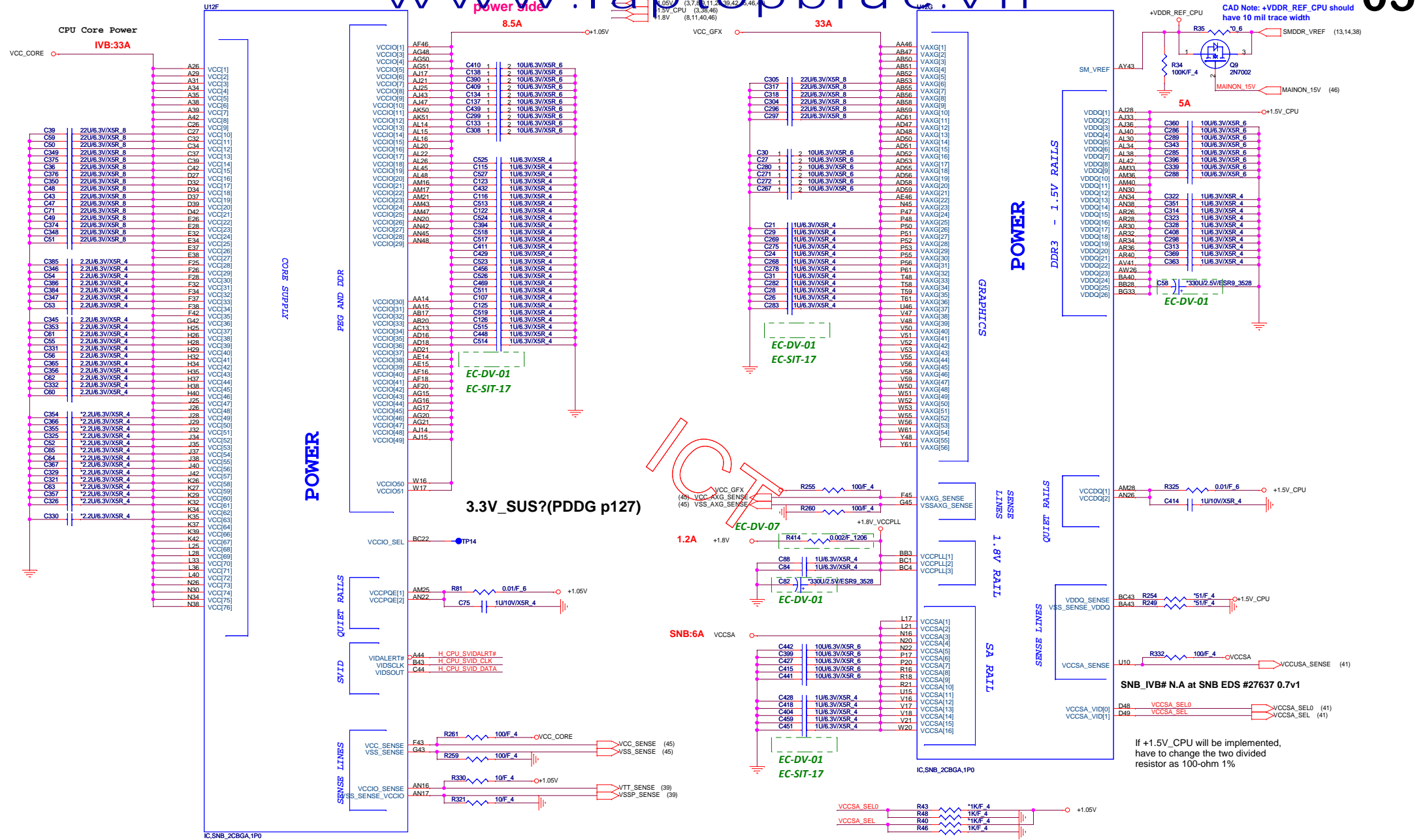


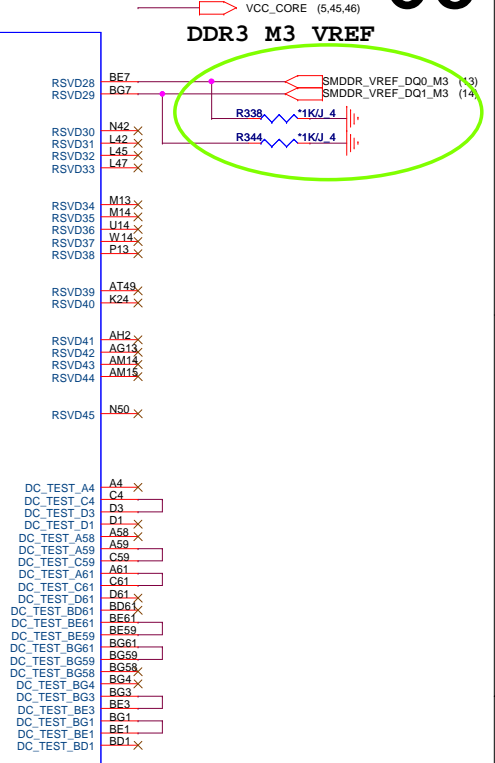
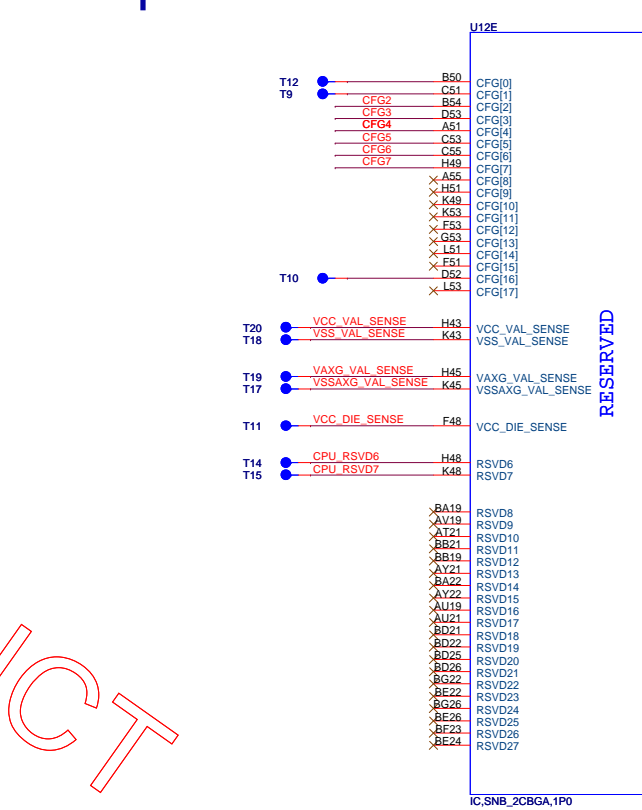
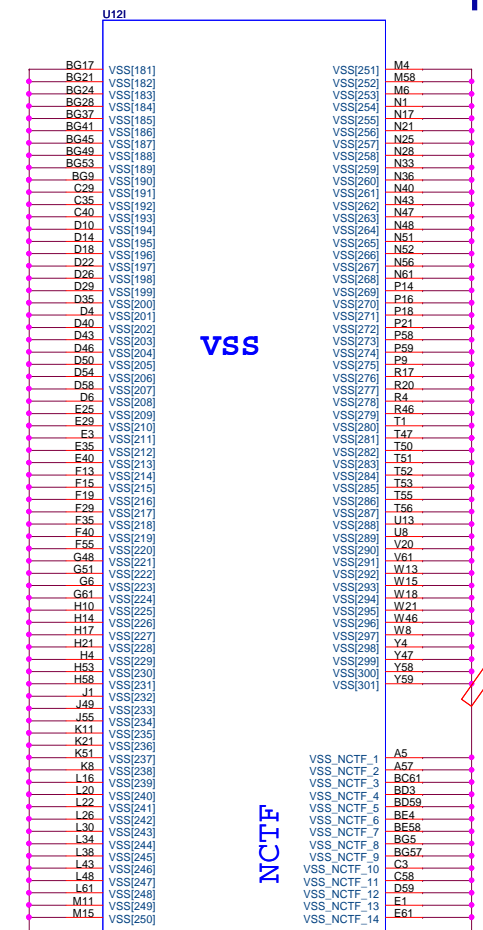
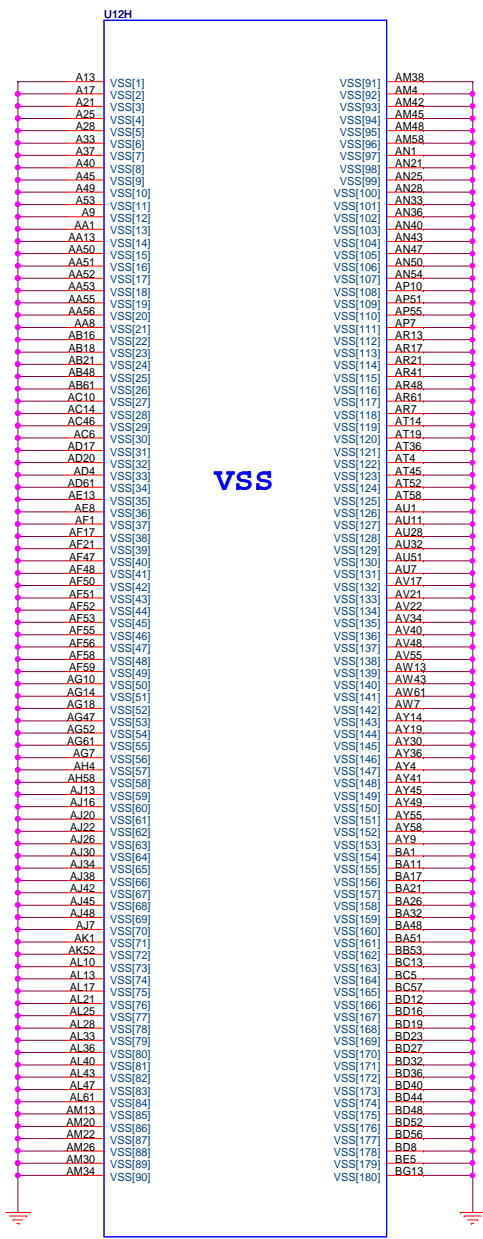
W Wy/Sandy Bridge Processor (DDR3)

04



 Quanta Computer Inc.		
PROJECT : LV3D		
Size	Document Number	Rev
	IVY 2/4 (DDR3 I/F)	1A
Date:	Monday, March 12, 2012	Sheet 4 of 56





CFG5 R37 *1KF 4

CFG6 R36 *1KF 4

CFG[6:5] (PCIe Strapping)

11: (Default) x16 - Device 1 functions 1 and 2 disabled

10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled

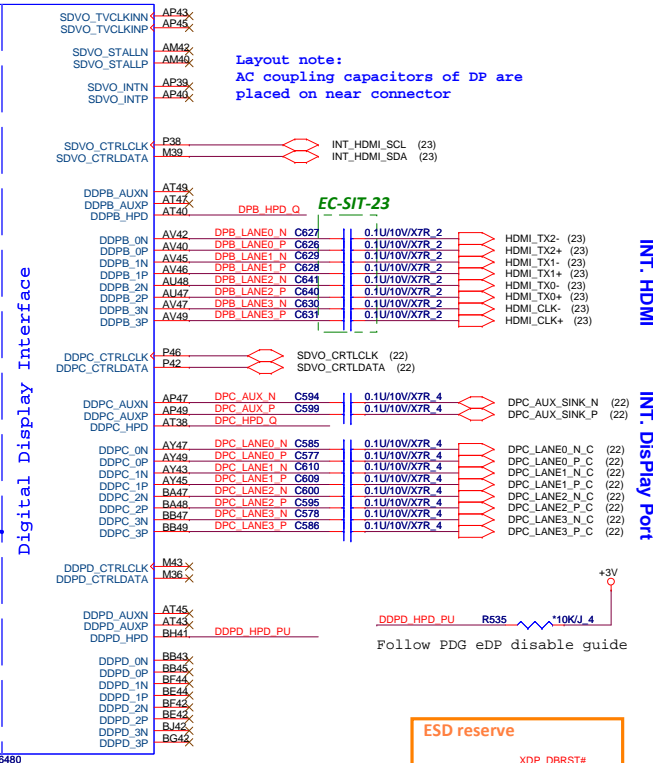
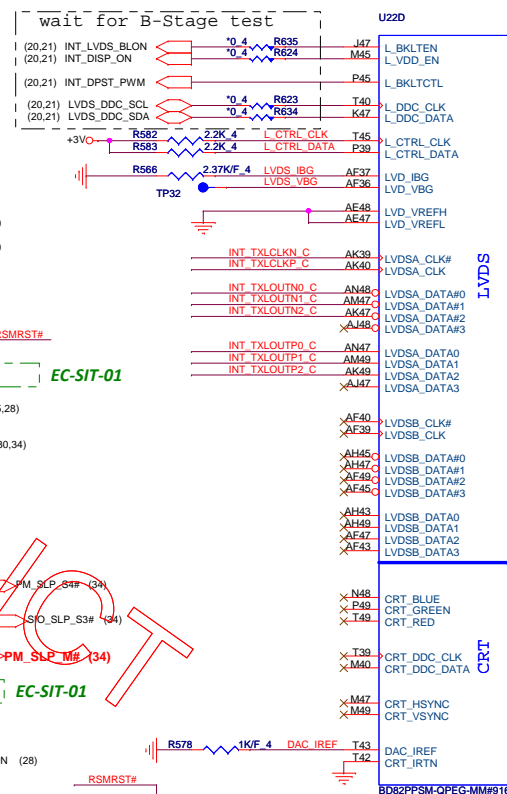
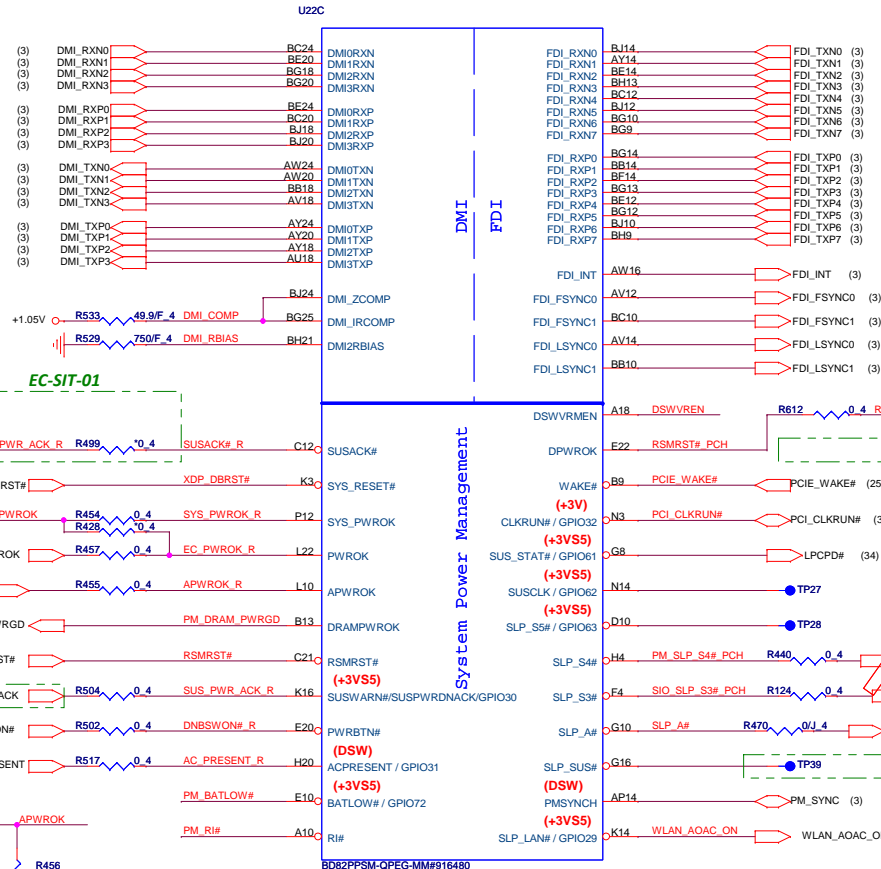
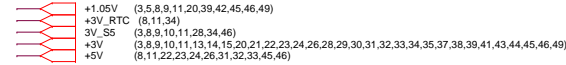
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)

00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

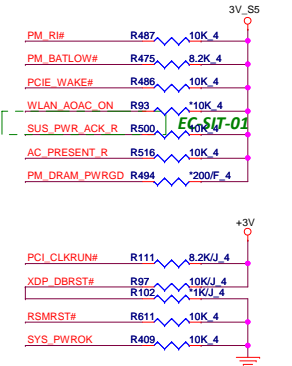
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

CFG	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

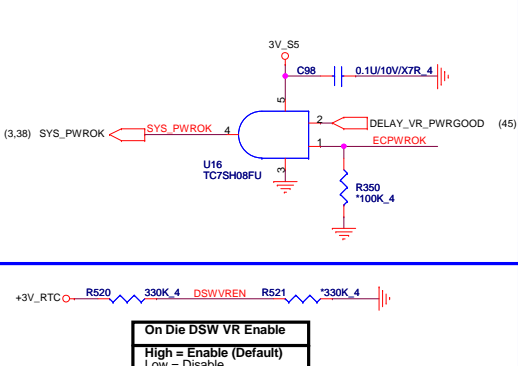




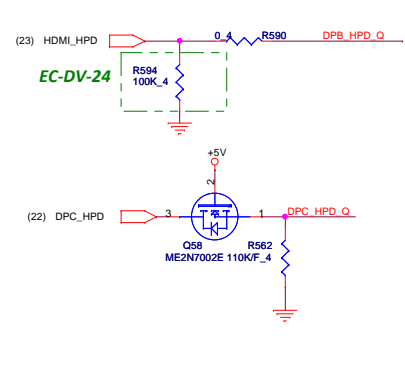
PCH Pull-high/low(CLG)



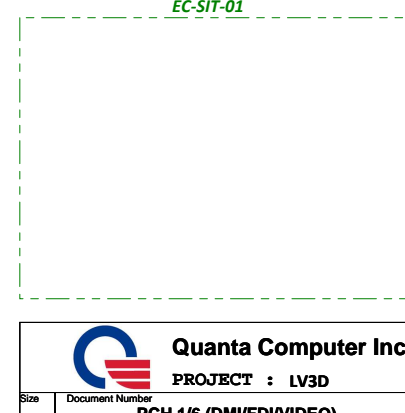
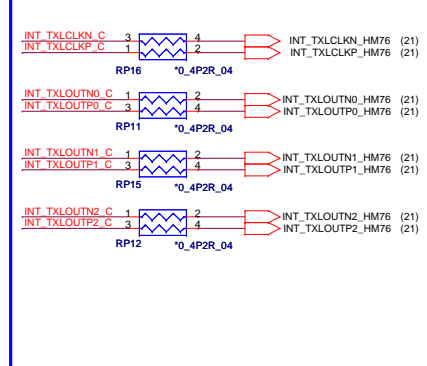
System PWR_OK(CLG)

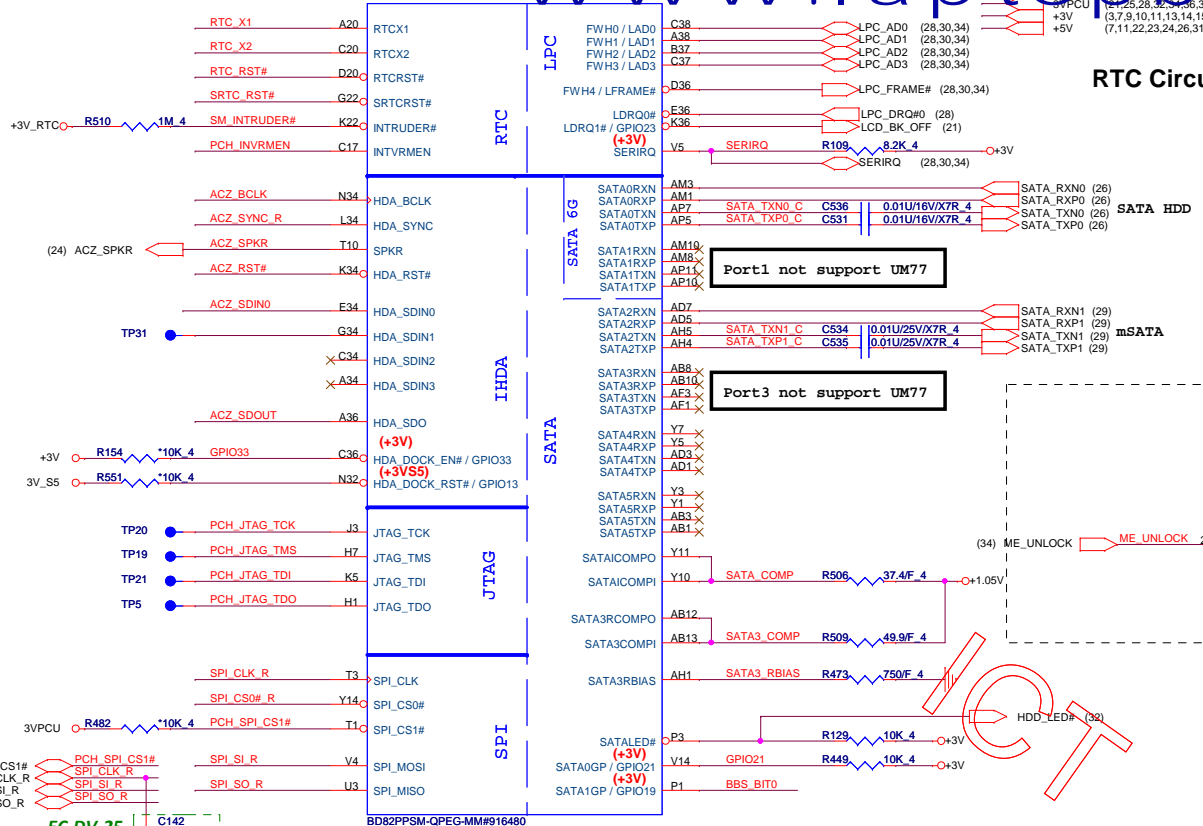


INT HDMI / Display Port DETECT

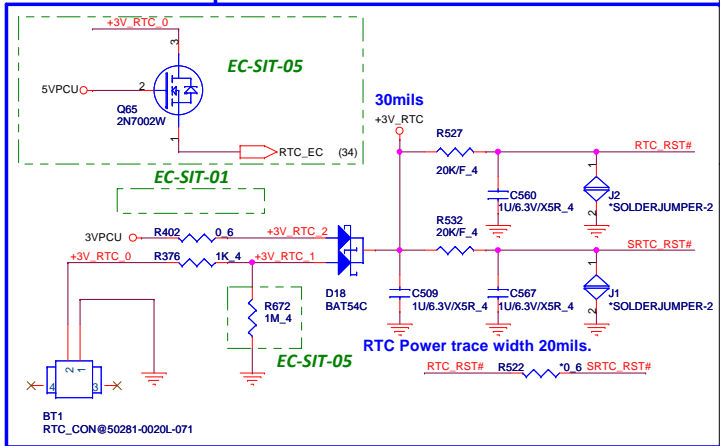
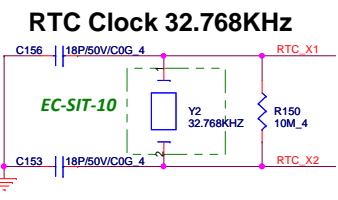


LVDS from HM77

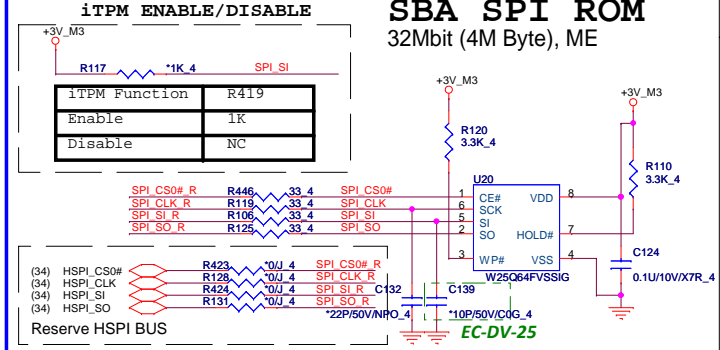




RTC Circuitry(RTC)



W25Q64CVSSIG: AKE3EFP0N04
 MX25L6406EM2I-12G: AKE3NFP0Z00
 EN25Q64-104HIP: AKE3EFP0Q00

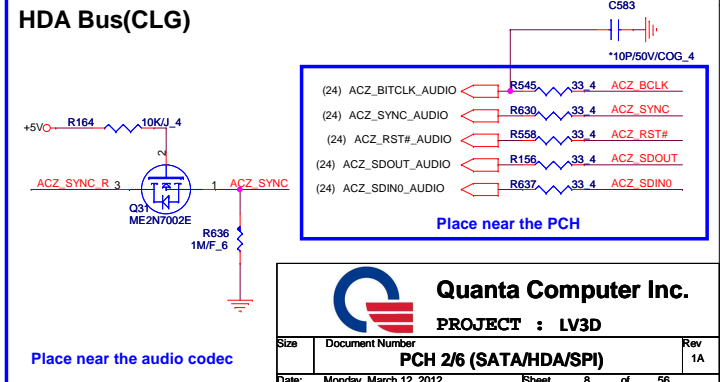


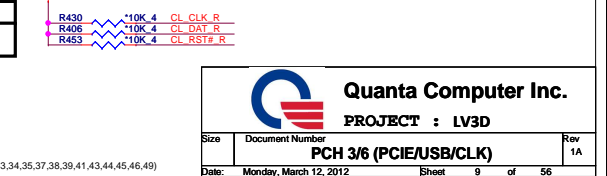
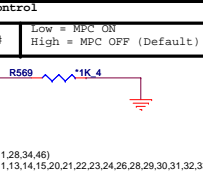
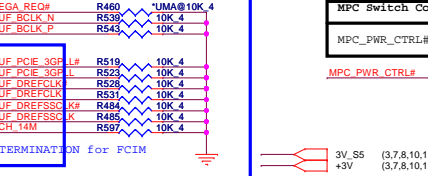
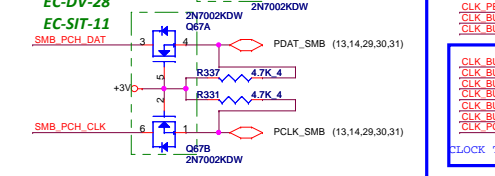
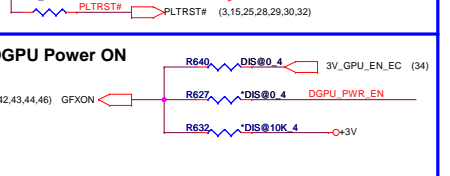
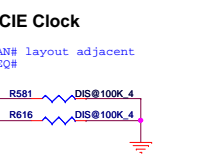
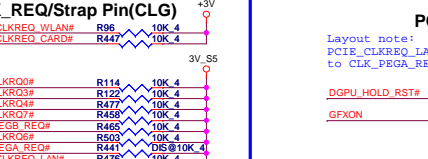
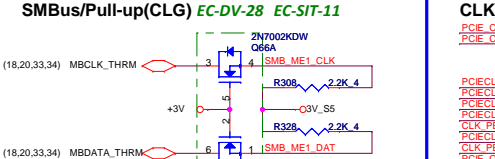
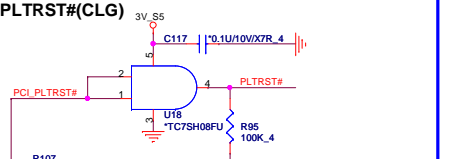
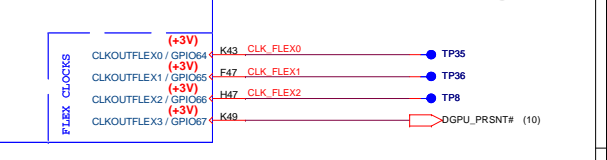
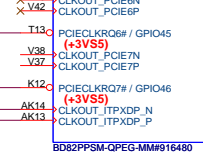
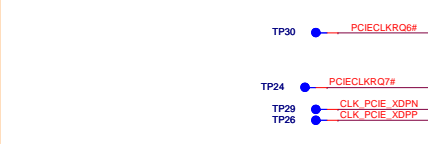
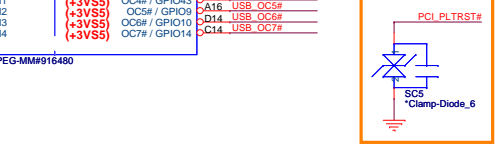
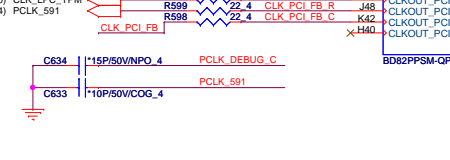
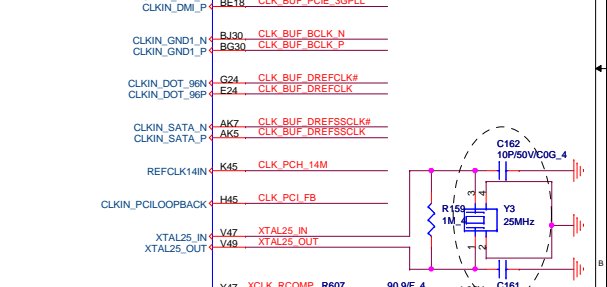
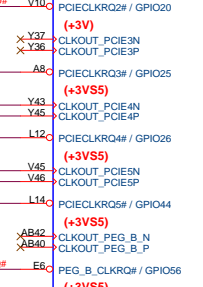
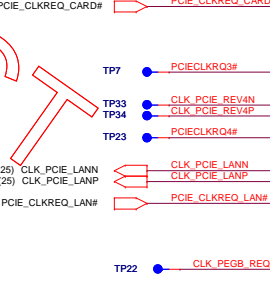
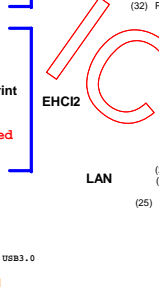
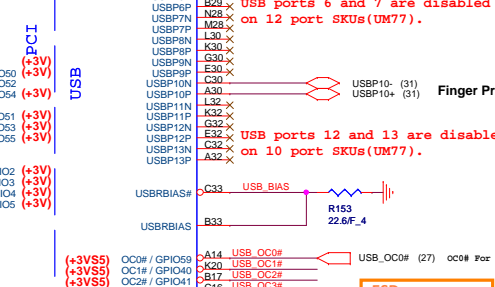
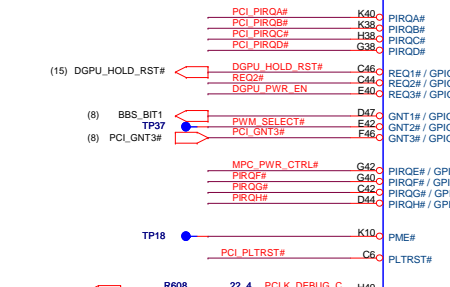
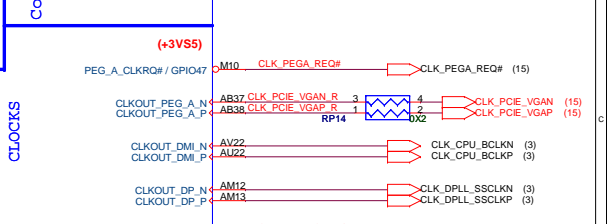
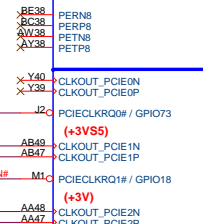
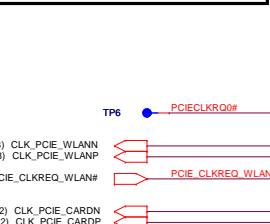
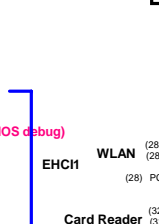
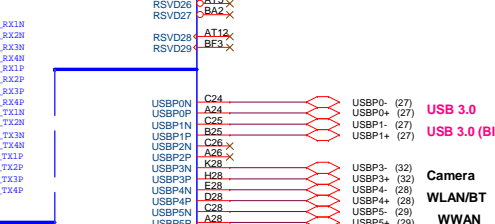
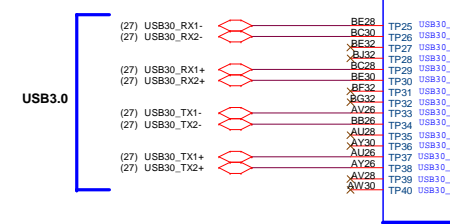
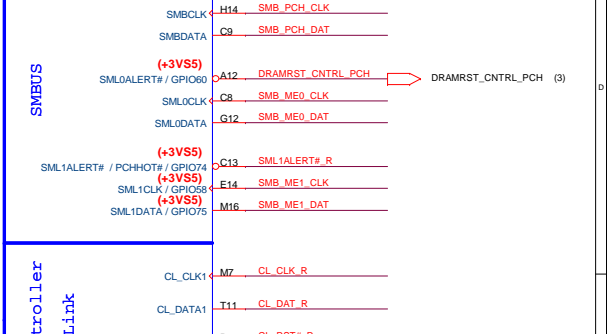
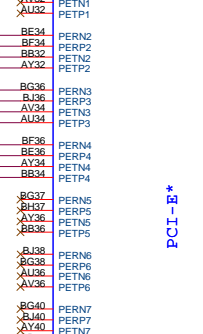
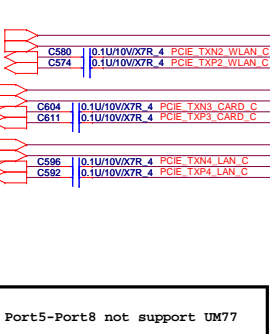
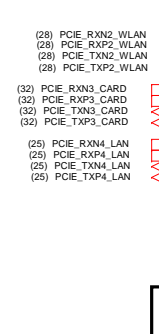
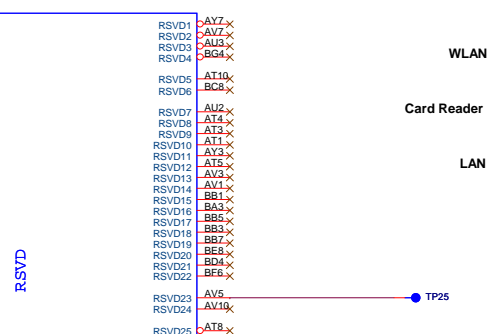
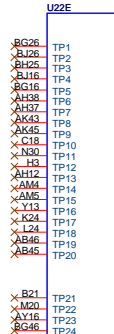
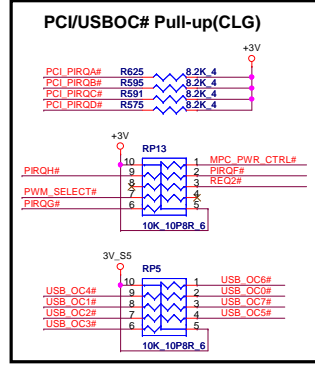
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R157 *1K 4 +3V									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R609 *1K 4 R621 *10K 4 +3V									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R524 *330K 4 +3V_RTC									
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R155 *1K 4 +3V_S5									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	[Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK		R127 *1K 4 R618 *1K 4 BBS_BIT0									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm	R471 *2.2K 4 +1.8V R478 *1K 4									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R161 *1K 4 ACZ_SYNC_R									
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite		Low = Disable (Default) High = Enable	(10) GPIO15 R104 *1K 4 +3V_S5									
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R434 *1K 4 PLL_ODRV_EN (10)									
DSWVREN	0: disable 1: enable												

if default boot destination is SPI, no external pull-up/down resistors on the board are necessary

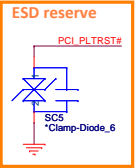
Support SBA Function will be Mounted

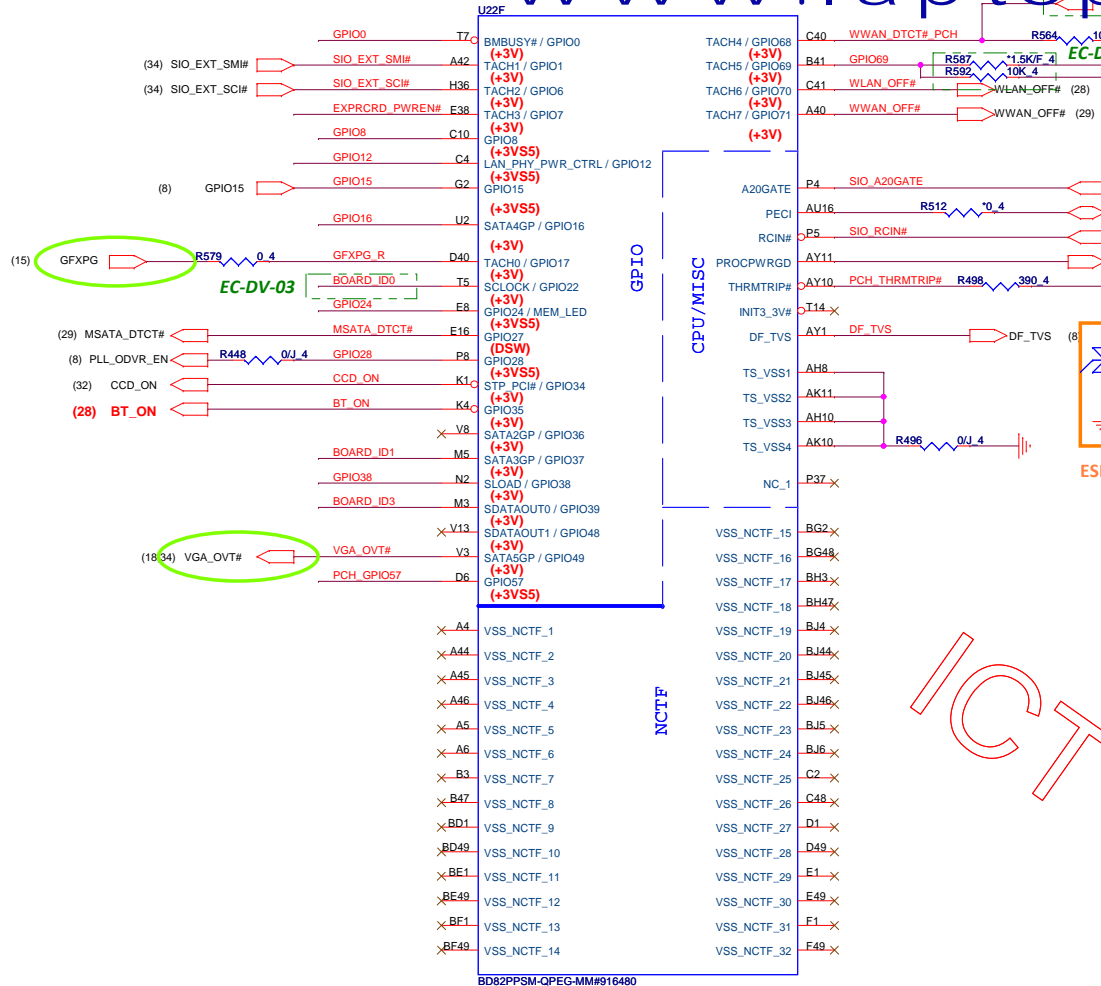




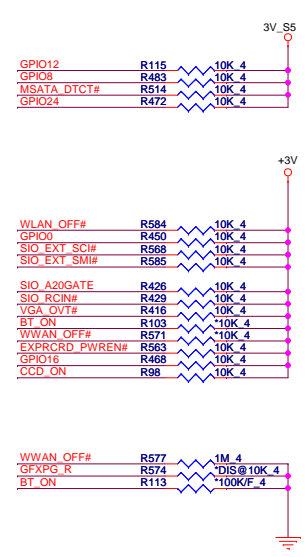
DO NOT

Port5-Port8 not support UM77



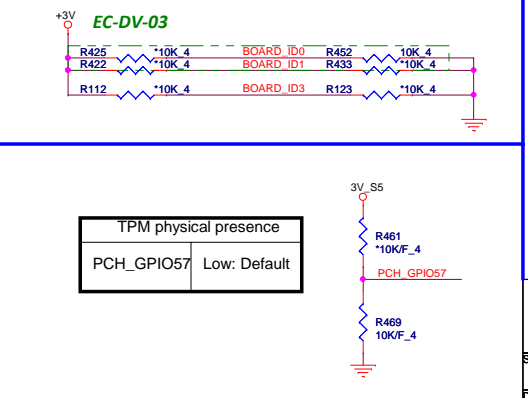
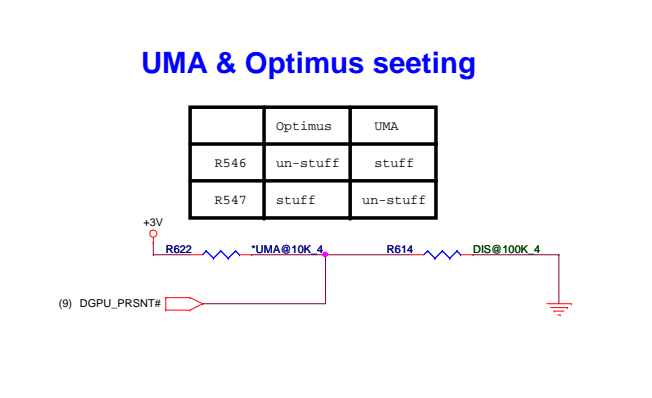
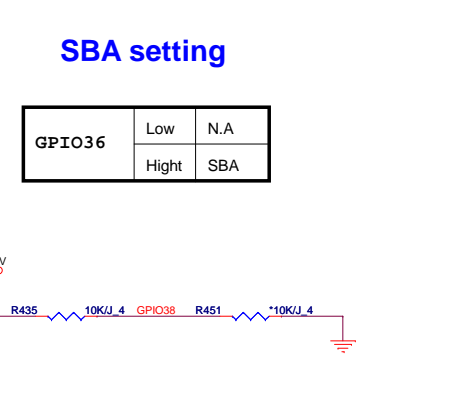


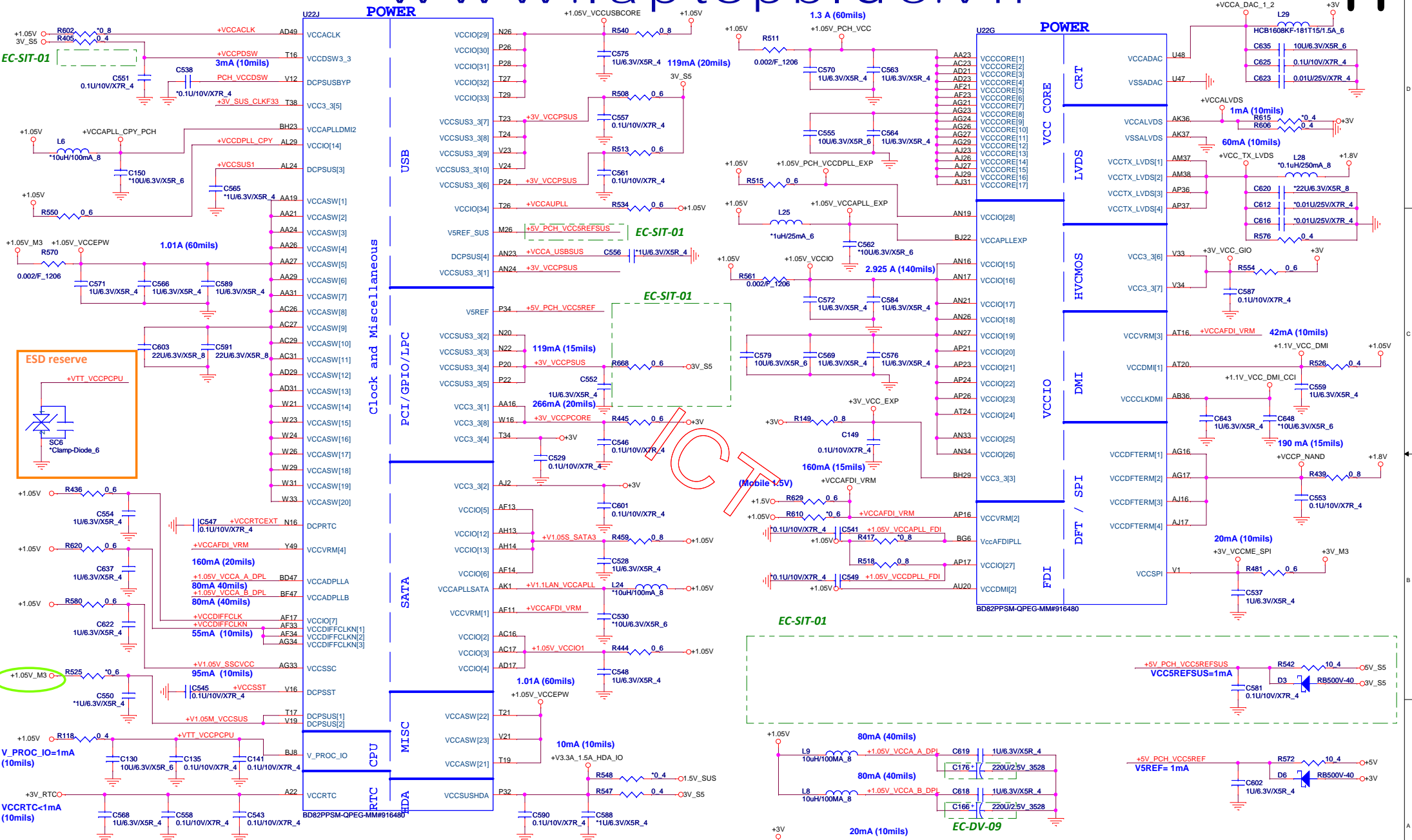
GPIO Pull-up/Pull-down(CLG)



BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3
For Function	GPIO22	GPIO37	GPIO38	GPIO39
SDV(ABBA)	0	0	0	0
SDV(Lovell)				
SIV(ABBA)				
SIV(Lovell)				
SIT(ABBA)				
SIT(Lovell)				
SVT(ABBA)				
SVT(Lovell)				
SOVP(ABBA)				
SOVP(Lovell)				



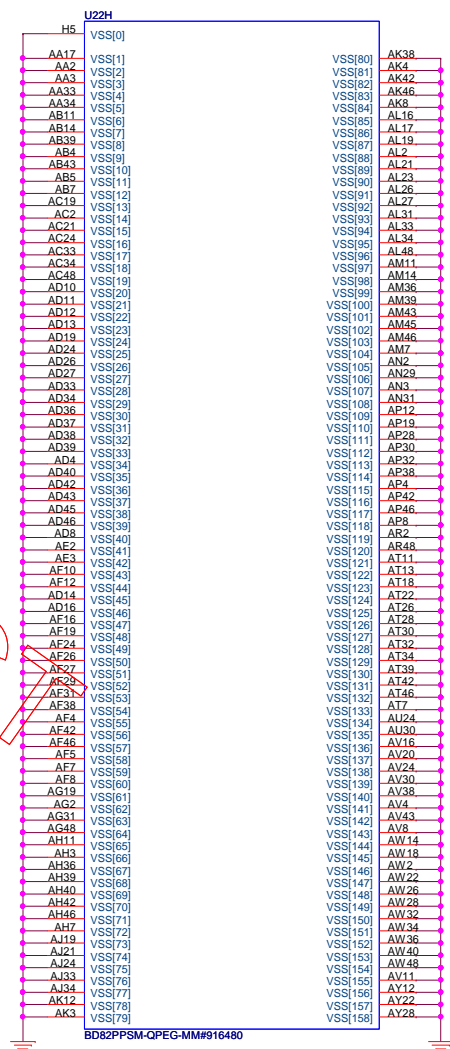
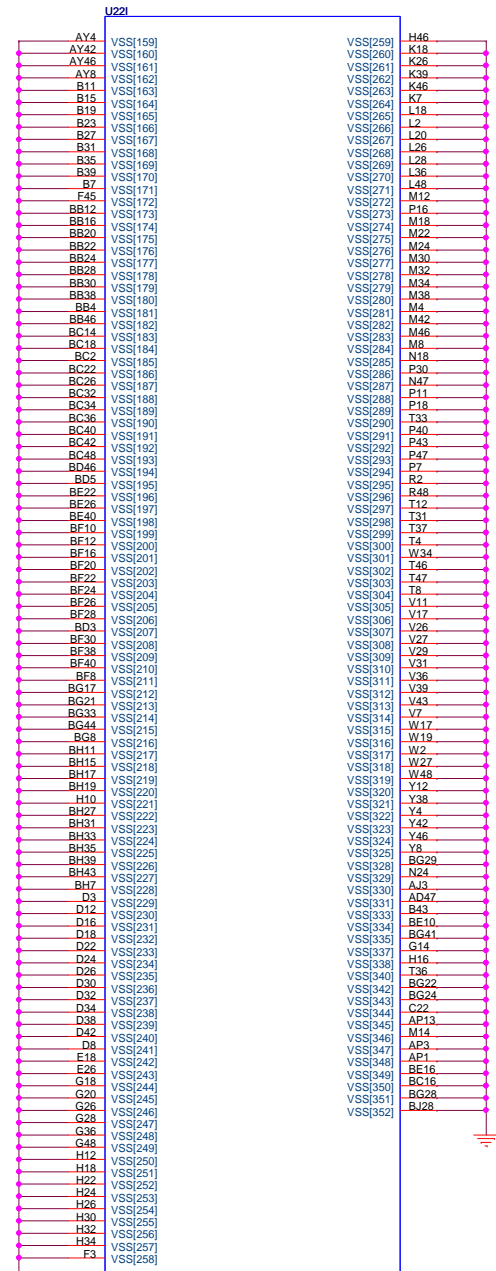


- +3V_M3 (8,25,48,49)
- +1.05V_M3 (48,49)
- +3V_RTC (7,8,34)
- 3V_S5 (3,7,8,9,10,28,34,46)
- +3V (3,7,8,9,10,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,43,44,45,46,49)
- 5V_S5 (27,46)
- +5V (7,8,22,23,24,26,31,32,33,45,46)
- +1.05V (3,5,7,8,9,20,39,42,45,46,49)
- 1.5V_SUS (3,13,14,35,38,42,46)
- +1.8V (5,8,40,46)

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PROJECT : LV3D

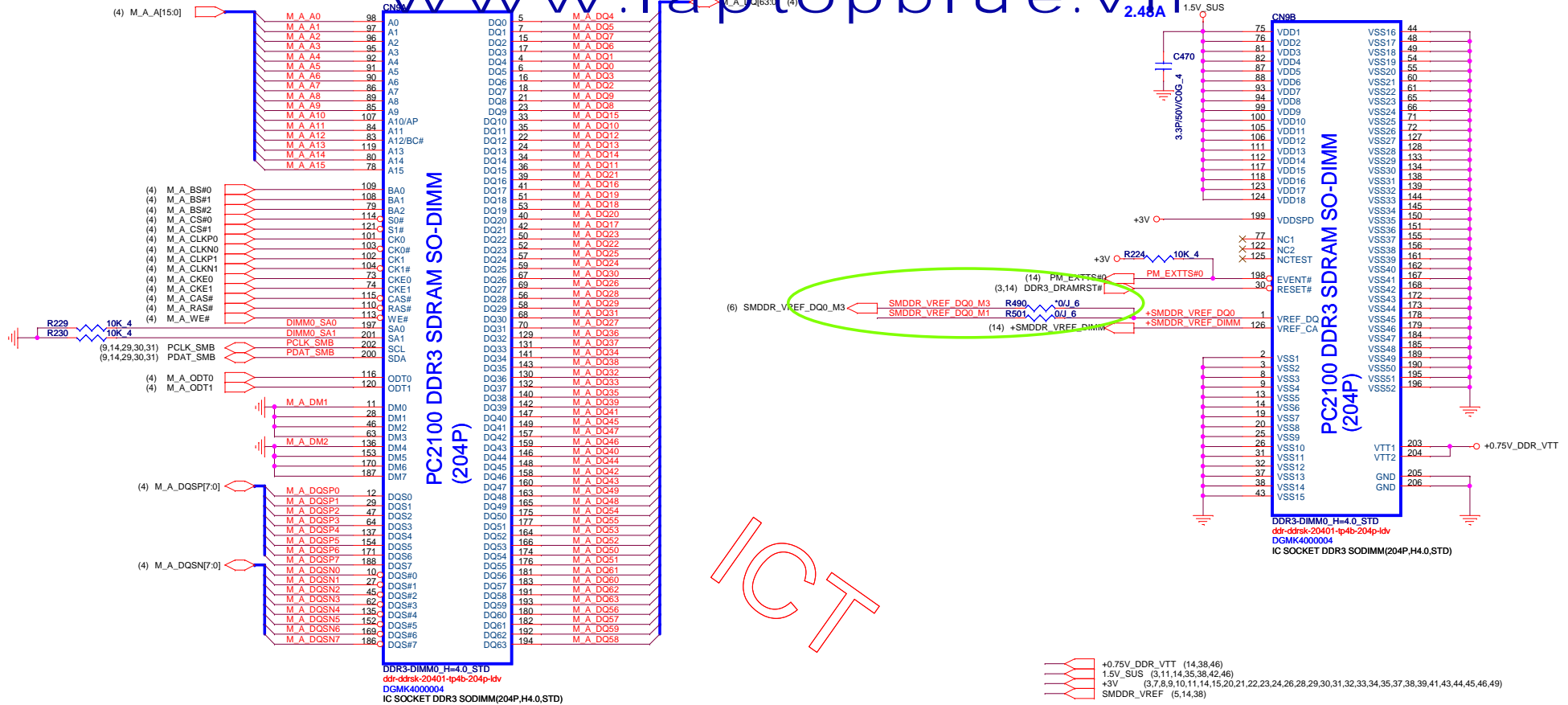
PCH 5/6 (POWER)

Size	Document Number	Rev
Date: Tuesday, March 13, 2012	Sheet 11 of 56	1A



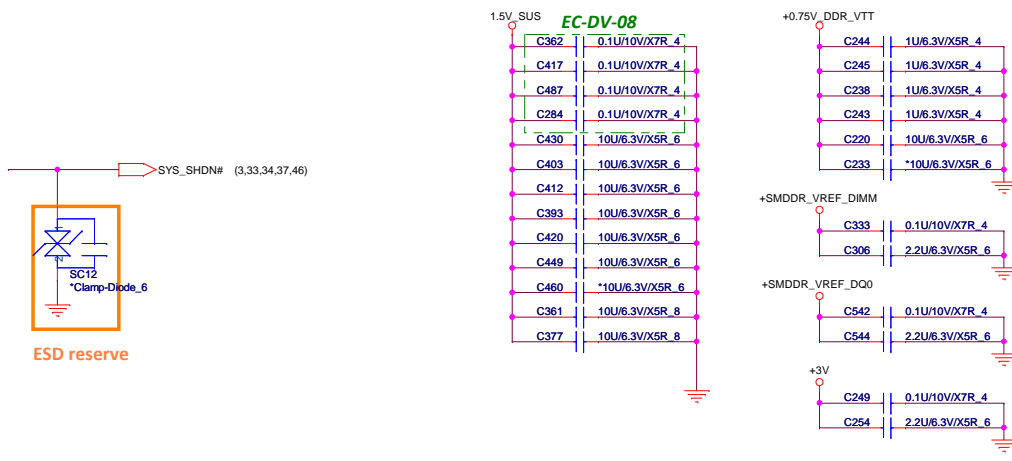
IC

Quanta Computer Inc.
 PROJECT : LV3D
 Size Document Number PCH 6/6 (GND) Rev 1A
 Date: Monday, March 12, 2012 Sheet 12 of 56

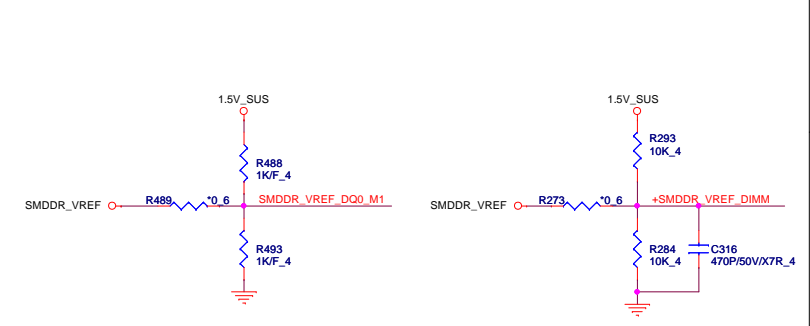


ICCT

Place these Caps near So-Dimm0.



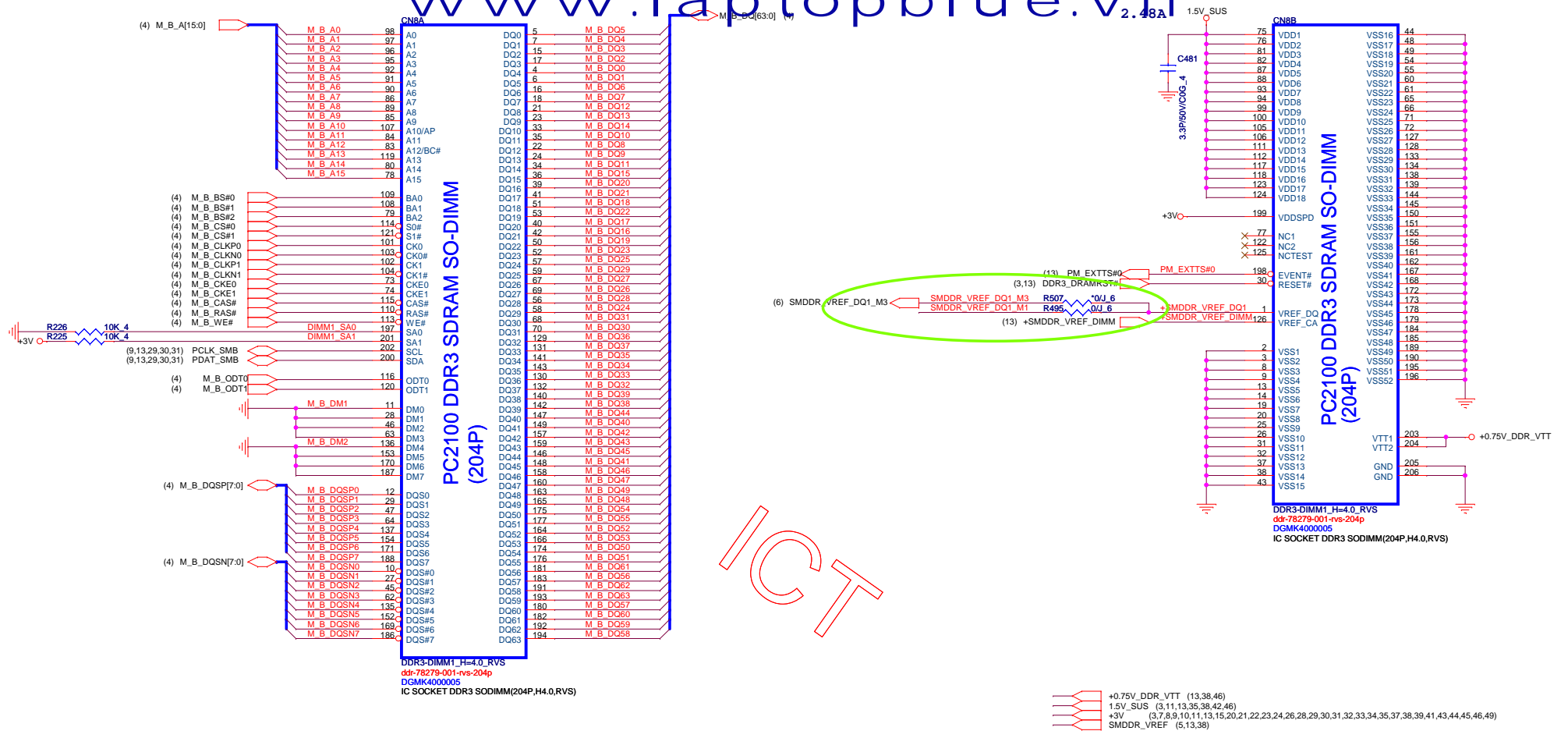
VREF DQ0 M1 Solution



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PROJECT : LV3D

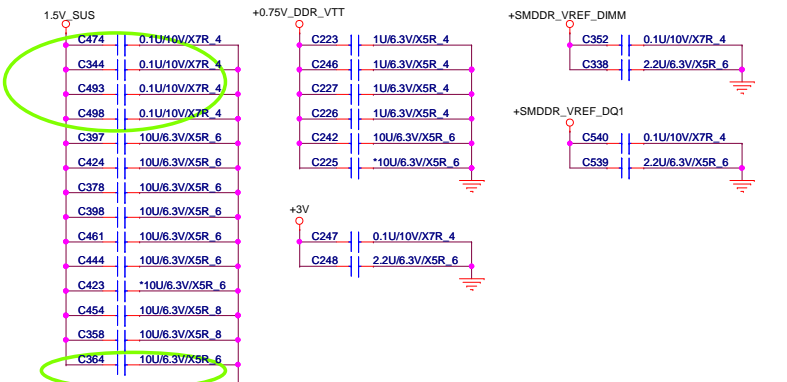
Size: Document Number: **DDR3 DIMM0-STD (5.2H)** Rev: 1A

Date: Monday, March 12, 2012 Sheet: 13 of 56

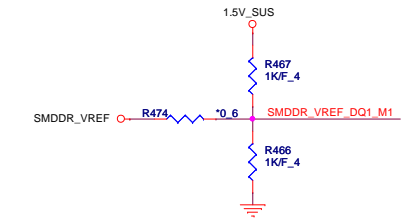


ICCT

Place these Caps near So-Dimm1.



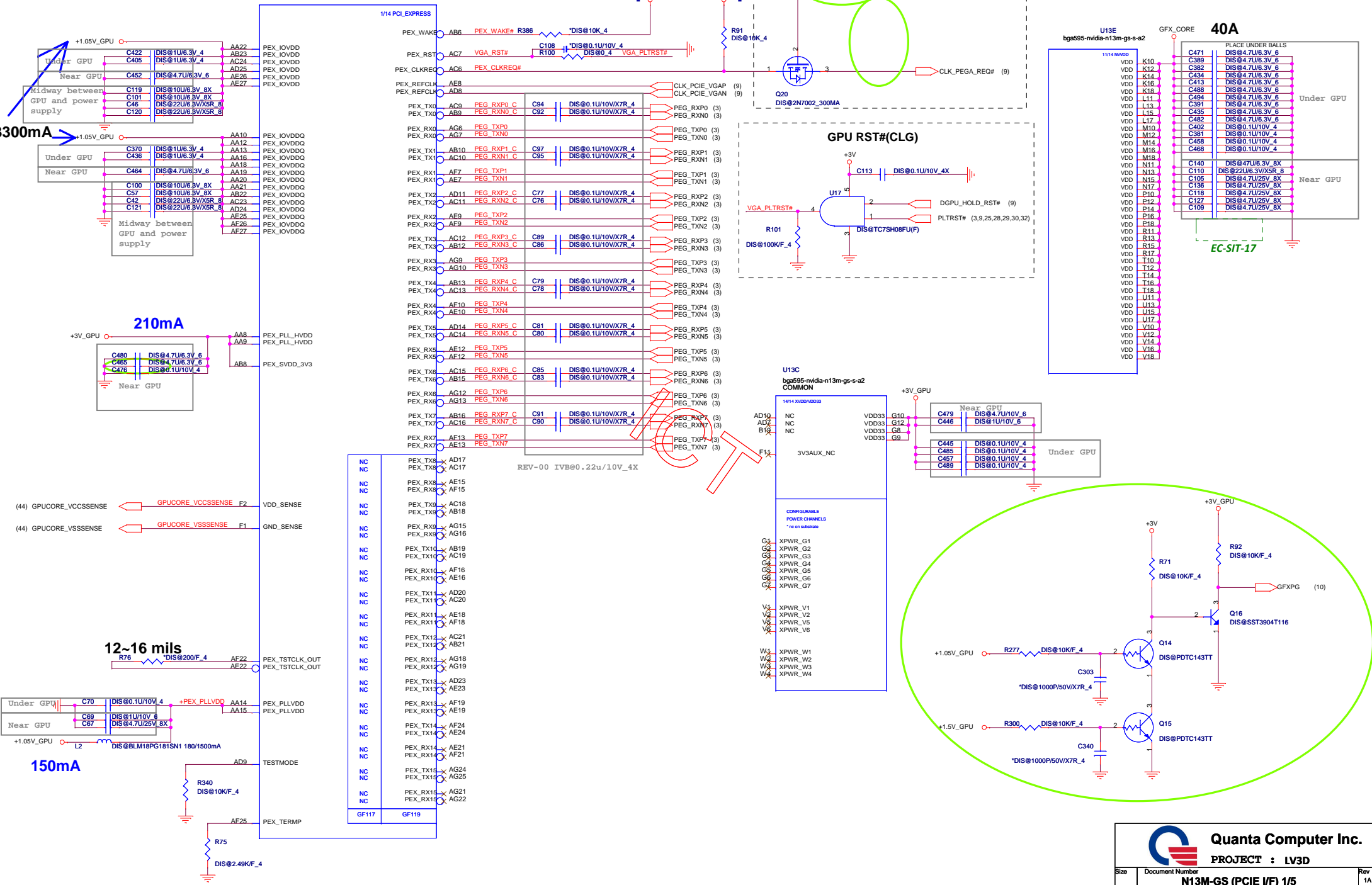
VREF DQ1 M1 Solution



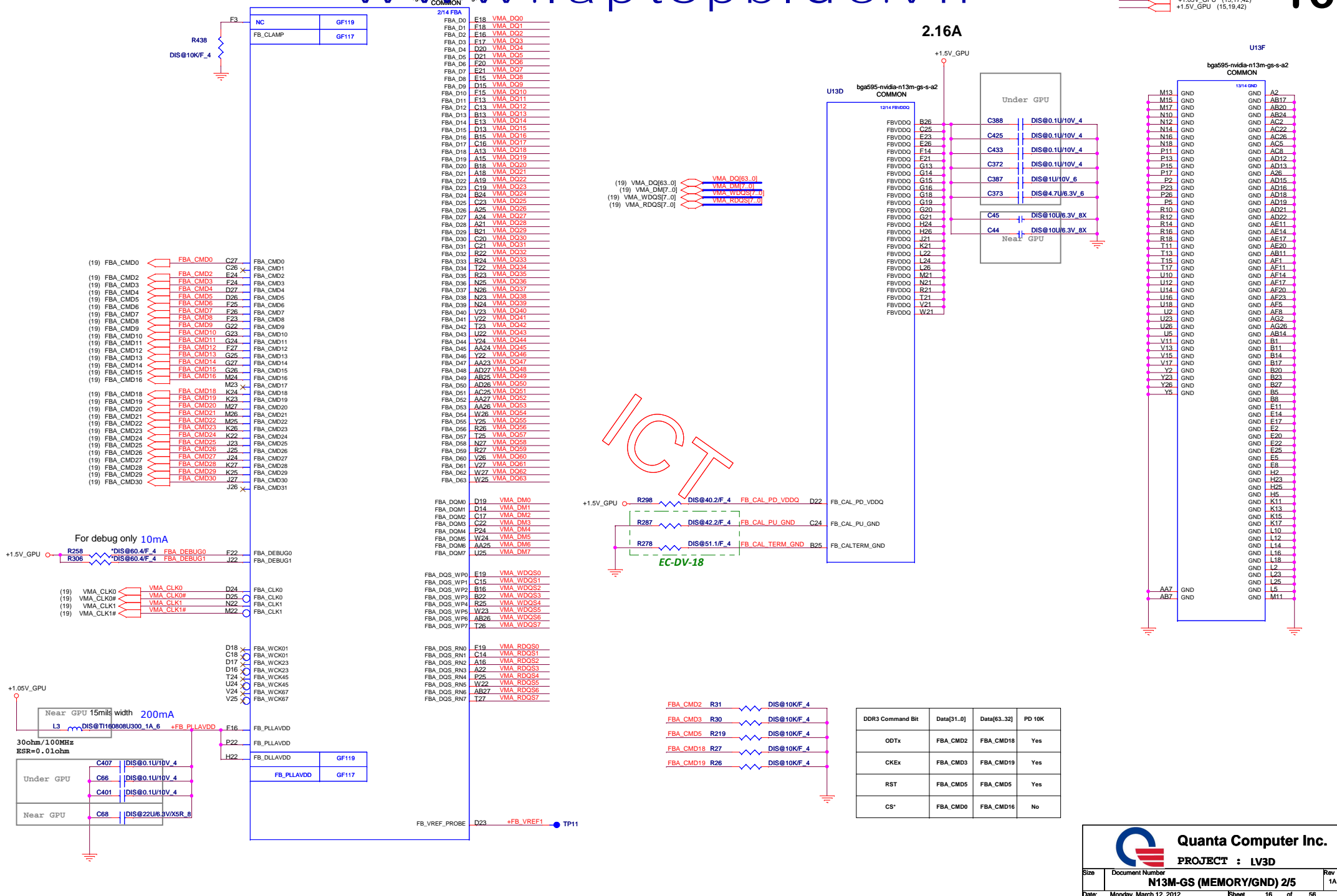
Quanta Computer Inc.
 PROJECT : LV3D

Size	Document Number	Rev
	DDR3 DIMM1-RVS (5.2H)	1A
Date:	Monday, March 12, 2012	Sheet 14 of 56

(17,18,43) +3V_GPU
(16,17,42) +1.05V_GPU
(44,46) GFX_CORE



+1.05V_GPU (15,17,42)
+1.5V_GPU (15,19,42)

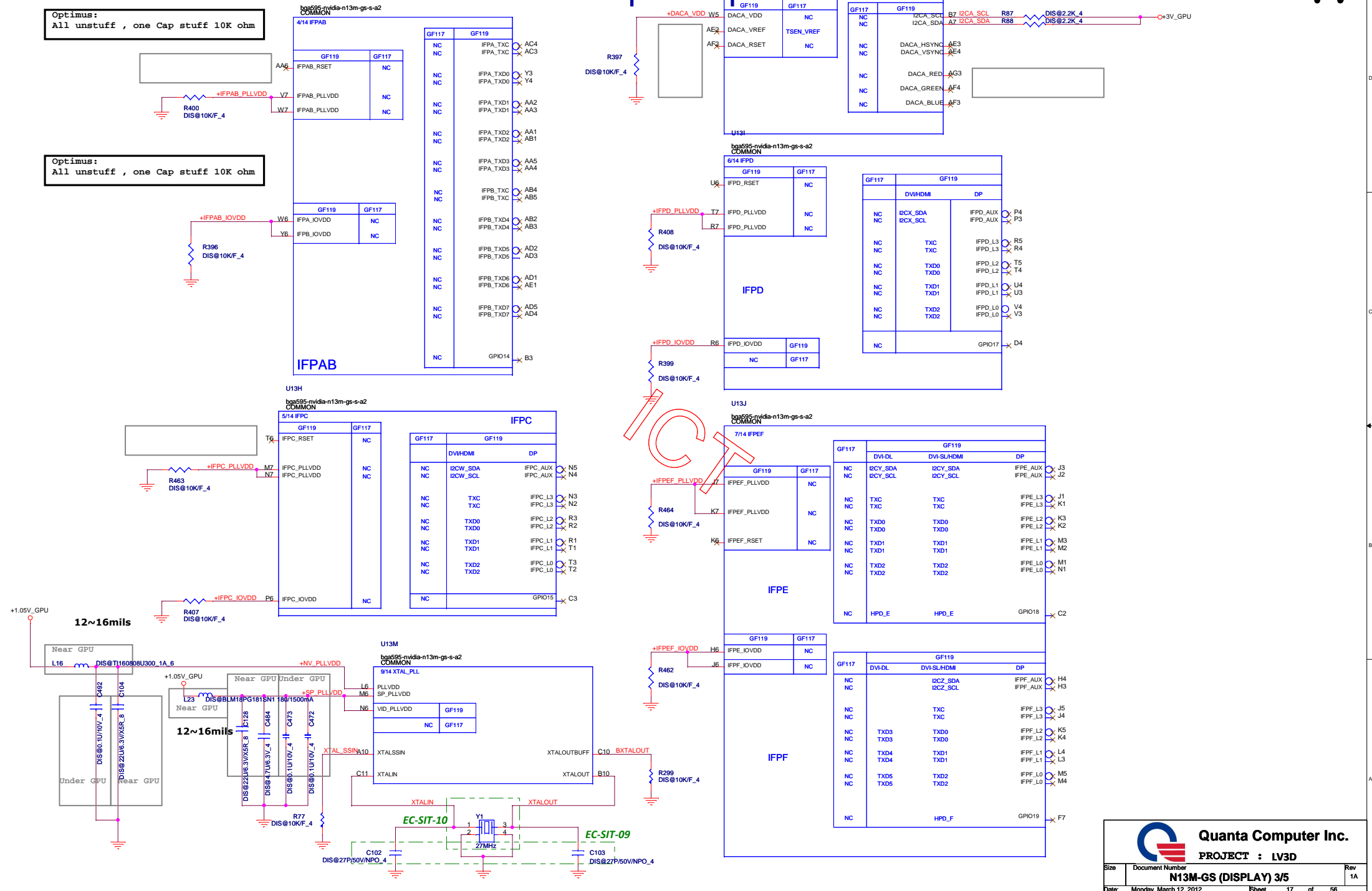


ICT

DDR3 Command Bit	Data[31..0]	Data[63..32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

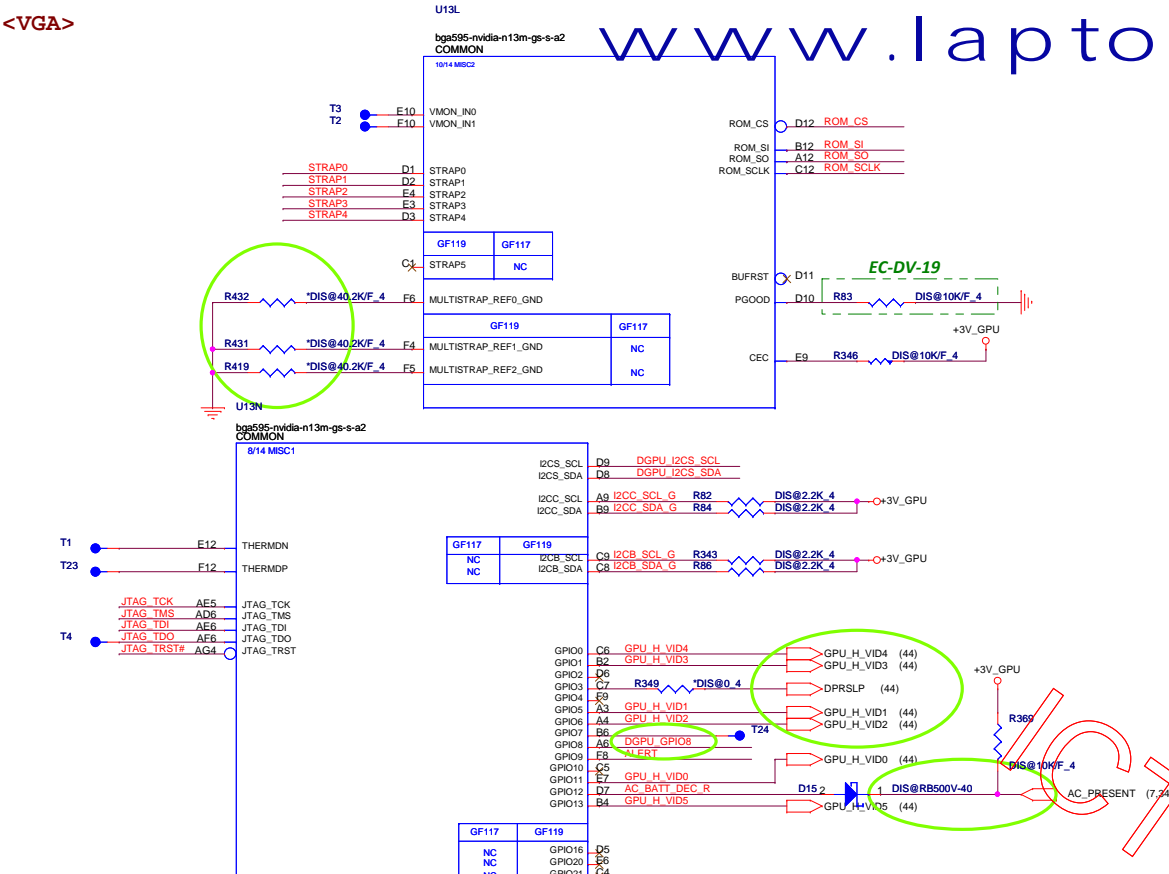
Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm



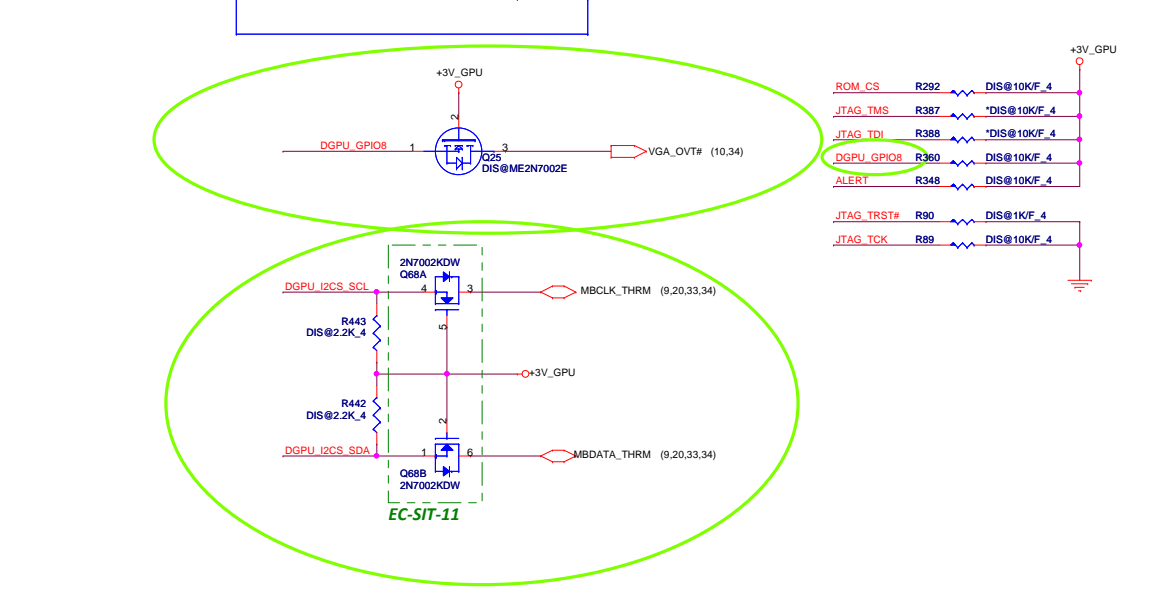
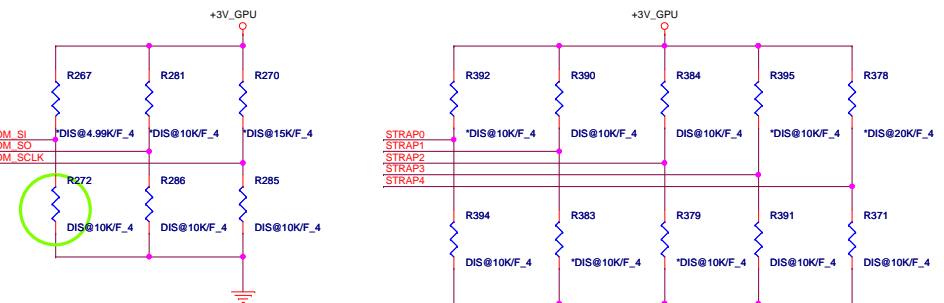
Quanta Computer Inc.
PROJECT : LV3D

Size	Document Number	Rev
	N13M-GS (DISPLAY) 3/5	1A
Date:	Monday, March 12, 2012	Sheet 17 of 56



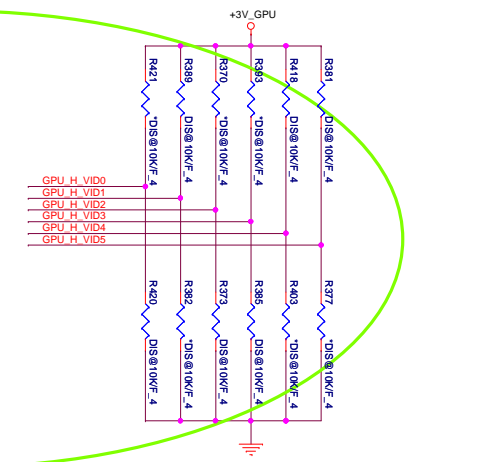
VRAM Configuration Table STRAP[0..3] "1": 10K pull high ; "0": 10K pull down

DESCRIPTION	Vendor	Vendor P/N	Strap0	Strap1	Strap2	Strap3
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Hynix	H5TQ2G63BFR-11C	0	1	1	0
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Samsung	K4W2G1646C-HC11	1	0	1	0
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Hynix	H5TQ2G63DFR-11C	0	0	1	1
DDR3 128Mx16x4pcs, 128bit, 1GB,900MHz	Samsung	K4W2G1646E-RC11				



NVDD Table

N13M-GS	NVDD (0.875V)
GPU_H_VID0	0 (R420)
GPU_H_VID1	1 (R389)
GPU_H_VID2	0 (R373)
GPU_H_VID3	0 (R385)
GPU_H_VID4	1 (R418)
GPU_H_VID5	1 (R381)



GPIO pin	Normal Function	I/O	Functional Description
GPIO0	GPU_VID4	0	GPU Core VDD VID4
GPIO1	GPU_VID3	0	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	0	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	0	Panel Power Enable
GPIO4	LCD_BLEH	0	Panel Backlight Enable
GPIO5	GPU_VID1	0	GPU Core VDD VID1
GPIO6	GPU_VID2	0	GPU Core VDD VID2
GPIO7	3D_VISION	0	3D Vision Left/Right signal
GPIO8	OVRT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_WRF_CTL	0	Memory WRF Control
GPIO11	GPU_VDD0	0	GPU Core VDD VID0
GPIO12	PWR_LEVEL	1	AC Power Detect Input, High/Low Battery
GPIO13	GPU_VID5	0	GPU Core VDD VID5
GPIO14	HPD_A	1	Hot Plug Detect for IFAH
GPIO15	HPD_C	1	Hot Plug Detect for IFPC
GPIO16	MEM_VDD_CTL	0	Memory VDD VID
GPIO17	HPD_D	1	Hot Plug Detect for IFD
GPIO18	HPD_E	1	Hot Plug Detect for IFPE
GPIO19	HPD_F	1	Hot Plug Detect for IFFF
GPIO20	Reserved		
GPIO21	Reserved		

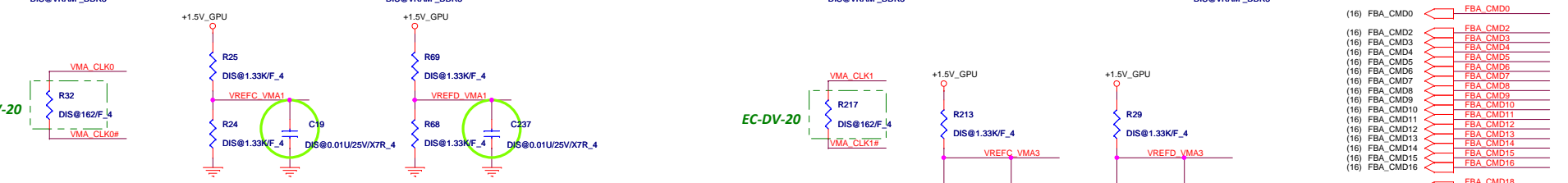
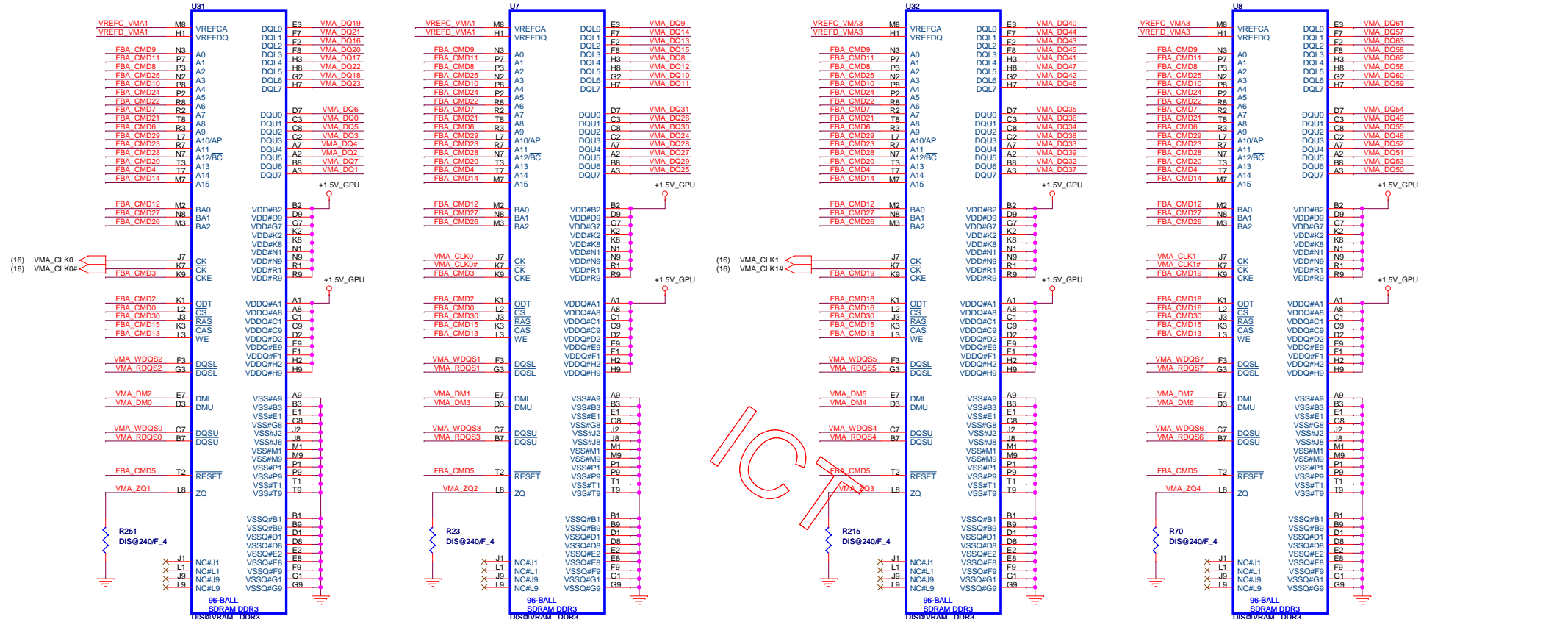
www.laptopblue.vn

CHANNEL A: 256MB/512MB DDR3

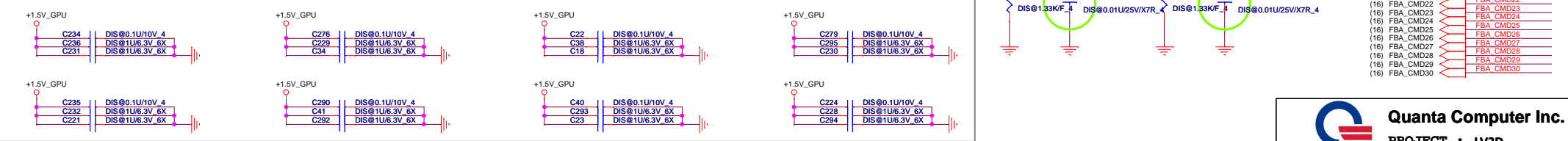
Double T Topology for DDR3 Memory

Hynix 64Mx16 P/N: H5TQ1G63DFR-11C
Hynix 128Mx16 P/N: H5TQ2G63BFR-11C
Samsung 64Mx16 P/N: K4W1G1646C-BC11
Samsung 128Mx16 P/N: K4W2G1646C-HC11

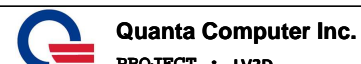
(16) VMA_DQ[63..0]
(16) VMA_DM[7..0]
(16) VMA_RDQS[7..0]
(16) VMA_RDOQS[7..0]



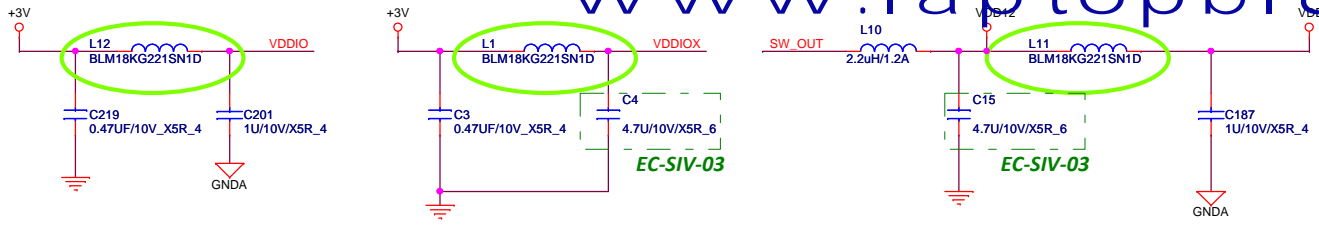
REV-00 change R3086 and R3091 from 240F_4 to 160 Ohms



- (16) FBA_CMD0
- (16) FBA_CMD2
- (16) FBA_CMD3
- (16) FBA_CMD4
- (16) FBA_CMD5
- (16) FBA_CMD6
- (16) FBA_CMD7
- (16) FBA_CMD8
- (16) FBA_CMD9
- (16) FBA_CMD10
- (16) FBA_CMD11
- (16) FBA_CMD12
- (16) FBA_CMD13
- (16) FBA_CMD14
- (16) FBA_CMD15
- (16) FBA_CMD16
- (16) FBA_CMD18
- (16) FBA_CMD19
- (16) FBA_CMD20
- (16) FBA_CMD21
- (16) FBA_CMD22
- (16) FBA_CMD23
- (16) FBA_CMD24
- (16) FBA_CMD25
- (16) FBA_CMD26
- (16) FBA_CMD27
- (16) FBA_CMD28
- (16) FBA_CMD29
- (16) FBA_CMD30

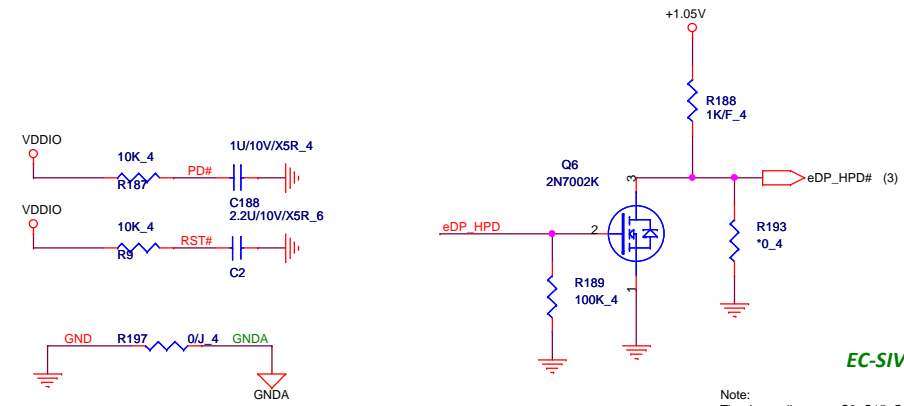


PROJECT : LV3D



Switching Regulator Layout Guideline

1. Place the switching regulator inductor (L3) close to SW_OUT pin (Pin13).
2. The SW_OUT output traces should be as wide as possible.
3. The GNDX pin (Pin14) should be connected to the main PCB ground plane, with the device GND pins of the PS8622 connected to separate GND island (GNDa) for the device. The GND island (GNDa) should be connected to the main GND plane (GND) with a single-point connection by use of a wide PCB trace.
4. Place the 4.7uF decoupling Capacitor (C4) for VDDIOX close to VDDIOX pin.
5. The GND of the 4.7uF capacitor (C4) for VDDIOX should be placed close to the GND of 4.7uF capacitor (C5) behind inductor.
6. Place the bead (L2) for VDDIOX close to PS8622.



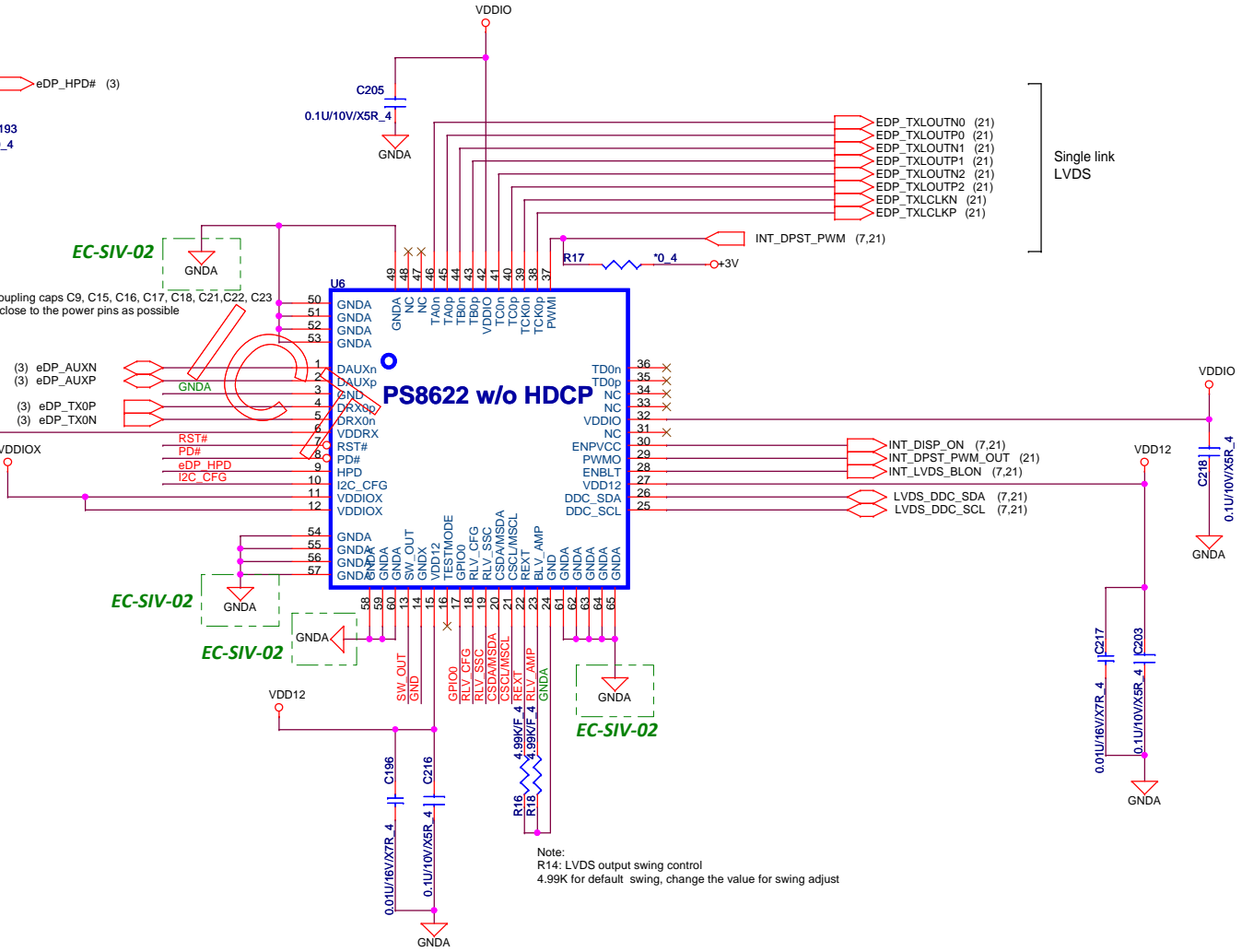
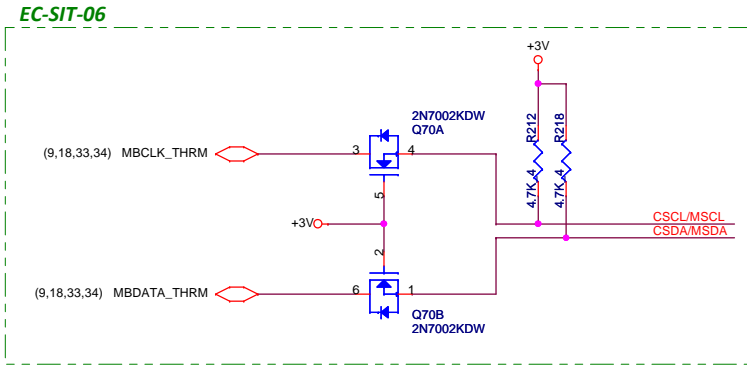
Note:
The decoupling caps C9, C15, C16, C17, C18, C21, C22, C23 shall be close to the power pins as possible

Power On Configuration

I2C_CFG: Initial code loading selection, internal pull-down ~80K
L: Reserved
M: No initial code loading, external I2C control is expected
H: Load initial code from external EEPROM through MSDL/MSDA

RLV_SSC: LVDS SSC selection, internal pull-down ~80K
L: SSC off
M: +/- 0.5% central spreading
H: +/- 1% central spreading

RLV_CFG: LVDS color depth and data mapping selection, internal pull-down ~80K
L: 8-bit LVDS, VESA mapping
M: 8-bit LVDS, JEIDA mapping
H: 6-bit LVDS, both VESA and JEIDA mapping



Note:
R14: LVDS output swing control
4.99K for default swing, change the value for swing adjust

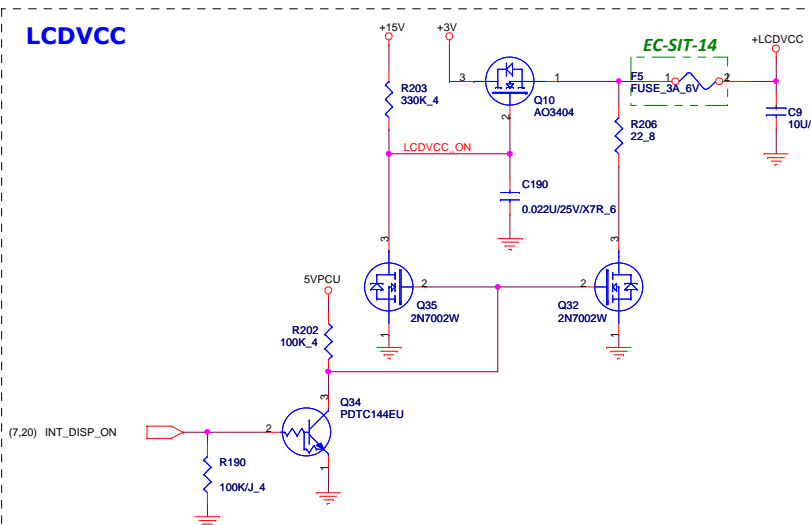
Single link
LVDS

Quanta Computer Inc.
PROJECT : LV3D

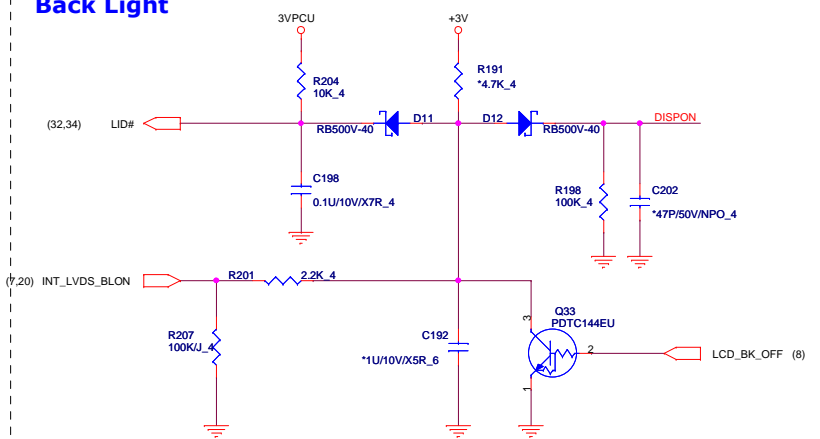
Size	Document Number	Rev
	PS8622 LVDS Converter	1A
Date:	Monday, March 12, 2012	Sheet 20 of 56

+3V	(3,7,8,9,10,11,13,14,15,20,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,41,42,44,45,46,48)
3VPCU	(8,25,28,32,34,36,37,39,40,46,48,49)
+15V	(30,32,37,38,42,43,46,48)
+5V	(7,8,11,22,23,24,26,31,32,33,45,46)
VIN	(35,36,37,38,39,41,44,45,46)
5VPCU	(8,36,37,38,39,40,41,42,43,44,46,48)

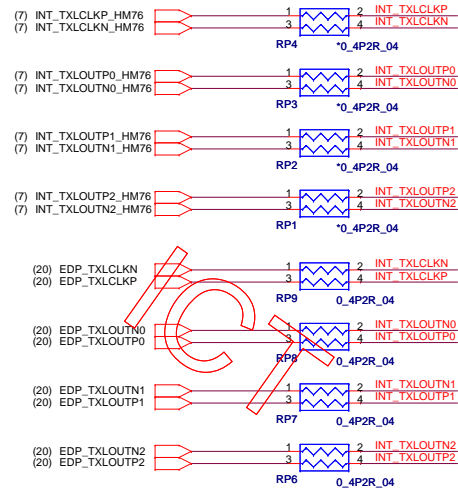
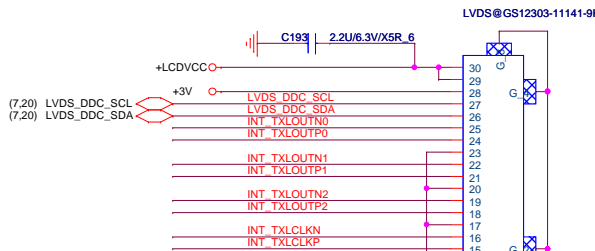
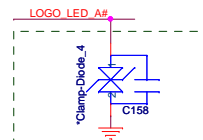
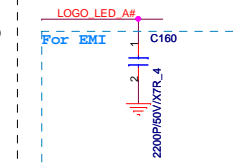
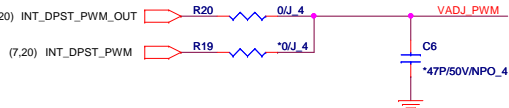
LCDVCC



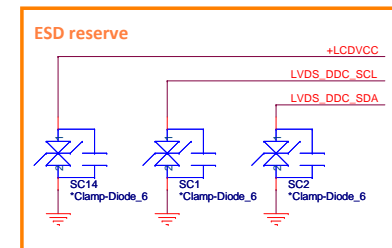
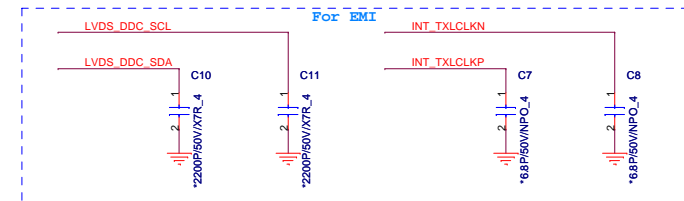
Back Light

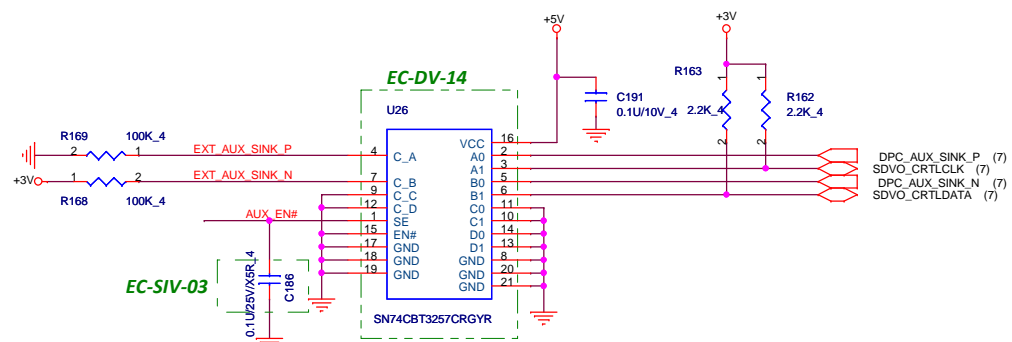


eDP converter HM76

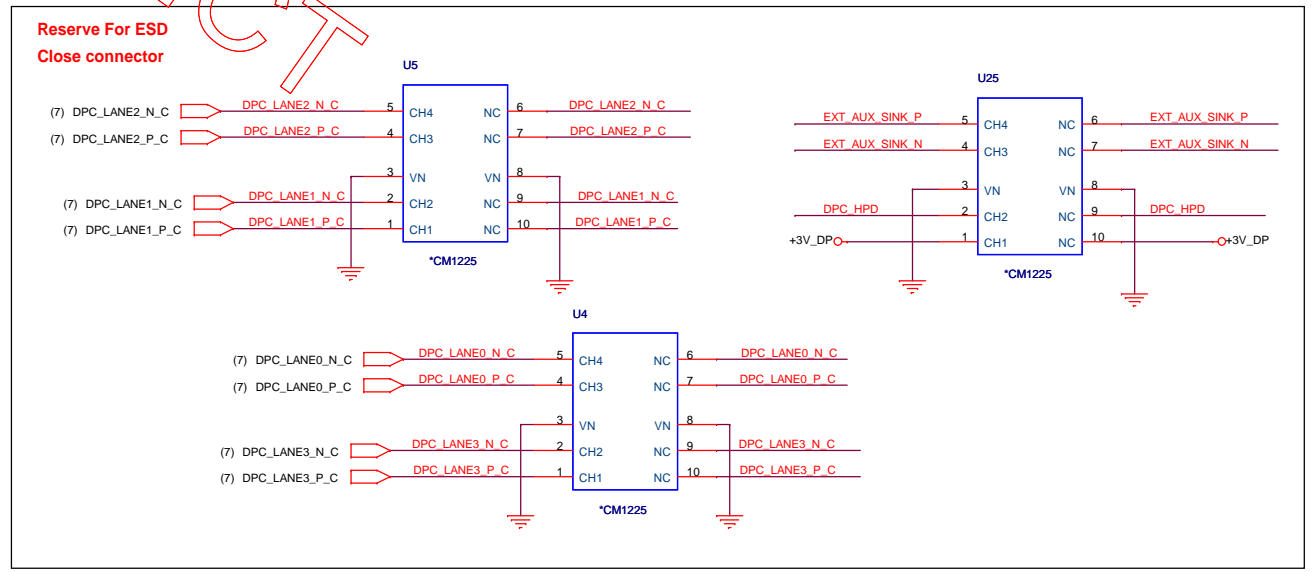
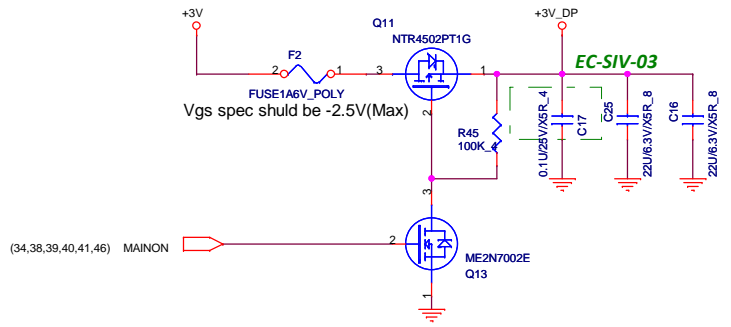
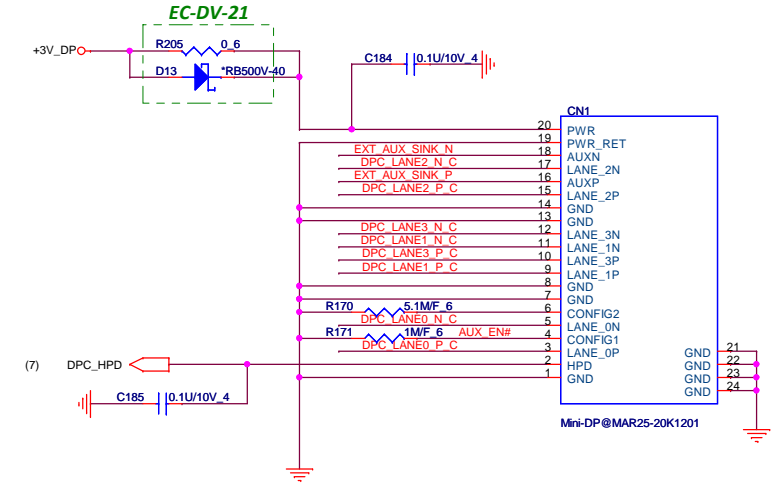


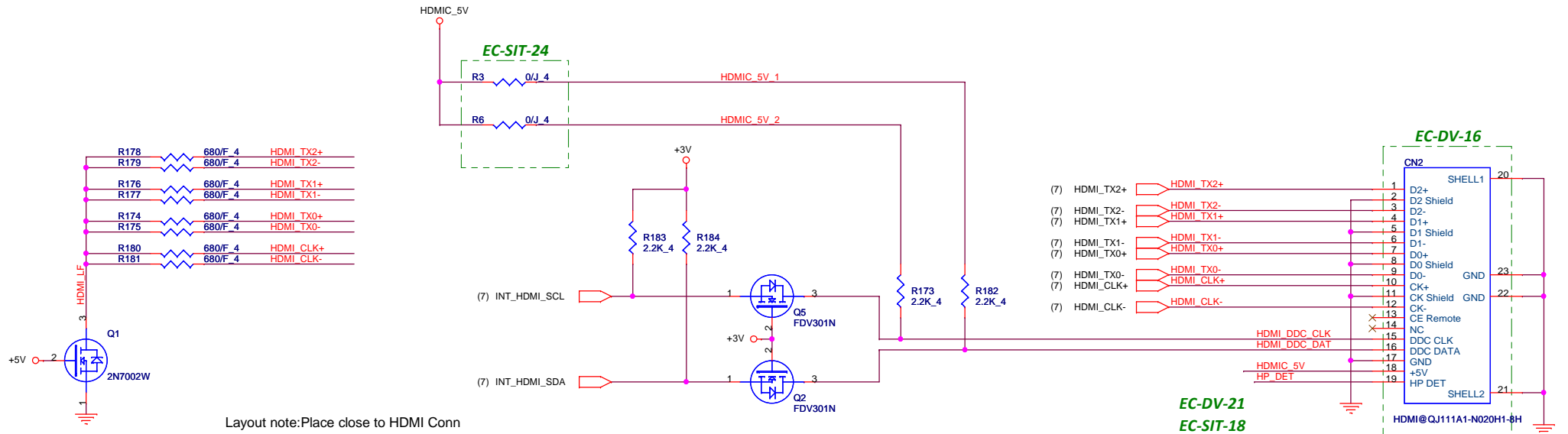
**LVDS (11.6")
(1024x600,
1366x768)**



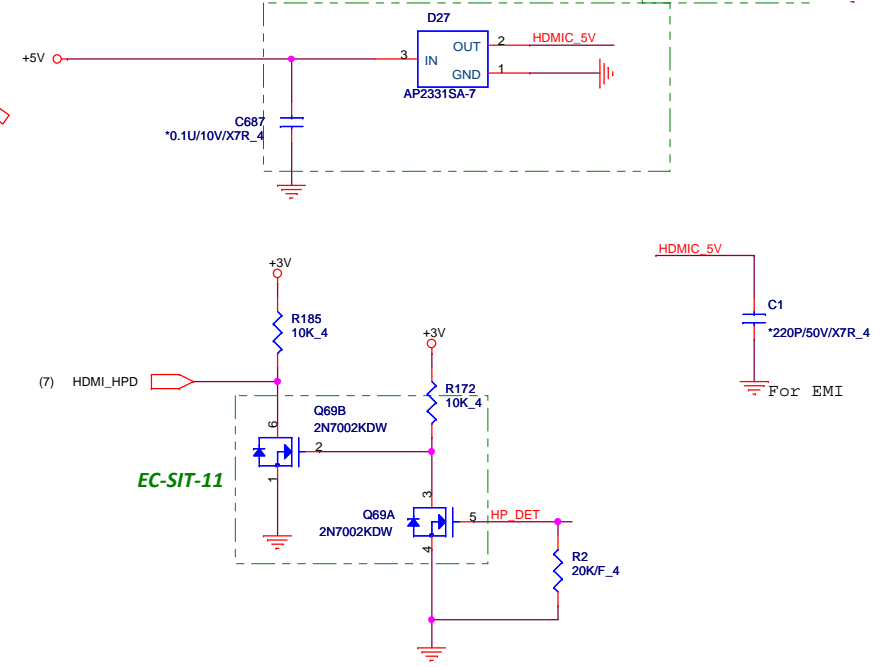
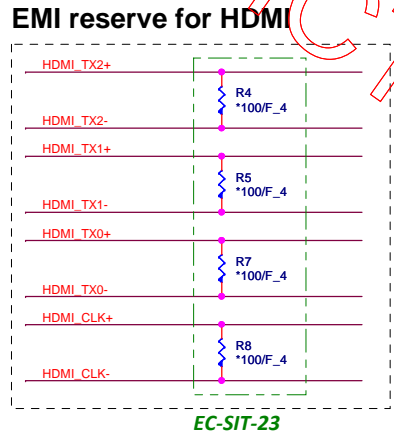
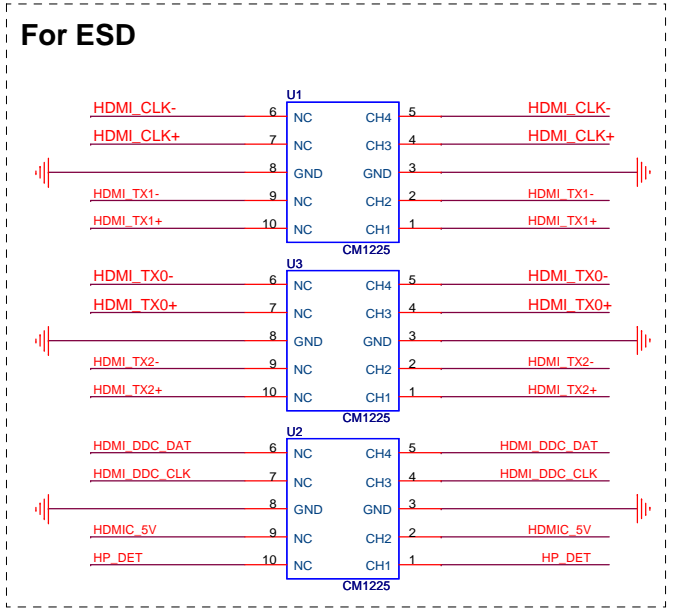


Low : Display port (Default)
High : Dongle attache(convert to DVI)



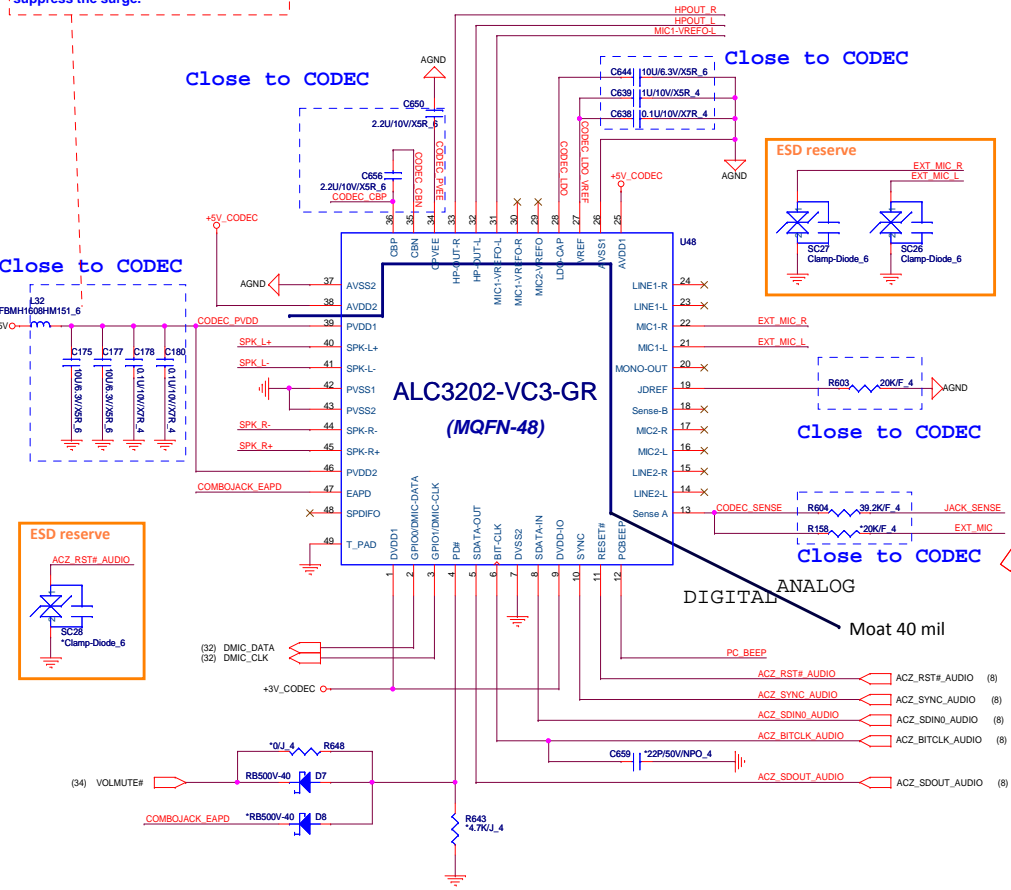
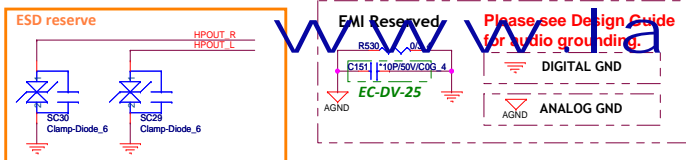


Layout note: Place close to HDMI Conn



CODEC(ADO)

<<Attention>>
 Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

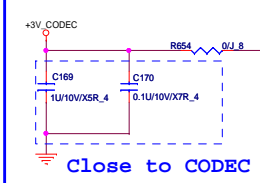


Codec Power(ADO)

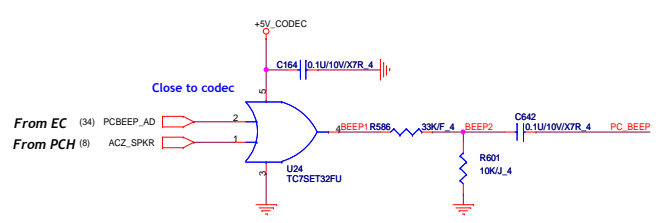


HDA Power(ADO)

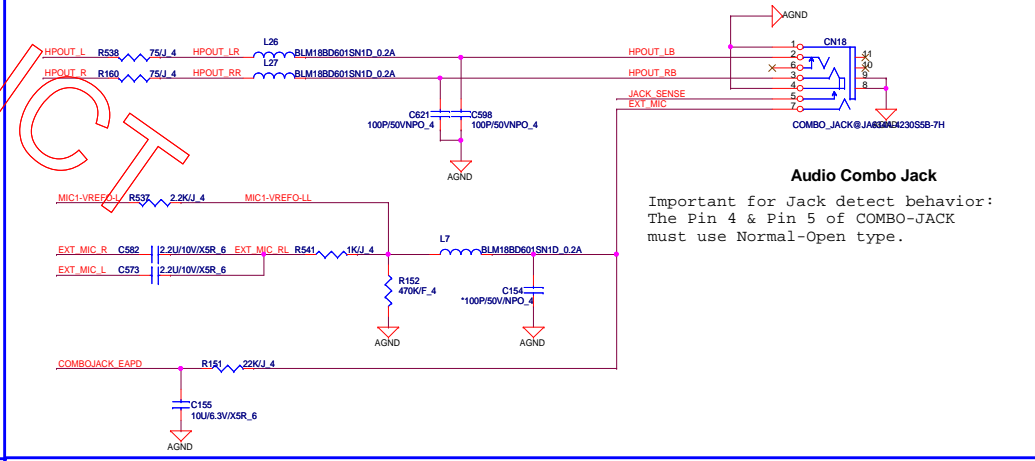
*Intel HDA Either +1.5V_S5 or +3V_S5



PC BEEP



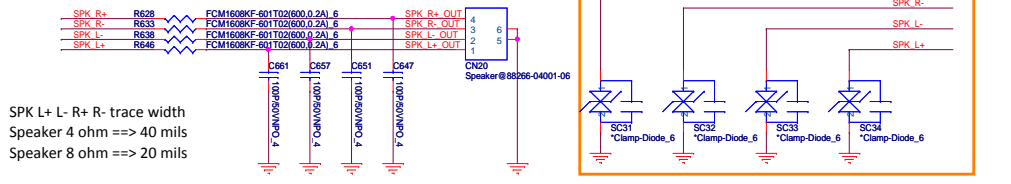
External MIC/Headphone Combo



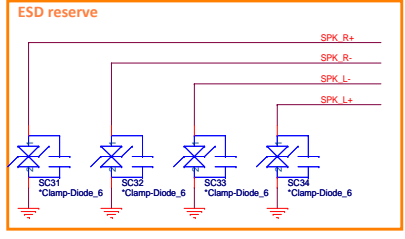
Audio Combo Jack
 Important for Jack detect behavior:
 The Pin 4 & Pin 5 of COMBO-JACK must use Normal-Open type.

Internal Speaker

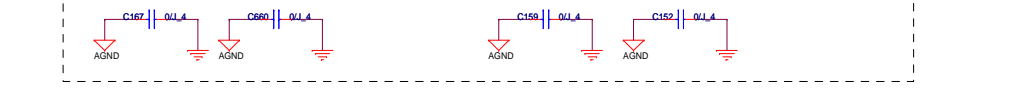
<<Attention>>
 Place there EMI components next to codec; For EMI issue, please also refer our ALC269 Layout guide document



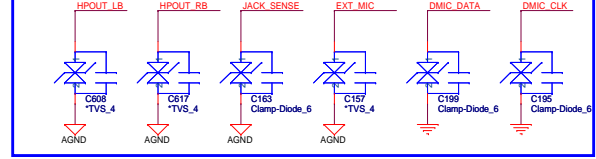
SPK L+ L- R+ R- trace width
 Speaker 4 ohm => 40 mils
 Speaker 8 ohm => 20 mils



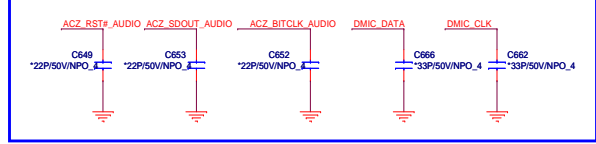
EMI Reserve

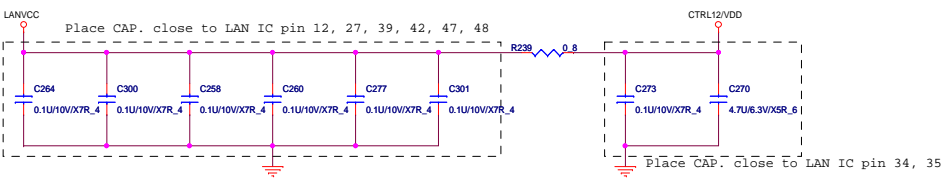
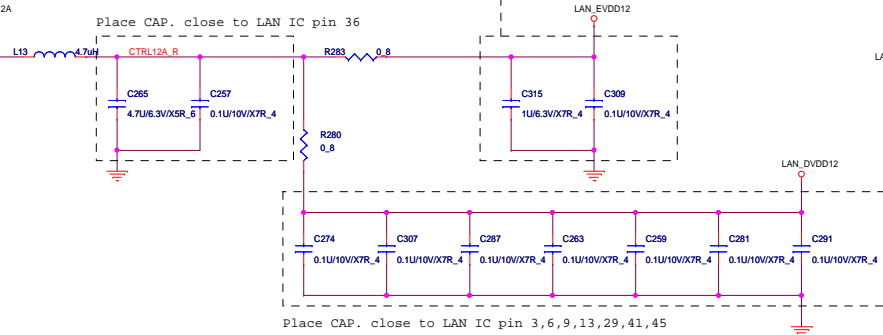
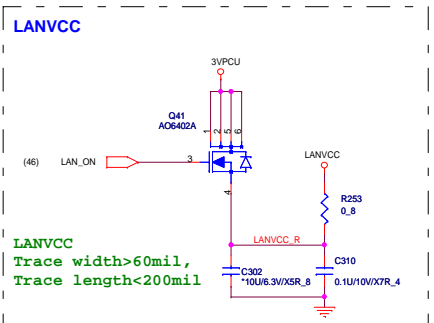


ESD Reserve

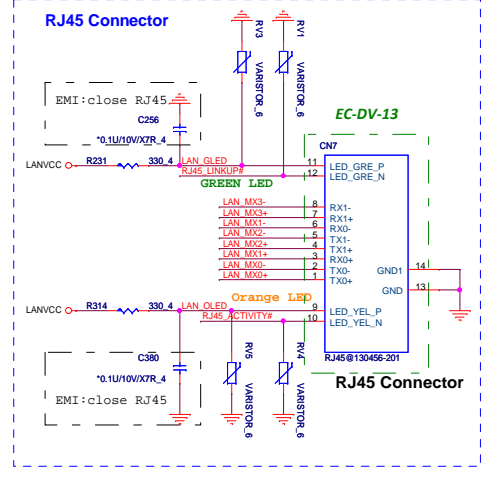
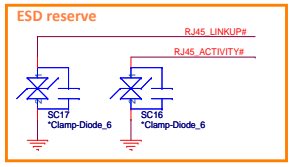
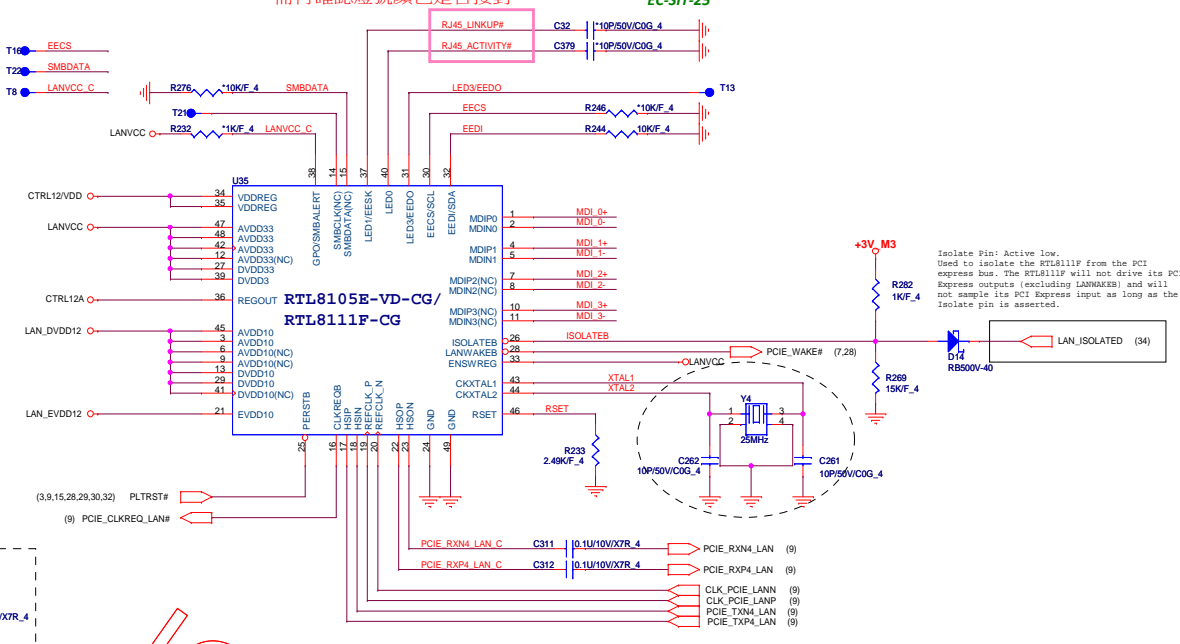
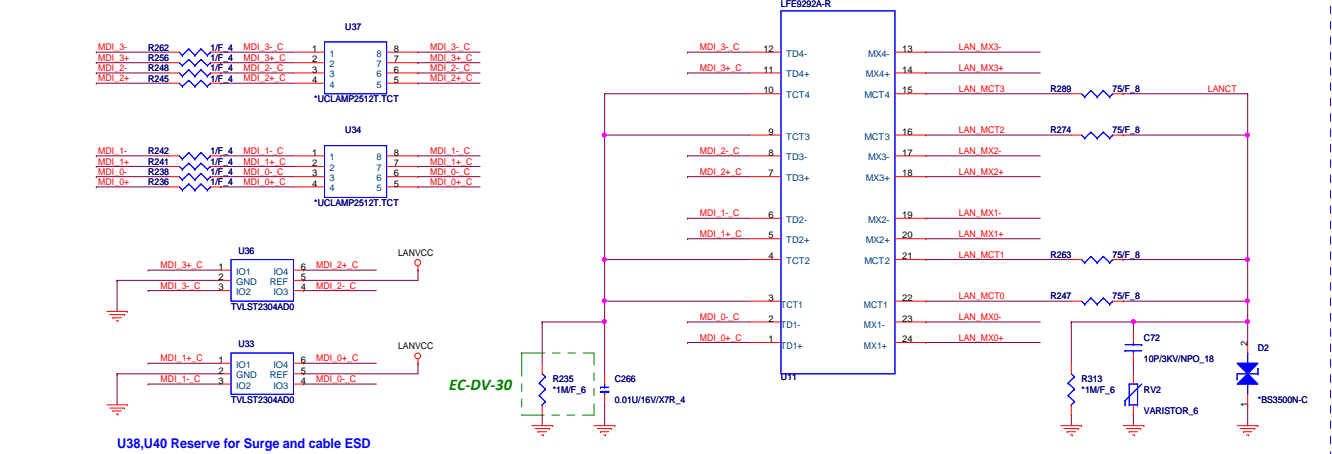


FOR EMI Reserve

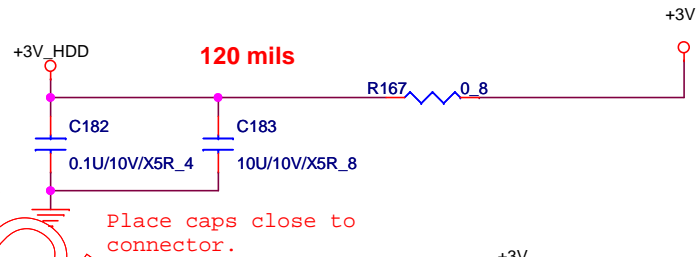
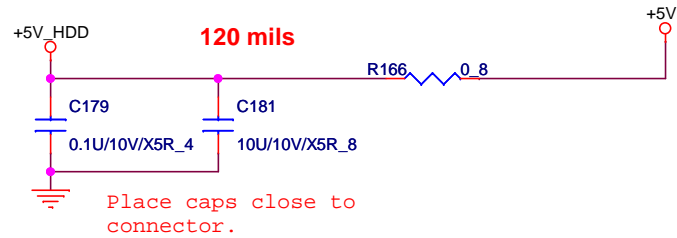
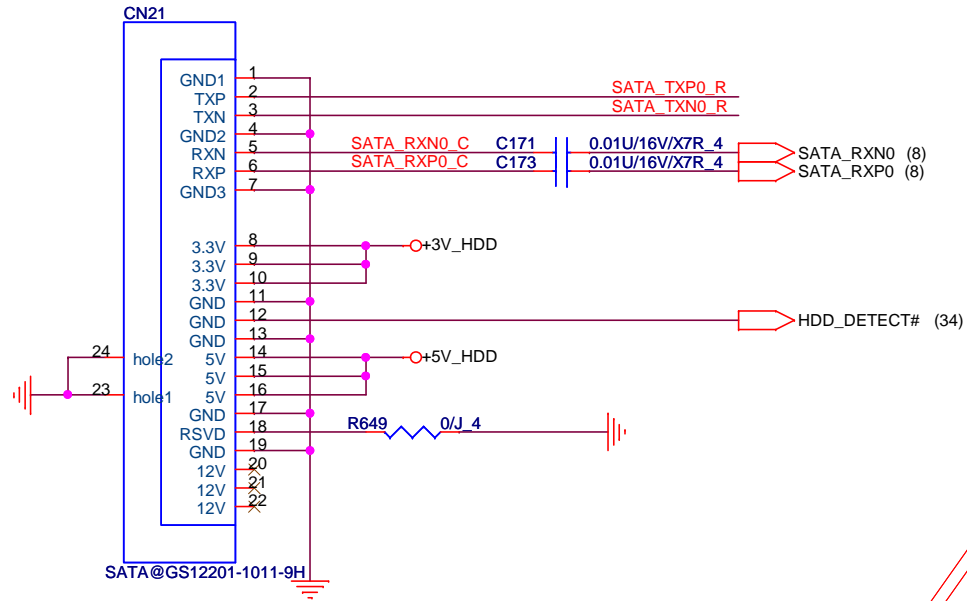




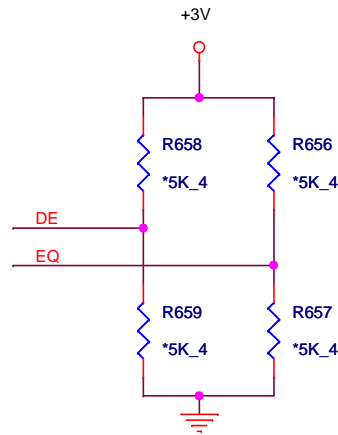
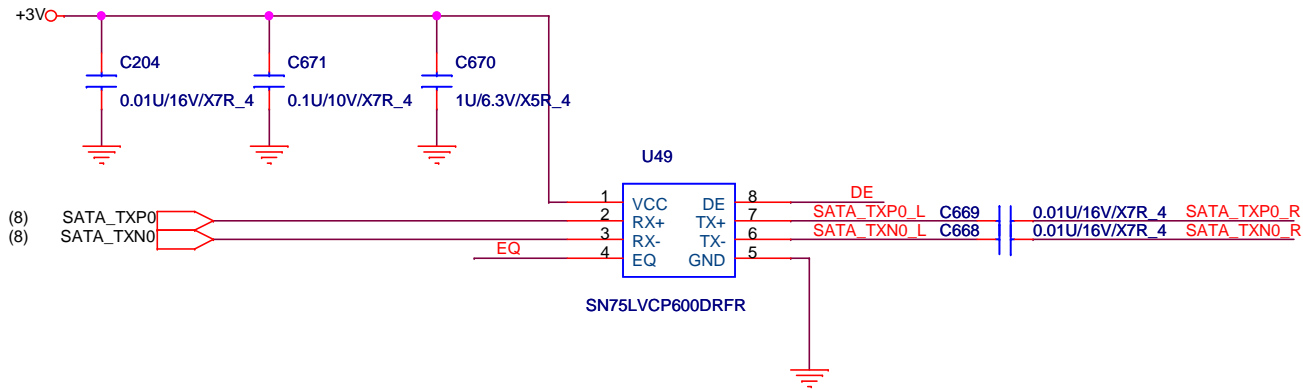
Transformer




SATA Connector

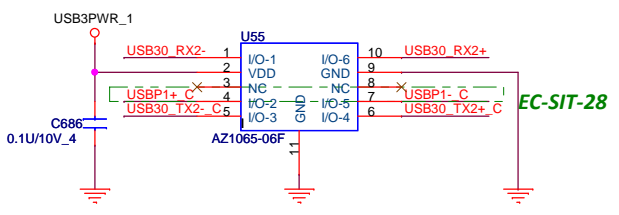
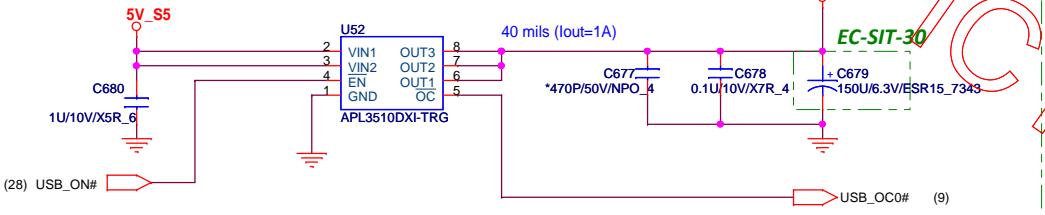
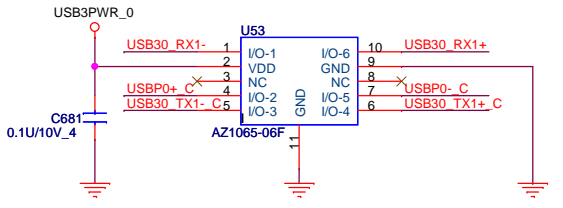
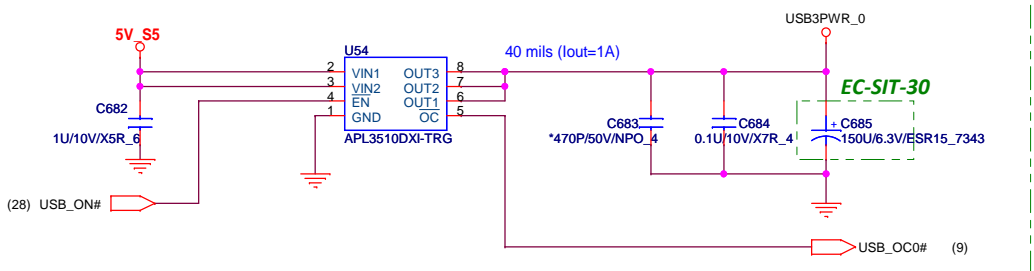


SATA Re-driver

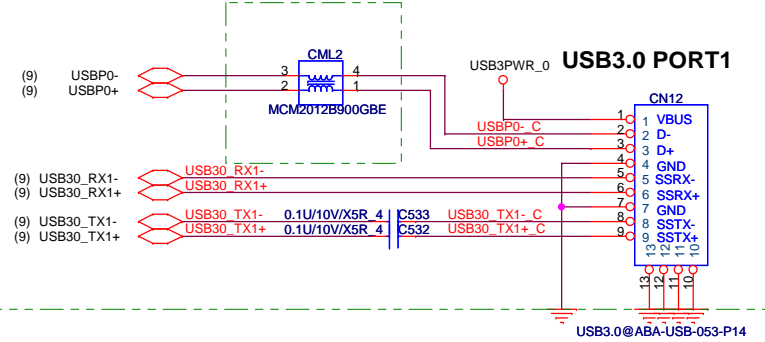


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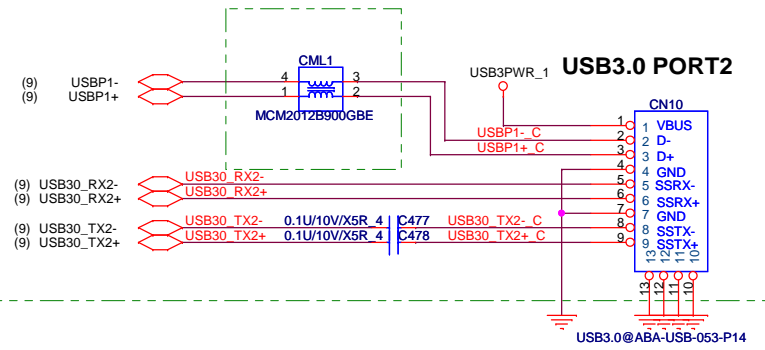
EC-SIT-22



EC-SIT-27



EC-SIT-22

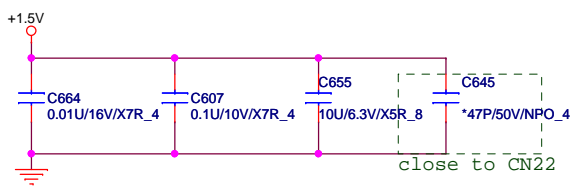
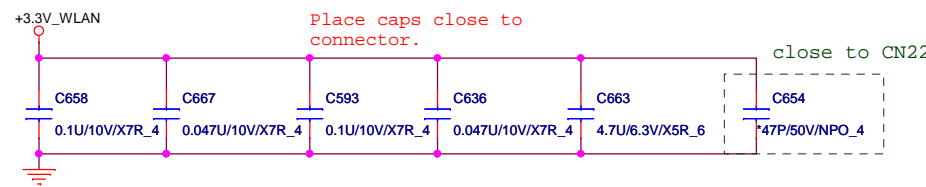
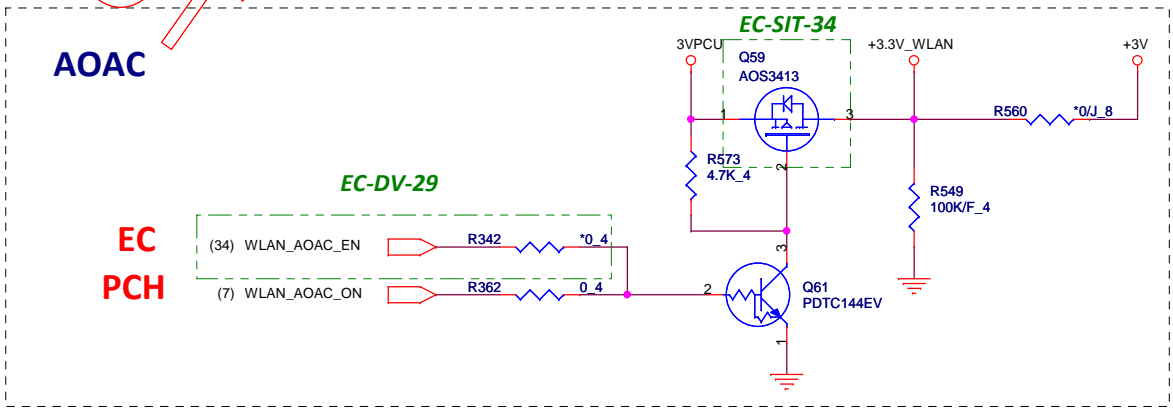
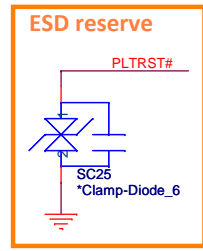
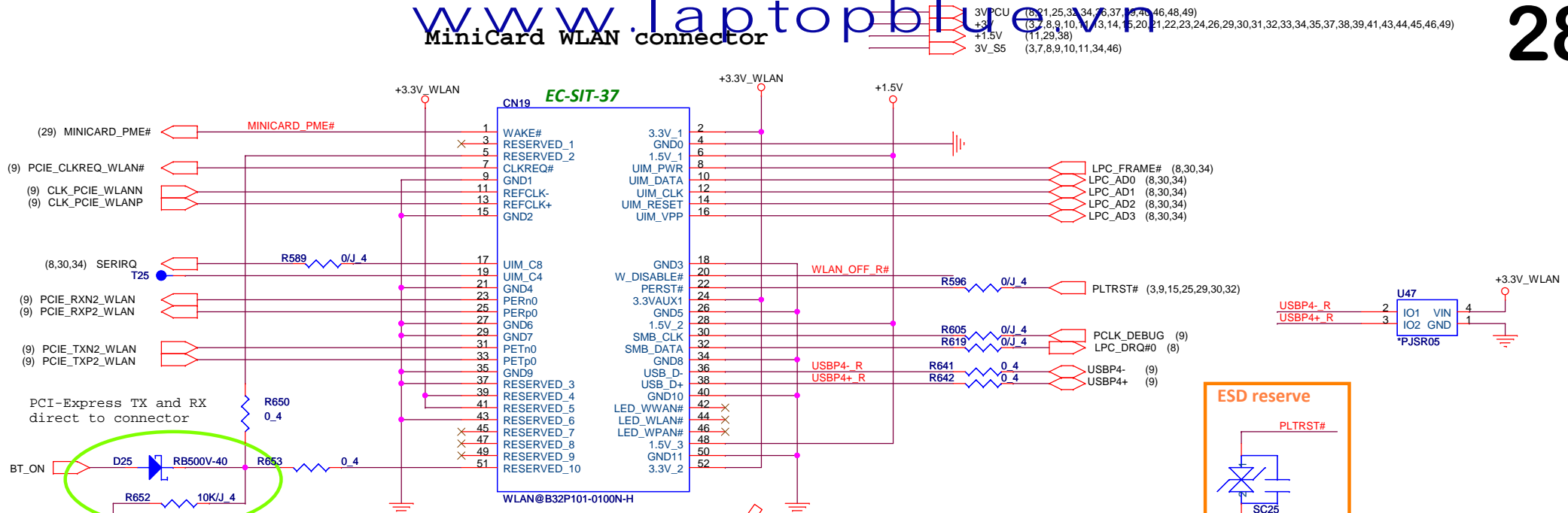


EC-SIT-27



Quanta Computer Inc.
 PROJECT : LV3D

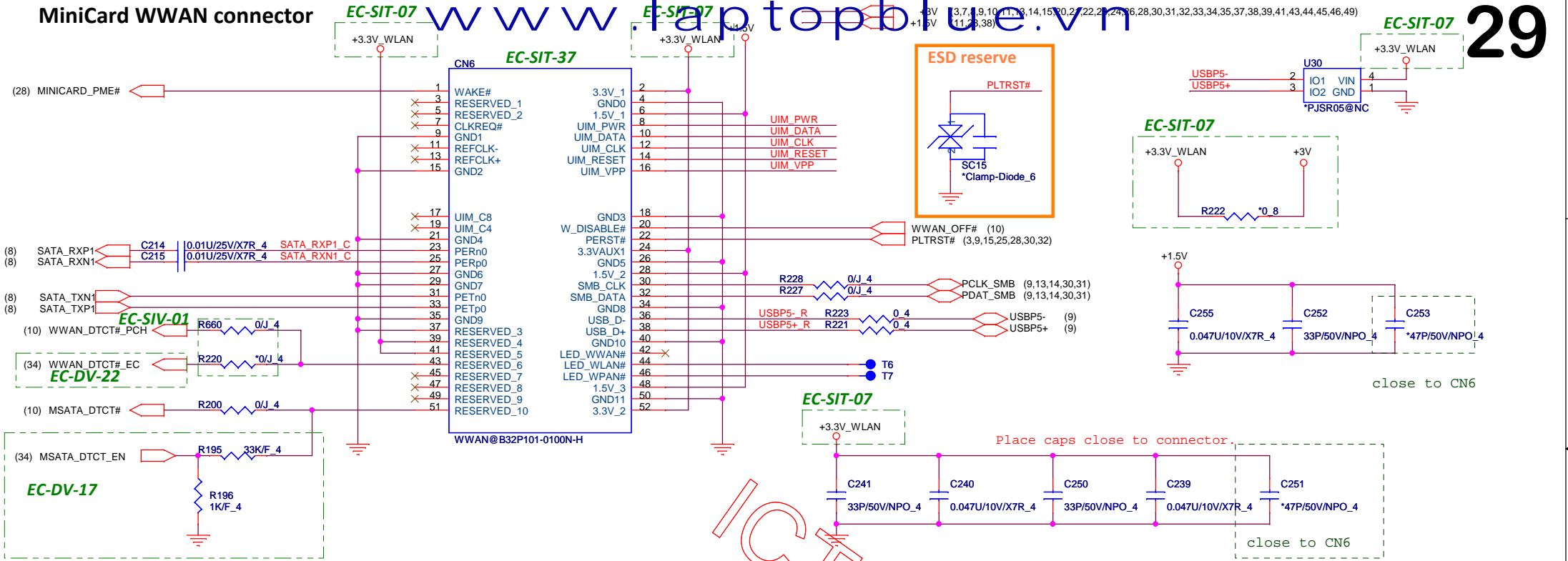
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WLAN/BT

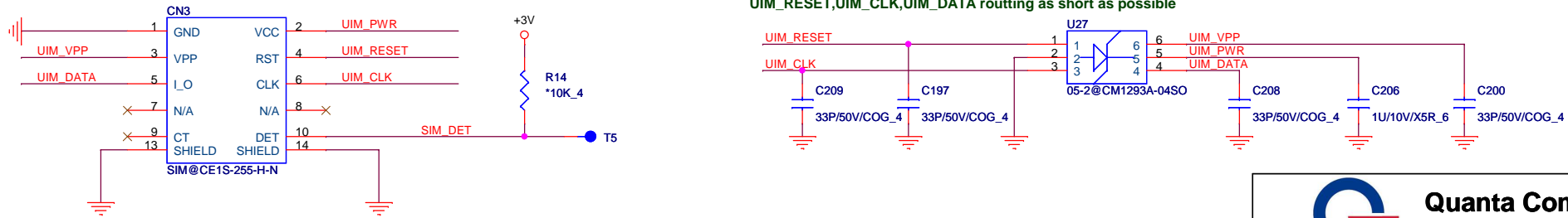
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MiniCard WWAN connector



SIM Card CONN

Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routing as short as possible

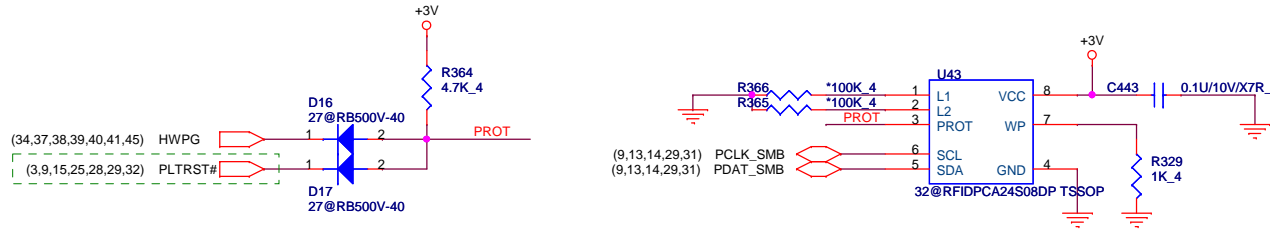


Quanta Computer Inc.

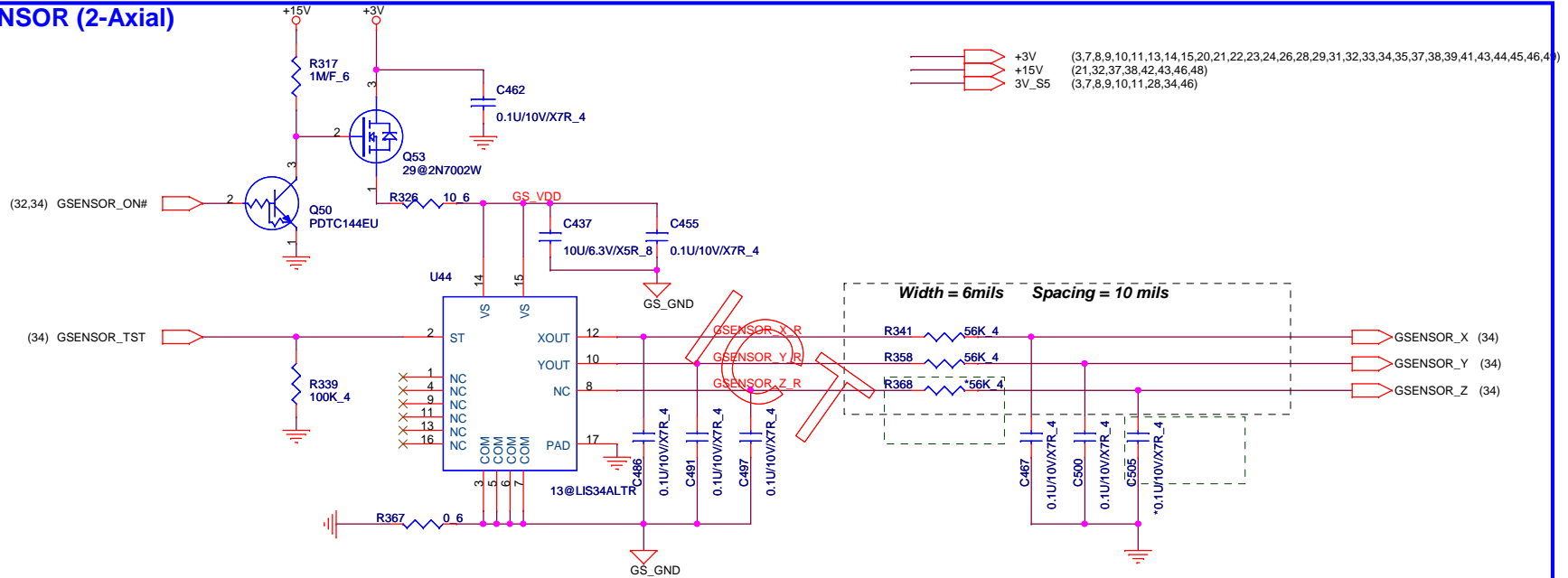
PROJECT : LV3D

WWAN(SSD)

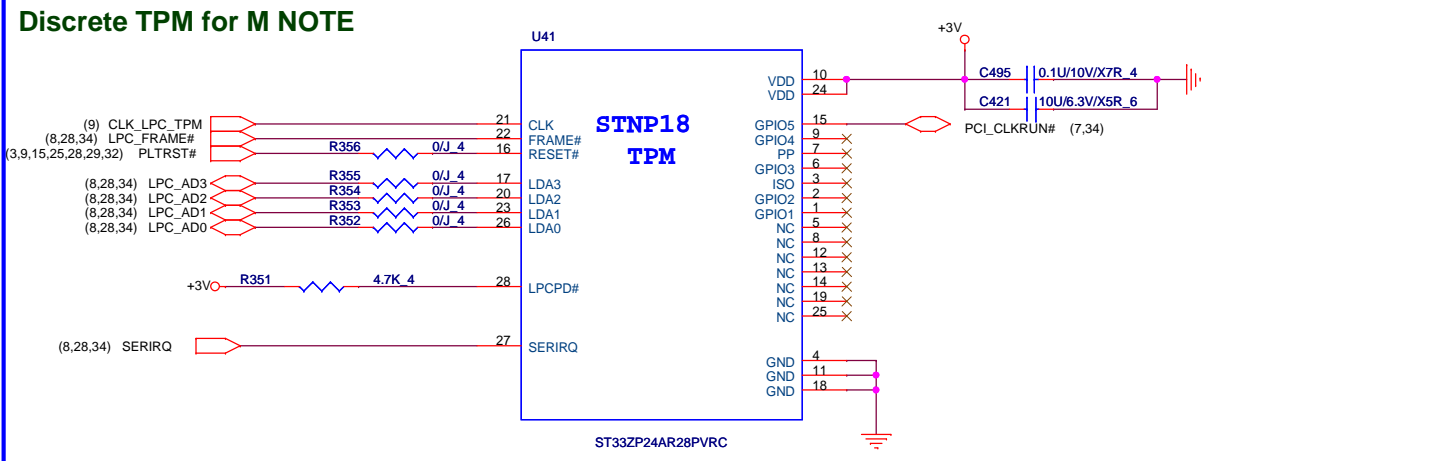
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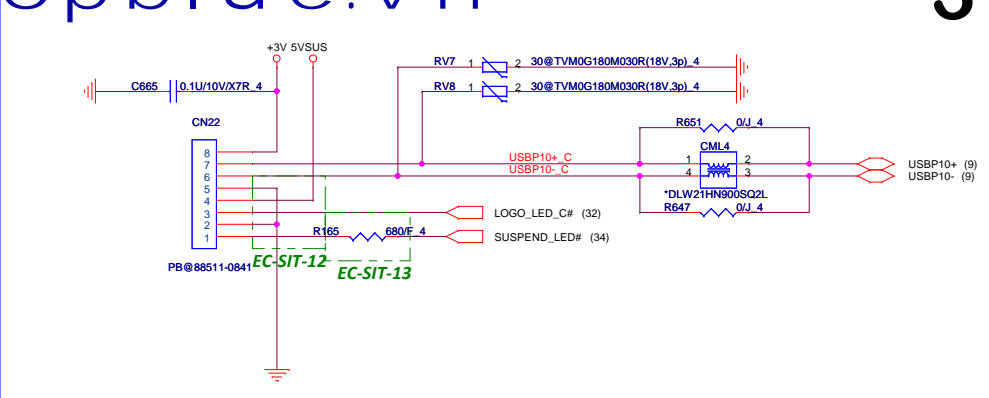
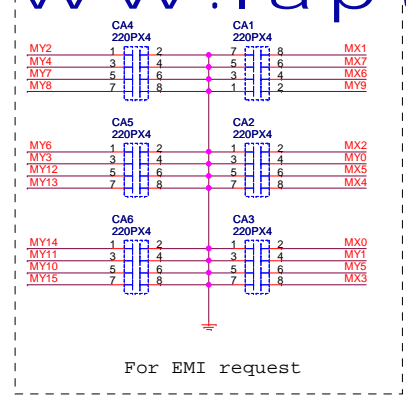
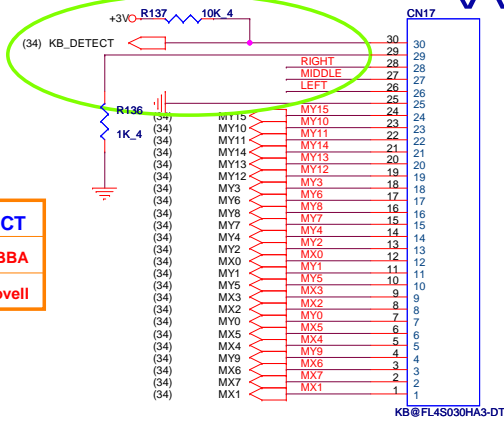
G-SENSOR (2-Axial)



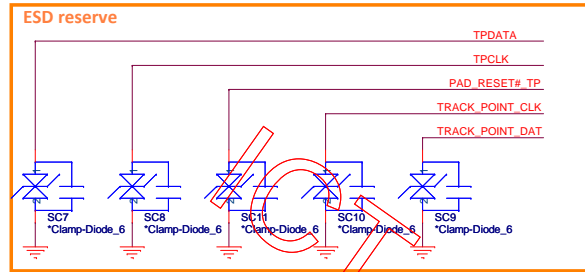
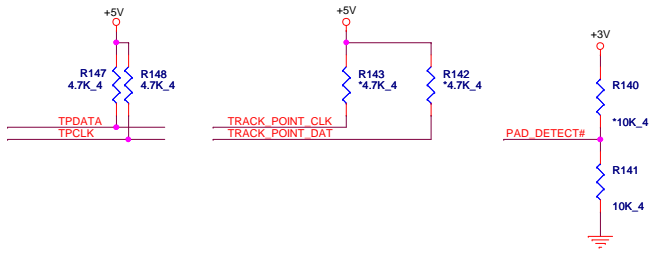
Discrete TPM for M NOTE



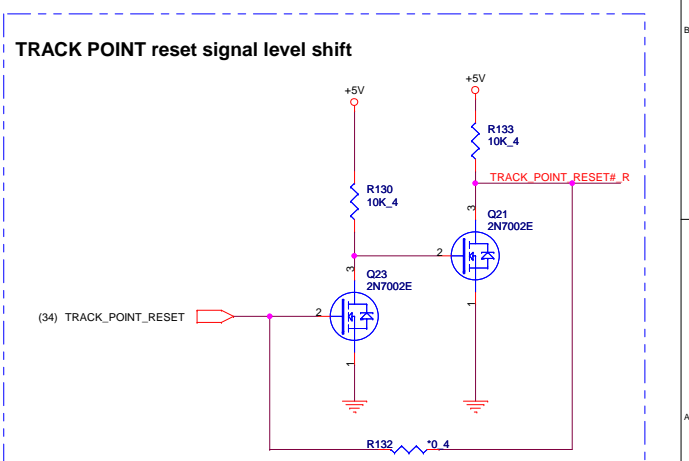
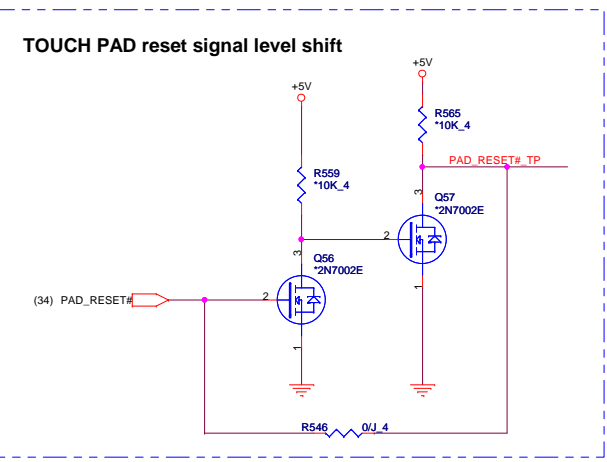
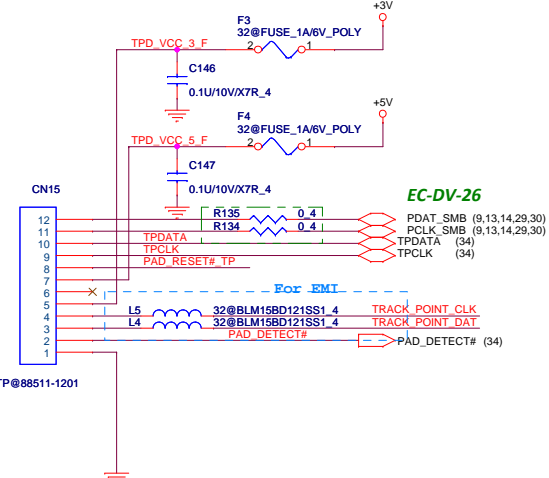
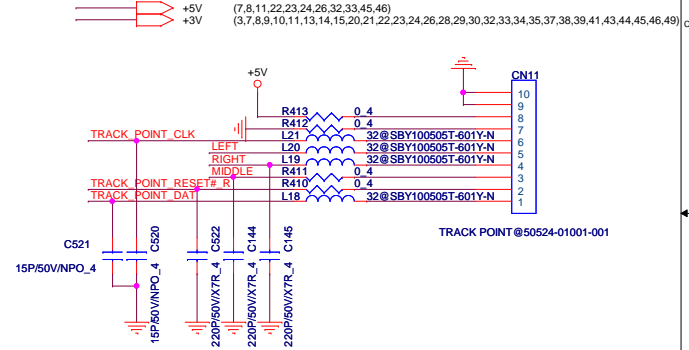
KB_DETECT	
High	ABBA
Low	Lowell



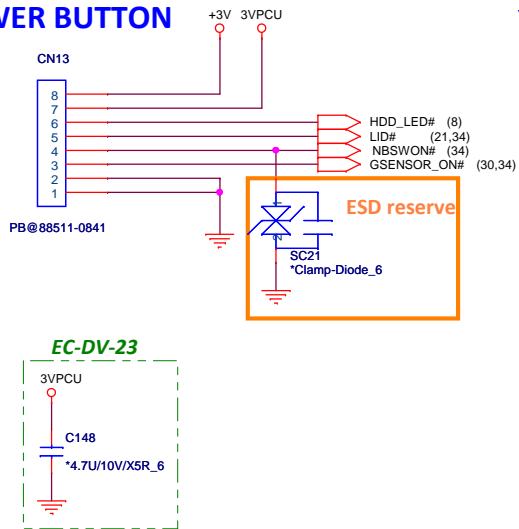
CLICK PAD



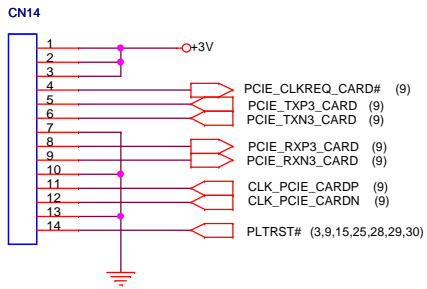
TRACK POINT



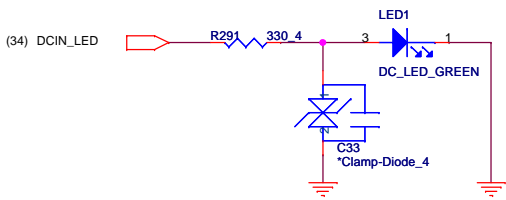
POWER BUTTON



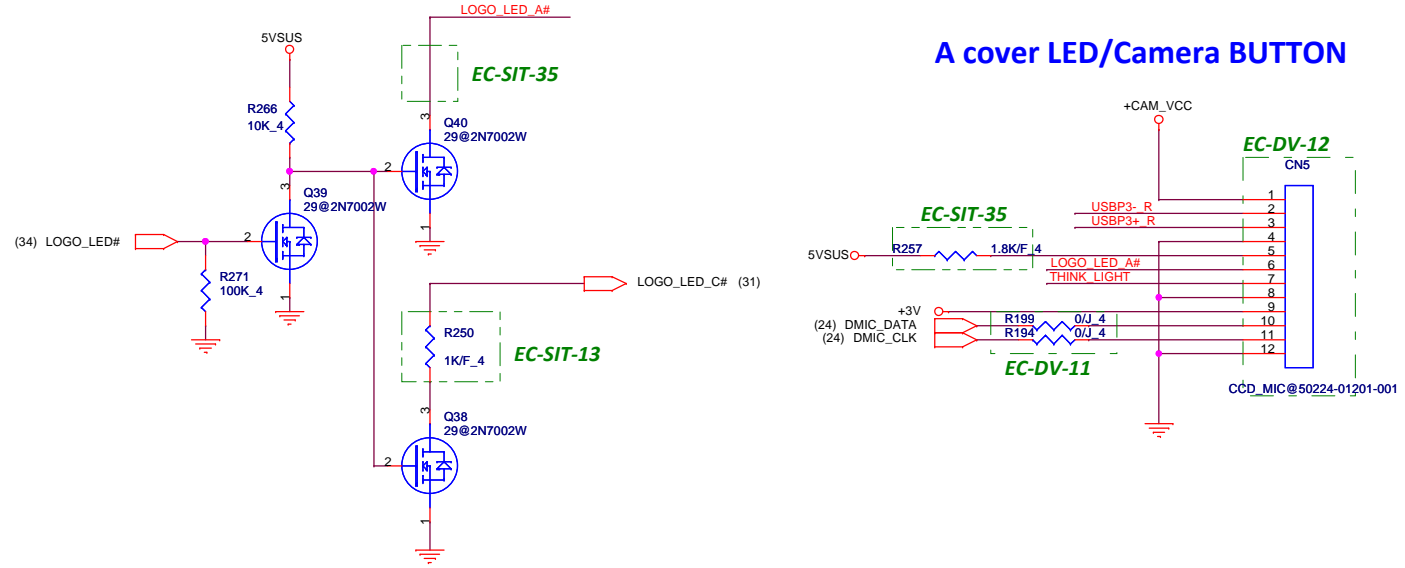
Card Reader Board



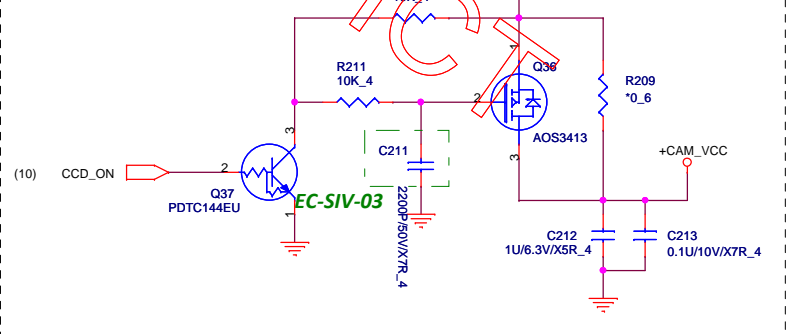
DC-IN LED



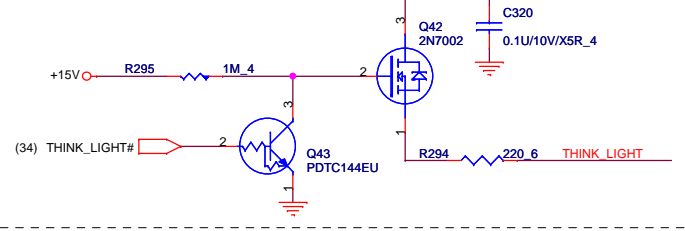
A cover LED/Camera BUTTON



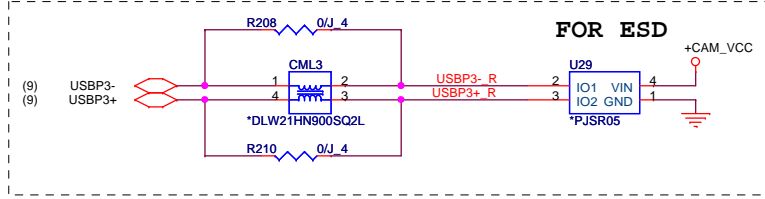
CAMERA VCC Control



THINK LIGHT LED ON

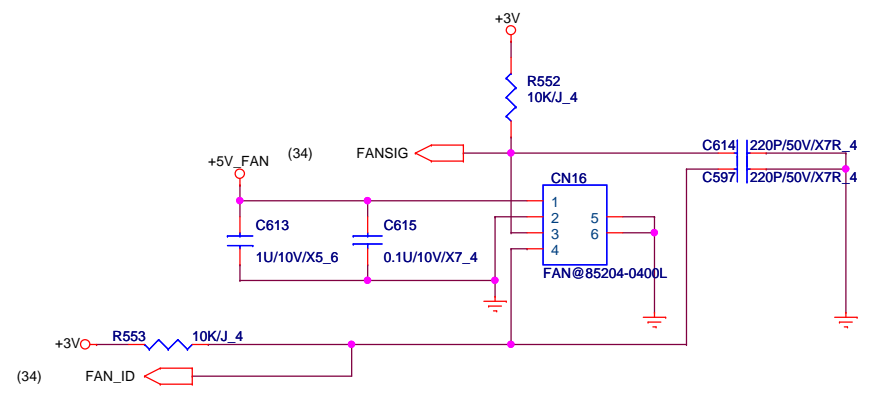
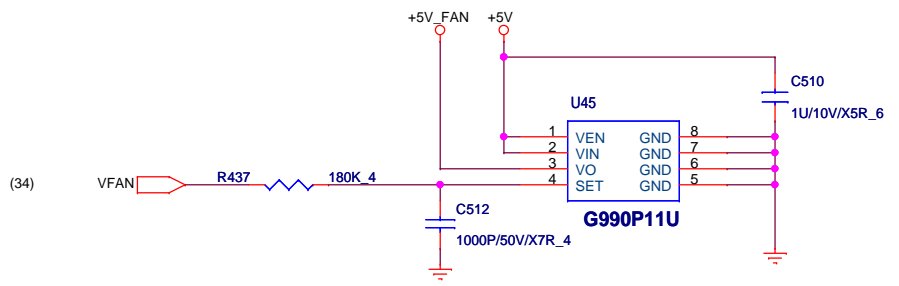


FOR ESD



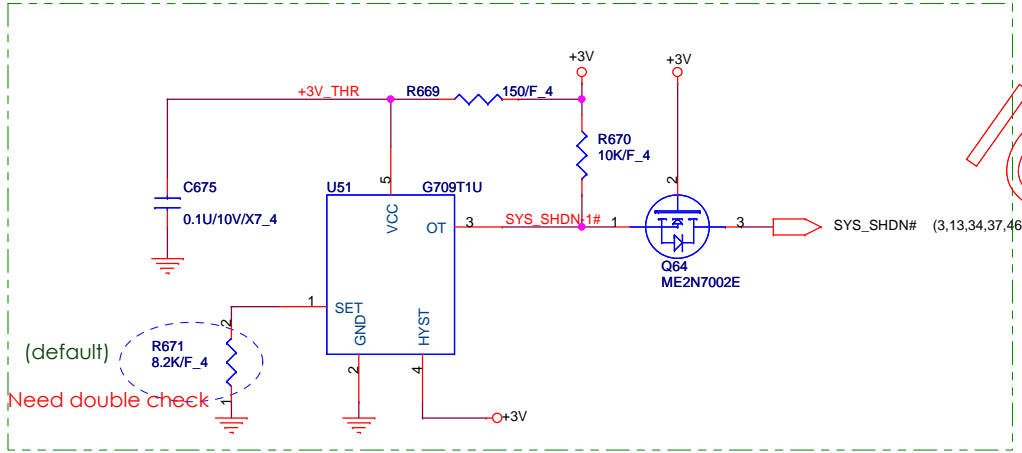
		Quanta Computer Inc. PROJECT : LV3D	
		Daughter board CON/LED/CCD	
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FAN CONTROL

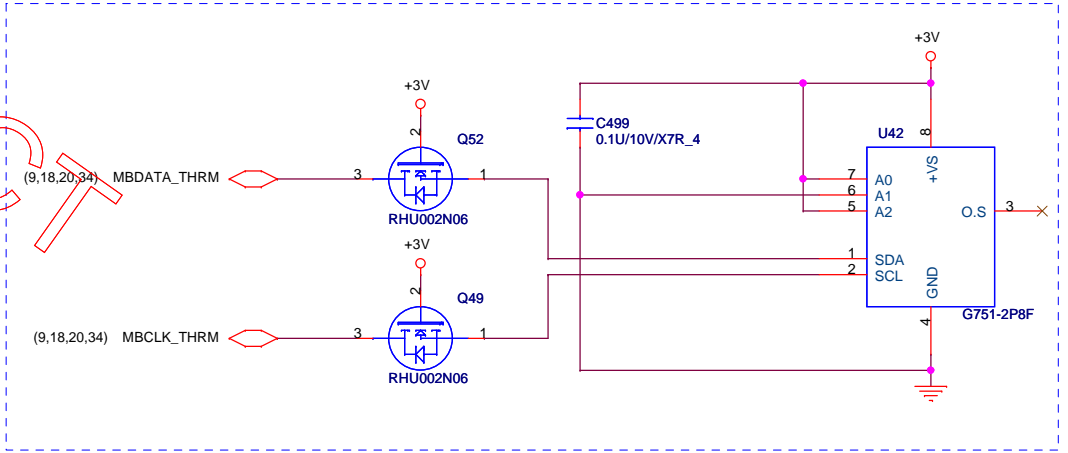


CPU Thermal Sensor

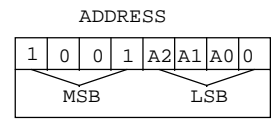
EC-SIT-03



Charger Thermal Sensor

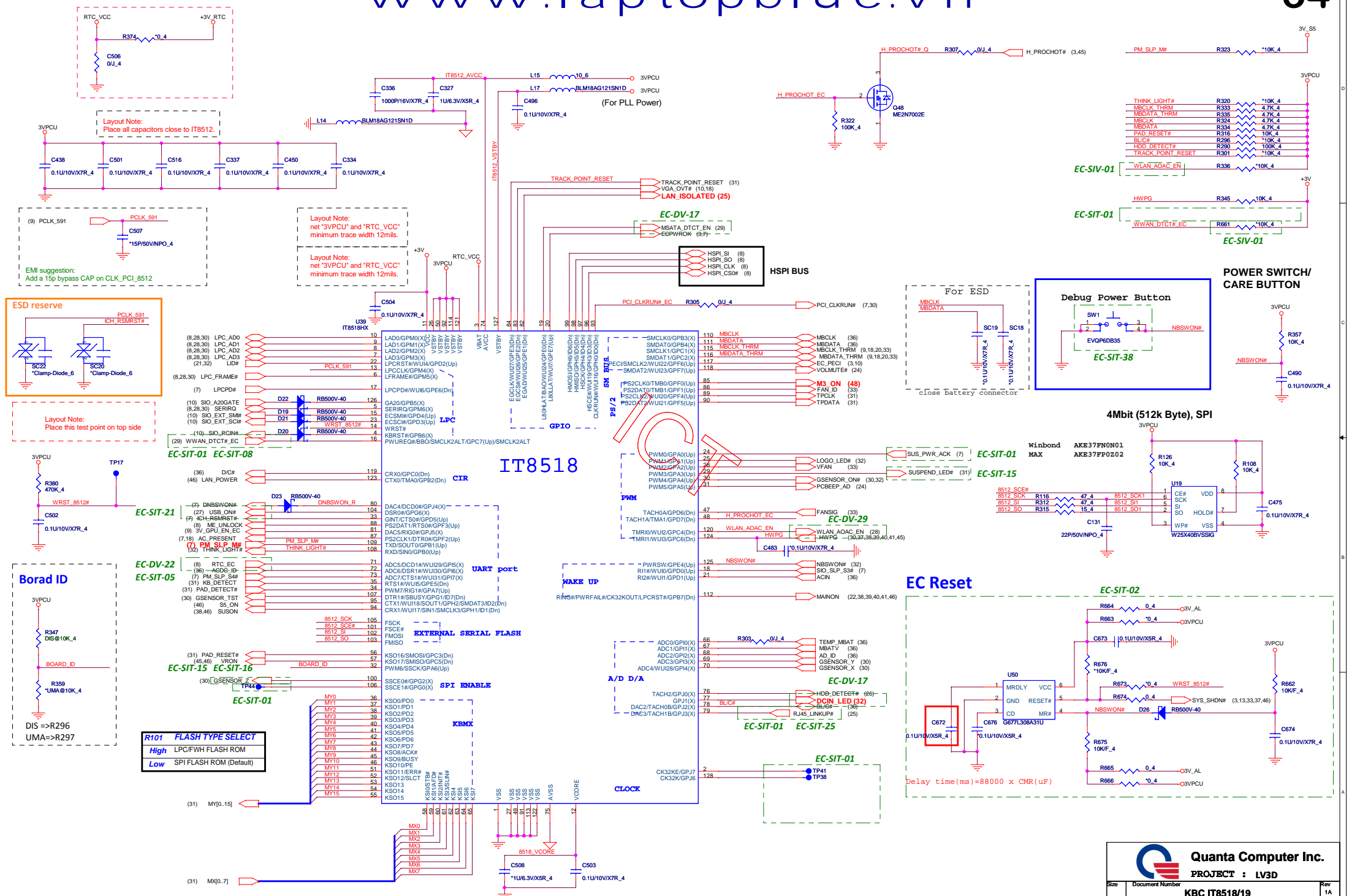


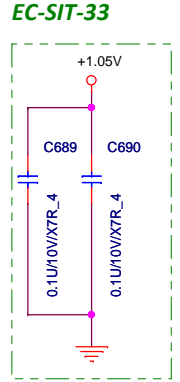
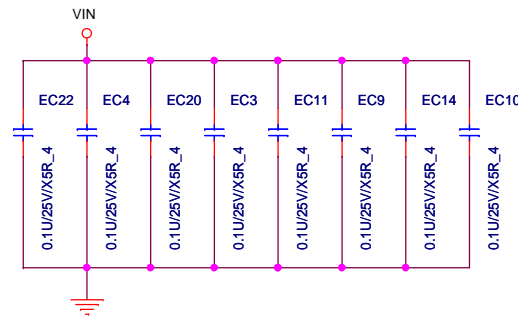
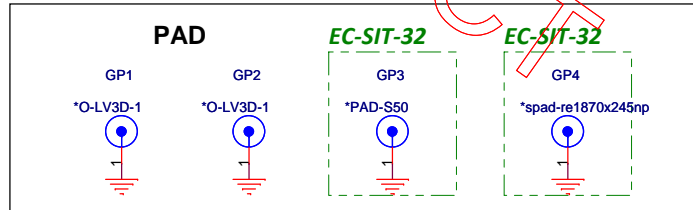
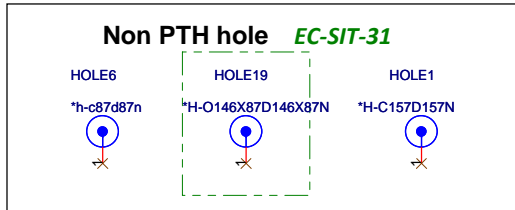
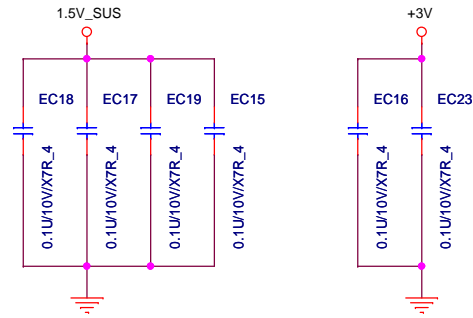
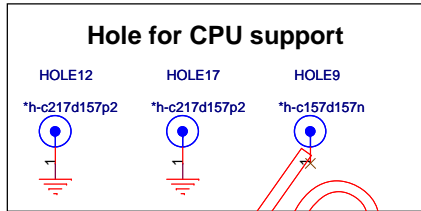
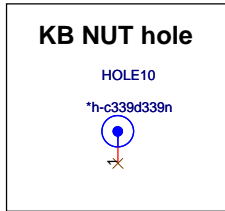
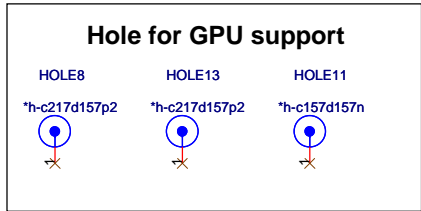
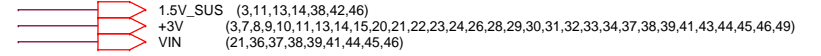
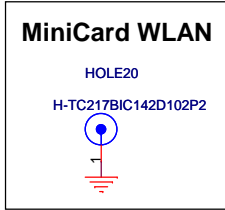
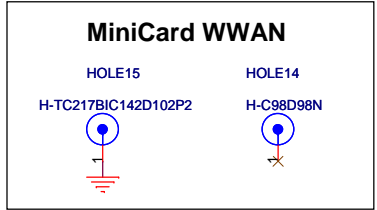
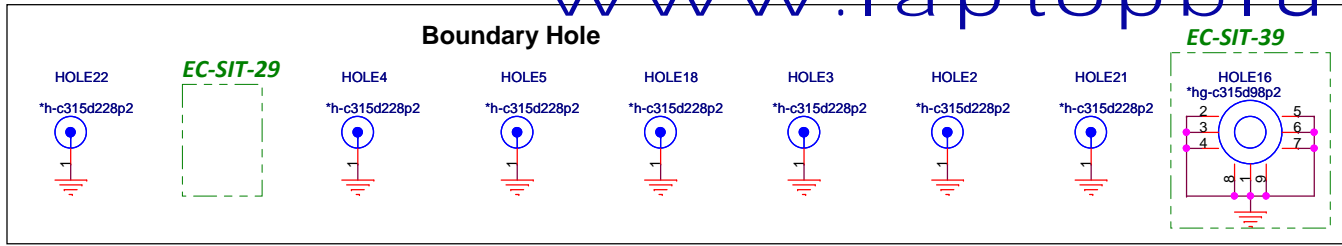
ADDRESS: 9AH



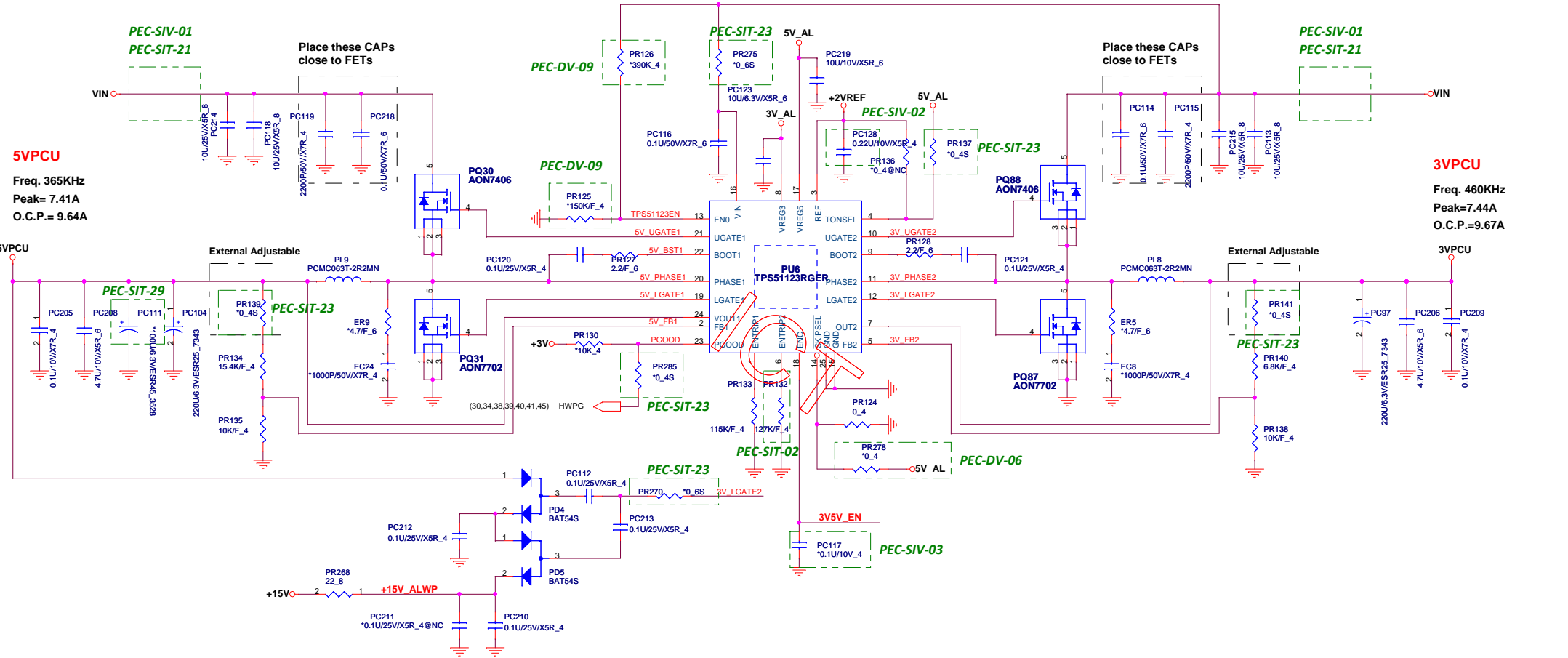
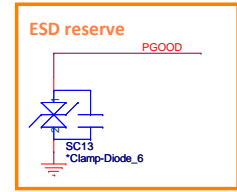
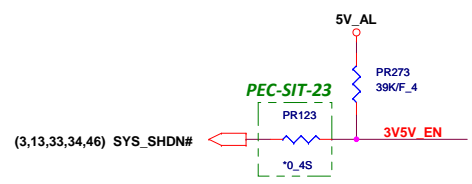
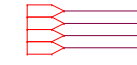
Quanta Computer Inc.
PROJECT : LV3D

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FAN & THERMAL		
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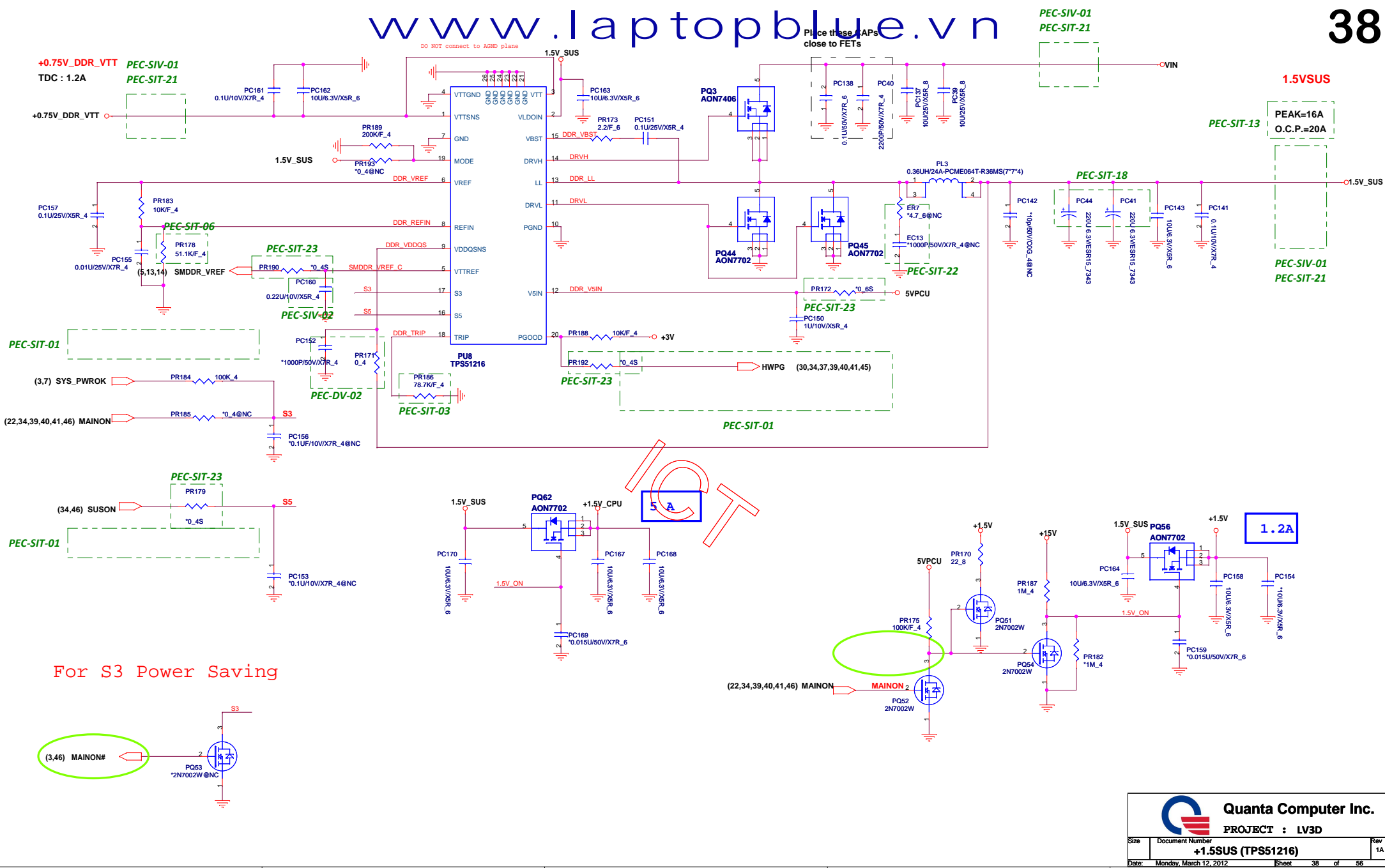


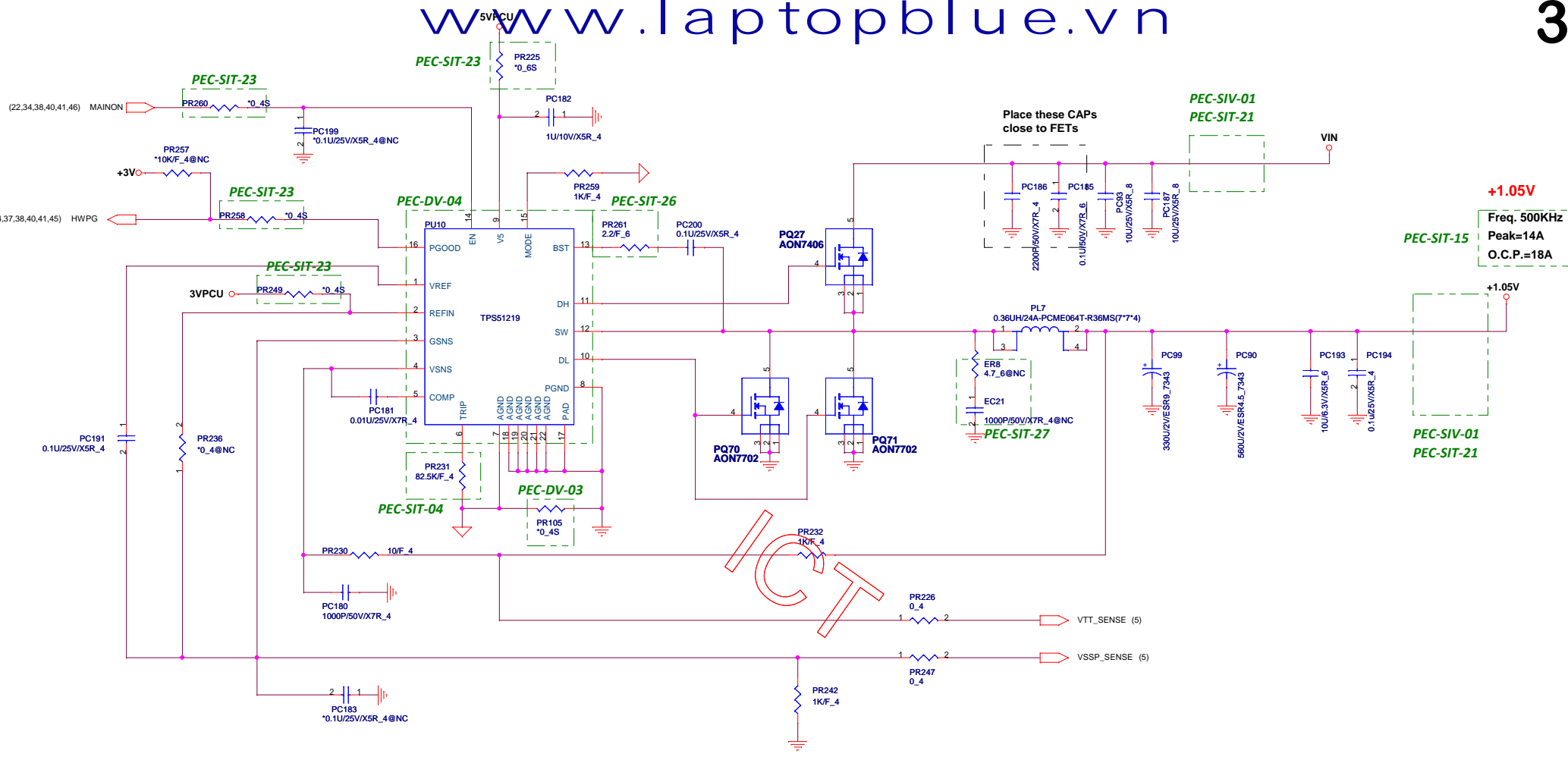
18 1 25,28,32,34,36,38,40,46,48,49) 3VPCU
16 1,36,38,39,40,41,42,43,44,46,48) 5VPCU
15 (21,30,32,38,42,43,46,48) +15V
14 (21,35,36,38,39,41,44,45,46) VIN



5VPCU
Freq. 365KHz
Peak= 7.41A
O.C.P.= 9.64A

3VPCU
Freq. 460KHz
Peak=7.44A
O.C.P.=9.67A





+1.05V
 Freq. 500KHz
 Peak=14A
 O.C.P.=18A

PEC-SIT-15

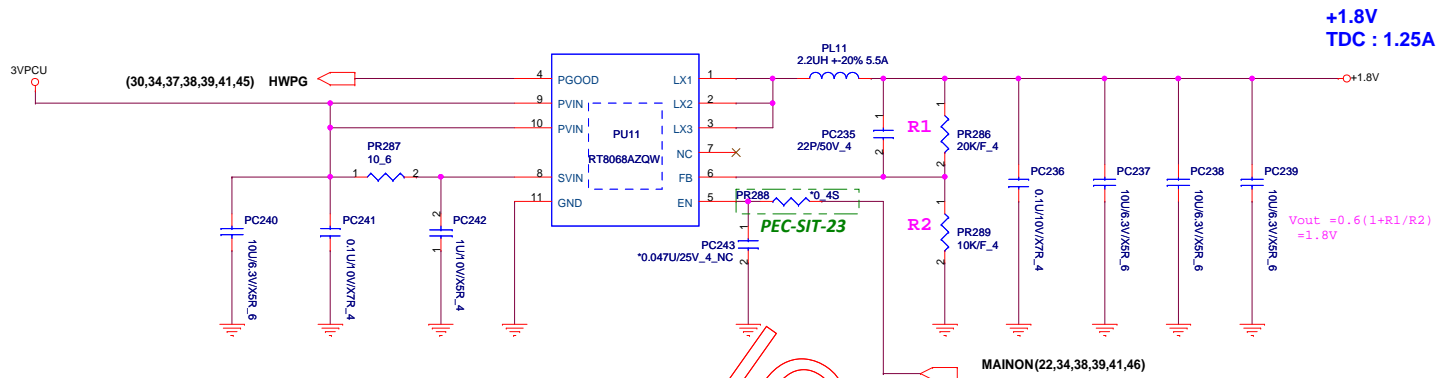
PEC-SIV-01
 PEC-SIT-21

PEC-SIV-01
 PEC-SIT-21

Place these CAPs
 close to FETs

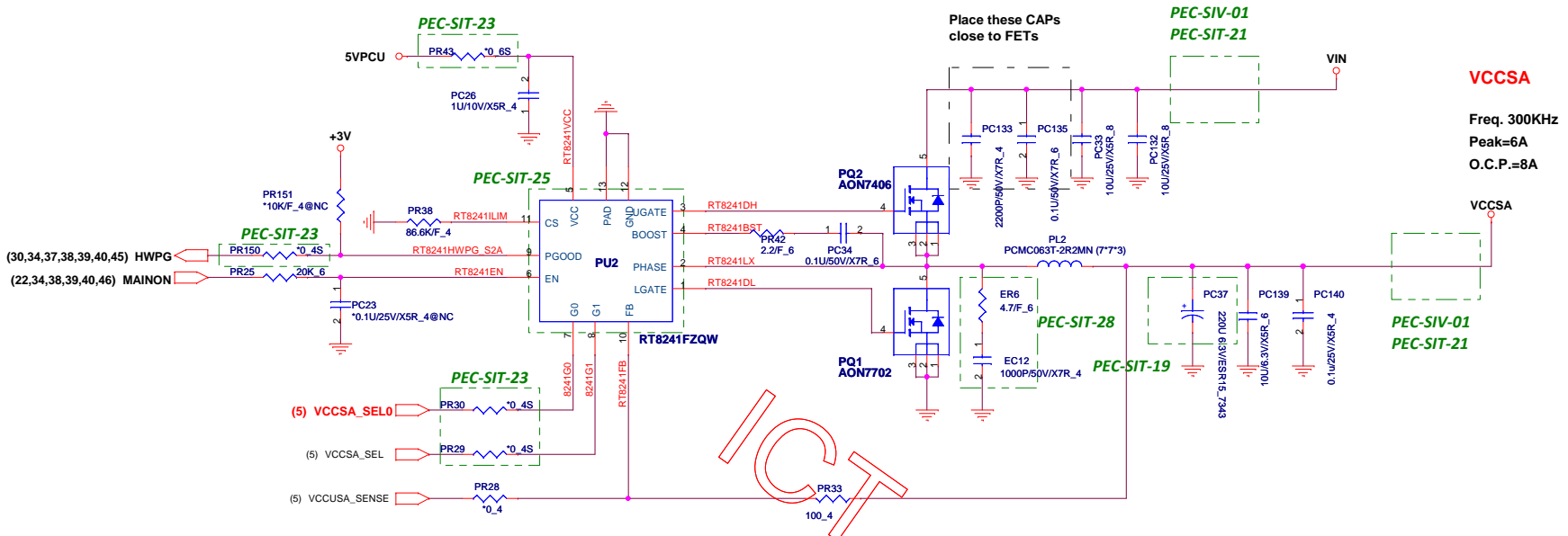
ICT

- MAINON (22,34,38,39,41,46)
- 3VPCU (8,21,25,28,32,34,36,37,39,46,48,49)
- +1.8V (5,8,11,46)



PROJECT

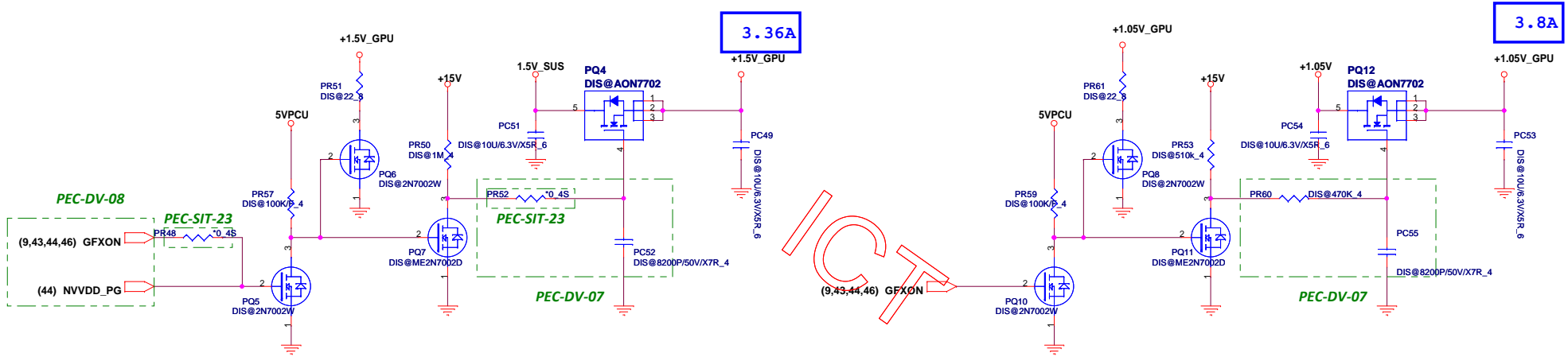
- MAINON (22,34,38,39,40,46)
- VCCSA_SEL (5)
- 5VPCU (8,21,35,37,38,39,40,42,43,44,46,48)
- VIN (21,35,36,37,38,39,44,45,46)
- VCCSA (5,46)
- +3V (3,7,8,9,10,11,13,14,15,20,21,22,23,24,26,28,29,30,31,32,33,34,35,37,38,39,43,44,45,46,49)
- HWP (30,34,37,38,39,40,45)
- VCCSA_SENSE (5)



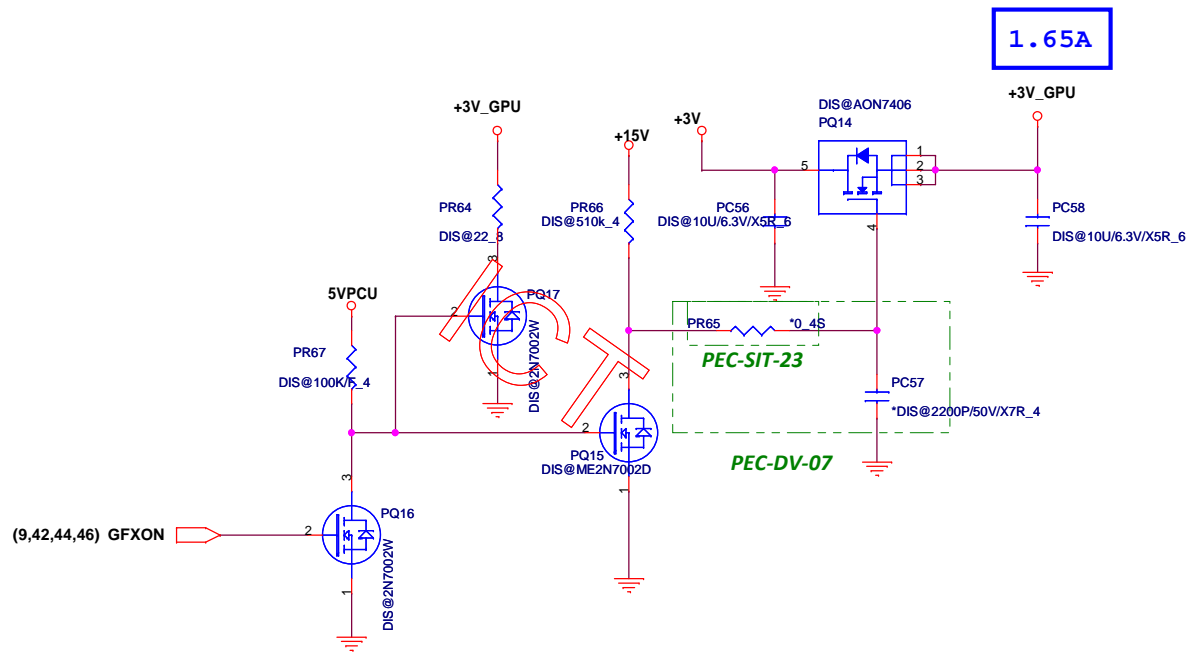
Processor	VCCSA_SELO G0	VCCSA_SEL G1	VCCSA Ultra segments
Sandy Bridge	0	0	0.9V
	0	1	0.85V
Ivy Bridge (ES sample)	1	0	0.725V
	1	1	0.675V


PEC-SIT-25

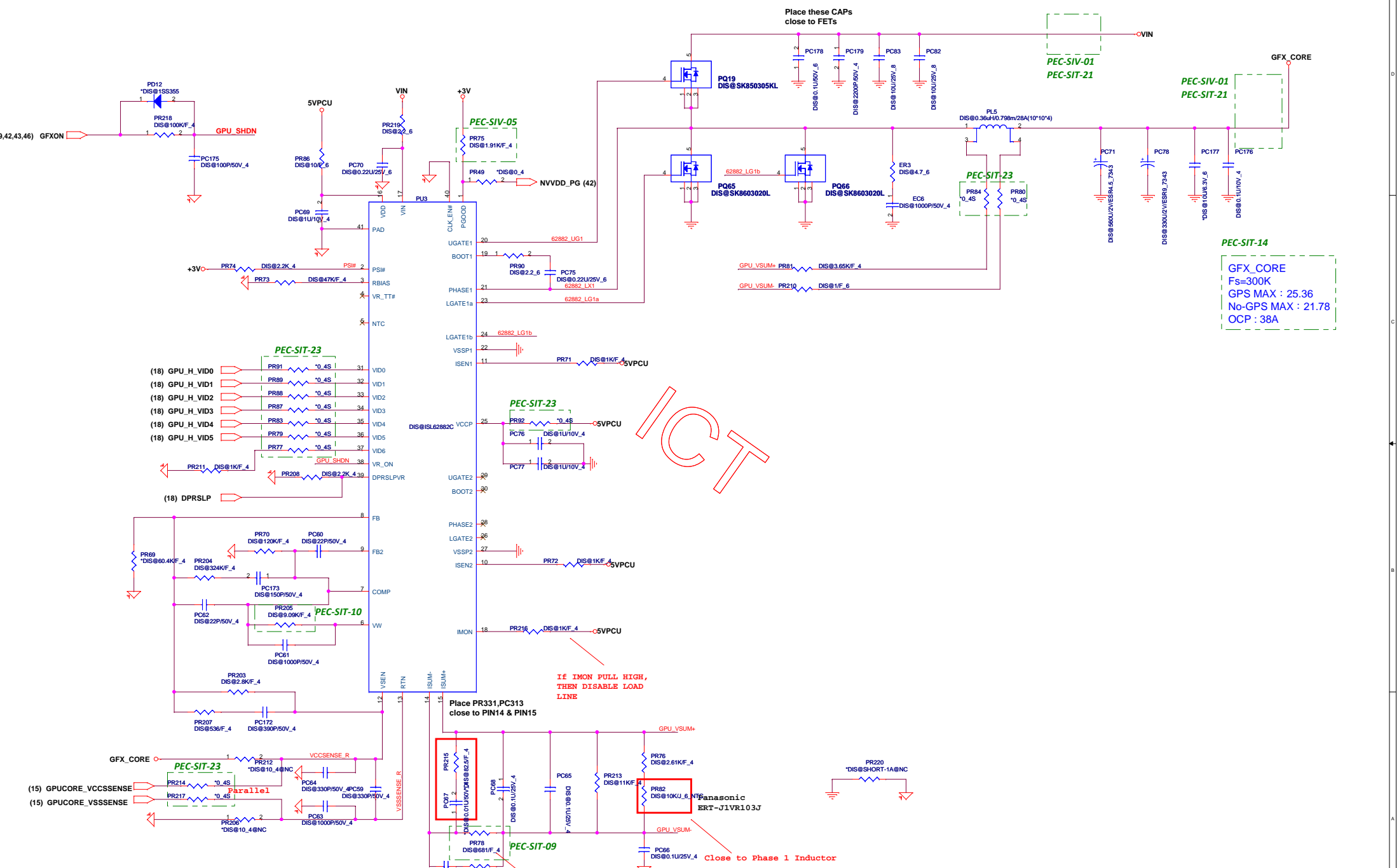
Processor	VCCSA_SELO G0	VCCSA_SEL G1	VCCSA Ultra segments
Sandy Bridge	0	0	0.9V
Ivy Bridge (ES sample)	0	1	0.85V
Ivy Bridge (QS sample)	1	0	0.775V
	1	1	0.75V



ICOPY



		Quanta Computer Inc.	
		PROJECT : LV3D	
Size	Document Number	Rev	
	+3V_GPU	1A	
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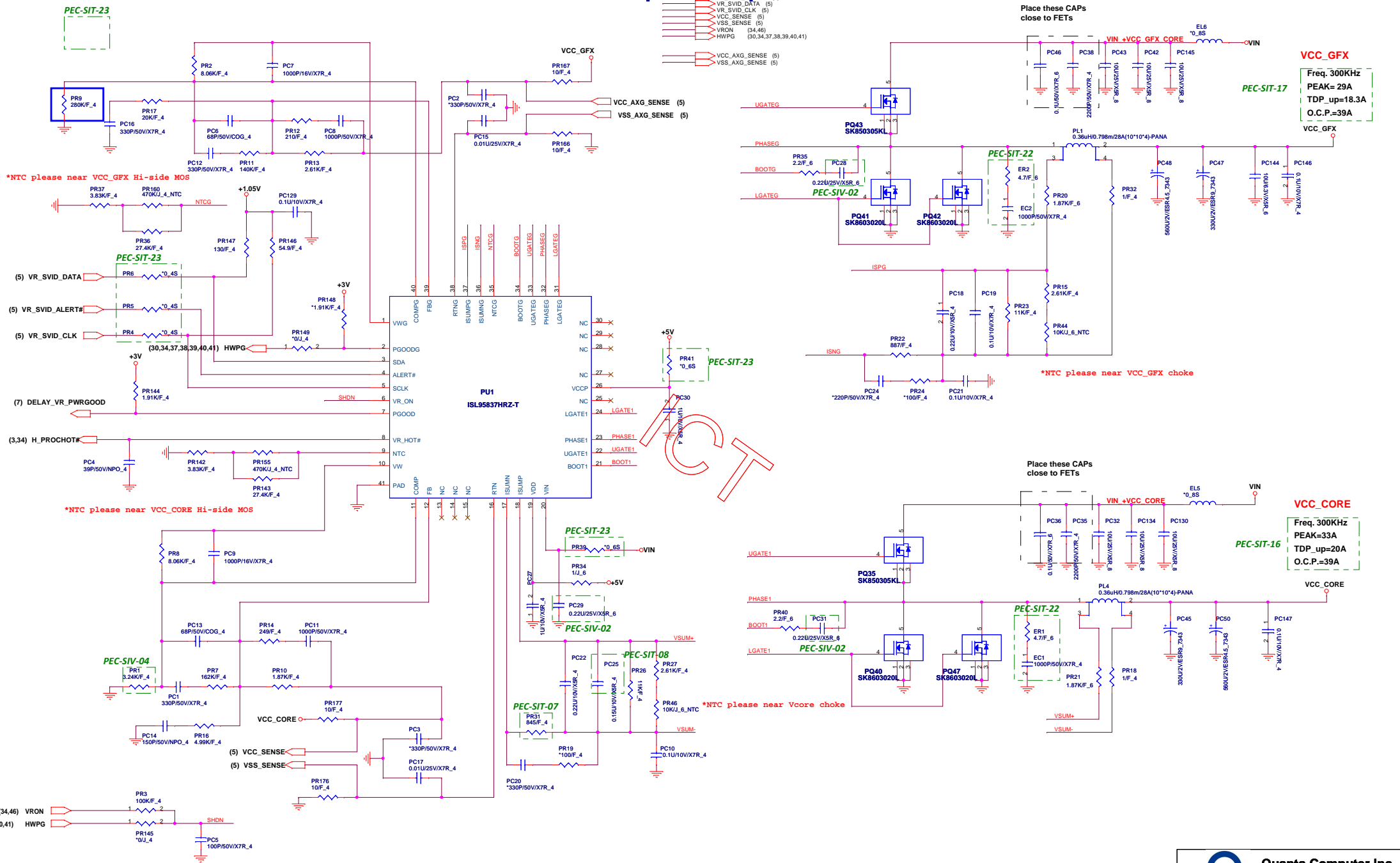


GFX_CORE
 Fs=300K
 GPS MAX : 25.36
 No-GPS MAX : 21.78
 OCP : 38A

If IMON PULL HIGH,
 THEN DISABLE LOAD
 LINE

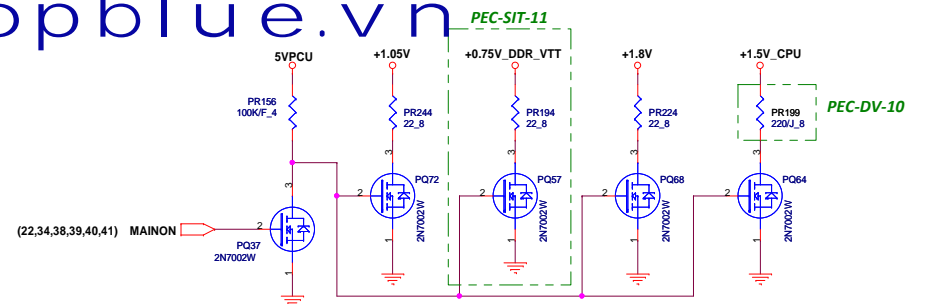
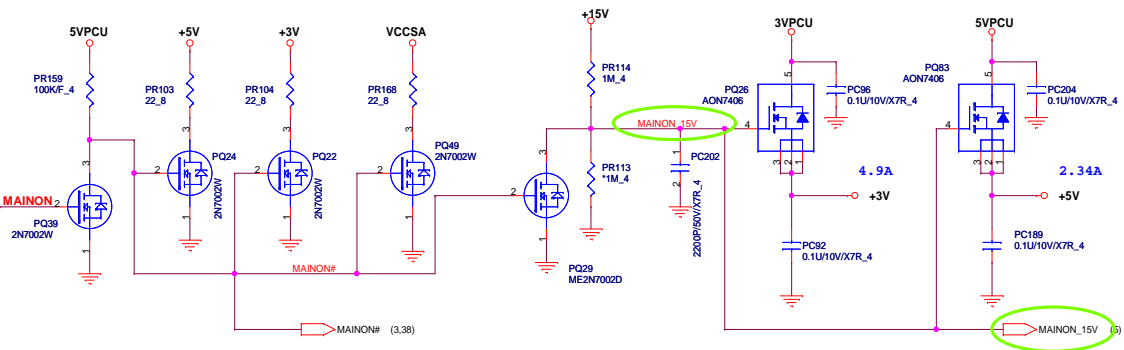
Place PR331, PC313
 close to PIN14 & PIN15

Close to Phase 1 Inductor

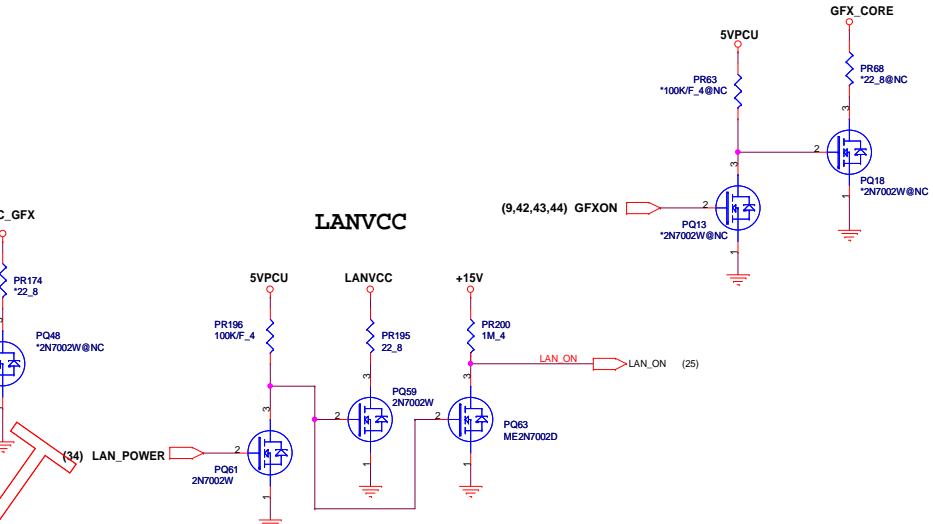
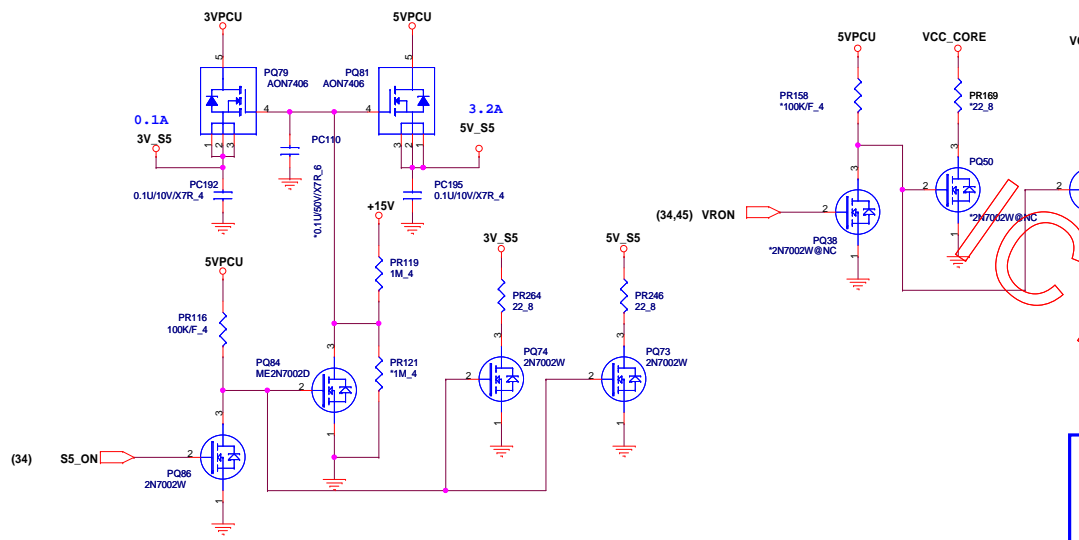


VCC_GFX
 Freq. 300KHz
 PEAK= 29A
 TDP_up=18.3A
 O.C.P.=39A

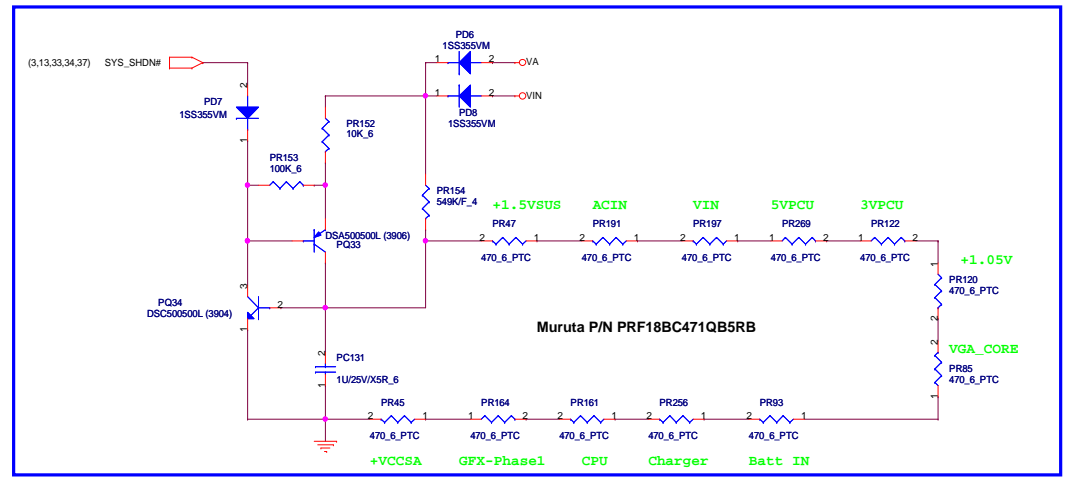
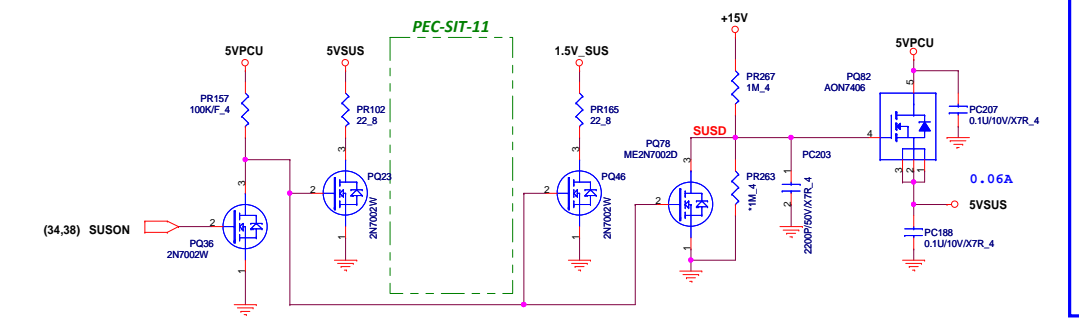
VCC_CORE
 Freq. 300KHz
 PEAK=33A
 TDP_up=20A
 O.C.P.=39A

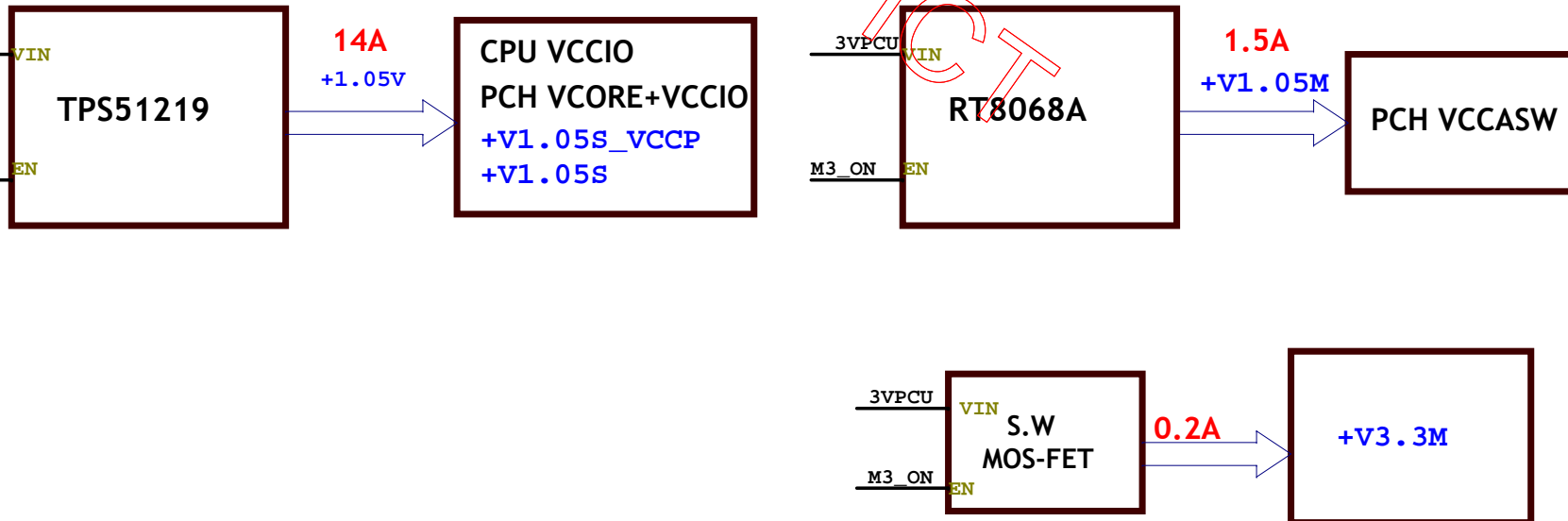
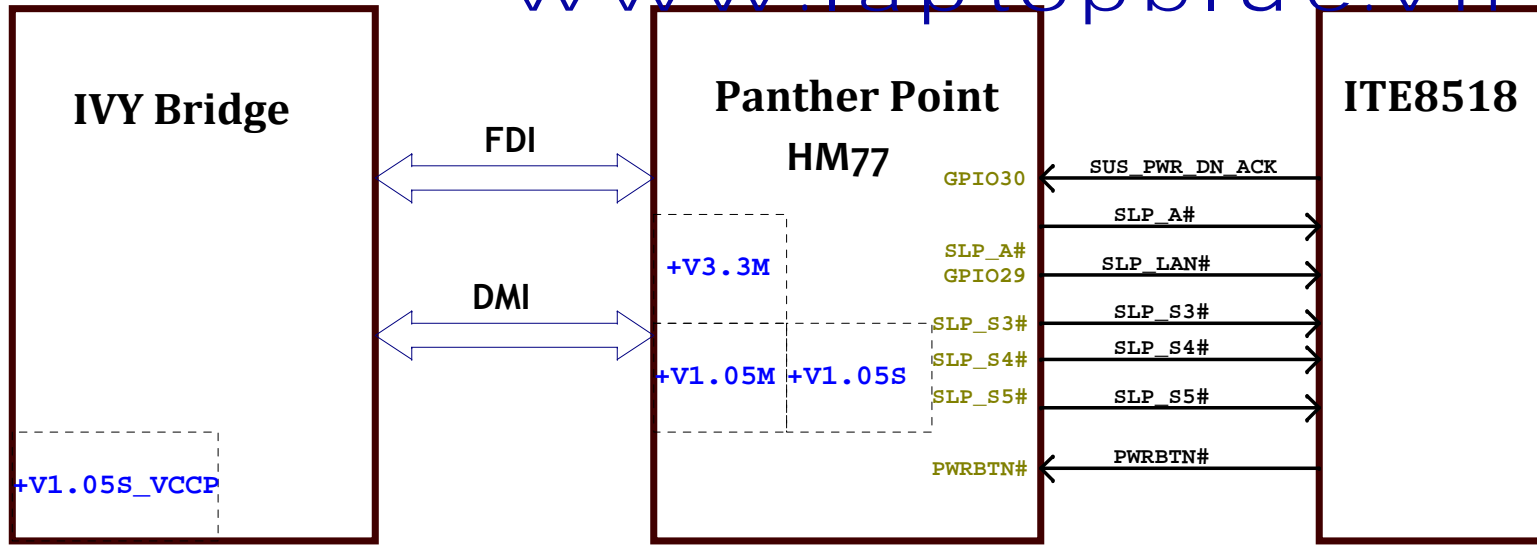


3V_S5, 5V_S5

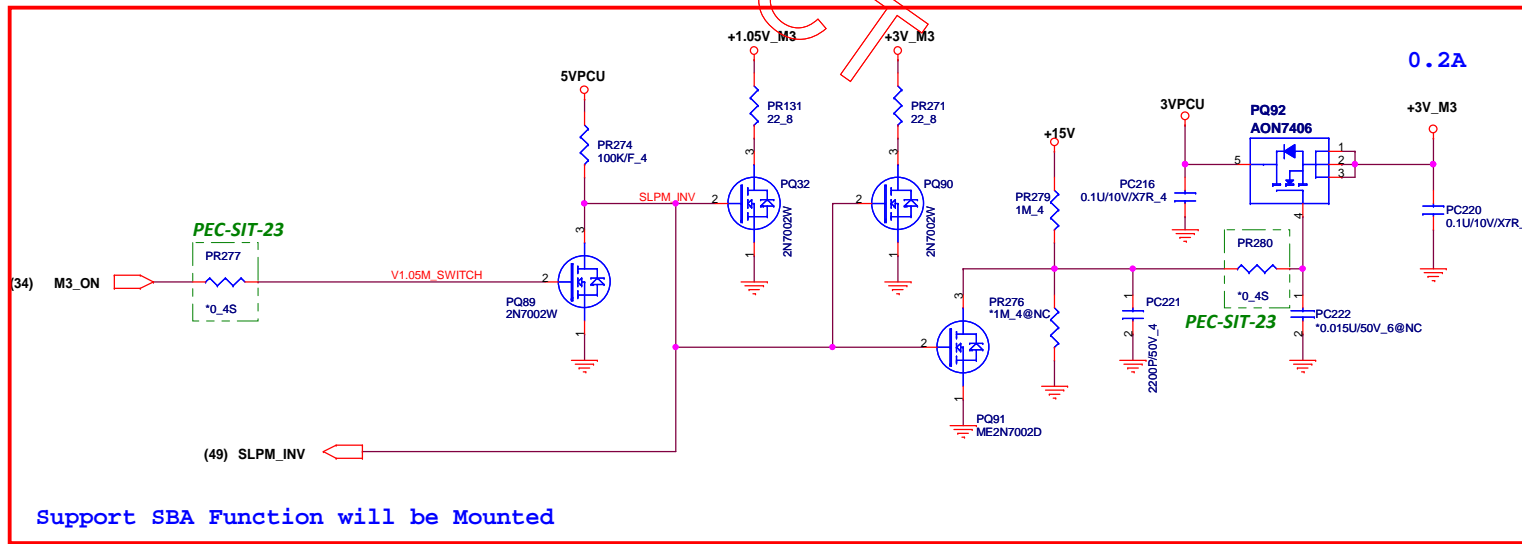
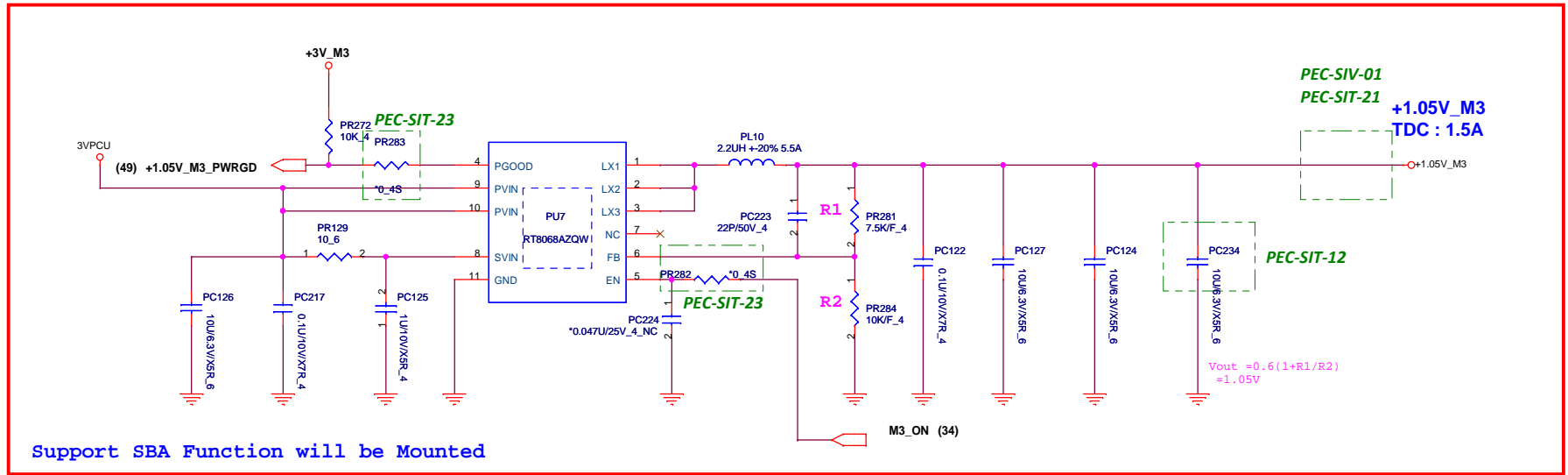


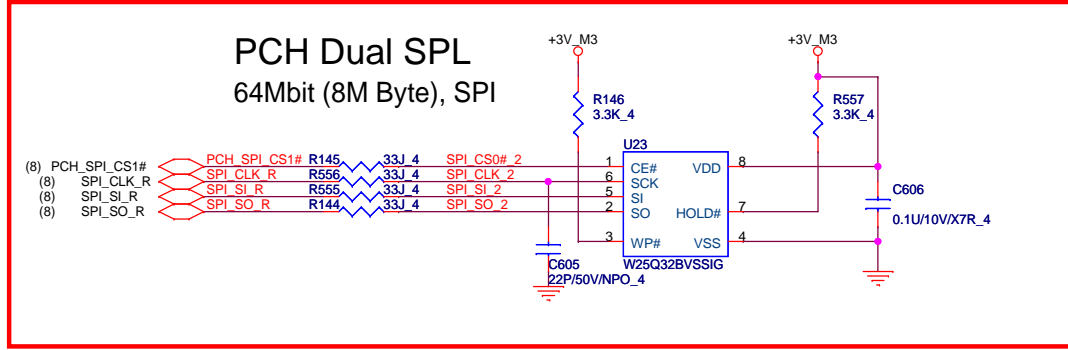
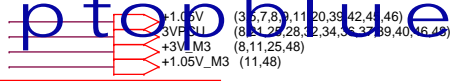
5VSUS



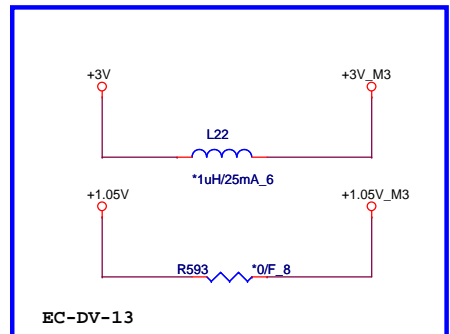


+3V_M3 (8,11,25,49)
+1.05V_M3 (11,49)

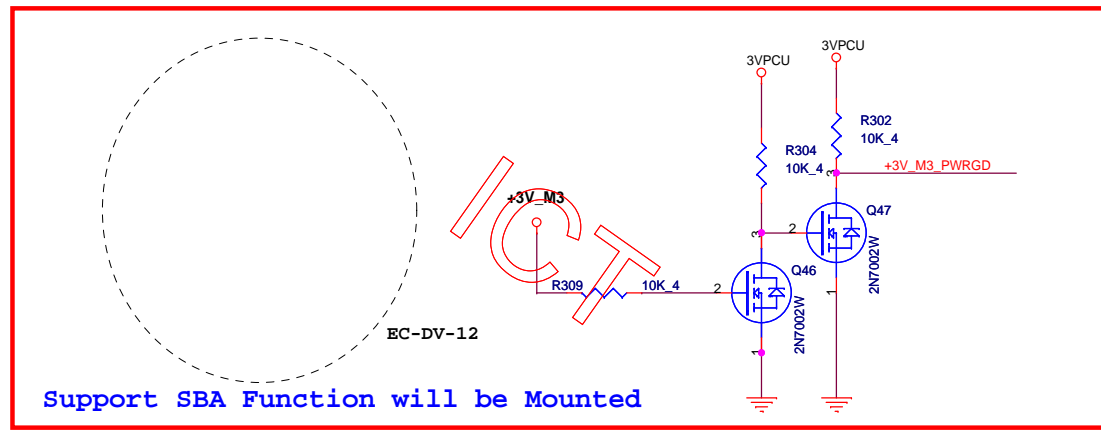




SBA POWERGD/SBA Power select

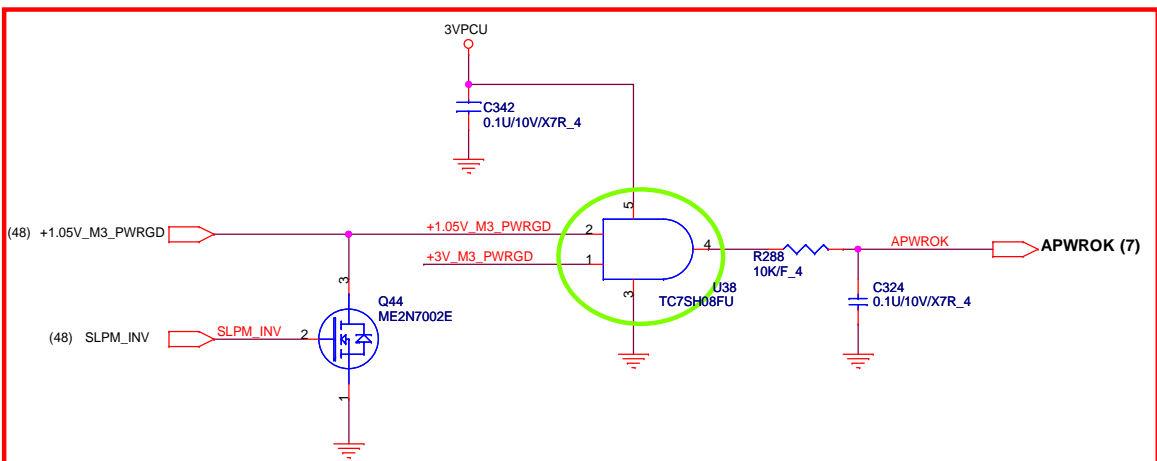


EC-DV-13
Without SBA Function will be Mounted




Support SBA Function will be Mounted

SBA LOGIC



Support SBA Function will be Mounted



Quanta Computer Inc.
PROJECT : LV3D

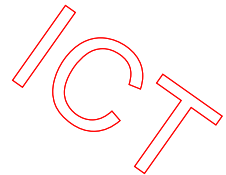
Size	Document Number	Rev
	Circuit for Intel SBA	1A
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EC #	Page	Description	Part Affected
EC-DV-01	5	Follow Intel schematic review suggestion	C487,C92,C93,C512,C478
EC-DV-02	3	Follow Intel schematic review suggestion to add resistor	R458
EC-DV-03	10	Reserve one board ID to identify ABBA & Lovell PCBA	R602,R605
EC-DV-04	5	Change component to "stuff" based on Intel suggestion	R433
EC-DV-05			
EC-DV-06	5	Change component to "stuff" based on Intel suggestion	R429
EC-DV-07	5	Add 0.002 ohm series resistor on +1.8V based on Intel suggestion	R166
EC-DV-08	13	Change 1.5V rail decoupling Caps from 1uF to 0.1uF based on Intel suggestion	C8561,C584,C574,C296
EC-DV-09	11	Change component to "stuff" based on Intel suggestion	C585,C586
EC-DV-10	10	External pull high for GPIO69 based on Intel suggestion	R595
EC-DV-11	32	Reserve 0 ohm for EMI	R459,R465
EC-DV-12	32	Modify CCD CONN to 12 pin	CN14
EC-DV-13	25	Modify RJ45 footprint	CN24
EC-DV-14	7,22	Reserve DP switch to support DP to DVI dongle by customer request	U2000
EC-DV-15	26	Stuff SATA Tx & Rx repeater IC for customer request	U10
EC-DV-16	23	Modify HDNI CONN footprint	CN10
EC-DV-17	29	Connect "MSATA_DTCT_EN" to EC to fix leakage issue if both have mSATA & WWAN design	R638,R8023
EC-DV-18	16	Follow up nVIDIA suggestion to modify Res value	R3014,R3015
EC-DV-19	18	Follow up nVIDIA suggestion to stuff PD Res	R3041
EC-DV-20	19	Follow up nVIDIA suggestion to modify Res value	R3086,R3091
EC-DV-21	22,23	Reserve diode to prevent leakage current from DP & HDMI device	R615,D26,R616,D29
EC-DV-22	29,34	Reserve WWAN_DTCT# pin from mini-PCIE slot to EC	
EC-DV-23	21	DXF team suggest keep 4.7uF to avoid using poor quality Hall Sensor ic	C435
EC-DV-24	7	DXF team suggest stuff the Res based on Intel Spec	R126
EC-DV-25	8,24	Reserve CAP for RF request	C656,C657,C659
EC-DV-26	31	Reserve 0 ohm Res for SMBus click pad inter touch function	R276,R279
EC-DV-27	3	If eDP is used, then the HPD should be pulled-high	R17
EC-DV-28	9	Change PN the same with LI2	
EC-DV-29	28,34	Reserve AOAC control GPIO from EC by customer request	
EC-DV-30	25	Reserve 1M Res to GND for Hi-pot test	

ICT

EC #	Page	Description	Part Affected
PEC-DV-01	36	Modify battery connector fottprint	PJP1
PEC-DV-02	38	Reserve RC	PC268,PR323
PEC-DV-03	39	Short signal GND & digital GND	PR95
PEC-DV-04	39	Modify +1.05V power control IC footprint	PU7
PEC-DV-05	36	Follow FAE suggestion change PC2 to 100p CH11006JB18	PC2
PEC-DV-06	37	Follow FAE suggestion to reserve PR79 connect PU3.14 to 5VAL	PR79
PEC-DV-07	42,43	Reserve RC circuit to adjust VGA power up sequence	
PEC-DV-08	42	Follow LZ8 design to change +1.5V_GPU enable signal	
PEC-DV-09	37	Follow LI2 design to un-stuff component	
PEC-DV-10	46	Follow LI2 design to change Res value	
PEC-DV-11			
PEC-DV-12			
PEC-DV-13			
PEC-DV-14			
PEC-DV-15			
PEC-DV-16			
PEC-DV-17			
PEC-DV-18			

ICT

EC #	Page	Description	Part Affected
EC-SIV-01	10,29	Follow up LI2 design to connect WWAN_DTCT# to PCH GPIO68	R660,R220
EC-SIV-02	20	Follow up LI2 vendor suffestion to connect pin57 to GNDA	U6
EC-SIV-03	20,22,32	Modify components footprint and PN for EOD parts	C211,C4,C15,C17,C186
			

EC #	Page	Description	Part Affected
PEC-SIV-01	37~41 44,45	Modify power jump to short pad	PJP11,PJP12,PJP14,PJP2,PJP4,PJP5,PJP17,PJP9,PJP8,PJP1,PJP3, PJP15,PJP6,PJP7,PJP13
PEC-SIV-02	45	Modify CAP value from 20% to 10%	PC28,PC29,PC31
PEC-SIV-03	37	Stuff the CAP to stable enable signal	PC117
PEC-SIV-04	45	Modify RES value to make OTP stable	PR1

ICT

EC #	Page	Description	Part Affected
EC-SIT-01	3,7,8 11,34	Remove Deep S3 circuit	Delete R79,R492,R499,R363,R372,D4,D5,Q29,R617,R626,Q30,C624,R297 R544,Q27,Q55,Q54,Q28,R536,R404,R415,R375,R361, Un-stuff R499,R361 Add R668
EC-SIT-02	34	Add EC Reset IC circuit	Add U50,D26,C672,C673,C674,C676,R664,R674,R675,R665,R662
EC-SIT-03	33	Add CPU temperature switch circuit	Add U51,Q64,R669,R670,R671,C675
EC-SIT-04	3	Add THERMTRIP# assert to SYS_SHDN# circuit	Add Q62,Q63,R667
EC-SIT-05	8	Add RTC detect circuit	Add Q65,R672
EC-SIT-06	20	Swap EC between MBDATA_THRM and MBCLK_THRM for eDP converter & remove EEPROM	Delete U28,Q7,Q8 ; Add Q70
EC-SIT-07	29	Add AOAC circuit need to support with WWAN	Un-stuff R222
EC-SIT-08	34	Change WWAN_DTCT#_EC GPIO pin	
EC-SIT-09	17	BOM NG,correct CAP value to 27p	C102,C103
EC-SIT-10	8,17	Modify XTAL PN & footprint for single source issue	Y1,Y2
EC-SIT-11	9,18,23	Change MOS to dual-MOS	Delete Q45,Q51,Q18,Q19,Q22,Q24,Q3,Q4 Add Q66,Q67,Q68,Q69
EC-SIT-12	31	Decrease 5VSUS to 1pin to add 1pin to GND	
EC-SIT-13	31,32	Change LOGO LED limited-current RES value due to FP/B no layout spacing	R165,R250
EC-SIT-14	21	Follow LI2 design to add LCD_VCC fuse	Add F5
EC-SIT-15	34	Change SUSPEND_LED# to PWM GPIO	
EC-SIT-16	34	Reserve G SENSOR_Z GPIO	
EC-SIT-17	5	Delete CAP due to DV test is Pass and found no issue if un-stuff it	Delete C87,C99,C5,C129
EC-SIT-18	23	Add diode to fix +5V under S5 leakage current issue	Delete R1,D1,F1 ; Add D27,C687
EC-SIT-19			
EC-SIT-20	27	Change USB power switch and add ESD component to fix USB port CDE fail issue	Delete C93,U15,C73,C143,C96 Add C680,U52,C677,C678,C679,C681,U53,C682,U54,C683,C684,C685 C686,U55
EC-SIT-21	34	Modify EC USB ON GPIO to low active for new USB power switch	
EC-SIT-22	27	Stuff USB common choke to fix EMI issue	Delete R138,R139,R80,R85 Stuff CML1,CML2
EC-SIT-23	7,23	Change CAP & RES footprint from 0402 to 0201 to fix ESD issue	C626,C627,C628,C629,C630,C631,C640,C641,R4,R5,R7,R8
EC-SIT-24	23	Delete diode due to we change design	Delete D9,D10
EC-SIT-25	25,34	Reserve EC GPIO RJ45_LINKUP# to support IBM wake up solution	

ICT

EC #	Page	Description	Part Affected
EC-SIT-26	03	Reserve CAP for S3 resume hang up issue	C688
EC-SIT-27	27	Change ESD solution	Delete U46,U21,U40,U14
EC-SIT-28	27	Swap net name for layout more smooth	U55
EC-SIT-29	35	ME no need for this screw hole	Delete HOLE7
EC-SIT-30	27	Change CAP size from 3528 to 7343 for shortage issue	C679,C685
EC-SIT-31	35	Modify Non-PTH hole footprint for layout request	HOLE19
EC-SIT-32	35	Add GND PAD for ESD request	GP3,GP4
EC-SIT-33	35	Add CAP to fix ESD issue	C689,C690
EC-SIT-34	28	Change MOSFET Spec to 3A to support WLAN/WWAN AOAC function	Q59
EC-SIT-35	32	Move the A cover LED limit-current RES near power side prevent from cable short risk	R257
EC-SIT-36	32	Change Thinklight LED limit-current RES footprint from 0402 to 0603	R294
EC-SIT-37	28,29	Modify footprint for SMT request	CN6,CN19
EC-SIT-38	34	Change debug switch footprint prevent from interference with ME base	SW1
EC-SIT-39	35	Change hole footprint for ESD request	HOLE16

ICT

EC #	Page	Description	Part Affected
PEC-SIT-01	38	Remove Deep S3 circuit	Delete PR180,PR181,PD10,PD11
PEC-SIT-02	37	Modify Res value to 127k for 3VPCU OCP fine tune	PR132
PEC-SIT-03	38	Modify Res value to 78.7k for 1.5V_SUS OCP fine tune	PR186
PEC-SIT-04	39	Modify Res value to 82.5k for 1.05V OCP fine tune	PR231
PEC-SIT-05	44	Stuff Res for VGA power good pull high	PR75
PEC-SIT-06	38	Modify Res value to 51.1k for 1.5V_SUS regulation fine tune	PR178
PEC-SIT-07	45	Modify Res value to 845 for Vcc_Core load line	PR31
PEC-SIT-08	45	Modify CAP value to 0.15u for Vcc_Core load line	PC25
PEC-SIT-09	44	Modify Res value to 681 for VGA OCP fine tune	PR78
PEC-SIT-10	44	Modify Res value to 9.09k for VGA OCP fine tune	PR205
PEC-SIT-11	46	Discharge gate change to mainon for 0.75V discharge stable	PQ57,PR194
PEC-SIT-12	48	Output add 10uF/6.3V CAP for 1.05V_M3 output stable	PC234
PEC-SIT-13	38	Updated 1.5V_SUS power budget to 16A,OCP change to 20A	
PEC-SIT-14	44	Updated VGA power budget to fix actual loading	
PEC-SIT-15	39	Updated 1.05V power budget to 14A,OCP change to 18A	
PEC-SIT-16	45	Updated VCC_CORE power budget to fix actual loading,add TDP-up 20A	
PEC-SIT-17	45	Updated VCC_GFX power budget to fix actual loading,add TDP-up 18.3A	
PEC-SIT-18	38	Change CAP footprint from 3528 to 7343 due to vendor can't support	PC41,PC44
PEC-SIT-19	41	Change CAP PN due to vendor can't support	PC37
PEC-SIT-20	36	Change CAP PN for component stress request	PC108,PC109
PEC-SIT-21		Delete power jump	PJP1 PJP2 PJP3 PJP4 PJP5 PJP8 PJP11 PJP12 PJP13 PJP14 PJP6 PJP7 PJP9 PJP10 PJP15 PJP17
PEC-SIT-22	38,45	Stuff components to fix EMI issue	Stuff ER1,ER2,ER7,EC1,EC2,EC13
PEC-SIT-23	37,38,39 41,42,43 44,45,48	Change 0 ohm RES footprint to short pad	PR137,PR139,PR141,PR285,PR123,PR270,PR275,PR179,PR190,PR192 PR172,PR249,PR258,PR260,PR225,PR150,PR29,PR30,PR43,PR52,PR48 PR65,PR214,PR217,PR80,PR84,PR92,PR77,PR79,PR83,PR87,PR88,PR89 PR91,PR4,PR5,PR6,PR39,PR41,PR277,PR280,PR282,PR283,PR288
PEC-SIT-24	40	Change +1.8V from LDO to PWM to enhance battery life	Delete PR240,PQ25,PQ67,PR111,PR229,PR97,PC89,PQ21,PR110,PC94 EL3,PC100,PC95,PR101,PC85,PR108,PU4,PR94,PR95,PC79,PC84,PC80 PR228 Add PC235,PC236,PC237,PC238,PC239,PC240,PC241,PC242,PC243,PU11 PR286,PR287,PR288,PR289,PL11
PEC-SIT-25	41	Change VCCSA VR chip for QS sample CPU	PU2

ICT

EC #	Page	Description	Part Affected
PEC-SIT-26	39	PR261 change to 2.2ohm for power stable	PR261
PEC-SIT-27	39	Add RC snubble for power stable	Stuff ER8,EC21
PEC-SIT-28	41	Add RC snubble for power stable	Stuff ER6,EC21
PEC-SIT-29	37	Un-stuff CAP for vendor not support 3525 size	PC111
PEC-SIT-30			
PEC-SIT-31			

ICT