

UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :None Installed
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CRV:Chief River

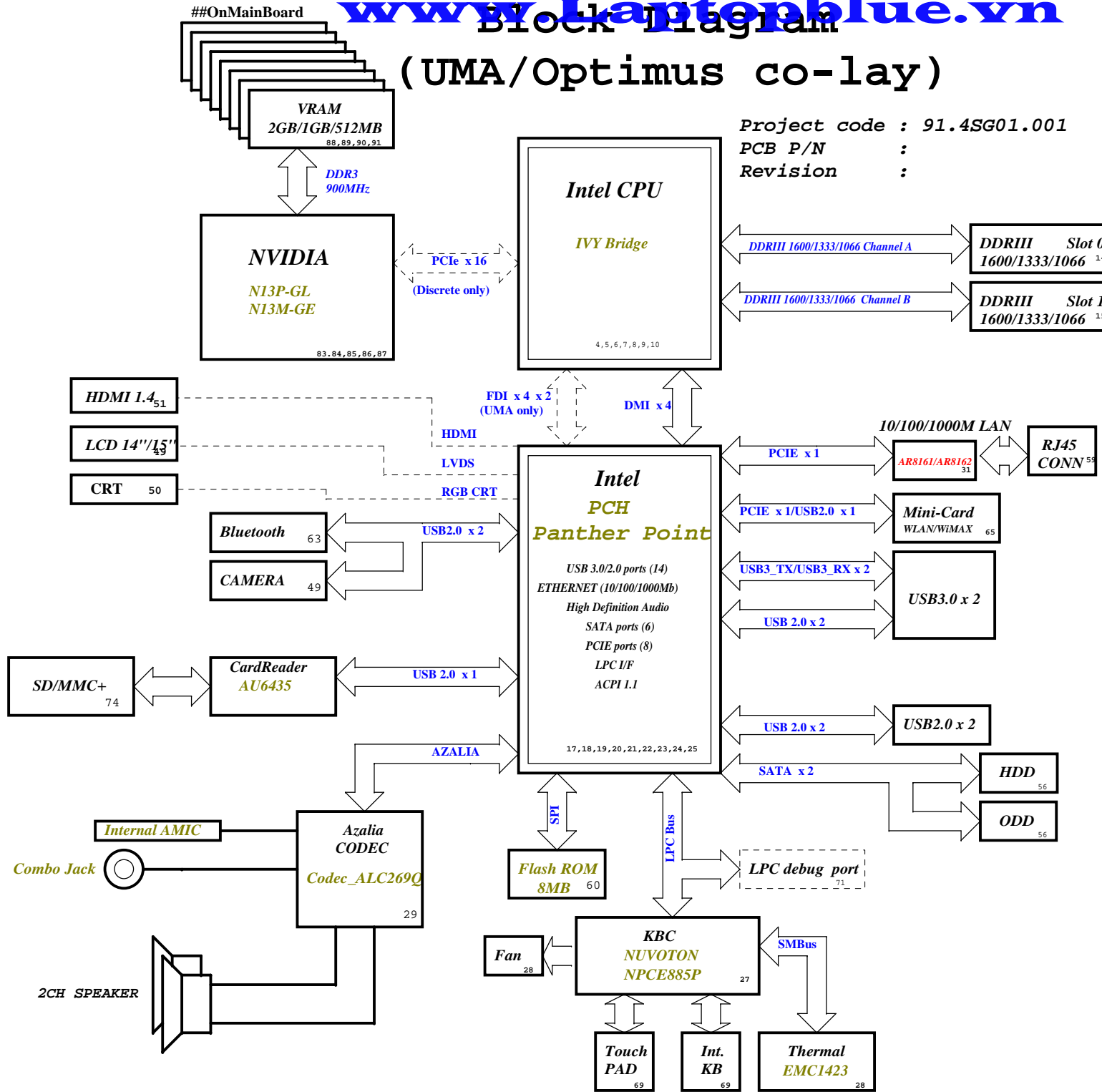
JV10-CS

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Cover Page			
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(UMA/Optimus co-lay)

Project code : 91.4SG01.001
PCB P/N :
Revision :

SYSTEM DC/DC TPS51461 48		CPU DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VCCSA	DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51211 45		SYSTEM DC/DC G977F 45	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	1D05V_S0	DCBATOUT	1D0V_S0
SYSTEM DC/DC TPS51123 41		SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5	DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
GFX DC/DC TPS51640RSLR 42~44		VGA ISL62882C 92	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE	DCBATOUT	VGA_CORE
CHARGER BQ24745 40		SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
AD+ BT+	DCBATOUT	3D3V_S5	1D8V_S0
VGA switches 93		Switches	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D5V_S3 3D3V_S0 1D05V_VTT	1D5V_VGA_S0 3D3V_VGA_S0 1D05V_VGA_S0	1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER			
L1:Top		L4:Signal	
L2:VCC		L5:GND	
L3:Signal		L6:Bottom	



Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0:	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

All Not update

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW_Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB	
		Address	Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA	
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA	
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK	

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	N/A
1	HDD1
2	N/A
3	N/A
4	ODD
5	N/A

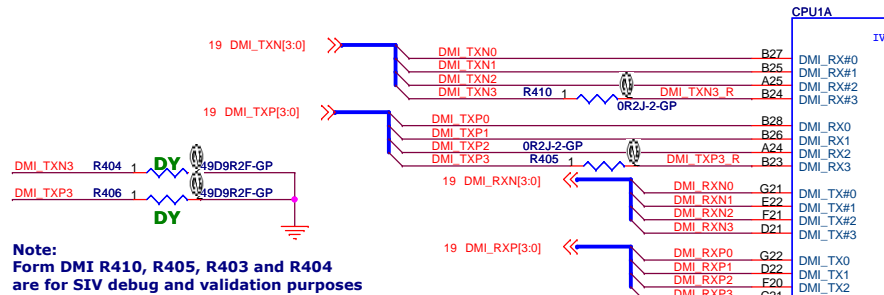
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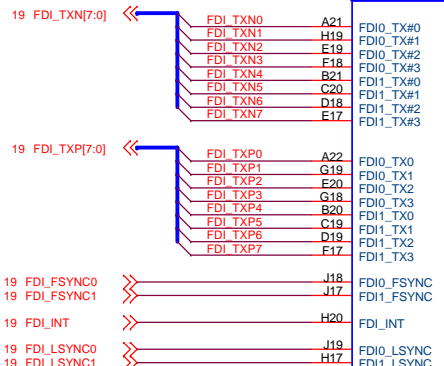
SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

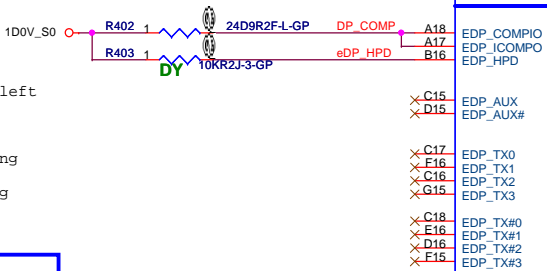
Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.



Note:
Lane reversal does not apply to FDI sideband signals.



Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

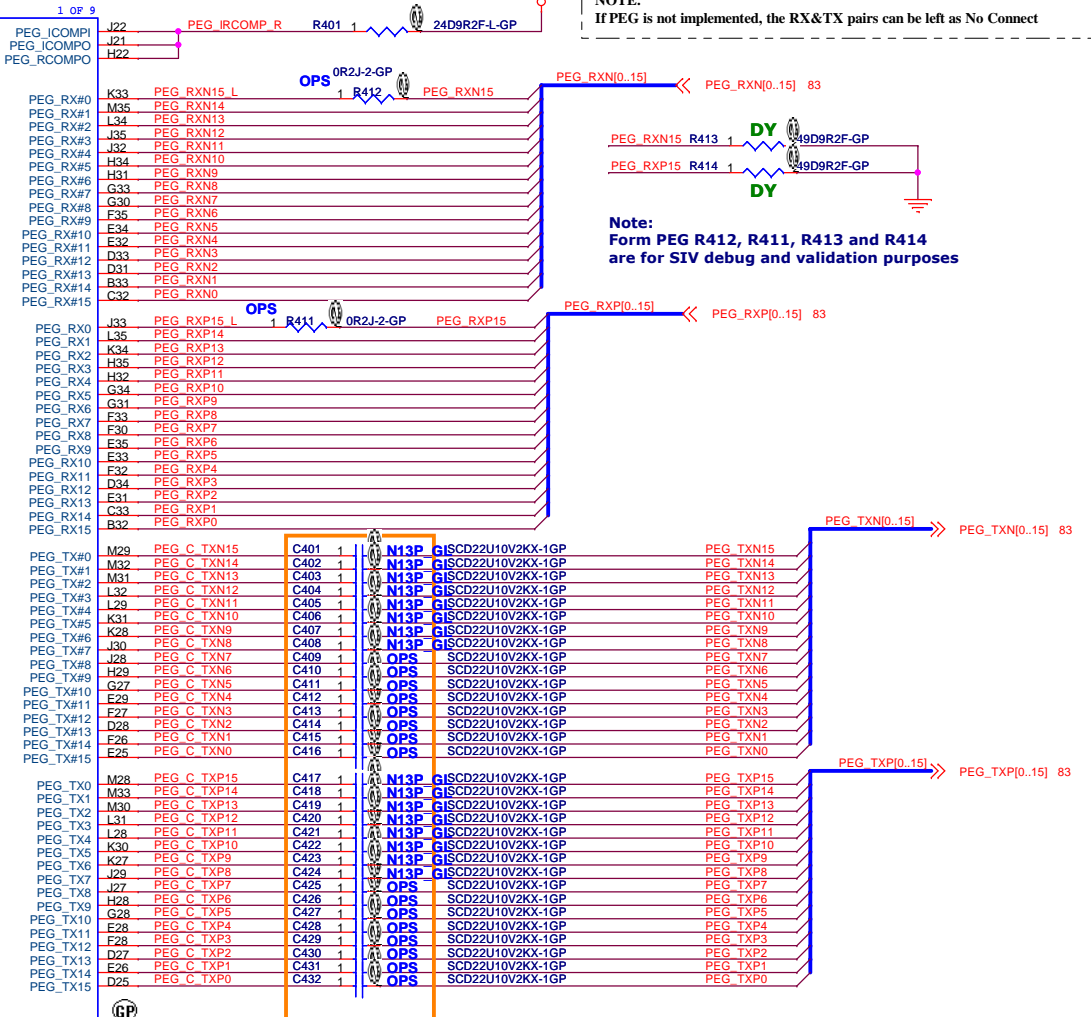
NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.



BOM_CTRL

- 62.10040.821
- 1st = 22.10252.171
- 2nd = 62.10040.821
- 3rd = 62.10055.551



G48-SA Modify
20110601

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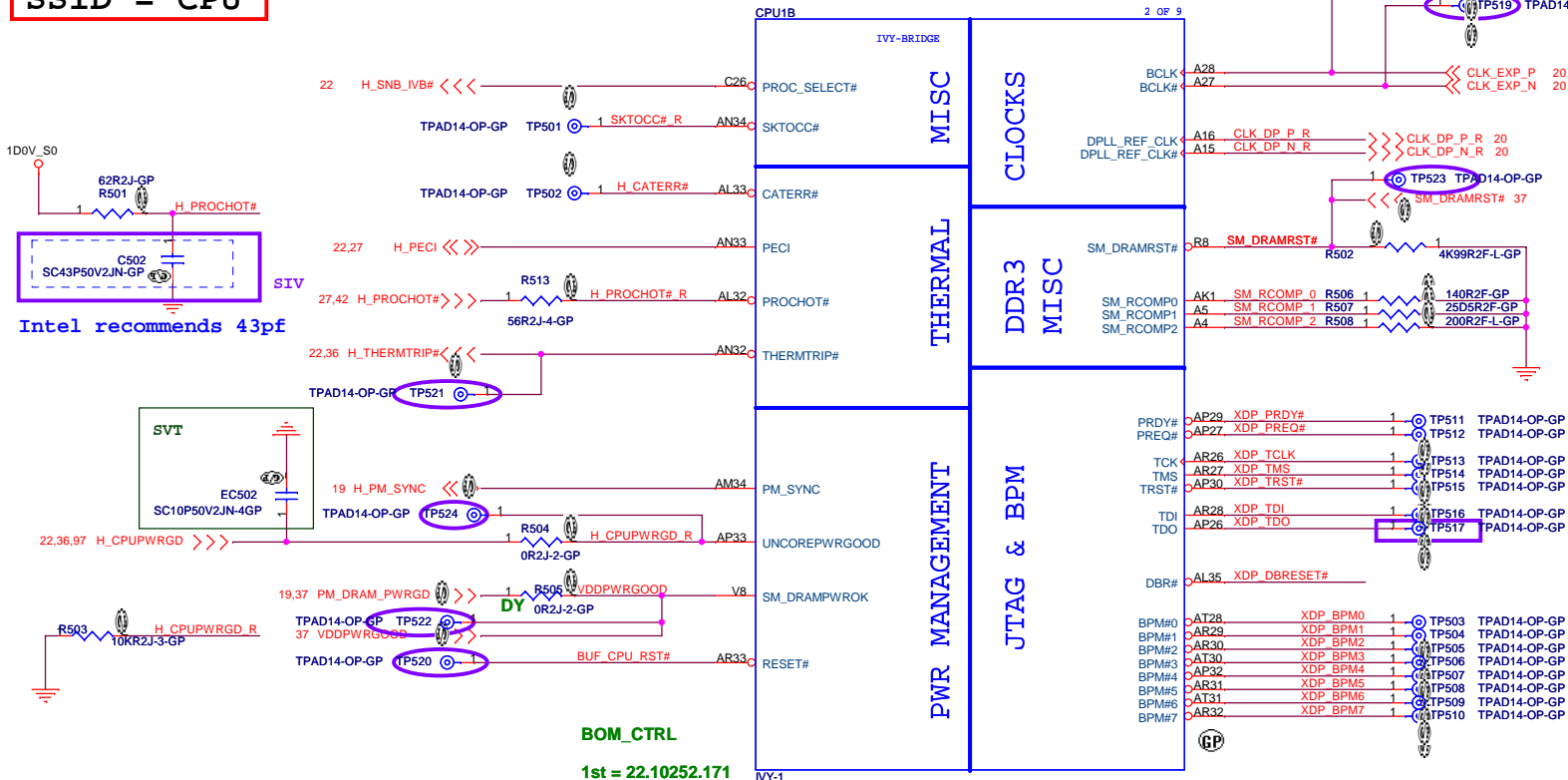
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Title CPU (PCIE/DMI/FDI)

Size A3 Document Number G48/G58 Rev SC

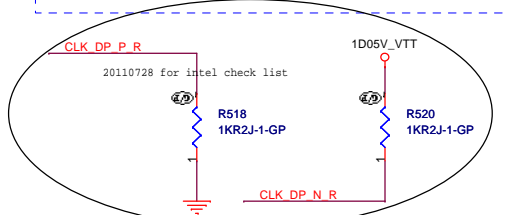
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SSID = CPU

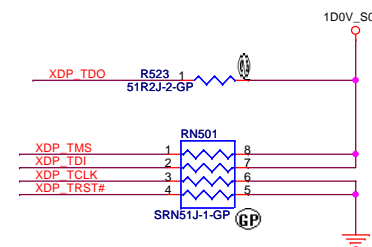


Intel recommends 43pf

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistor (power (~15 mW) may be wasted).



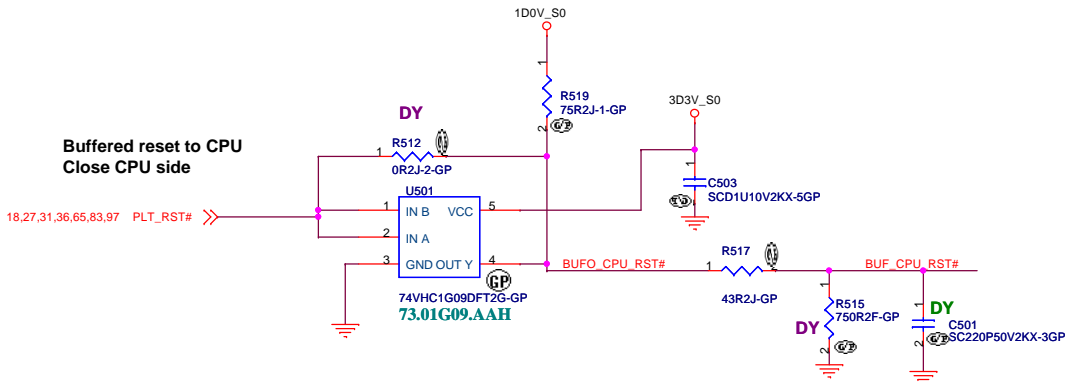
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



BOM_CTRL

- 1st = 22.10252.171
- 2nd = 62.10040.821
- 3rd = 62.10055.551

Buffered reset to CPU
Close CPU side



NOTE

	U501	R512	R519	R517	R515	C503	C501
HR	DY	0 ohm 63.R0034.1DL	DY	1.5K ohm 64.15015.6DL	750 ohm 64.75005.6DL	DY	DY
CRV	73.01G09.AAH	DY	75 ohm 63.75034.1DL	43 ohm 63.43034.1DL	DY	0.1uF 78.10423.2FL	DY

Default CRV

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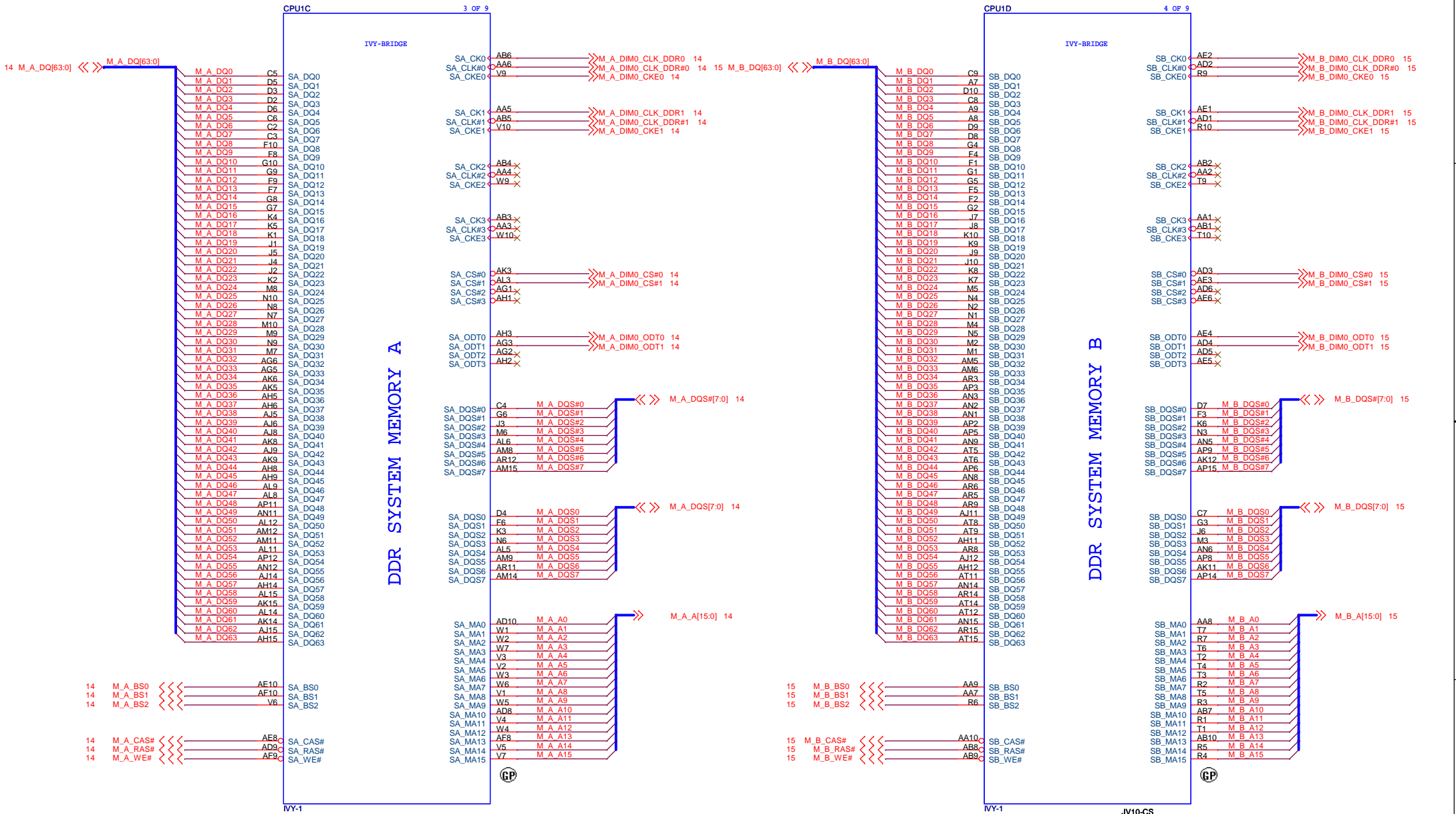
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Title: **THERMAL/CLOCK/PM**

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SSID = CPU



62.10040.821

62.10040.821

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BOM_CTRL

1st = 22.10252.171
 2nd = 62.10040.821
 3rd = 62.10055.551

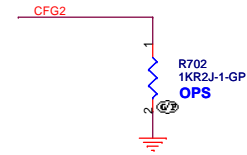
BOM_CTRL

1st = 22.10252.171
 2nd = 62.10040.821
 3rd = 62.10055.551

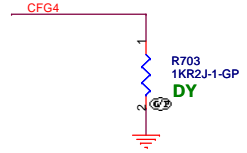
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Title		CPU (DDR)	
Size	Document Number	G48/G58	
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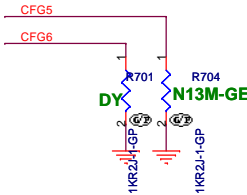
SSID = CPU



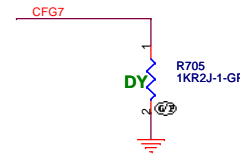
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



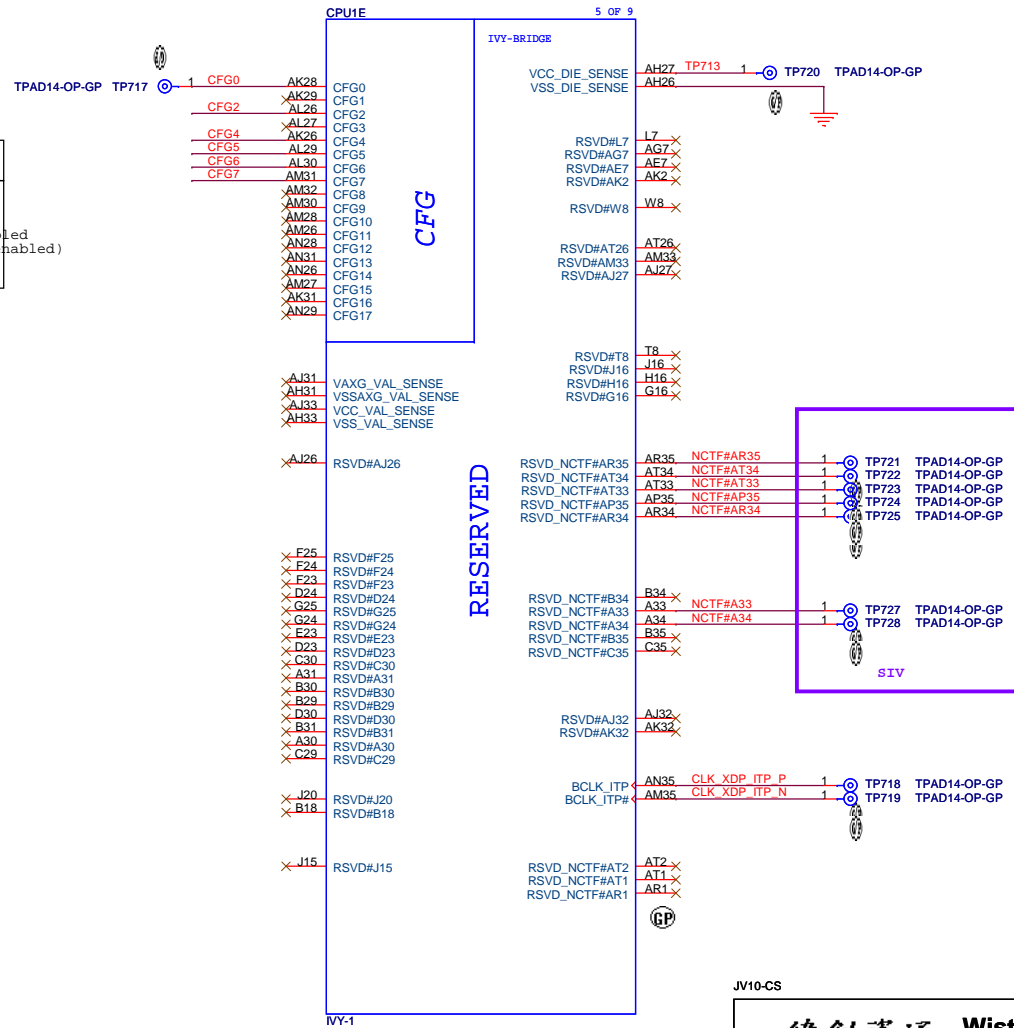
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



62.10040.821

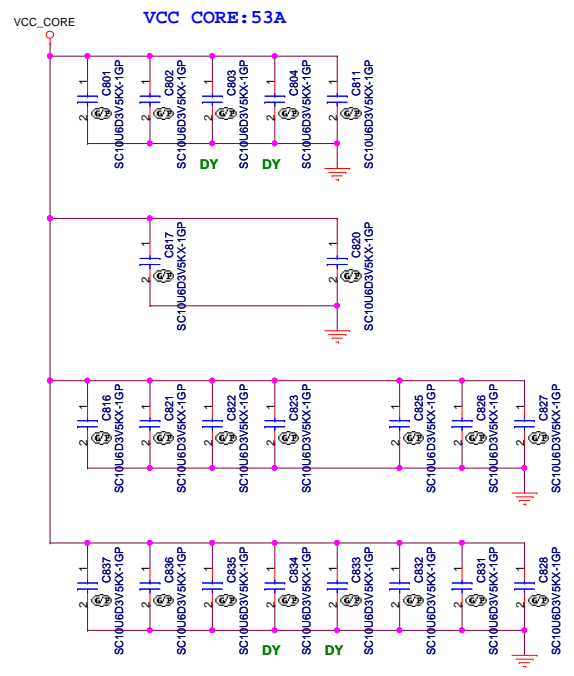
BOM_CTRL

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CPU (RESERVED)	
Title	
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SSID = CPU

CPU1F	POWER	6 OF 9
AG35	VCC1	IVY-BRIDGE
AG34	VCC2	
AG33	VCC3	
AG32	VCC4	
AG31	VCC5	
AG30	VCC6	
AG29	VCC7	
AG28	VCC8	
AG27	VCC9	
AG26	VCC10	
AF35	VCC11	
AF34	VCC12	
AF33	VCC13	
AF32	VCC14	
AF31	VCC15	
AF30	VCC16	
AF29	VCC17	
AF28	VCC18	
AF27	VCC19	
AF26	VCC20	
AD35	VCC21	
AD34	VCC22	
AD33	VCC23	
AD32	VCC24	
AD31	VCC25	
AD30	VCC26	
AD29	VCC27	
AD28	VCC28	
AD27	VCC29	
AD26	VCC30	
AC35	VCC31	
AC34	VCC32	
AC33	VCC33	
AC32	VCC34	
AC31	VCC35	
AC30	VCC36	
AC29	VCC37	
AC28	VCC38	
AC27	VCC39	
AC26	VCC40	
AA35	VCC41	
AA34	VCC42	
AA33	VCC43	
AA32	VCC44	
AA31	VCC45	
AA30	VCC46	
AA29	VCC47	
AA28	VCC48	
AA27	VCC49	
AA26	VCC50	
Y35	VCC51	
Y34	VCC52	
Y33	VCC53	
Y32	VCC54	
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Y30	VCC56	
Y29	VCC57	
Y28	VCC58	
Y27	VCC59	
Y26	VCC60	
V35	VCC61	
V34	VCC62	
V33	VCC63	
V32	VCC64	
V31	VCC65	
V30	VCC66	
V29	VCC67	
V28	VCC68	
V27	VCC69	
V26	VCC70	
U35	VCC71	
U34	VCC72	
U33	VCC73	
U32	VCC74	
U31	VCC75	
U30	VCC76	
U29	VCC77	
U28	VCC78	
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R35	VCC81	
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R30	VCC86	
R29	VCC87	
R28	VCC88	
R27	VCC89	
R26	VCC90	
P35	VCC91	
P34	VCC92	
P33	VCC93	
P32	VCC94	
P31	VCC95	
P30	VCC96	
P29	VCC97	
P28	VCC98	
P27	VCC99	
P26	VCC100	



VCC_CORE

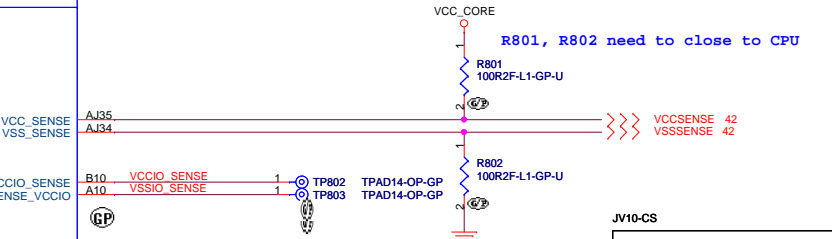
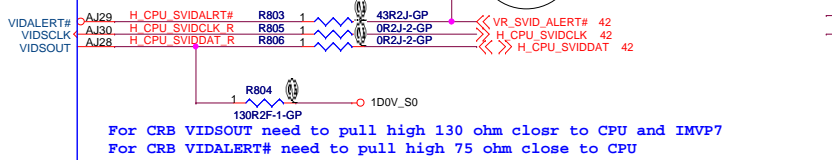
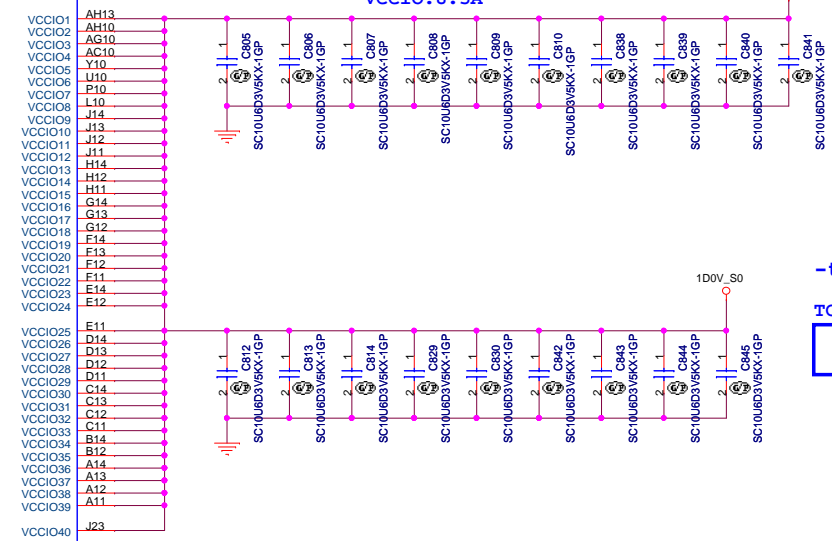
BOM_CTRL

CORE SUPPLY

SVID

SENSE LINES

PEG AND DDR



-to 17pcs
TC8xx
470uF x2

R807 need to close to CPU



For CRB VIDSKL need to pull high 130 ohm closer to CPU and IMPV7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

R801, R802 need to close to CPU

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Title: **mCPU (VCC_CORE)**

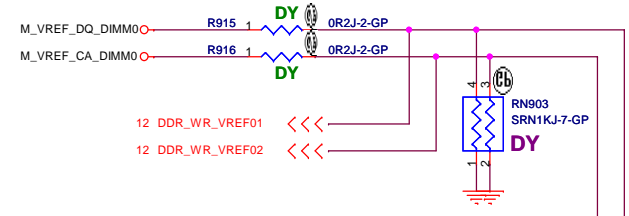
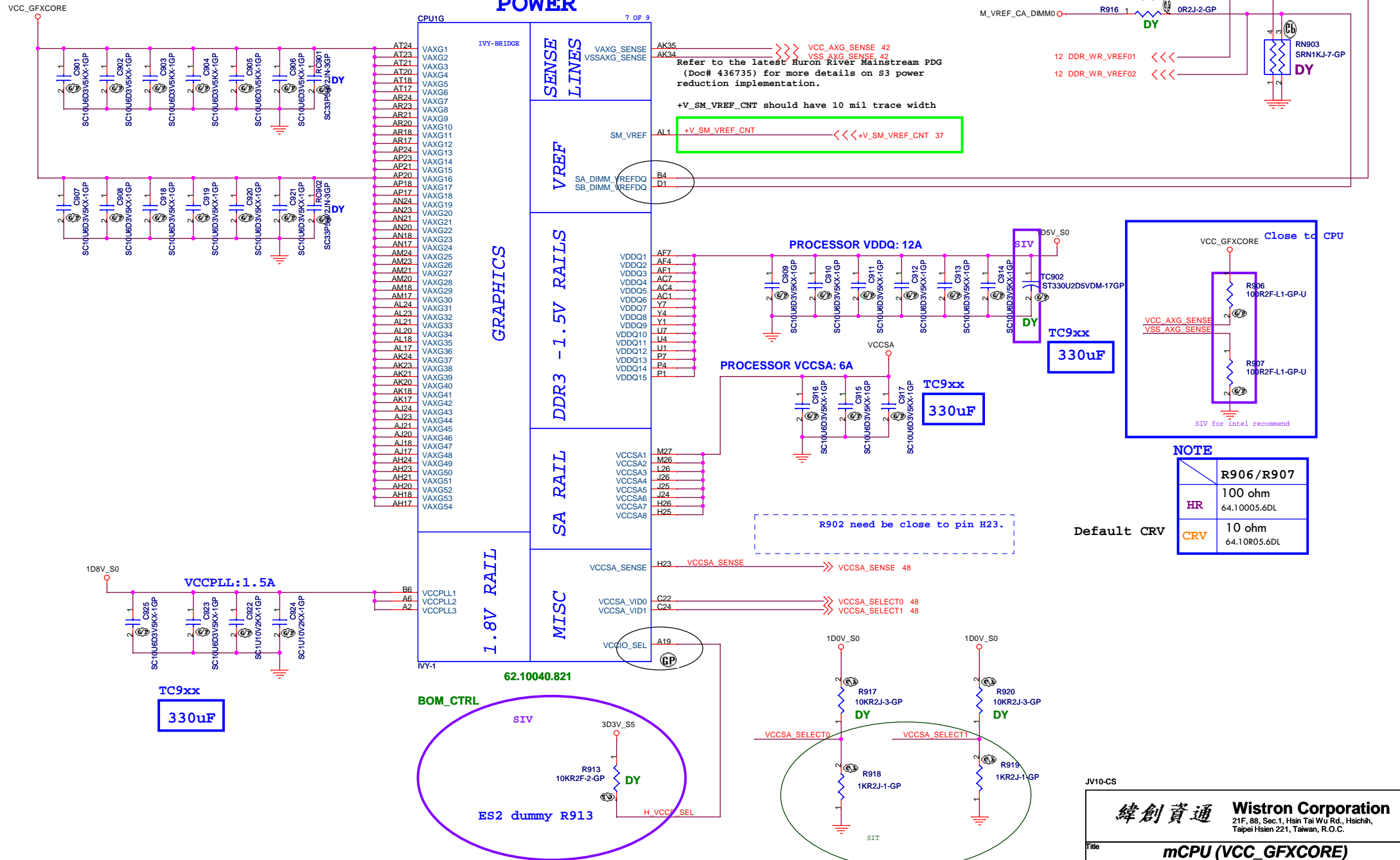
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SSID = CPU

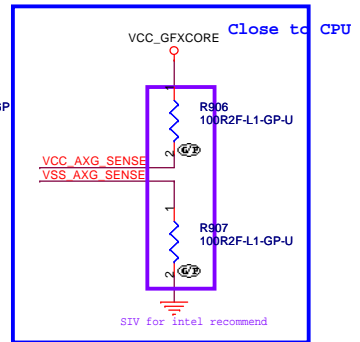
Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

M3 - Processor Generated SO-DIMM VREF_DQ



Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

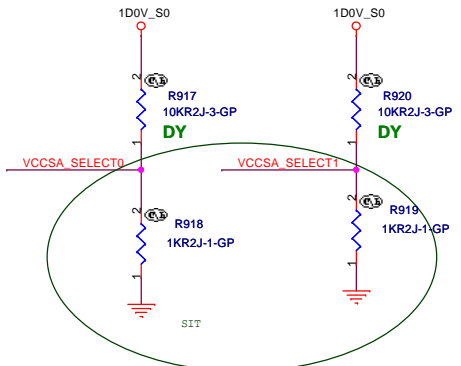
+V_SM_VREF_CNT should have 10 mil trace width



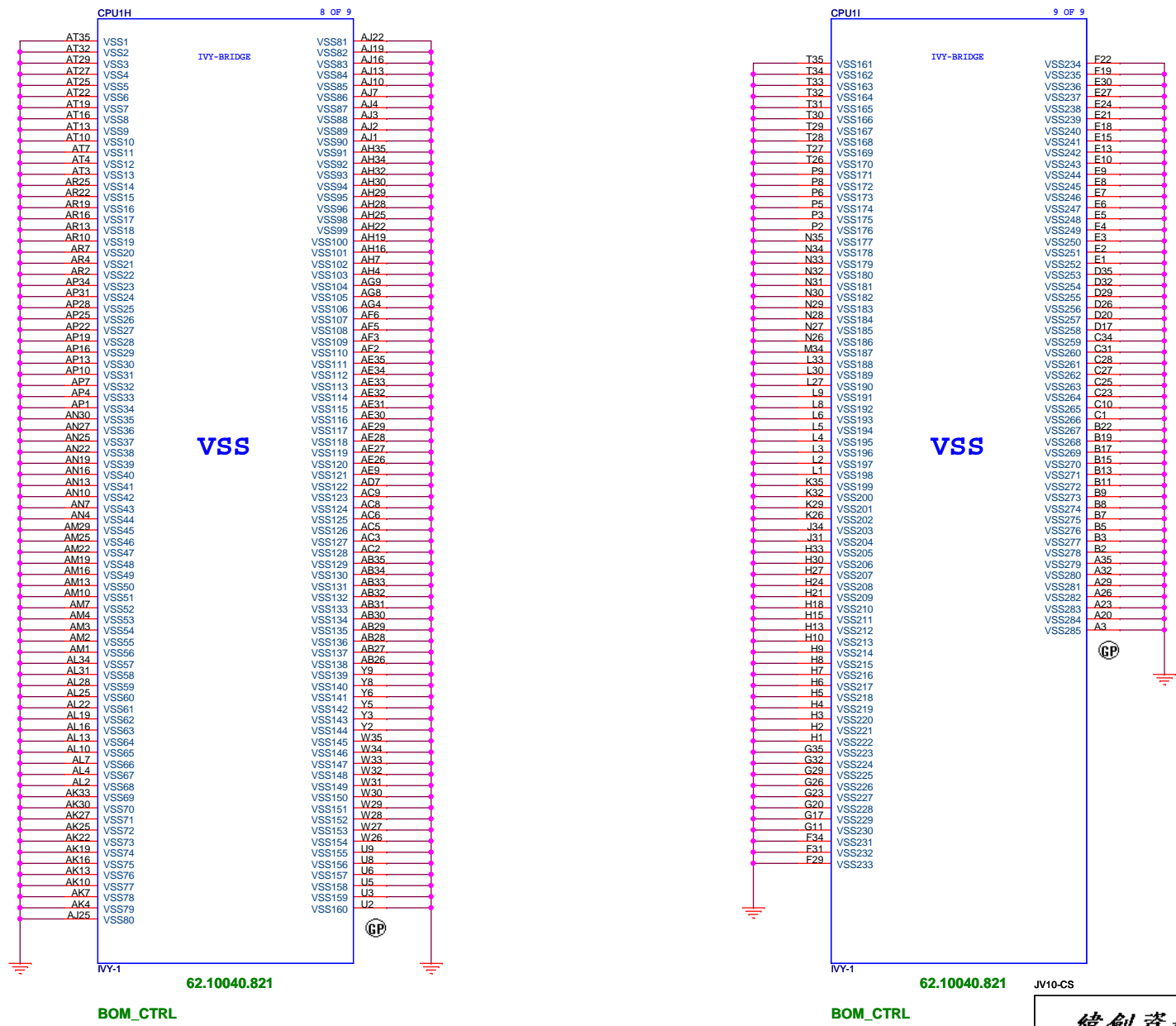
NOTE

	R906/R907
HR	100 ohm 64.10005.6DL
CRV	10 ohm 64.10R05.6DL

Default CRV



SSID = CPU



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Title: **CPU(VSS)**

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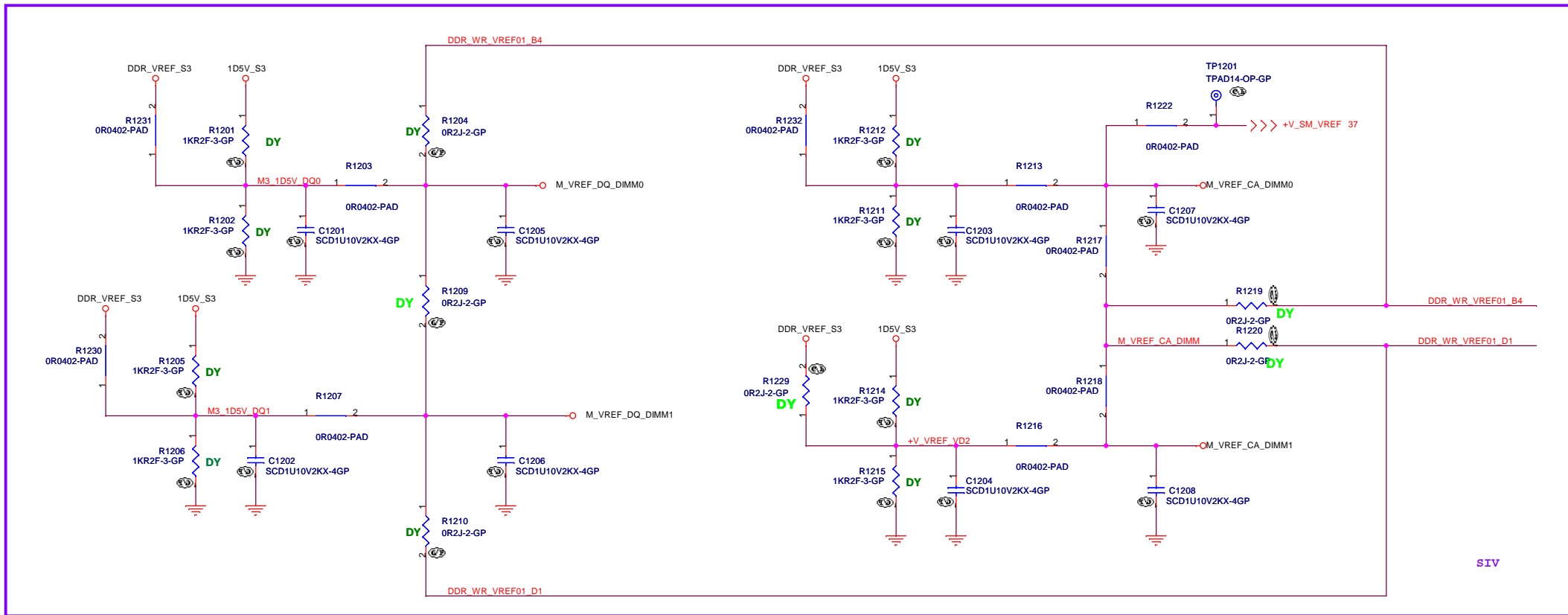
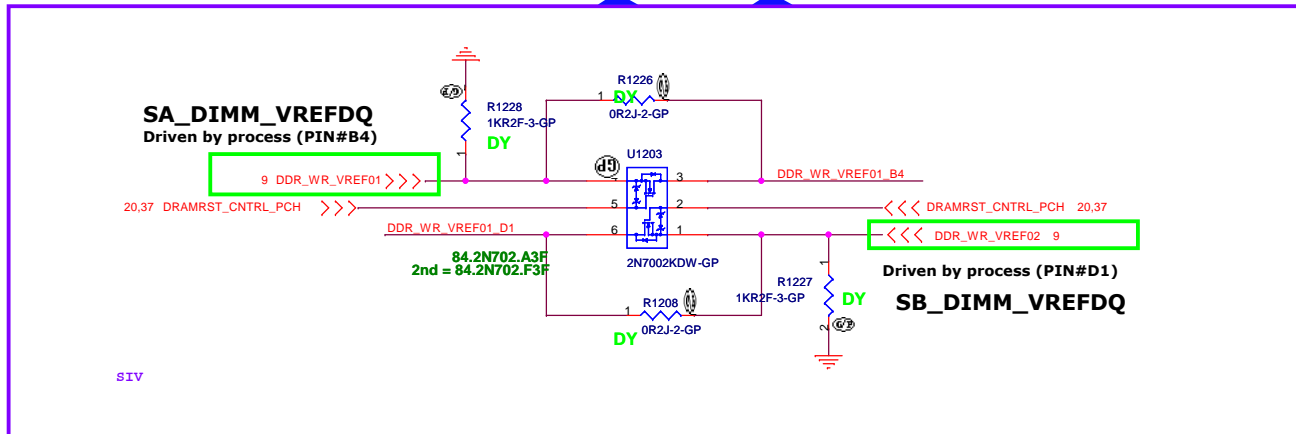
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VREF circuit -M1 (Voltage Driver Network) & M3 (Driver Processor) Implementation

For CRV:



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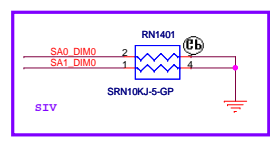
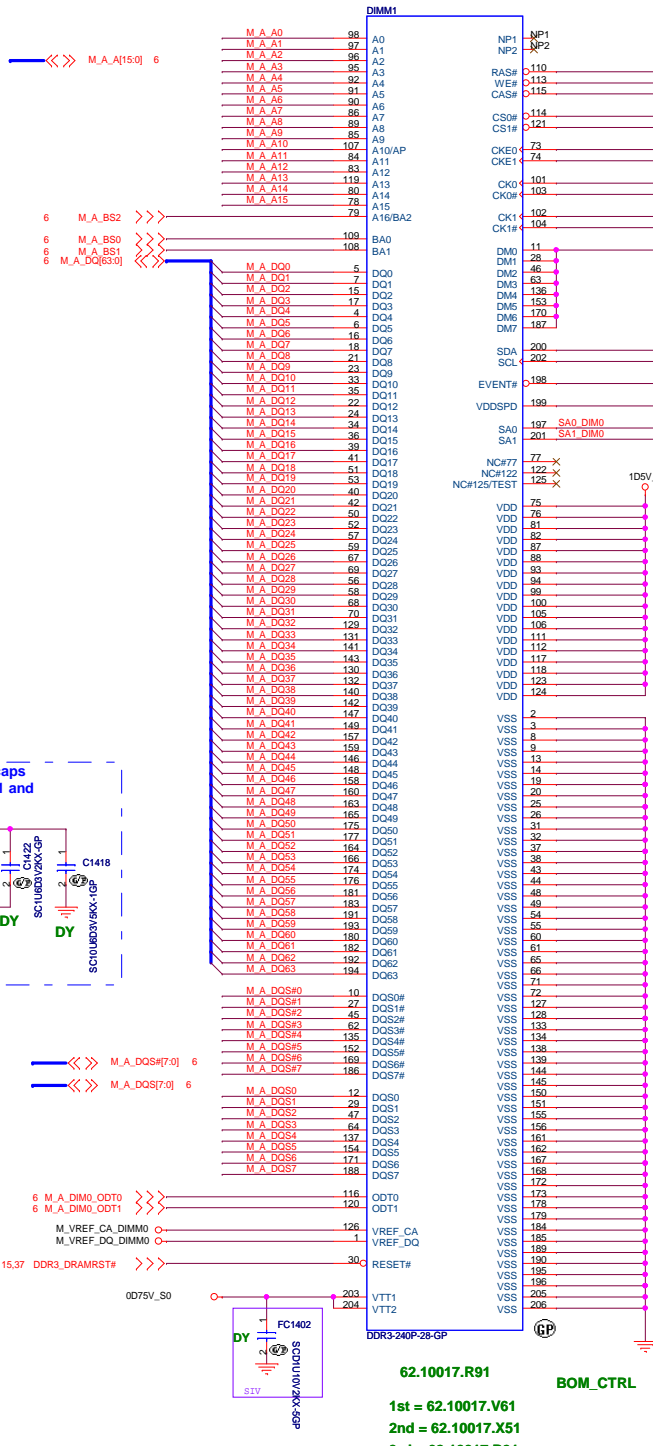
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Size Document Number	G48/G58
Date: Friday, February 17, 2012	Rev SC
Sheet 12 of 103	

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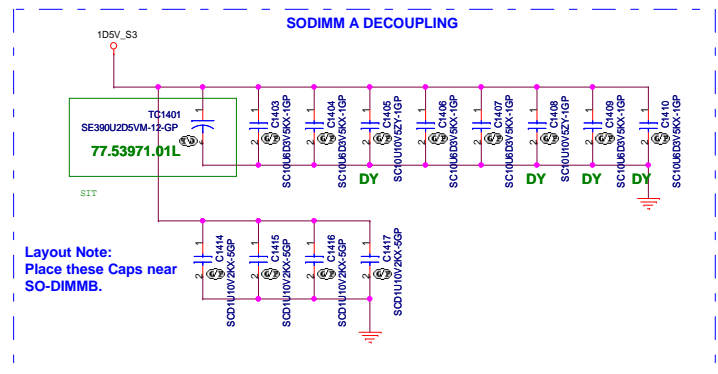
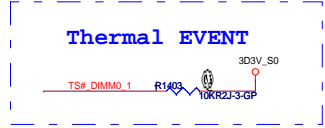
JV10-CS

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Title Reserved			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 13	of 103

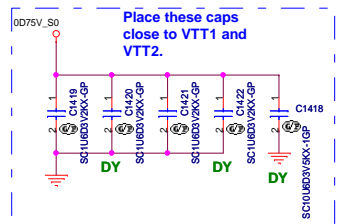
SSID = MEMORY



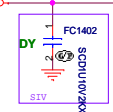
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0x40
SO-DIMMA TS Address is 0x30
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Layout Note:
Place these Caps near SO-DIMMB.



Place these caps close to VTT1 and VTT2.



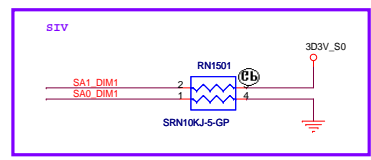
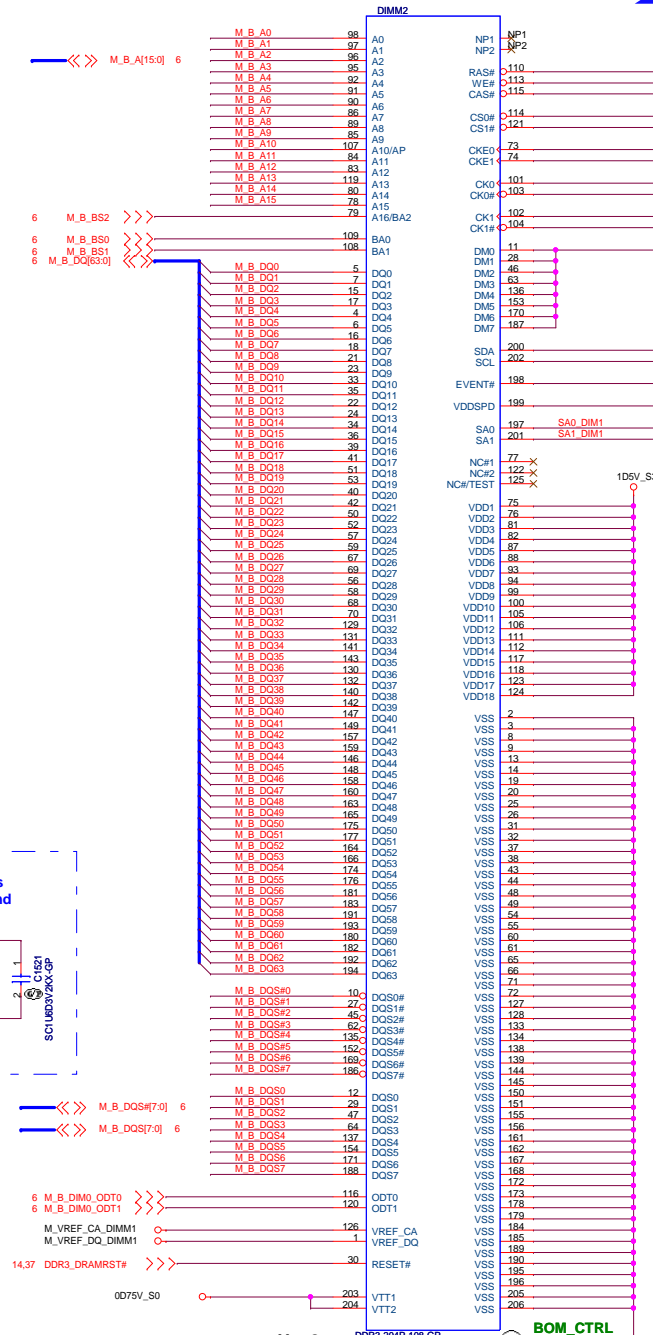
62.10017.R91 BOM_CTRL
1st = 62.10017.V61
2nd = 62.10017.X51
3rd = 62.10017.R91

After layout, BOM change P/N

JV10-CS

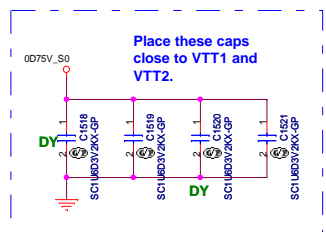
Wistron Corporation
DDR3-SODIMM1
Document Number G48/G58
Date: Friday, February 17, 2012 Sheet 14 of 103

SSID = MEMORY

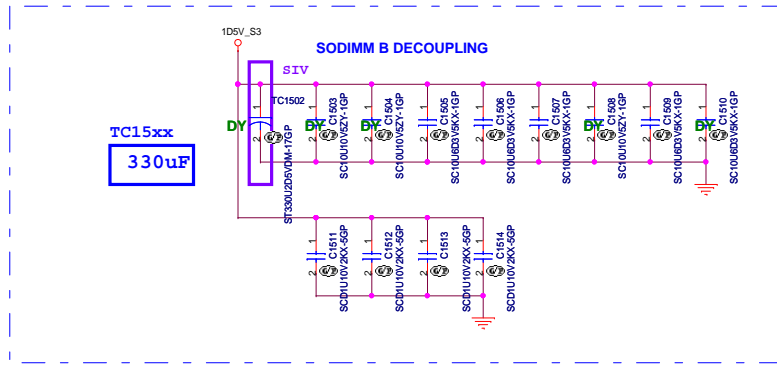


Note:
SO-DIMM SPD Address is 0x4
SO-DIMM TS Address is 0x34

SO-DIMM is placed farther from the Processor than SO-DIMMA



Place these caps close to VTT1 and VTT2.



After layout, BOM change P/N

- H = 8mm DDR3-204P-108-GP
- 62.10017.X41
 - 1st = 62.10024.G21
 - 2nd = 62.10017.X41
 - 3rd = 62.10017.M51

JV10-CS

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Title: **DDR3-SODIMM2**

Size: Document Number **G48/G58** Rev **SC**

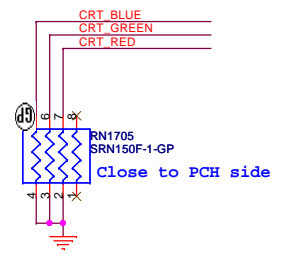
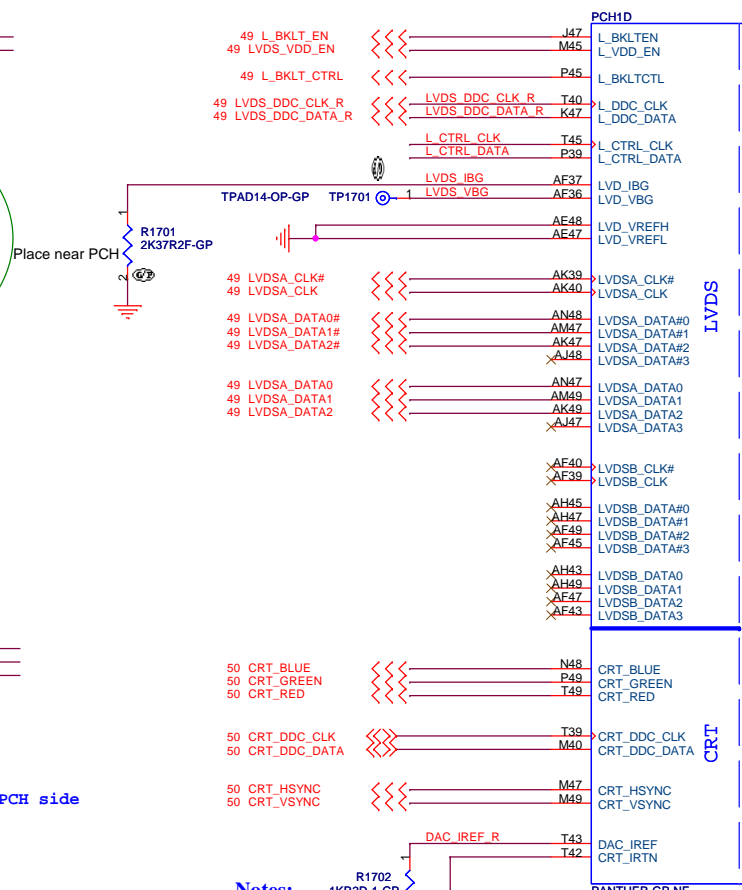
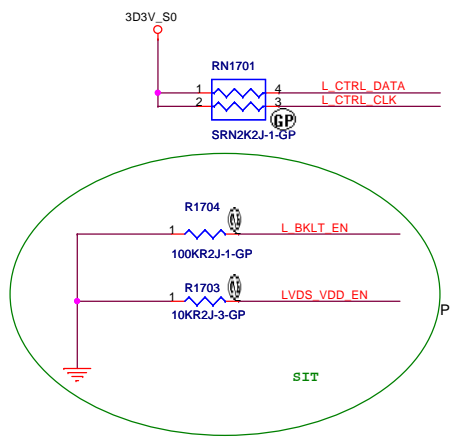
Date: Friday, February 17, 2012 Sheet 15 of 103

(Blanking)

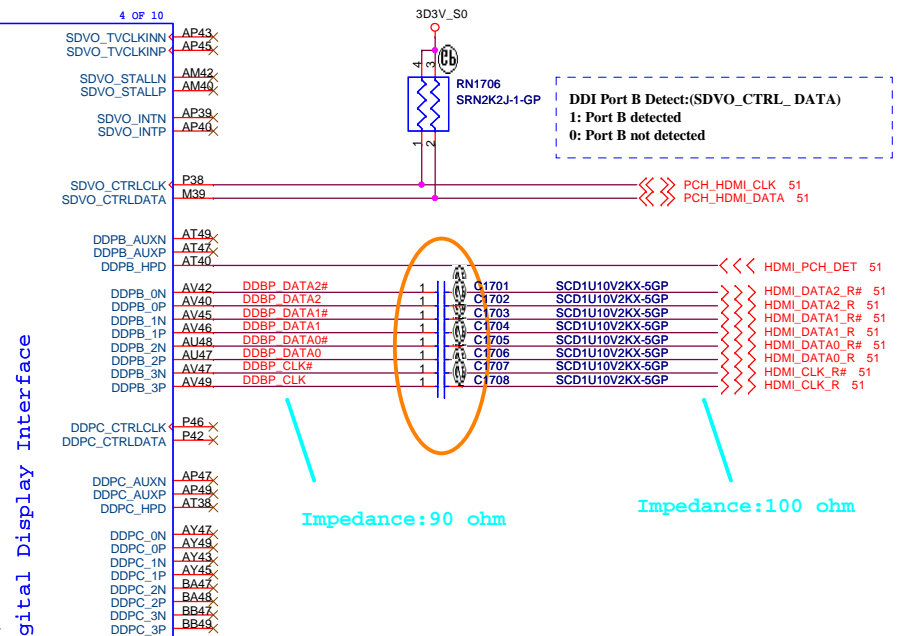
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Title			
DDR3-SODIMM3			
Size	Document Number	G48/G58	Rev
			SC
Date: Friday, February 17, 2012		Sheet 16	of 103

L_DDC_DATA(K47):
 This signal is on the LVDS interface.
 This signal needs to be left NC if eDP is
 used for the local flat panel display



Notes:
 1K 0.5% 0402.



DDI Port B Detect:(SDVO_CTRL_DATA)
 1: Port B detected
 0: Port B not detected

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPDP	NA	DDPB_HPDP	HDMIB_HPDP
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

BOM_CTRL
SIV = 71.PANTH.DOU
PCH料號: 71.PANTH.DOU

JV10-CS

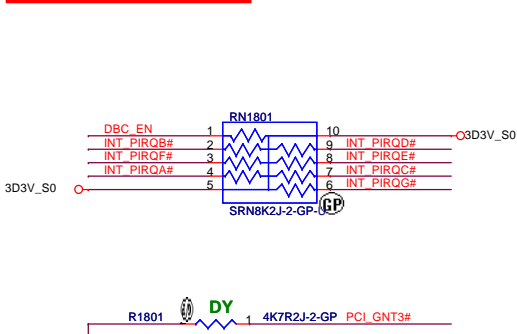
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/HDMI)**

Size: Document Number **G48/G58** Rev **SC**

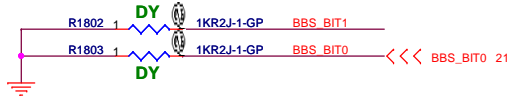
Date: Friday, February 17, 2012 Sheet 17 of 103

SSID = PCH

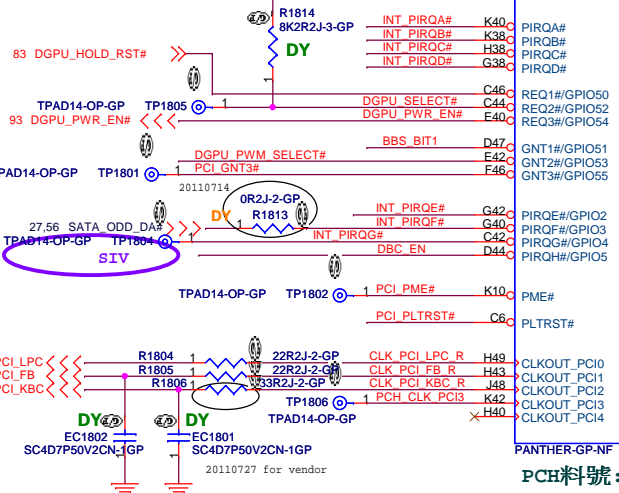
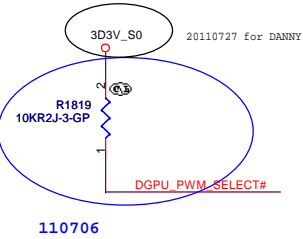


A16 swap override Strap/Top-Block Swap Override jumper

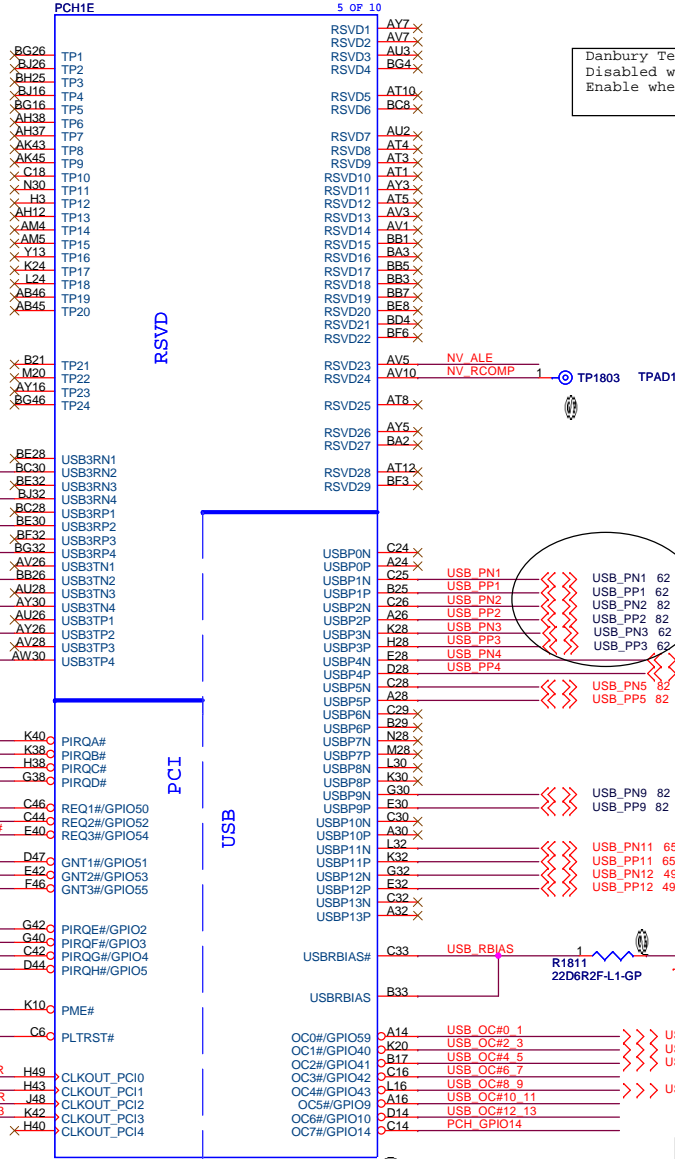
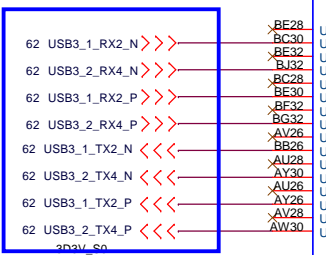
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-----------	---



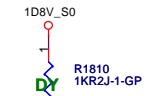
BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



For PPT USB3.0 feature



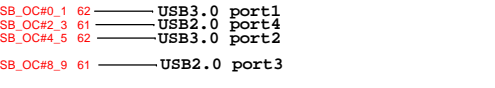
Danbury Technology:
Disabled when Low.
Enable when High.



USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

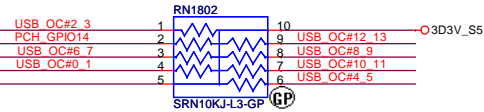
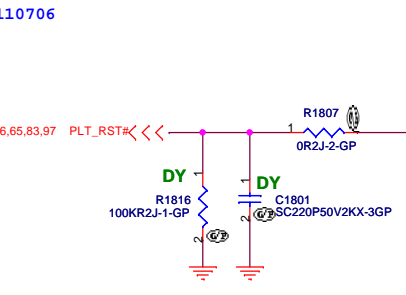
Utilize Port 9 for USB debug



Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

PCH料號: 71.PANTH.00U

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)



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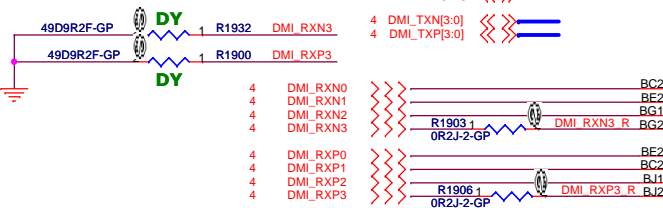
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI/USB/NVRAM)**

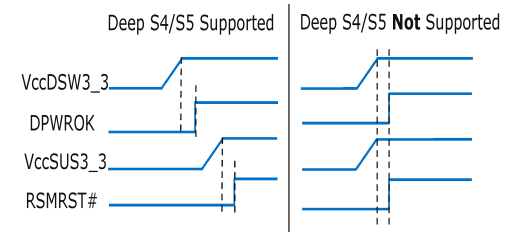
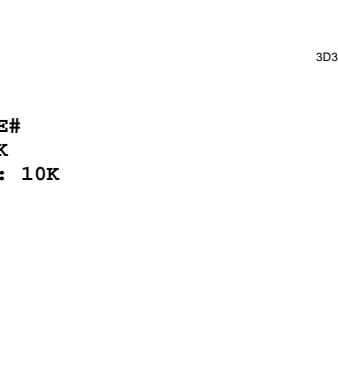
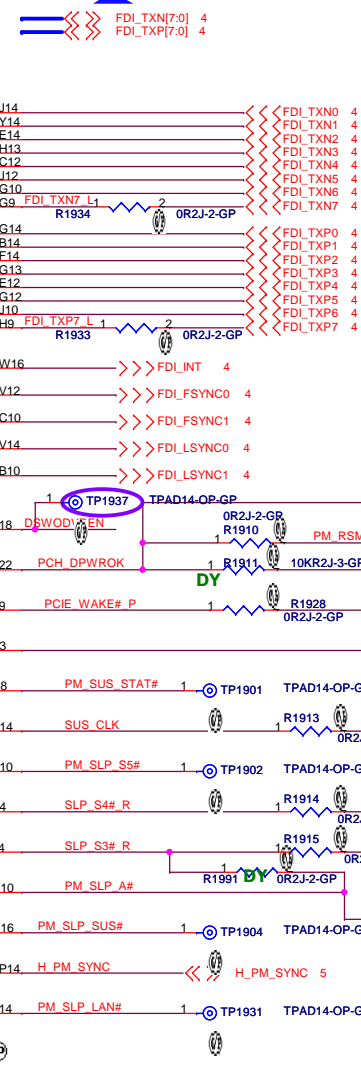
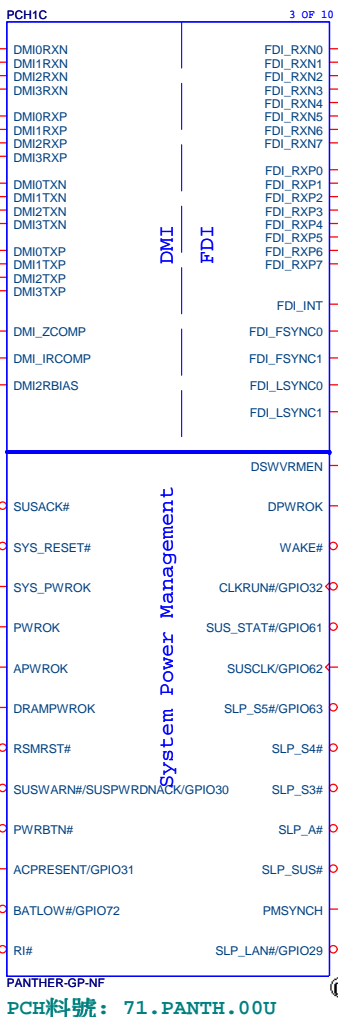
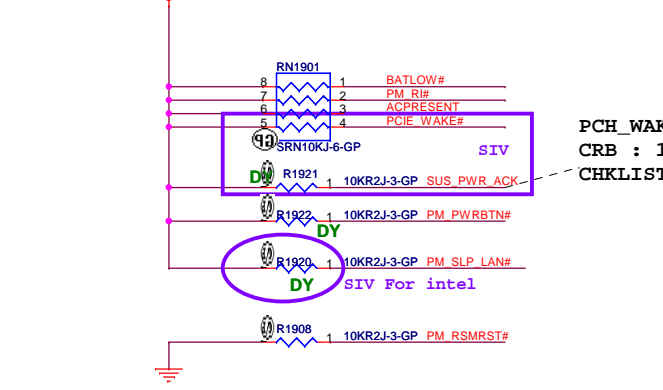
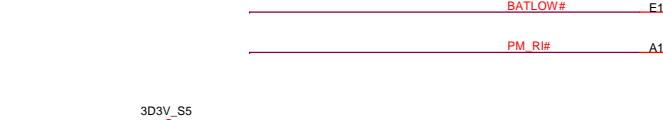
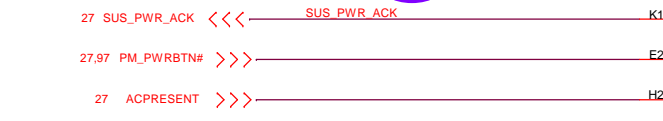
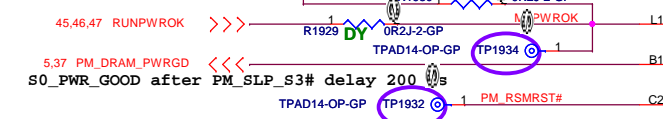
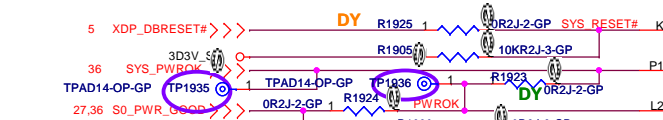
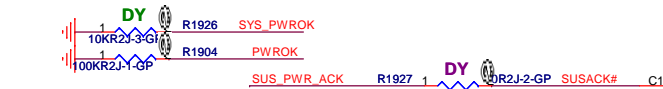
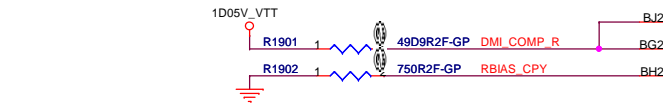
Size: Document Number **G48/G58** Rev **SC**

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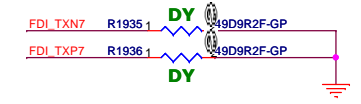
SSID = PCH



Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

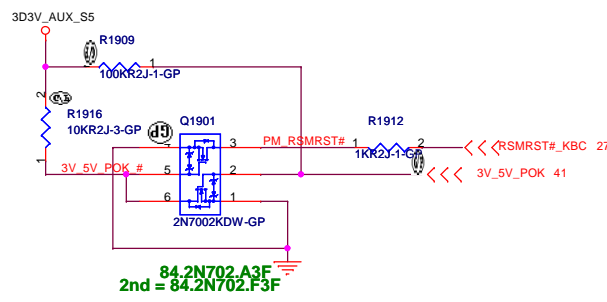
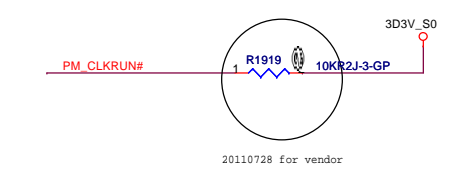


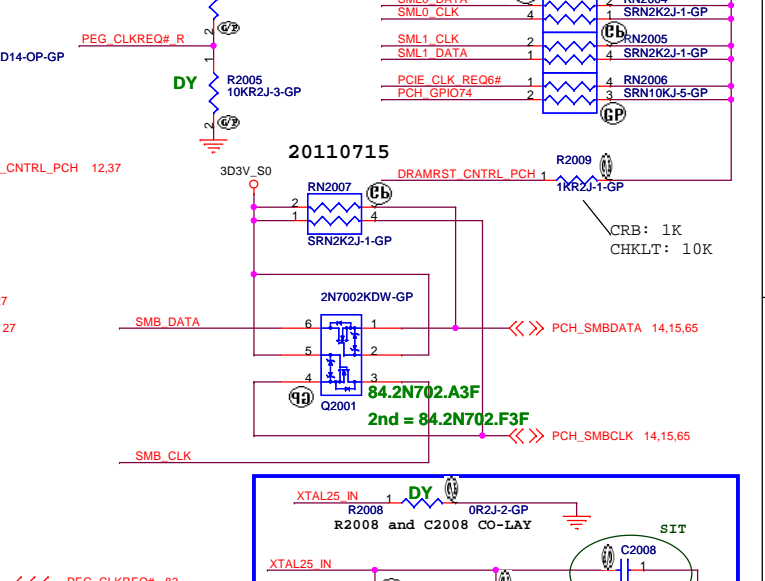
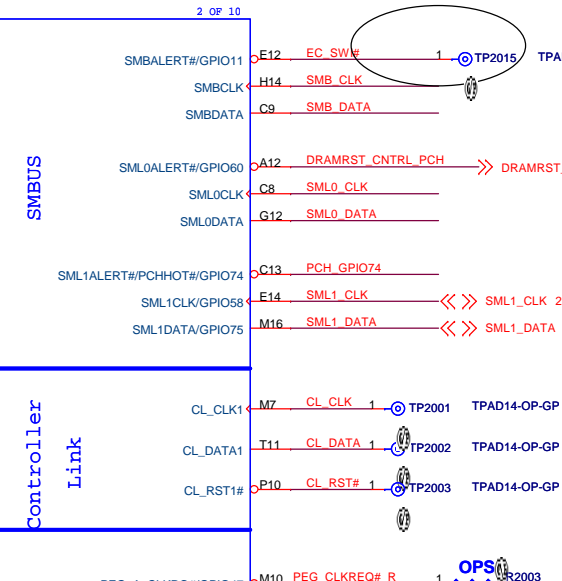
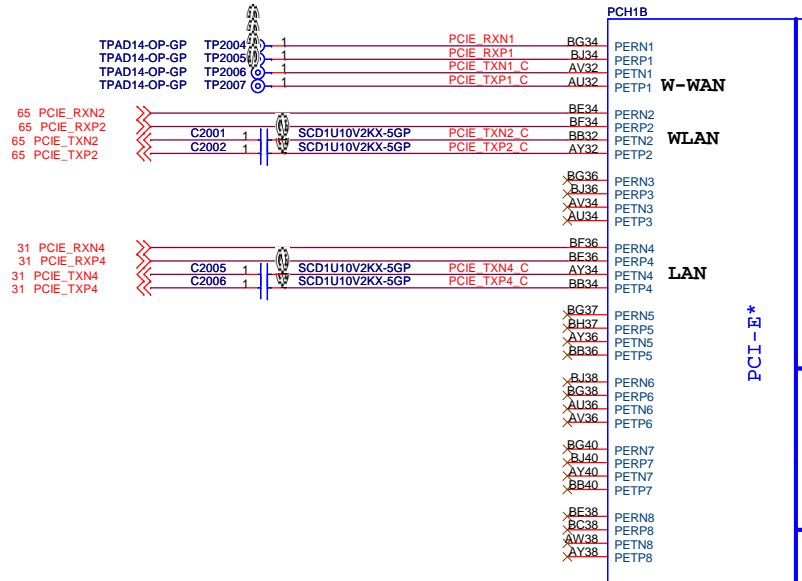
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30



DSWODVREN - On Die DSW VR Enable

Signal	State
HIGH	Enabled (DEFAULT)
LOW	Disabled

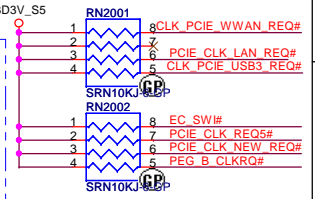
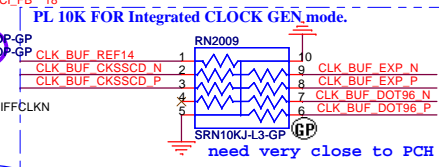
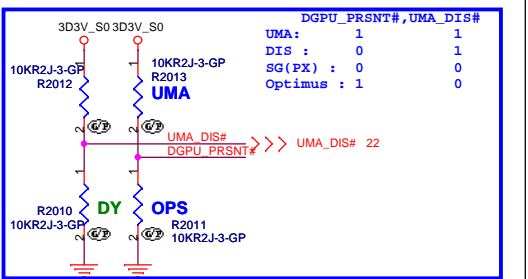
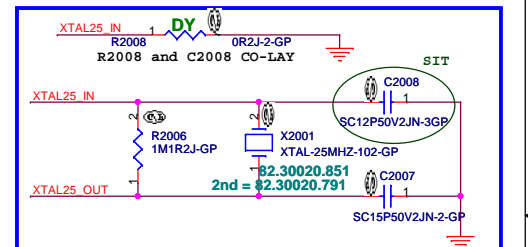
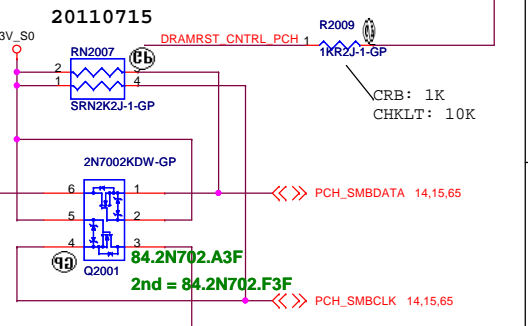
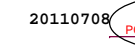
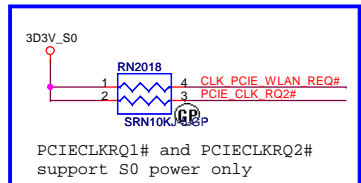




WWAN CLK

WLAN CLK

LAN CLK



TPAD14-OP-GP TP2010 1 PCIE_CLK_XDP_N AK14
TPAD14-OP-GP TP2011 1 PCIE_CLK_XDP_P AK13

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

PCH料號: 71.PANTH.00U

JV10-CS

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **PCH (PCI-E/SMBUS/CLOCK/CL)**

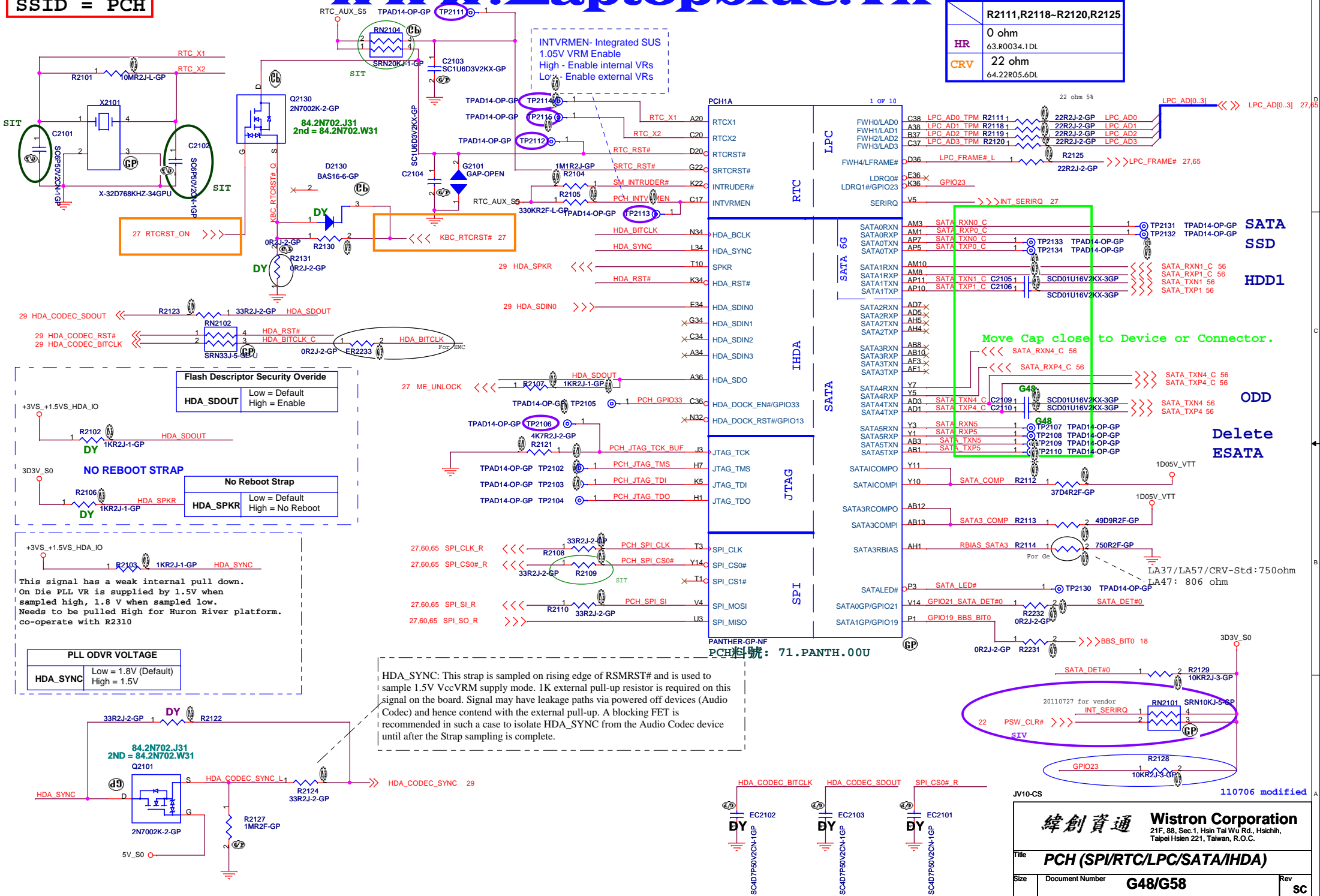
Size Document Number **G48/G58** Rev **SC**

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SSID = PCH

NOTE

	R2111,R2118-R2120,R2125
HR	0 ohm 63.R0034.1DL
CRV	22 ohm 64.22R05.6DL



INTVRMEN- Integrated SUS
 1.05V VRM Enable
 High - Enable internal VRs
 Lo - Enable external VRs

Move Cap close to Device or Connector.

Flash Descriptor Security Override
 HDA_SDOUT Low = Default
 High = Enable

NO REBOOT STRAP
 HDA_SPKR Low = Default
 High = No Reboot

PLL ODVR VOLTAGE
 HDA_SYNC Low = 1.8V (Default)
 High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

110706 modified

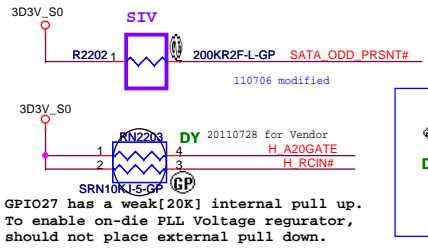
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size Document Number **G48/G58** Rev **SC**

Date: Friday, February 17, 2012 Sheet 21 of 103

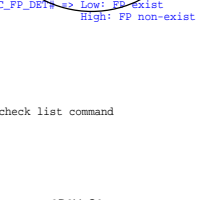
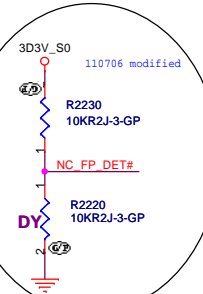
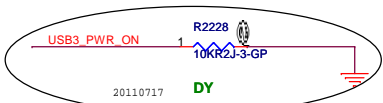
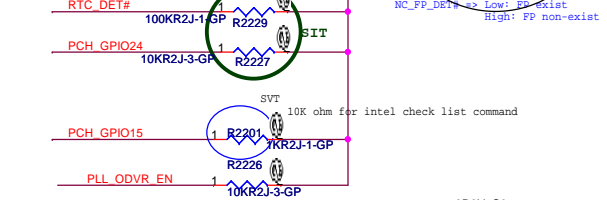
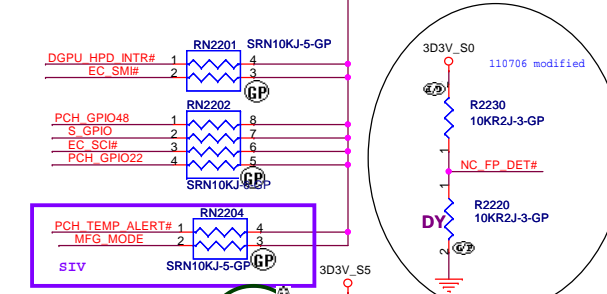
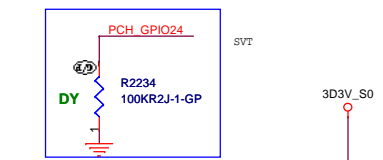
	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



Note

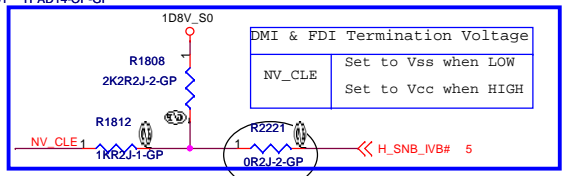
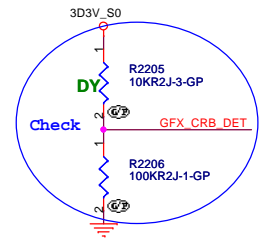
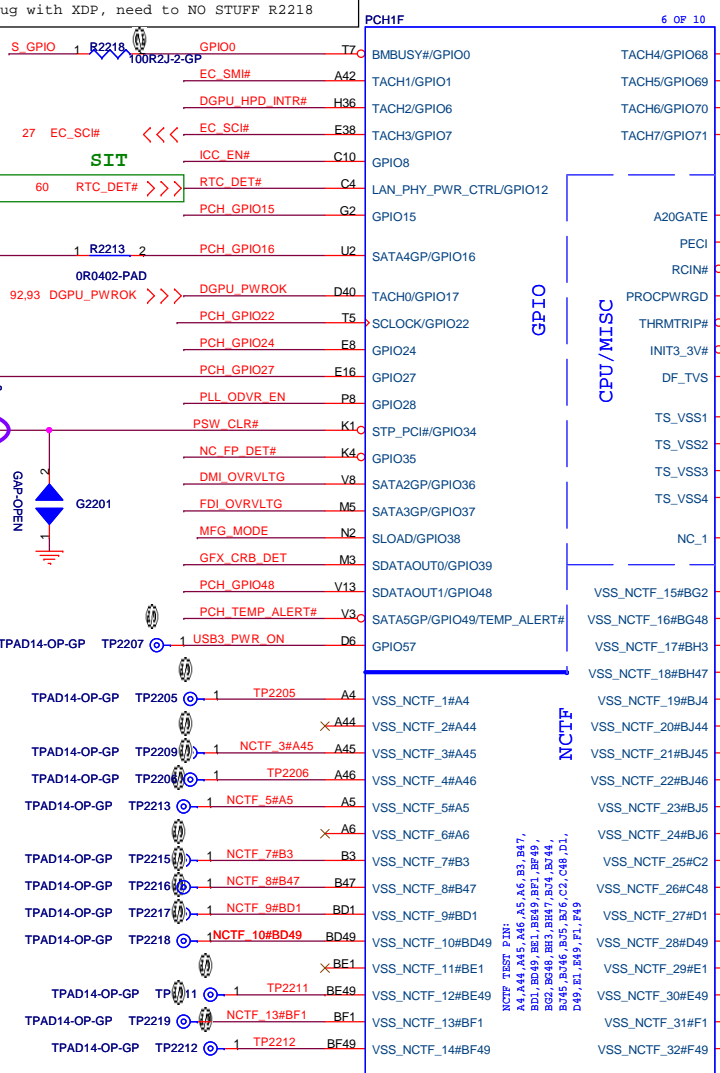
	R2202	----
HR	200K ohm 64.20035.6DL	
CRB	10K ohm 63.10334.1DL	

PCH_GPIO15 pull high => HM76
PCH_GPIO15 pull Low => HM70



PLL ON DIE VR ENABLE

NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE

GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE

GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

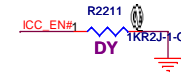
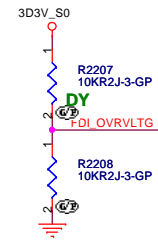
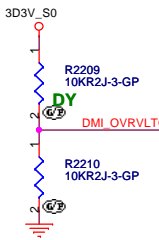
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable

ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT]
	LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up. Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PANTHER-GP-NF
PCH料號: 71.PANTH.00U



JV10-CS

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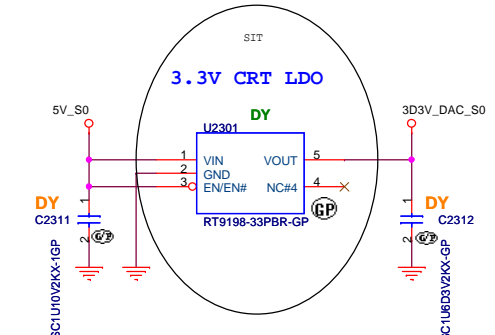
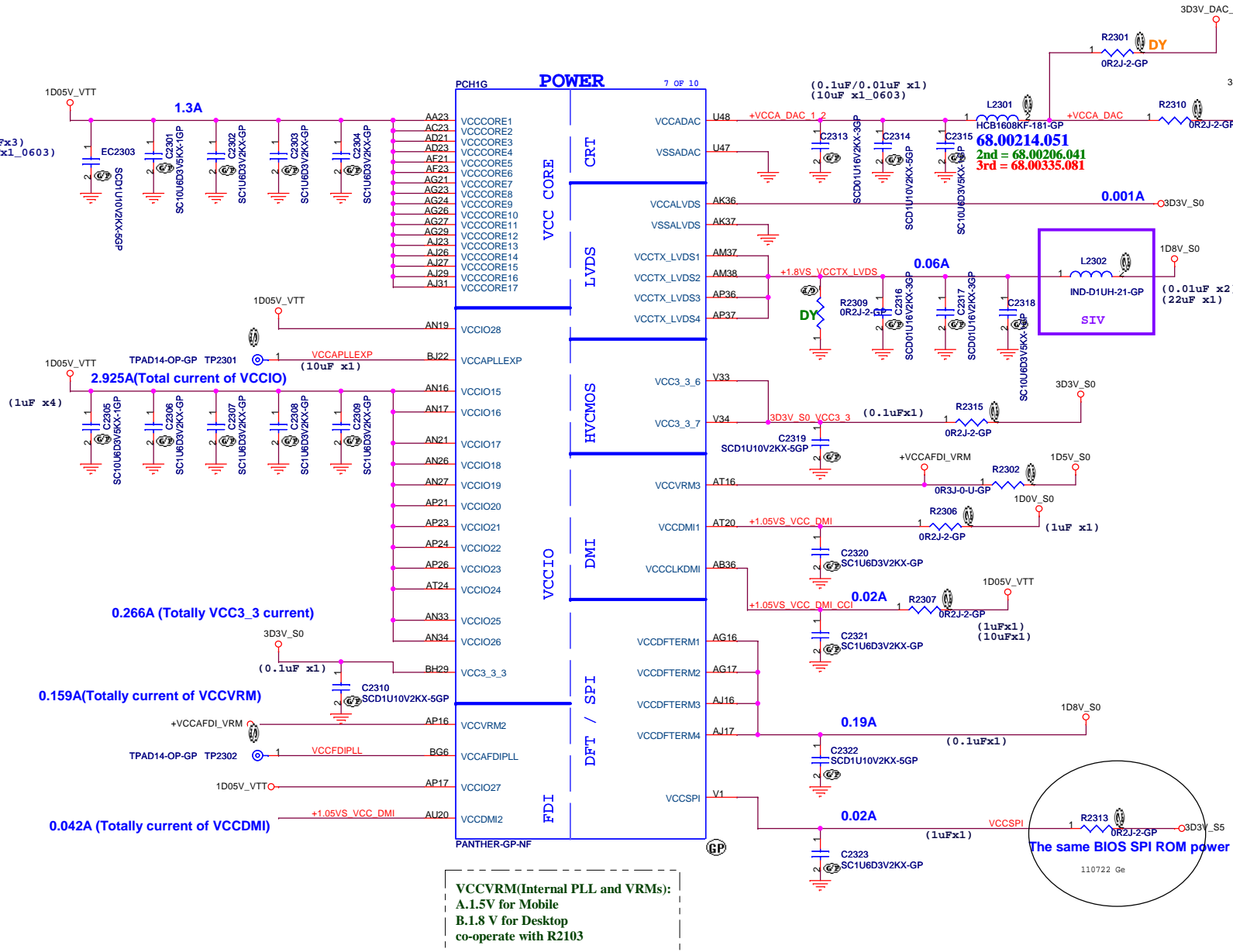
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size: Document Number **G48/G58** Rev **SC**

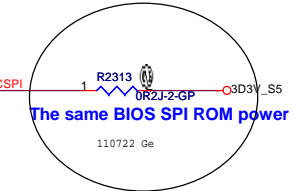
Date: Friday, February 17, 2012 Sheet 22 of 103

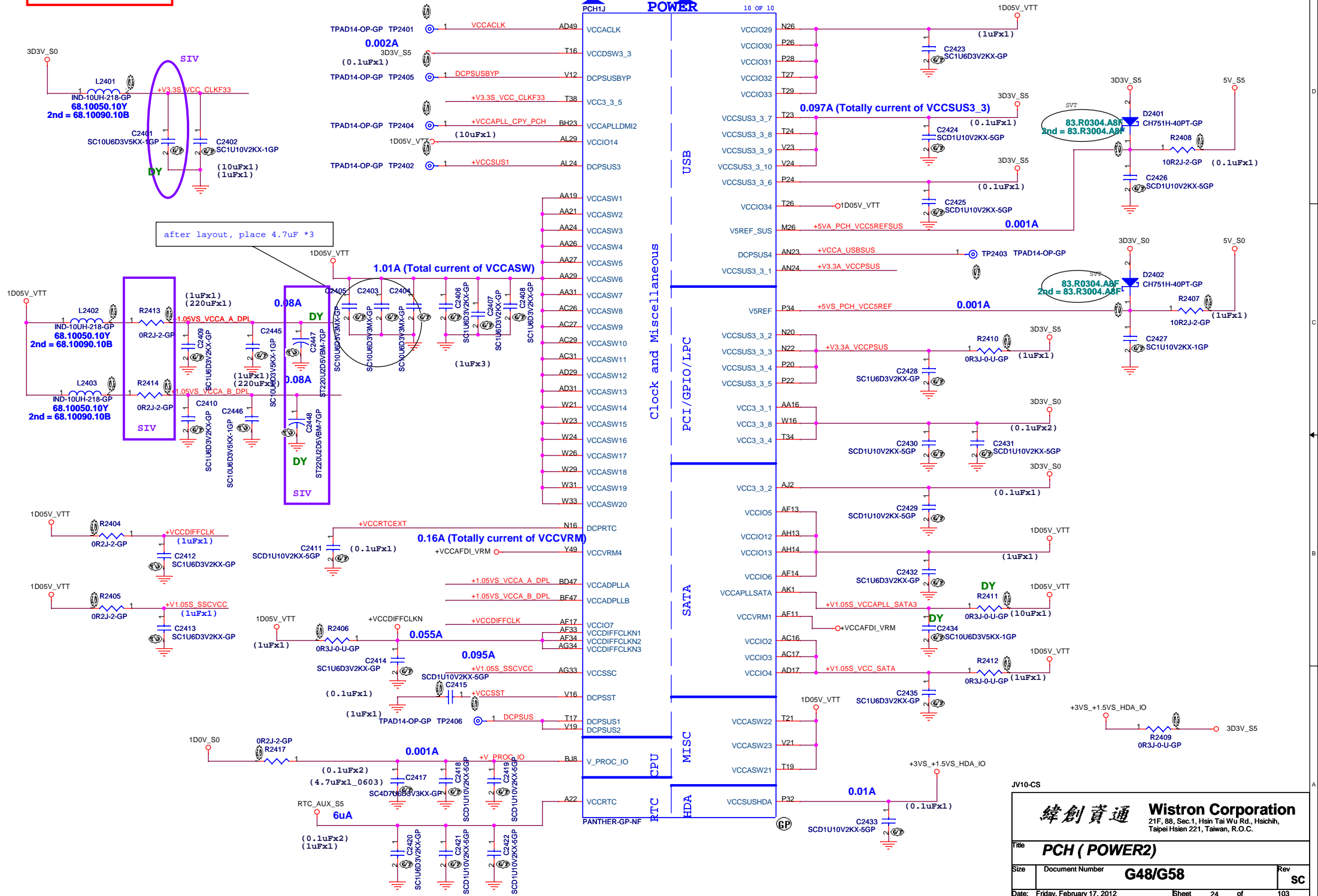
SSID = PCH 6A



Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture





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Title	PCH (POWER2)		
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		Sheet 24 of	103

SSID = PCH

PCH1H 8 OF 10

H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK1
AA3	VSS3	VSS82	AK42
AA34	VSS4	VSS83	AK46
AB11	VSS5	VSS84	AK8
AB14	VSS6	VSS85	AL16
AB39	VSS7	VSS86	AL17
AB4	VSS8	VSS87	AL19
AB43	VSS9	VSS88	AL2
AB5	VSS10	VSS89	AL23
AB7	VSS11	VSS90	AL26
AC19	VSS12	VSS91	AL27
AC2	VSS13	VSS92	AL31
AC21	VSS14	VSS93	AL33
AC24	VSS15	VSS94	AL34
AC33	VSS16	VSS95	AL48
AC34	VSS17	VSS96	AM11
AC48	VSS18	VSS97	AM14
AD10	VSS19	VSS98	AM36
AD11	VSS20	VSS99	AM39
AD12	VSS21	VSS100	AM43
AD13	VSS22	VSS101	AM45
AD19	VSS23	VSS102	AM46
AD24	VSS24	VSS103	AM7
AD26	VSS25	VSS104	AN2
AD27	VSS26	VSS105	AN29
AD33	VSS27	VSS106	AN3
AD34	VSS28	VSS107	AN31
AD36	VSS29	VSS108	AP12
AD37	VSS30	VSS109	AP19
AD38	VSS31	VSS110	AP28
AD39	VSS32	VSS111	AP30
AD4	VSS33	VSS112	AP32
AD40	VSS34	VSS113	AP38
AD42	VSS35	VSS114	AP4
AD43	VSS36	VSS115	AP42
AD45	VSS37	VSS116	AP46
AD46	VSS38	VSS117	AP8
AD8	VSS39	VSS118	AR2
AE2	VSS40	VSS119	AR48
AE3	VSS41	VSS120	AT11
AE10	VSS42	VSS121	AT13
AE12	VSS43	VSS122	AT18
AD14	VSS44	VSS123	AT22
AD16	VSS45	VSS124	AT26
AF16	VSS46	VSS125	AT28
AF19	VSS47	VSS126	AT30
AF24	VSS48	VSS127	AT32
AF26	VSS49	VSS128	AT34
AF27	VSS50	VSS129	AT38
AF29	VSS51	VSS130	AT42
AF31	VSS52	VSS131	AT46
AF38	VSS53	VSS132	AT7
AF4	VSS54	VSS133	AU24
AF42	VSS55	VSS134	AU30
AF46	VSS56	VSS135	AV16
AF5	VSS57	VSS136	AV20
AF7	VSS58	VSS137	AV24
AF8	VSS59	VSS138	AV30
AG19	VSS60	VSS139	AV38
AG2	VSS61	VSS140	AV4
AG31	VSS62	VSS141	AV43
AG48	VSS63	VSS142	AV8
AH11	VSS64	VSS143	AW14
AH3	VSS65	VSS144	AW18
AH36	VSS66	VSS145	AW2
AH39	VSS67	VSS146	AW22
AH40	VSS68	VSS147	AW26
AH42	VSS69	VSS148	AW28
AH46	VSS70	VSS149	AW34
AH7	VSS71	VSS150	AW38
AJ19	VSS72	VSS151	AW40
AJ21	VSS73	VSS152	AW48
AJ24	VSS74	VSS153	AV11
AJ33	VSS75	VSS154	AY22
AJ34	VSS76	VSS155	AY28
AK12	VSS77	VSS156	
VSS78	VSS78	VSS157	
VSS79	VSS79	VSS158	

PANTHER-GP-NF



PCH1 9 OF 10

AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY8	VSS162	VSS262	K38
B11	VSS163	VSS263	K46
B15	VSS164	VSS264	K7
B19	VSS165	VSS265	L18
B23	VSS166	VSS266	L2
B27	VSS167	VSS267	L20
B31	VSS168	VSS268	L28
B35	VSS169	VSS269	L36
B39	VSS170	VSS270	L48
B7	VSS171	VSS271	M12
F45	VSS172	VSS272	M16
BB12	VSS173	VSS273	M18
BB16	VSS174	VSS274	M22
BB20	VSS175	VSS275	M24
BB24	VSS176	VSS276	M30
BB28	VSS177	VSS277	M32
BB30	VSS178	VSS278	M34
BB38	VSS179	VSS279	M38
BB4	VSS180	VSS280	M4
BB44	VSS181	VSS281	M42
BC14	VSS182	VSS282	M46
BC18	VSS183	VSS283	M8
BC2	VSS184	VSS284	N18
BC22	VSS185	VSS285	P30
BC26	VSS186	VSS286	N47
BC32	VSS187	VSS287	P11
BC34	VSS188	VSS288	P18
BC36	VSS189	VSS289	T33
BC40	VSS190	VSS290	P40
BC42	VSS191	VSS291	P43
BC48	VSS192	VSS292	P47
BD46	VSS193	VSS293	P7
BD5	VSS194	VSS294	R2
BE22	VSS195	VSS295	R48
BE26	VSS196	VSS296	T12
BE40	VSS197	VSS297	T31
BF10	VSS198	VSS298	T37
BF12	VSS199	VSS299	T4
BF16	VSS200	VSS300	W34
BF20	VSS201	VSS301	T46
BF22	VSS202	VSS302	T47
BF24	VSS203	VSS303	T8
BF26	VSS204	VSS304	V11
BF28	VSS205	VSS305	V17
BF3	VSS206	VSS306	V26
BF30	VSS207	VSS307	V27
BF38	VSS208	VSS308	V29
BF40	VSS209	VSS309	V31
BF8	VSS210	VSS310	V36
BG17	VSS211	VSS311	V39
BG21	VSS212	VSS312	V43
BG33	VSS213	VSS313	V7
BG44	VSS214	VSS314	W17
BG8	VSS215	VSS315	W19
BH11	VSS216	VSS316	W2
BH15	VSS217	VSS317	W27
BH17	VSS218	VSS318	W48
BH19	VSS219	VSS319	Y12
H10	VSS220	VSS320	Y38
BH27	VSS221	VSS321	Y4
BH31	VSS222	VSS322	Y42
BH33	VSS223	VSS323	Y46
BH35	VSS224	VSS324	Y8
BH39	VSS225	VSS325	BG29
BH43	VSS226	VSS326	N24
BH7	VSS227	VSS327	AJ3
D3	VSS228	VSS328	AD47
D12	VSS229	VSS329	B43
D16	VSS230	VSS330	BE10
D18	VSS231	VSS331	BG41
D22	VSS232	VSS332	G14
D24	VSS233	VSS333	H16
D26	VSS234	VSS334	T36
D30	VSS235	VSS335	BG22
D32	VSS236	VSS336	BG24
D34	VSS237	VSS337	C22
D38	VSS238	VSS338	AP13
D42	VSS239	VSS339	M14
D48	VSS240	VSS340	AP3
E18	VSS241	VSS341	AP1
E26	VSS242	VSS342	BE16
G18	VSS243	VSS343	BC16
G20	VSS244	VSS344	BG28
G26	VSS245	VSS345	BJ28
G28	VSS246	VSS346	
G36	VSS247	VSS347	
G48	VSS248	VSS348	
H12	VSS249	VSS349	
H18	VSS250	VSS350	
H22	VSS251	VSS351	
H24	VSS252	VSS352	
H26	VSS253		
H30	VSS254		
H32	VSS255		
H34	VSS256		
F3	VSS257		
	VSS258		

PANTHER-GP-NF



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緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title PCH (VSS)			
Size	Document Number	G48/G58	Rev
			SC
Date:	Friday, February 17, 2012	Sheet	25 of 103

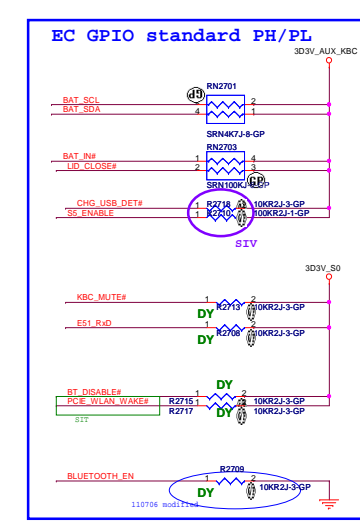
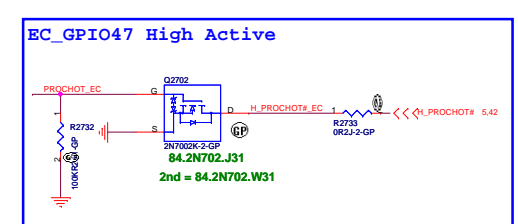
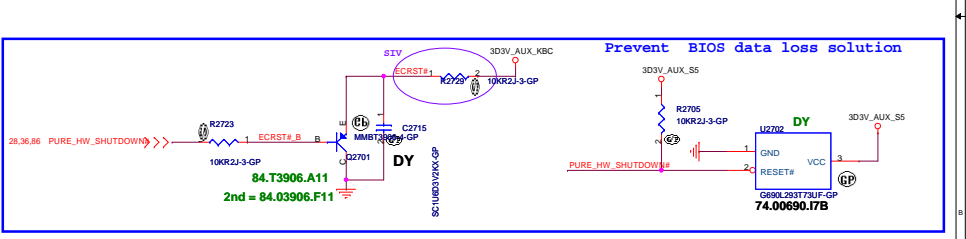
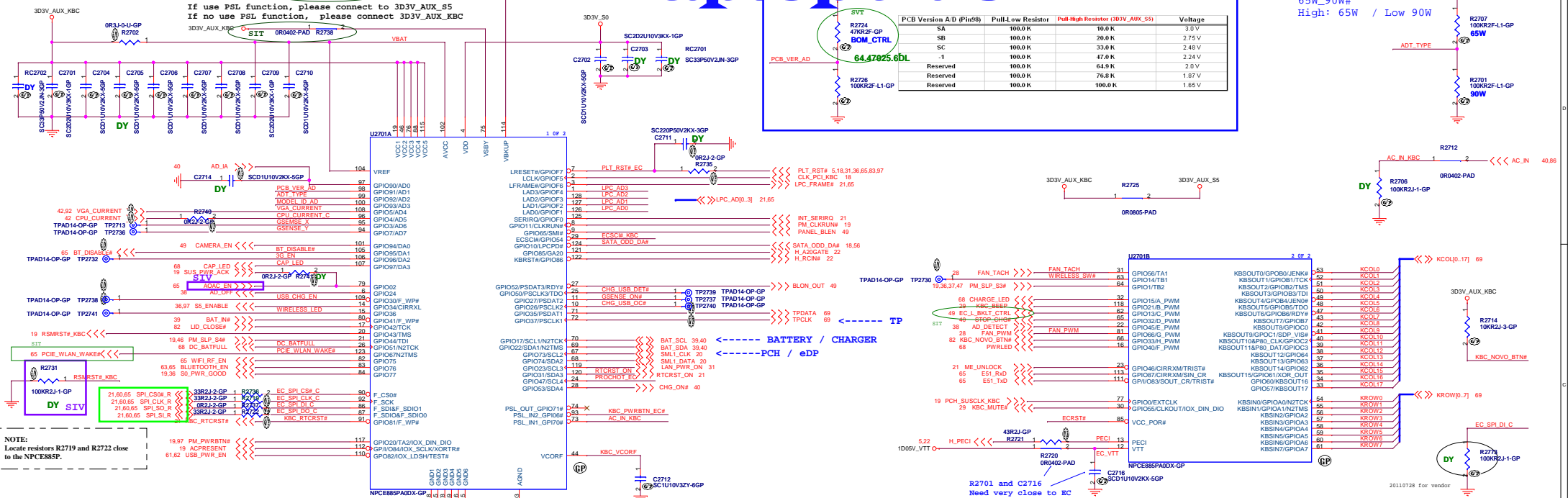
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JV10-CS

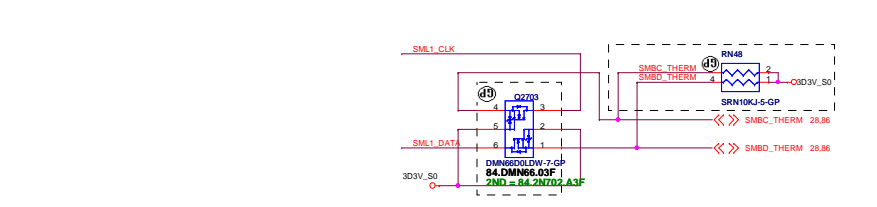
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
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SSID = KBC

65W_90W#
High: 65W / Low 90W



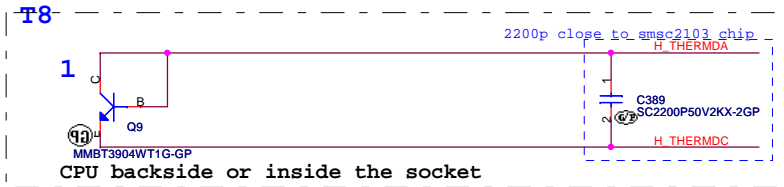
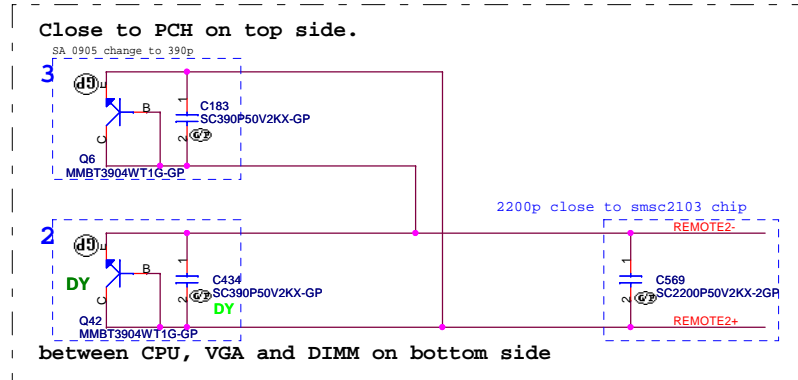
LILI Multi GPIO setting



MODEL_ID AD (Pin#)	Pull-Low Register	Pull-High Register	Voltage
LG48 UMA	100.0 K	10.0 K	3.000 V
LG48 OPTIMUS	100.0 K	20.0 K	2.750 V
LG58 UMA	100.0 K	33.0 K	2.481 V
LG58 OPTIMUS	100.0 K	47.0 K	2.245 V

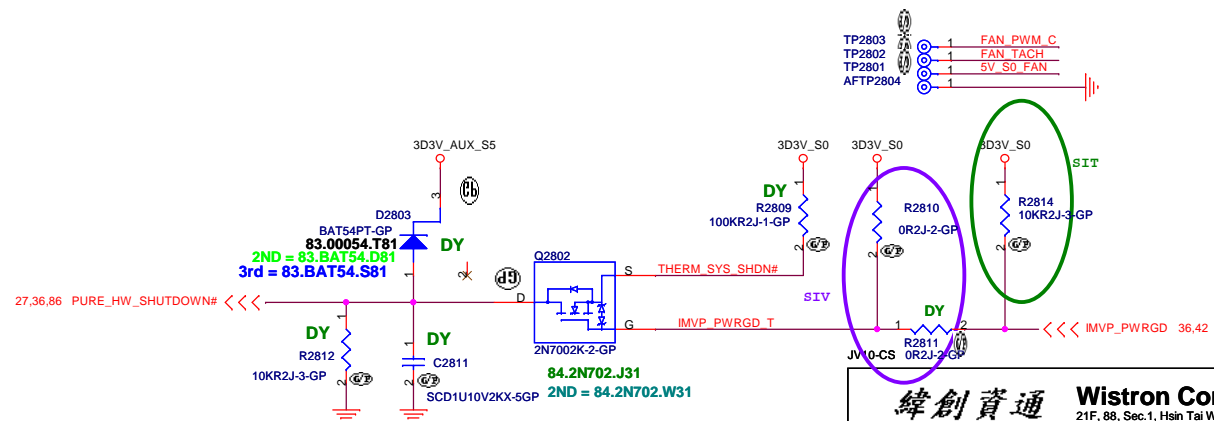
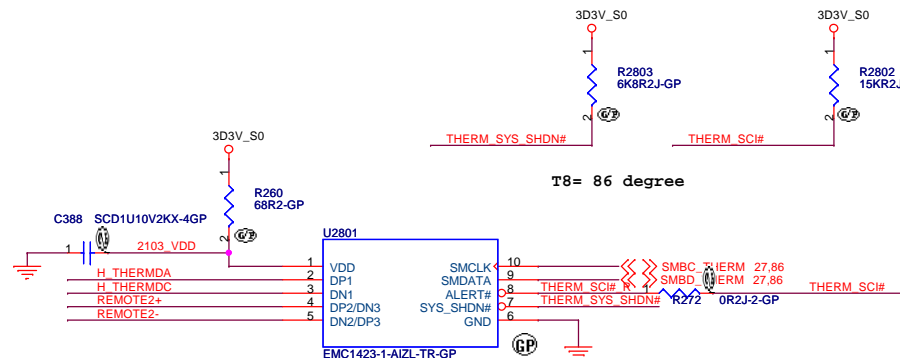
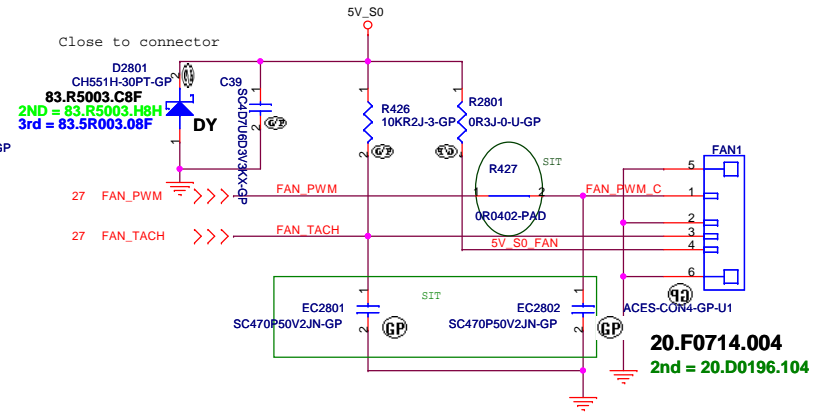
SSID = Thermal

Thermal sensor



CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

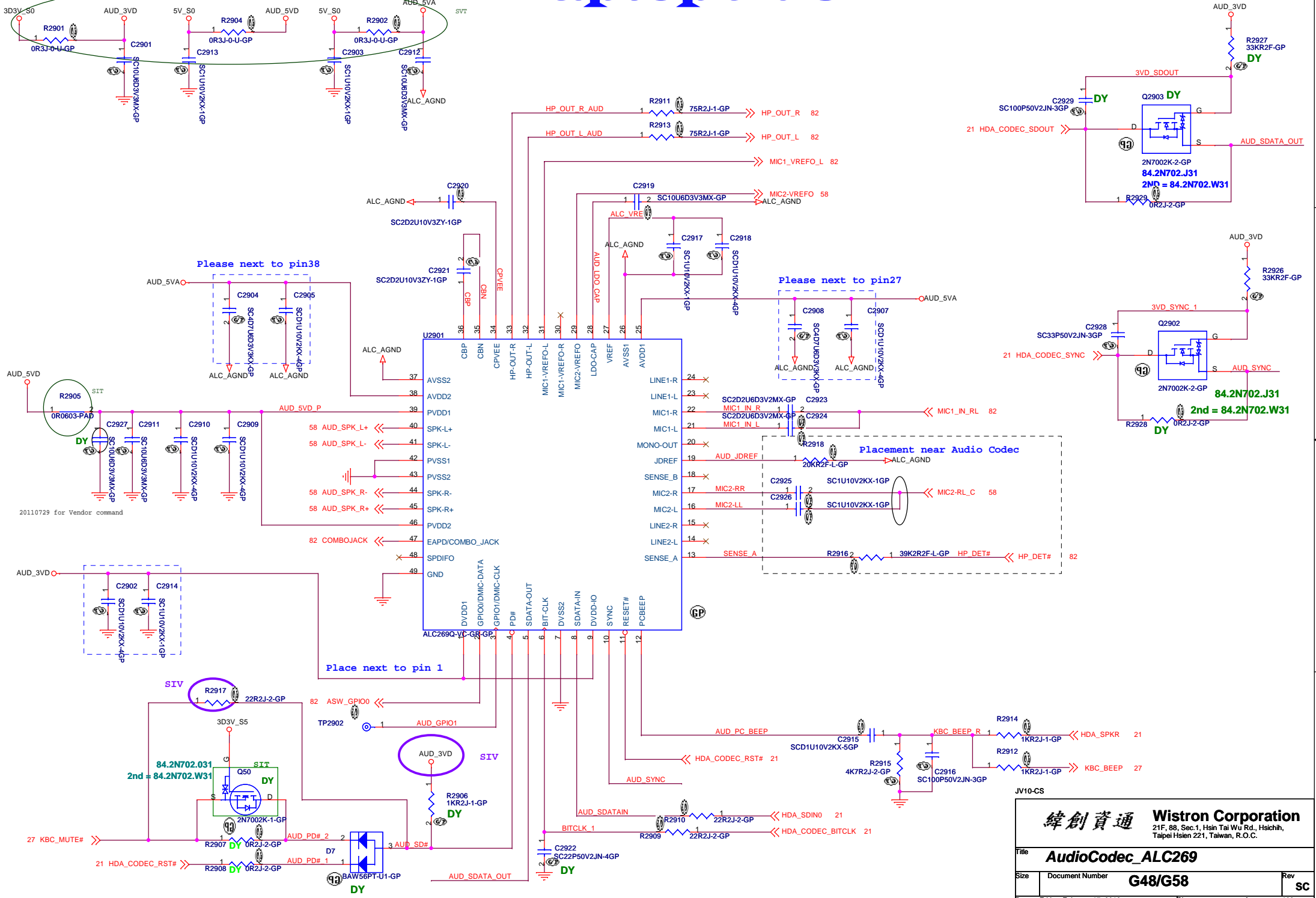
4 WIRE PWM Fan Control circuit



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Title **THERMAL EMC1423**

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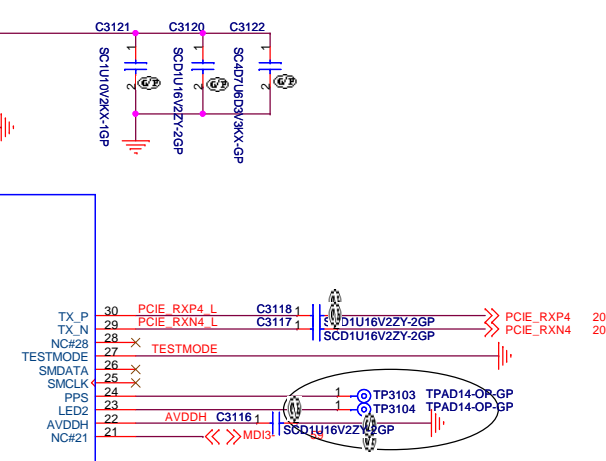
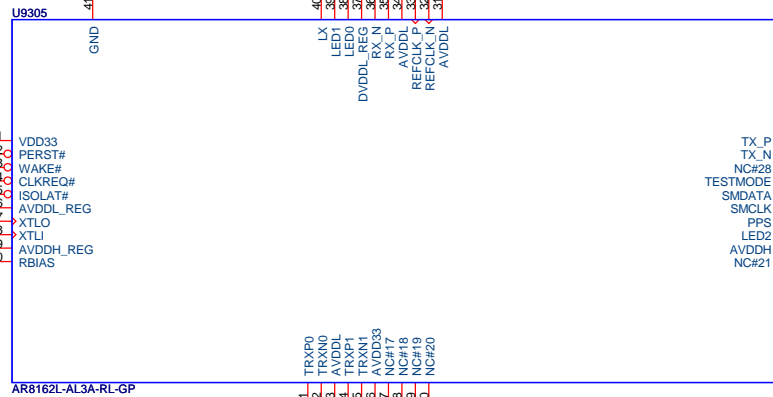
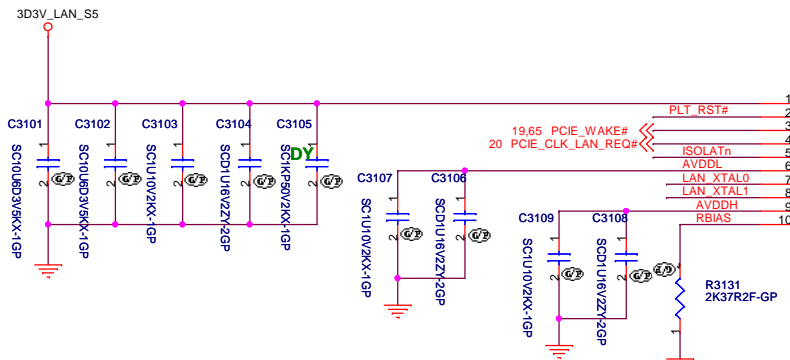
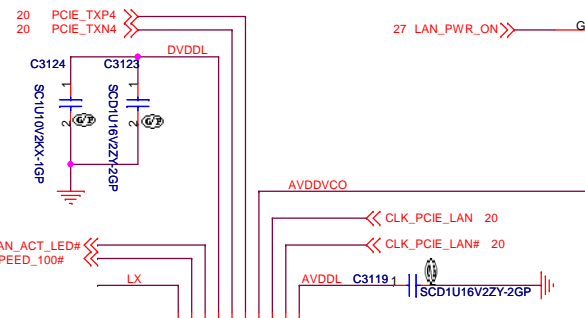
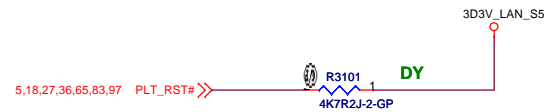
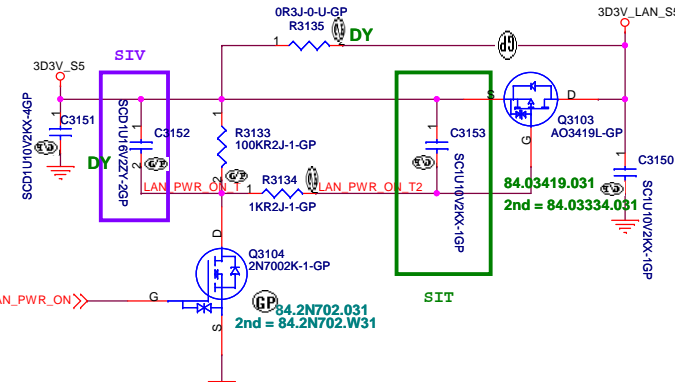
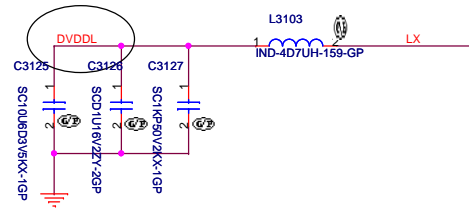
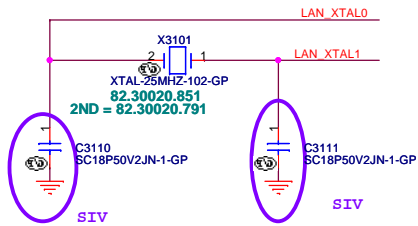
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AudioCodec_ALC269	
Title	Document Number
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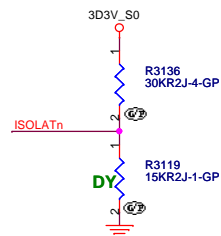
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio_AMP			
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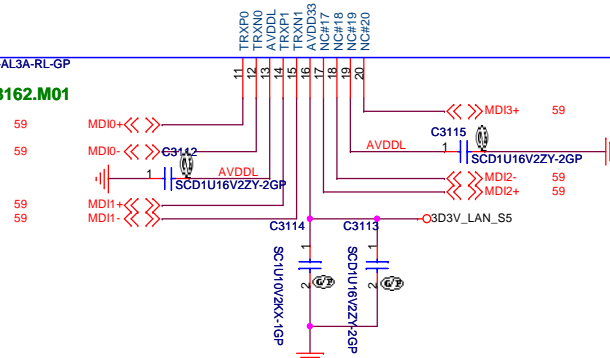
25MHz XTAL



ISOLATn is active low to isolate the whole chip to place in lowest power consumption mode.



71.08162.M01
BOM_CTRL



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Title		LOM	
Size	Document Number	G48/G58	Rev
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Card reader			
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 1394			
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Smart card			
Size	Document Number	G48/G58	Rev SC
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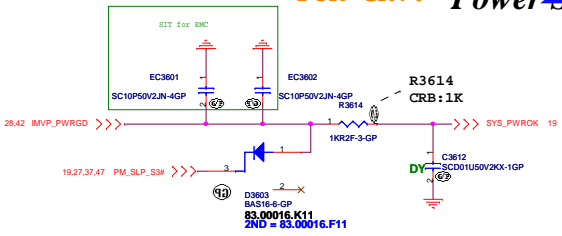
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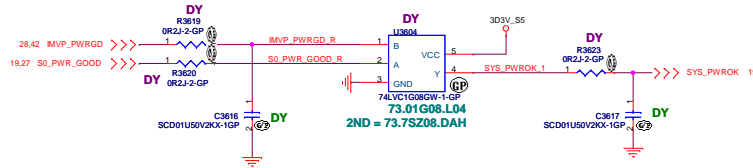
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **USB 3.0 CONTROLLER**

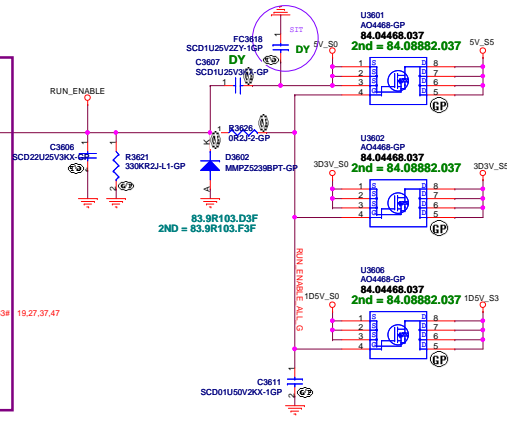
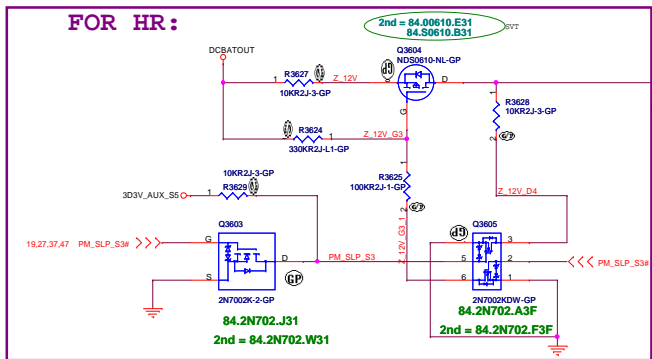
Size	Document Number	Rev
	G48/G58	SC



FOR HR:

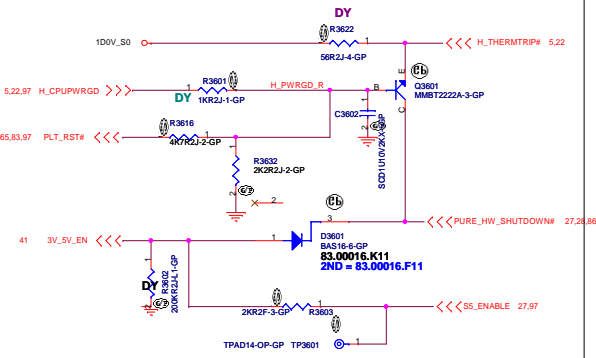
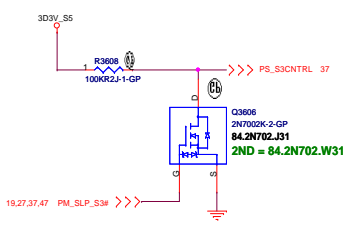
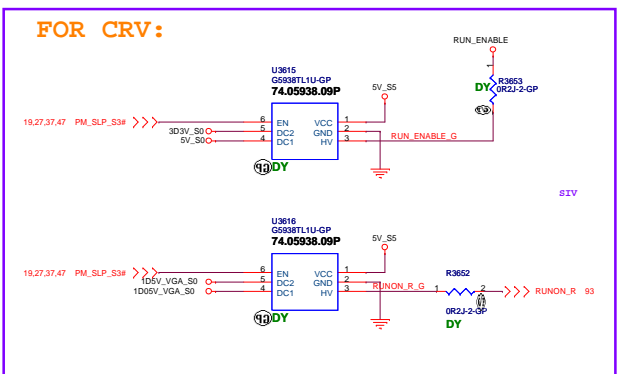


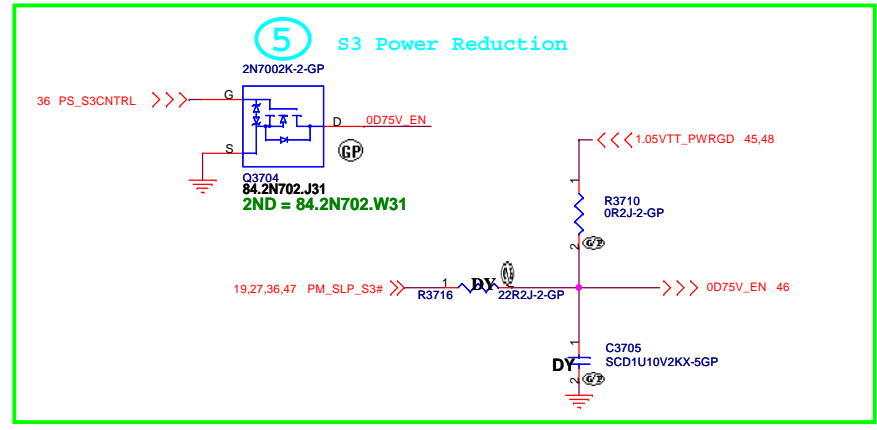
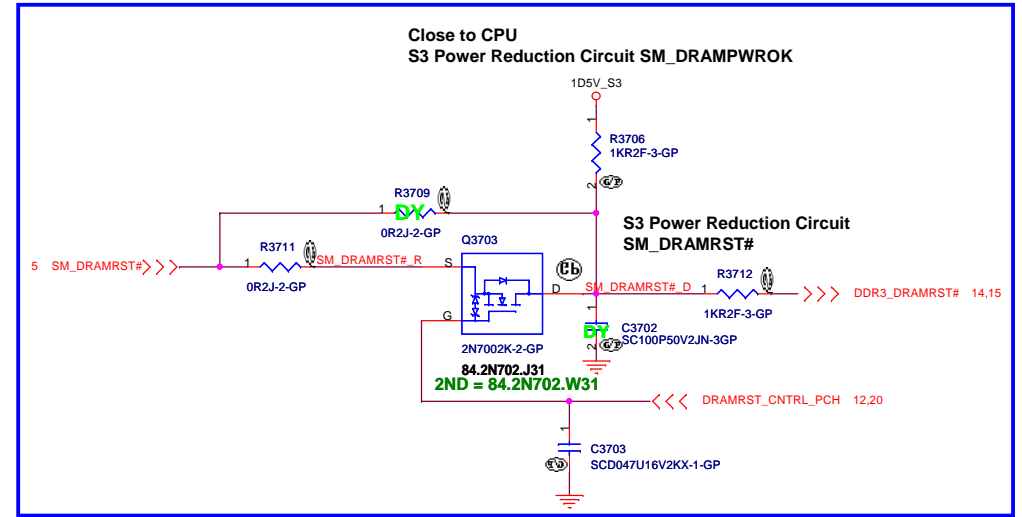
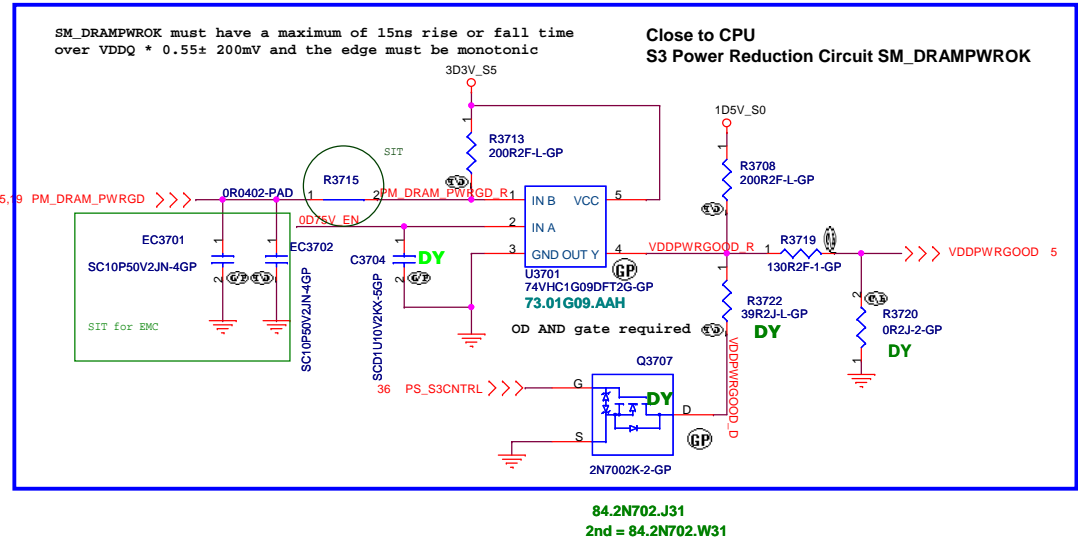
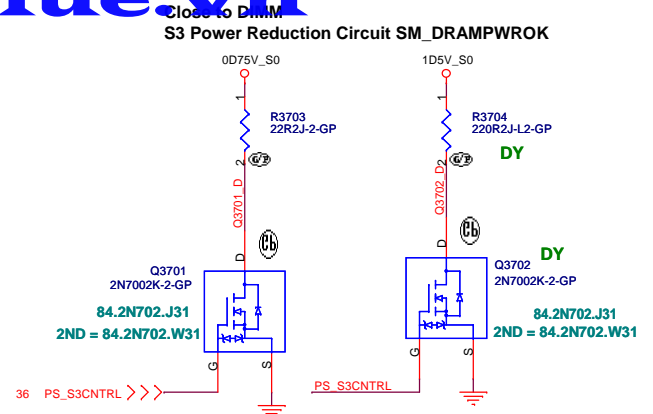
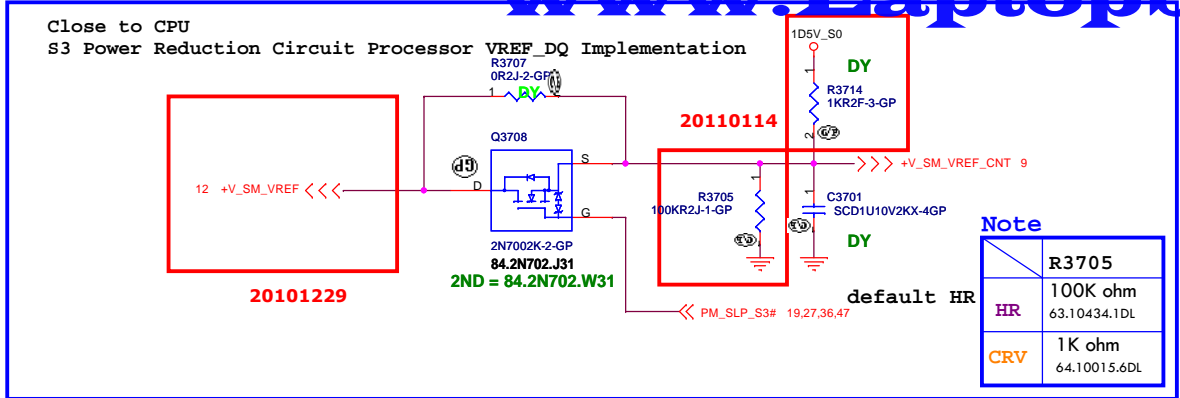
FOR HR:



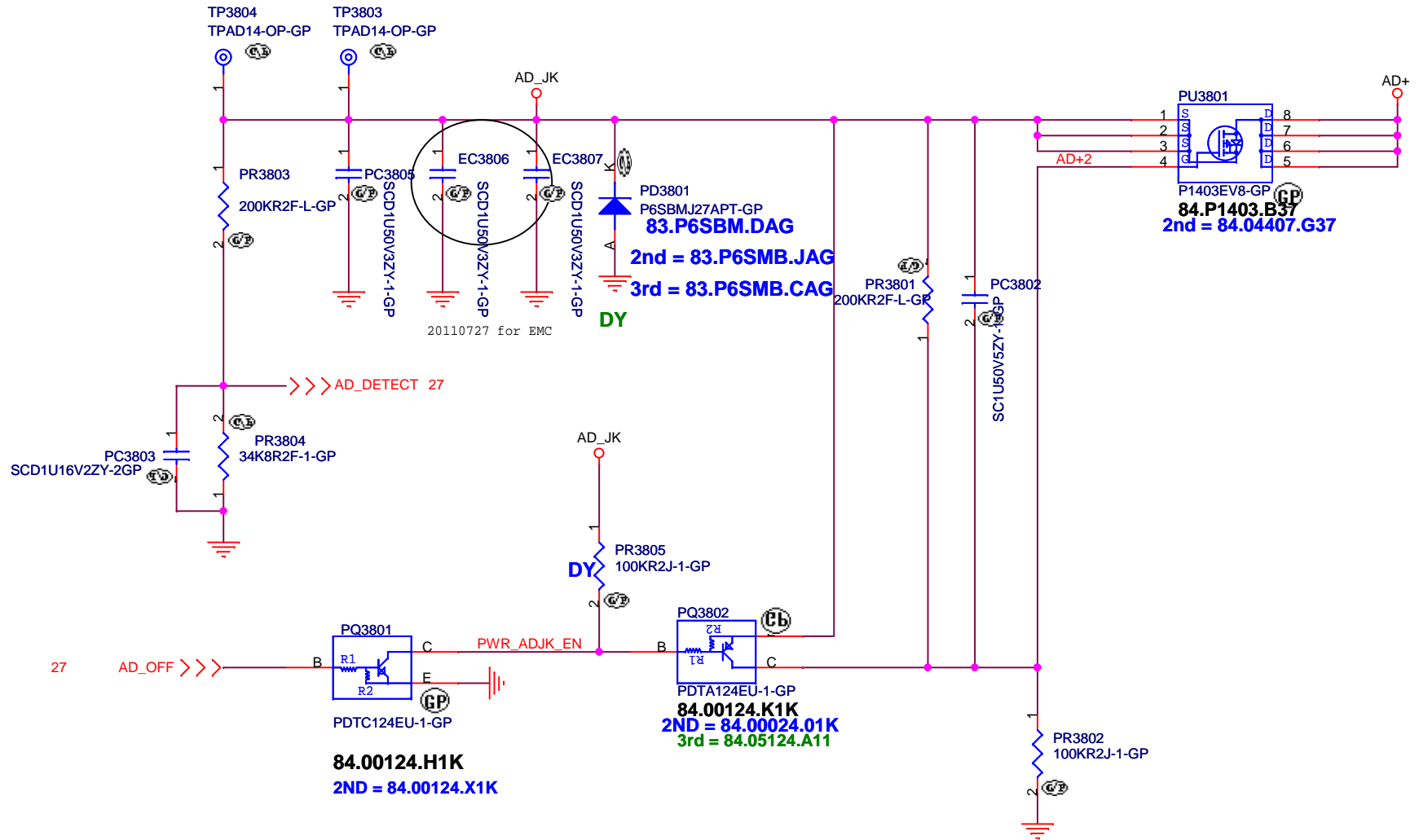
1D5V_S0
MAX Current 3000 mA
Design Current 2100 mA
Total = 11.39A

FOR CRV:





Adaptor in to generate DCBATOUT



JV10-CS

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **DCIN JACK**

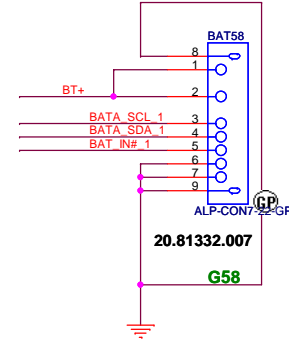
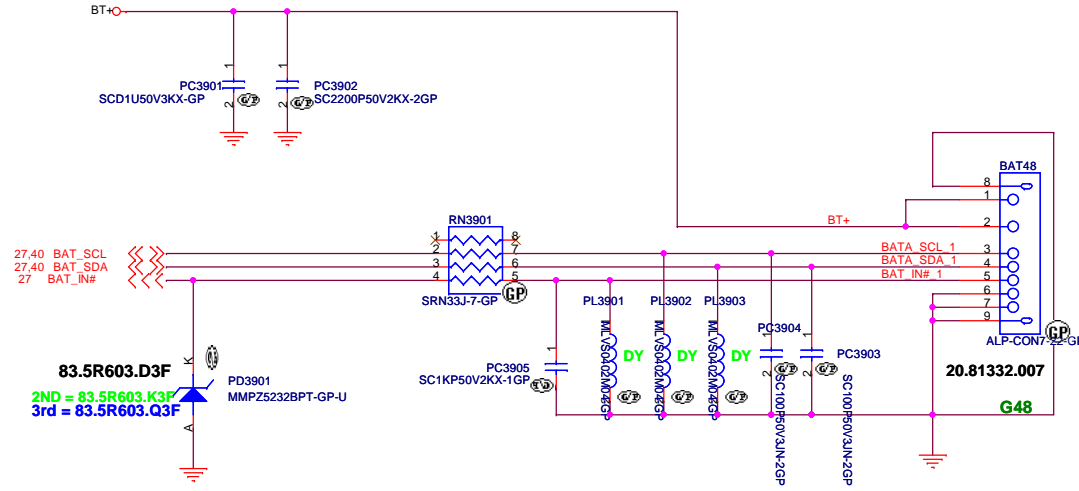
Size Document Number **G48/G58**

Rev **SC**

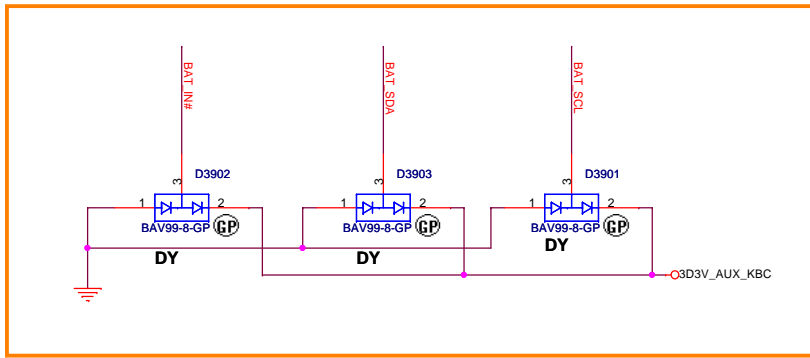
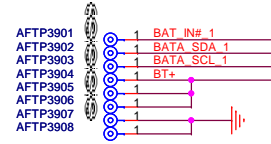
Date: Friday, February 17, 2012

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BATTERY CONNECTOR

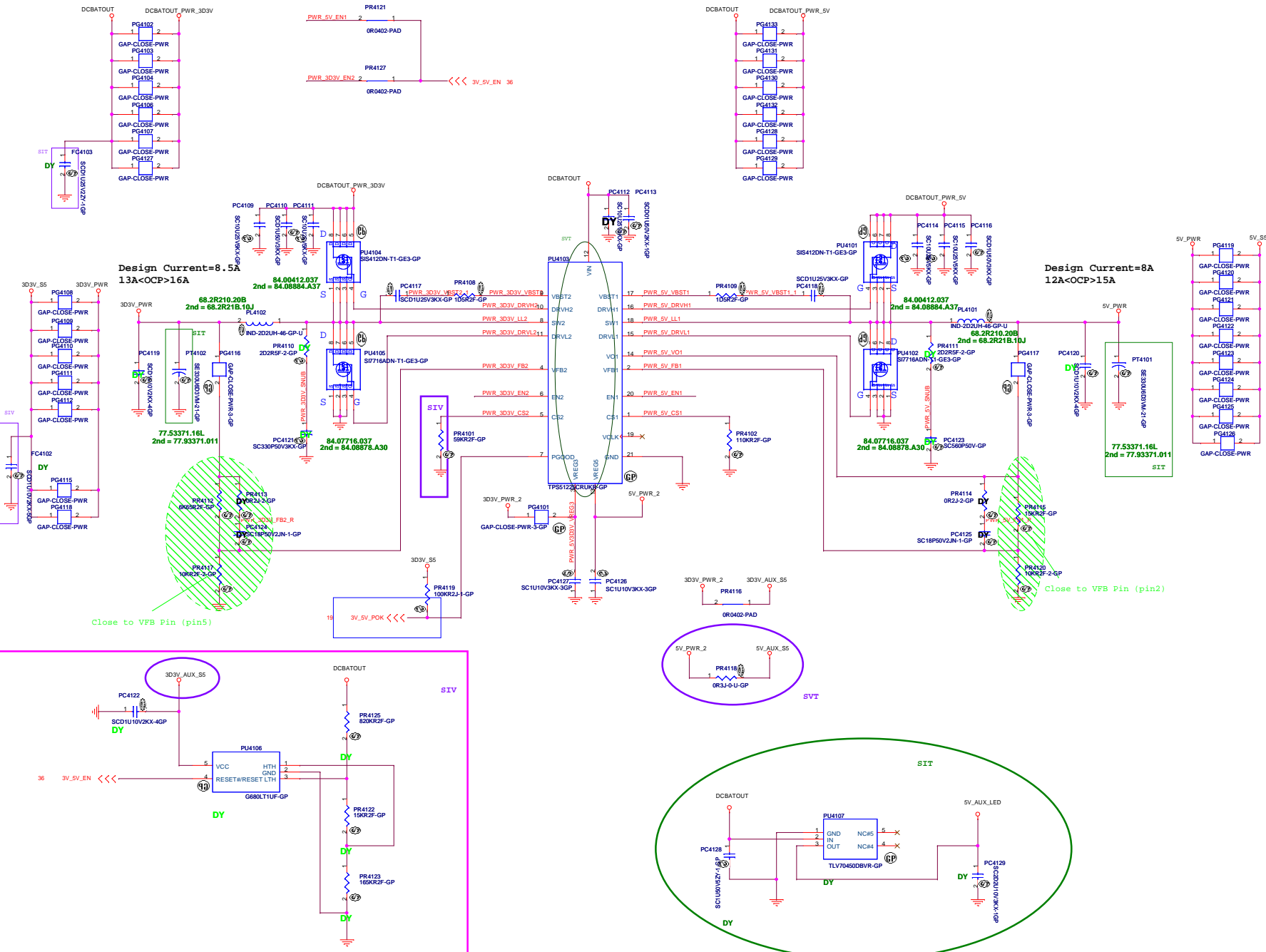


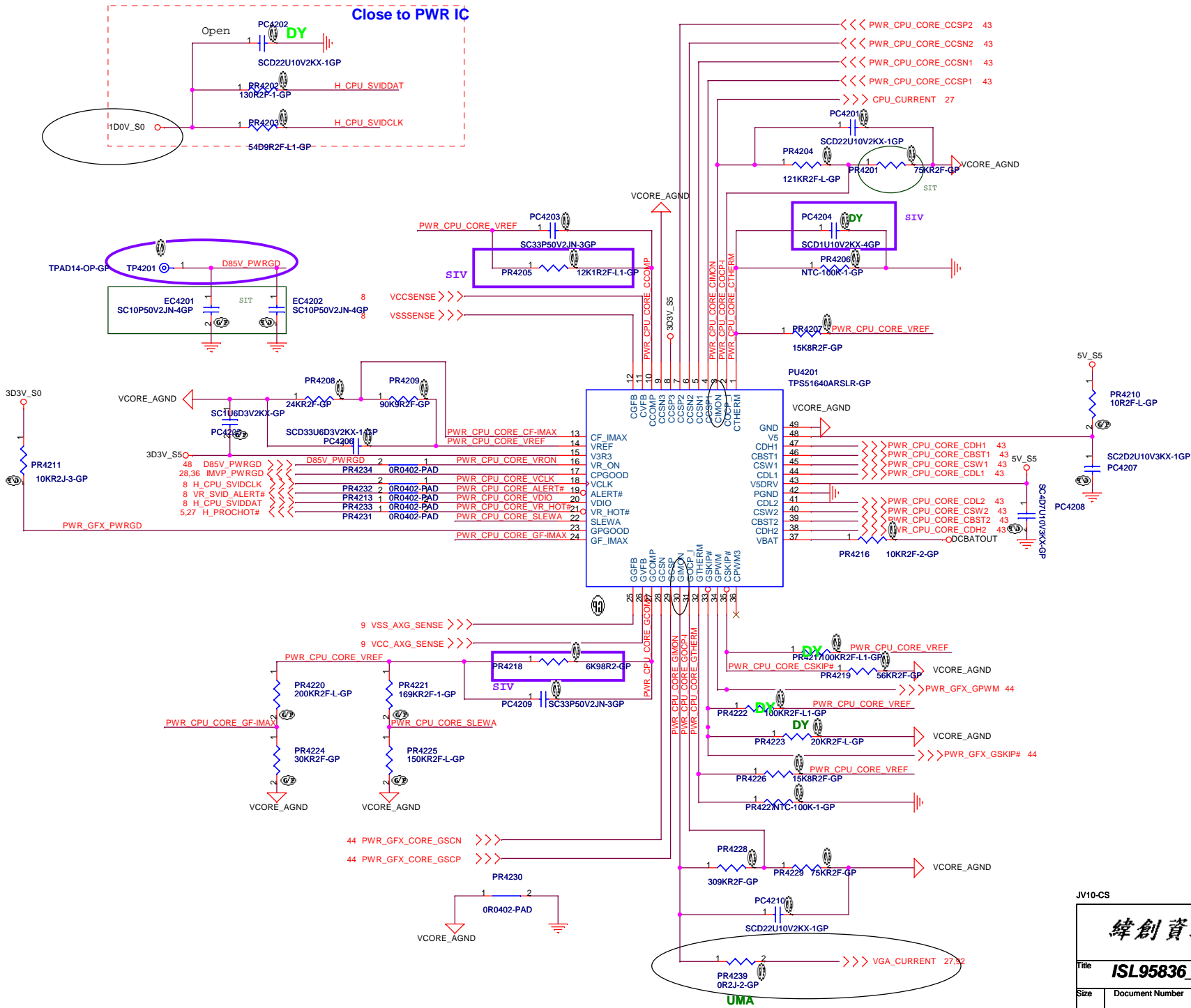
83.5R603.D3F
 2ND = 83.5R603.K3F
 3rd = 83.5R603.Q3F



JV10-CS

<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
Title	BATT CONN
Size	Document Number G48/G58
Date	Friday, February 17, 2012
Rev	SC
Sheet	39 of 103





JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

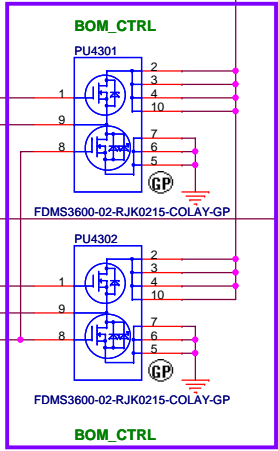
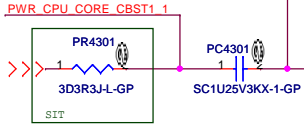
Title ISL95836_CPU_CORE(1/3)

Size Document Number G48/G58 Rev SC

Date: Friday, February 17, 2012 Sheet 42 of 103

1st = 84.03660.037
2nd = 84.00038.A37

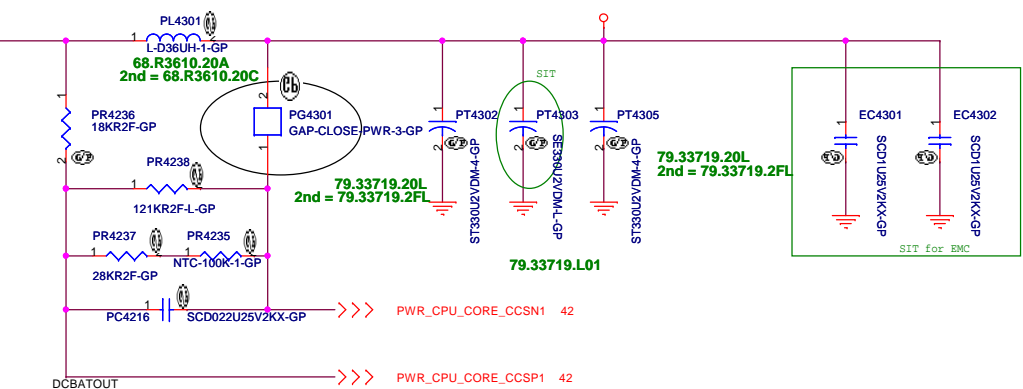
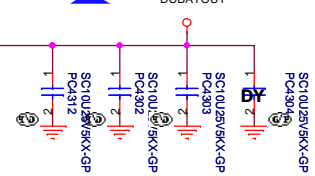
42 PWR_CPU_CORE_CDH1 >>>
42 PWR_CPU_CORE_CSW1 >>>
42 PWR_CPU_CORE_CBST1 >>>
42 PWR_CPU_CORE_CDL1 >>>



SIV
1st = 84.03660.037
2nd = 84.00038.A37

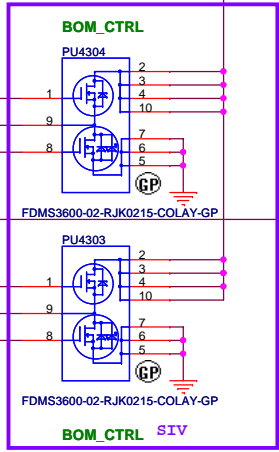
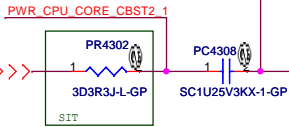
PU4301, PU4302, PU4303, PU4304 change to 84.07608.037 for BOM

Countinue current: 53A

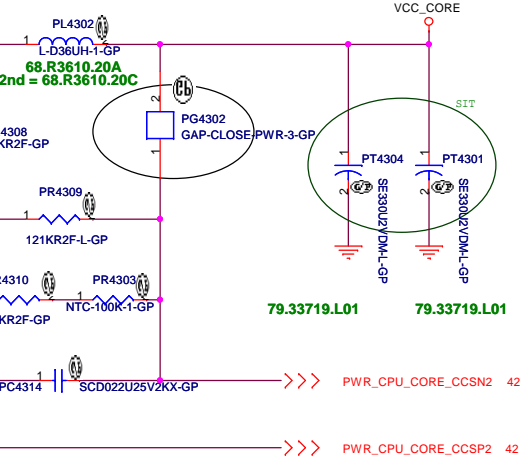
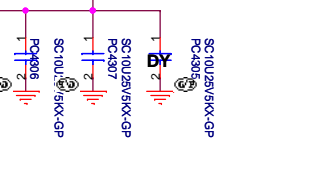


1st = 84.03660.037
2nd = 84.00038.A37

42 PWR_CPU_CORE_CDH2 >>>
42 PWR_CPU_CORE_CSW2 >>>
42 PWR_CPU_CORE_CBST2 >>>
42 PWR_CPU_CORE_CDL2 >>>

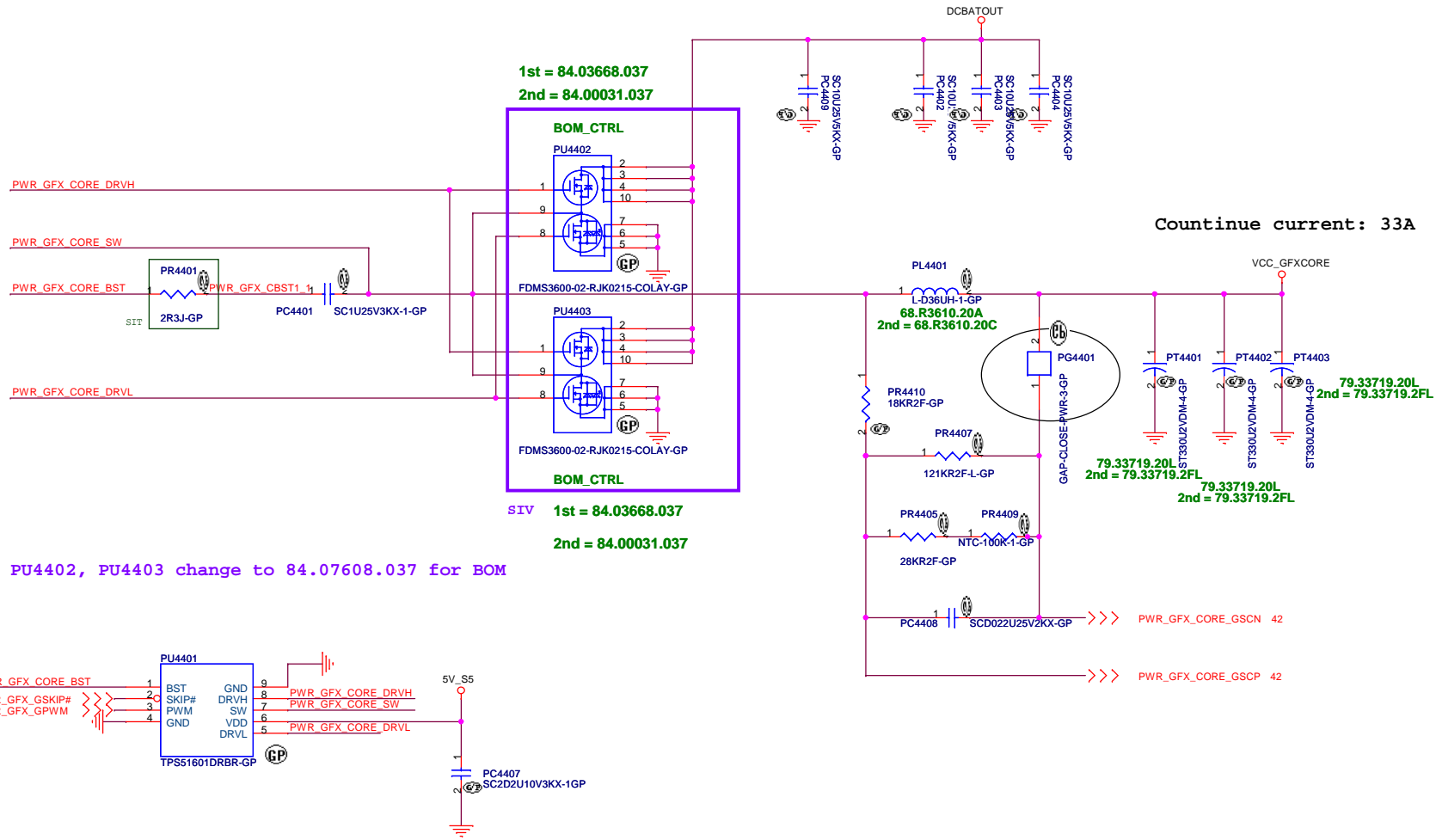


SIV
1st = 84.03660.037
2nd = 84.00038.A37

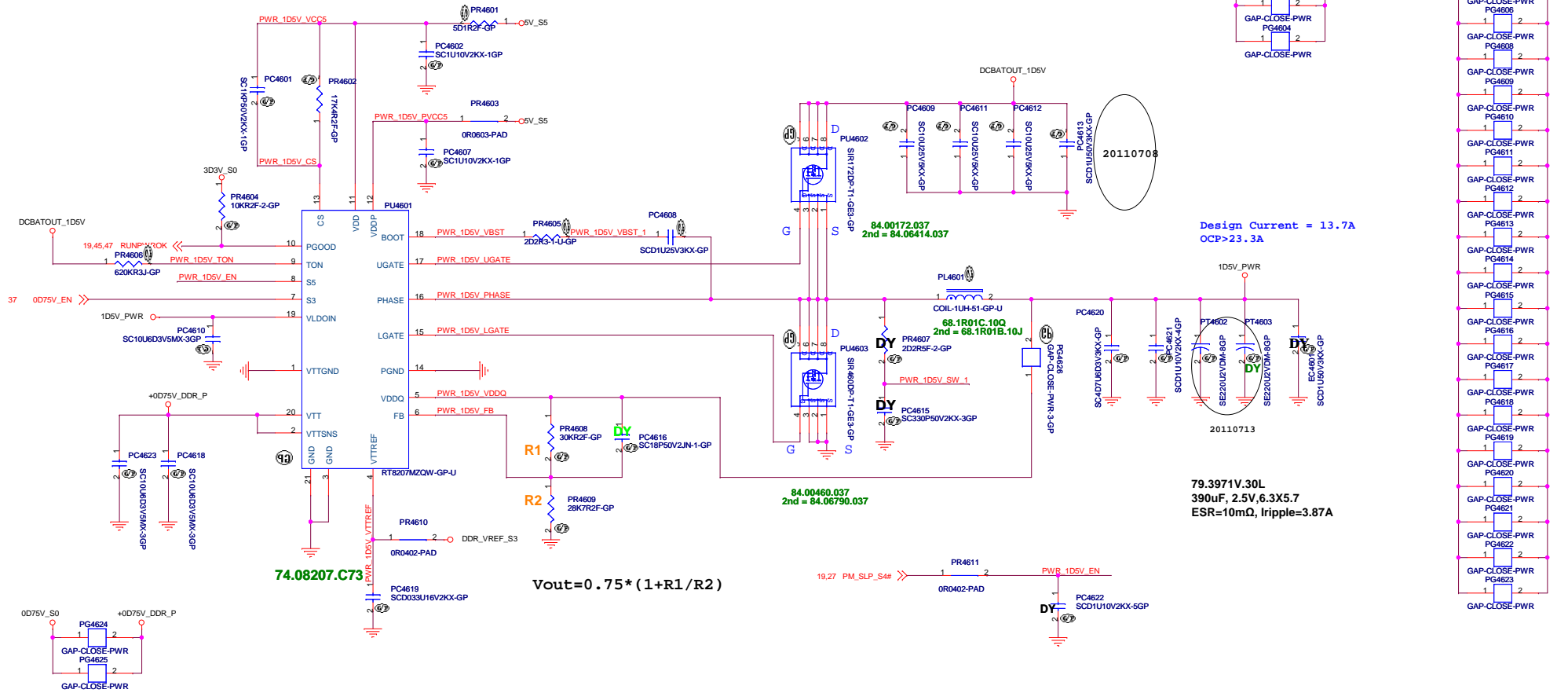


JV10-CS

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ISL95836_CPU_CORE(2/3)	
Size Document Number	G48/G58
Date Monday, February 20, 2012	Sheet 43 of 103



JV10-CS

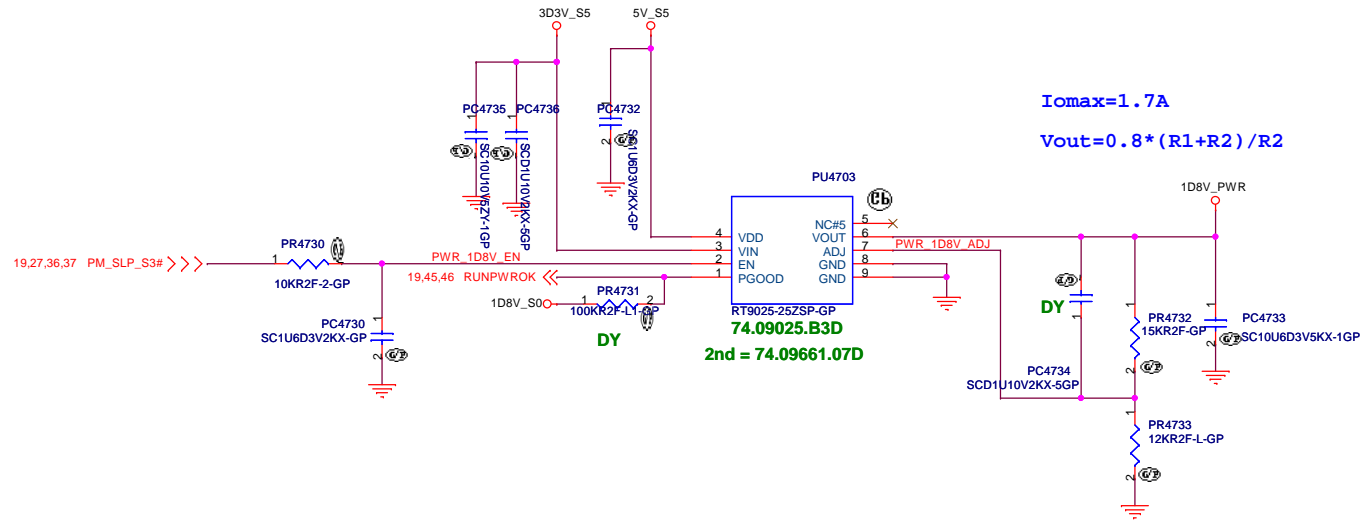
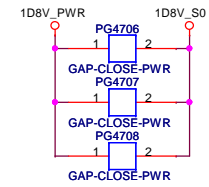


JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsien Tai Wu Rd., Hsichū,
Taipei Hsien 221, Taiwan, R.O.C.

Title			RT8207_1D5V_0D75V
Size	Document Number	G48/G58	
Date:	Friday, February 17, 2012	Sheet	46 of 103
Rev	SC		

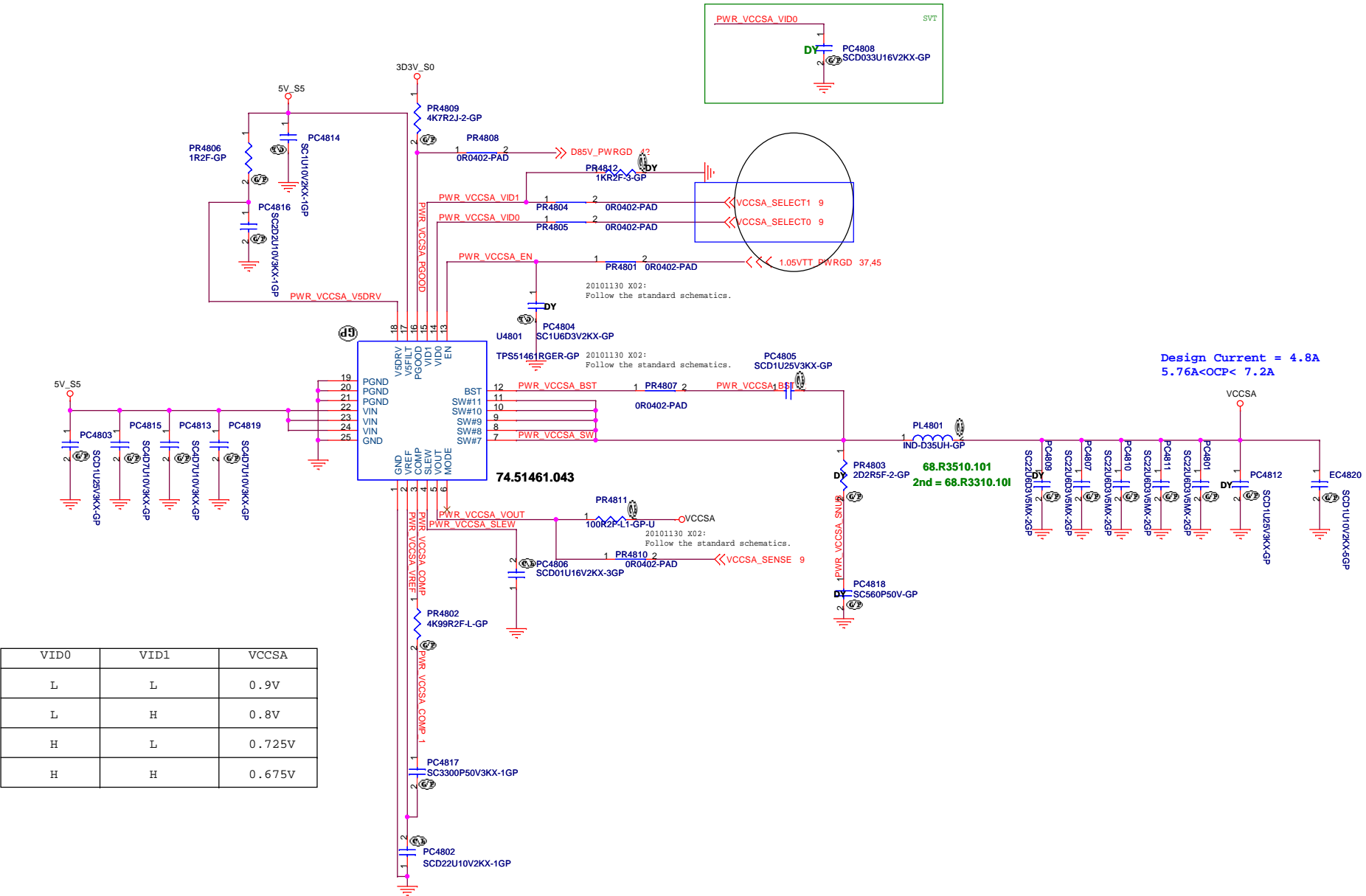
RT9025 for 1D8V_S0



JV10-CS

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RT9205_1D8V	
Size	Document Number G48/G58
Date: Friday, February 17, 2012	Sheet 47 of 103
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TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

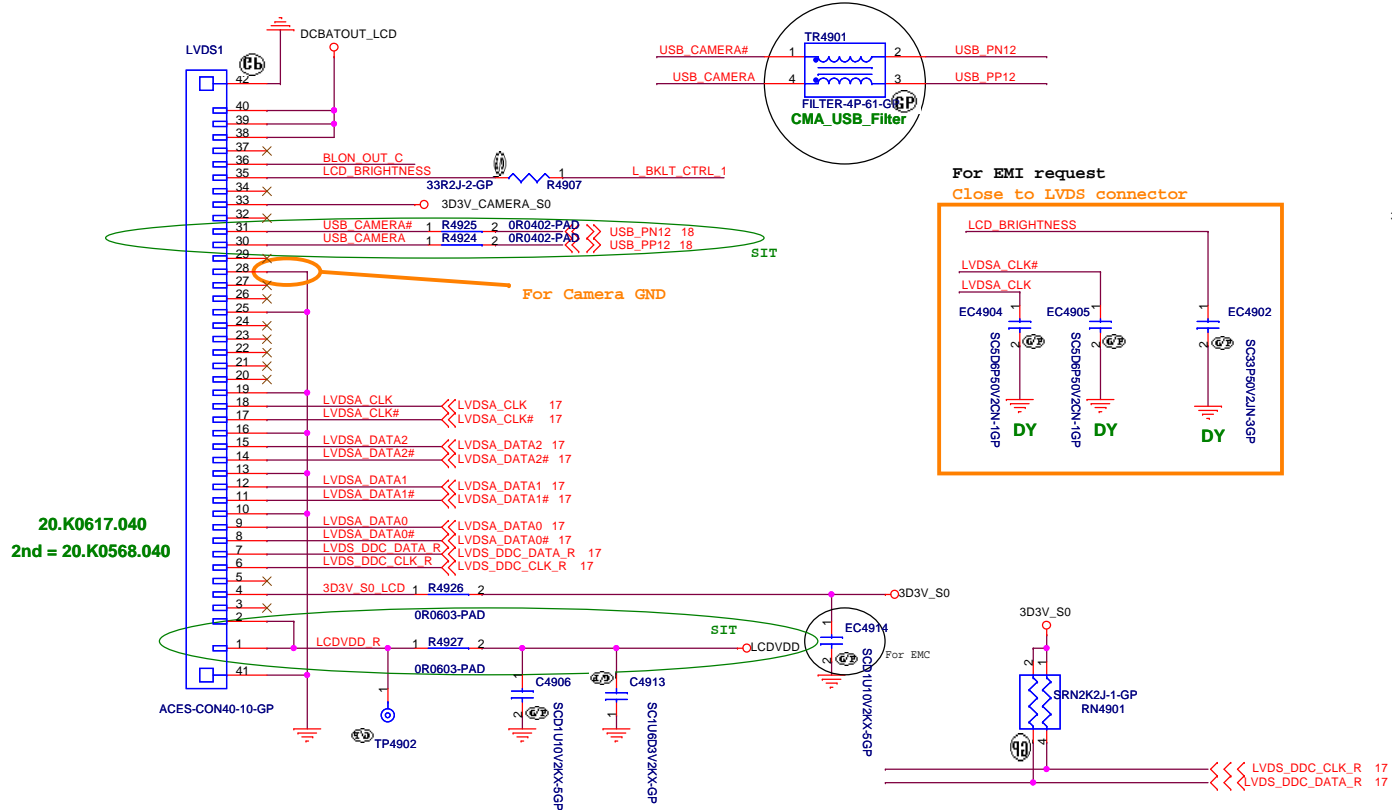
JV10-CS

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title VCCSA_TPS51461	
Size	Document Number G48/G58
Date: Friday, February 17, 2012	Sheet 48 of 103

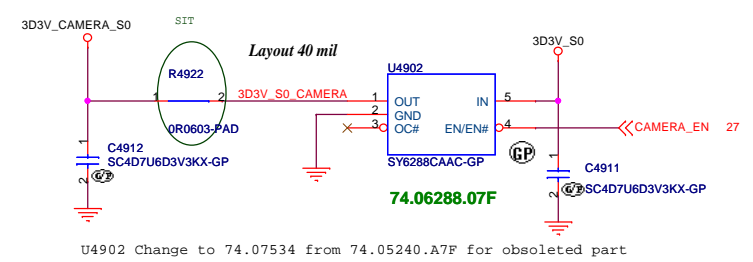
SSID = VIDEO

LVDS connector

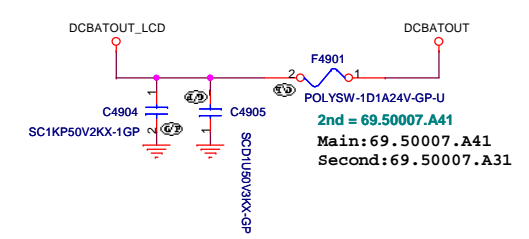
20110727 for EMC



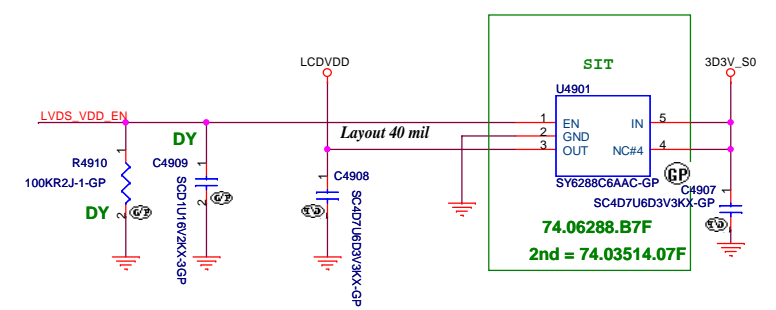
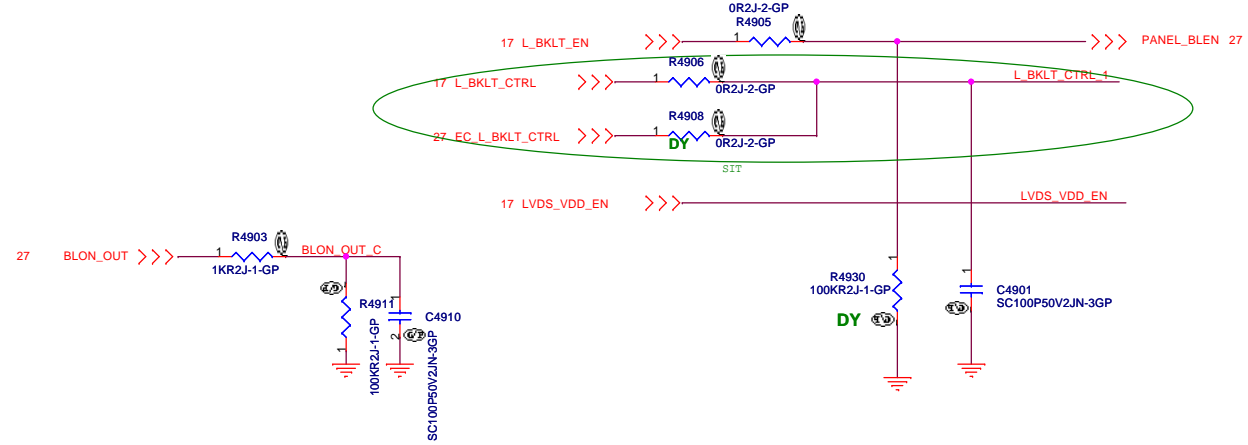
CAMERA POWER



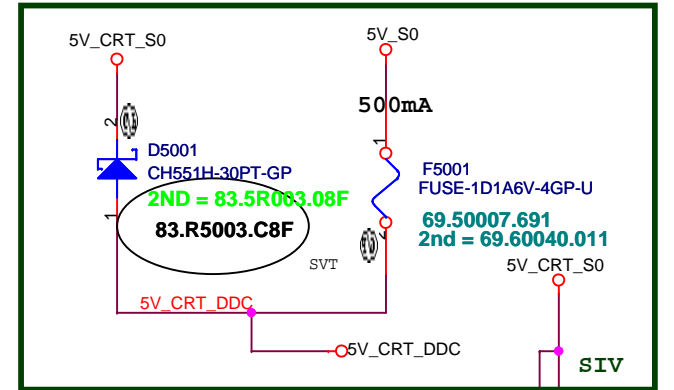
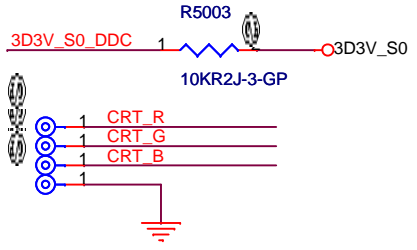
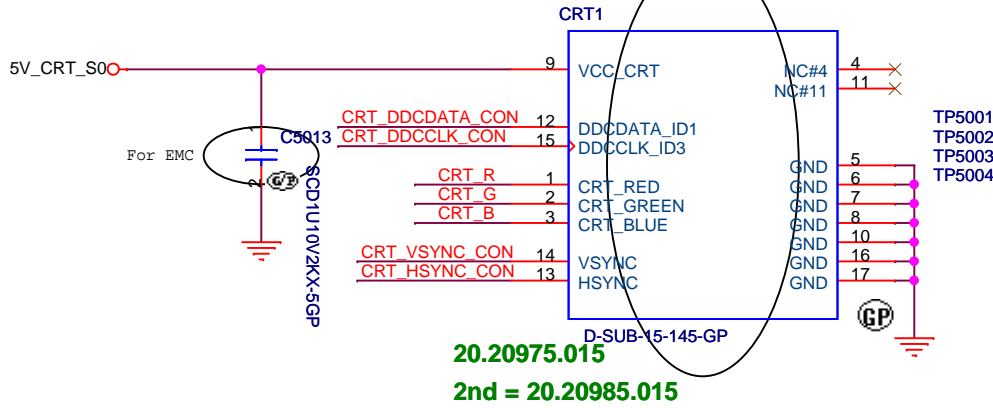
LCD POWER



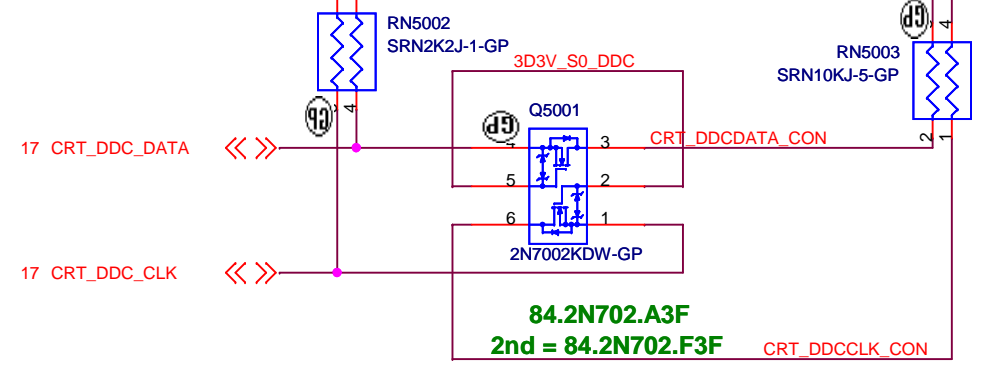
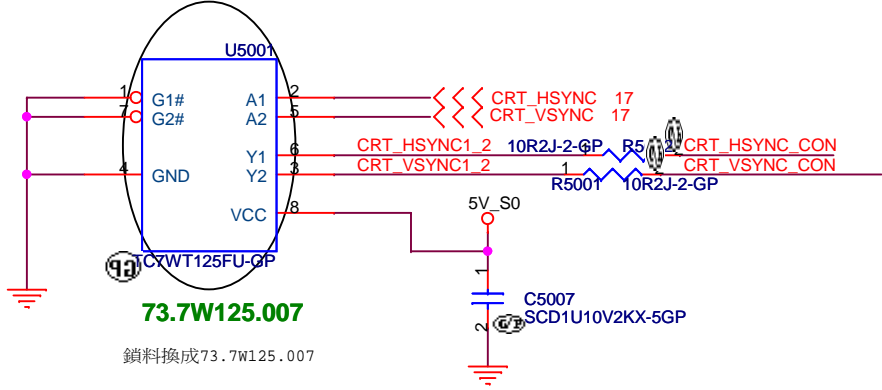
Panel BL brightness/Power En/BL En



JV10-CS

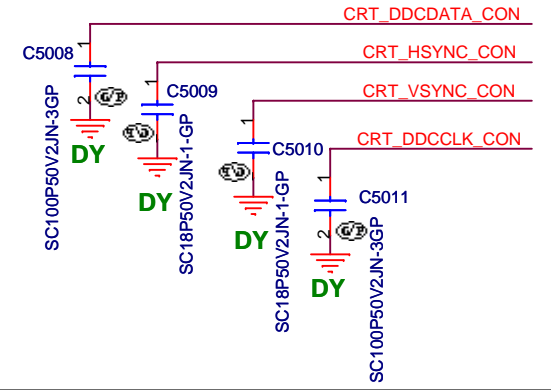
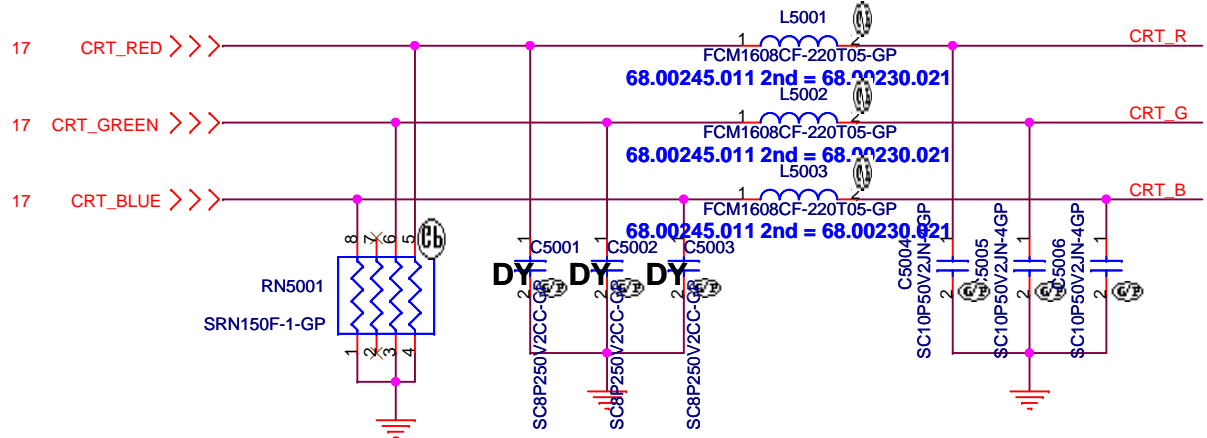


CRT Hsync & Vsync level shift



CRT RGB

R,G,B place 22pF and ESD diode for intel check list



JV10-CS

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **CRT Board Connector**

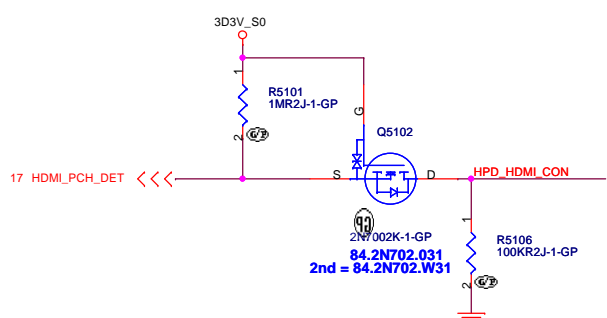
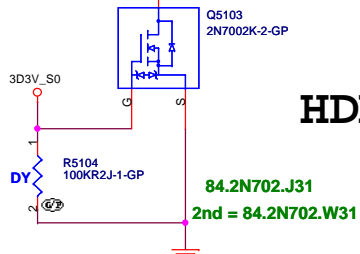
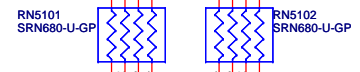
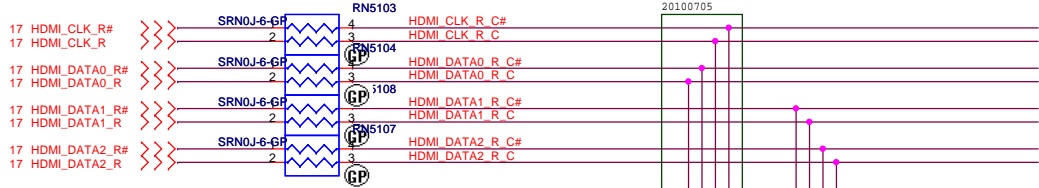
Size	Document Number	Rev
	G48/G58	SC

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SSID = VIDEO

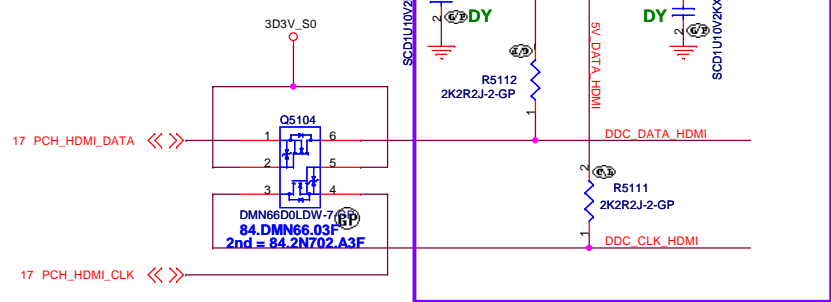
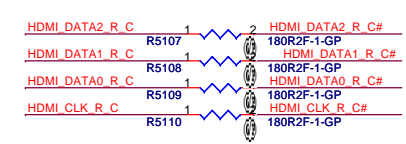
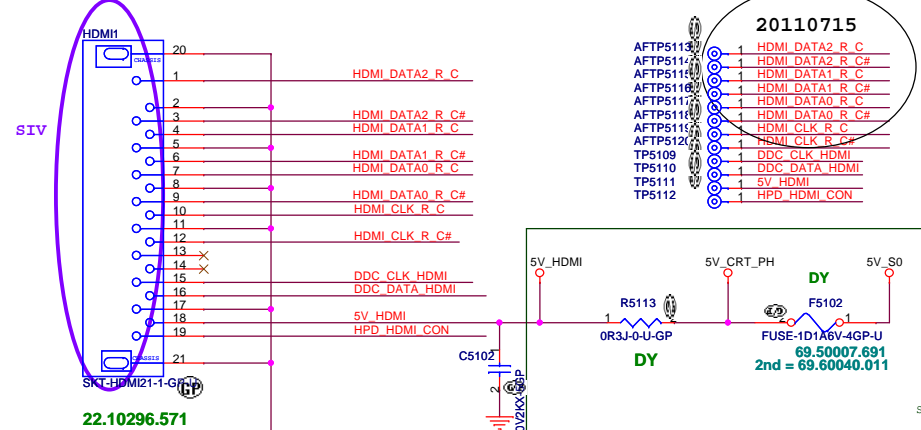
HDMI Passive Level Shifter

Close to HDMI Connector



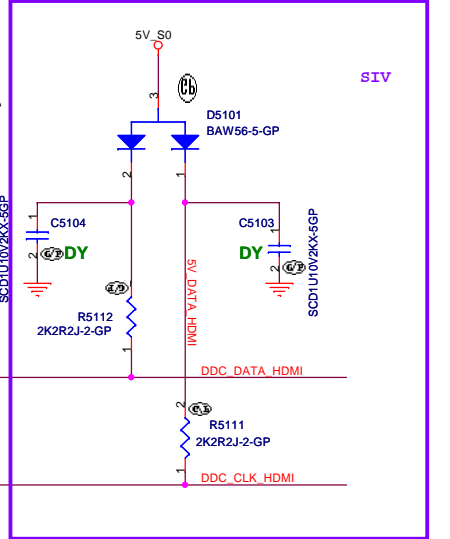
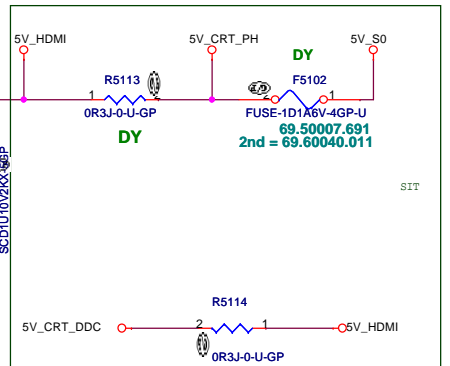
HDMI DDC Passive Level Shifter

R5112, R5111 2.2-kΩ ±5% pull-up to 5 V after the level shifter for intel check list



20110715

AFTP5113	1	HDMI_DATA2_R_C
AFTP5114	1	HDMI_DATA2_R_C#
AFTP5115	1	HDMI_DATA1_R_C
AFTP5116	1	HDMI_DATA1_R_C#
AFTP5117	1	HDMI_DATA0_R_C
AFTP5118	1	HDMI_DATA0_R_C#
AFTP5119	1	HDMI_CLK_R_C
AFTP5120	1	HDMI_CLK_R_C#
TP5109	1	DDC_CLK_HDMI
TP5110	1	DDC_DATA_HDMI
TP5111	1	5V_HDMI
TP5112	1	HPD_HDMI_CON



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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Display Port			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 52	of 103

(Blanking)

JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)S-Video			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 53 of	103

(Blanking)

JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)DVI			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet	54 of 103

(Blanking)

JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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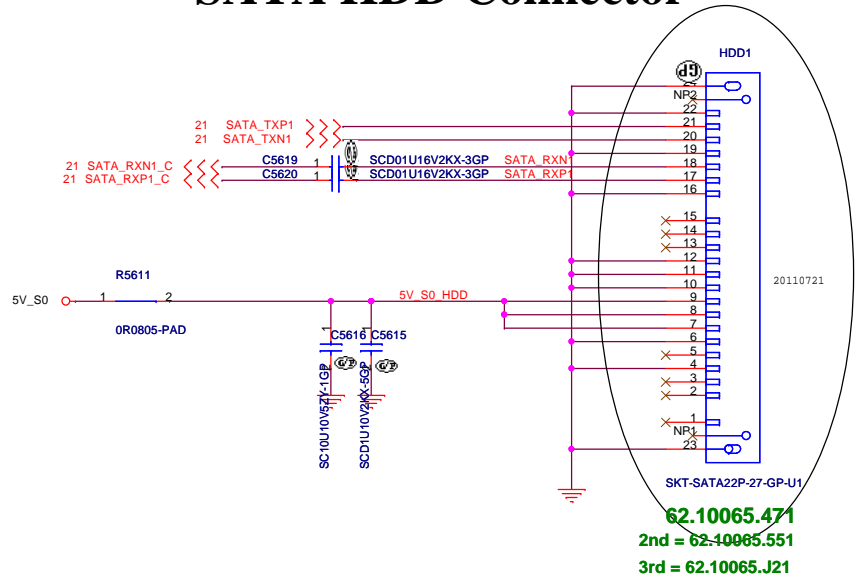
Title **(Reserved)ITP**

Size	Document Number	G48/G58	Rev	SC
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Date: Friday, February 17, 2012 Sheet 55 of 103

SSID = SATA

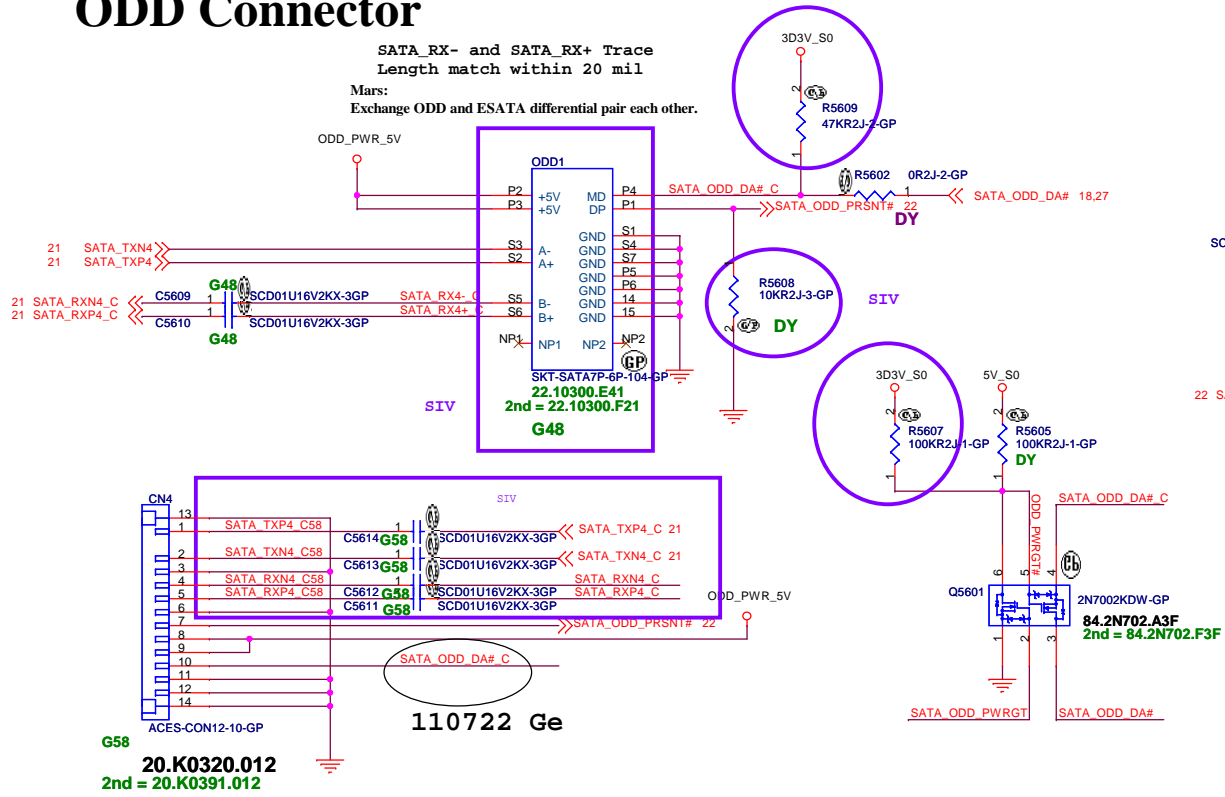
SATA HDD Connector



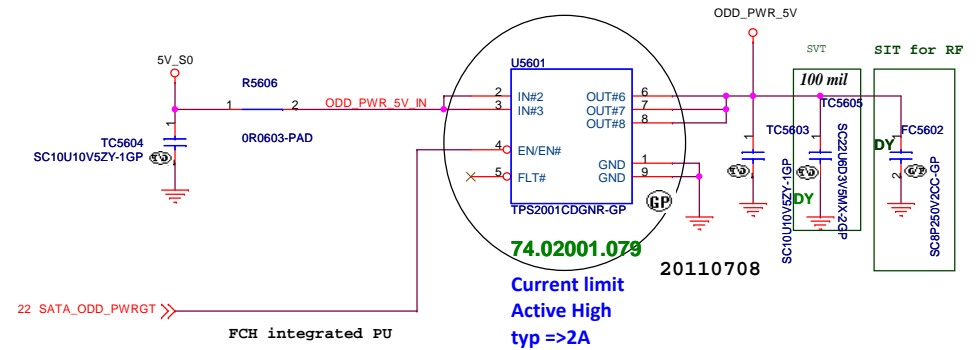
ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD



SUPPORT ZERO SATA ODD

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

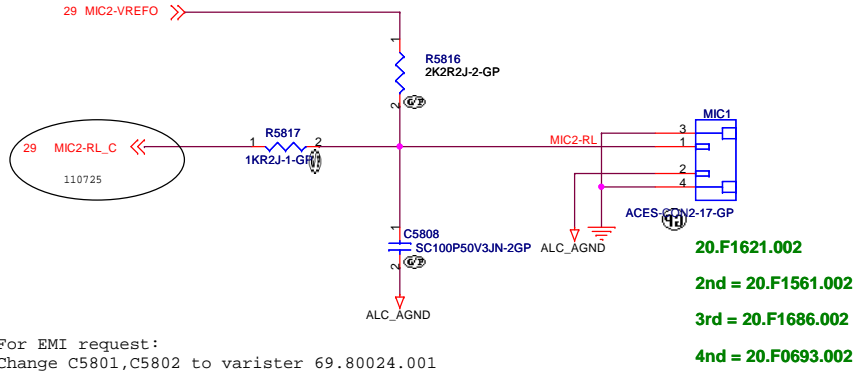
Title		HDD/ODD	
Size	Document Number	G48/G58	
Date: Friday, February 17, 2012	Sheet	56	of 103
			Rev SC

(Blanking)

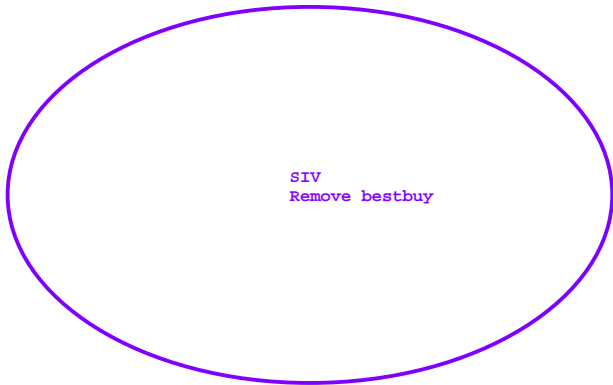
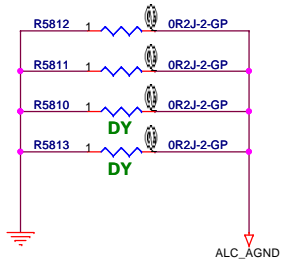
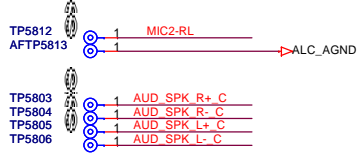
JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)E-SATA			
Size	Document Number	G48/G58	Rev SC
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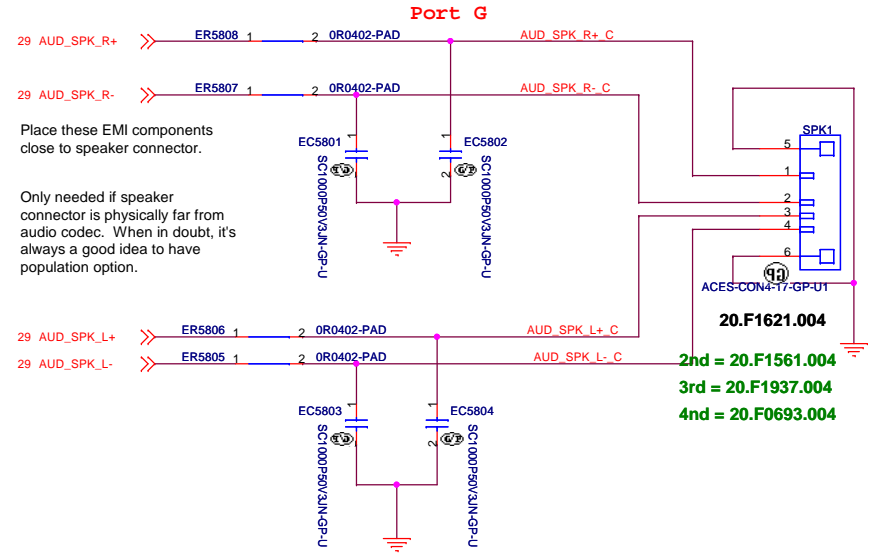
Analog Internal Mic



For EMI request:
Change C5801,C5802 to varister 69.80024.001

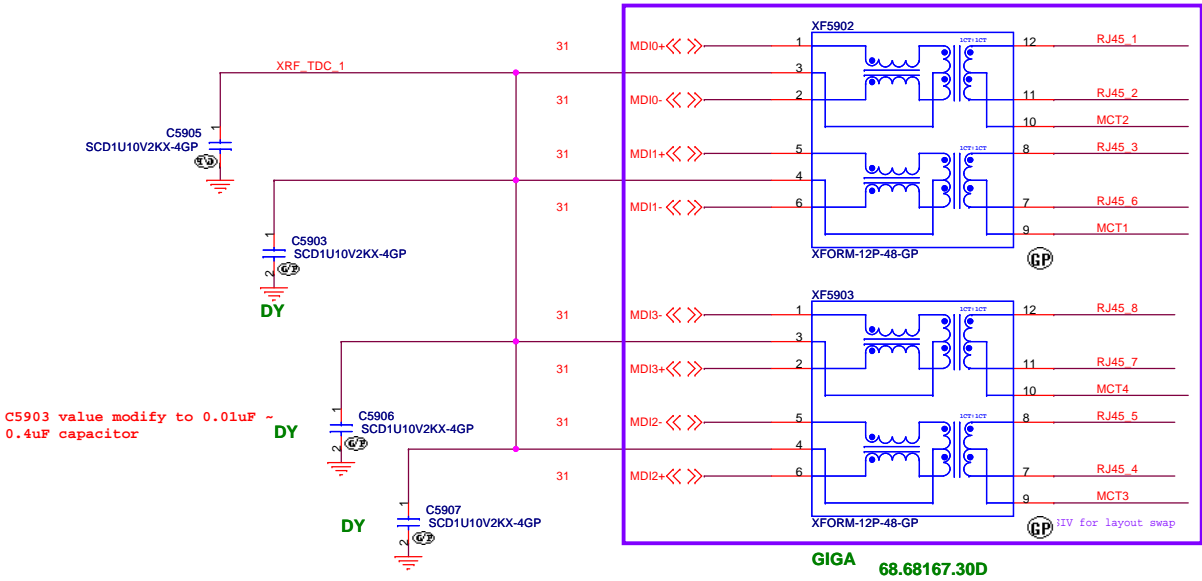


INTERNAL STEREO SPEAKERS



JV10-CS

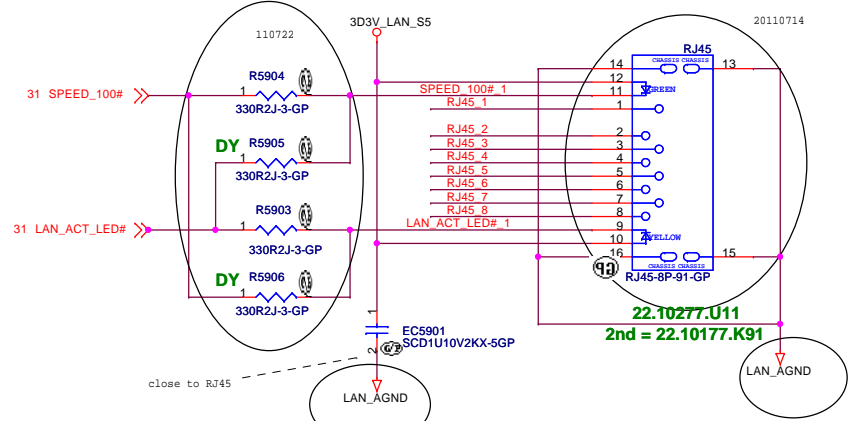
FOR CO-LAY GIGA Lan Transformer



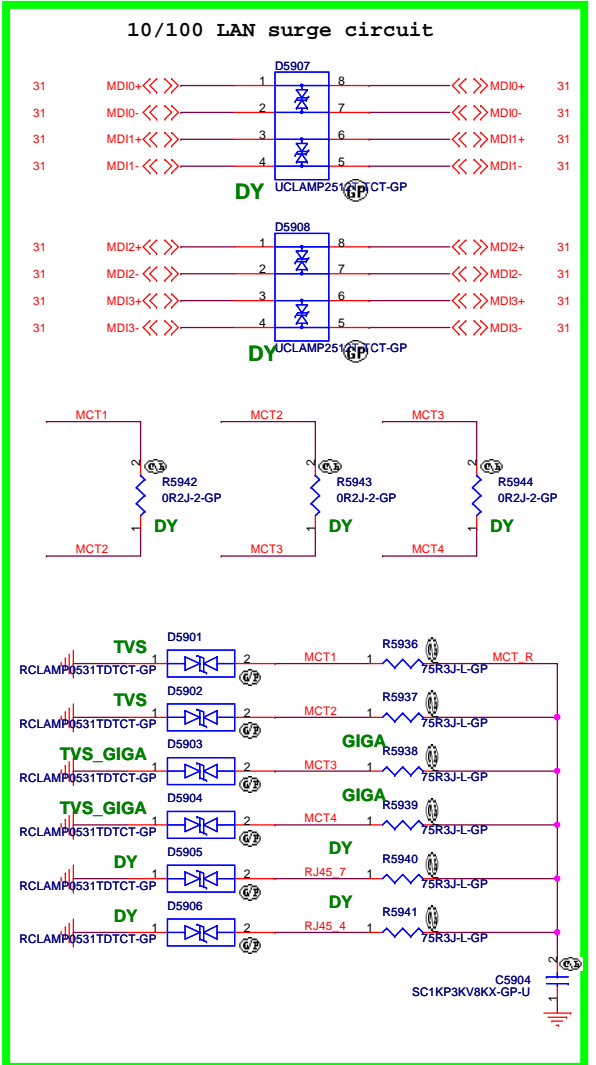
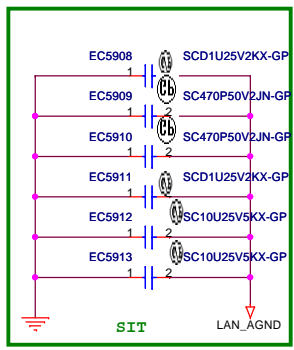
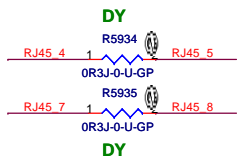
C5903 value modify to 0.01uF ~ 0.4uF capacitor

For AR8162(10/100M): C5906, C5907, R5938, R5939 can be DY.
 For AR8161(GIGA): Dummy R5934, R5935, R5940, R5941

LAN Connector



TPAD14-OP-GP	TP5909	1	3D3V LAN S5
TPAD14-OP-GP	TP5901	1	RJ45_1
TPAD14-OP-GP	TP5902	1	RJ45_2
TPAD14-OP-GP	TP5903	1	RJ45_3
TPAD14-OP-GP	TP5904	1	RJ45_4
TPAD14-OP-GP	TP5905	1	RJ45_5
TPAD14-OP-GP	TP5906	1	RJ45_6
TPAD14-OP-GP	TP5907	1	RJ45_7
TPAD14-OP-GP	TP5908	1	RJ45_8
TPAD14-OP-GP	TP5910	1	SPEED_100#
TPAD14-OP-GP	TP5912	1	LAN_ACT_LED#
TPAD14-OP-GP	TP5911	1	LAN_ACT_LED#_1
TPAD14-OP-GP	AFTP5912	1	LAN_ACT_LED#
TPAD14-OP-GP	AFTP5913	1	SPEED_100#_1
TPAD14-OP-GP	AFTP5914	1	LAN_AGND



83.00531.0AF
 2nd = 83.00511.0A0

83.00531.0AF
 2nd = 83.00511.0A0

83.00531.0AF
 2nd = 83.00511.0A0

83.00531.0AF
 2nd = 83.00511.0A0

JV10-CS

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

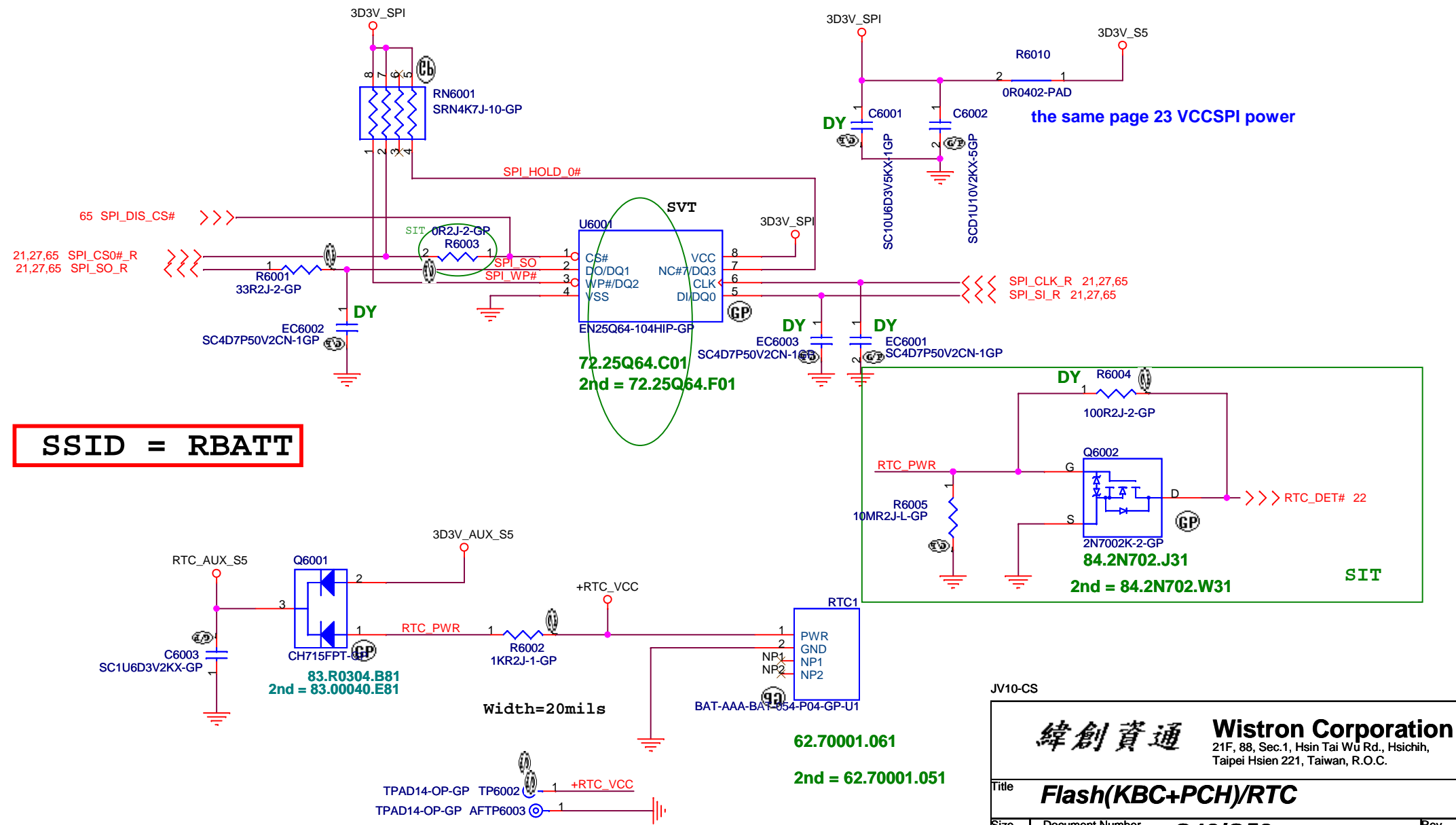
Title: **RJ45**

Size: Document Number **G48/G58** Rev: **SC**

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SSID = Flash.ROM

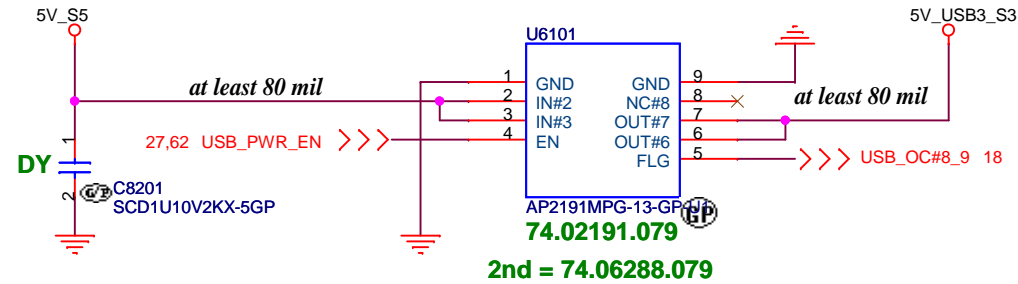
SPI FLASH ROM (8M byte) for PCH



JV10-CS	
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Flash(KBC+PCH)/RTC	
Size	Document Number G48/G58
Date	Rev SC
Friday, February 17, 2012	Sheet 60 of 103

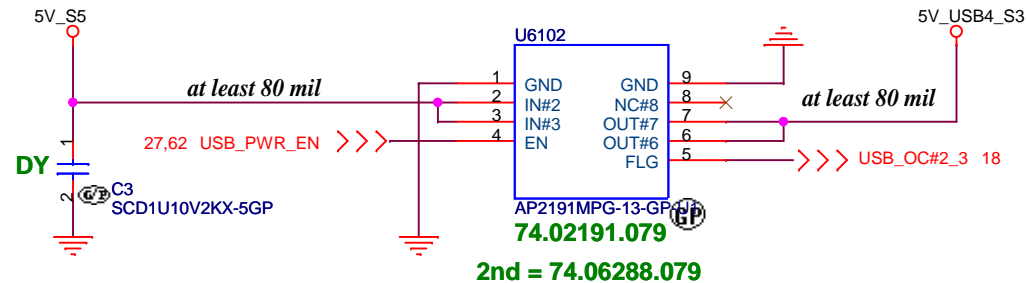
SSID = USB

USB Ext. port3 power SW



U6101 place near to USBCN3

USB Ext. port4 power SW

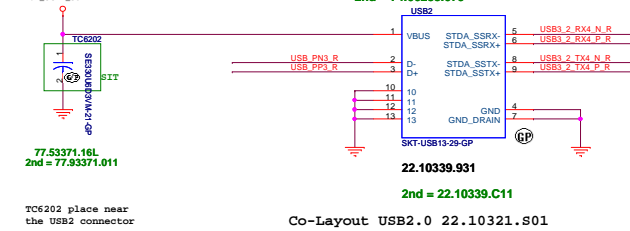
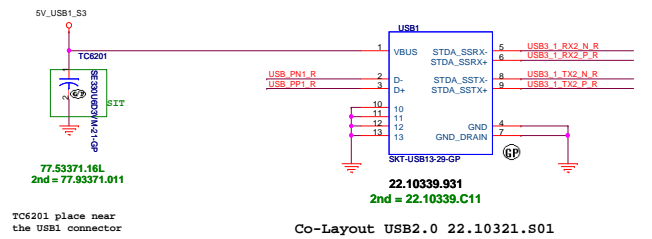
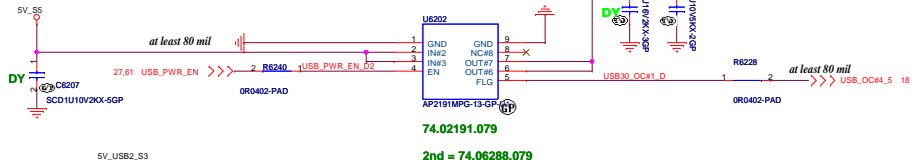
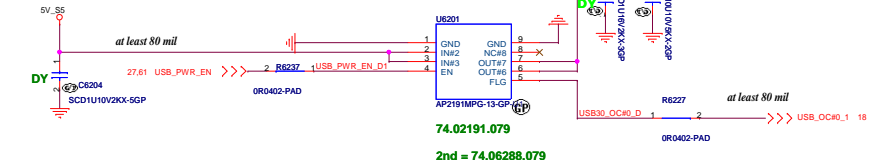


U6102 place near to CDRCN2

JV10-CS

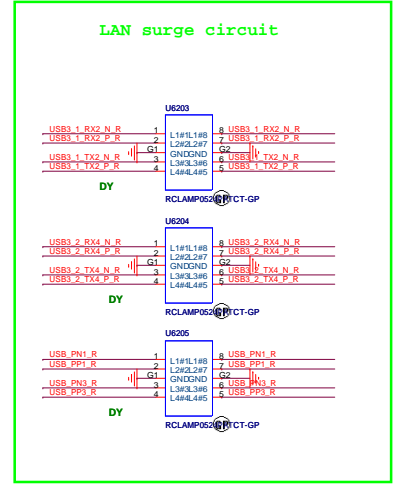
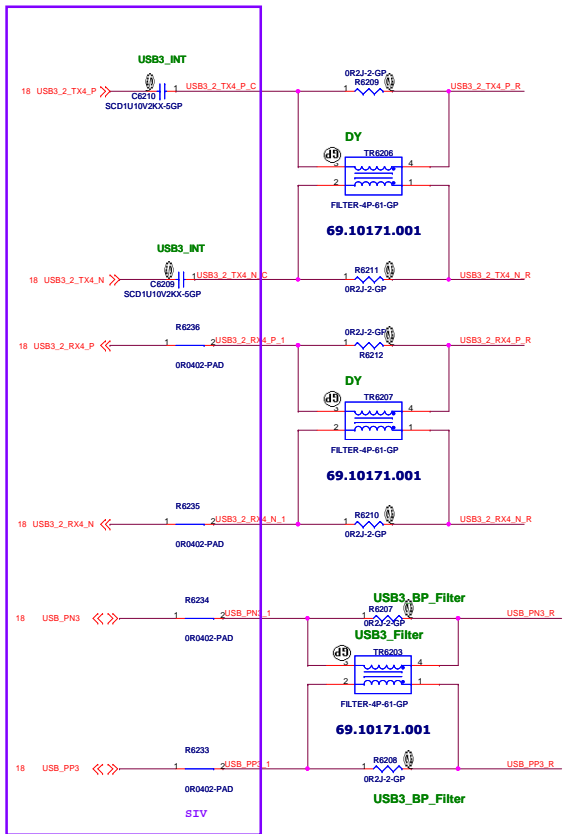
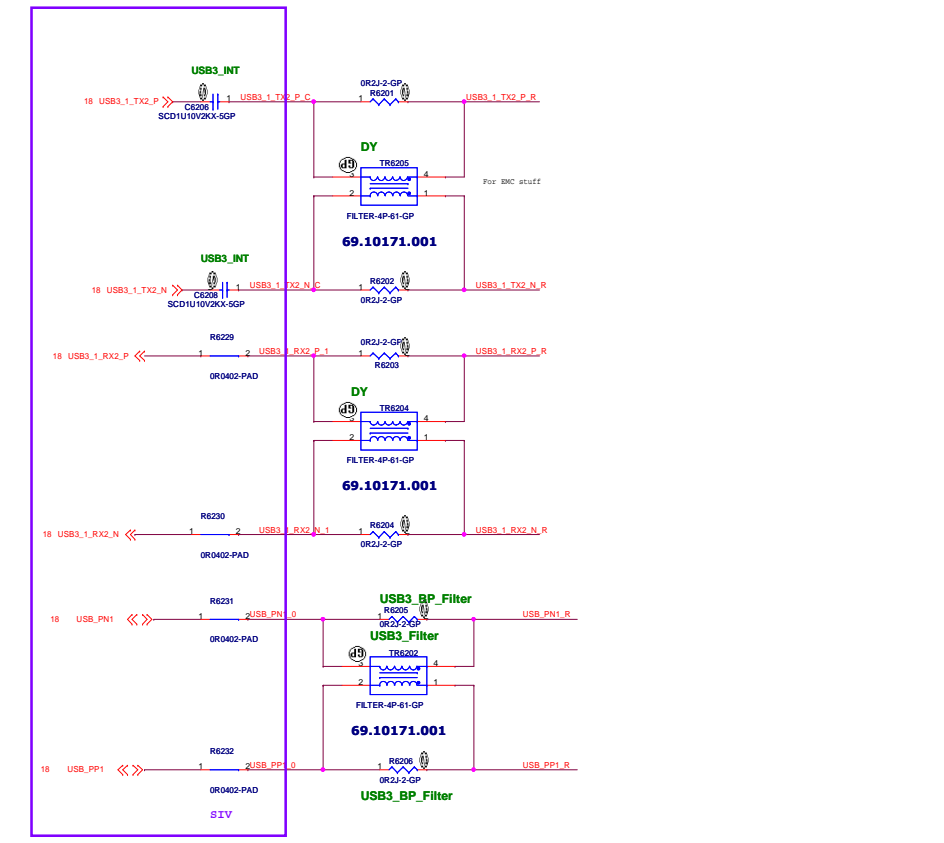
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB2.0 Port Power SW			
Size	Document Number	G48/G58	
		Rev	SC
Date: Friday, February 17, 2012		Sheet	61 of 103

USB3.0 Port1



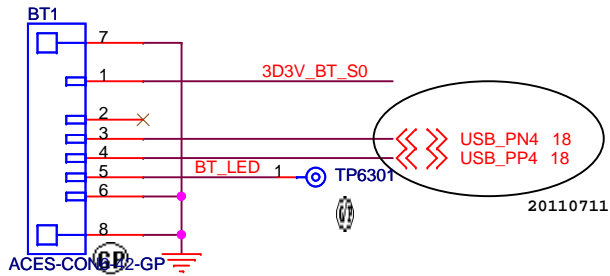
Co-Layout USB2.0 22.10321.S01

Co-Layout USB2.0 22.10321.S01

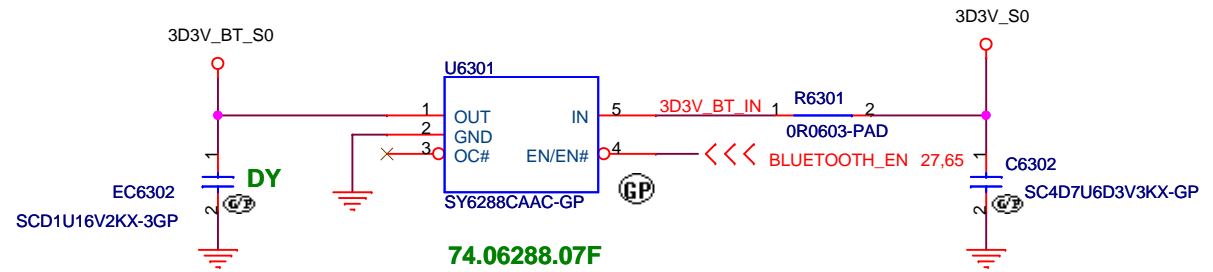


SSID = User.Interface

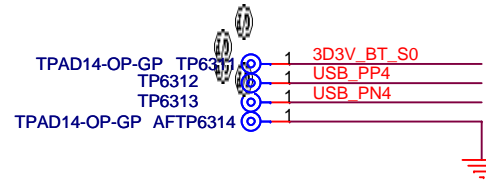
Bluetooth conn.



20.F1705.006
 2nd = 20.F1804.006
 3rd = 20.F1571.006



EC6302 put near
 BLUE1 / all USB
 put one choke
 near connector
 by EMI request



JV10-CS

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **BLUETOOTH**

Size	Document Number	G48/G58	Rev	SC
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Date: Friday, February 17, 2012 Sheet 63 of 103

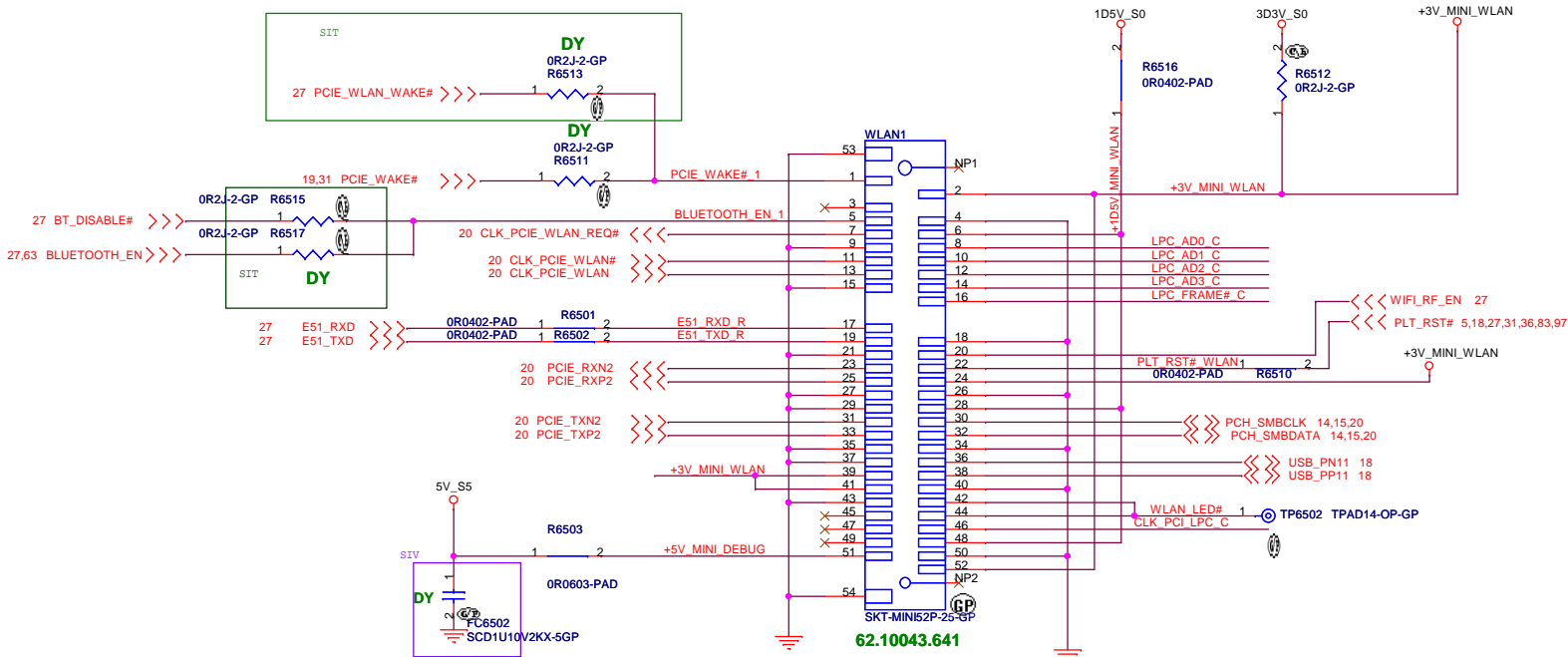
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JV10-CS

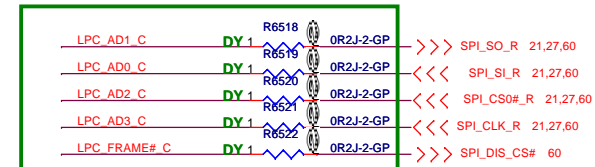
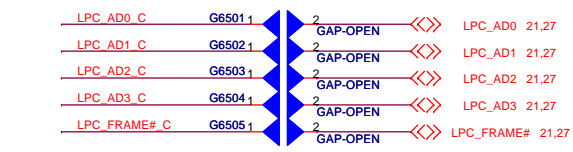
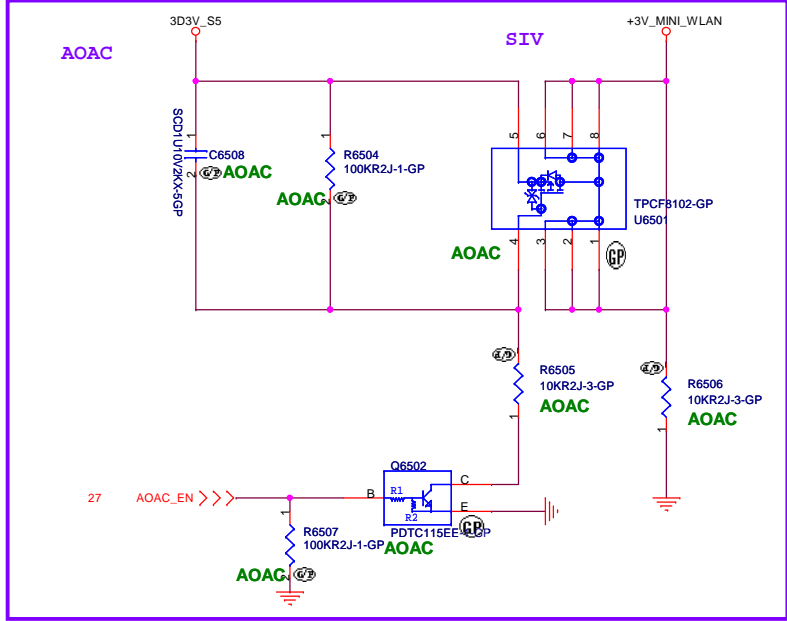
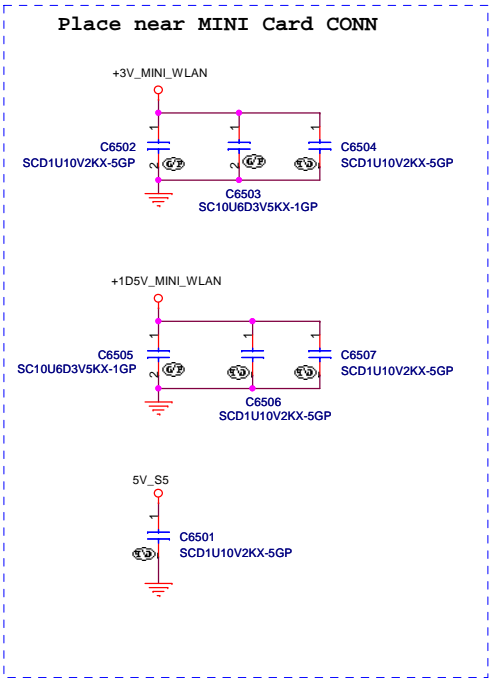
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Finger Print Con.			
Size	Document Number	G48/G58	Rev SC
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SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



62.10043.641
2nd = 62.10043.F01
3rd = 62.10043.F21



SSID = Wireless

Mini Card Connector(WWAN)

(Blanking)

JV10-CS

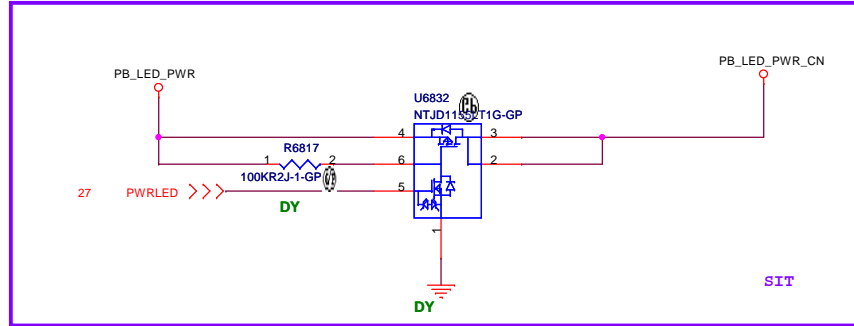
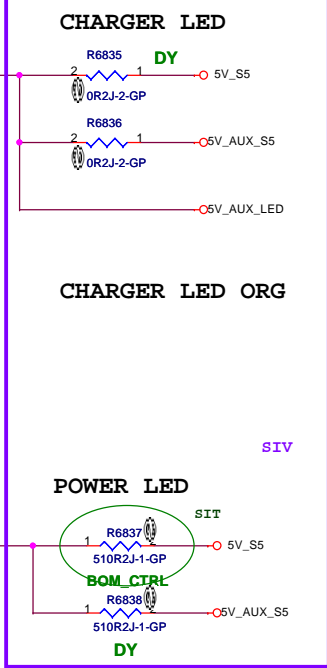
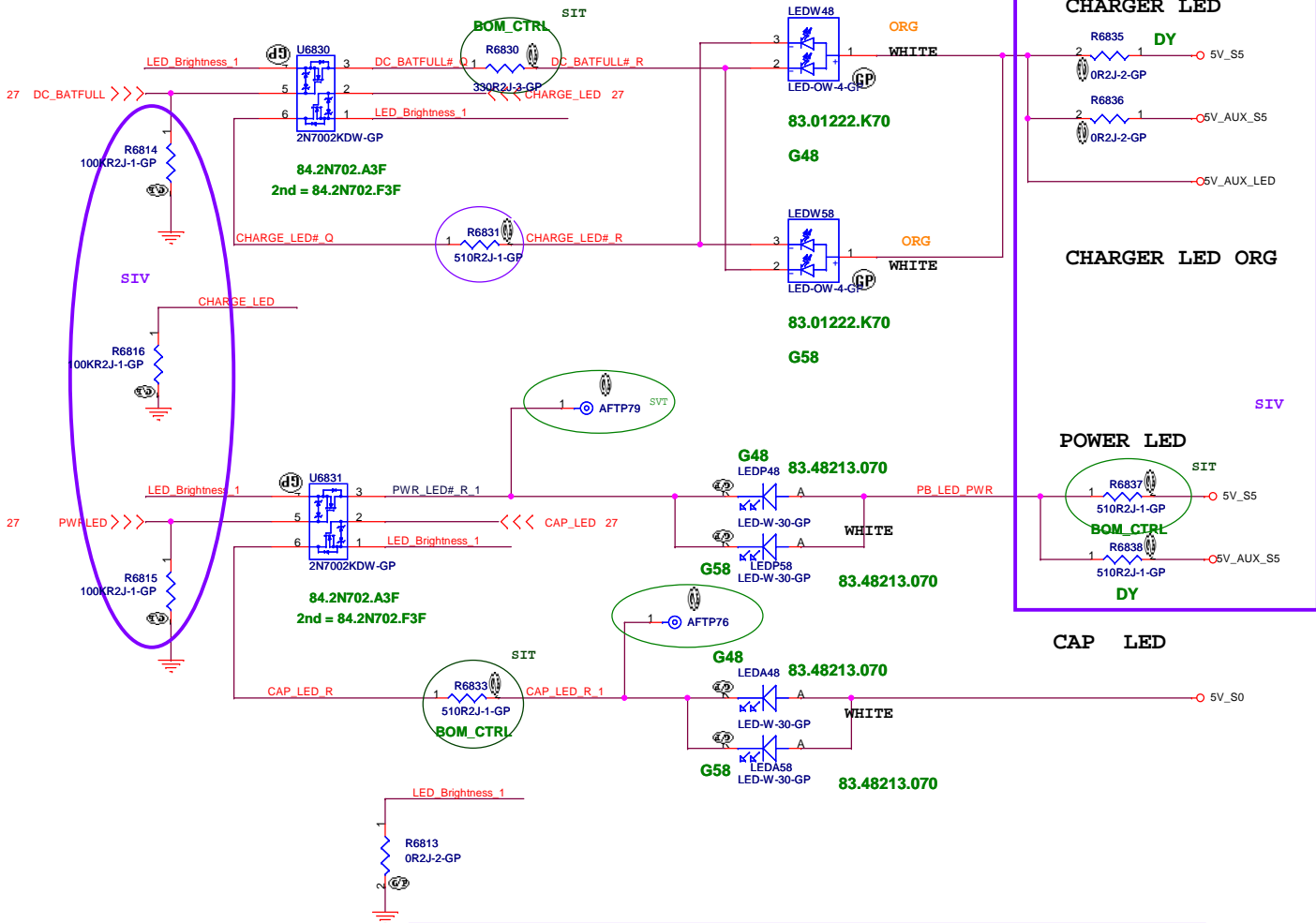
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)WWAN CONN			
Size	Document Number	G48/G58	Rev SC
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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)3rd MINICARD			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 67	of 103

SSID = User.Interface



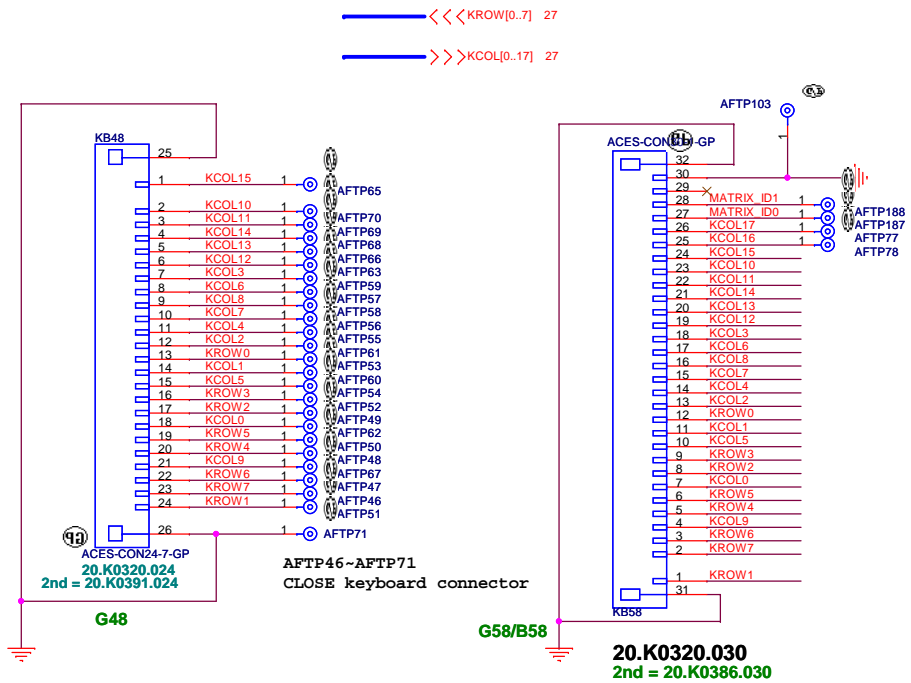
JV10-CS

<p>緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title LED/Power Button/key</p>	
Size	<p>Document Number G48/G58</p>
Date: Friday, February 17, 2012	<p>Rev SC</p>
<p>Sheet 68 of 103</p>	

SSID = KBC

KBL Follow LA47

Internal KeyBoard Connector



14"

* Membrane Pin Out Top View :

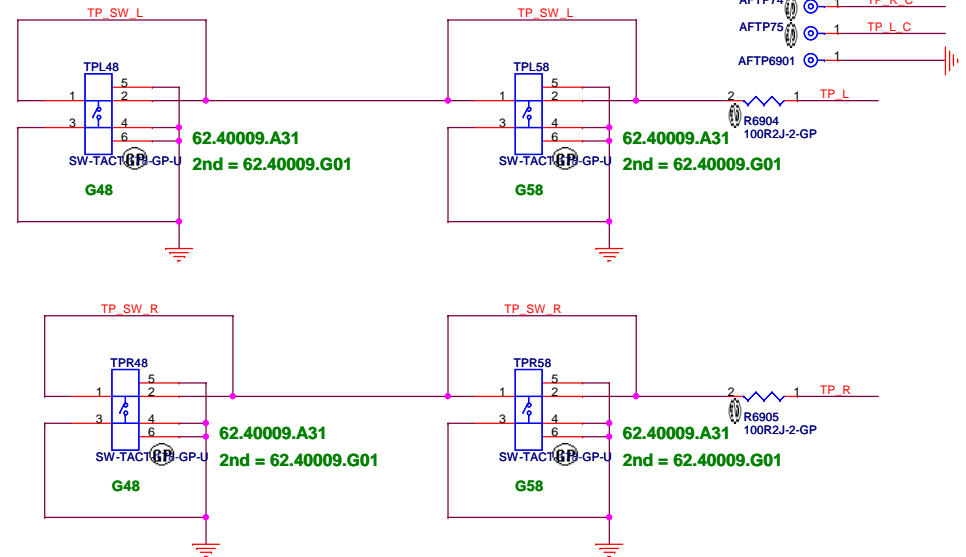
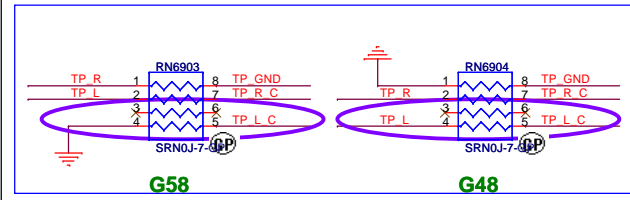
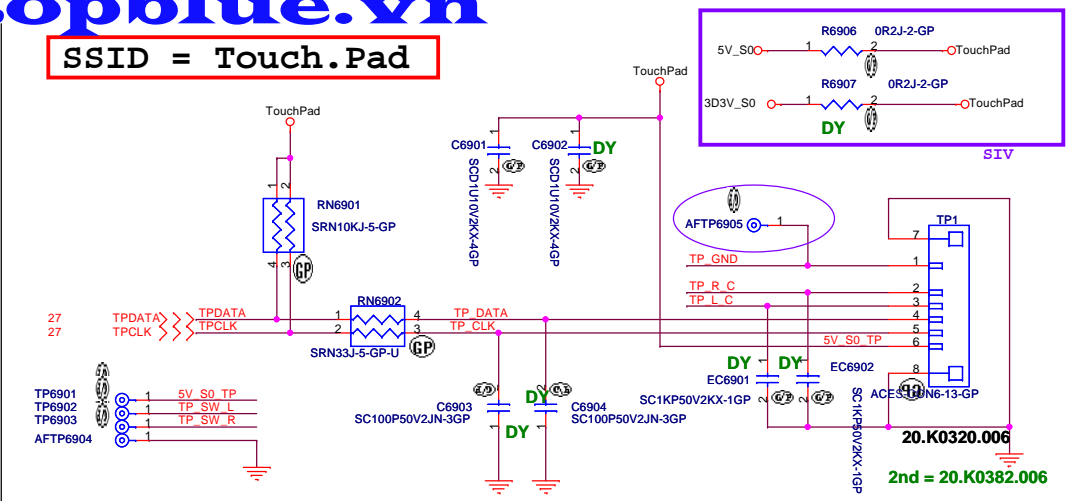
PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

15"

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	D 17	D 18	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Key Board/Touch Pad**

Size: Document Number **G48/G58** Rev: **SC**

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JV10-CS

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **Hall Sensor**

Size	Document Number	Rev
	G48/G58	SC

(Blanking)

JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Debug connector			
Size	Document Number	G48/G58	Rev SC
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)RJ11+MDC			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 72 of	103

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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)1394 CONN			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 73 of	103

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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)CARD Reader CONN			
Size	Document Number	G48/G58	Rev SC
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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Express Card			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 75 of	103

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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Smart Card Socket			
Size	Document Number	G48/G58	Rev SC
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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

Title **(Reserved)TPM**

Size	Document Number	G48/G58	Rev	SC
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JV10-CS

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)SIO			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 78	of 103

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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)G-Sensor			
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet	79 of 103

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JV10-CS

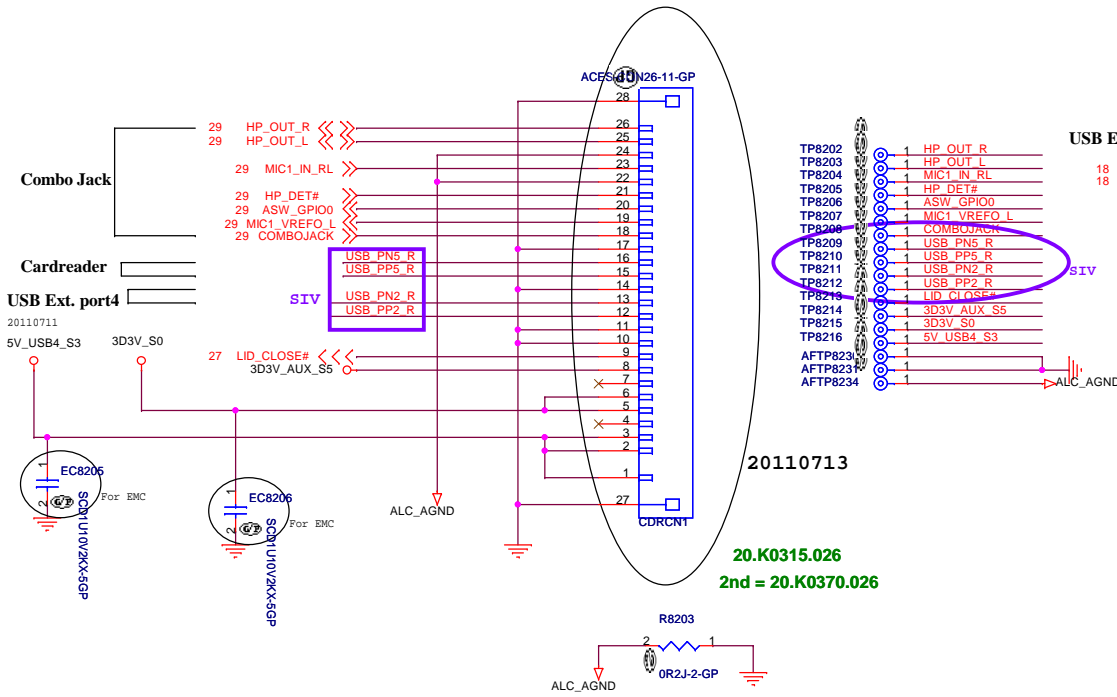
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)RF/Other			
Size	Document Number	G48/G58	Rev SC
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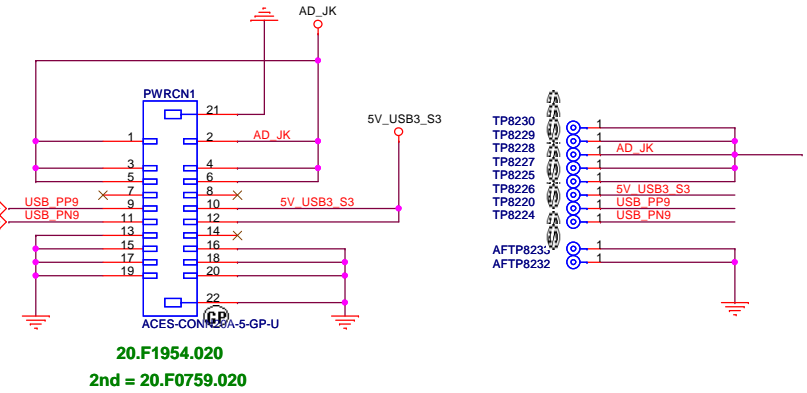
JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Screw Holes,SPR			
Size	Document Number	G48/G58	Rev SC
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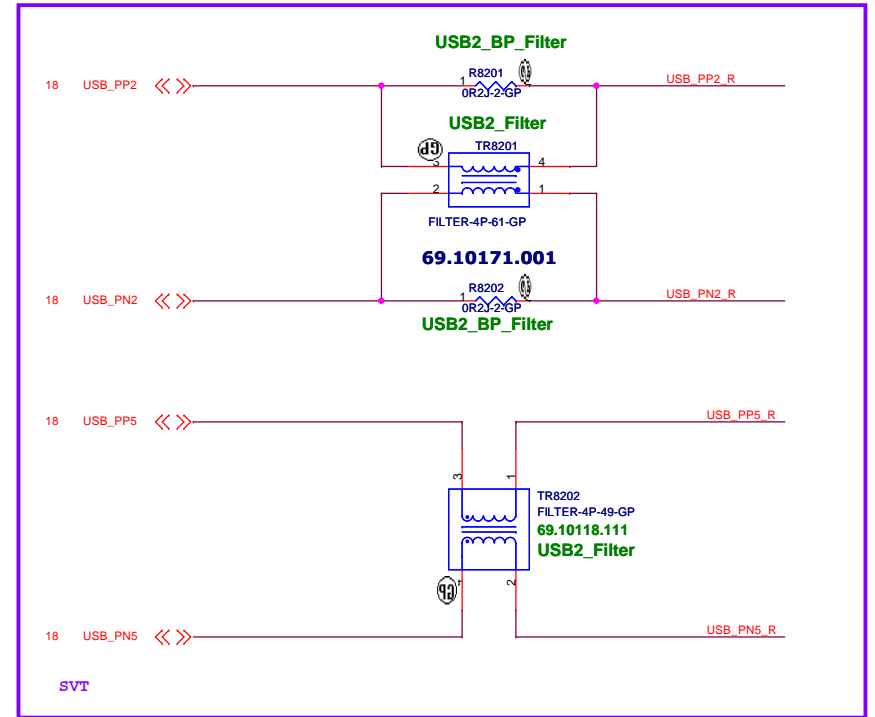
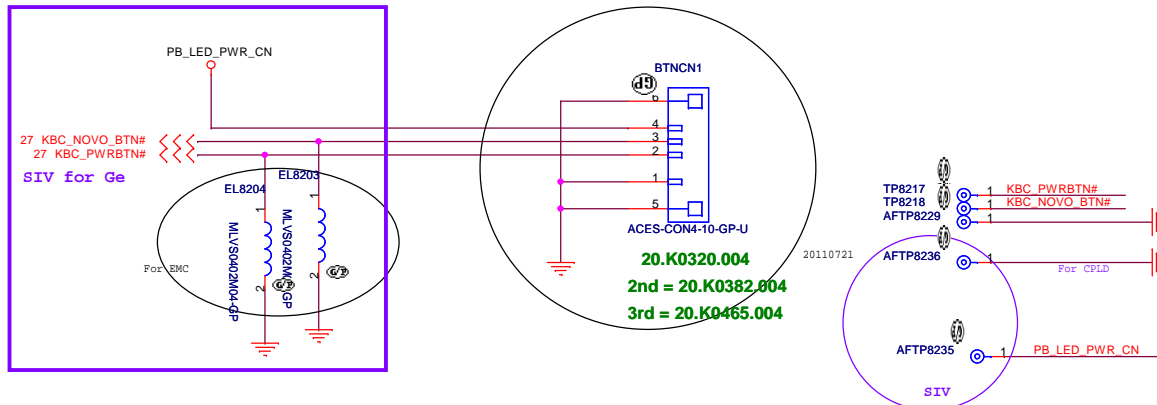
Cardreader BD connector
(Cardreader/Combo Jack/USB2.0 port4)



USB BD connector
(DC Jack/USB2.0 port3)



Button BD connector
(Power button/NOVO button)



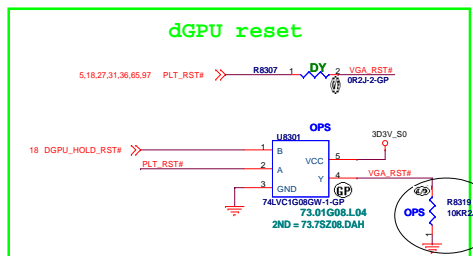
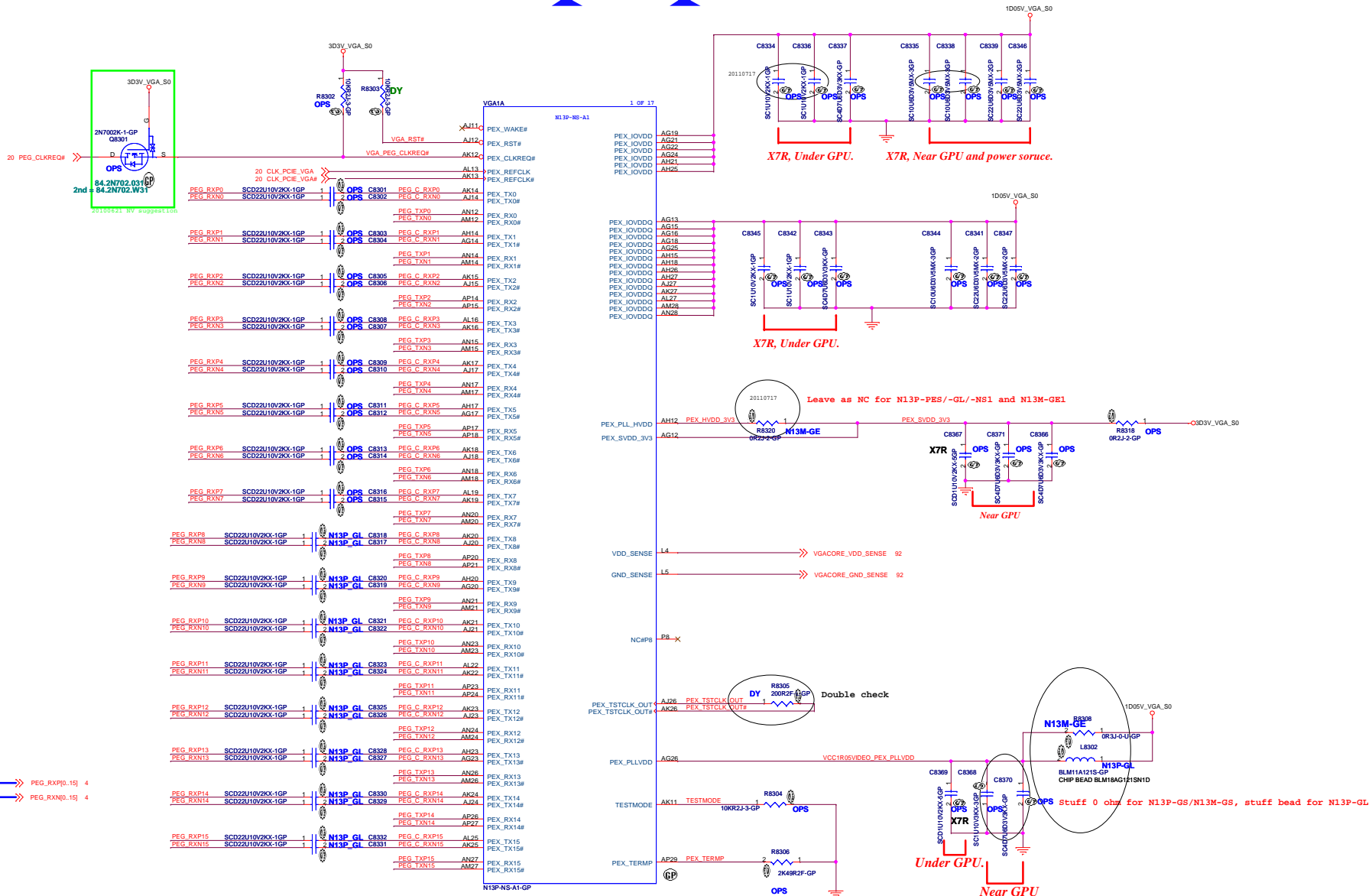
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

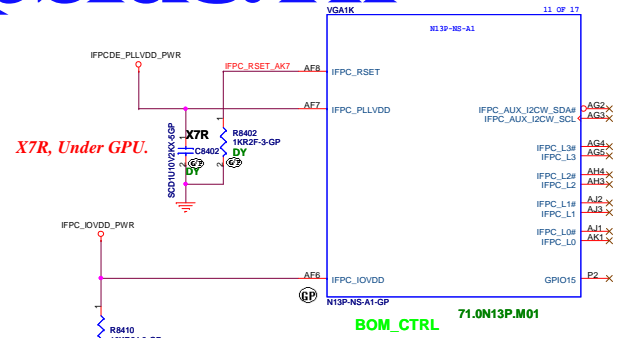
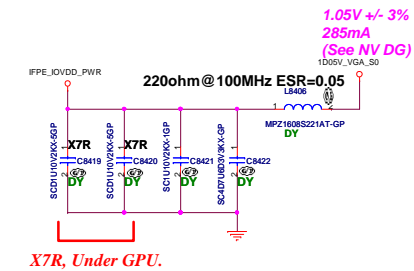
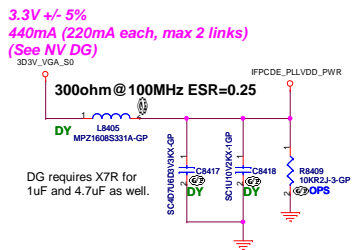
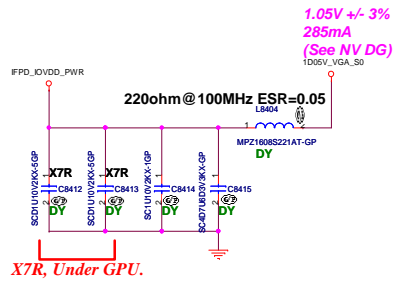
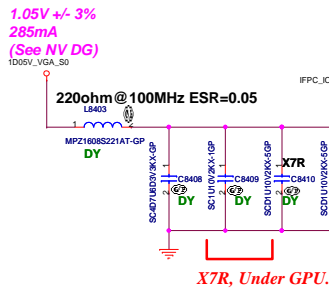
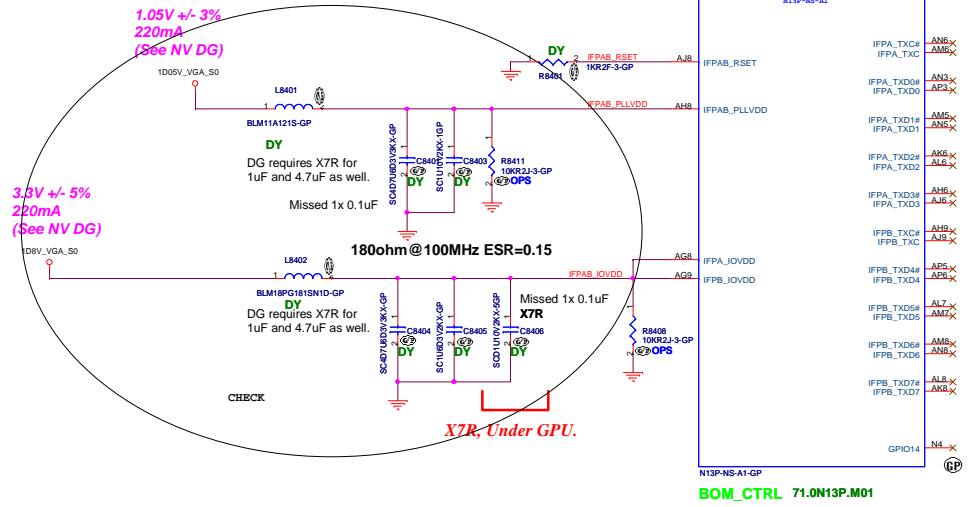
Title IO Board Connector

Size Document Number G48/G58 Rev SC

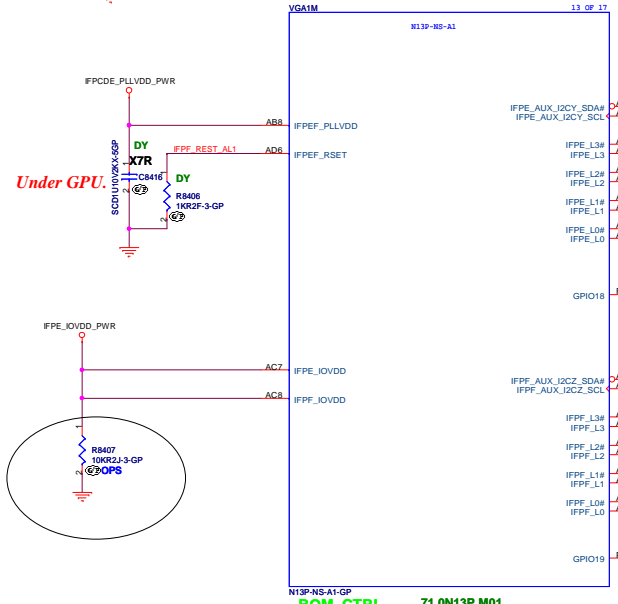
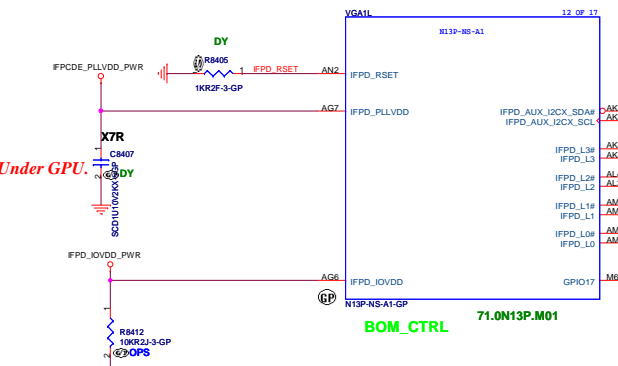
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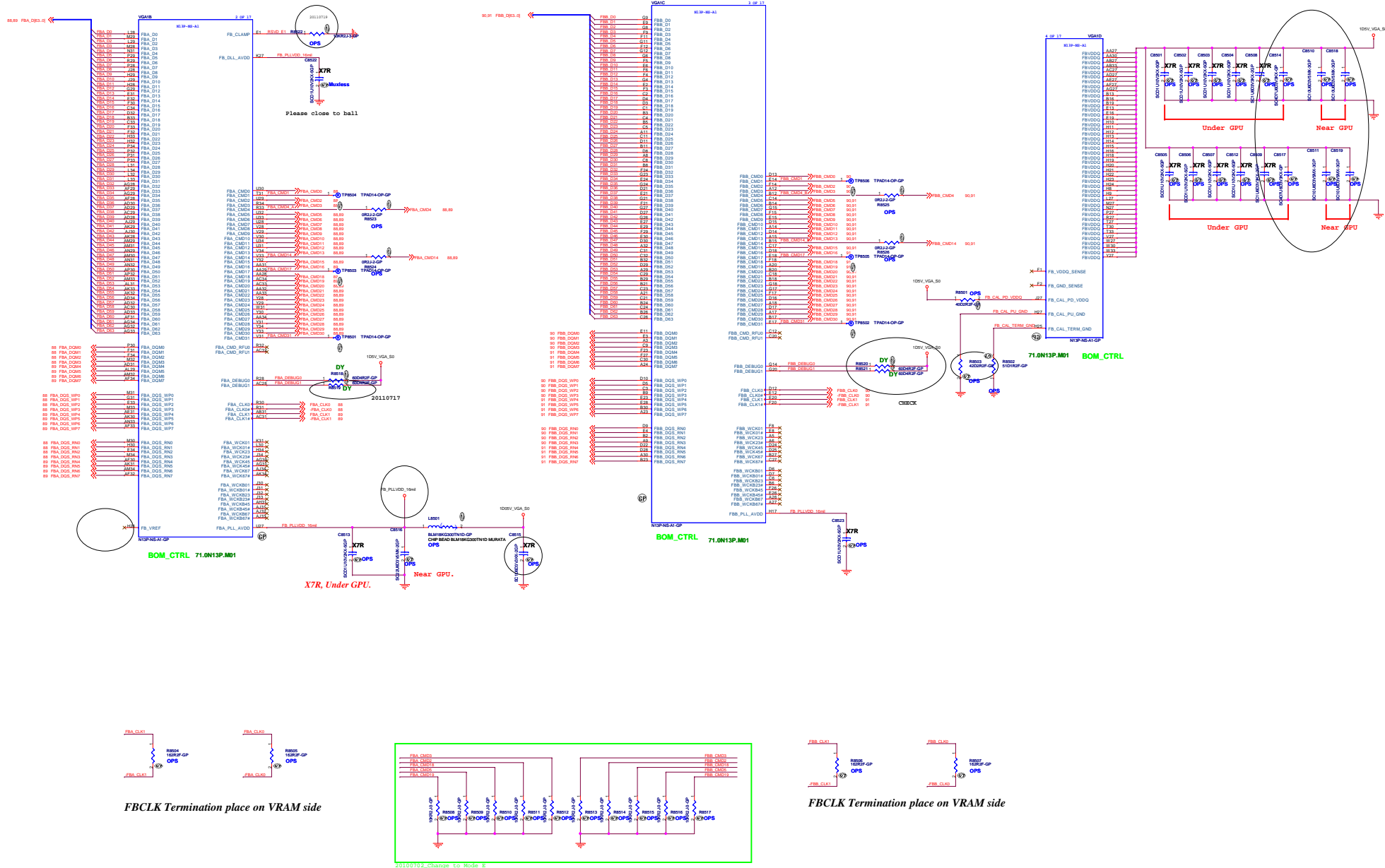


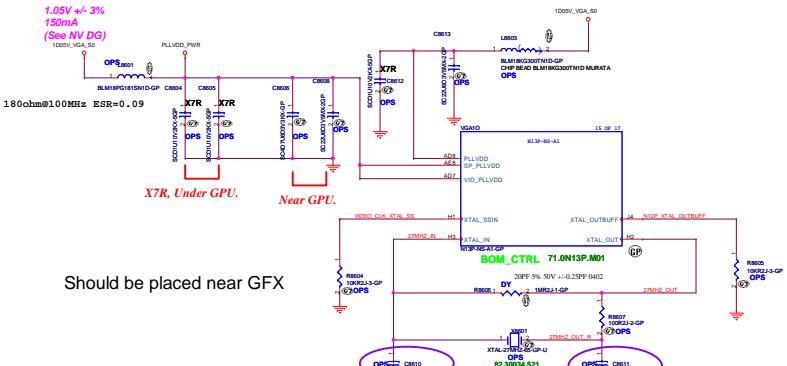
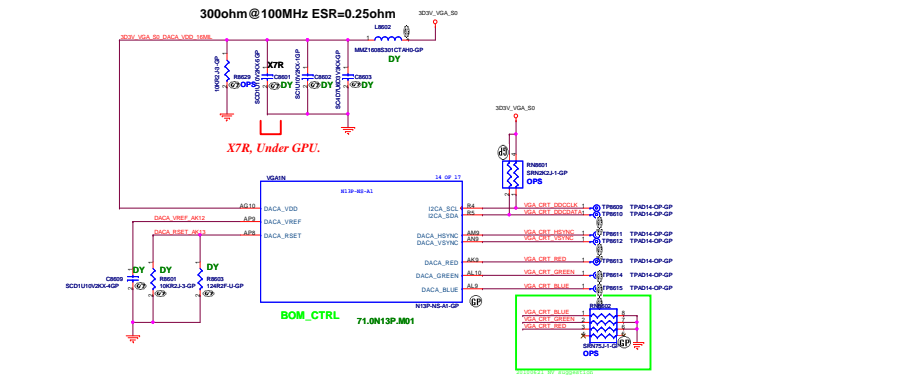
LVDS Interface



HDMI Interface



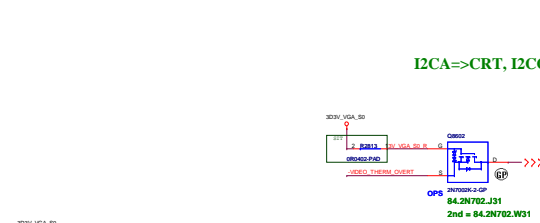
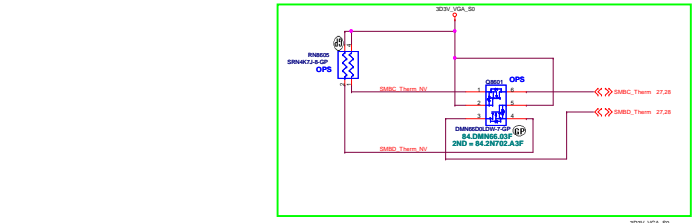




Should be placed near GFX

Should be placed near GFX

I2CA=>CRT, I2CC=>LVDS.



HARMONY 27MHz,
12P 30PPM
HSX30G

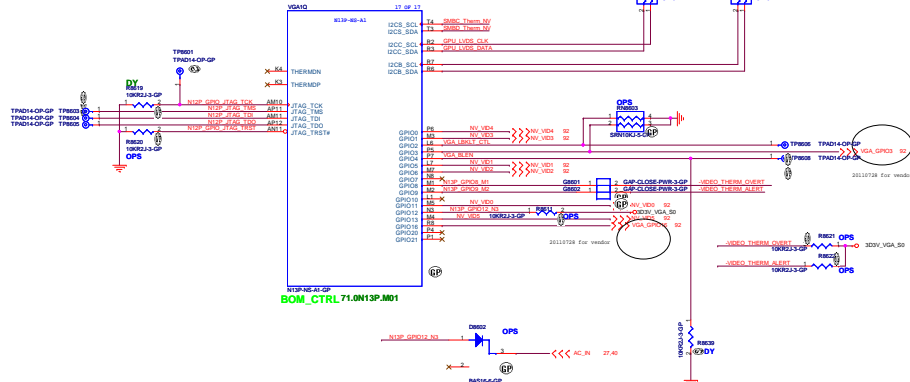
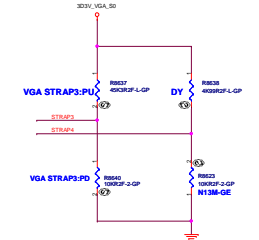
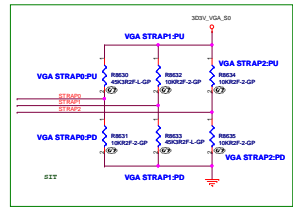


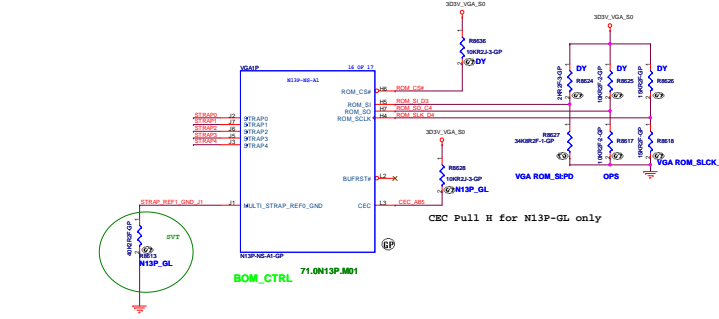
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STRAP0	R8630(PU) R8631(PD) DY
STRAP1	R8632(PU) R8633(PD)
STRAP2	R8634(PU) R8635(PD)
STRAP3	R8637(PU) R8640(PD)
STRAP4	R8638(PU) R8623(PD)

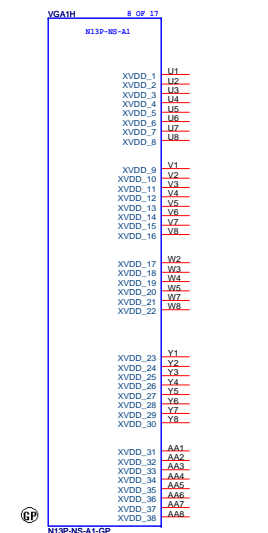
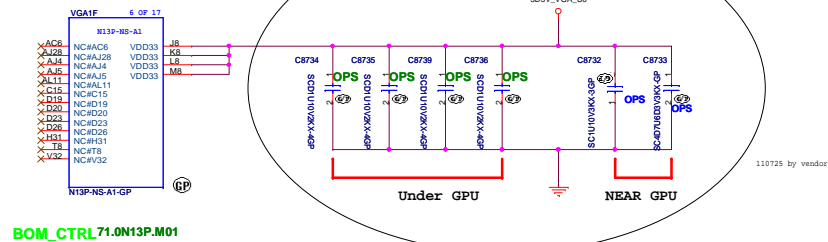
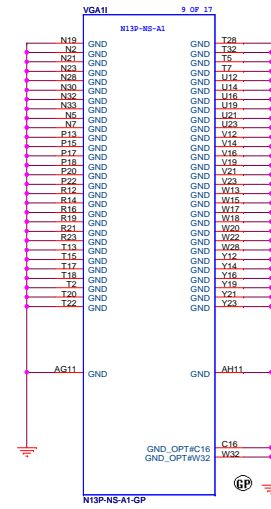
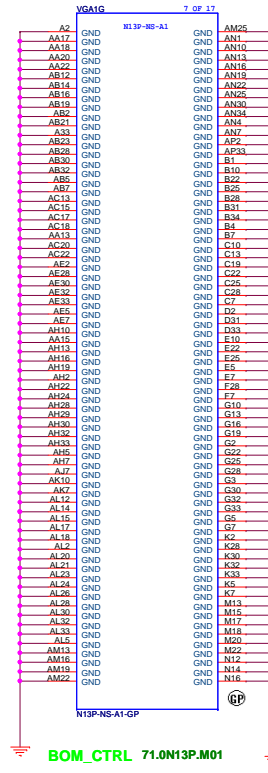
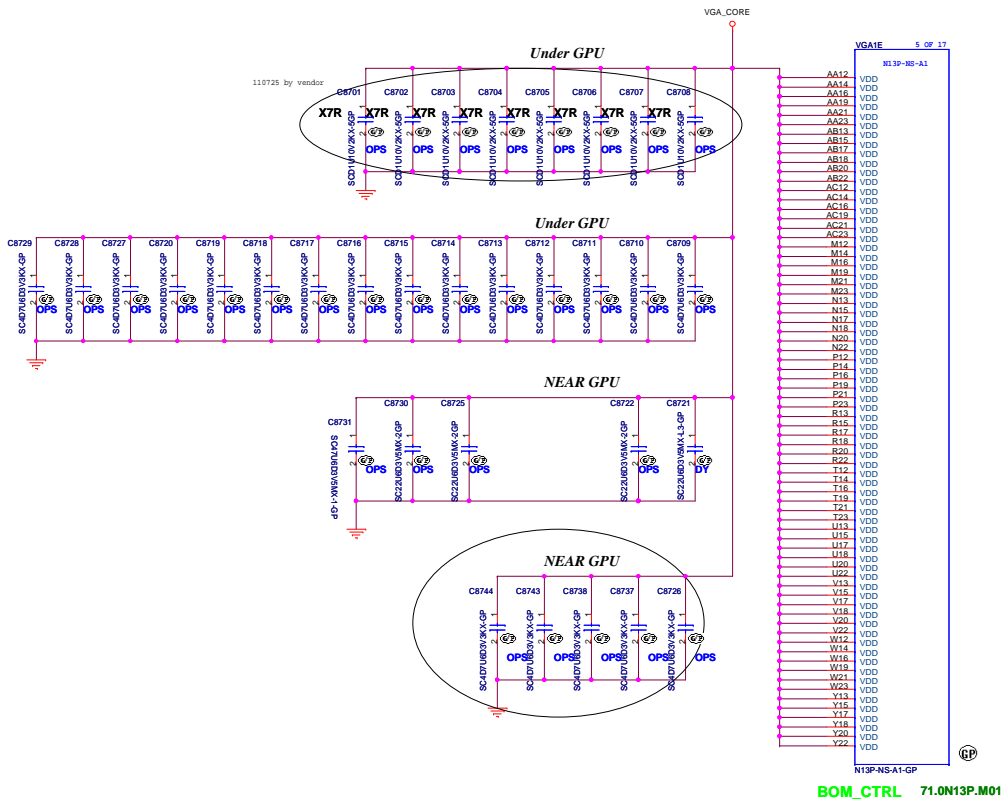
N13M-GE(PS)					
TABLE NVIDIA	SAMSUNG 128Mx16 72.42164.D0U	SAMSUNG 128Mx16 72.42164.G0U	HYNIX 128Mx16 72.52G63.C0U	Samsung 64Mx16	HYNIX 64Mx16
STRAP0	R8630(PU) R8631(PD) DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL
STRAP1	R8632(PU) R8633(PD)	DY 10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL
STRAP2	R8634(PU) R8635(PD)	10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL
STRAP3	R8637(PU) R8640(PD)	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL
STRAP4	R8638(PU) R8623(PD)	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL	DY 10Kohm 64.10025.6DL

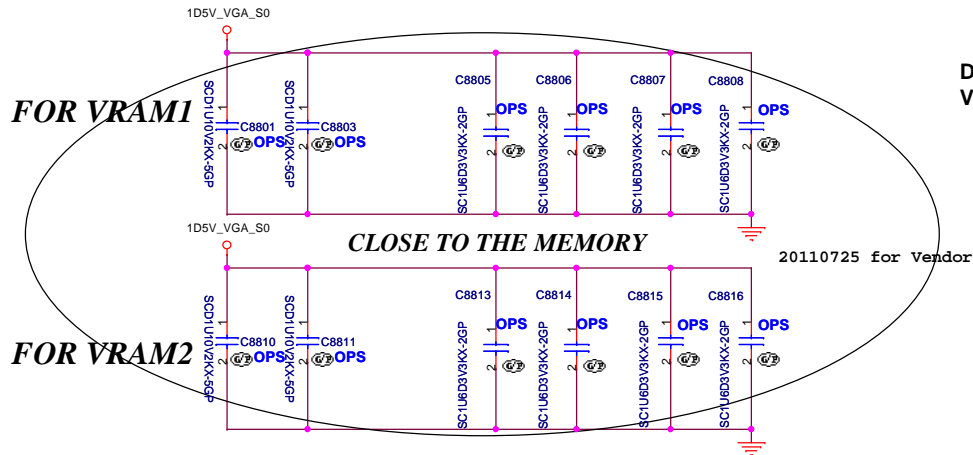
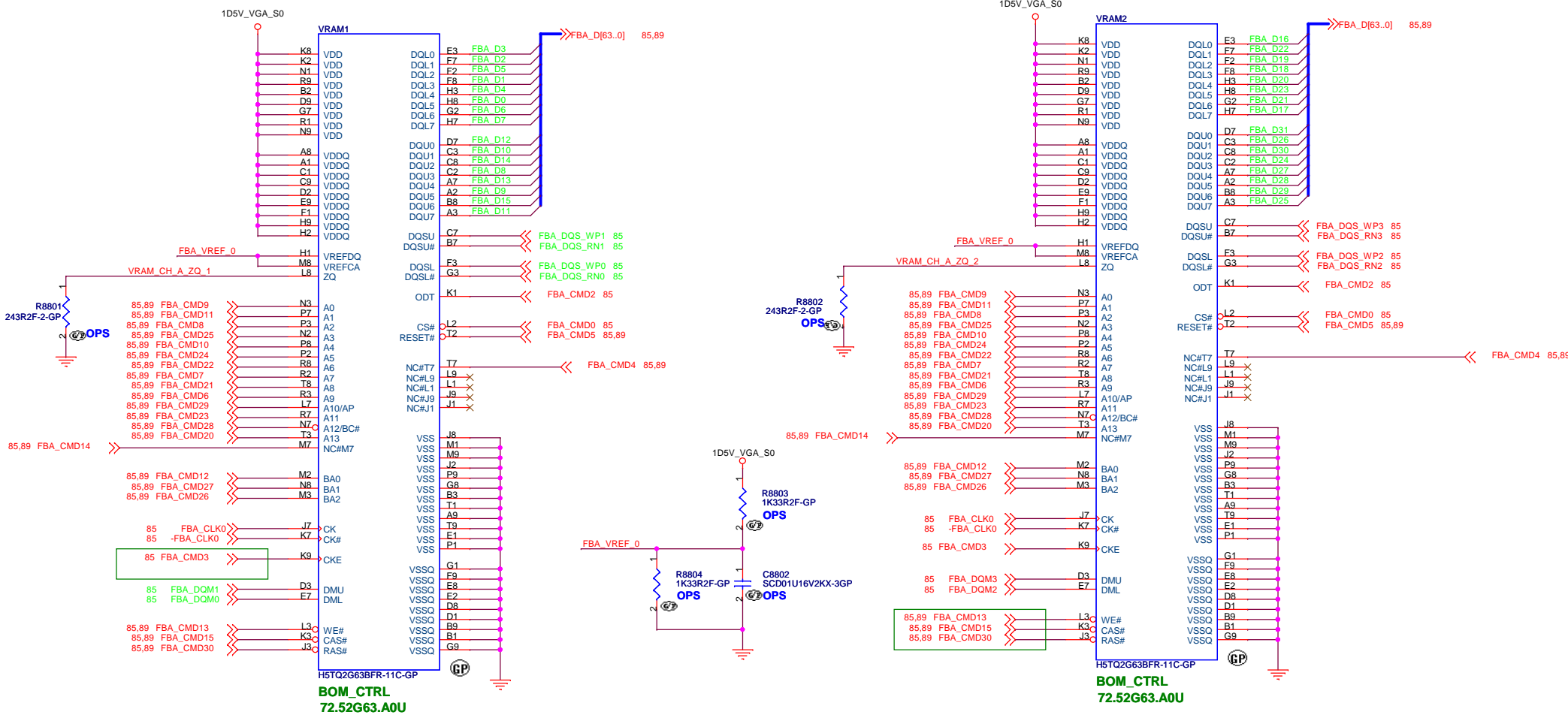
TABLE VIDEO MEMORY

Nvidia VGA	900MHz	HYNIX 128Mx16	SAMSUNG 128Mx16	HYNIX 64Mx16	Samsung 64Mx16
		72.52G63.C0U	72.42164.D0U 72.42164.G0U	72.51G63.H0U	72.41646.Q0U
N13P-GL	ROM_SI PD R8627	30.1Kohm 64.30125.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL
N13M-GE	ROM_SI PD R8627	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL

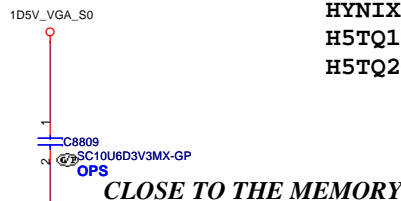
VGA	N13P-GL(PS) 71.0N13P.E0U	N13M-GE(PS) 71.0N13M.BIU
ROM_SO PD R8617	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
ROM_SCLK PD R8618	15Kohm 64.15025.6DL	10Kohm 64.10025.6DL







DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VRAM

SAMSUNG:

K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
 K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:

H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
 H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT A

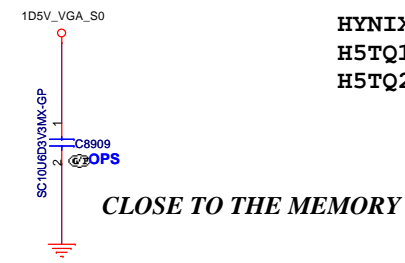
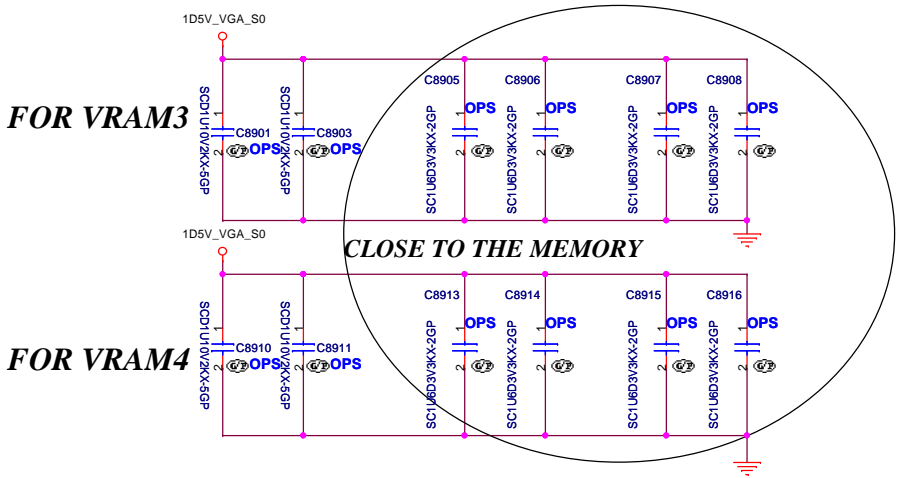
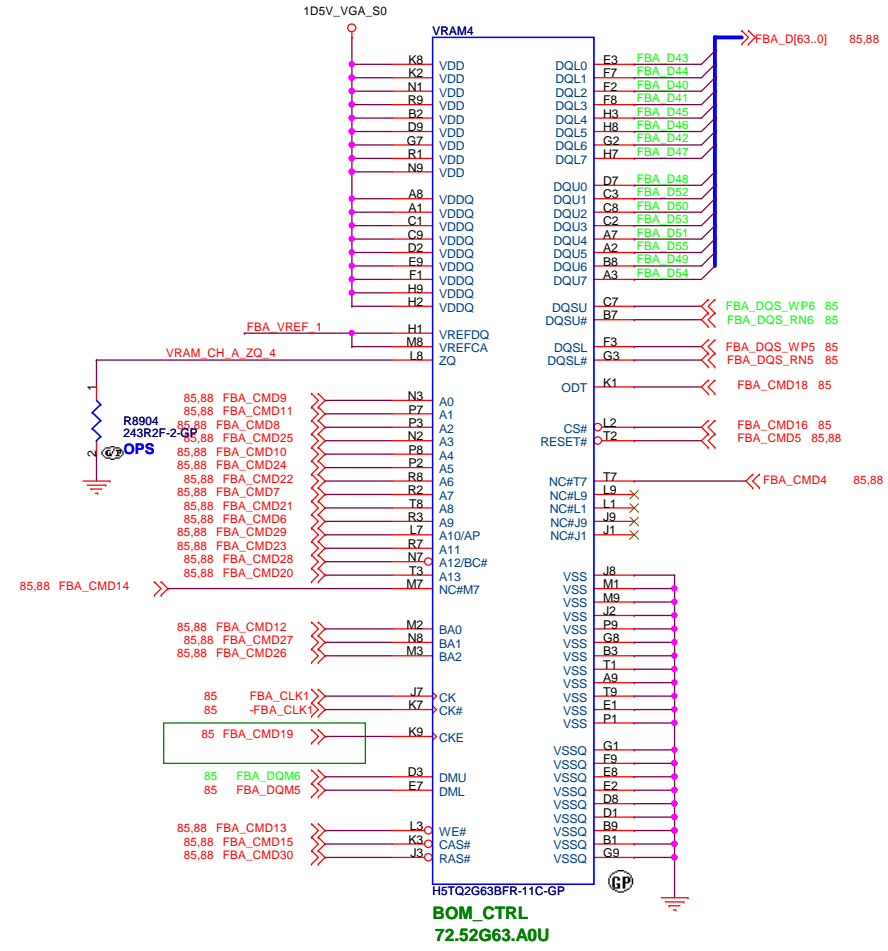
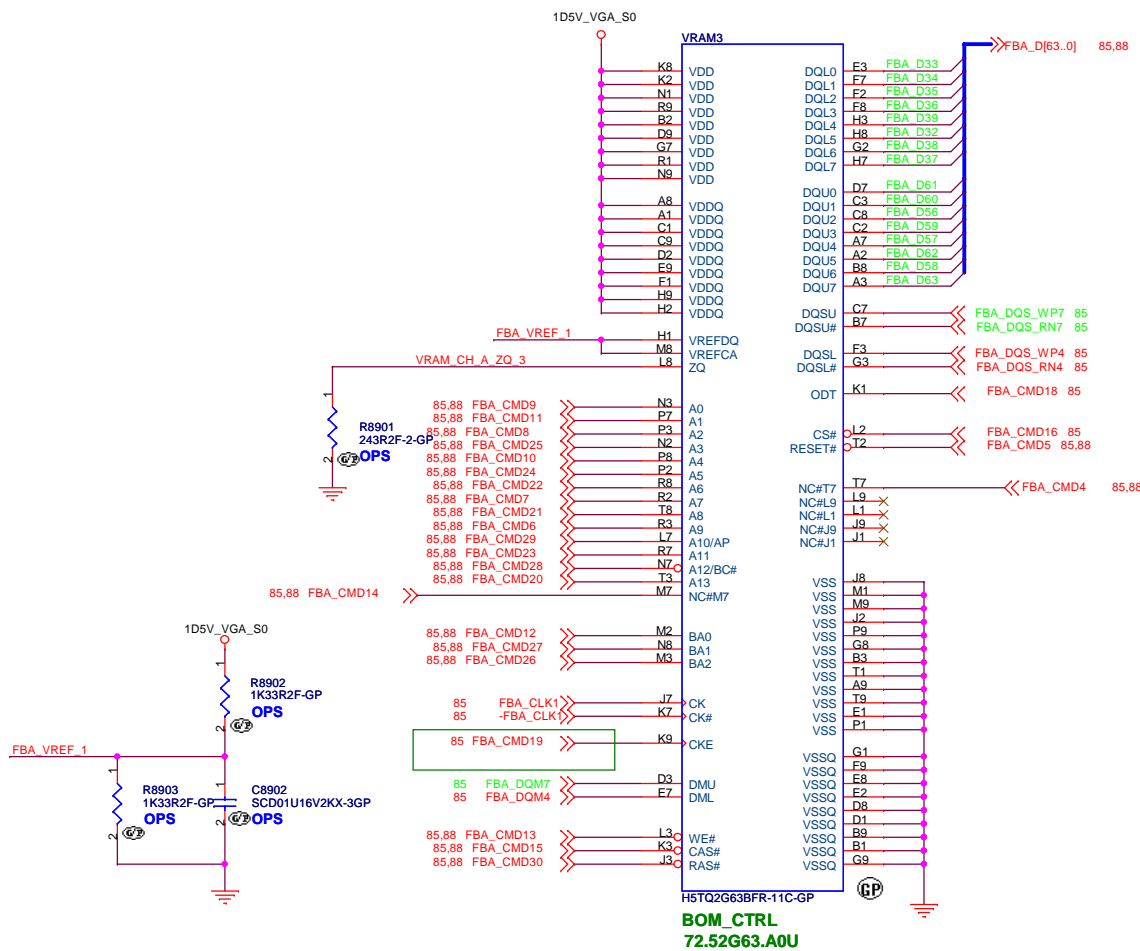
JV10-CS

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **VRAM1,2 (1/4)**

Size Document Number **G48/G58** Rev **SC**

Date: Friday, February 17, 2012 Sheet 88 of 103

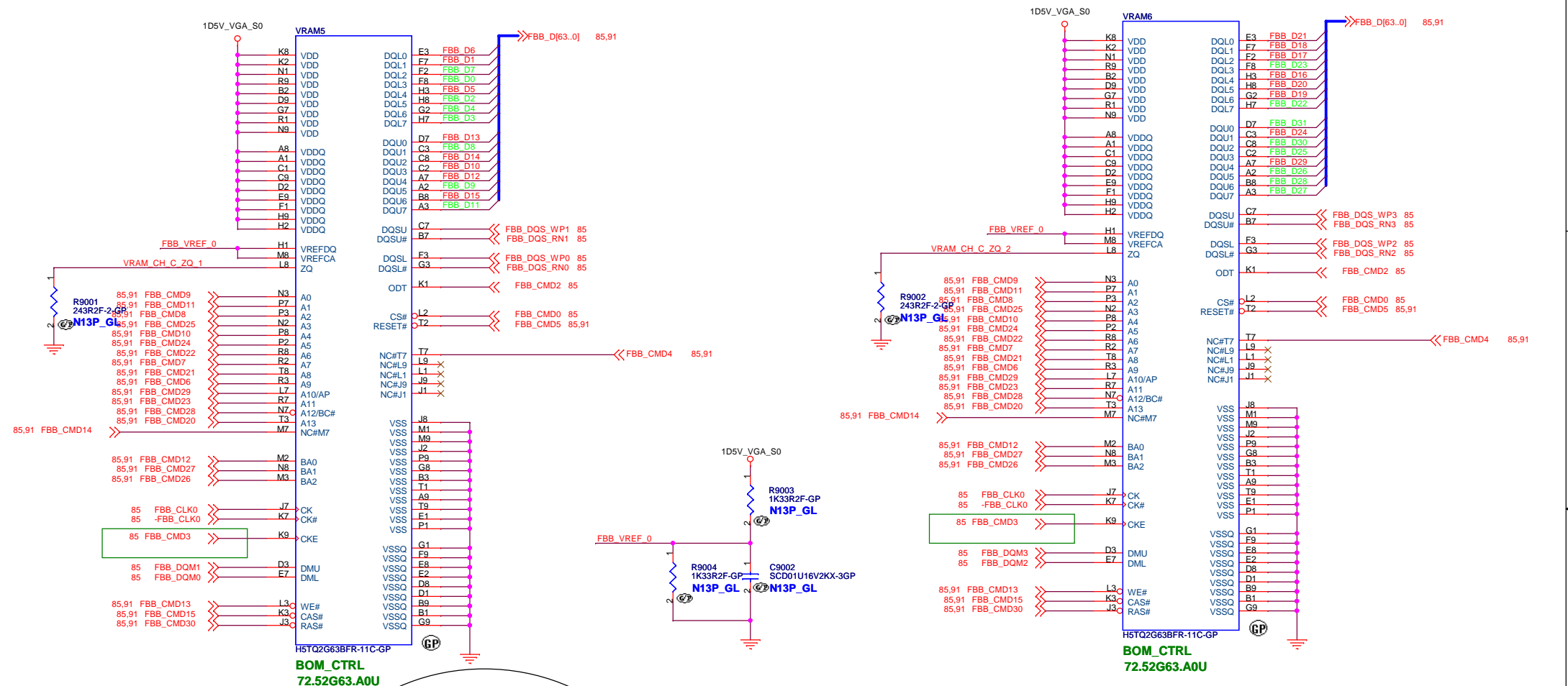


VRAM
SAMSUNG:
 K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
 K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
 H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
 H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT A
 JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM3,4 (2/4)
Size	Document Number G48/G58
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BOM_CTRL
72.52G63.A0U

BOM_CTRL
72.52G63.A0U

DG requires 4x0.1uF and 8x1.0uF per VRAM chip

FOR VRAM5

FOR VRAM6

CLOSE TO THE MEMORY

CLOSE TO THE MEMORY

VRAM

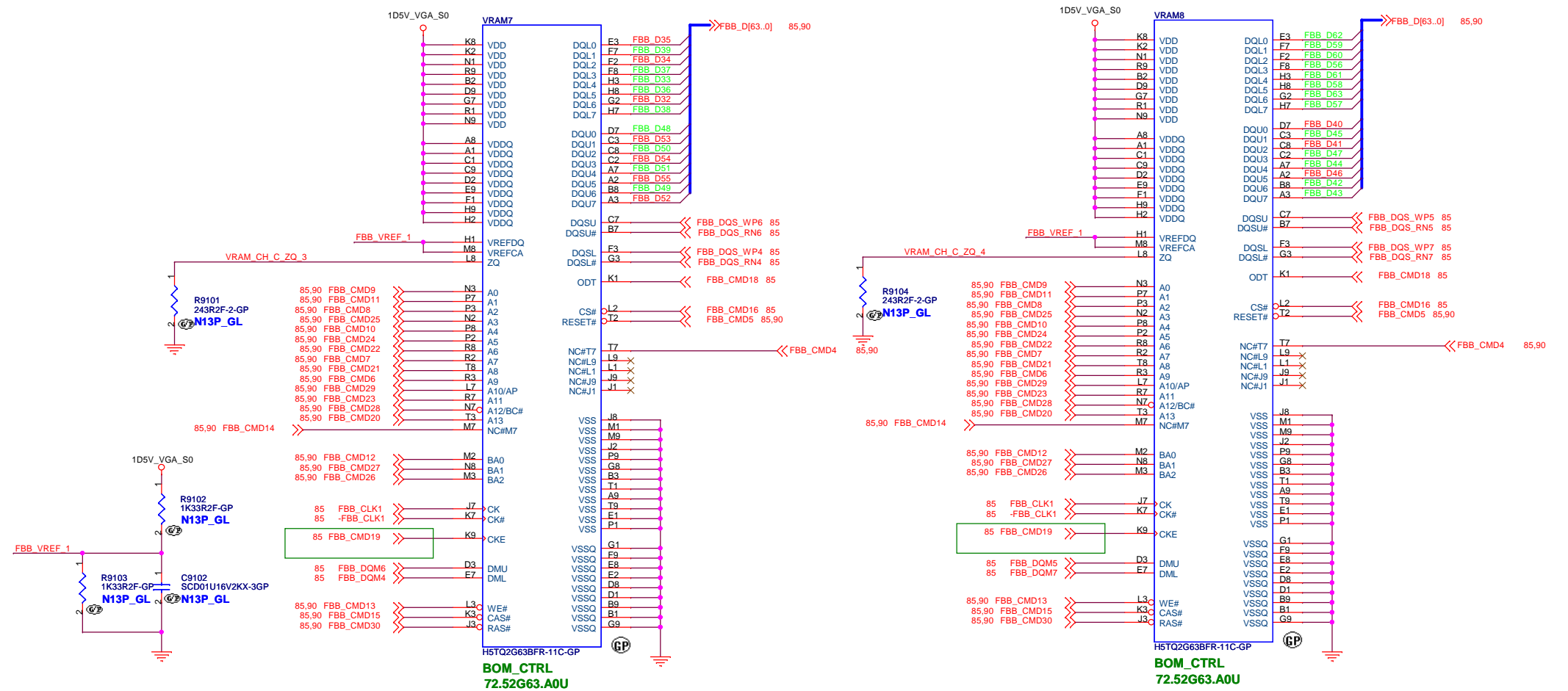
SAMSUNG:

K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:

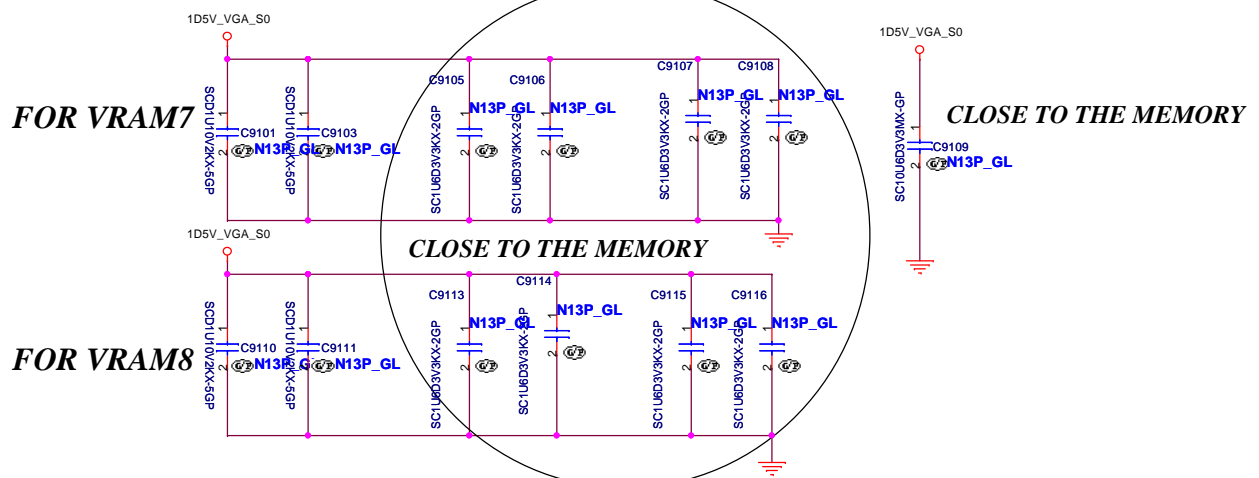
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

JV10-CS		VIDEO FRAME BUFFER PORT C	
緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	VRAM5,6 (3/4)		
Size	Document Number	G48/G58	Rev
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VRAM
SAMSUNG:
 K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHZ
 K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHZ

HYNIX:
 H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHZ
 H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHZ



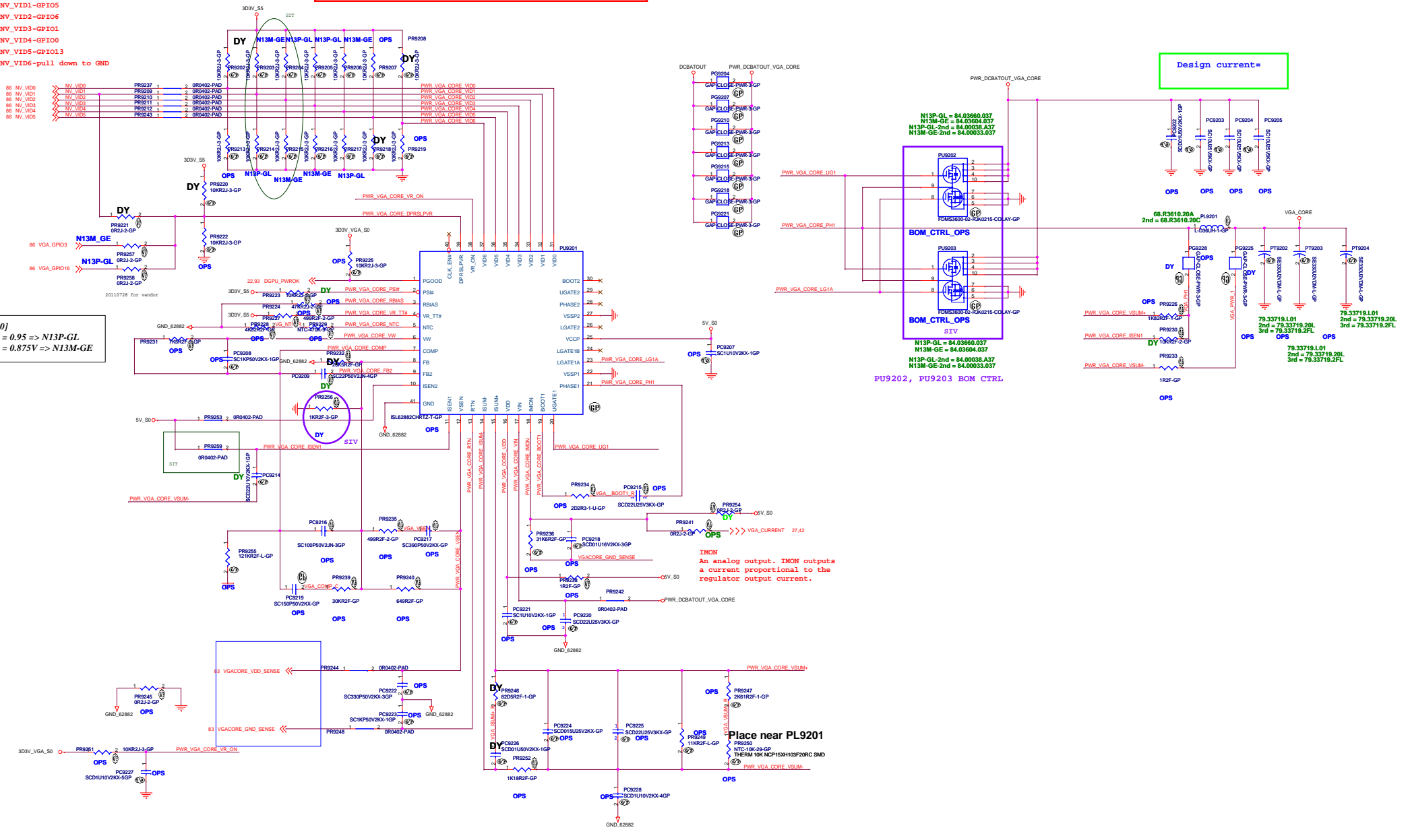
VIDEO FRAME BUFFER PORT C
 JV10-CS

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title		VRAM7,8 (4/4)	
Size	Document Number	G48/G58	
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SSID = PWR.Plane.Regulator_VGACORE

NV_VID0-GPI011
NV_VID1-GPI05
NV_VID2-GPI06
NV_VID3-GPI01
NV_VID4-GPI00
NV_VID5-GPI03
NV_VID6-pull down to GND

VID[5..0]
101100 = 0.95 => N13P-GL
110010 = 0.875V => N13M-GE



Design current=

N13P-GL = 84.03660.037
N13M-GE = 84.03664.037
N13P-GL-2nd = 84.00038.A37
N13M-GE-2nd = 84.00033.037

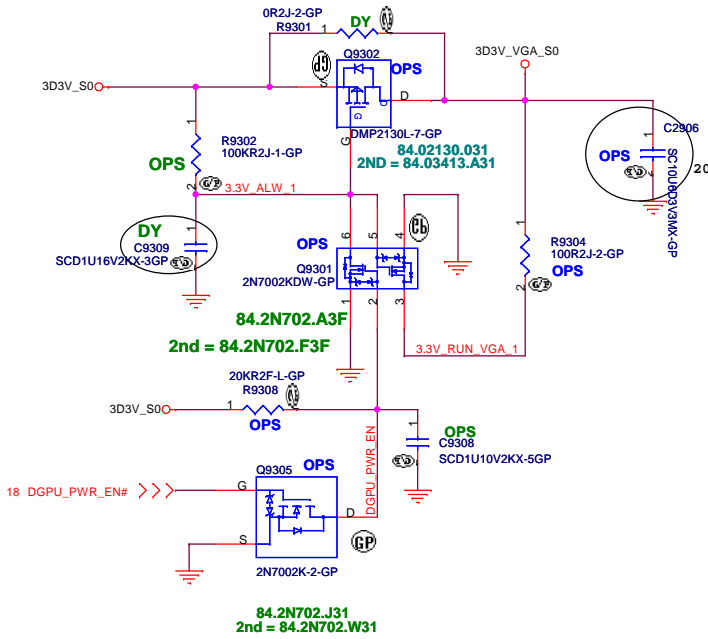
N13P-GL = 84.03660.037
N13M-GE = 84.03664.037
N13P-GL-2nd = 84.00038.A37
N13M-GE-2nd = 84.00033.037

PU9202, PU9203 BOM CTRL

IMON
An analog output. IMON outputs
a current proportional to the
regulator output current.

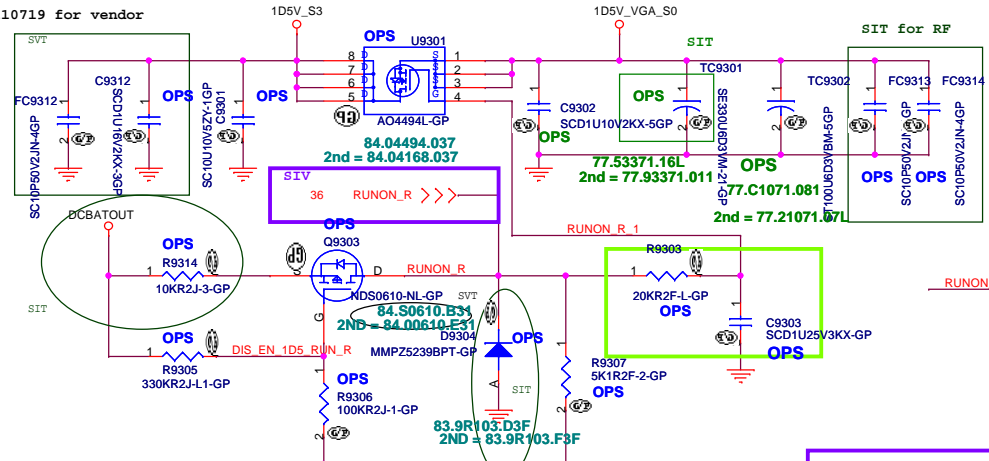
Place near PL9201

+3VS to 3.3V_DELAY Transfer

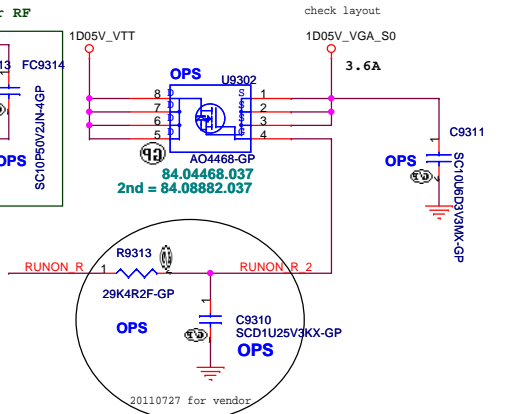


AO4468, SO-8
 Id=11.6A, Qg=9-12nC
 Rds(on)=17.4-22m ohm

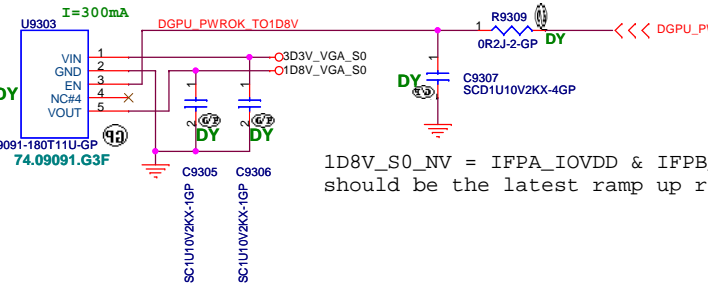
1D5V_VGA_S0



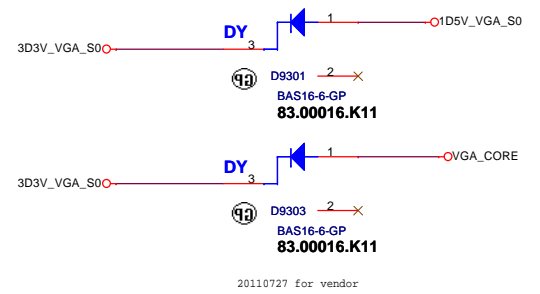
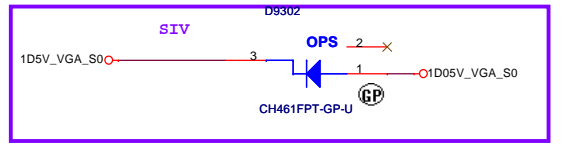
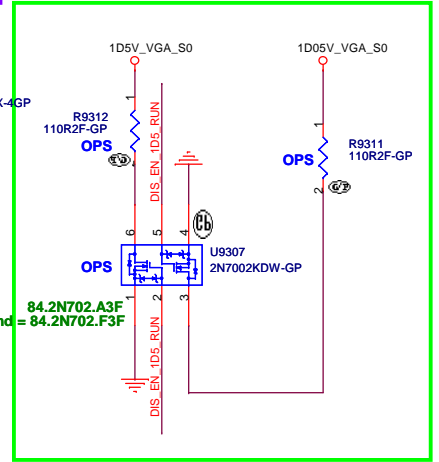
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



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DISCRETE VGA POWER	
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JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)SW GFX LCD(1/2)			
Size	Document Number	G48/G58	Rev SC
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(Blanking)

JV10-CS

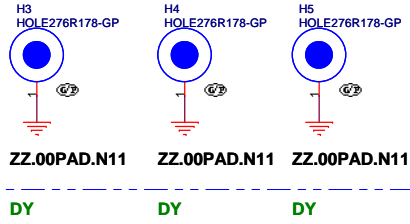
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)SW GFX CRT(2/2)			
Size	Document Number	G48/G58	Rev SC
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(Blanking)

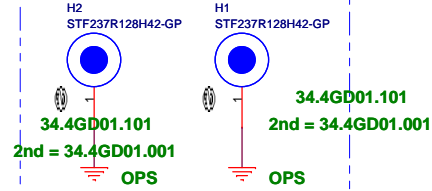
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)Touch panel CONN			
Size	Document Number	G48/G58	Rev SC
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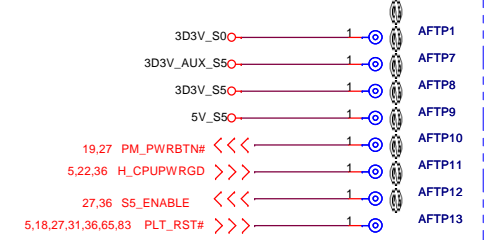
CPU Plate



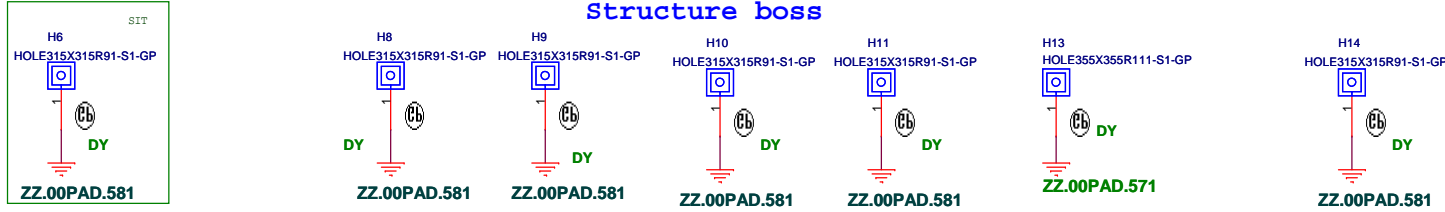
VGA Std-Off



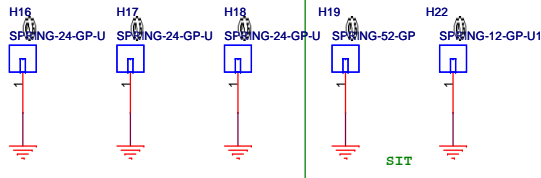
Check test point



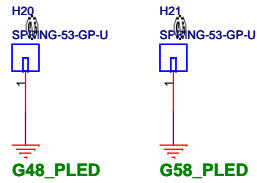
Structure boss



Spring

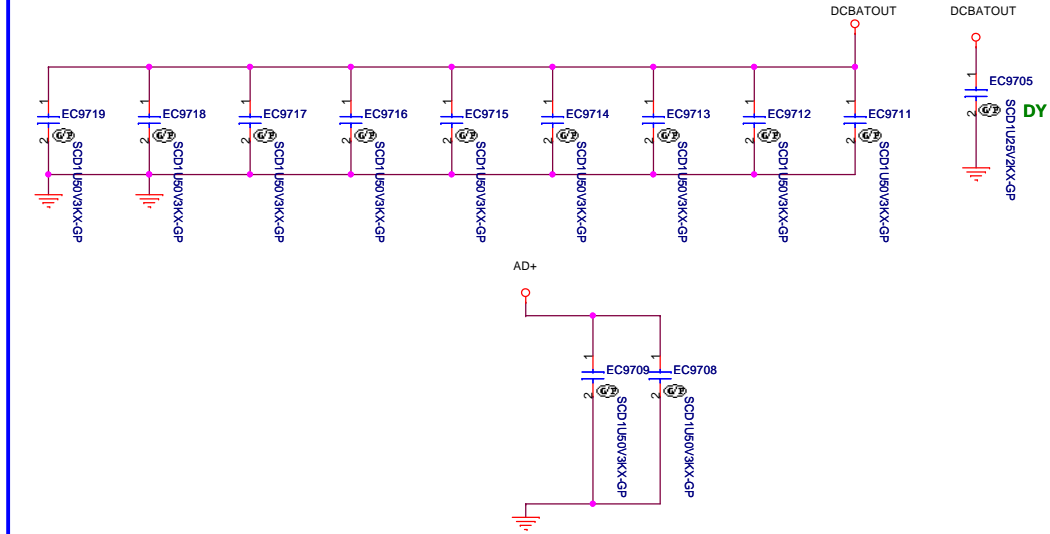


Washer



SIV

EMI Cap.



JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title UNUSED PARTS/EMI Capacitors

Size Document Number G48/G58 Rev SC

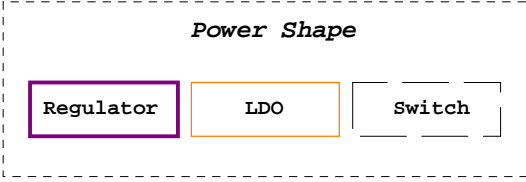
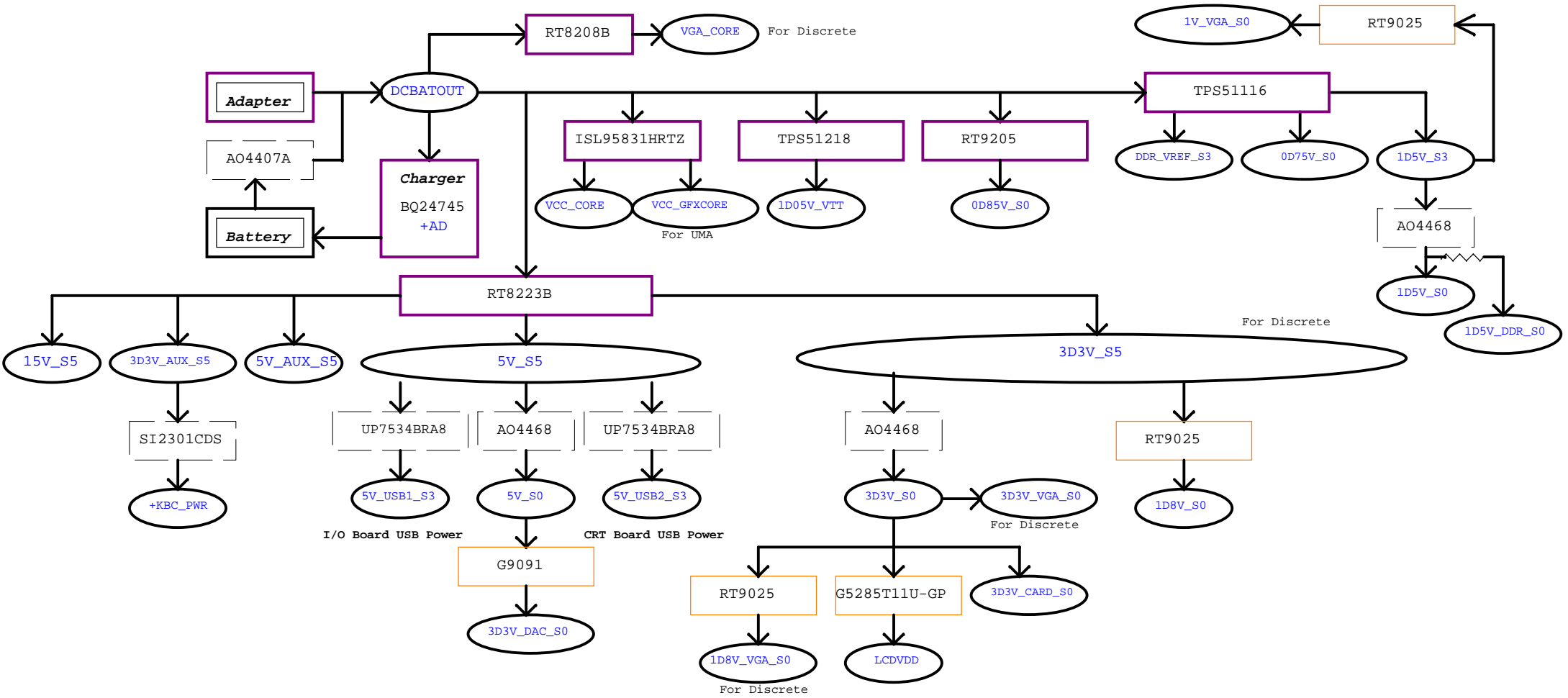
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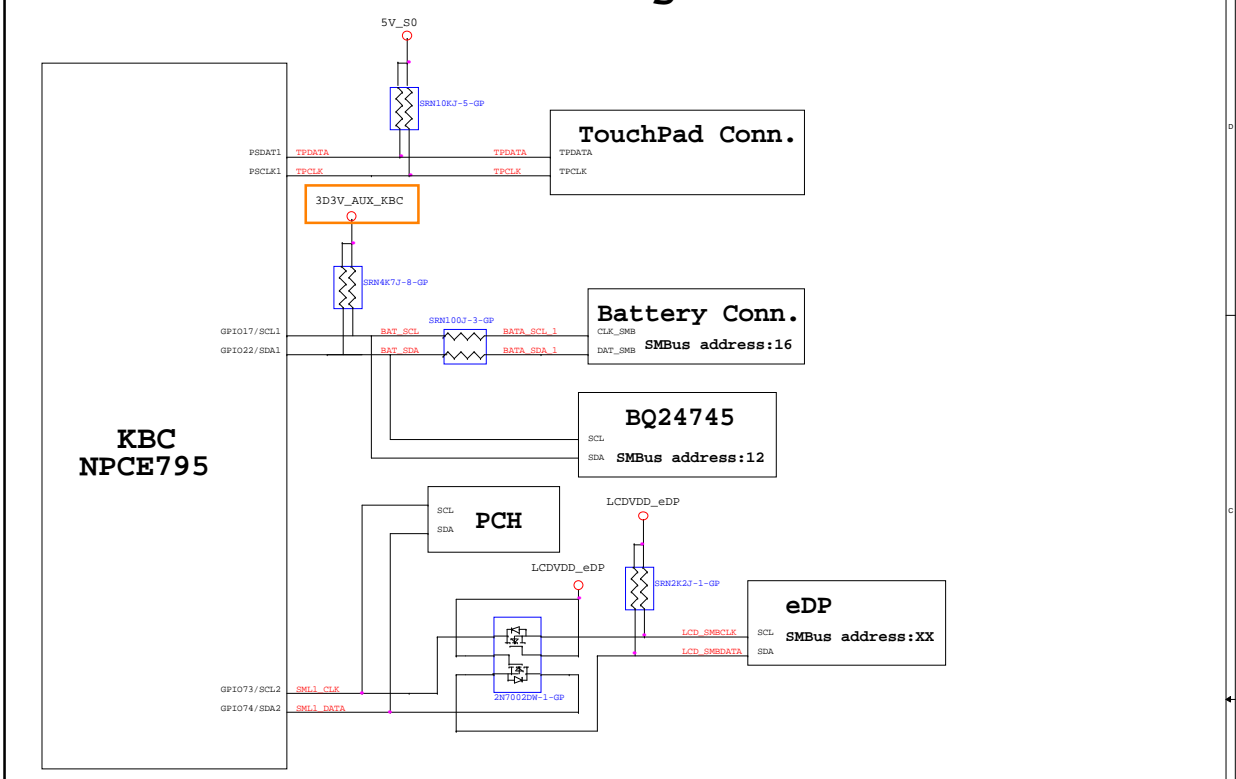
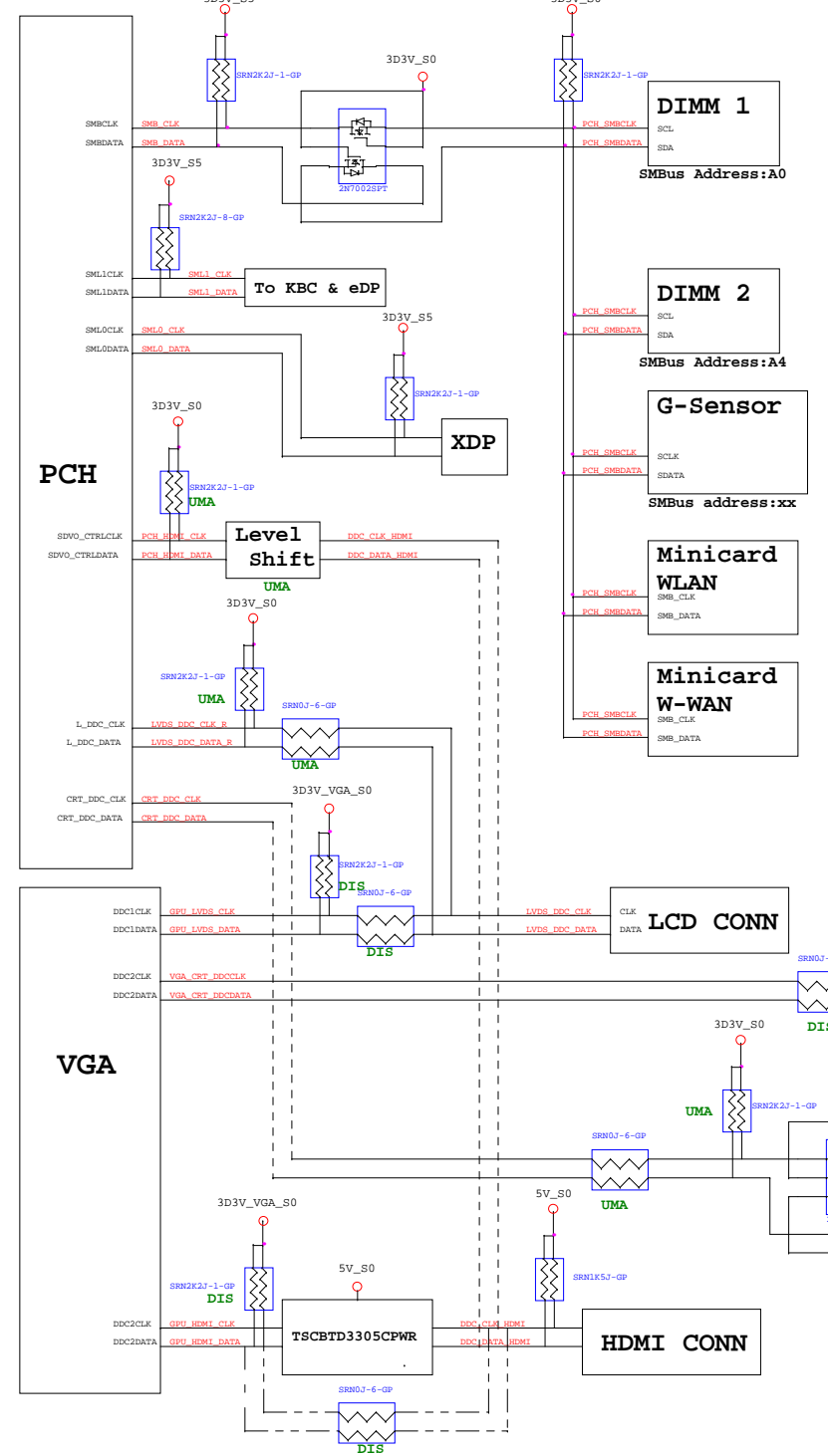
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Change-History			
Size	Document Number	G48/G58	Rev SC
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Not Update



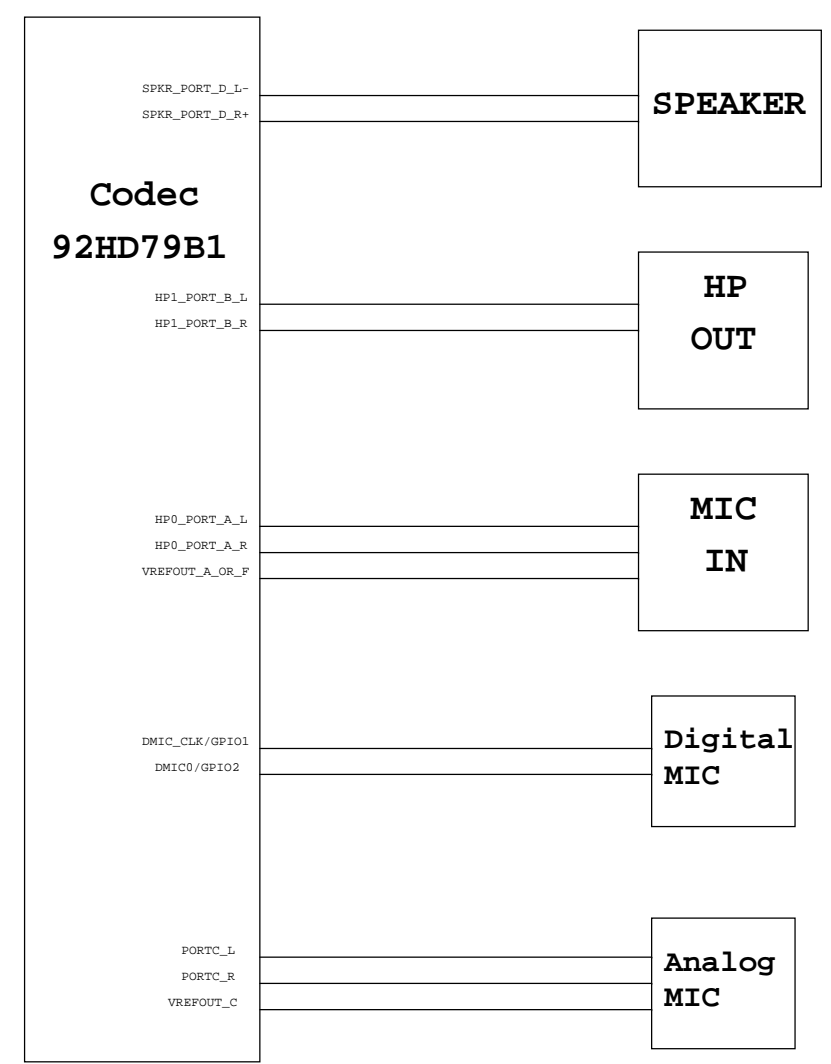
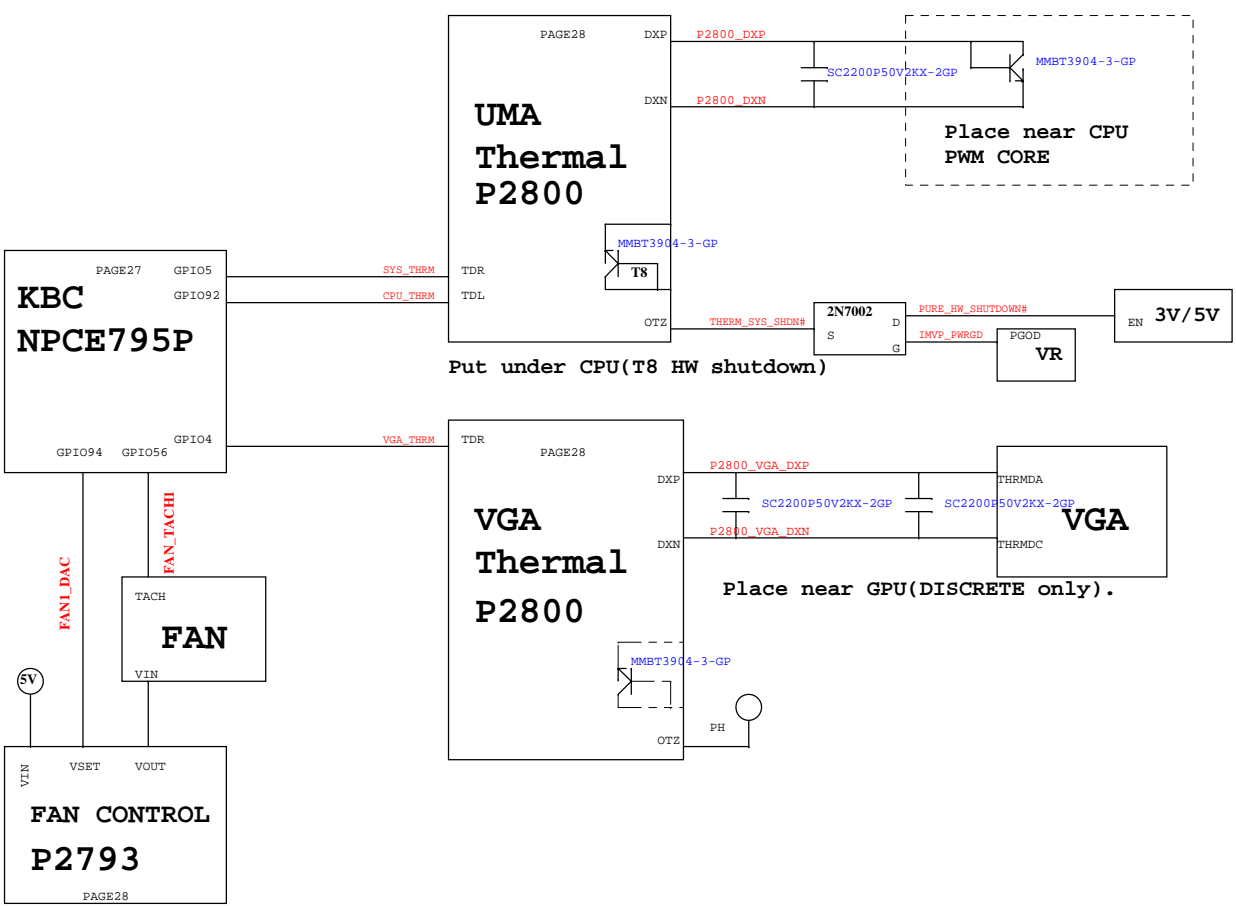
PCH SMBus Block Diagram

KBC SMBus Block Diagram



Thermal Block Diagram

Audio Block Diagram



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Title Change History			
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