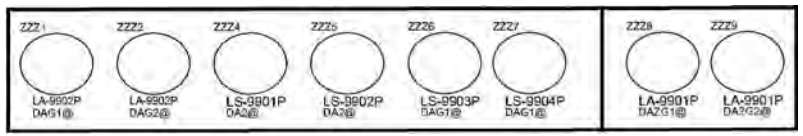

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G400S/G500S UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

LA-9902P

2013-05-06

REV:1.0

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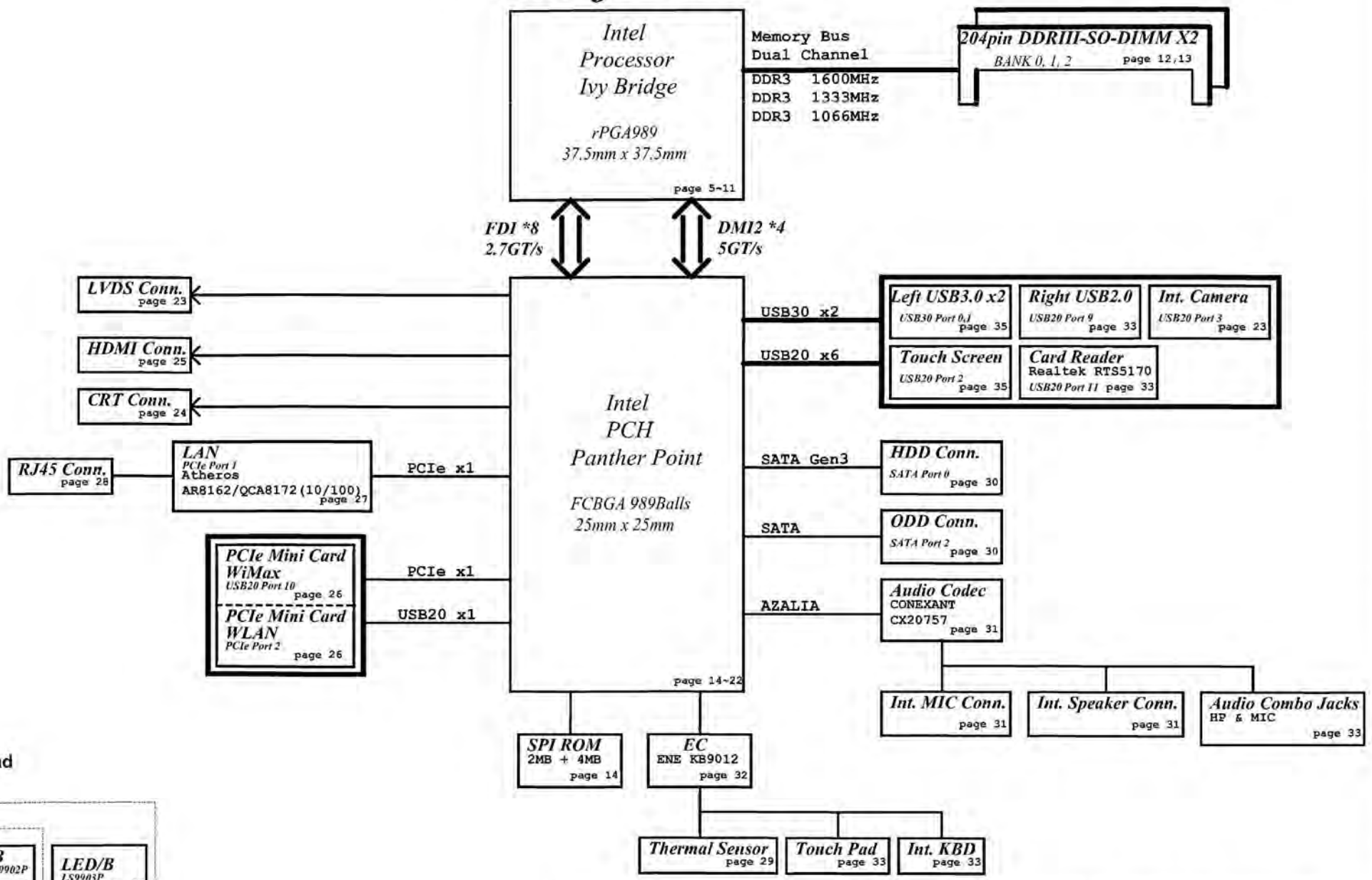
Chief River



Sub-borad

15"

14"

- Power/B LS9902P page 33
- LED/B LS9903P page 33
- IO/B LS9901P page 33
- ODD/B LS9904P page 30

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID table for AD channel

Vcc	3.3V					
Ra	100K +/- 1%					
Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001 100xb

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	USB Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB2.0)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
45 LEVEL	45@
Connector	ME@
For VILG2 (14")	14@
For VILG1 (15")	15@
HDMI	HDMI@
Camera	CMOS@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
10/100 LAN(AR8162L)	8162@
10/100 LAN(QCA8172)	8172@
Green clock(DIS sku)	GCLK304@
Green clock(UMA sku)	GCLK244@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Touch Screen SKU	TS@
Optimus SKU	OPT@
UMA SKU	UMA@
PCH(NM70 sku)	NM70@
PCH(HM70 sku)	HM70@
PCH(HM76 sku)	HM76@
VRAM(1000MHz)	1000M@
VRAM(900MHz)	900M@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	V +3VS_VGA	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS_VGA	X	V +3VS	X	X	V +3VS	X

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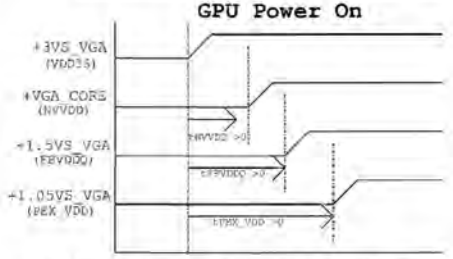
N14x GPIO Pin Definition Table

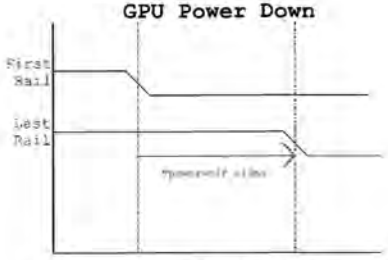
Pin Name	Normal Function	I/O	Functional Description	Default PU/PD
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID:Strap to boot FBVDD/Q
GPIO2~4	Non-support for LCD	O	Panel	100k PD
GPIO5	Reserve			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100k PD
GPIO8	OVERT	IO	Active Low Thermal Catastrophic Over Temperature	100k PU
GPIO9	ALERT	IO	Active Low Thermal Alert	100k PU
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100k PD
GPIO11	PWM_VID	O	GPU Core VDD PWM control supply overdraw input	
GPIO12	PWR_LEVEL	I	AC power detact or control signal	100k PU
GPIO13	PSI	O	Phase Shedding	PSI:100k PU to enable two phase
GPIO14~19	Non-support for HDA	I	Hot Plug	
GPIO20~21	Reserve			

GPU Power On



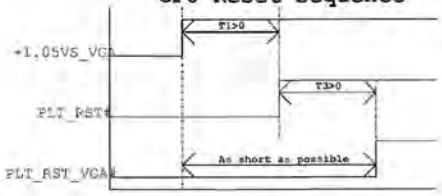
1. All power rail ramp up time should be larger than 400s
2. The total time for all rails to run should be within 85ms
3. A power rail has to ramp up 90% before the next power rail in sequence can start ramping up
4. No signal should be applied to the GPU before the power rail are fully ramped.

GPU Power Down

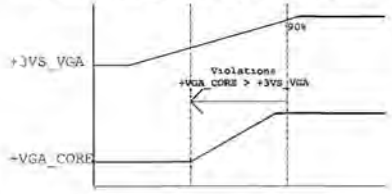


1.All GPU power rails should be turned off within 10ms

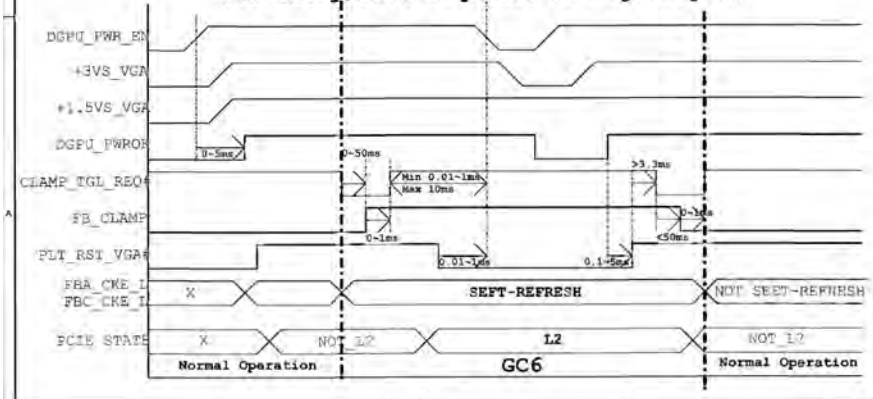
GPU Reset Sequence



Power sequencing violations



GC6 Entry/Exit Sequence Timing Diagram



For N14P-GV2 strap table

X76

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M* 16* 4 1GB	Hynix H5TQ2G63DFR-N0C	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 35K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PU 5K

For N14P-GS strap table

X75

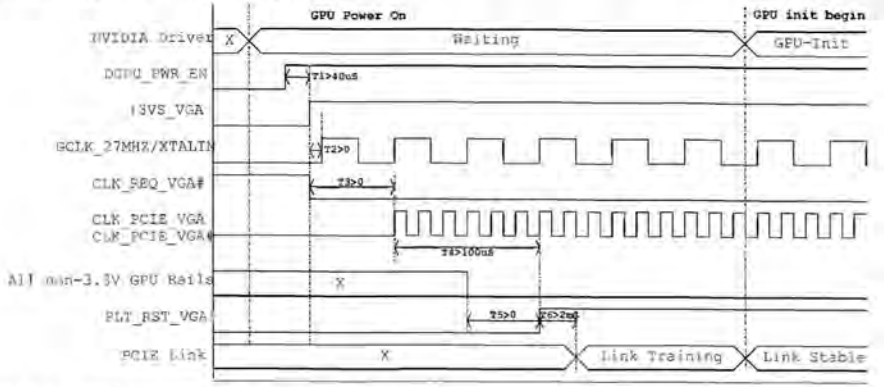
GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M* 16* 8 2GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M* 16* 8 2GB	Hynix H5TQ2G63DFR-N0C	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 35K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M* 16* 8 4GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PD 15K

For N14M-GE strap table

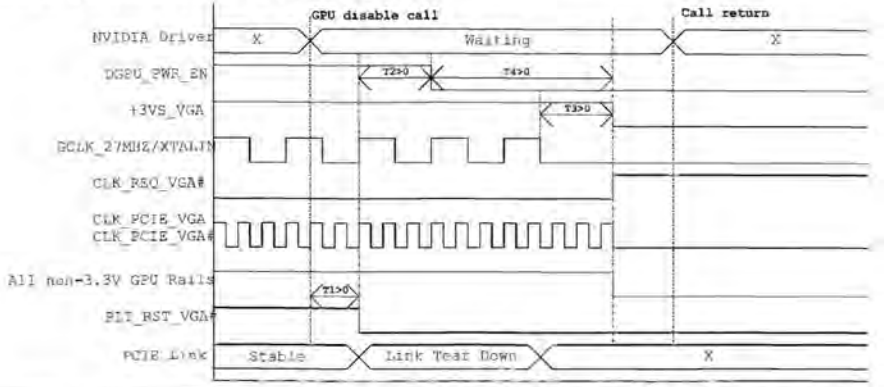
X76

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M* 16* 4 1GB	Samsung K4W2G1646E-BC1A	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Micron MT41J128M16JT-093G:K	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M* 16* 4 1GB	Hynix H5TQ2G63DFR-N0C	R PD 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Samsung K4W4G1646B-HC11	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M* 16* 4 2GB	Micron MT41K256M16HA-107G:E	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

Optimus Typical Power-Up Sequence



Optimus Typical Power-Down Sequence



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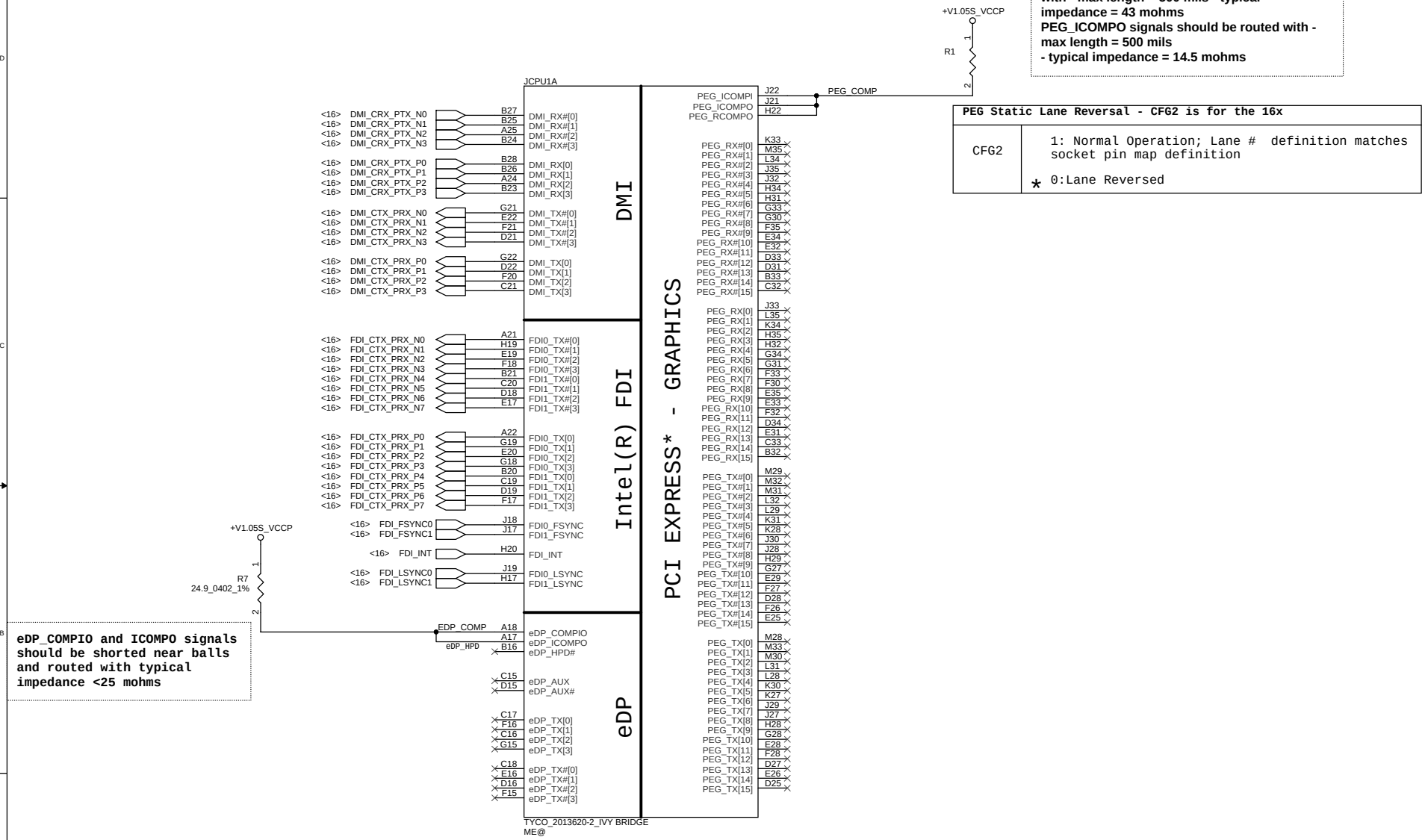

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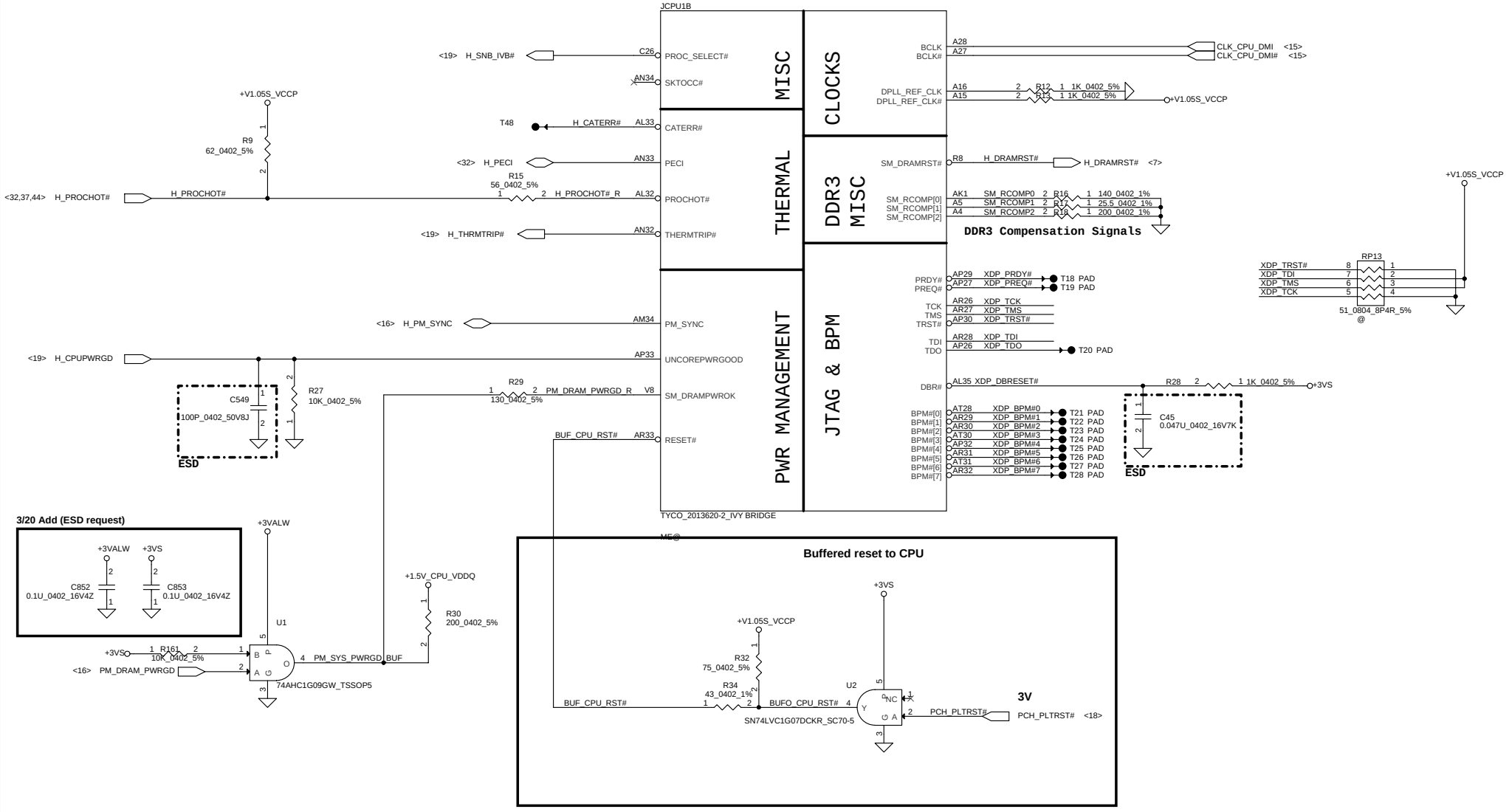

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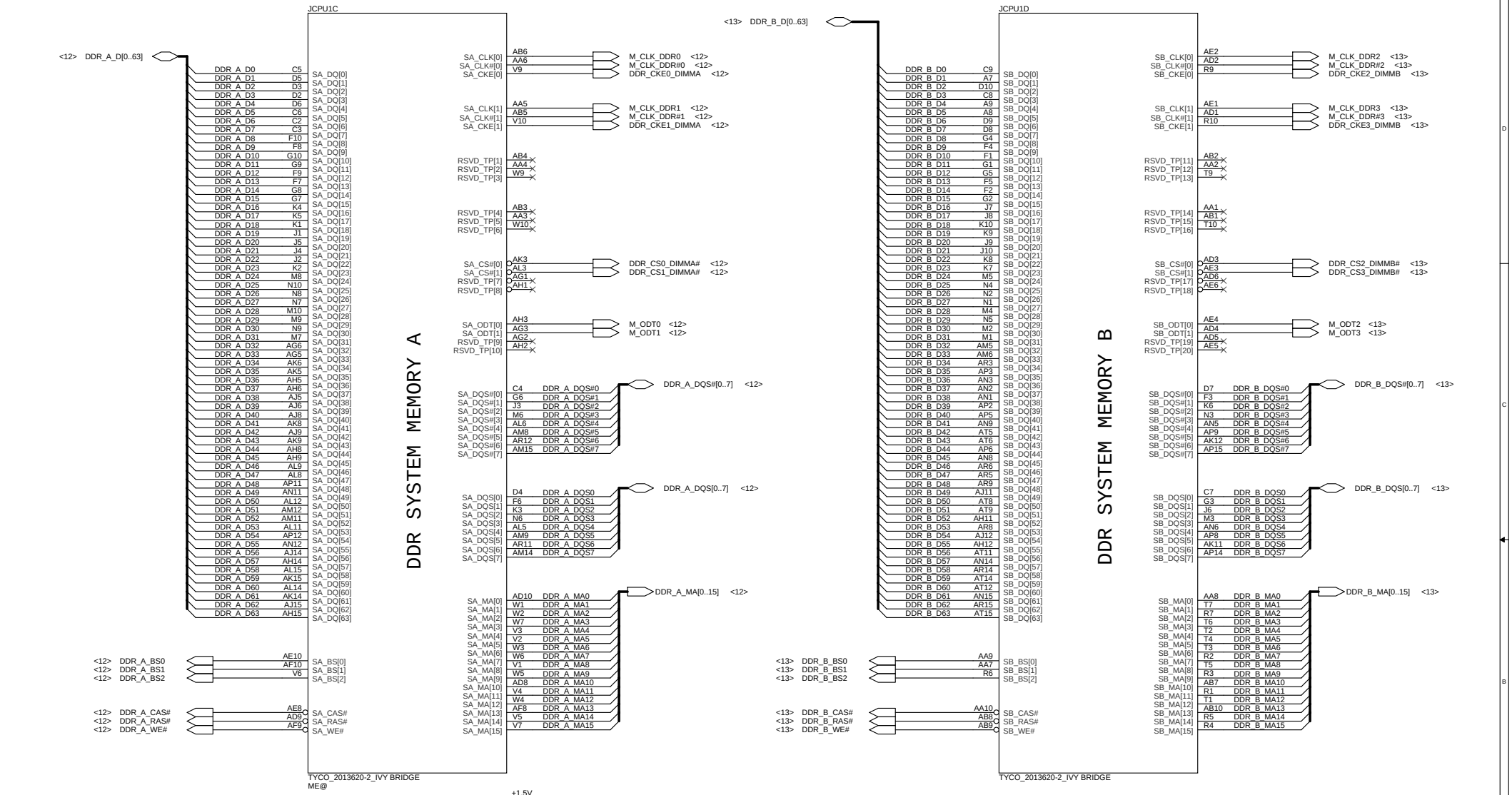

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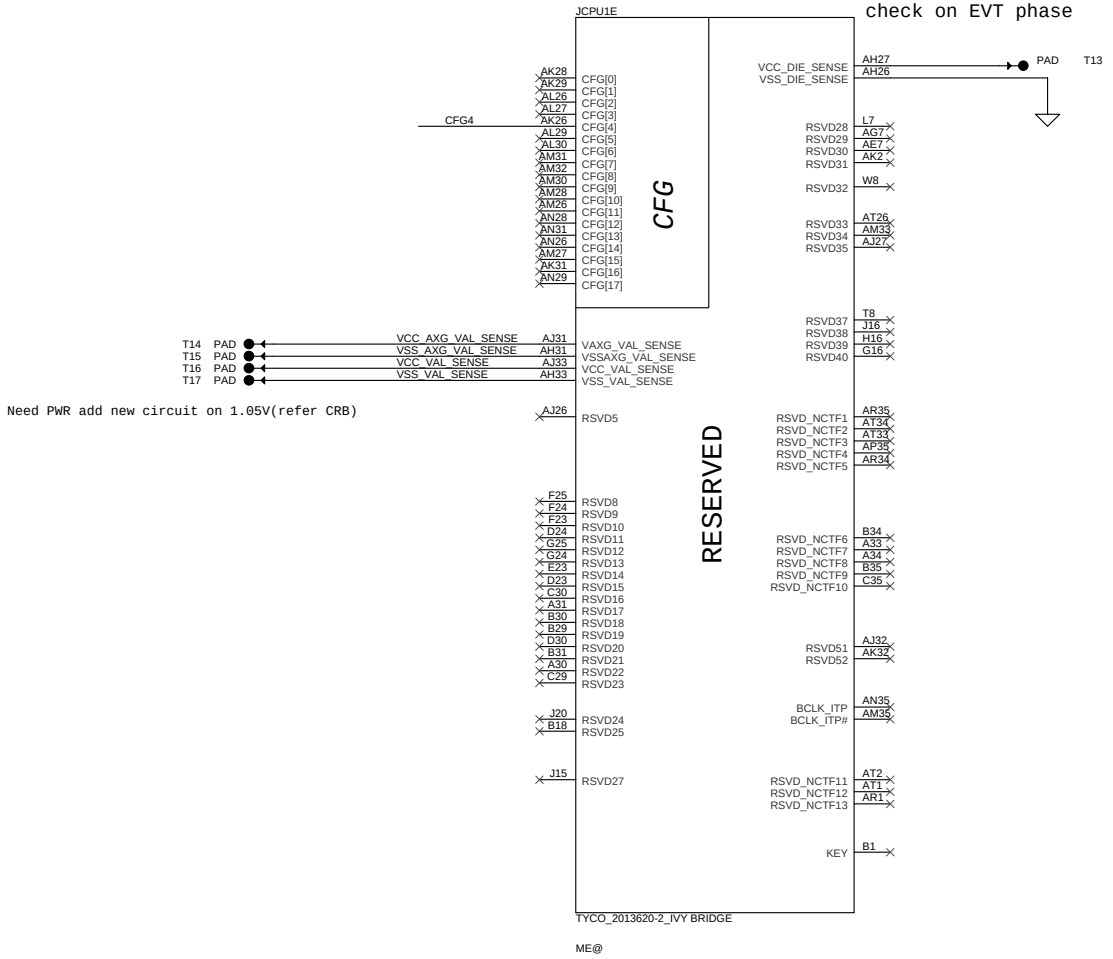
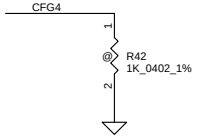
CFG Straps for Processor

Interl request AH26 short GND
check on EVT phase



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

SVID

+V1.05S_VCCP

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT#	AJ29	H_CPU_SVIDALRT#	1 R47 2 43_0402_5%	VR_SVID_ALRT# <44>
VIDSCLK	AJ30			VR_SVID_CLK <44>
VIDSOUT	AJ28			VR_SVID_DAT <44>

R50 2 1 130_0402_5% +V1.05S_VCCP

0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51 100_0402_1%

VCC_SENSE	AJ35		VCCSENSE <44>
VSS_SENSE	AJ34		VSSSENSE <44>

R54 100_0402_1%

VCCIO_SENSE	B10		VCCIO_SENSE <43>
VSS_SENSE_VCCIO	A10	VSSIO_SENSE_L 1 R74 2 10_0402_1%	

R74 & R79 put together

VSSIO_SENSE_L <43>

+V1.05S_VCCP

R79 2 1 10_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

ME@

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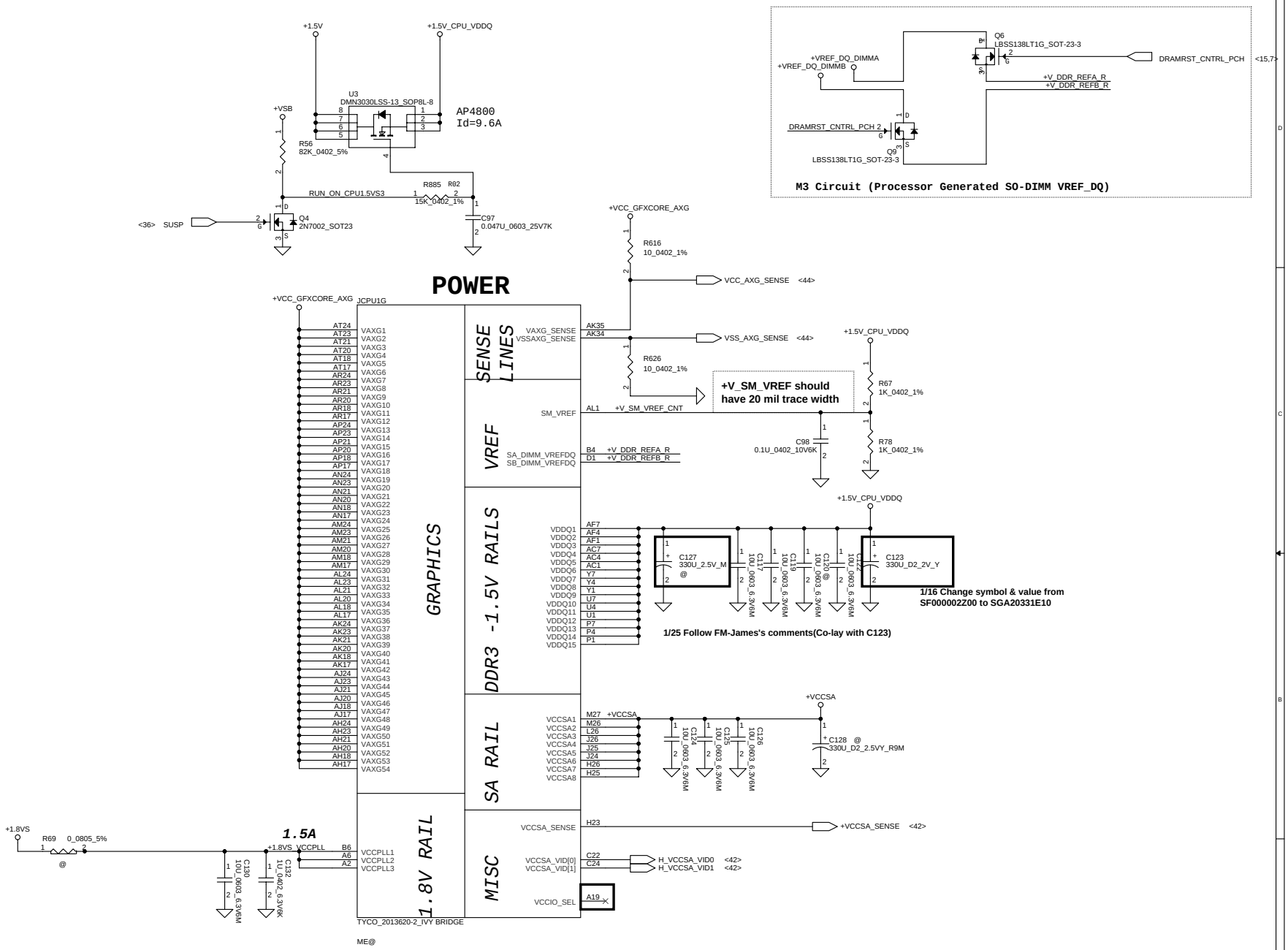

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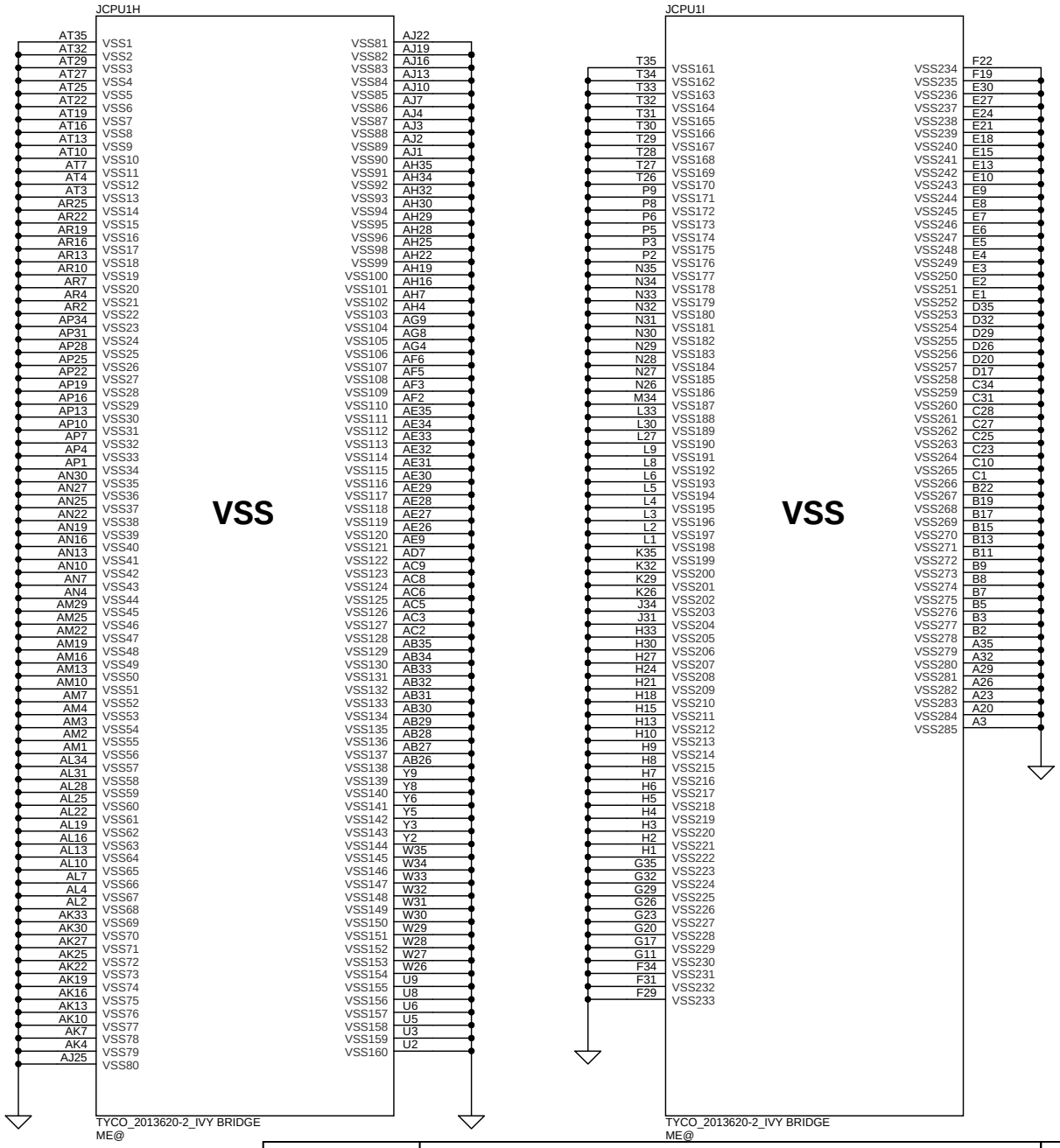

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DDR3 SO-DIMM A

JDIMM1

	+VREF_DQ_DIMMA	1	VREF_DQ	VSS1	2		
DDR_A_D0		3	VSS2	DQ4	4	DDR_A_D4	
DDR_A_D1		5	DQ0	DQ5	6	DDR_A_D5	
		7	DQ1	VSS3	8		
		9	VSS4	DQS#0	10	DDR_A_DQS#0	
		11	DM0	DQS0	12	DDR_A_DQS0	
DDR_A_D2		13	VSS5	DQ6	14	DDR_A_D6	
DDR_A_D3		15	DQ2	DQ7	16	DDR_A_D7	
		17	DQ3	VSS6	18		
DDR_A_D8		19	VSS7	DQ12	20	DDR_A_D12	
DDR_A_D9		21	DQ8	DQ13	22	DDR_A_D13	
		23	DQ9	VSS7	24		
DDR_A_DQS#1		25	VSS9	DM1	26		
DDR_A_DQS1		27	DQS#1	RESET#	28	DDR3_DRAMRST#	DDR3_DRAMRST# <13,7>
		29	DQS1	VSS12	30		
DDR_A_D10		31	VSS11	DQ14	32	DDR_A_D14	
DDR_A_D11		33	DQ10	DQ15	34	DDR_A_D15	
		35	DQ11	VSS13	36		
DDR_A_D16		37	VSS13	DQ20	38	DDR_A_D20	
DDR_A_D17		39	DQ16	DQ21	40	DDR_A_D21	
		41	DQ17	VSS15	42		
DDR_A_DQS#2		43	VSS15	DM2	44		
DDR_A_DQS2		45	DQS#2	VSS17	46		
		47	DQS2	DQ22	48	DDR_A_D22	
DDR_A_D18		49	VSS18	DQ23	50	DDR_A_D23	
DDR_A_D19		51	DQ18	VSS19	52		
		53	DQ19	DQ28	54	DDR_A_D28	
DDR_A_D24		55	VSS20	DQ29	56	DDR_A_D29	
DDR_A_D25		57	DQ24	VSS21	58		
		59	DQ25	DQS#3	60	DDR_A_DQS#3	
		61	VSS22	DQS3	62	DDR_A_DQS3	
DDR_A_D26		63	DM3	VSS24	64		
DDR_A_D27		65	VSS23	DQ30	66	DDR_A_D30	
		67	DQ26	DQ31	68	DDR_A_D31	
		69	DQ27	VSS26	70		
		71	VSS25		72		
<7> DDR_CKE0_DIMMA	DDR_CKE0_DIMMA	73	CKE0	CKE1	74	DDR_CKE1_DIMMA	DDR_CKE1_DIMMA <7>
		75	VDD1	VDD2	76		
<7> DDR_A_BS2	DDR_A_BS2	77	NC1	A15	78	DDR_A_MA15	
		79	BA2	A14	80	DDR_A_MA14	
DDR_A_MA12		81	VDD3	VDD4	82		
DDR_A_MA9		83	A12/BC#	A11	84	DDR_A_MA11	
		85	A9	A7	86	DDR_A_MA7	
DDR_A_MA8		87	VDD5	VDD6	88		
DDR_A_MA5		89	A8	A6	90	DDR_A_MA6	
		91	A5	A4	92	DDR_A_MA4	
DDR_A_MA3		93	VDD7	VDD8	94		
DDR_A_MA1		95	A3	A2	96	DDR_A_MA2	
		97	A1	A0	98	DDR_A_MA0	
		99	VDD9	VDD10	100		
<7> M_CLK_DDR0	M_CLK_DDR0	101	CK0	CK1	102	M_CLK_DDR1	M_CLK_DDR1 <7>
<7> M_CLK_DDR#0	M_CLK_DDR#0	103	CK0#	CK1#	104	M_CLK_DDR#1	M_CLK_DDR#1 <7>
		105	VDD11	VDD12	106		
DDR_A_MA10		107	A10/AP	BA1	108	DDR_A_BS1	DDR_A_BS1 <7>
<7> DDR_A_BS0	DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS#	DDR_A_RAS# <7>
		111	VDD13	VDD14	112		
<7> DDR_A_WE#	DDR_A_WE#	113	WE#	S0#	114	DDR_CS0_DIMMA#	DDR_CS0_DIMMA# <7>
<7> DDR_A_CAS#	DDR_A_CAS#	115	CAS#	ODT0	116	M_ODT0	M_ODT0 <7>
		117	VDD15	VDD16	118		
DDR_A_MA13		119	A13	ODT1	120	M_ODT1	M_ODT1 <7>
<7> DDR_CS1_DIMMA#	DDR_CS1_DIMMA#	121	S1#	NC2	122		
		123	VDD17	VDD18	124		
		125	NCTEST	VREF_CA	126		+VREF_CA
		127	VSS27	VSS28	128		
DDR_A_D32		129	DQ32	DQ36	130	DDR_A_D36	
DDR_A_D33		131	DQ33	DQ37	132	DDR_A_D37	
		133	VSS29	VSS30	134		
DDR_A_DQS#4		135	DQS#4	DM4	136		
DDR_A_DQS4		137	DQS4	VSS31	138		
		139	VSS32	DQ38	140	DDR_A_D38	
DDR_A_D34		141	DQ34	DQ39	142	DDR_A_D39	
DDR_A_D35		143	DQ35	VSS33	144		
		145	VSS34	DQ44	146	DDR_A_D44	
DDR_A_D40		147	DQ40	DQ45	148	DDR_A_D45	
DDR_A_D41		149	DQ41	VSS35	150		
		151	VSS36	DQS5	152	DDR_A_DQS#5	
		153	DM5	VSS38	154	DDR_A_DQS5	
DDR_A_D42		155	VSS37	DQ46	156		
DDR_A_D43		157	DQ42	DQ47	158	DDR_A_D46	
		159	DQ43	VSS39	160	DDR_A_D47	
DDR_A_D48		161	VSS39	DQ52	162		
DDR_A_D49		163	DQ48	DQ53	164	DDR_A_D52	
		165	DQ49	VSS42	166	DDR_A_D53	
DDR_A_DQS#6		167	VSS41	DM6	168		
DDR_A_DQS6		169	DQS#6	VSS43	170		
		171	DQS6	DQ54	172		
DDR_A_D50		173	VSS44	DQ55	174	DDR_A_D54	
DDR_A_D51		175	DQ50	VSS45	176	DDR_A_D55	
		177	DQ51	DQ60	178		
DDR_A_D56		179	VSS46	DQ61	180	DDR_A_D60	
DDR_A_D57		181	DQ56	VSS47	182	DDR_A_D61	
		183	DQ57	DQS#7	184		
		185	VSS48	DQS7	186	DDR_A_DQS#7	
DDR_A_D58		187	DM7	VSS50	188	DDR_A_DQS7	
DDR_A_D59		189	VSS49	DQ62	190		
		191	DQ58	DQ63	192	DDR_A_D62	
		193	DQ59	VSS52	194	DDR_A_D63	
		195	VSS51	EVENT#	196		
		197	SA0	SDA	198		
		199	VDDSPD	SCL	200	SMB_DATA_S3	SMB_DATA_S3 <13,15,26>
		201	SA1	VTT2	202	SMB_CLK_S3	SMB_CLK_S3 <13,15,26>
		203	VTT1		204		+0.75VS
		205	G1	G2	206		

LCN_DAN06-K4806-0103

ME@

<7> DDR_A_D[0..63]

<7> DDR_A_DQS[0..7]

<7> DDR_A_DQS#[0..7]

<7> DDR_A_MA[0..15]

RP15: +VREF_DQ_DIMMA, +VREF_DQ_DIMMB, +1.5V — 1K_0804_8P4R_1%

RP16: +VREF_CA, +VREF_CB, +1.5V — 1K_0804_8P4R_1%

C133 0.1U_0402_10V6K

C135 0.1U_0402_10V6K

C156 0.1U_0402_10V6K

R136 0_0402_5% +3VS

+3V_DIMM

+VREF_CA

+0.75VS

0.65A@0.75V

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note: Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

+1.5V

C139 10U_0603_6.3V6M
C140 10U_0603_6.3V6M
C141 10U_0603_6.3V6M
C142 10U_0603_6.3V6M
C143 10U_0603_6.3V6M
C144 10U_0603_6.3V6M
C145 @ 0.1U_0402_10V6K
C146 0.1U_0402_10V6K
C147 0.1U_0402_10V6K
C148 0.1U_0402_10V6K
C149 @ 220U_6.3V_M

Layout Note: Place near DIMM

+0.75VS

C150 1U_0402_6.3V6K
C152 1U_0402_6.3V6K

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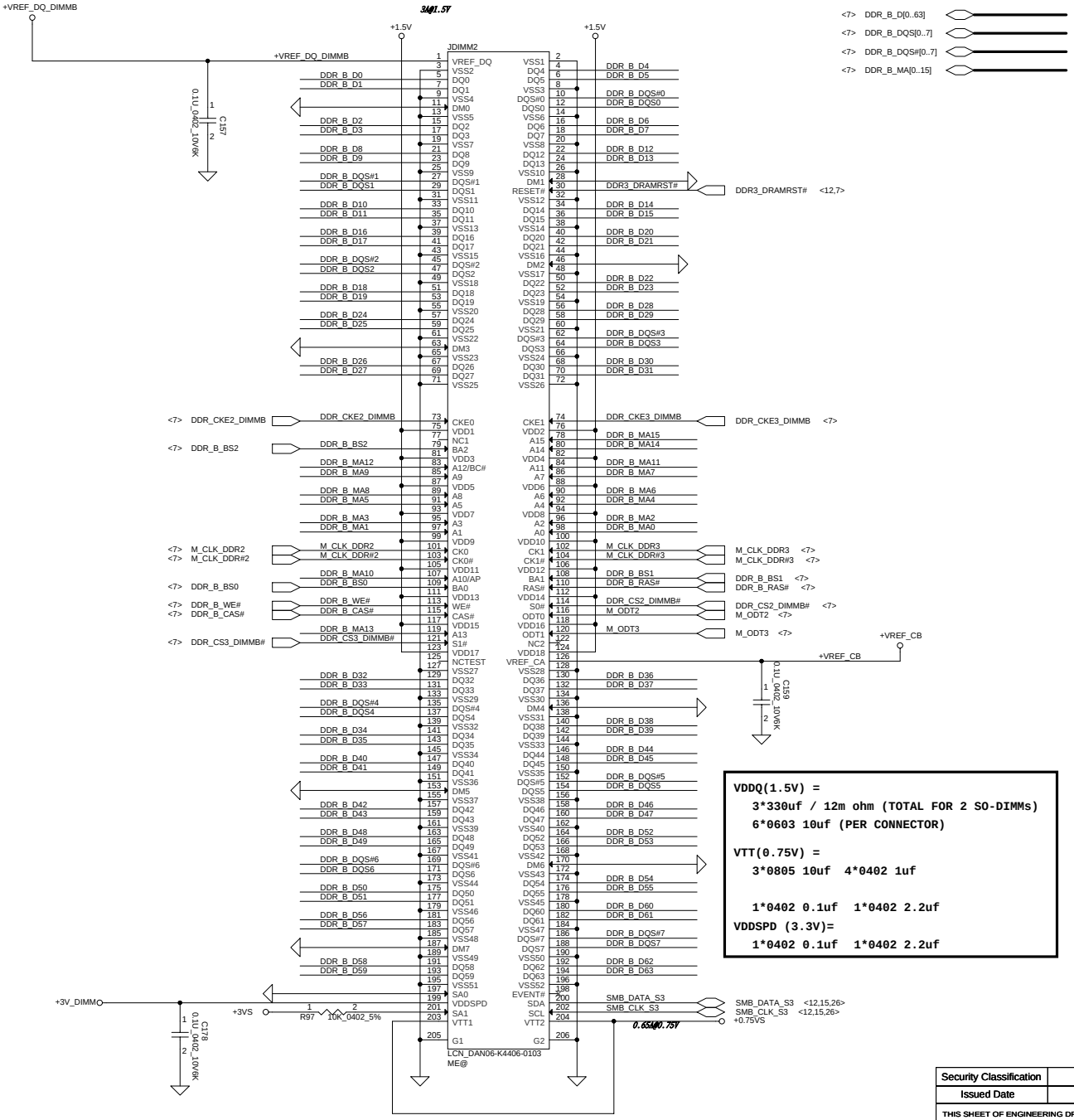


VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

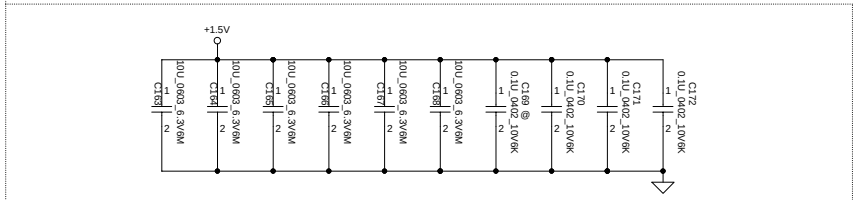
VTT(0.75V) =
3*0805 10uf 4*0402 1uf

1*0402 0.1uf 1*0402 2.2uf

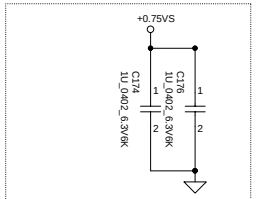
VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4



Layout Note:
Place near DIMM



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W=20mils +RTCVCC — R99 1K_0402_5% — W=20mils +RTCBATT; C179 1U_0603_10V4Z

+RTCVCC — R101 1M_0402_5% SM_INTRUDER# — R102 330K_0402_5% PCH_INTVRMEN

INTVRMEN

* H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS — R105 @ 1K_0402_5% HDA_SPKR

HIGH= Enable (No Reboot)
* LOW= Disable (Default)

+3V_PCH — R106 @ 1K_0402_5% ME_FLASH

* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH — R108 1K_0402_5% HDA_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high(For mobile only)
* 1.8V when sampled low(For Desktop only)
Needs to be pulled High for Chief River platfrom

<31> HDA_BITCLK_AUDIO — RP12 33_0804_8P4R_5% — HDA_BIT_CLK
<31> HDA_SYNC_AUDIO — HDA_SYNC_R
<31> HDA_RST_AUDIO# — HDA_RST#
<31> HDA_SDOUT_AUDIO — ME_FLASH

For EMI

+5VS — Q10 LBSS138LT1G_SOT-23-3 — HDA_SYNC
R878 1M_0402_5%; R175 0_0402_5%

check with vender
Del Q10 check with codec
VDDIO using 3VALW

DPDG1.1

PCH_RTCX1 — R98 10M_0402_5% — PCH_RTCX2; NOGCLK@; Y1 32.768KHZ_12.5PF_CM31532768DZFT
C180 12P_0402_50V8J NOGCLK@; C181 12P_0402_50V8J NOGCLK@

R187 0_0402_5% @ GCLK_32K — GCLK_32K <34>

CMOS

+RTCVCC — C183 1U_0603_10V4Z — R103 20K_0402_5% — R100 20K_0402_5% — C182 1U_0603_10V4Z
CLRP2 SHORT PADS; CLRP3 SHORT PADS

U4A

PCH_RTCX1	A20	RTCX1	RTC
PCH_RTCX2	C20	RTCX2	
PCH_RTCRST#	D20	RTCRST#	
PCH_SRTCRST#	G22	SRTCRST#	
SM_INTRUDER#	K22	INTRUDER#	
PCH_INTVRMEN	C17	INTVRMEN	
HDA_BIT_CLK	N34	HDA_BCLK	IHDA
HDA_SYNC	L34	HDA_SYNC	
<31> HDA_SPKR	T10	SPKR	
HDA_RST#	K34	HDA_RST#	
<31> HDA_SDIN0	E34	HDA_SDIN0	
	G34	HDA_SDIN1	
	C34	HDA_SDIN2	
	A34	HDA_SDIN3	
<32> ME_FLASH	A36	HDA_SDO	
	C36	HDA_DOCK_EN# / GPIO33	
	N32	HDA_DOCK_RST# / GPIO13	
T41 PAD	PCH_JTAG_TCK	J3	JTAG
T35 PAD	PCH_JTAG_TMS	H7	
T36 PAD	PCH_JTAG_TDI	K5	
T37 PAD	PCH_JTAG_TDO	H1	
SPI_CLK_PCH_R	T3	SPI_CLK	SPI
SPI_SB_CS0#	Y14	SPI_CS0#	
SPI_SB_CS1#	T1	SPI_CS1#	
SPI_SI	V4	SPI_MOSI	
SPI_SO_R	U3	SPI_MISO	

LPC:

FWH0 / LAD0	C38	LPC_AD0	LPC_AD0 <32>
FWH1 / LAD1	A38	LPC_AD1	LPC_AD1 <32>
FWH2 / LAD2	B37	LPC_AD2	LPC_AD2 <32>
FWH3 / LAD3	C37	LPC_AD3	LPC_AD3 <32>
FWH4 / LFRAME#	D36	LPC_FRAME#	LPC_FRAME# <32>
LDRQ0#	E36		
LDRQ1# / GPIO23	K36		
SERIRQ	V5	SERIRQ	SERIRQ <32>

EC and Mini card debug port

SATA 6G:

SATA0RXN	AM3	SATA_DTX_C_IRX_N0	SATA_DTX_C_IRX_N0 <30>
SATA0RXP	AM1	SATA_DTX_C_IRX_P0	SATA_DTX_C_IRX_P0 <30>
SATA0TXN	AP7	SATA_ITX_C_DRX_N0	SATA_ITX_C_DRX_N0 <30>
SATA0TXP	AP5	SATA_ITX_C_DRX_P0	SATA_ITX_C_DRX_P0 <30>

HDD

SATA1RXN	AM10		
SATA1RXP	AM8		
SATA1TXN	AP11		
SATA1TXP	AP10		
SATA2RXN	AD7	SATA_DTX_C_IRX_N2	SATA_DTX_C_IRX_N2 <30>
SATA2RXP	AD5	SATA_DTX_C_IRX_P2	SATA_DTX_C_IRX_P2 <30>
SATA2TXN	AH5	SATA_ITX_C_DRX_N2	SATA_ITX_C_DRX_N2 <30>
SATA2TXP	AH4	SATA_ITX_C_DRX_P2	SATA_ITX_C_DRX_P2 <30>

ODD

SATA3RXN	AB8		
SATA3RXP	AB10		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	Y7		
SATA4RXP	Y5		
SATA4TXN	AD3		
SATA4TXP	AD1		
SATA5RXN	Y3		
SATA5RXP	Y1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	Y11	R111 37.4_0402_1% +V1.05S_VCCP	
SATAICOMPI	Y10	SATA_COMP	
SATA3RCOMPO	AB12	R113 49.9_0402_1% +V1.05S_VCCP	
SATA3COMPI	AB13	SATA3_COMP	
SATA3RBIAS	AH1	RBIAS_SATA3; R115 750_0402_1%	
SATALED#	P3	SATALED#	
SATA0GP / GPIO21	V14		
SATA1GP / GPIO19	P1	BBS_BIT0_R	

GPIO19 has internal Pull UP

PANTHER-POINT_FCBGA989
HM76@

U4 HM70@ — SA00005MQ80
S IC BD82HM70 SJTNV C1 BGA 989P PCH C38!

+3V_ROM
R266 2_SPI_WP#1 3.3K_0402_5%
R221 2SPI_HOLD#1 3.3K_0402_5%
R127 2_SPI_WP# 3.3K_0402_5%
R129 2SPI_HOLD# 3.3K_0402_5%

+3VS — RP17 10K_0804_8P4R_5%
BBS_BIT0_R; SATALED#; PCH_GPIO16; SERIRQ
<19> PCH_GPIO16

SPI_CLK_PCH_R — R124 33_0402_5% @ — C190 22P_0402_50V @ For EMI

R124;c190 close to U4.T3 pin

11/30 Add(Share ROM)

Near U5

RP27 0_0804_8P4R_5% @

<32> EC_SPI_SO	EC_SPI_SO	8	1 SPI_SO_L
<32> EC_SPI_SI	EC_SPI_SI	7	2 SPI_SI_R
<32> EC_SPI_CLK	EC_SPI_CLK	6	3 SPI_CLK_PCH_0
<32> EC_SPI_CS#	EC_SPI_CS#	5	4 SPI_SB_CS0#

8MB SPI ROM FOR ME & Non-share ROM.

+3V_ROM — U6 64M W25Q64FVSSIQ SOIC 8P @
SPI_SB_CS1# — R188 0_0402_5% @ — SPI_SO_R
SPI_SO1; SPI_WP#1
CS# VCC; SO HOLD#; WP# SCLK; GND SI
SPI_HOLD#1; SPI_CLK_PCH; SPI_SI1
R198 0_0402_5% @ SPI_CLK_PCH_R
R196 0_0402_5% @ SPI_SI
For EMI

U6 Rersver 4M+2M Solution

+3V_ROM — U5 64M W25Q64FVSSIQ SOIC 8P
SPI_SB_CS0# — R131 0_0402_5% @ — SPI_SO_R
SPI_SO_L; SPI_WP#
CS# VCC; SO HOLD#; WP# SCLK; GND SI
SPI_HOLD#; SPI_CLK_PCH; SPI_SI_R
R135 0_0402_5% @ SPI_CLK_PCH_R
R133 0_0402_5% @ SPI_SI
For EMI

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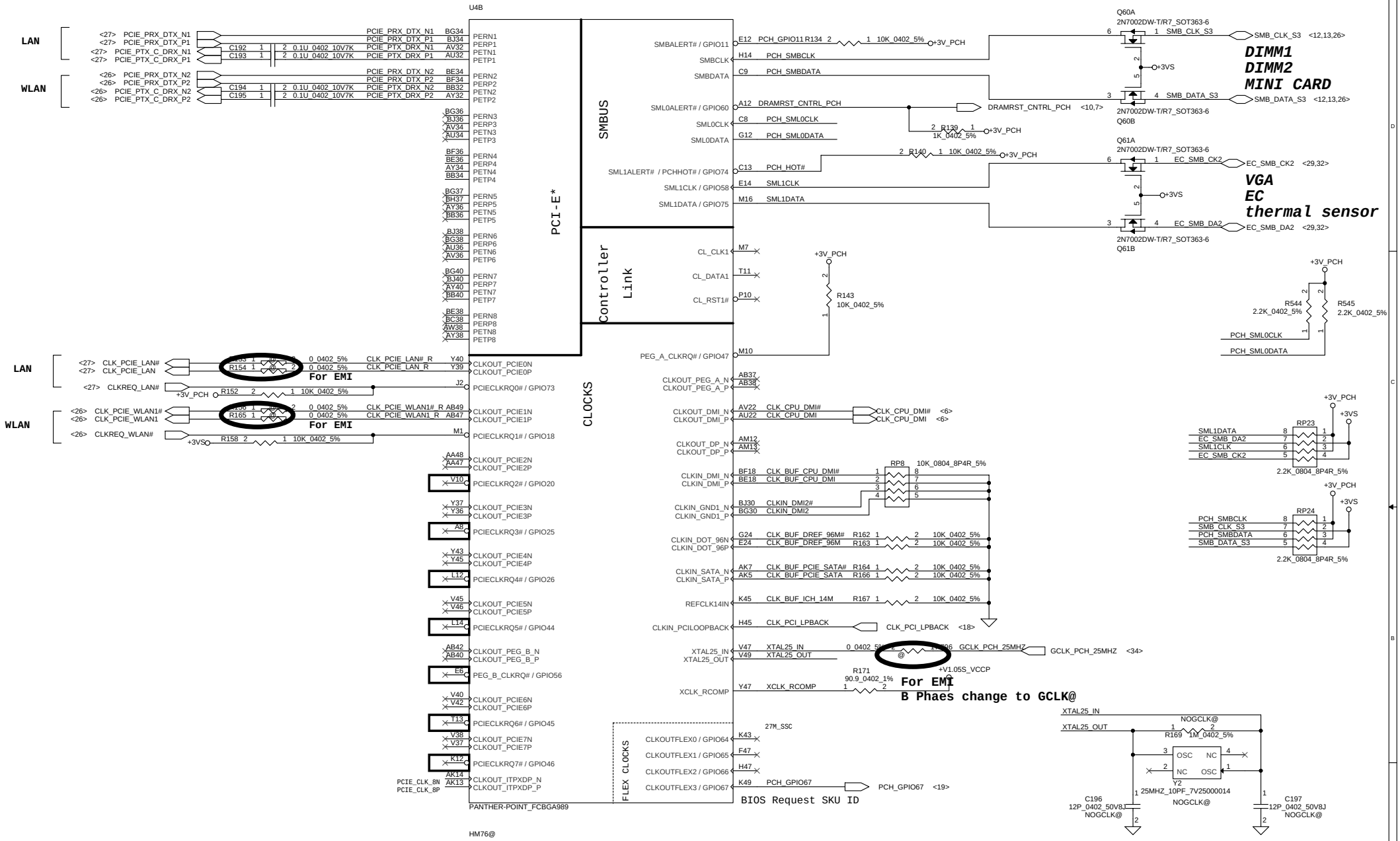

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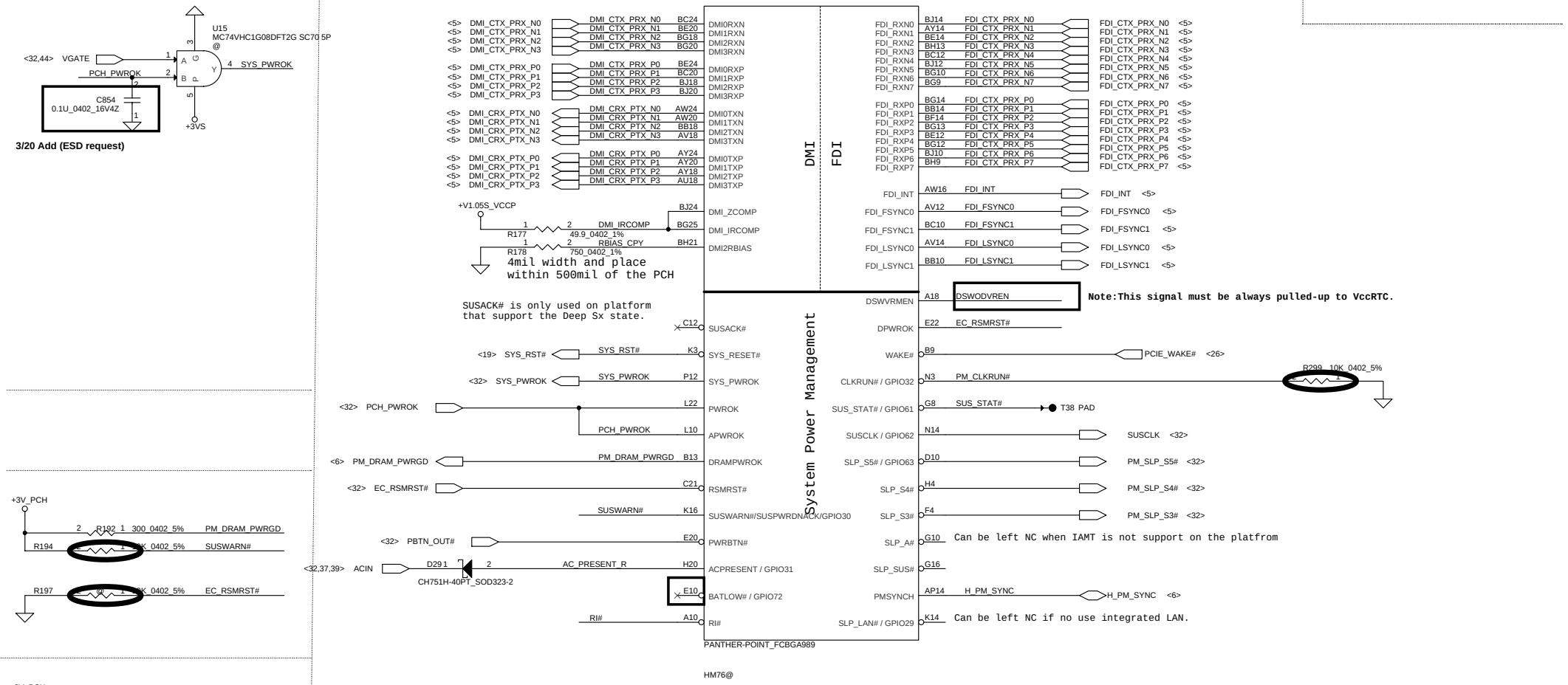

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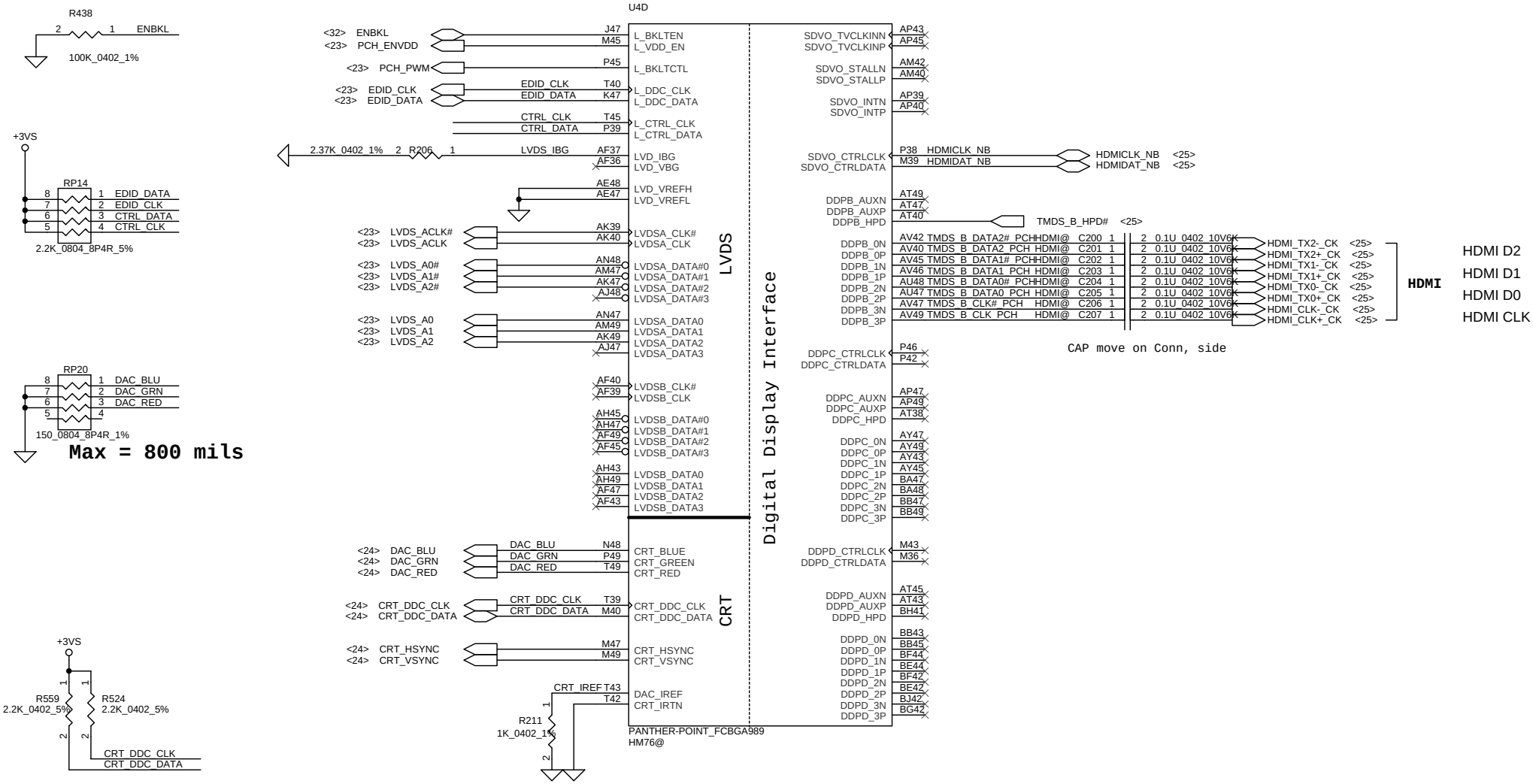

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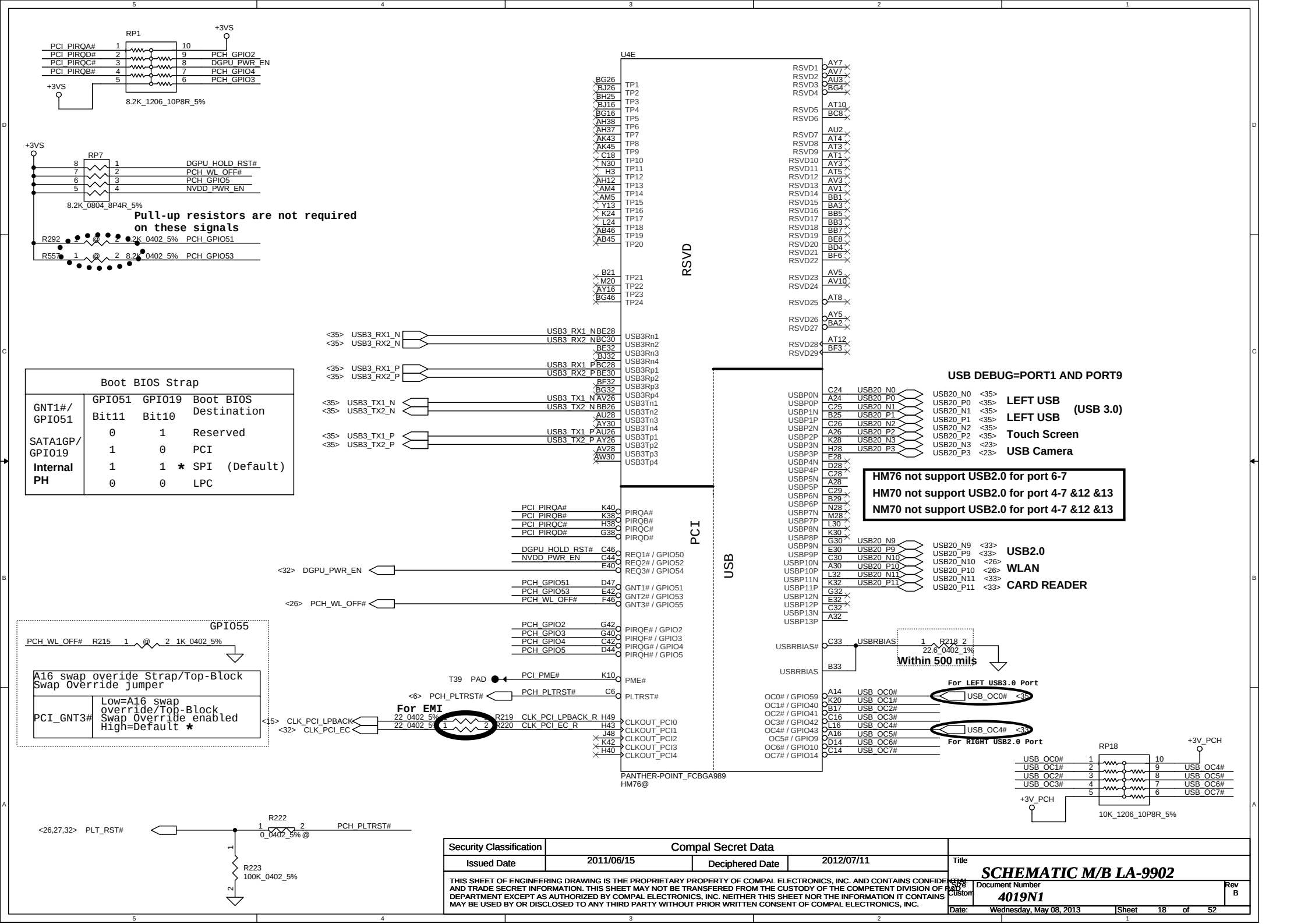

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PCH_GPIO69	PCH_GPIO70	Function
-	-	NM70
-	-	Reserved
-	1	HM70
-	0	HM76

PCH_GPIO71	Function
1	N14M-GE 1000MHz
0	N14M-GE 900MH

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

R240 1 @ 2 1K_0402_5% PCH_GPIO28

*
PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.

+3VS
R248 @ 10K_0402_5% PCH_GPIO37
R881 10K_0402_5% @
+3VS
R250 @ 10K_0402_5% PCH_GPIO36
R547 10K_0402_5% @

BIOS Request SKU ID

+3VS
R711 UMA@ 10K_0402_5%
R246 UMA@ 10K_0402_5%
PCH_GPIO38
PCH_GPIO67 PCH_GPIO67 <15>
R708 OPT@ 10K_0402_5%
R298 OPT@ 10K_0402_5%

+3VS
RP10 10K_0804_8P4R_5%
8 PCH_GPIO39
7 SYS_RST# SYS_RST# <16>
6 PCH_BT_ON#
5 PCH_GPIO35

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

+3VS
R702 @ 10K_0402_5% PCH_GPIO69
R707 @ 10K_0402_5%
+3VS
R703 HM70@ 10K_0402_5% PCH_GPIO70
R705 HM76@ 10K_0402_5%
+3VS
R704 1000M@ 10K_0402_5% PCH_GPIO71
R706 900M@ 10K_0402_5%

U4F

GPIO
T7 BMBUSY# / GPIO0
A42 TACH1 / GPIO1
H36 TACH2 / GPIO6
<32> EC_SCI# EC_SCI# E38 TACH3 / GPIO7
<16,32> EC_SMI# EC_SMI# C10 GPIO8
C4 LAN_PHY_PWR_CTRL / GPIO12
+3V_PCH R230 1 2 1K_0402_5% EC_LID_OUT# G2 GPIO15
<32> EC_LID_OUT#
<14> PCH_GPIO16 PCH_GPIO16 U2 SATA4GP / GPIO16
PAD T67 DGPU_PWROK D40 TACH0 / GPIO17
<26> PCH_BT_ON# PCH_BT_ON# T5 SCLOCK / GPIO22
<30> ODD_EN ODD_EN E8 GPIO24
+3V_PCH R241 1 2 10K_0402_5% PCH_GPIO27 E16 GPIO27
PCH_GPIO28 P8 GPIO28
<26> INTEL_BT_OFF# INTEL_BT_OFF# R242 1 2 10K_0402_5% +3VS K1 STP_PCI# / GPIO34
PCH_GPIO35 K4 GPIO35
PCH_GPIO36 V8 SATA2GP / GPIO36
PCH_GPIO37 M5 SATA3GP / GPIO37
PCH_GPIO38 N2 SLOAD / GPIO38
PCH_GPIO39 M3 SDATAOUT0 / GPIO39
V13 SDATAOUT1 / GPIO48
V3 SATA5GP / GPIO49 / TEMP_ALERT#
D6 GPIO57

CPU/MISC
TACH4 / GPIO68 C40
TACH5 / GPIO69 B41 PCH_GPIO69
TACH6 / GPIO70 C41 PCH_GPIO70
TACH7 / GPIO71 A40 PCH_GPIO71
A20GATE P4 GATEA20 <32>
PECI AU16
RCIN# P5 KBRST# KBRST# <32>
PROCPWRGD AY11 H_CPUPWRGD <6>
THRMTRIP# AY10 PCH_THRMTRIP# R 1 2 H_THRMTRIP# R239 390_0402_5% H_THRMTRIP# <6>
INIT3_3V# T14
DF_TVS AY1
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37

NCTF
VSS_NCTF_1 A4
VSS_NCTF_2 A44
VSS_NCTF_3 A45
VSS_NCTF_4 A46
VSS_NCTF_5 A5
VSS_NCTF_6 A6
VSS_NCTF_7 B3
VSS_NCTF_8 B47
VSS_NCTF_9 BD1
VSS_NCTF_10 BD49
VSS_NCTF_11 BE1
VSS_NCTF_12 BE49
VSS_NCTF_13 BF1
VSS_NCTF_14 BF49
VSS_NCTF_15 BG2
VSS_NCTF_16 BG48
VSS_NCTF_17 BH3
VSS_NCTF_18 BH47
VSS_NCTF_19 BJ4
VSS_NCTF_20 BJ44
VSS_NCTF_21 BJ45
VSS_NCTF_22 BJ46
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ6
VSS_NCTF_25 C2
VSS_NCTF_26 C48
VSS_NCTF_27 D1
VSS_NCTF_28 D49
VSS_NCTF_29 E1
VSS_NCTF_30 E49
VSS_NCTF_31 F1
VSS_NCTF_32 F49

PANTHER-POINT_FCBGA989

HM76@

+3VS
R236 10K_0402_5%
KBRST# R226 1 2 10K_0402_5%

INIT3_3V
This signal has weak internal PU,can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

+1.8VS
R216 2.2K_0402_5%
NV_CLE
R217 1K_0402_5% H_SNB_IVB# <6>
Weak internal PU,Do not pull low
CLOSE TO THE BRANCHING POINT

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L1 Change to 1 ohm P/N
S RES 1/10W 1 +-1% 0603

POWER

U4G

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Intel recommand **VCCVRM==>1.5V FOR MOBILE**
stuff R265 and unstuff R266 **VCCVRM==>1.8V FOR DESKTOP**

VCCVRM = 160mA detal waiting for newest spec

11/30 Add(Share ROM)

12/20 Place @ first

PANTHER-POINT_FCBGA989

HM76@

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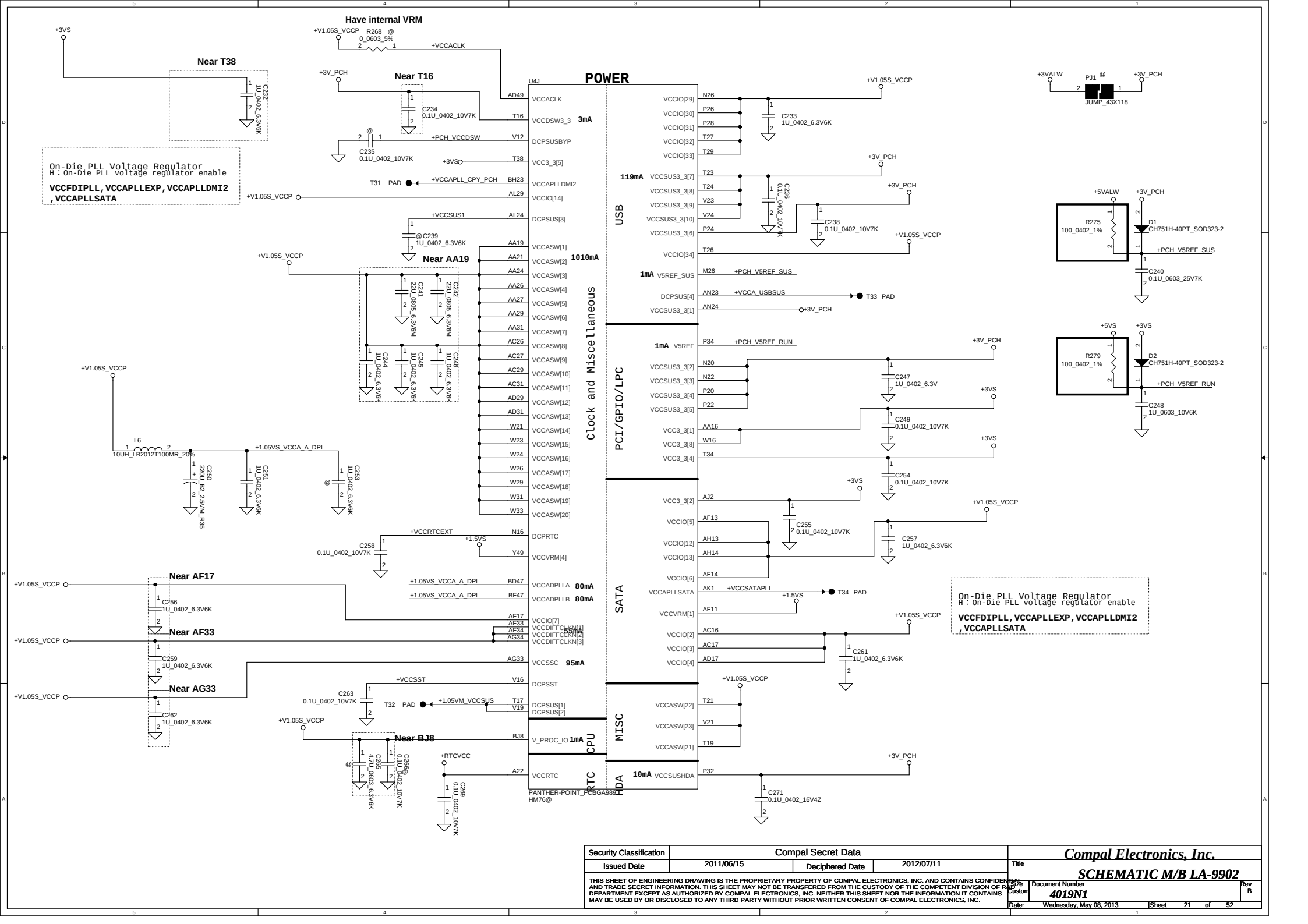

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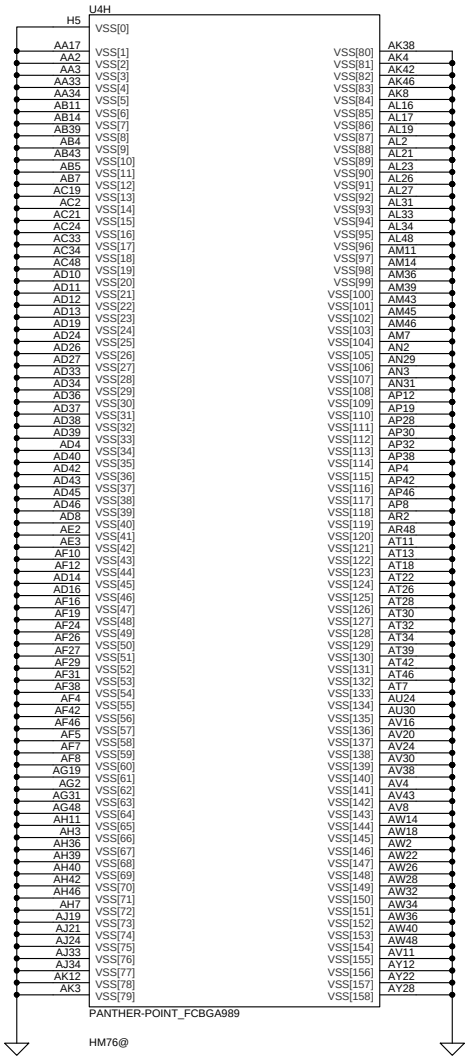

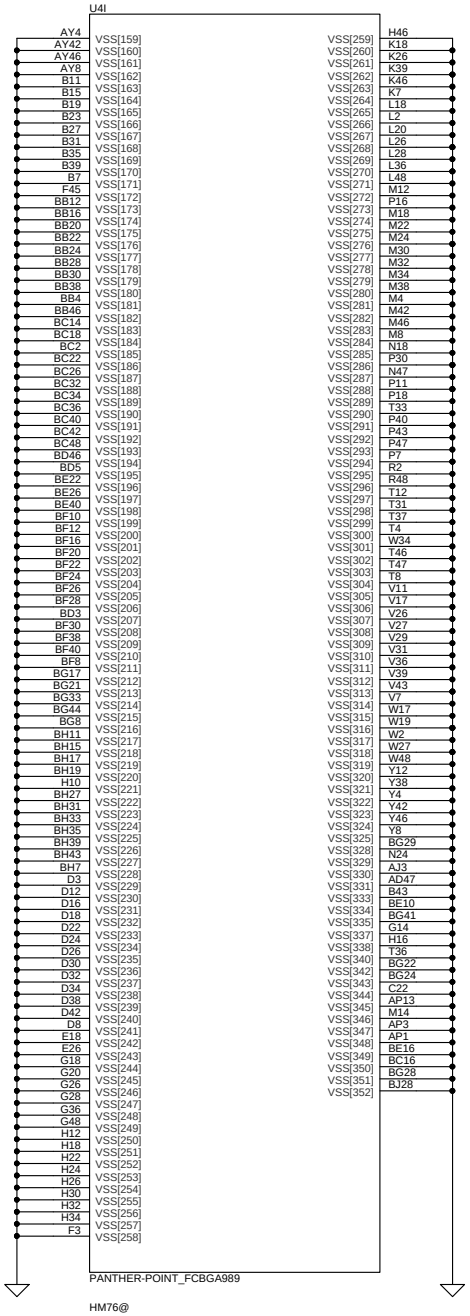

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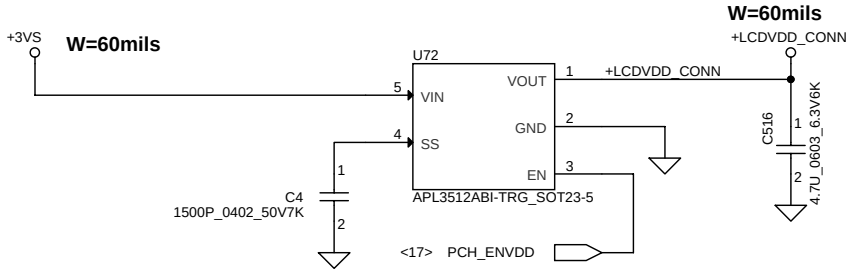
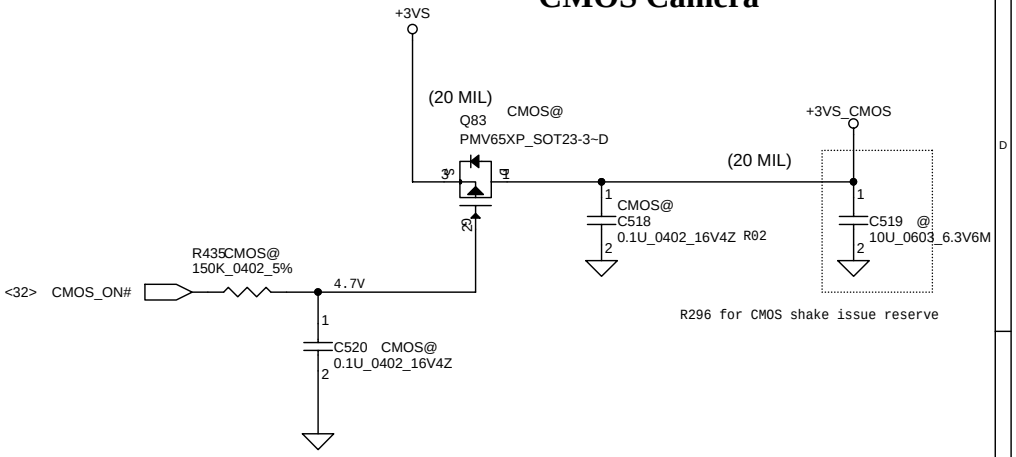
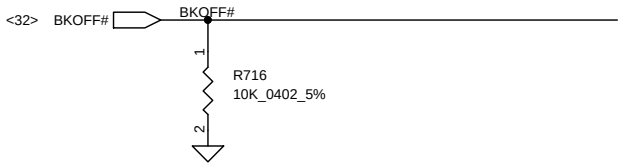
LCD POWER CIRCUIT



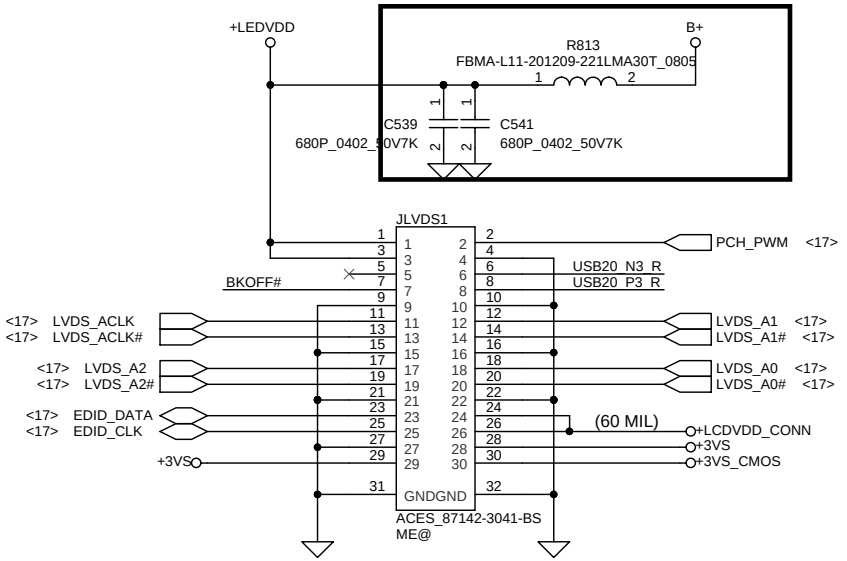
CMOS Camera



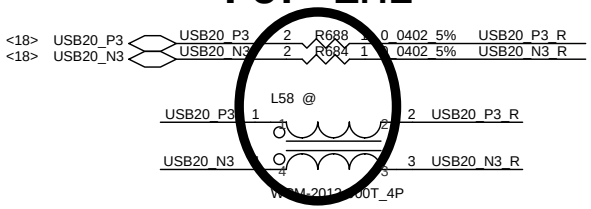
VGA LCD/PANEL BD. Conn.



12/12 Mount C539/C541 of 680pF,Chanage R813 to 220 ohm bead.(For EMI request)



For EMI



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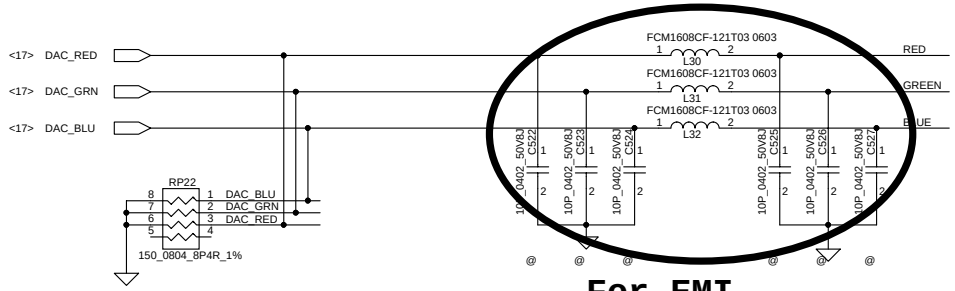
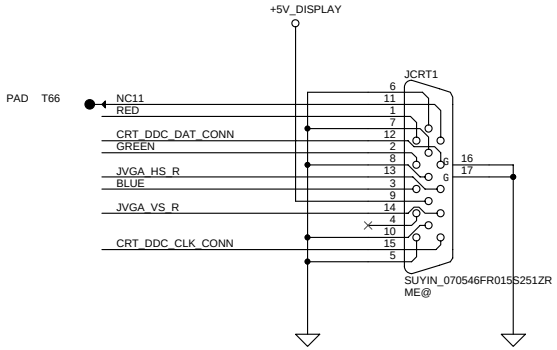
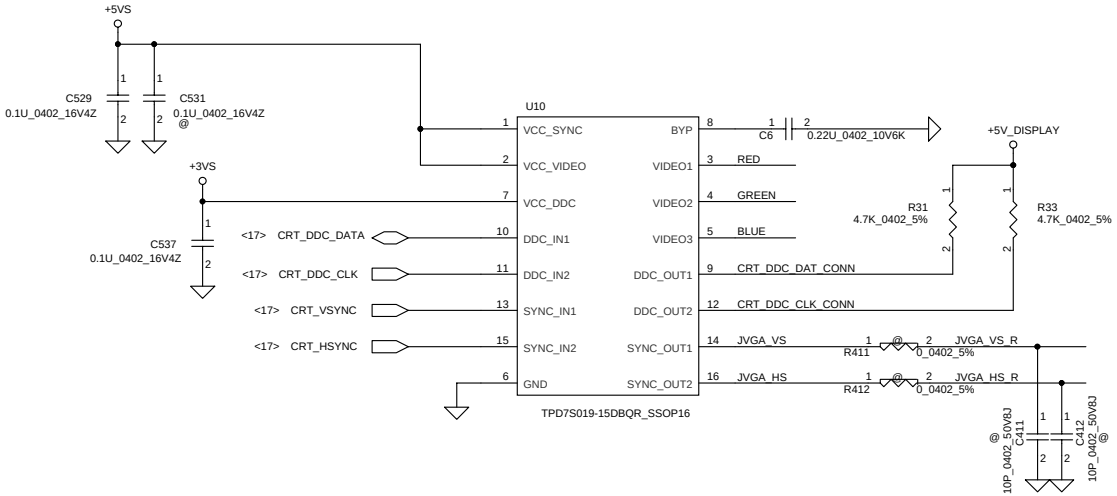


For EMI





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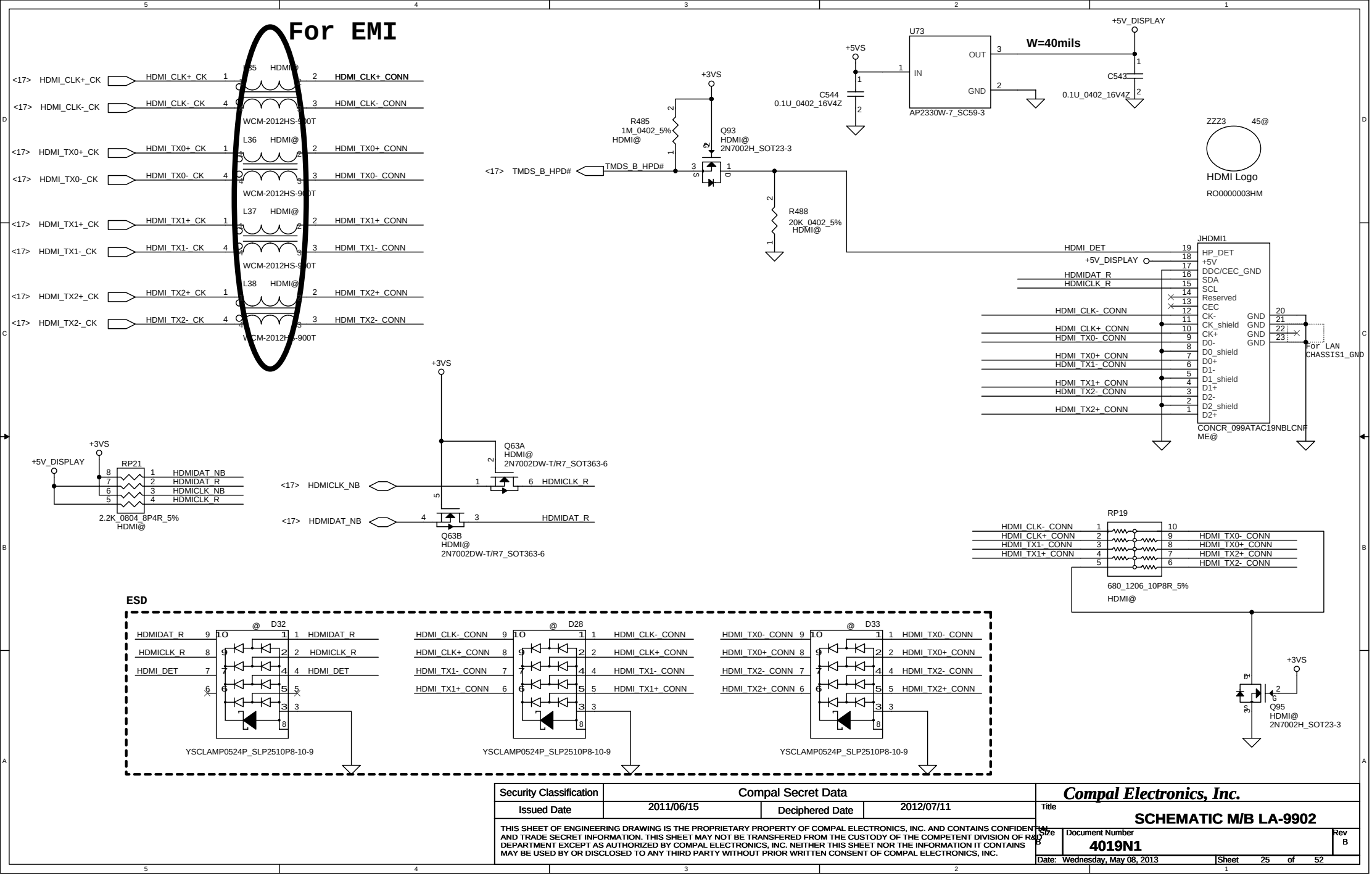

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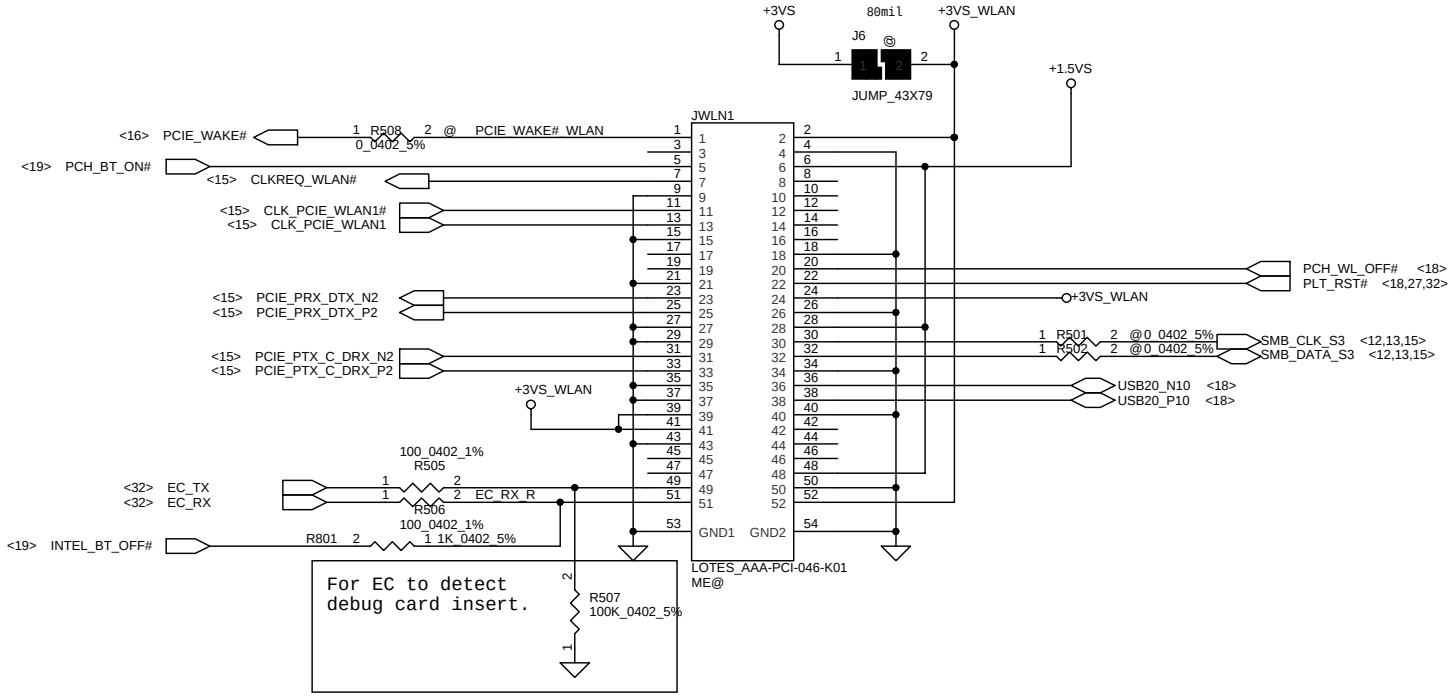
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

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For LAN & Green CLK

+3VALW
+3V_LAN
J12
JUMP_43X79
QL1
LP2301ALT1G-SOT23-3
RL3
<32> LAN_PWR_ON#
LAN_PWR_ON#
10K_0402_5%
CL7
0.1U_0402_16V7K

Vendor recommand reseve the PU resistor close LAN chip

Close together

+LX
LL1 SWR@
4.7UH_SIA4012-4R7M_2.7A
+LX_R
CL1 1000P_0402_50V7K
CL2 0.1U_0402_16V4Z
CL3 10U_0603_6.3V6M
10U
SWR@SWR@SWR@

Note: Place Close to LAN chip
LL1 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

LL2 FBMA-L11160808601LMA10T_2P
LL3 SWR@ FBMA-L11160808601LMA10T_2P
+1.1_AVDDL_L
+1.1_AVDDL
+LX_R
CL4 0.1U_0402_16V4Z
CL5 1U_0402_6.3V4Z
CL6 4.7U_0603_6.3V6K

Place close to Pin34

+3V_LAN
RL4 4.7K_0402_5%
<18,26,32> PLT_RST#
PLT_RST#

UL1 8172@
QCA8172-BL3A-R

Pin	Configure signal	Description	
LED[1]	Regulator select	1	Switch mode regulator(SWR) mode
		0	Linear regulator (LDO) mode ★

+3V_LAN
CL10 0.1U_0402_16V4Z
CL8 1U_0402_6.3V4Z

Place close to Pin16

Place Close to Chip

UL1
Atheros
AR8151/AR8161

<15> PCIE_PRX_DTX_N1 — CL9 0.1U_0402_16V7K — PCIE_PRX_C_DTX_N1 — 29 TX_N
<15> PCIE_PRX_DTX_P1 — CL11 0.1U_0402_16V7K — PCIE_PRX_C_DTX_P1 — 30 TX_P
<15> PCIE_PTX_C_DRX_N1 — 36 RX_N
<15> PCIE_PTX_C_DRX_P1 — 35 RX_P
<15> CLK_PCIE_LAN# — 32 REFCLK_N
<15> CLK_PCIE_LAN — 33 REFCLK_P
PLT_RST# — 2 PERST#
PCIE_WAKE# R — 3 WAKE#
<32> LAN_WAKE# — RL7 0_0402_5%
+3V_LAN — RL9 4.7K_0402_5%
25 SMCLK
26 SMDATA
28 NC
27 TESTMODE

Vendor recommand reseve the PU resistor close LAN chip

+3V_LAN — RL11 4.7K_0402_5%
LAN_XTALO — 7 XTLO
LAN_XTALI — 8 XTLI
<15> CLKREQ_LAN# — 4 CLKREQ#

LED_0 38
LED_1 39
LED_2 23
RL12 10K_0402_5% LDO@
mount RL12 if use LDO modue

TRXN0 12 MDI0- — MDI0- <28>
TRXP0 11 MDI0+ — MDI0+ <28>
TRXN1 15 MDI1- — MDI1- <28>
TRXP1 14 MDI1+ — MDI1+ <28>
TRXN2 17
TRXP2 21
TRXN3 20
TRXP3

RBIAS 10 — LAN_RBIAS — RL8 2.37K_0402_1%
Place Close to PIN1

VDD33 1 +3V_LAN
LX 40 +LX
VDDCT/ISOLAN 5 +1.7_VDDCT — RL10 30K_0402_5% — +3V_LAN
DVDDL/PPS 24
DVDDL_REG/DVDDL 37 +LX_R

Place Close to PIN1
+3V_LAN
CL12 1000P_0402_50V7K
CL13 0.1U_0402_16V4Z
CL14 1U_0402_6.3V4Z
CL15 10U_0603_6.3V6M
CL16 10U_0603_6.3V6M

don't @ (could be B C cost done)

+1.1_AVDDL — 13 AVDDL
+1.1_AVDDL — 19 AVDDL
+1.1_AVDDL — 31 AVDDL
+1.1_AVDDL_L — 34 AVDDL
+1.1_AVDDL — 6 AVDDL
AVDDL_REG/AVDDL
41 GND
AR8162-BL3A-R_QFN40_5X5
8162@

16 +3V_LAN
22 +2.7_AVDDH — AVDDH/AVDDH33
9 +2.7_AVDDH — AVDDH_REG
+2.7_AVDDH

CL17 0.1U_0402_16V4Z — Near Pin13
CL18 0.1U_0402_16V4Z — Near Pin19
CL19 0.1U_0402_16V4Z — Near Pin31
CL20 1U_0402_6.3V4Z
CL21 0.1U_0402_16V4Z
Near Pin6
CL22 0.1U_0402_16V4Z
CL23 1U_0402_6.3V4Z — Near Pin9
CL24 0.1U_0402_16V4Z — Near Pin22
CL25 0.1U_0402_16V4Z
CL26 1U_0402_6.3V4Z — Near Pin37

For EMI
B Phaes change to GCLK@

<34> GCLK_LAN_25MHZ — RL13 0_0402_5%
value shoud be discuss ORB 5P
CL27 5P_0402_50V8C
LAN_XTALI
YL1 25MHZ_10PF_7V25000014 NC OSC OSC NC
LAN_XTALO
CL28 15P_0402_50V8J NOGCLK@
CL29 15P_0402_50V8J NOGCLK@

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ESD

Place Close to TL1

DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

@
DL1
AZC099-04S.R7G_SOT23-6
MDI1+ 1 I/O1
I/O3 4 MDI0+
2 GND
VDD 5
MDI0- 3 I/O2
I/O4 6 MDI1-

Reserve gas tube for EMI go rural solution

For EMI

CL30
10P_0603_50V
CHASSIS1_GND
BS4200N-C-LV_SMB-F2
GAS@

Place Close to TL1

For EMI

TL1
<27> MDI0+ MDI0+ 1 TD+ TX+ 16 MDO0+
<27> MDI0- MDI0- 2 TD- TX- 15 MDO0-
3 CT CT 14 MCT
4 NC NC 13
5 NC NC 12
6 CT CT 11 MCT
<27> MDI1+ MDI1+ 7 RD+ RX+ 10 MDO1+
<27> MDI1- MDI1- 8 RD- RX- 9 MDO1-
MHPC_NS681612A

12/12 Change BOM Structure of CL31 from @ to mount(EMI request)

CL31
0.01U_0402_16V7K

For EMI

CL63
0.1U_0603_50V7K
CHASSIS1_GND

JLAN1
MCT 8 PR4-
MCT 7 PR4+
MDO1- 6 PR2-
MCT 5 PR3-
MCT 4 PR3+
MDO1+ 3 PR2+
MDO0- 2 PR1-
MDO0+ 1 PR1+
SHLD1 10
SHLD2 9
PS_HPKR0125-08A1A0R
ME@
CHASSIS1_GND

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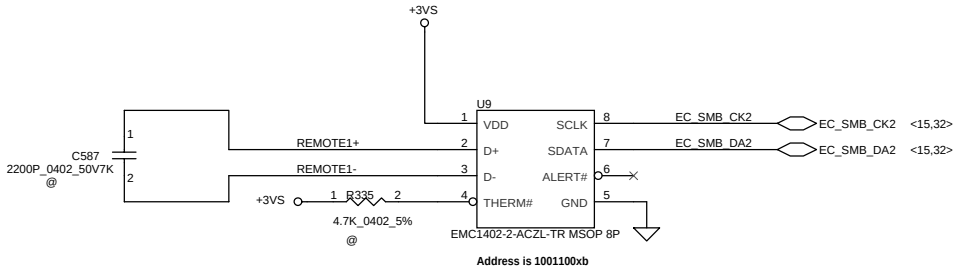
2 Channel

SMSC thermal sensor placed near VRAM



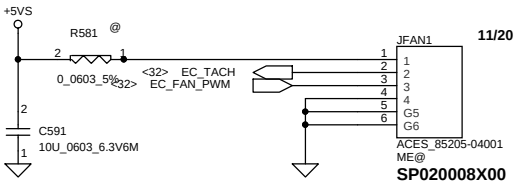
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

MINI WLAN VGA CPU

H1 H_3P3 H2 H_3P3 H4 H_3P3 H5 H_3P8 H6 H_3P8 H7 H_3P8

FD1 FD2 FD3 FD4

FAN1 Conn



11/20 Change symbol of JFAN1 to SP020008X00

H14 H_2P8 H15 H_2P8 H19 H_2P8 H20 H_2P8 H22 H_2P8 H23 H_2P8

R

H16 H_3P0X4P0N H24 H_3P0N H25 H_3P0N

E

M/B 橢圓孔 M/B 圓孔

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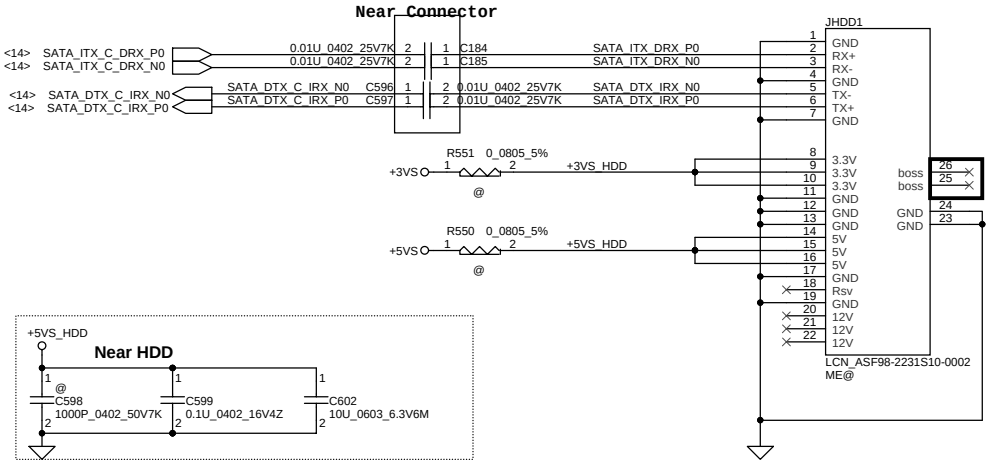
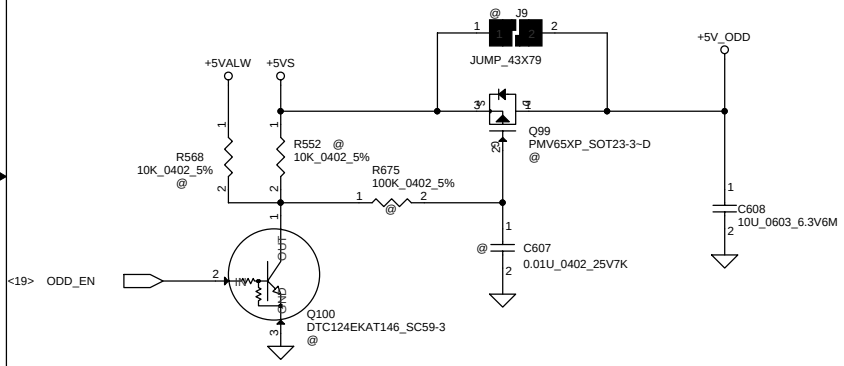
SATA HDD Conn.



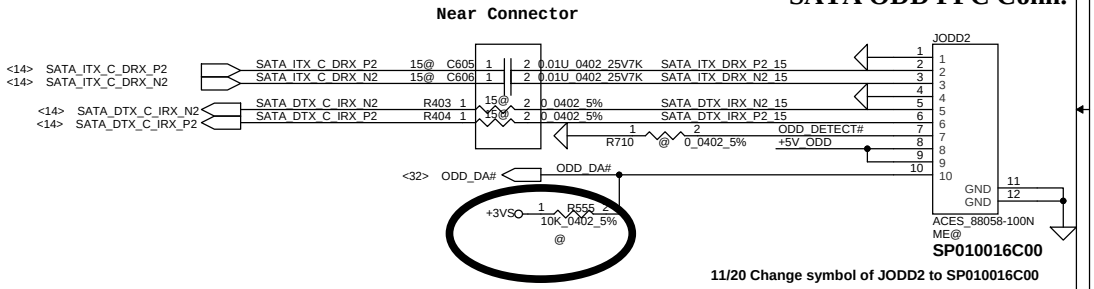
1/16 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 toDC010009C00)

ODD Power Control



FOR 15"

SATA ODD FFC Conn.

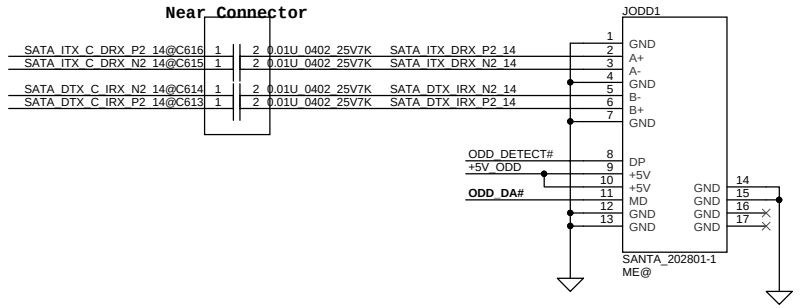


11/20 Change symbol of JODD2 to SP010016C00

Co-lay

FOR 14"

SATA ODD Conn.



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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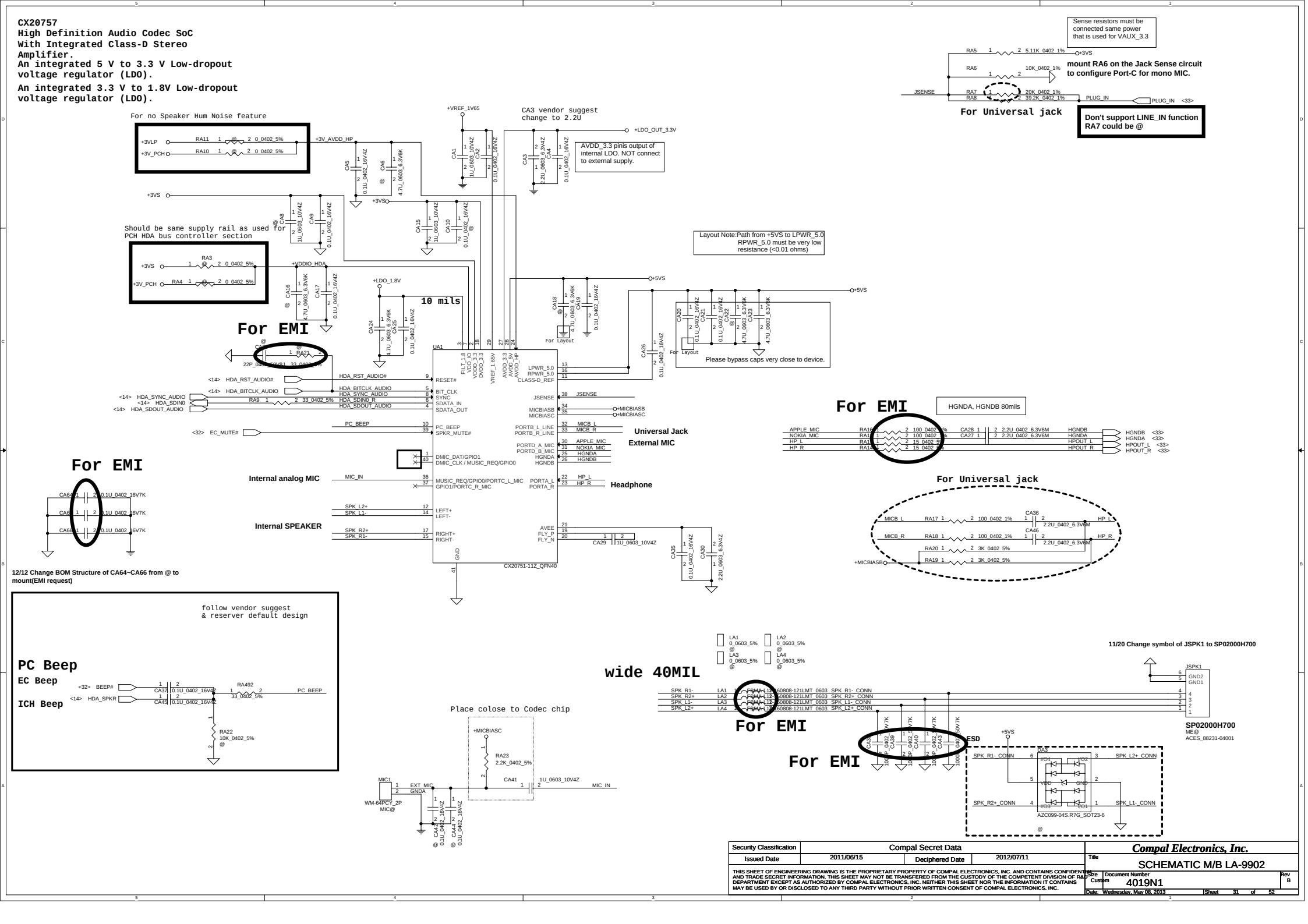
CX20757
High Definition Audio Codec SoC With Integrated Class-D Stereo Amplifier.
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



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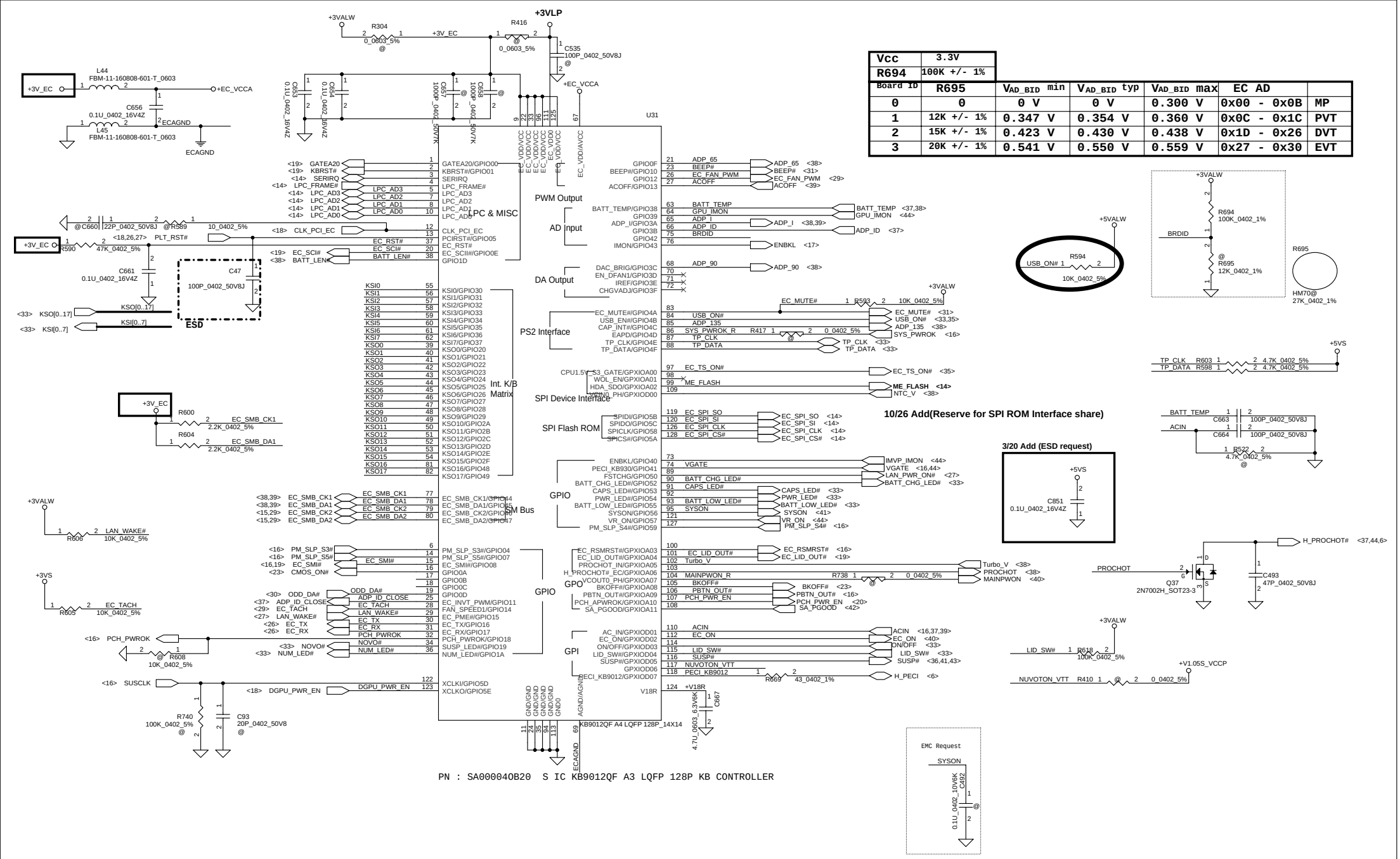

Vcc	3.3V					
R694	100K +/- 1%					
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

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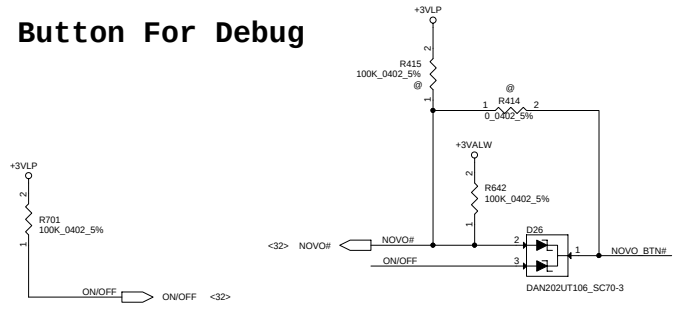
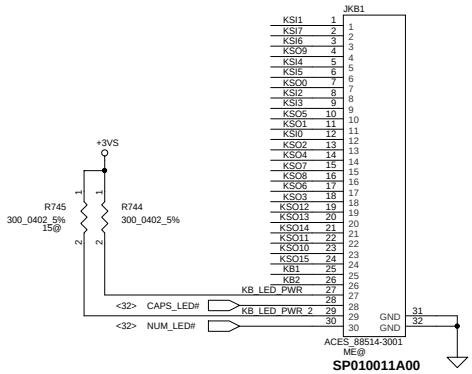
PWR Button For Debug



Key Board Conn.

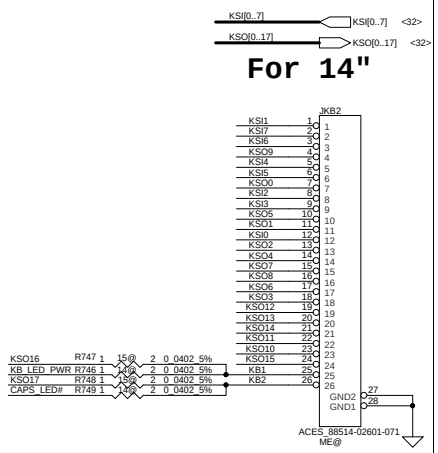
For 15"



SP010011A00

11/20 Change symbol of JKB1 to SP010011A00

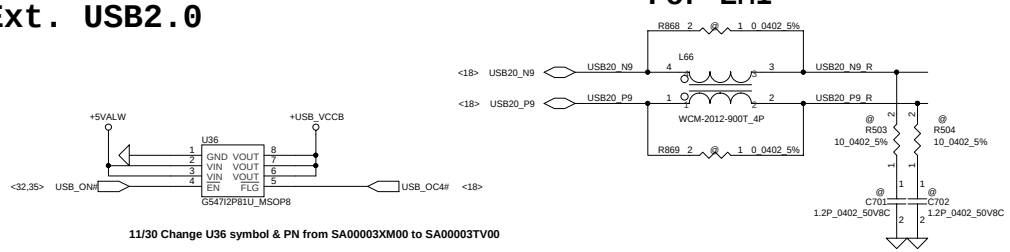
For 14"



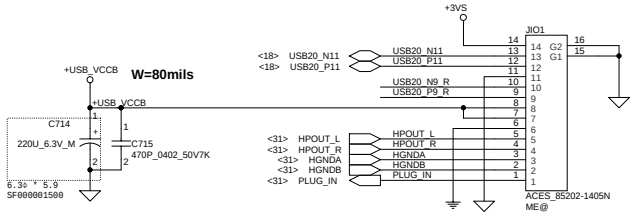
IO/B Conn.

Ext. USB2.0

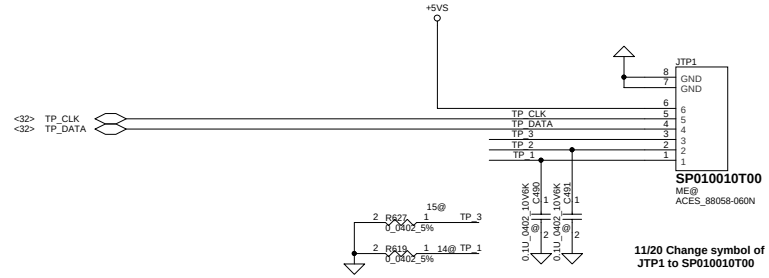
For EMI



11/30 Change U36 symbol & PN from SA00003XM00 to SA00003TV00

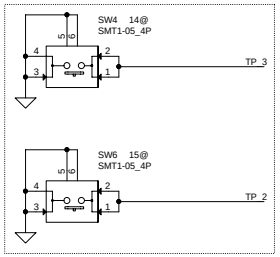


TP Switch & TP Conn.

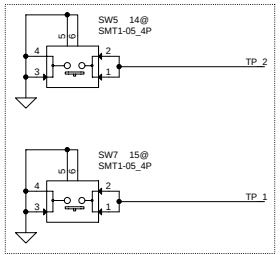


11/20 Change symbol of JTP1 to SP010010T00

L



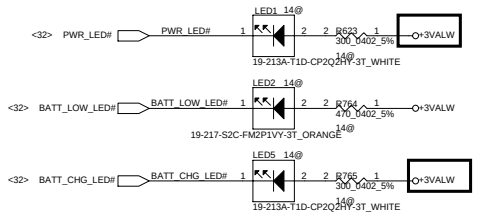
R



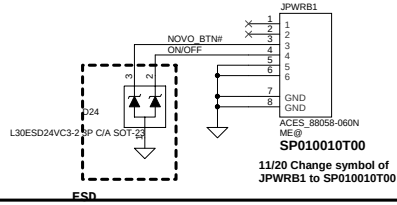
15"	
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"	
1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

LED



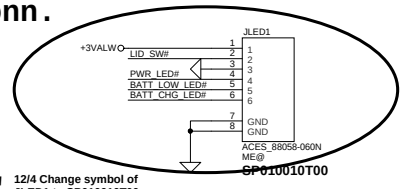
PWR/B Conn.



SP010010T00

11/20 Change symbol of JPWRB1 to SP010010T00

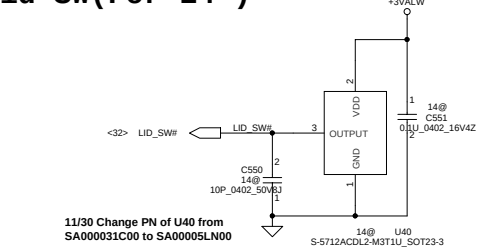
LED/B Conn.



SP010010T00

For 15" **12/4 Change symbol of JLED1 to SP010010T00**

Lid SW(For 14")



11/30 Change PN of U40 from SA000031C00 to SA00005LN00

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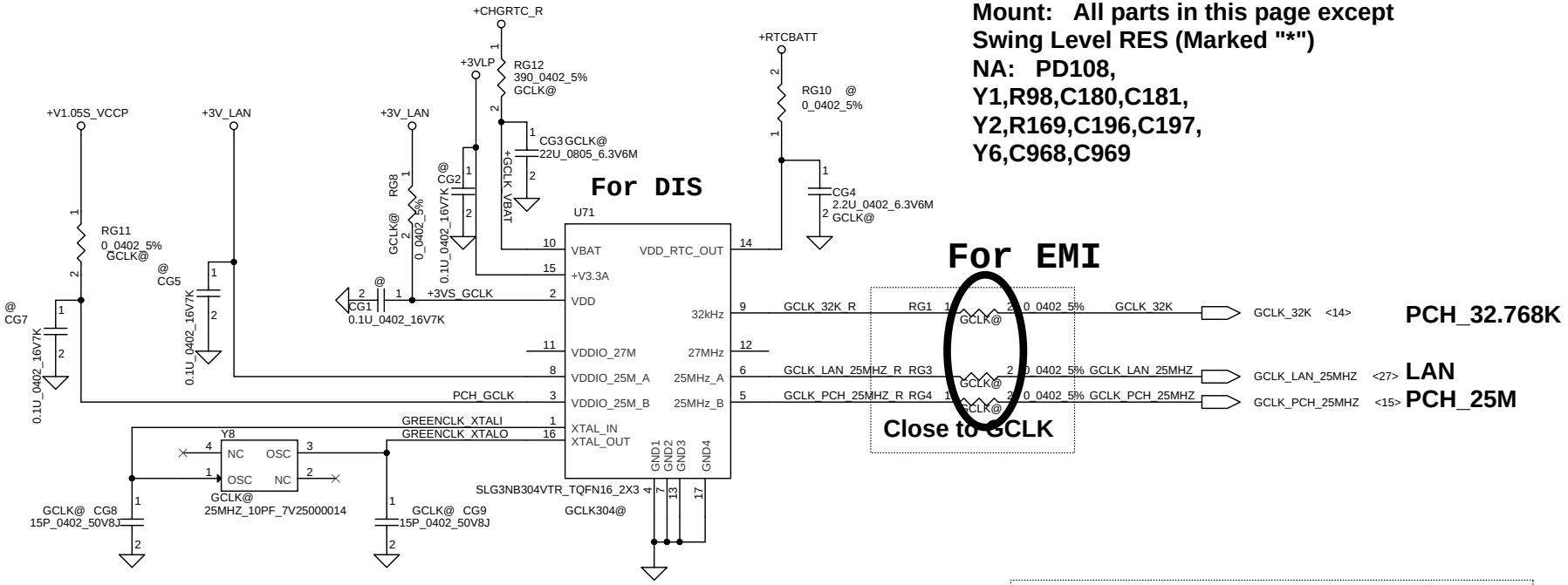
For UMA

U71 GCLK244@

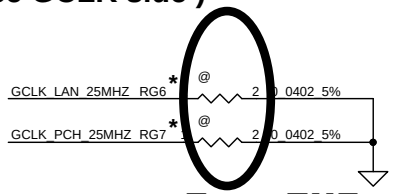
SLG3NB244VTR_TQFN16_2X3

Every power trace need:
W=20mils

For GreenCLK generate CLK:
Mount: All parts in this page except Swing Level RES (Marked "*")
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969



Reserved for Swing Level adjustment (Close GCLK side)



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Issued Date	2011/06/15	Deciphered Date 2012/07/11	Title: SCHEMATIC M/B LA-9902
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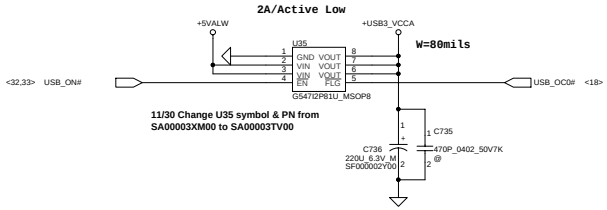
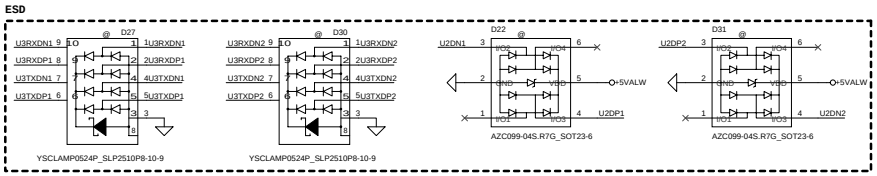
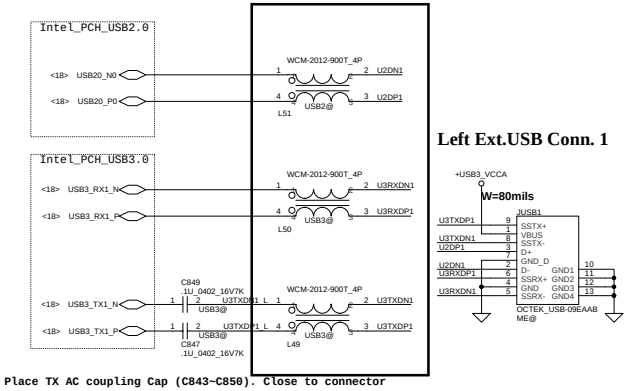
Touch Screen

USB3.0





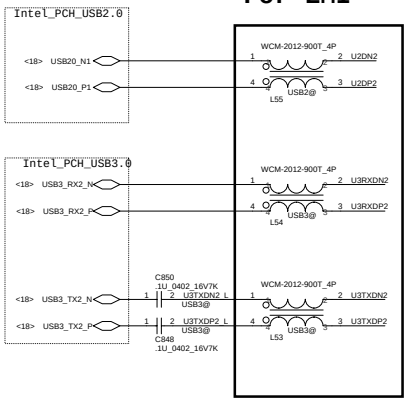
For EMI



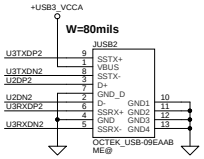
Left Ext.USB Conn. 1

Place TX AC coupling Cap (C843~C850). Close to connector

For EMI



Left Ext.USB Conn. 2



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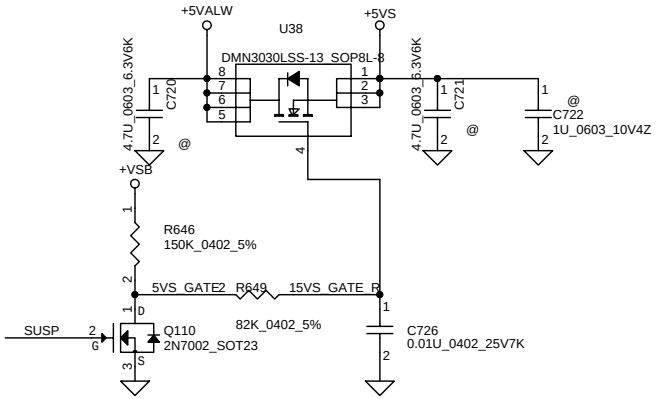
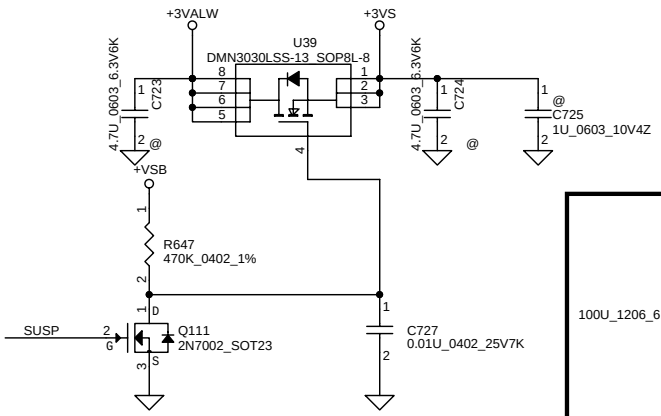
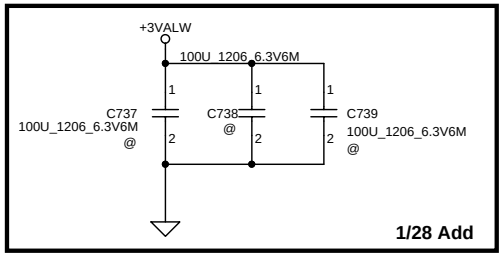
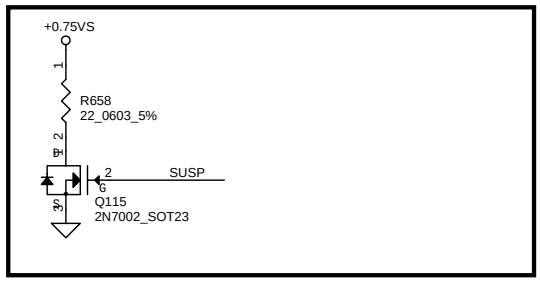
+5VALW to +5VS



+3VALW to +3VS

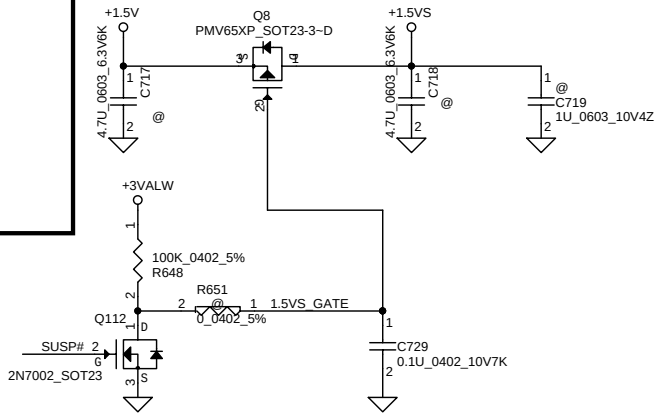


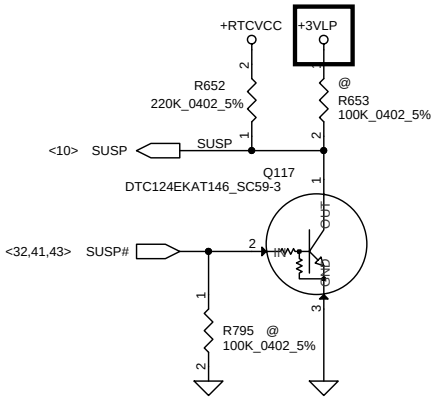




For Intel S3 Power Reduction.

+1.5V to +1.5VS





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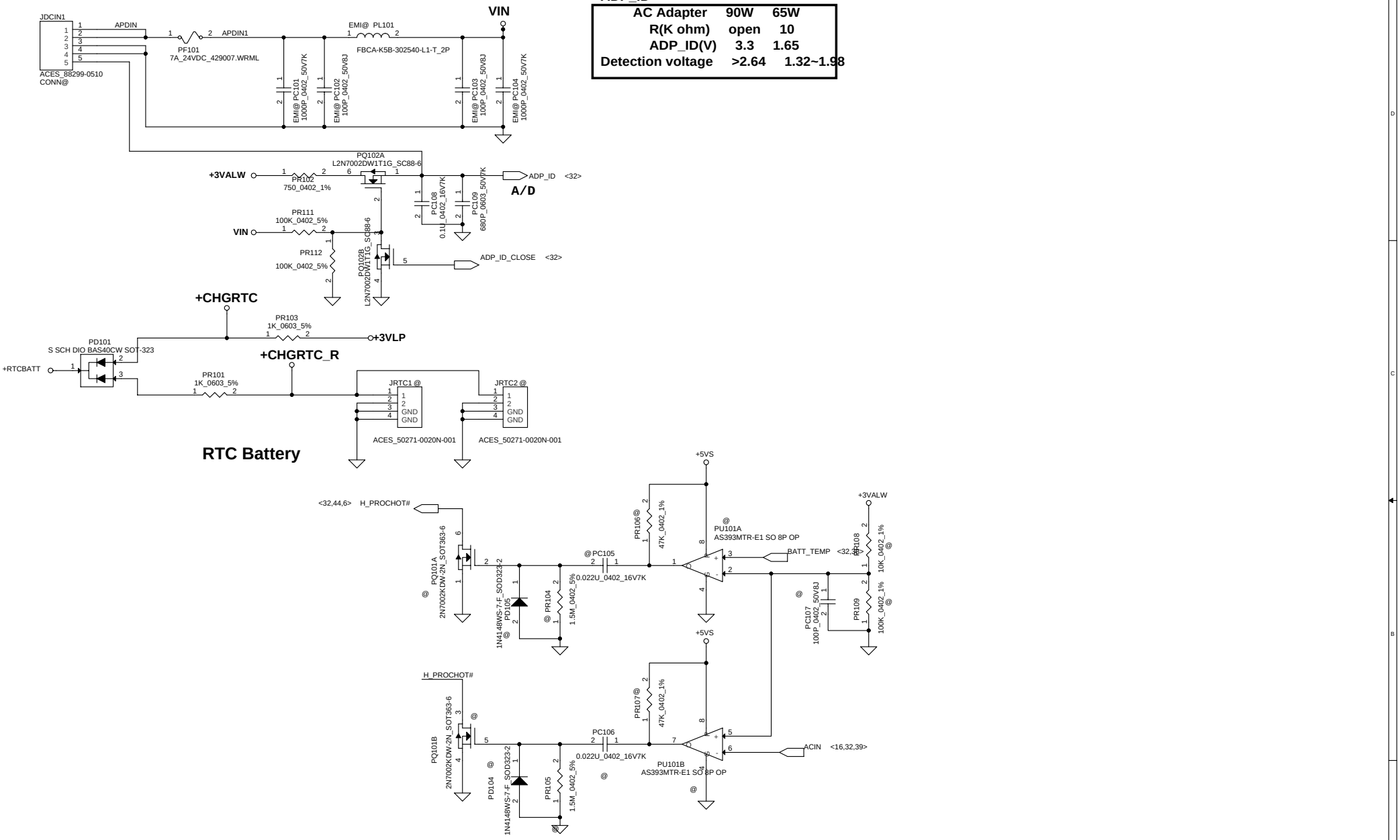

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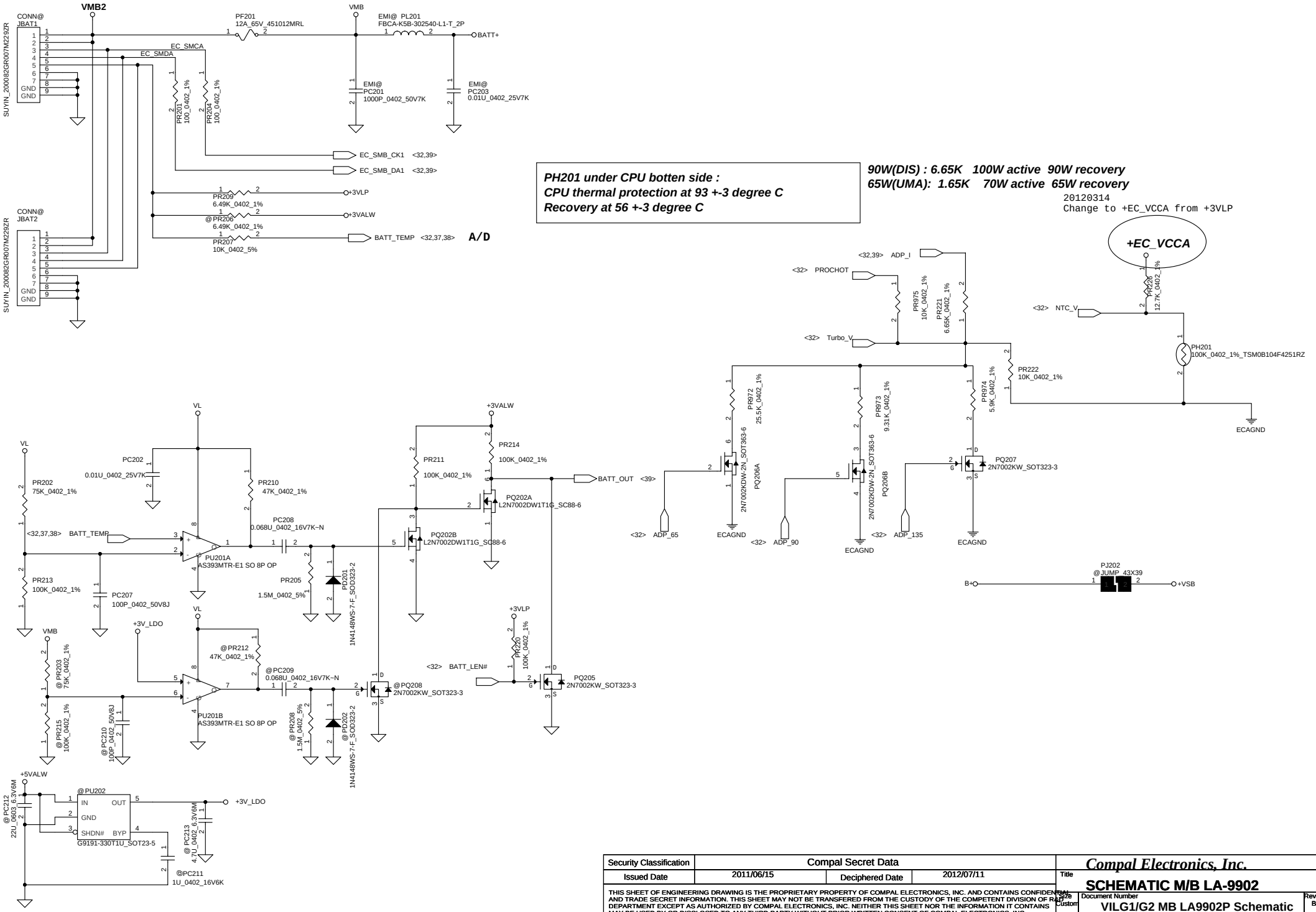

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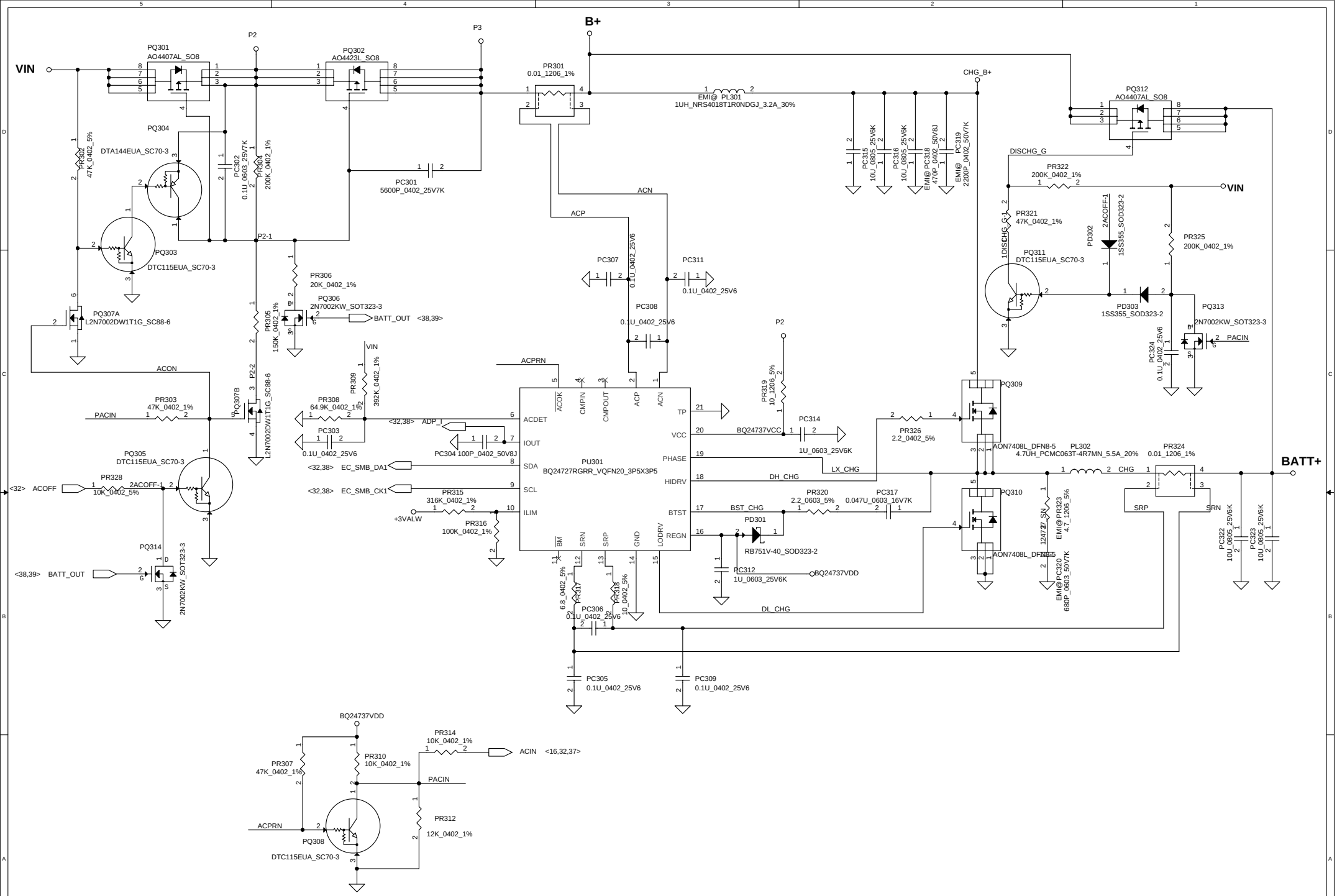

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Compal Electronics, Inc.

Title: **CHARGER**

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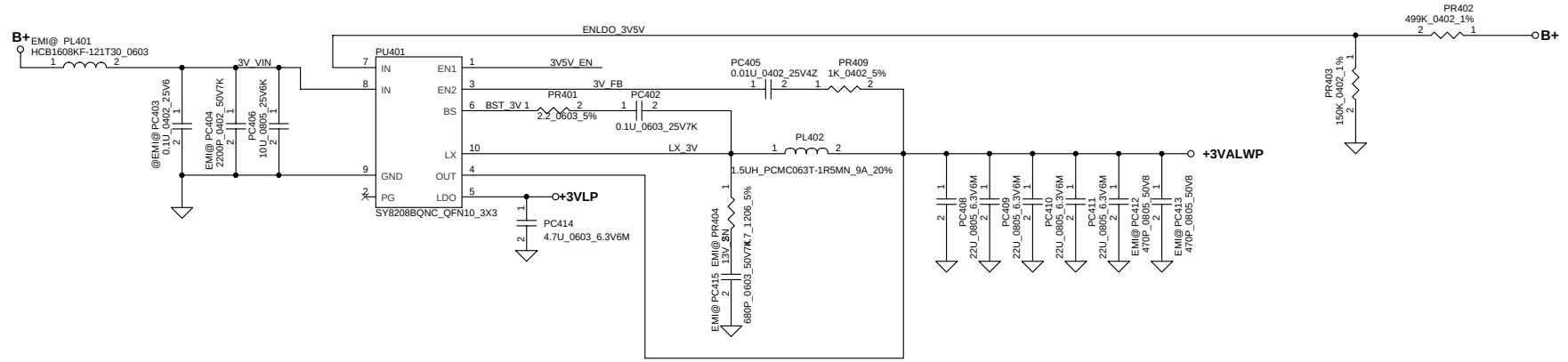

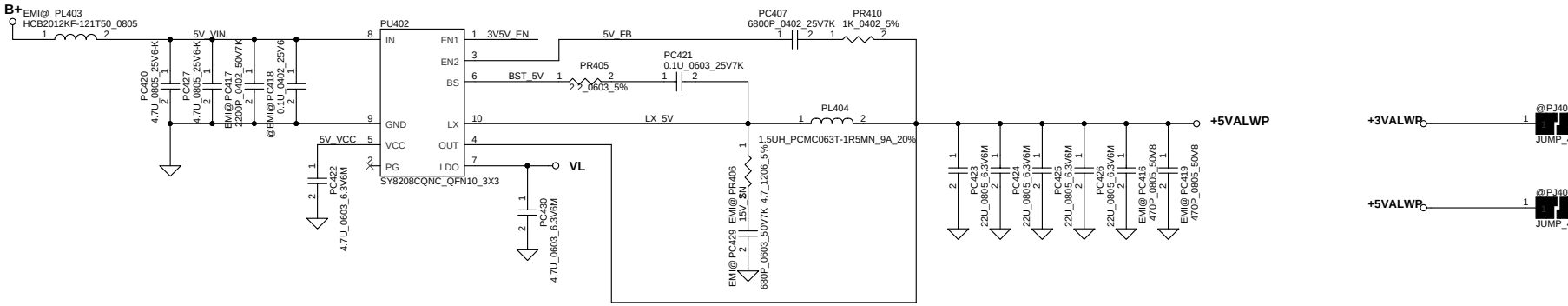

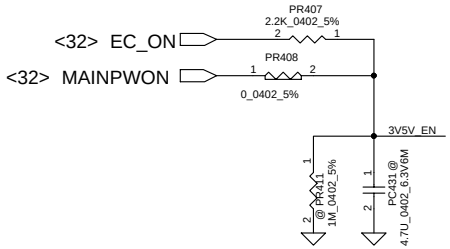

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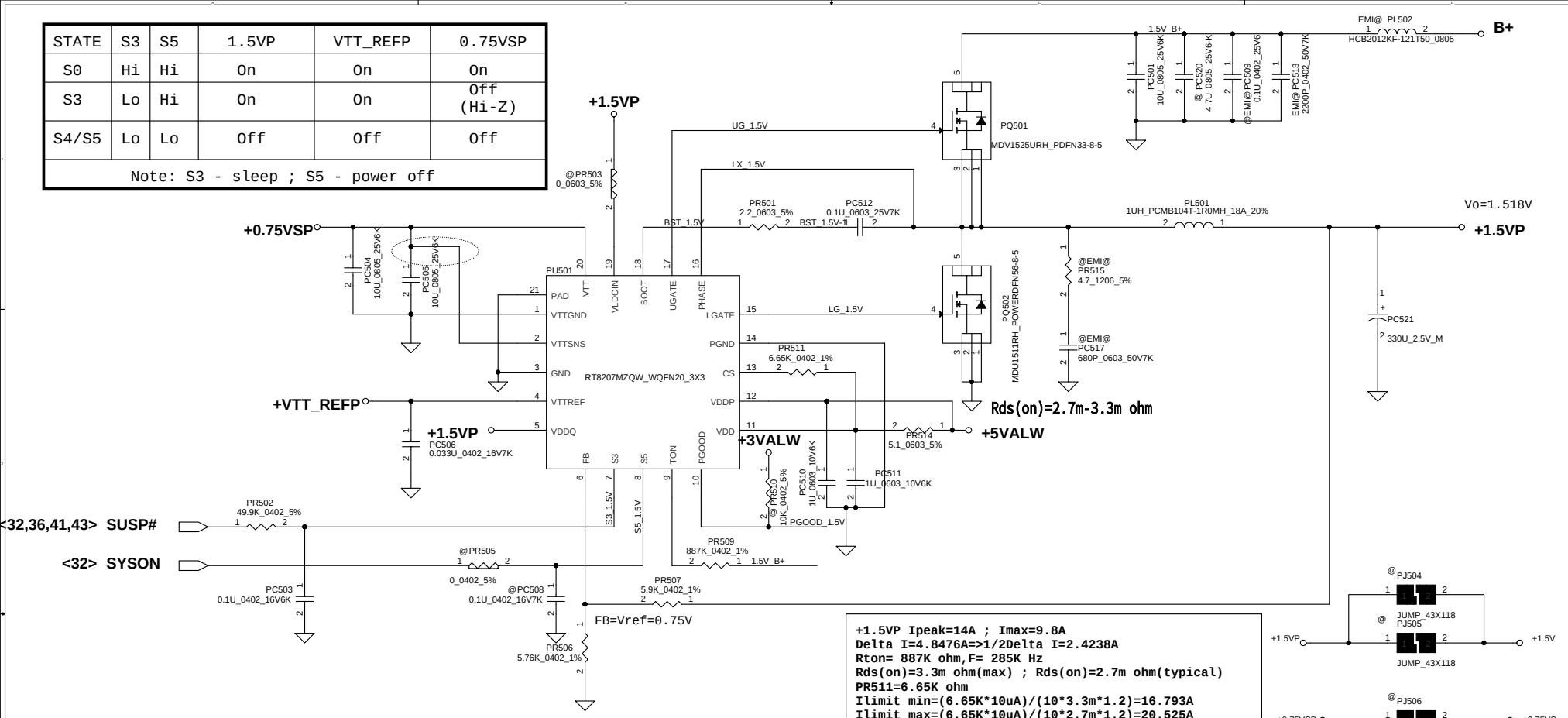
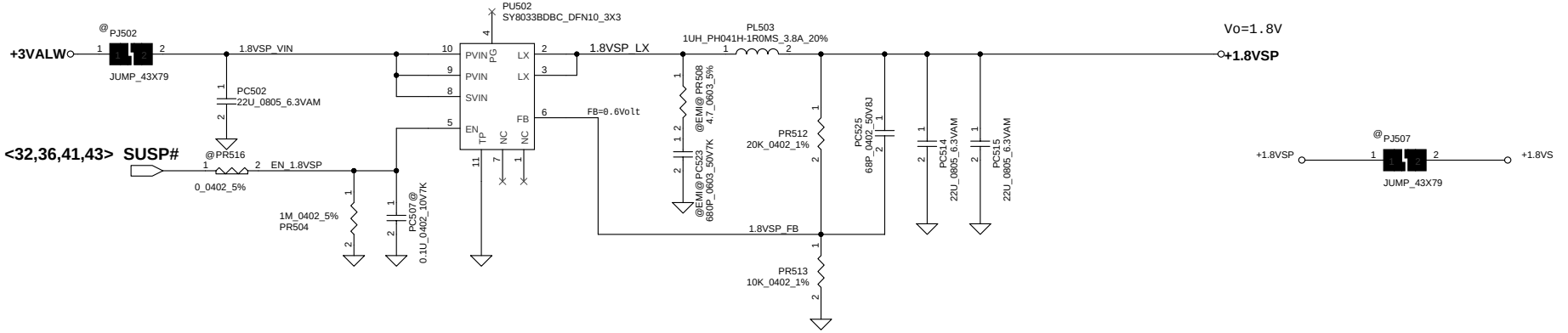
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					





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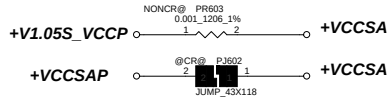
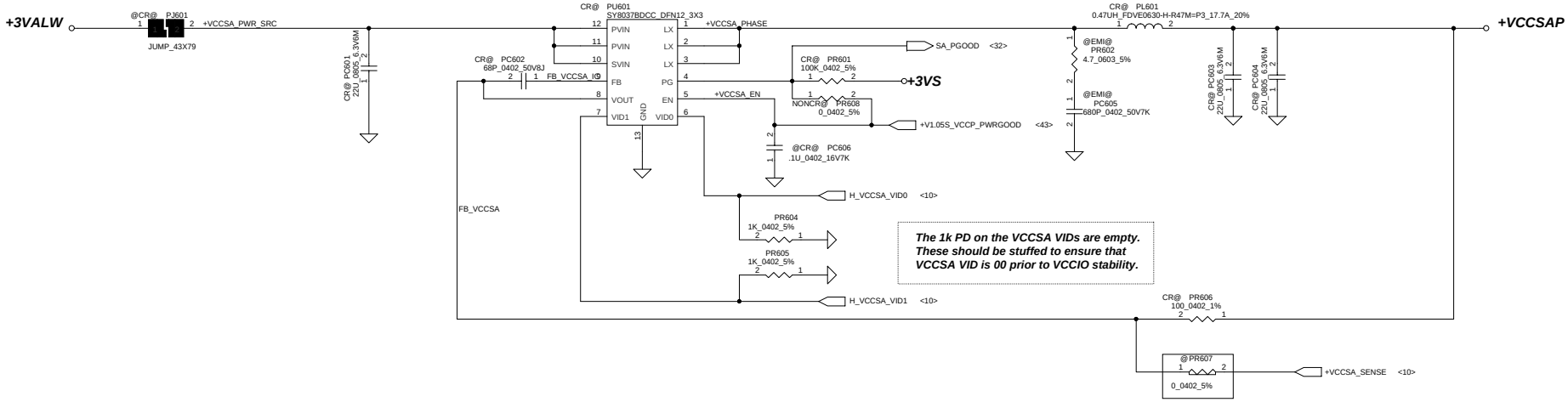
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network





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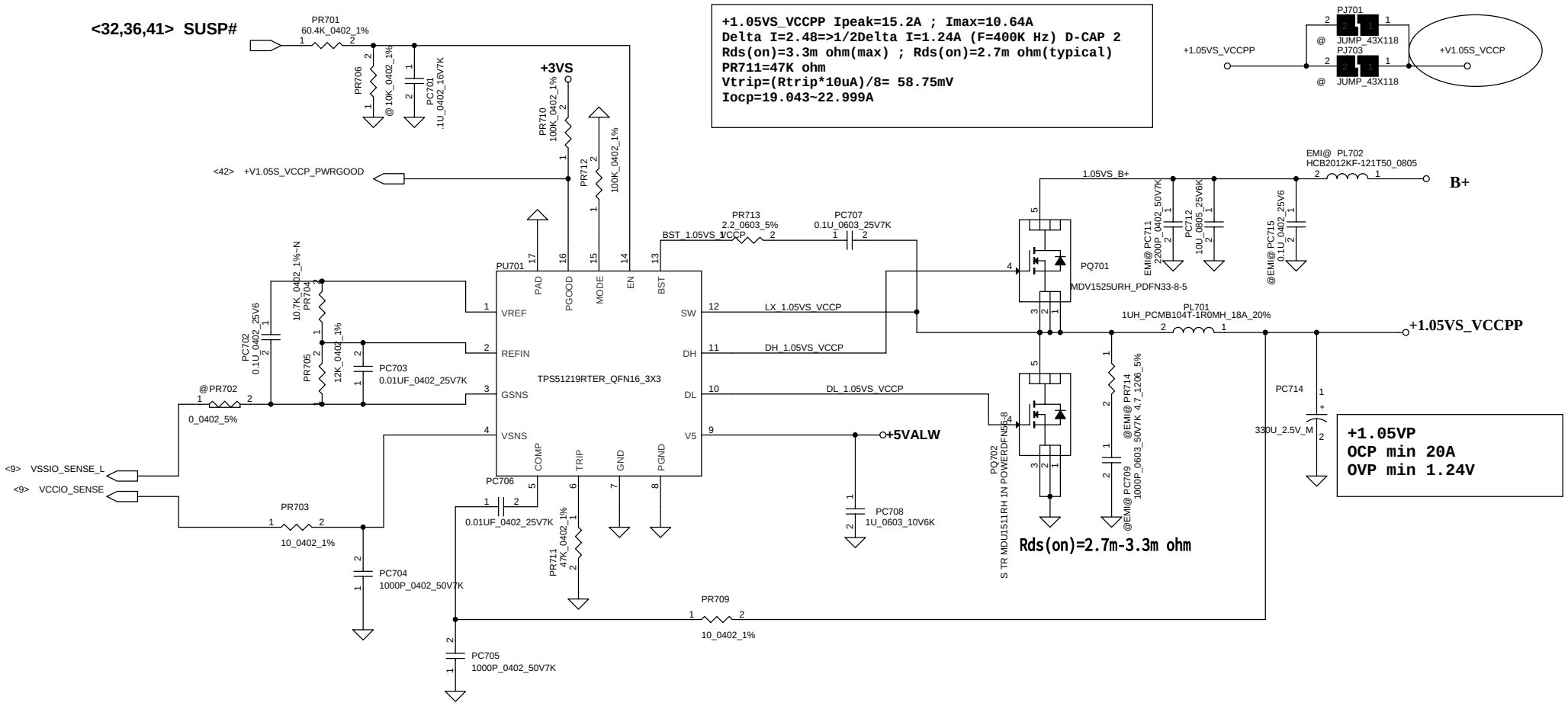

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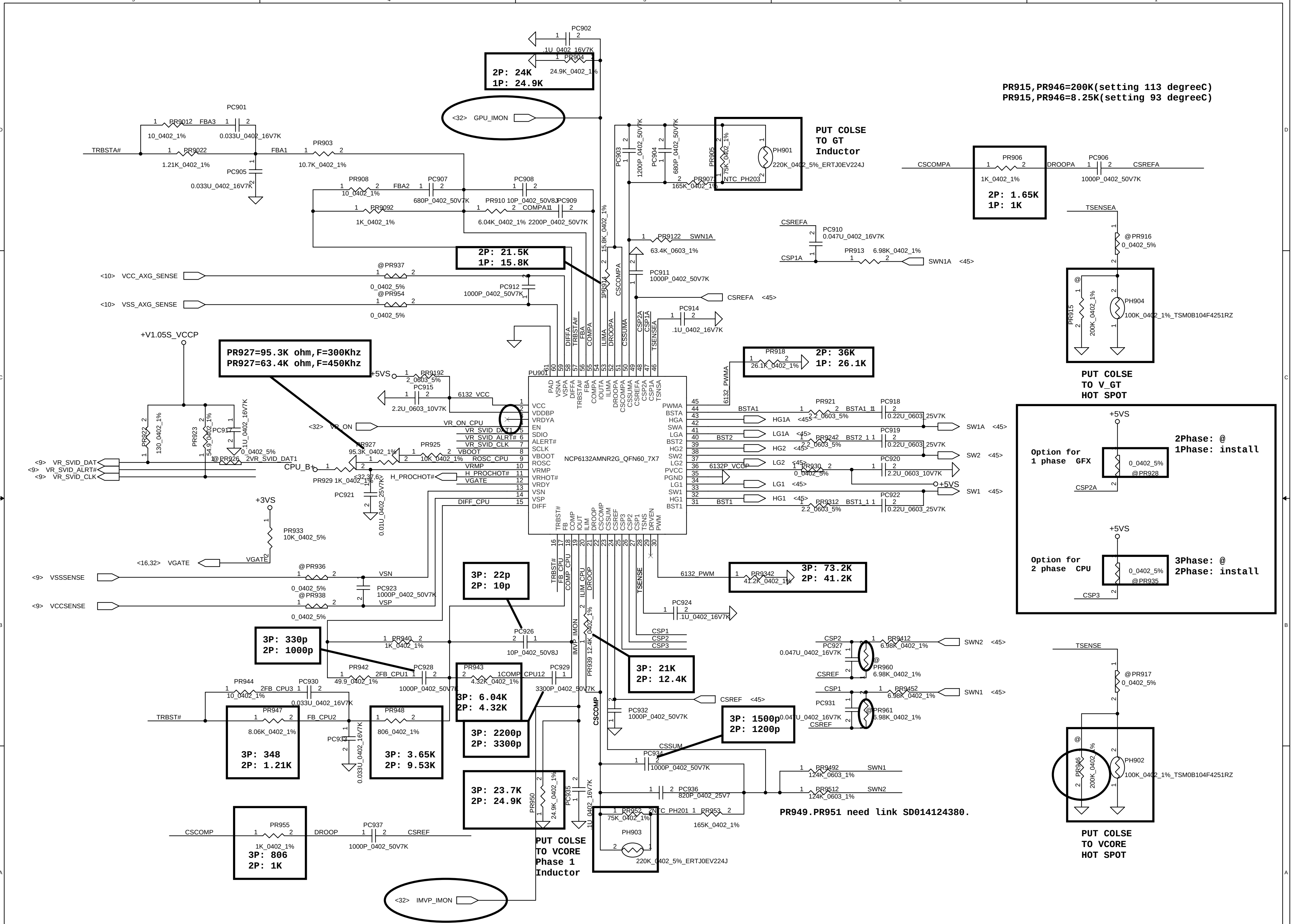

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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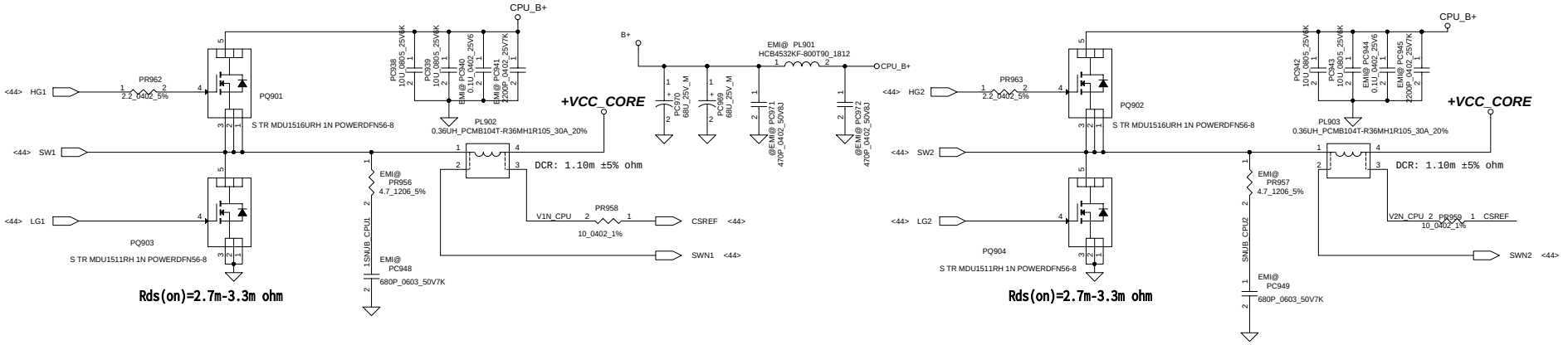
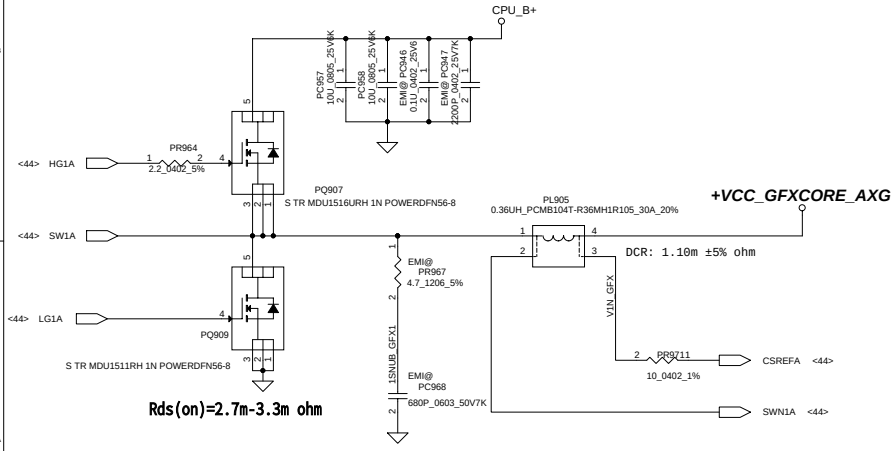


QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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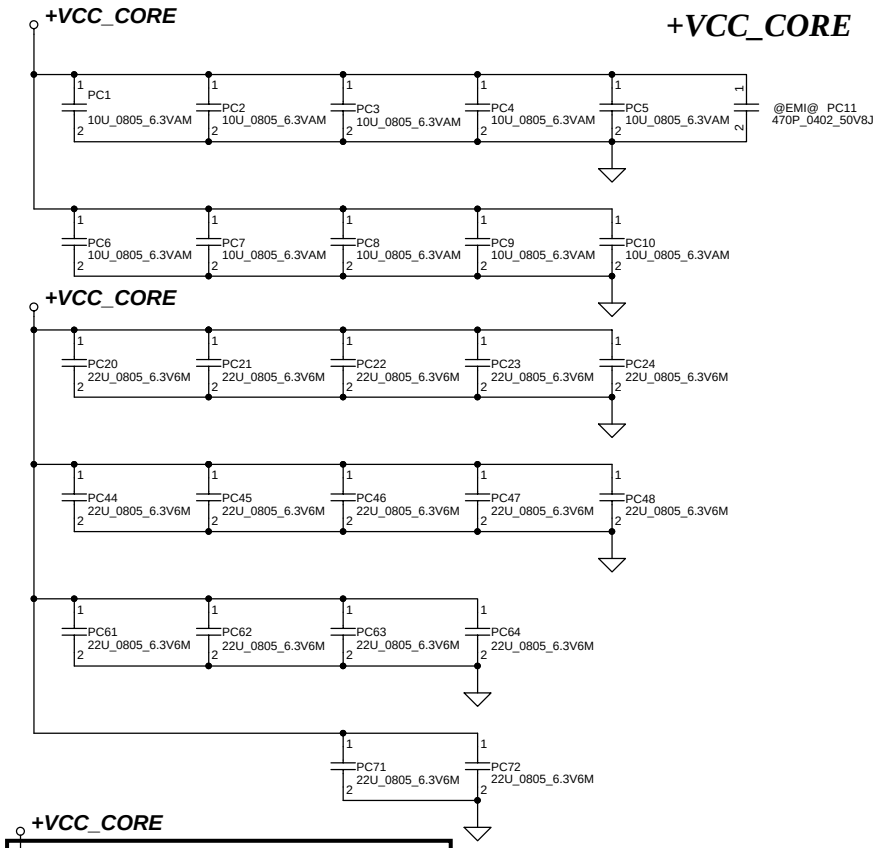
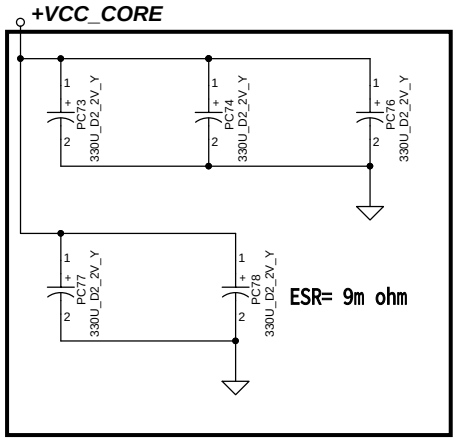
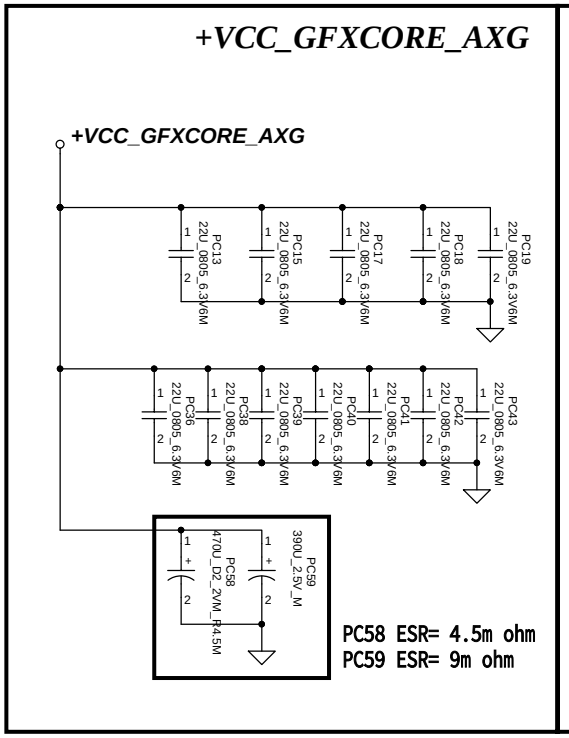
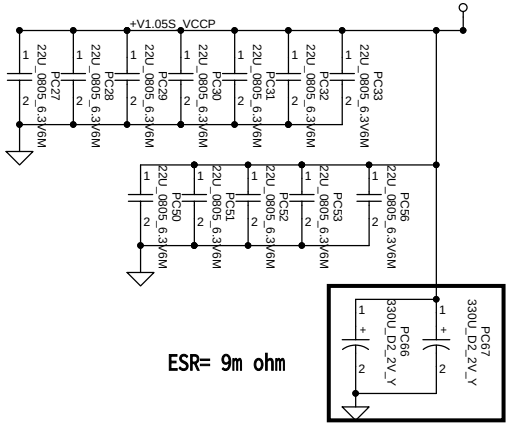






Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Design Change of IC Package.	40	Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM)	2012/11/22	DVT
2	Design Change of IC Package.	40	Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM)	2012/11/22	DVT
3	Add ADP_ID Circuit.	37	Add PQ102 to SB00000EO10(S TR 2N7002KDW 2N SOT-363-6 PANJIT) Add PR111.PR112 to SD028100380(S RES 1/16W 100K +-5% 0402)	2012/12/03	DVT
4	Factory lack of material.	41	Change PC521 to SF000003H00(S_A-P_CAP 330U 2.5V M 6.3X4.2 LESR16M SL)	2012/12/06	DVT
5	Factory lack of material.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2012/12/06	DVT
6	EMI request adjust +3VALWP/+5VALWP snubber function.	40	Change @PR404.@PC415.@PR406.@PC429 to PR404.PC415.PR406.PC429.	2012/12/06	DVT
7	EMI request adjust +3VALWP/+5VALWP boost resistor.	40	Change PR401.PR405 to SD013220B80(S RES 1/10W 2.2 +-5% 0603).	2012/12/06	DVT
8	EMI request add bypass capacitor.	40	Add PC412.PC413.PC416.PC419 to SE001471J80(S CER CAP 470P 50V J NPO 0805 H0.6)	2012/12/06	DVT
9	EMI request adjust CPU/GFX CORE snubber function.	45	Change @PR956.@PC948.@PR957.@PC949.@PR967.@PC968 to PR956.PC948.PR957.PC949.PR967.PC968.	2012/12/06	DVT
10	EMI request adjust bypass capacitor.	45	Change @PC940 to PC940.	2012/12/06	DVT
11	EMI request add bypass capacitor.	45	Add PC944.PC946 to SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PC945.PC947 to SE075222K80(S CER CAP 2200P 25V K X7R 0402)	2012/12/06	DVT
12	Design Change of input capacitor.	40	Change PC420 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25) Add PC427 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25)	2012/12/07	DVT
13	Design Change of IC Application.	40	Add @PR409.@PR410 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC405 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC407 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/10	DVT
14	Design Change of IC Application.	44	Change PC936 to SE000008980(S CER CAP 820P 25V K X7R 0402) Change PC929 to SE074332K80(S CER CAP 3300P 50V K X7R 0402) Change PC926 to SE071100J80(S CER CAP 10P 50V J NPO 0402) Change PC928 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR943 to SD00000J280(S RES 1/16W 4.32K +-1% 0402) Change PR949.PR951 to SD014124380(S RES 1/10W 124K +-1% 0603 YAGEO)	2012/12/17	DVT
15	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000NM00(S COIL 0.22UH +-20% PCMB104T-R22MS 35A)	2012/12/21	DVT
16	Design Change of VCCSA(LDO).	42	Delete PC607.PC608.PC609.PC610.PC611.PC612.PC613.PC614.PJ603.PJ604.PR608.PR609.PR610.PR611.PU602	2012/12/21	DVT
17	Reduction Part Count.	37	Delete PR110.	2013/01/18	PVT
18	Reduction Part Count.	42	Delete PR603.	2013/01/18	PVT
19	Reduction Part Count.	44	Delete PC916.	2013/01/18	PVT
20	Design Change of IC Application.	40	Change @PC405.@PR490.@PC407.@PR410 to PC405.PR490.PC407.PR410. Change PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT

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Item	Reason for change	PG#	Modify List	Date	Phase
21	Reduction Part Count.	41	Change PR505.PR516 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR503 to SD013000080(S RES 1/10W 0 +-5% 0603)	2013/01/18	PVT
22	Design Change of Thermal Application.	41	Change PC521 to SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2013/01/18	PVT
23	Reduction Part Count.	43	Change PR702 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
24	Reduction Part Count.	44	Change PR926.PR916.PR917 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
25	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2013/01/18	PVT
26	Design Change of CPU/GFX CORE Frequence.	44	Change PR927 to SD034953280(S RES 1/16W 95.3K +-1% 0402)	2013/01/18	PVT
27	Factory lack of material.	40	Change PC420.PC427 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	2013/01/18	PVT
28	Reduction Part Count.	40	Delete PR411.	2013/01/21	PVT
29	Design Change of Power Circuit Application.	38	Change PC208 to SE000003J80(S CER CAP 0.068U 16V K X7R 0402)	2013/01/23	PVT
30	Design Change of Power Circuit Application.	39	Add PR328 to SD028100280(S RES 1/16W 0 +-5% 0402) Add PQ314 to SB000009Q80(S TR 2N7002KW 1N SOT323-3)	2013/01/23	PVT
31	Design Change of Power Circuit Application.	40	Change PC405 to SE072103Z80(S CER CAP .01U 25V Z Y5V 0402) Change PC407 to SE075682K80(S CER CAP 6800P 25V K X7R 0402)	2013/03/04	PVT
32	Design Change of Power Circuit Application.	42	Add PR608 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/03/14	Pre-MP

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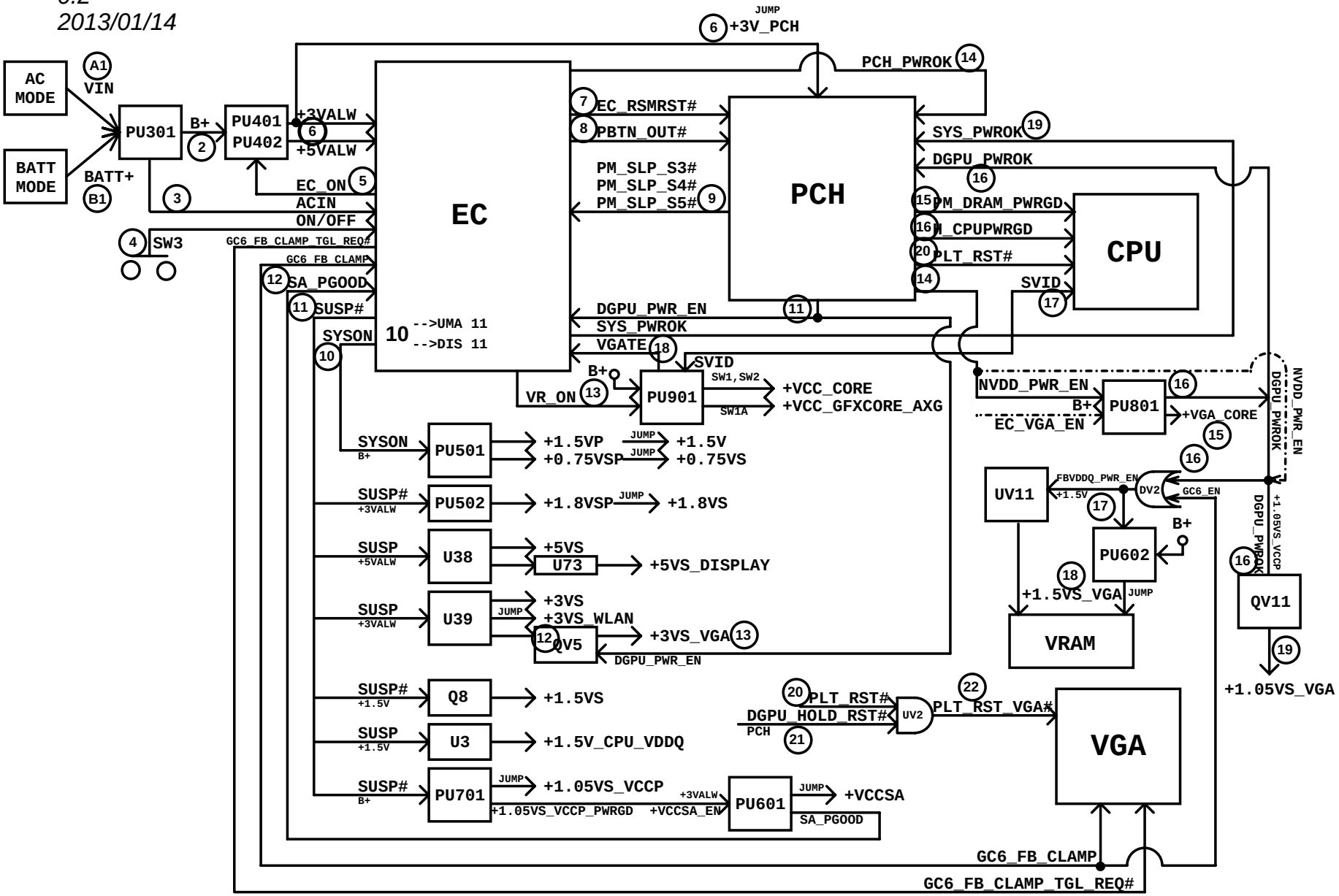
MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9901P*
REVISION: *0.2*
DATE: *2013/01/14*



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VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.5~11	Change footprint of JCPU1	For Lenovo rule
2	P.14	Add R406, R407, R408, R409	Reserve for improvement factory processes
3	P.42	Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
4	P.42	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
5	P.42	Reserve R410	Reserve Pull-high for GPIO use
6	P.42	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
7	P.42	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
8	P.42	Change ENBKL from EC Pin.73 to EC Pin.76	For common design
9	P.42	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
10	P.42	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
11	P.34	Add R411, R412, C411, C412	Reserve for EMI
12	P.20	Add Q21, R40, C237, Q22,R418, C243,C252,R413	Reserve for power consumption
13	P.25	Del Q12/R806	For Change Audio Jack type from Normal close to Normal open

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VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			DVT TO PVT
1	P.26	Reserve R508	For leakage current issue of Atheros WLAN
2	P.31	Change RA22 to reserve	For PC Beep issue(can't heard sound of "di" on BIOS setup menu)
3	P.31	Reserve RA10/RA11	For solve Codec speaker Hum noise issue(Zizi)
4	P.32	Reserve R416	Reserve +3VLP power rail to EC
5	P.32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC
6	P.32	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC
7	P.14	Change U5 from 4MB to 8MB ROM	Follow common design
			PVT TO Pre-MP
1	P.32	Chagne R416 to shortpad	
2	P.42	Reserve +1.05S_VCCP_PWRGOOD of +V1.05S_VCCP to connect to SA_PGOOD	For Celeron/Pentium CPU

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45					
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