UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CR:Chief River
V: V-Series installed

<Core Design>

緯創資通
Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title: **Cover Page**		
Size: A4	Document Number: **LA480**	Rev: SD
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Block Diagram (UMA/Optimus co-lay)

	LA480	LA580
Project Code	91.4TD01.001	91.4TE01.001
PCB P/N	11264	11273
Revision	SC	SC

##OnMainBoard

VRAM 2GB/1GB/512MB 88,89,90,91

DDR3 800MHz

NVIDIA N13P-GL (V) N13M-GE1 (B) 83.84,85,86,87

PCIe x 16 (Discrete only)

Intel CPU IVY Bridge DDRIII: 1066/1333/1600 MHz 4,5,6,7,8,9,10

DDRIII 1066/1333/1600 Channel A

DDRIII 1066/1333/1600 Channel B

DDRIII Slot 0 1066/1333/1600 14

DDRIII Slot 1 1066/1333/1600 15

FDI x 4 x 2 (UMA only)

DMI x 4

71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

HDMI 51

LCD 49

CRT 50

HDMI

LVDS

RGB CRT

Intel PCH Panther Point

USB 3.0/2.0 ports (14)
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25

PCIE x 1

GLAN REALTEK RTL8111F 33

RJ45 CONN 59

PCIE x 1/USB2.0 x 1

Mini-Card WLAN 65

SATA x 1/USB2.0 x 1

Mini-Card 66

USB 3.0 x 2

USB x 2

USB 2.0 x 2

USB x 2

Bluetooth 63

CAMERA 49

Finger Print BD

Finger Print 64

USB2.0 x 3

SD/MMC+/MS/ MS Pro/xD 74

CardReader ALCOR AU6435B52

USB 2.0 x 1

AZALIA

SATA x 2

HDD 56

ODD 56

(V only) Internal DMIC

(B only) Analog DMIC

Combo Jack

Azalia CODEC REALTEK ALC269Q-VC2 29

2CH SPEAKER

SPI

Flash ROM 8MB 60

LPC Bus

LPC debug port 71

KBC NUVOTON NPCE885G 27

SMBus

G-Sensor (V only) 79

Touch PAD 69

Int. KB 69

Thermal EMC2103-2-AP 28

Fan 28

CPU DC/DC TPS51640 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207M 46	
INPUTS	OUTPUTS
DCBATOUT	0D75V_S0 1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA TPS51728 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Chief River Schematic Checklist Rev0.72

Fin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table

port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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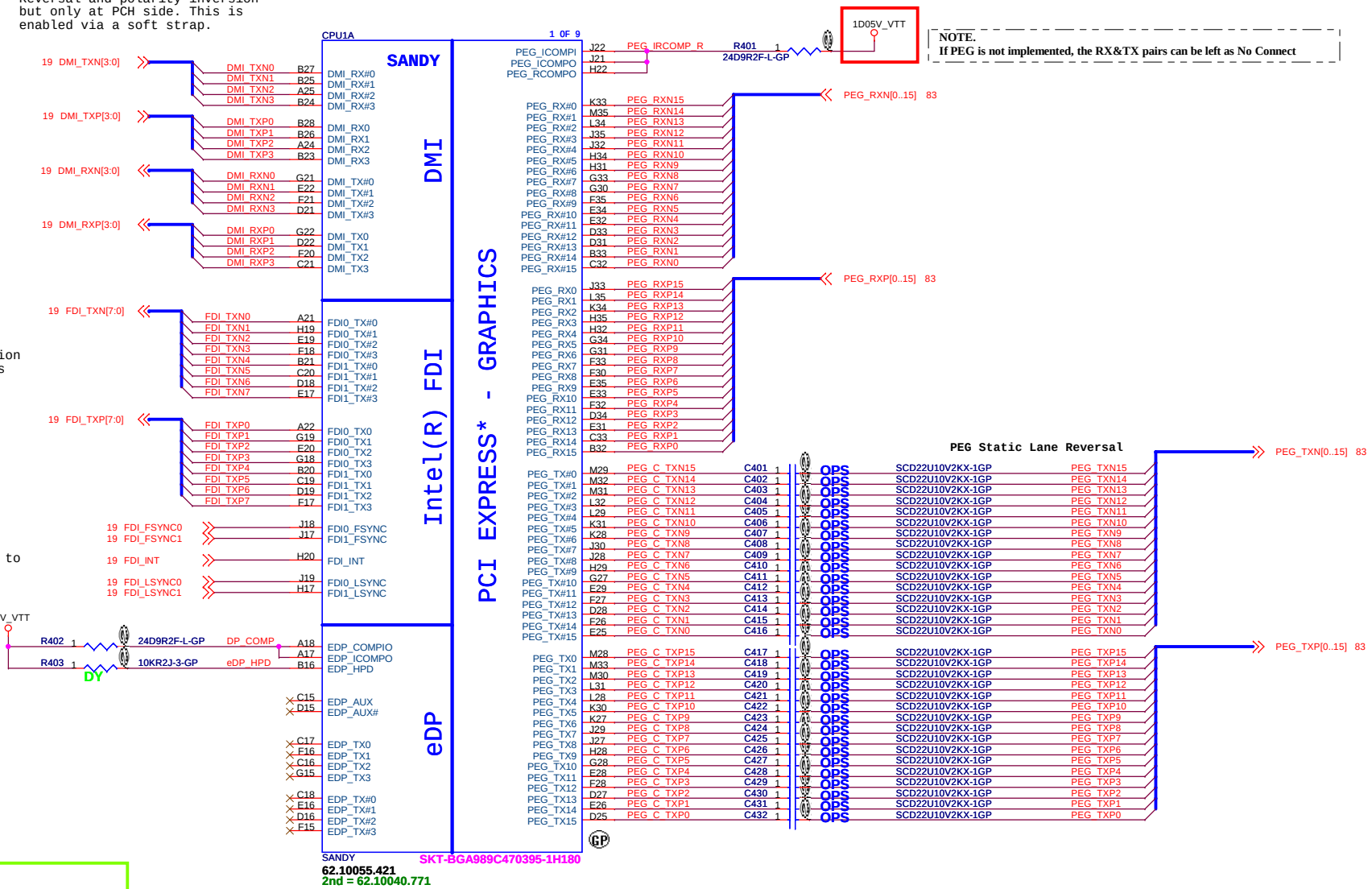
SSID = CPU

01.00IVY.000 IVY BRIDGE ORCAD SYMBOL.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Core Design>

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Title: **CPU (PCIE/DMI/FDI)**

Size	Document Number	Rev
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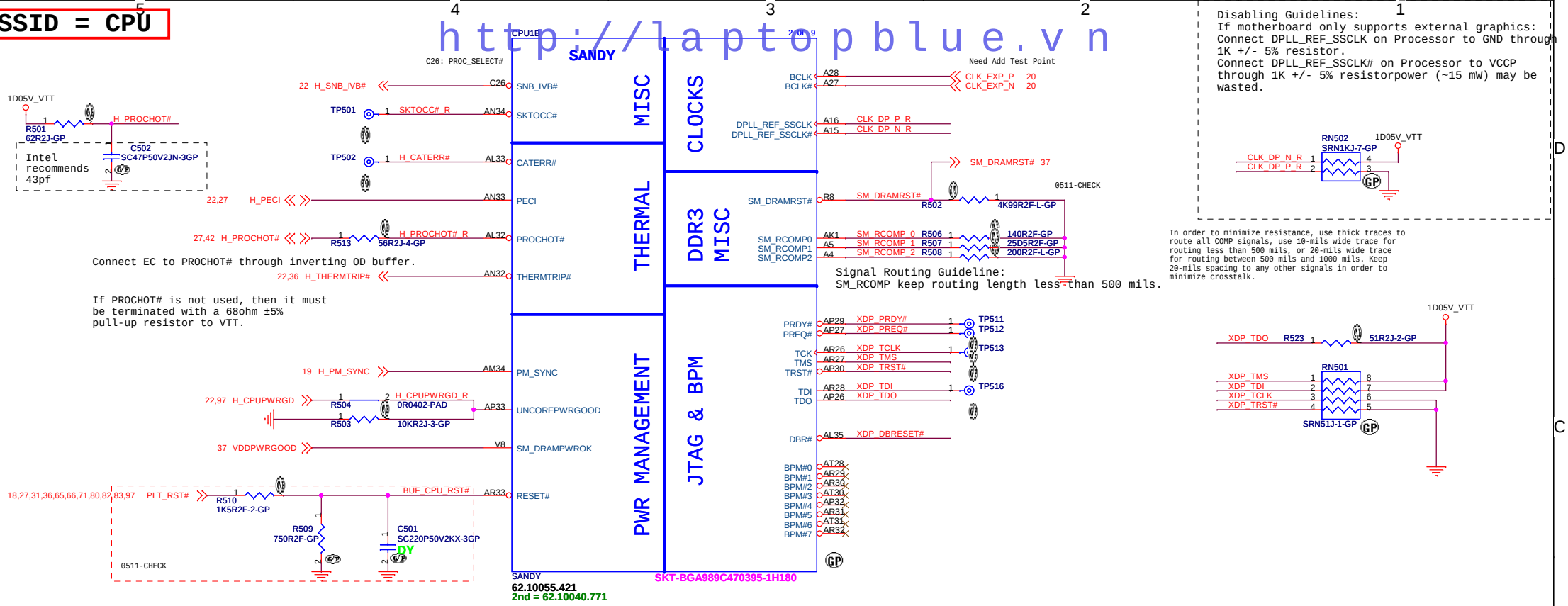
SSID = CPU



1D05V_VTT
R501 62R2J-GP
H_PROCHOT#
C502 SC47P50V2JN-3GP
Intel recommends 43pf

TP501 SKTOCC#_R
TP502 H_CATERR#
22,27 H_PECI
27,42 H_PROCHOT# R513 56R2J-4-GP H_PROCHOT#_R
22,36 H_THERMTRIP#

Connect EC to PROCHOT# through inverting OD buffer.

If PROCHOT# is not used, then it must be terminated with a 68ohm ±5% pull-up resistor to VTT.

19 H_PM_SYNC
22,97 H_CPUPWRGD R504 0R0402-PAD H_CPUPWRGD_R
R503 10KR2J-3-GP
37 VDDPWRGOOD

18,27,31,36,65,66,71,80,82,83,97 PLT_RST#
R510 1K5R2F-2-GP
BUF_CPU_RST#
R509 750R2F-GP
C501 SC220P50V2KX-3GP DY
0511-CHECK

SM_DRAMRST# 37
R502 4K99R2F-L-GP
SM_RCOMP_0 R506
SM_RCOMP_1 R507
SM_RCOMP_2 R508

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

RN502 SRN1KJ-7-GP 1D05V_VTT
CLK_DP_N_R
CLK_DP_P_R

In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.

1D05V_VTT
XDP_TDO R523 51R2J-2-GP
RN501 SRN51J-1-GP
XDP_TMS
XDP_TDI
XDP_TCLK
XDP_TRST#

3D3V_S0
19 XDP_DBRESET# R516 1KR2J-1-GP

DEL U501
DEL R519
DEL C503
DEL R517
DEL R515

ASM R510
ASM R509

62.10055.421
2nd = 62.10040.771

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: CPU (THERMAL/CLOCK/PM)
Size: A3
Document Number: LA480
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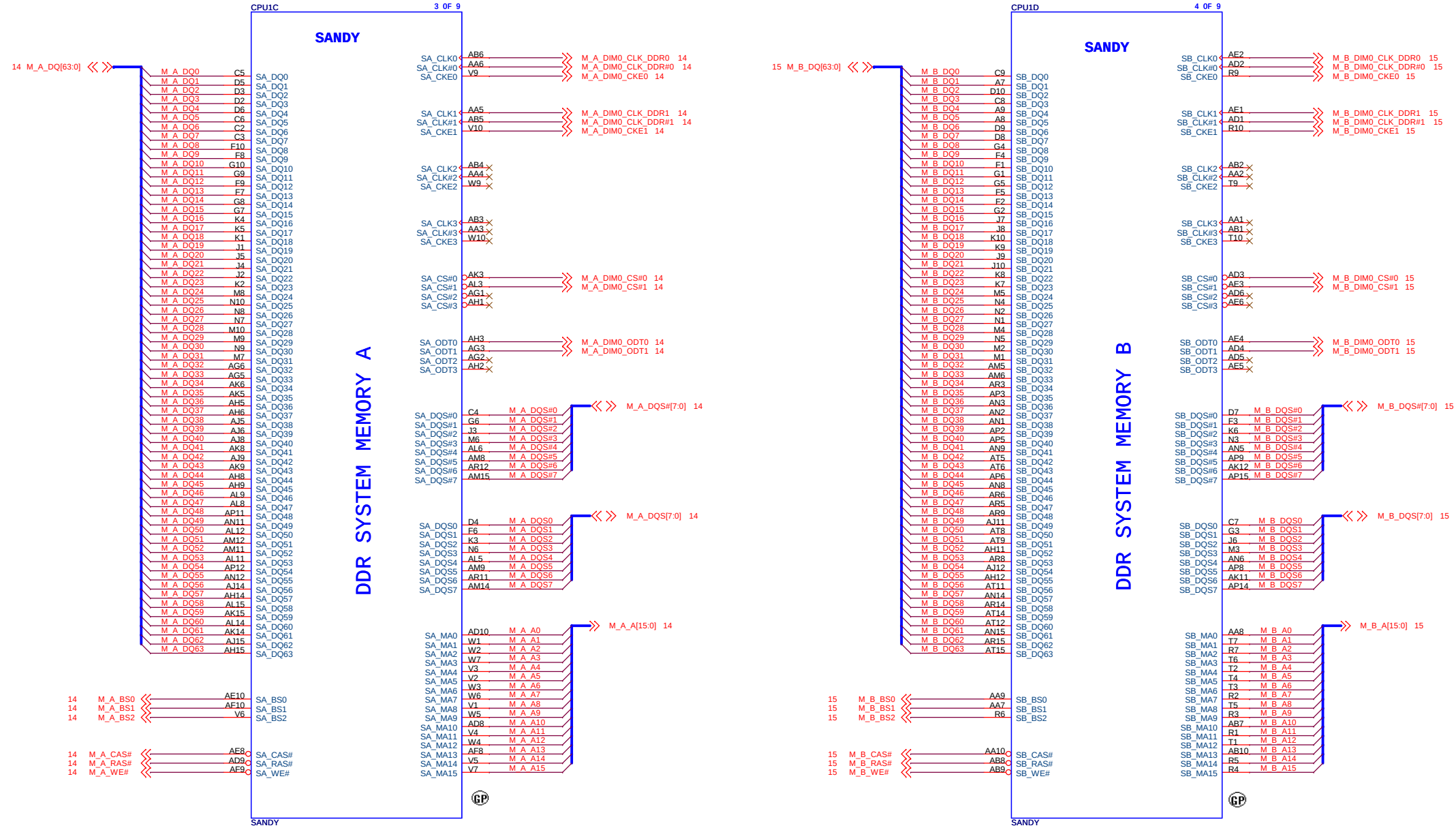
SSID = CPU



<Core Design>

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Title	CPU (DDR)	
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SSID = CPU

CFG2

R702 1KR2J-1-GP

OPS

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

CFG4

R703 1KR2J-1-GP

DY

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG5

CFG6

R701 1KR2J-1-GP DY

R704 1KR2J-1-GP DY

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG7

R705 1KR2J-1-GP DY

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CPU1E

5 OF 9

SANDY

RESERVED

TP717 CFG0 AK28 CFG0

TP702 CFG1 AK29 CFG1

CFG2 AL26 CFG2

TP703 CFG3 AL27 CFG3

CFG4 AK26 CFG4

CFG5 AL29 CFG5

CFG6 AL30 CFG6

CFG7 AM31 CFG7

AM32 CFG8

AM30 CFG9

AM28 CFG10

AM26 CFG11

AN28 CFG12

AN31 CFG13

AN26 CFG14

AM27 CFG15

TP704 CFG16 AK31 CFG16

AN29 CFG17

RSVD#L7 L7

RSVD#AG7 AG7

RSVD#AE7 AE7

RSVD#AK2 AK2

RSVD#W8 W8

RSVD#AT26 AT26

RSVD#AM33 AM33

RSVD#AJ27 AJ27

RSVD#T8 T8

RSVD#J16 J16

RSVD#H16 H16

RSVD#G16 G16

AJ31 RSVD#AJ31

AH31 RSVD#AH31

AJ33 RSVD#AJ33

AH33 RSVD#AH33

RSVD#AR35 AR35

RSVD#AT34 AT34

RSVD#AT33 AT33

RSVD#AP35 AP35

RSVD#AR34 AR34

AJ26 RSVD#AJ26

12 DDR_WR_VREF01 B4 RSVD#B4

12 DDR_WR_VREF02 D1 RSVD#D1

RSVD#B34 B34

RSVD#A33 A33

RSVD#A34 A34

RSVD#B35 B35

RSVD#C35 C35

F25 RSVD#F25

F24 RSVD#F24

F23 RSVD#F23

D24 RSVD#D24

G25 RSVD#G25

G24 RSVD#G24

F23 RSVD#E23

D23 RSVD#D23

C30 RSVD#C30

A31 RSVD#A31

B30 RSVD#B30

B29 RSVD#B29

D30 RSVD#D30

B31 RSVD#B31

A30 RSVD#A30

C29 RSVD#C29

RSVD#AJ32 AJ32

RSVD#AK32 AK32

RSVD#AH27 AH27 TP713 TP720

RSVD#AN35 AN35 CLK_XDP_ITP_P TP718

RSVD#AM35 AM35 CLK_XDP_ITP_N TP719

TP705 H_VCCP_SEL J20 RSVD#J20

B18 RSVD#B18

A19 RSVD#A19

RSVD#AT2 AT2

RSVD#AT1 AT1

RSVD#AR1 AR1

J15 RSVD#J15

SANDY SKT-BGA989C470395-1H180

62.10055.421

2nd = 62.10040.771

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POWER

0511-CHECK CAP.

VCC CORE:53A

VCC_CORE

C801 SC10U6D3V5KX-1GP
C802 SC10U6D3V5KX-1GP DY
C803 SC10U6D3V5KX-1GP
C804 SC10U6D3V5KX-1GP DY
C811 SC10U6D3V5KX-1GP

C815 SC10U6D3V5KX-1GP
C817 SC10U6D3V5KX-1GP
C818 SC10U6D3V5KX-1GP
C819 SC10U6D3V5KX-1GP
C820 SC10U6D3V5KX-1GP

C816 SC10U6D3V5KX-1GP
C821 SC10U6D3V5KX-1GP
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP DY
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP

C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 SC10U6D3V5KX-1GP DY
C831 SC10U6D3V5KX-1GP
C828 SC10U6D3V5KX-1GP

CPU1F

SANDY

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

0511-CHECK CAP.

VCCIO:8.5A

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

VCCIO: J23

0511-CHECK
1D05V_VTT

C805 SC10U6D3V5KX-1GP
C806 SC10U6D3V5KX-1GP
C807 SC10U6D3V5KX-1GP
C808 SC10U6D3V5KX-1GP
C809 SC10U6D3V5KX-1GP
C810 SC10U6D3V5KX-1GP
C838 SC10U6D3V5KX-1GP
C839 SC10U6D3V5KX-1GP
C840 SC10U6D3V5KX-1GP DY
C841 SC10U6D3V5KX-1GP

Reserve C846 & C847

1D05V_VTT

C812 SC10U6D3V5KX-1GP
C813 SC10U6D3V5KX-1GP
C814 SC10U6D3V5KX-1GP
C829 SC10U6D3V5KX-1GP
C830 SC10U6D3V5KX-1GP
C842 SC10U6D3V5KX-1GP
C843 SC10U6D3V5KX-1GP
C844 SC10U6D3V5KX-1GP DY
C845 SC10U6D3V5KX-1GP

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

R807 75R2F-2-GP 1D05V_VTT
R803 43R2J-GP
VR_SVID_ALERT# 42
H_CPU_SVIDCLK 42
H_CPU_SVIDDAT 42
R804 130R2F-1-GP 1D05V_VTT
0511-CHECK

check
Place neer PCU pin.
1D05V_VTT
R808 10R2F-L-GP
VCCIO_SENSE
VSSIO_SENSE
R809 10R2F-L-GP

VCC_CORE
R801 100R2F-L1-GP-U
VCC_SENSE AJ35
VSS_SENSE AJ34
VCCSENSE 42
VSSSENSE 42
R802 100R2F-L1-GP-U
VCCIO_SENSE B10
VSSIO_SENSE A10
VCCIO_SENSE 45
VSSIO_SENSE 45

SANDY
62.10055.421
2nd = 62.10040.771

<Core Design>

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POWER

0511-CHECK CAP

VCC_GFXCORE

PROCESSOR VAXG: 24A

0511-CHECK

C901 C902 C903 C904 C905 C906 RC901 — SC10U6D3V5KX-1GP, SC33P50V2JN-3GP, DY

C907 C908 C918 C919 C920 C921 RC902 — SC10U6D3V5KX-1GP, SC33P50V2JN-3GP, DY

CPU1G — 7 OF 9 — SANDY

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

SANDY

GRAPHICS

SENSE LINES

VAXG_SENSE — AK35 — VCC_AXG_SENSE 42

VSSAXG_SENSE — AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF — AL1 — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

VDDQ:5A

1D5V_S0

VDDQ — AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP, DY

SA RAIL

VCCA:6A

VCCSA

C916 C915 C917 — SC10U6D3V5KX-1GP

VCCSA — M27 M26 L26 J26 J25 J24 H26 H25

+V0.85S - VCCSA - System Agent rail voltage can be
[0.9, 0.725, 0.8, 0.675] V for IVB
[0.9, 0.8] V for SNB

1.8V RAIL

1D8V_S0

VCCPLL:1.2A

C926 C923 C922 C924 — SC10U6D3V5KX-1GP, SC1U10V2KX-1GP

VCCPLL — B6 A6 A2

MISC

VCCSA_SENSE — H23 — VCCSA_SENSE 48

FC_C22 — C22
VCCSA_VID1 — C24

VCCSA_SELECT0 48
VCCSA_SELECT1 48

RN901 SRN1KJ-7-GP

SANDY
62.10055.421
2nd = 62.10040.771

VCC_GFXCORE

R906 100R2F-L1-GP-U

VCC_AXG_SENSE
VSS_AXG_SENSE

R907 100R2F-L1-GP-U

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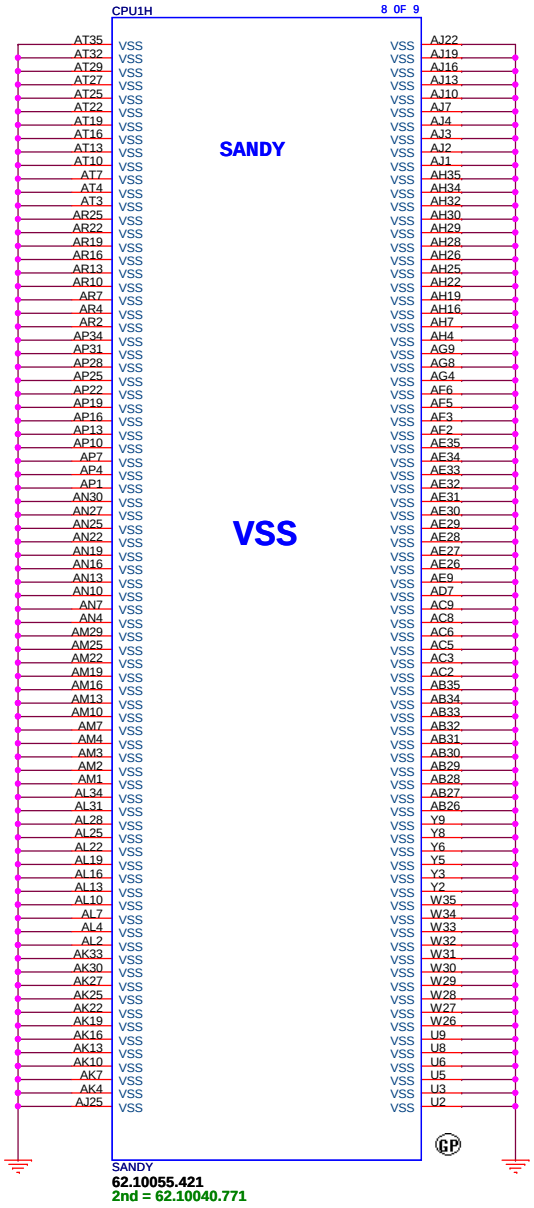
Title: **CPU (VCC_GFXCORE)**

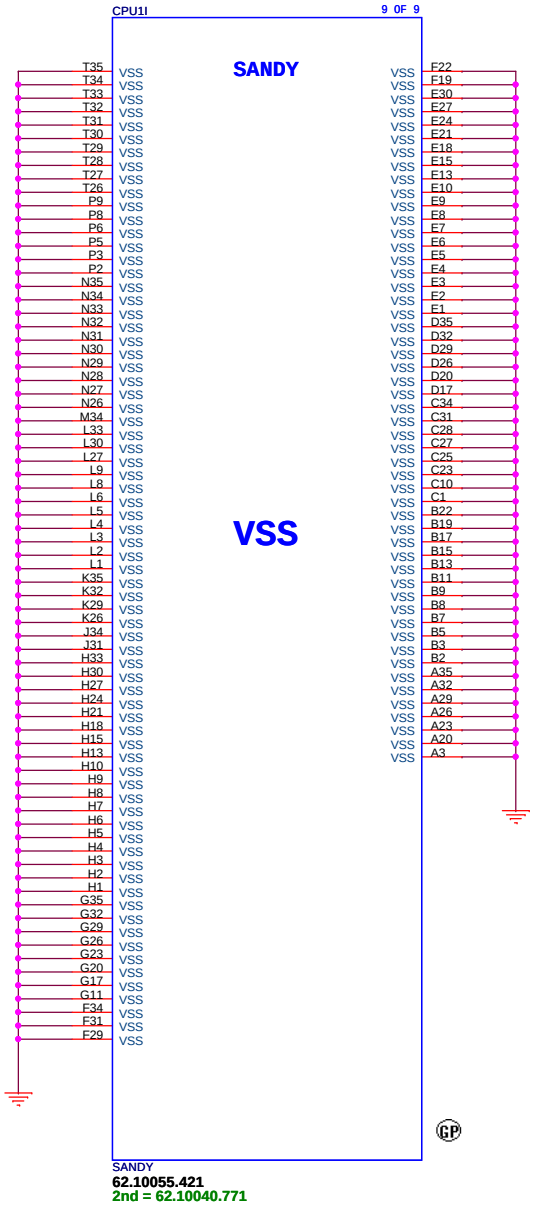
Size: A3 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 9 of 103

SSID = CPU

http://laptopblue.vn





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Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 10 of 103

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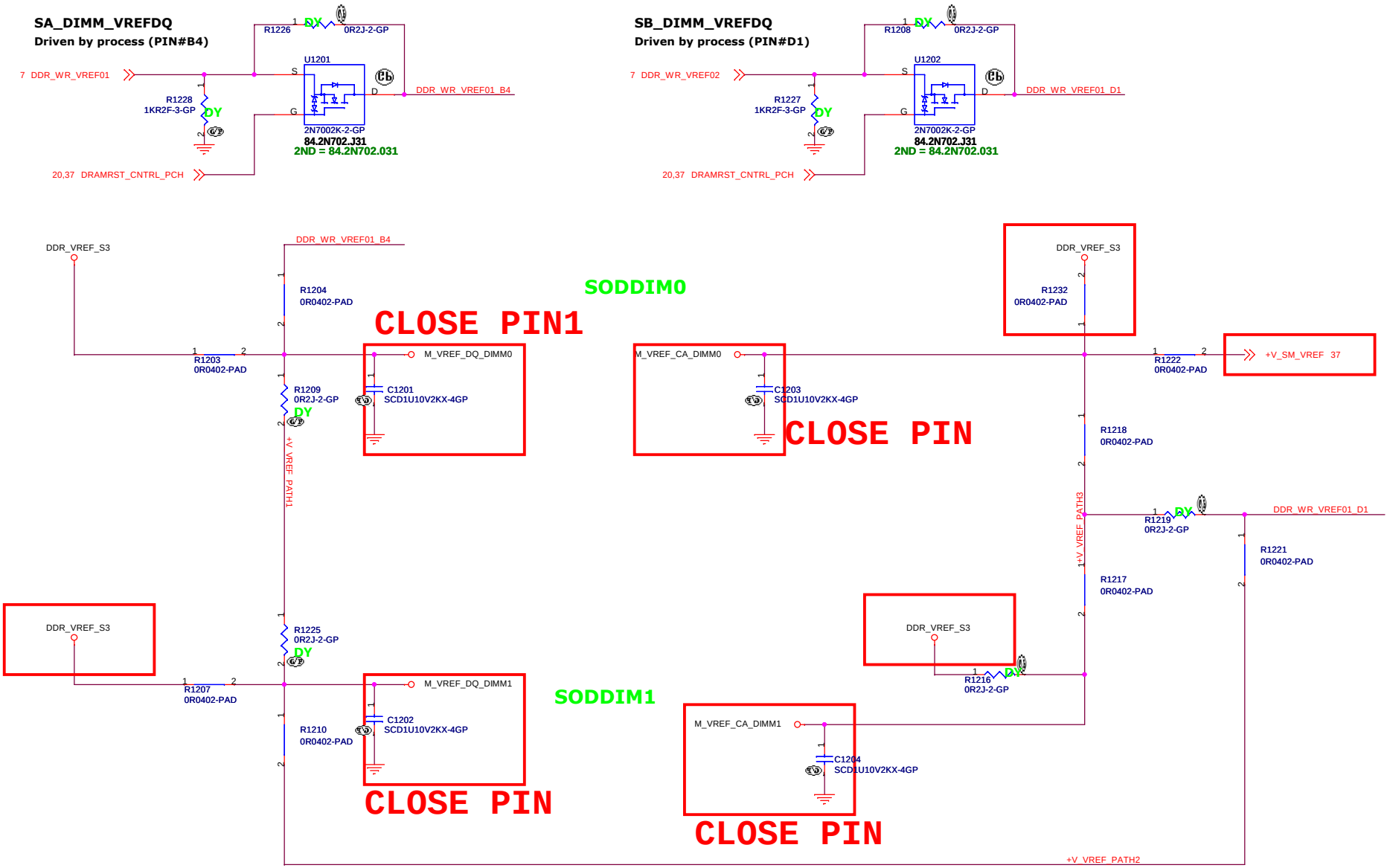
Title: <Title>		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 11 of 103	

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations is acceptable if required due to tight routing constraints.



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Title			
M3			
Size A3	Document Number LA480		Rev SD
Date: Friday, January 06, 2012	Sheet 12 of 103		

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Title: <Title>		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 13 of 103	

SSID = MEMORY

DIMM1

DDR3-204P-96-GP-U1
62.10017.V61

2ND = *62.10017.X51
3RD = *62.10017.V61
(H=8mm)

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

Place these caps close to VTT1 and VTT2.

<Core Design>
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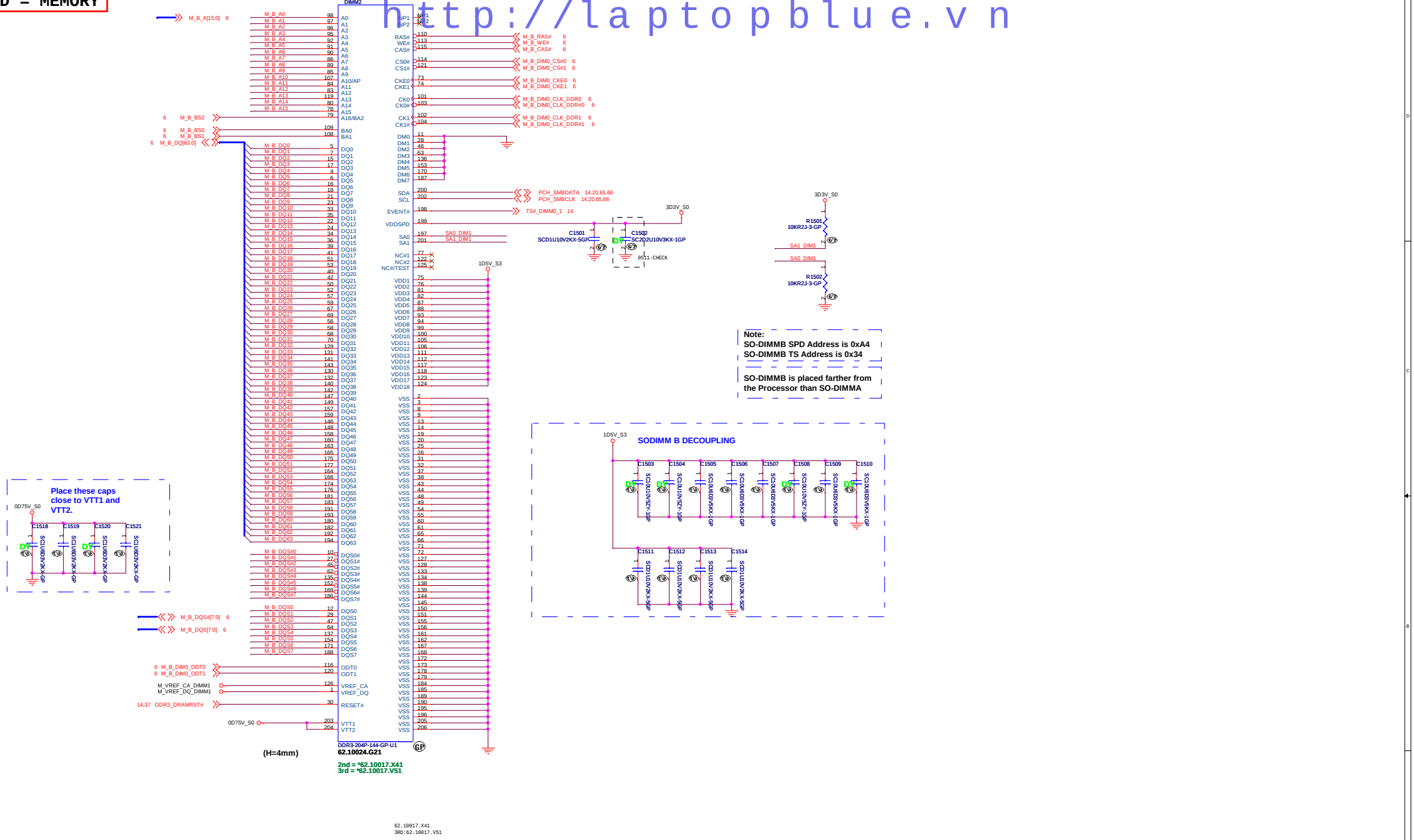
Title: DDR3-SODIMM1
Size: A2 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 14 of 103

SSID = MEMORY



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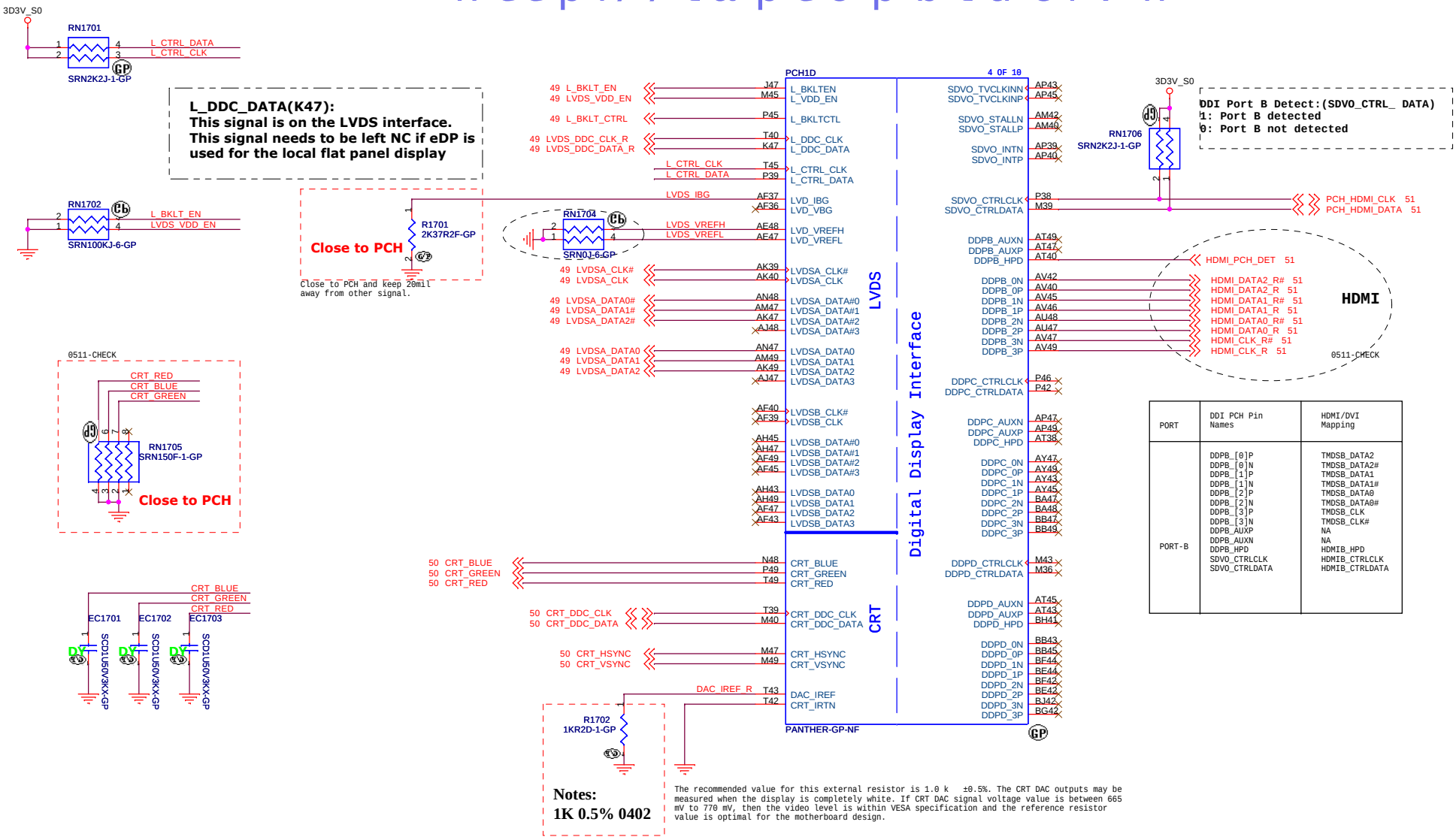
Title
DDR3-SODIMM2

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 16 of 103



PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_[0]P DDPB_[0]N DDPB_[1]P DDPB_[1]N DDPB_[2]P DDPB_[2]N DDPB_[3]P DDPB_[3]N DDPB_AUXP DDPB_AUXN DDPB_HPD SDVO_CTRLCLK SDVO_CTRLDATA	TMDSB_DATA2 TMDSB_DATA2# TMDSB_DATA1 TMDSB_DATA1# TMDSB_DATA0 TMDSB_DATA0# TMDSB_CLK TMDSB_CLK# NA NA HDMIB_HPD HDMIB_CTRLCLK HDMIB_CTRLDATA

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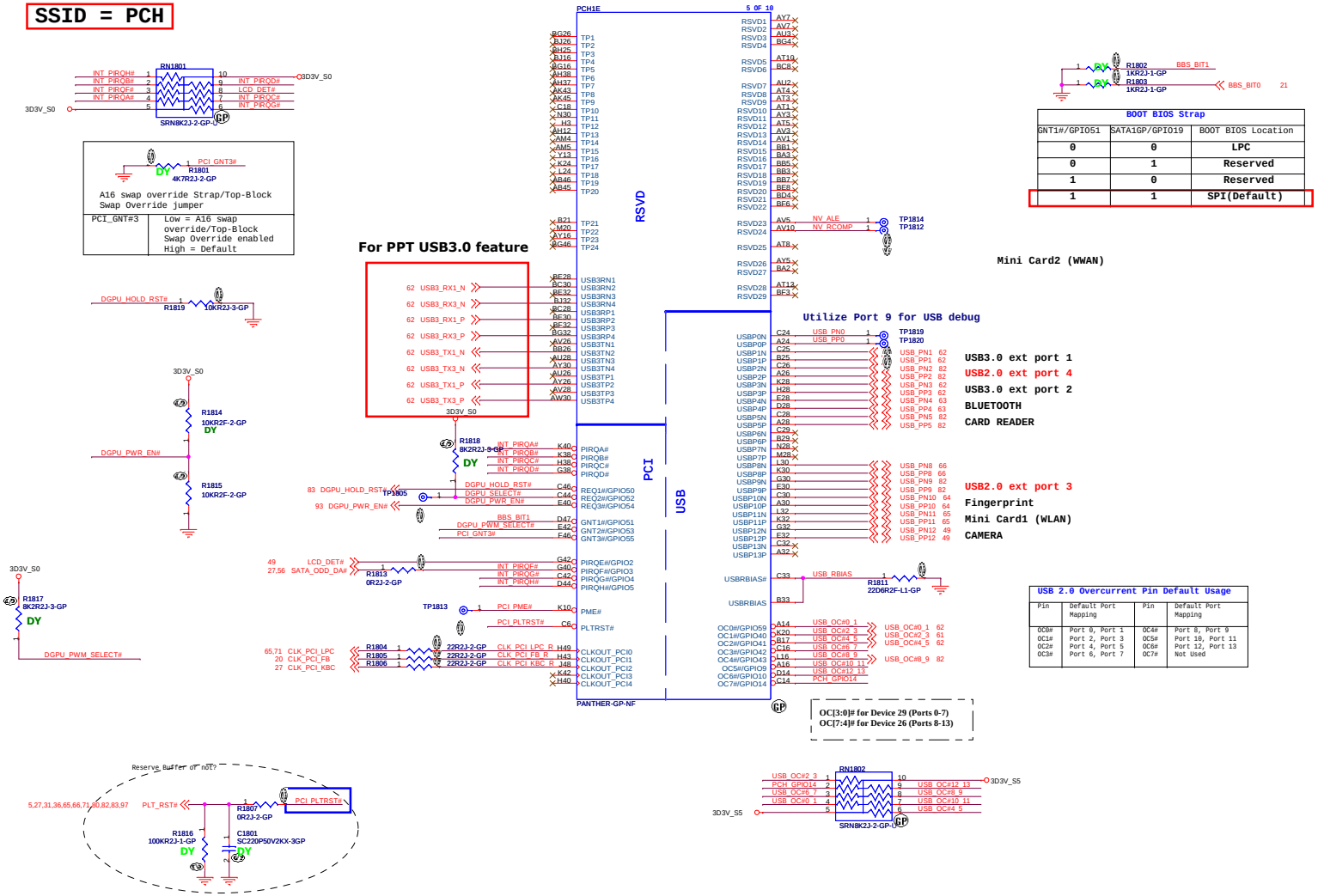
Title: PCH : LVDS/CRT/DDI

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 17 of 103

SSID = PCH



BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	CARD READER
6	X
7	X
8	3G
9	USB2.0, ext. port 3
10	Finger Print
11	Mini Card1 (WLAN)
12	CAMERA
13	X

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Title: PCH : PCI/USB/NVRAM/RSVD

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 18 of 103

SSID = PCH

For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10

DMI: DMI_RXN[3:0] → DMI_RXN0 BC24, DMI_RXN1 BE20, DMI_RXN2 BG18, DMI_RXN3 BG20
DMI: DMI_RXP[3:0] → DMI_RXP0 BE24, DMI_RXP1 BC20, DMI_RXP2 BJ18, DMI_RXP3 BJ20
DMI: DMI_TXN[3:0] → DMI_TXN0 AW24, DMI_TXN1 AW20, DMI_TXN2 BB18, DMI_TXN3 AV18
DMI: DMI_TXP[3:0] → DMI_TXP0 AY24, DMI_TXP1 AY20, DMI_TXP2 AV18, DMI_TXP3 AU18
DMI_ZCOMP BJ24 — R1901 49D9R2F-GP — DMI_COMP_R — BG25
DMI_IRCOMP — R1902 750R2F-GP — RBIAS_CPY — BH21

FDI: FDI_TXN[7:0] 4 → FDI_RXN0 BJ14, FDI_RXN1 AY14, FDI_RXN2 BE14, FDI_RXN3 BH13, FDI_RXN4 BC12, FDI_RXN5 BJ12, FDI_RXN6 BC10, FDI_RXN7 BG9
FDI: FDI_TXP[7:0] 4 → FDI_RXP0 BG14, FDI_RXP1 BB14, FDI_RXP2 BF14, FDI_RXP3 BG13, FDI_RXP4 BE12, FDI_RXP5 BG12, FDI_RXP6 BJ10, FDI_RXP7 BH9
FDI_INT AW16 → FDI_INT 4
FDI_FSYNC0 AV12 → FDI_FSYNC0 4
FDI_FSYNC1 BC10 → FDI_FSYNC1 4
FDI_LSYNC0 AV14 → FDI_LSYNC0 4
FDI_LSYNC1 BB10 → FDI_LSYNC1 4

System Power Management:
DSWVRMEN A18 ← DSWODVREN
DPWROK E22 ← PCH_DPWROK (R1992 0R0402-PAD, R1911 10KR2J-3-GP)
WAKE# B9 → PCIE_WAKE# 31,65,66
CLKRUN#/GPIO32 N3 → PM_CLKRUN# 27
SUS_STAT#/GPIO61 G8 → PM_SUS_STAT# → TP1901
SUSCLK/GPIO62 N14 ← SUS_CLK (R1913 0R0402-PAD) → PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 D10 → PM_SLP_S5# → TP1902
SLP_S4# H4 → PM_SLP_S4# 27,46,97
SLP_S3# F4 → PM_SLP_S3# 27,36,37,47
SLP_A# G10 → PM_SLP_A# 27,45
SLP_SUS# G16 → PM_SLP_SUS# → TP1904
PMSYNCH AP14 → H_PM_SYNC 5
SLP_LAN#/GPIO29 K14 → PM_SLP_LAN# → TP1905
SUSACK# C12 ← SUS_PWR_ACK (R1915 0R2J-2-GP)
SYS_RESET# K3 ← SYS_RESET# (R1916 0R0402-PAD) ← 5 XDP_DBRESET#
SYS_PWROK P12 ← SYS_PWROK (R1923 0R2J-2-GP) ← 36 SYS_PWROK
PWROK L22 ← PWROK (R1914 0R0402-PAD) ← 27 SO_PWR_GOOD
APWROK L10 ← MEPWROK (R1930 0R2J-2-GP Non-SBA; R1931 0R2J-2-GP SBA) ← 45 MPWROK
DRAMPWROK B13 ← 37 PM_DRAM_PWRGD
RSMRST# C21 ← PM_RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30 K16 ← SUS_PWR_ACK
PWRBTN# E20 ← PM_PWRBTN# 27,97
ACPRESENT/GPIO31 H20 ← AC_PRESENT 27
BATLOW#/GPIO72 E10 ← BATLOW#
RI# A10 ← PM_RI#
PANTHER-GP-NF

SUS_ACK#: For non-DWS platforms, this signal can be left unconnected. Due to the internal pull-up on this signal it will be pulled high in order for the boot sequence to proceed.

SYS_PWROK: the system is ready to start the exit from reset (de-asserts PLT_RST# to the processor)
PWROK: it indicates to PCH that its CORE well power is stable.
Active Sleep Well (ASW) Power OK
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

Platforms supporting Deep S4/S5, but not wake from S4/S5 to participate in the handshake during wake and Deep S4/S5 entry may tie SUSACK# to SUSWARN#.

SUSPWRDNACK : No longer requires a 10-K pull-up to VccSUS (3.3 V).

PCH_WAKE#
CRB : 1K
CHKLIST: 10K

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 330KR2J-L1-GP

3D3V_S0 — PM_CLKRUN# — R1919 8K2R2J-3-GP

This signal is used to control power planes to the IntelR ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP_A# will have the same timings as SLP_S3#.

For platforms supporting DEEP S4/S5 state, a low on this signal indicates that PCH is in Deep Sleep state and that EC/platform logic does not need to keep the Suspend Rails ON.
If high means EC must keep SUS rails ON.
If DEEP S4/S5 is not supported, then this pin can be left unconnected.

3D3V_S5 — RN1901 SRN10KJ-6-GP — BATLOW# / PM_RI# / SUS_PWR_ACK / PCIE_WAKE#
R1909 10KR2J-3-GP — AC_PRESENT
R1922 10KR2J-3-GP — PM_PWRBTN#
R1908 10KR2J-3-GP — PM_RSMRST#

3D3V_AUX_S5 — R1925 100KR2J-1-GP — R1924 10KR2J-3-GP — 3V_5V_POK # — Q1901 2N7002KDW-GP (84.2N702.A3F, 2nd = 84.DM601.03F) — PM_RSMRST# — R1921 1KR2J-1-GP — RSMRST#_KBC 27 / 3V_5V_POK 41

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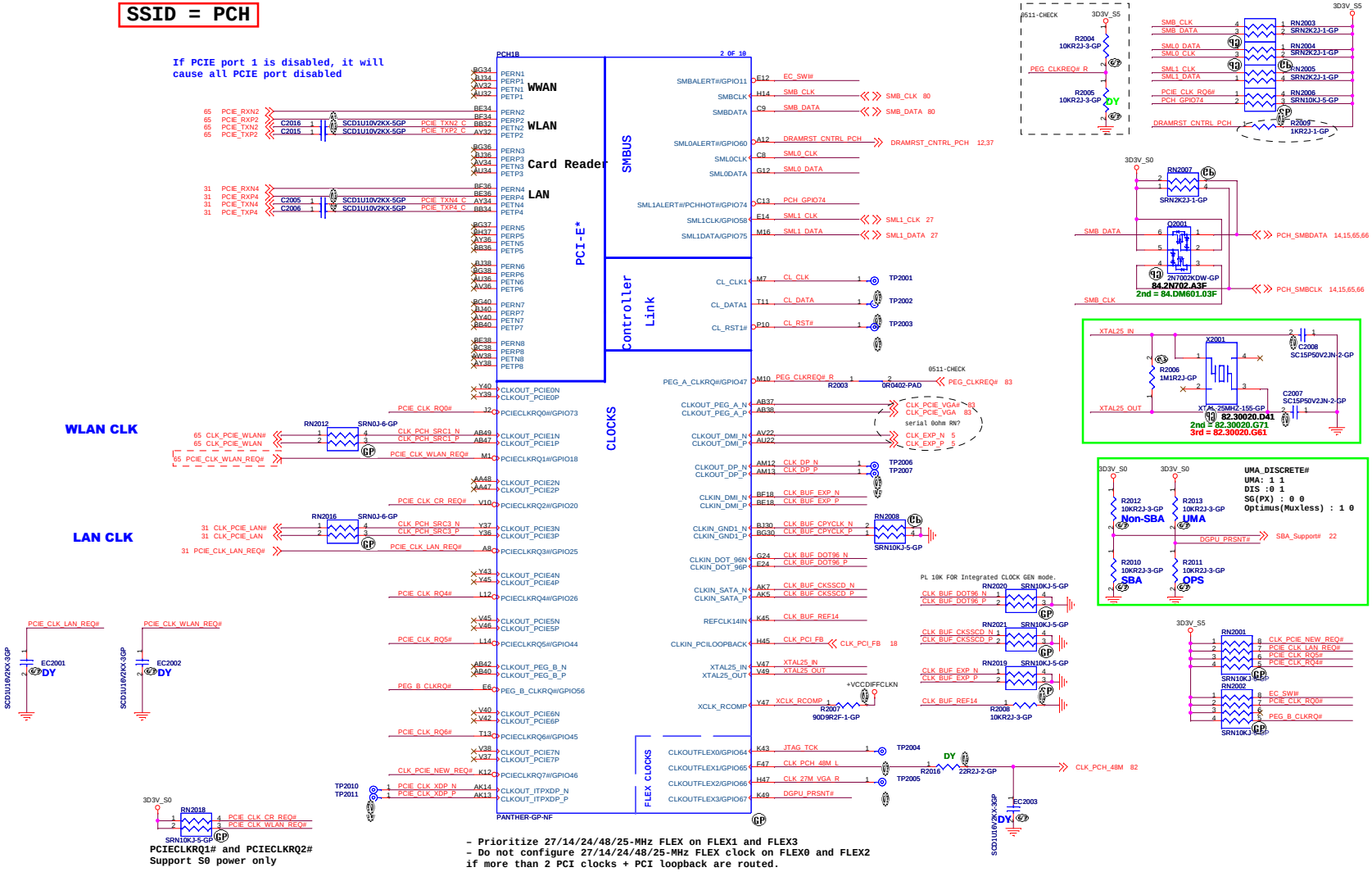
Title: PCH : DMI/FDI/PM
Size: A2 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 19 of 103

SSID = PCH



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Title: PCH : PCIE/SMBUS/CLK		
Size: A2	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 20 of 103	

SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Check with SW

m-SATA

HDD1

mSATA, CRV USE PORT2

ODD

E-SATA

Flash Descriptor Security Overide

HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap

HDA_SPKR	Low = Default High = No Reboot

Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

This signal has a weak internal pull-down.
On Die PLL VR is supplied by 1.5 V from VccVRM when sampled high, 1.8 V from VccVRM when sampled low.

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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Title: PCH : HDA/JTAG/SATA

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 21 of 103

R2202
HR:200K (64.20035.6DL)
CRV:10K (63.10334.1DL)

3D3V_S0 — R2202 10KR2J-3-GP — SATA_ODD_PRSNT#

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_A20GATE, H_RCIN#

GPIO27 has a weak[20K] internal pull up. To enable on-die PLL Voltage regurator, should not place external pull down.

G-Sensor	ST	KIXNOK
R2226	DY	10K
R2221	10K	DY

Note:
For PCH debug with XDP, need to NO STUFF R2218

PCH1F — 6 OF 10 — PANTHER-GP-NF

GPIO: BMBUSY#/GPIO0, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, LAN_PHY_PWR_CTRL/GPIO12, GPIO15, SATA4GP/GPIO16, TACH0/GPIO17, SCLOCK/GPIO22, GPIO24, GPIO27, GPIO28, STP_PCI#/GPIO34, GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SATA5GP/GPIO49/TEMP_ALERT#, GPIO57

CPU/MISC: TACH4/GPIO68, TACH5/GPIO69, TACH6/GPIO70, TACH7/GPIO71, A20GATE, PECI, RCIN#, PROCPWRGD, THRMTRIP#, INIT3_3V#, DF_TVS, TS_VSS1, TS_VSS2, TS_VSS3, TS_VSS4, NC_1

NCTF: VSS_NCTF_1#A4 … VSS_NCTF_32#F49 (NCTF_TEST_PIN)

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

PROCPWRGD (PCH) --> UNCOREPOWRGOOD (CPU)
Indicates that VccSA, VDDQ, VccA (1.0V) and VccIO power supplies are stable. This signal will be asserted only after PWROK assertion.

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

PLL ON DIE VR ENABLE

NOTE:This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

R2211 BOM CTRL
HR:1K
CRV:DY

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

<Core Design>

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Title: PCH : GPIO/NTCF/MISC
Size: A2 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 22 of 103

SSID = PCH

6A

POWER

PCH1G 7 OF 10

PANTHER-GP-NF

VCC CORE: VCCORE1 VCCORE2 VCCORE3 VCCORE4 VCCORE5 VCCORE6 VCCORE7 VCCORE8 VCCORE9 VCCORE10 VCCORE11 VCCORE12 VCCORE13 VCCORE14 VCCORE15 VCCORE16 VCCORE17

VCCIO: VCCIO28 VCCAPLLEXP VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCC3_3_3 VCCVRM2 VCCAFDIPLL VCCIO27 VCCDMI2

CRT: VCCADAC VSSADAC

LVDS: VCCALVDS VSSALVDS VCCTX_LVDS1 VCCTX_LVDS2 VCCTX_LVDS3 VCCTX_LVDS4

HVCMOS: VCC3_3_6 VCC3_3_7

DMI: VCCVRM3 VCCDMI1 VCCCLKDMI

DFT / SPI: VCCDFTERM1 VCCDFTERM2 VCCDFTERM3 VCCDFTERM4 VCCSPI

FDI

1D05V_VTT

1.3A(Total current of VCCCORE)

C2311 SC1U6D3V2KX-GP, C2312 SC1U6D3V2KX-GP, C2302 SC1U6D3V2KX-GP, C2304 SC1U6D3V2KX-GP, C2303 SCD1U10V2KX-5GP

1D05V_VTT

AN19 VCCIO28

TP2301 VCCAPLLEXP (10uF x1)

BJ22 VCCAPLLEXP

1D05V_VTT

2.925A(Total current of VCCIO)

C2327 SC1U6D3V2KX-GP, C2328 SC1U6D3V2KX-GP, C2306 SC1U6D3V2KX-GP, C2307 SCD1U10V2KX-5GP, C2308 SCD1U10V2KX-5GP, C2309 SC1U6D3V2KX-GP

AN16 VCCIO15, AN17 VCCIO16, AN21 VCCIO17, AN26 VCCIO18, AN27 VCCIO19, AP21 VCCIO20, AP23 VCCIO21, AP24 VCCIO22, AP26 VCCIO23, AT24 VCCIO24, AN33 VCCIO25, AN34 VCCIO26

0.266A (Totally VCC3_3 current)

3D3V_S0

(0.1uF x1) C2310 SCD1U10V2KX-5GP

BH29 VCC3_3_3

0.159A(Totally current of VCCVRM)

+VCCAFDI_VRM AP16 VCCVRM2

TP2302 VCCFDIPLL BG6 VCCAFDIPLL

1D05V_VTT AP17 VCCIO27

+1.05VS_VCC_DMI AU20 VCCDMI2

0.042A (Totally current of VCCDMI)

VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop

VCCADAC U48 +VCCA_DAC_1_2 0.001A

C2313 SCD1U10V2KX-1GP, C2314 SCD1U10V2KX-5GP, C2315 SC1U6D3V2KX-GP, C2333 SC1U6D3V3MX-GP

L2301 BLM18PG181SN1D-GP

3D3V_DAC_S0 DY R2301 0R2J-2-GP

+VCCA_DAC_3V

3D3V_S0 R2302 0R2J-2-GP

C2326 SC1U6D3V3MX-GP

VSSADAC U47 0.001A

VCCALVDS AK36

VSSALVDS AK37

+3VS_VCCA_LVDS

3D3V_S0 R2304 0R0603-PAD

VCCTX_LVDS1 AM37

VCCTX_LVDS2 AM38

VCCTX_LVDS3 AP36

VCCTX_LVDS4 AP37

0.06A +1.8VS_VCCTX_LVDS (0.01uF x2) (22uF x1)

C2316 SCD01U50V2KX-1GP, C2317 SCD01U50V2KX-1GP

1D8V_S0 R2305 0R0603-PAD

C2330 SC1U6D3V2KX-GP, C2329 SC1U6D3V2KX-GP

VCC3_3_6 V33

VCC3_3_7 V34 0.266A (0.1uFx1)

3D3V_S0 Reserve 0ohm for power measurement?

C2319 SCD1U10V2KX-5GP

+VCCAFDI_VRM R2308 0R0402-PAD

1D5V_S0

VCCVRM3 AT16 0.16A

VCCDMI1 AT20 0.042A +1.05VS_VCC_DMI R2306 0R0402-PAD

1D05V_VTT

C2320 SC1U6D3V2KX-GP (1uF x1)

VCCCLKDMI AB36 0.02A +1.05VS_VCC_DMI_CCI R2307 0R0402-PAD

1D05V_VTT

C2321 SC1U6D3V2KX-GP (1uFx1) (10uFx1)

VCCDFTERM1 AG16

VCCDFTERM2 AG17

VCCDFTERM3 AJ16 0.19A

1D8V_S0 Reserve 0ohm for power measurement? (0.1uFx1)

VCCDFTERM4 AJ17

C2322 SCD1U10V2KX-5GP

VCCSPI V1 0.02A VCCSPI_3D3V R2309 0R0402-PAD

3D3V_S5

C2323 SC1U6D3V2KX-GP (1uFx1)

3.3V CRT LDO

5V_S0 DY C2325 SC1U10V2KX-1GP

U2302 DY AME8818BEEV330Z-GP 74.08818.B3F

IN GND EN OUT NC#4

3D3V_DAC_S0 DY C2324 SC1U6D3V2KX-GP

74.09091.J3F GMT OBS REASON:G9091
series is going to EOL and no room for further cost reduction.
Pls help to use AME AME8818 , TI TLV702 and GMT G9090 for replacement.

74.09198.G7F OBS

Refer to NPCE795 shared SPI flash architecture

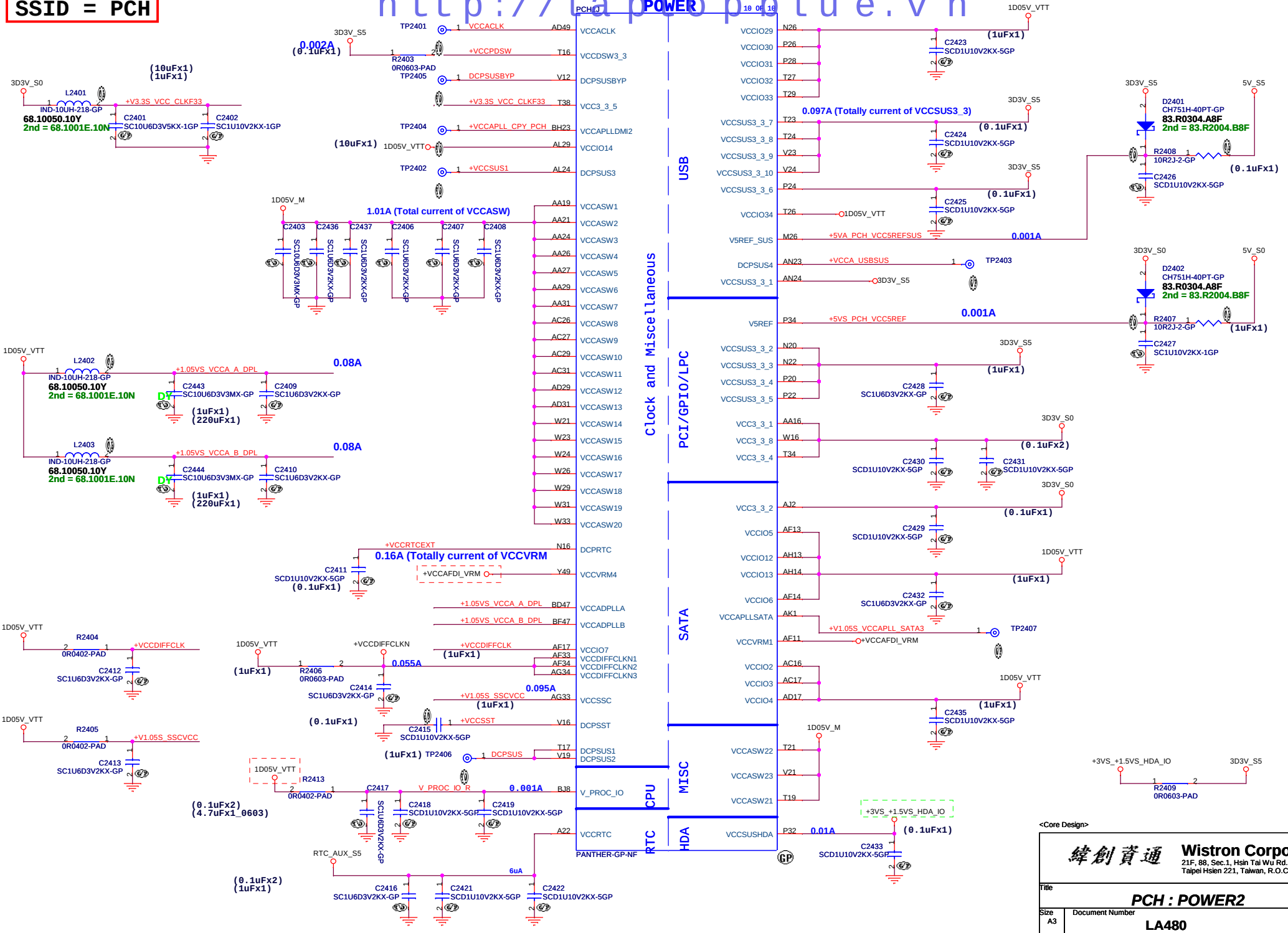
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH : POWER1	
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 23 of 103	

SSID = PCH

POWER



<Core Design>

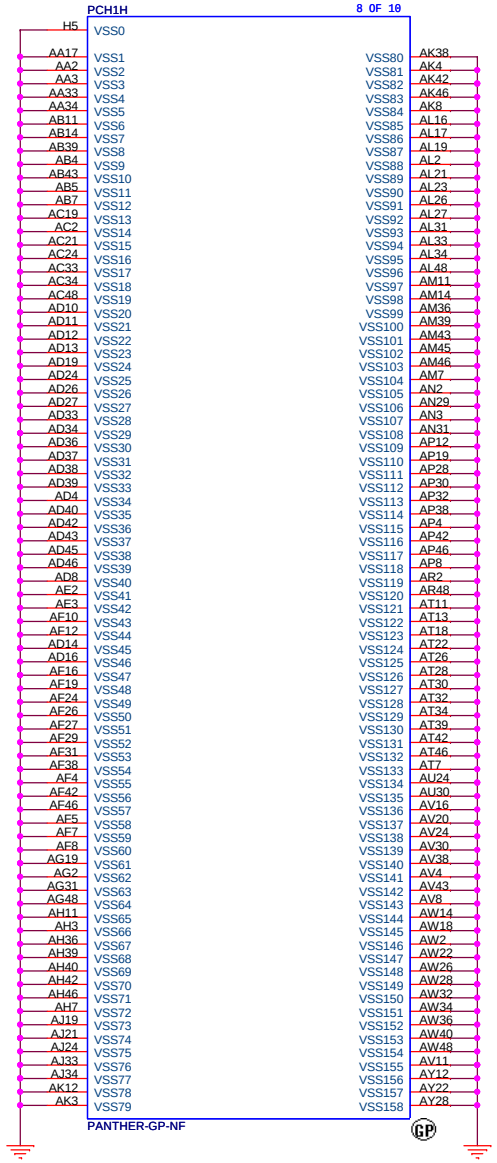
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

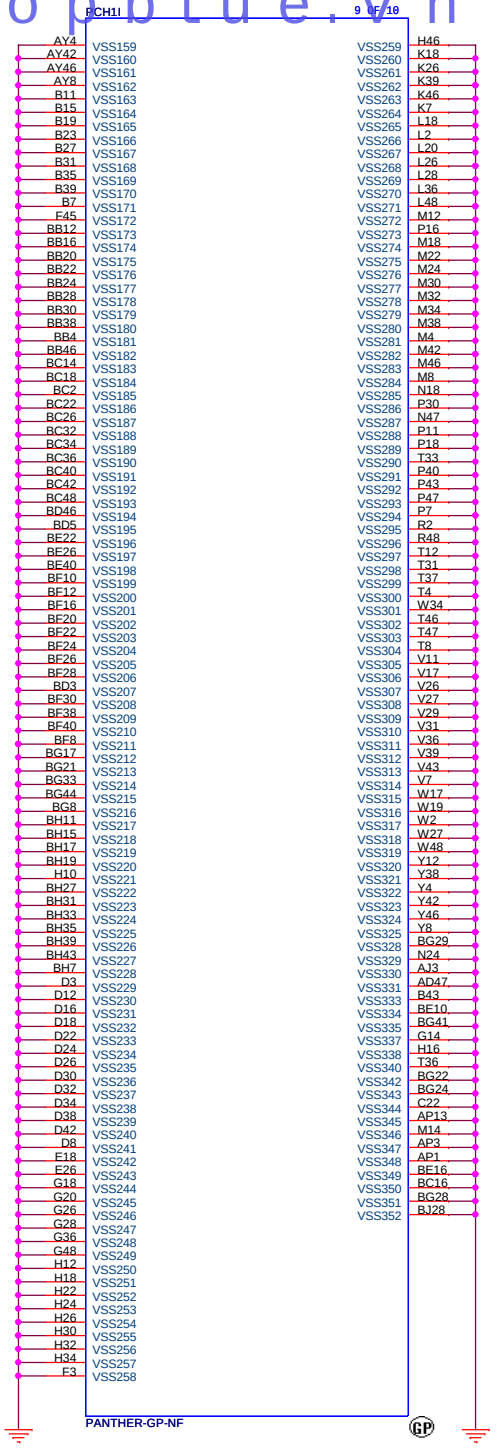
Title: PCH : POWER2

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 24 of 103

SSID = PCH





<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : VSS**

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 25 of 103

BLANK

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

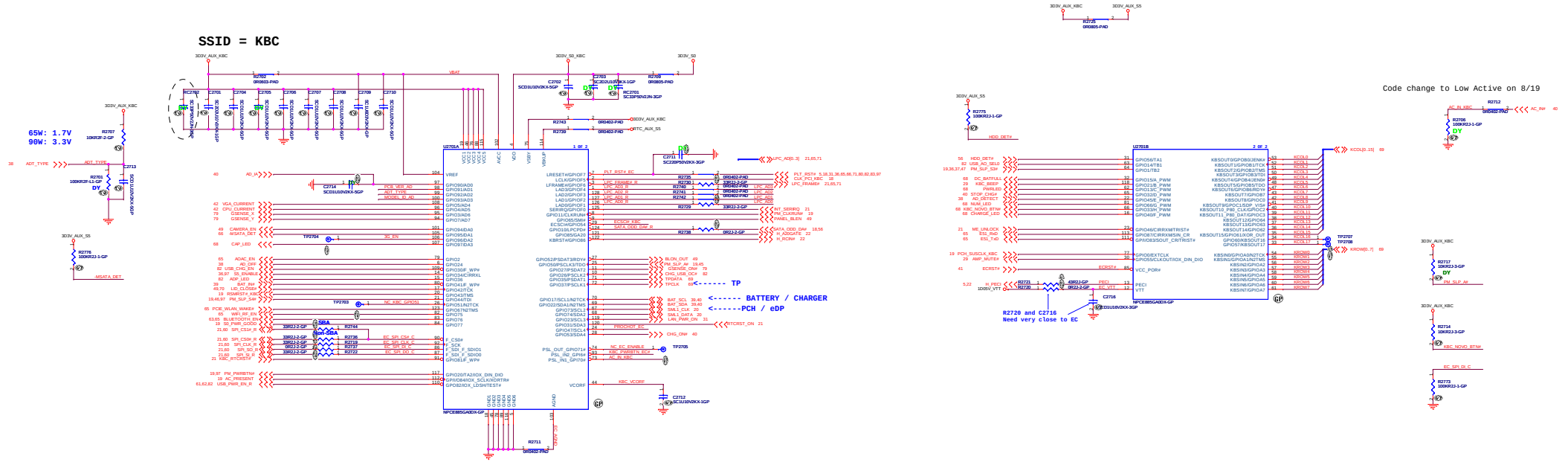
Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

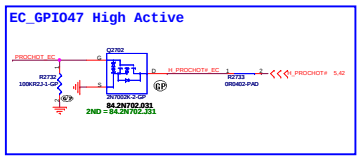
Date: Friday, January 06, 2012 Sheet 26 of 103

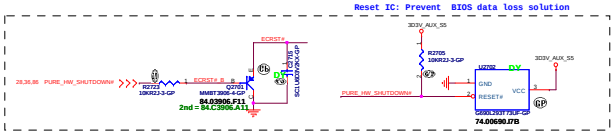
SSID = KBC

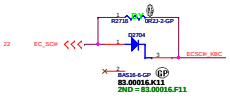
65W: 1.7V
90W: 3.3V

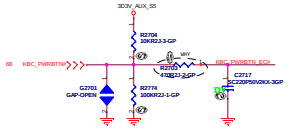


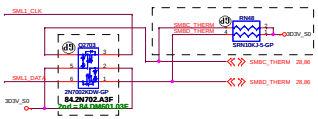
Code change to Low Active on 8/19

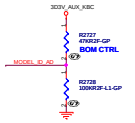




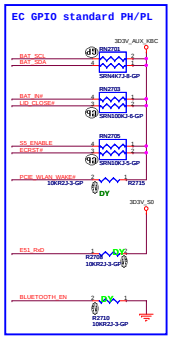


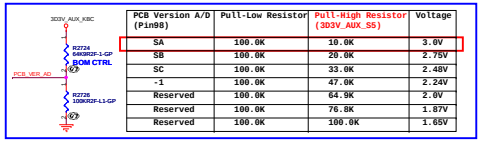






MODEL_ID_AD (Pin100)	Pull Down	Pull High	Voltage
UMA	100.0K	33.0K	2.481V
OPTIMUS	100.0K	47.0K	2.245V





PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

<Core Design>
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21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C
Title: <Title>
Size: A1 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 27 of 183

SSID = Thermal

Thermal sensor

20110718_Carrey:
For Vendor suggestion, add 390pF Cap. as closed to pin B/C and E of Q2803

Close to SO-DIMM on top side.

SA 0905 change to 390p

3
C2803 SC390P50V2KX-GP
Q2802 MMBT3904WT1G-GP

2200p close to smsc2103 chip

2
C2804 SC390P50V2KX-GP DY
Q2804 MMBT3904WT1G-GP
C2805 SC2200P50V2KX-2GP
REMOTE2-
REMOTE2+

between CPU, VGA and DIMM on bottom side

T8

1
Q2803 MMBT3904WT1G-GP
C2808 SC390P50V2KX-GP
2200p close to smsc2103 chip
C2802 SC2200P50V2KX-2GP
H_THERMDA
H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

20110718_Carrey:
For Vendor suggestion, add 10k pull high to 3D3V_S0

3D3V_S0
R2812 10KR2J-3-GP DY
THERM_SCI#

3D3V_S0
R2801 6K8R2J-GP
SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0
R2805 68R2-GP
C2806 SCD1U10V2KX-4GP
2103_VDD

U2801
VDD
DP1
DN1
DP2/DN3
ND2/DP3
SYS_SHDN#
ALERT#
SMCLK
SMDATA
GPIO1
GPIO2
TACH
PWM
TRIP_SET
SHDN_SEL
GND
GND
EMC2103-2-AP-GP

H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-
THERM_SYS_SHDN#
THERM_SCI#
27,86 SMBC_THERM
27,86 SMBD_THERM
2103_4
2103_5
TP2802
TP2803
RN2801
SRN10KJ-5-GP
3D3V_S0
FAN_TACH_1
D2801
FAN_TACH
FAN_PWM
TRIP_SET R2806
SHDN_SEL
649R2F-GP
T8 = 98
CH551H-30PT-GP
83.R5003.C8F
1st = 83.R5003.J8F
2ND = 83.R5003.I8F

TRIP_SET: 649 ohm => 87 dgree C

pin6, ALERT# OD
pin7, SYS_SHDN# OD

4 WIRE PWM Fan Control circuit

5V_S0
C2801 SC4D7U6D3V3KX-GP
R2803 10KR2J-3-GP
R2802 0R0805-PAD AFTP2807
FAN1
5V_S0_FAN
FAN_TACH
FAN_PWM
R2804 0R0402-PAD
EC2802 SC1KP50V2KX-1GP DY
EC2801 SC1KP50V2KX-1GP DY
FAN_PWM_C
ACES-CON4-GP-U1
20.F0714.004
CHECK PIN DEFINE
20100707_EMI

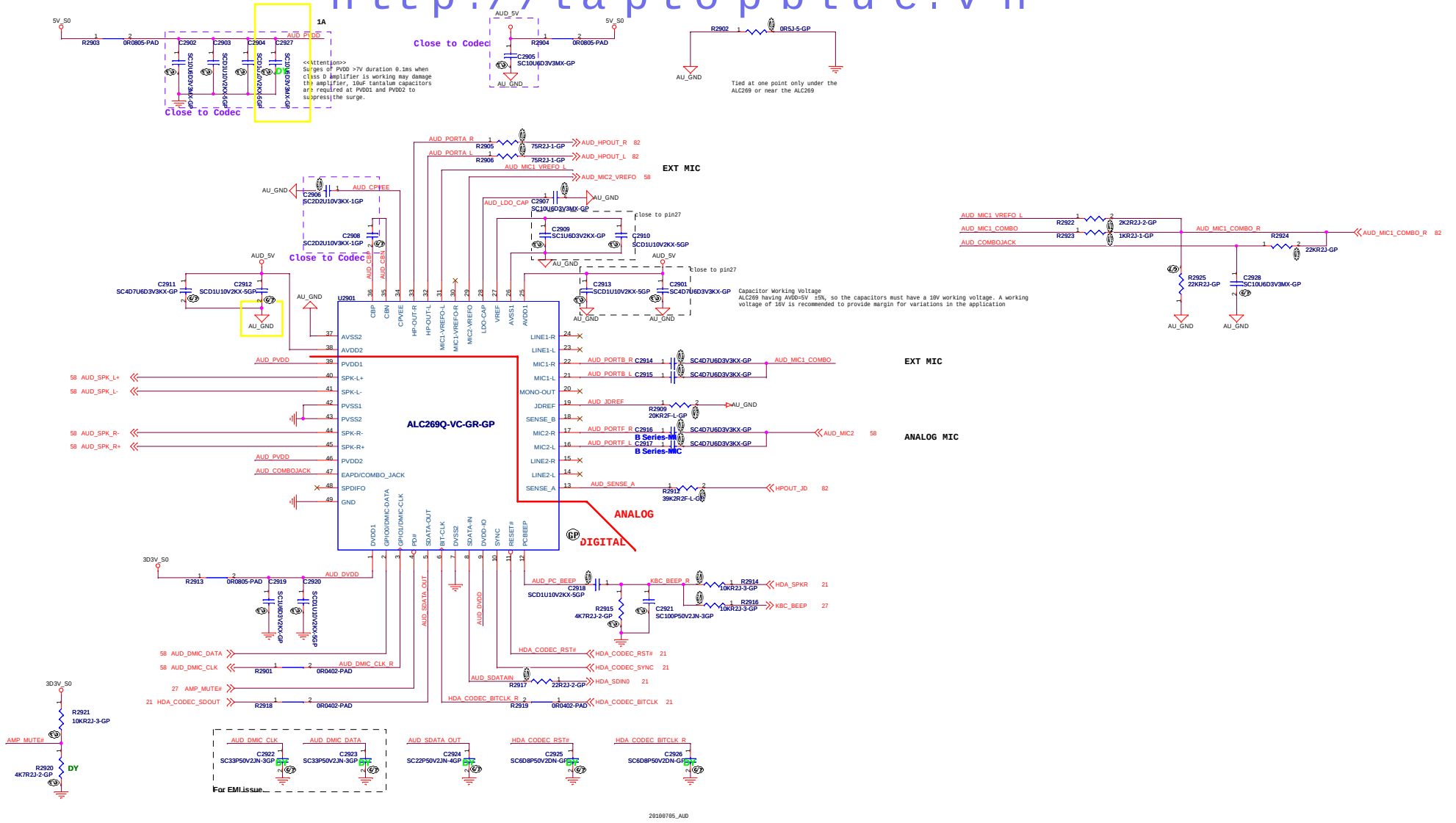
AFTP2801
AFTP2805
AFTP2806
FAN_PWM_C
FAN_TACH
5V_S0_FAN

3D3V_AUX_S5
D2802 BAT54PT-GP DY
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
27,36,86 PURE_HW_SHUTDOWN#
R2810 10KR2J-3-GP DY
C2807 SCD1U10V2KX-5GP DY
Q2801 2N7002K-2-GP
84.2N702.031
2ND = 84.2N702.J31
THERM_SYS_SHDN#
IMVP_PWRGD_T
3D3V_S0
R2808 100KR2J-1-GP
3D3V_S0
R2809 10KR2J-3-GP
R2811 0R0402-PAD
IMVP_PWRGD 36,42

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL SENSOR SMSC EMC2103
Size: A3 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 28 of 103



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 29 of 103

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<Core Design>

緯創資通 Wistron Corporation
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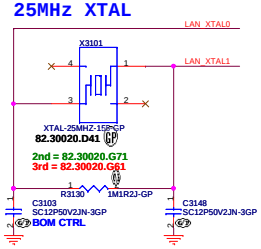
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 30 of 103

25MHz XTAL

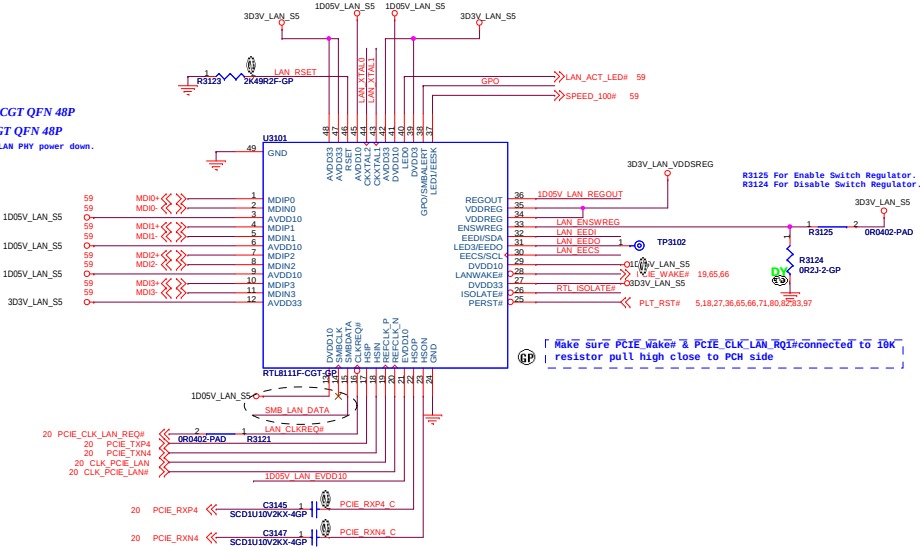


	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF

71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

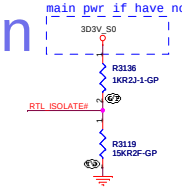
71.08111.J03, IC PCI-E RTL8111E-VL-CGT QFN 48P

8111F can use GPIO to inform system to do LAN PHY power down.

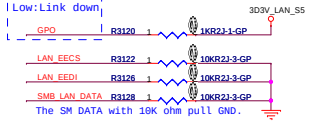


Make sure PCIE_Wake & PCIE_CLK_LAN_Req connected to 10K resistor pull high close to PCH side

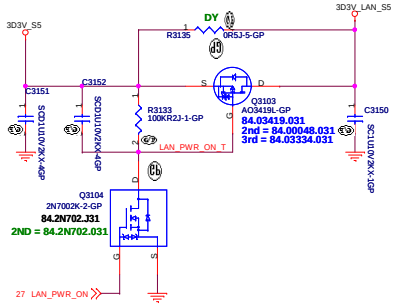
main pwr if have no ASF

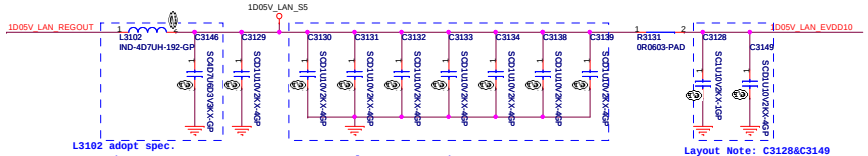


High:Link up
Low:Link down



The SM DATA with 10K ohm pull GND.

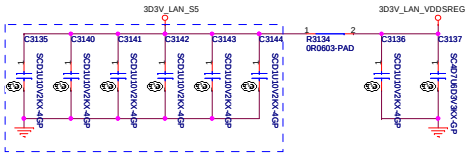




L3102 adopt spec.
C3104 change to 4.7uF X5R type capacitor

Layout Note: Close to U3101 pin C3130 ~ C3134,C3138,C3139 For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149 Close to U3101 pin21



Layout Note: C3135, C3140~C3144 Close to U3101 pin For VDD33 pins - 12, 27, 39, 42, 47, 48.

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN_RTL8111F		
Size: A2	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 31 of 103	

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5U220 (CARD READER)

Size	Document Number	Rev
A1	LA480	SD

Date: Friday, January 06, 2012 Sheet 32 of 353

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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size: A4	Document Number: **LA480**
Rev: **SD**	
Date: Friday, January 06, 2012	Sheet 33 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 34 of 103

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<Core Design>

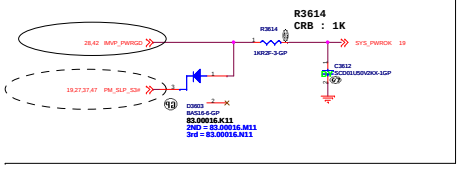
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

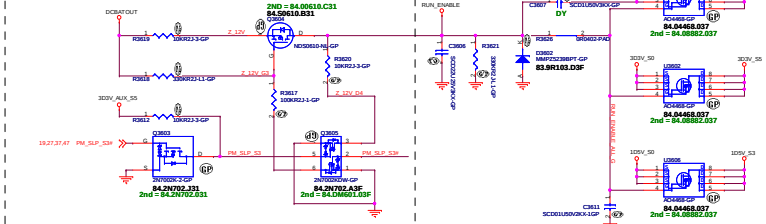
Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 35 of 103

Power Sequence

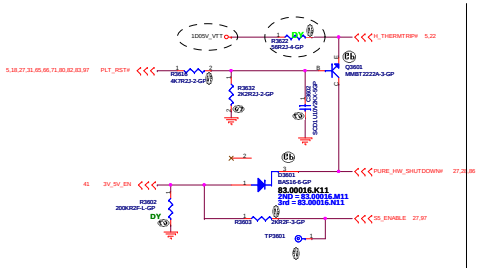


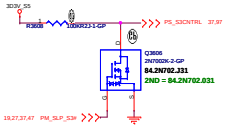
Run Power



1D5V_S0

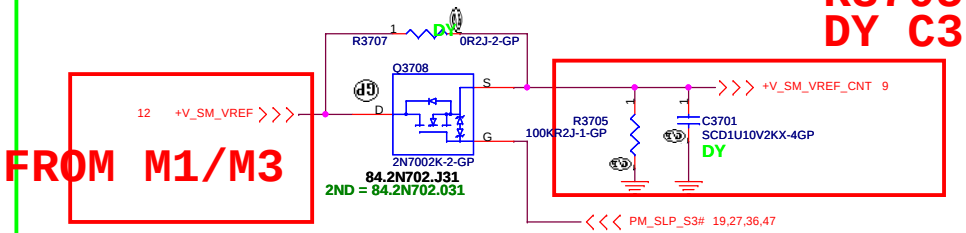
MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A



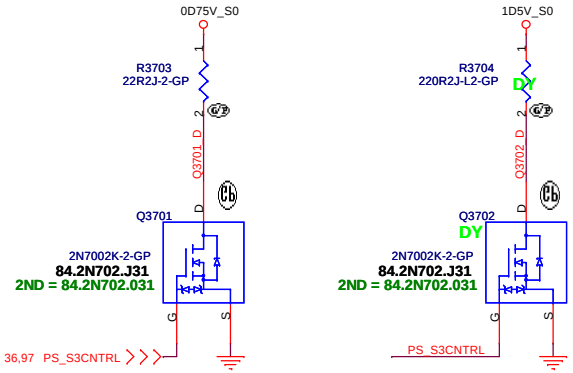


DEL R3714
R3705 ->100K
DY C3701

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

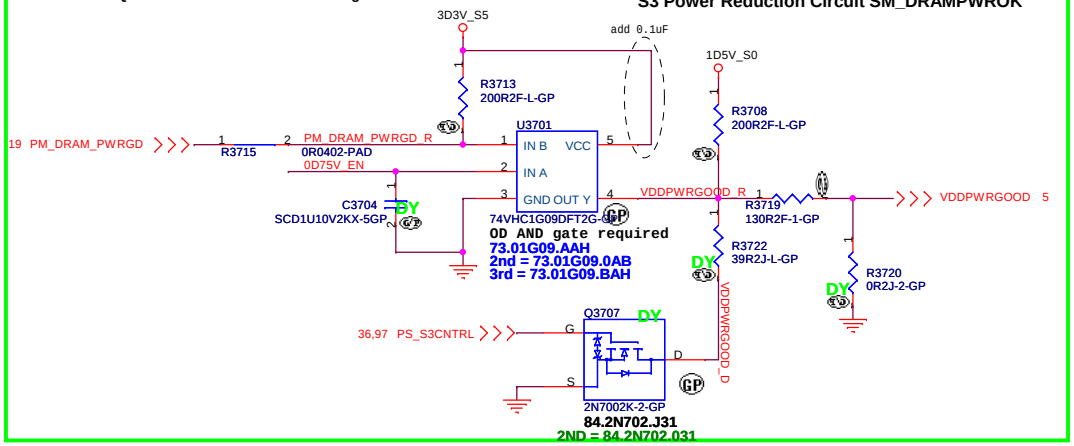


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

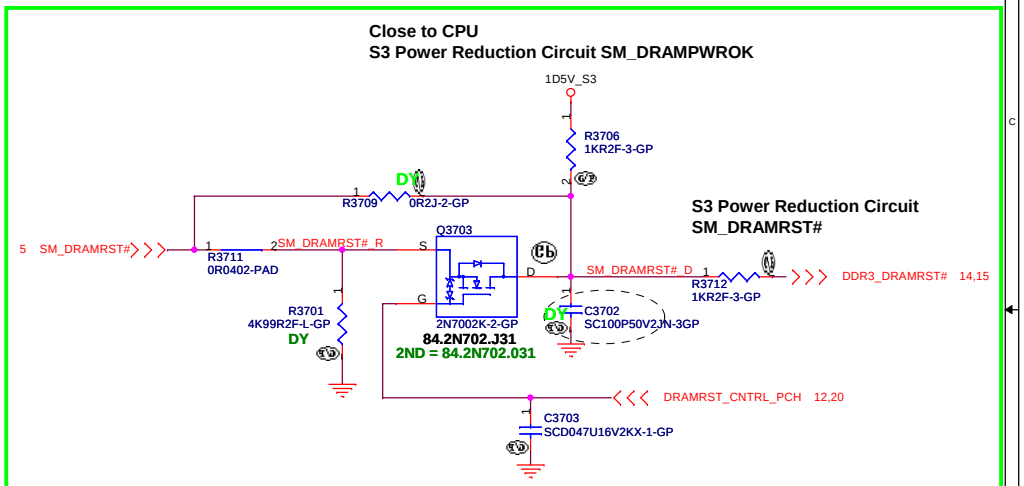


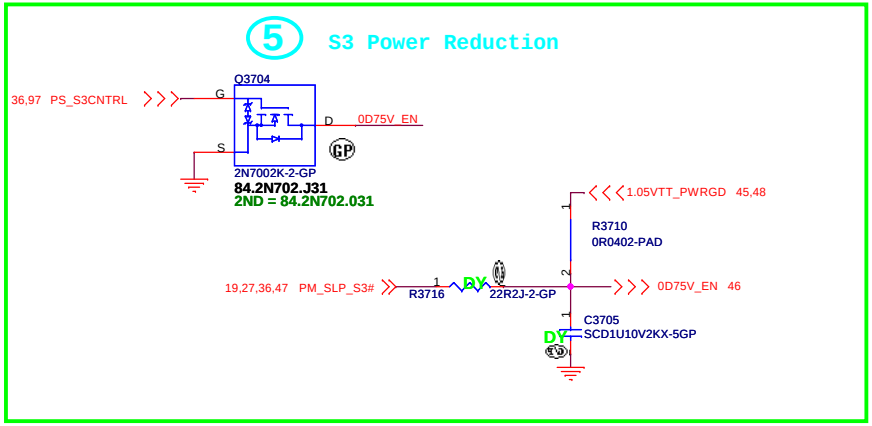
SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK





<Core Design>

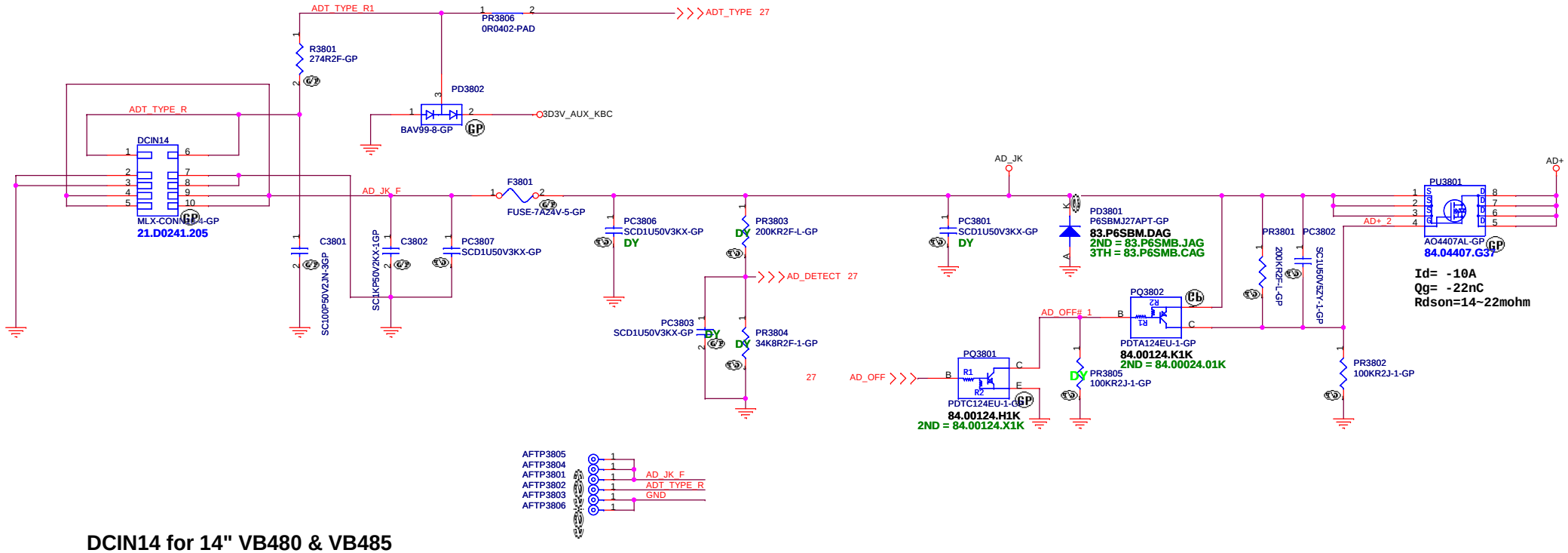
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 37 of 103

Adaptor in to generate DCBATOUT



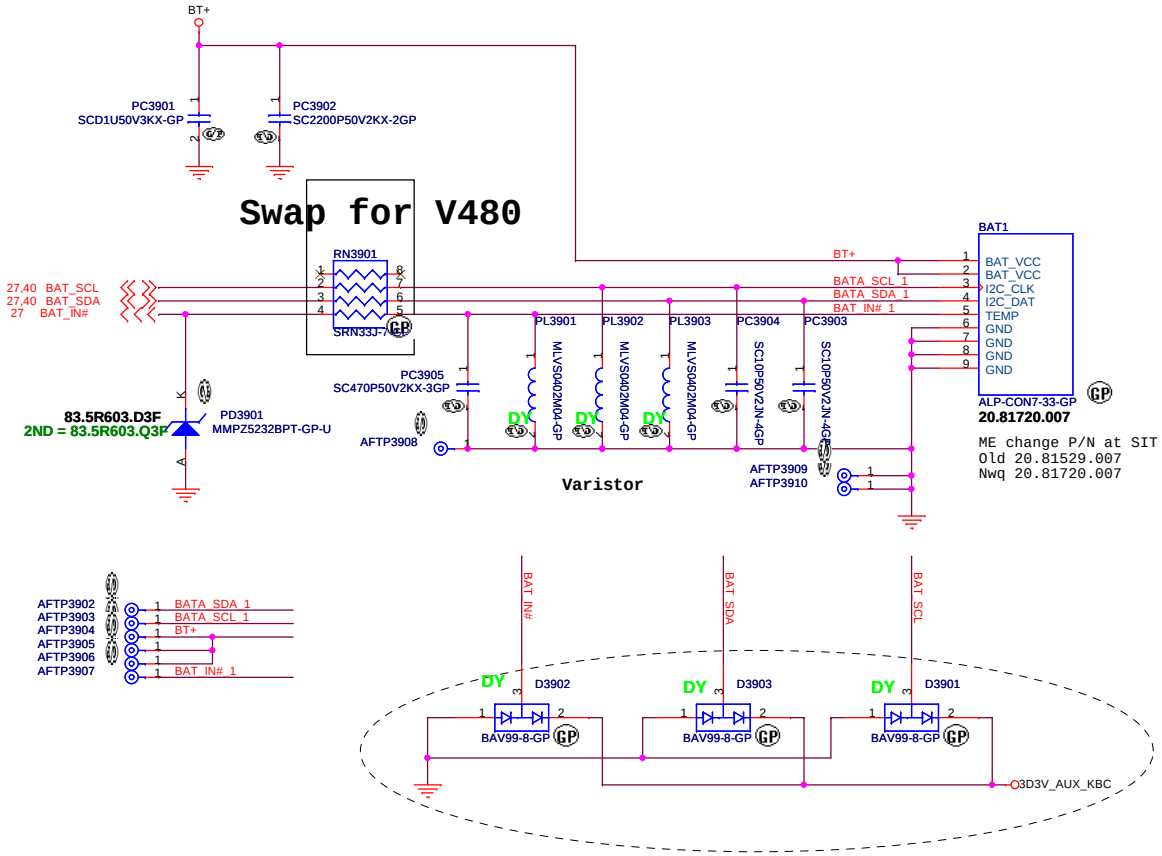
DCIN14 for 14" VB480 & VB485
DCIN15 for 15" VB580 & VB585

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *DCIN_JACK*		
Size: A3	Document Number: **LA480**	Rev: **SD**
Date: Friday, January 06, 2012	Sheet 38 of 103	

BATTERY CONNECTOR



DY on LAB stage

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BATT_CONN	
Size	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 39 of 103	

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118K	100K

STOP_CHG#
connects to KBC

Id= -10A
Qg= -22nC
Rdson=14~22mohm

Id= -10A
Qg= -22nC
Rdson=14~22mohm

68.00143.041

68.00143.041

Charger Current=1.4~3.6A

84.2N702.A3F
2nd = 84.DM601.03F

84.2N702.E31
2ND = 84.2N702.D31

<Core Design>

Wistron Corporation
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

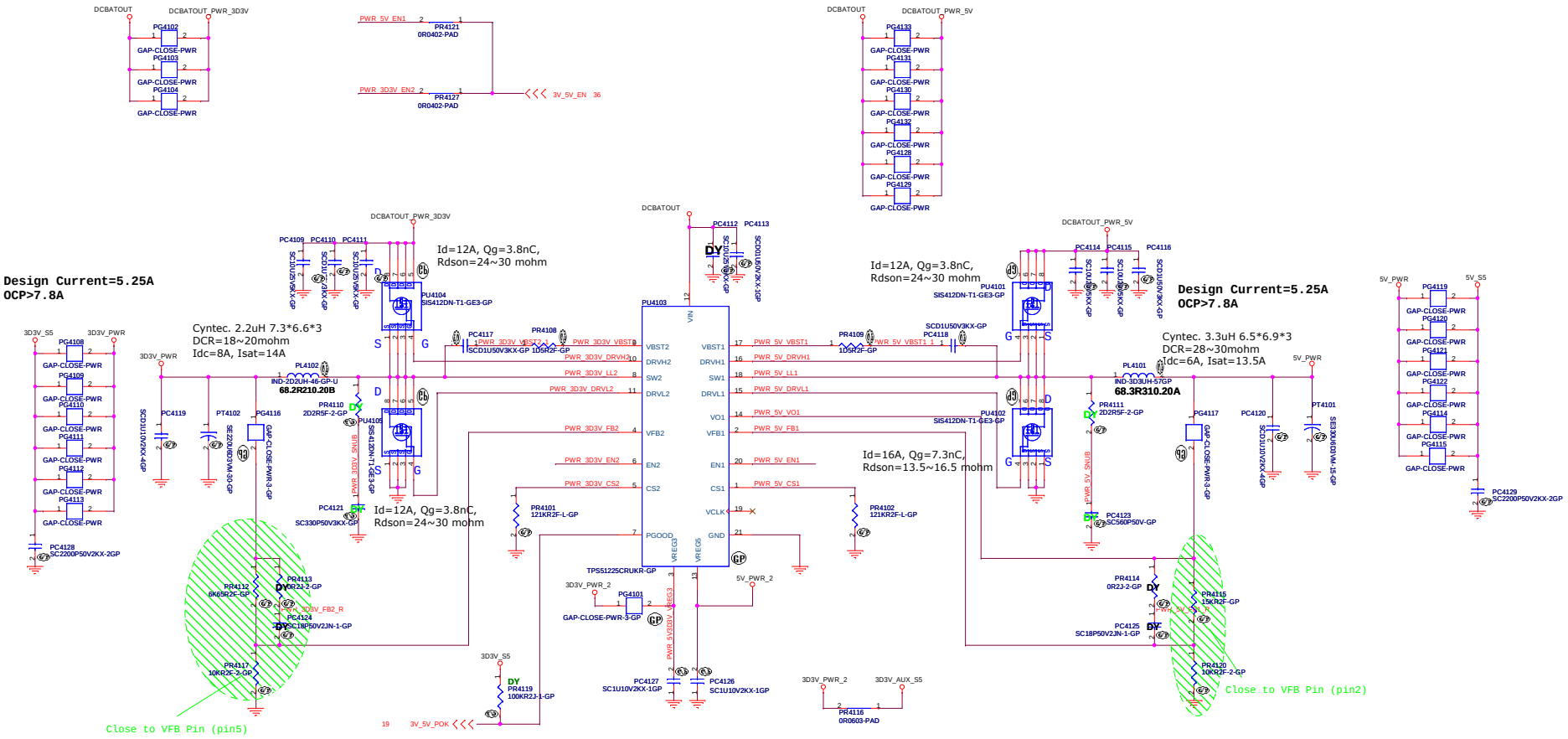
Title: <Title>

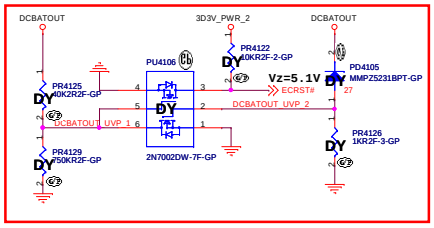
Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v

http://laptopblue.vn





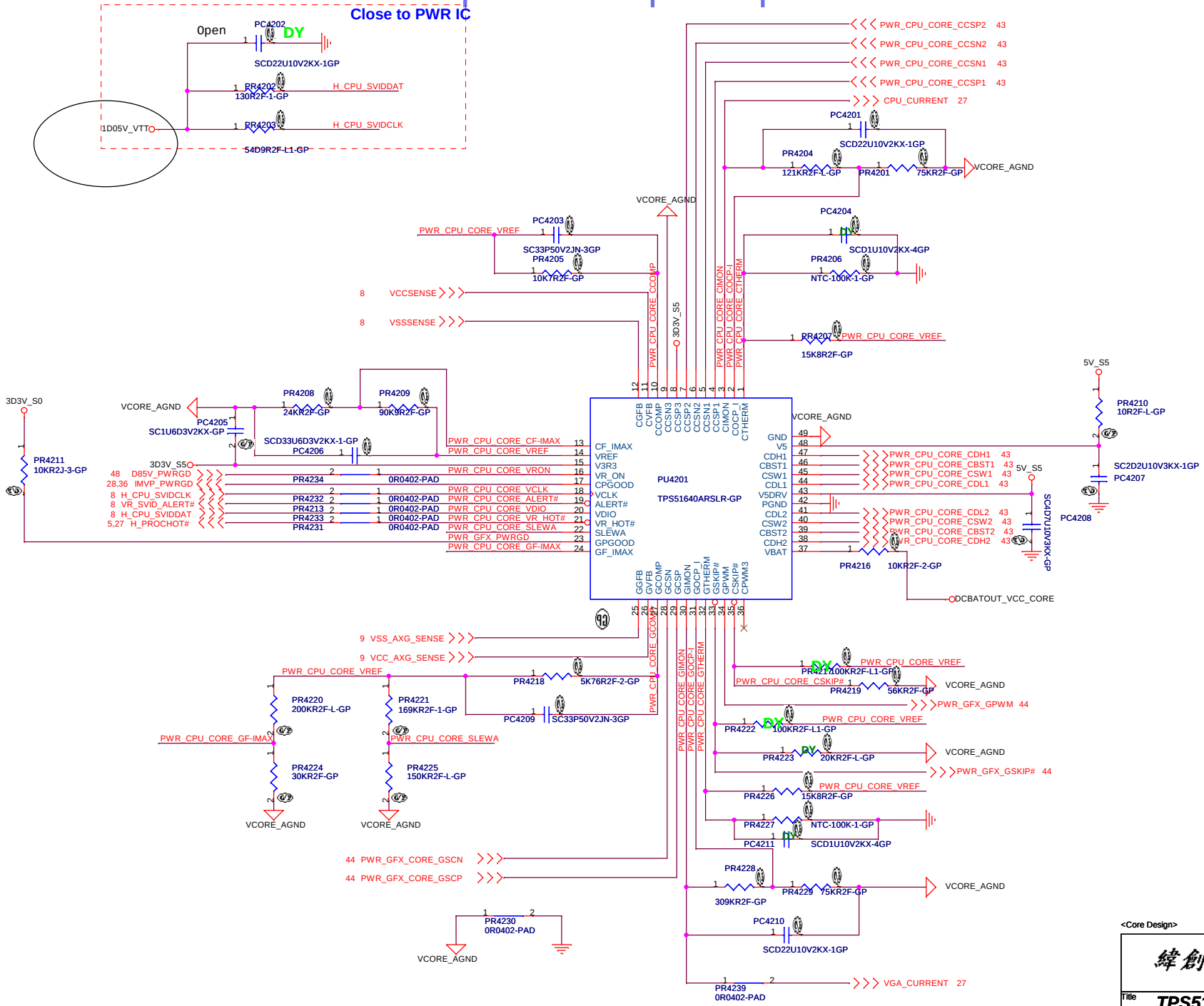
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123_5V_3D3V

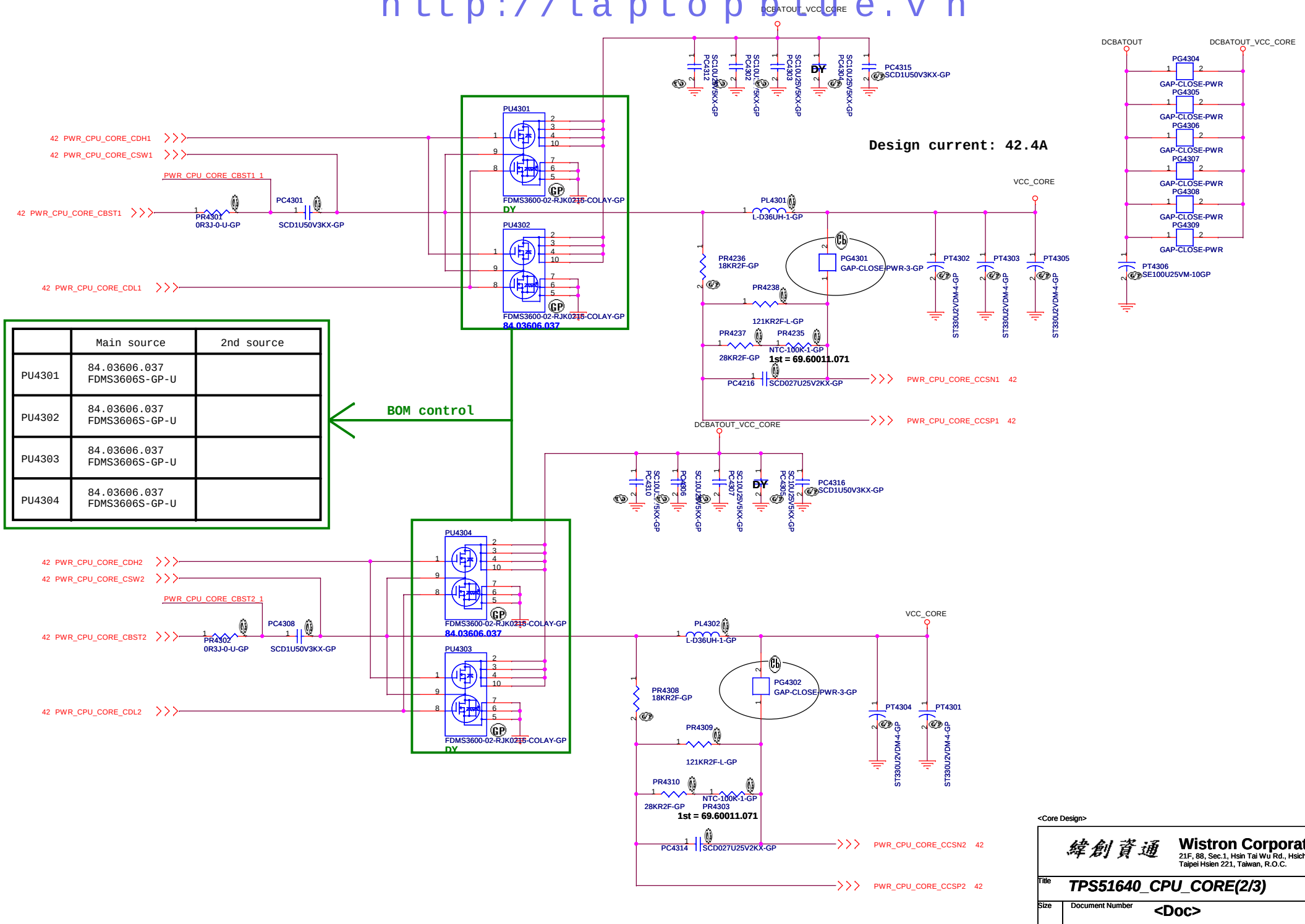
Size | Document Number | Rev: SD

Date: Friday, January 06, 2012 | Sheet 41 of 103



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51640_CPU_CORE(1/3)		
Size	Document Number: <Doc>	Rev: SD
Date: Friday, January 06, 2012	Sheet 42 of 103	



	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

BOM control

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51640_CPU_CORE(2/3)

Size | Document Number: <Doc> | Rev: SD

Date: Friday, January 06, 2012 | Sheet 43 of 103

	Main source	2nd source
PU4402	84.07608.037 FDMS7608S-GP	
PU4403	84.07608.037 FDMS7608S-GP	

BOM control

DCBATOUT
DCBATOUT_VCC_GFXCORE
PG4401 GAP-CLOSE-PWR
PG4402 GAP-CLOSE-PWR
PG4403 GAP-CLOSE-PWR
PG4404 GAP-CLOSE-PWR

PU4402
PU4403
FDMS3600-02-RJK0215-COLAY-GP
84.07608.037

PWR_GFX_CORE_DRVH
PWR_GFX_CORE_SW
PWR_GFX_CORE_BST
PWR_GFX_CORE_DRVL
PR4401 0R3J-0-U-GP
PWR_GFX_CBST1_1
PC4401 SC1U25V3KX-1-GP

PC4409 SC10U25V5KX-GP
PC4402 SC10U25V5KX-GP
PC4403 SC10U25V5KX-GP
PC4404 SC10U25V5KX-GP
PC4410 SCD1U50V3KX-GP

Design current: 22A

PL4401 L-D36UH-1-GP
VCC_GFXCORE
PR4410 18KR2F-GP
PG4303 GAP-CLOSE-PWR-3.5G
PR4407 121KR2F-L-GP
PT4401 PT4402 PT4403 ST330U2VDM-4-GP
PR4405 28KR2F-GP
NTC-100K-1-GP PR4409
1st = 69.60011.071
PC4408 SCD022U25V2KX-GP
PWR_GFX_CORE_GSCN 42
PWR_GFX_CORE_GSCP 42

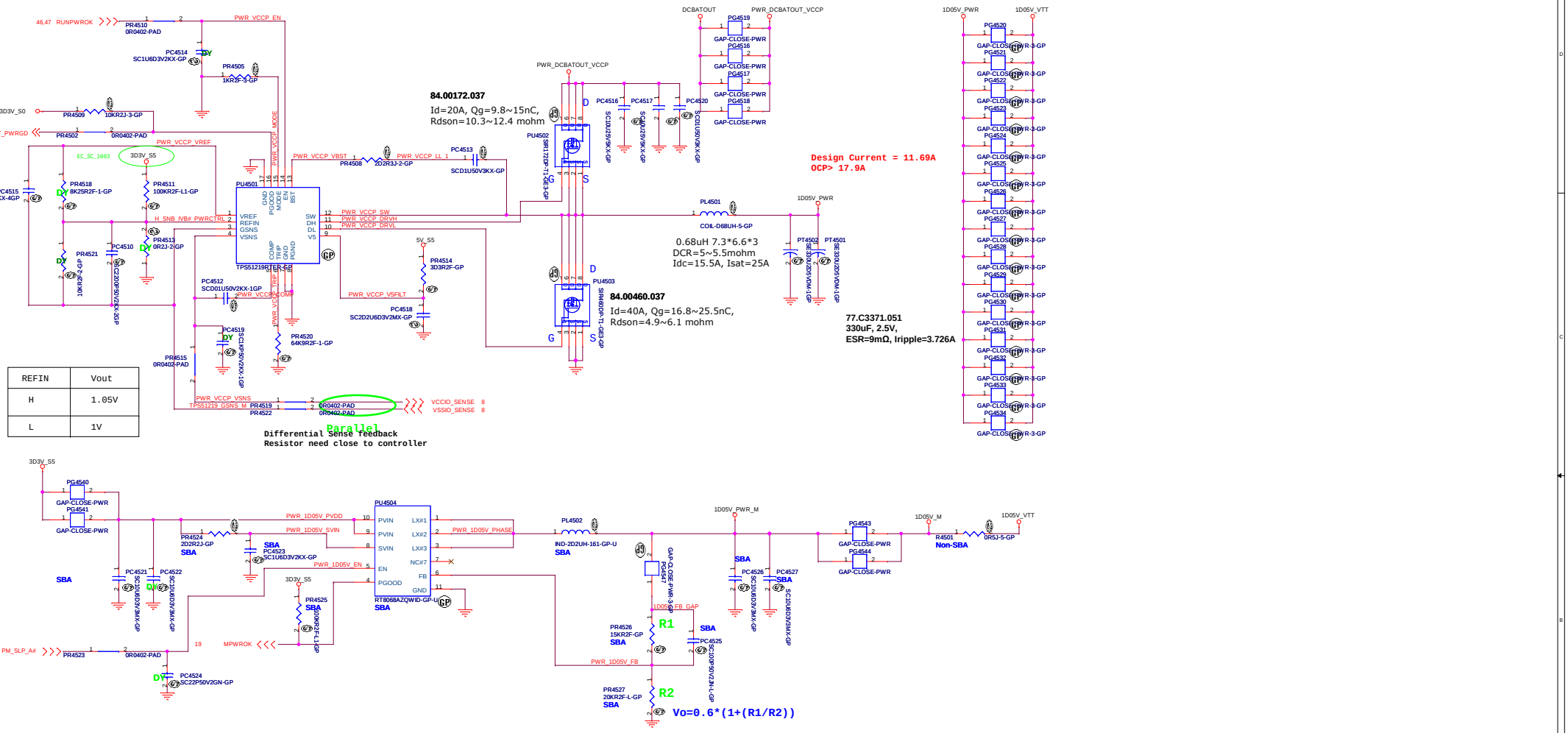
PU4401
PWR_GFX_CORE_BST
42 PWR_GFX_GSKIP#
42 PWR_GFX_GPWM
BST SKIP# PWM GND
GND DRVH SW VDD DRVL
PWR_GFX_CORE_DRVH
PWR_GFX_CORE_SW
PWR_GFX_CORE_DRVL
TPS51601DRBR-GP
5V_S5
PC4407 SC2D2U10V3KX-1GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51640_CPU_CORE(3/3)
Size | Document Number: <Doc> | Rev: SD
Date: Friday, January 06, 2012 | Sheet 44 of 103

TPS51219 for 1D05V



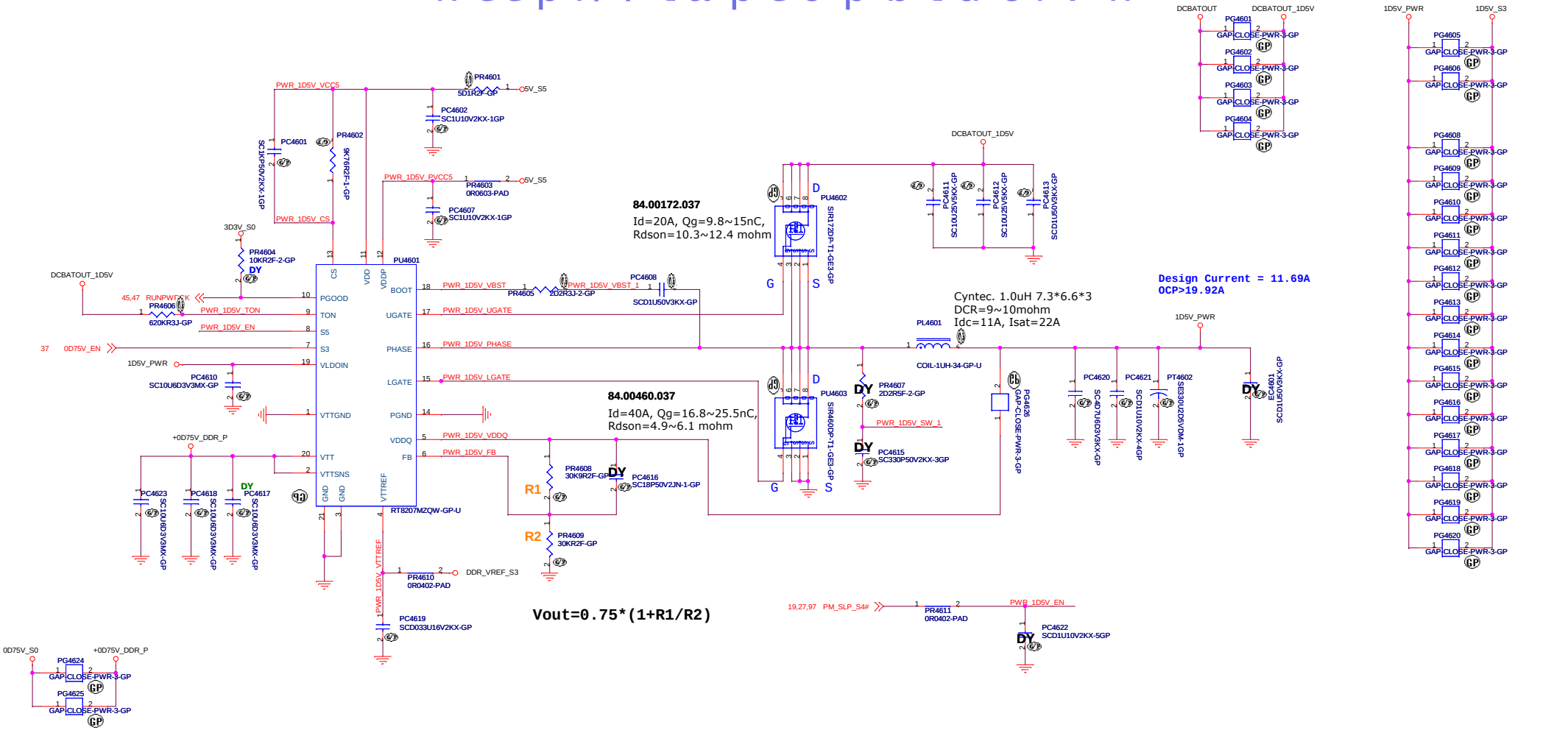
REFIN	Vout
H	1.05V
L	1V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51211_1D05V	
Size	Document Number	Rev SD
Date: Friday, January 06, 2012	Sheet 45 of 103	

SSID = PWR.Plane.Regulator_1p5v0p75v



<Core Design>

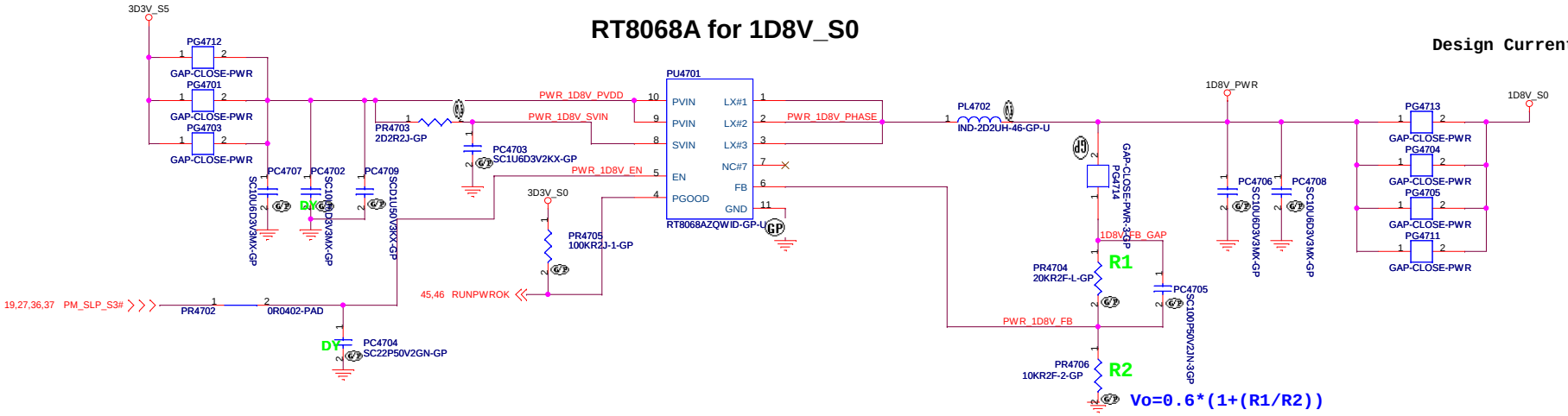
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8207M_1D5V_0D75V	
Size	Document Number <Doc>	Rev SD
Date: Friday, January 06, 2012	Sheet 46 of 103	

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

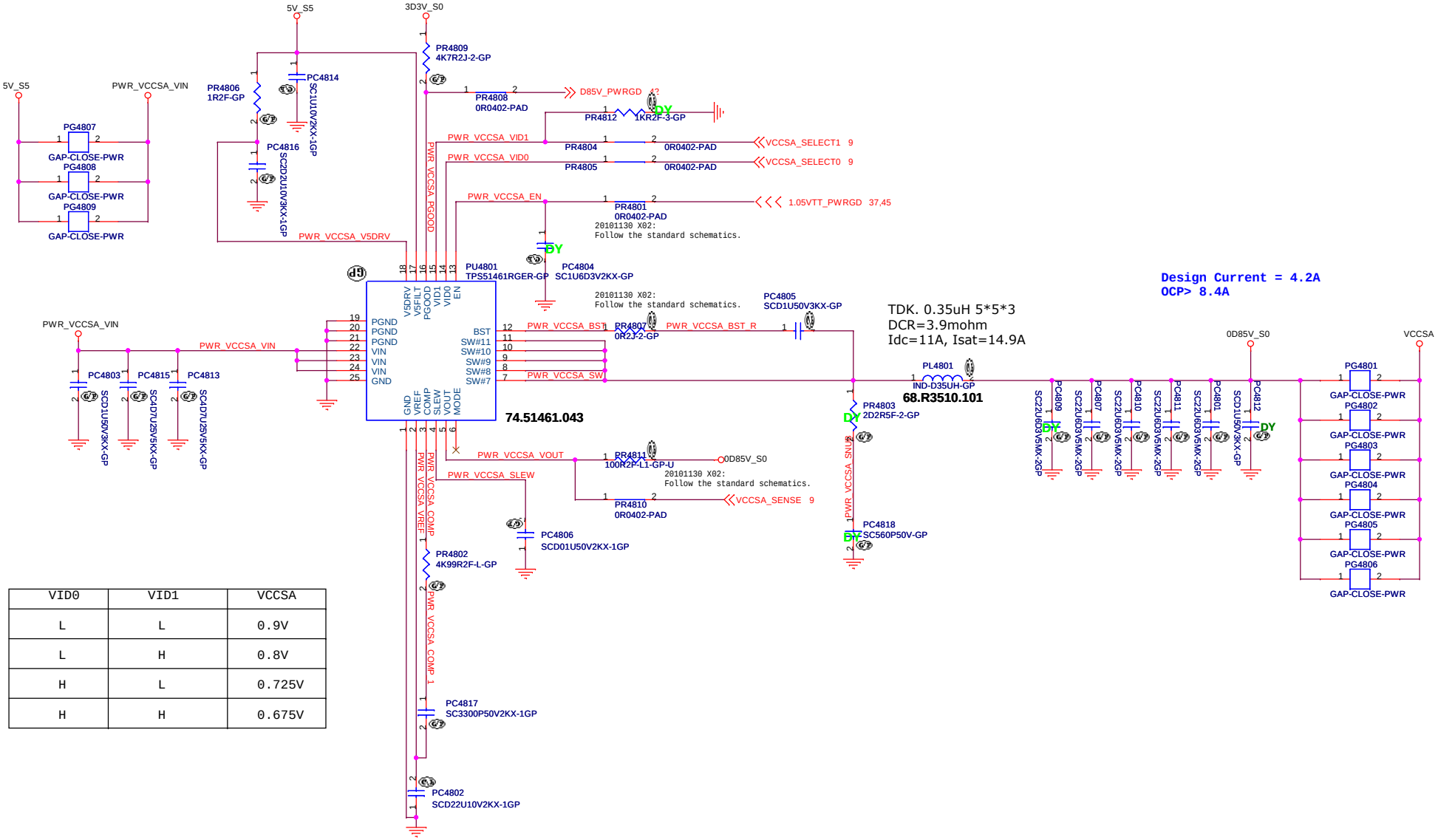
Design Current=1.1A



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PWM_1D8V_RT8015B***
Size / Document Number	Rev: SD
Date: Friday, January 06, 2012	Sheet 47 of 103

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

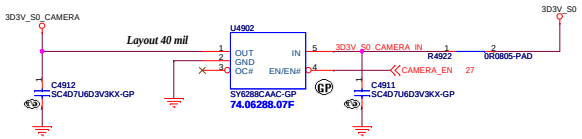
Title	VCCSA_TPS51461	
Size	Document Number <Doc>	Rev SD
Date: Friday, January 06, 2012	Sheet 48 of 103	

SSID = VIDEO

LVDS connector

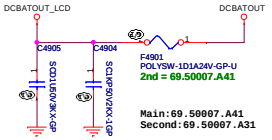
LCD / Inverter Connector

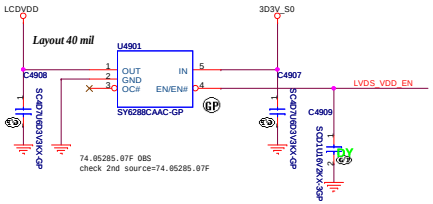
CAMERA POWER

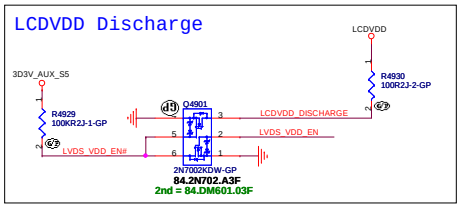


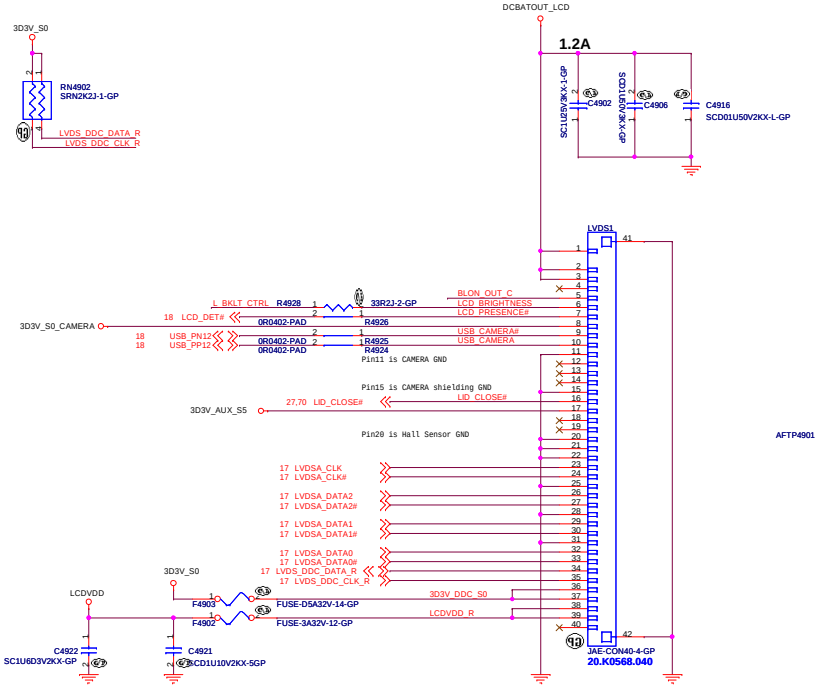
SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

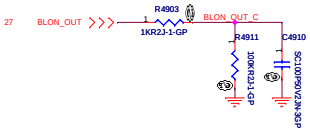
LCD POWER



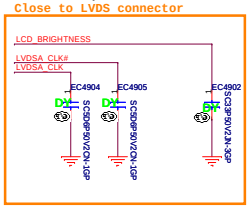




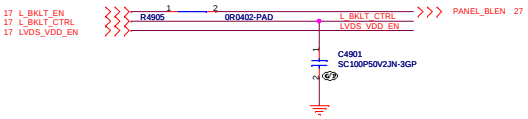




For EMI request
Close to LVDS connector



Panel BL brightness/Power En/BL En



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size: A2 | Document Number: LA480 | Rev: SD

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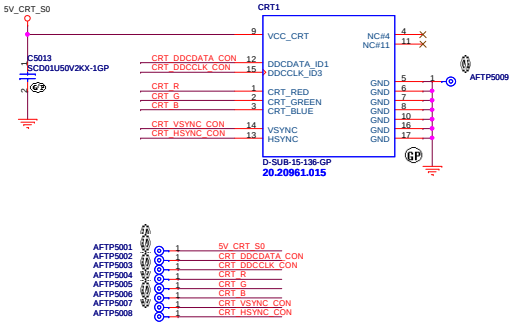
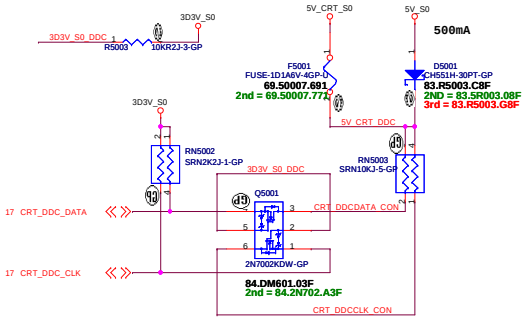
CRT connector

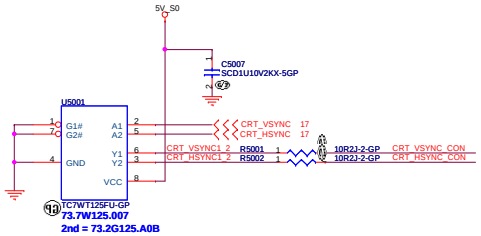


CRT DDCDATA & DDCCLK level shift

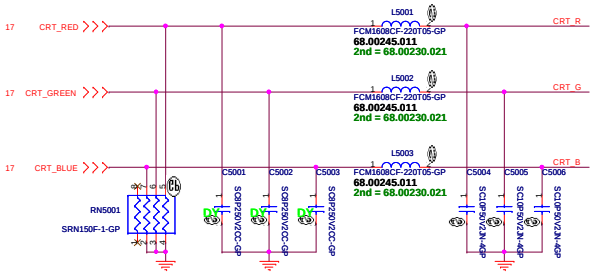
Pull High 5V Design on CRT Board

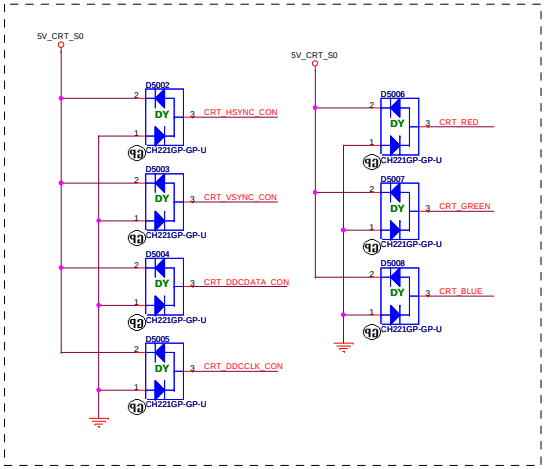


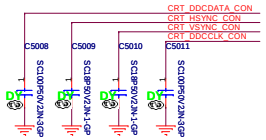
CRT Hsync & Vsync level shift



CRT RGB







<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A2	LA480	SD

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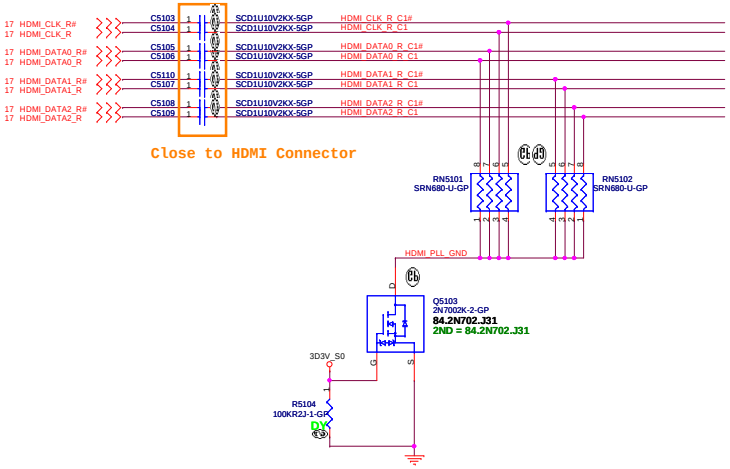
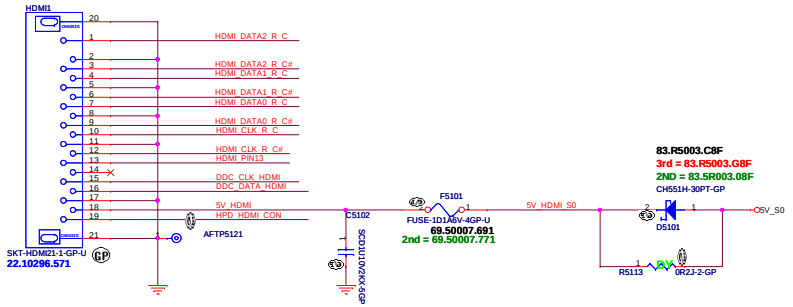
SSID = VIDEO

HDMI Passive Level Shifter

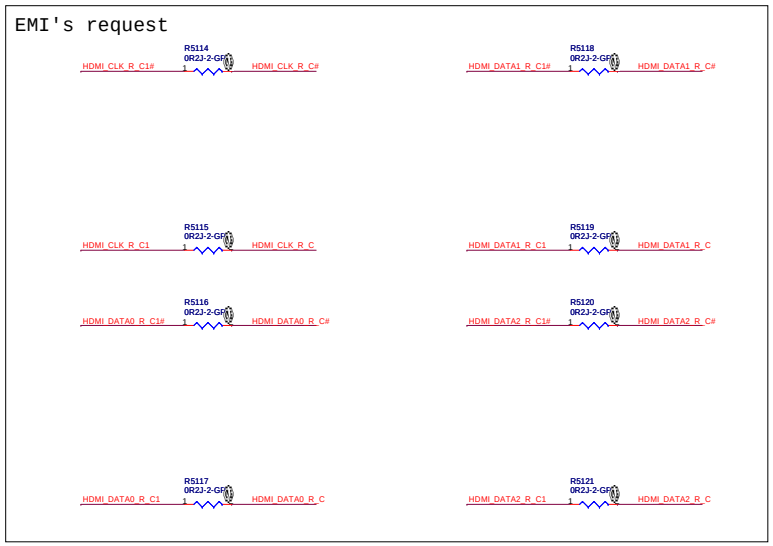
Close to HDMI Connector

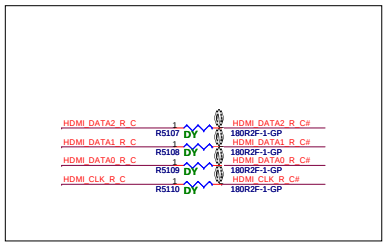


HDMI CONNECTOR

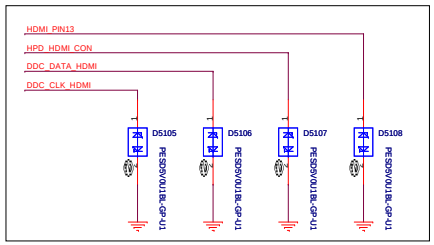


EMI's request

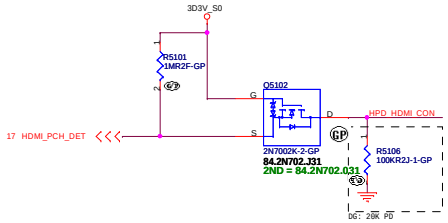


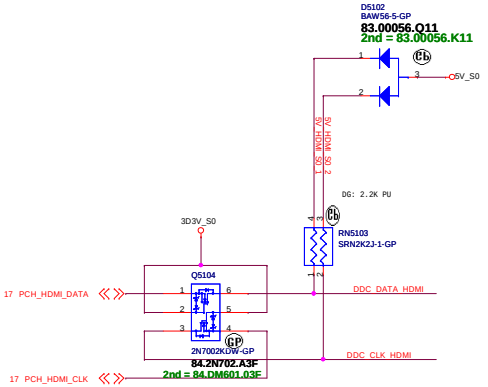


ESD Request



HDMI DDC Passive Level Shifter





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 51 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 52 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 53 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

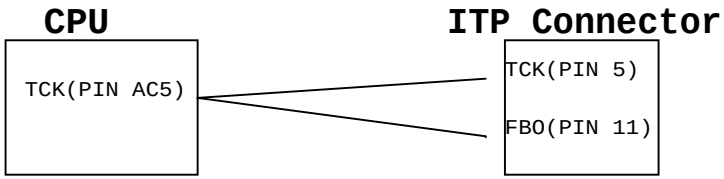
Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 54 of 103

SSID = User.Interface

ITP Connector

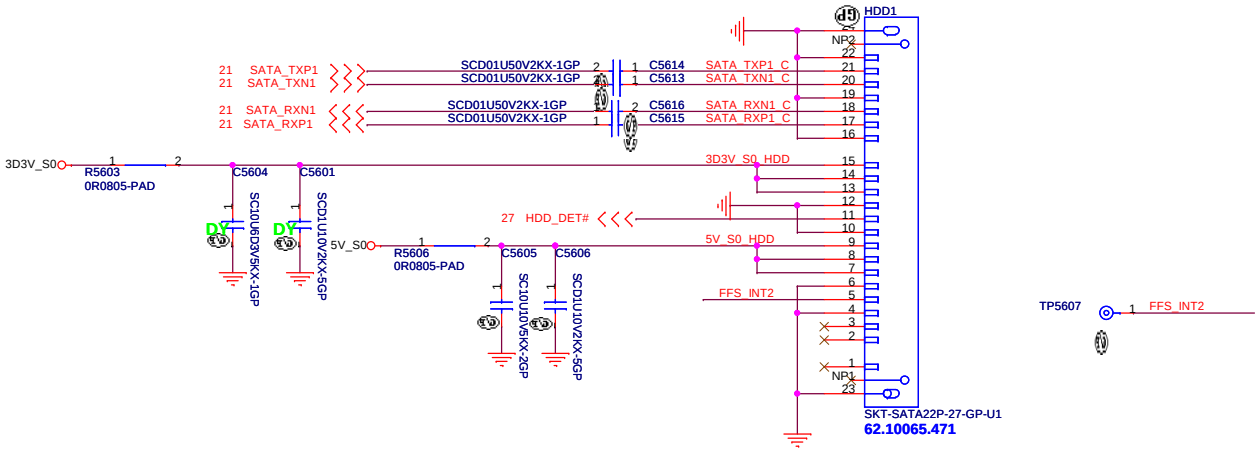
H_CPURST# use pull-up Resistor close ITP connector 500 mil (max), others place near CPU side.



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ITP		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 55 of 103	

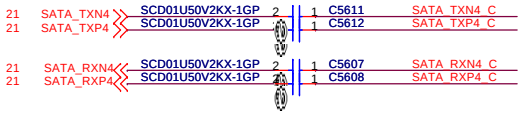
SATA HDD Connector

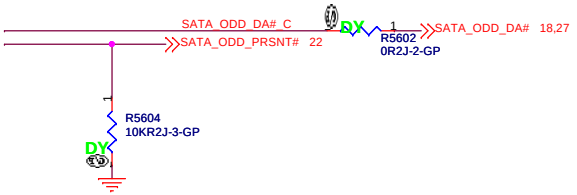


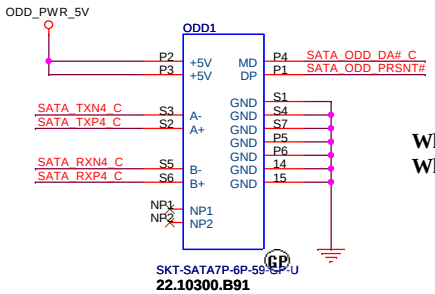
ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.





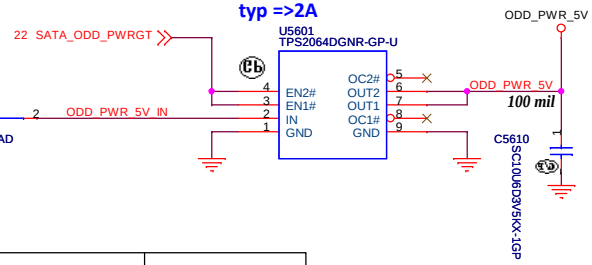


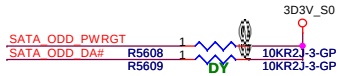
74.02069.079 TI TPS2069DGNR MSOP 8P
74.07534.D79 UPI UP7534PRA8-15 MSOP 8P
74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
74.07534.A79 UPI UP7534ARA8-15 MSOP8P

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

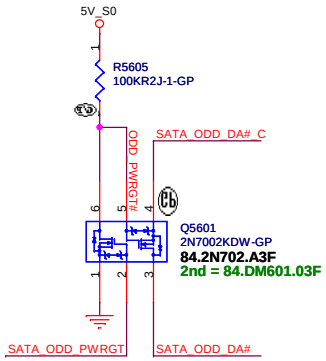
SATA Zero Power ODD

Current limit
Active High
typ =>2A





SUPPORT ZERO SATA ODD



TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD/ODD	
Size A3	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 56 of 103	

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<Core Design>

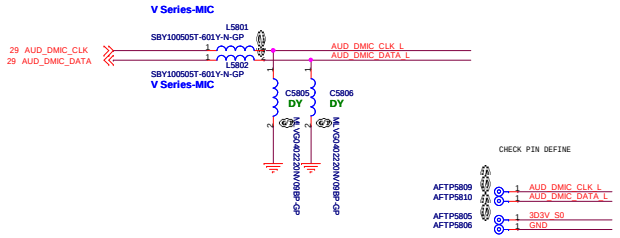
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

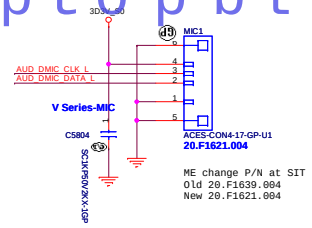
Title: *E-SATA+USB*

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 57 of 103

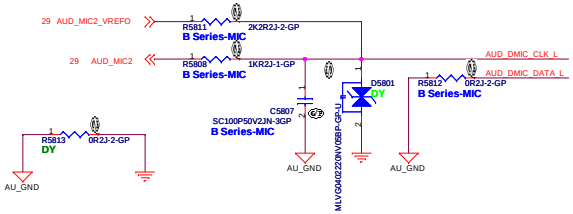
Int. Digital MIC for V series



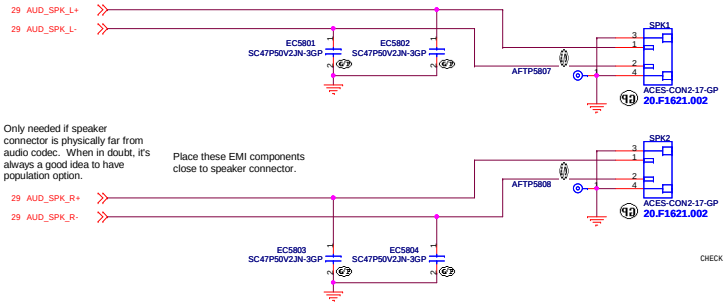


ME change P/N at SIT
Old 20.F1639.004
New 20.F1621.004

Int. Mono Analog MIC for B series



INTERNAL STEREO SPEAKERS



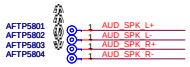


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size	Document Number	Rev
A2	LA480	SD

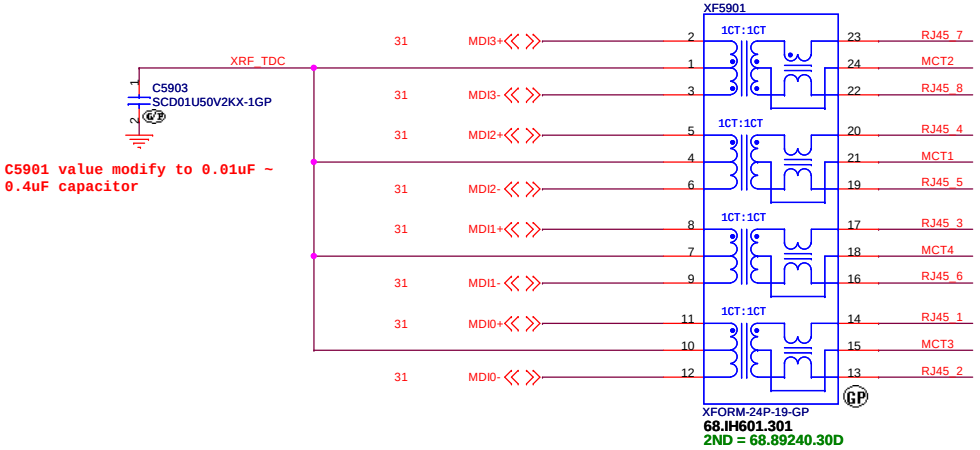
Date: Friday, January 06, 2012 Sheet 58 of 103

FOR CO-LAY

GIGA Lan Transformer

83.00005.BAE
DIODE ARR SRV05-4.TCT SOT-23-6

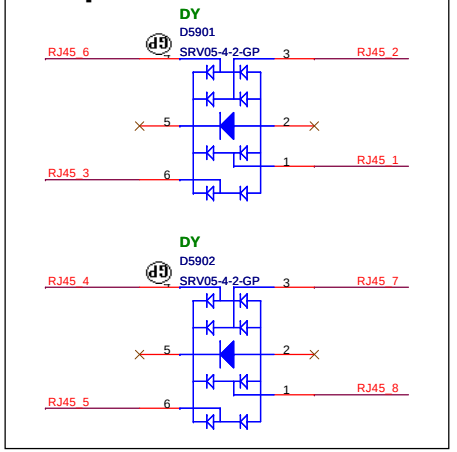
83.09904.AAE
DIODE ESD AZC099-04S SOT23-6L



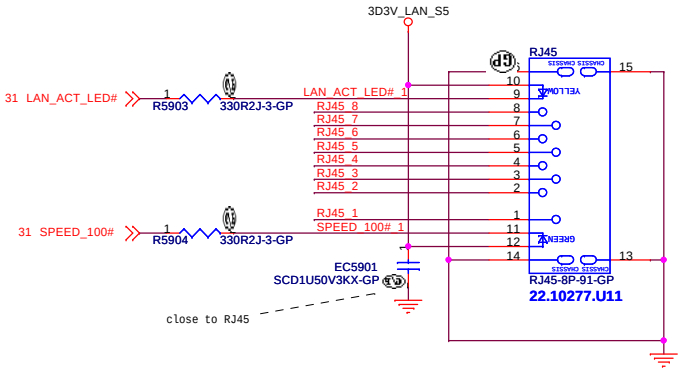
C5901 value modify to 0.01uF ~ 0.4uF capacitor

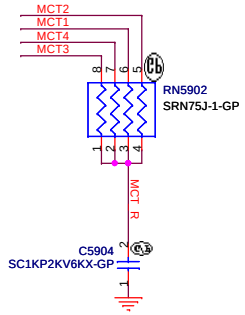
1st
68.IH601.301(Taimag) for 1000
68.HH035.301(Taimag) for 10/100
2nd
68.2413S.30A(Lankom) for 1000
68.H6441.301(Lankom) for 10/100

Swap for V480



LAN Connector





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

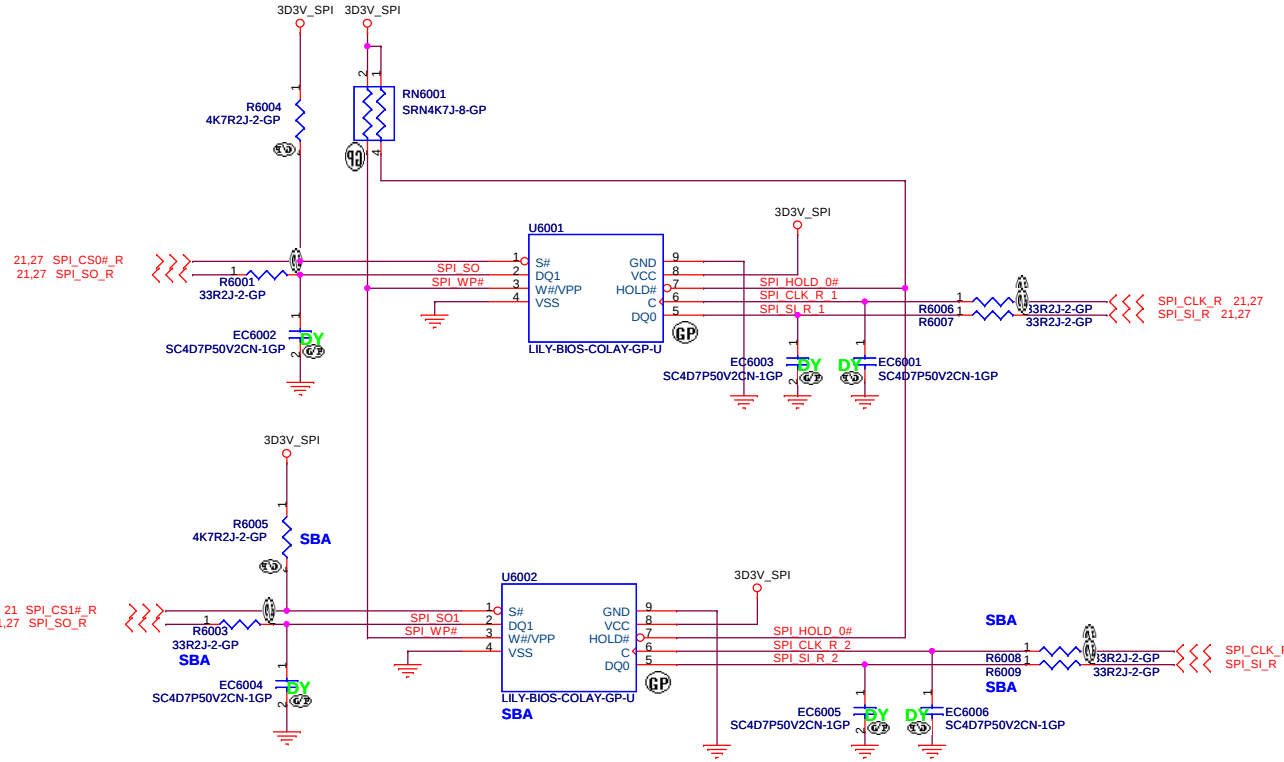
Title: RJ45 / Transformer

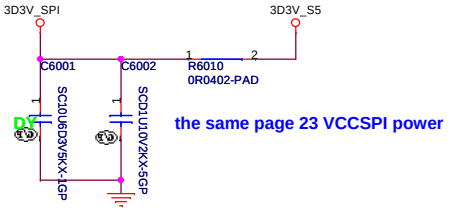
Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 59 of 103

SSID = Flash.ROM

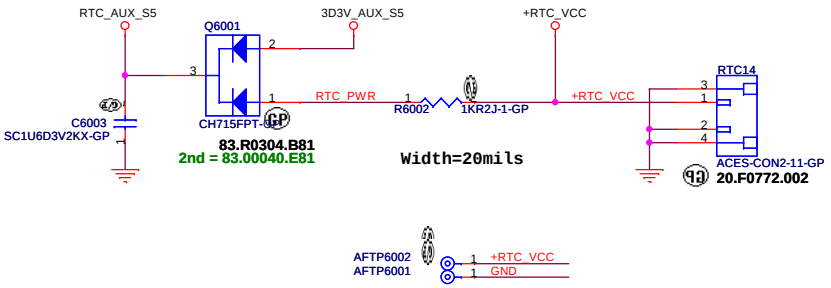
SPI FLASH ROM (8M byte) for PCH

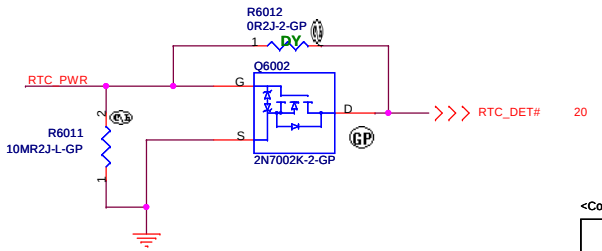




4MB			
SO8	Marcronix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marcronix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSON	Marcronix	MX25L12836EZNI-10G	72.25128.X01
		MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF840	72.25128.B03

SSID = RBATT





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

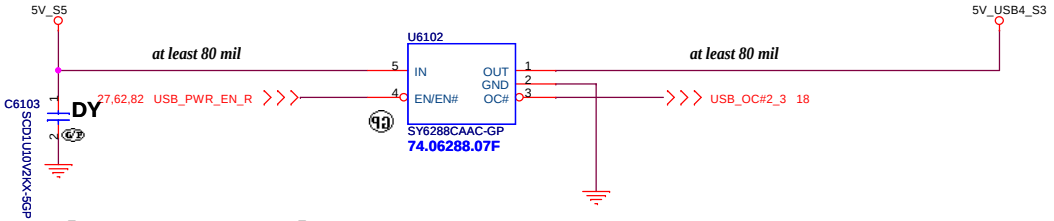
Title: Flash/RTC

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 60 of 103

USB Board CONN.

Support 2A



Place U6102 close to USBCN1

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Connector***

Size	Document Number	Rev
A3	LA480	SD

Date: Friday, January 06, 2012 Sheet 61 of 103

USB3.0 Port1

USB3.0 Port2

USB3.0 Port3

USB3.0 Port4

2A

5V_S5

C6205 27,81,82 USB_PWR_EN_R

SCD1U10V2KX-5GP

U6201

GND IN EN1# EN2# | GND OC1# OUT1 OUT2 OC2#

TPS2064DGNR-GP-U

USB_OC#0_1 18

USB_OC#4_5 18

at least 80 mil

5V_USB1_S3

5V_USB2_S3

USB1

USB2

VBUS D- D+ GND

STDA_SSRX- STDA_SSRX+ STDA_SSTX- STDA_SSTX+ GND_DRAIN

USB_PN1_R USB_PP1_R

USB_PN3_R USB_PP3_R

USB3_RX1_N_R USB3_RX1_P_R USB3_TX1_N_R USB3_TX1_P_R

USB3_RX3_N_R USB3_RX3_P_R USB3_TX3_N_R USB3_TX3_P_R

TC6201 TC6202

SKT-USB13-77-GP

22.10339.K61

TC6201 place near the USB1 connector

TC6202 place near the USB2 connector

D6204

D6201

L1#1L1#8 L2#2L2#7 GNDGND L3#3L3#6 L4#4L4#5

RCLAMP0524P-GP

1st = 83.3V3U4.0A0

R6201 R6202 R6203 R6204 R6205 R6206

R6207 R6208 R6210 R6209 R6211 R6212

0R0402-PAD

C6206 C6208 C6209 C6210

SCD1U16V2KX-3GP

D6202 D6203

PRTR5V0U2X-GP

DY

<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

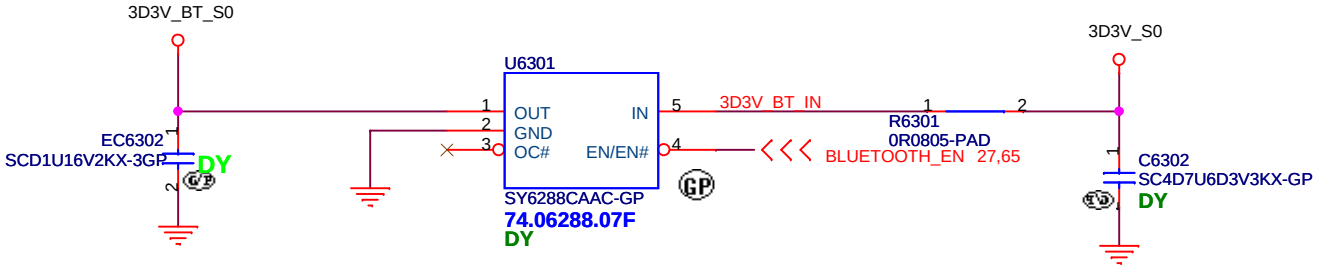
Title: USB 3.0 Port*2

Size: A2 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 62 of 103

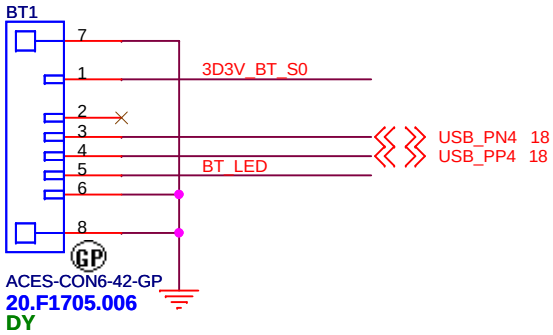
SSID = User.Interface

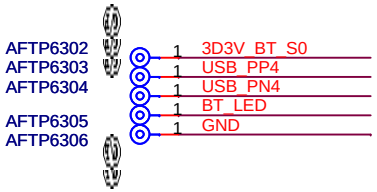
Bluetooth conn.



SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

BT Module pin definition is same as LA470





<Core Design>

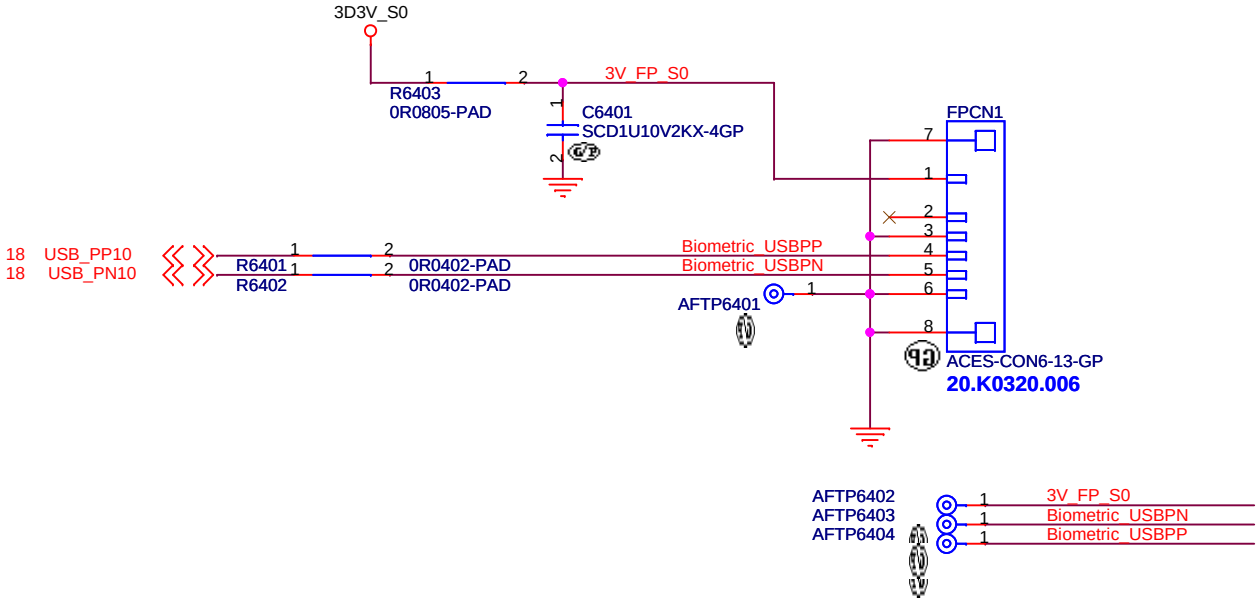
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 63 of 103

Finger Printer Connector

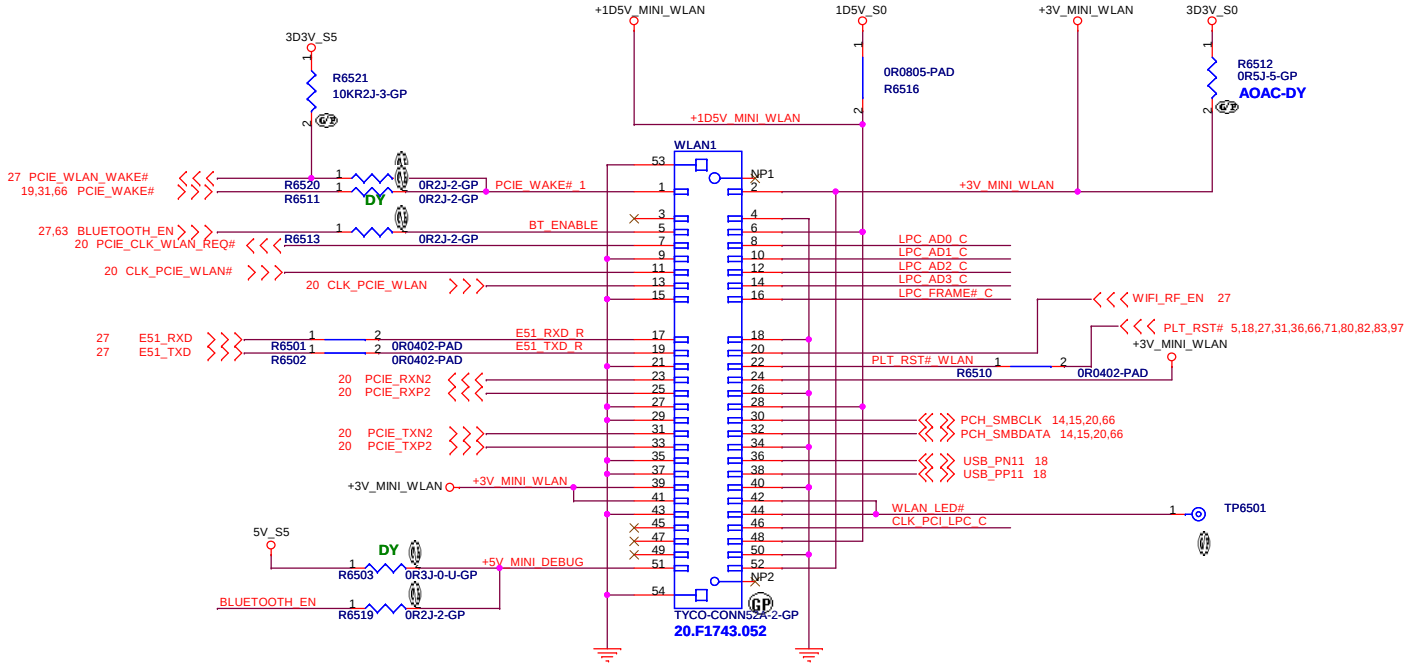


<Core Design>

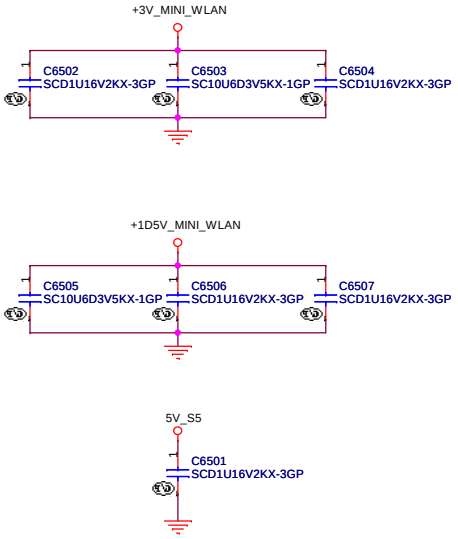
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Finger Printer Connector*		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 64 of 103	

SSID = Wireless

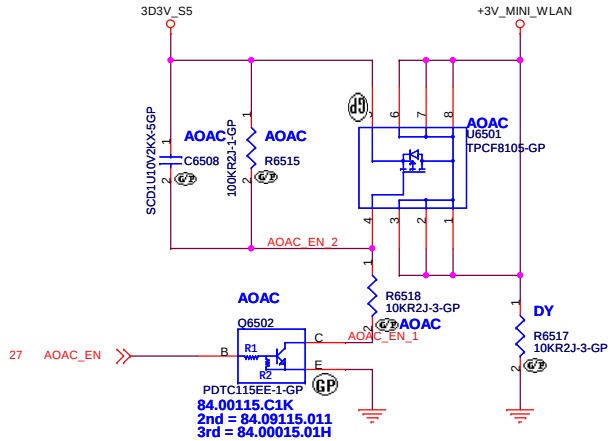
Mini Card Connector(802.11a/b/g/n)

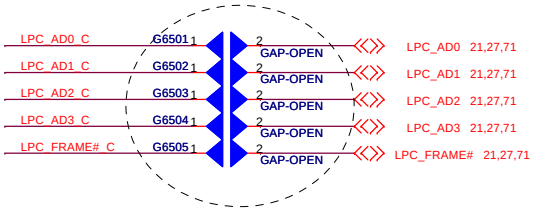


Place near MINI Card CONN



Reserve for AOAC





G6506~G6511
placememt close close WLAN1
in bottom side

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/ITP CONN

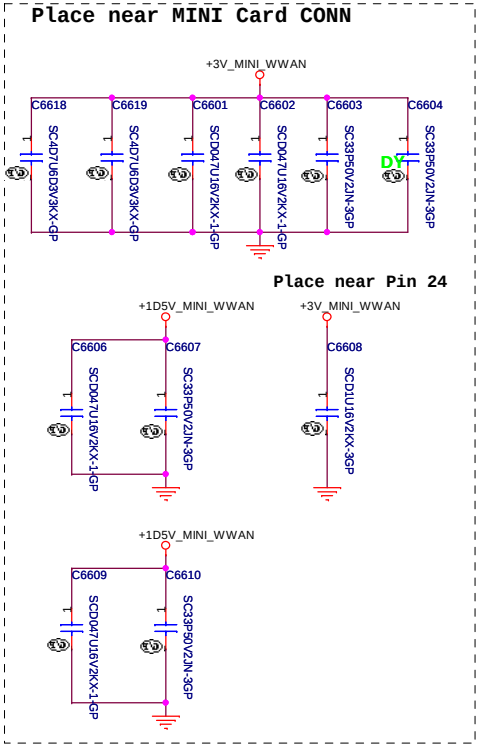
Size	Document Number	Rev
A3	LA480	SD

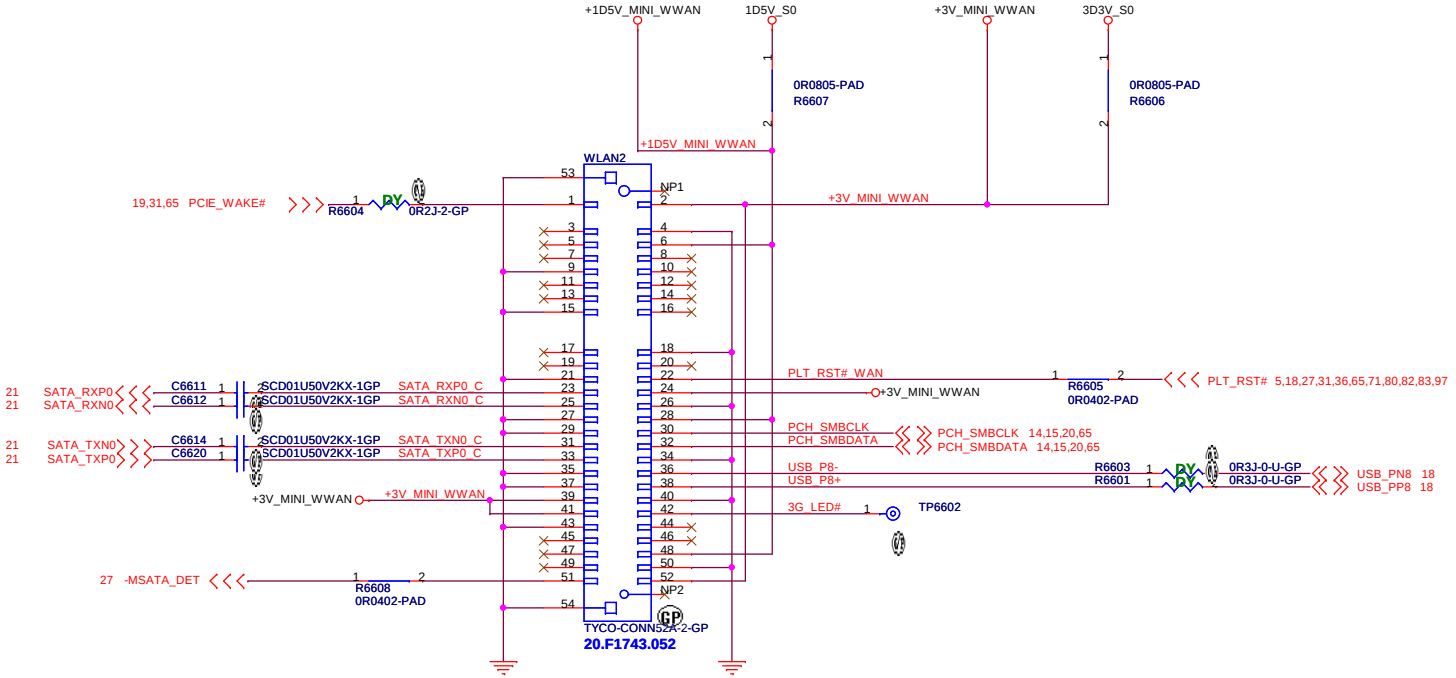
Date: Friday, January 06, 2012 Sheet 65 of 103

SSID = Wireless

mSATA for V Series Only

Mini Card Connector(Full Card)





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN Connector

Size: A3 | Document Number: LA480 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 66 of 103

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<Core Design>

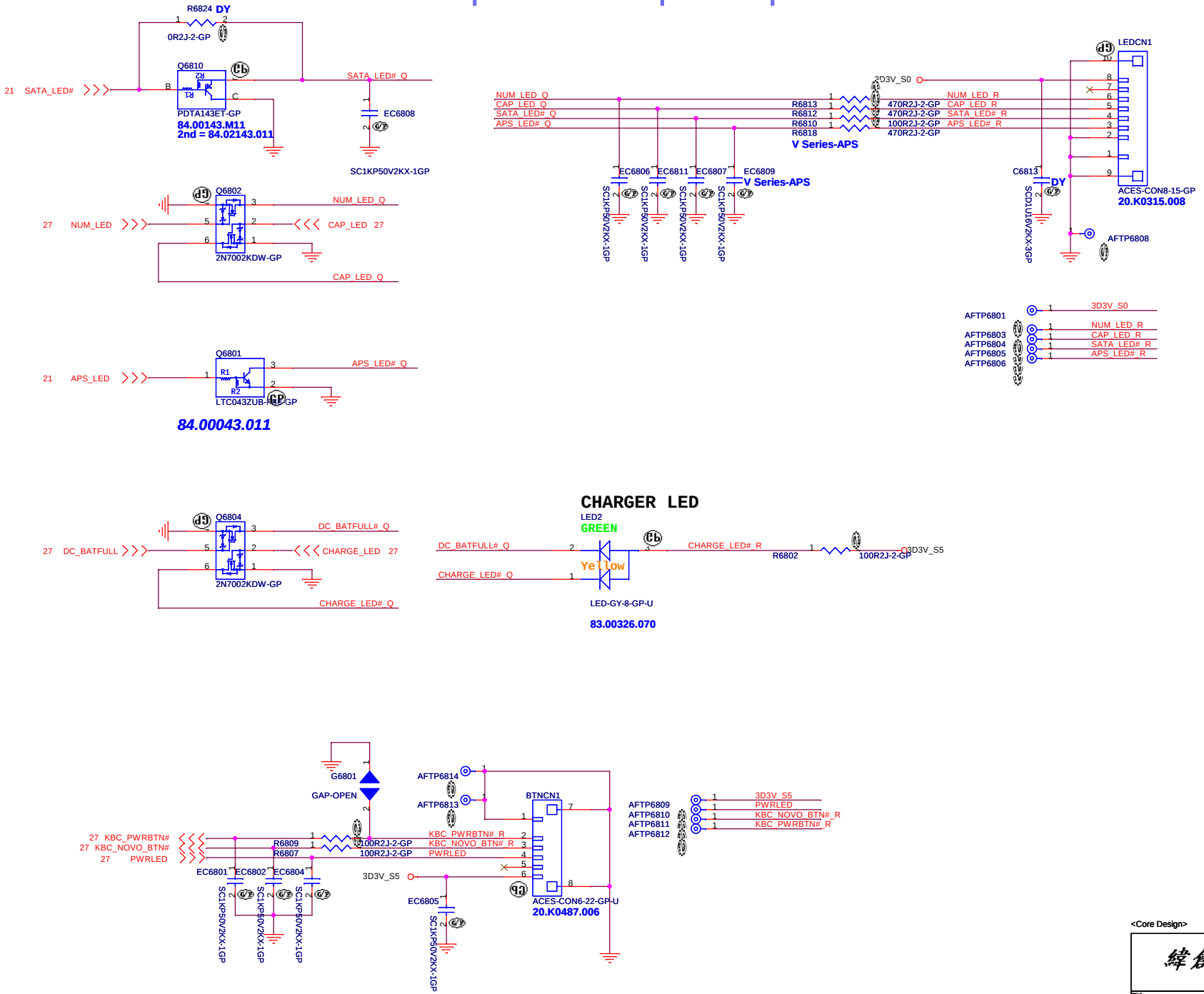
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 67 of 103

SSID = User.Interface

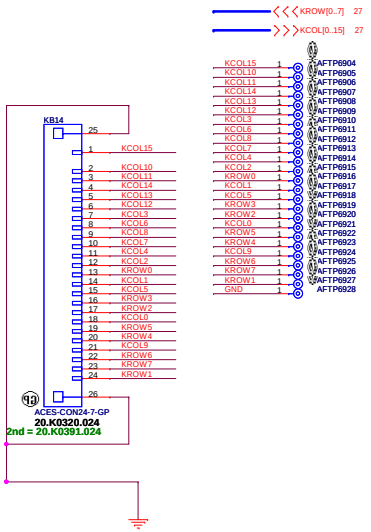


<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LED Bard/Power Button***
Size: A3	Document Number: **LA480**
Rev: **SD**	
Date: Friday, January 06, 2012	Sheet 68 of 103

SSID = KBC

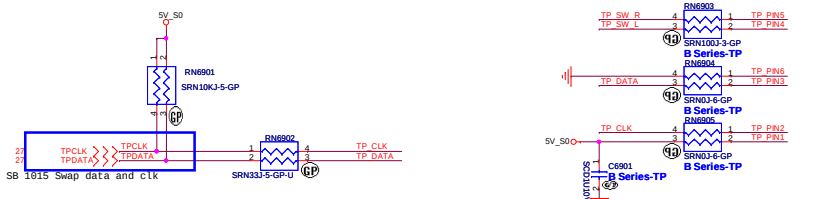
Internal KeyBoard Connector

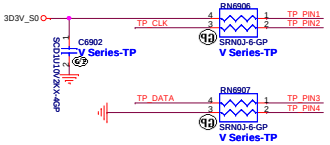


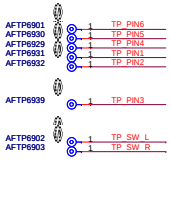
KB14 for 14" VB480 & VB485
KB15 for 15" VB580 & VB585

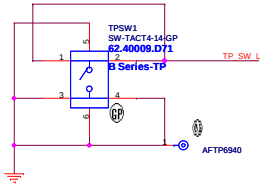
SSID = Touch.Pad

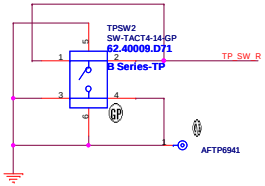
Normal Pad for B Series 5V
ClickPad for V Series 3.3V

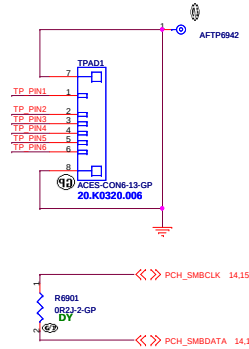












Synaptics P/N	Models			
	B480	V480	B580	V580
TM-01146-006	✓			
TM-02023-001		✓		
TM-02060-001			✓	
TM-02045-001				✓
VDD	5V	3.3V	5V	3.3V
Pin 1	VDD	VDD	VDD	VDD
Pin 2	CLK	CLK	CLK	CLK
Pin 3	DAT	DAT	DAT	DAT
Pin 4	Left button	GND	GND	GND
Pin 5	Right button	NC	Left button	NC
Pin 6	GND	NC	Right button	NC

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	S1	S2	S3	S4	S5	S6	S7	S8

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PAD CONNECTOR

Size	Document Number	Rev
A2	LA480	SD

Date: Friday, January 06, 2012 Sheet 69 of 103

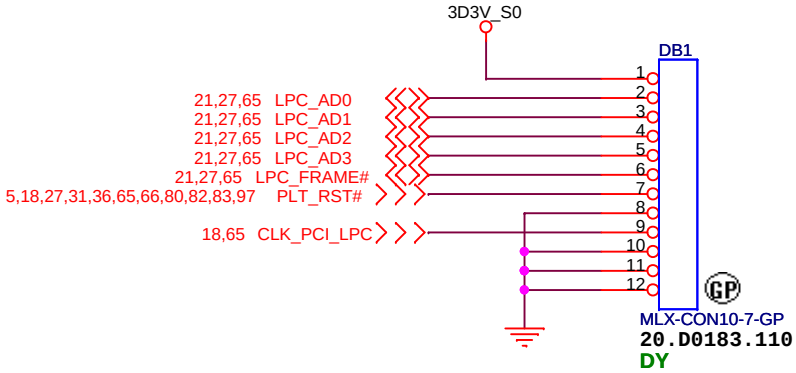
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 70 of 103



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	LA480	SD

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Size	Document Number	Rev
A4	LA480	SD

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Title: CARD Reader CONN

Size	Document Number	Rev
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Title: *New Card*

Size	Document Number	Rev
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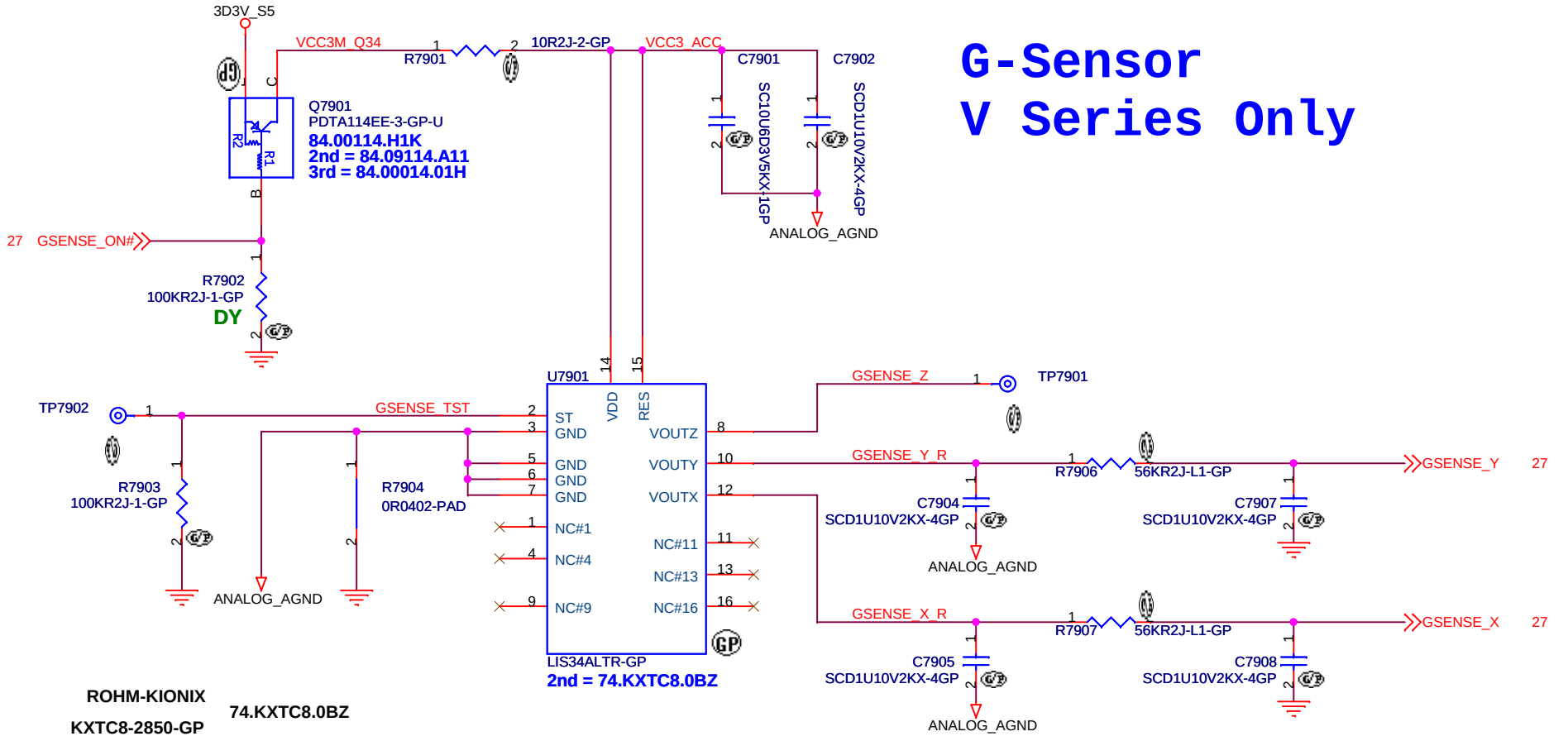
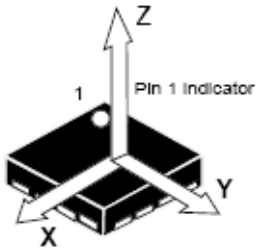
G-Sensor
V Series Only





Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

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Title: G-Sensor		
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RFID

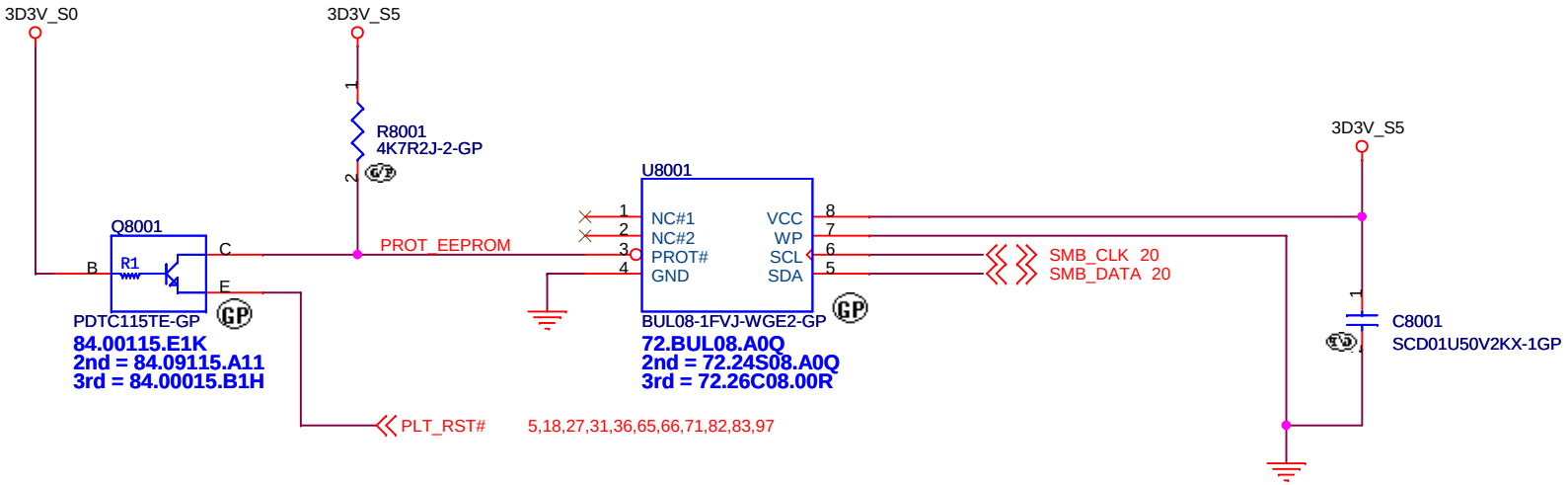

Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

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Title: **RF ID**

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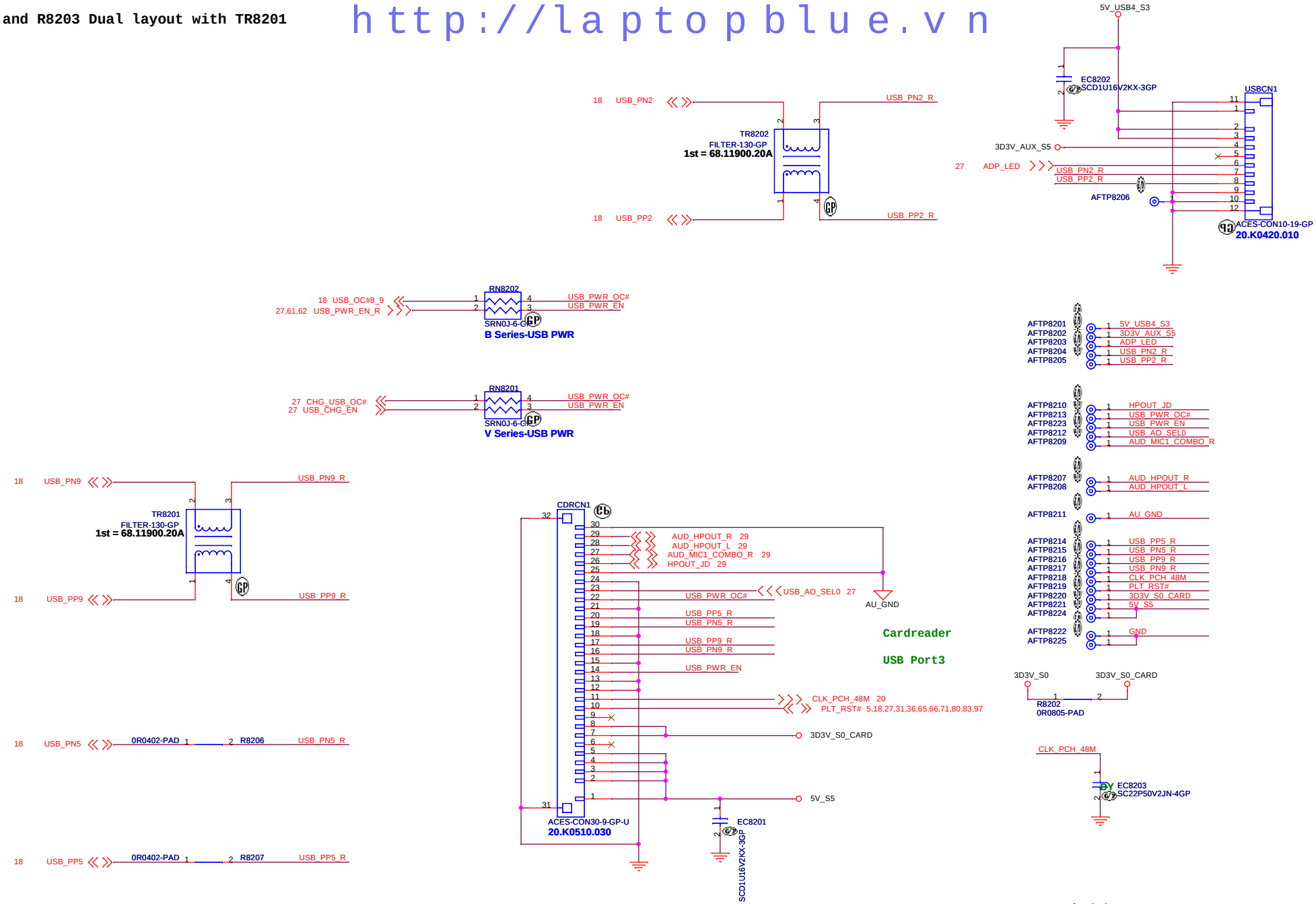
R8201 and R8203 Dual layout with TR8201



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Title: IO Board Connector

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SPEC. (DG-05587-001_v03_p.70)
PEX_CLK_REQ_N is an open-drain bi-directional signal;
by default it should have a 10 kΩ pull-up to 3.3V.
This signal is an active low signal.

PCI Express PEX_IOVVD/Q Combined (DG-05587-001_v03_p.72_Table 10)

Capacitor	Type	Footprint	Population	Location
1.0uF	X6S	0402	4	Under GPU
4.7uF	X6S	0603	2	Near GPU
10uF	X5R	0805	4	Midway Between GPU and Power Supply
22uF	X5R	0805	4	Midway Between GPU and Power Supply

X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

1.05V ±30mV 3300mA total
(DG-05587-001_v03_p.71_Table 9)

1uF(X5R) K0402 ×4 | 4.7uF(X5R) K0603 ×2 | 10uF(X5R) M0805 ×4 | 22uF(X5R) M0805 ×4

Under GPU | Near GPU | Midway Between GPU and Power Supply

SPEC. (DG-05587-001_v03_p.70)
For PCI ECPRESS connection,
please use 0.22uF,20%,0402,X5R
or better AC couplimg capacitors.

0.22uF(X5R) K0402

PCI Express PEX_SVDD/PLL_HVDD Connected to NV3V3 (DG-05587-001_v03_p.72_Table 12)

Capacitor	Type	Footprint	Population	Location
0.1uF	X5R	0402	1	Near GPU
4.7uF	X5R	0603	2	Near GPU

X5R (+/-15%、-55~85℃)

3.3V ±10% 210mA total
(DG-05587-001_v03_p.71_Table 9)

0.1uF(X5R) K0402 ×1 | 4.7uF(X5R) K0603 ×2

Near GPU

dGPU reset

SPEC. (DG-05587-001_v03_p.70)
PEX_TSTCLK_OUT should be
terminated with a 200Ω resistor.

PCI Express PEX_PLLVDD (DG-05587-001_v03_p.72_Table 11)

Capacitor	Type	Footprint	Population	Location
100nF	X6S	0402	1	Under GPU
1.0uF	X5R	0603	1	Near GPU
4.7uF	X5R	0805	1	Near GPU

X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

100nF(X7R) K0402 ×1 | 1.0nF(X5R) K0402 ×1 | 4.7nF(X5R) K0603 ×1

1.05V ±30mV 150mA total
(DG-05587-001_v03_p.71_Table 9)

Under GPU | Near GPU

Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,
Stuff bead(68.00082.001) for N13P-GL/N13M-GE

SPEC. (DG-05587-001_v03_p.214)
By default, pull-down the TESTMODE pin to GND with a 10kΩ resistor.
For XOR tree testing, TESTMODE should be pulled up to 3v3 with a 10 kΩ resistor.

SPEC. (DG-05587-001_v03_p.70)
PEX_TERMP is used for internal calibration;
pull-down this signal with 2.49 kΩ,1% resistor.

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Title: N13P_GPU (1/5): PEG

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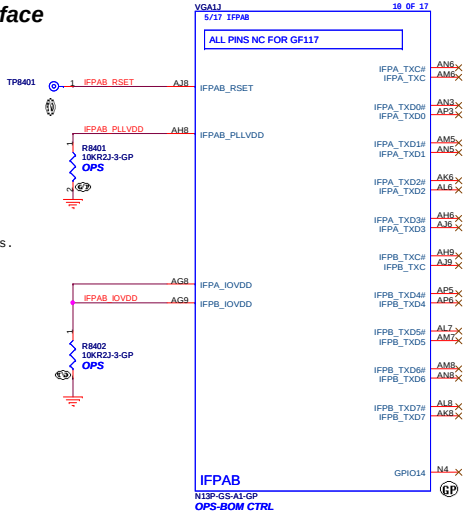
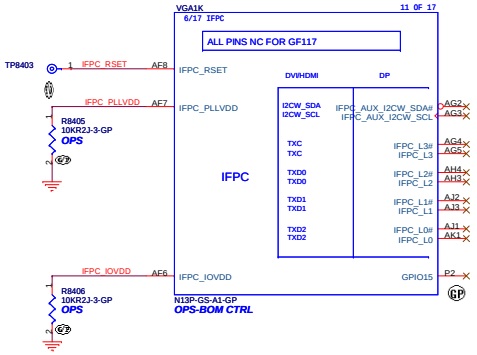
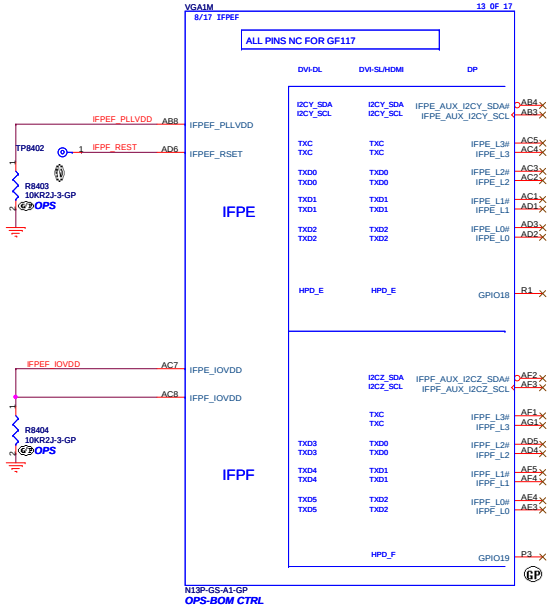
LVDS Interface

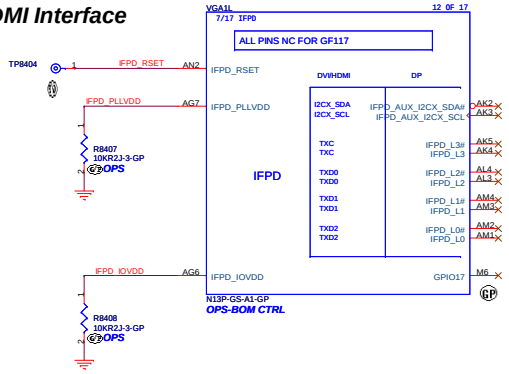
SPEC. (DG-05587-001_v03_p.160)
Pull down IFPxy IOVDD with 10kΩ resistor.
Pull down IFPxy PLLVDD with 10kΩ resistor.
The other IO pins can be NC, this includes unused data lines.







HDMI Interface



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Title	N13P_GPU (2/5): DIGITALOUT
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E1 (DA-05691-001_v03_p44_Table 2)
N13P-GL NC
N13M_GE1 NC
N13M-GS Pull down FB_CLAMP with a 10kΩ
N13P-GS Pull down FB_CLAMP with a 10kΩ

35mA
(DG-05587-001_v03_p.88_Table 25)

Mode D Command Mapping
(DG-05587-001_v03_p.78_Table 16)

N13x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		

FB CMD mapping
Mode D-N13x

FB CMD mapping
Mode D-N13x

GPU FBVDDQ Decoupling (DG-05587-001_v03_p.86_Table 22)

Capacitor	Type	Footprint	Population	Location
0.1uF	X7R	0402	8	Under GPU
1uF	X7R	0603	2	Under GPU
4.7uF	X6S	0603	2	Under GPU
10uF	X5R	0805	4	Near GPU

X7R (+/-15%、-55~125℃)
X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

0.1uF(X7R)
K0402 ×8
Under GPU
1uF(X7R)
K0603 ×4
Near GPU
4.7uF(X5R)
K0603 ×2
10uF(X5R)
M0805 ×2

Default GPU Drive Calibration for DDR3 (DG-05587-001_v03_p.82_Table 17)

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PU_VDDQ	FBCAL_TERM_GND
DDR3	1.5V	42.2Ω	40.2Ω	51.1Ω

*Use only 1% resistors for driver calibration.

66mA
(DG-05587-001_v03_p.88_Table 25)
1.05V ±30mV 167mA total
100nF(X7R)
K0402 ×3
Under GPU

66mA
(DG-05587-001_v03_p.88_Table 25)

Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,
Stuff bead(68.00084.H41) for N13P-GL/N13M-GE

FBx_PLL_AVDD, FB_DLL_AVDD and PLLVDD combined
(DG-05587-001_v03_p.88_Table 26)

Capacitor	Type	Footprint	Population	Location
100nF	X7R	0402	1 per pin	Under GPU
22uF	X5R	0805	1	Near GPU
Bead Type				
30Ω @100MHz (ESR=0.01Ω)		0603	1	Near GPU

X7R (+/-15%、-55~125℃)
X5R (+/-15%、-55~85℃)

FBCLK Termination placed at each VRAM (DG-05587-001_v03_p.83_Table 19)

Memory ODTx, CKEx and RST Termination (DG-05587-001_v03_p.84_Table 20)

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Title: N13P_GPU (3/5): VRAM I/F
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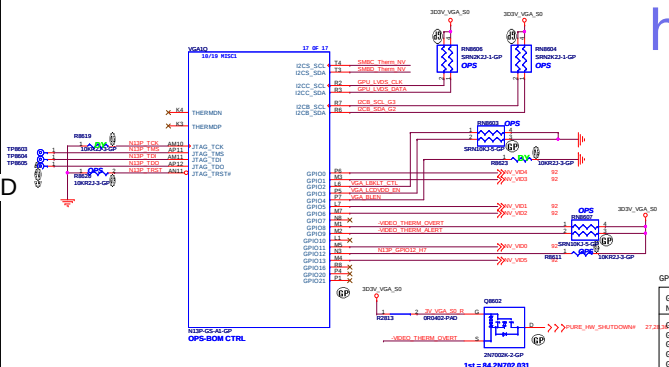
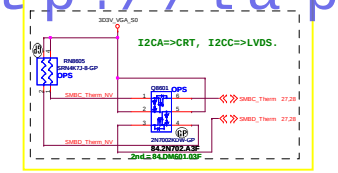
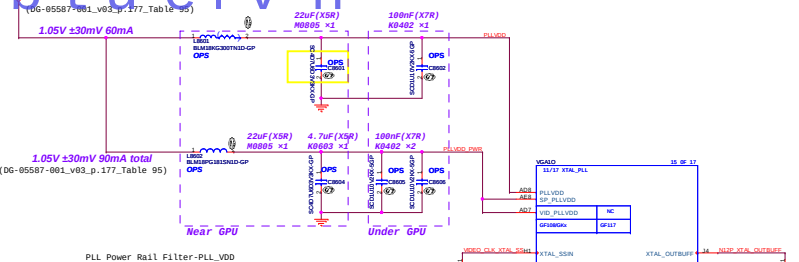




GPIO Description (DG-05587-001_v03_p.82_Tale 98)

GPIO pin Name	Normal Function	I/O	Function Description
GPIO0	GPU_VID4	O	GPU Core VDD VID4
GPIO1	GPU_VID3	O	GPU Core VDD VID3
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control
GPIO3	LCD_VCC	O	Panel Power Enable
GPIO4	LCD_BLEN	O	panel Backlight Enale
GPIO5	GPU_VID1	O	GPU Core VDD VID1
GPIO6	GPU_VID2	O	GPU Core VDD VID2
GPIO7	3D Vision	O	3D Vision Left/Right signal
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	I/O	Active Low Thermal Alert
GPIO10	MEM_VREF_CTL	O	Memory VREF Control
GPIO11	GPU_VID0	O	GPU Core VDD VID0
GPIO12	PWR_LEVEL	I	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	O	GPU Core VDD VID5
GPIO14	HPD_AB	I	Hot Plug Detect for IFPAB
GPIO15	HPD_C	I	Hot Plug Detect for IFPC
GPIO16	MEM_VDD_CTL	O	Memory VDD VID
GPIO17	HPD_D	I	Hot Plug Detect for IFPD
GPIO18	HPD_E	I	Hot Plug Detect for IFPE
GPIO19	HPD_F	I	Hot Plug Detect for IFPF
GPIO20	Reserved		
GPIO21	Reserved		



PLL Power Rail Filter-PLL_VDD
(DG-05587-001_v03_p.177_Table 96)

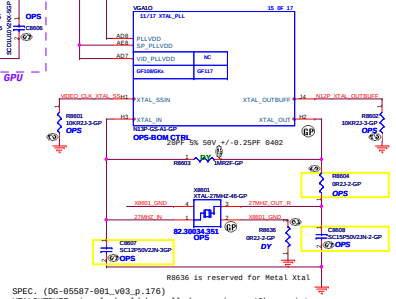
Capacitor Type		Footprint	Population	Location
100nF 22uF	X7R X7R	0402 0805	1 1	Under GPU Near GPU
Bead Type				
30Ω(ESR=0.05)		0402	1	Near GPU

X7R (+/-15%、-55~125℃)

PLL Power Rail Filter-SP_PLLVDD and VIDPLLVDD Combined
(DG-05587-001_v03_p.178_Table 97)

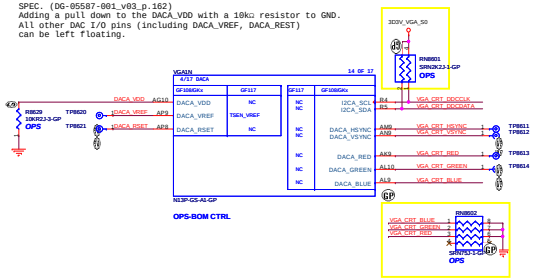
Capacitor Type		Footprint	Population	Location
100nF 4.7uF 22uF	X7R X7R X7R	0402 0402 0805	2 1 1	Under GPU Near GPU Near GPU
Bead Type				
180Ω(ESR=0.2)		0603	1	Near GPU

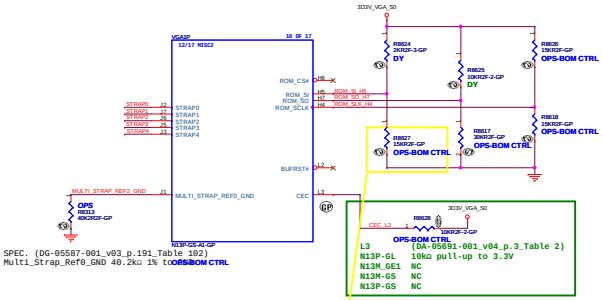
X7R (+/-15%、-55~125℃)



SPEC. (DG-05587-001_v03_p.176)
XTALOUTBUFF signal should be pull down using a 10kΩ resistor.
XTALSSIN signal should be pull down using a 10kΩ resistor.
REmember to place components as close ti the GPU as possible.

SPEC. (DG-05587-001_v03_p.162)
Adding a pull down to the DACA_VDD with a 10kΩ resistor to GND.
All other DAC I/O pins (including DACA_VREF, DACA_REST)
can be left floating.





SPEC. (DG-05587-001_v03_p.191_Table 102)
Multi_Strap_Ref0_GND 40.2kΩ 1% to GND

L3 (DA-05091-001_v04.p.3_Table 2)
N13P-GL 10kΩ pull-up to 3.3V
N13M_GE1 NC
N13M-GS NC
N13P-GS NC

The GB4-128 package is available in a 29 mm × 29mm footprint.
128-bit memory interfaces respectively.

Recommended NVVDD Voltage Regulator Phase Coount

GPU SKU	Phase Count Target
N13M-GE1	Single phase
N13M-GS	Two phase
N13P-GL	Two phase
N13P-GS	Two phase

29 x 29 PACKAGE
V: N13P-GS/GL (25~30w)
B: N13M-GS/GE (15~20w)

128Mx16:

hynix - H5TQ2G63BFR-11C
Samsung - K4W2G1646C-HC11

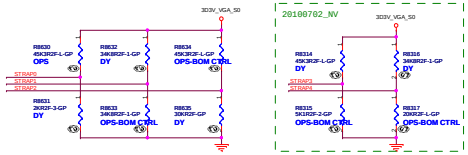
64Mx16:

Hynix - H5TQ1G63DFR-11C
Samsung - K4W1G1646G-BC11

TABLE VIDEO MEMORY

	HYNIX 128Mx16 0110	SAMSUNG 128Mx16 0111	HYNIX 64Mx16 0010	Samsung 64Mx16 0011
900MHz	72.52G63.A0U 1-007155	72.42164.D0U 1-007156	72.51G63.H0U 1-007157	72.41164.Q0U 1-007356
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

	TABLE NVIDIA	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: 0x0DF7(ES)	N12M-GE DEV ID: 0xA7A 1010
STRAP1	R8632	DY	DY	35Kohm 64.34825.6DL
	R8633	35Kohm 64.34825.6DL	35Kohm 64.34825.6DL	DY
STRAP2	R8634	DY	45Kohm 64.45325.6DL	15Kohm 64.15025.6DL
	R8635	30Kohm 64.30025.6DL	DY	DY



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Title: N13P_GPU (4/5): GPIO/STRAP
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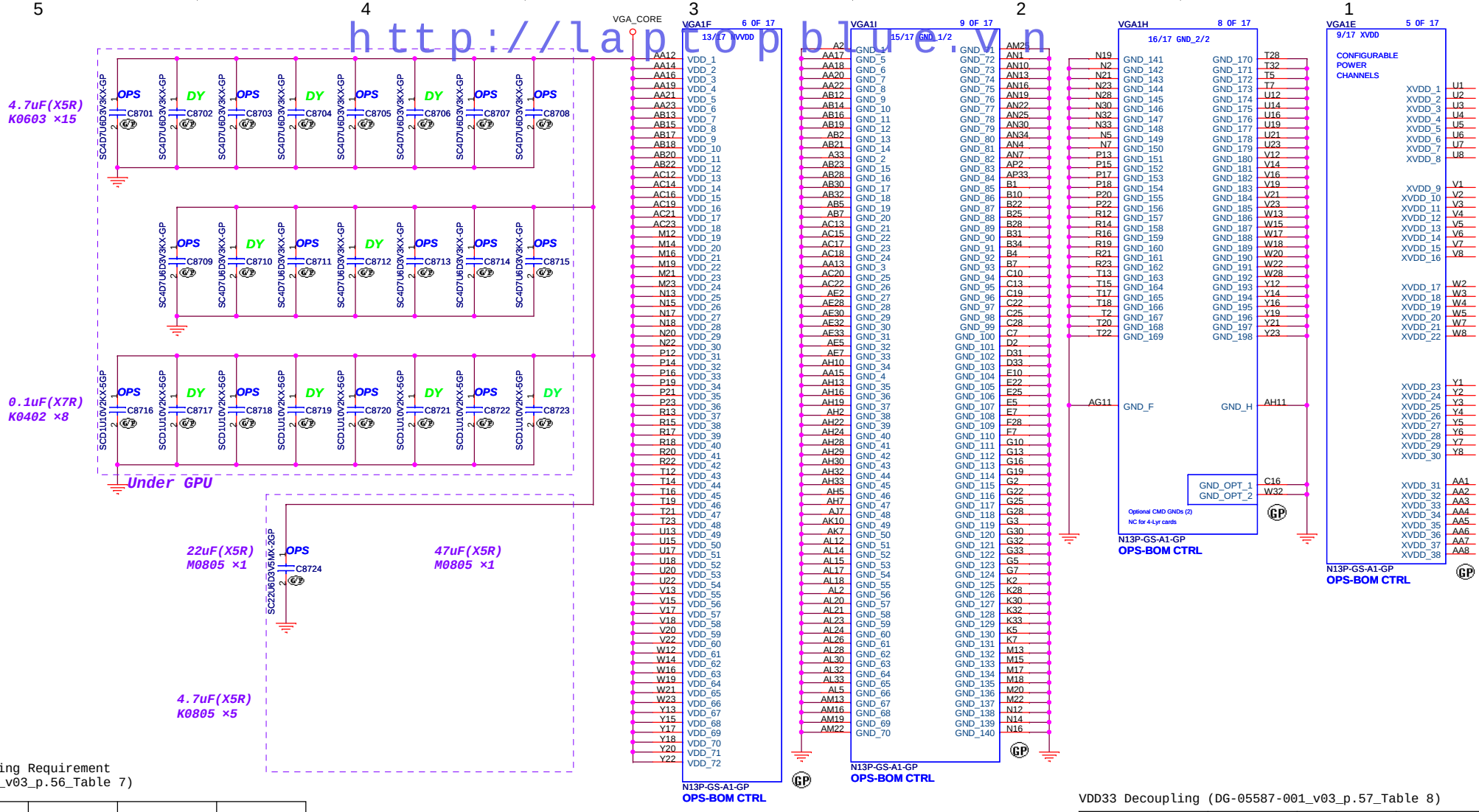
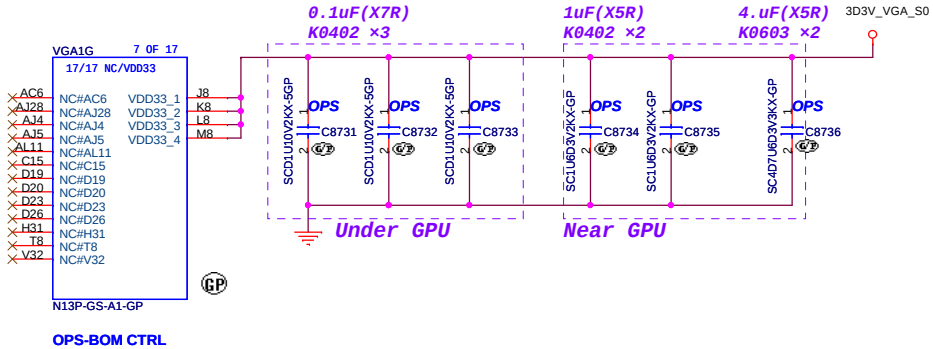


NVVDD Decoupling Requirement
(DG-05587-001_v03_p.56_Table 7)

Capacitor Type		Footprint		Population	Location
4.7uF	X6S	0603	15	10	Under GPU
0.1uF	X7R	0402	8	4	Under GPU
47uF	X5R	0805	1	1	Near GPU
22uF	X5R	0805	1	1	Near GPU
4.7uF	X5R	0805	5	5	Near GPU

X7R (+/-15%、-55~125℃)
X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)



VDD33 Decoupling (DG-05587-001_v03_p.57_Table 8)

Capacitor Type		Footprint		Population	Location
0.1uF	X7R	0402	3	3	Under GPU
1uF	X5R	0402	2	2	Near GPU
4.7uF	X5R	0603	1	1	Near GPU

X7R (+/-15%、-55~125℃)
X5R (+/-15%、-55~85℃)

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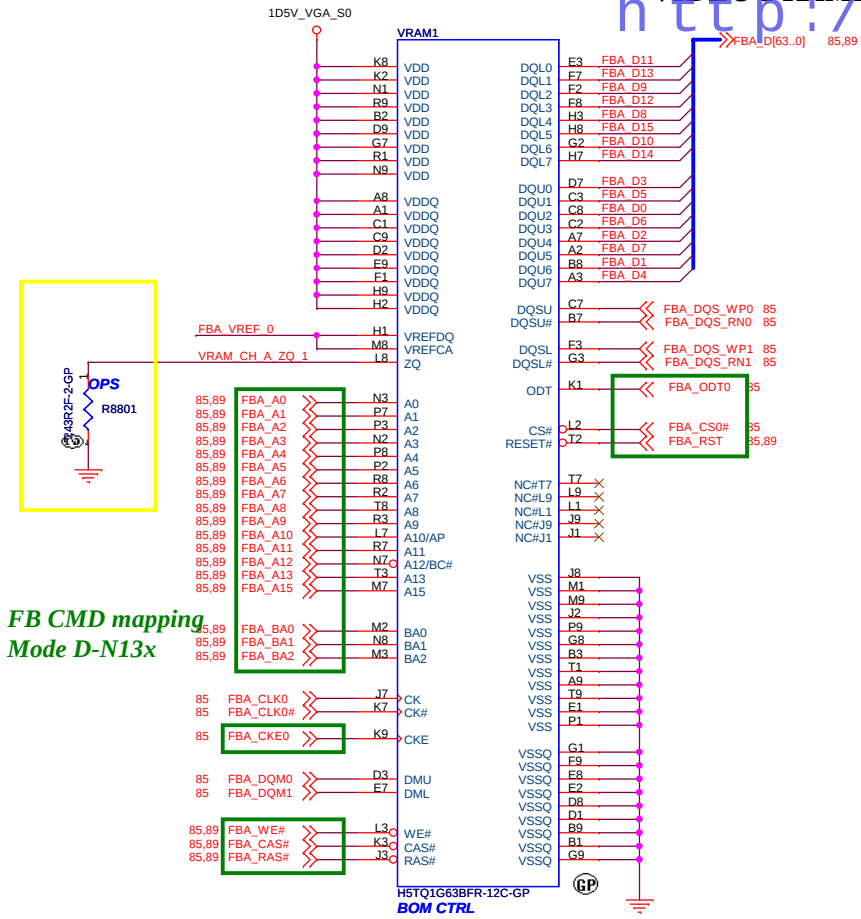
Taipei Hsien 221, Taiwan, R.O.C

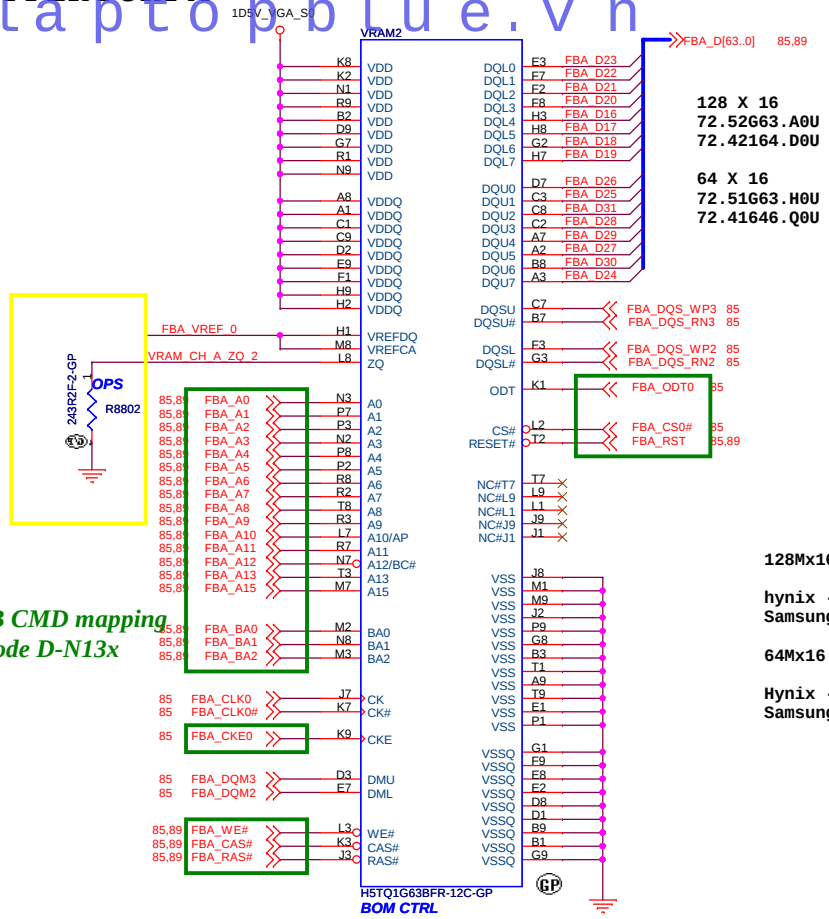
Title: N13P_GPU (5/5): PWR/GND

Size	Document Number	Rev
A3	LA48	SD

Date: Friday, January 06, 2012 Sheet 87 of 103

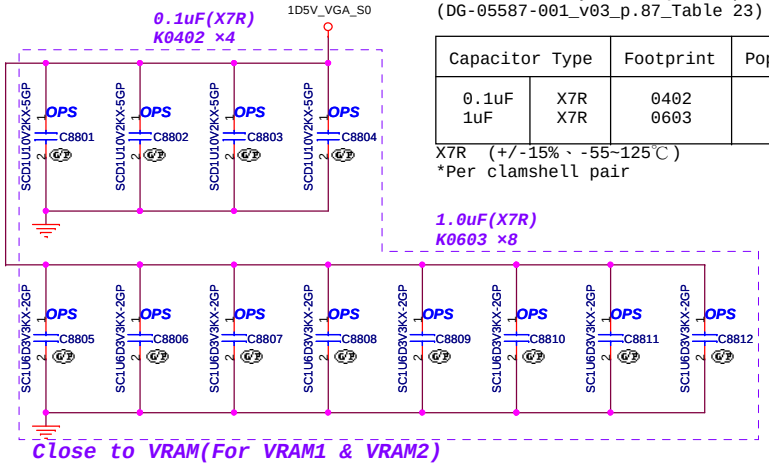
VIDEO FRAME BUFFER PORT A






```
128 X 16
72.52G63.A0U
72.42164.D0U  IC VRAM K4W2G1646C-HC11 FBGA96

64 X 16
72.51G63.H0U  IC VRAM H5TQ1G63DFR-11C FBGA 96BALLS
72.41646.Q0U  IC VRAM K4W1G1646G-BC11 FBGA 96BALLS
```

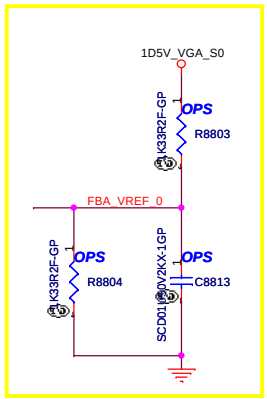
```
128Mx16:

hynix - H5TQ2G63BFR-11C
Samsung - K4W2G1646C-HC11

64Mx16:

Hynix - H5TQ1G63DFR-11C
Samsung - K4W1G1646G-BC11
```



Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair



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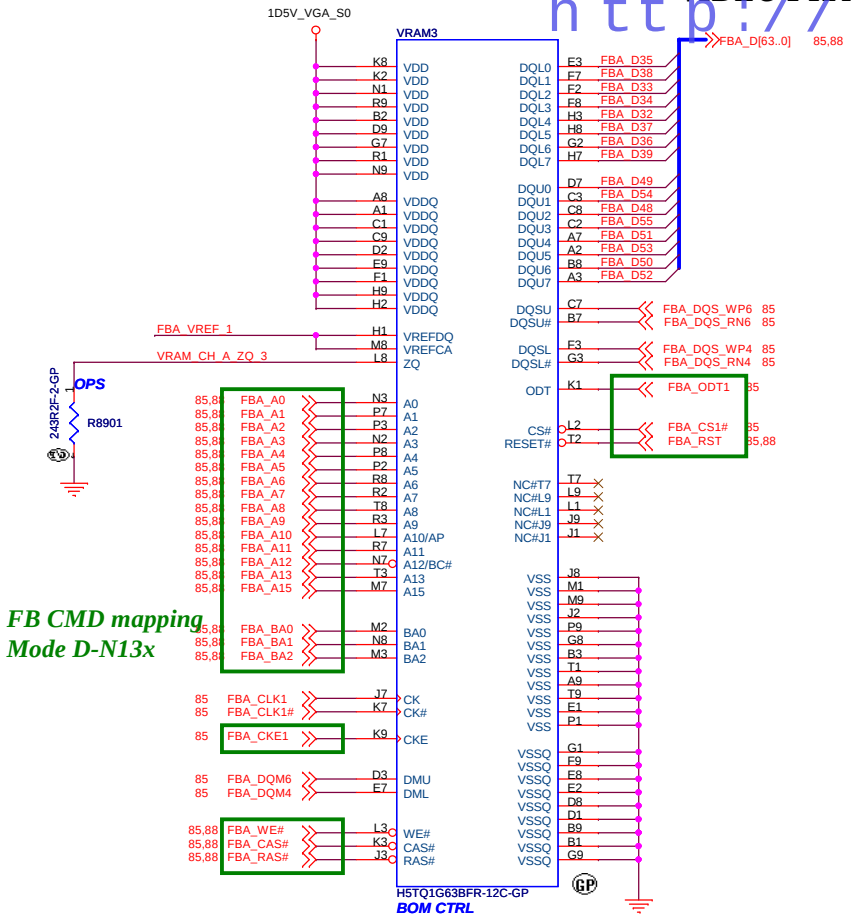
Taipei Hsien 221, Taiwan, R.O.C.

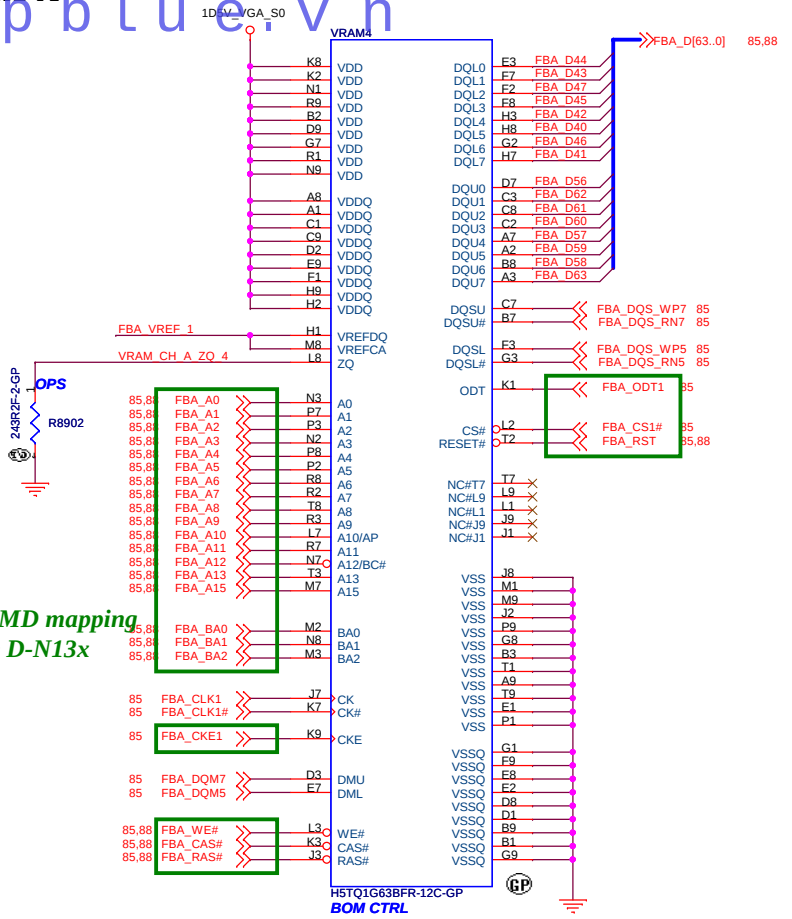
Title: CHANNEL-A_VRAM1,2 (1/4)

Size	Document Number	Rev
A3	LA48	SD

Date: Friday, January 06, 2012 Sheet 88 of 103

VIDEO FRAME BUFFER PORT A

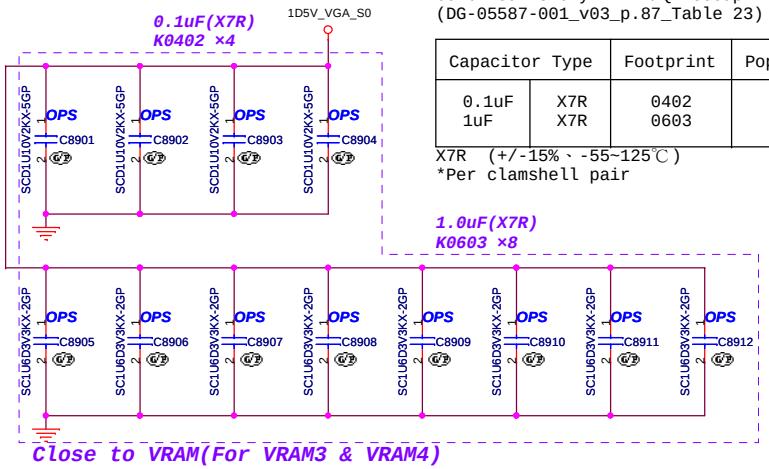


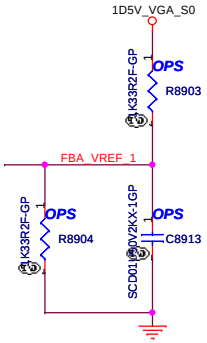


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair





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Title: CHANNEL-A_VRAM3,4 (2/4)

Size: A3 | Document Number: LA48 | Rev: SD

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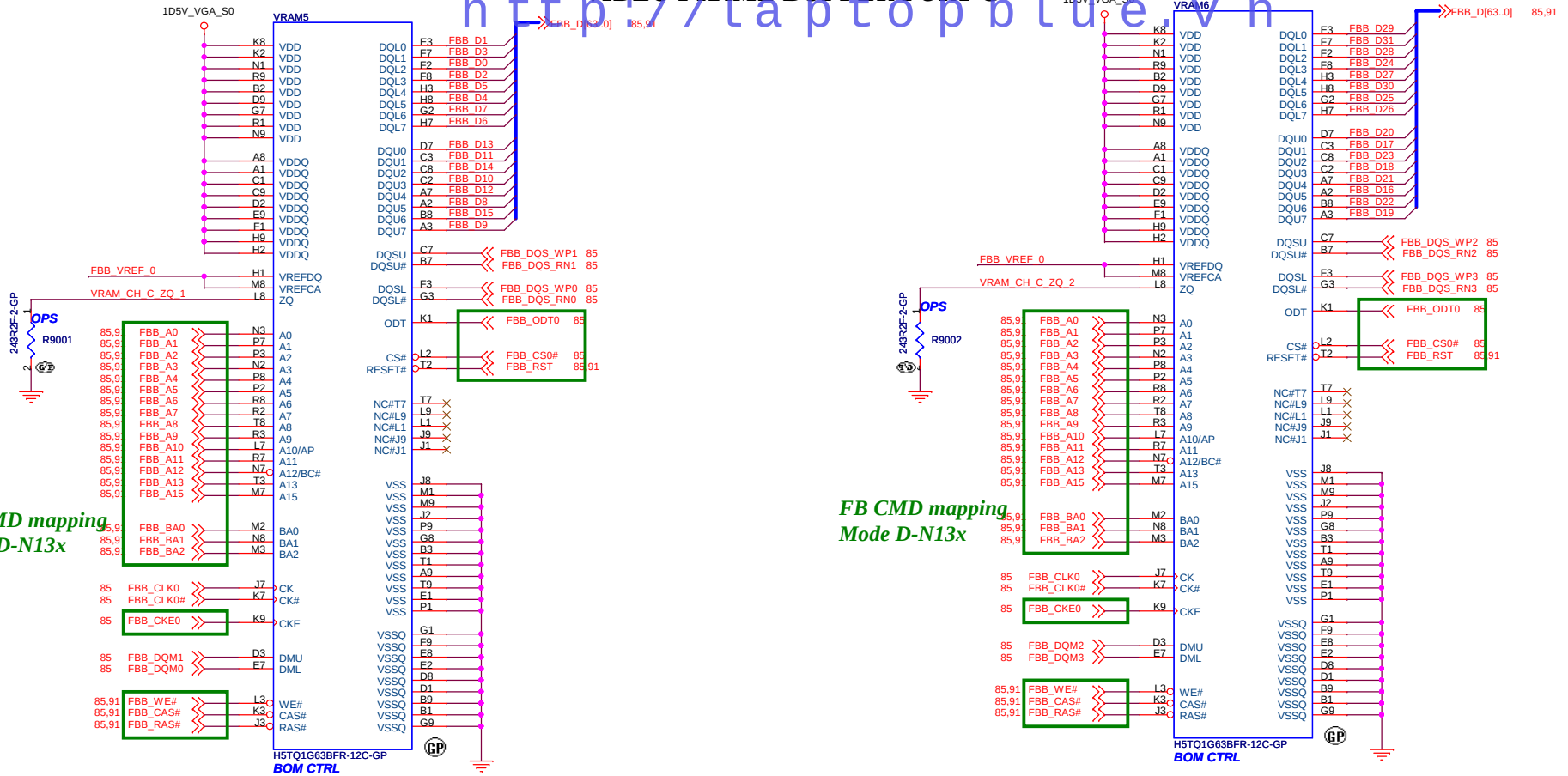
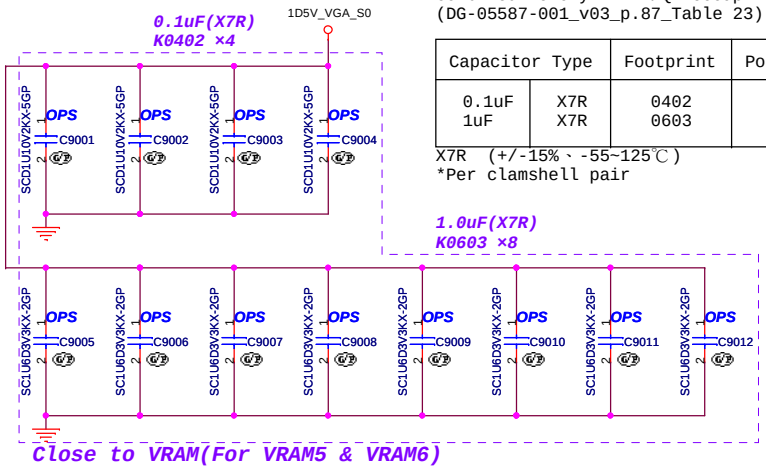
VIDEO FRAME BUFFER PORT C

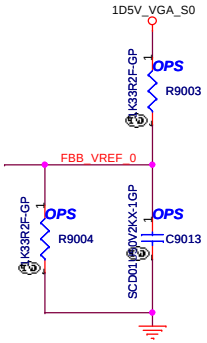


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair





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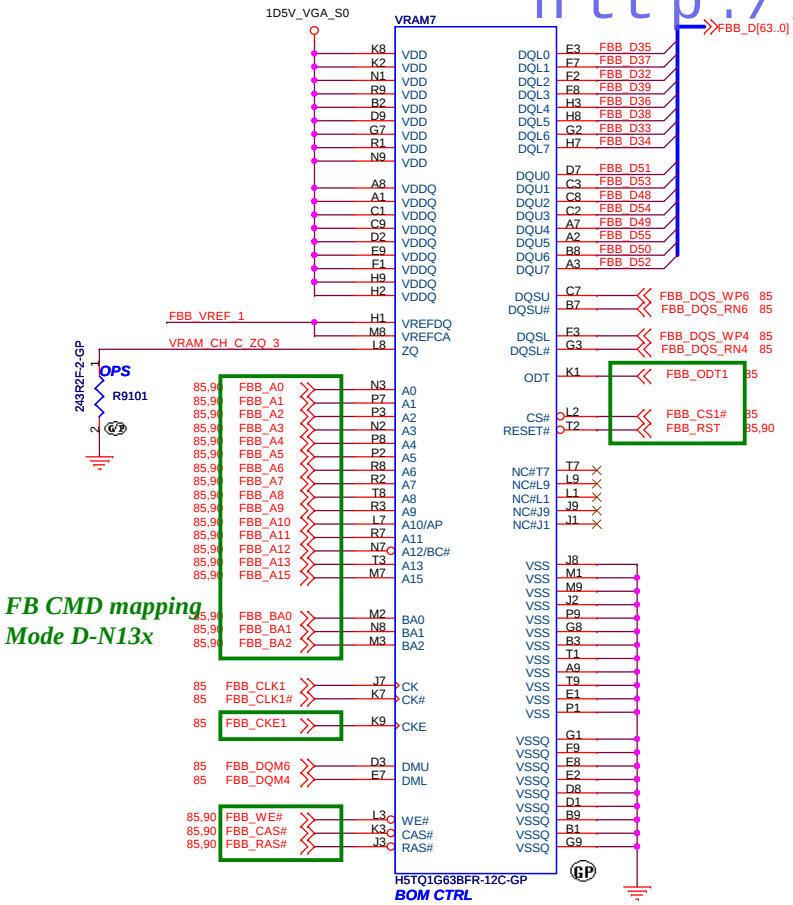
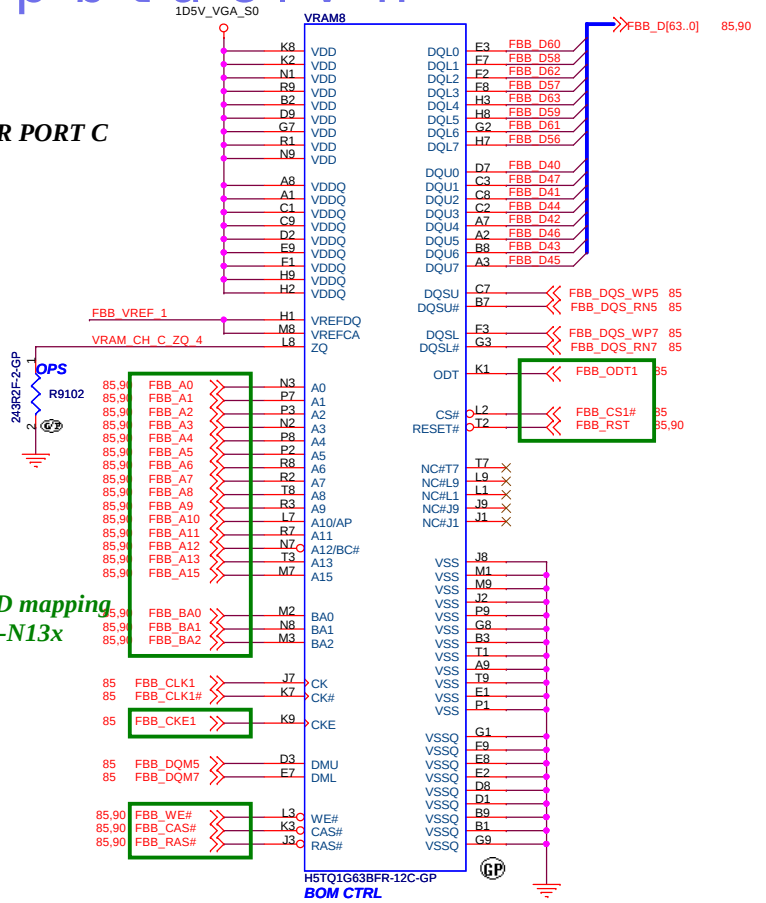
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHANNEL-C_VRAM5,6 (3/4)	
Size A3	Document Number LA48	Rev SD
Date: Friday, January 06, 2012	Sheet 90 of 103	

VIDEO FRAME BUFFER PORT C

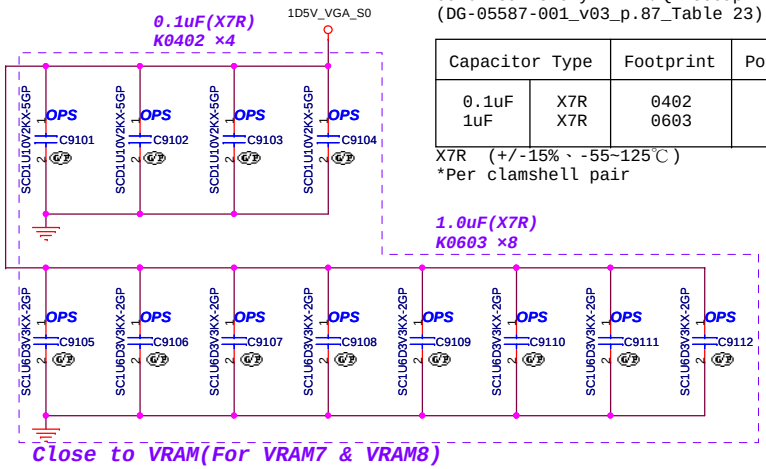


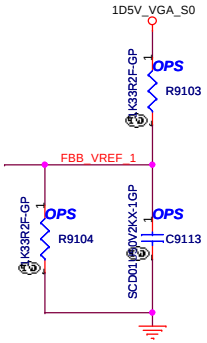


Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125℃)
*Per clamshell pair





<Core Design>

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Title: CHANNEL-C_VRAM7,8 (4/4)

Size: A3 | Document Number: LA48 | Rev: SD

Date: Friday, January 06, 2012 | Sheet 91 of 103

SSID = PWR.Plane.Regulator_GFX

	Main source	2nd source
PU9202	84.03606.037 FDMS3606S-GP-U	
PU9206	84.03606.037 FDMS3606S-GP-U	

BOM control

		N13P-GS 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U	N13M-GE1 71.0N13M.C0U
NVVDD Boot Voltage		0.9V VID[6:0]=0110000	0.975V VID[6:0]=0101010	0.9V VID[6:0]=0110000	0.875V VID[6:0]0110010
NV_VID1	PR9215	DY	63.10334.1DL	DY	63.10334.1DL
	PR9230	63.10334.1DL	DY	63.10334.1DL	DY
NV_VID3	PR9217	DY	63.10334.1DL	DY	DY
	PR9232	63.10334.1DL	DY	63.10334.1DL	63.10334.1DL
NV_VID4	PR9218	63.10334.1DL	DY	63.10334.1DL	63.10334.1DL
	PR9233	DY	63.10334.1DL	DY	DY

Q1: Id=11A, Qg=10~14nC, Rdson=7.5~9.8 mohm
Q2: Id=23A, Qg=27~38nC, Rdson=1.7~2.1 mohm

Panasonic. 0.36uH 10*11.5*4
DCR=1.1mohm
Idc=17A, Isat=24A

<Core Design>

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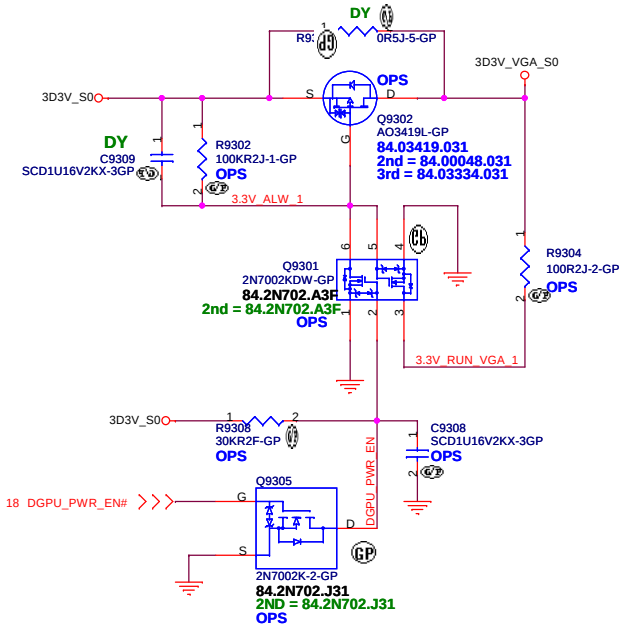
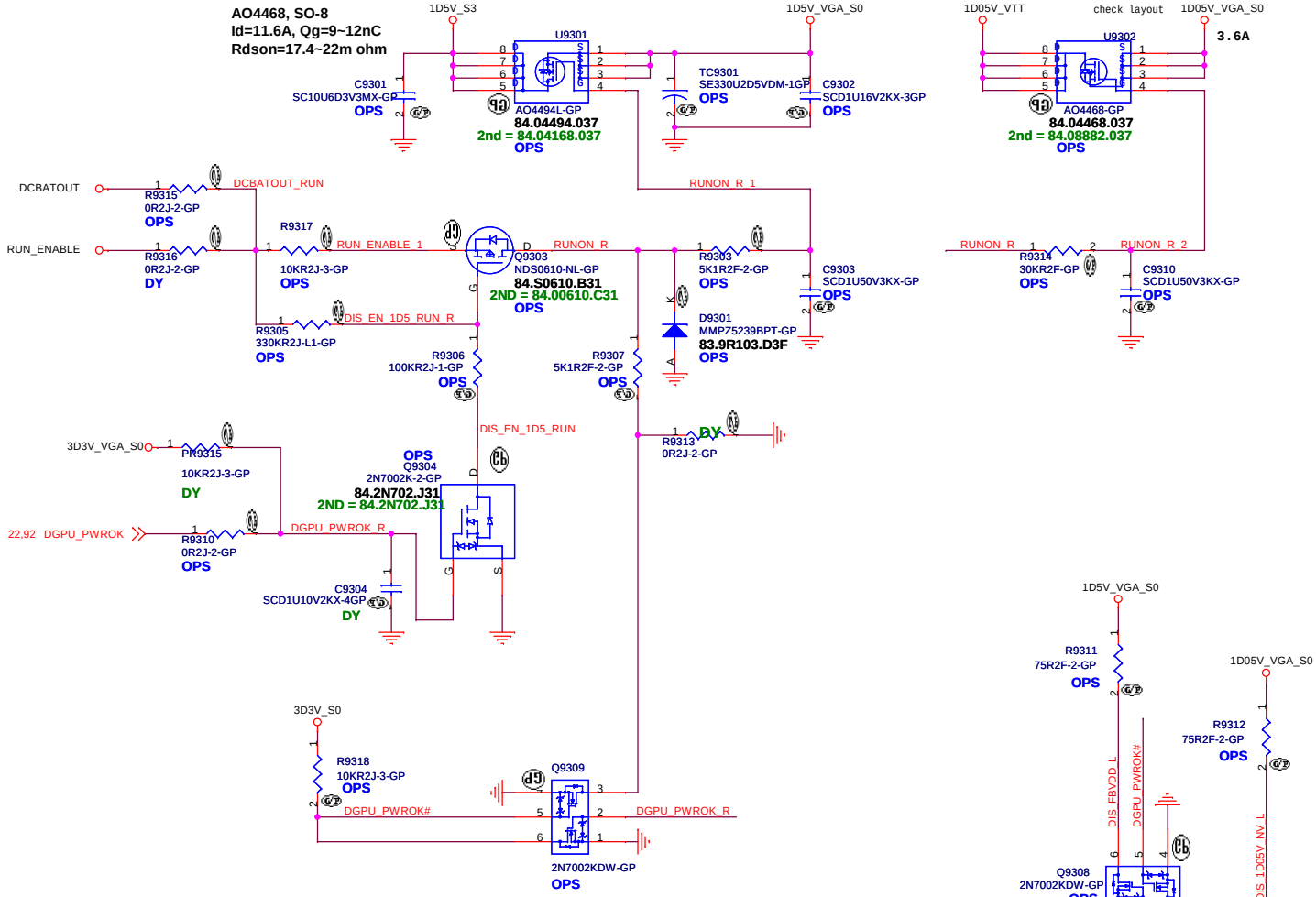
Title: TPS51728_VGA_CORE
Size: Document Number: <Doc> Rev: SD
Date: Friday, January 06, 2012 Sheet 92 of 103

+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm



1.05V to 1.05V_VGA_S0 Transfer

<Core Design>

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Title: DISCRETE VGA POWER		
Size: A3	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 93 of 103	

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緯創資通
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

Title: <Title>		
Size: A4	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet 94 of 103	

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Title: ***Reserved***

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 95 of 103

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緯創資通 Wistron Corporation
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Title

TOUCH PANEL

Size	Document Number	Rev
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CPU Plate

H14 HOLET157B276R134-GP ZZ.SCREW.091
H15 HOLET157B276R134-GP ZZ.SCREW.091
H16 HOLET157B276R134-GP ZZ.SCREW.091
H17 HOLET157B276R134-GP ZZ.SCREW.091

VGA Std-Off

H1 STF237R128H42-1-GP 34.4GD01.001
H2 STF237R128H42-1-GP 34.4GD01.001
H21 STF237R128H42-1-GP 34.4GD01.001

MINI PCIE

H18 STF256R89H178-GP 34.4B417.001

DCBATOUT
EC9729 SCD1U25V2KX-GP
EC9727 SCD1U25V2KX-GP
EC9728 SCD1U25V2KX-GP
VCCSA
EC9730 SC1KP50V2KX-1GP
DY EC9731 SCD1U25V2KX-GP
DY EC9732 SCD1U25V2KX-GP
DY EC9733 SCD1U25V2KX-GP
XDP_DBRESET# 5,19
H_CPUPWRGD 5,22
PLT_RST# 5,18,27,31,36,65,66,71,80,82,83

14" Structure boss

H3 HOLE256R115-GP ZZ.00PAD.D11
H4 HOLE256R115-GP ZZ.00PAD.D11
H5 HOLE315X315R91-S1-GP ZZ.00PAD.581
H7 HOLE355X355R111-S1-GP ZZ.00PAD.571
H8 HOLE335R115-GP ZZ.00PAD.D01
H10 HOLE237R95-GP ZZ.00PAD.921
H11 HOLE237R95-GP ZZ.00PAD.921
H12 HOLE335R115-GP ZZ.00PAD.D01
H13 HOLE237R95-GP ZZ.00PAD.921
H19 HOLE315R95-GP ZZ.00PAD.911

DCBATOUT
EC9705 EC9706 EC9707 EC9708 EC9709 EC9710 EC9711 EC9712 EC9713 EC9714 SCD1U25V2KX-GP
3D3V_S0_CAMERA
EC9715 SCD1U25V2KX-GP
3D3V_AUX_S5
EC9716 SCD1U25V2KX-GP
3D3V_AUX_KBC
EC9717 SCD1U25V2KX-GP
3D3V_VGA_S0
EC9718 SCD1U25V2KX-GP
ODD_PWR_5V
EC9719 SCD1U25V2KX-GP
VCC_CORE
EC9720 EC9721 SCD1U25V2KX-GP
5V_S5
EC9722 EC9723 EC9724 SCD1U25V2KX-GP

3D3V_S0
R9704 100R2J-2-GP DY
3D3V_RUNPWR
Q9704 2N7002A-7-GP DY
PS_S3CNTRL

5V_S0
R9705 100R2J-2-GP DY
5V_RUNPWR
Q9705 2N7002A-7-GP DY
PS_S3CNTRL

5V_USB2_S3
EC9725 SCD1U25V2KX-GP
5V_USB1_S3
EC9726 SCD1U25V2KX-GP

1D05V_VTT
R9701 100R2J-2-GP DY
VTT_RUNPWR
Q9701 2N7002A-7-GP DY
36,37 PS_S3CNTRL
PS_S3CNTRL

VCC_CORE
R9706 100R2J-2-GP DY
CORE_RUNPWR
Q9706 2N7002A-7-GP DY
PS_S3CNTRL

VCC_GFXCORE
R9707 100R2J-2-GP DY
GFX_RUNPWR
Q9707 2N7002A-7-GP DY
PS_S3CNTRL

VCCSA
R9709 100R2J-2-GP DY
1D05V_RUNPWR
Q9709 2N7002A-7-GP DY
PS_S3CNTRL

1D8V_S0
R9702 100R2J-2-GP DY
1D8V_RUNPWR
Q9702 2N7002A-7-GP DY
PS_S3CNTRL

AD+
EC9702 EC9703 EC9704 SCD1U25V2KX-GP

For Discharge

3D3V_S5
R9710 100KR2J-1-GP DY
PM_SLP_S4
Q9710 2N7002A-7-GP DY
19,27,46 PM_SLP_S4#

1D5V_S3
R9711 100R2J-2-GP DY
1D5V_RUNPWR
Q9711 2N7002A-7-GP DY

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: LA480 | Rev: SD
Date: Friday, January 06, 2012 | Sheet 97 of 103

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<Core Design>

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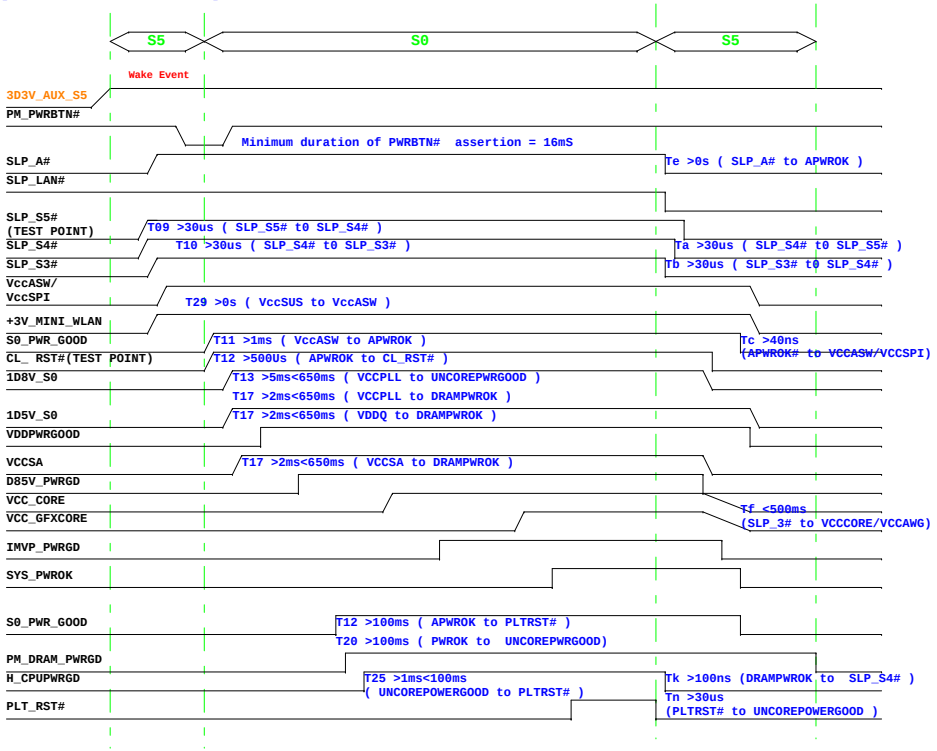
Title: *Change History*

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 98 of 103

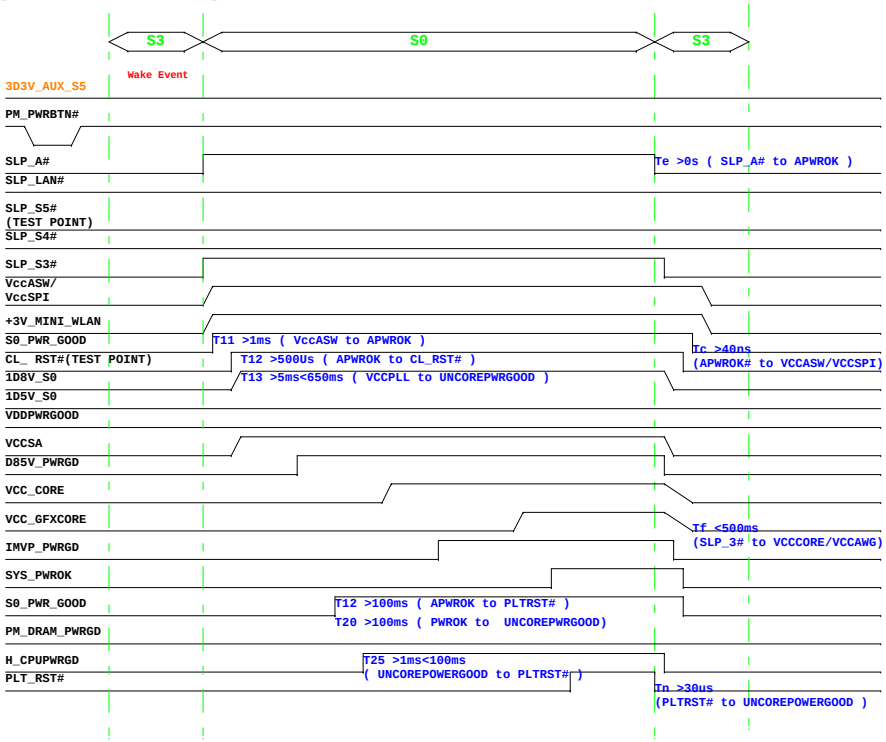
Intel-Power Sequence

(S5-to-S0-to-S5)



Intel PCH Pin Name	Main board PCH Pin Name
VccSUS (5V/3V)	3D3V_AUX_S5
PWRBTN#	PM_PWRBTN#
SLP_A#	SLP_A#
SLP_LAN#	SLP_LAN#
SLP_S5#	PM_SLP_S5#
SLP_S4#	PM_SLP_S4#
SLP_S3#	PM_SLP_S3#
VccASW/ VccSPI	VccASW/ VccSPI
Vcc_WLAN	+3V_MINI_WLAN
PWROK/APWROK	S0_PWR_GOOD
CL_ RST#	CL_ RST#
VCCPLL	1D8V_S0
VDDQ	1D5V_S0
VR_VDDQPWRGOOD	VDDPWRGOOD
VCCSA	VCCSA
IMVP7_VR_EN	D85V_PWRGD
VccCore	VCC_CORE
VccAXG	VCC_GFXCORE
IMVP7_PWRGD	IMVP_PWRGD
SYS_PWROK	SYS_PWROK
PWROK	S0_PWR_GOOD
DRAMPWROK	PM_DRAM_PWRGD
UNCOREPWRGOOD	H_CPUPWRGD
PLTRST#	PLT_RST#

(S3-to-S0-to-S3)



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
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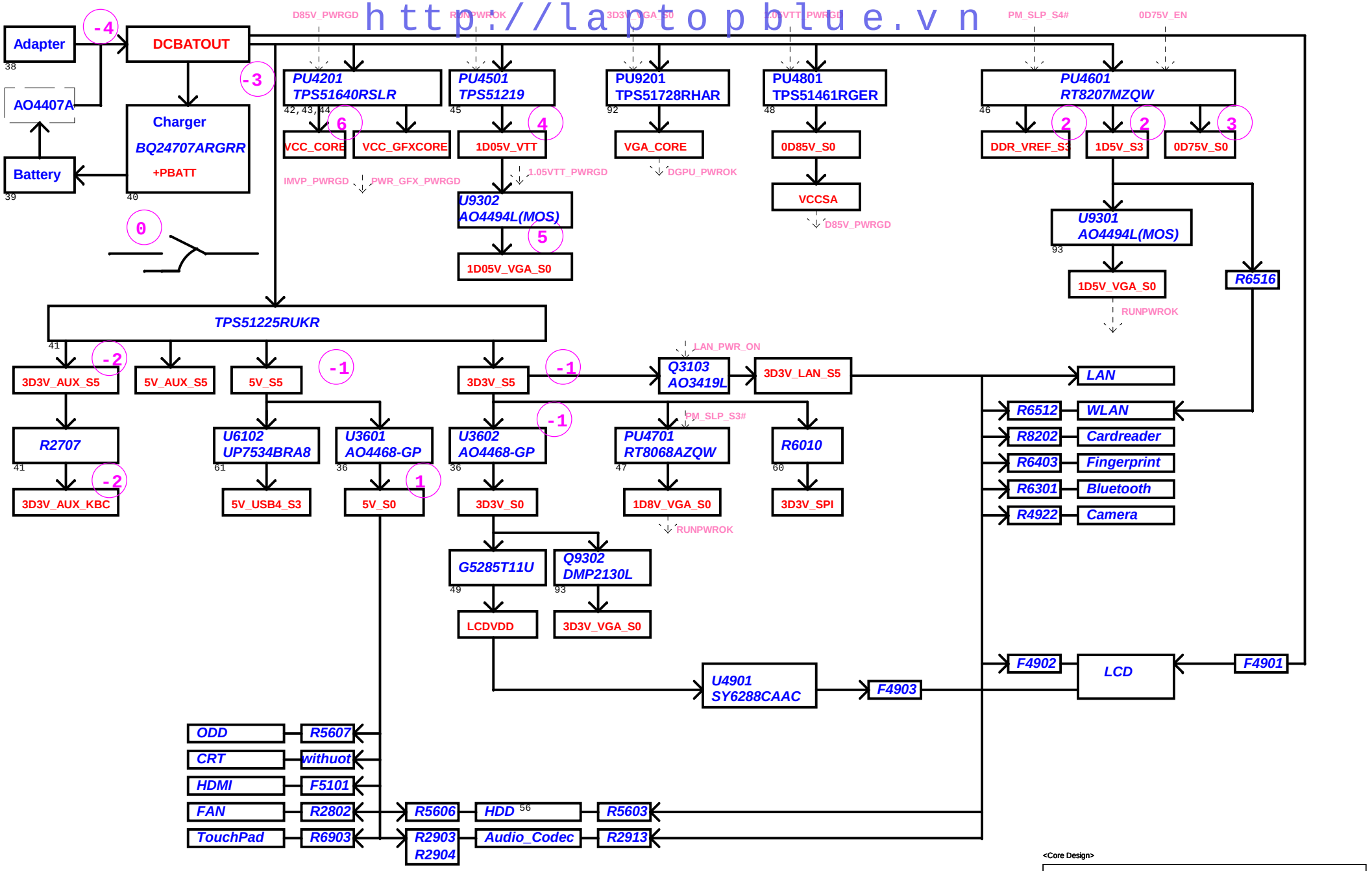
Date: Friday, January 06, 2012 Sheet 99 of 103



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Wistron Corporation
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Title: Power Block Diagram

Size	Document Number	Rev
A3	LA480	SD

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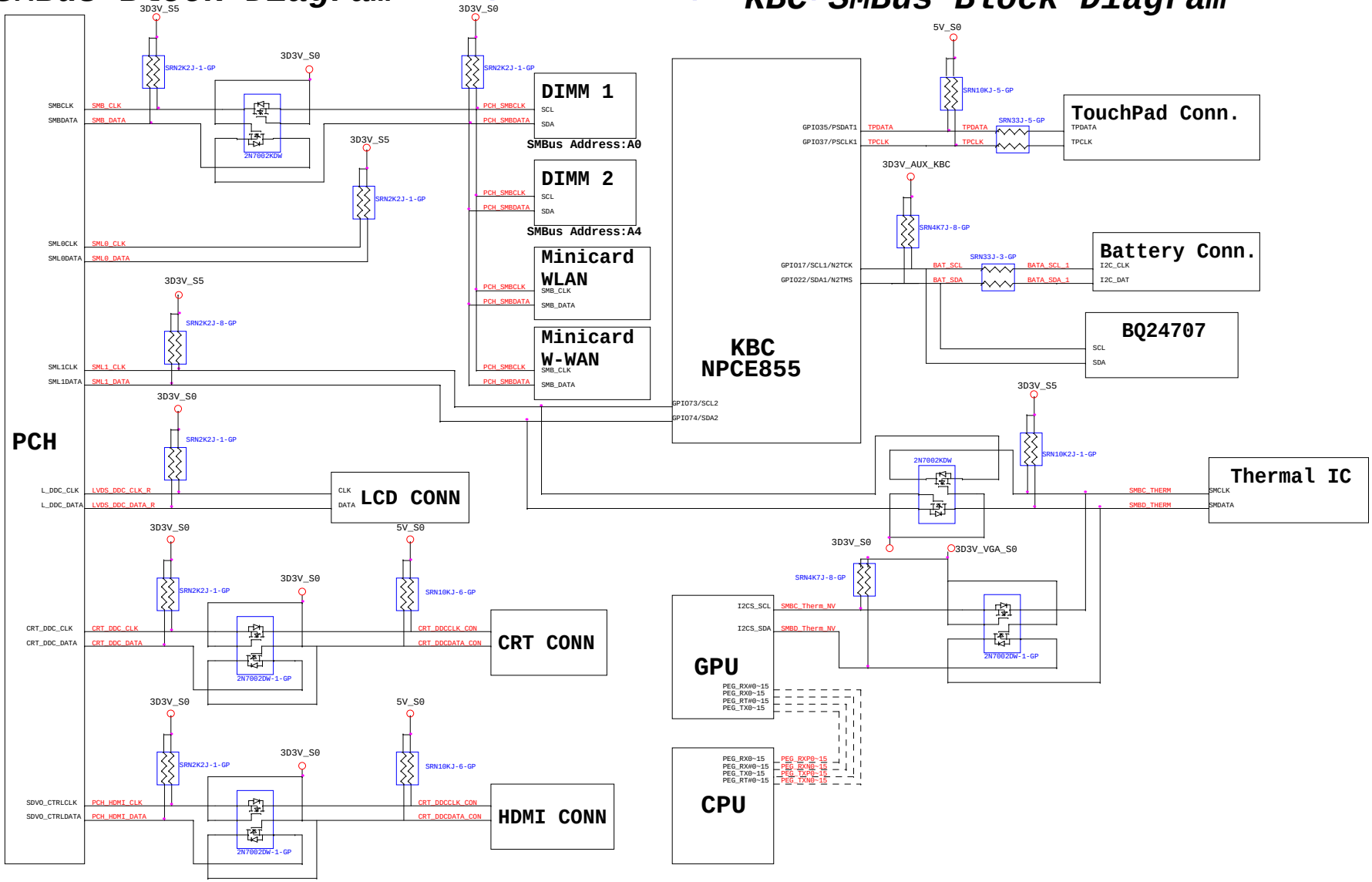
PCH SMBus Block Diagram



KBC SMBus Block Diagram

Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	LA480	SD

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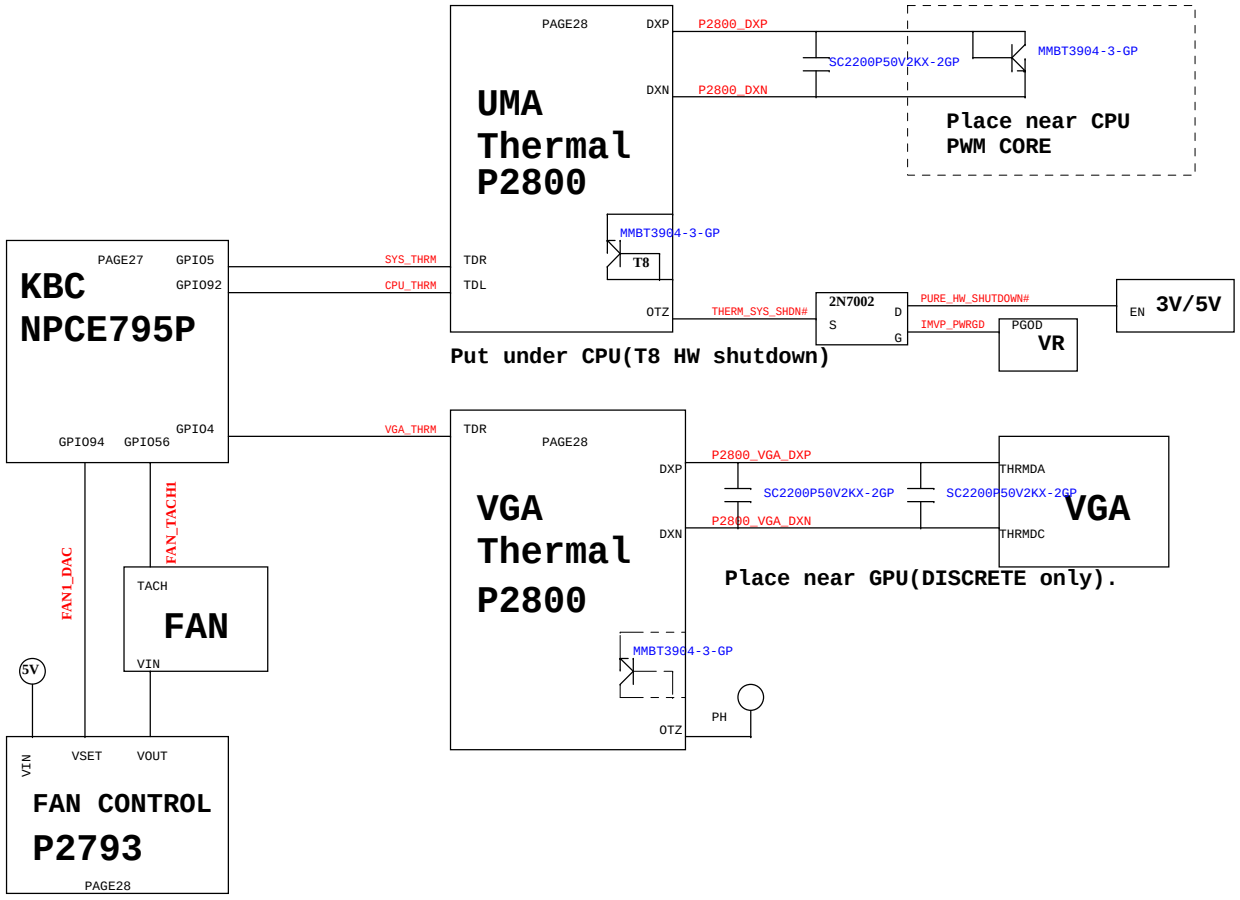
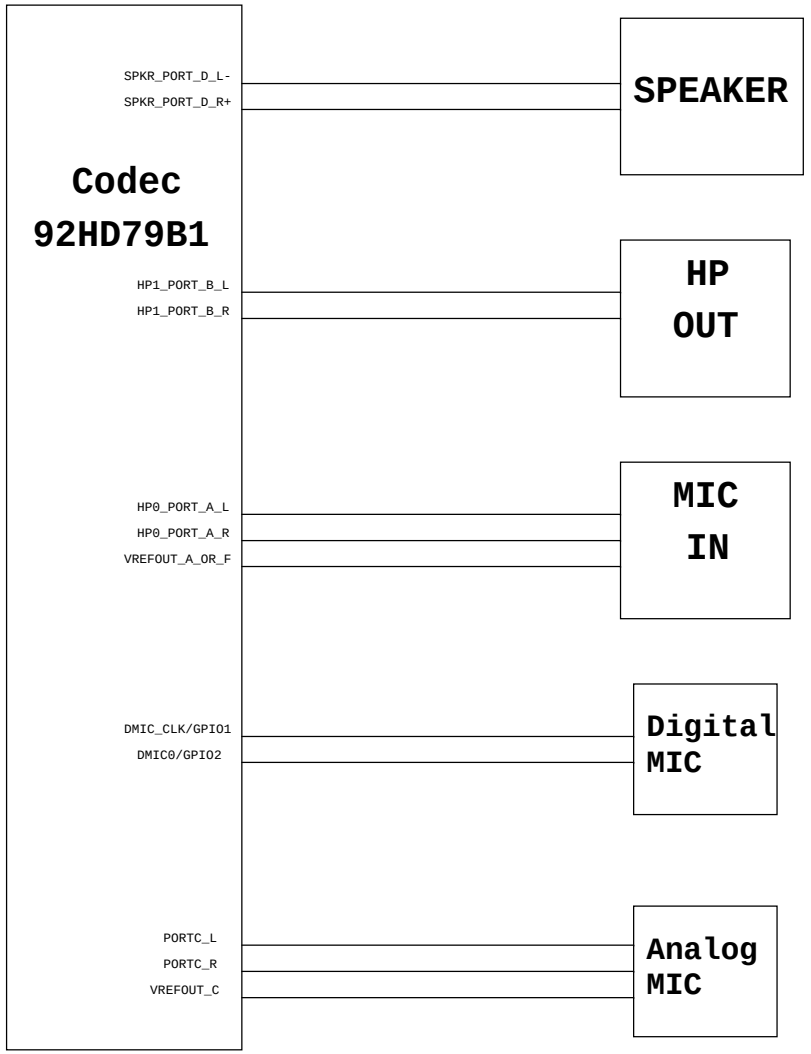
Thermal Block Diagram



Audio Block Diagram



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	LA480	SD

Date: Friday, January 06, 2012 Sheet 102 of 103

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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Change History*

Size	Document Number	Rev
A4	LA480	SD

Date: Friday, January 06, 2012 Sheet 103 of 103