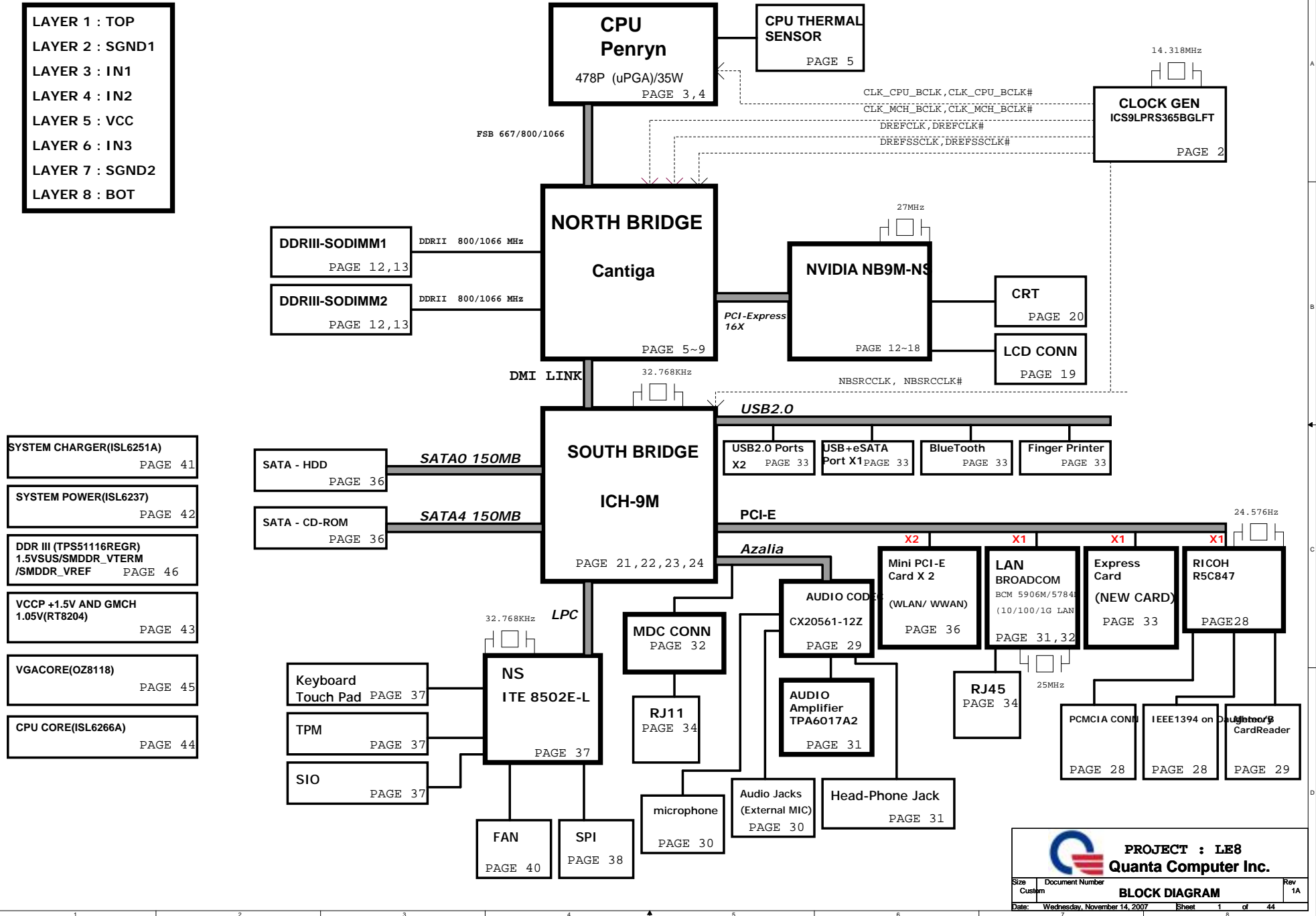


PCB STACK UP
8L

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

LE8(K43) BLOCK DIAGRAM

01







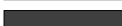


PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev	
Custom	BLOCK DIAGRAM	1A	
Date: Wednesday, November 14, 2007		Sheet	1 of 44

Board Stack up Description

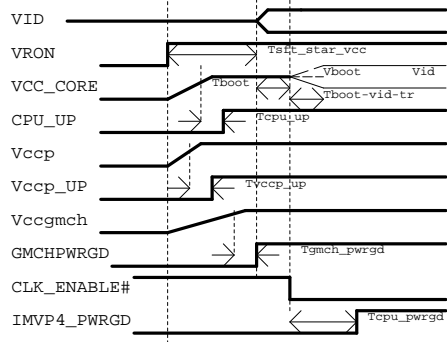
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

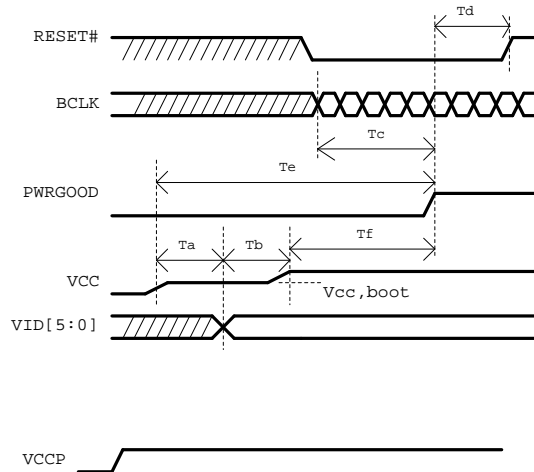
Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.5VSUS	X	X			SUSON
SMDRR_VTERM/+3V/+5V/+15V/+1.8V	X				MAINON
+VGACORE/+VGA1.1V	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

Power On Sequencing Timing Diagram

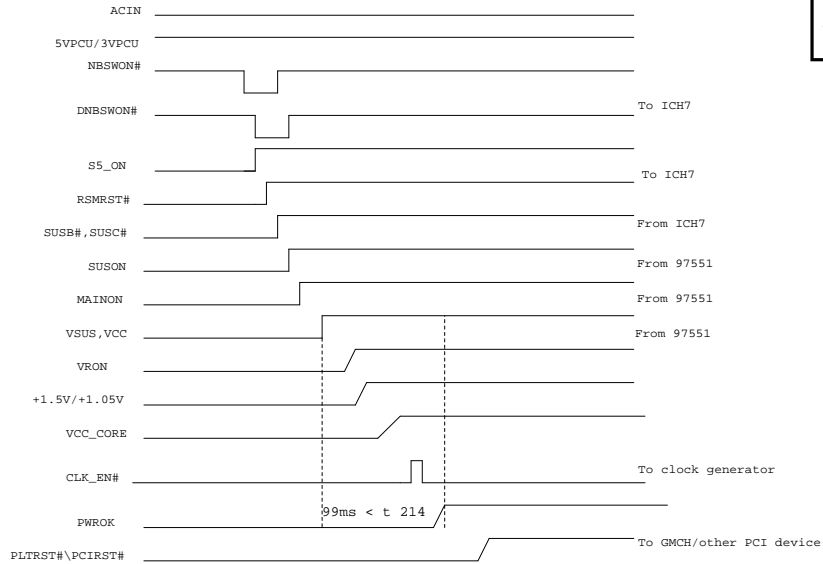


YONAH Power-up Timing Specifications



Ta=VCC and VCCP assertion to VID[5:0] valid
 Tb=VID[5:0] stable to VCC valid
 Tc=BCLK stable to PWRGOOD assertion
 Td=PWRGOOD to RESET# de-assertion time
 Te=Vcc,boot valid to PWRGOOD assertion time

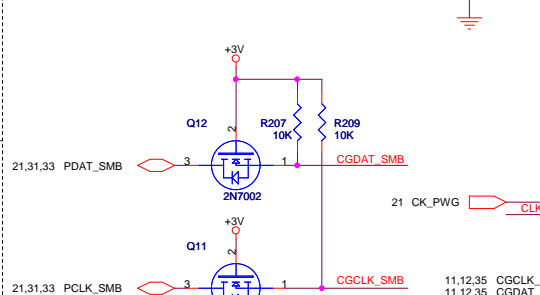
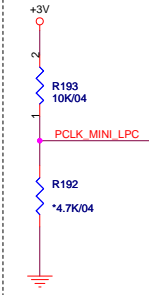
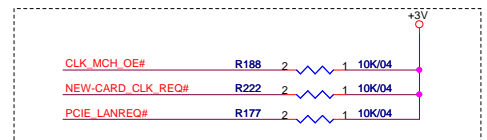
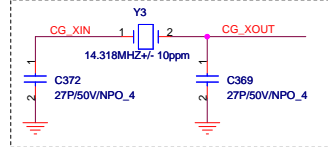
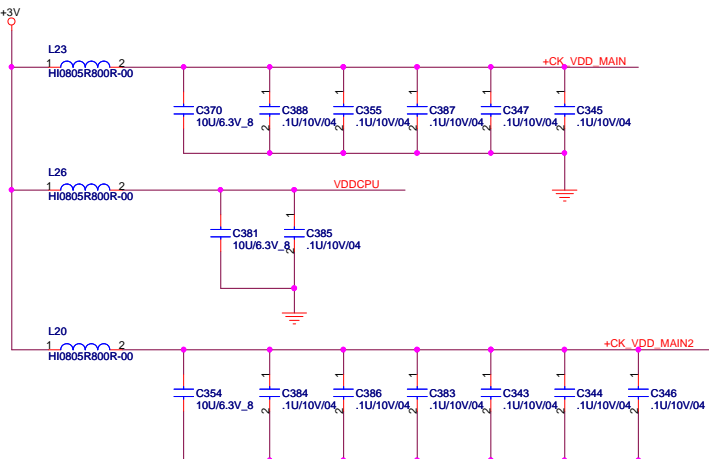
ACIN POWER ON TIMING



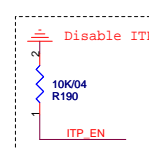
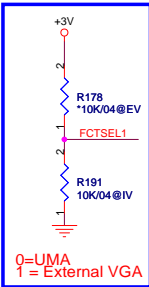
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICOH847	AD21	REQ0# / GNT0#	INT E# / F#

PROJECT : LE8
 Quanta Computer Inc.

Size: Custom Document Number: SYSTEM INFORMATION Rev: 1A
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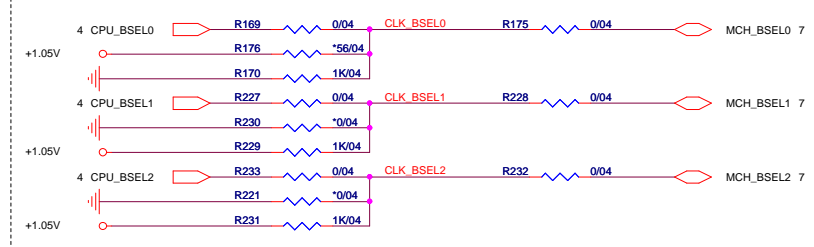
0=overlocking of CPU and SRC Allowed
1 = overlocking of CPU and SRC not Allowed



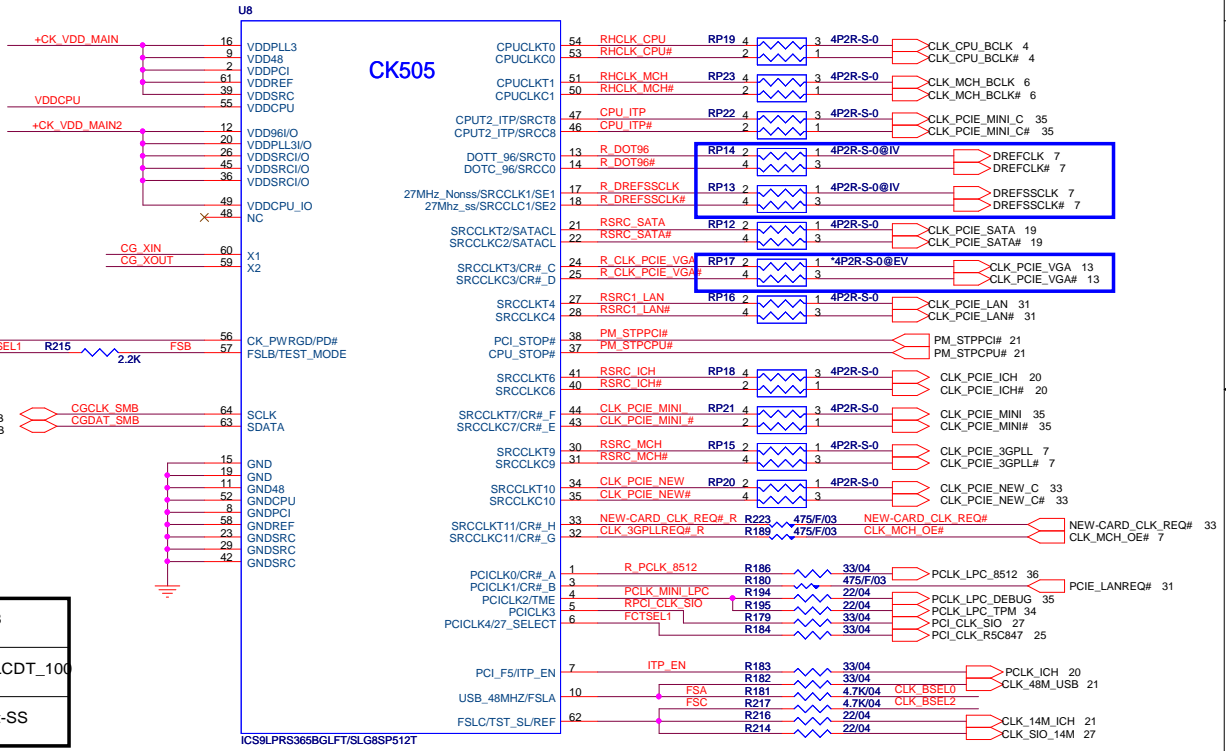
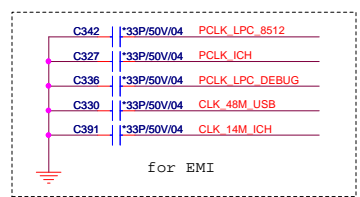
GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CPU Clock select

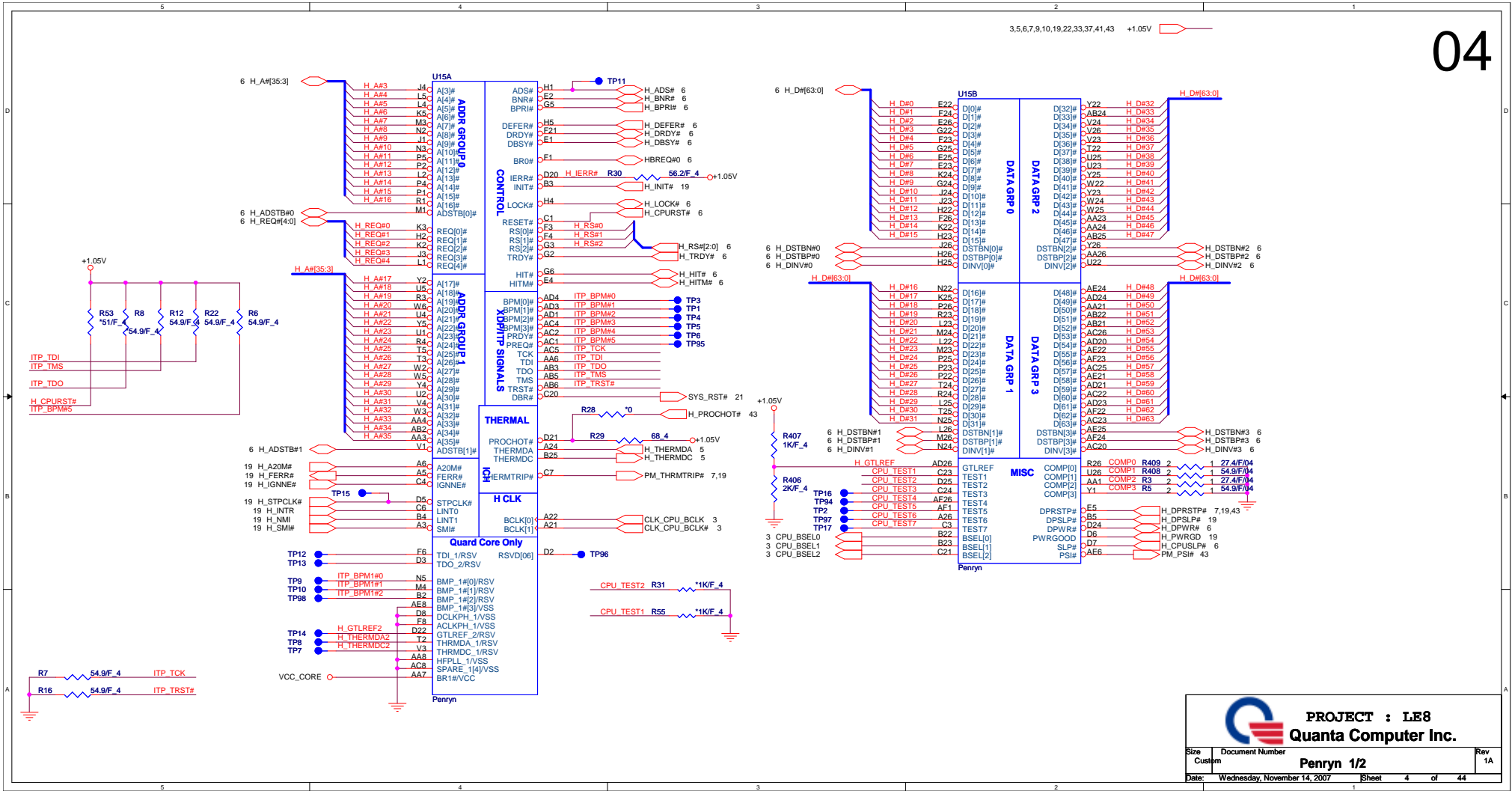



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



PROJECT : LE8
QUANTA Computer Inc.

Size: Custom | Document Number: **CLOCK GENERATOR** | Rev: 1A
Date: Wednesday, November 14, 2007 | Sheet: 3 of 44

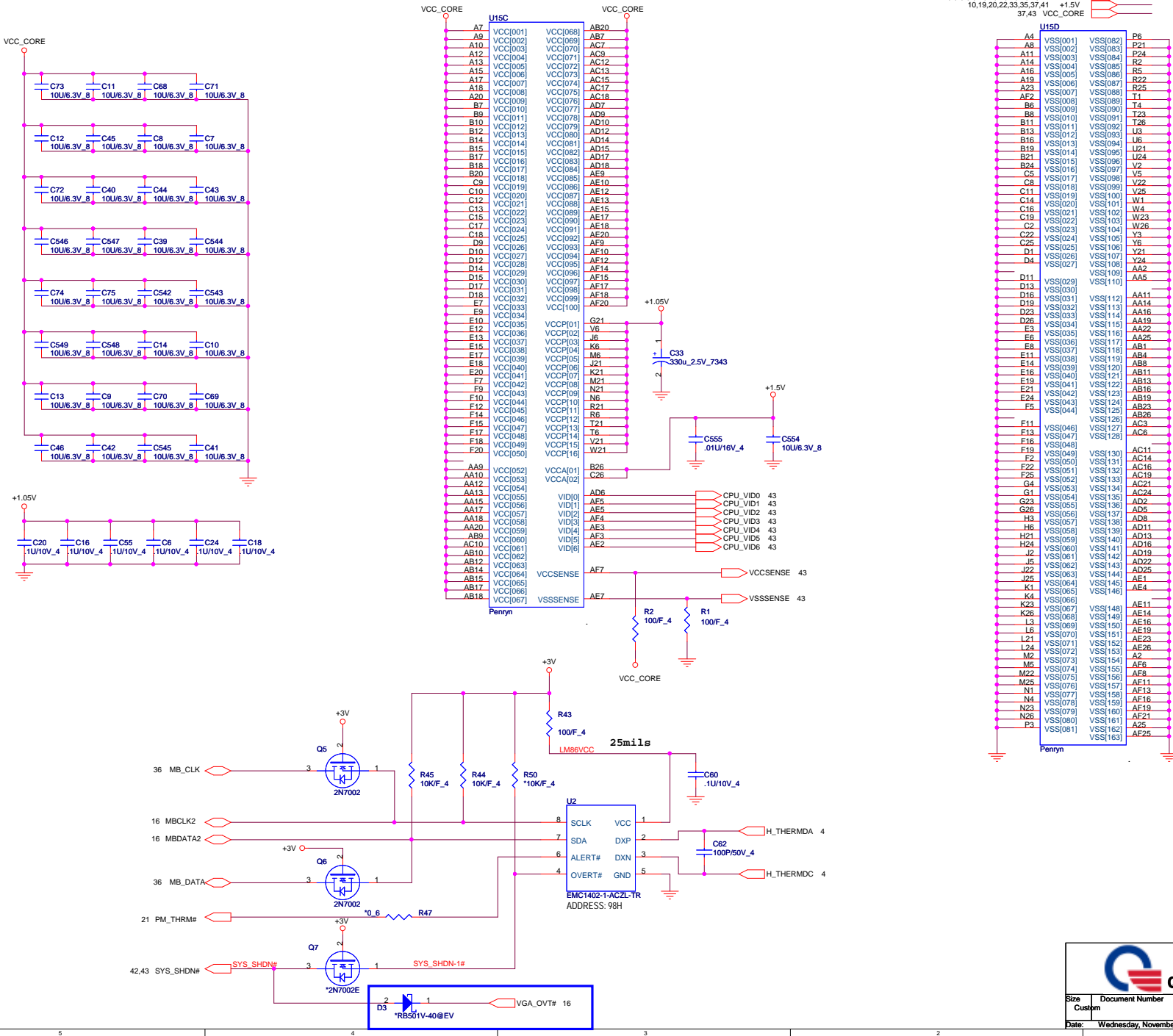




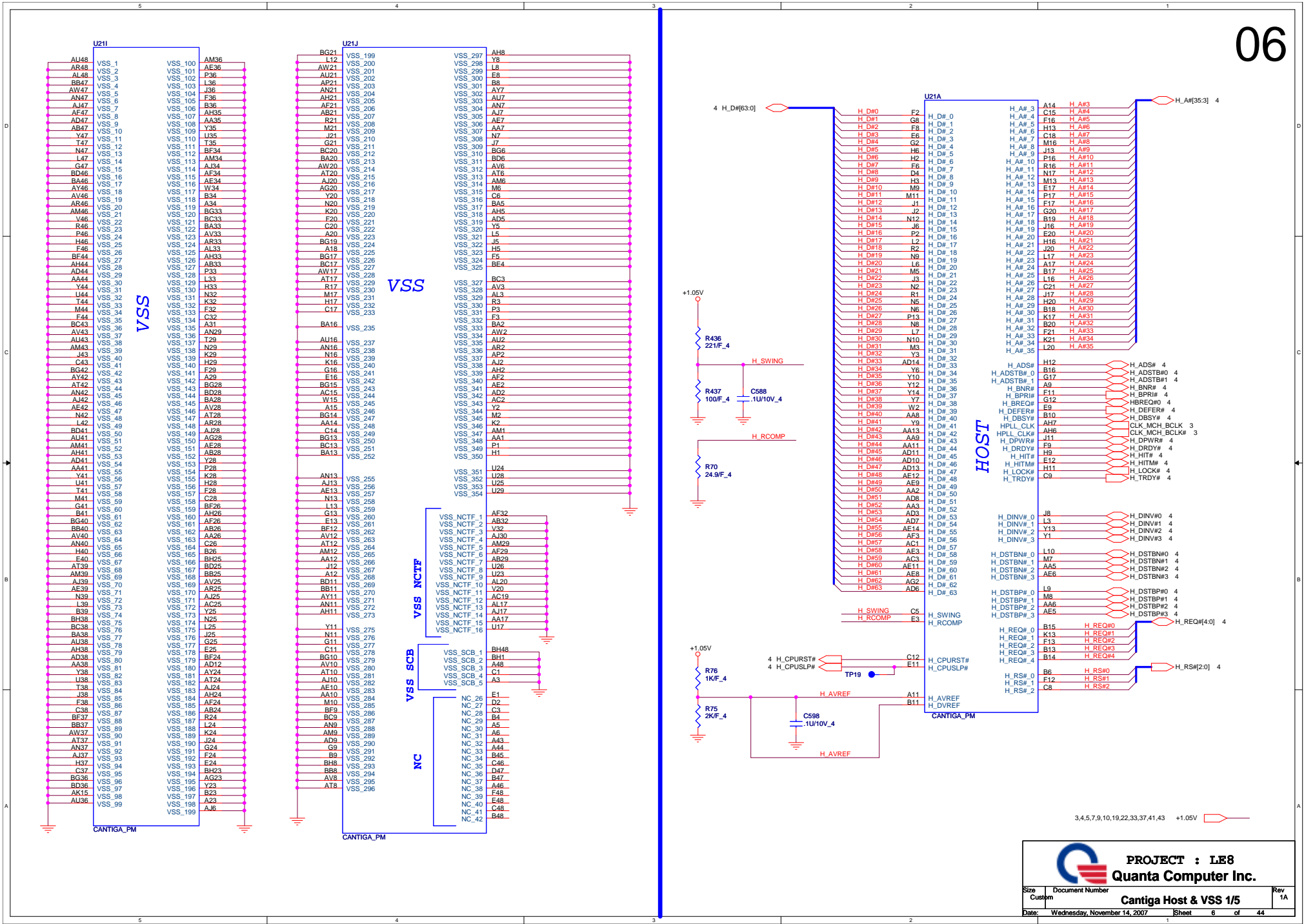
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn 1/2	1A
Date:	Wednesday, November 14, 2007	Sheet 4 of 44

3,7,10,11,12,13,15,16,19,20,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44 +3V
3,4,6,7,9,10,19,22,33,37,41,43 +1.05V
10,19,20,22,33,35,37,41 +1.5V
37,43 VCC_CORE



PROJECT : LE8
Quanta Computer Inc.
 Size Custom Document Number
 Penryn & TH Monitor 2/2
 Date: Wednesday, November 14, 2007 1:58 PM
 Sheet 5 of 44



3,4,5,7,9,10,19,22,33,37,41,43 +1.05V

PROJECT : LE8
Quanta Computer Inc.

Size: Custom Document Number: Cantiga Host & VSS 1/5
 Date: Wednesday, November 14, 2007 Sheet 6 of 44

3.5,10,11,12,13,16,19,20,21,22,23,24,25,26,27,28,30,31,33,34,36,37,38,40,41,42,43,44
 +3V 8,10,11,12,33,37,39,44 1.5VSUS
 +1.05V_PEG 10 1.05V_PEG

07

- MCH_CFG_5 DMiX2 selection
 - Low: DMiX2
 - High: DMiX4 (Default)
- MCH_CFG_16 FSB Dynamic ODT
 - Low: Dynamic ODT disabled
 - High: Dynamic ODT enabled (Default)
- MCH_CFG_9 PCI Express Graphic Lane
 - Low: Reverse Lane
 - High: Normal operation(Default)
- MCH_CFG_19 DIMI Lane Reversal
 - Low: Normal (Default)
 - High: Lane Reserved
- MCH_CFG_6 ITPM Host Interface
 - Low: ITPM Host Interface enabled
 - High: ITPM Host Interface disabled (Default)
- MCH_CFG_7 Intel (R) Management Engine Crypto
 - Low: Intel (R) Management Engine Crypto
 - High: TLS cipher suite with no confidentiality
- MCH_CFG_10 PCIe Linkback Enable
 - Low: Enabled
 - High: Disabled (Default)
- MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating
 - Low: Enabled
 - High: Disabled (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

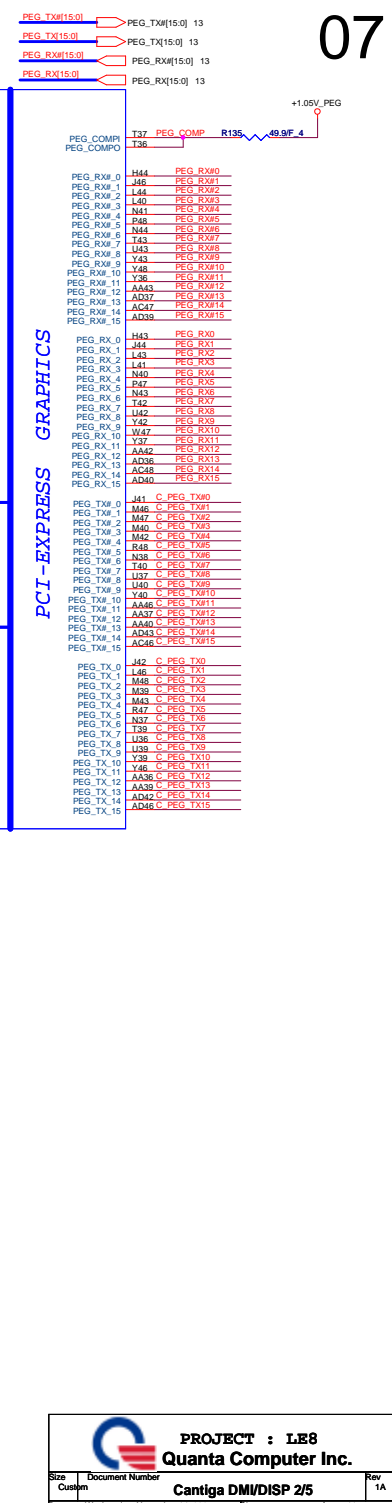
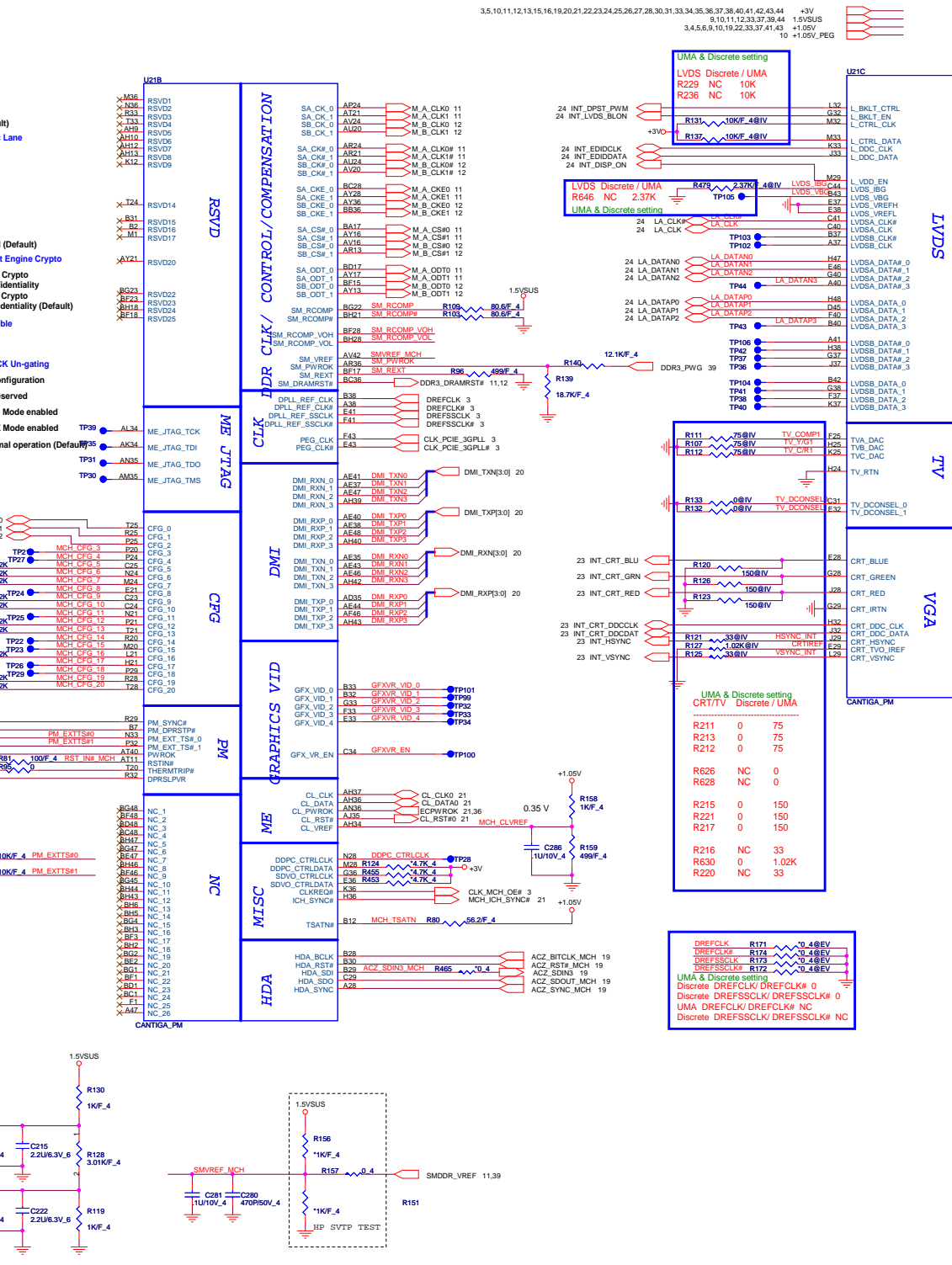
0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

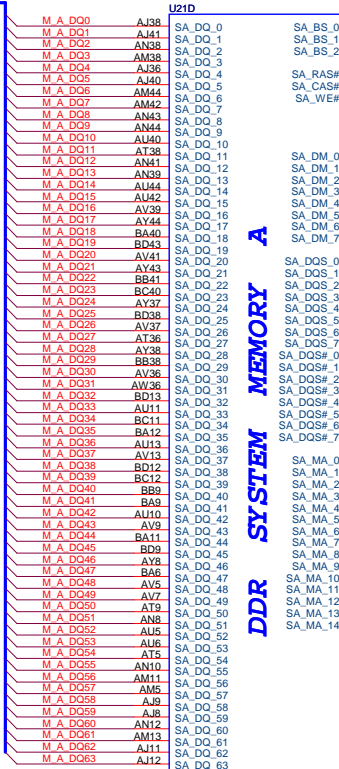
0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

MCH_CFG_12 MCH_CFG_13 Configuration

0	0	Reserved
0	0	XOR Mode enabled
1	0	All-Z Mode enabled
0	1	Normal operation (Default)

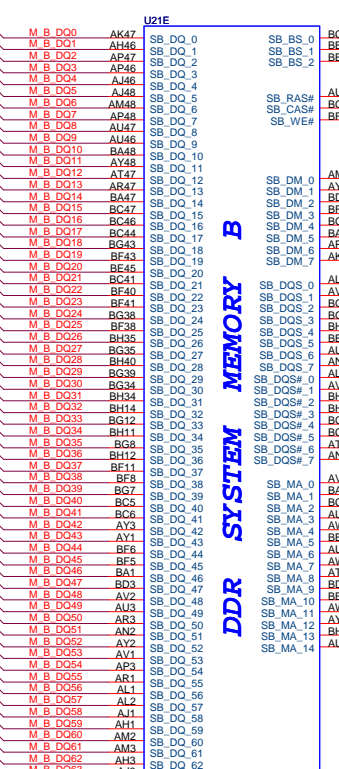


11 M_A_DQ[63:0]



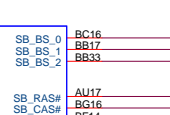
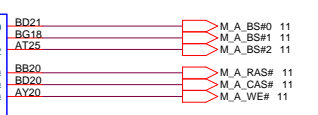
CANTIGA_PM

12 M_B_DQ[63:0]

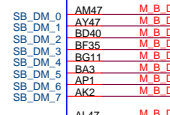
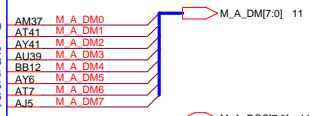


CANTIGA_PM

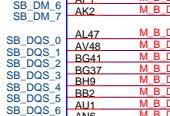
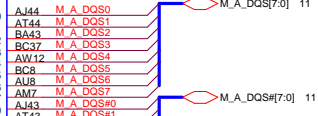
11 M_A_BS[0:11]



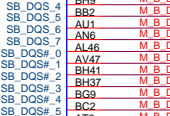
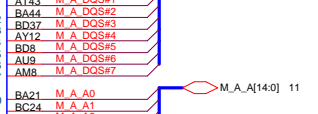
11 M_A_DM[7:0]



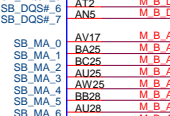
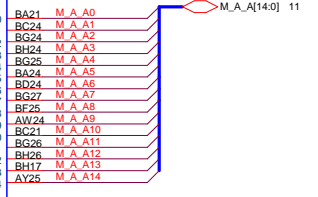
11 M_A_DQS[7:0]



11 M_A_DQS# [7:0]



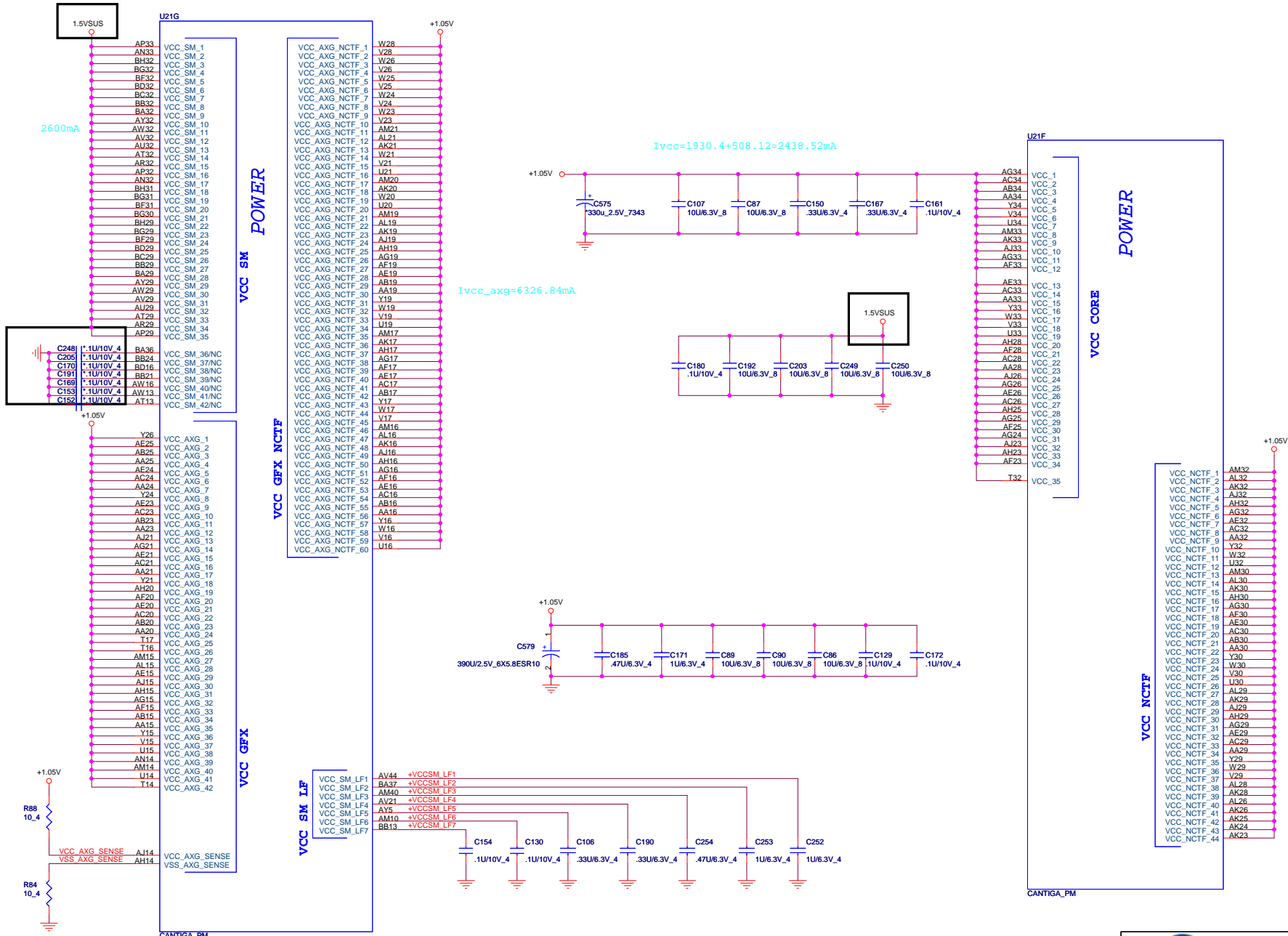
11 M_A_A [14:0]



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Quanta Computer Inc.

Size: Custom Document Number
 Cantiga DDR3 3/5 Rev 1A

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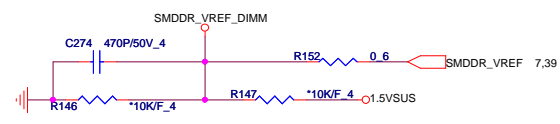
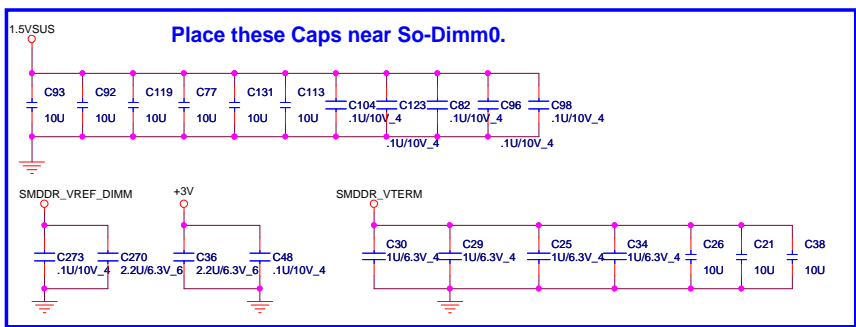
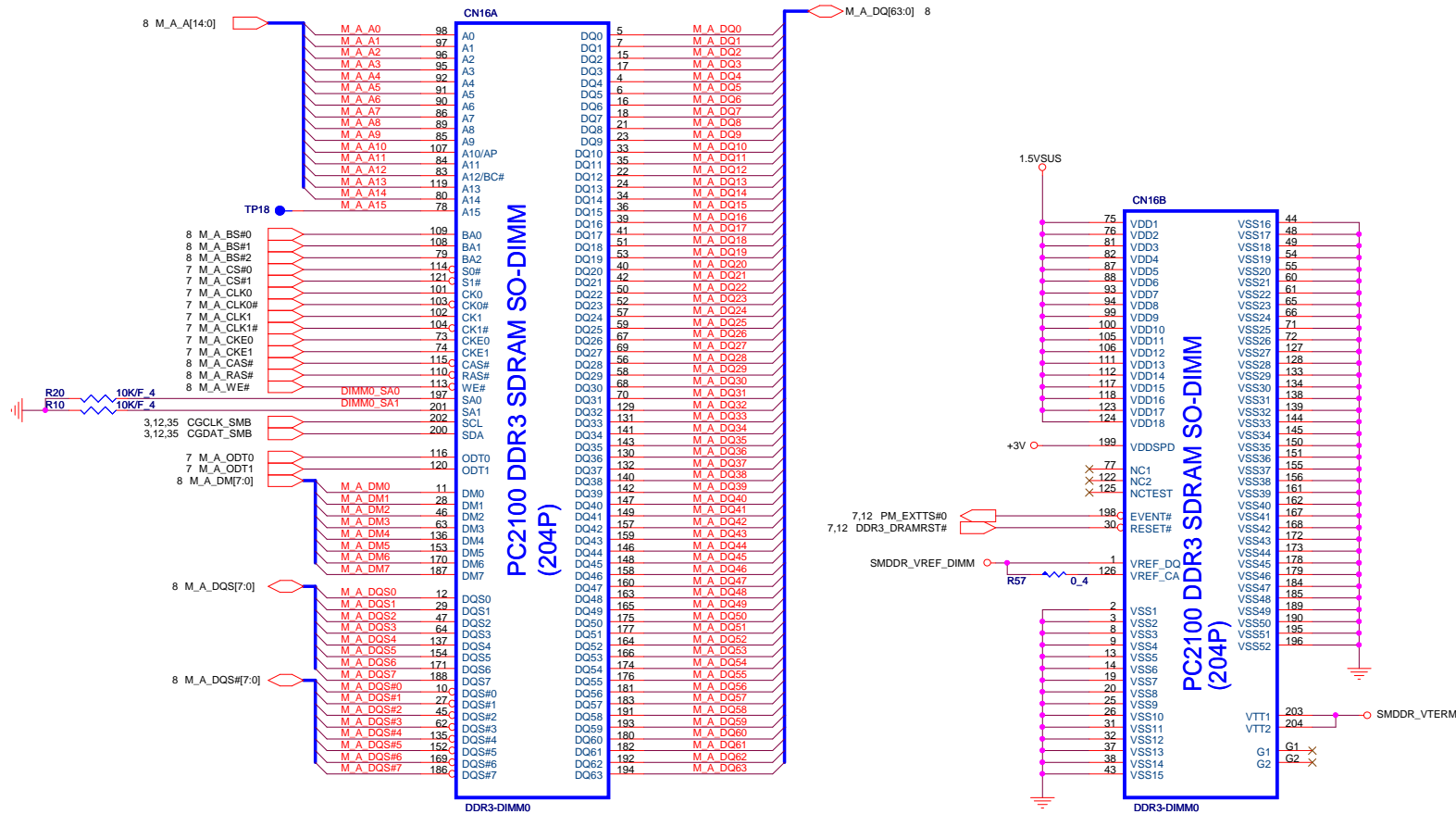


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Quanta Computer Inc.

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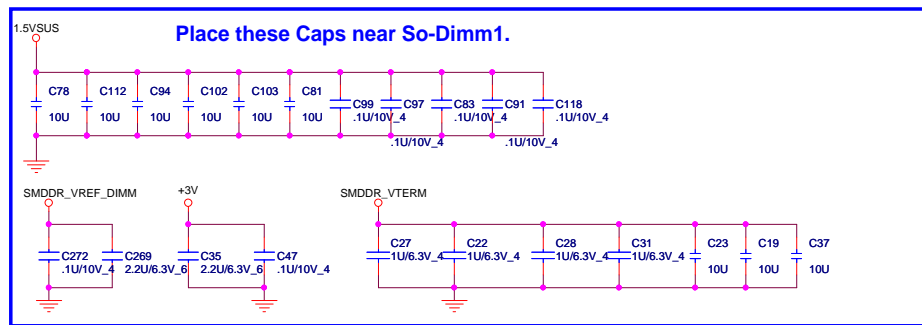
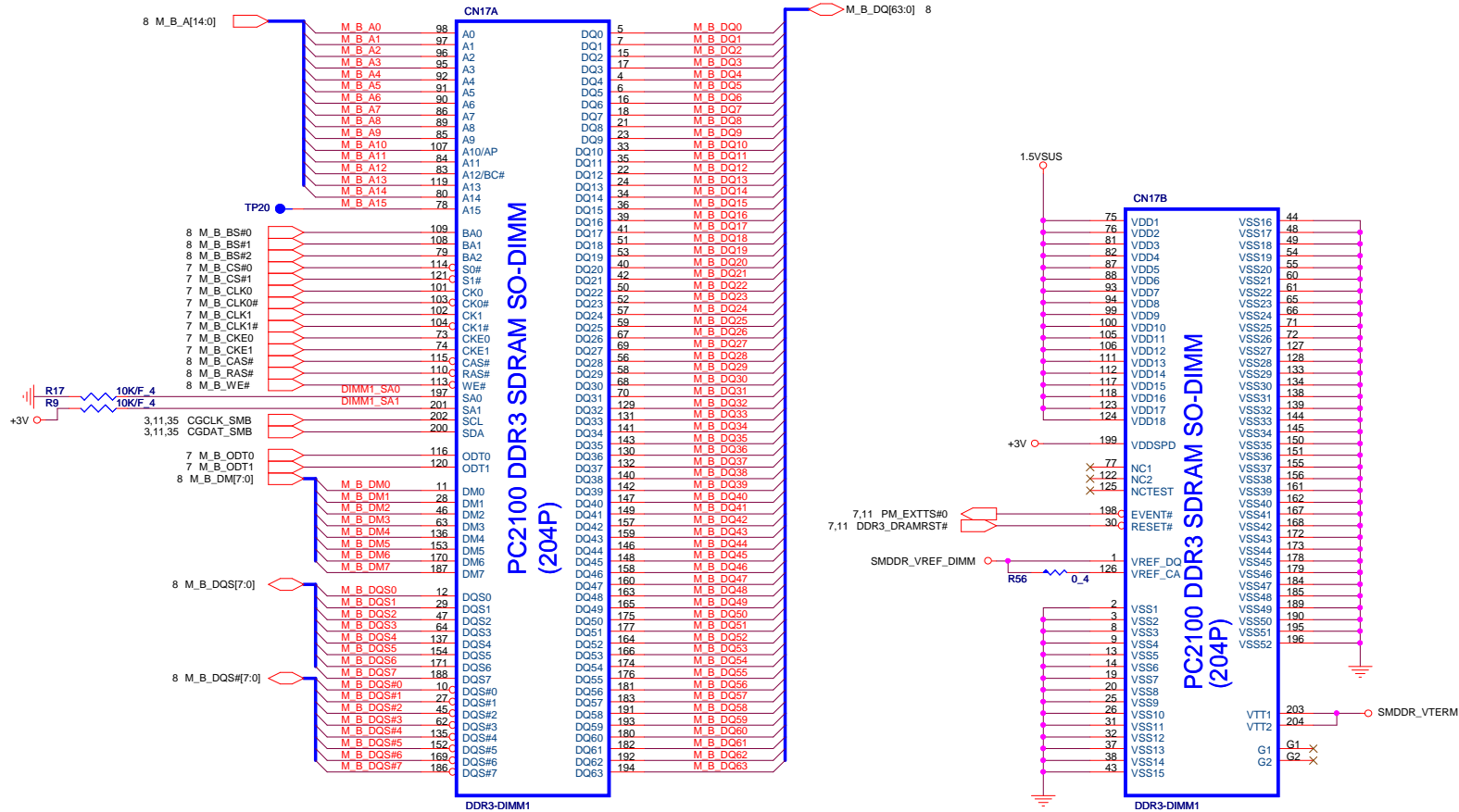
7,10,11,12,33,37,39,44 1.5VSUS
 3,4,5,6,7,10,19,22,33,37,41,43 +1.05V

CANTIGA_Vcc 4/5 Rev 1A



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Quanta Computer Inc.

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Custom	DDR3 DIMM-0(H=5.2)	1A
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3,5,7,10,11,12,13,15,16,19,21,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44
 5,10,19,22,33,35,37,41 +1.5V
 +3V
 21,25,26,28,33,34,35,37,39,43 3V3US

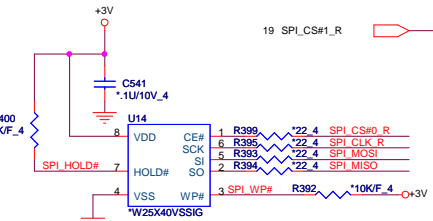


MINI CARD PCI-E(WLAN)

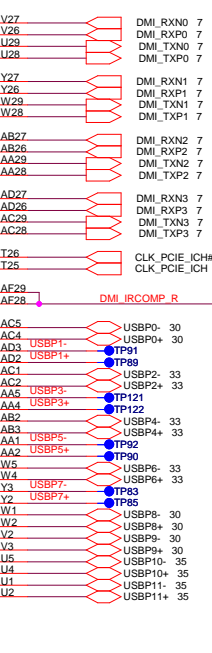
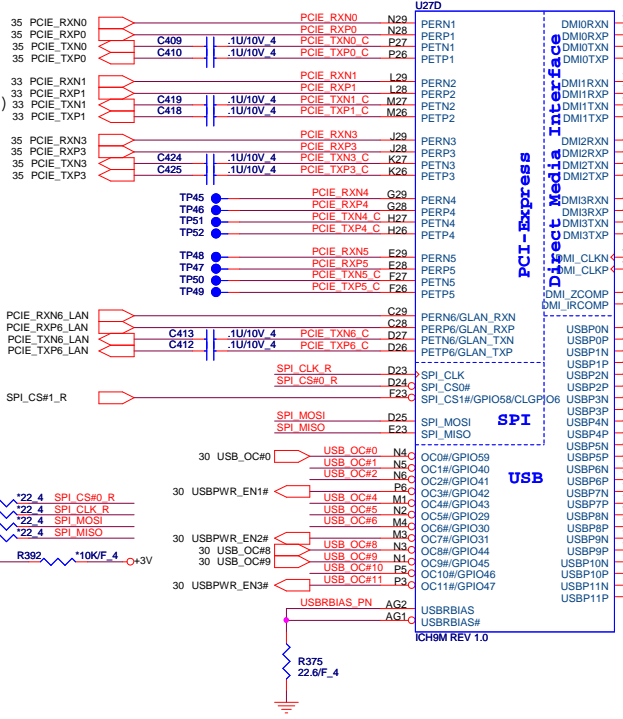
EXPRESS CARD (NEW CARD)

MINI CARD PCI-E(WWAN)

PCI-E-LAN



512K byte SPI ROM
For HDCP only



USB Connector

Finger Printer

BLUETOOTH

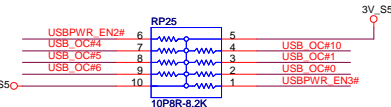
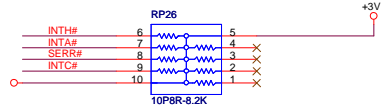
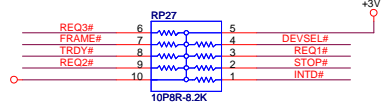
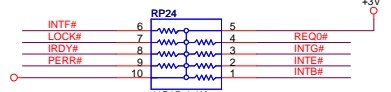
NEW CARD

USB Connector

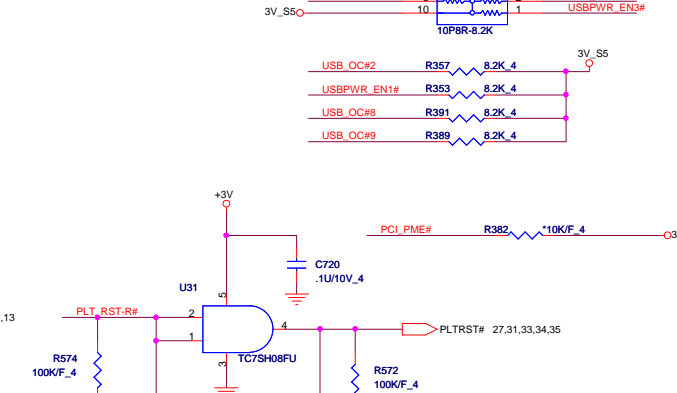
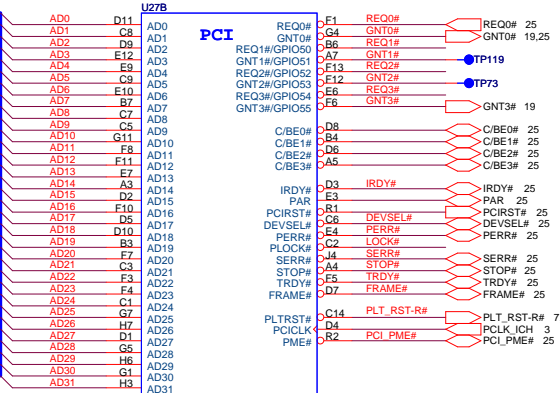
USB Connector

WWAN Min-Card

WLAN Min-Card



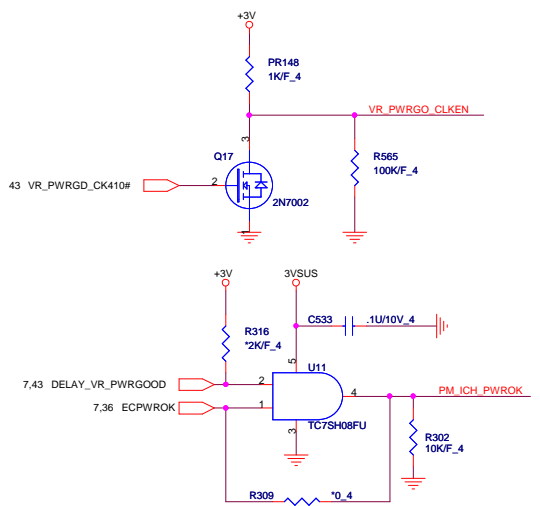
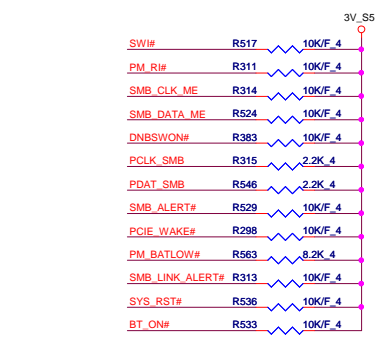
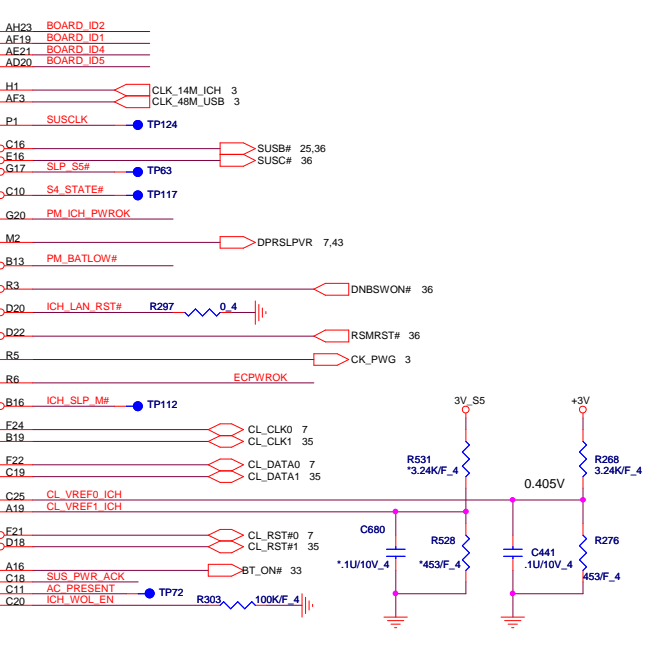
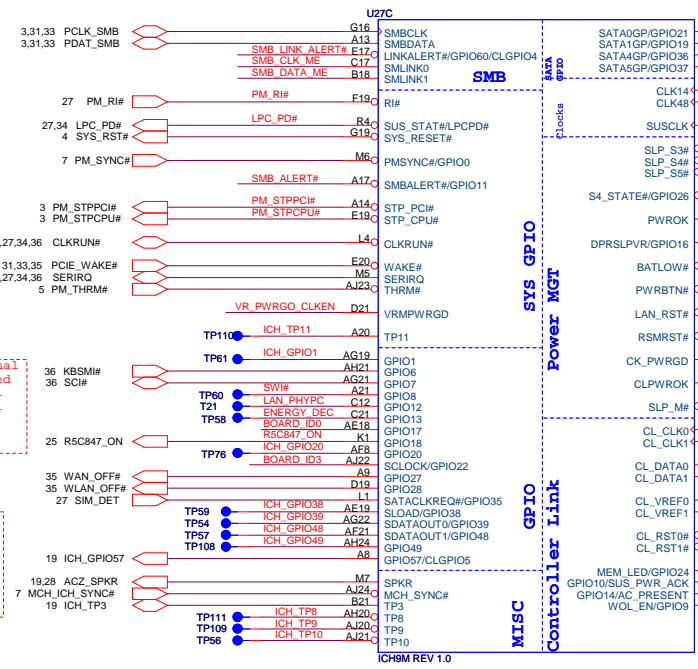
25 AD[0..31]



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTE#, F#, G#	RICOH R5C847

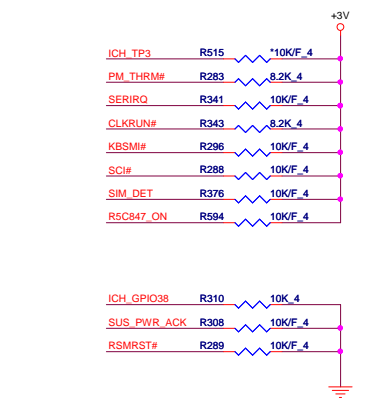
PROJECT : LE8
Quanta Computer Inc.
 Size: Custom Document Number: ICH9-M PCIE 2/4 Rev 1A
 Date: Wednesday, November 14, 2007 Sheet 20 of 44

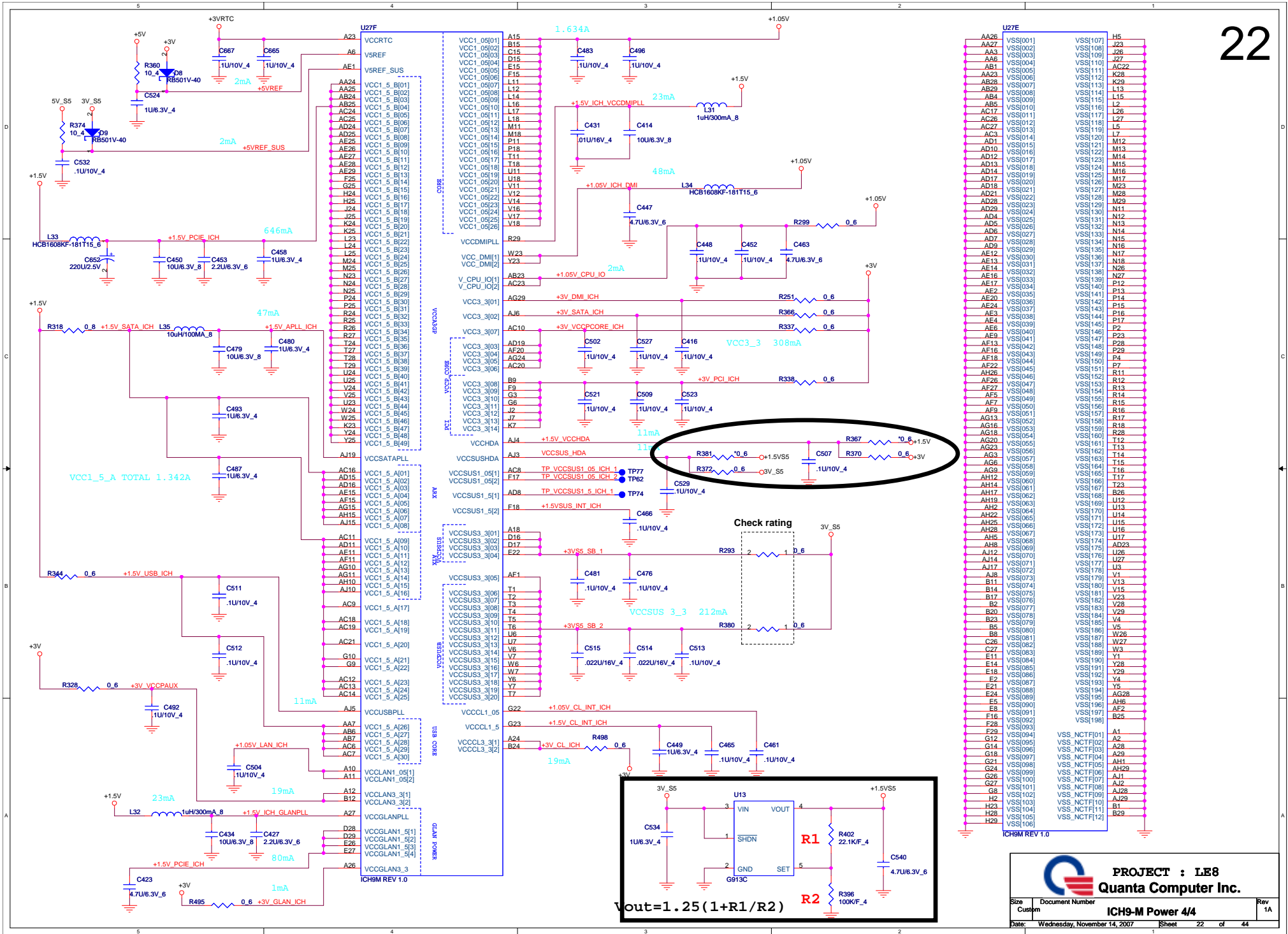
5,10,19,20,22,33,35,37,41 +1.5V
 3,5,7,10,11,12,13,15,16,19,20,22,23,24,25,26,27,28,30,31,33,34,35,36,37,38,40,41,42,43,44 +3V
 19,20,22,37 3V_S5
 25,26,28,33,34,35,37,39,43 3VSUS



Board ID For Function	ID3 GPIO122	ID2 GPIO121	ID1 GPIO19	ID0 GPIO17
Default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	0	1
	1	1	1	0
	1	1	1	1

Board ID For Model	ID5 GPIO37	ID4 GPIO36
LE6	0	0
LE7	0	1
LE8	1	0
LE9	1	1

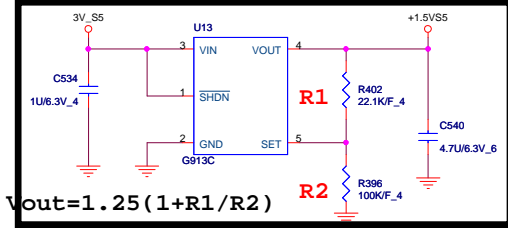




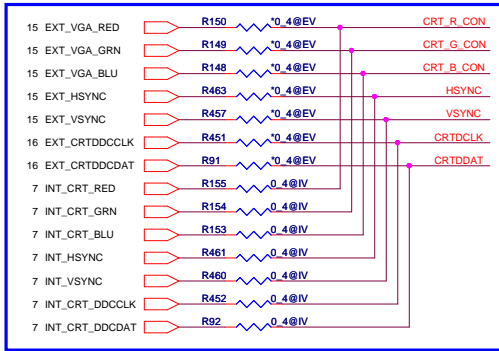
AA26	VSS[001]	VSS[107]	H5
AA27	VSS[002]	VSS[108]	J2
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AB2	VSS[006]	VSS[112]	L2
AB29	VSS[007]	VSS[113]	L26
AB3	VSS[008]	VSS[114]	L27
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L7
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD21	VSS[021]	VSS[127]	M28
AD28	VSS[022]	VSS[128]	M29
AD4	VSS[023]	VSS[129]	M12
AD29	VSS[024]	VSS[130]	N11
AD5	VSS[025]	VSS[131]	N13
AD6	VSS[026]	VSS[132]	N14
AD7	VSS[027]	VSS[133]	N15
AD9	VSS[028]	VSS[134]	N17
AE12	VSS[029]	VSS[135]	N18
AE13	VSS[030]	VSS[136]	N28
AE14	VSS[031]	VSS[137]	N27
AE17	VSS[032]	VSS[138]	P12
AE2	VSS[033]	VSS[139]	P13
AE20	VSS[034]	VSS[140]	P15
AE24	VSS[035]	VSS[141]	P16
AE4	VSS[036]	VSS[142]	P17
AE6	VSS[037]	VSS[143]	P2
AE9	VSS[038]	VSS[144]	P23
AF13	VSS[039]	VSS[145]	P27
AF16	VSS[040]	VSS[146]	P28
AF18	VSS[041]	VSS[147]	P29
AF22	VSS[042]	VSS[148]	P7
AH26	VSS[043]	VSS[149]	P12
AF28	VSS[044]	VSS[150]	P15
AF5	VSS[045]	VSS[151]	P16
AF7	VSS[046]	VSS[152]	P17
AG13	VSS[047]	VSS[153]	R12
AG16	VSS[048]	VSS[154]	R14
AG18	VSS[049]	VSS[155]	R15
AG20	VSS[050]	VSS[156]	R16
AG23	VSS[051]	VSS[157]	R17
AG3	VSS[052]	VSS[158]	R18
AG6	VSS[053]	VSS[159]	R2
AG9	VSS[054]	VSS[160]	R28
AG23	VSS[055]	VSS[161]	R11
AG3	VSS[056]	VSS[162]	T14
AG6	VSS[057]	VSS[163]	T13
AG9	VSS[058]	VSS[164]	T14
AH12	VSS[059]	VSS[165]	T16
AH14	VSS[060]	VSS[166]	T17
AH17	VSS[061]	VSS[167]	T26
AH19	VSS[062]	VSS[168]	T28
AH2	VSS[063]	VSS[169]	U13
AH22	VSS[064]	VSS[170]	U14
AH25	VSS[065]	VSS[171]	U15
AH28	VSS[066]	VSS[172]	U16
AH5	VSS[067]	VSS[173]	U17
AH8	VSS[068]	VSS[174]	AD23
AJ12	VSS[069]	VSS[175]	U28
AJ14	VSS[070]	VSS[176]	U27
AJ17	VSS[071]	VSS[177]	U3
AJ8	VSS[072]	VSS[178]	U3
B11	VSS[073]	VSS[179]	V1
B14	VSS[074]	VSS[180]	V15
B17	VSS[075]	VSS[181]	V23
B2	VSS[076]	VSS[182]	V28
B20	VSS[077]	VSS[183]	V29
B23	VSS[078]	VSS[184]	V4
B5	VSS[079]	VSS[185]	V5
B8	VSS[080]	VSS[186]	V26
C26	VSS[081]	VSS[187]	W27
C27	VSS[082]	VSS[188]	W3
E11	VSS[083]	VSS[189]	V1
E14	VSS[084]	VSS[190]	V28
E18	VSS[085]	VSS[191]	V29
E2	VSS[086]	VSS[192]	V4
E21	VSS[087]	VSS[193]	V5
E24	VSS[088]	VSS[194]	AG28
E5	VSS[089]	VSS[195]	AH6
E8	VSS[090]	VSS[196]	AF2
F16	VSS[091]	VSS[197]	E25
F29	VSS[092]	VSS[198]	
F29	VSS[093]	VSS[199]	
G12	VSS[094]	VSS[200]	
G14	VSS[095]	VSS[201]	
G18	VSS[096]	VSS[202]	
G21	VSS[097]	VSS[203]	
G21	VSS[098]	VSS[204]	
G24	VSS[099]	VSS[205]	
G26	VSS[100]	VSS[206]	
G27	VSS[101]	VSS[207]	
G8	VSS[102]	VSS[208]	
H2	VSS[103]	VSS[209]	
H23	VSS[104]	VSS[210]	
H28	VSS[105]	VSS[211]	
H29	VSS[106]	VSS[212]	

PROJECT : LE8
Quanta Computer Inc.

Size: Custom
 Document Number: ICH9-M Power 4/4
 Date: Wednesday, November 14, 2007
 Sheet: 22 of 44

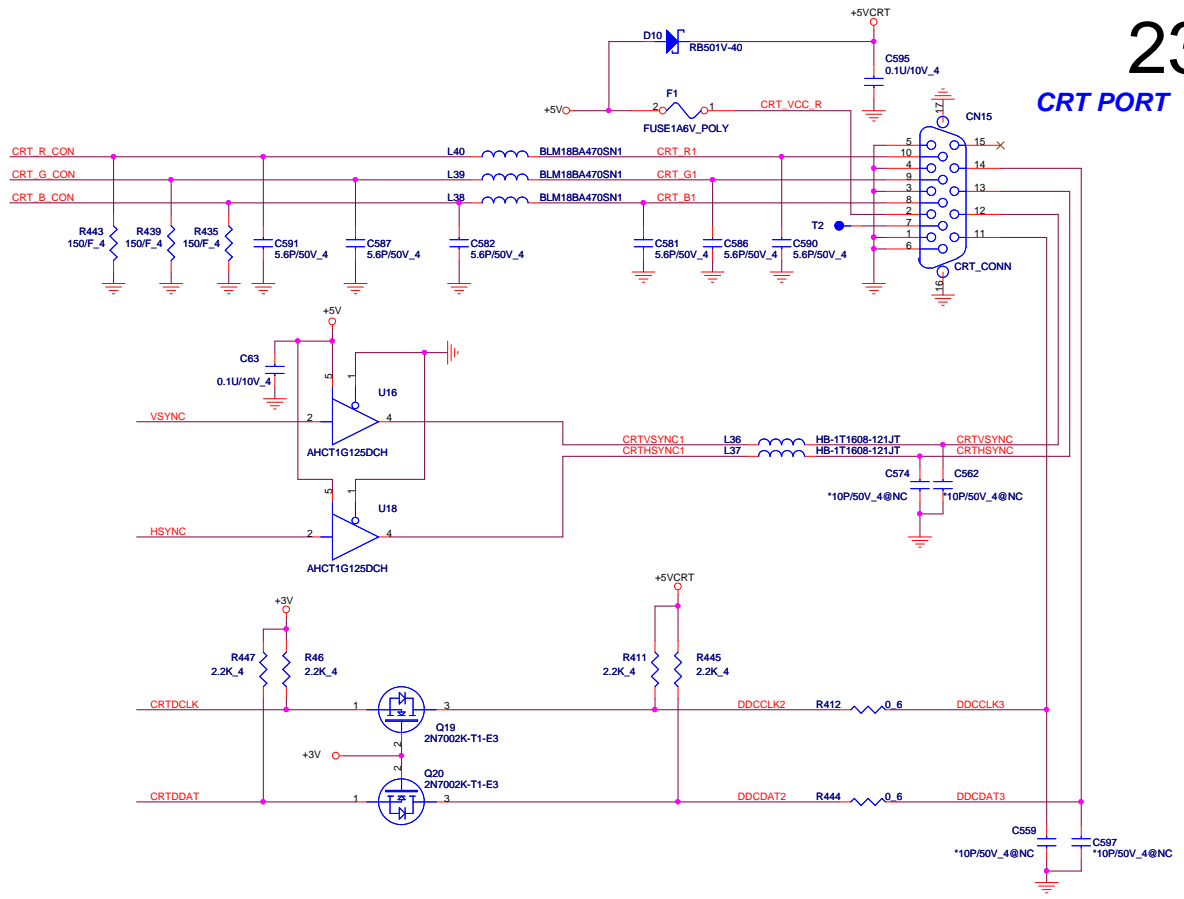


CRT SWITCH



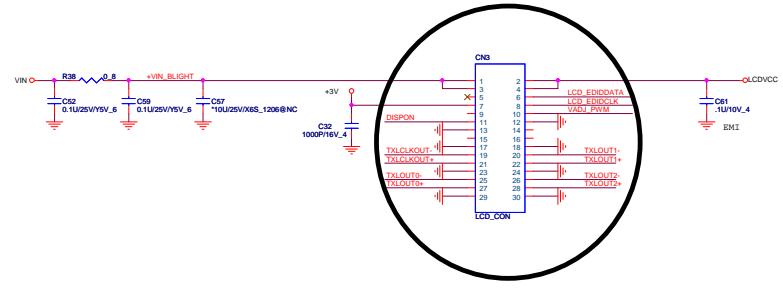
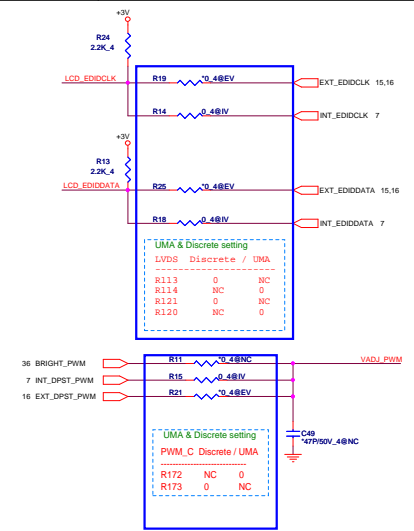
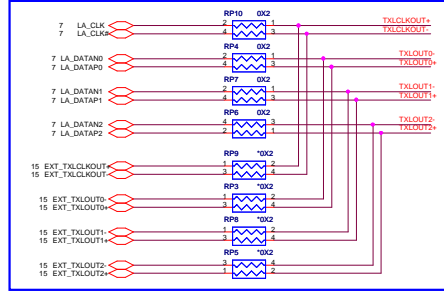
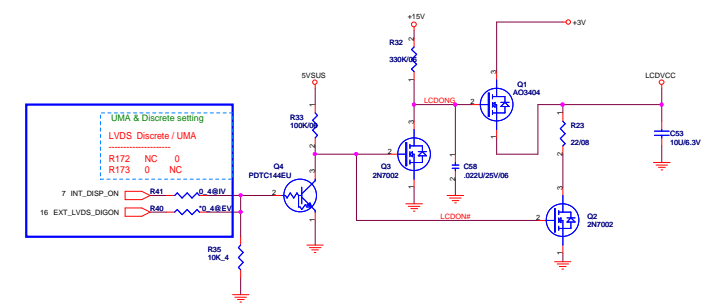
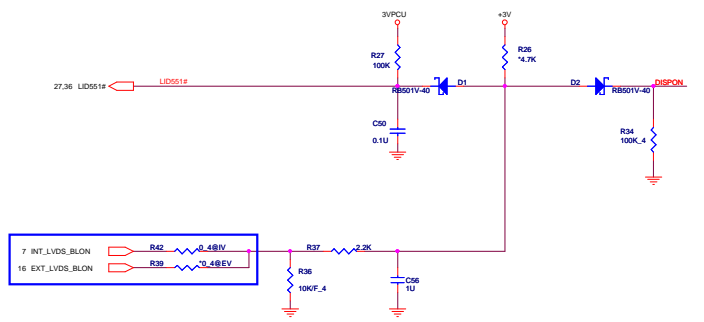
UMA & Discrete setting

LVDS Discrete / UMA		
R556	0	NC
R553	0	NC
R552	0	NC
R557	0	NC
R558	0	NC
R554	0	NC
R555	0	NC
R543	NC	0
R542	NC	0
R541	NC	0
R544	NC	0
R545	NC	0
R547	NC	0
R546	NC	0



PROJECT : LE8
Quanta Computer Inc.

Size Custom	Document Number CRT CON	Rev 1A
Date: Wednesday, November 14, 2007 Sheet 23 of 44		

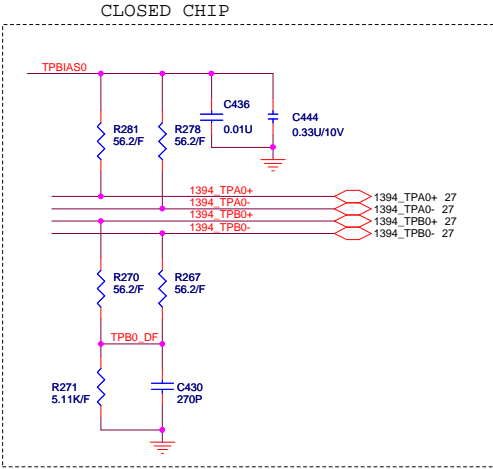
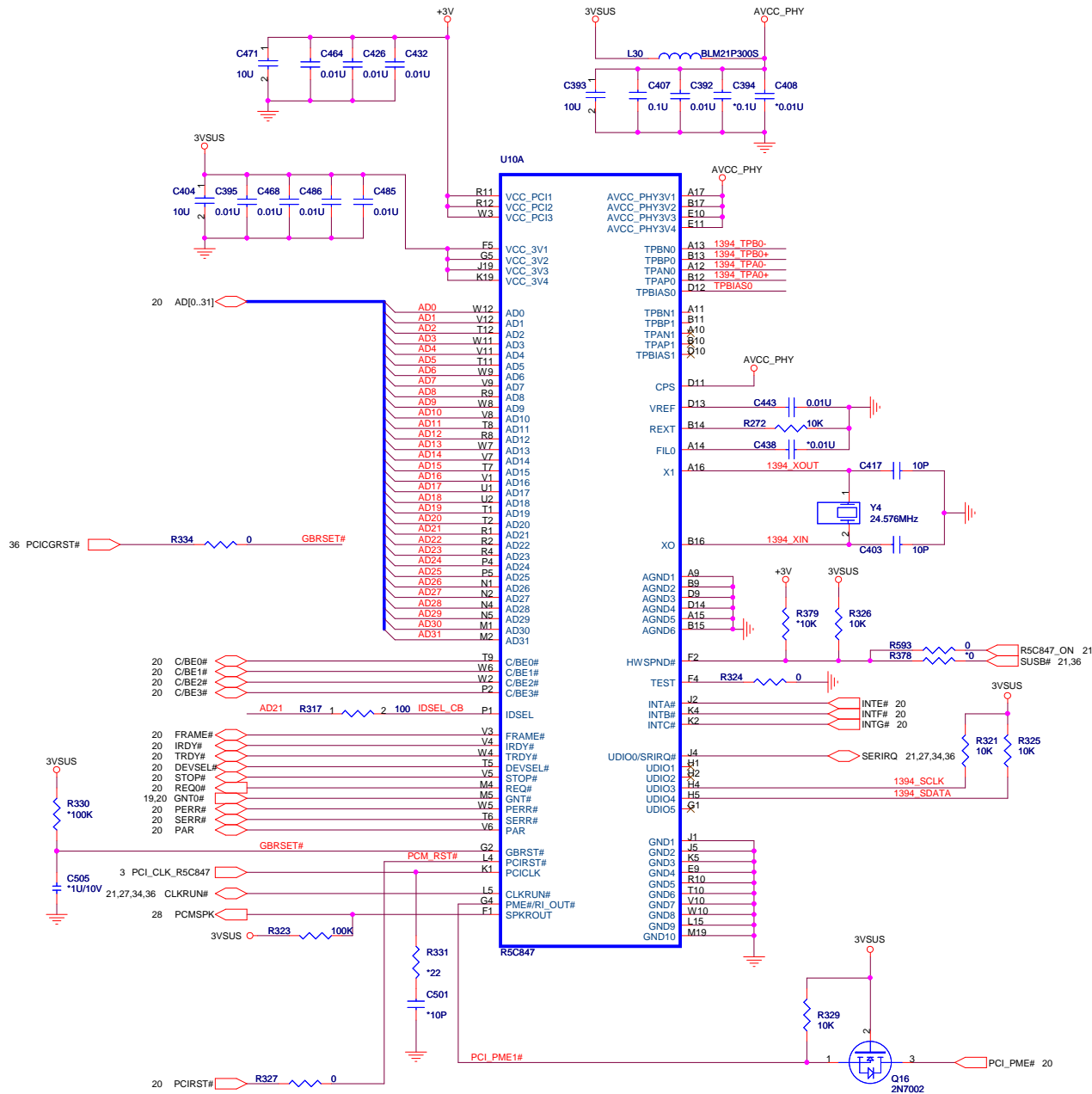


7	INT_LVDS_BLON	R42	0.48kV
16	EXT_LVDS_BLON	R39	0.48kV

UMA & Discrete setting			
LVDS Discrete / UMA			
R172	NC	0	
R173	0	NC	
7	INT_DISP_ON	R41	0.48kV
16	EXT_LVDS_DIGON	R36	0.48kV

UMA & Discrete setting			
LVDS Discrete / UMA			
R113	0	NC	
R114	NC	0	
R121	0	NC	
R120	NC	0	

UMA & Discrete setting			
PWM_C Discrete / UMA			
R172	NC	0	
R173	0	NC	

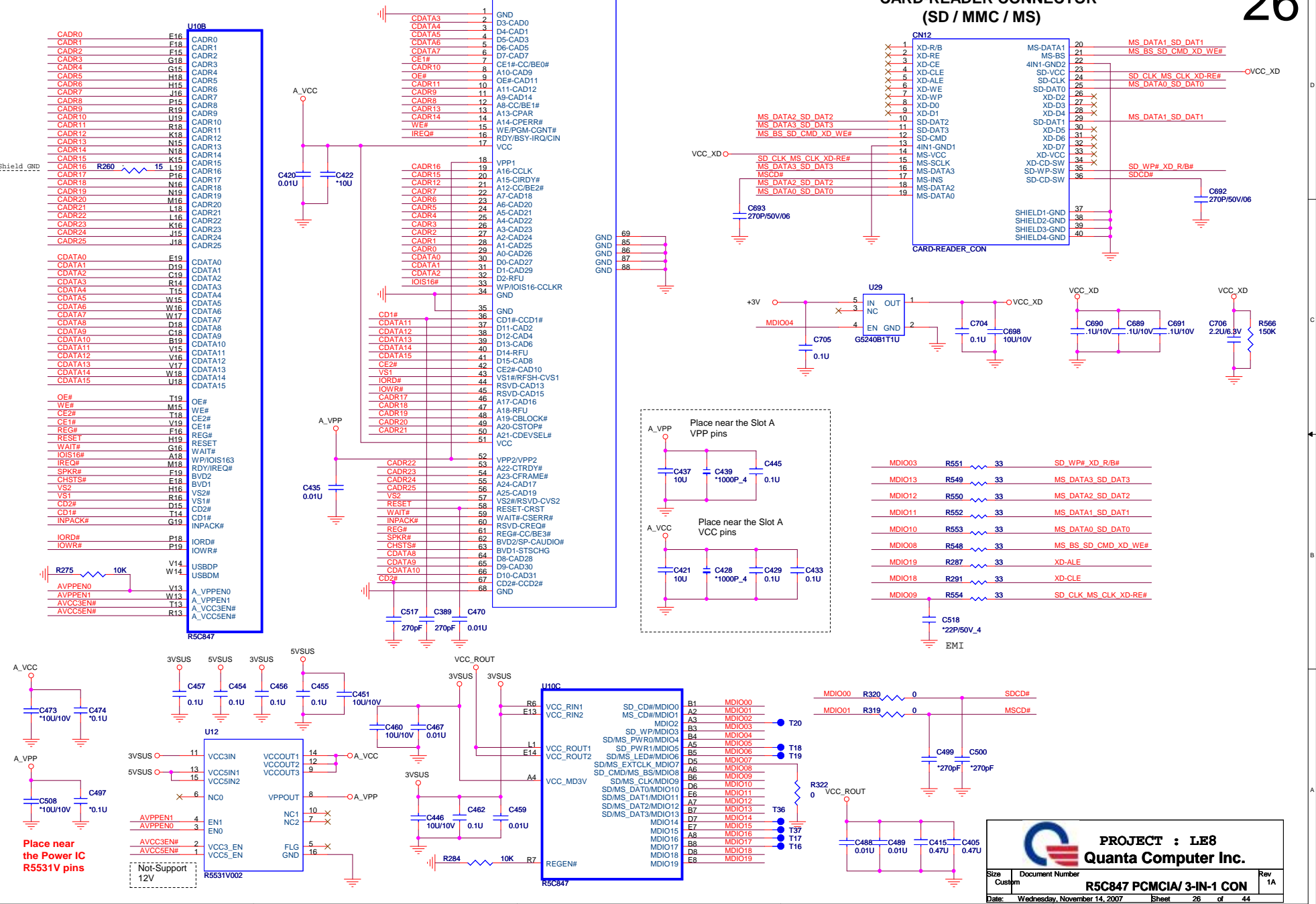


R5C847 pin to pin compatible with R5C843/R5C841

		PROJECT : LE8	
		Quanta Computer Inc.	
Size Custom	Document Number R5C847 PCI/1394	Rev 1A	
Date: Wednesday, November 14, 2007		Sheet 25 of 44	

PCMCIA CONNECTOR

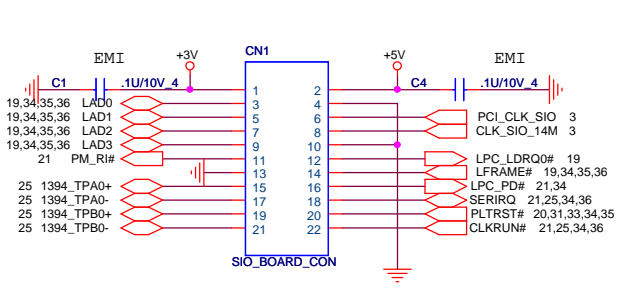
CARD-READER CONNECTOR (SD / MMC / MS)



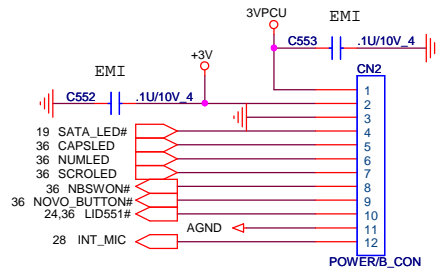
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	R5C847 PCMCIA/ 3-IN-1 CON	1A
Date:	Wednesday, November 14, 2007	Sheet 26 of 44

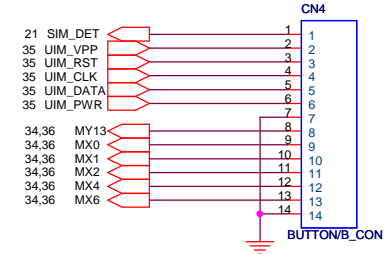
SIO BOARD



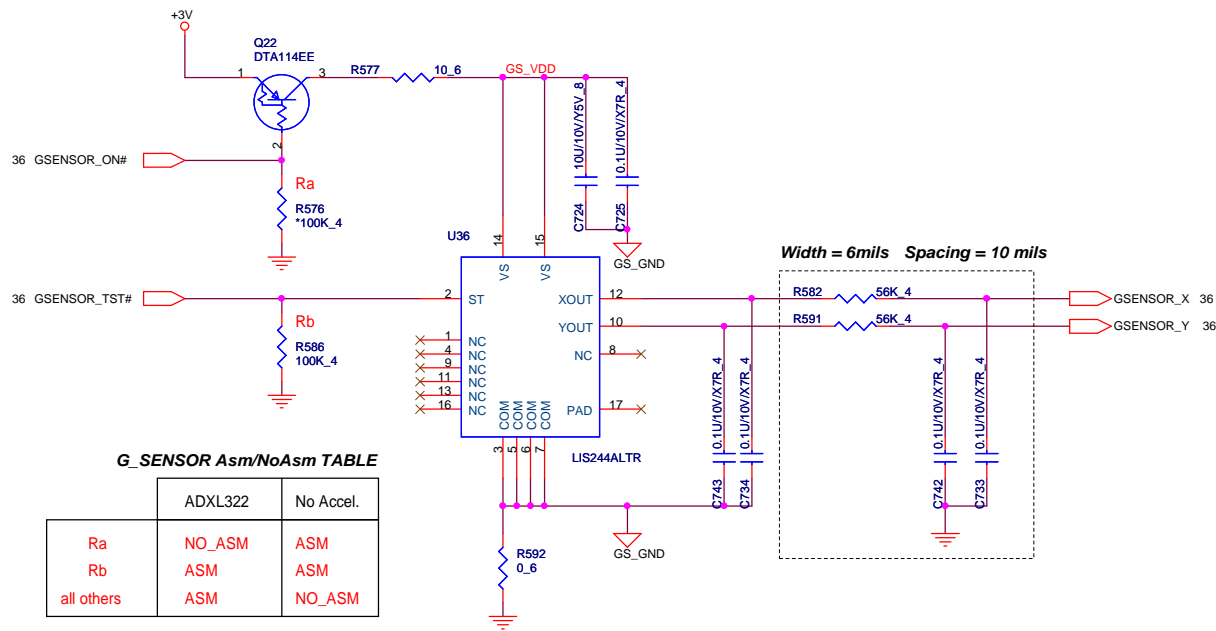
POWER BOARD




BUTTON BOARD



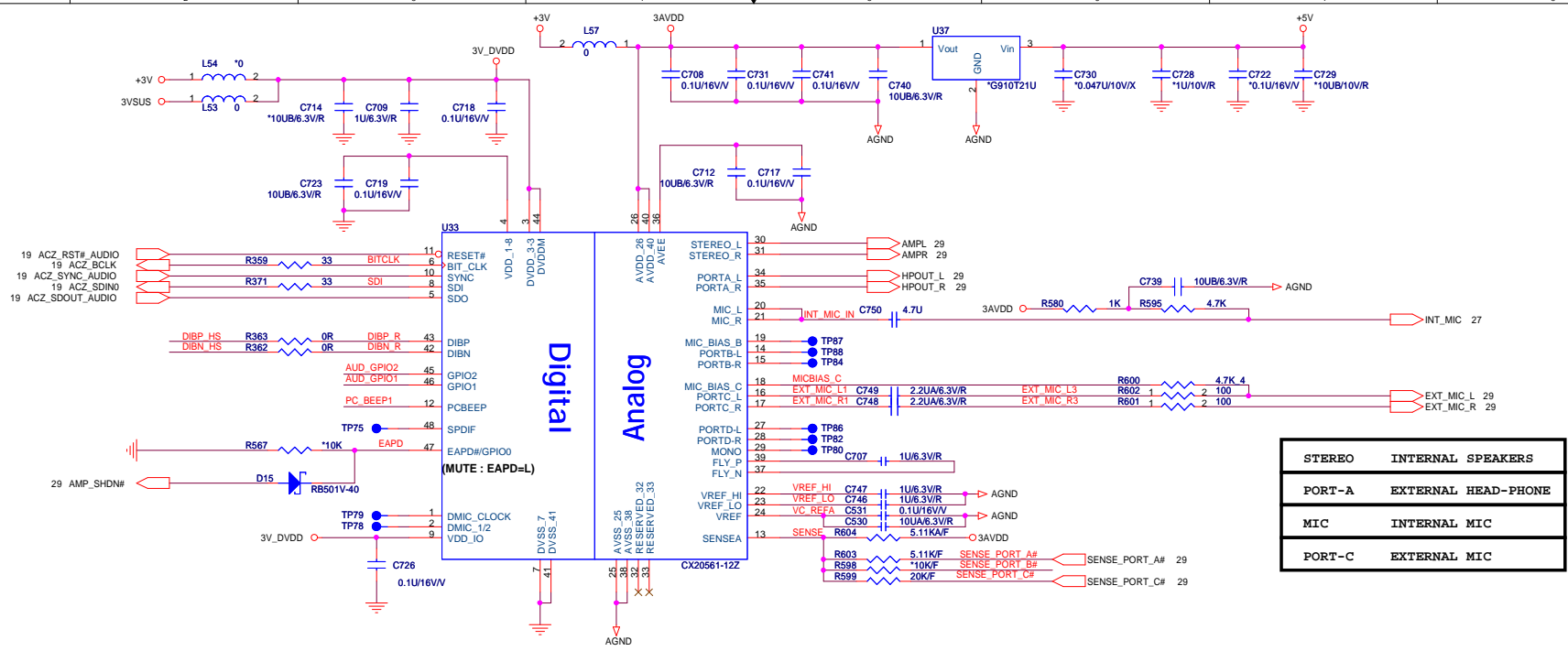
G-SENSOR





PROJECT : LE8
Qanta Computer Inc.

Size Custom	Document Number T/Bs & G-SENSOR	Rev 1A
Date: Wednesday, November 14, 2007 Sheet 27 of 44		



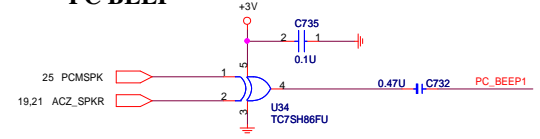
STEREO	INTERNAL SPEAKERS
PORT-A	EXTERNAL HEAD-PHONE
MIC	INTERNAL MIC
PORT-C	EXTERNAL MIC

GAIN	10K GPIO RESISTORS	
	GPIO1	GPIO2
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-16dB	Omit	Populate

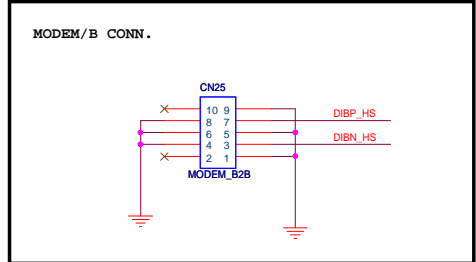
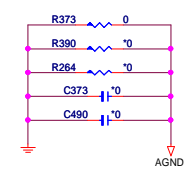
Default gain is -6dB without populating the 10K ohm pull down resistors going to GPIO1 and GPIO2



PC BEEP



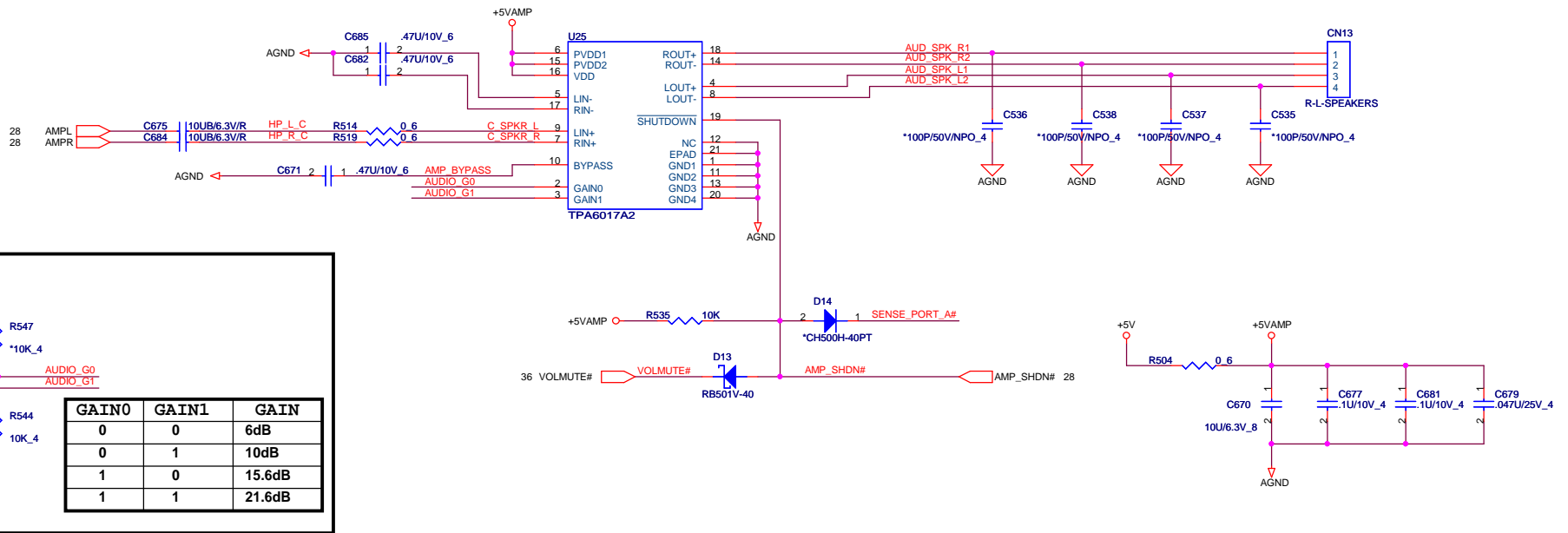
FOR EMI SOLUTION



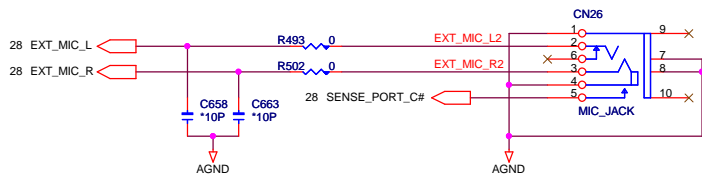
PROJECT : L88
Quanta Computer Inc.

Site Customer	Document Number AUDIO CODEC+MODEM	Rev 1A
Date: Wednesday, November 14, 2007		Sheet 28 of 44

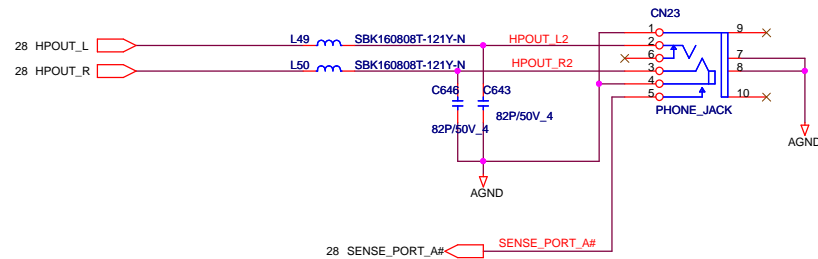
INTERNAL SPEAKER AMPLIFIER




MIC-IN JACK



HEADPHONE

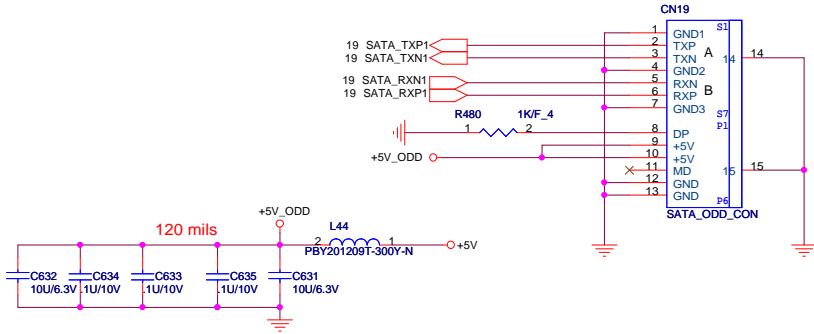




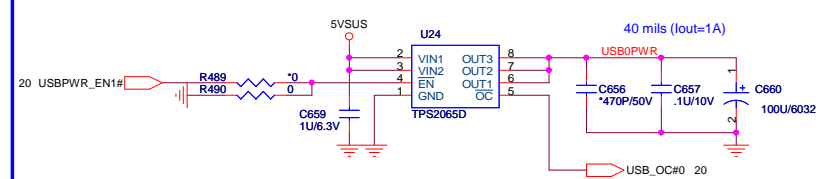
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev	
Custom	AMP_TPA6017 & JACKS	1A	
Date: Wednesday, November 14, 2007		Sheet	29 of 44

SATA CD-ROM

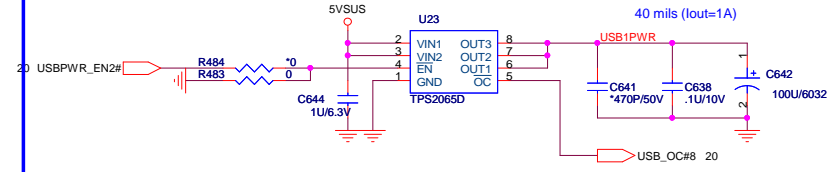
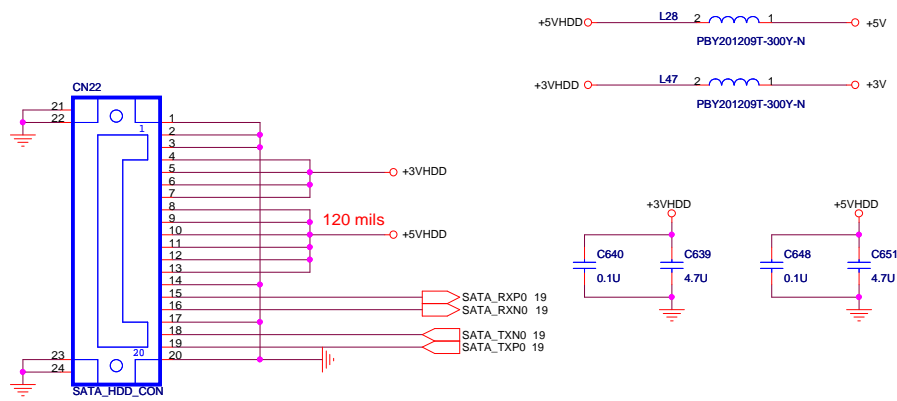


USB2



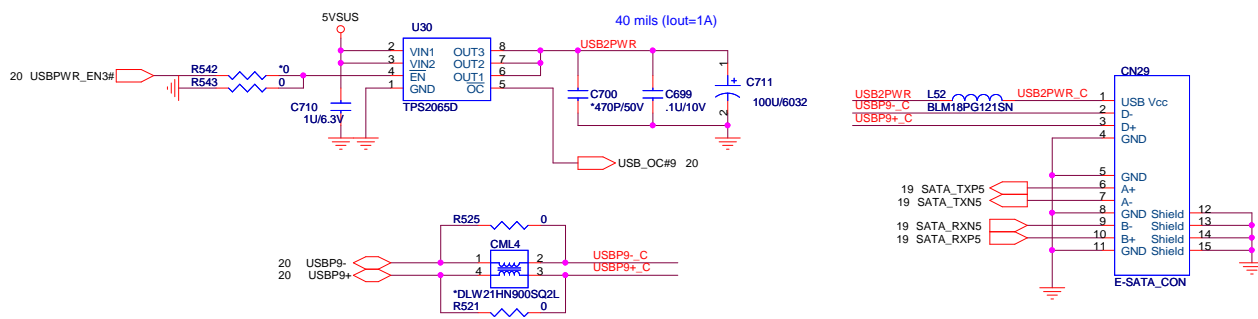
USB 0

SATA-HDD CONNECTOR



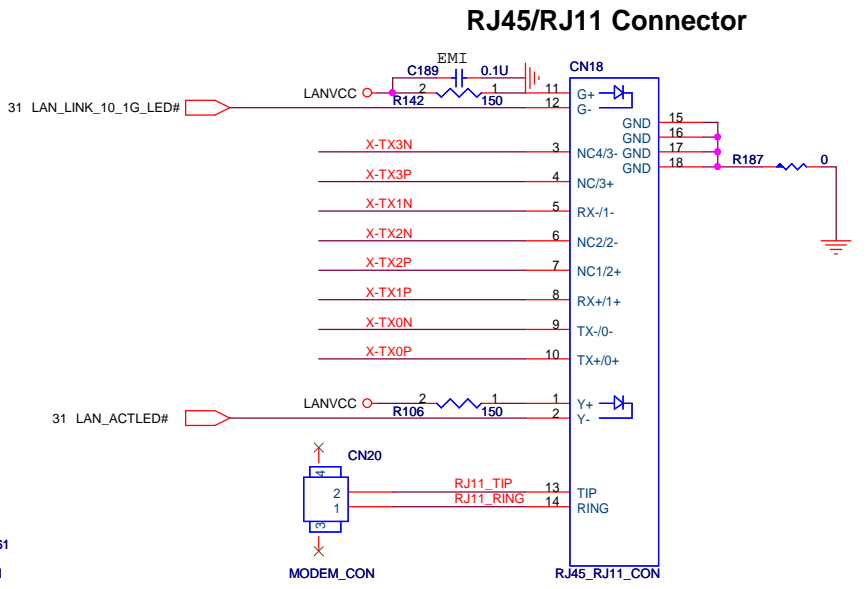
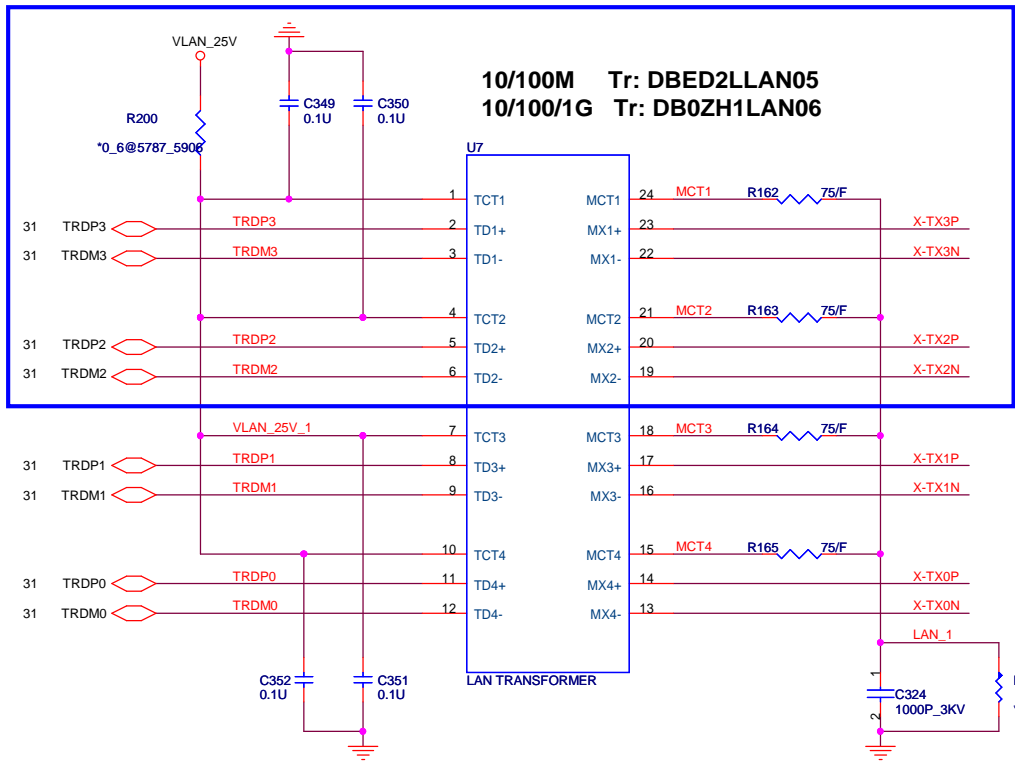
USB 1

USB + eSATA CONNECTOR



PROJECT : LE8
Quanta Computer Inc.

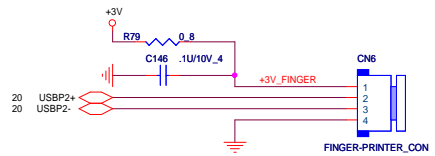
Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USB/ESATA	1A
Date:	Wednesday, November 14, 2007	Sheet 30 of 44



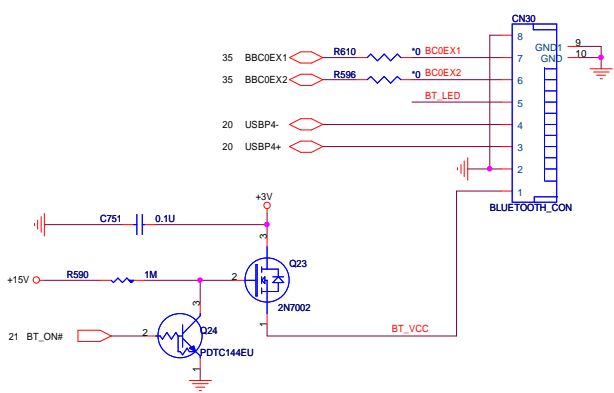
PROJECT : LE8
Quanta Computer Inc.

Size Custom	Document Number RJ11/RJ45 CONNECTOR	Rev 1A
Date: Wednesday, November 14, 2007	Sheet 32 of 44	

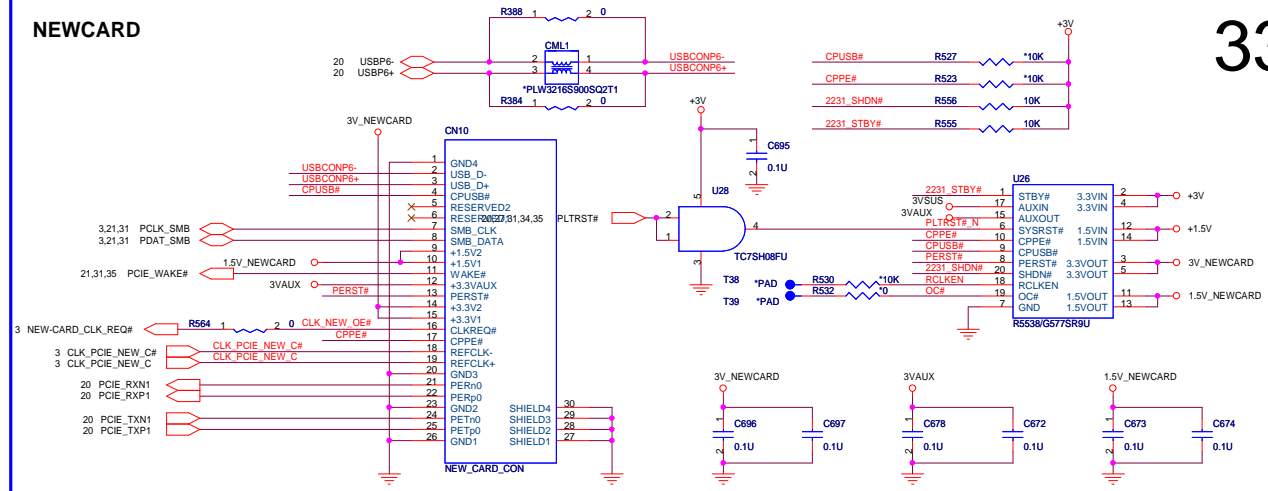
FINGER PRINTER



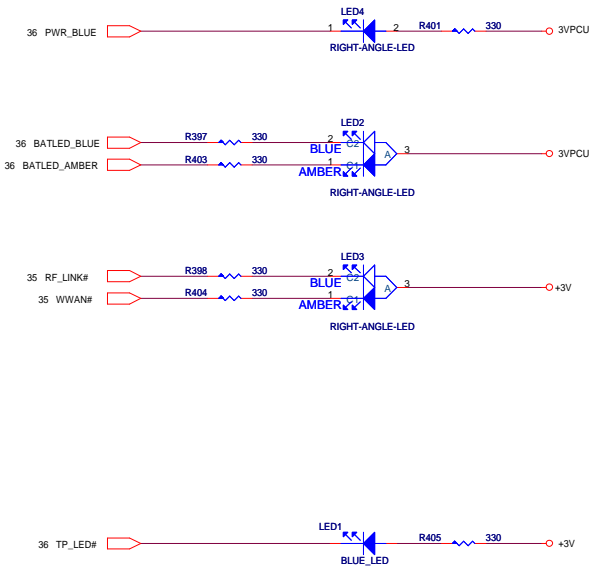
BLUETOOTH



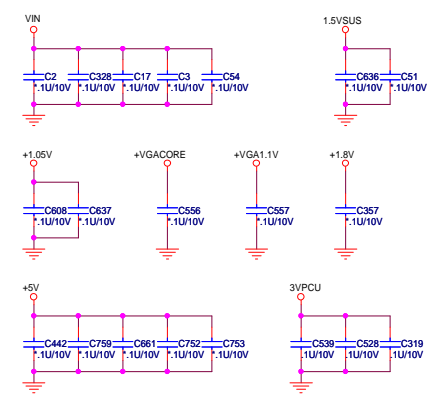
NEWCARD



LED



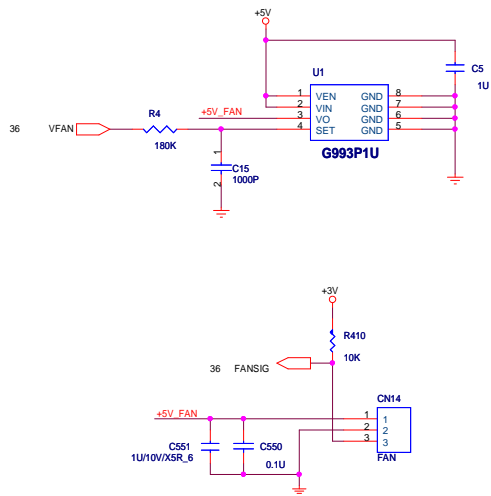
EMI CAPACITORS



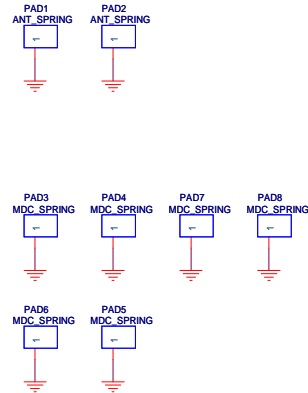
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	F/P, NEW CARD, B/T, LED	1A
Date:	Wednesday, November 14, 2007	Sheet 33 of 44

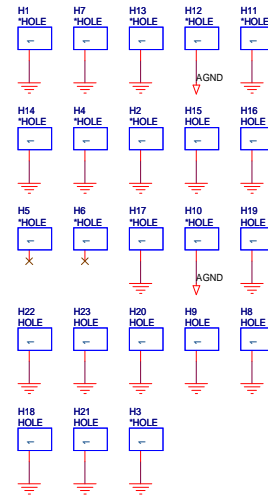
FAN CONTROL



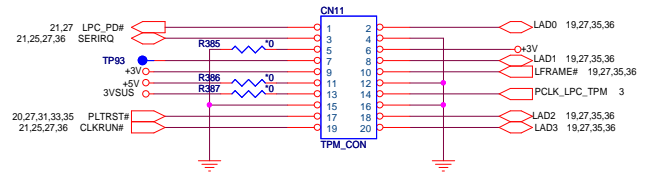
EMI PAD



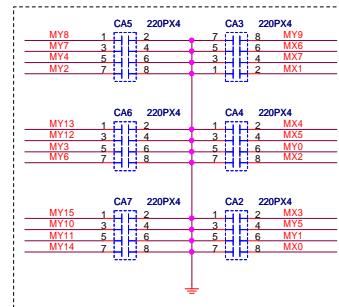
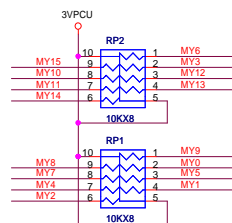
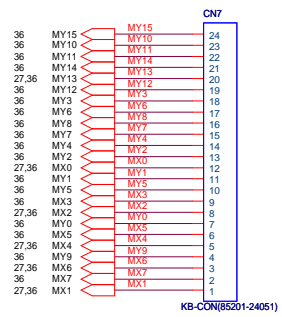
HOLES



Board TO Board TPM MODULE

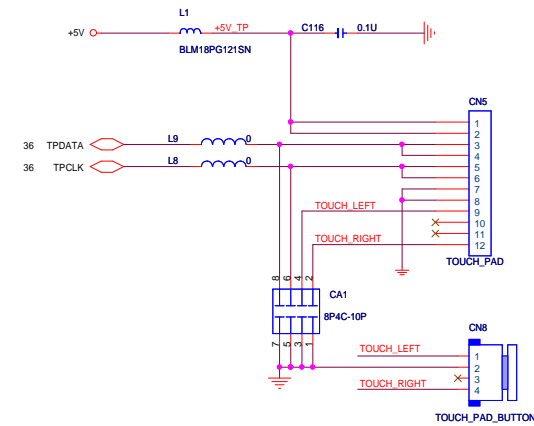


KEYBOARD



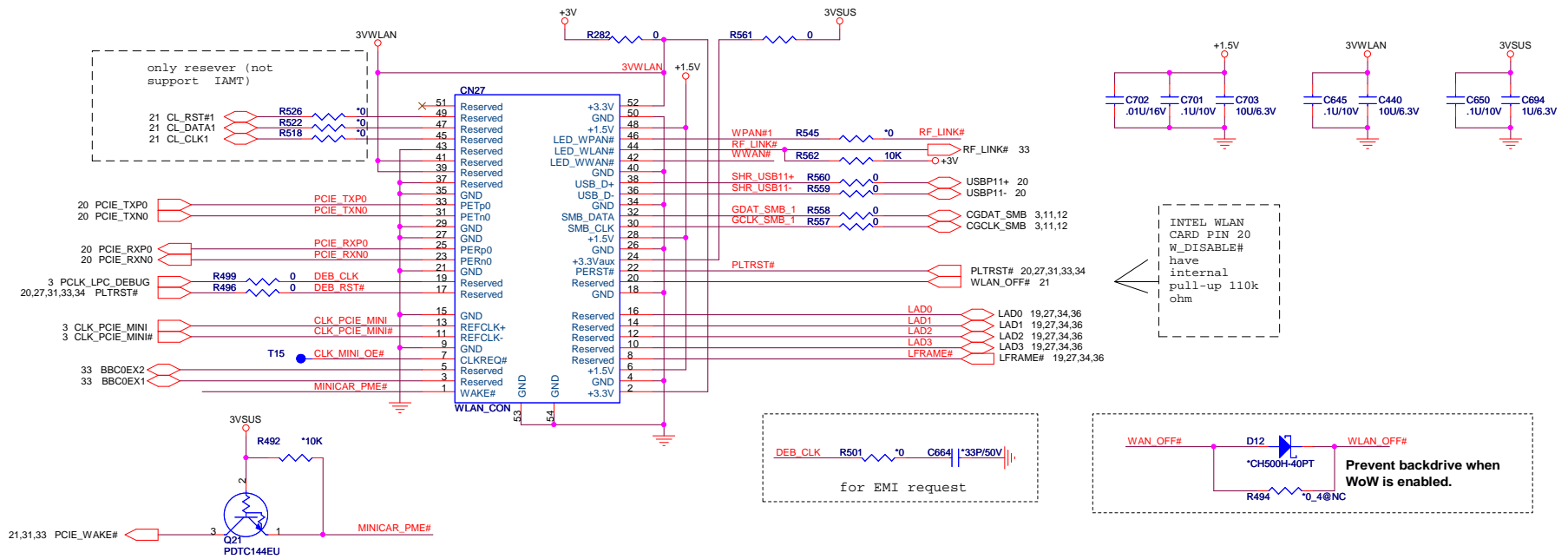
For EMI request

TOUCH PAD

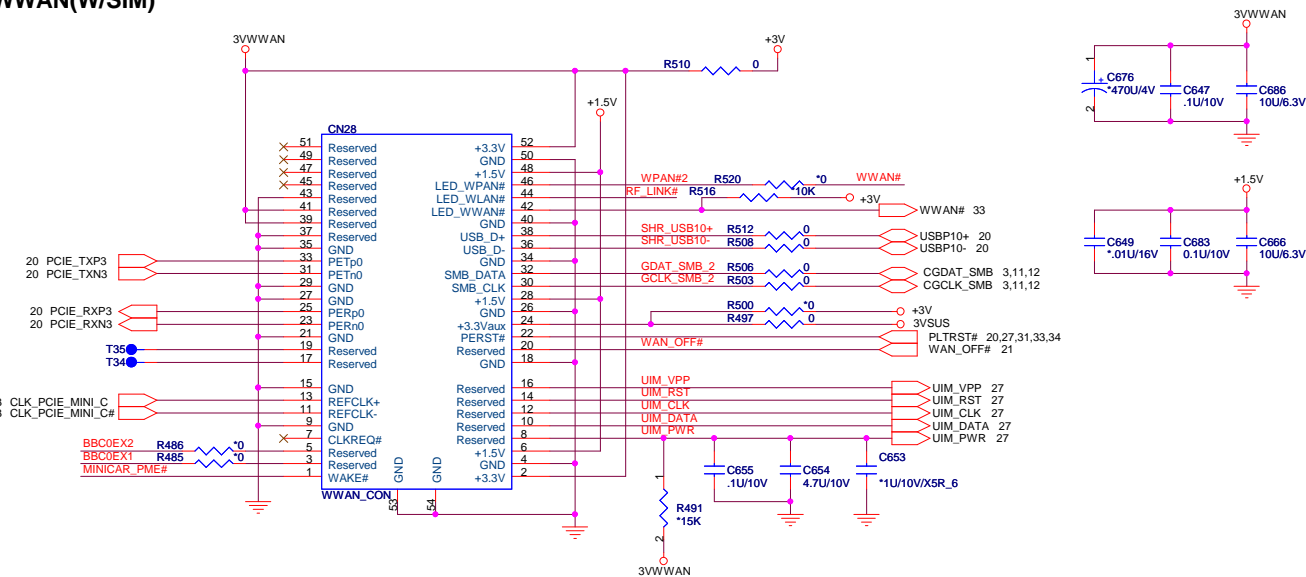



Mini PCI-E Card 1 WLAN

35



Mini PCI-E Card 2 WWAN(W/SIM)

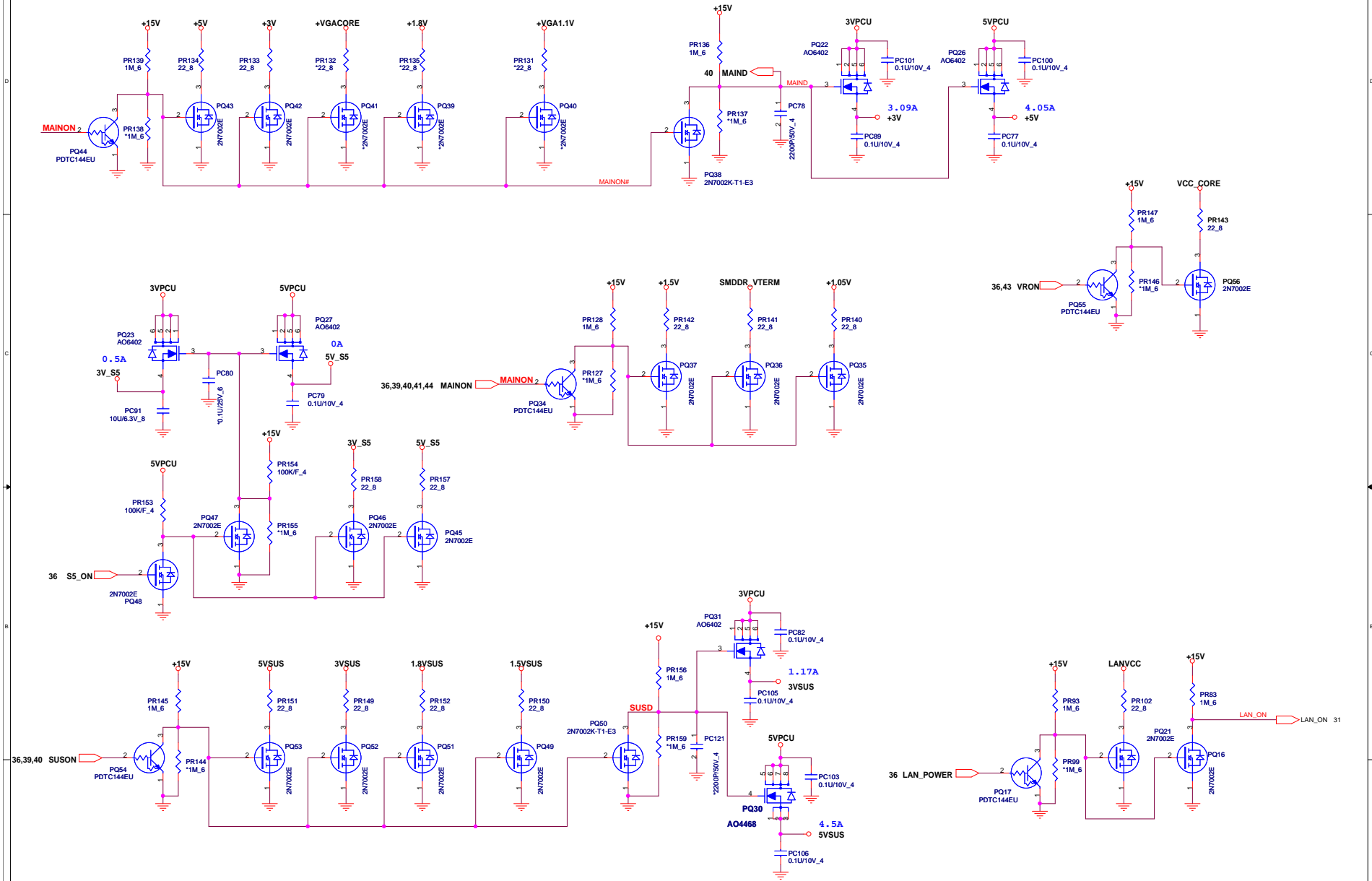


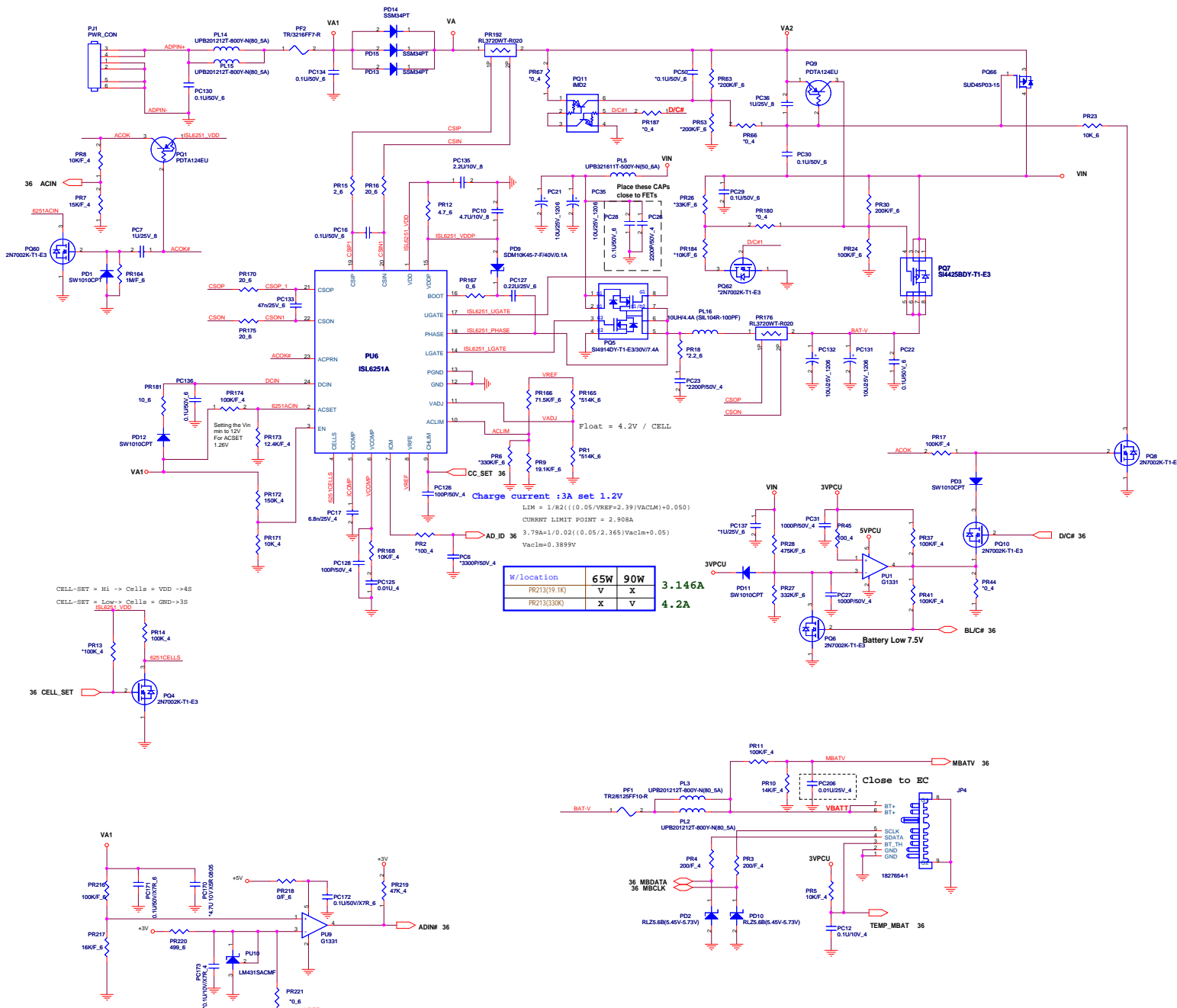


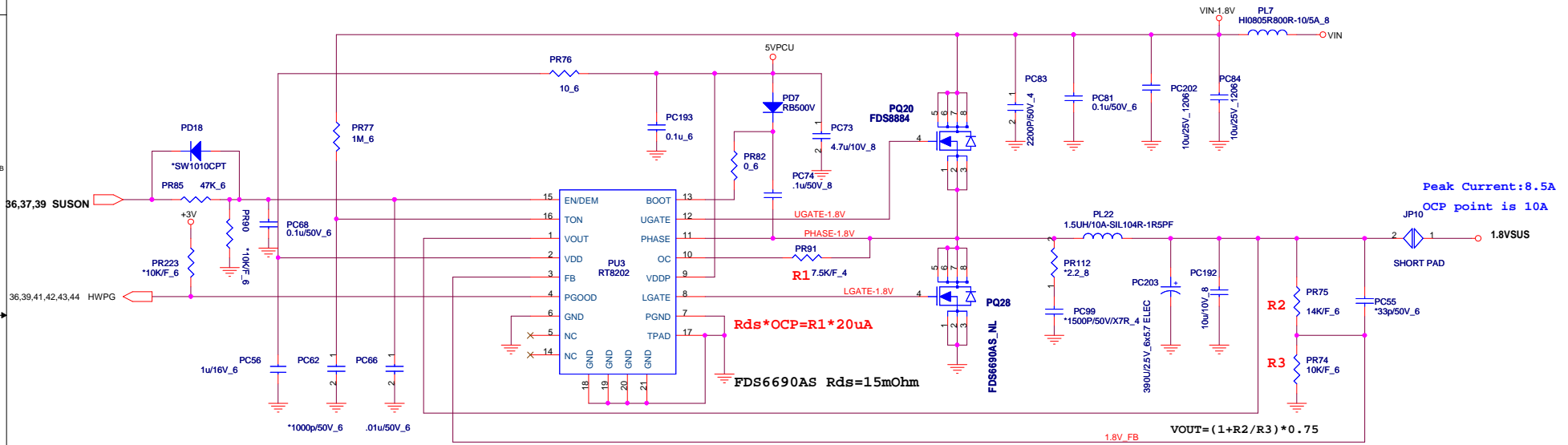
PROJECT : LE8
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN & WWAN CON	1A
Date:	Wednesday, November 14, 2007	Sheet 35 of 44

DISCHARGE







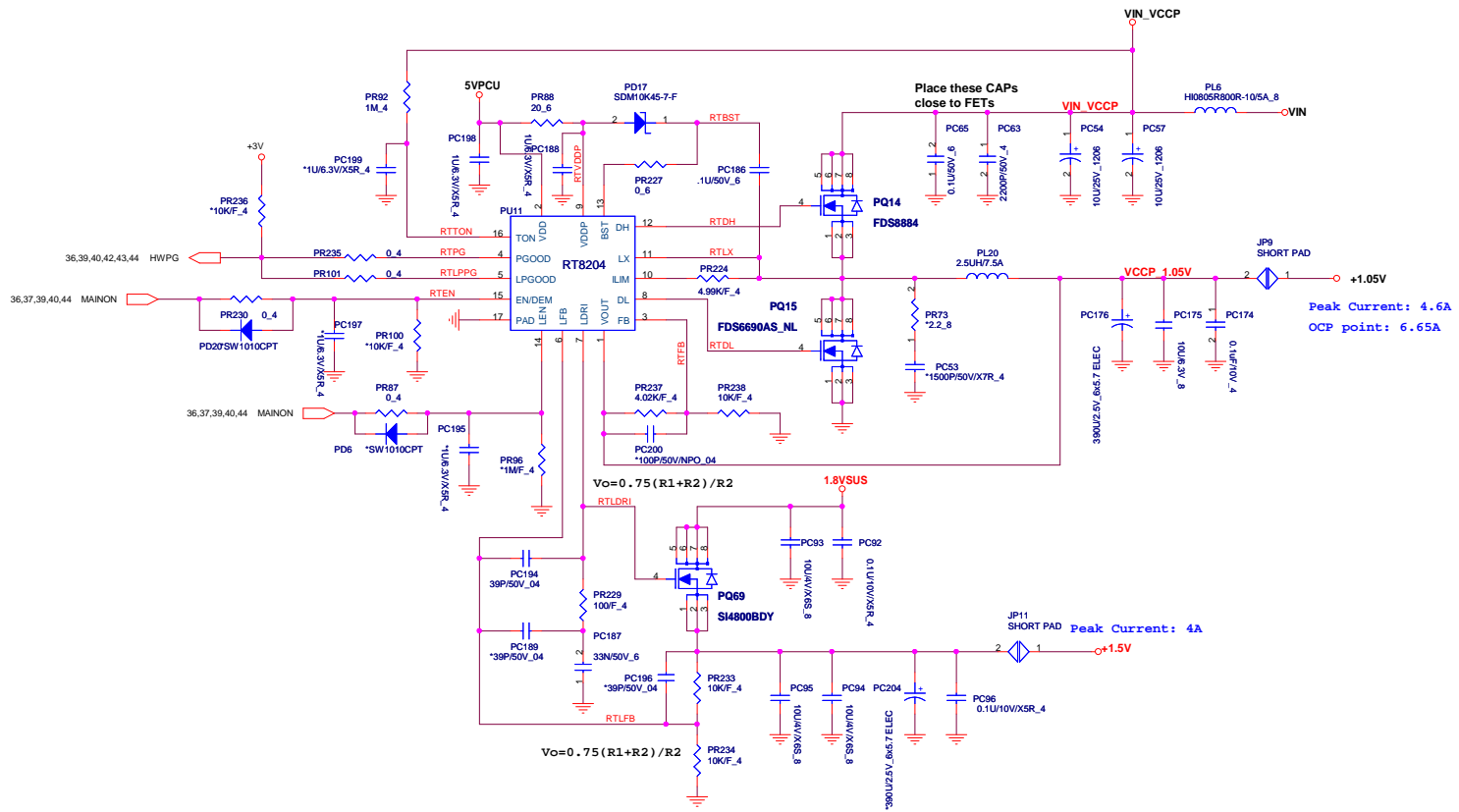
$TON = 3.85p * RTON * Vout / (Vin - 0.5)$

$Frequency = Vout / (Vin * TON)$

$Rds * OCP = R1 * 20uA$

FDS6690AS Rds=15mOhm

$VOUT = (1 + R2 / R3) * 0.75$



DC/DC 3VPCU/5VPCU/+15V

