Compal Confidential

G400/G500 UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

2013-02-27

LA-9632P

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: Cover Page

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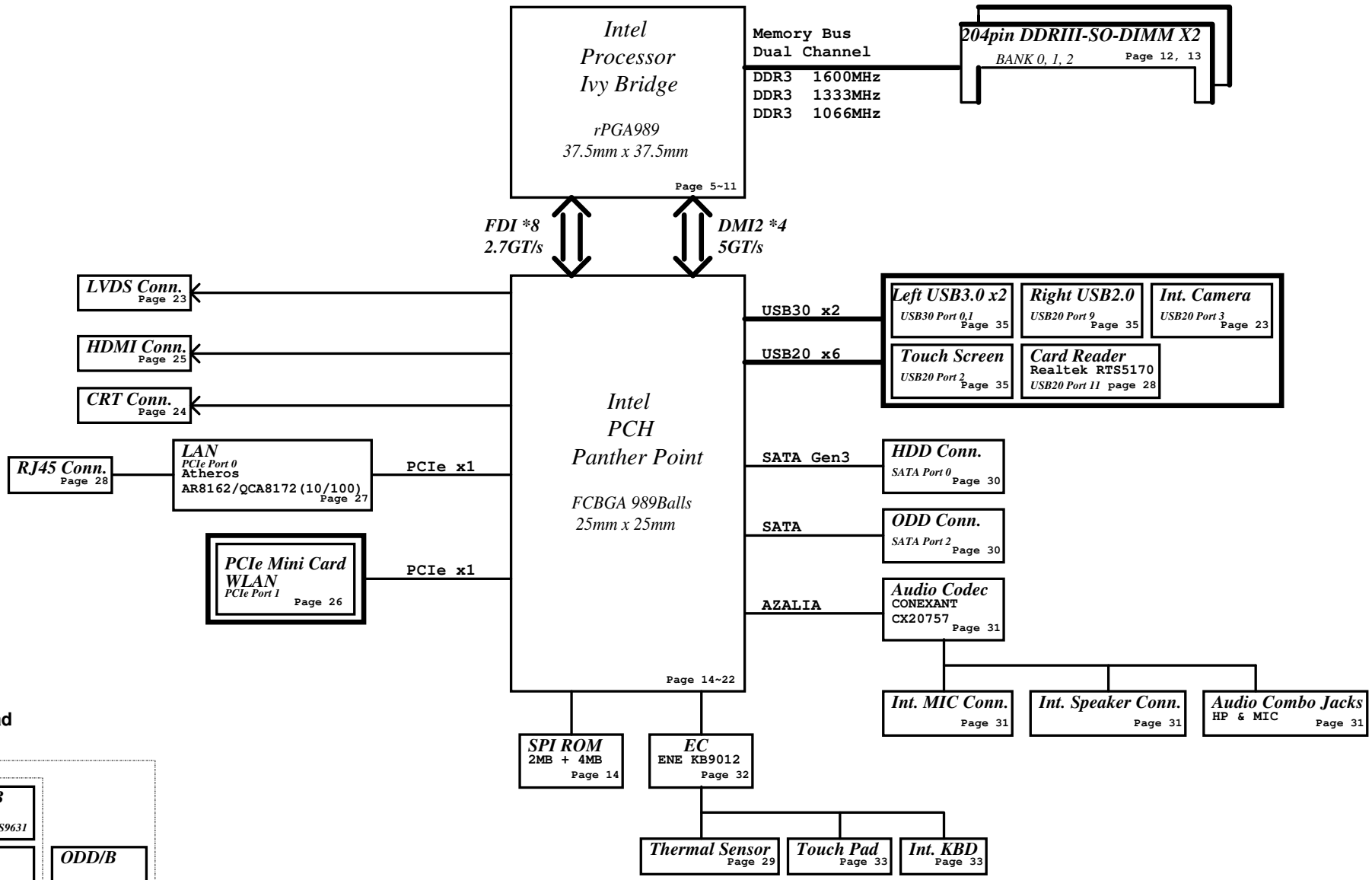
Compal confidential
Project Name : VIWGP (14") / VIWGR (15")

Chief River



Sub-borad

15"
14"

- Power/B (LID) LS9631
- USB/B LS9632
- ODD/B LS9634
- IO/B (Card Reader) LS9633
- Switch/B (LED, LID) LS9635

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Title: MB Block Diagram

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V					
R694	100K +/- 1%					
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0 V	0x00 – 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C – 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D – 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 – 0x30	EVT

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	
DDR_JDIMM1	1010 000x	A0h
DDR_JDIMM2	1010 010x	A4h

AMD-GPU SM Bus address

Device	Address	
Internal thermal sensor	0100 0001	41h

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76,HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VGS	X	X	X	X	V +3VS	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X	V +3VS	X

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Title: Notes List

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Title: VGA Notes List

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ZZZ1 14@

14" UMA PCB_LA9632P
DA6000WP000
PCB 0Y0 LA-9632P REV0 M/B UMA 3

ZZZ2 15@

15" UMA PCB_LA9632P
DA6000WPT00
PCB 0Y0 LA-9632P REV0 M/B UMA 5

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

+V1.05S_VCCP

R1
24.9_0402_1%

JCPU1A

<16> DMI_CRX_PTX_N0	B27	DMI_RX#[0]	DMI
<16> DMI_CRX_PTX_N1	B25	DMI_RX#[1]	
<16> DMI_CRX_PTX_N2	A25	DMI_RX#[2]	
<16> DMI_CRX_PTX_N3	B24	DMI_RX#[3]	
<16> DMI_CRX_PTX_P0	B28	DMI_RX[0]	
<16> DMI_CRX_PTX_P1	B26	DMI_RX[1]	
<16> DMI_CRX_PTX_P2	A24	DMI_RX[2]	
<16> DMI_CRX_PTX_P3	B23	DMI_RX[3]	
<16> DMI_CTX_PRX_N0	G21	DMI_TX#[0]	
<16> DMI_CTX_PRX_N1	E22	DMI_TX#[1]	
<16> DMI_CTX_PRX_N2	F21	DMI_TX#[2]	
<16> DMI_CTX_PRX_N3	D21	DMI_TX#[3]	
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<16> DMI_CTX_PRX_P2	F20	DMI_TX[2]	
<16> DMI_CTX_PRX_P3	C21	DMI_TX[3]	
<16> FDI_CTX_PRX_N0	A21	FDI0_TX#[0]	Intel(R) FDI
<16> FDI_CTX_PRX_N1	H19	FDI0_TX#[1]	
<16> FDI_CTX_PRX_N2	E19	FDI0_TX#[2]	
<16> FDI_CTX_PRX_N3	F18	FDI0_TX#[3]	
<16> FDI_CTX_PRX_N4	B21	FDI1_TX#[0]	
<16> FDI_CTX_PRX_N5	C20	FDI1_TX#[1]	
<16> FDI_CTX_PRX_N6	D18	FDI1_TX#[2]	
<16> FDI_CTX_PRX_N7	E17	FDI1_TX#[3]	
<16> FDI_CTX_PRX_P0	A22	FDI0_TX[0]	
<16> FDI_CTX_PRX_P1	G19	FDI0_TX[1]	
<16> FDI_CTX_PRX_P2	E20	FDI0_TX[2]	
<16> FDI_CTX_PRX_P3	G18	FDI0_TX[3]	
<16> FDI_CTX_PRX_P4	B20	FDI1_TX[0]	
<16> FDI_CTX_PRX_P5	C19	FDI1_TX[1]	
<16> FDI_CTX_PRX_P6	D19	FDI1_TX[2]	
<16> FDI_CTX_PRX_P7	F17	FDI1_TX[3]	
<16> FDI_FSYNC0	J18	FDI0_FSYNC	
<16> FDI_FSYNC1	J17	FDI1_FSYNC	
<16> FDI_INT	H20	FDI_INT	
<16> FDI_LSYNC0	J19	FDI0_LSYNC	
<16> FDI_LSYNC1	H17	FDI1_LSYNC	
EDP_COMP	A18	eDP_COMPIO	eDP
	A17	eDP_ICOMPO	
eDP_HPD	B16	eDP_HPD#	
	C15	eDP_AUX	
	D15	eDP_AUX#	
	C17	eDP_TX[0]	
	F16	eDP_TX[1]	
	C16	eDP_TX[2]	
	G15	eDP_TX[3]	
	C18	eDP_TX#[0]	
	E16	eDP_TX#[1]	
	D16	eDP_TX#[2]	
	F15	eDP_TX#[3]	

PEG_ICOMPI	J22	PEG_COMP
PEG_ICOMPO	J21	
PEG_RCOMPO	H22	
PEG_RX#[0]	K33	PCI EXPRESS* - GRAPHICS
PEG_RX#[1]	M35	
PEG_RX#[2]	L34	
PEG_RX#[3]	J35	
PEG_RX#[4]	J32	
PEG_RX#[5]	H34	
PEG_RX#[6]	H31	
PEG_RX#[7]	G33	
PEG_RX#[8]	G30	
PEG_RX#[9]	F35	
PEG_RX#[10]	E34	
PEG_RX#[11]	E32	
PEG_RX#[12]	D33	
PEG_RX#[13]	D31	
PEG_RX#[14]	B33	
PEG_RX#[15]	C32	
PEG_RX[0]	J33	
PEG_RX[1]	L35	
PEG_RX[2]	K34	
PEG_RX[3]	H35	
PEG_RX[4]	H32	
PEG_RX[5]	G34	
PEG_RX[6]	G31	
PEG_RX[7]	F33	
PEG_RX[8]	F30	
PEG_RX[9]	E35	
PEG_RX[10]	E33	
PEG_RX[11]	F32	
PEG_RX[12]	D34	
PEG_RX[13]	E31	
PEG_RX[14]	C33	
PEG_RX[15]	B32	
PEG_TX#[0]	M29	
PEG_TX#[1]	M32	
PEG_TX#[2]	M31	
PEG_TX#[3]	L32	
PEG_TX#[4]	L29	
PEG_TX#[5]	K31	
PEG_TX#[6]	K28	
PEG_TX#[7]	J30	
PEG_TX#[8]	J28	
PEG_TX#[9]	H29	
PEG_TX#[10]	G27	
PEG_TX#[11]	F29	
PEG_TX#[12]	F27	
PEG_TX#[13]	D28	
PEG_TX#[14]	F26	
PEG_TX#[15]	E25	
PEG_TX[0]	M28	
PEG_TX[1]	M33	
PEG_TX[2]	M30	
PEG_TX[3]	L31	
PEG_TX[4]	L28	
PEG_TX[5]	K30	
PEG_TX[6]	K27	
PEG_TX[7]	J29	
PEG_TX[8]	J27	
PEG_TX[9]	H28	
PEG_TX[10]	G28	
PEG_TX[11]	E28	
PEG_TX[12]	F28	
PEG_TX[13]	D27	
PEG_TX[14]	E26	
PEG_TX[15]	D25	

TYCO_2013620-2_IVY BRIDGE

ME@

PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

+V1.05S_VCCP

R7
24.9_0402_1%

EDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

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Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

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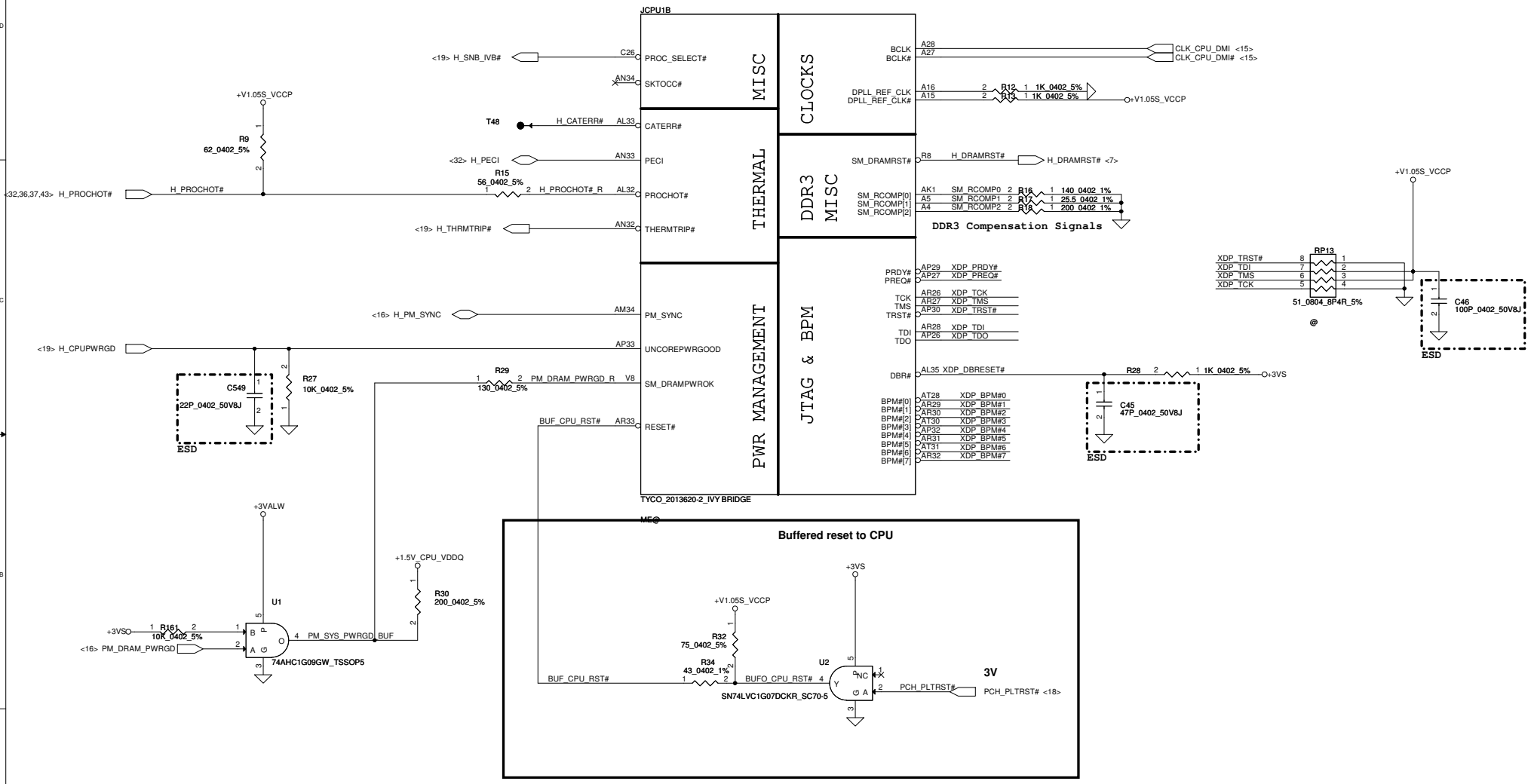

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Compal Electronics, Inc.

Title: **PROCESSOR(2/7) PM,XDP,CLK**

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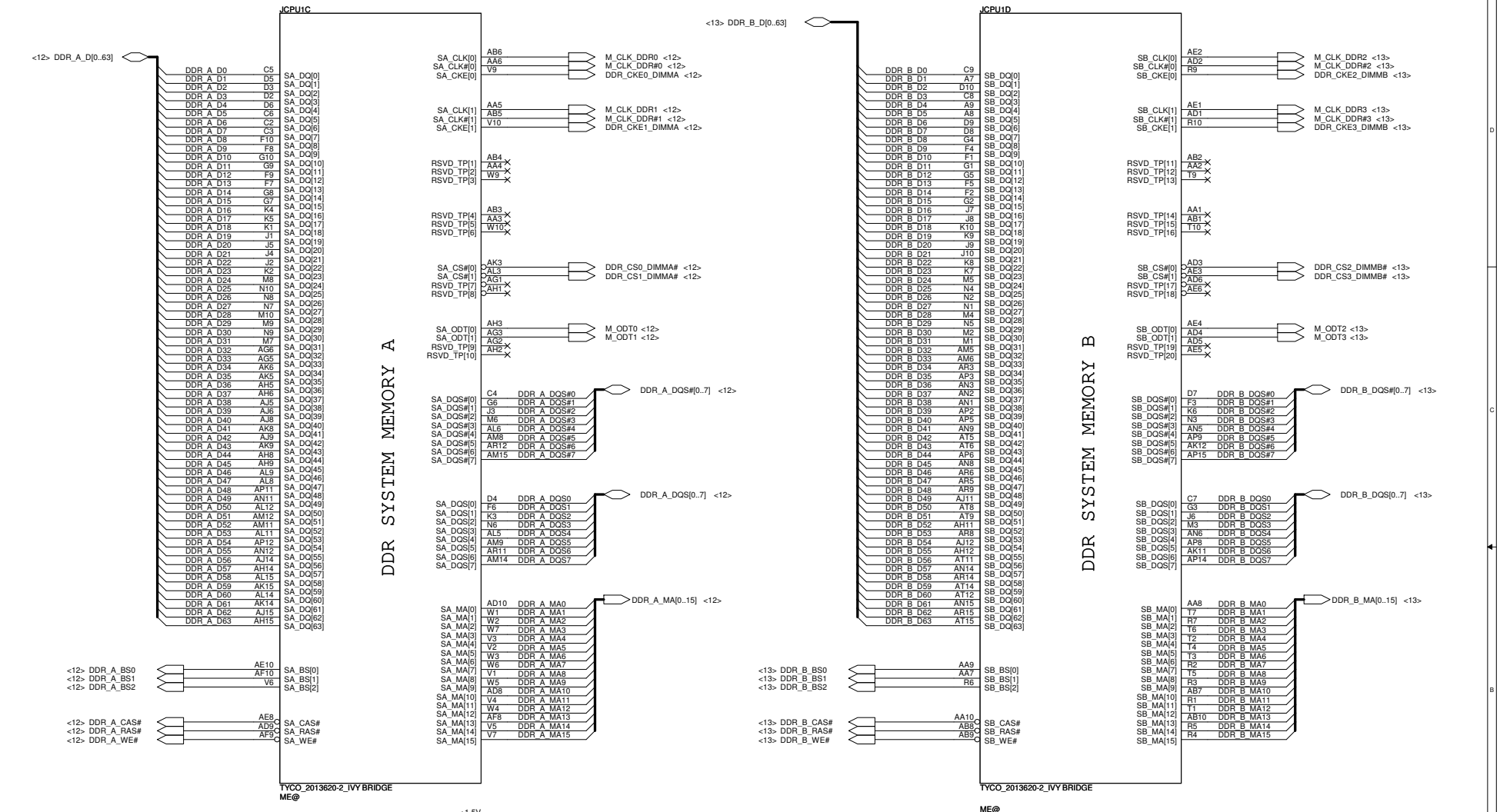

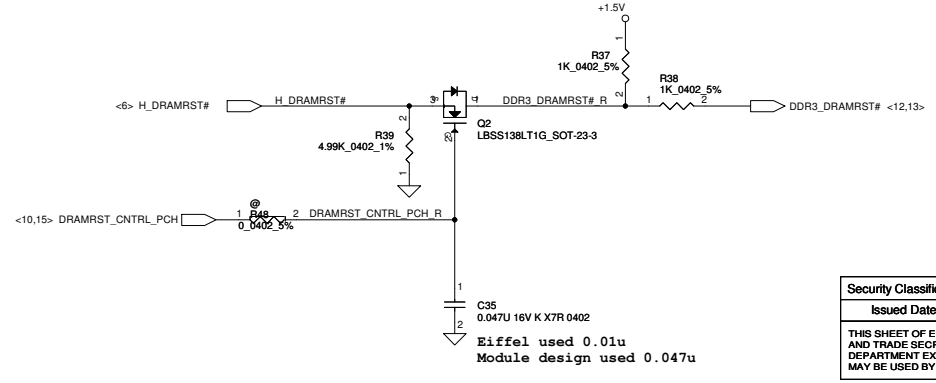

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Compal Electronics, Inc.

Title: **PROCESSOR(3/7) DDRIII**

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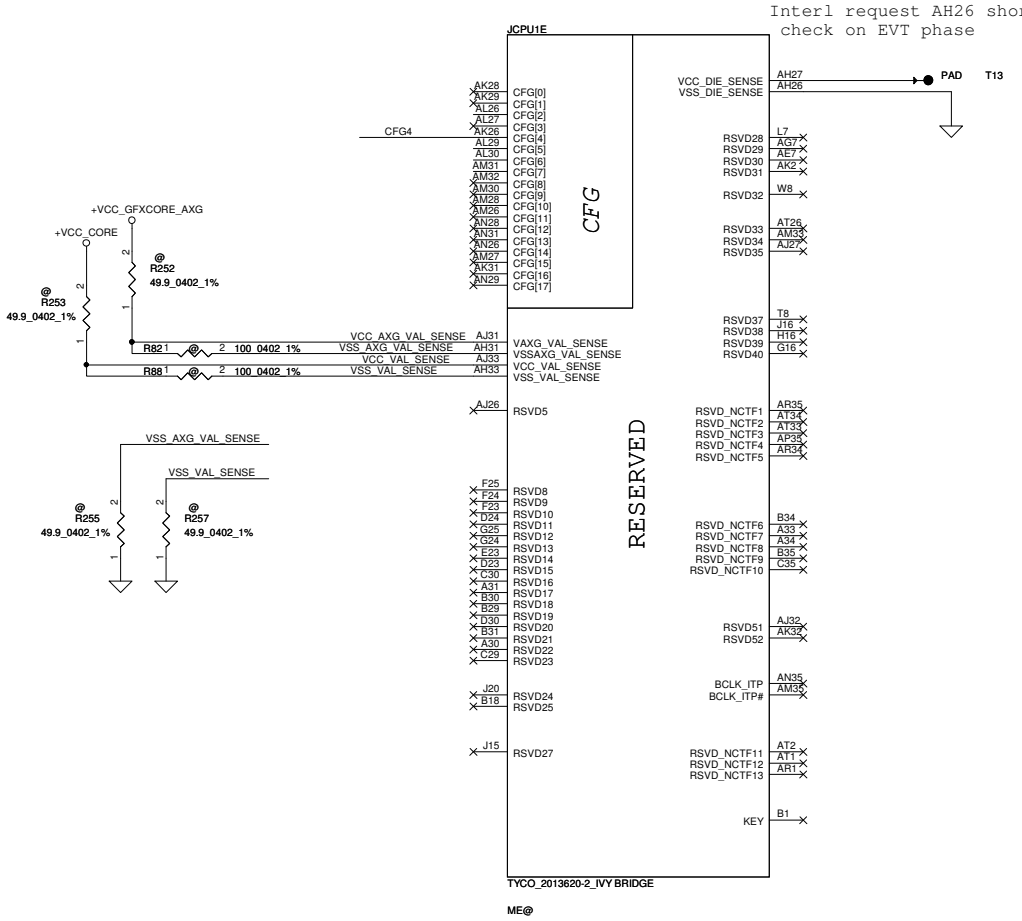
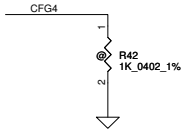
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

SVID

VIDALERT#	AJ29	H_CPU_SVIDALRT#
VIDSCLK	AJ30	
VIDSOUT	AJ28	

+V1.05S_VCCP

R46
75_0402_5%

VR_SVID_CLK series-resistors close to VR

R47 43_0402_5%

VR_SVID_ALRT# <43>
VR_SVID_CLK <43>
VR_SVID_DAT <43>

R50 130_0402_5% +V1.05S_VCCP 0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

VCC_SENSE	AJ35	
VSS_SENSE	AJ34	
VCCIO_SENSE	B10	
VSS_SENSE_VCCIO	A10	VSSIO_SENSE_L

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51
100_0402_1%

VCCSENSE <43>
VSSSENSE <43>

R54
100_0402_1%

R74 10_0402_1% 2VSSIO_SENSE

VCCIO_SENSE <42>

R74 & R79 put together

VSSIO_SENSE_L <42>

+V1.05S_VCCP

R79
10_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

ME@

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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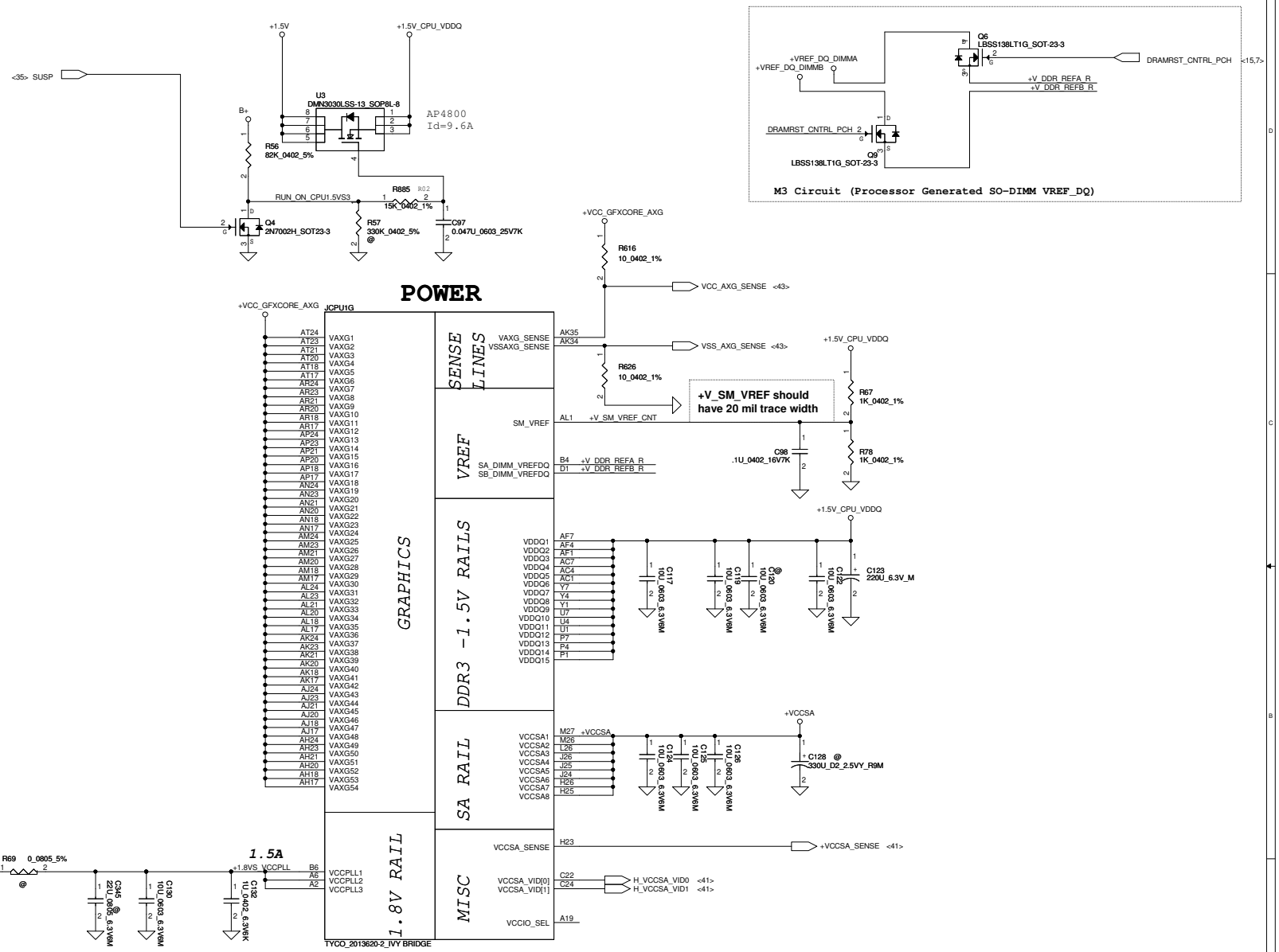
Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: LA-9632P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 9 of 60



IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0
Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: **PROCESSOR(6/7) PWR**

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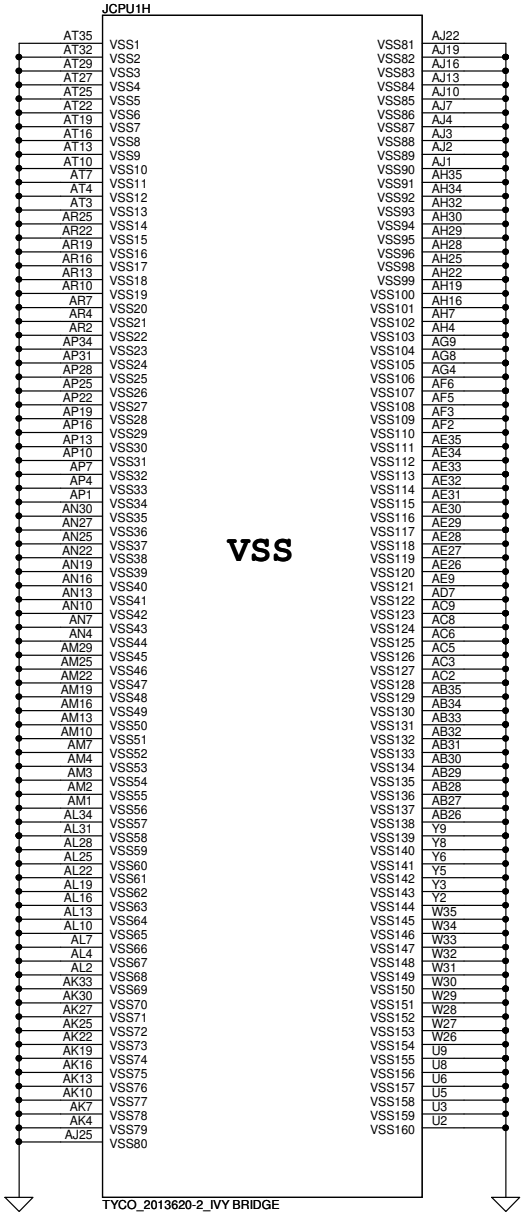
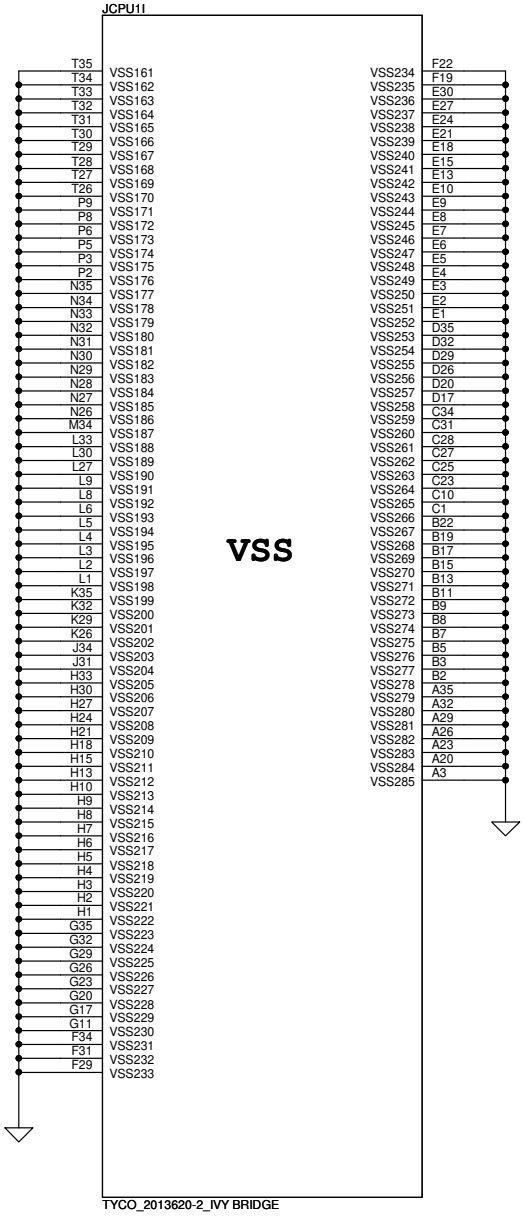
Date: Wednesday, February 27, 2013 | Sheet 10 of 60





ME@

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

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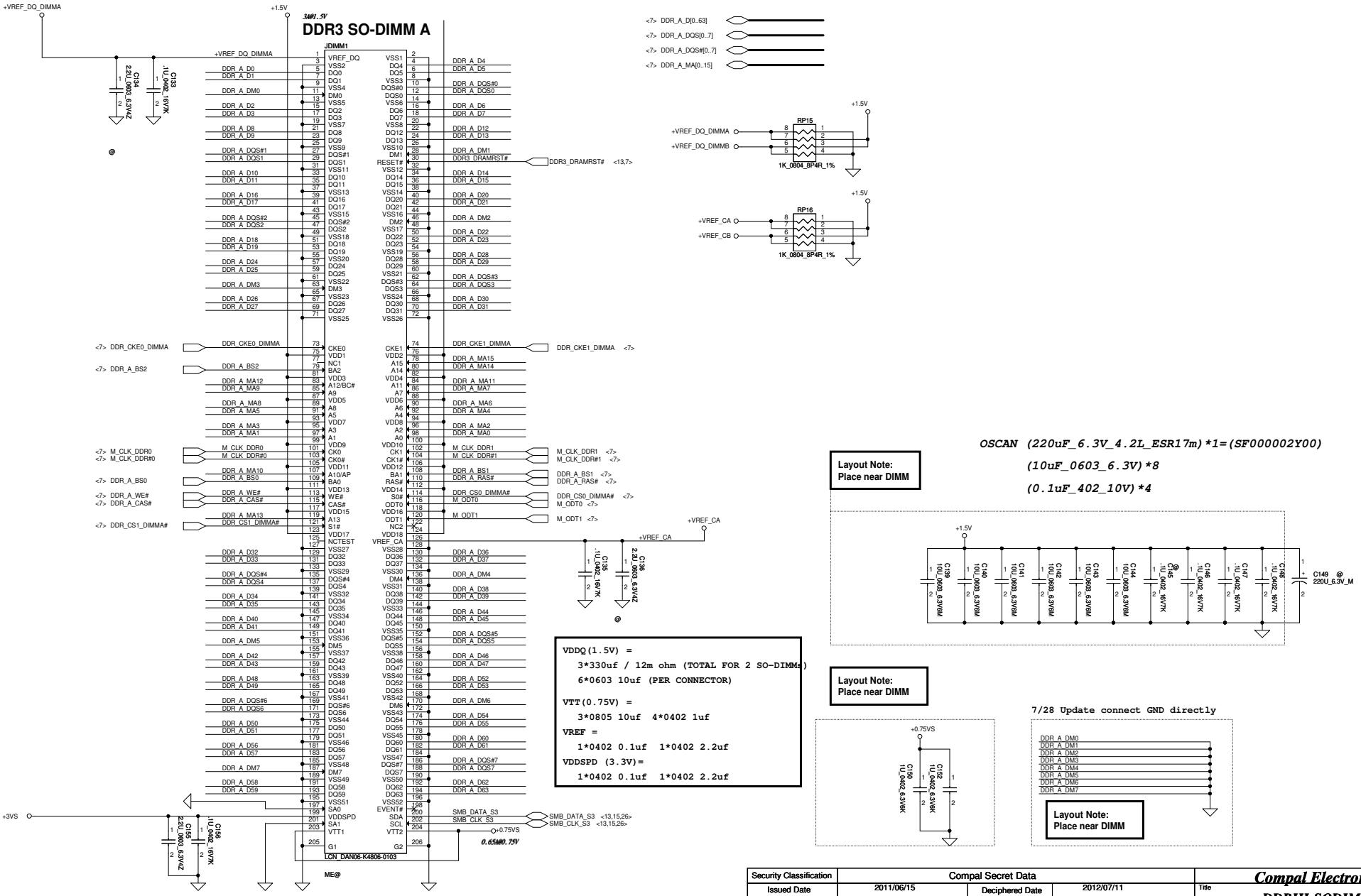
DDR3 SO-DIMM A

JDIMM1




```
VDDQ(1.5V) =
  3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
  6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
  3*0805 10uf  4*0402 1uf
VREF =
  1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
  1*0402 0.1uf  1*0402 2.2uf
```

Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

7/28 Update connect GND directly

Layout Note:
Place near DIMM

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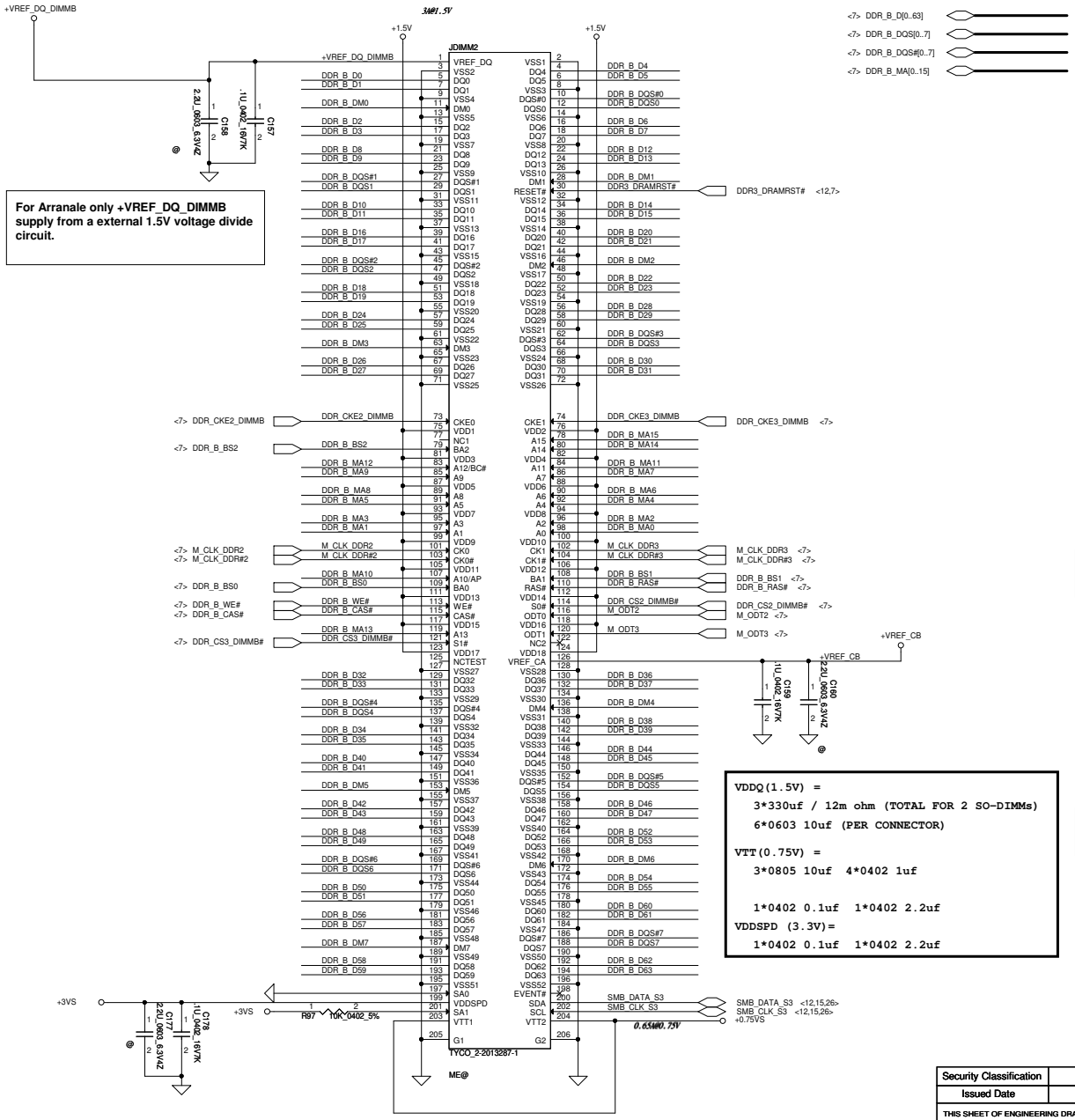
Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: LA-9632P | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 12 of 60



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

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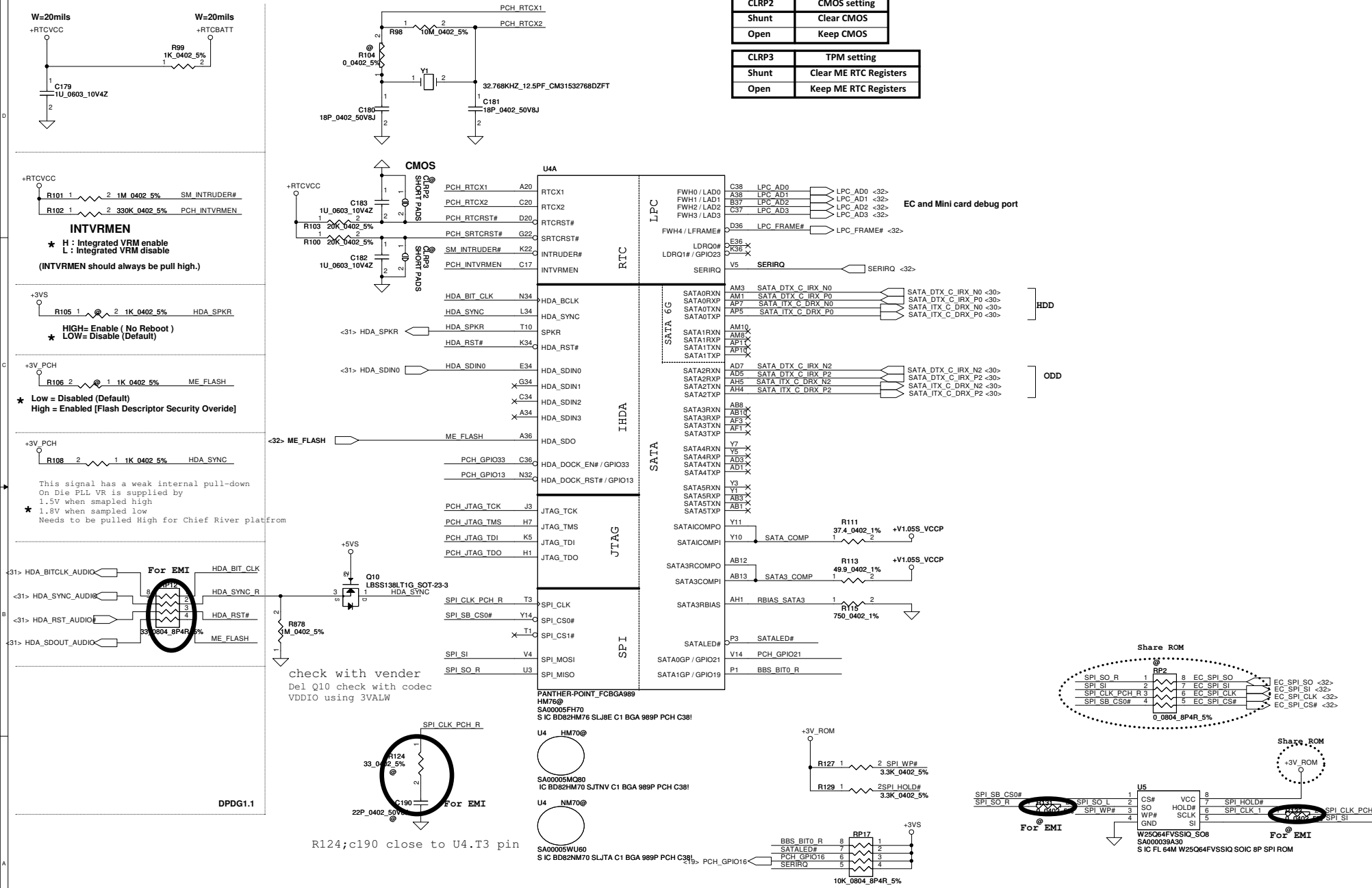
CLRP2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

CLRP3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



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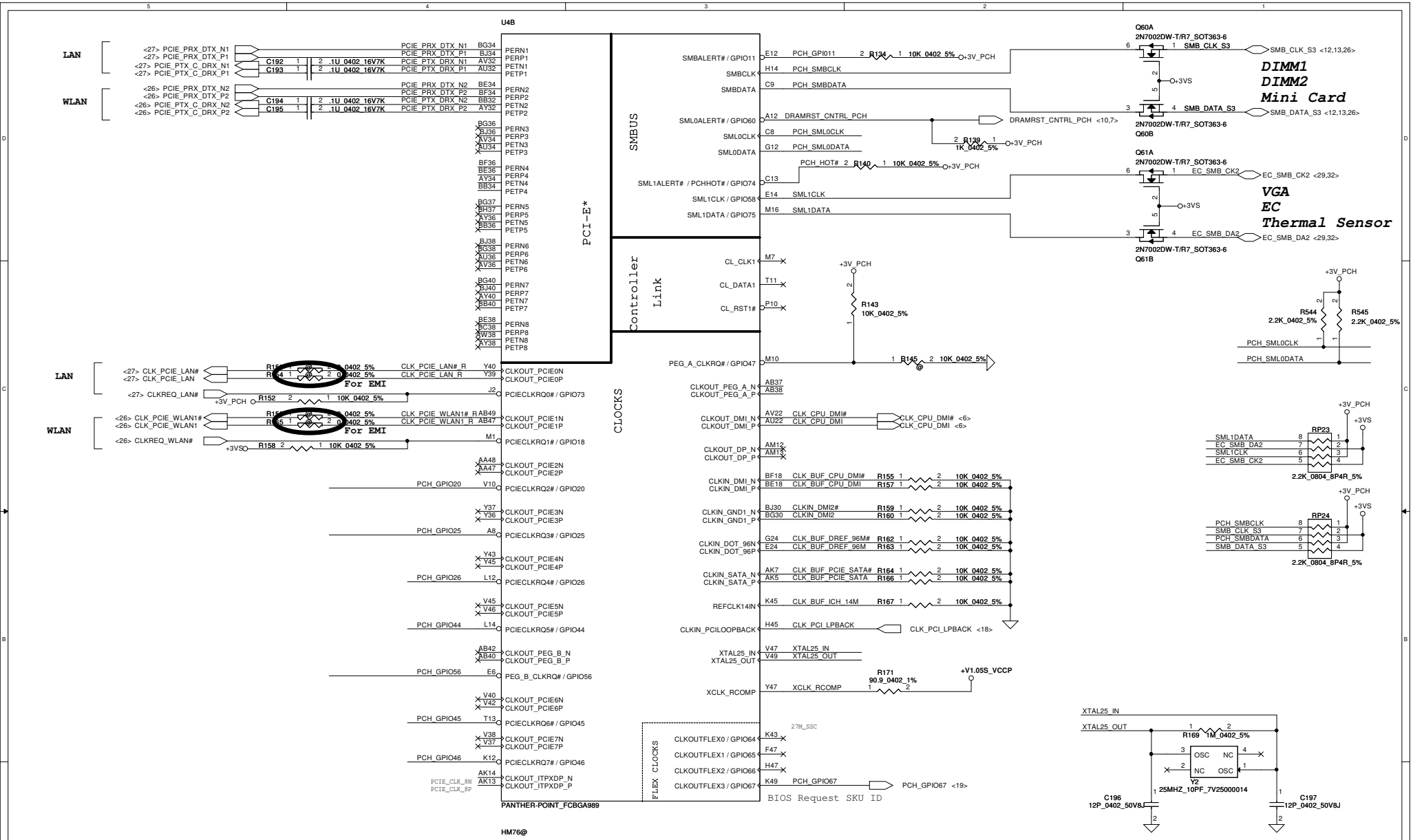
Compal Electronics, Inc.

Title: **PCH (1/9) SATA,HDA,SPI, LPC, XDP**

Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 14 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

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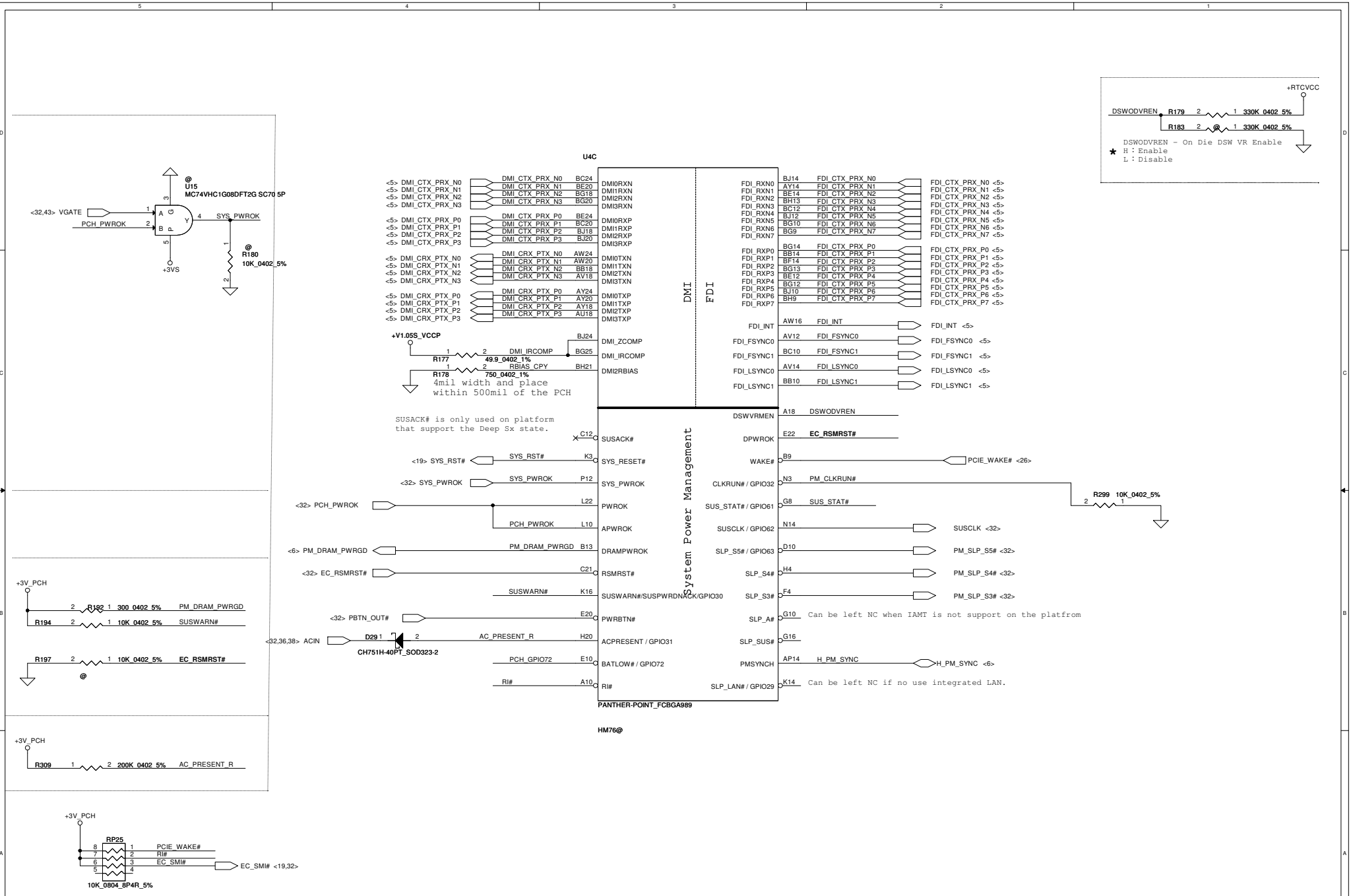
Date: Wednesday, February 27, 2013 | Sheet 15 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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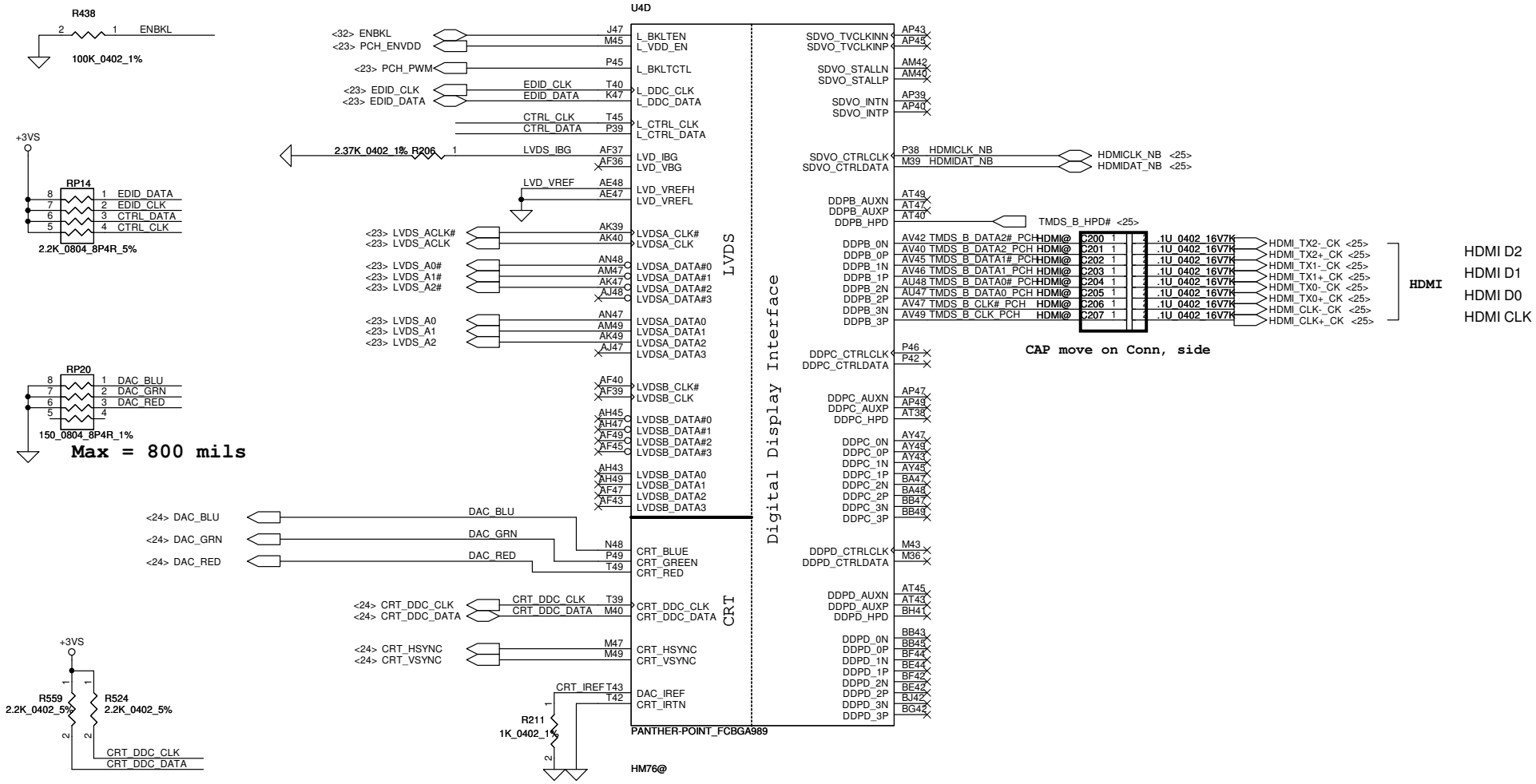
Compal Electronics, Inc.

Title: **PCH (3/9) DMI,FDI,PM,**

Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 16 of 60



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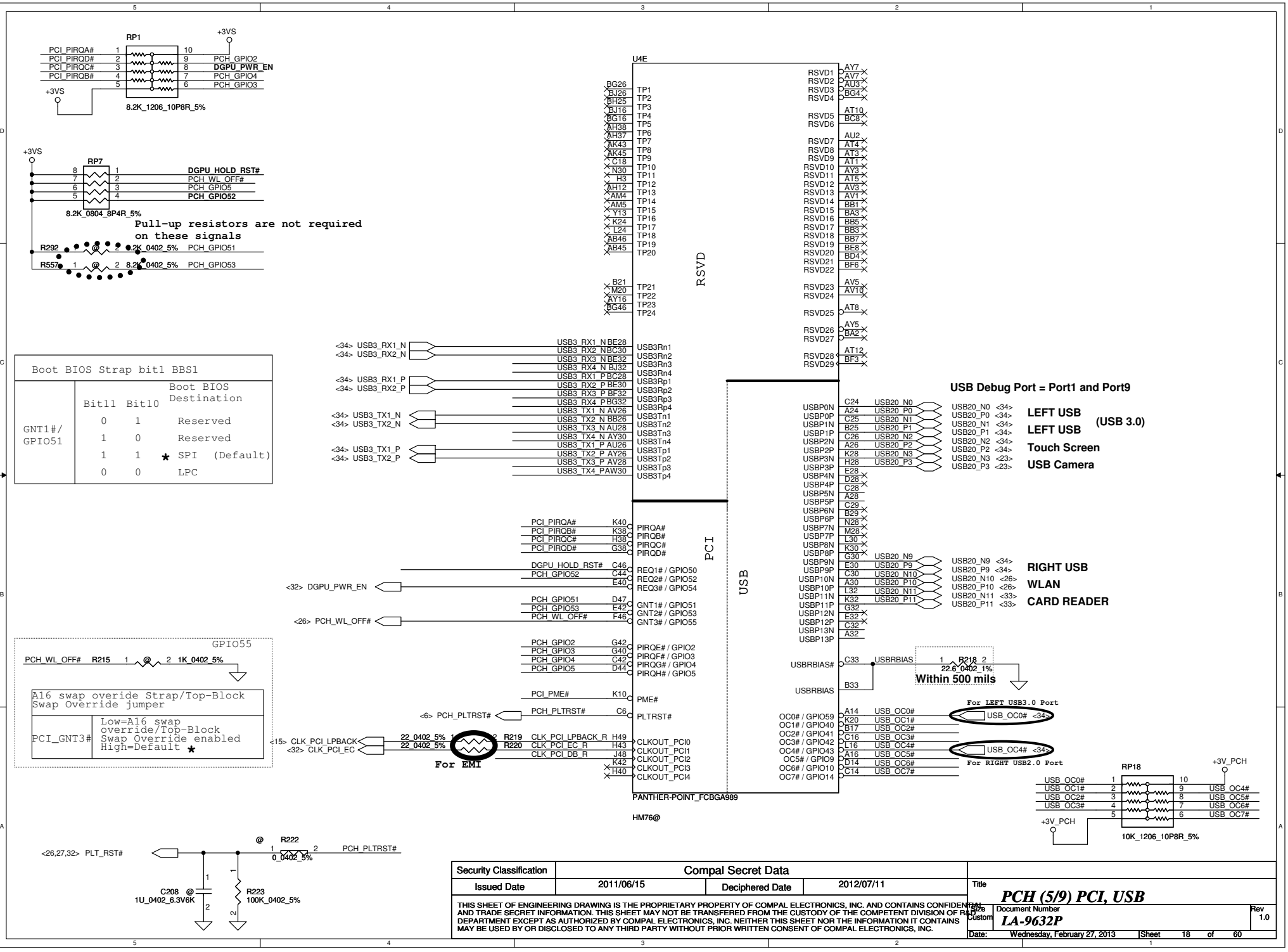
Title: **PCH (4/9) LVDS,CRT,DP,HDMI**

Size: B | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 17 of 60



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Title: **PCH (5/9) PCI, USB**

Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

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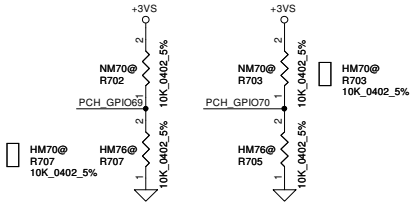
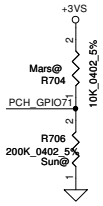
PCH_GPIO69	PCH_GPIO70	Function
1	1	NM70
1	0	Reserved
0	1	HM70
0	0	HM76



PCH_GPIO71	Function
1	Mars XT
0	Sun Pro



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

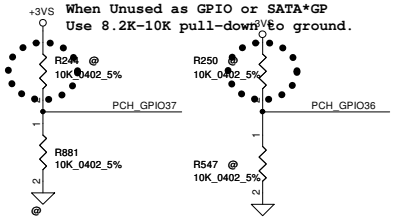
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 1 @ 2 1K_0402_5% PCH_GPIO28

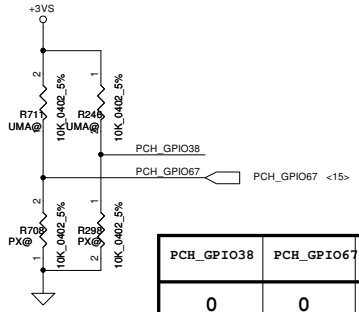
* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

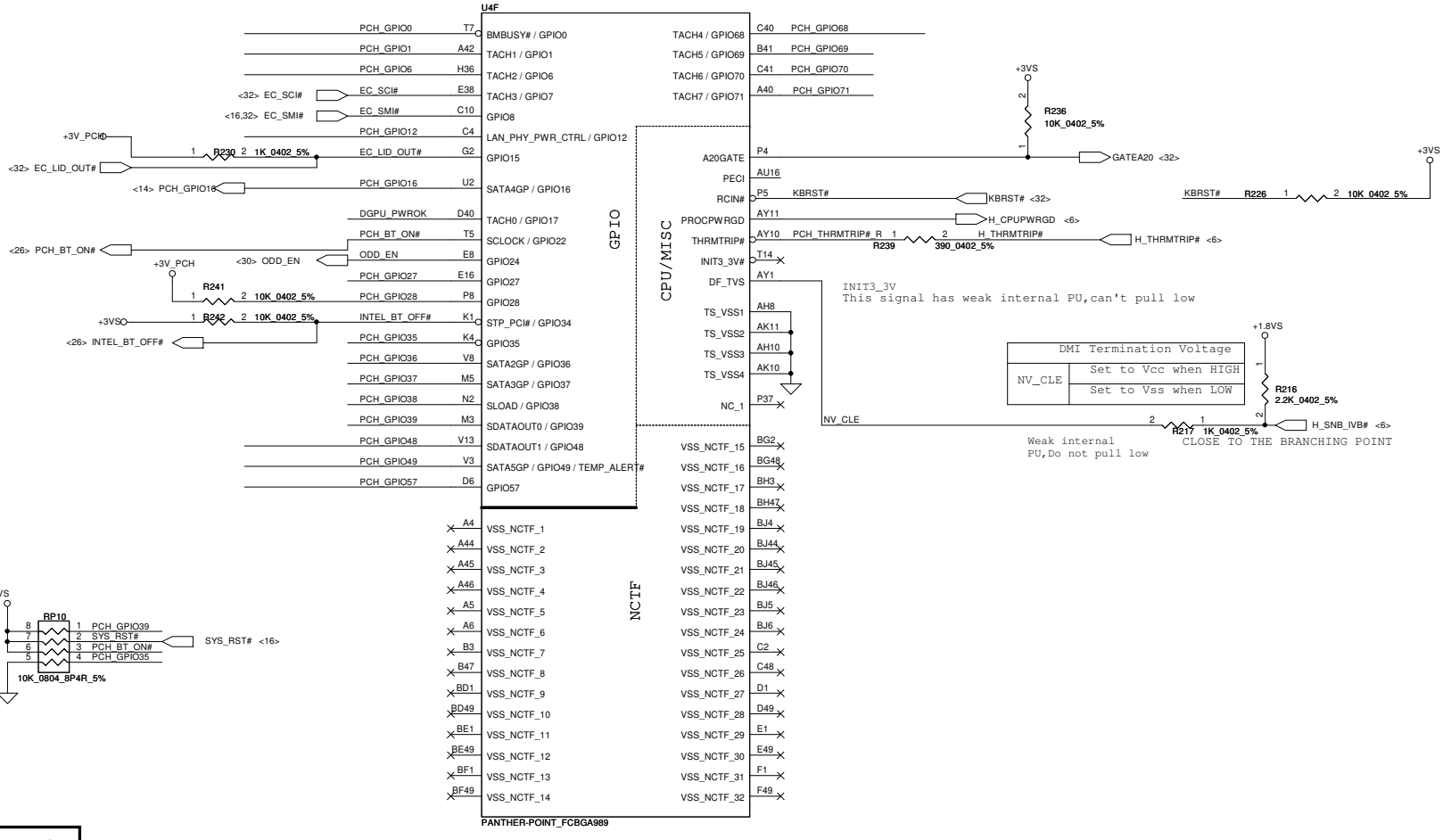
GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.



BIOS Request SKU ID



PCH_GPIO38	PCH_GPIO67	Function
0	0	SG(Optimus / PX)
0	1	Reserved
1	0	DIS
1	1	UMA



DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

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Title: **PCH (6/9) GPIO, CPU, MISC**

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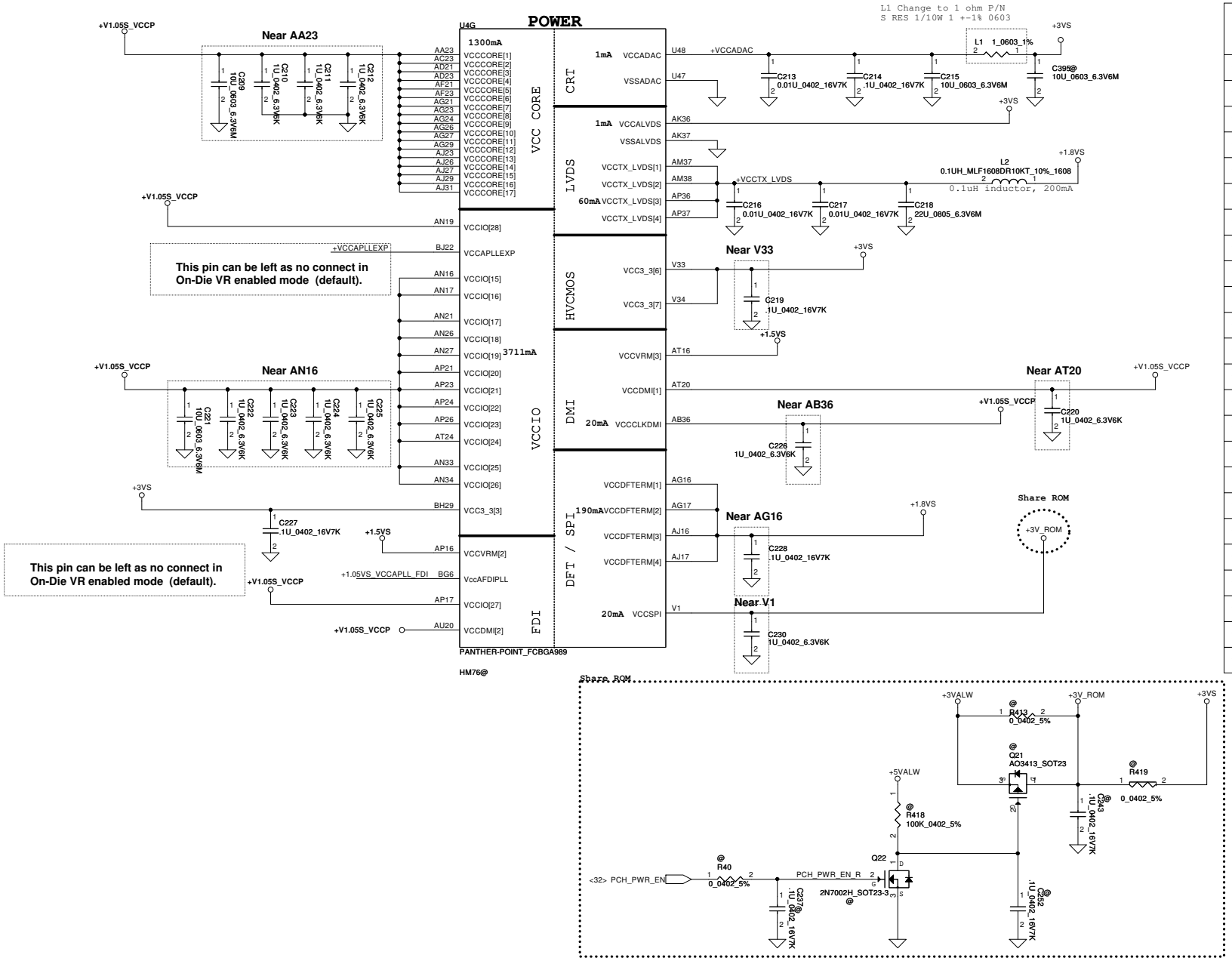

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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Compal Electronics, Inc.

Title: PCH (7/9) PWR

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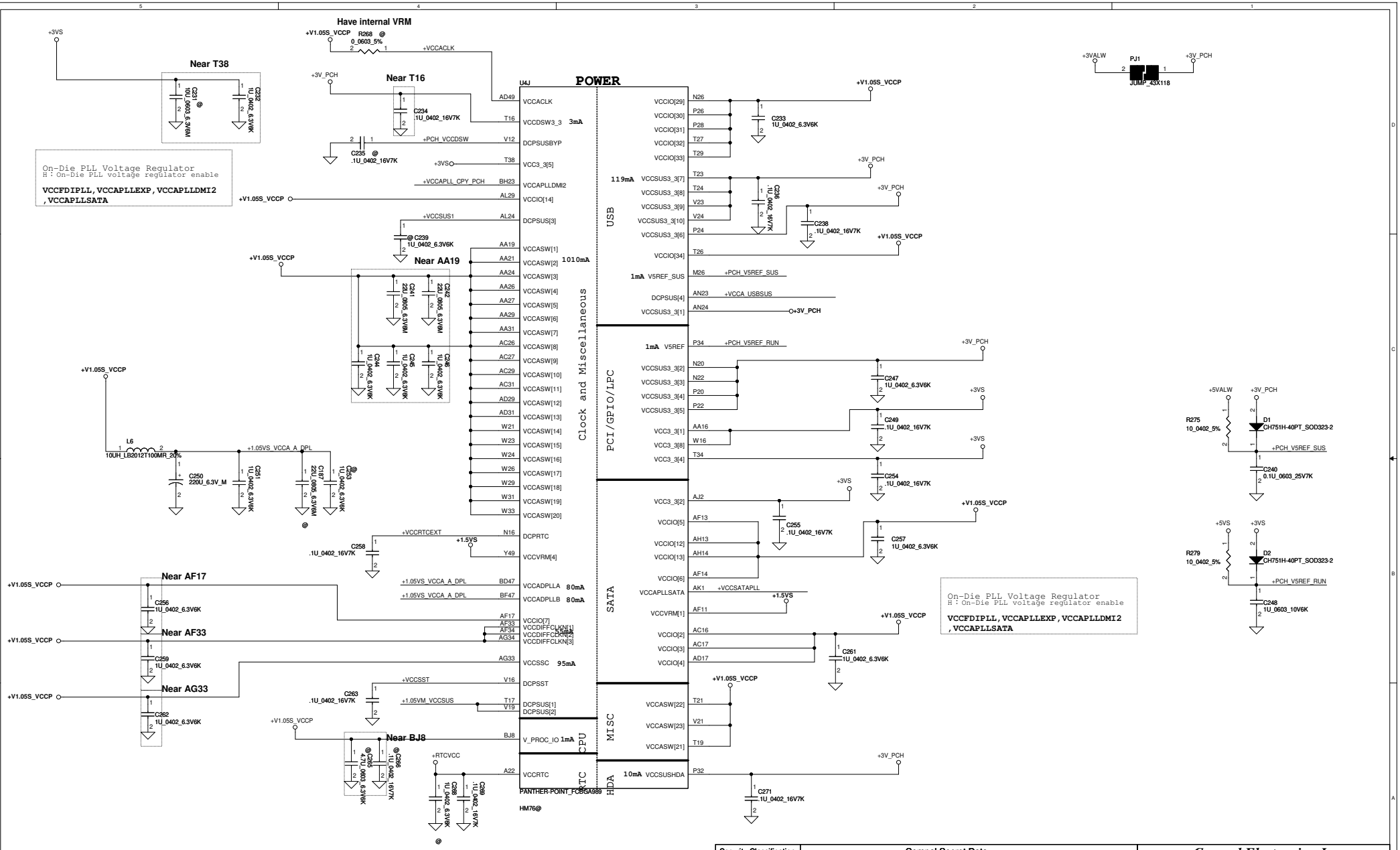
Date: Wednesday, February 27, 2013 | Sheet 20 of 60



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Title: **Compal Electronics, Inc.**
PCH (8/9) PWR

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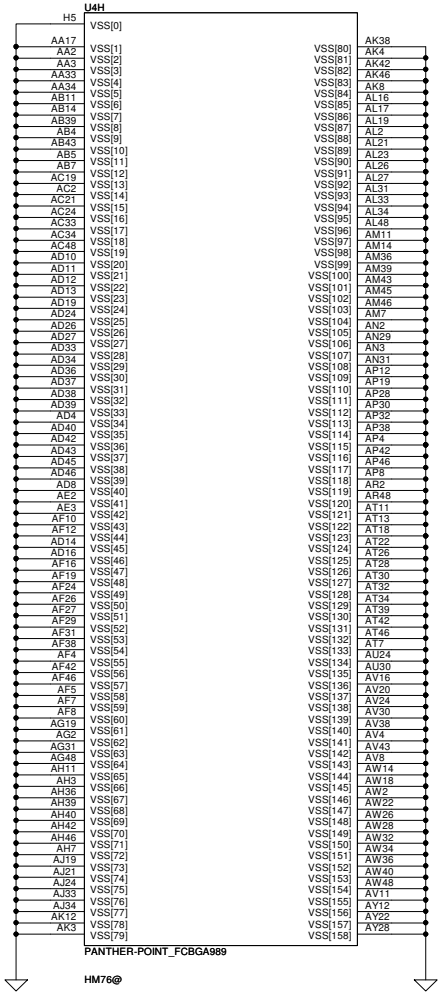
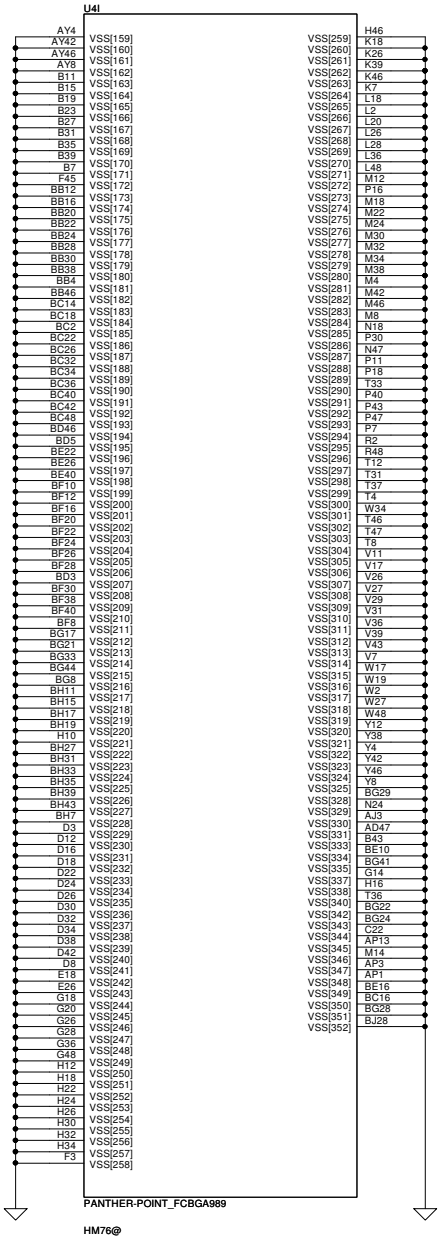
Date: Wednesday, February 27, 2013 | Sheet 21 of 60





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Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

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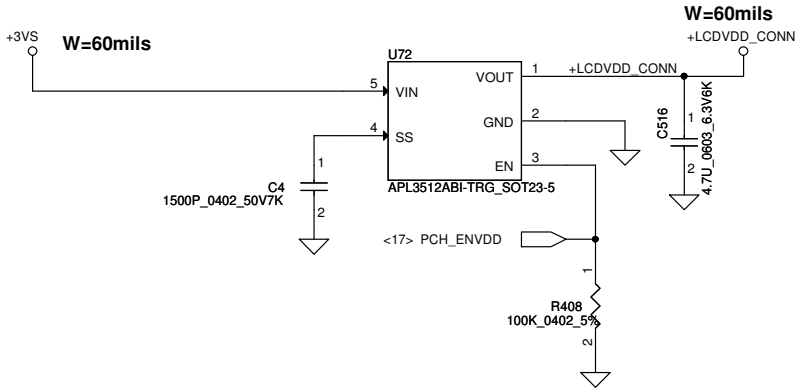
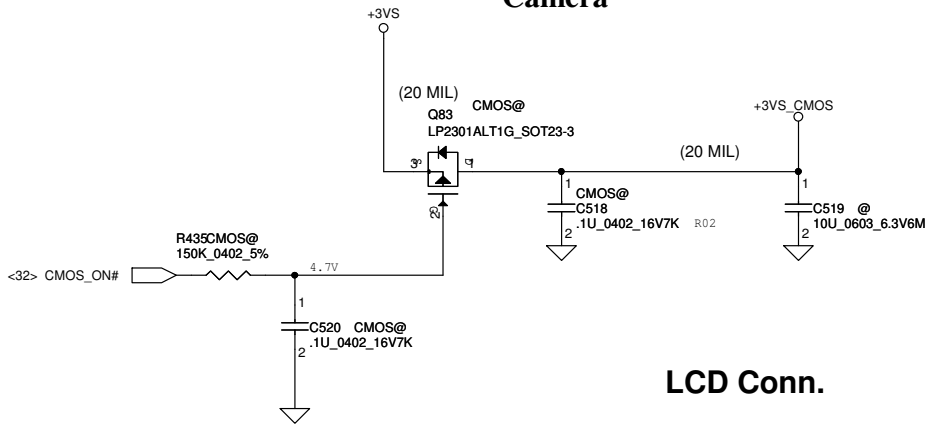
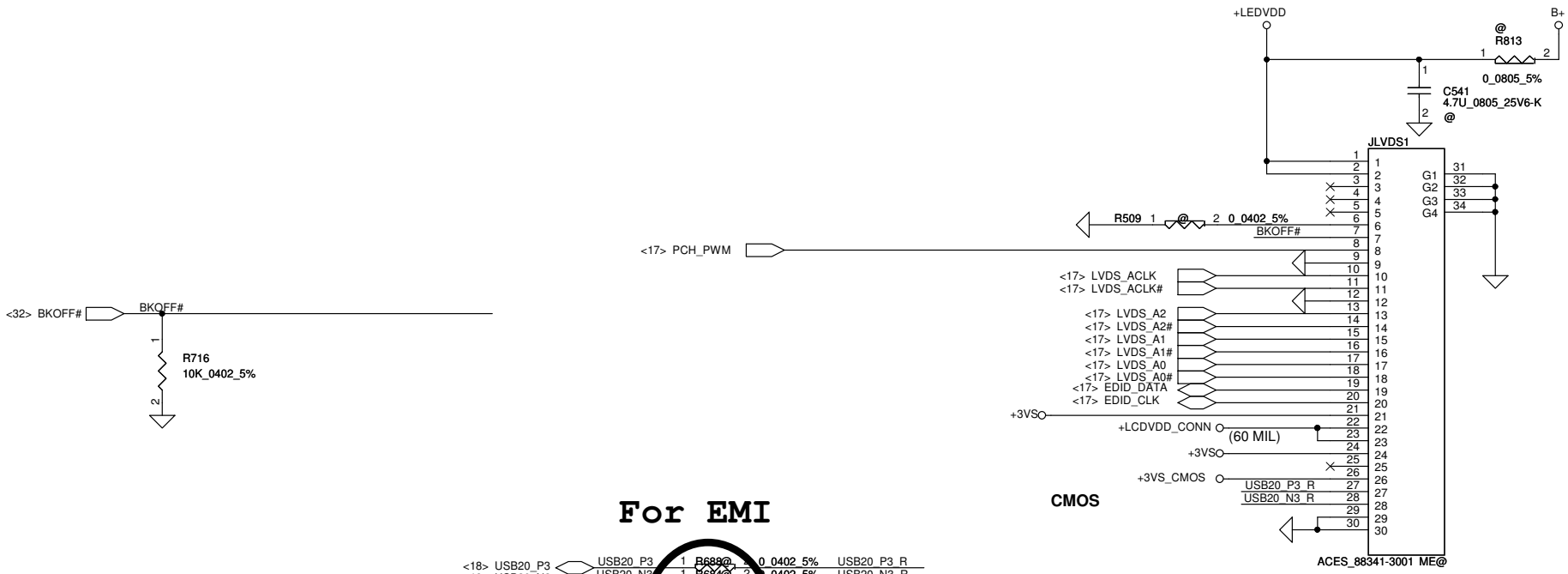
LCD POWER CIRCUIT



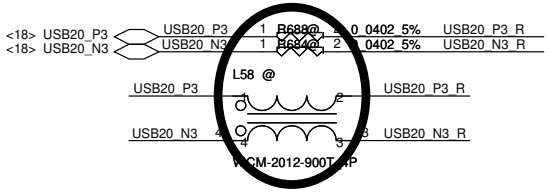
Camera



LCD Conn.



For EMI



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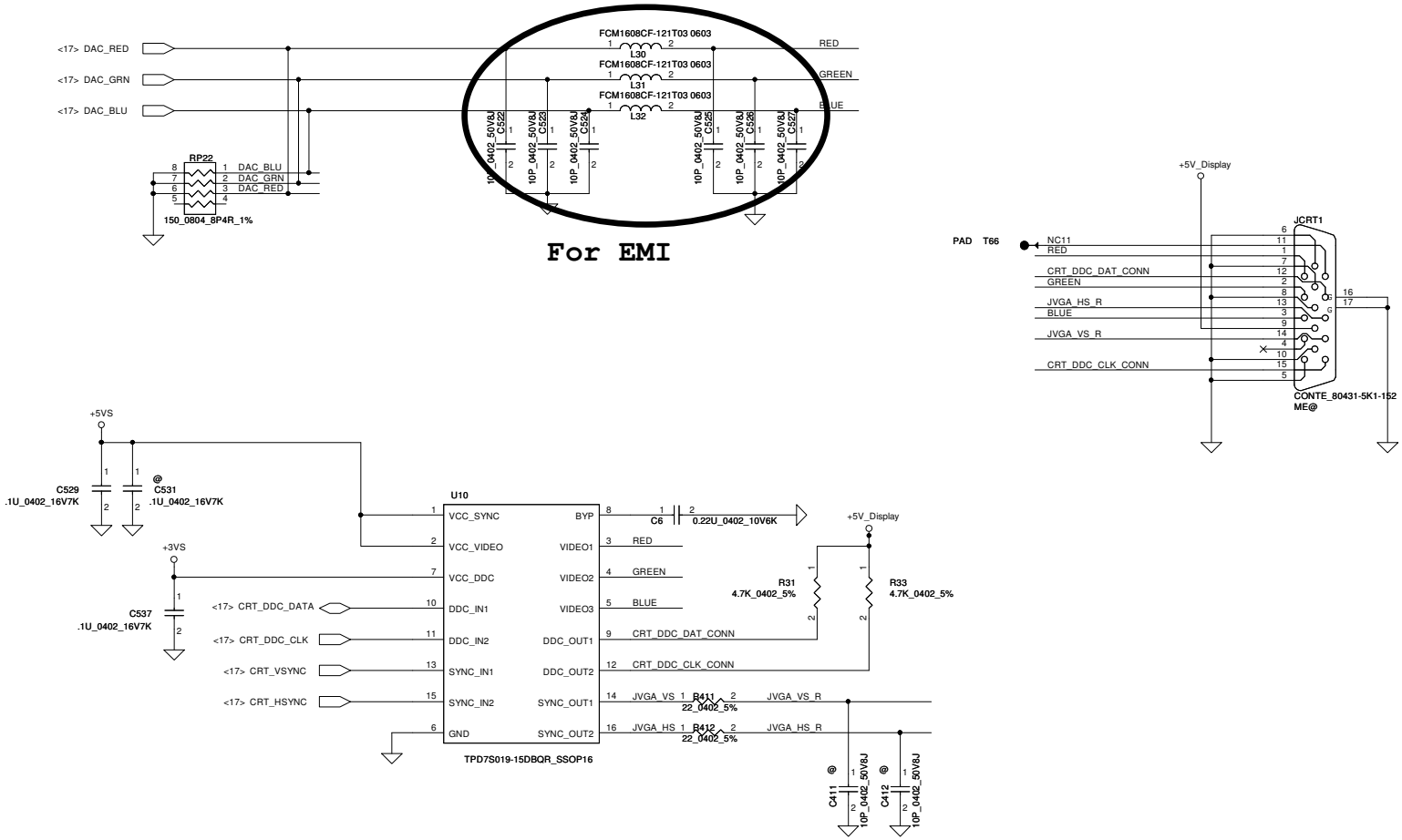
Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 23 of 60



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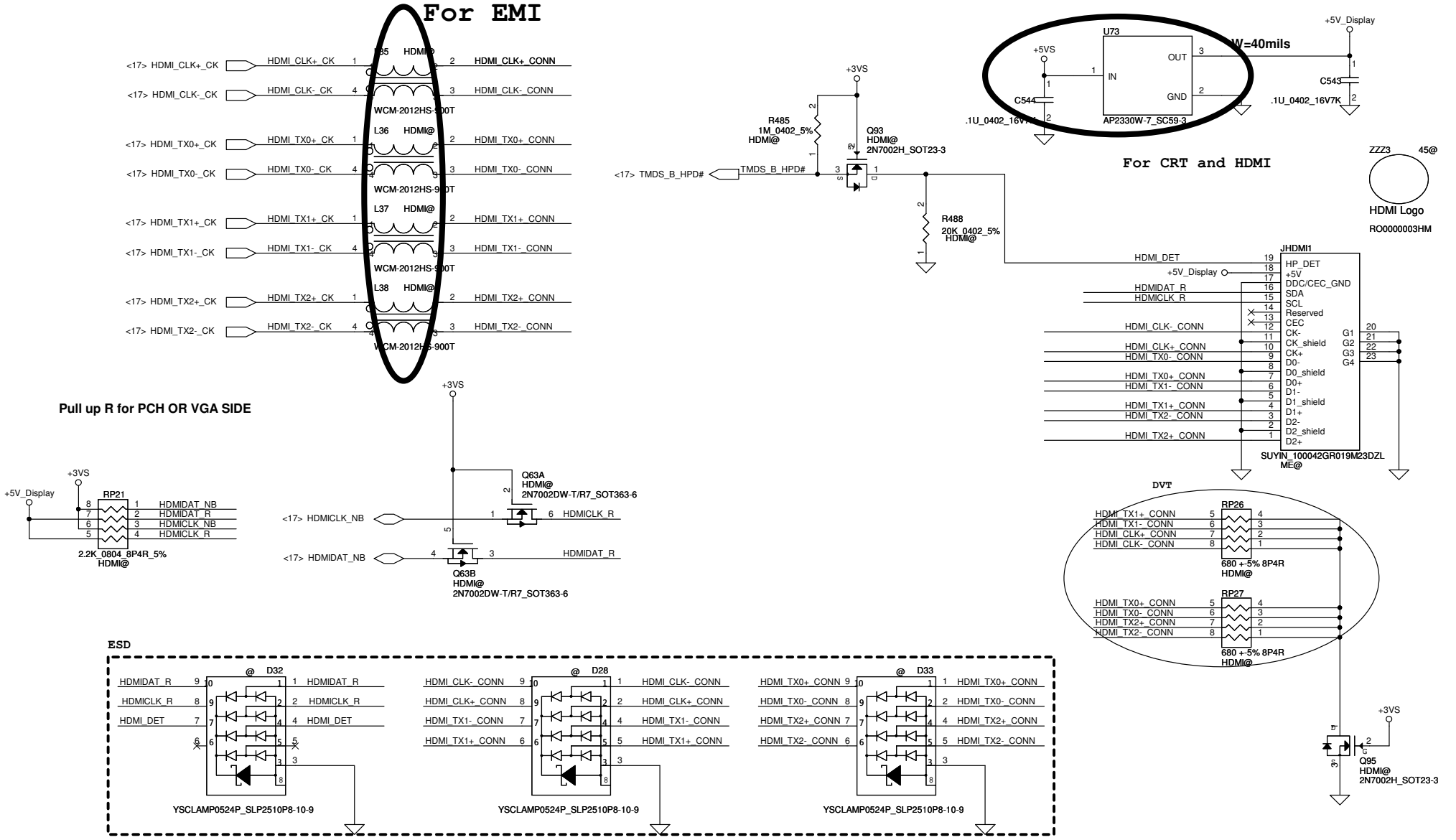
Compal Electronics, Inc.

Title: **CRT Connector**

Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 24 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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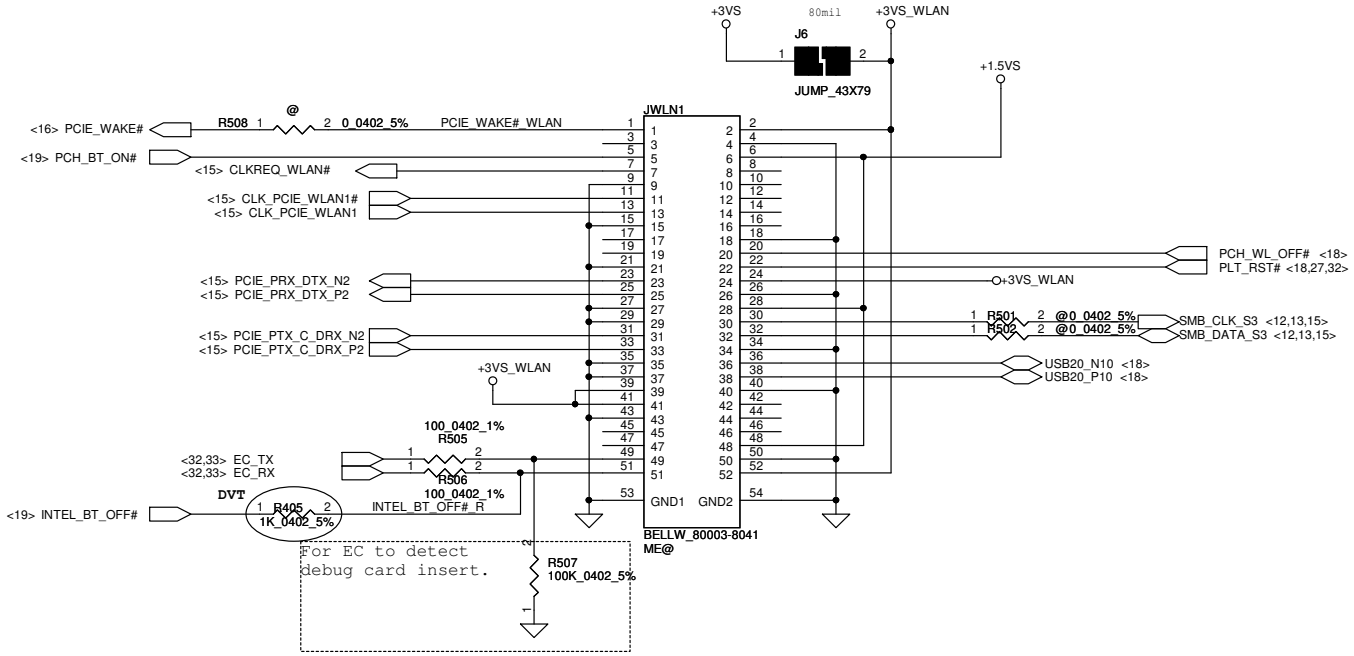
Compal Electronics, Inc.

Title: **HDMI CONN**

Size: B | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 25 of 60

Mini Card for WLAN/WiMAX(Half)



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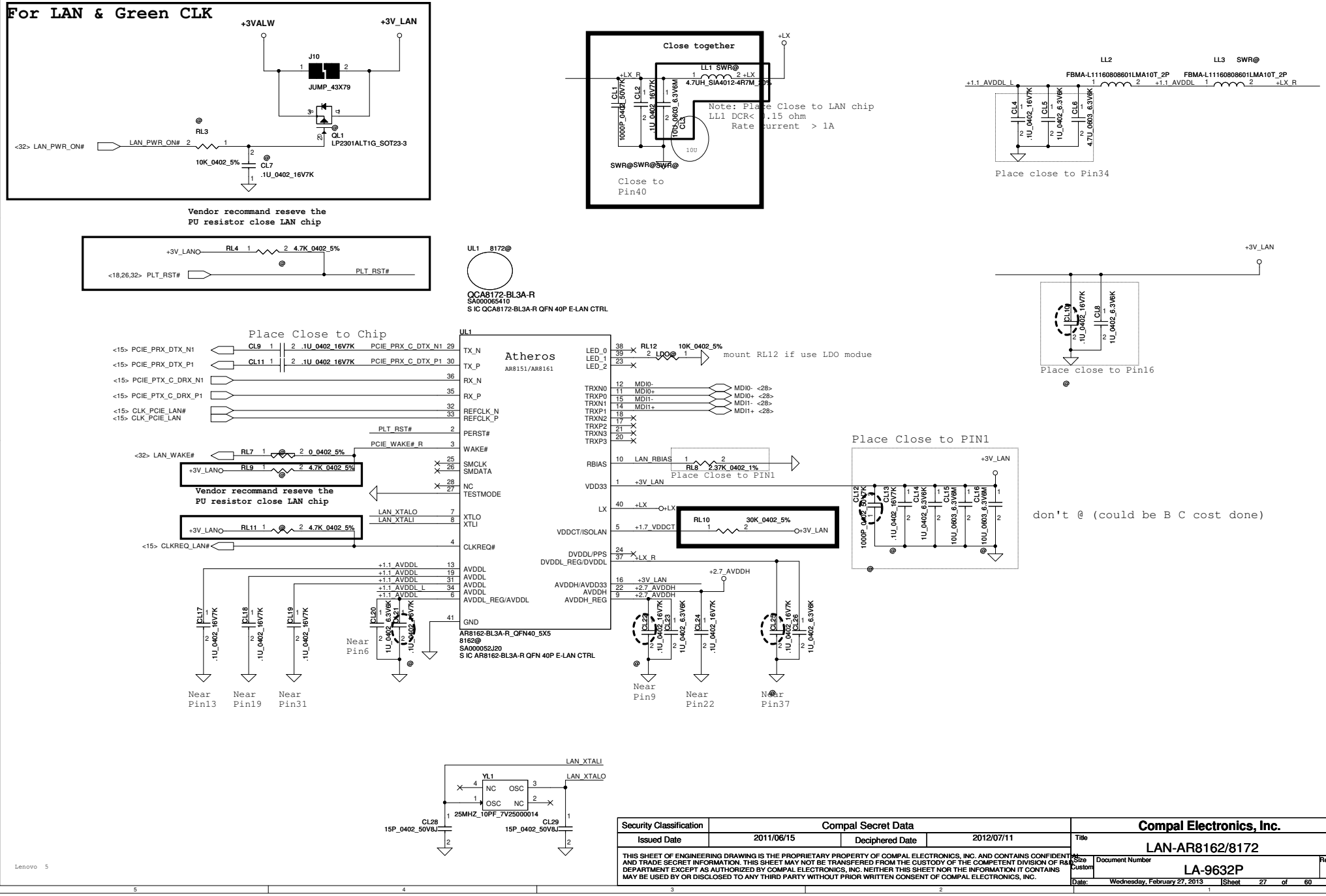
Compal Electronics, Inc.

Title: **Mini-Card/NEW Card/SIM**

Size | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 26 of 60



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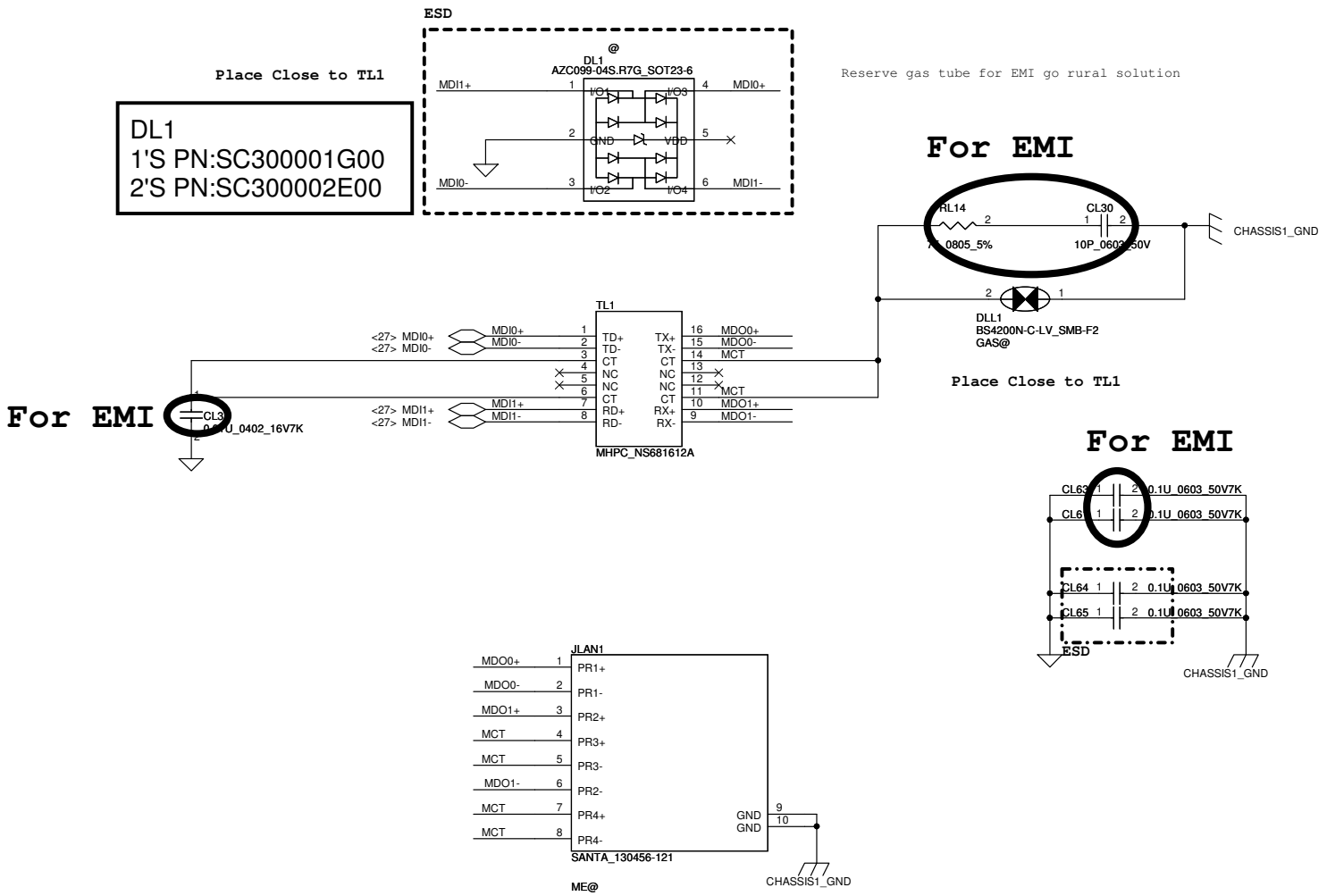
				Date: Wednesday, February 27, 2013; Sheet 27 of 60

Lenovo 5



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: LAN_Transformer
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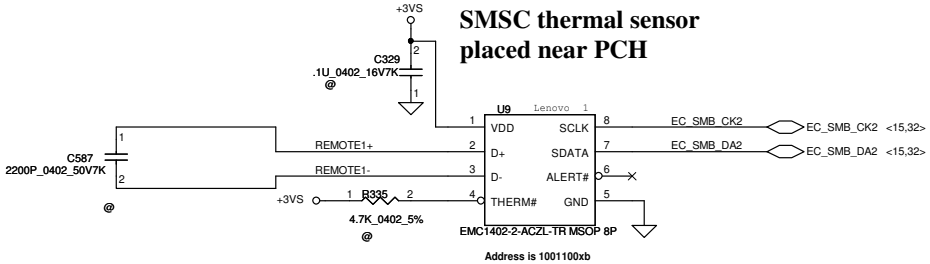
				Date: Wednesday, February 27, 2013 / Sheet 28 of 60

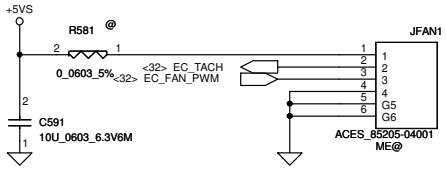
2 Channel

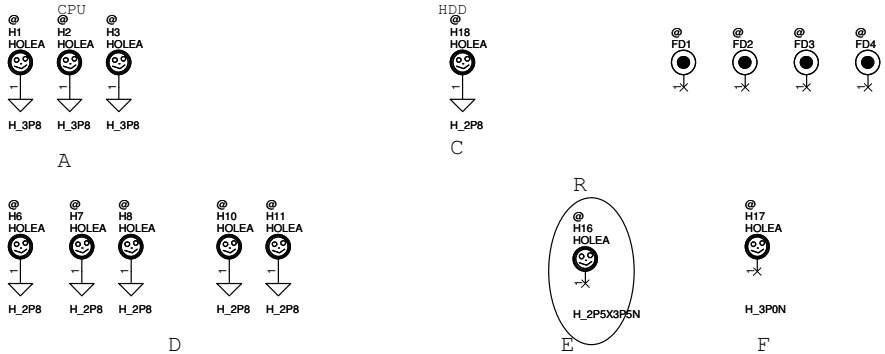
SMSC thermal sensor placed near PCH



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn





2P8 * 9 pcd

M/B 橢圓孔

M/B 圓孔

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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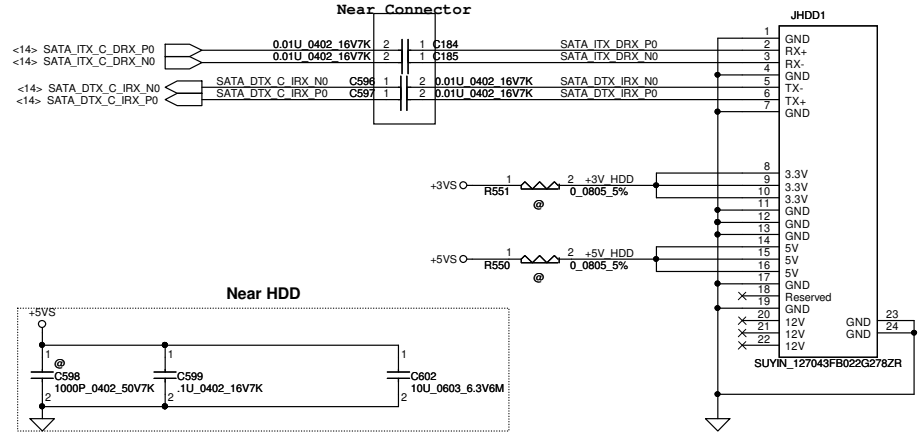
Compal Electronics, Inc.

Title: **Fintek-Thermal IC/FAN/screw**

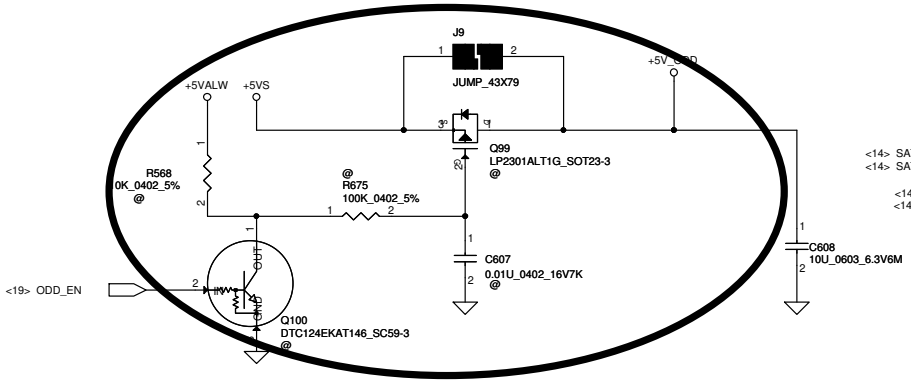
Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 29 of 60

SATA HDD Conn.

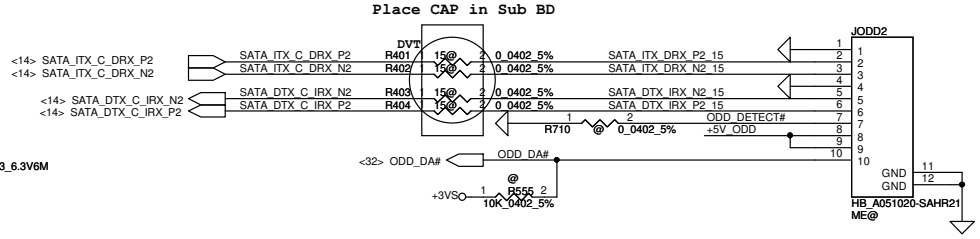


ODD Power Control



FOR 15"

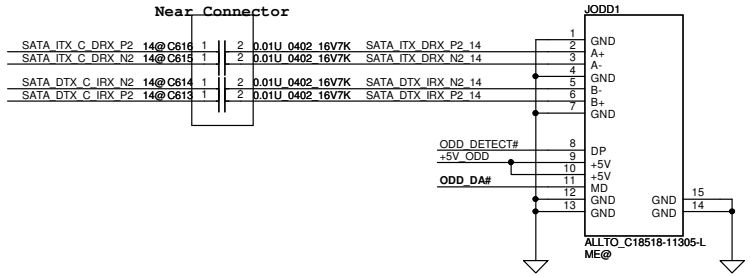
SATA ODD FFC Conn.



Co-lay

FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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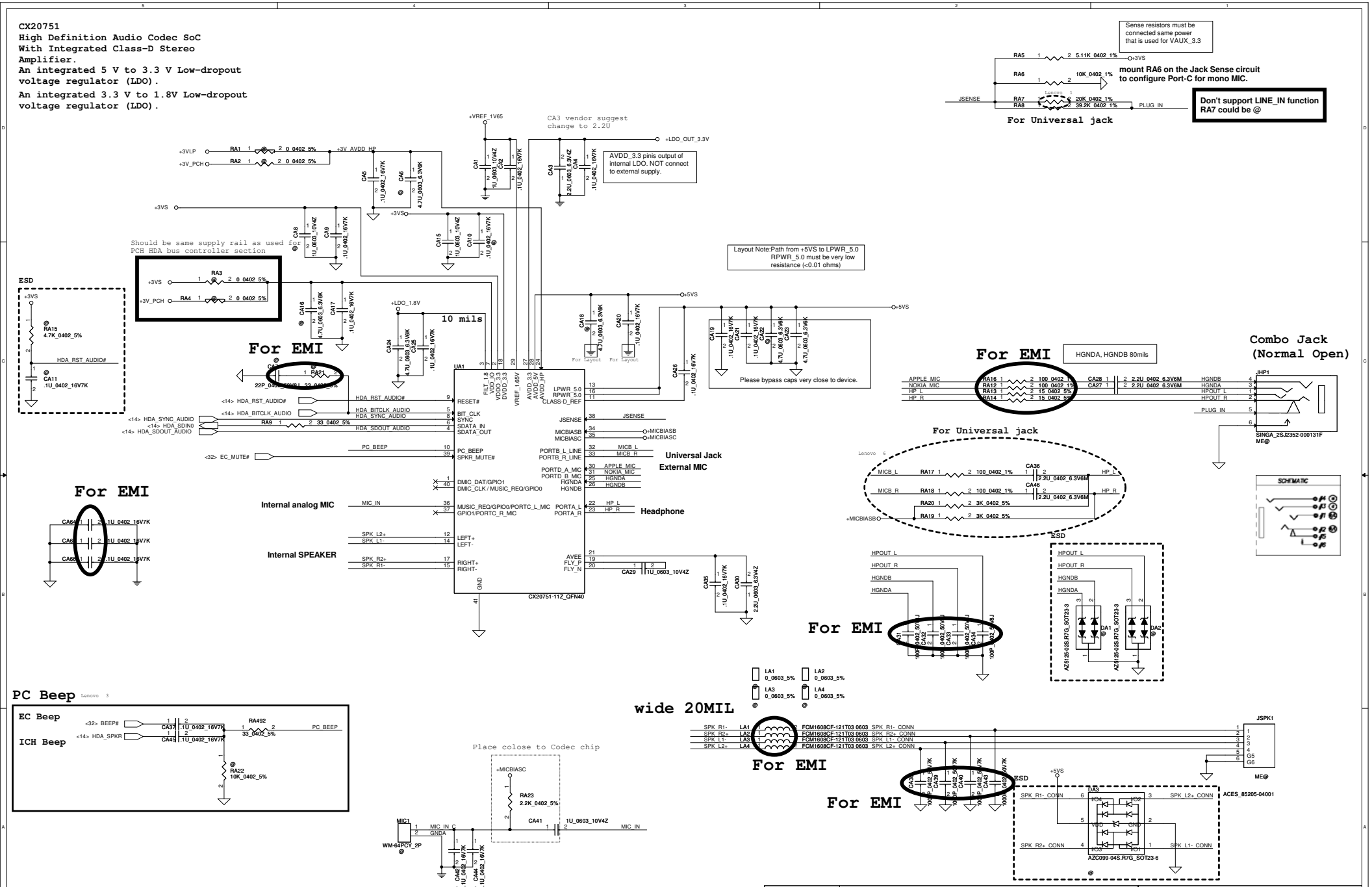
Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 30 of 60

CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: CX20751 Codec
				Size: Custom; Document Number: LA-9632P; Rev: 1.0
				Date: Tuesday, March 05, 2013; Sheet 31 of 60

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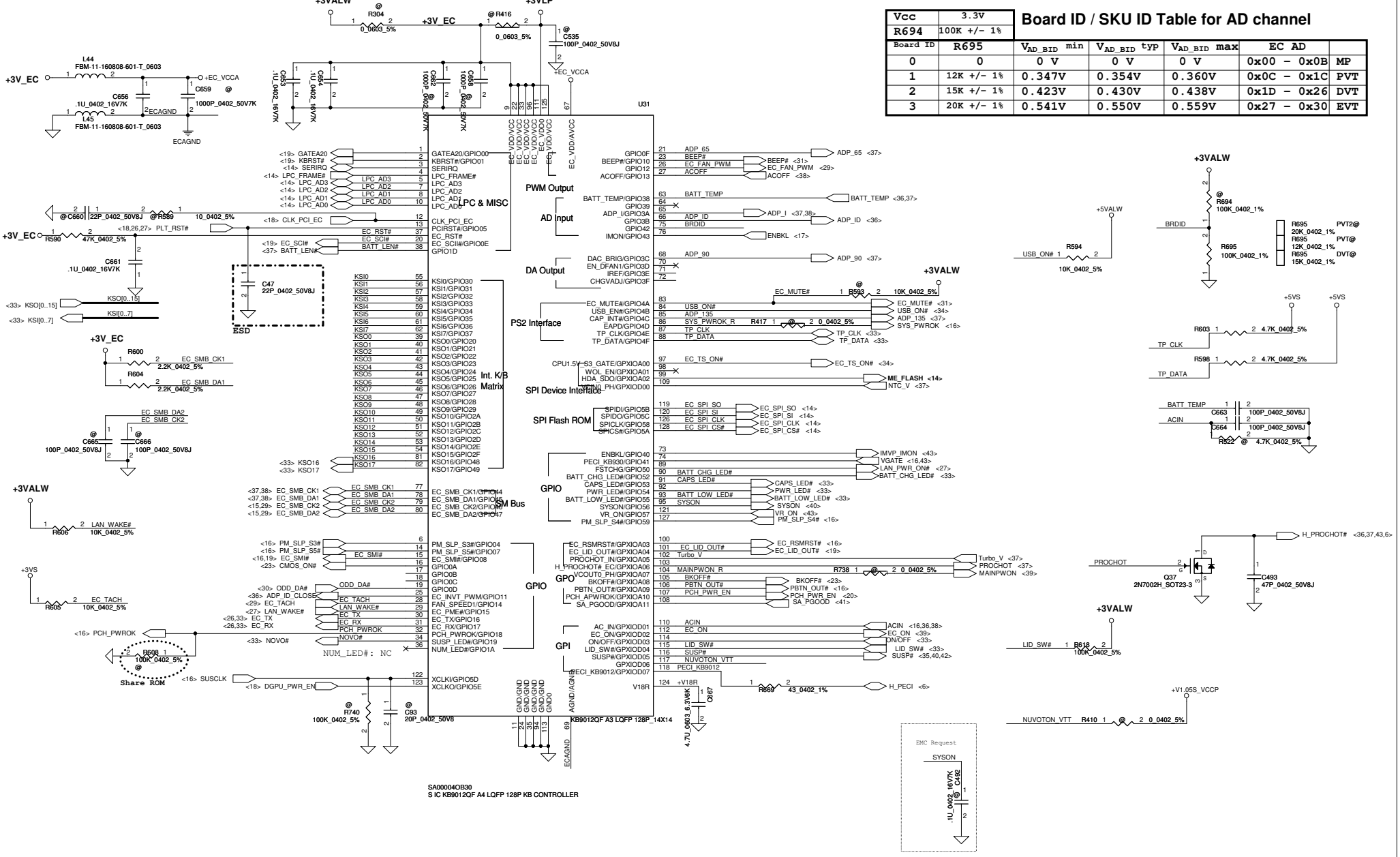
Board ID / SKU ID Table for AD channel

Vcc	3.3V					
R694	100K +/- 1%					
Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	EVT



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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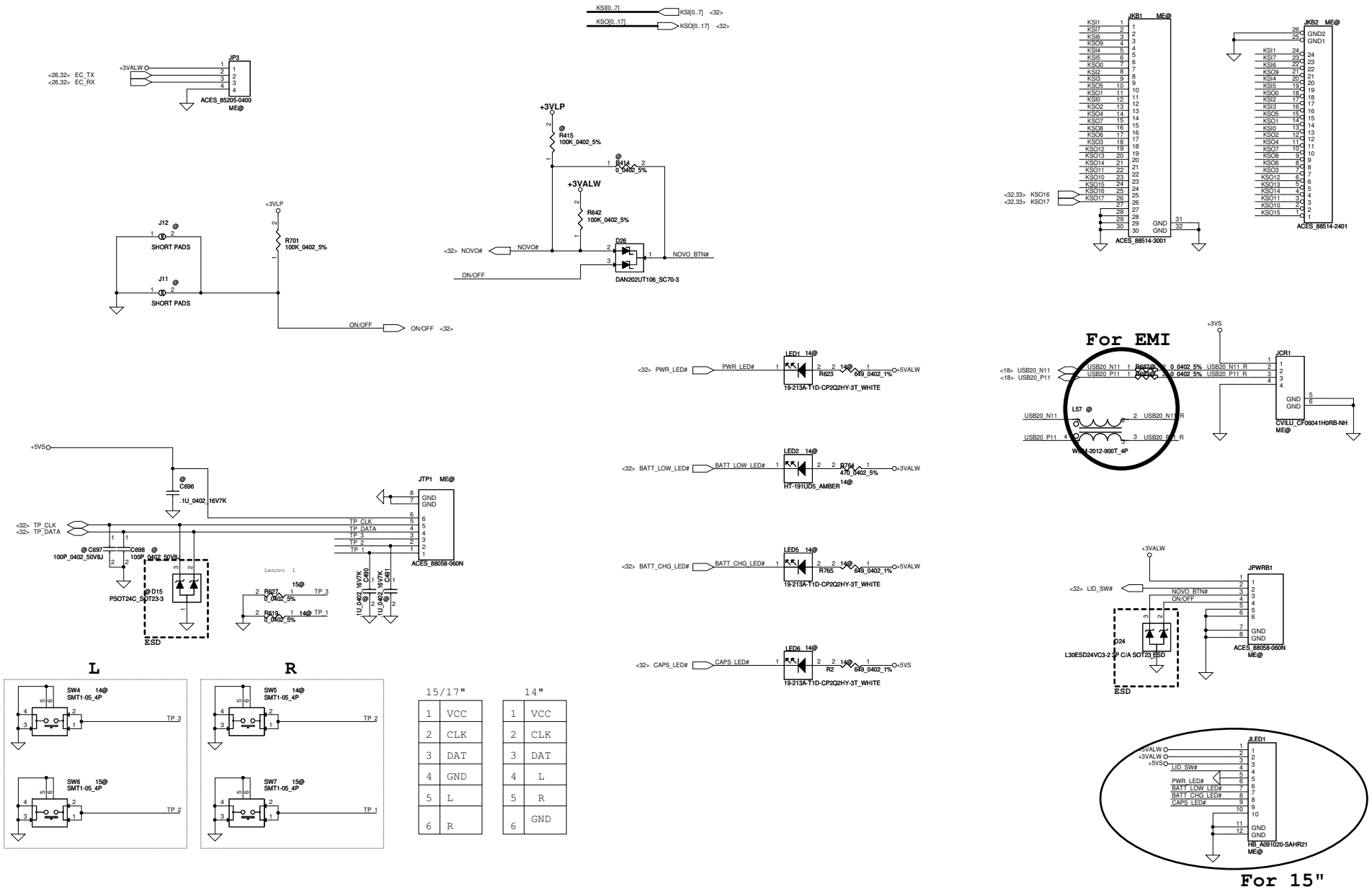
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size: Custom | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 32 of 60



15/17"	
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"	
1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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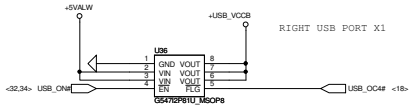
Compal Electronics, Inc.

Title: **ROM/KBD/PWR/CR/LED/TP Conn.**

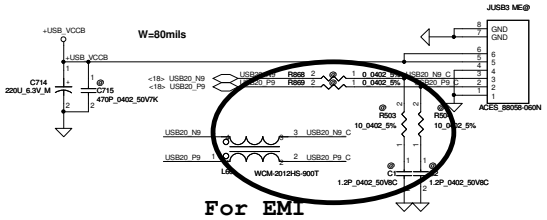
Size: C | Document Number: **LA-9632P** | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 33 of 60

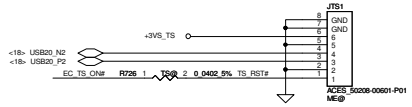
Ext. USB2.0

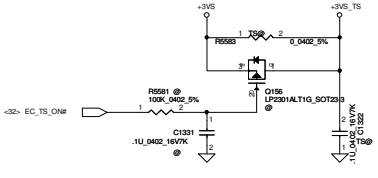


Right Ext.USB Conn.

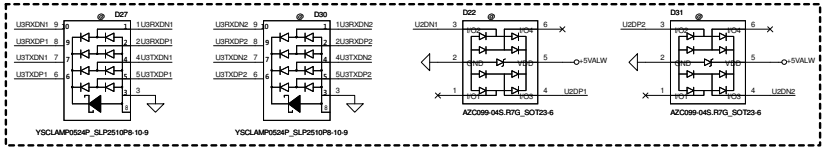


Touch Screen

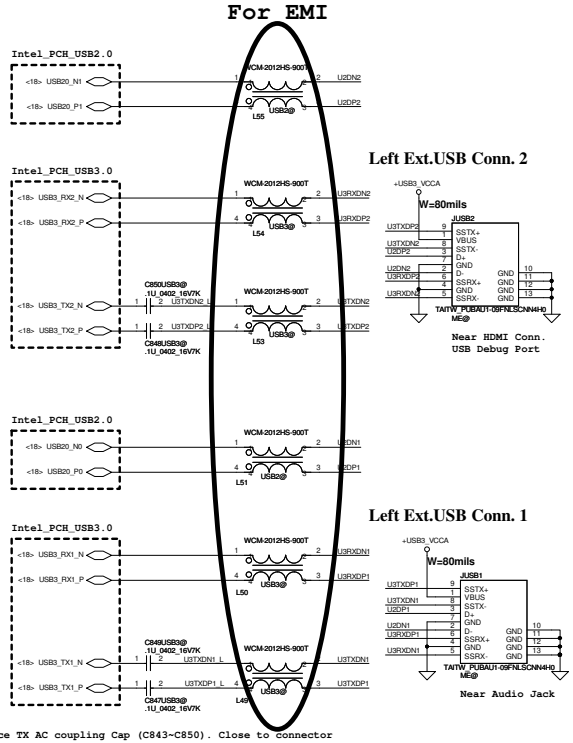


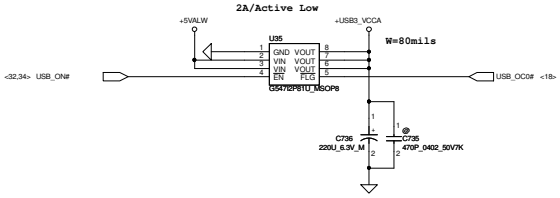


ESD



USB3.0





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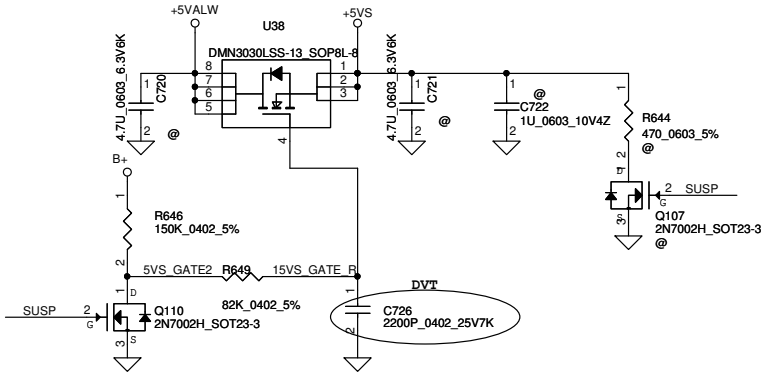
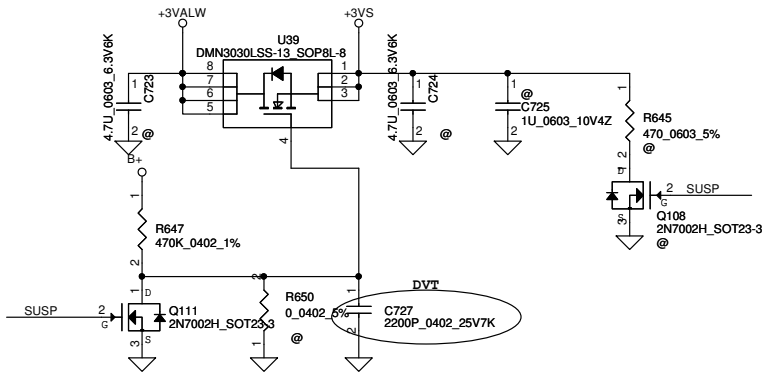
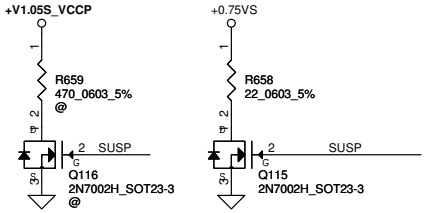
				Date: Wednesday, February 27, 2013 Sheet 34 of 60

+5VALW to +5VS

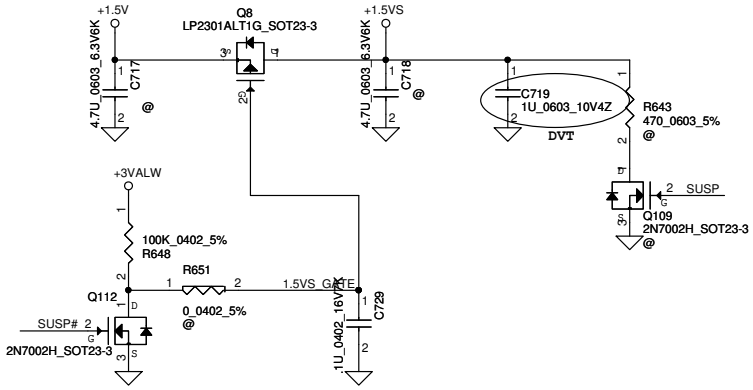


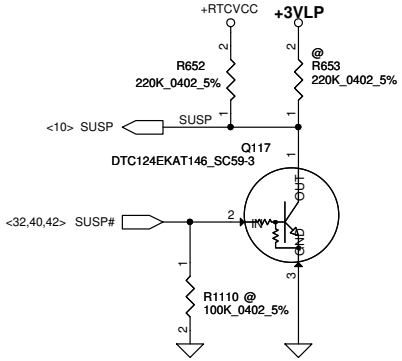
+3VALW to +3VS





+1.5V to +1.5VS





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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: DC Interface
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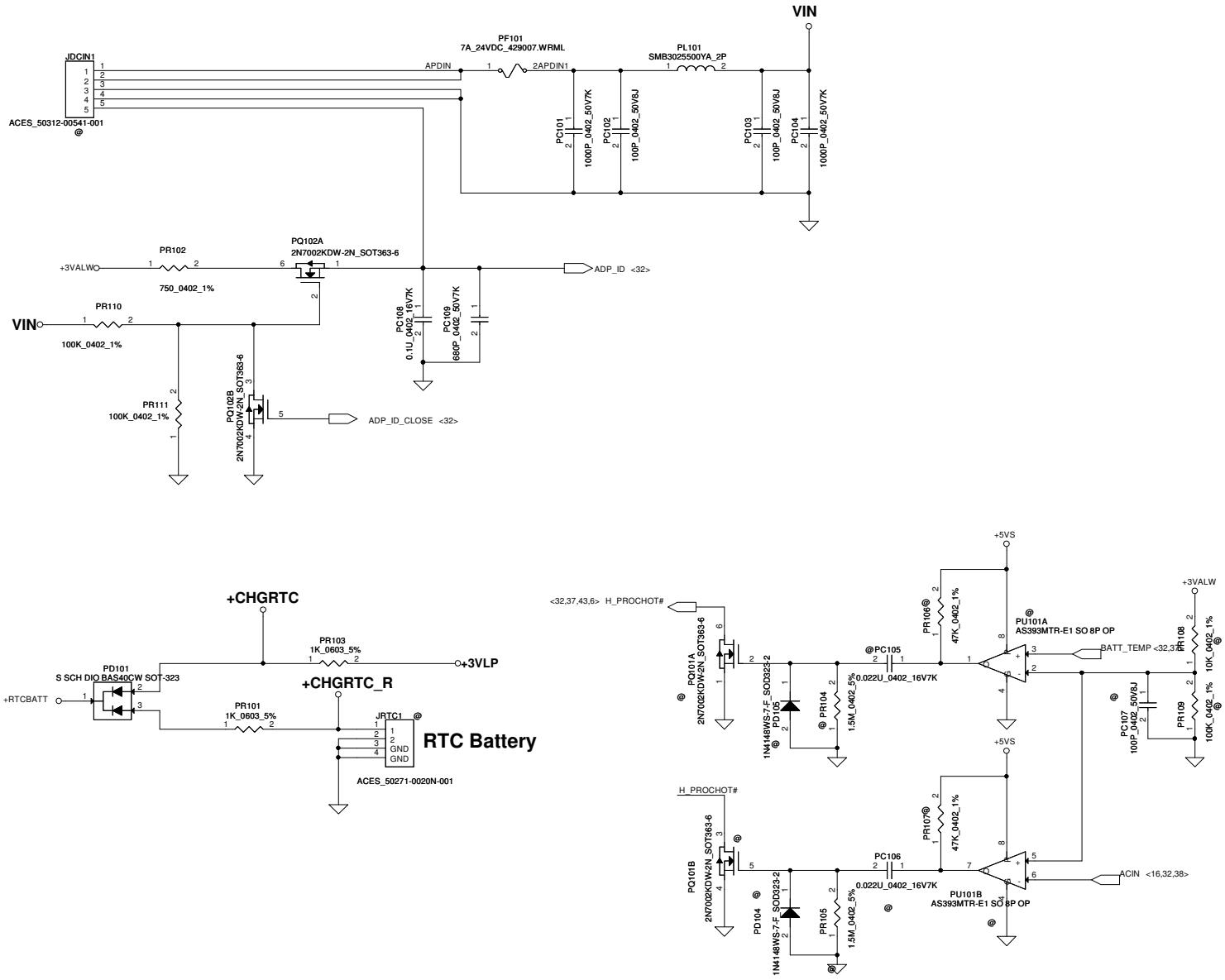
				Date: Wednesday, February 27, 2013 / Sheet 35 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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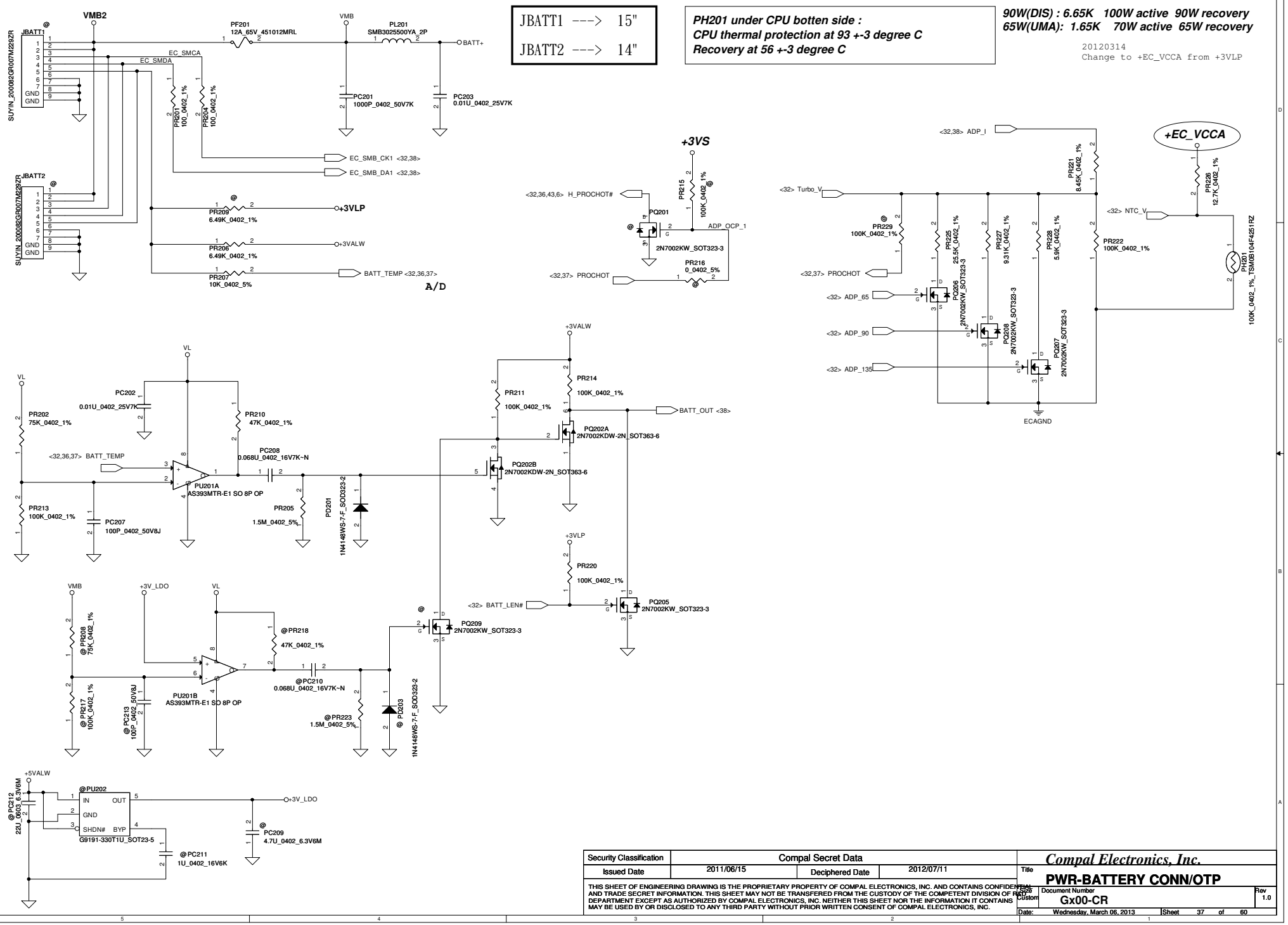
Compal Electronics, Inc.

Title: **PWR DCIN / RTC Battery**

Size: Custom | Document Number: **Gx00** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 36 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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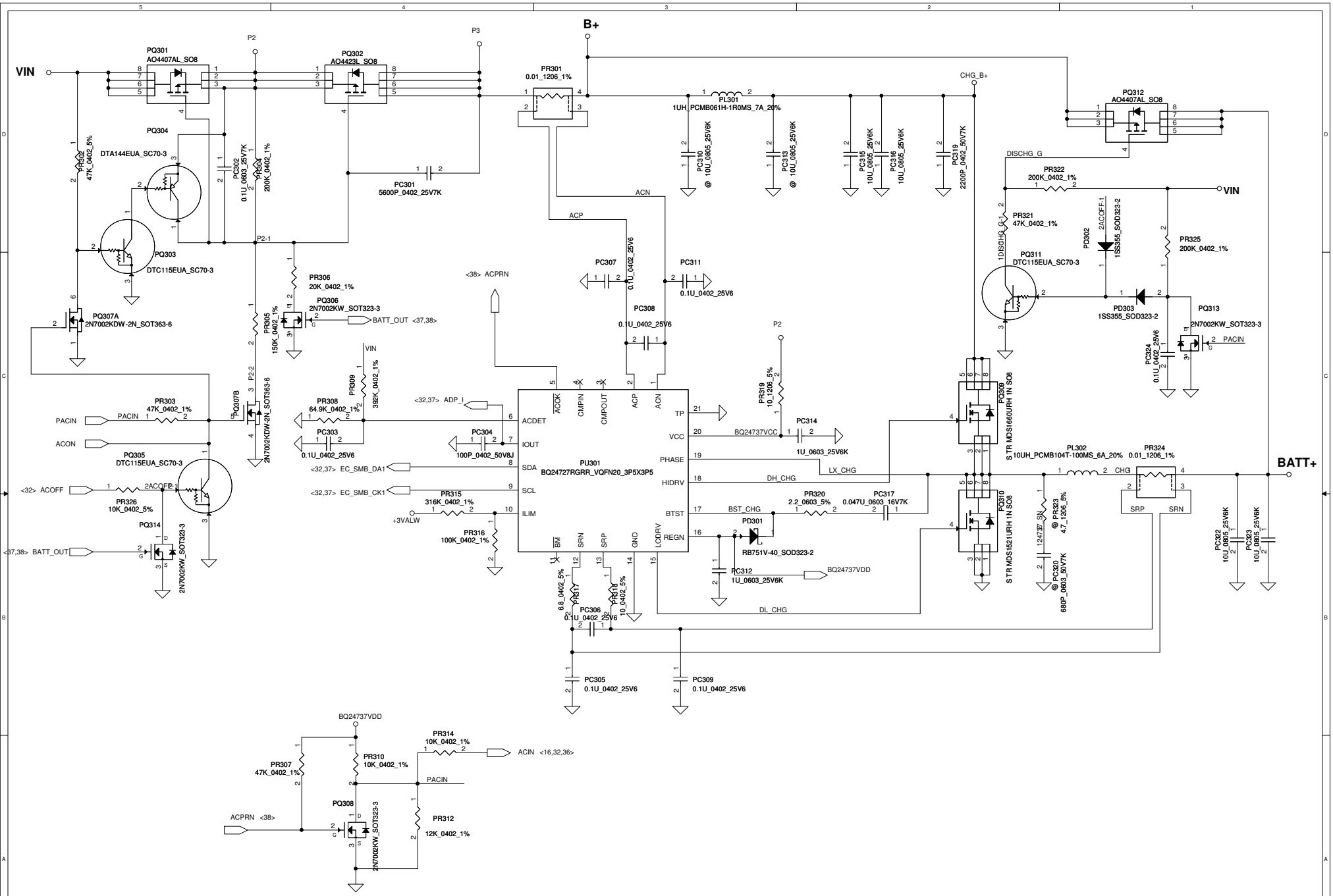
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 06, 2013 | Sheet 37 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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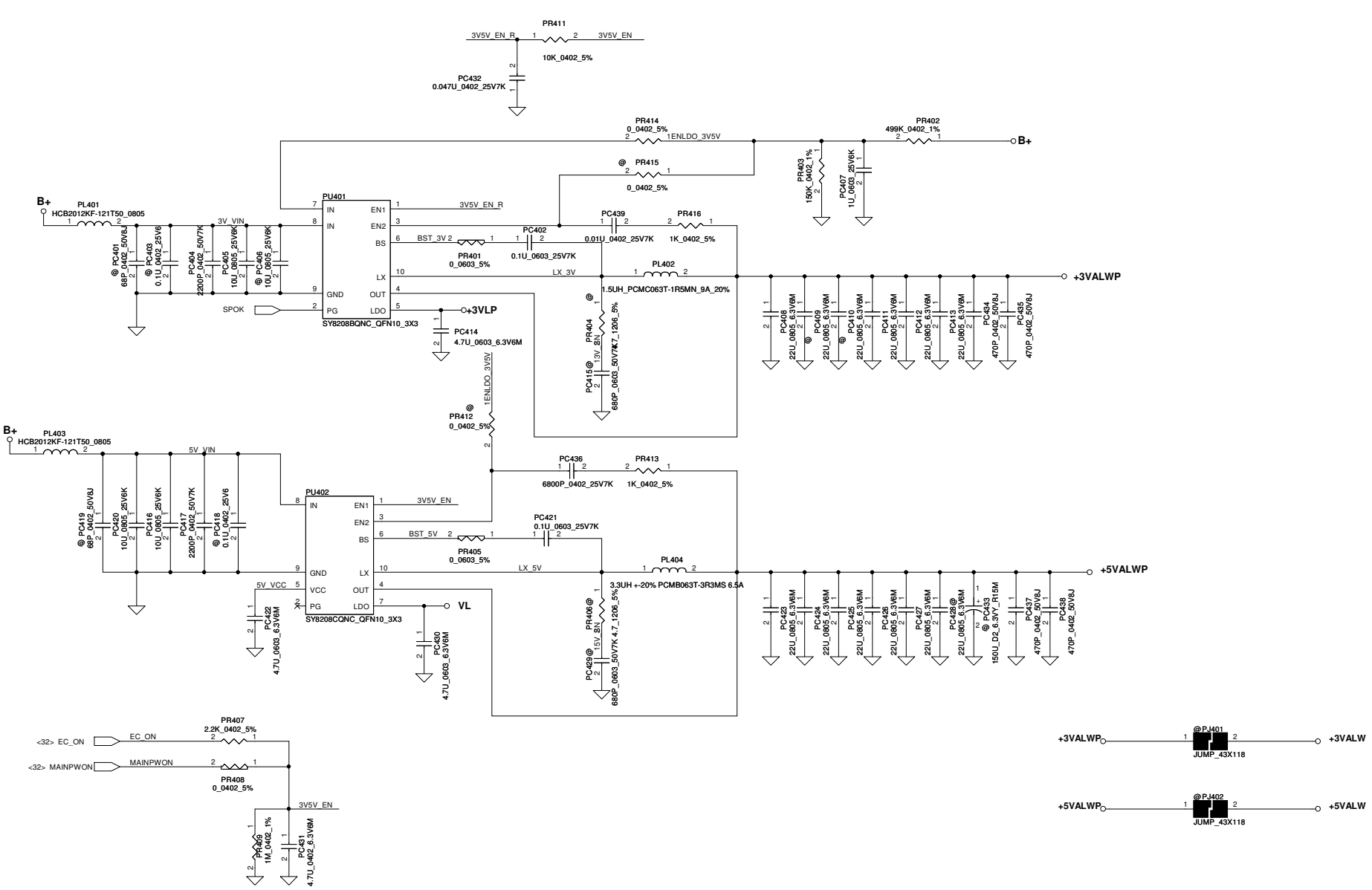
Compal Electronics, Inc.

Title: **CHARGER**

Size | Document Number: **Gx00-CR** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 38 of 60



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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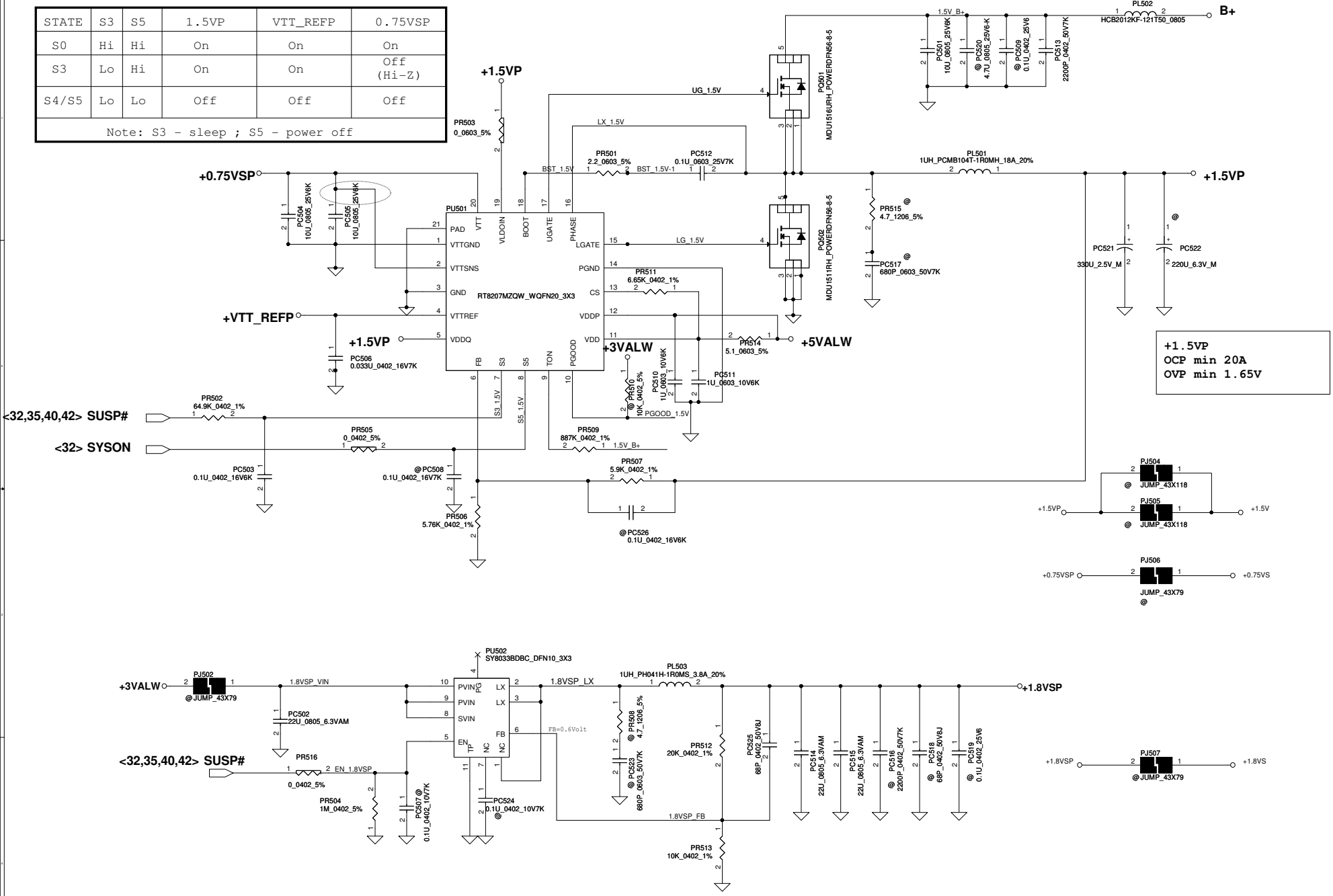
Compal Electronics, Inc.

Title: **+1.05VS VCCP**

Size: Custom | Document Number: **Gx00-CR** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 39 of 60

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: **+1.5VP/+1.8VSP**

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

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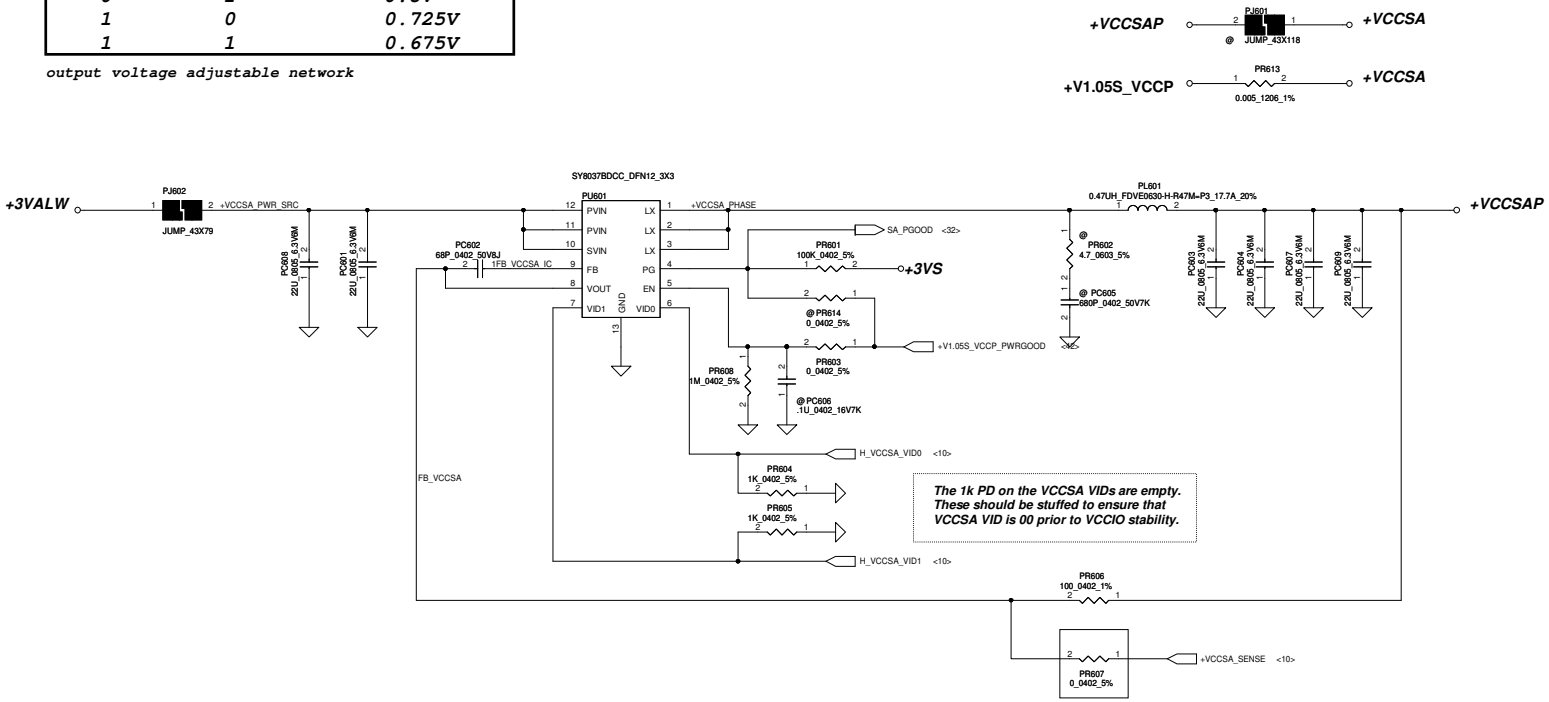
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



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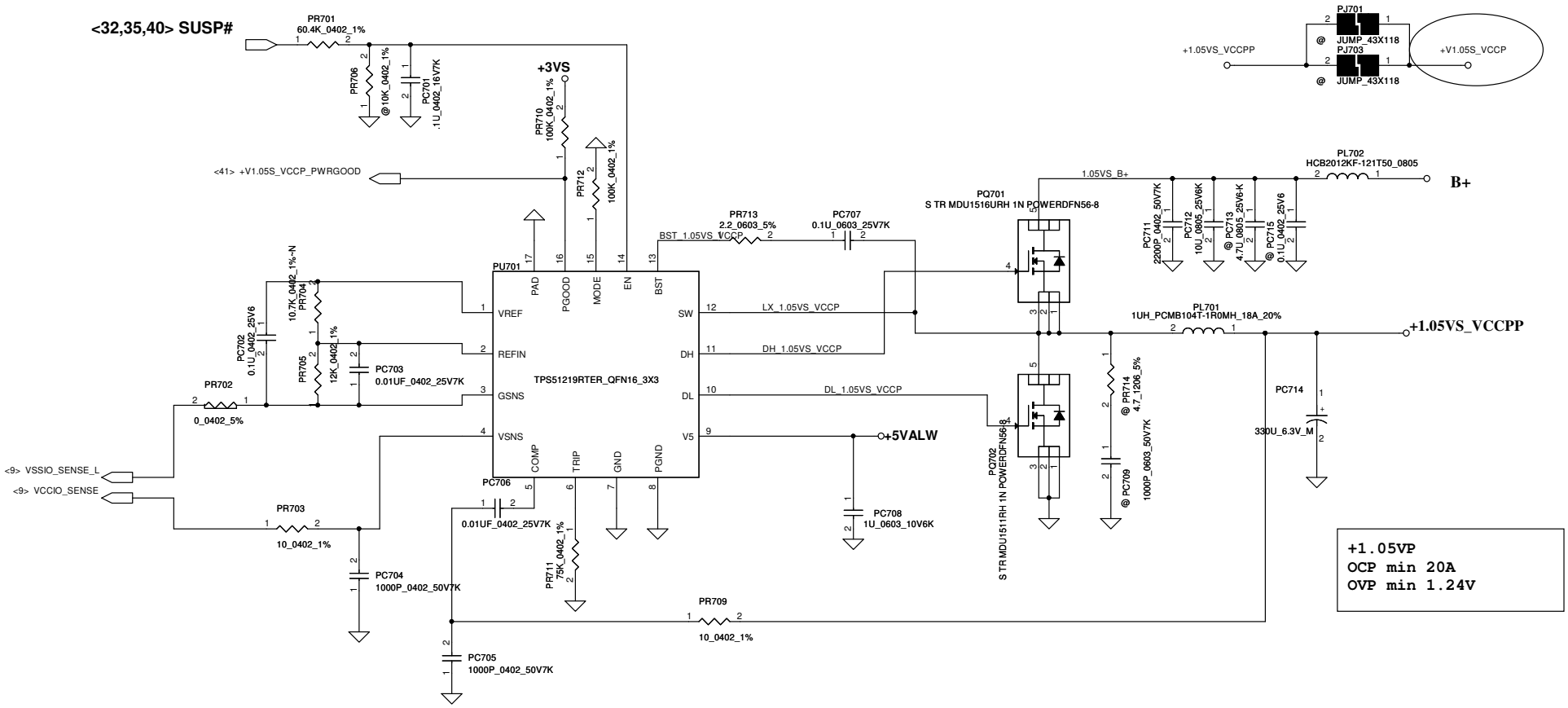
Compal Electronics, Inc.

Title: +VCCSAP

Size: C | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 41 of 60



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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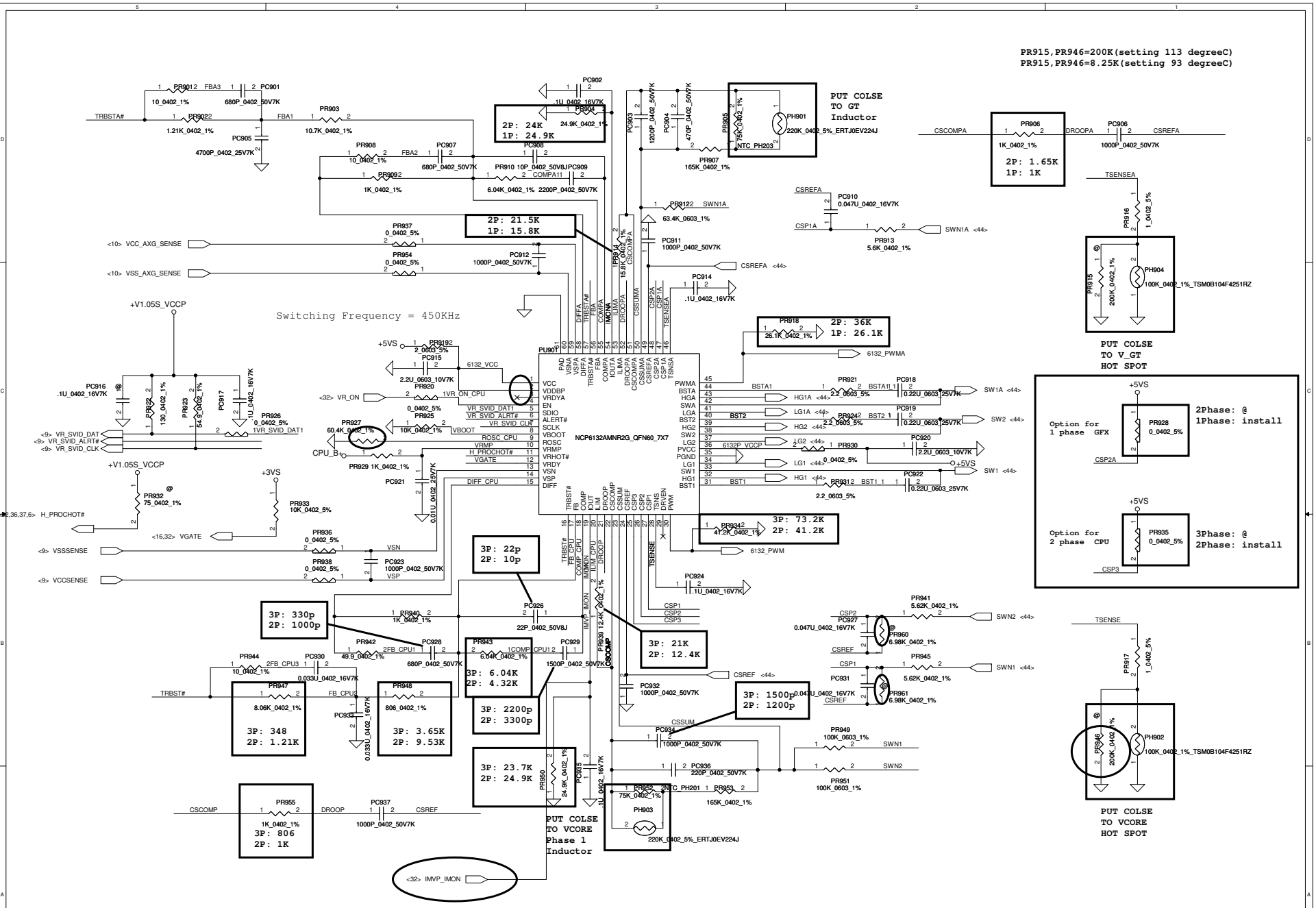
Compal Electronics, Inc.

Title: **+1.05VS_VCCP**

Size: Custom | Document Number: **Gx00-CR** | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 42 of 60



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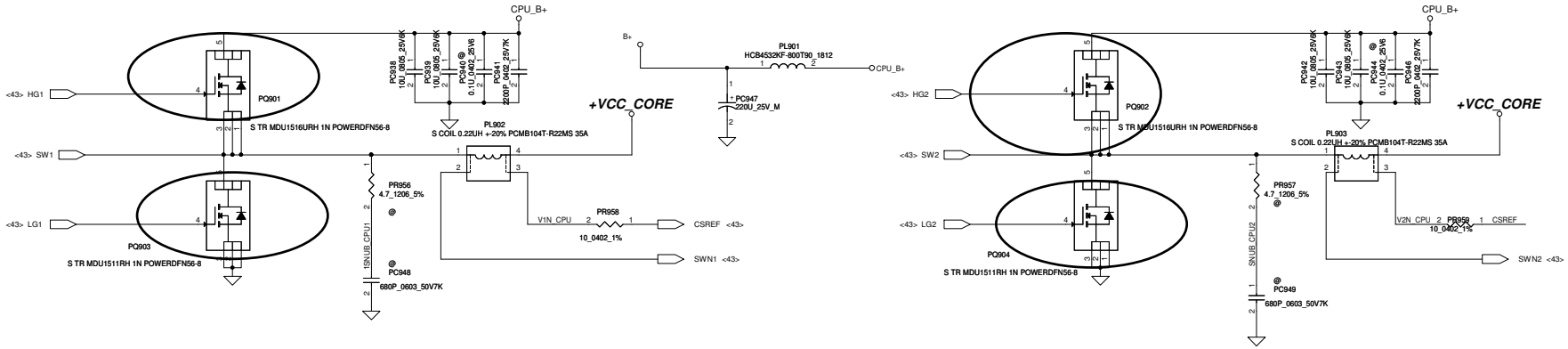
Compal Electronics, Inc.

Title: ***PWR-CPU_CORE***

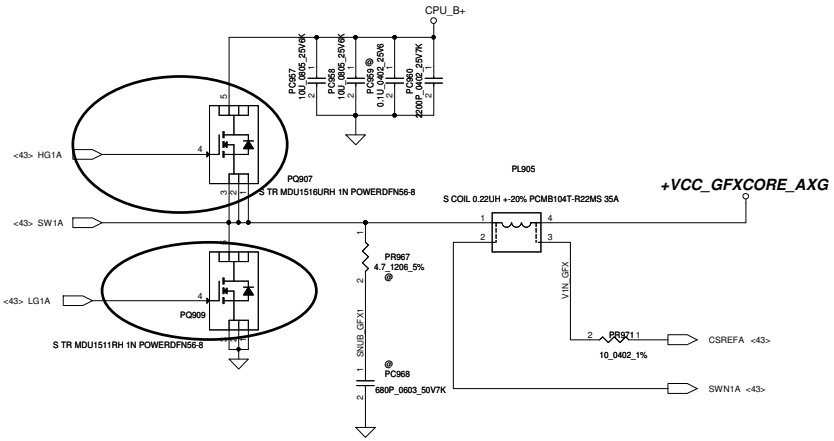
Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 43 of 60



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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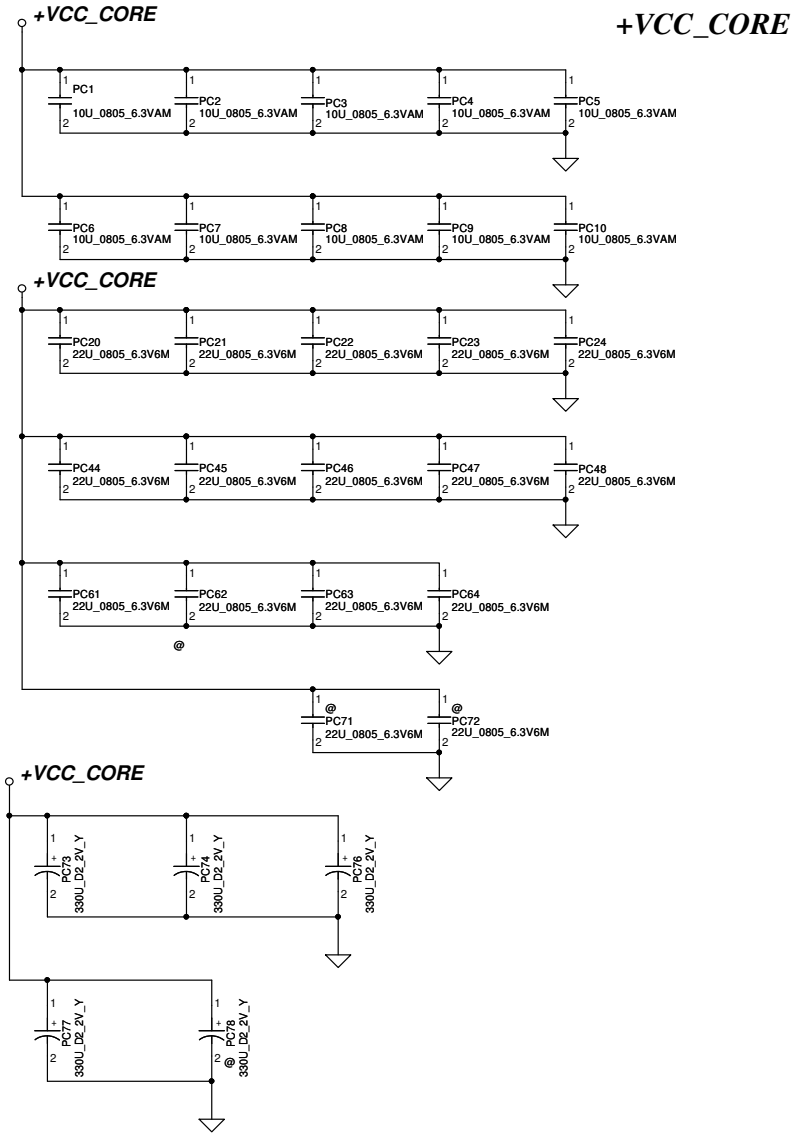
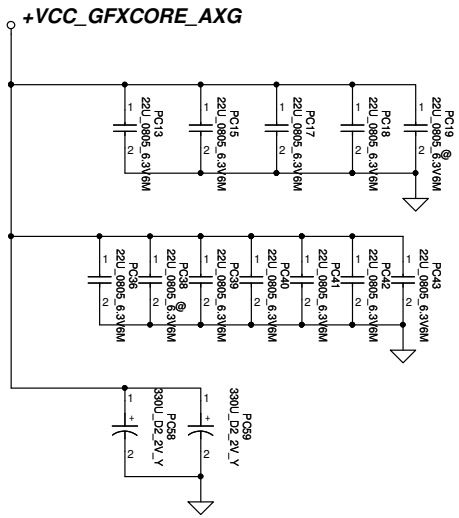
Compal Electronics, Inc.

Title: ***PWR-CPU_CORE***

Size: C | Document Number: Gx00-CR | Rev: 1.0

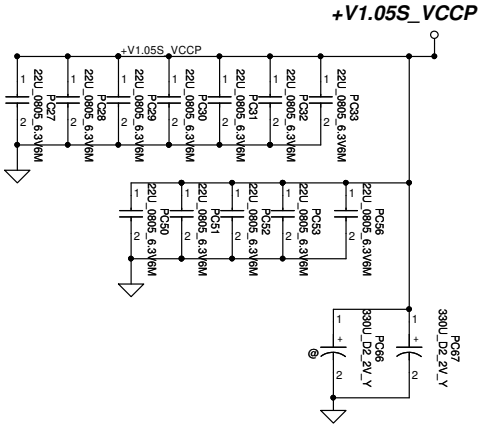
Date: Wednesday, February 27, 2013 | Sheet 44 of 60





Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



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Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size | Document Number: *LA-9632P* | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 45 of 60

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE	EVT TO DVT
1	P.46	Add PR102,PC108,PC109	For ADP_ID pin detect	
2	P.47	Add PR225,PR227,PR228,PQ206,PQ207,PQ208	For protect adapter function	
3	P.49	Add PR410,PC433	For 3VALWP/5VALWP sequence	
4	P.49	Add PC434,PC435,PC436,PC437	For EMI solution	
5	P.49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple	
6	P.50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence	
7	P.51	Add PC637	For +0.95VGSP sequence	
8	P.54	Change PC907,PR912,PR927,PC928	For CPU Transient Compensation	
9				
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Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

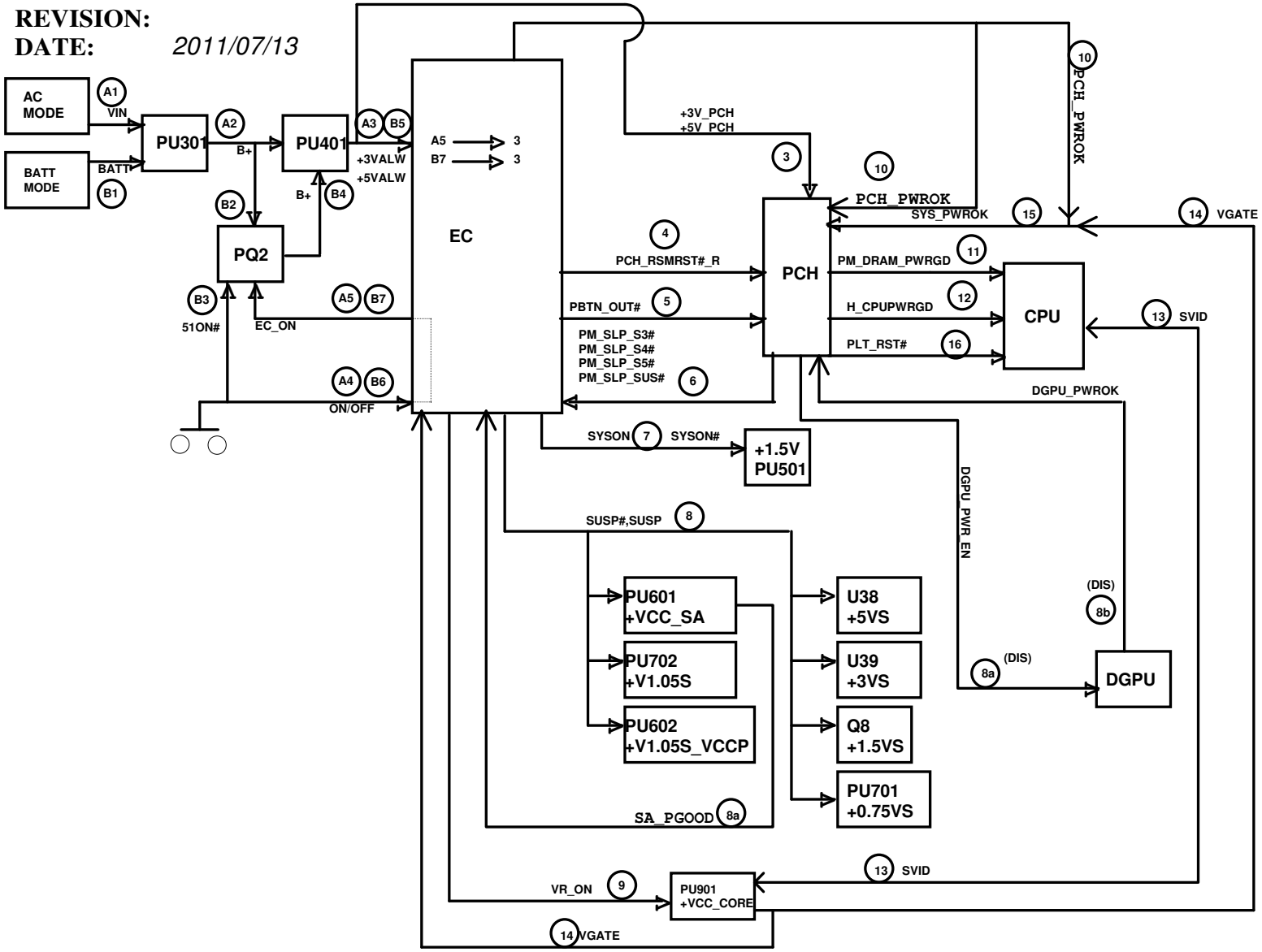
Title: PIR (PWR)

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 46 of 60

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9631P*
REVISION:
DATE: *2011/07/13*



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Compal Electronics, Inc.

Title: ***Power sequence***

Size: Custom | Document Number: *LA-9632P* | Rev: 1.0

Date: Wednesday, February 27, 2013 | Sheet 47 of 60

VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.36	Change C726, C727 to 2.2nF	For Sequence
2	P.26	Add R405	For Intel Combo Card
3	P.25	Delete RP19. Add RP26, RP27	Because ME modify MIC location
4	P.14	Add R406, R407, R408, R409	Reserve for improvement factory processes
5	P.32	Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
6	P.32	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
7	P.32	Reserve R410	Reserve Pull-high for GPIO
8	P.5~22	Change footprint of JCPU1, U4	For Lenovo rule
9	P.21	Add Q21, R40, C237, R225, C243	Reserve for power consumption
10	P.24	Add R411, R412, C411, C412	Reserve for EMI
11	P.32	Add ADP_65 to EC Pin.21	For adapter protection
12	P.32	Add ADP_90 to EC Pin.68	For adapter protection
13	P.32	Add ADP_135 to EC Pin.85	For adapter protection
14	P.32	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
15	P.32	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
16	P.32	Add ADP_ID to EC Pin.66	For adapter
17	P.32	Change PCH_ENBKL from EC Pin.73 to EC Pin.76	For common design
18	P.32	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
19	P.32	Add VGATE to EC Pin.74	Reserve for sequence
20	P.32	Add SYS_PWROK to EC Pin.86	Reserve for sequence
21	P.32	Change EC_TS_ON# from EC Pin.85 to EC Pin.97	For common design
22	P.32	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
23	P.32	Change SUSCLK from EC Pin.123 to EC Pin.122	For common design

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: HW-PIR1

Size: Custom | Document Number: LA-9632P | Rev: 1.0

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VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			DVT TO PVT
1	P.30	Delete R416, Add J9	No need Zero ODD Function
2	P.26	Reserve R508	For leakage current issue of Atheros WLAN
3	P.23	Add R509	protect BKOFF# damage
4	P.32	Reserve R416	Reserve +3VLP power rail to EC
5	P.32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.
6	P.32	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC.
7	P.14	Change U5 from 4MB to 8MB ROM	Follow common design
8	P.14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it
1	P.31	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5
2	P.32	Reserve resistance in EC for share ROM.	Follow common design
3	P.41	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU

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