UMA /Muxless Schematics Document
AMD LIANO CPU FS1
AMD Hudson M2/M3 and Seymour XT

http://j.gs/47mr

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A4	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 1 of 102	

PROJECT CODE : 91.4M001.001
PCB P/N : 11230
REVISION : -1

LB475 Block Diagram

Fingerprint BD

POWER BD

Cardreader BD
USB2 x 1

DDR3
1066/1333 MHz
14,15,16

DDR3
1066/1333 MHz
14,15,16

DDRIII 1066/1333

DDRIII 1066/1333

AMD Liano APU
(FS1 socket 35W)
722-Pin uFCPGA722
GPP X4 port
DP X6 Port
4,5,6,7,8

DDR3 VRAM
1GB/2GB
88,89,90,91

DDR3
900MHz

X8 PCI EXPRESS GRAPHIC(Muxless Lan8 ~Lan15)
X16 PCI EXPRESS GRAPHIC(Diserete only Lan0 ~Lan15)

Seymour XT
ATI
83,84,85,86,87

DP2(PCI EXPRESS Lan0~Lan3)

DP0

HDMI
51

PCIE x 2

UMI-Link
4X4

DP1

TRAVIS
9

LCD
49

CRT
50

CRT

RJ45
CONN 59

GLAN
RTL8111E
31

PCIE x 1

Mini-Card
WLAN
65

PCIE x 1

USB2.0 x 1

FCH
HUDSON-M2/M3
Integrated Display DAC
USB 3.0 (4parts)
USB 2.0
(10 parts or 14 port
if USB 3.0 do not used)
GPP X4 port
USB 1.1 (2 parts)
SATA (6 parts)
INT RTC
INT CLK GEN
HW MONITOR
ACPI 1.1
17,18,19,20,21,22

USB 3.0 x 1

MB
USB1 x 1
62

USB 2.0 x 1/SATAII x 1

E-SATA/USB
comb
57

SATA x 2

HDD
56

ODD
56

BD
USB x 2

Bluetooth
63

CAMERA
49

USB2.0 x 4

LPC Bus

LPC debug port
71

SD/MMC+/MS/
MS Pro/xD
74

CardReader
Realtek
RTS5139

USB 2.0 x 1

AZALIA

KBC
NUVOTON
NPCE791G
27

SPI

Internal DMIC

HP1

MIC IN

Azalia
CODEC
Realtek
ALC269Q
29

Flash ROM
2MB
60

Touch
PAD
69

Int.
KB
69

Thermal
EMC2103-2-AP
28

Fan
28

2CH SPEAKER

GMT
G1454

PCB STACKUP

TOP	L1
GND	L2
S	L3
S	L4
VCC	L5
S	L6
GND	L7
BOTTOM	L8

SYSTEM DC/DC
TPS51123 41

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 5V_AUX_S5 3D3V_AUX_S5

TPS51211 45

INPUTS	OUTPUTS
DCBATOUT	1D1V_S5

TPS51211 45

INPUTS	OUTPUTS
DCBATOUT	1D2V_S0

TPS51216 46

INPUTS	OUTPUTS
5V_S5	0D75_S0

TPS51216 46

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

CHARGER
BQ24707 40

INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC
ISL6267 42

INPUTS	OUTPUTS
DCBATOUT	APU_VDD

GFX Core
ISL6267 43

INPUTS	OUTPUTS
DCBATOUT	APU_VDDNB

VGA
RT8208 92

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 2 of 102

Strapping

REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

USB Table

USB	
Pair	Device
0	USB_Z
1	WLAN/WiMAX
2	Finger Print
3	Bluetooth
4	WWAN
5	Card Reader(IO Board)
6	E-SATA
7	CCD
8	USB3(RJ45_USB Board)
9	USB2(IO Board)
10	NC
11	NC
12	NC
13	NC

PCIE Routing

	APU
LANE0	LAN
LANE1	
LANE2	WLAN
LANE3	

	FCH
LANE0	
LANE1	
LANE2	
LANE3	

http://j.gs/47mr

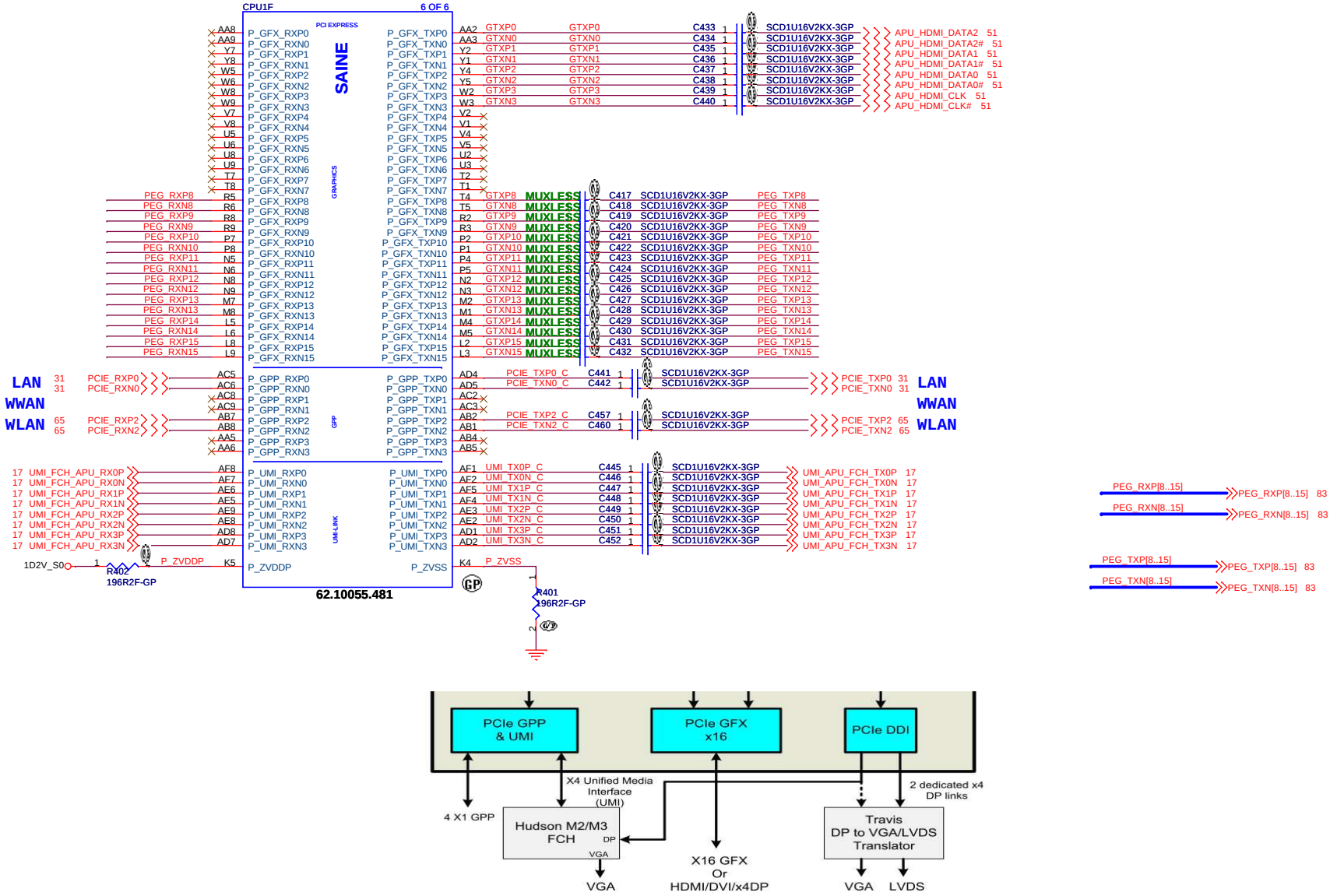
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

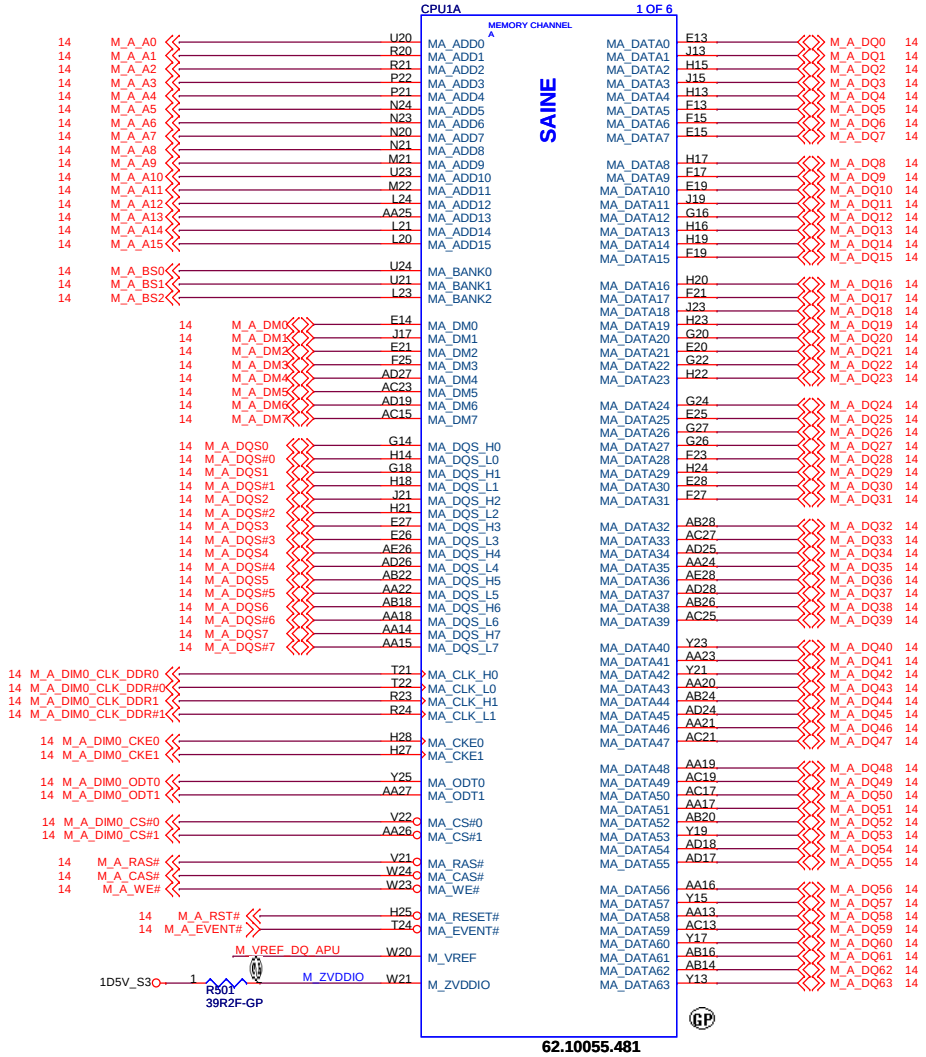
Size: A3 | Document Number: LB475 | Rev: -1

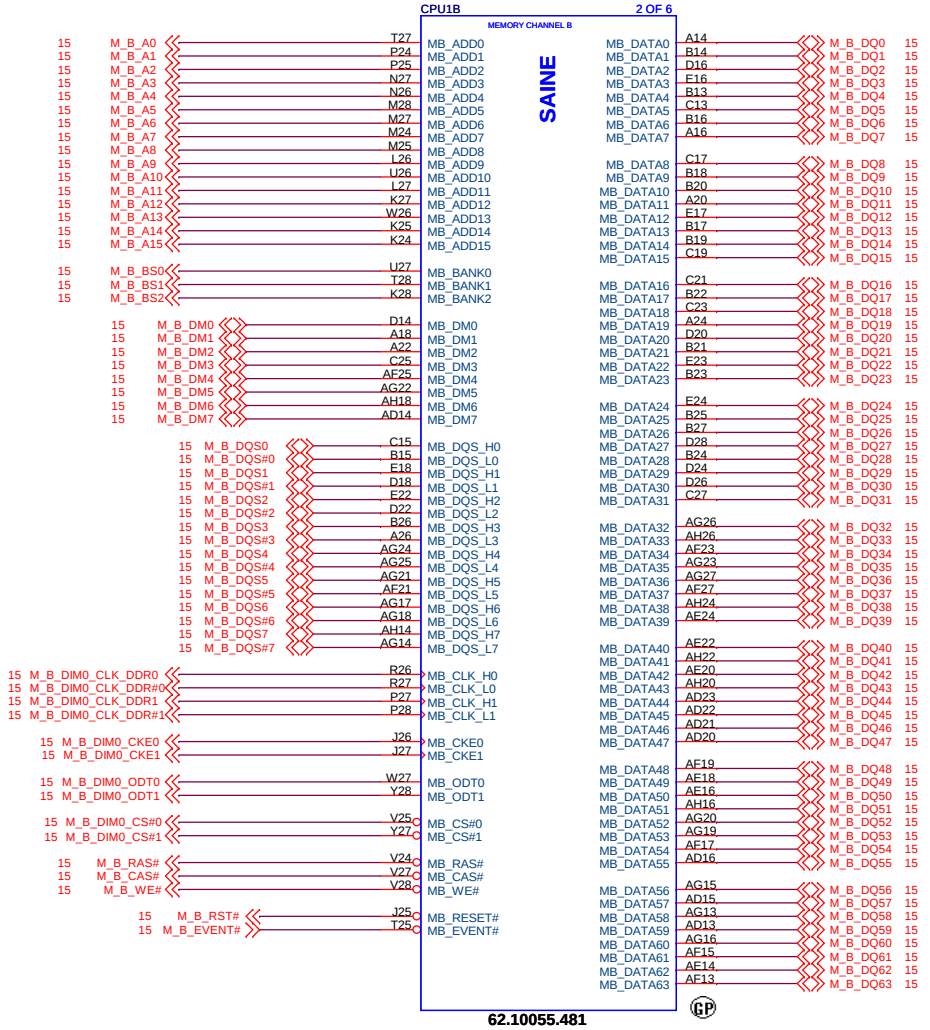
Date: Tuesday, August 02, 2011 | Sheet 3 of 102



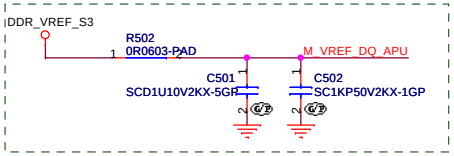
<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: APU_PCIE(1/5)		
Size: A3	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 4 of 102	

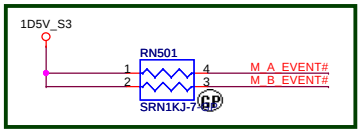


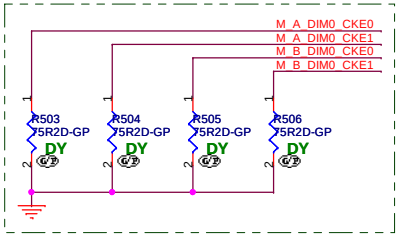


APU_VREF_DQ



LAYOUT: place them close to APU





<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APU_DDR(2/5)

Size: A3 | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 5 of 102

SVC	SVD	Boot Voltage (VCC/GND)	Boot Voltage (Open)
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.1
1	1	0.8	0.9

TRAVIS LVDS Panel

VGA output from FCH

CPU1C

SAINE

62.10055.481

[AMD HDMI desing guidance]

Strap define PU :Enable HDMI
PD:Disable HDMI

[AMD FAE Frank]:
this is electrical key
do not allow power to turn on if this pin is still "L"
FS1 package is open pin
in the furtur,FS1r2 will have this pin tied to VSS
if the wrong processor is plugged the socket
This is more of a problem on desktop platforms
(changing CPUs)

http://j.gs/47mr

CPU exceeds to 125℃

S3 Power

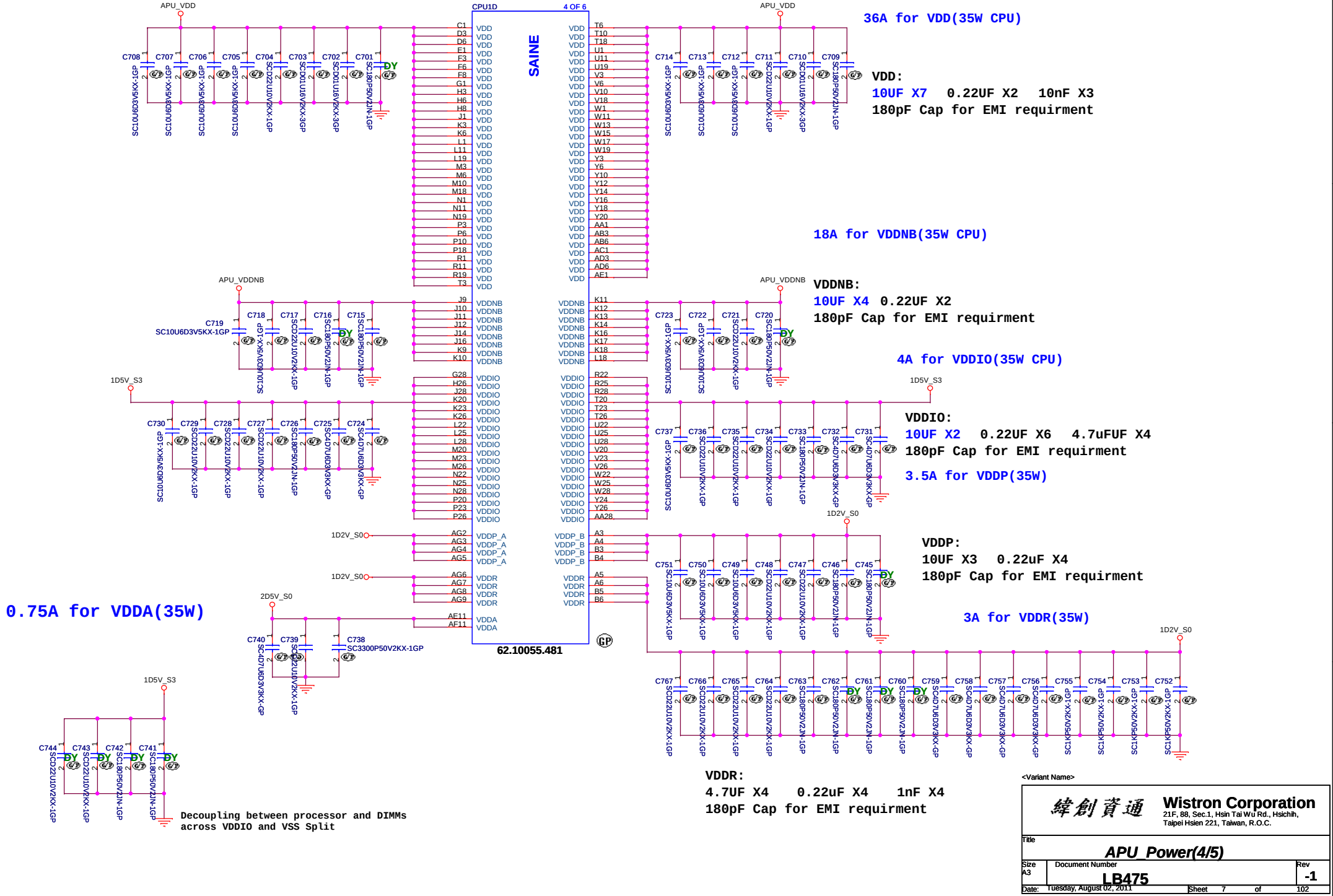
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APU_Control&Debug(3/5)

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 6 of 102



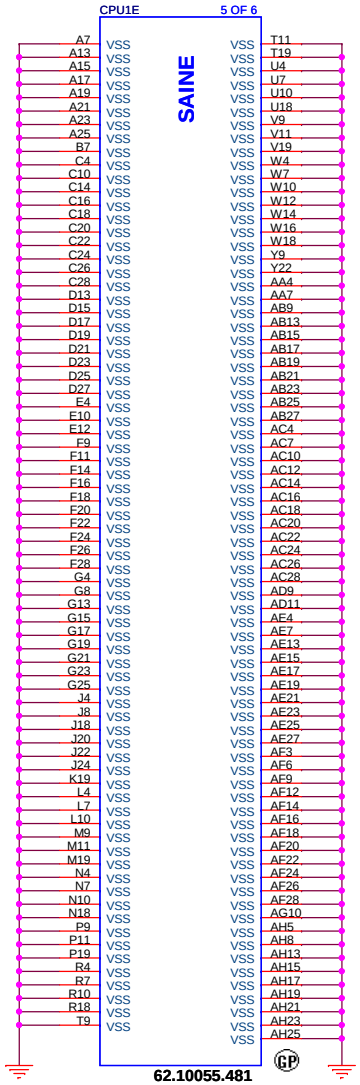
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APU_Power(4/5)

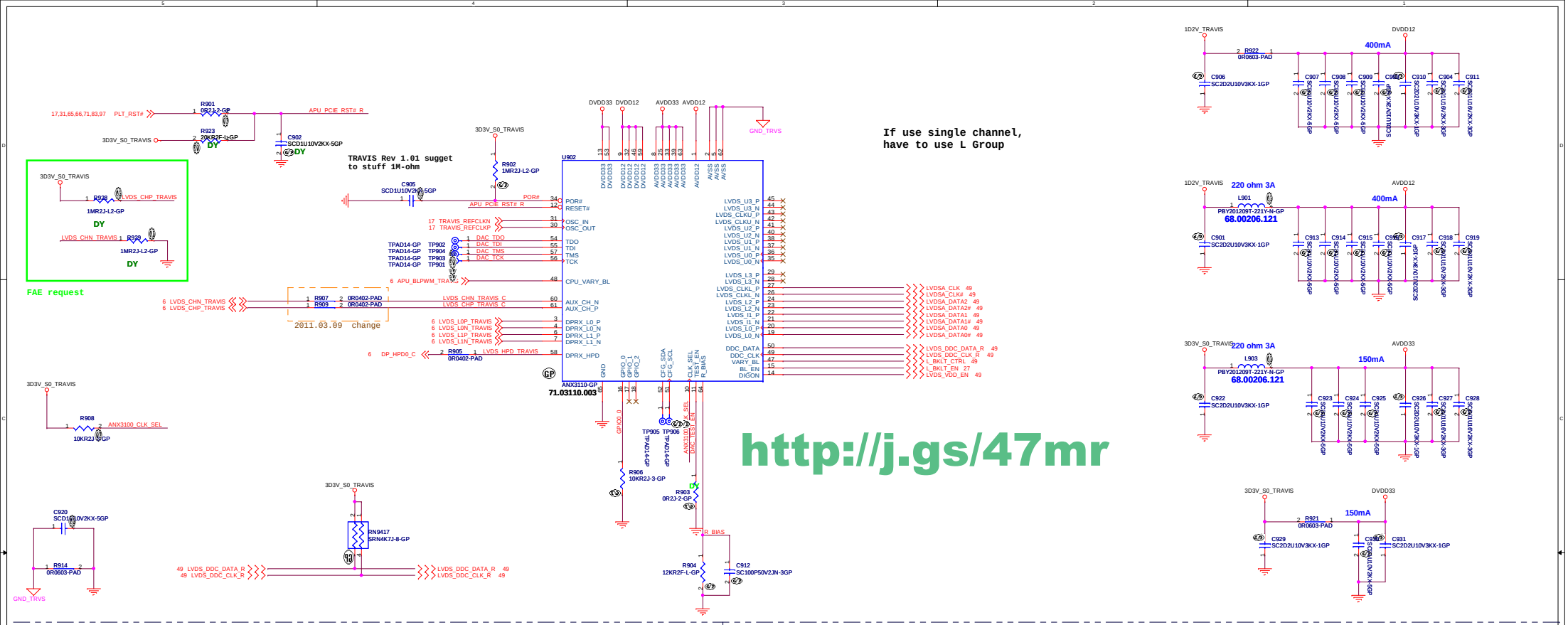
Size	Document Number	Rev
A3	LB475	-1

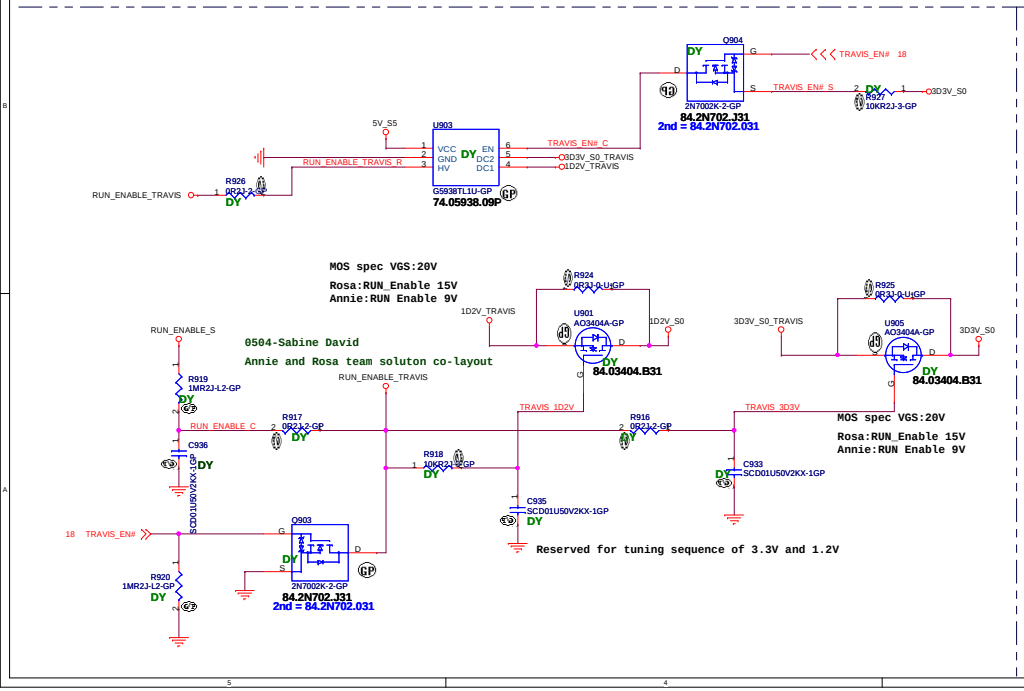
Date: Tuesday, August 02, 2011 Sheet 7 of 102



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *APU_VSS(5/5)*		
Size: A3	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 8 of 102	





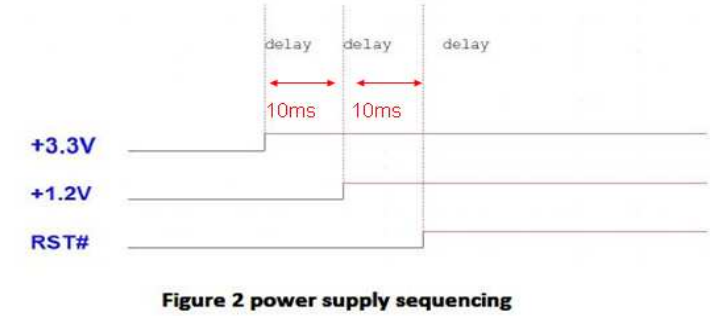


Figure 2 power supply sequencing

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TRAVIS**

Size	Document Number	Rev
A2	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 9 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 10 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 11 of 102

(Blanking)

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 12 of 102	

(Blanking)

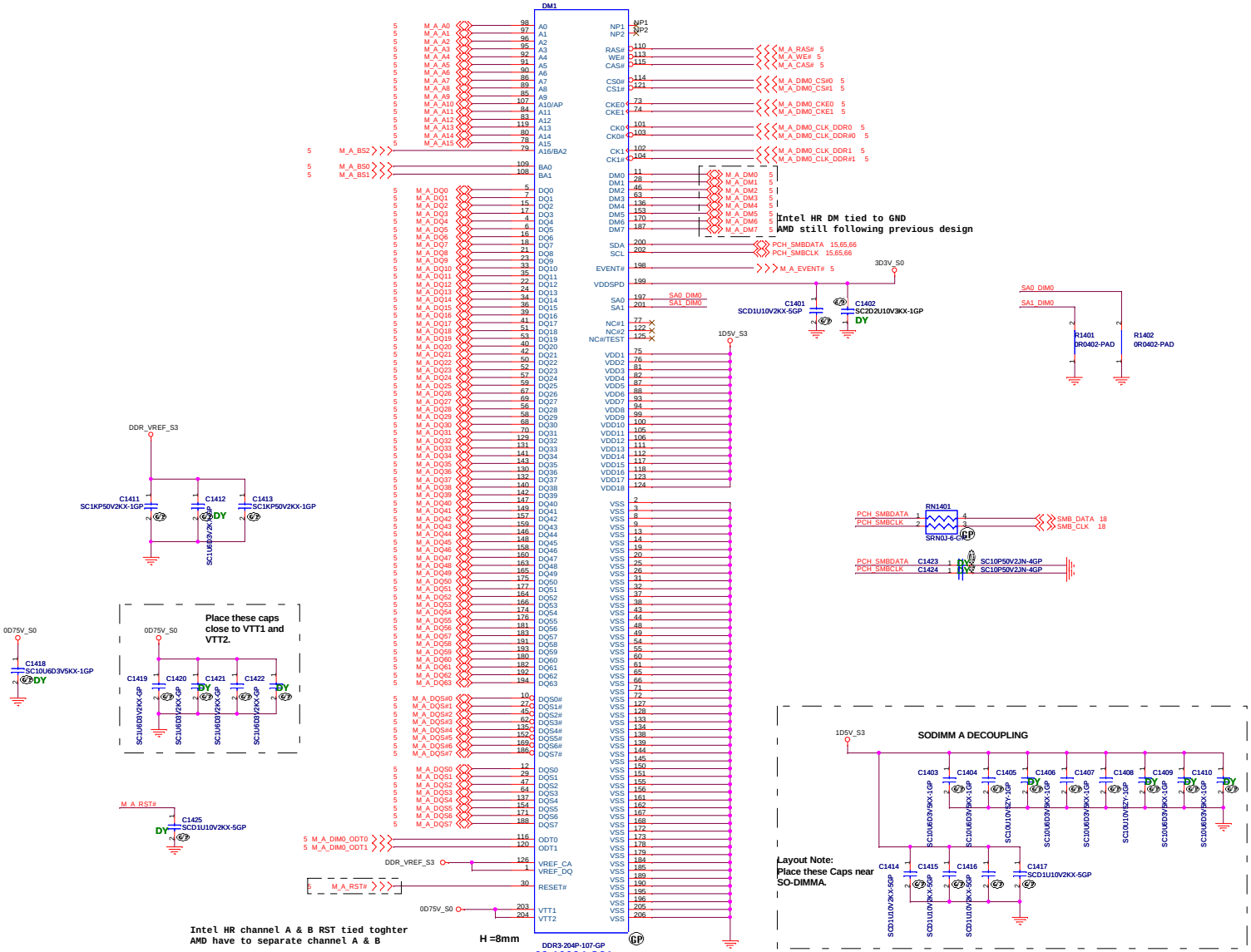
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 13 of 102



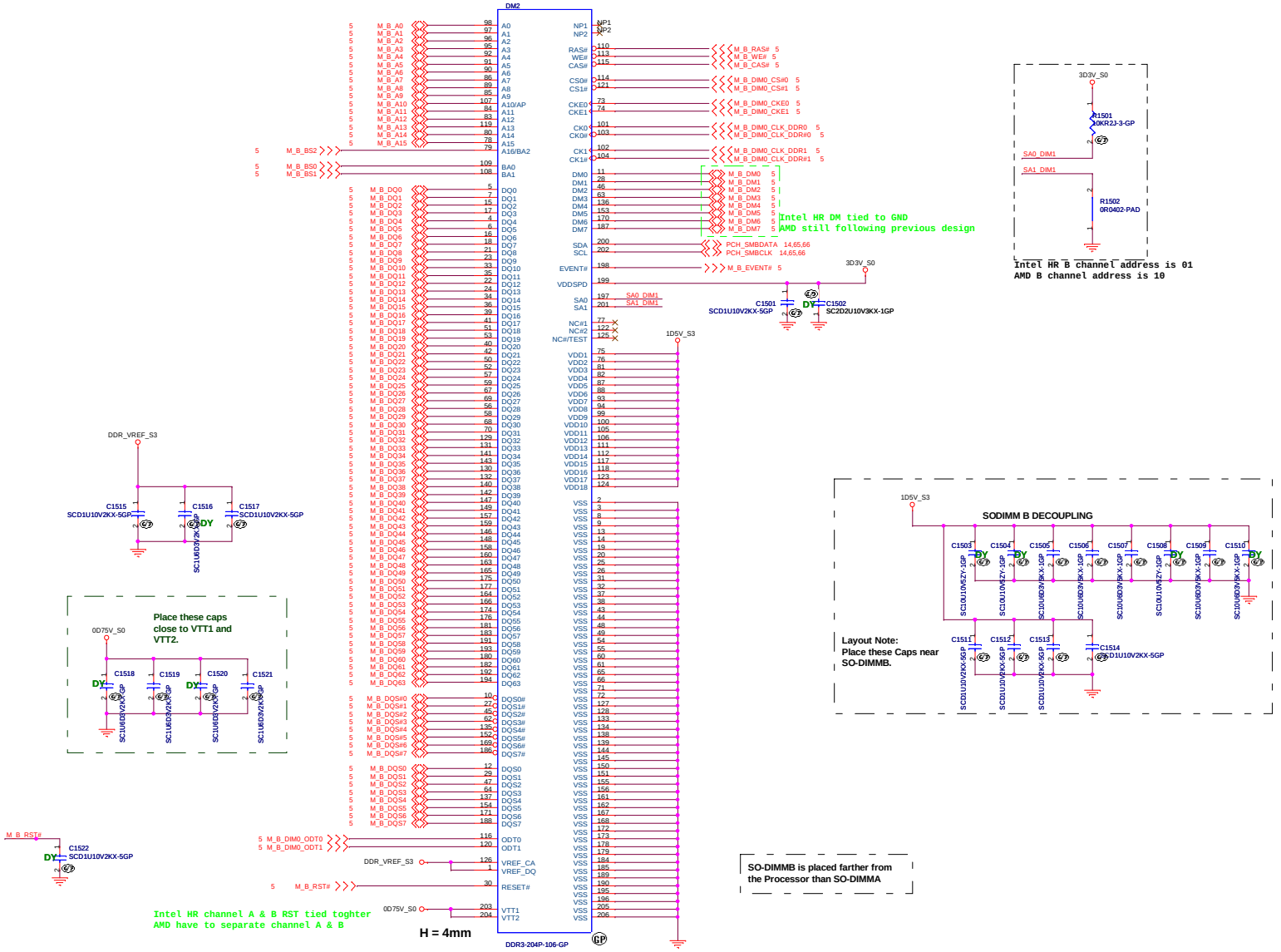
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
A2	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 14 of 102



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
A2	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 15 of 102

(Blanking)

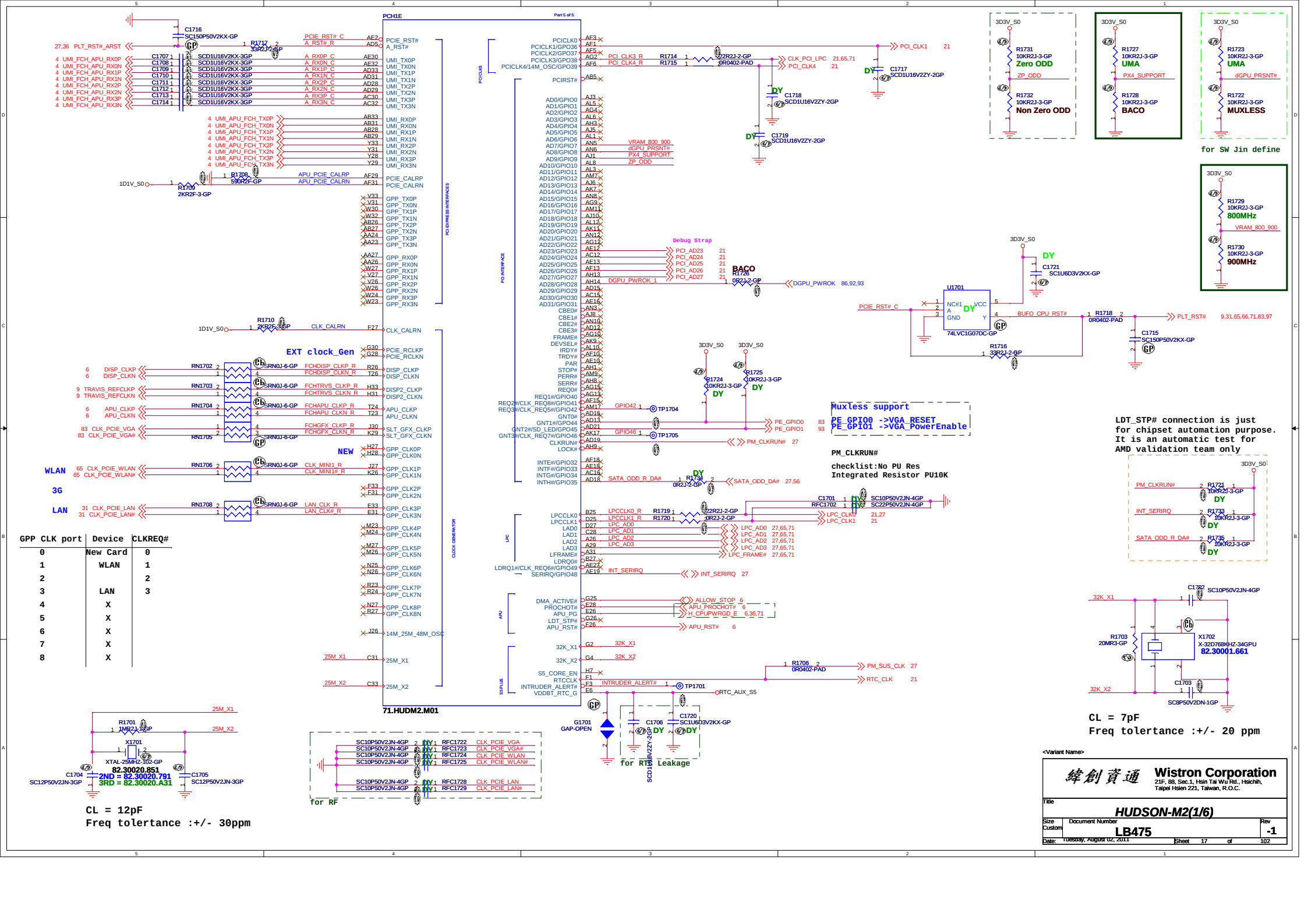
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 16 of 102



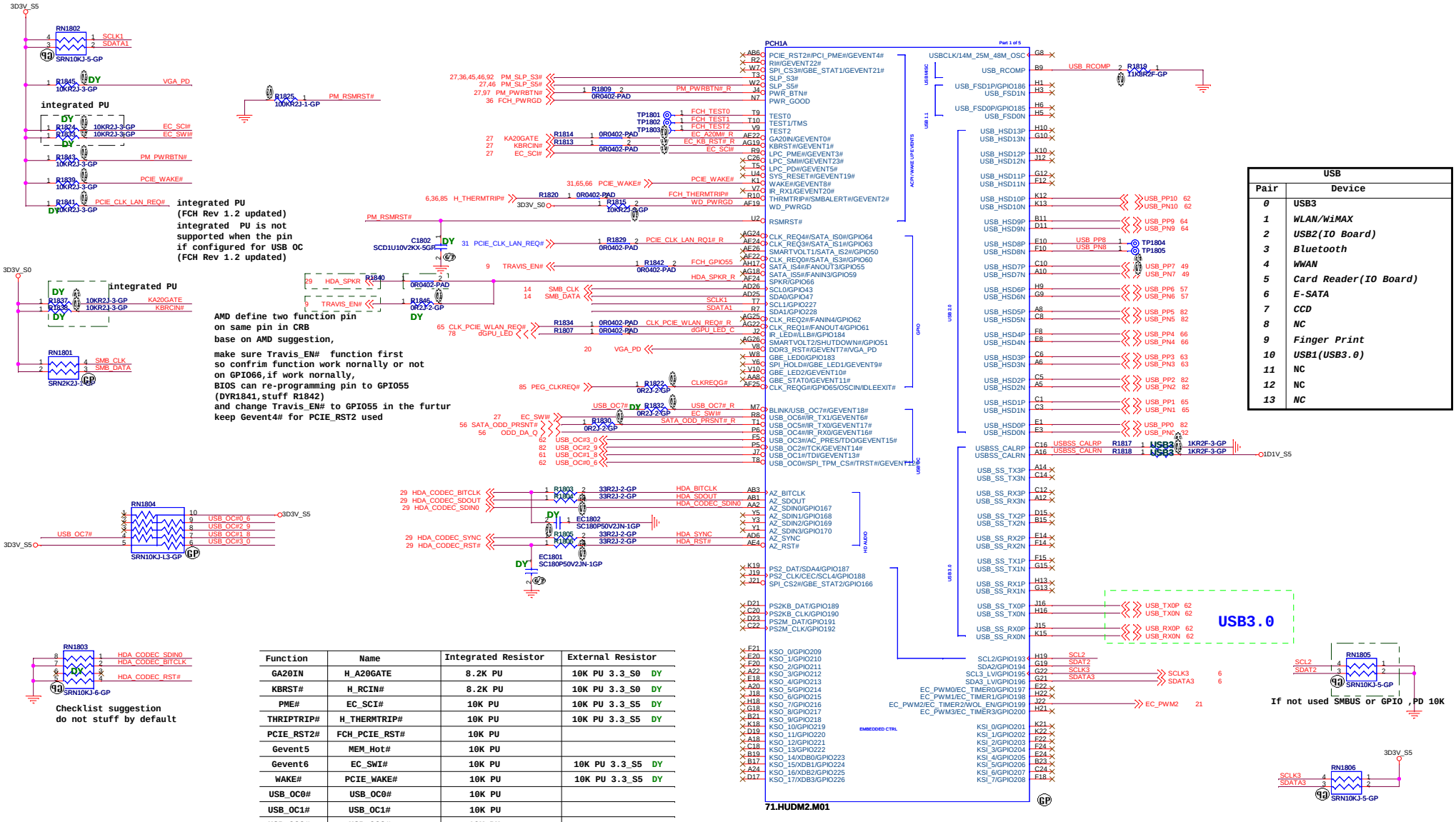
GPP CLK port	Device	CLKREQ#
0	New Card	0
1	WLAN	1
2		2
3	LAN	3
4	X	
5	X	
6	X	
7	X	
8	X	

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HUDSON-M2(1/6)

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 17 of 102



Function	Name	Integrated Resistor	External Resistor	
GA20IN	H_A20GATE	8.2K PU	10K PU 3.3_S0	DY
KBRST#	H_RCIN#	8.2K PU	10K PU 3.3_S0	DY
PME#	EC_SCI#	10K PU	10K PU 3.3_S5	DY
THRIPTRIP#	H_THERMTRIP#	10K PU	10K PU 3.3_S5	DY
PCIE_RST2#	FCH_PCIE_RST#	10K PU		
Gevent5	MEM_Hot#	10K PU		
Gevent6	EC_SWI#	10K PU	10K PU 3.3_S5	DY
WAKE#	PCIE_WAKE#	10K PU	10K PU 3.3_S5	DY
USB_OC0#	USB_OC0#	10K PU		
USB_OC1#	USB_OC1#	10K PU		
USB_OC2#	USB_OC2#	10K PU		
Gevent15#	SATA_ODD_PRSNT#	10K PU		
Gevent16#	ODD_DA	10K PU		
USB_OC5#	USB_OC5#	10K PU		
Gevent17#	EC_SWI#	10K PU	10K PU 3.3_S0	DY
USB_OC7#	USB_OC7#	10K PU		
LPC_SMI#	EC_SMI#	8.2K PU	10K PU 3.3_S5	DY
GPIO35	SATA_ODD_DA#	8.2K PU		
SERIRQ	INT_SERIRQ	8.2K PU	10K PU 3.3_S0	DY
CLK_REQ0	CLK_PCIE_NEW_REQ#	8.2K PU		
CLK_REQ1	CLK_PCIE_WLAN_REQ#	8.2K PU		
CLK_REQ2	CLK_PCIE_WWAN_REQ#	8.2K PU		
CLK_REQ3	PCIE_CLK_LAN_RQ1#	8.2K PU		
CLK_REQ6	PEG_CLKREQ#	8.2K PU		

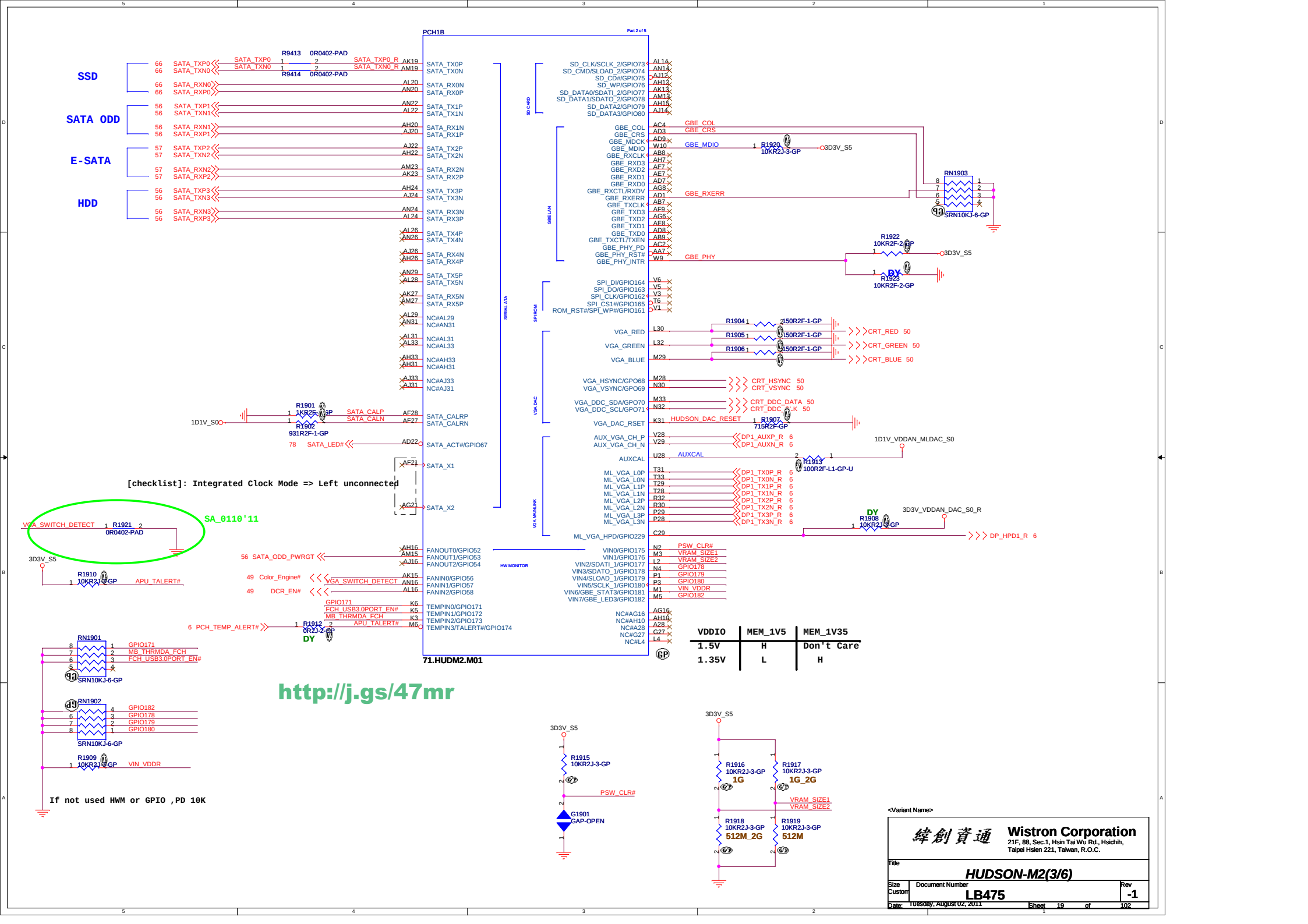
USB	
Pair	Device
0	USB3
1	WLAN/WiMAX
2	USB2(IO Board)
3	Bluetooth
4	WWAN
5	Card Reader(IO Board)
6	E-SATA
7	CCD
8	NC
9	Finger Print
10	USB1(USB3.0)
11	NC
12	NC
13	NC

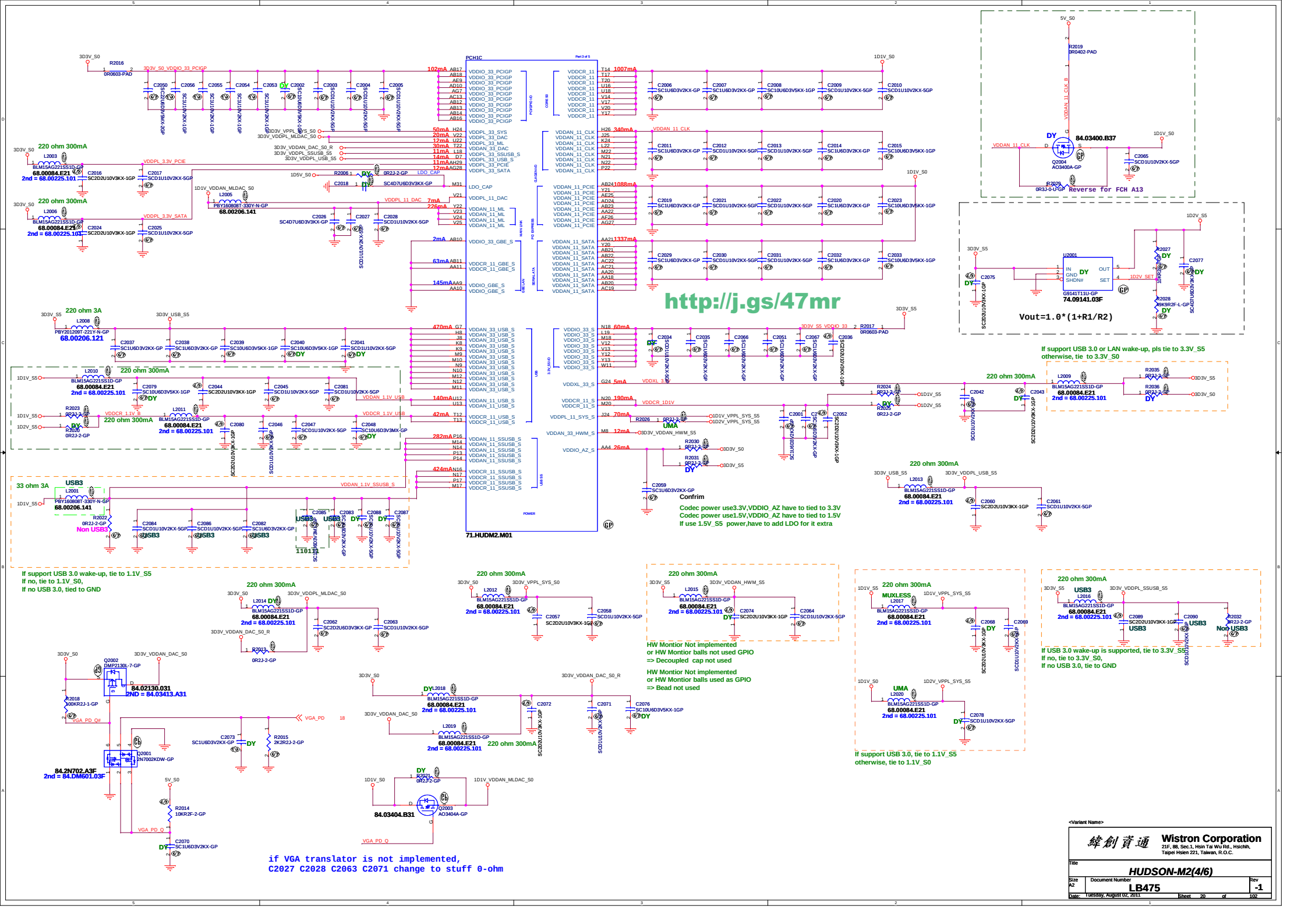
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: HUDSON-M2(2/6)

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 18 of 102

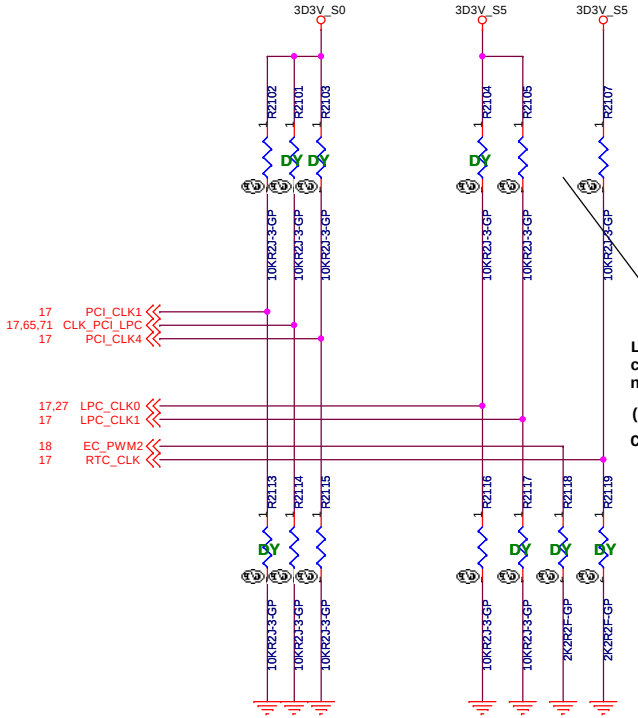

PCH1B
Part 2 of 5
SSD
SATA ODD
E-SATA
HDD
R9413 0R0402-PAD
R9414 0R0402-PAD
SATA_TXP0
SATA_TXN0
SATA_TXP0_R
SATA_TXN0_R
SATA_RXN0
SATA_RXP0
SATA_TXP1
SATA_TXN1
SATA_RXN1
SATA_RXP1
SATA_TXP2
SATA_TXN2
SATA_RXN2
SATA_RXP2
SATA_TXP3
SATA_TXN3
SATA_RXN3
SATA_RXP3
SATA_TX0P
SATA_TX0N
SATA_RX0N
SATA_RX0P
SATA_TX1P
SATA_TX1N
SATA_RX1N
SATA_RX1P
SATA_TX2P
SATA_TX2N
SATA_RX2N
SATA_RX2P
SATA_TX3P
SATA_TX3N
SATA_RX3N
SATA_RX3P
SATA_TX4P
SATA_TX4N
SATA_RX4N
SATA_RX4P
SATA_TX5P
SATA_TX5N
SATA_RX5N
SATA_RX5P
NC#AL29
NC#AN31
NC#AL31
NC#AL33
NC#AH33
NC#AH31
NC#AJ33
NC#AJ31
SATA_CALRP
SATA_CALRN
SATA_ACT#/GPIO67
SATA_X1
SATA_X2
SERIAL ATA
R1901 1KR2F-GP
R1902 931R2F-1-GP
SATA_CALP
SATA_CALN
SATA_LED#
1D1V_S0
SD_CLK/SCLK_2/GPIO73
SD_CMD/SLOAD_2/GPIO74
SD_CD#/GPIO75
SD_WP/GPIO76
SD_DATA0/SDATI_2/GPIO77
SD_DATA1/SDATO_2/GPIO78
SD_DATA2/GPIO79
SD_DATA3/GPIO80
SD CARD
GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN
R1920 10KR2J-3-GP
3D3V_S5
RN1903
SRN10KJ-6-GP
R1922 10KR2F-2-GP
R1923 10KR2F-2-GP
DY
SPI_DI/GPIO164
SPI_DO/GPIO163
SPI_CLK/GPIO162
SPI_CS1#/GPIO165
ROM_RST#/SPI_WP#/GPIO161
SPI ROM
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_HSYNC/GPO68
VGA_VSYNC/GPO69
VGA_DDC_SDA/GPO70
VGA_DDC_SCL/GPO71
VGA_DAC_RSET
R1904 150R2F-1-GP
R1905 150R2F-1-GP
R1906 150R2F-1-GP
R1907 715R2F-GP
CRT_RED 50
CRT_GREEN 50
CRT_BLUE 50
CRT_HSYNC 50
CRT_VSYNC 50
CRT_DDC_DATA 50
CRT_DDC_CLK 50
HUDSON_DAC_RESET
VGA DAC
AUX_VGA_CH_P
AUX_VGA_CH_N
AUXCAL
ML_VGA_L0P
ML_VGA_L0N
ML_VGA_L1P
ML_VGA_L1N
ML_VGA_L2P
ML_VGA_L2N
ML_VGA_L3P
ML_VGA_L3N
ML_VGA_HPD/GPIO229
DP1_AUXP_R 6
DP1_AUXN_R 6
DP1_TX0P_R 6
DP1_TX0N_R 6
DP1_TX1P_R 6
DP1_TX1N_R 6
DP1_TX2P_R 6
DP1_TX2N_R 6
DP1_TX3P_R 6
DP1_TX3N_R 6
DP_HPD1_R 6
1D1V_VDDAN_MLDAC_S0
R1913 100R2F-L1-GP-U
3D3V_VDDAN_DAC_S0_R
R1908 10KR2J-3-GP
VGA MAINLINK
FANOUT0/GPIO52
FANOUT1/GPIO53
FANOUT2/GPIO54
FANIN0/GPIO56
FANIN1/GPIO57
FANIN2/GPIO58
TEMPIN0/GPIO171
TEMPIN1/GPIO172
TEMPIN2/GPIO173
TEMPIN3/TALERT#/GPIO174
VIN0/GPIO175
VIN1/GPIO176
VIN2/SDATI_1/GPIO177
VIN3/SDATO_1/GPIO178
VIN4/SLOAD_1/GPIO179
VIN5/SCLK_1/GPIO180
VIN6/GBE_STAT3/GPIO181
VIN7/GBE_LED3/GPIO182
PSW_CLR#
VRAM_SIZE1
VRAM_SIZE2
VIN_VDDR
GPIO178
GPIO179
GPIO180
HW MONITOR
NC#AG16
NC#AH10
NC#A28
NC#G27
NC#L4
56 SATA_ODD_PWRGT
49 Color_Engine#
49 DCR_EN#
VGA_SWITCH_DETECT
GPIO171
FCH_USB3.0PORT_EN#
MB_THRMDA_FCH
APU_TALERT#
6 PCH_TEMP_ALERT#
R1912 0R2J-2-GP
DY
71.HUDM2.M01
[checklist]: Integrated Clock Mode => Left unconnected
SA_0110'11
VGA_SWITCH_DETECT
R1921 0R0402-PAD
3D3V_S5
R1910 10KR2J-3-GP
APU_TALERT#
RN1901
SRN10KJ-6-GP
RN1902
SRN10KJ-6-GP
R1909 10KR2J-3-GP
VIN_VDDR
If not used HWM or GPIO ,PD 10K
http://j.gs/47mr
R1915 10KR2J-3-GP
PSW_CLR#
G1901 GAP-OPEN
R1916 10KR2J-3-GP 1G
R1917 10KR2J-3-GP 1G_2G
R1918 10KR2J-3-GP 512M_2G
R1919 10KR2J-3-GP 512M
VDDIO | MEM_1V5 | MEM_1V35
1.5V | H | Don't Care
1.35V | L | H
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HUDSON-M2(3/6)
Size Custom
Document Number
LB475
Rev
-1
Date: Tuesday, August 02, 2011
Sheet 19 of 102


PCH1C
71.HUDM2.M01
http://j.gs/47mr
Vout=1.0*(1+R1/R2)
Reverse for FCH A13
UMA
Confrim
Codec power use3.3V,VDDIO_AZ have to tied to 3.3V
Codec power use1.5V,VDDIO_AZ have to tied to 1.5V
If use 1.5V_S5 power,have to add LDO for it extra
If support USB 3.0 or LAN wake-up, pls tie to 3.3V_S5
otherwise, tie to 3.3V_S0
If support USB 3.0 wake-up, tie to 1.1V_S5
If no, tie to 1.1V_S0,
If no USB 3.0, tied to GND
HW Montior Not implemented
or HW Montior balls not used GPIO
=> Decoupled cap not used
HW Montior Not implemented
or HW Montior balls used as GPIO
=> Bead not used
If support USB 3.0, tie to 1.1V_S5
otherwise, tie to 1.1V_S0
If USB 3.0 wake-up is supported, tie to 3.3V_S5
If no, tie to 3.3V_S0,
If no USB 3.0, tie to GND
if VGA translator is not implemented,
C2027 C2028 C2063 C2071 change to stuff 0-ohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HUDSON-M2(4/6)
LB475
-1
Tuesday, August 02, 2011
20
102

SSID = S.B

REQUIRED STRAPS

CRB:PU 3.3V_AUX_S5
checklist:PU 3.3V_S5
no support S5 PLUS funciton,PU 3.3V_S5



LPC ROM implemented
checklistsuggestion:
no PU or PD required

(integrated PU 10K)

CRB: do not stuff PU Res

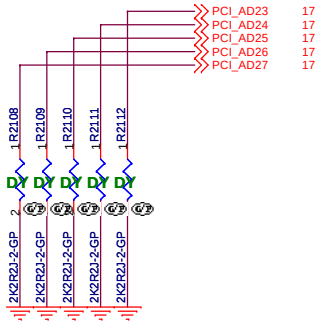
REQUIRED SYSTEM STRAPS

USE this pin to determine INT/EXT CLK

	EC_PWM2 PCH GPO199	PCI_CLK1	RTC_CLK	CLK_PCI_LPC	PCI_CLK4	LPC_CLK0	LPC_CLK1
PULL HIGH	LPC ROM DEFAULT	Allow PCIE GEN2 DEFAULT	S5_PLUS Mode DISABLE DEFAULT	USE DEBUG STRAPS	non_Fusion CLOCK mode	ENABLE EC	CLKGEN ENABLED (Use Internal) DEFAULT
PULL LOW	SPI ROM	Force PCIE GEN1	S5_PLUS Mode ENABLE	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK mode DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED (Use External)

Ball Name	Strap Function	Description
EC_PWM2	ROM Type	SPI ROM: 2.2-KΩ 5% pull-down LPC ROM: Pull-up to 3.3V_S5. External pull-up resistor is not required as FCH has integrated 10-KΩ pull-up to 3.3V_S5.

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL (DEFAULT)	Disable ILA AUTORUN (DEFAULT)	USE FC PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Disable PCI MEM BOOT (DEFAULT)
PULL LOW	BYPASS PCI PLL	Enable ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	Enable PCI MEM BOOT

Note: FCH has 15K internal PU FOR PCI_AD[27:23]

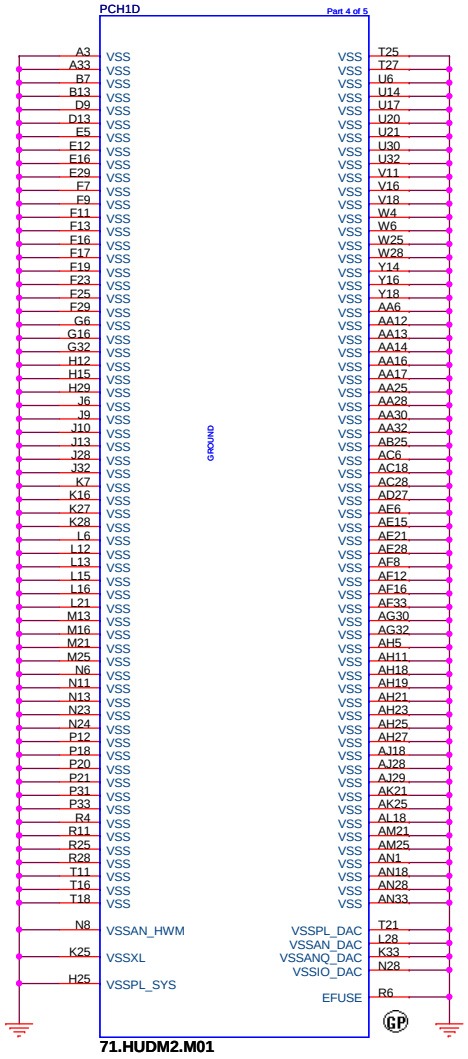
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HUDSON-M2(5/6)

Size: A3 | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 21 of 102



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *HUDSON-M2(6/6)*

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 22 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 23 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 24 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 25 of 102

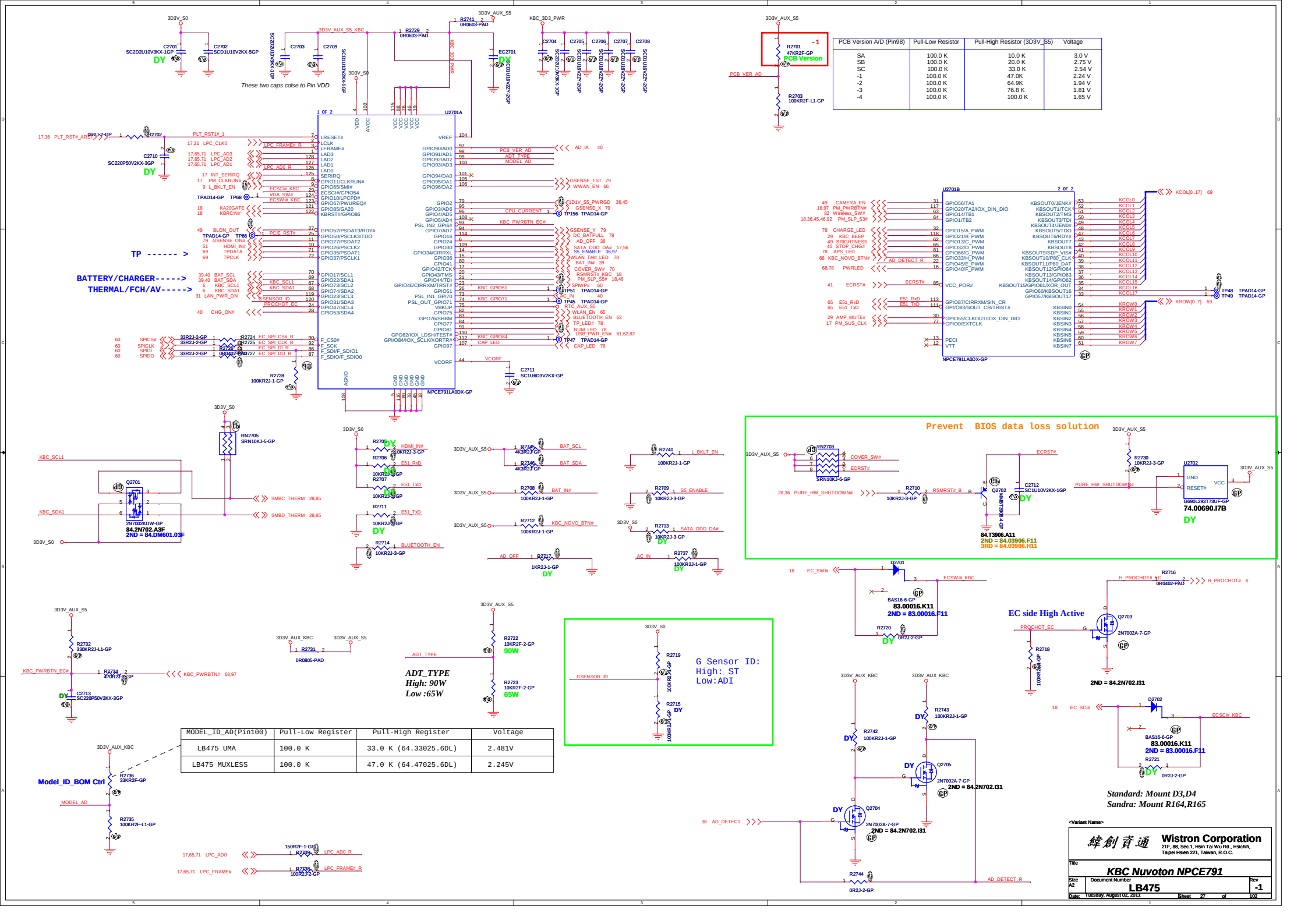
(Blanking)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 26 of 102	



PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.54 V
-1	100.0 K	47.0K	2.24 V
-2	100.0 K	64.9K	1.94 V
-3	100.0 K	76.8 K	1.81 V
-4	100.0 K	100.0 K	1.65 V

MODEL_ID_AD(Pin100)	Pull-Low Register	Pull-High Register	Voltage
LB475 UMA	100.0 K	33.0 K (64.33025.6DL)	2.481V
LB475 MUXLESS	100.0 K	47.0 K (64.47025.6DL)	2.245V

SSID = Thermal

Thermal sensor

Close to FCH on top side.

SA 0905 change to 390p

3

C2800 SC390P50V2KX-GP

Q6 MMBT3904WT1G-GP

2200p close to smsc2103 chip

REMOTE2-

REMOTE2+

2

C2801 SC390P50V2KX-GP DY

C2802 SC2200P50V2KX-2GP

Q42 MMBT3904WT1G-GP

between CPU, VGA and DIMM on bottom side

T8

1

2200p close to smsc2103 chip

H_THERMDA

C2803 SC2200P50V2KX-2GP

H_THERMDC

Q9 MMBT3904WT1G-GP

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

4 WIRE PWM Fan Control circuit

Close to connector

5V_S0

D2801 CH551H-30PT-GP

83.R5003.C8F

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

DY

C2806 SC4D7U6D3V3KX-GP

R2806 10KR2J-3-GP

AFTP2801

FAN1

FAN_PWM

FAN_TACH

R427 0R0402-PAD

FAN_PWM_C

EC2801 SC1K5P50V2KX-1GP DY

EC2802 SC1K5P50V2KX-1GP

ACES-CON4-GP-U1

20.F0714.004

2nd = 20.D0196.104

FAN_TACH

FAN_PWM_C

AFTP2802

AFTP2803

3D3V_S0

R2800 6K8R2J-GP

SHDN_SEL

SHDN --> 2N3904 ON External diode

3D3V_S0

R260 68R2-GP

C2804

2103_VDD

SCD1U10V2KX-4GP

U2801

H_THERMDA

H_THERMDC

REMOTE2+

REMOTE2-

THERM_SCI#

TP69 TPAD14-GP

R272 0R0402-PAD

THERM_SYS_SHDN#

THERM_SCI# R

27,85 SMBC_THERM

27,85 SMBD_THERM

VDD

DP1

DN1

DP2/DN3

ND2/DP3

SYS_SHDN#

ALERT#

SMCLK

SMDATA

GPIO1

GPIO2

TACH

PWM

TRIP_SET

SHDN_SEL

GND

GND

2103_4

2103_5

TP65 TPAD14-GP

TP67 TPAD14-GP

FAN_TACH_R

TRIP_SET

SHDN_SEL

R2805 604R2F-2-GP

T8 = 105

EMC2103-2-AP-GP

RN49

SRN10KJ-5-GP

3D3V_S0

D2802

FAN_TACH

FAN_PWM

CH551H-30PT-GP

2ND = 83.5R003.08F

83.R5003.C8F

pin6, ALERT# OD

pin7, SYS_SHDN# OD

3D3V_AUX_S5

D2803 BAT54PT-GP

83.00054.T81

DY

2ND = 84.2N702.031

84.2N702.J31

2N7002K-2-GP

2ND = 83.BAT54.D81

3rd = 83.BAT54.S81

27,36 PURE_HW_SHUTDOWN#

R2801 10KR2J-3-GP DY

C2805 SCD1U10V2KX-4GP DY

Q2802

THERM_SYS_SHDN#

R2802 100KR2J-1-GP

3D3V_S0

<Variant Name>

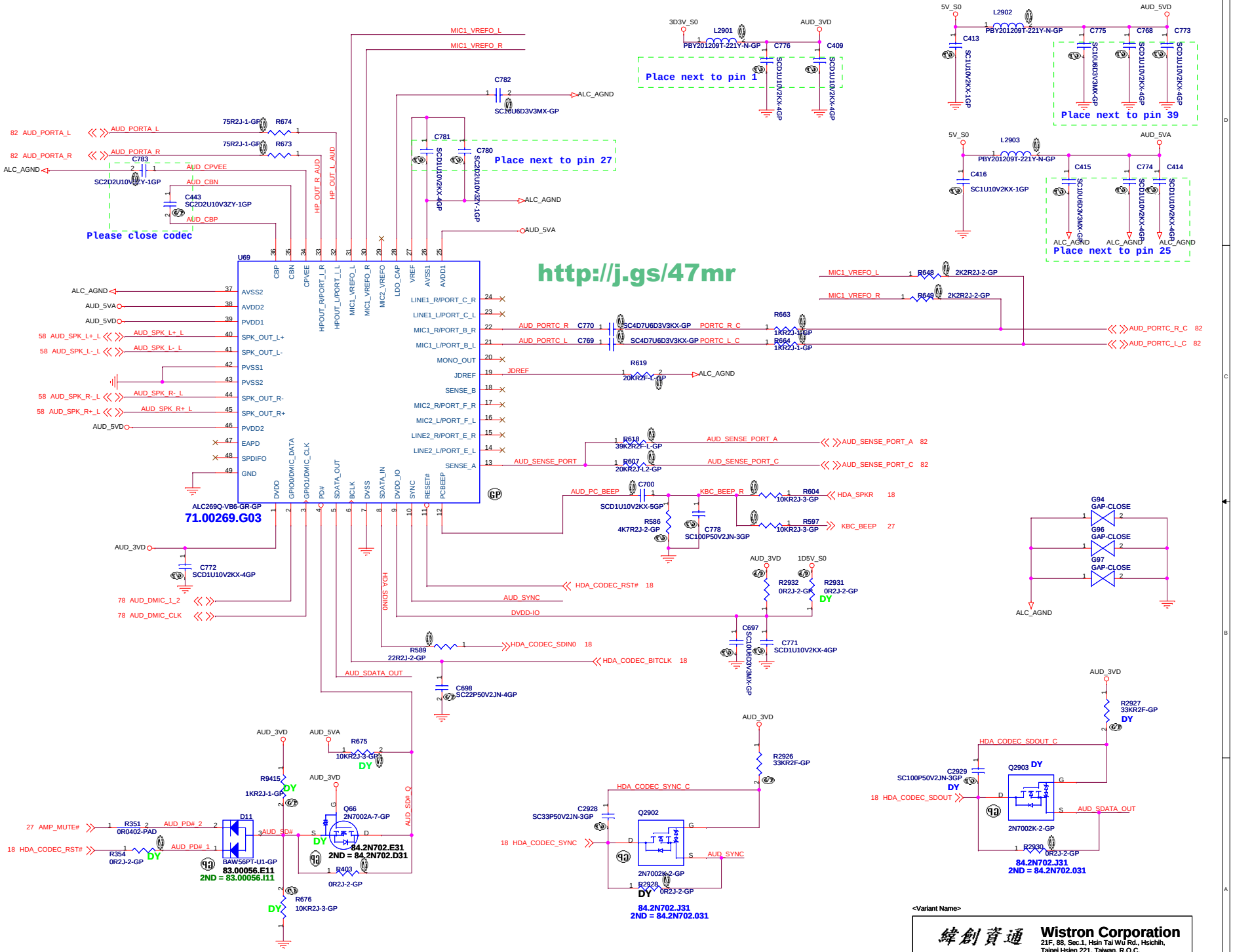
緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal EMC2103

Size: A3 | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 28 of 102



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC_ALC272&G1454

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 29 of 102

(Blanking)

<Variant Name>

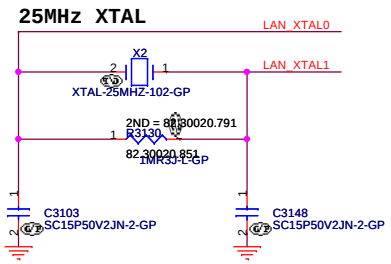
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

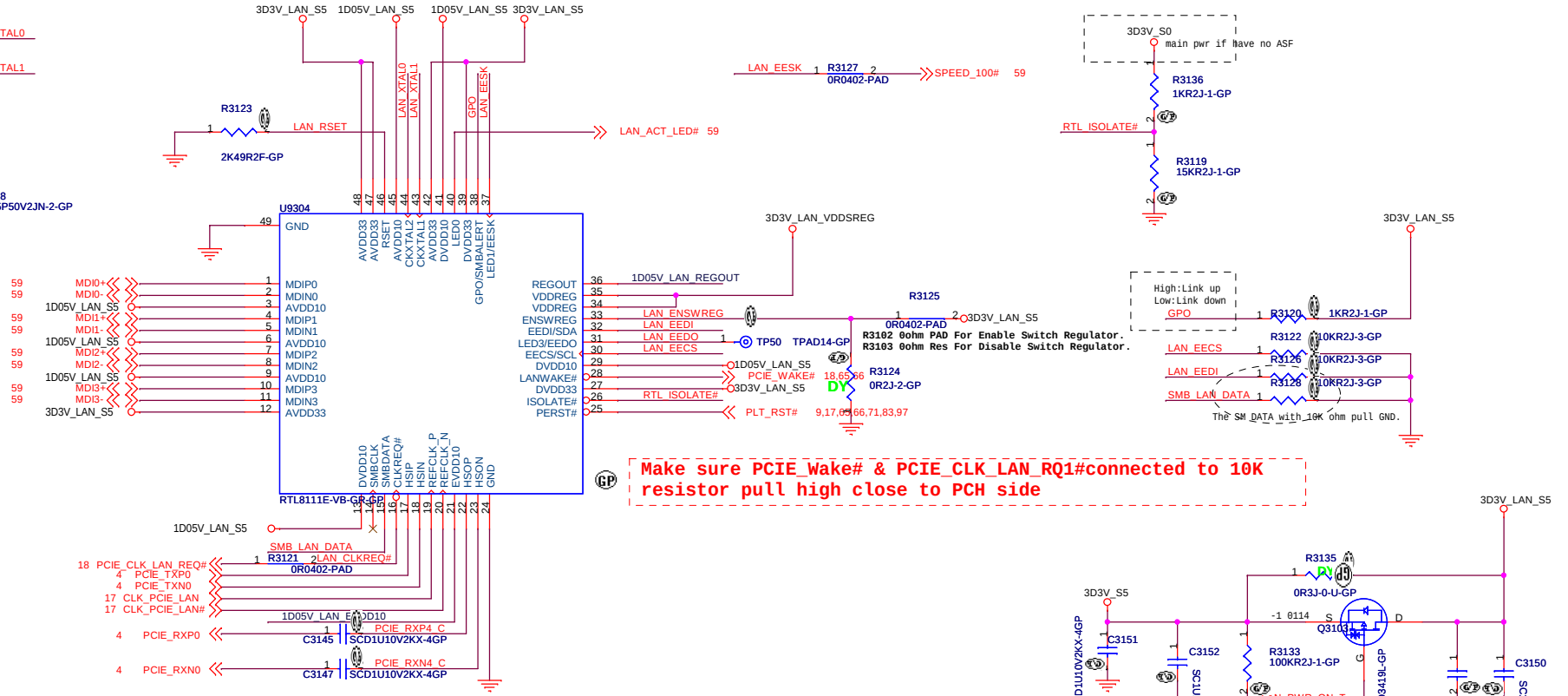
Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 30 of 102

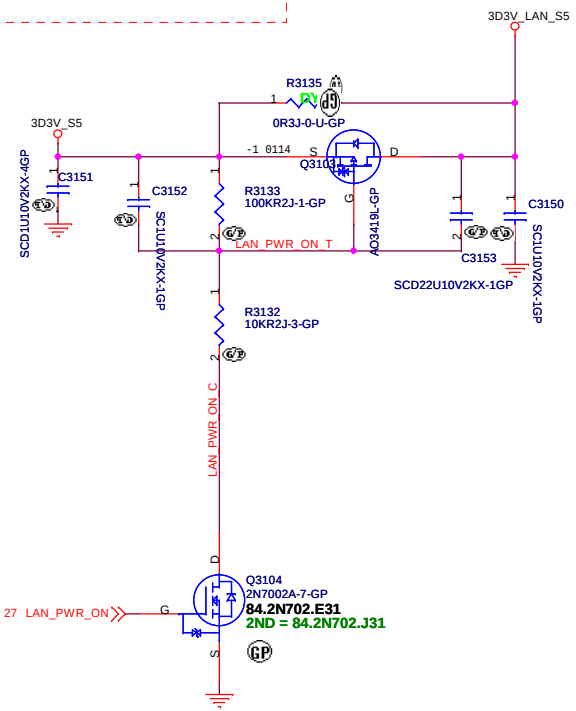
25MHz XTAL

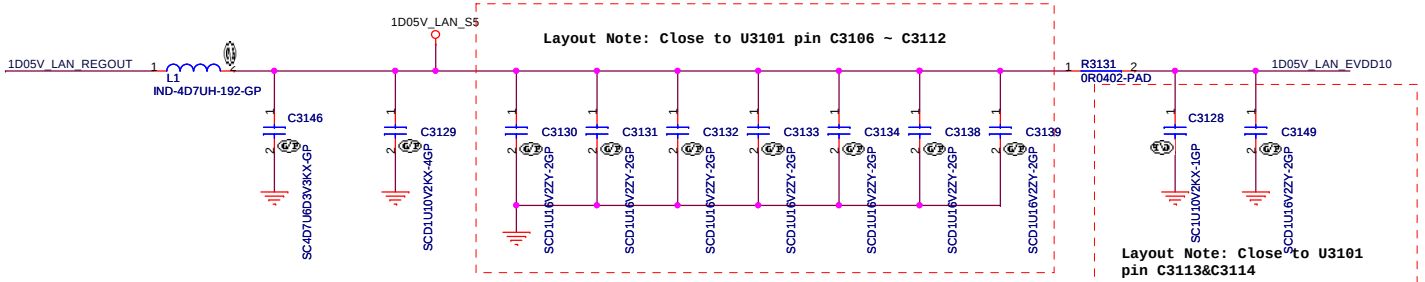


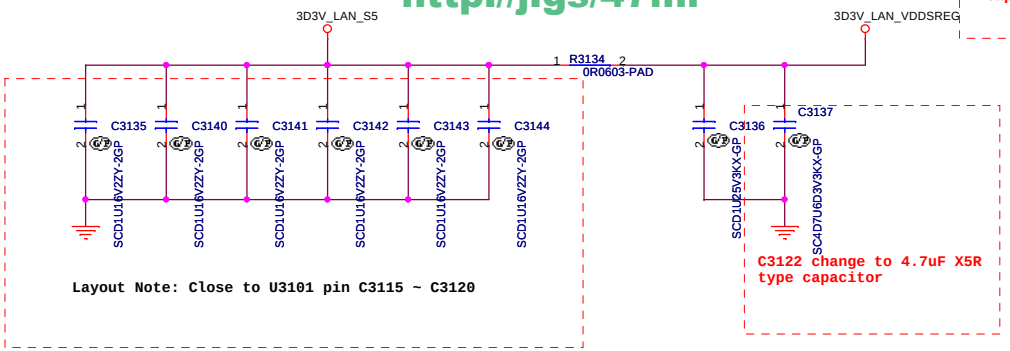
Pin-XTAL2 is External Clock Input Pin.
R3121 is need when using external clock source.



Make sure PCIE_Wake# & PCIE_CLK_LAN_RQ1#connected to 10K resistor pull high close to PCH side







<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LOM		
Size: A3	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 31 of 102	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A3	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 32 of 102	

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 33 of 102

(Blanking)

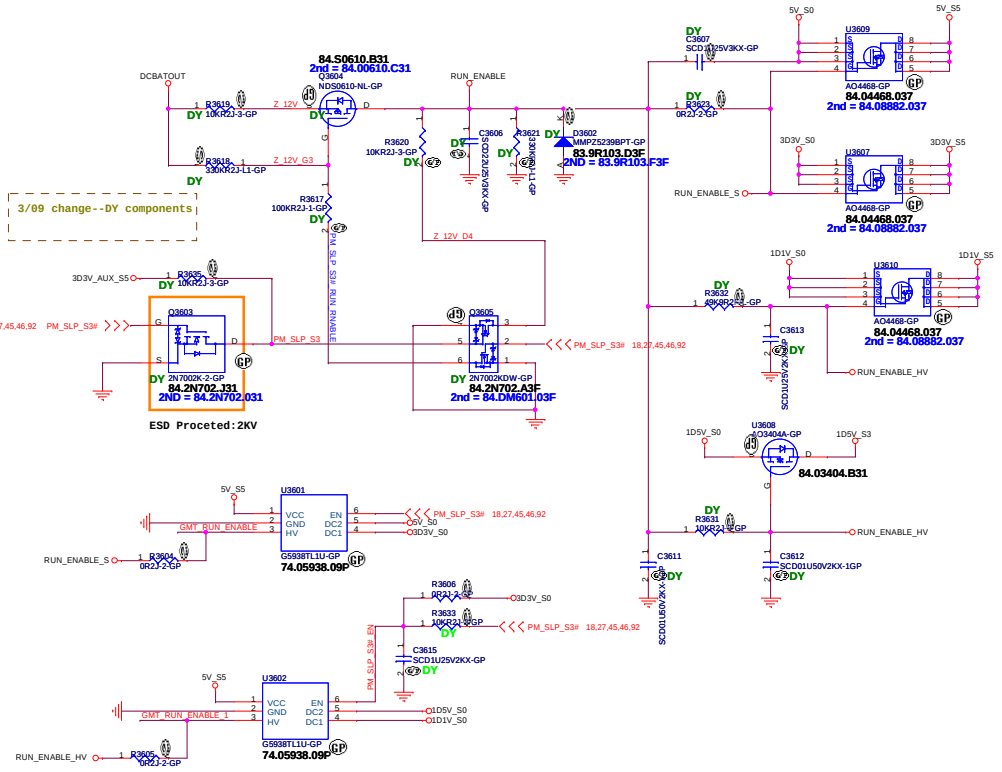
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 34 of 102	

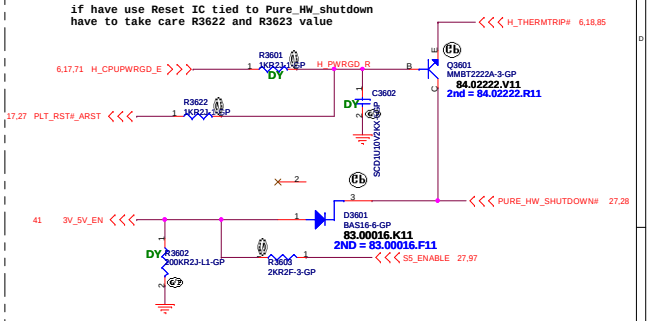
(Blanking)

<Variant Name>

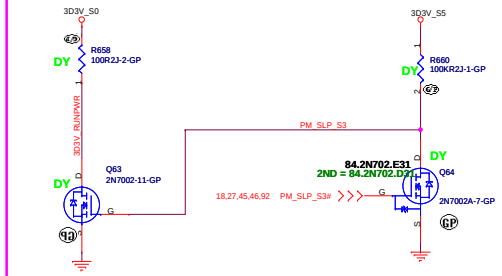
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 35 of 102	



if have use Reset IC tied to Pure_HW_shutdown
have to take care R3622 and R3623 value

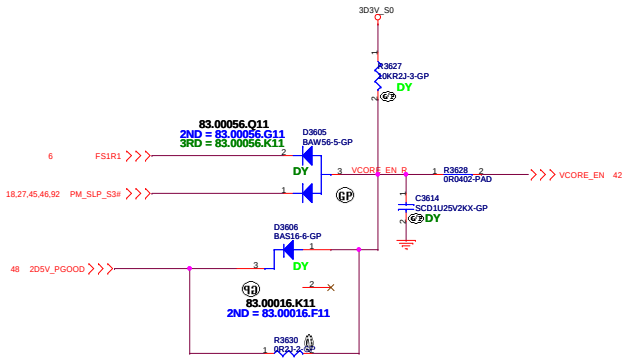


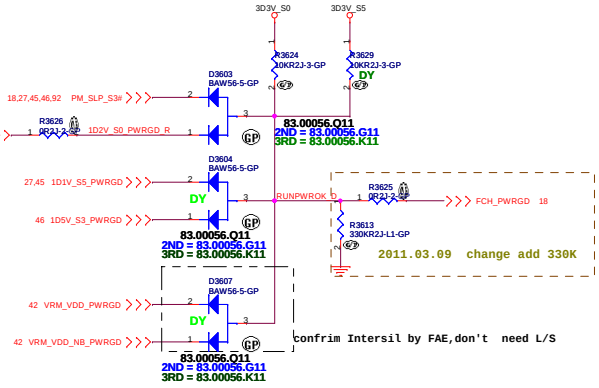
For Discharge



2011.04.16 Add 3D3V_S0 Discharge circuit

Power Sequence





<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Power On Logic***	
Size: Custom	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 36 of 102	

(Blanking)

<Variant Name>

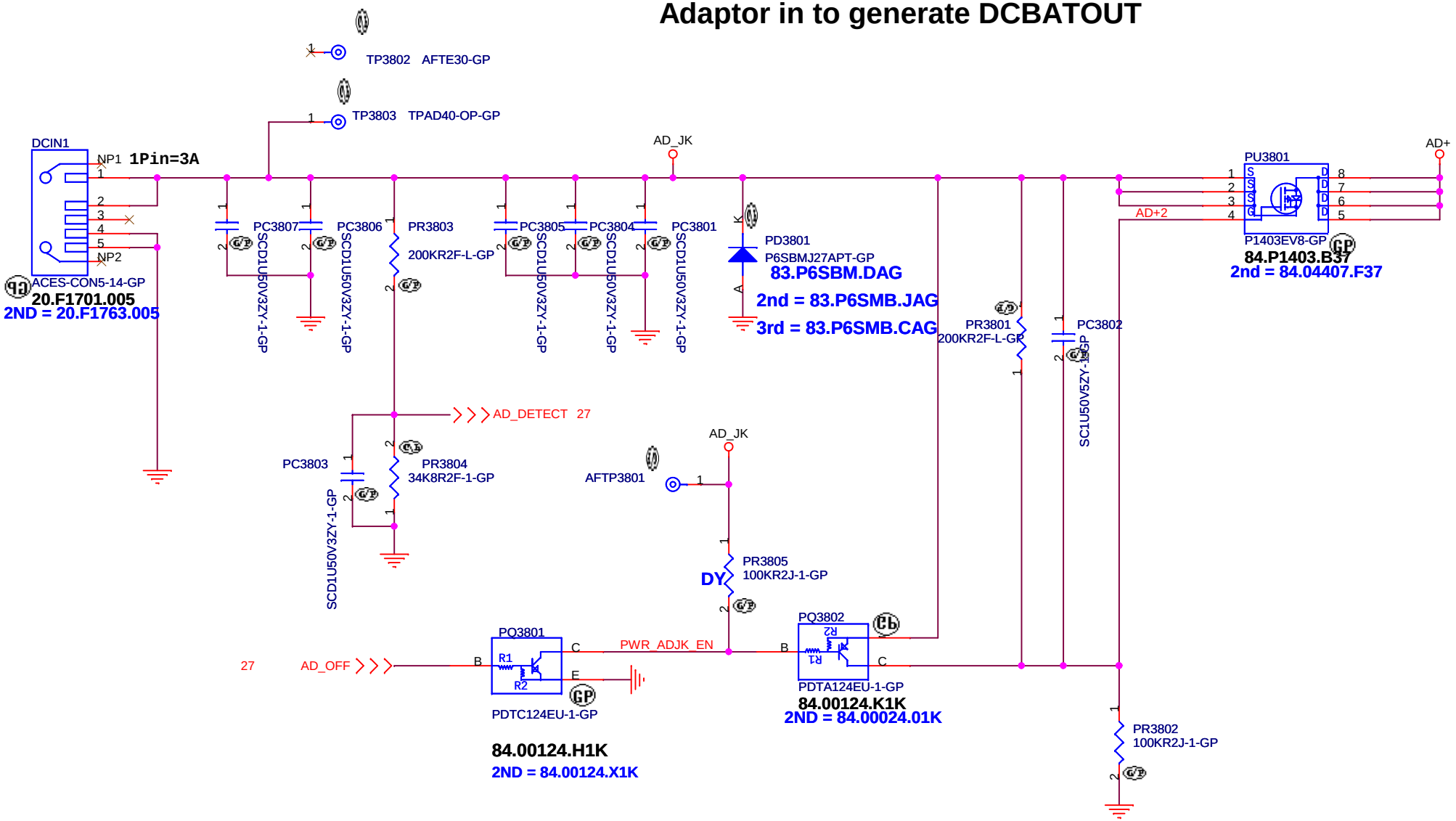
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 37 of 102

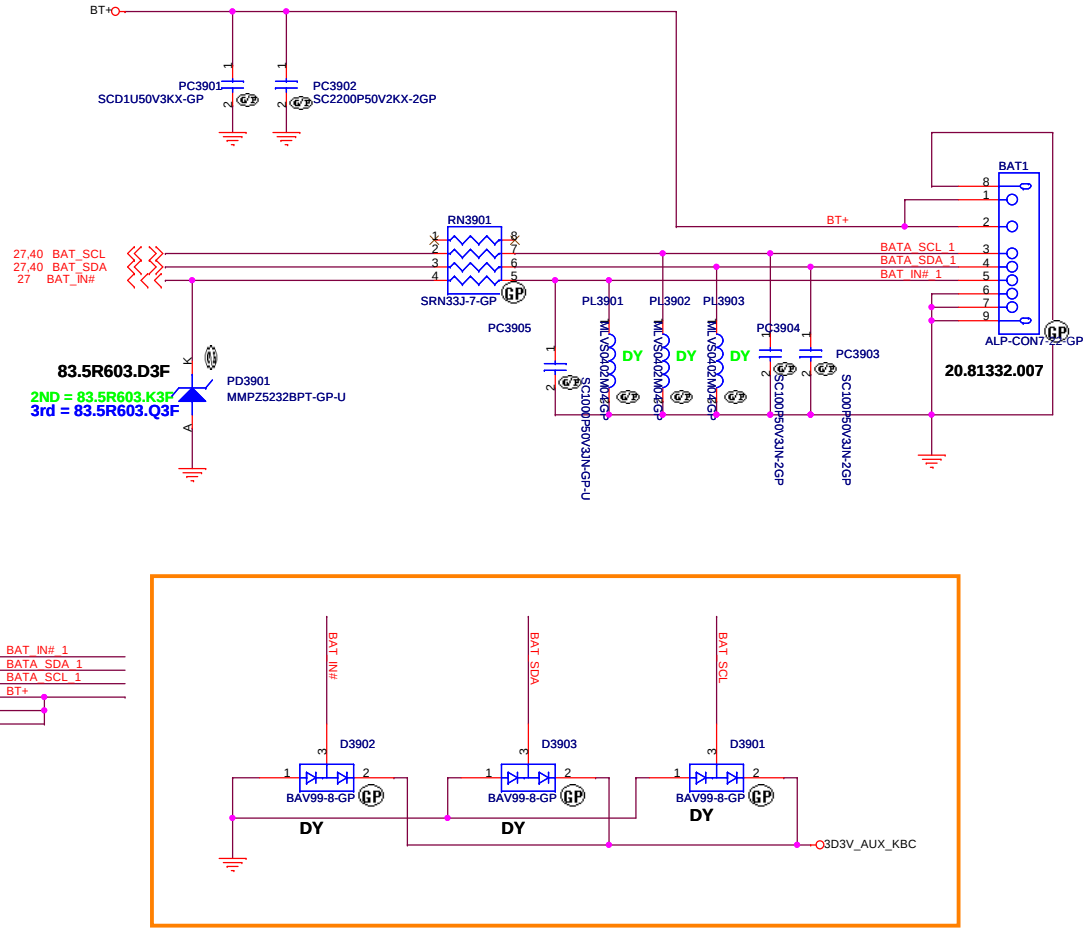
Adaptor in to generate DCBATOUT

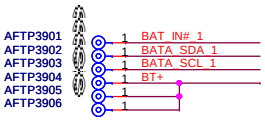


<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DCIN_JACK***
Size: A4	Document Number: **LB475**
Rev: **-1**	
Date: Tuesday, August 02, 2011	Sheet 38 of 102

BATTERY CONNECTOR





<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***BATT_CONN***
Size A3 / Document Number	**LB475** / Rev **-1**
Date: Tuesday, August 02, 2011	Sheet 39 of 102

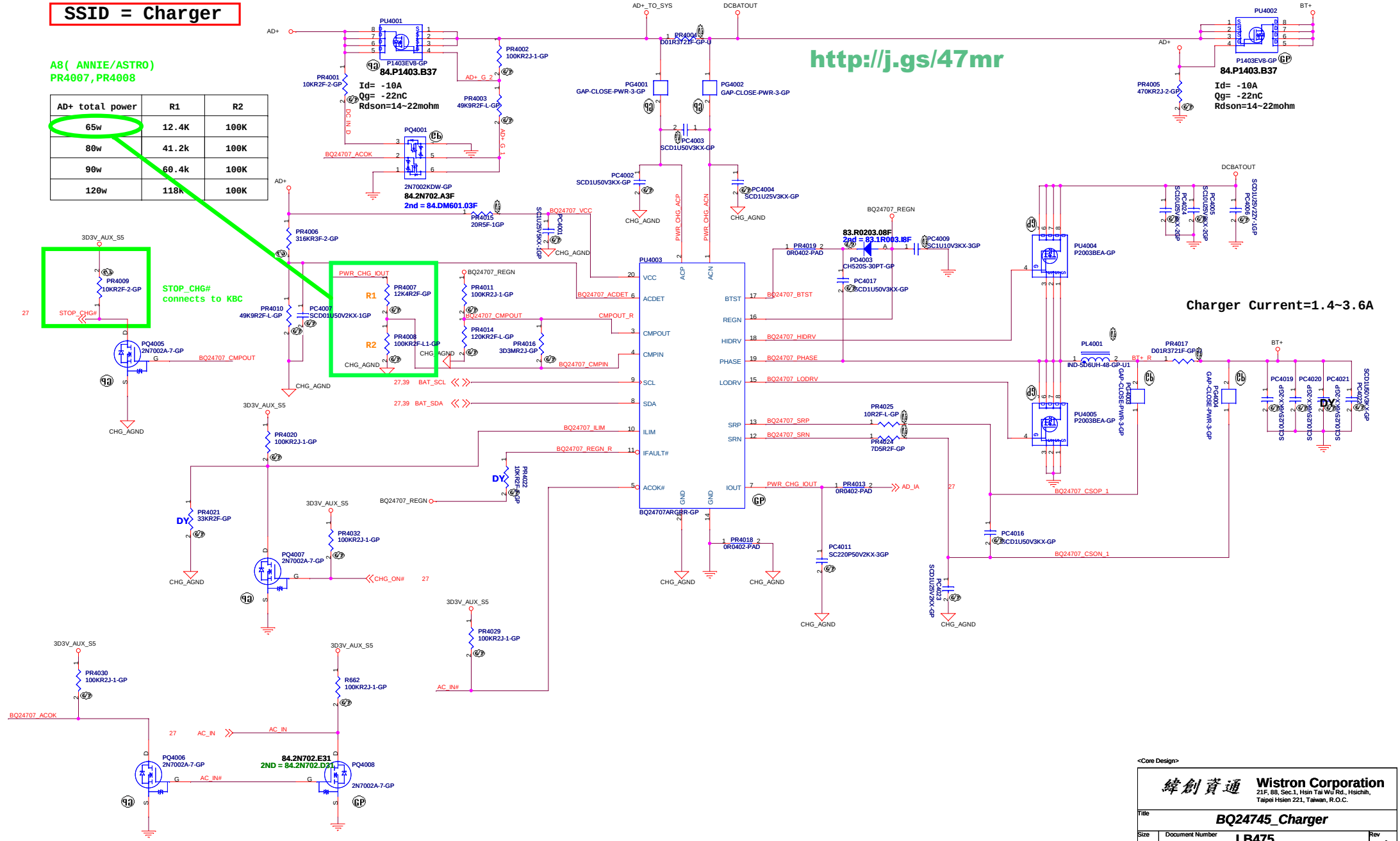
SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K

http://j.gs/47mr

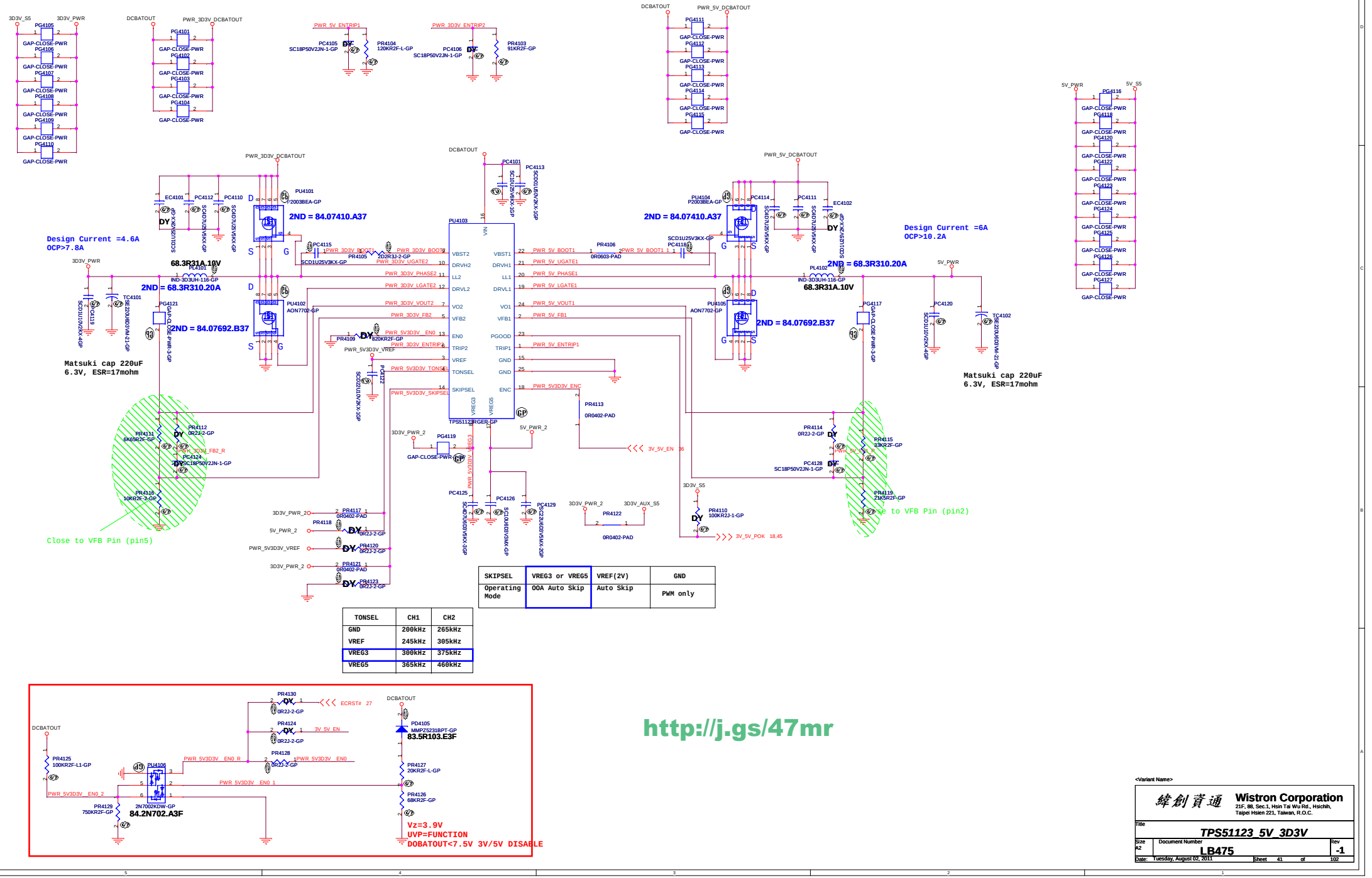
Charger Current=1.4~3.6A



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BQ24745_Charger		
Size	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 40 of 102	

SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

http://j.gs/47mr

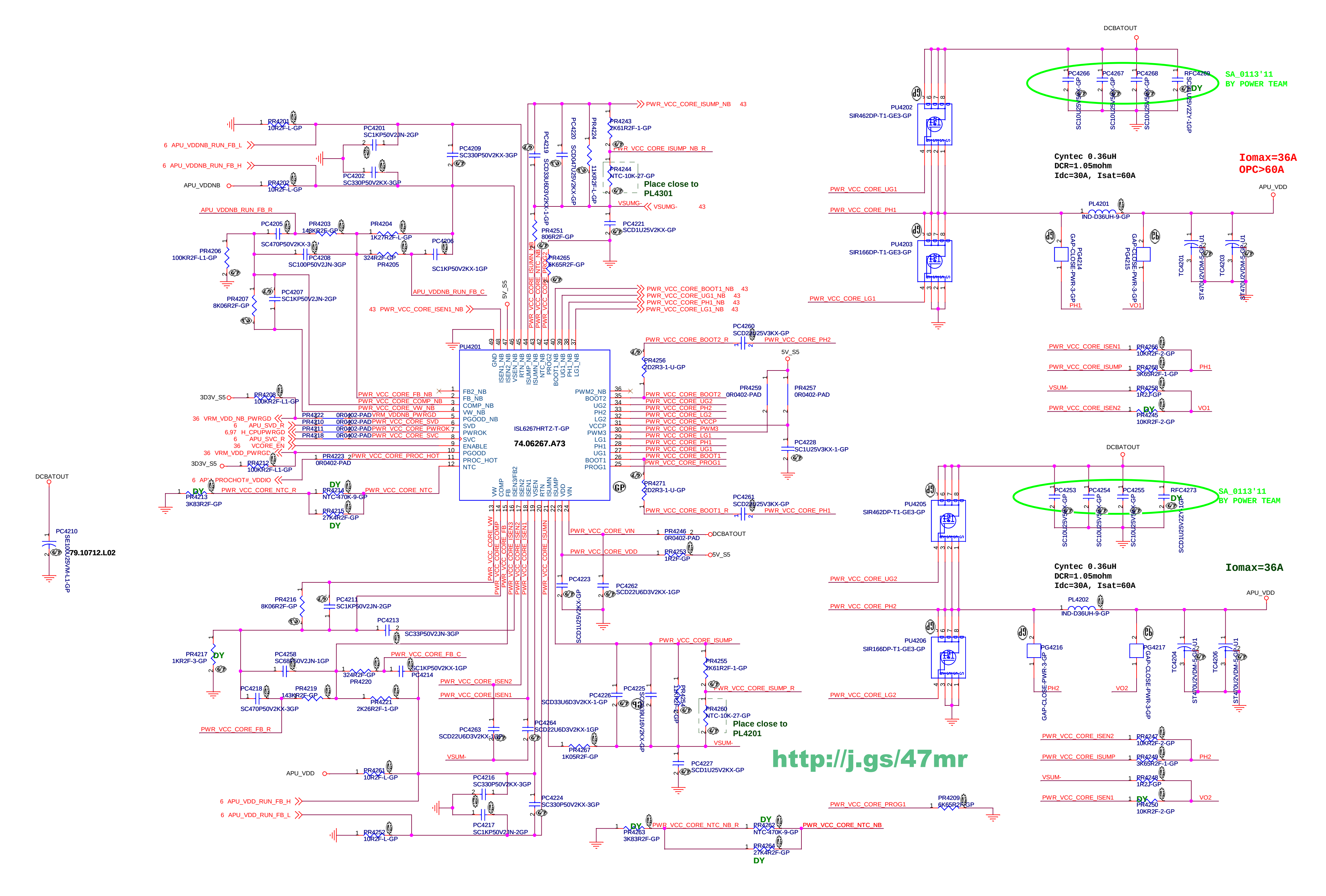
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123_5V_3D3V

Size: A2 | Document Number: LB475 | Rev: -1

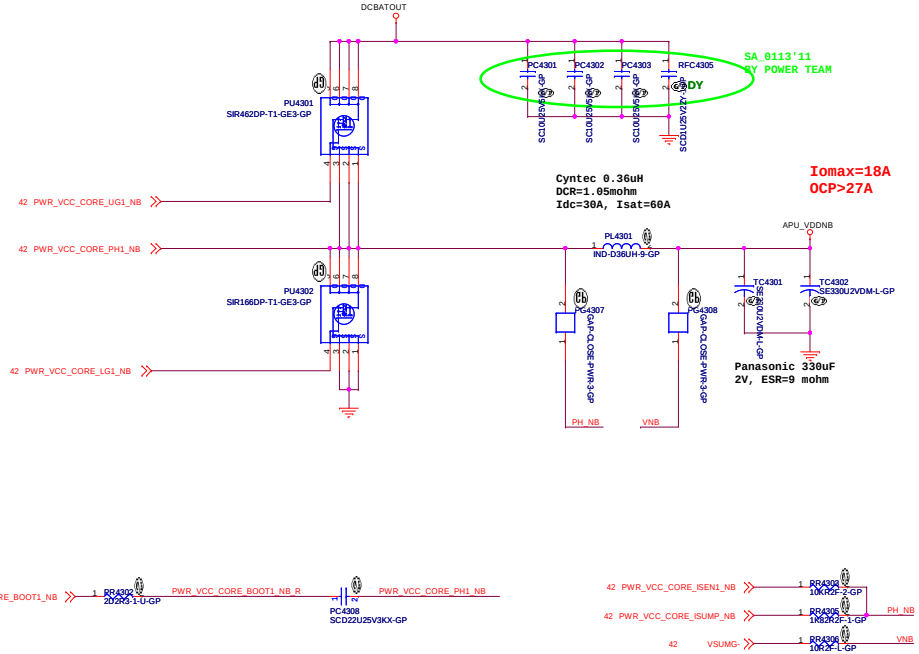
Date: Tuesday, August 02, 2011 | Sheet 41 of 102



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL6267_VDD_CORE	
Size: Custom	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 42 of 102	



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*ISL6267_VDDNB*
Size: A2	Document Number: LB475
Rev: -1	
Date: Tuesday, August 02, 2011	Sheet 43 of 102

(Blanking)

<Variant Name>

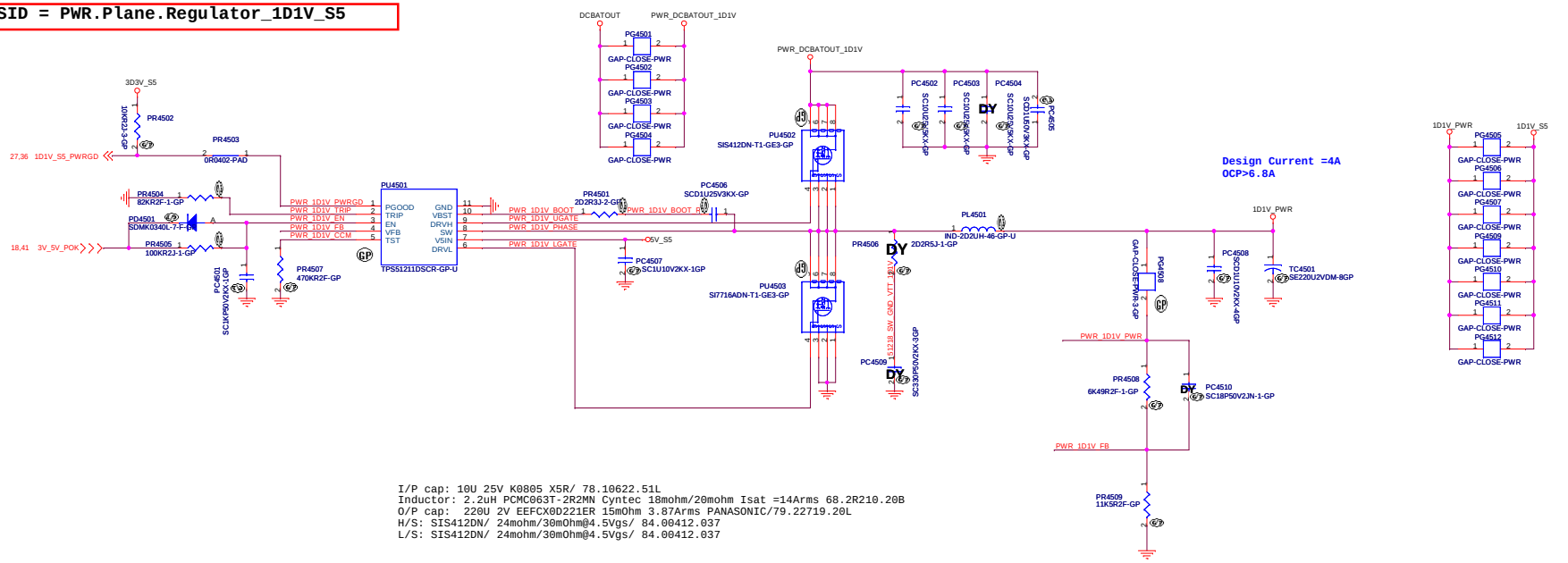
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 44 of 102

SSID = PWR.Plane.Regulator_1D1V_S5

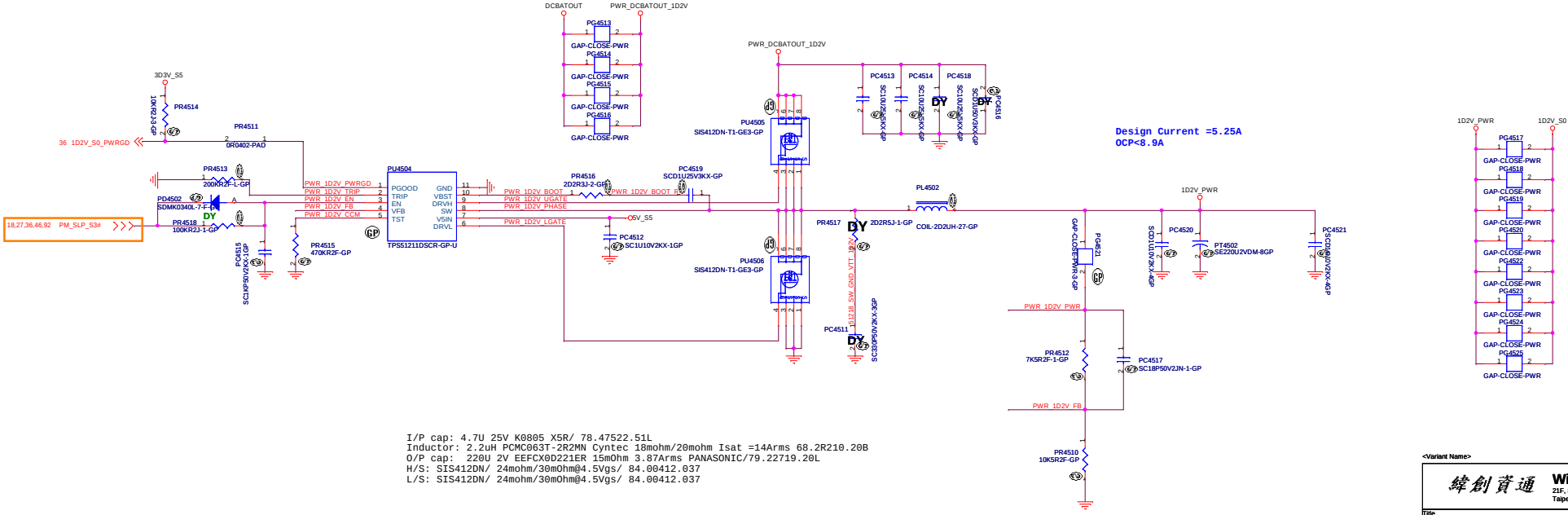


Design Current =4A
OCP>6.8A

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2

SSID = PWR.Plane.Regulator_1D2V_S0



Design Current =5.25A
OCP<8.9A

I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 3.87Arms PANASONIC/79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037

Vout=0.704V*(R1+R2)/R2

<Variant Name>

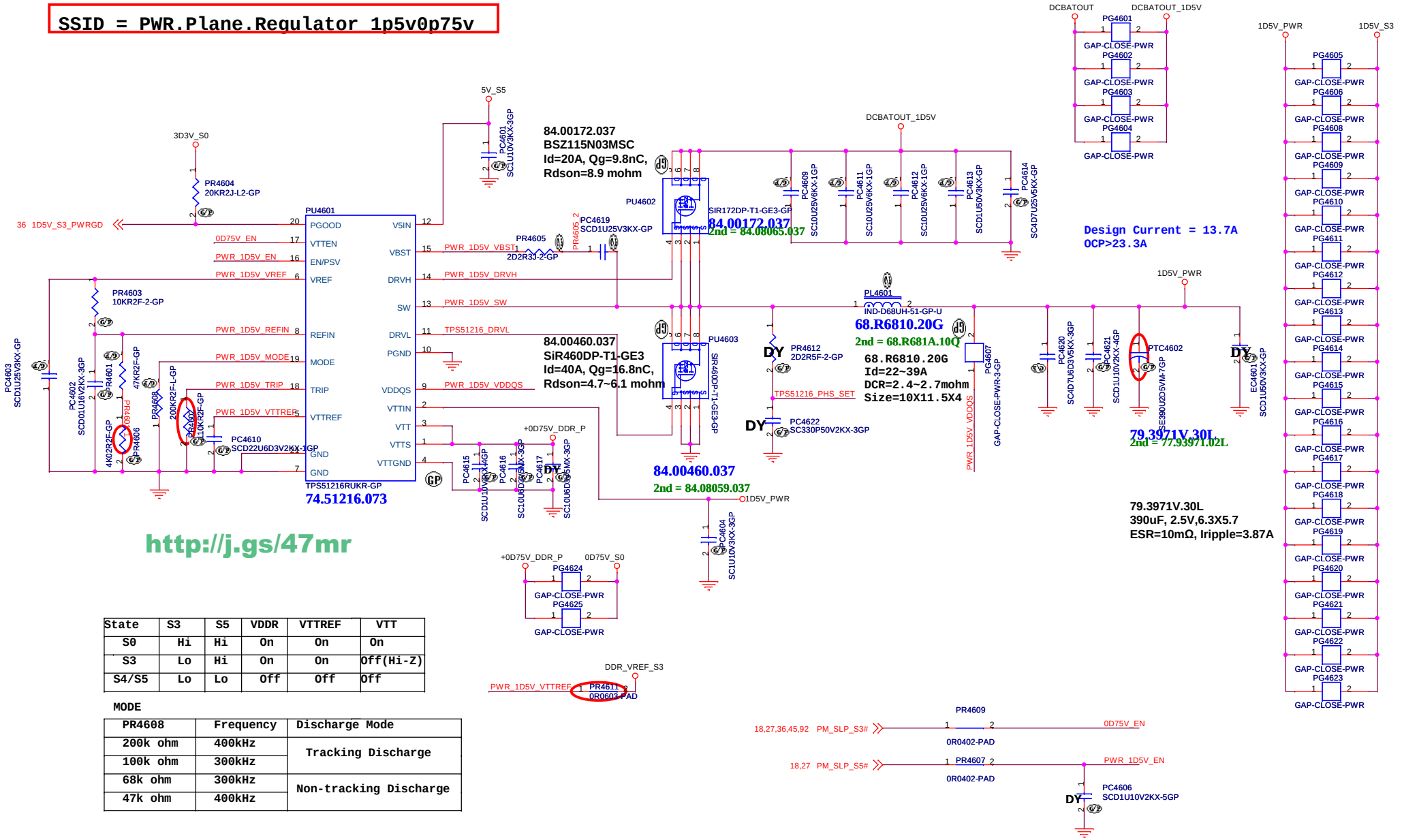
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TPS51211_1D1V_1D2V*

Size	Document Number	Rev
A2	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 45 of 102

SSID = PWR.Plane.Regulator 1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: 1D5V&0D75V

Size: Custom | Document Number: LB475 | Rev: -1

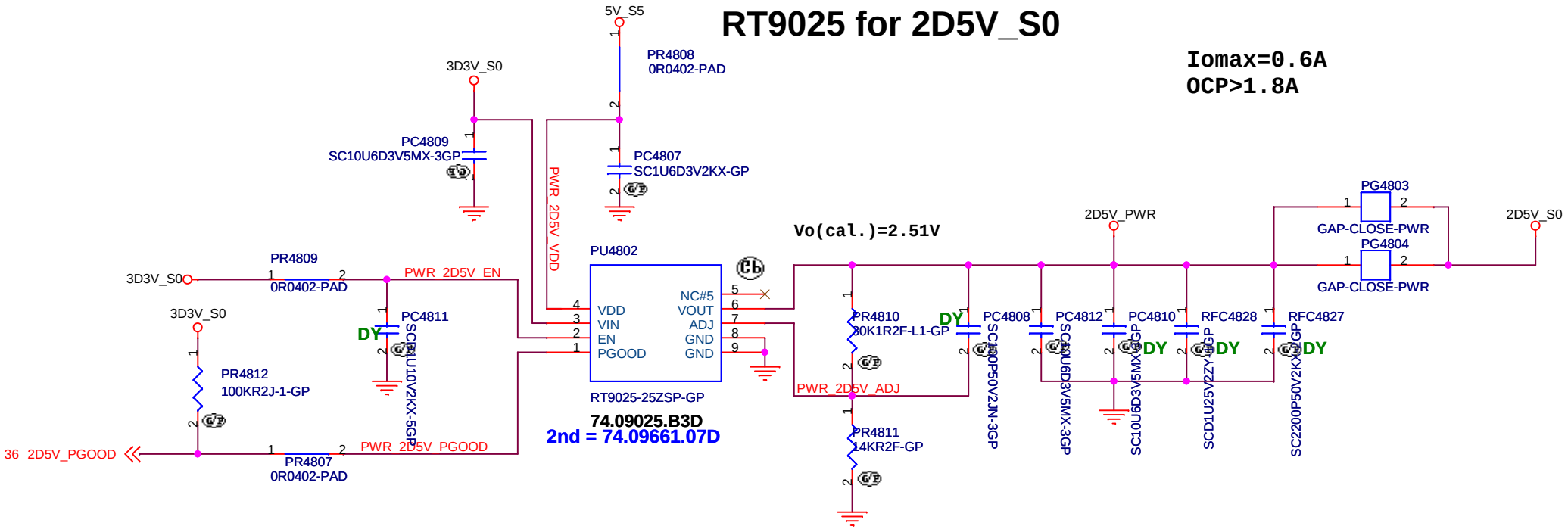
Date: Tuesday, August 02, 2011 | Sheet 46 of 102

(Blanking)

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 47 of 102	

RT9025 for 2D5V_S0

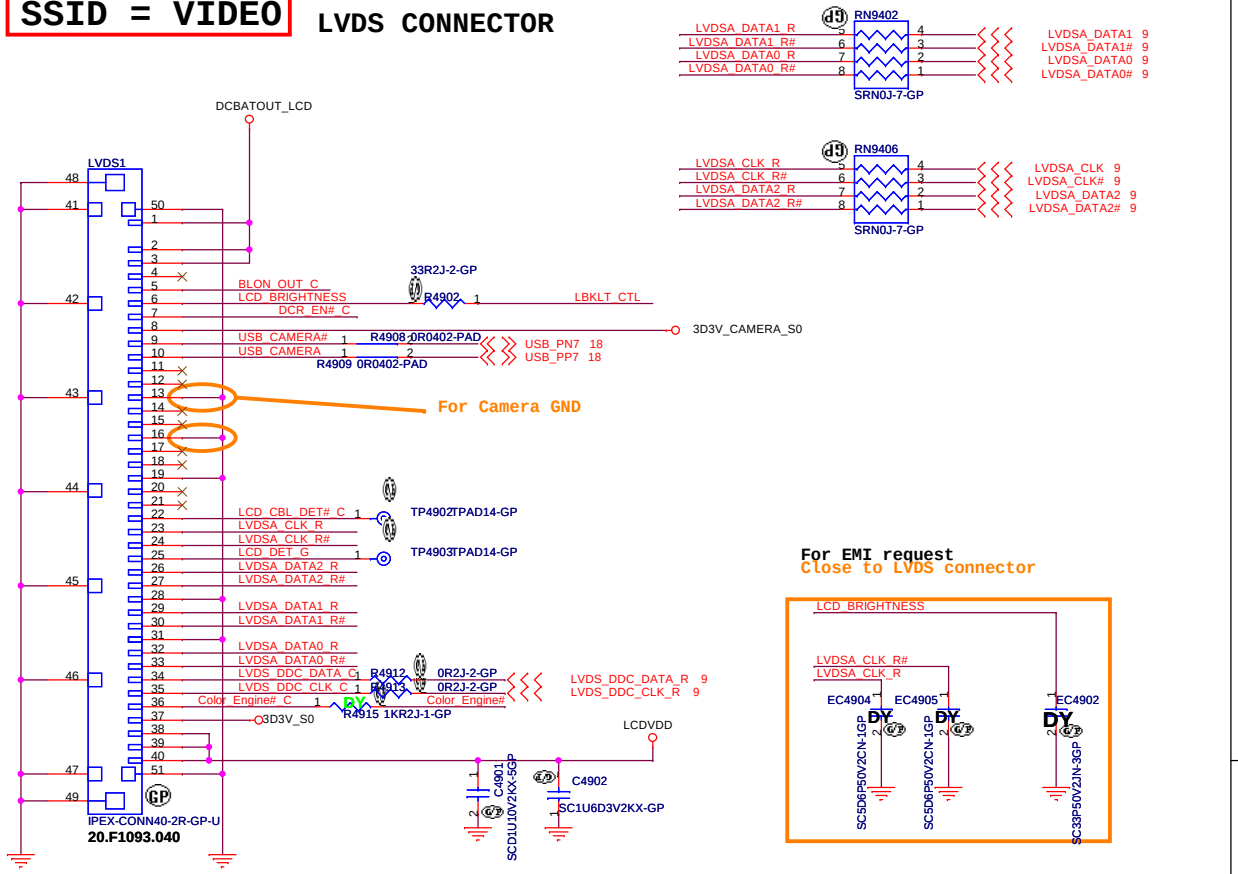


<Variant Name>

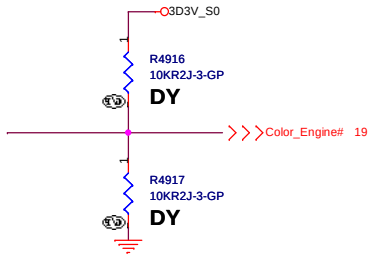
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *RT9025(2D5V_S0)*		
Size: A4	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 48 of 102	

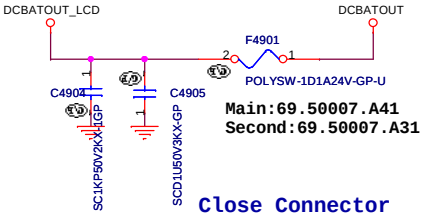
SSID = VIDEO

LVDS CONNECTOR

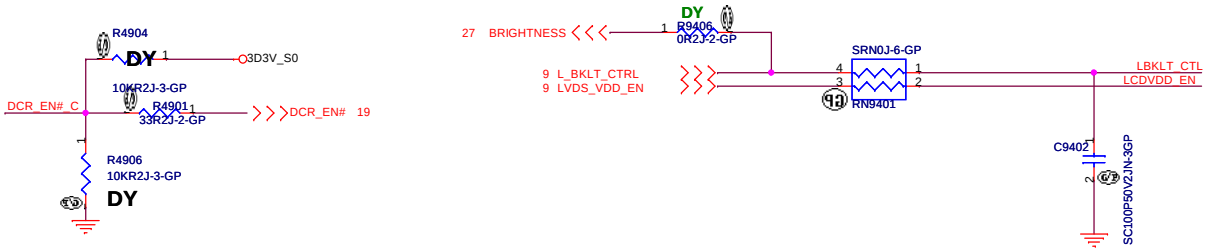


For EMI request
Close to LVDS connector

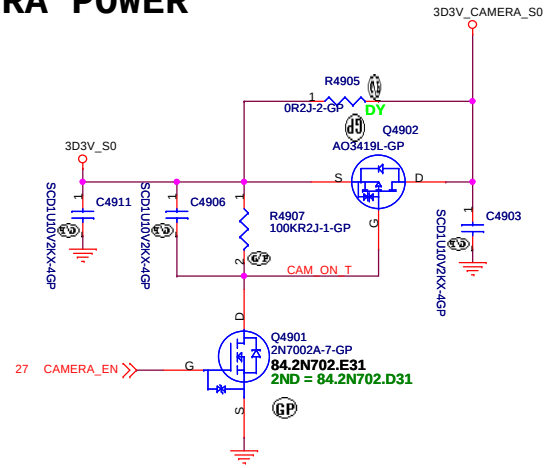




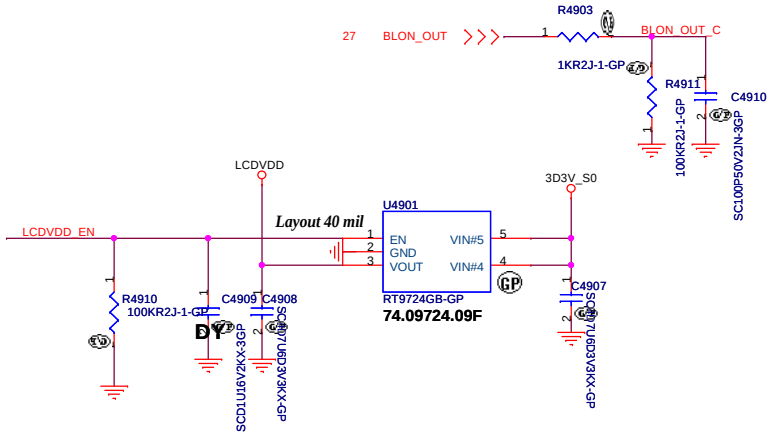
Panel BL brightness/Power En/BL En



CAMERA POWER



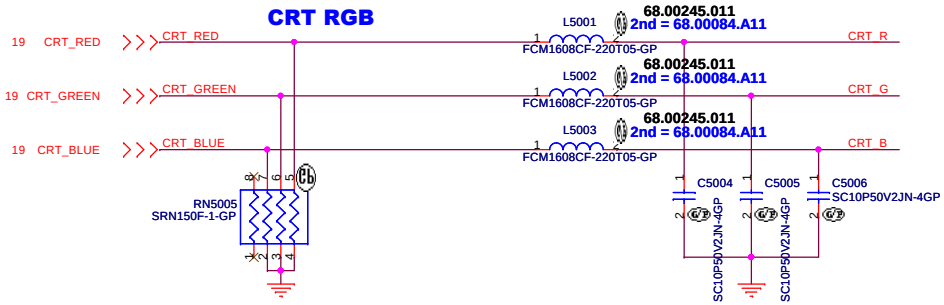
SSID = VIDEO

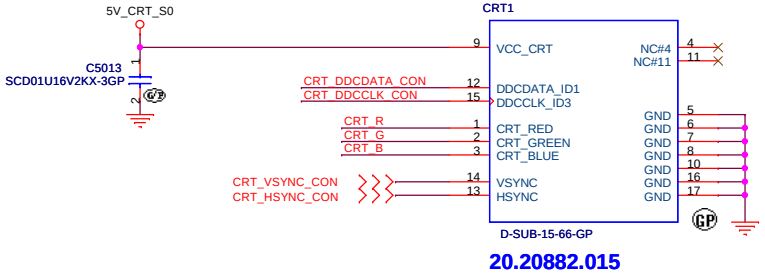


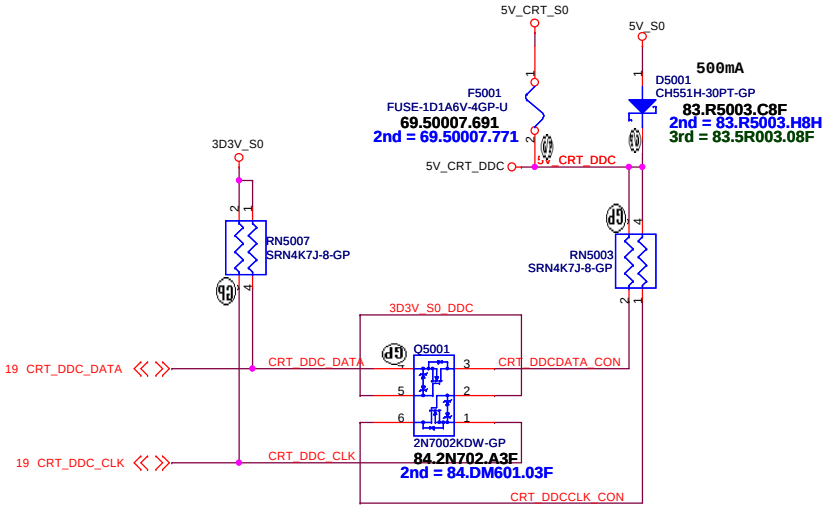
<Variant Name>

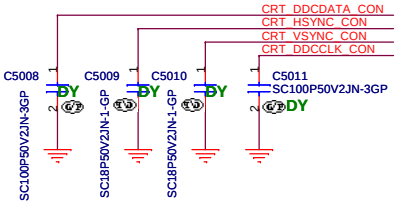
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

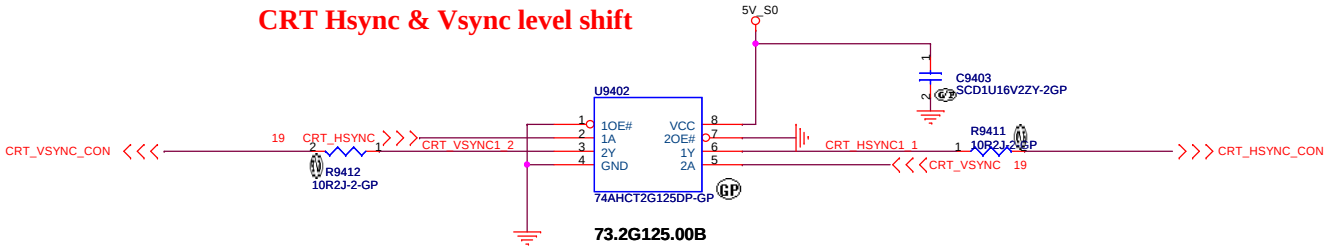
Title	LCD/Inverter Connector	
Size A3	Document Number LB475	Rev -1
Date: Tuesday, August 02, 2011	Sheet 49 of 102	











<variant_name>

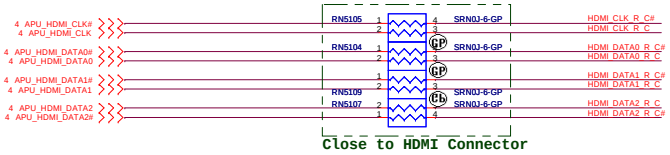
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

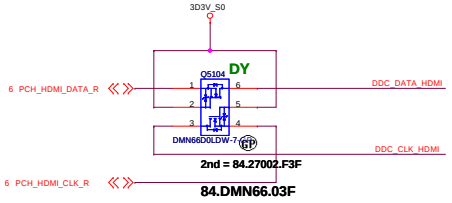
Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 50 of 102

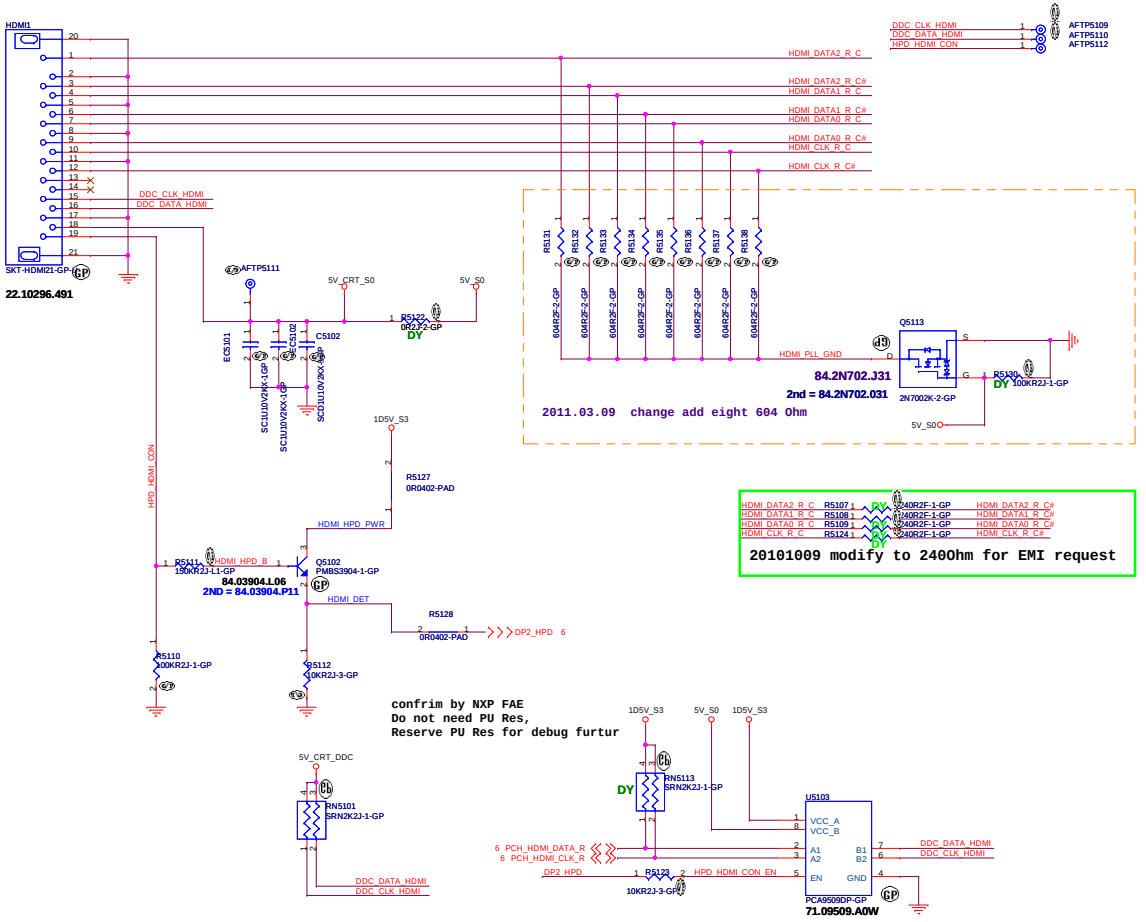
HDMI Level Shifter & CONNECTOR



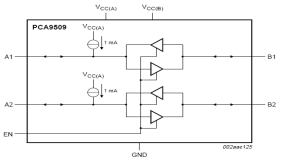
Qualify LZ57 HDMI DDC Passive Level Shifter
2011.04.20



HDMI CONN



Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up.



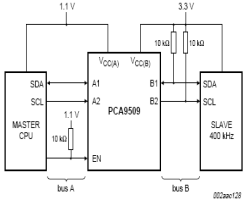
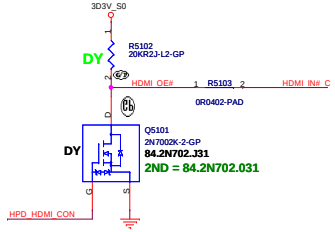


Fig 4. Typical application



<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	HDMI Level Shifter/Connector
Size A2	Document Number LB475
Rev	-1
Date: Tuesday, August 02, 2011	Sheet 51 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*		
Size: A4	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 52 of 102	

(Blanking)

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 53 of 102	

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

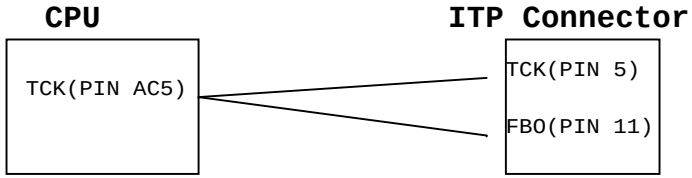
Reserved

Size	Document Number	Rev
A4	LB475	-1

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



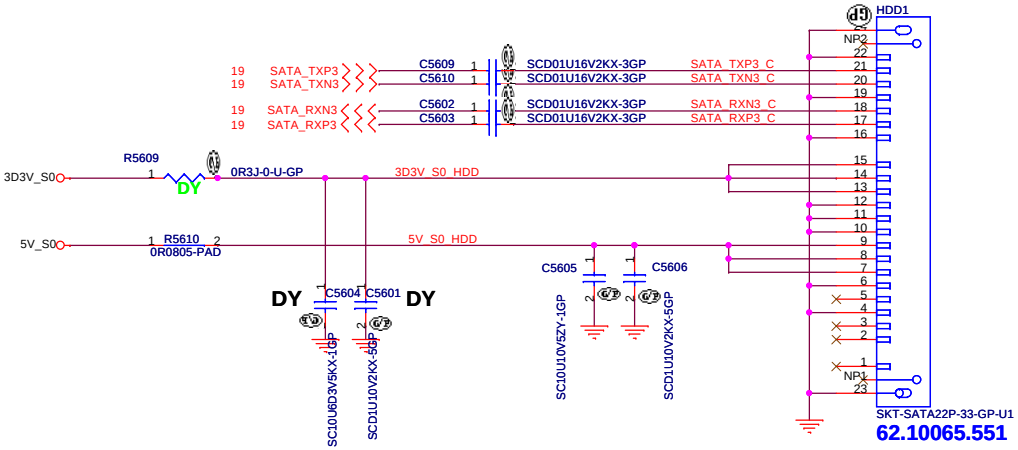
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

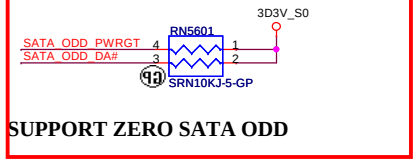
Title: *ITP*		
Size: A4	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 55 of 102	

SSID = SATA

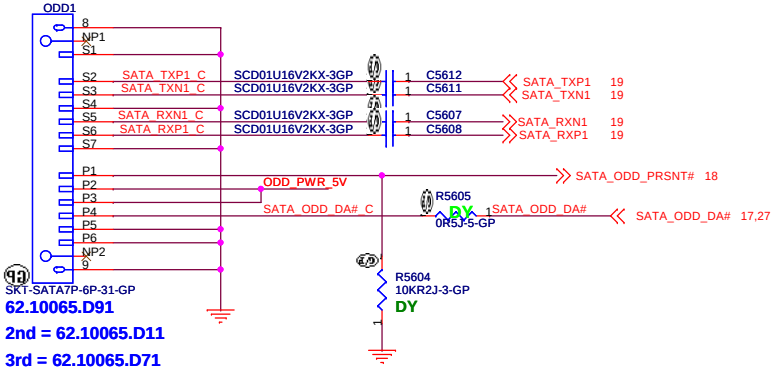
SATA HDD Connector



ODD Connector



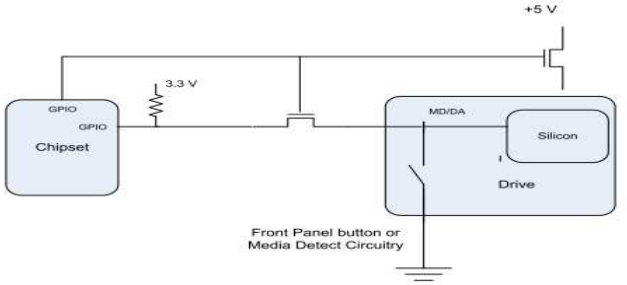
SUPPORT ZERO SATA ODD



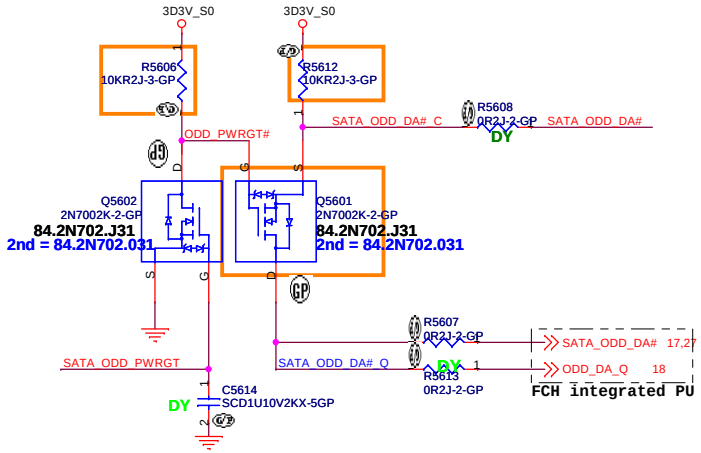
62.10065.D91

2nd = 62.10065.D11

3rd = 62.10065.D71

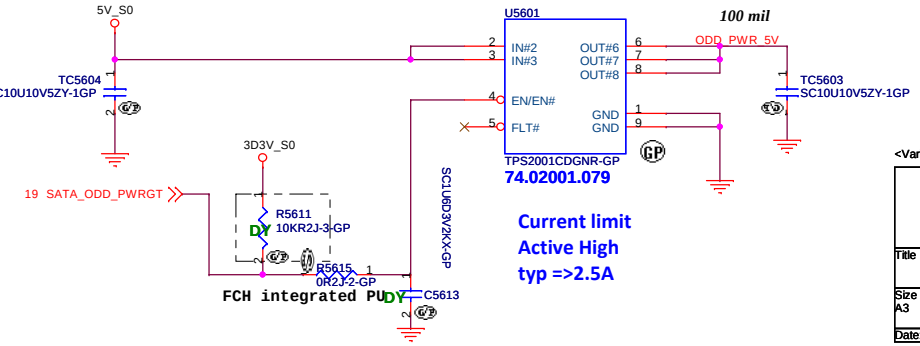


If support Zero Power ODD
Stuff R5604,R5612,Q5601 and R5613 TC5604 and U5601
DY R5603



SATA_RX- and SATA_RX+ Trace Length match within 10 mil

Following AMD routing table



Current limit
Active High
typ =>2.5A

When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

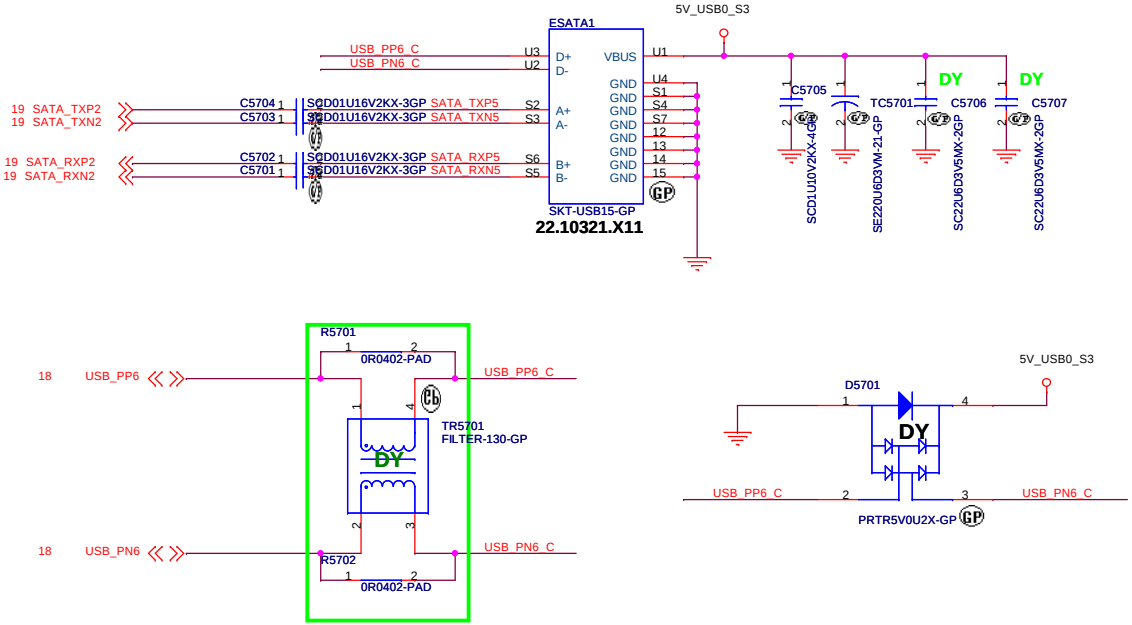
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/ODD**

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 56 of 102



<variant_name>

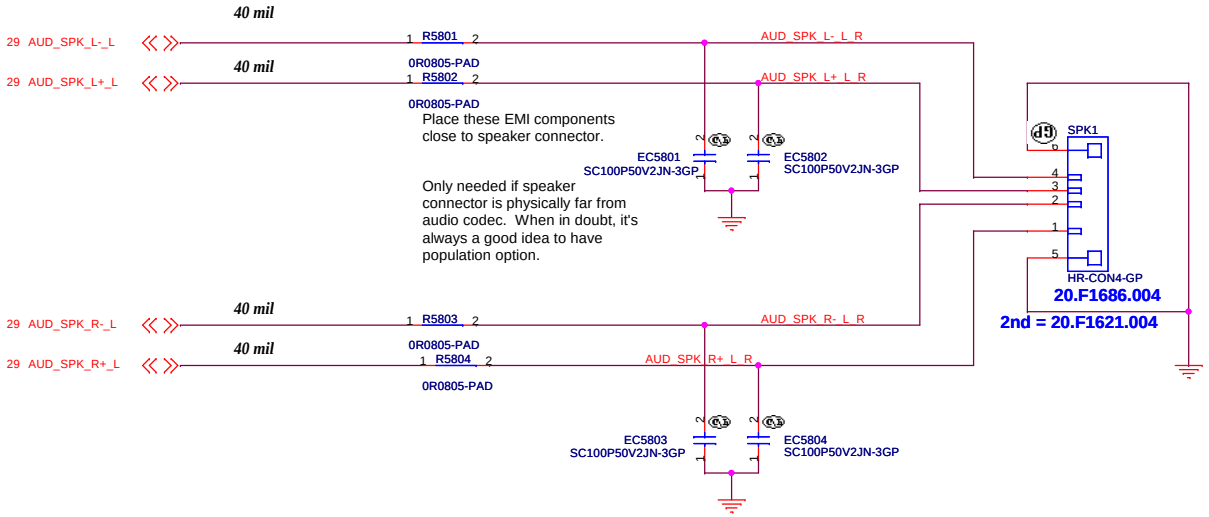
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

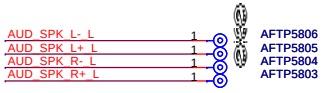
Title: ESATA/USB Charger

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 57 of 102

INTERNAL STEREO SPEAKERS

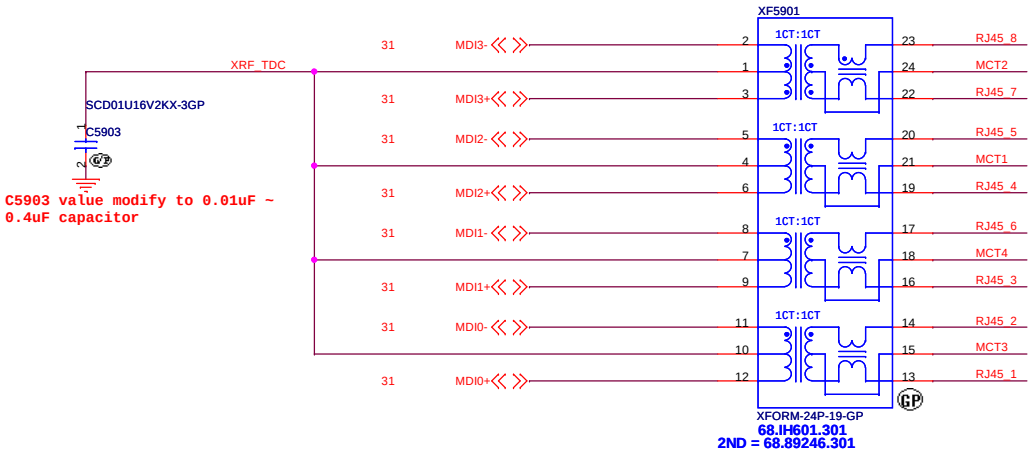


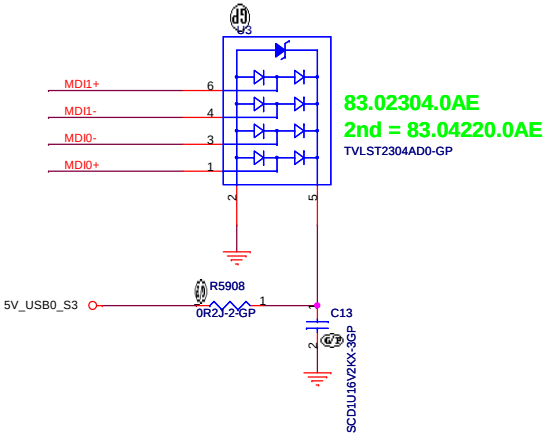


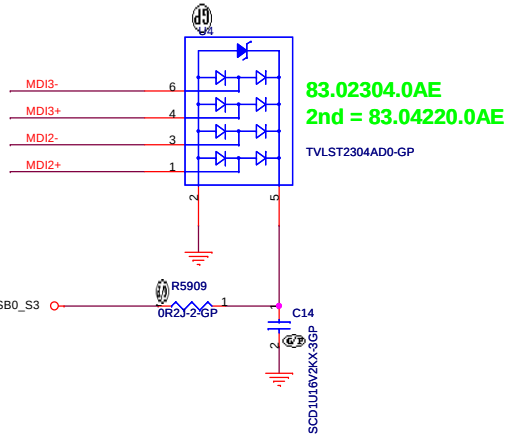
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Audio Jack***
Size A3	Document Number **LB475** Rev **-1**
Date: Tuesday, August 02, 2011	Sheet 58 of 102

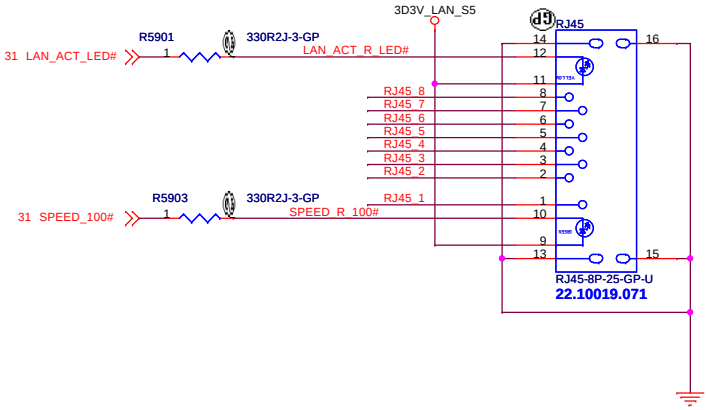
GIGA Lan Transformer

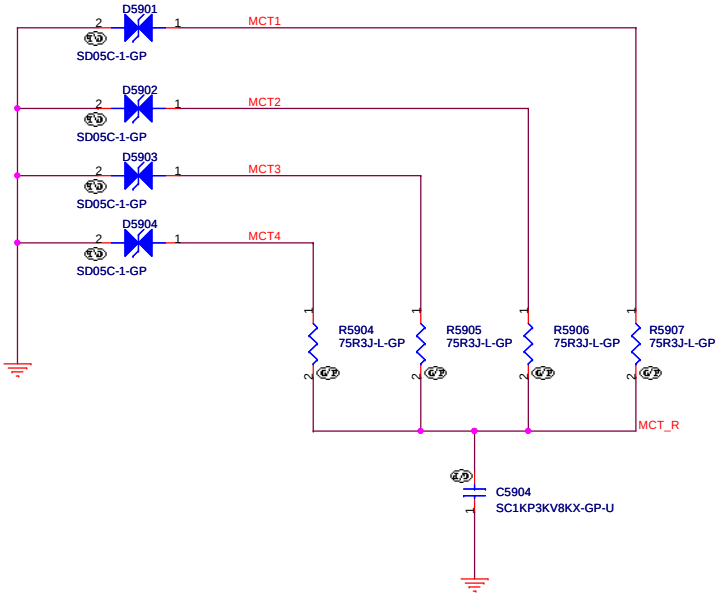






LAN Connector





<Variant Name>

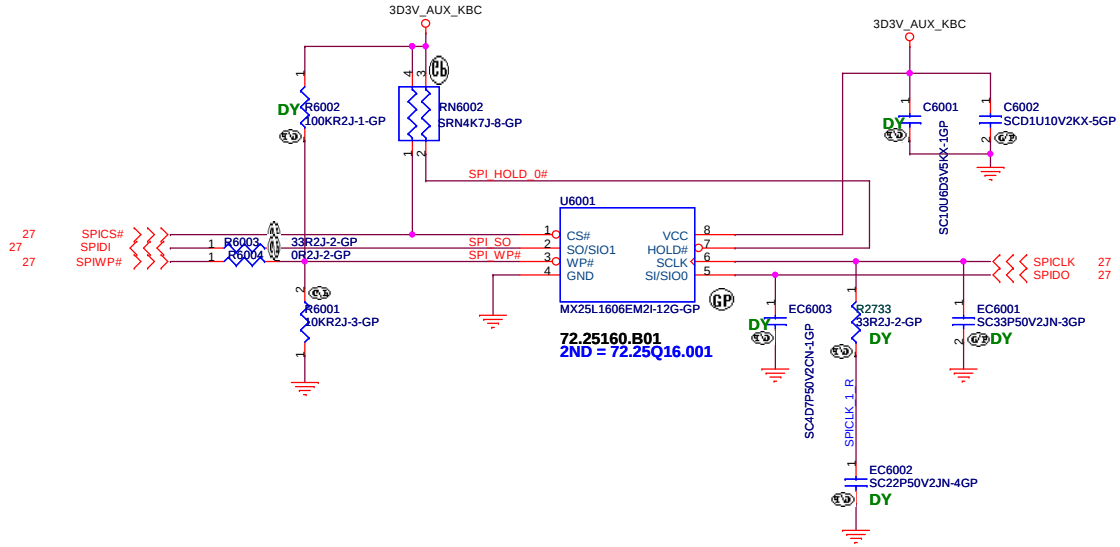
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

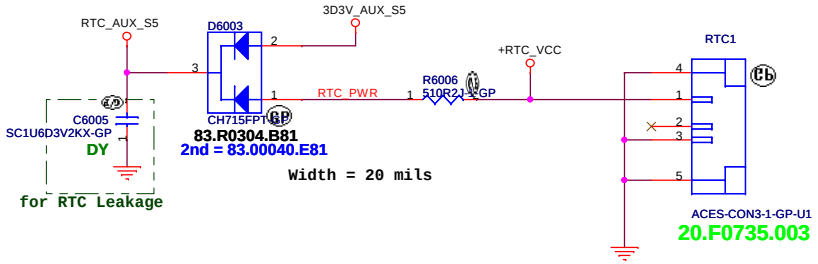
Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 59 of 102

SPI FLASH ROM (2M byte) for KBC



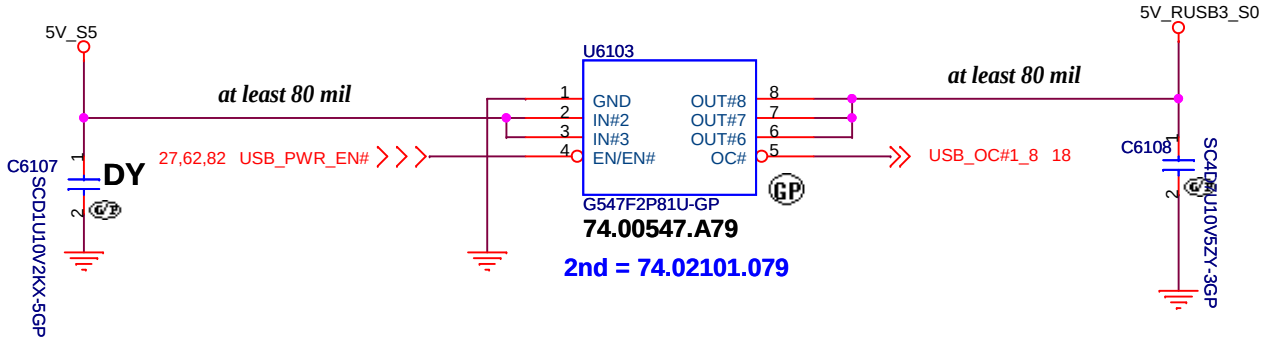
SSID = RBATT



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Flash/RTC*	
Size A3	Document Number LB475	Rev -1
Date: Tuesday, August 02, 2011	Sheet 60 of 102	



<Variant Name>

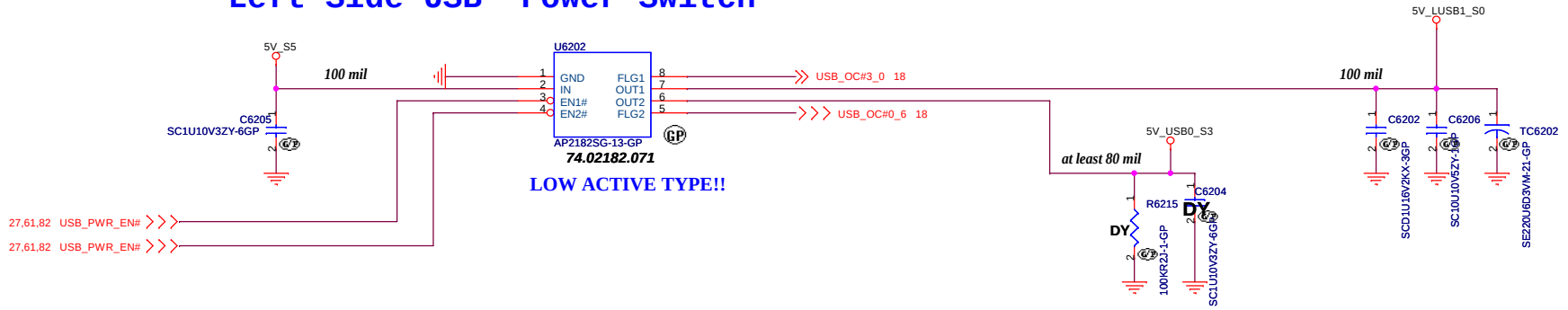
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

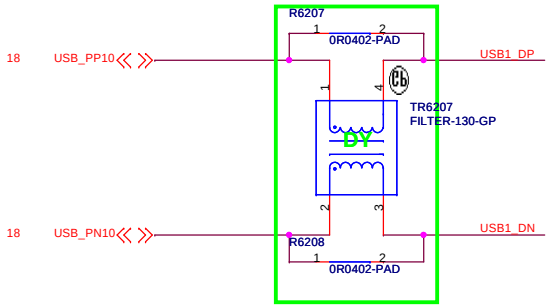
Title: ***USB Power SW***

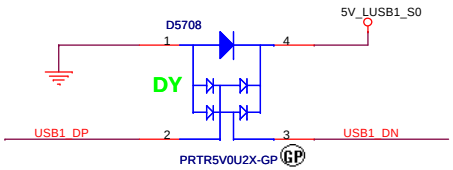
Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 61 of 102

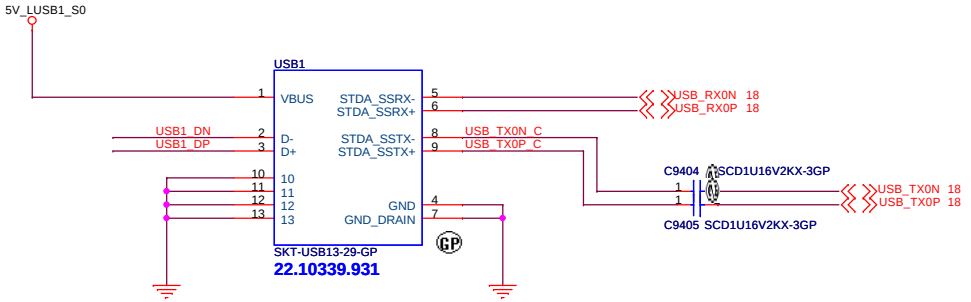
Left Side USB Power Switch







USB3.0



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

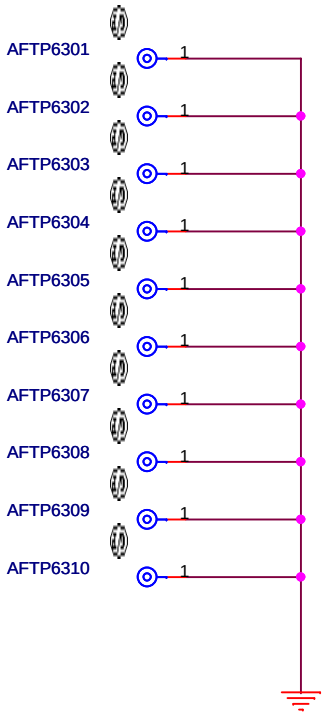
<Variant Name>

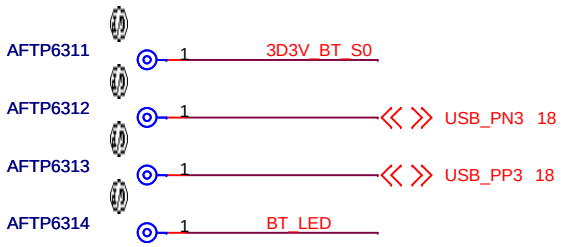
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 2.0/3.0

Size: A3 | Document Number: LB475 | Rev: -1

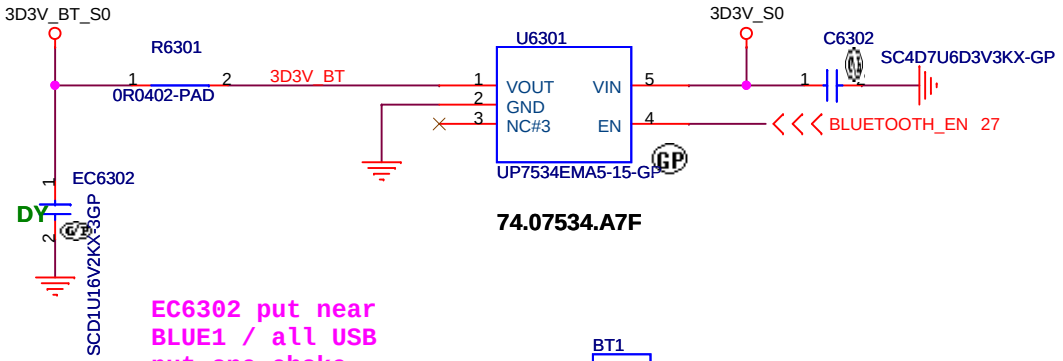
Date: Tuesday, August 02, 2011 | Sheet 62 of 102





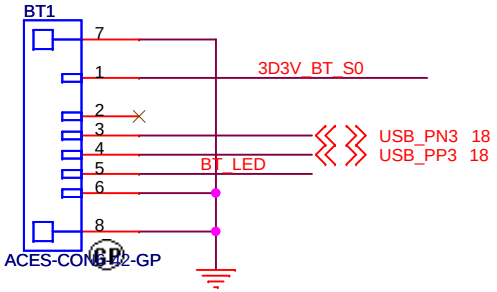
Bluetooth Module

1.5A / High Active Voltage 2V

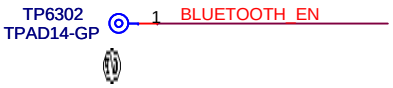


74.07534.A7F

EC6302 put near
BLUE1 / all USB
put one choke
near connector
by EMI request



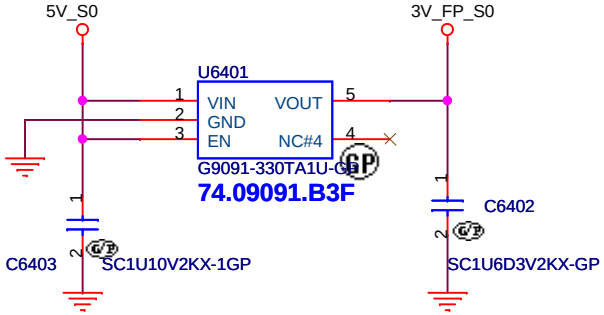
20.F1705.006



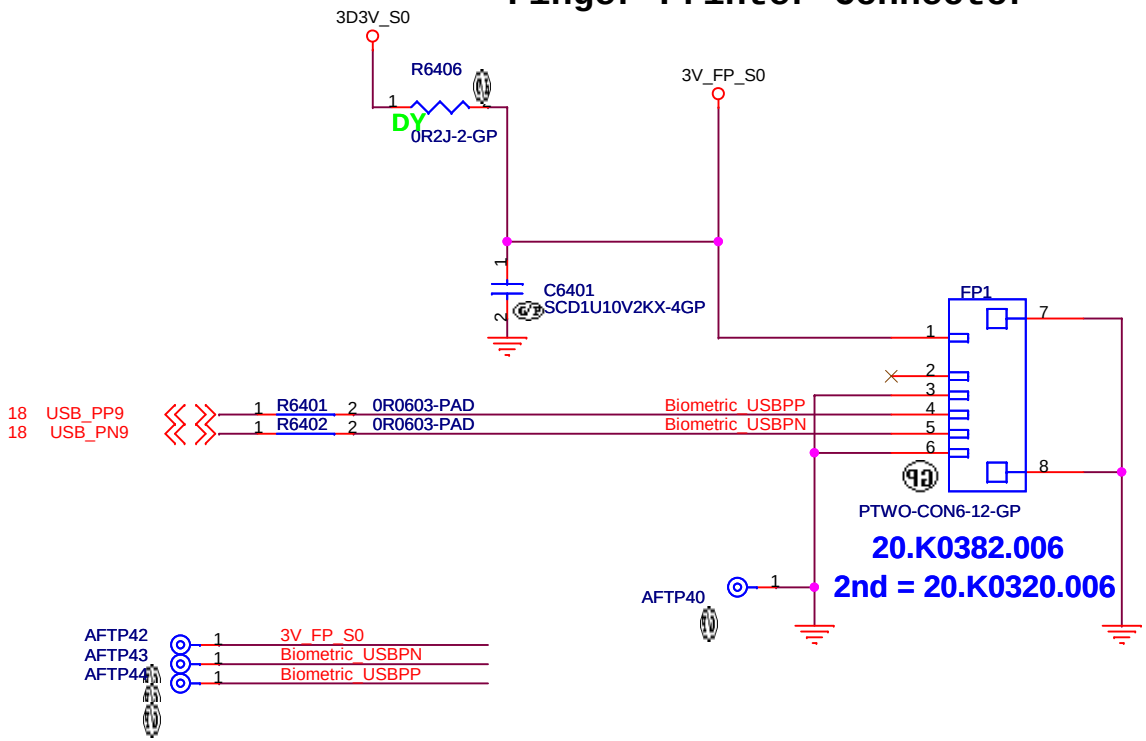
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLUE TOOTH**		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 63 of 102	



Finger Printer Connector



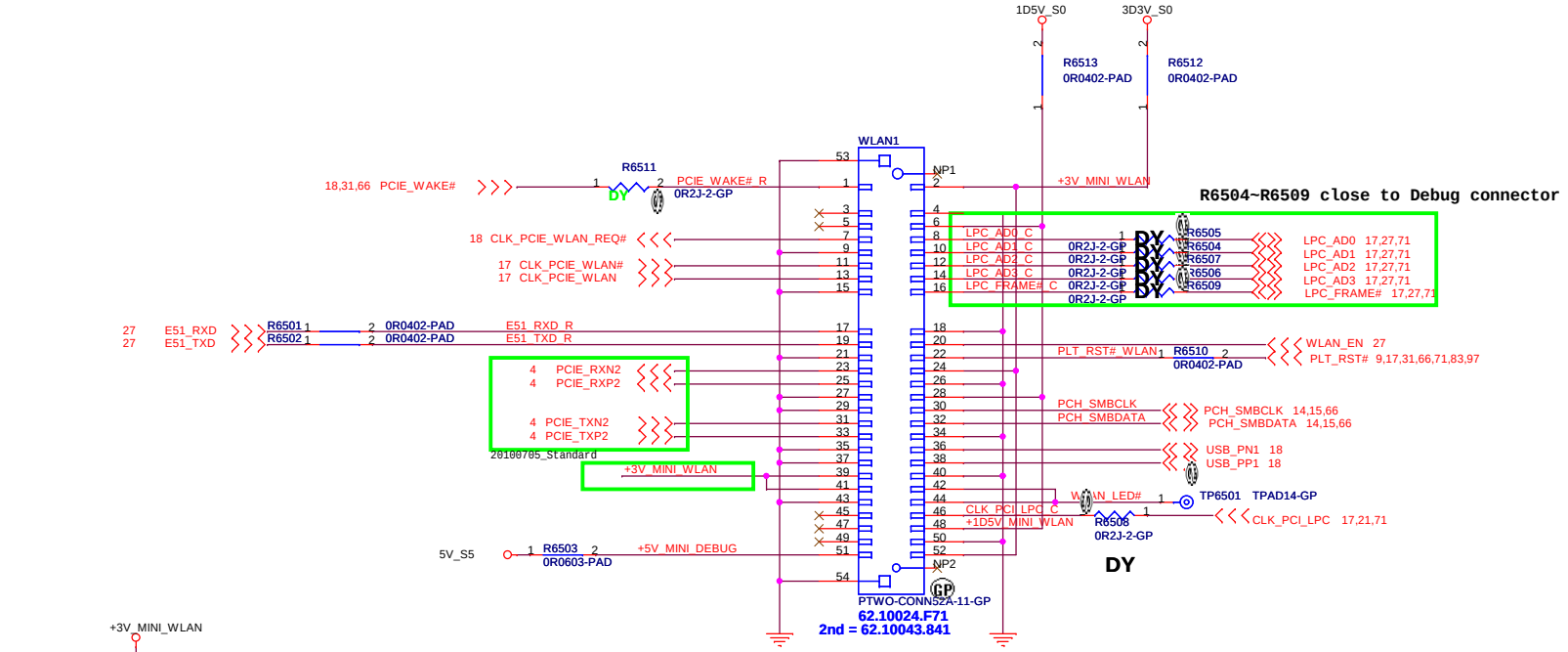
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Print***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 64 of 102	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

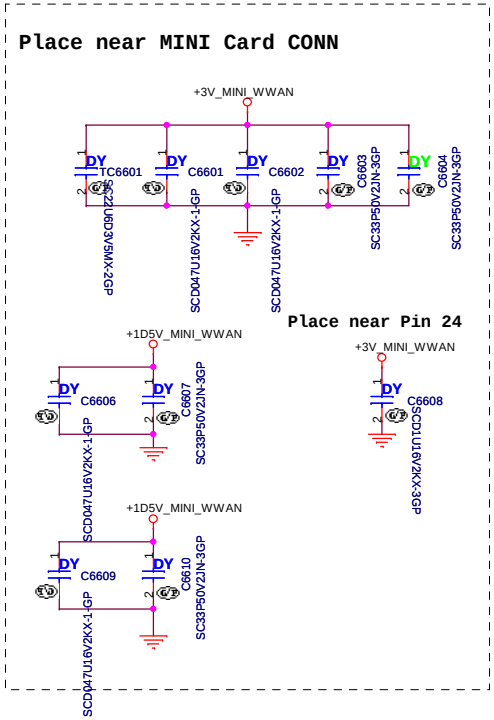
Title: ***MINICARD(WLAN)/ITP CONN***

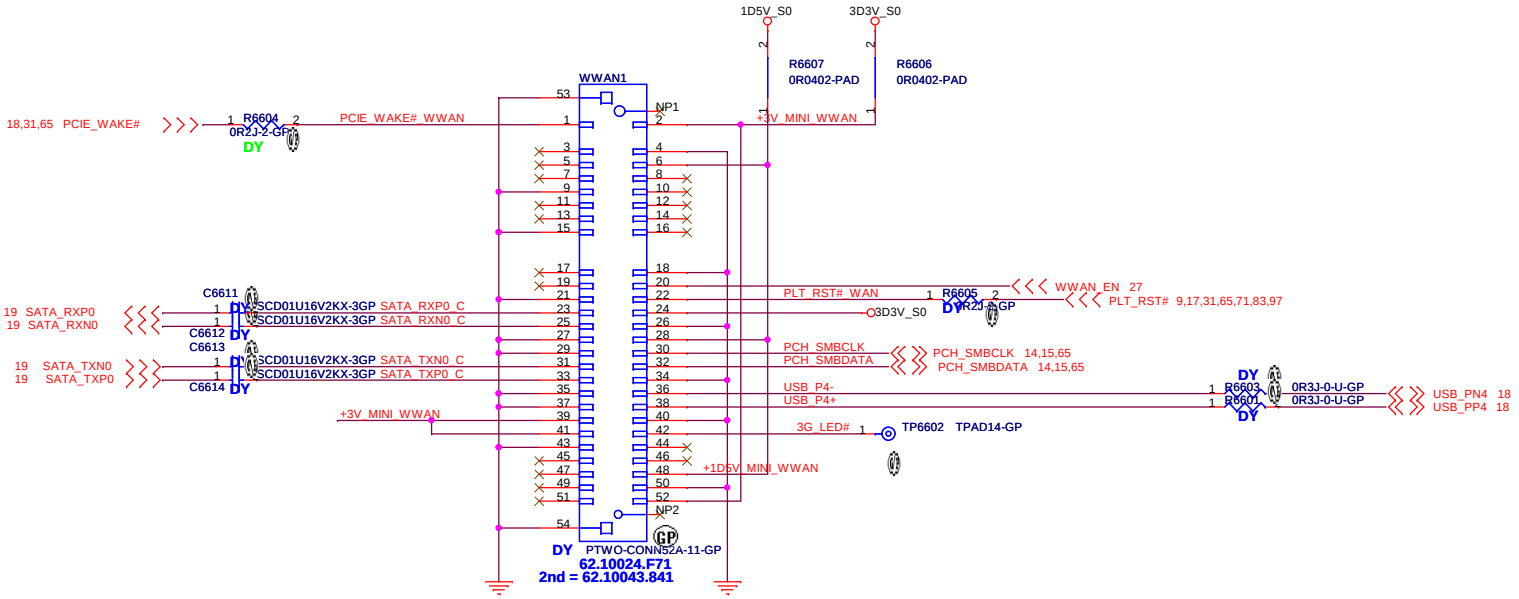
Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 65 of 102

SSID = Wireless

Mini Card Connector(WWAN)





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: WWAN		
Size: A3	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 66 of 102	

(Blanking)

<Variant Name>

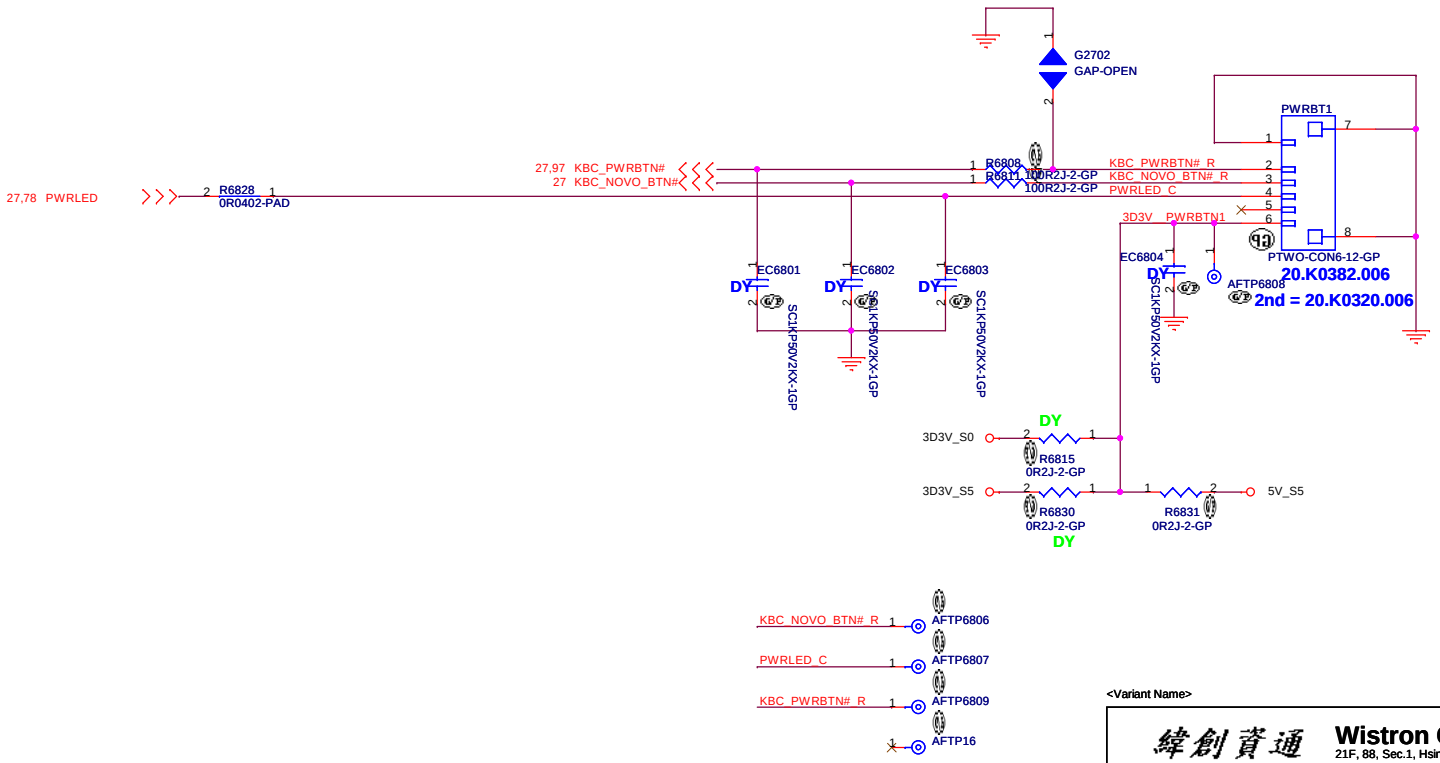
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
SIM Card

Size	Document Number	Rev
A4	**LB475**	**-1**

Date: Tuesday, August 02, 2011 Sheet 67 of 102

Power button LED(White)

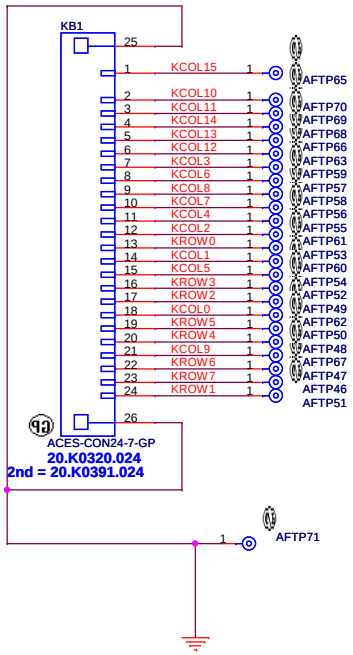


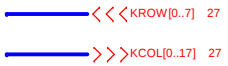
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LED Bard/Power Button***
Size A3	Document Number **LB475** Rev **-1**
Date: Tuesday, August 02, 2011	Sheet 68 of 102

SSID = KBC

Internal KeyBoard Connector

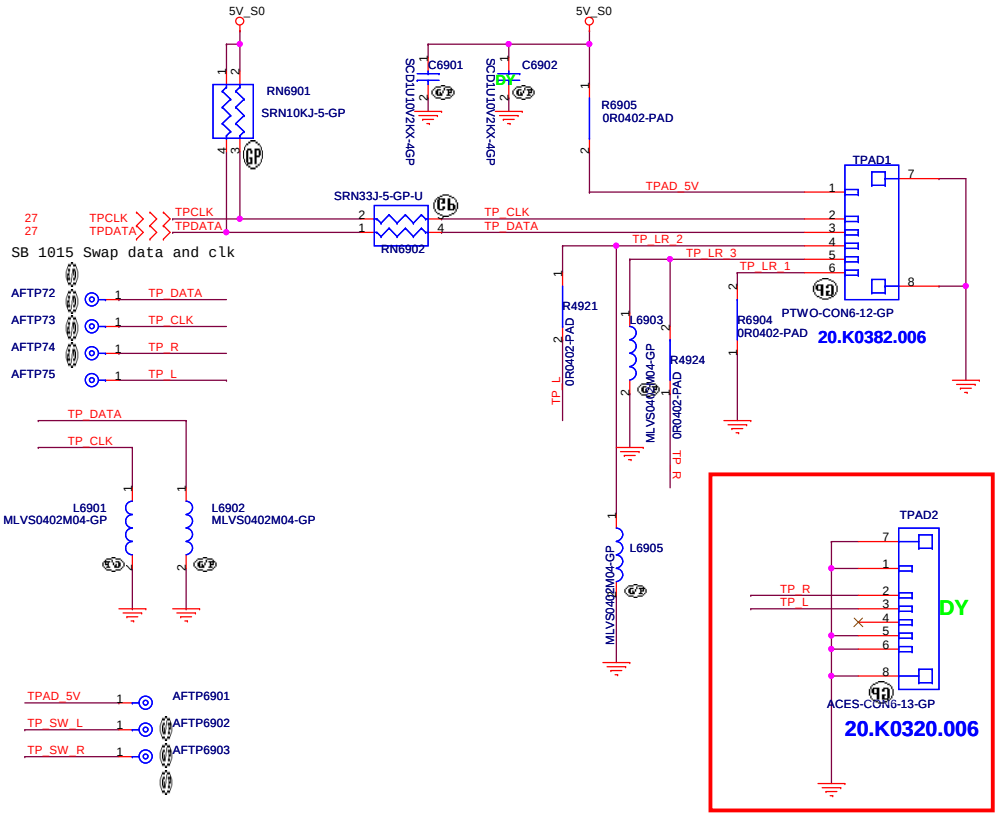


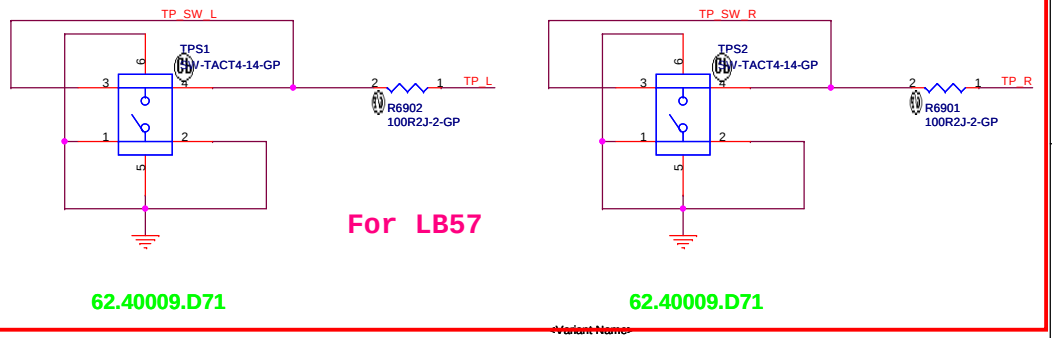


* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad





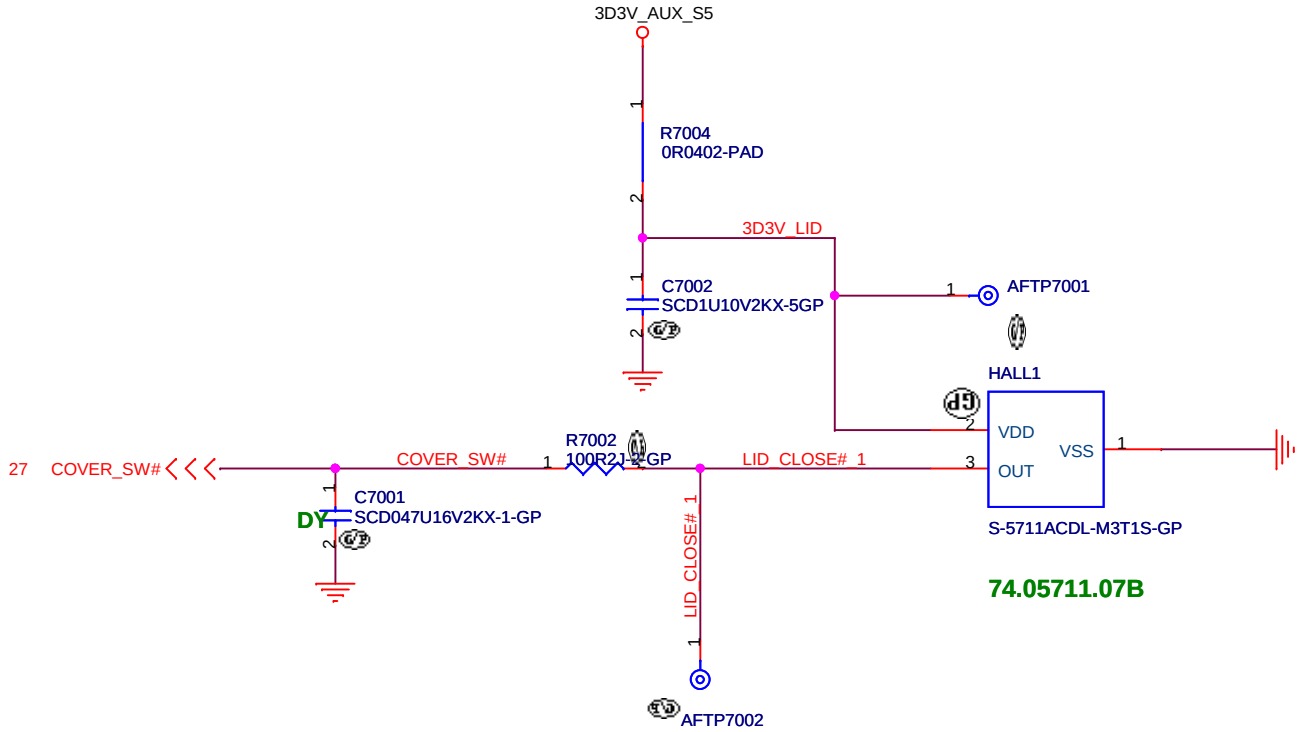
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 69 of 102



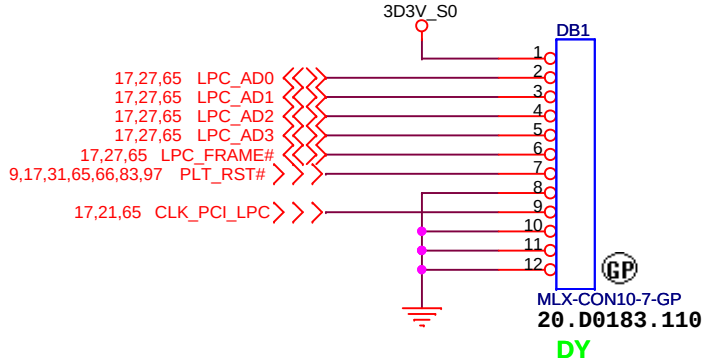
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

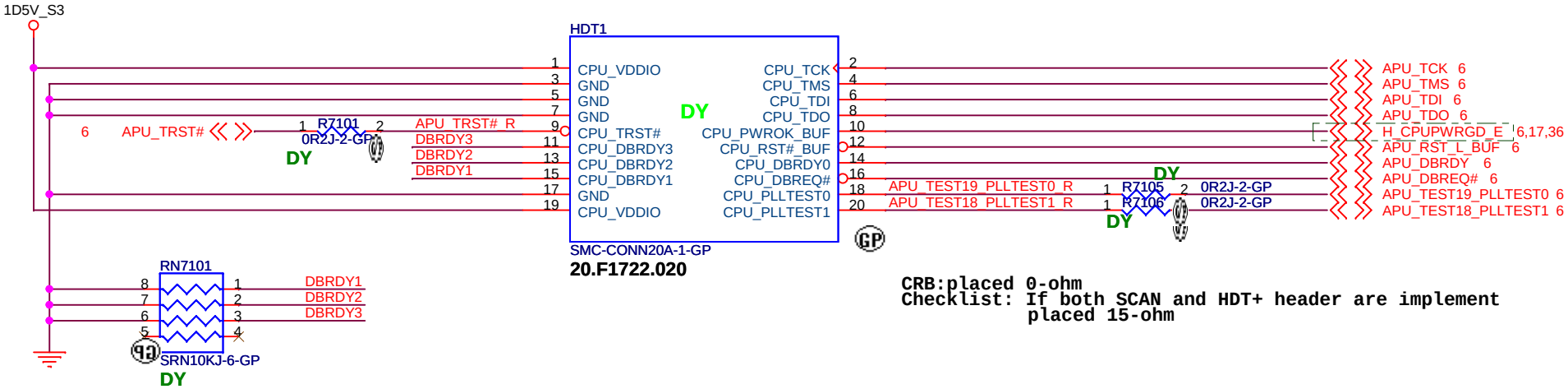
Title: ***Hall Sensor***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 70 of 102



HDT+ Connectors



CRB:placed 0-ohm
Checklist: If both SCAN and HDT+ header are implement
placed 15-ohm

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Dubug connector*		
Size: A4	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 71 of 102	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 72 of 102

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 73 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CARD Reader CONN*

Size	Document Number	Rev
A4	LB475	-1

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Express Card*

Size	Document Number	Rev
A4	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 75 of 102

(Blanking)

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **LB475**	Rev: **-1**
Date: Tuesday, August 02, 2011	Sheet 76 of 102	

(Blanking)

<Variant Name>

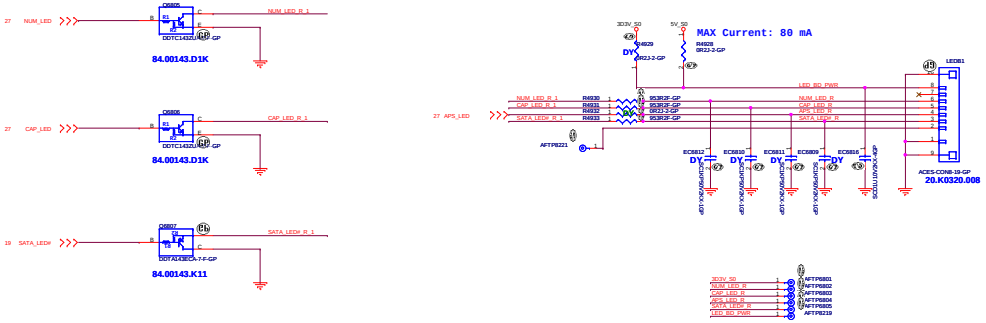
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

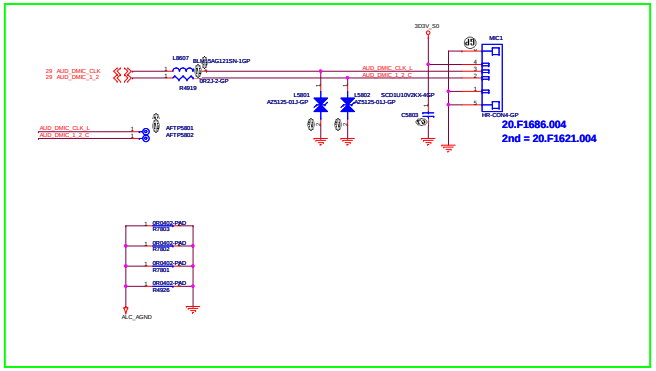
Size	Document Number	Rev
A4	**LB475**	**-1**

Date: Tuesday, August 02, 2011 Sheet 77 of 102

LED Bord CONN.

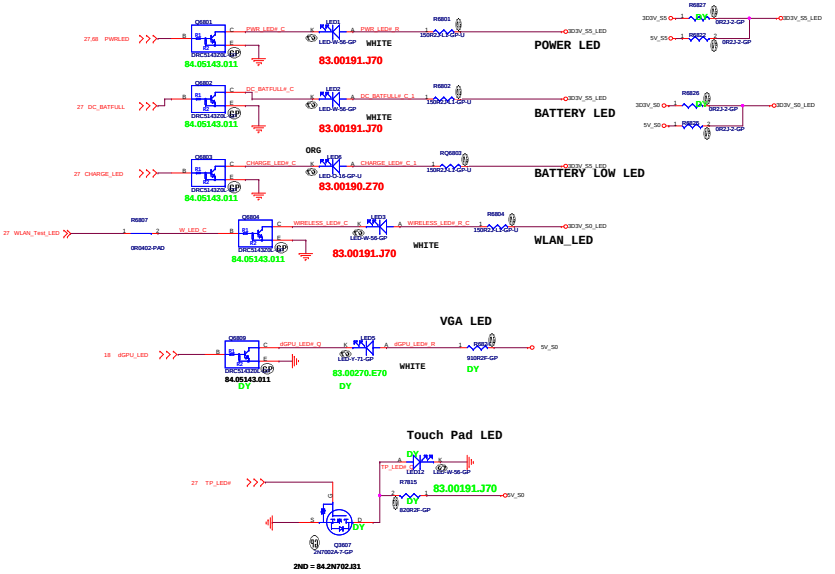


B475 => Digital Mic circuit.



LED

1209 All LED POWER CHANGE 5V_S5



VGA LED

Touch Pad LED

<Variant Name>

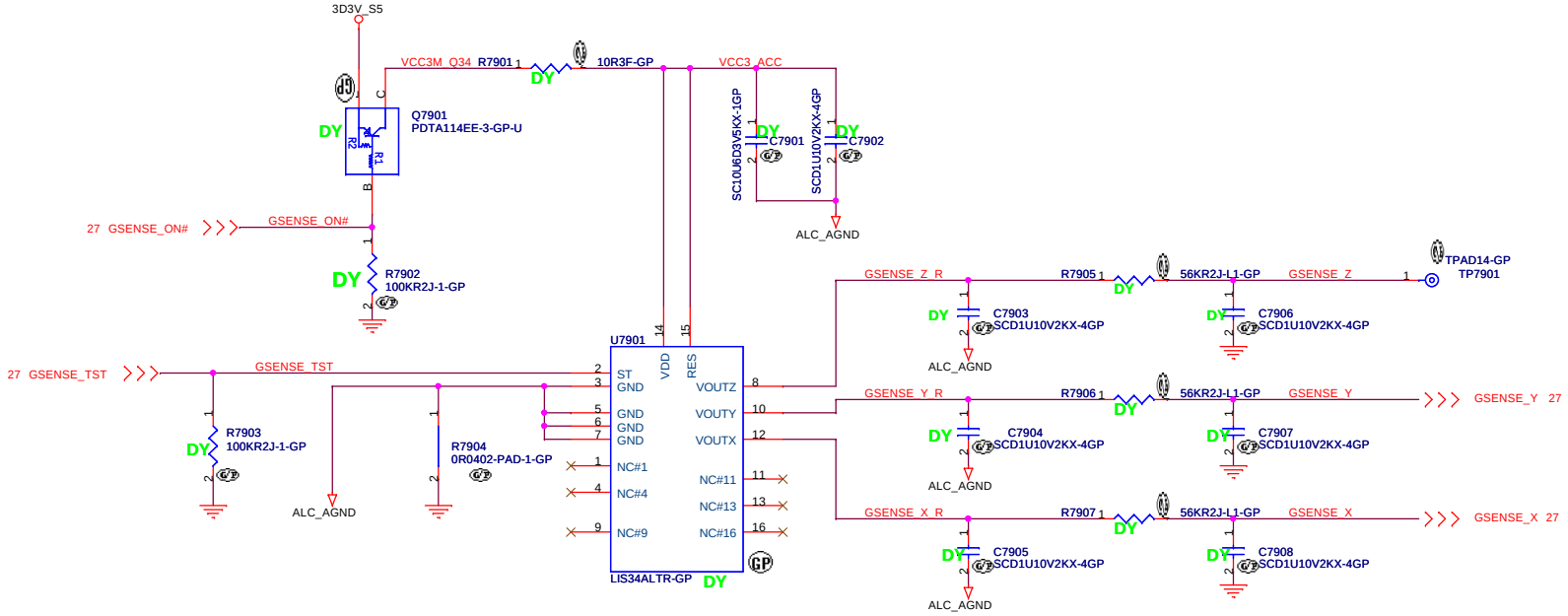
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: AVBD/LED/MIC

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 78 of 102

G-Sensor



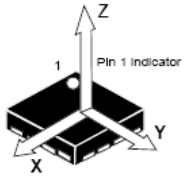
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*G-sensor*	
Size A3	Document Number LB475	Rev -1
Date: Tuesday, August 02, 2011	Sheet 79 of 102	

(Blanking)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A	**LB475**	**-1**

Date: Tuesday, August 02, 2011 Sheet 80 of 102

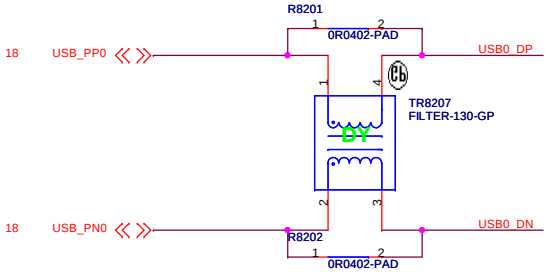
(Blanking)

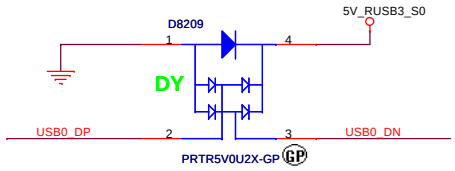
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

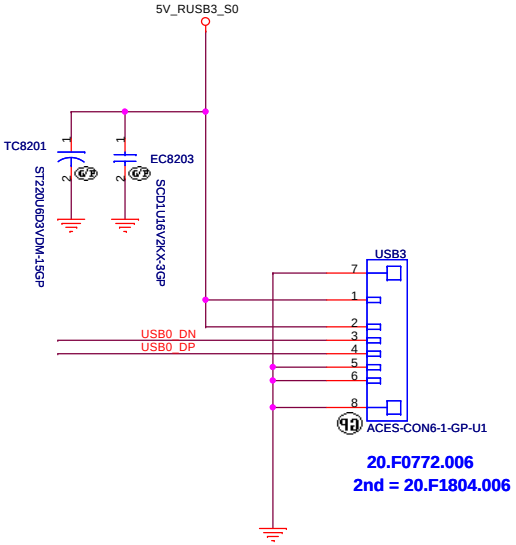
Title
UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A4	**LB475**	**-1**

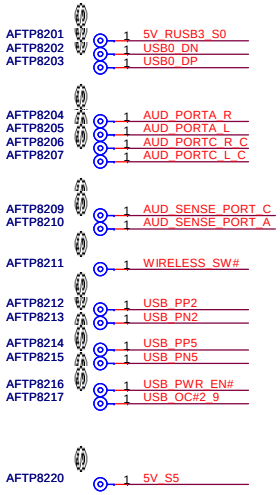


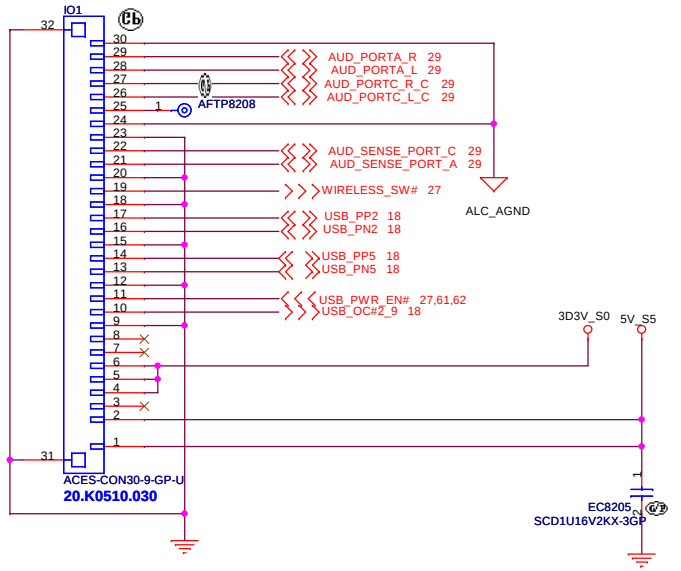


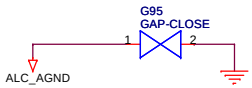
USB3



Card Reader Board CONN.







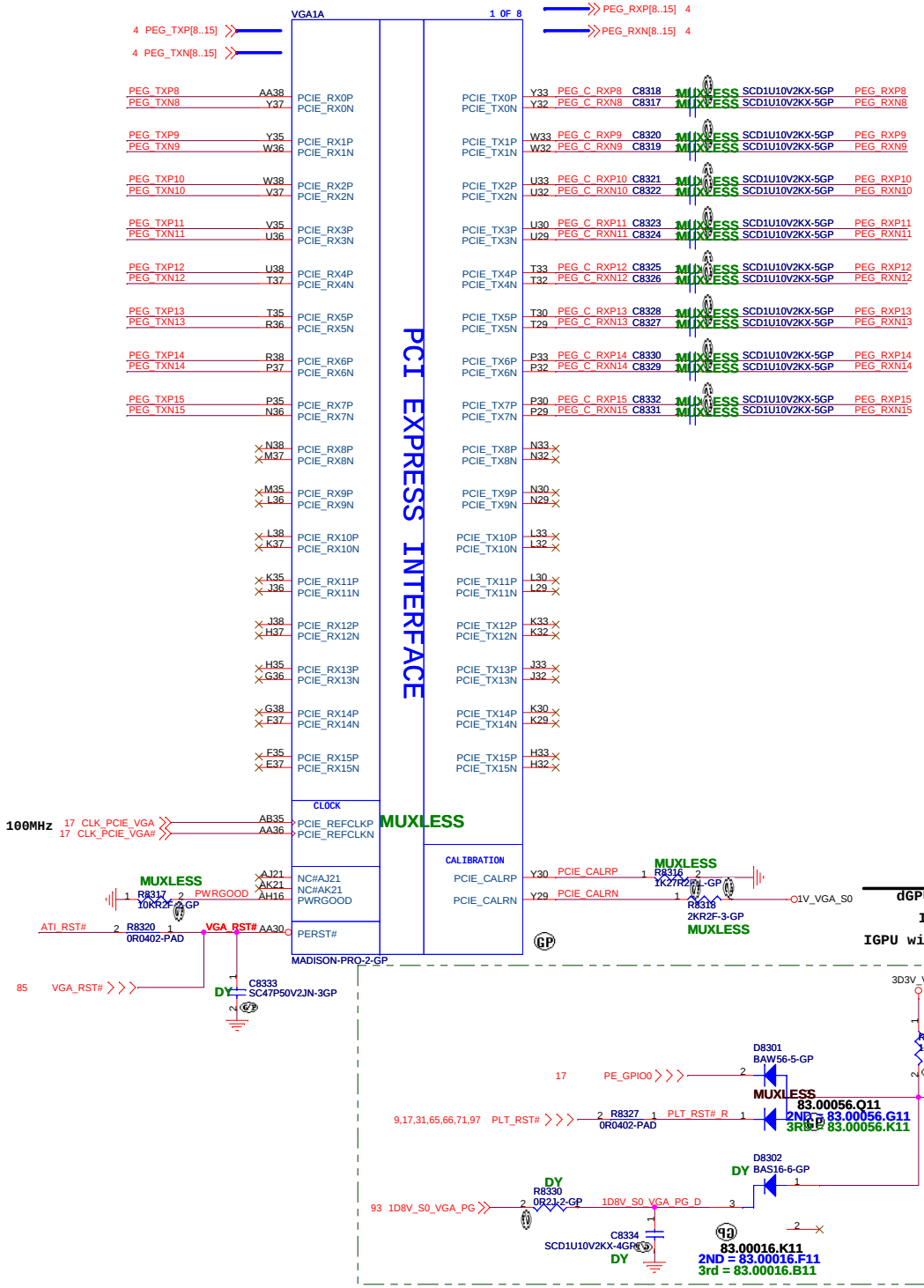
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 82 of 102



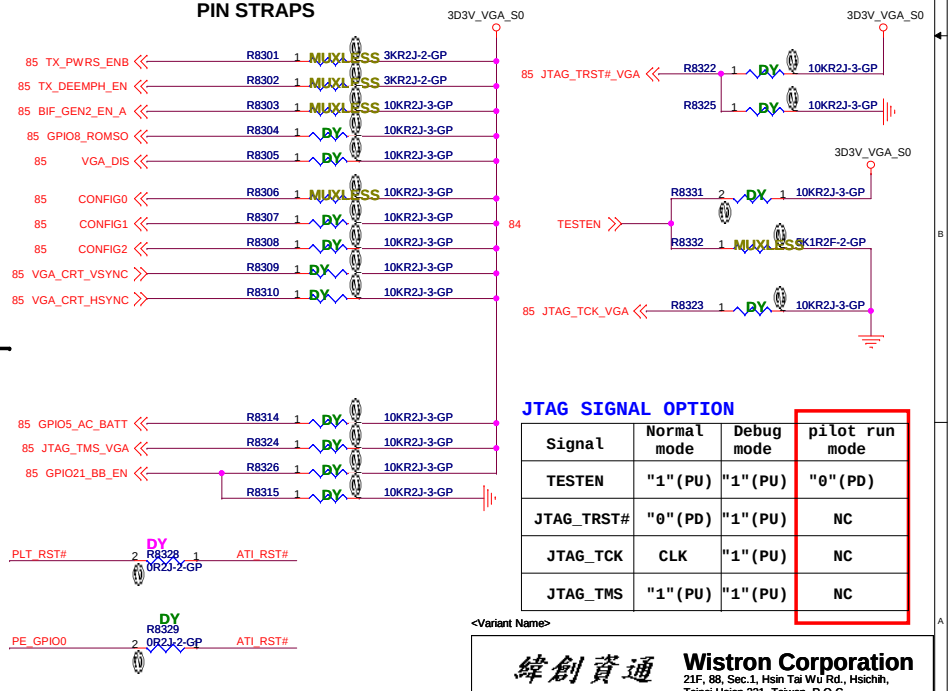
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

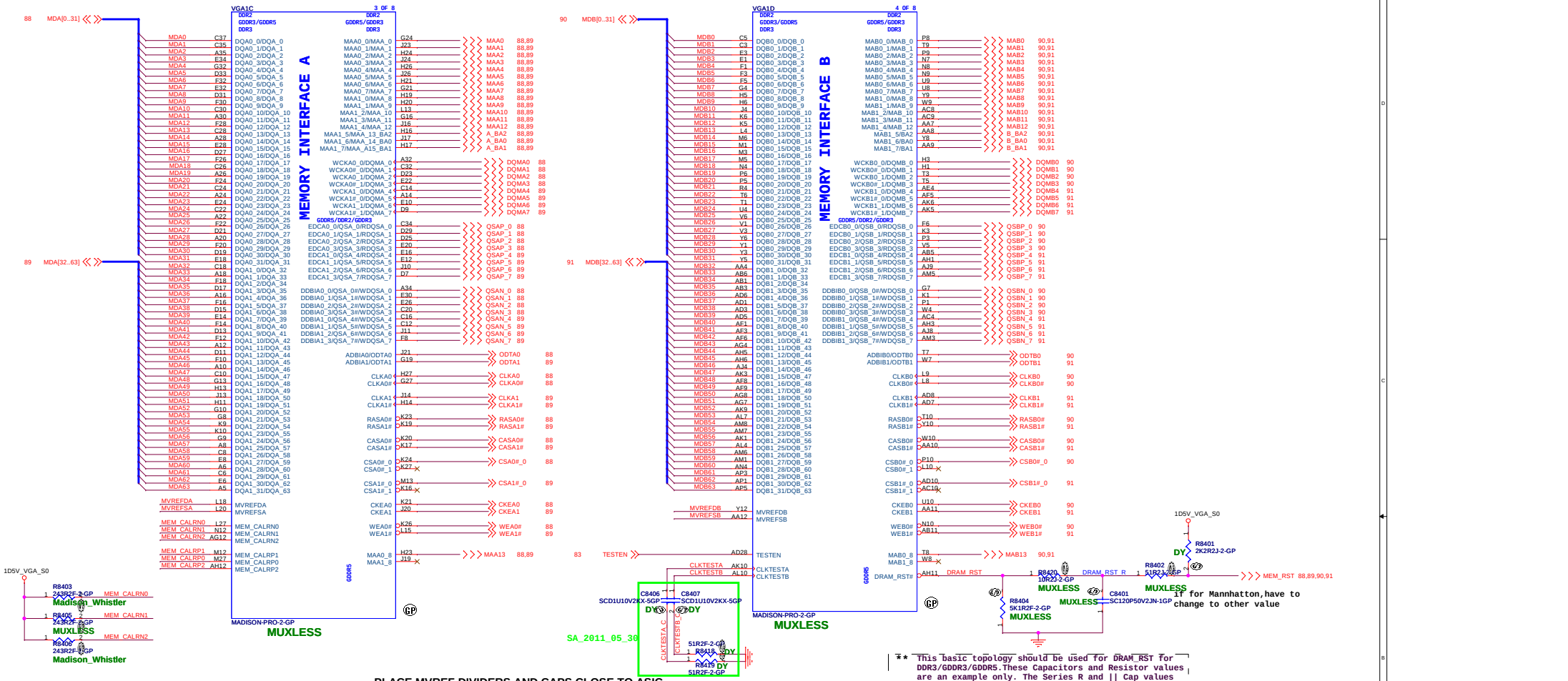
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **GPU_PCIE/STRAPPING(1/5)**

Size: Custom | Document Number: LB475 | Rev: -1

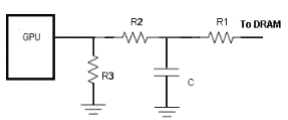
Date: Tuesday, August 02, 2011 | Sheet 83 of 102



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

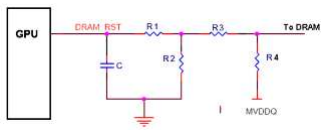
** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Vancouver



C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

Mannhatton



C	R1	R2	R3	R4
68 pF	51 Ω	10 kΩ	0 Ω	DNI

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_Memory(2/5)

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 84 of 102

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

Address	DVPDATA[3:0]	Vender	PN	Speed
0	0 0 0 0	Hynix	H5TQ2G63BFR-11C 2GB (128Mx16)	900Mhz
1	0 0 0 1	Hynix		
2	0 0 1 0	Reserve		
3	0 0 1 1	Hynix	H5TQ1G63DFR-11C 1GB (64Mx16)	900Mhz
4	0 1 0 0	Hynix		
5	0 1 0 1	Reserve		
6	0 1 1 0	Reserve		
7	0 1 1 1	Hynix		
8	1 0 0 0	Samsung	K4W1G1646G-BC11 1GB (64Mx16)	900Mhz
9	1 0 0 1	Samsung		
10	1 0 1 0	Reserve		
11	1 0 1 1	Samsung	K4W2G1646C-HC11 2GB (128Mx16)	900Mhz
12	1 1 0 0	Samsung		
13	1 1 0 1	Reserve		
14	1 1 1 0	Reserve		
15	1 1 1 1	Samsung		

LVDS Interface

I2C Bus for LVDS

Straps

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

Bead:470-ohm 1.5A

DDC1/DDC2/DDC6 have 5V-tolerant

DDC1 channel for CRT

DDC2 channel for HDMI

AUXP PD 100K
AUXN PU 100K
Draw on EDP circuit page

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

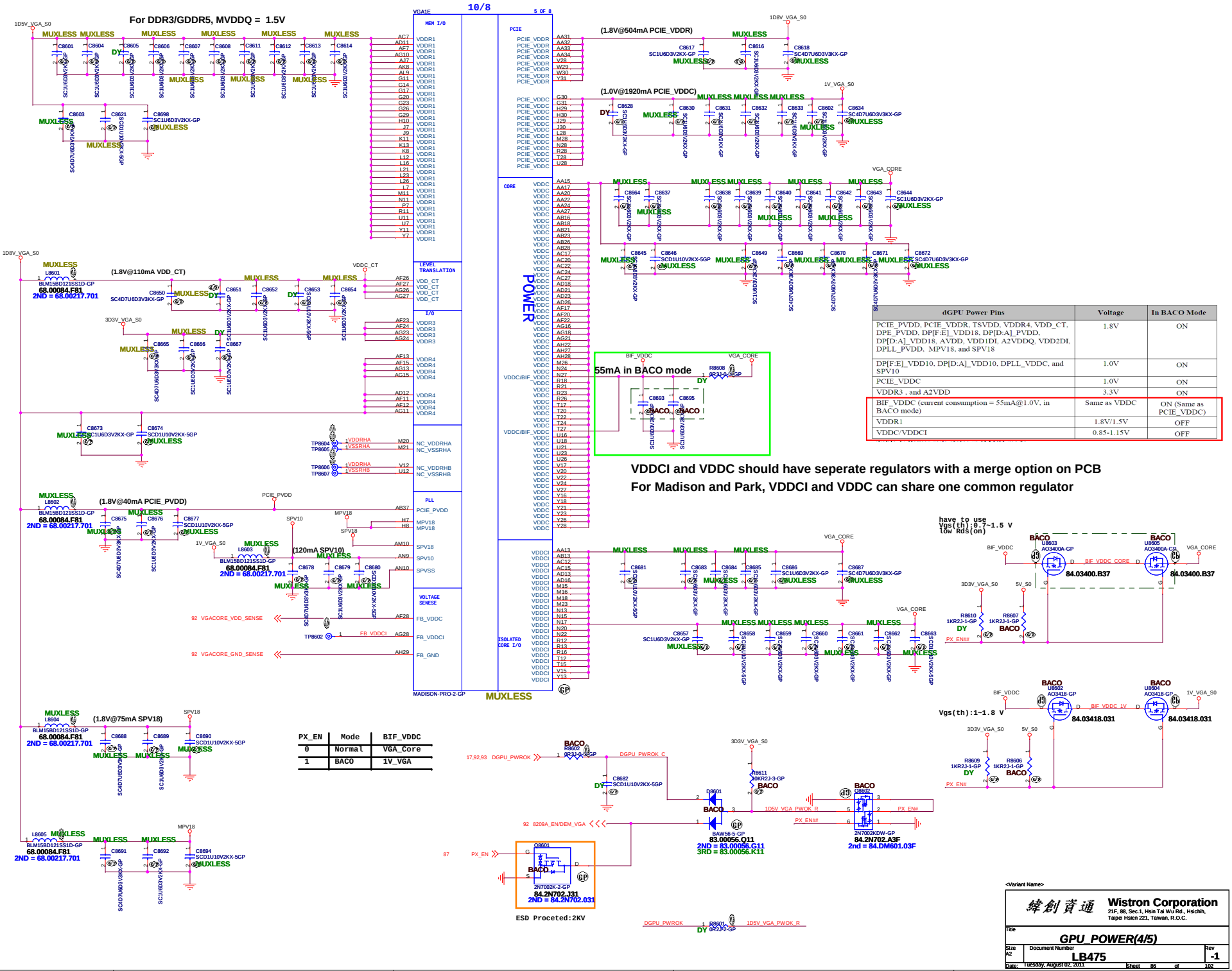
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size	Document Number	Rev
A2	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 85 of 102



dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3 , and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85~1.15V	OFF

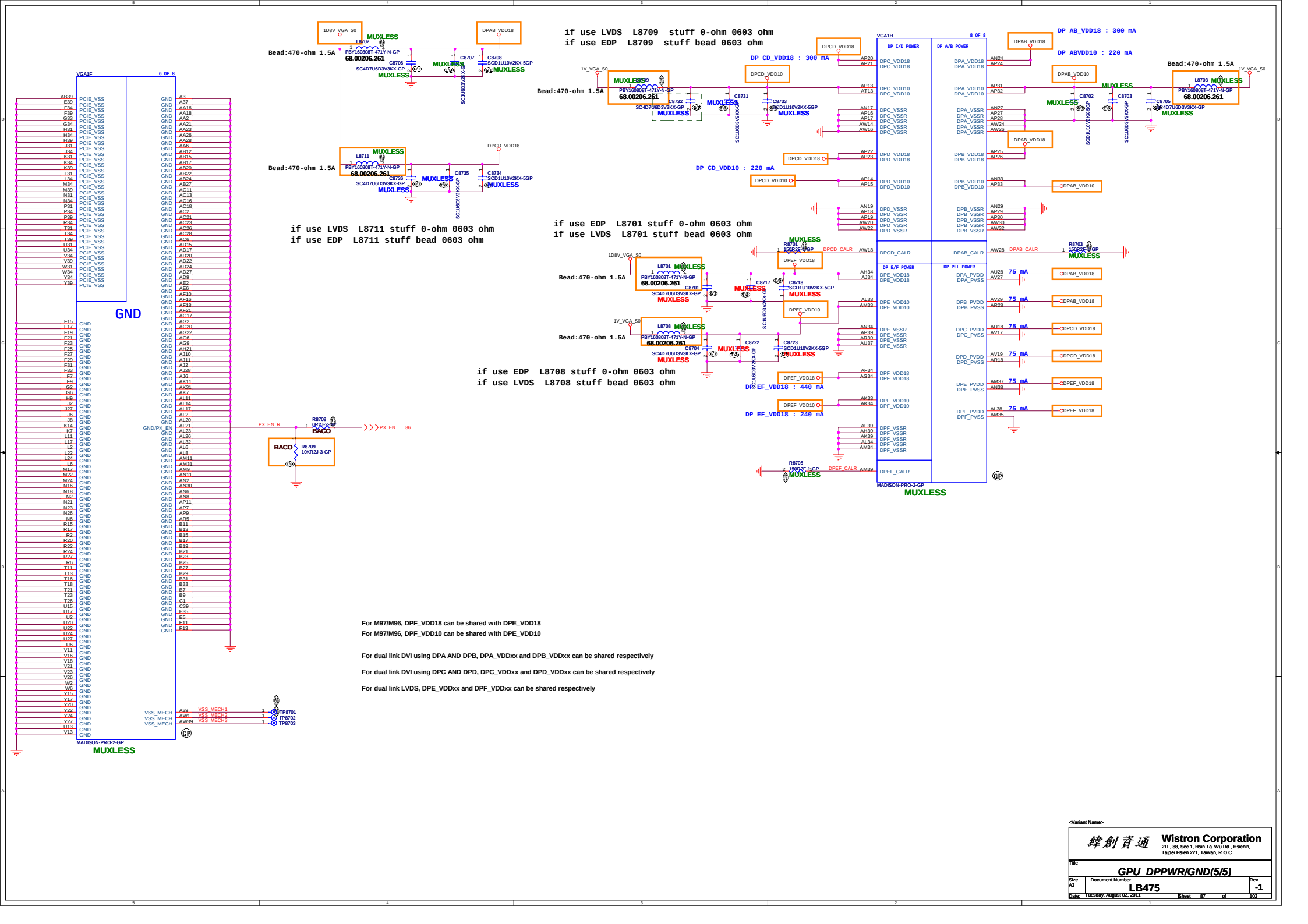
PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A2 | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 86 of 102



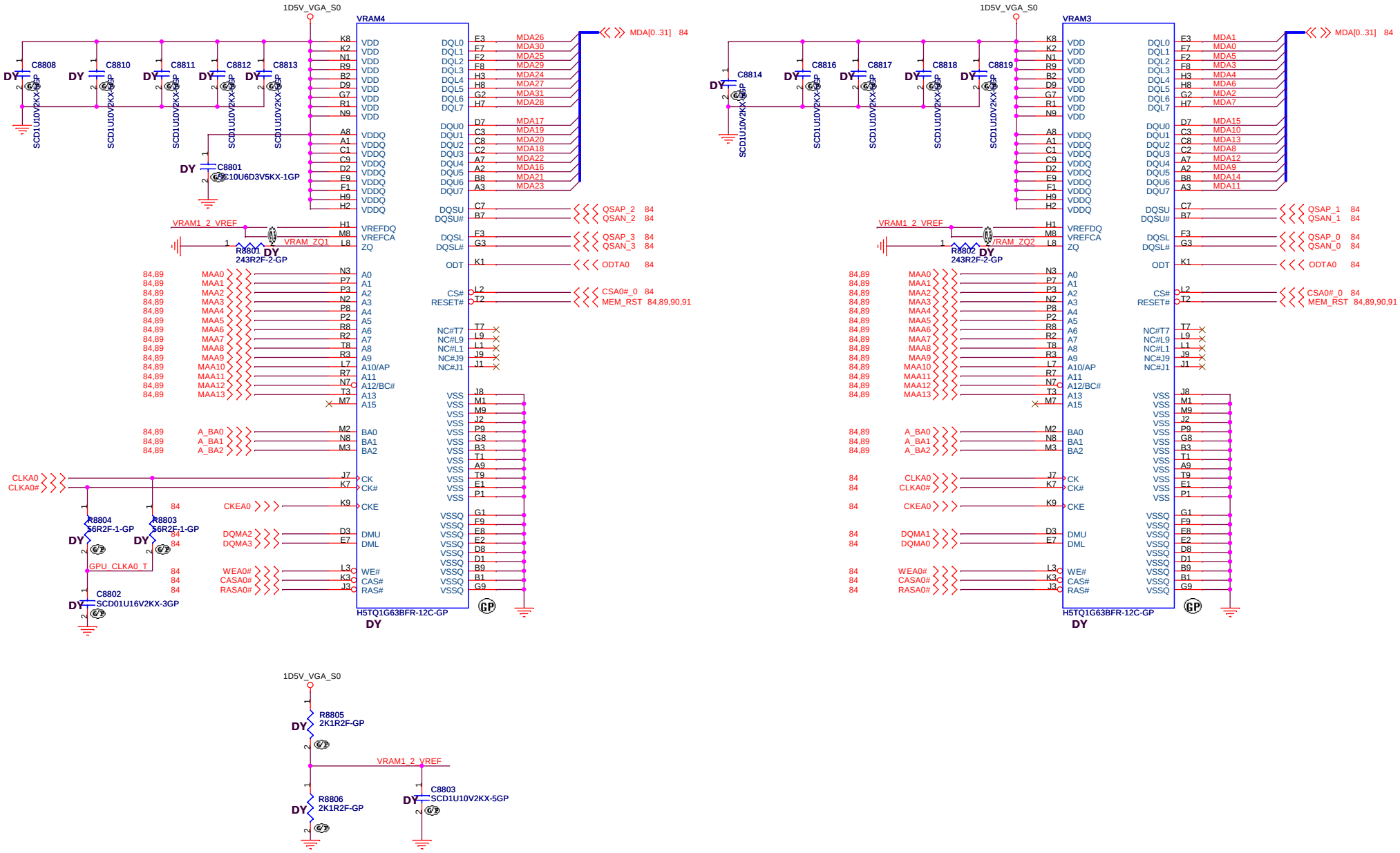
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

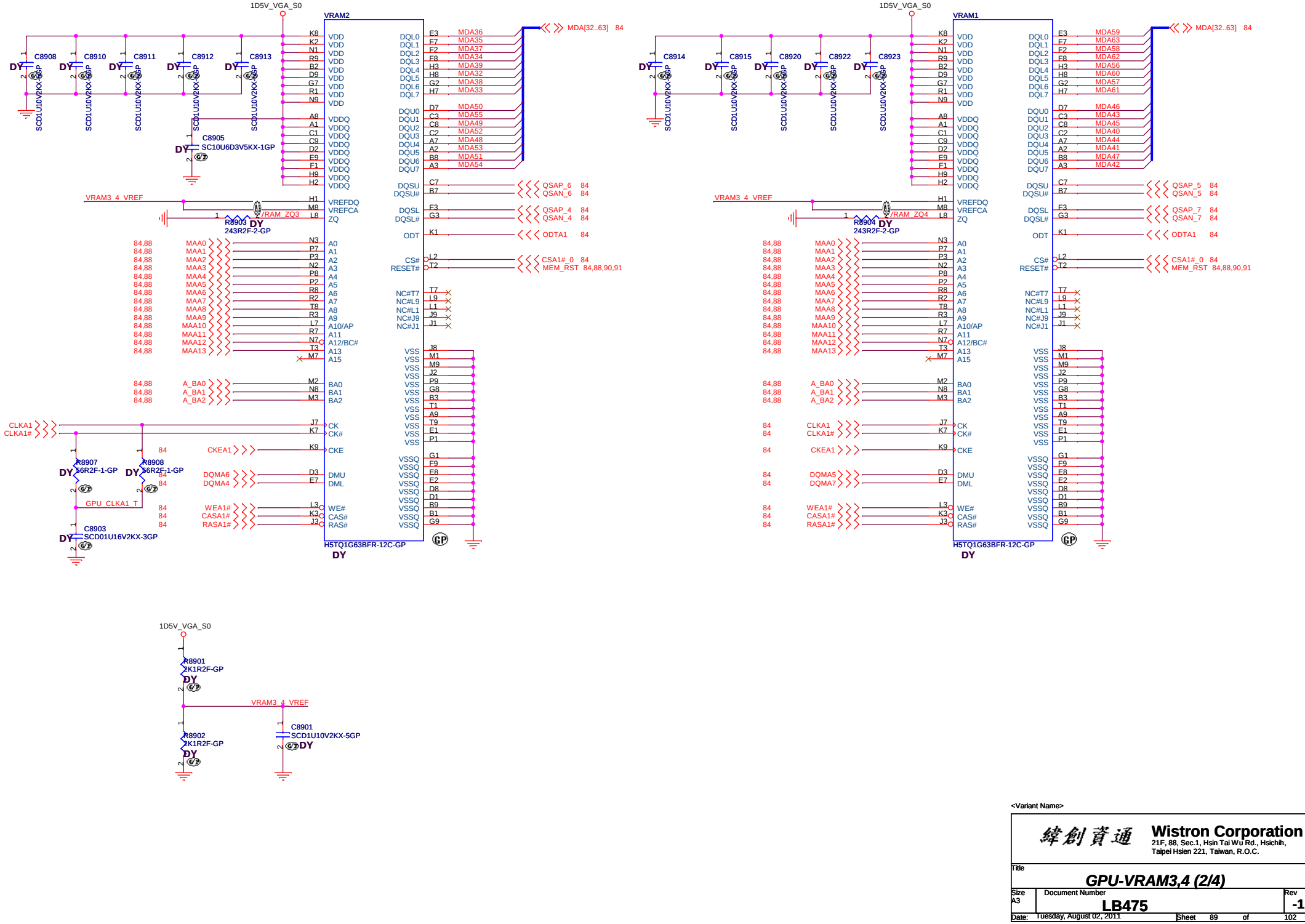
Size	Document Number	Rev
A2	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 87 of 102



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GPU-VRAM1,2 (1/4)***
Size A3	Document Number **LB475** Rev **-1**
Date: Tuesday, August 02, 2011	Sheet 88 of 102



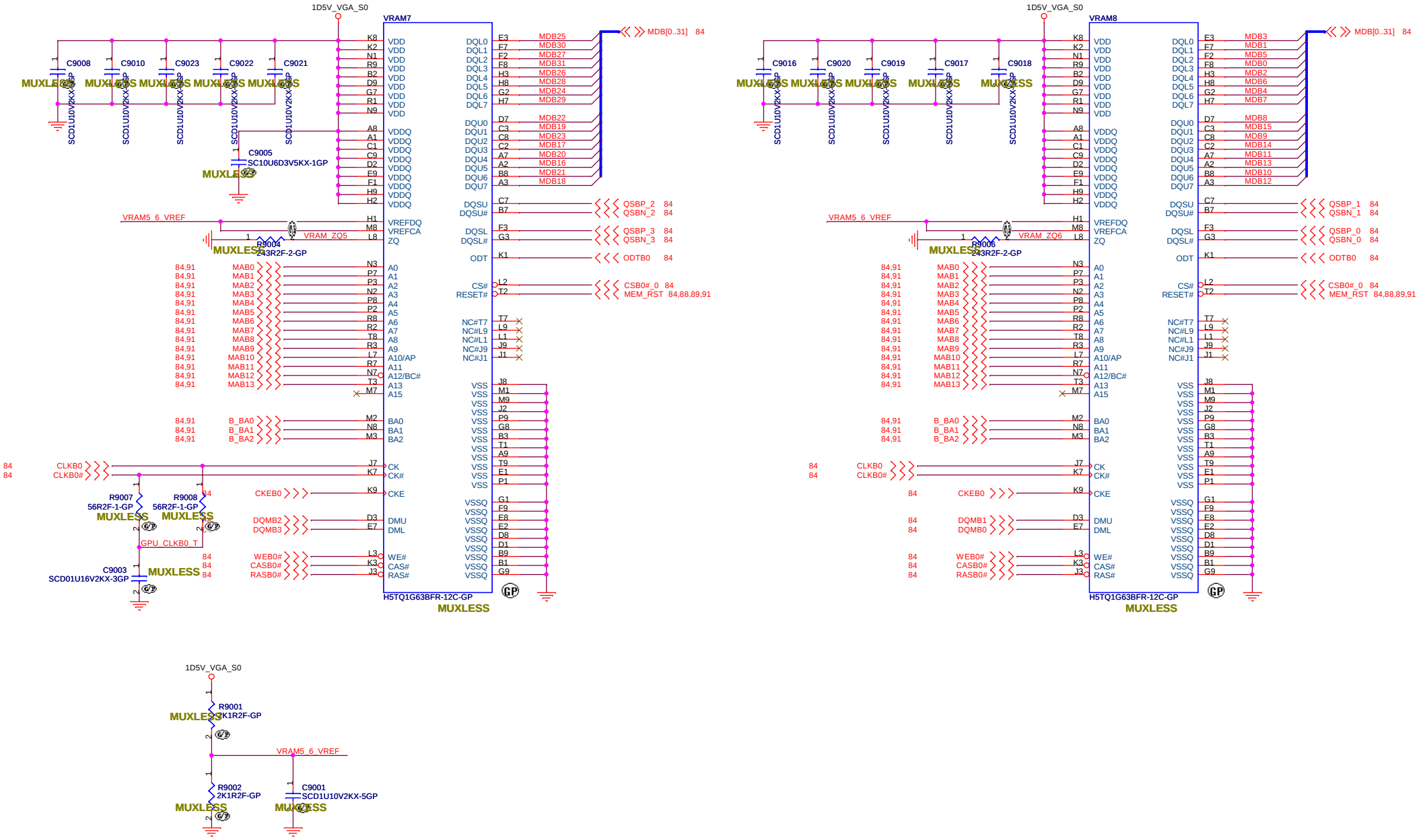
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 89 of 102



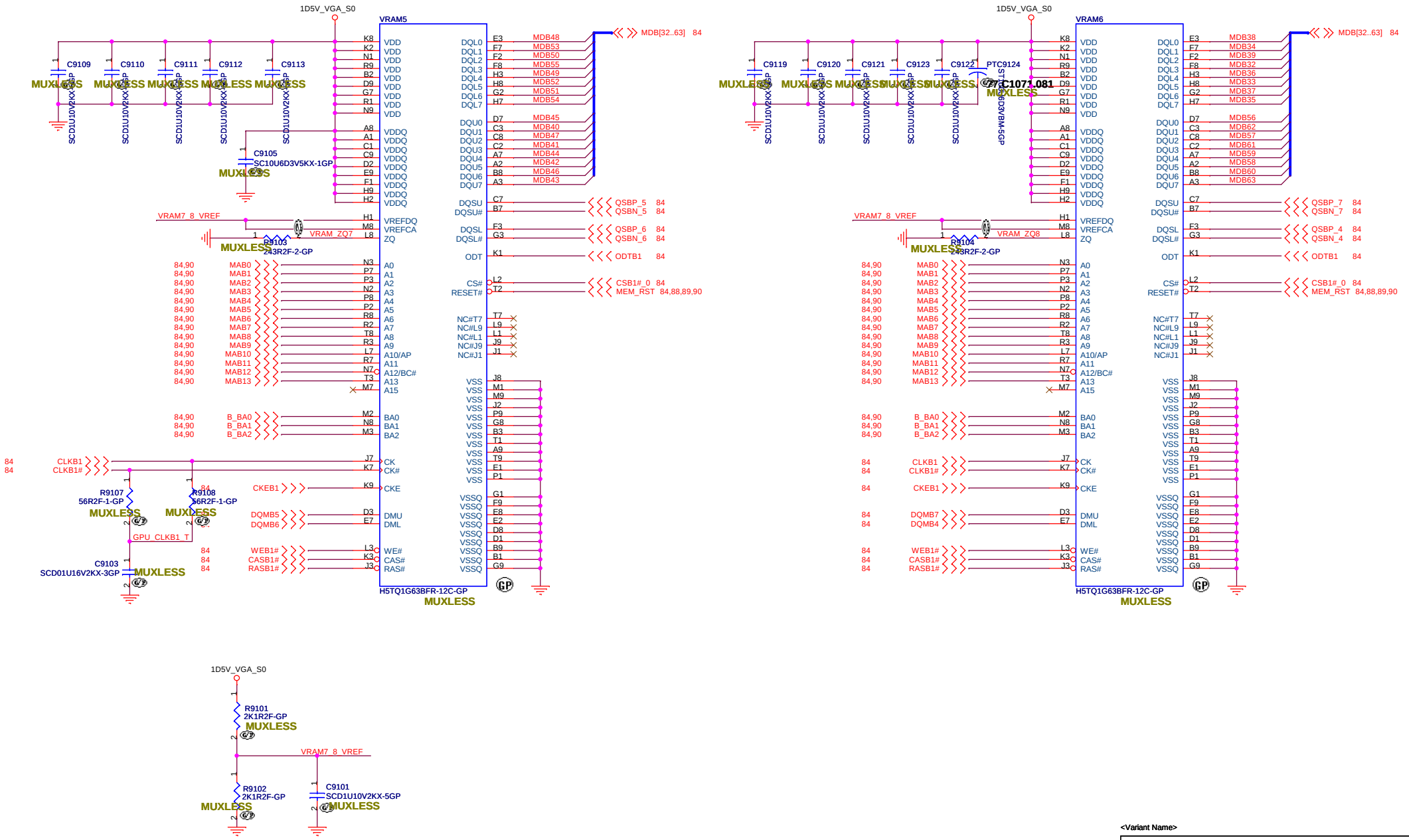
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
A3	LB475	-1

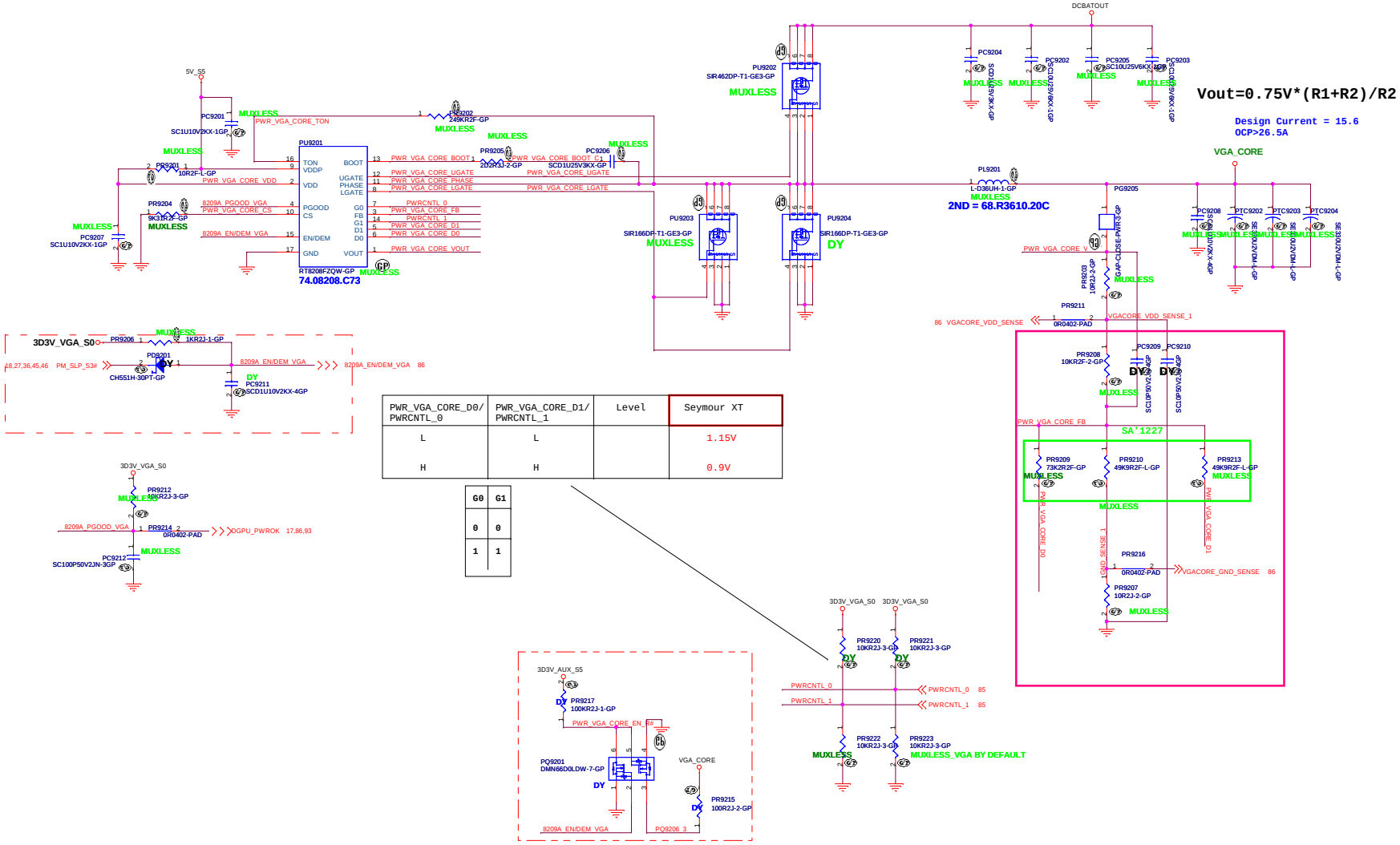
Date: Tuesday, August 02, 2011 Sheet 90 of 102



<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM7,8 (4/4)		
Size: A3	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 91 of 102	

SSID = PWR.Plane.Regulator_GFX



PWR_VGA_CORE_D0/ PWRCNTL_0	PWR_VGA_CORE_D1/ PWRCNTL_1	Level	Seymour XT
L	L		1.15V
H	H		0.9V

G0	G1
0	0
1	1

<Variant Name>

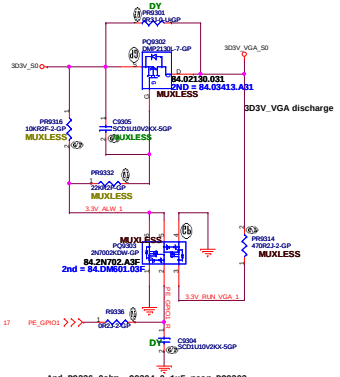
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208F_VGA_CORE

Size: A2 | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 92 of 102

+3VS to 3.3V_DELAY Transfer



And R9336 0ohm, C9304 0.1uF near PQ9303
For 3D3V_VGA_S0 power noise
2011.04.20

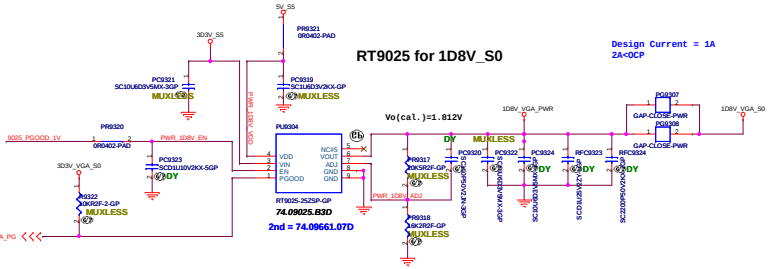
3D3V_VGA_S0 should ramp-up before VGA_Core

VGA_Coreshould ramp-up before 1V_VGA_S0

1V_VGA_S0 should ramp up before 1D8V_VGA_S0

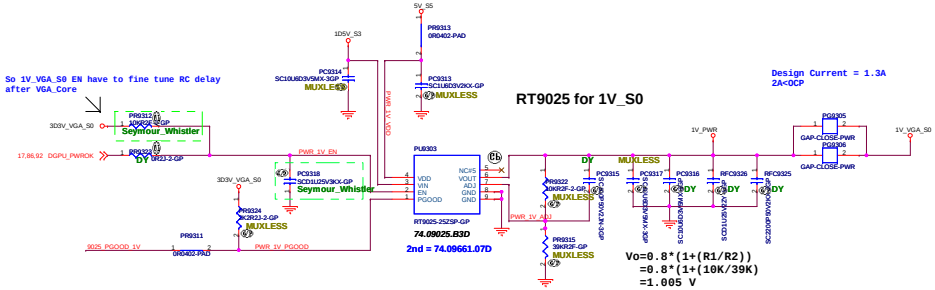
RT9025 for 1D8V_S0

Design Current = 1A
2A<OCP

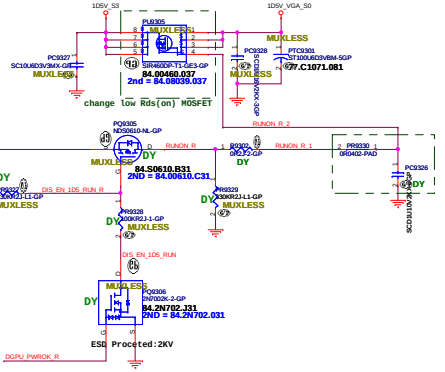


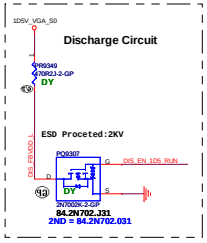
RT9025 for 1V_S0

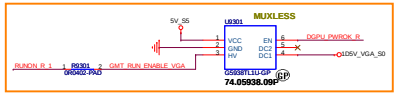
Design Current = 1.3A
2A<OCP

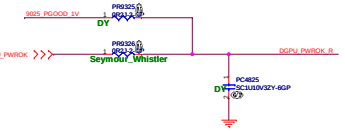


AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm









3D3V_VGA_S0 should ramp-up before VGA_Core

VGA_Coreshould ramp-up before 1V_VGA_S0

1V_VGA_S0 should ramp up before 1D8V_VGA_S0

1D5V_VGA_S0 sequence no define specially

So 1D5V_VGA_S0 EN have to fine tune RC delay after 1V_VGA_S0

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size: Custom | Document Number: LB475 | Rev: -1

Date: Tuesday, August 02, 2011 | Sheet 83 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A3	LB475	-1

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 95 of 102

(Blanking)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Touch Panel

Size	Document Number	Rev
A	**LB475**	**-1**

Date: Tuesday, August 02, 2011 Sheet 96 of 102

CPU Plate

H1 HOLE276R178-GP — ZZ.00PAD.N11
H2 HOLE276R178-GP — ZZ.00PAD.N11
H3 HOLE276R178-GP — ZZ.00PAD.N11

VGA Std-Off

H4 STF237R128H42-1-GP — 34.4GD01.001
H5 STF237R128H42-1-GP — 34.4GD01.001

H16 STF178R69H123-GP — DY — 34.41Z01.001
H17 STF178R69H123-GP — DY — 34.41Z01.001

Check test point

3D3V_S0	AFTP1
3D3V_AUX_S5	AFTP7
3D3V_S5	AFTP8
5V_S5	AFTP9
18,27 PM_PWRBTN#	AFTP10
6,42 H_CPUPWRGD	AFTP11
27,36 S5_ENABLE	AFTP12
9,17,31,65,66,71,83 PLT_RST#	AFTP13

Test Point放在Dimm Door打開可量測處

Structure boss

H7 HOLE335R115-GP — ZZ.00PAD.D01
H9 HOLE335R115-GP — ZZ.00PAD.D01
H10 HOLE335R115-GP — ZZ.00PAD.D01
H11 HOLE335R115-GP — ZZ.00PAD.D01

H8 HOLE256R115-GP — ZZ.00PAD.D11
H12 HOLE256R115-GP — ZZ.00PAD.D11
H13 HOLE256R115-GP — ZZ.00PAD.D11
H15 HOLE256R115-GP — ZZ.00PAD.D11

MiniPCI Std-Off

H14 STF256R89H178-GP — 34.4B417.001

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN# → TP9701 TPAD40-GP, TP9700 TPAD40-GP

POWER TESTING POINT--Bottom

27,68 KBC_PWRBTN# → TP9702 TPAD40-GP, TP9703 TPAD40-GP

AD+
EC9711 DY SCD1U25V2KX-GP
EC9712 DY SCD1U25V2KX-GP

DCBATOUT
EC9723 DY SCD1U25V2KX-GP
EC9724 DY SCD1U25V2KX-GP
EC9725 DY SCD1U25V2KX-GP
EC9722 SCD1U25V2KX-GP
EC9721 DY SCD1U25V2KX-GP
EC9720 DY SCD1U25V2KX-GP
EC9719 SCD1U25V2KX-GP
EC9718 SCD1U25V2KX-GP
EC9717 SCD1U25V2KX-GP

AD_JK
EC9716 DY SCD1U25V2KX-GP
EC9715 SCD1U25V2KX-GP

DCBATOUT
EC9714 SCD1U25V2KX-GP

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/CAP
Size: A3 | Document Number: LB475 | Rev: -1
Date: Tuesday, August 02, 2011 | Sheet 97 of 102

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Change History

Size	Document Number	Rev
A4	**LB475**	**-1**

Date: Tuesday, August 02, 2011 Sheet 98 of 102

POWER SEQUENCE

14,15,46 0D75V_S0 — 0D75V_S0
46 +0D75V_DDR_P — +0D75V_DDR_P
17,27,60 RTC_AUX_S5 — RTC_AUX_S5

4,6,7,9,45 1D2V_S0 — 1D2V_S0
9 1D2V_TRAVIS — 1D2V_TRAVIS
9 AVDD12 — AVDD12
9 DVDD12 — DVDD12
20 1D2V_VPPL_SYS_S5 — 1D2V_VPPL_SYS_S5
20 1D2V_S5 — 1D2V_S5
45 1D2V_PWR — 1D2V_PWR

65 +1D5V_MINI_WLAN — +1D5V_MINI_WLAN
6,20,29,36,65,66 1D5V_S0 — 1D5V_S0
5,6,7,14,15,36,46,51,71,93 1D5V_S3 — 1D5V_S3
5,14,15,46 DDR_VREF_S3 — DDR_VREF_S3
46 DCBATOUT_1D5V — DCBATOUT_1D5V
46 1D5V_PWR — 1D5V_PWR

17,19,20,36 1D1V_S0 — 1D1V_S0
19,20 1D1V_VDDAN_MLDAC_S0 — 1D1V_VDDAN_MLDAC_S0
20 1D1V_VPPL_SYS_S5 — 1D1V_VPPL_SYS_S5
18,20,36,45 1D1V_S5 — 1D1V_S5
45 1D1V_PWR — 1D1V_PWR

6,18,27,28,36,40,41,60,70,92,97 3D3V_AUX_S5 — 3D3V_AUX_S5
6,9,14,15,17,18,20,21,27,28,29,31,36,46,48,49,50,51,56,63,64,65,66,68,71,78,82,85,93,97 3D3V_S0 — 3D3V_S0
6,18,19,20,21,31,36,41,42,45,68,78,79,93,97 3D3V_S5 — 3D3V_S5
6,9 3D3V_S0_TRAVIS — 3D3V_S0_TRAVIS
9 AVDD33 — AVDD33
9 DVDD33 — DVDD33
19,20 3D3V_VDDAN_DAC_S0_R — 3D3V_VDDAN_DAC_S0_R
20 3D3V_VDDPL_SSUSB_S5 — 3D3V_VDDPL_SSUSB_S5
20 3D3V_VDDAN_HWM_S5 — 3D3V_VDDAN_HWM_S5
20 3D3V_VPPL_SYS_S0 — 3D3V_VPPL_SYS_S0
20 3D3V_VDDPL_MLDAC_S0 — 3D3V_VDDPL_MLDAC_S0
20 3D3V_VDDPL_SSUSB_S5 — 3D3V_VDDPL_SSUSB_S5
20 3D3V_VDDPL_USB_S5 — 3D3V_VDDPL_USB_S5
20 3D3V_USB_S5 — 3D3V_USB_S5
27,39,60 3D3V_AUX_KBC — 3D3V_AUX_KBC
29 AUD_3VD — AUD_3VD
31,59 3D3V_LAN_S5 — 3D3V_LAN_S5
31 3D3V_LAN_VDDSREG — 3D3V_LAN_VDDSREG
41 3D3V_PWR — 3D3V_PWR
41 PWR_3D3V_DCBATOUT — PWR_3D3V_DCBATOUT
41 3D3V_PWR_2 — 3D3V_PWR_2
49 3D3V_CAMERA_S0 — 3D3V_CAMERA_S0
65 +3V_MINI_WLAN — +3V_MINI_WLAN
63 3D3V_BT_S0 — 3D3V_BT_S0
83,85,86,92,93 3D3V_VGA_S0 — 3D3V_VGA_S0

86 VDDC_CT — VDDC_CT
86 PCIE_PVDD — PCIE_PVDD
86 MPV18 — MPV18
86 SPV10 — SPV10
86 SPV18 — SPV18
86 BIF_VDDC — BIF_VDDC
85 A2VDD — A2VDD
85 AVDD — AVDD
85 VDD1DI — VDD1DI
85 VDD2DI — VDD2DI
85 A2VDDQ — A2VDDQ

48 2D5V_PWR — 2D5V_PWR
7,48 2D5V_S0 — 2D5V_S0

7,42,43 APU_VDDNB — APU_VDDNB

9 RUN_ENABLE_TRAVIS — RUN_ENABLE_TRAVIS
9,36 RUN_ENABLE_S — RUN_ENABLE_S
36 RUN_ENABLE_HV — RUN_ENABLE_HV

31 1D05V_LAN_S5 — 1D05V_LAN_S5

83,85,86,87,93 1V_VGA_S0 — 1V_VGA_S0
84,86,88,89,90,91,93 1D5V_VGA_S0 — 1D5V_VGA_S0

36,40,41,42,43,45,46,49,92,97 DCBATOUT — DCBATOUT
38,97 AD_JK — AD_JK
38,40,97 AD+ — AD+
39,40 BT+ — BT+

9,36,41,42,45,46,48,61,62,65,68,78,82,92,93,97 5V_S5 — 5V_S5
20,28,29,36,50,51,56,64,69,78,86 5V_S0 — 5V_S0
29 AUD_5VA — AUD_5VA
36,40,41,42,43,45,46,49,92,97 PWR_DCBATOUT_VGA_CORE — DCBATOUT

87 DPAB_VDD18 — DPAB_VDD18
87 DPCD_VDD18 — DPCD_VDD18
87 DPCD_VDD10 — DPCD_VDD10

41 5V_PWR_2 — 5V_PWR_2
41 5V_PWR — 5V_PWR
41 PWR_5V_DCBATOUT — PWR_5V_DCBATOUT

50,51 5V_CRT_S0 — 5V_CRT_S0
57,59,62 5V_USB0_S3 — 5V_USB0_S3
61,82 5V_RUSB3_S0 — 5V_RUSB3_S0
62 5V_LUSB1_S0 — 5V_LUSB1_S0

49 DCBATOUT_LCD — DCBATOUT_LCD
49 LCDVDD — LCDVDD
7,42 APU_VDD — APU_VDD
60 +RTC_VCC — +RTC_VCC

85,86,87,93 1D8V_VGA_S0 — 1D8V_VGA_S0

86,92 VGA_CORE — VGA_CORE

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER SEQUENCE

Size	Document Number	Rev
A3	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 99 of 102

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

Size	Document Number	Rev
A3	**LB475**	**-1**
Date: Tuesday, August 02, 2011	Sheet 100 of 102	

<Variant Name>

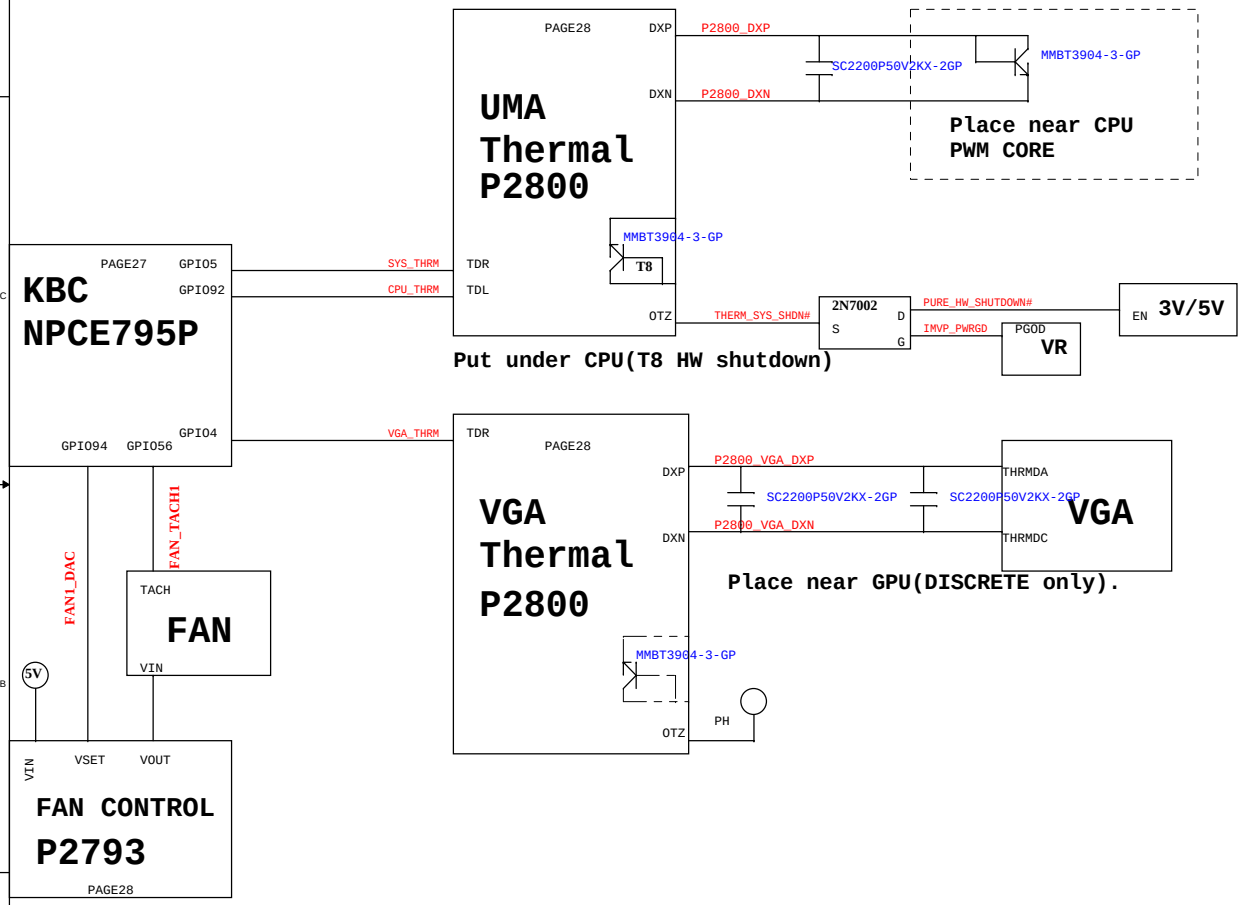
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SMBUS BLOCK DIAGRAM***

Size	Document Number	Rev
A2	LB475	-1

Date: Tuesday, August 02, 2011 Sheet 101 of 102

Thermal Block Diagram



Audio Block Diagram

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: THERMAL/AUDIO BLOCK DIAGRAM		
Size: Custom	Document Number: LB475	Rev: -1
Date: Tuesday, August 02, 2011	Sheet 102 of 102	