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- BT BD

Thermal Sensor EMC2103 1,2

Clock GEN CK505 3

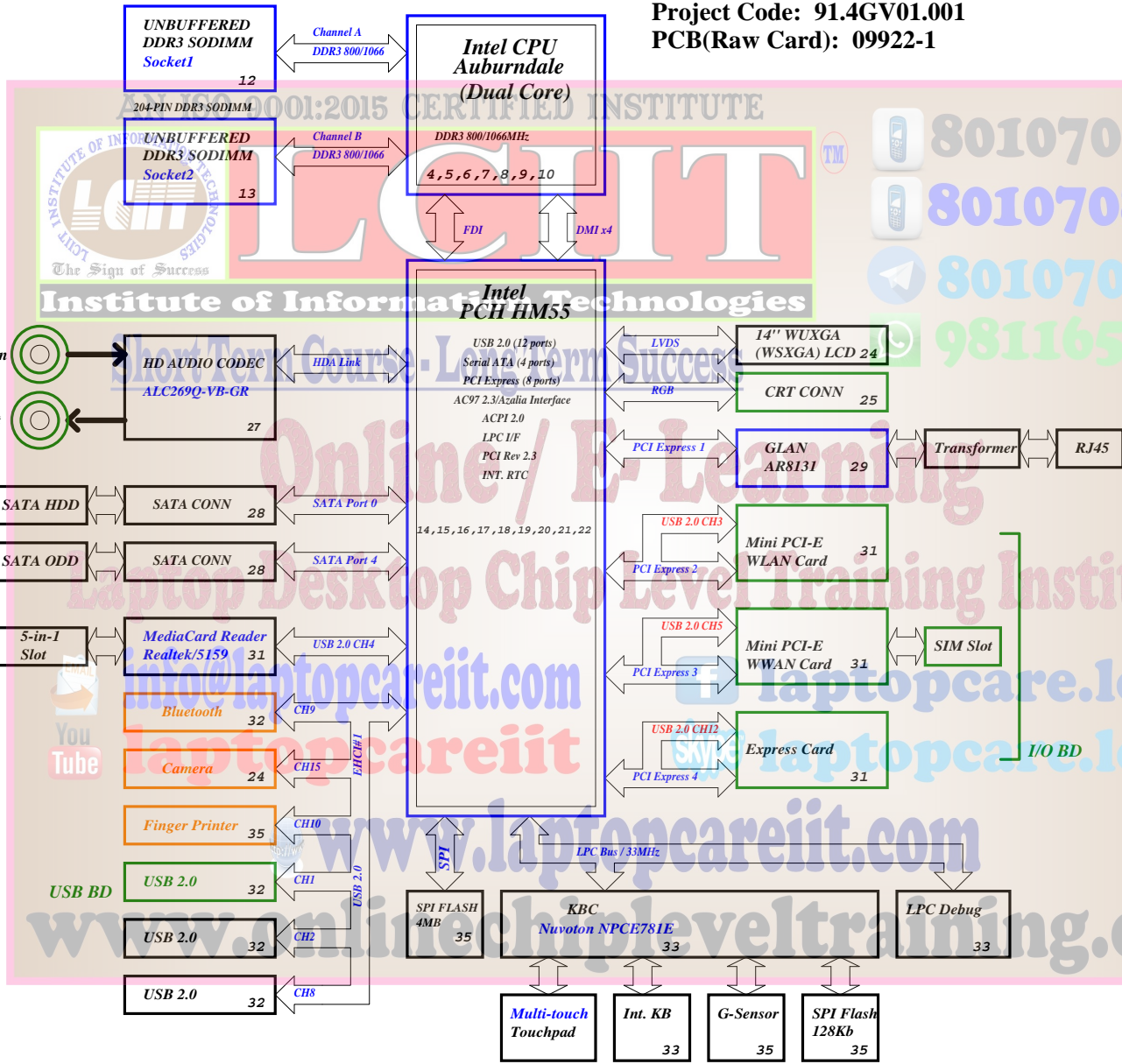
LA46 UMA Block Diagram

LA46-UMA-1_0104

Project Code: 91.4GV01.001

PCB(Raw Card): 09922-1

PCB LAYER	
L1:	Top
L2:	VCC
L3:	Signal
L4:	Signal
L5:	GND
L6:	Bottom



CPU DC/DC ISL62882 38, 39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51123 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8209E 41	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC RT8209E 42	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO RT9025 43	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO RT9026 43	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC ISL62881 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

CHARGER BQ24745 46	
INPUTS	OUTPUTS
DCBATOUT	BT+

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Block Diagram		
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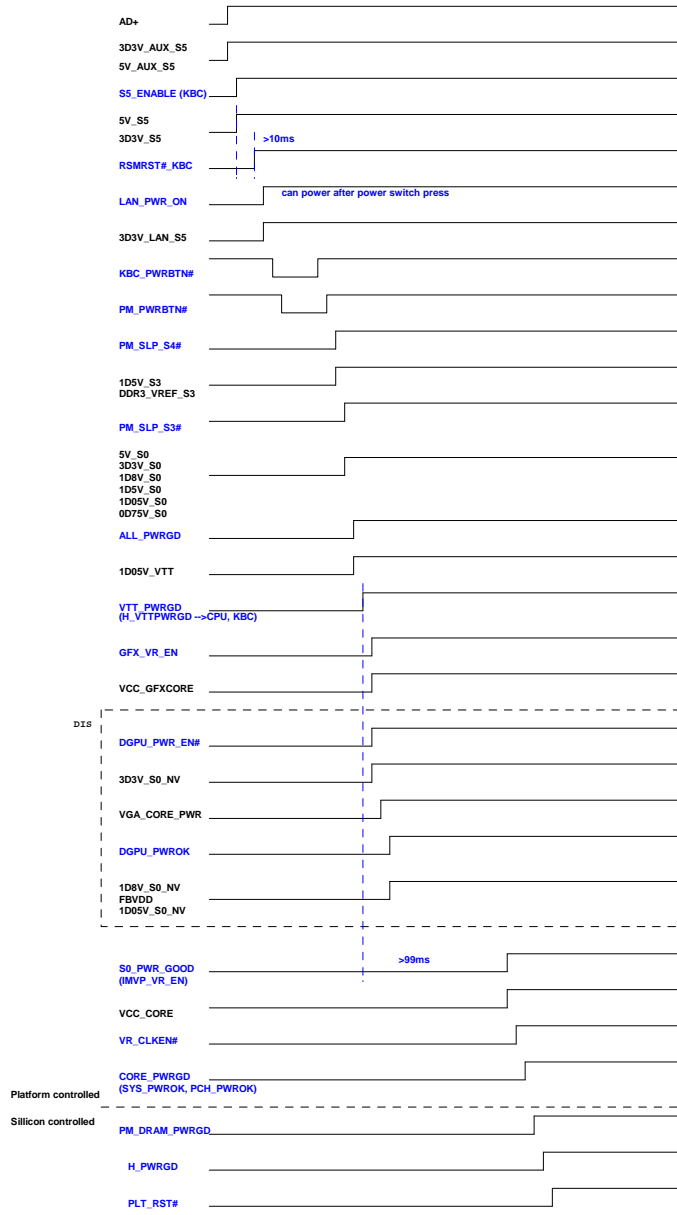
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01k Ohm/5% resistor. Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCH Strapping

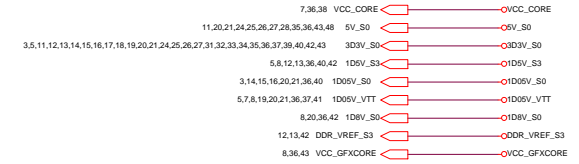
Name	Schematics Notes
SFKR	Reboot option at power-up Default Mode: Internal weak pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_SVB	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable MB in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_ENH /GPIO133	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Sequence AC



PLANAR_ID[1..0]

KBC GPin	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0	LA46_UMA-SA	SA
	0	0	LA46_UMA-SB	SB
	0	1	LA46_UMA-SC	SC
	1	0	LA46_UMA-1	-1

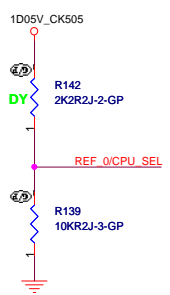
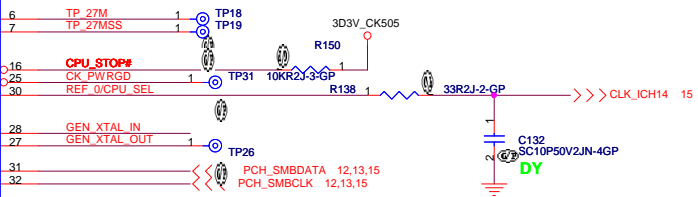
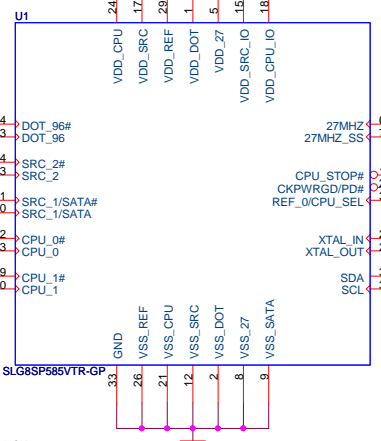
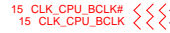
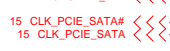
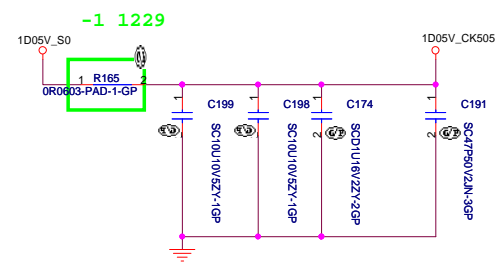
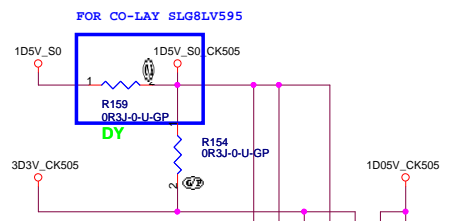
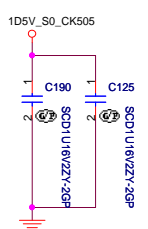
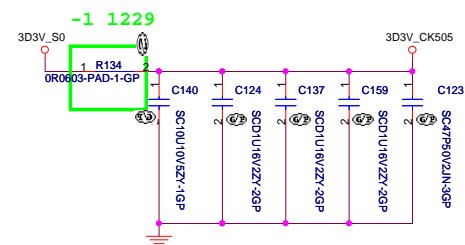


Platform controlled

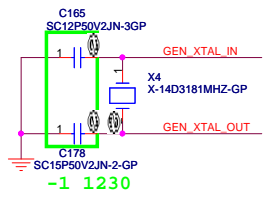
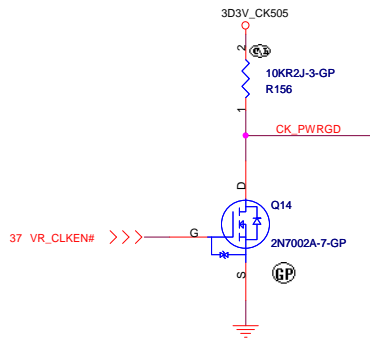
Silicon controlled

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A2	Document Number LA46-UMA	1
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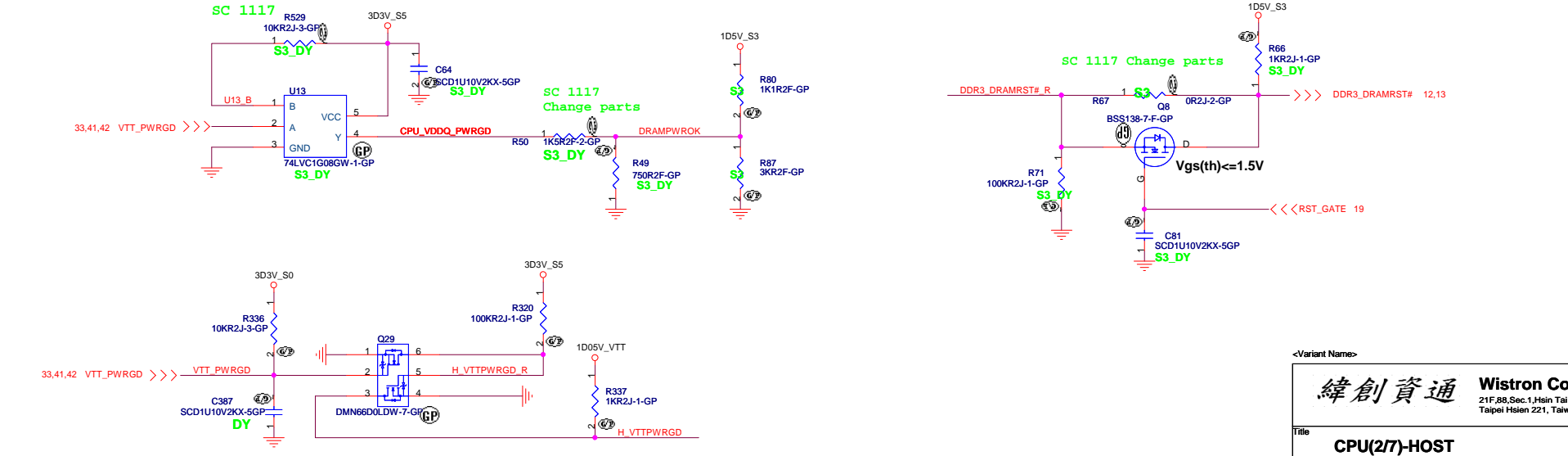
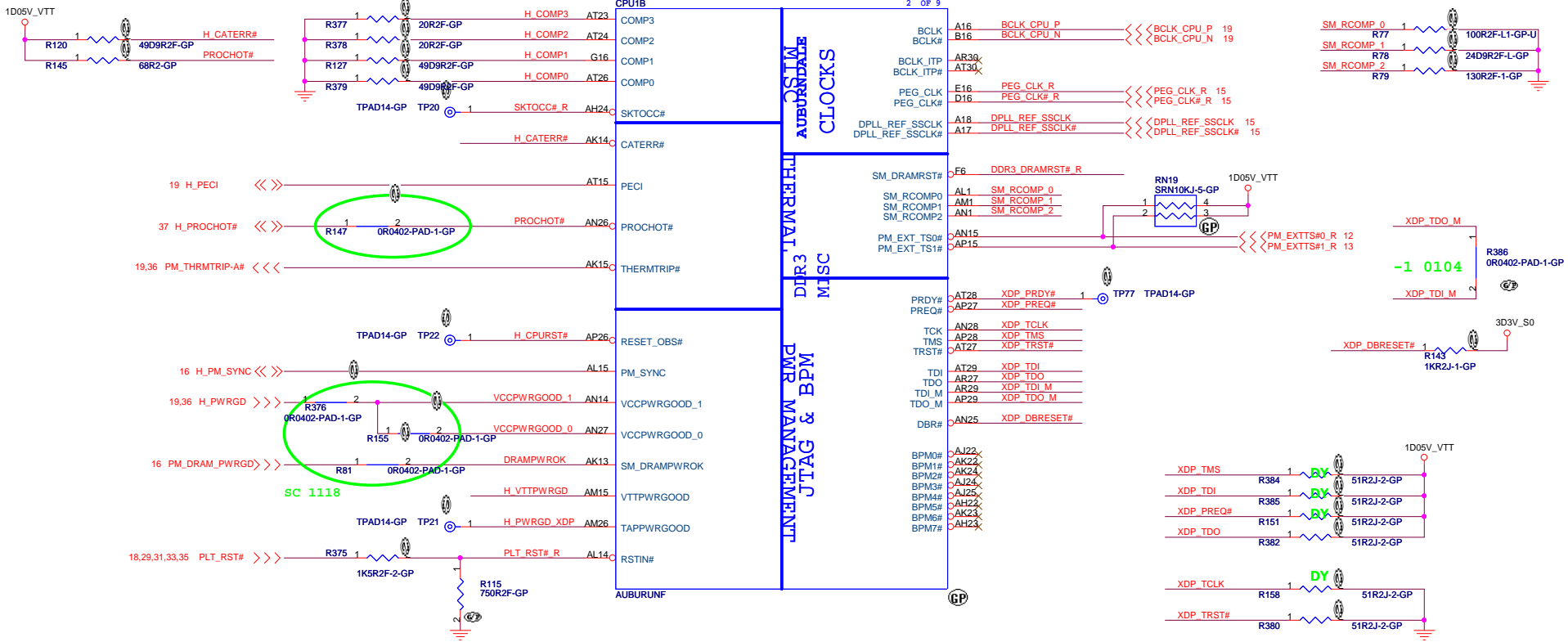


FSC	0	1
SPEED	133MHz (Default)	100MHz



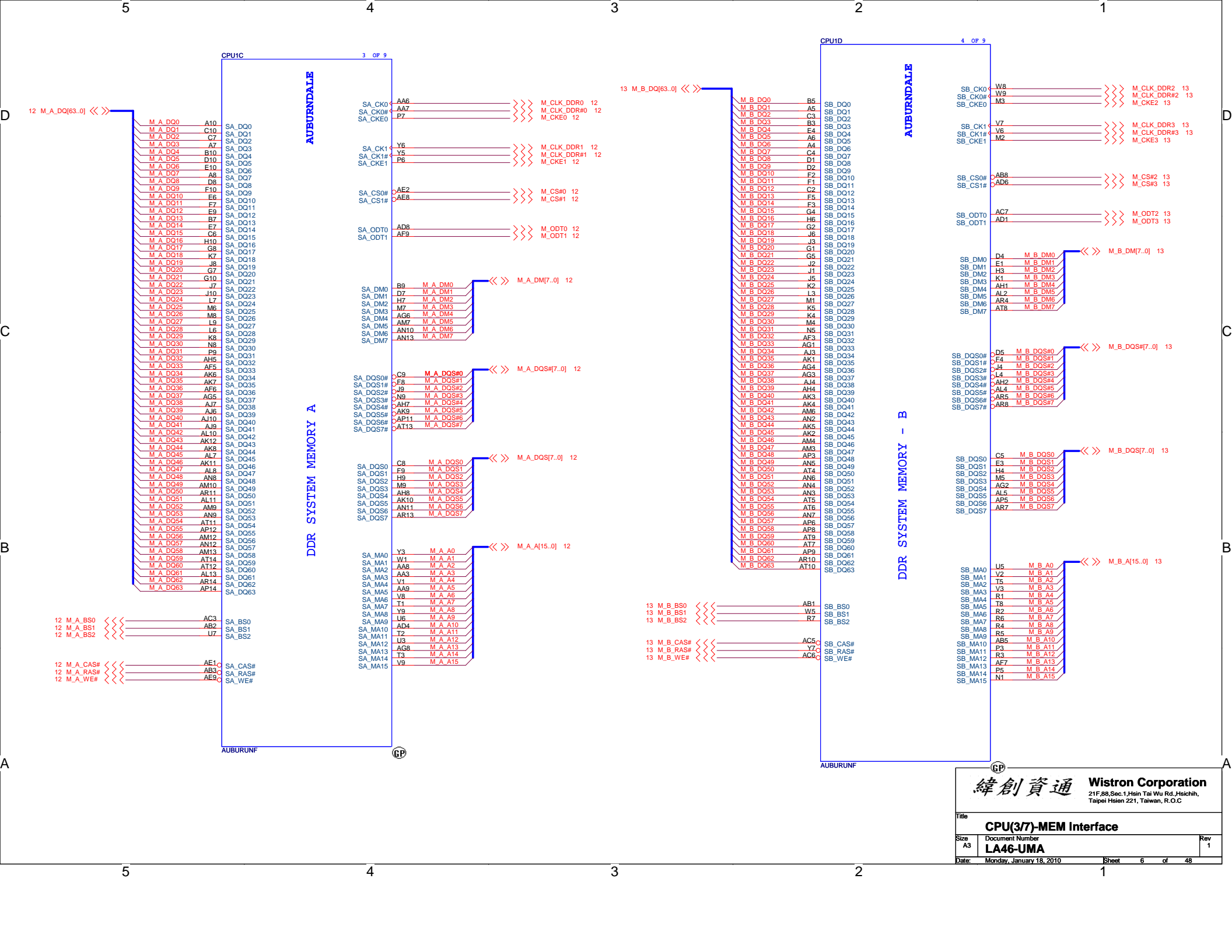
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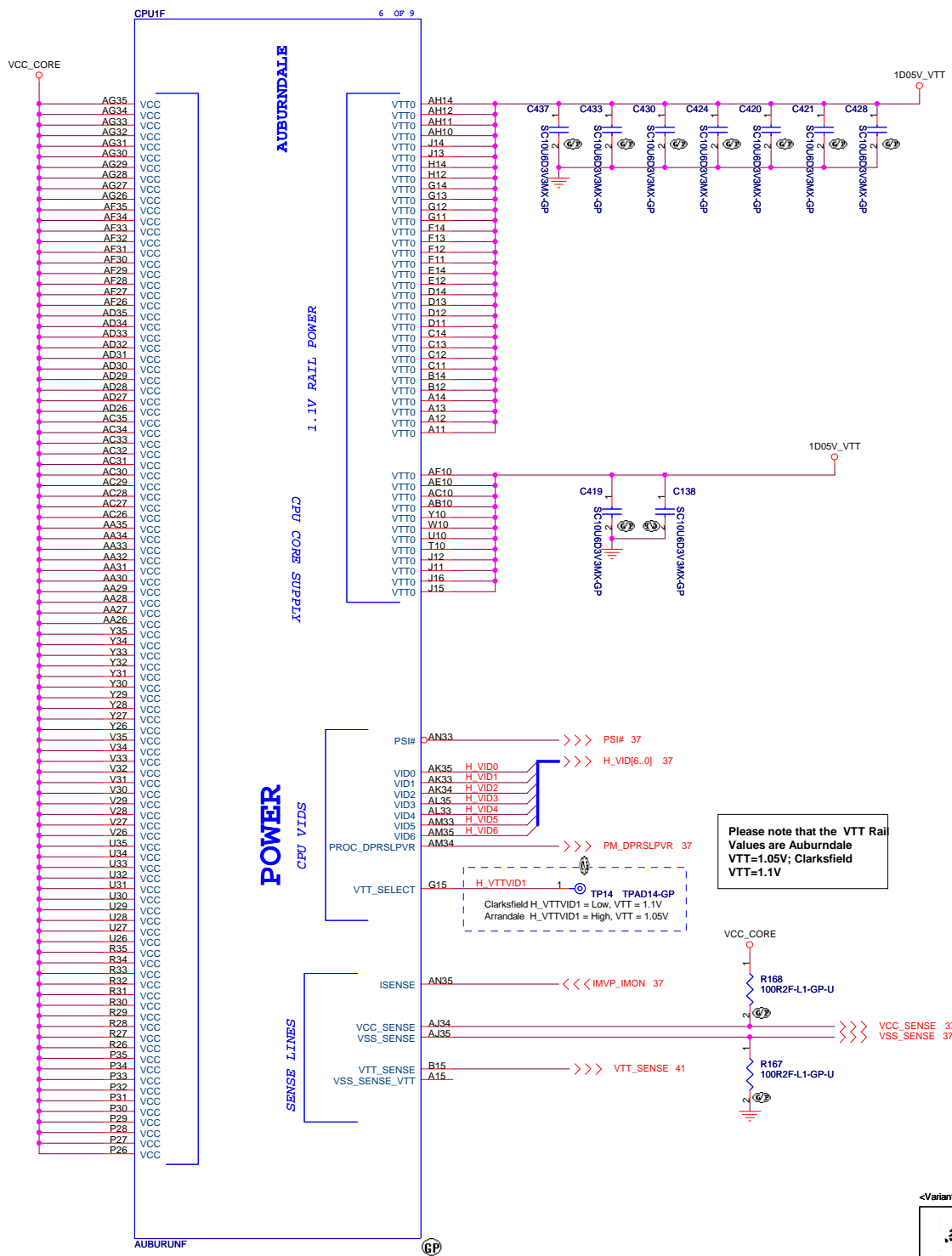
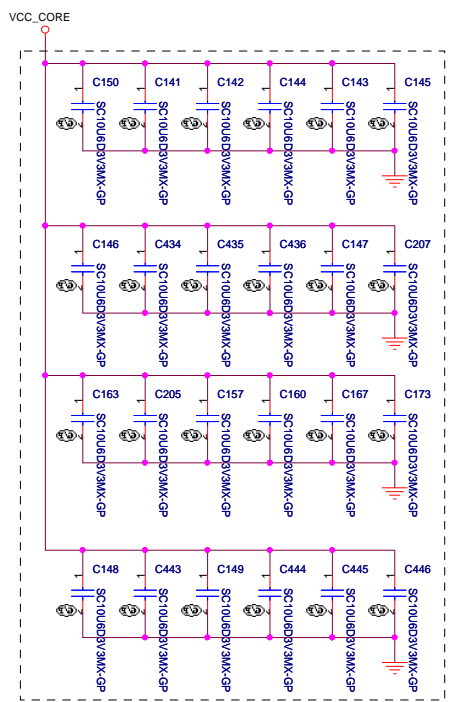
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CLKGEN.		
Size	Document Number	Rev
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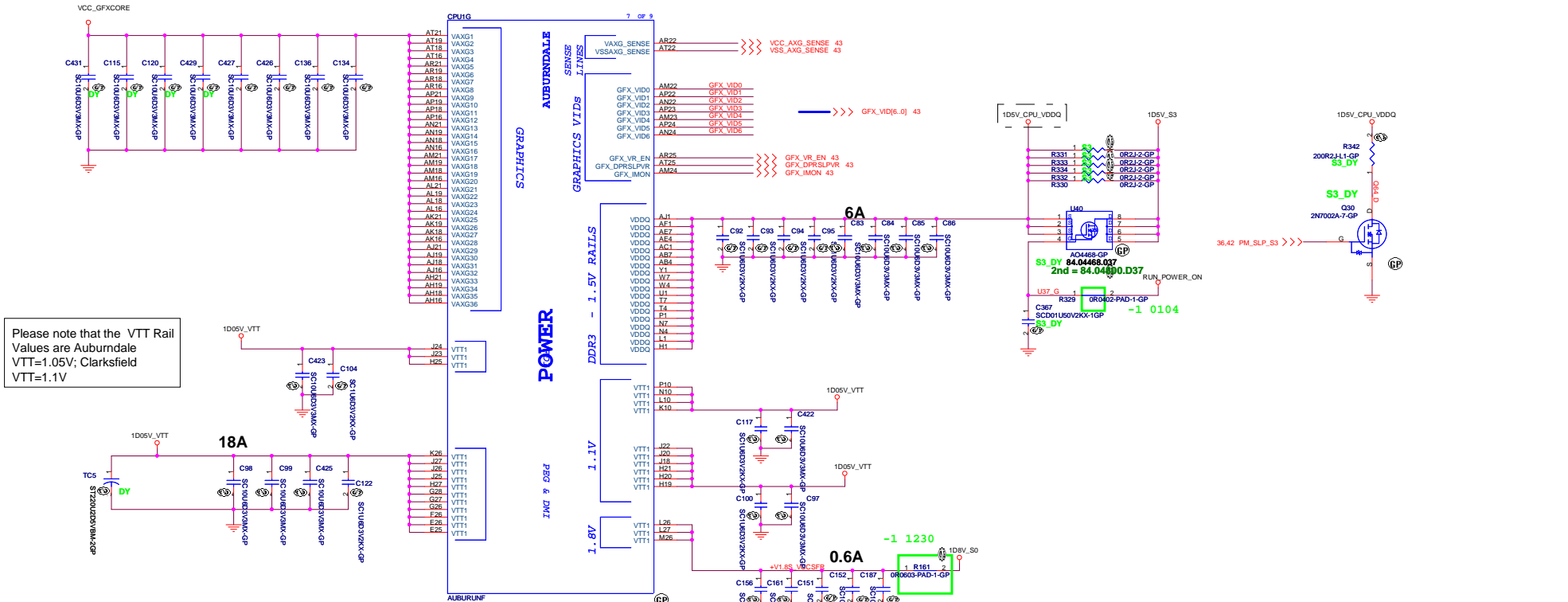
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Title			
CPU(27)-HOST			
Size			
LA46-UMA			
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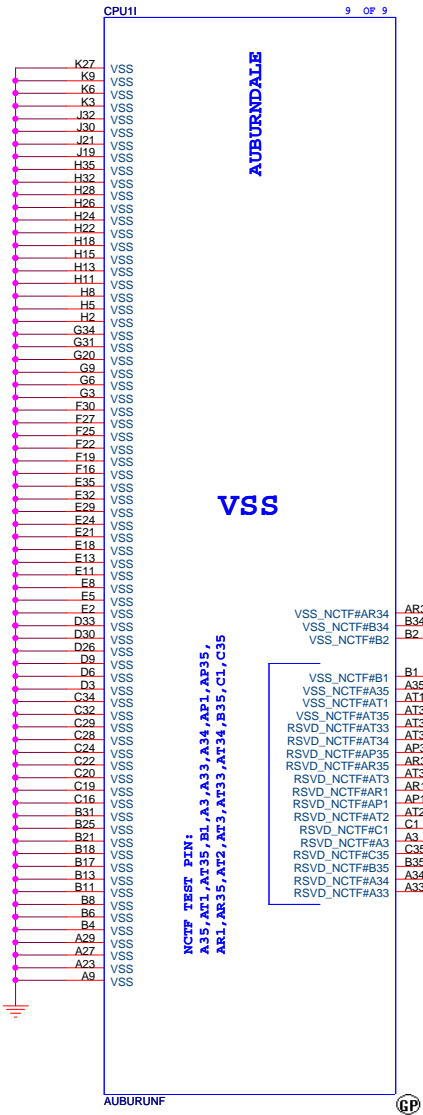
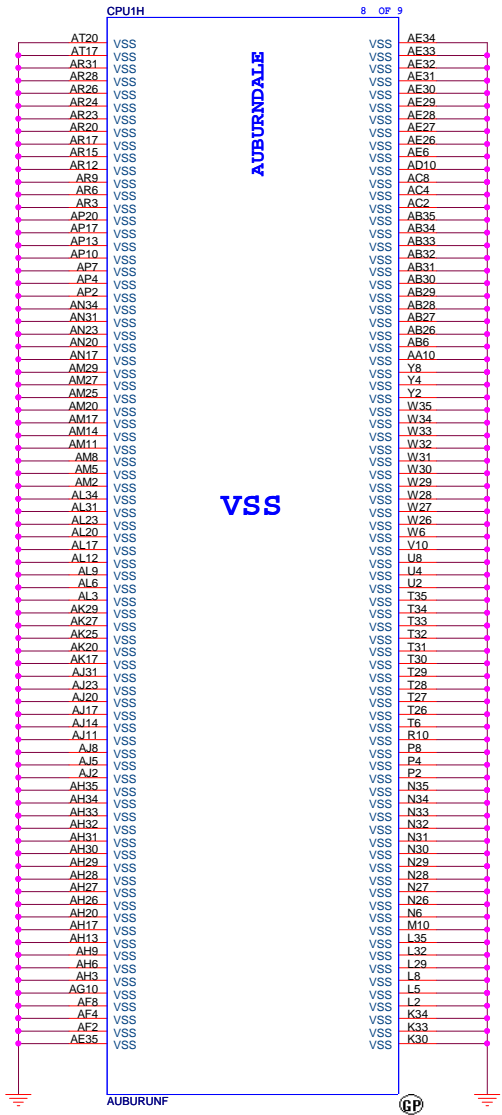




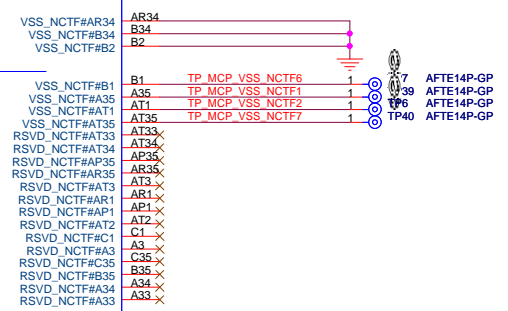
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksville VTT=1.1V

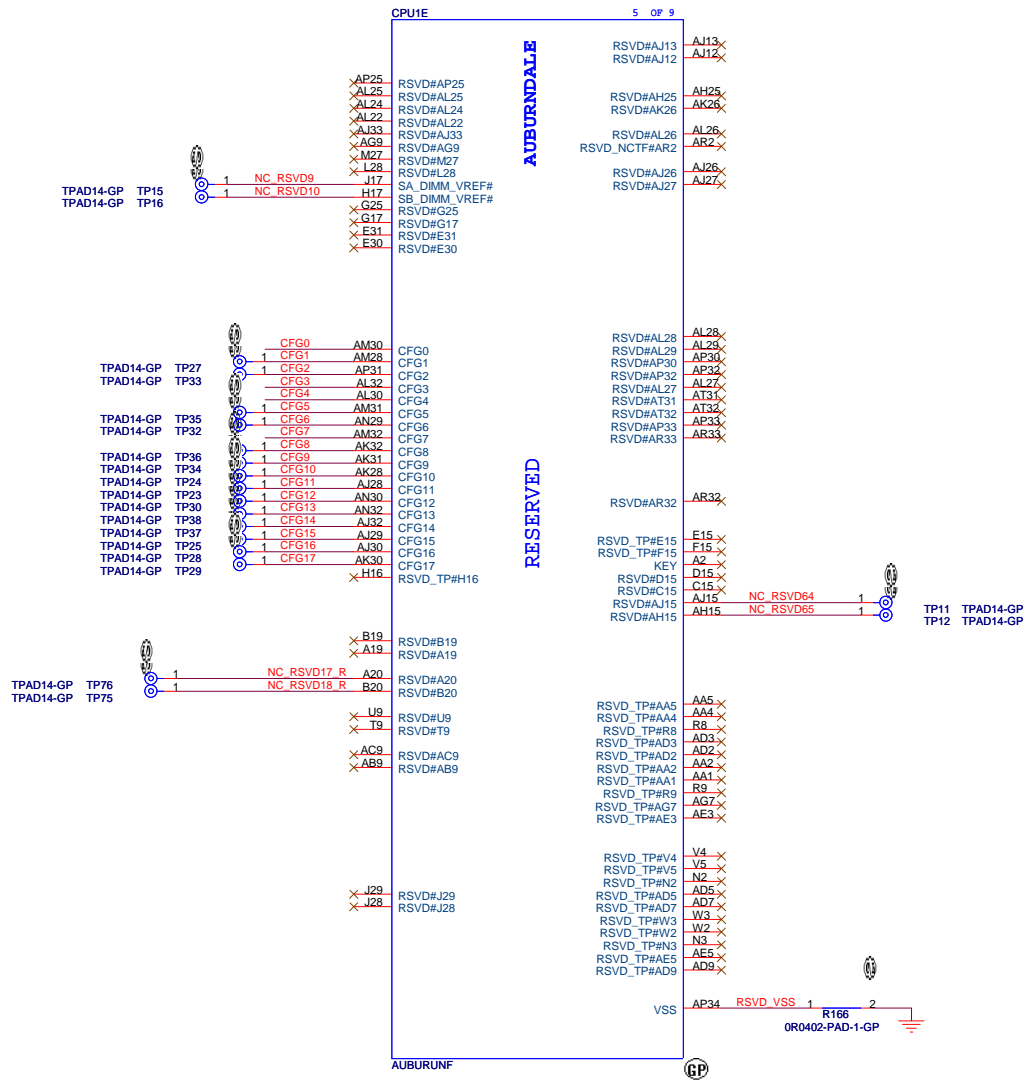


Please note that the VTT Rail Values are Auburndale
 VTT=1.05V; Clarkfield
 VTT=1.1V



NCTF TEST PIN:
 A35, AT1, AR35, BL, A3, A33, A34, AP1, AP35,
 AR1, AR35, AT2, AT3, AT33, AT34, B35, C1, C35





PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1:Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

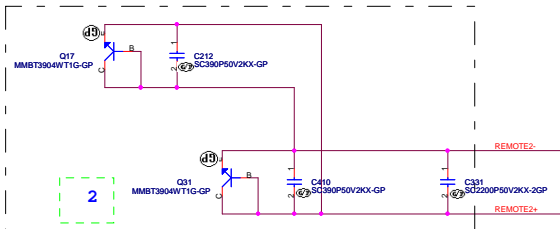
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW/33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

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Title		
CPU(77)-RESERVED		
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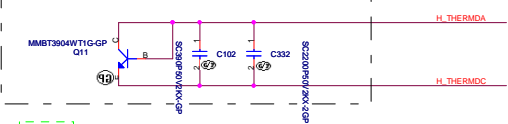
3 Close to PCH on top side.



AMBIENT TEMP:
 REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing. Locate Cap near thermal diode.

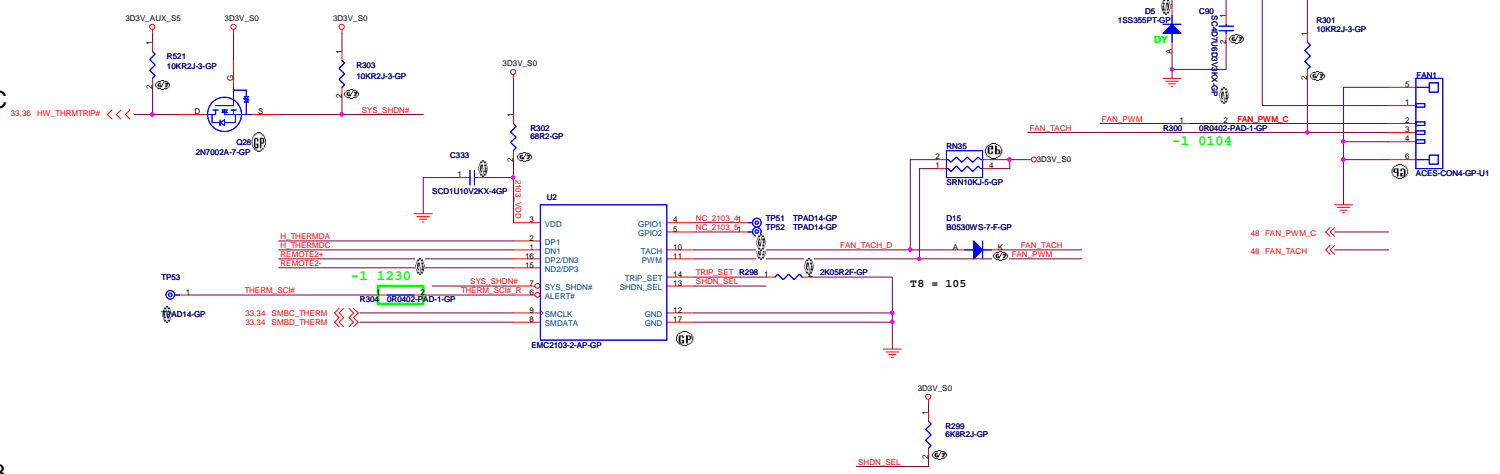
CPU TEMP:

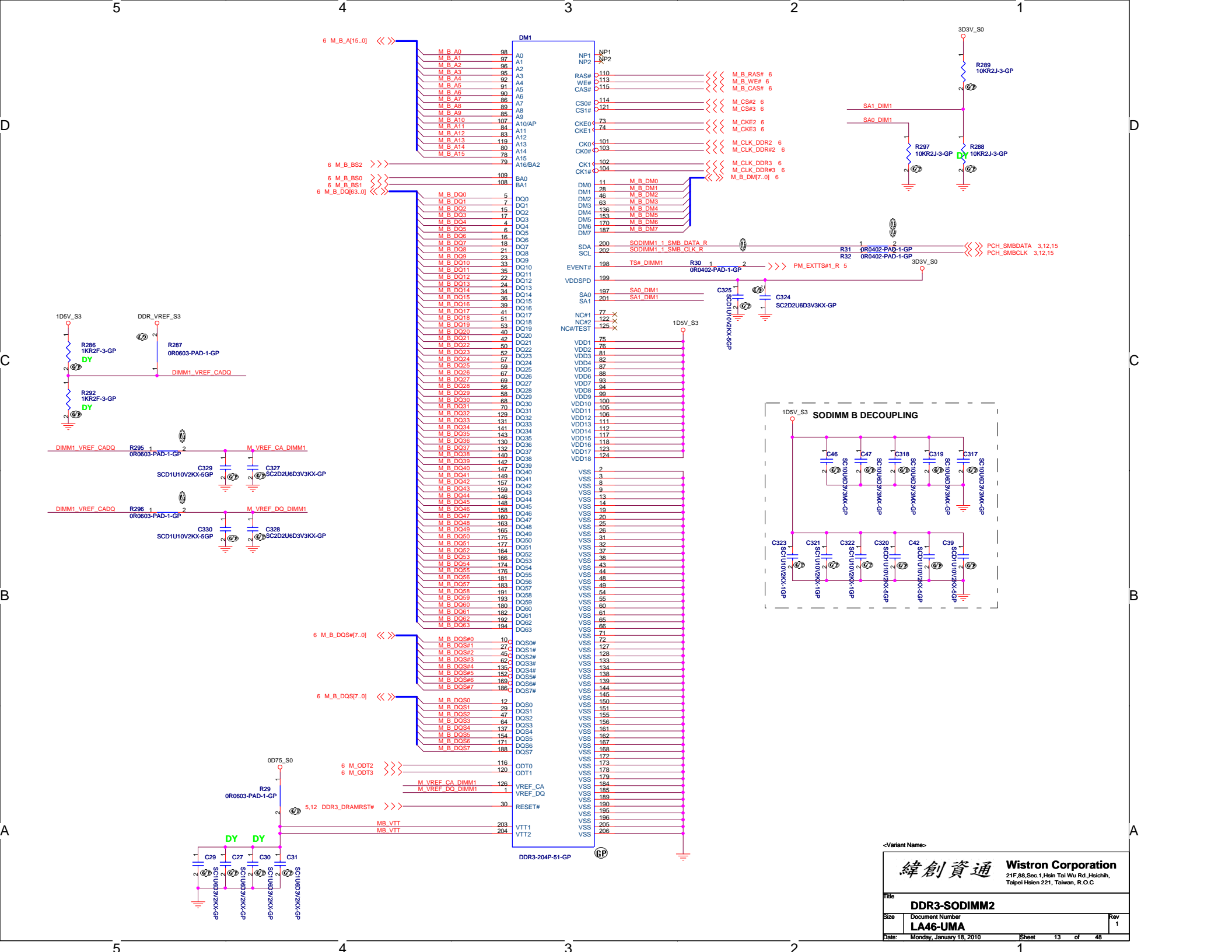
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

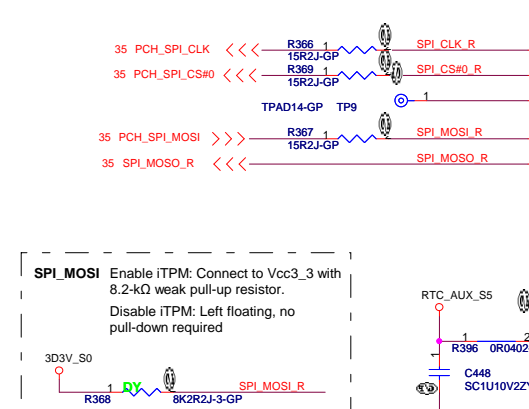
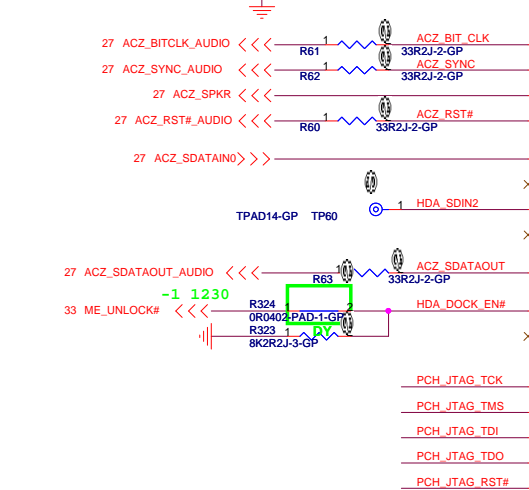
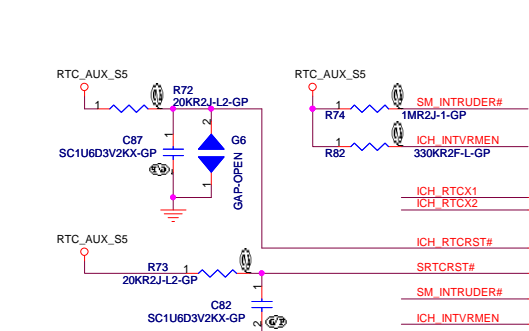
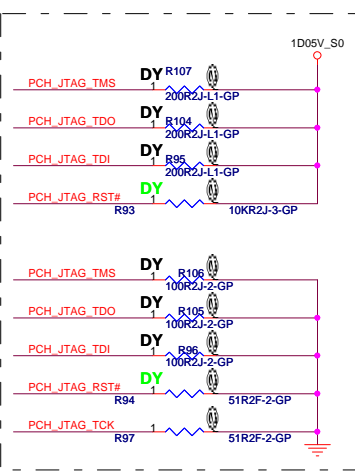
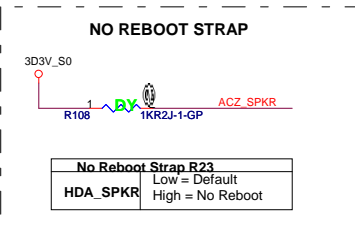
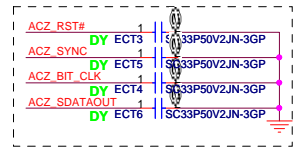
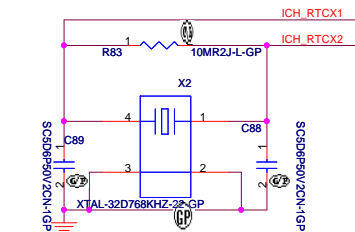


1 CPU backside or inside the socket

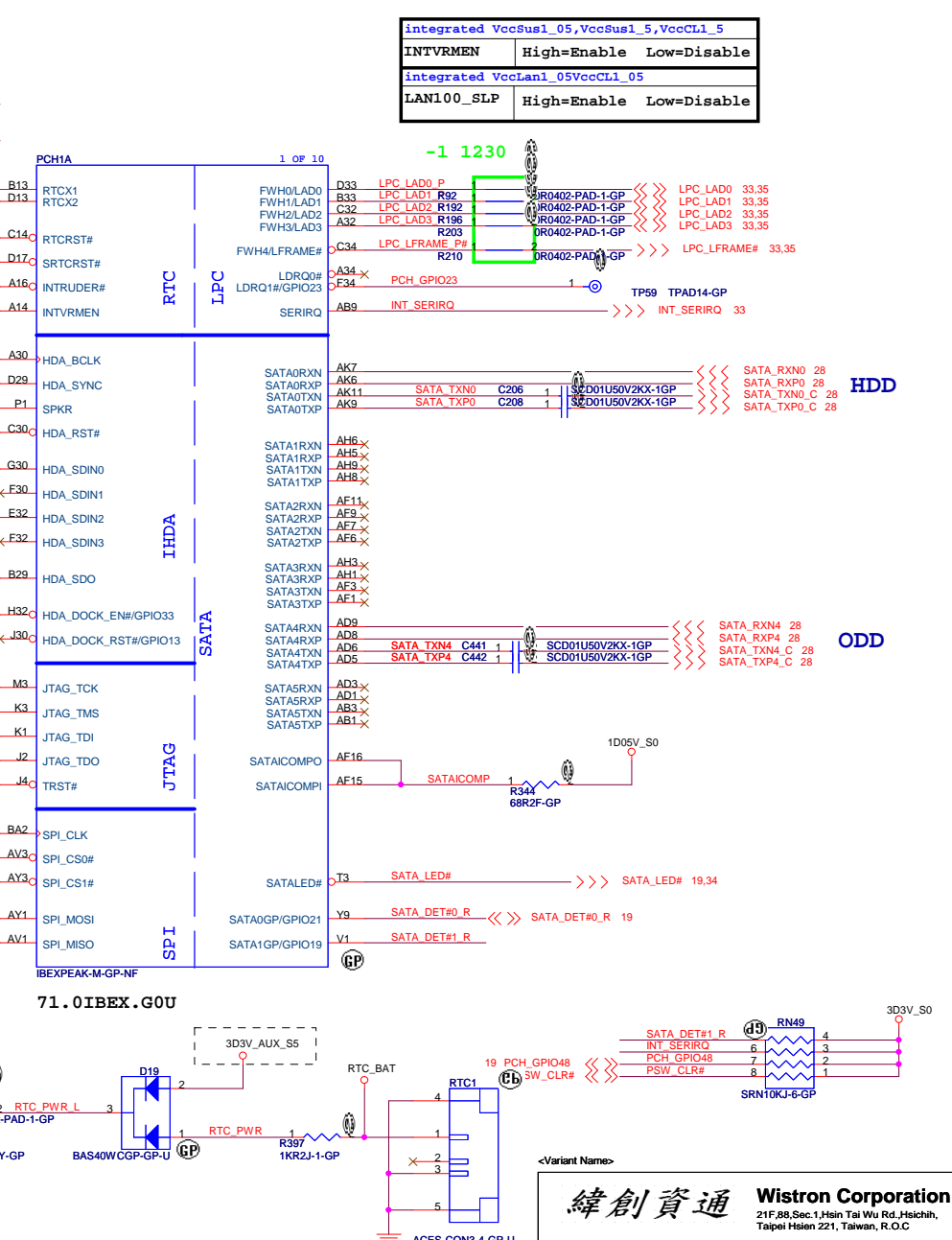
4 WIRE PWM Fan Control circuit



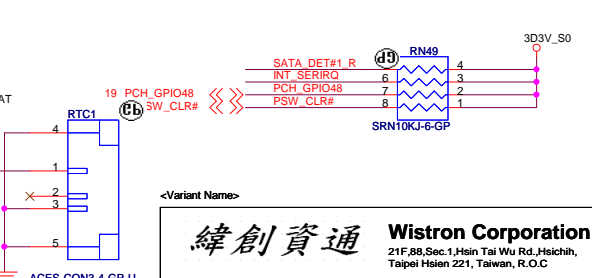
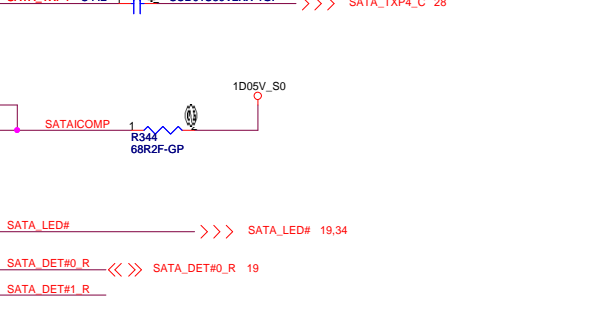
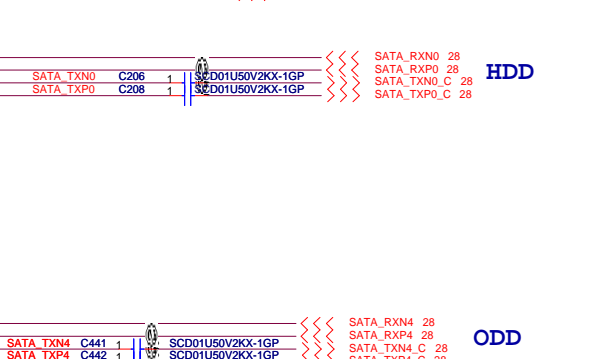
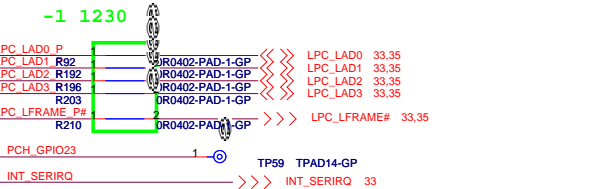




SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required



integrated VccSus1_05,VccSus1_5,VccCl1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCl1_05		
LAN100_SLP	High=Enable	Low=Disable



<Variant Name>

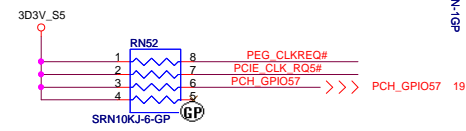
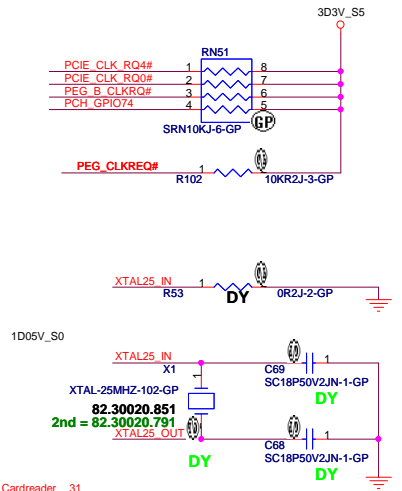
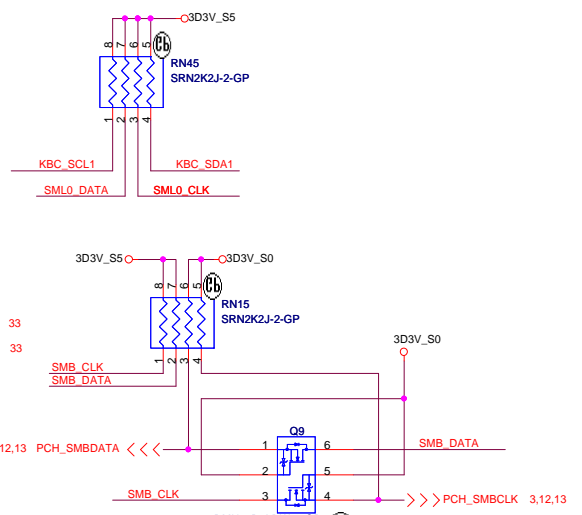
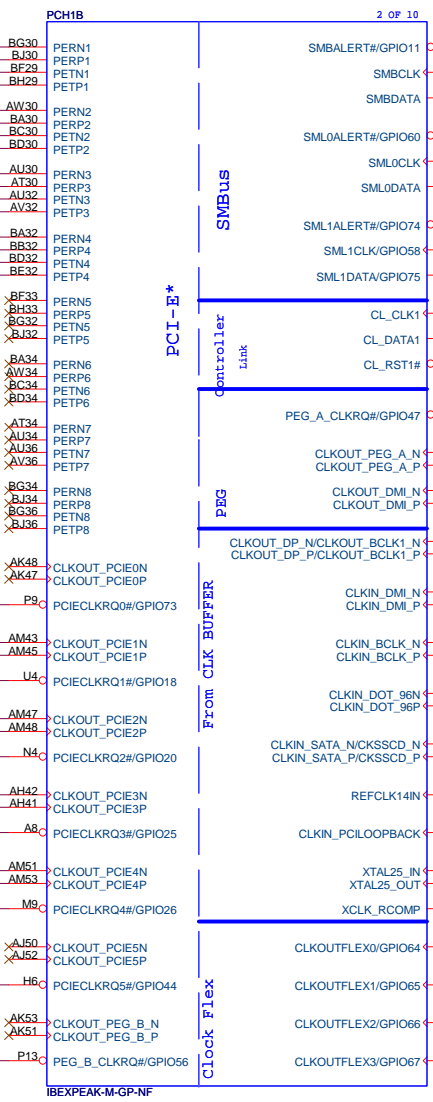
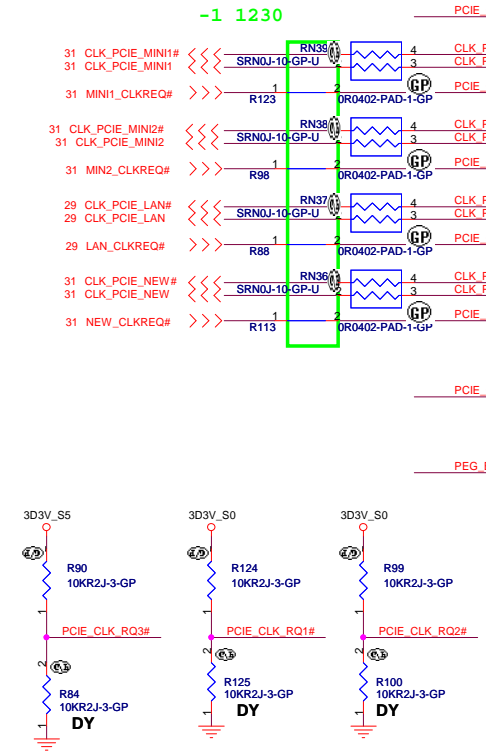
Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C	
Title	PCH (I9)-SATA / SPI / LPC
Size	LA46-UMA
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LAN

MINICARD1

MINICARD2

NEW CARD

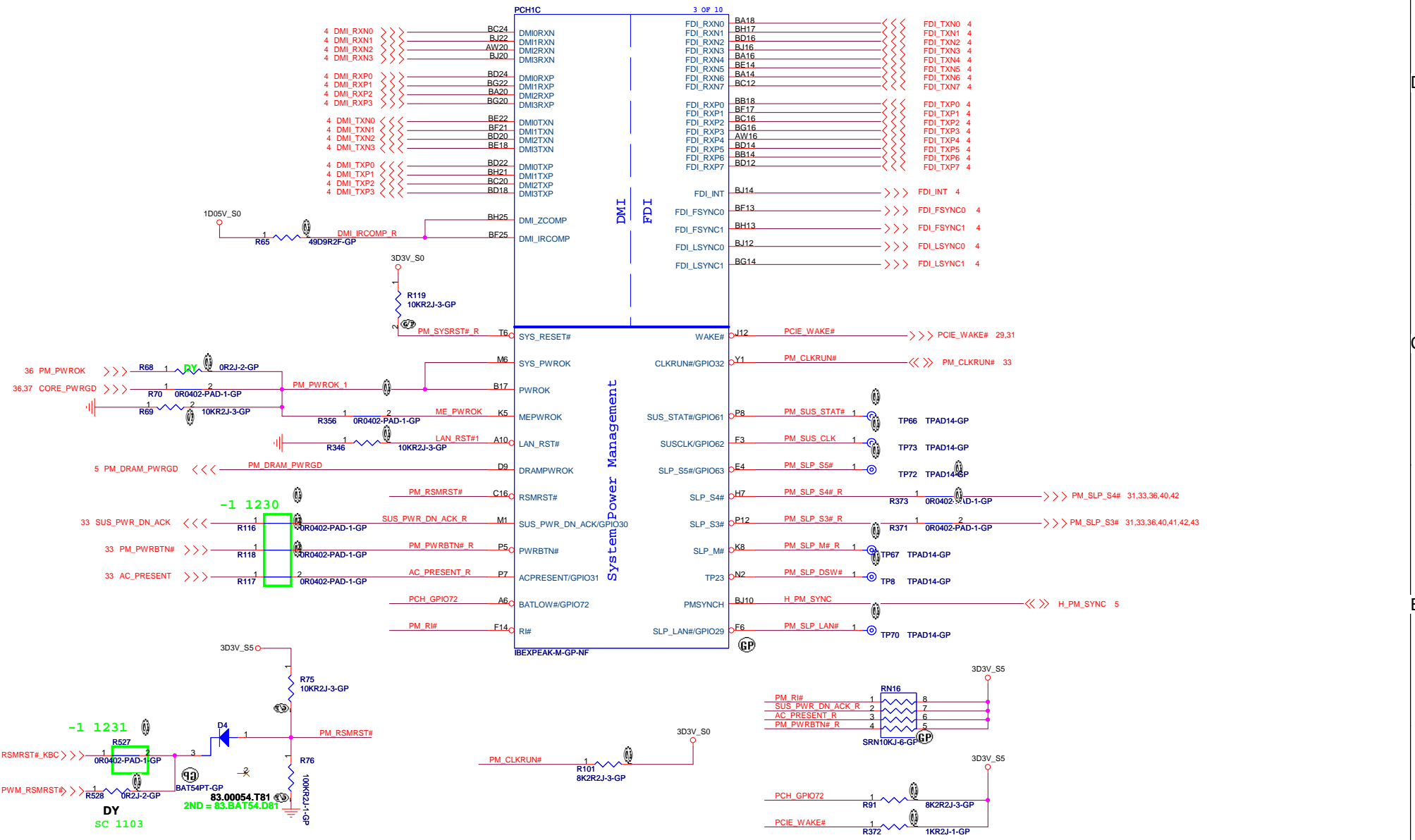


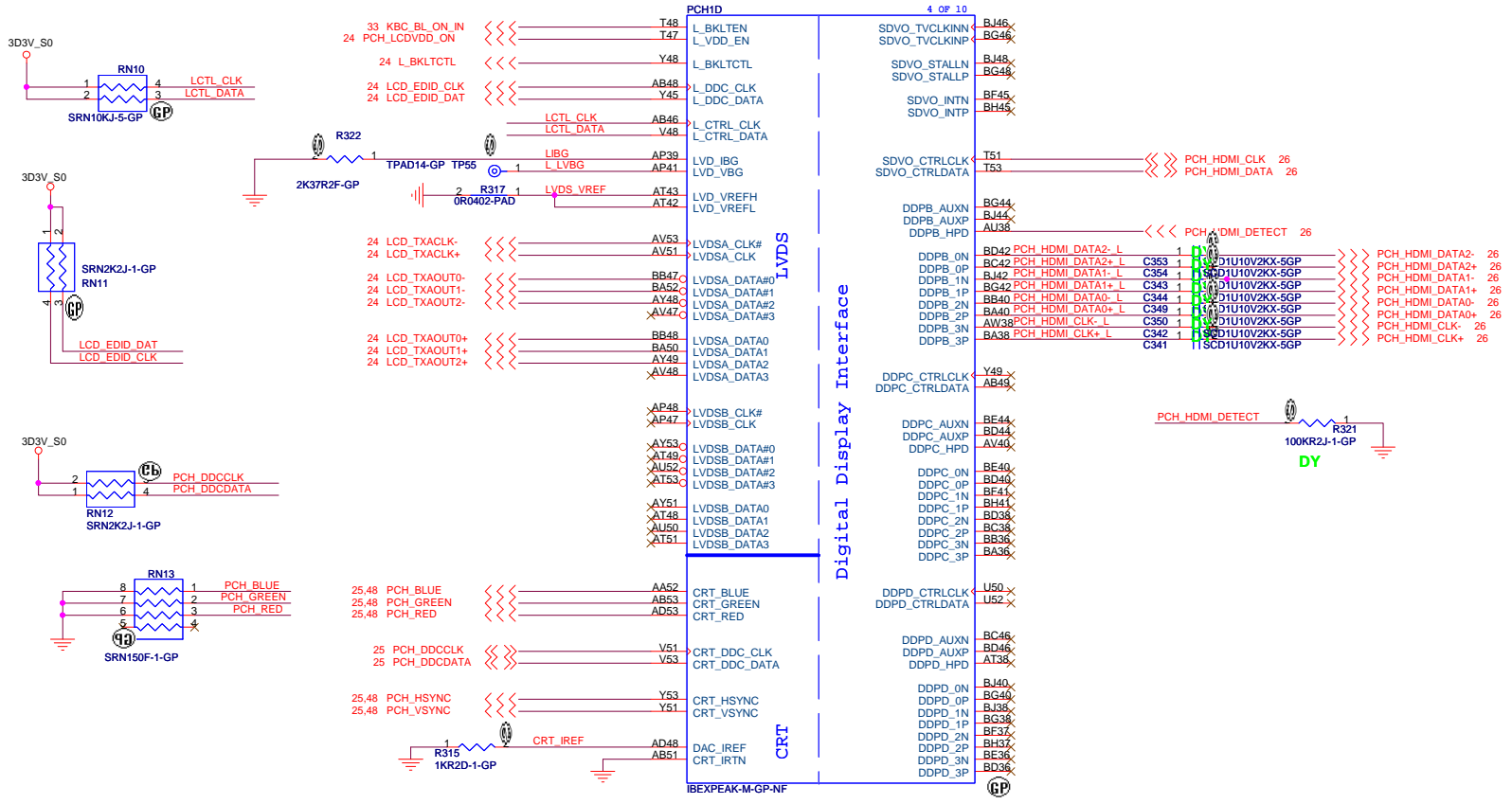
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Title: **PCH (2/9)-PCIE / SMBUS / CLK**

Size: A3 Document Number: **LA46-UMA** Rev: 1

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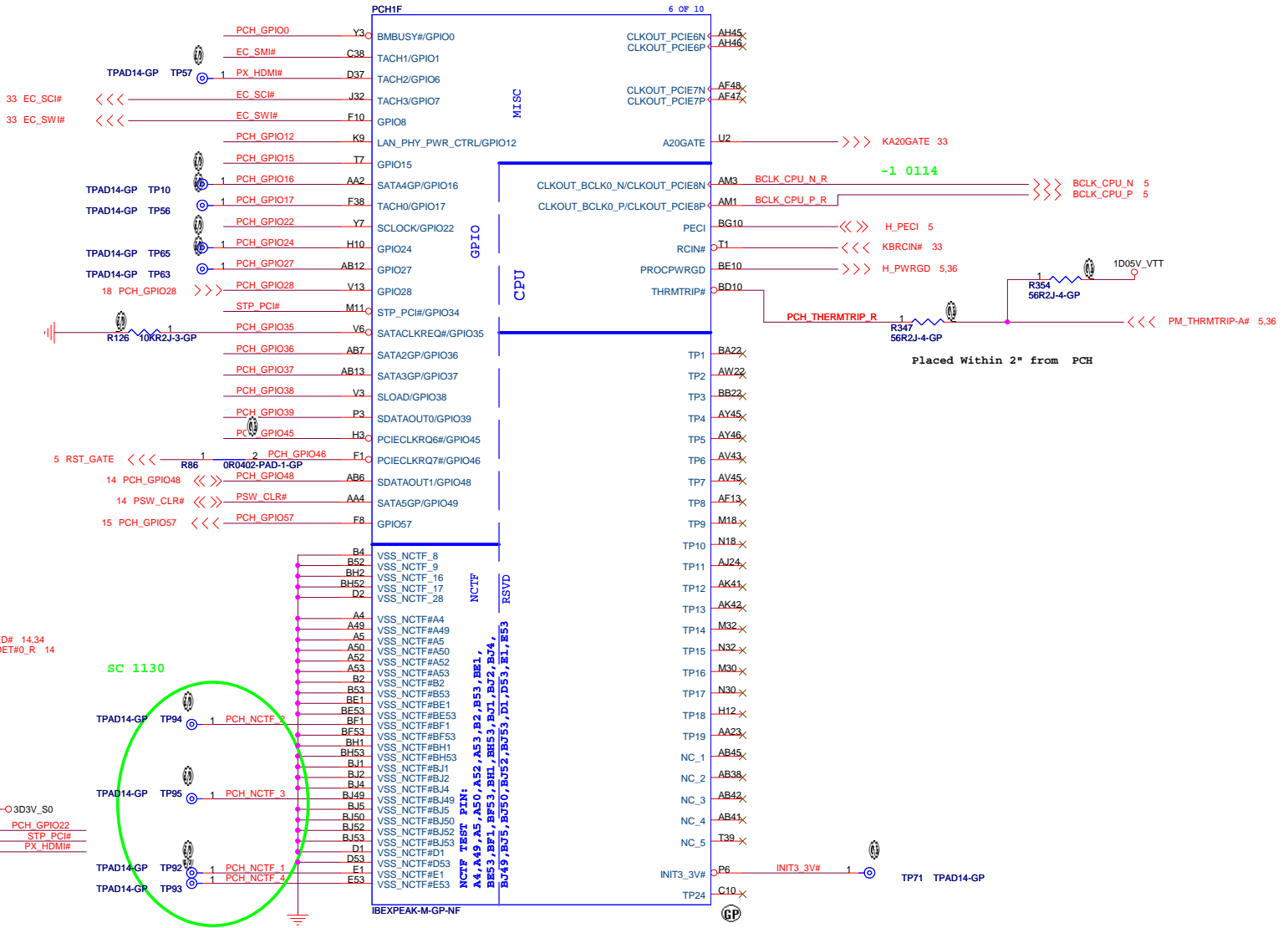
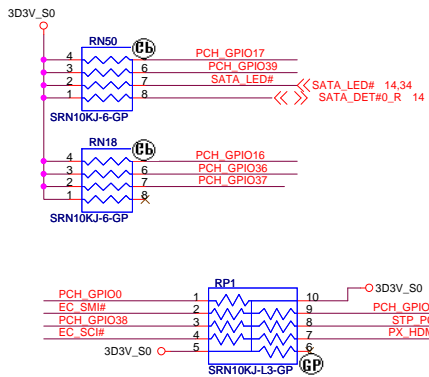
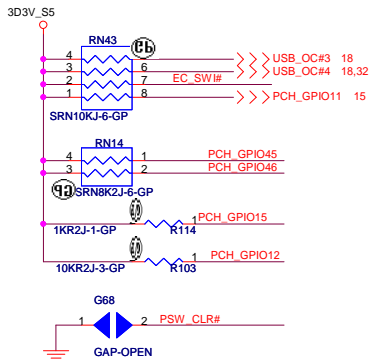
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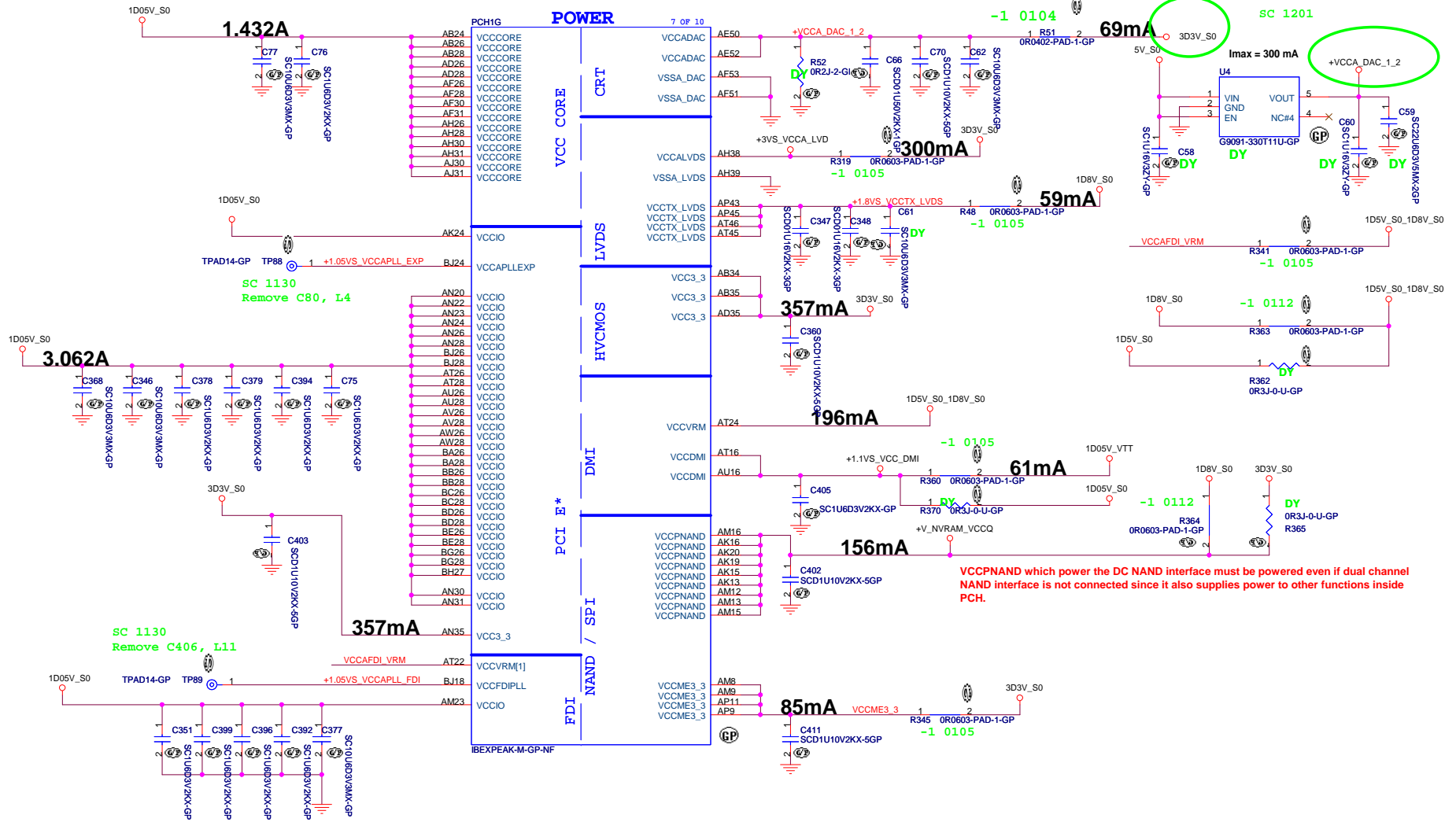
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Size	Document Number	Rev	
A3	LA46-UMA	1	
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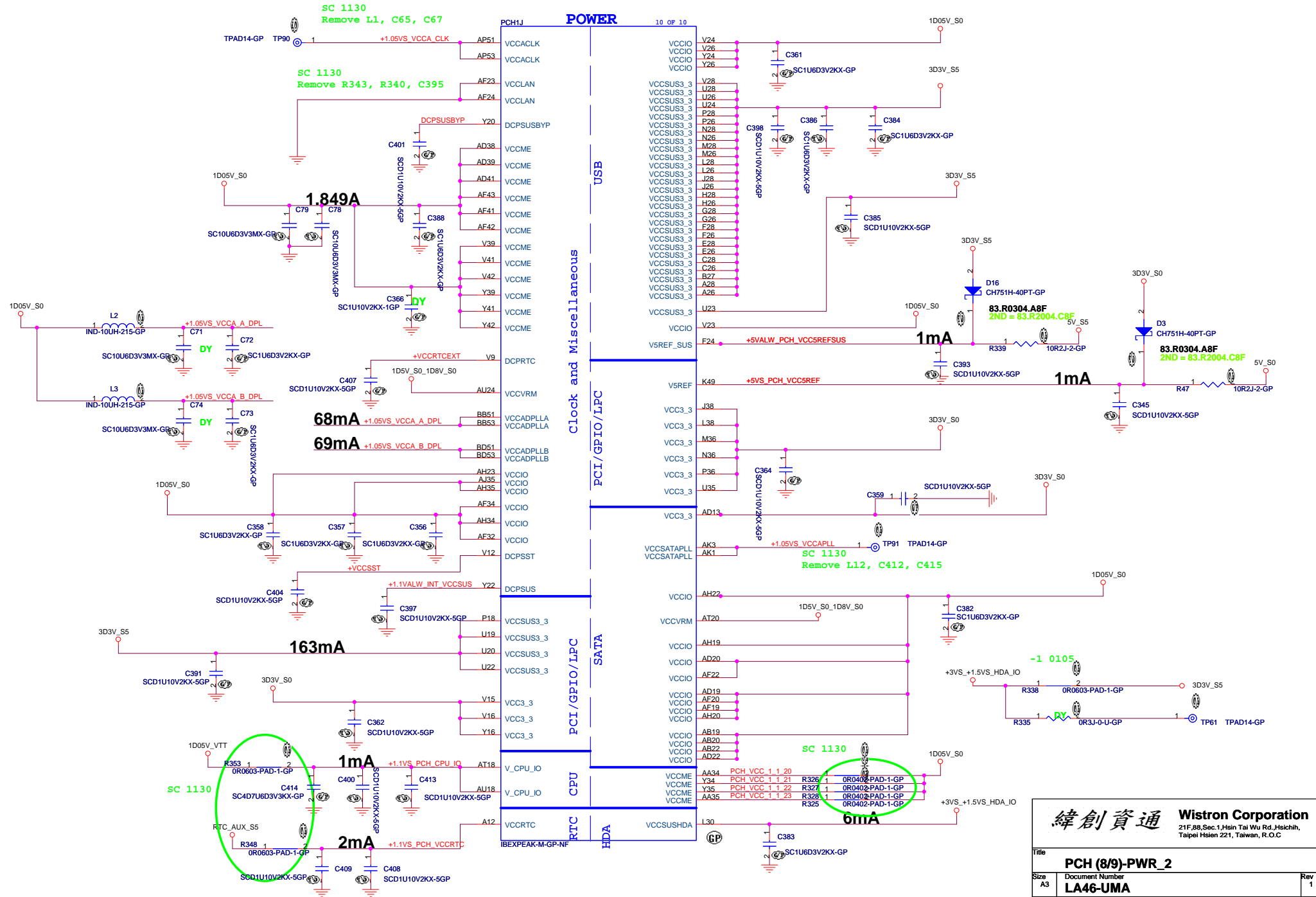
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

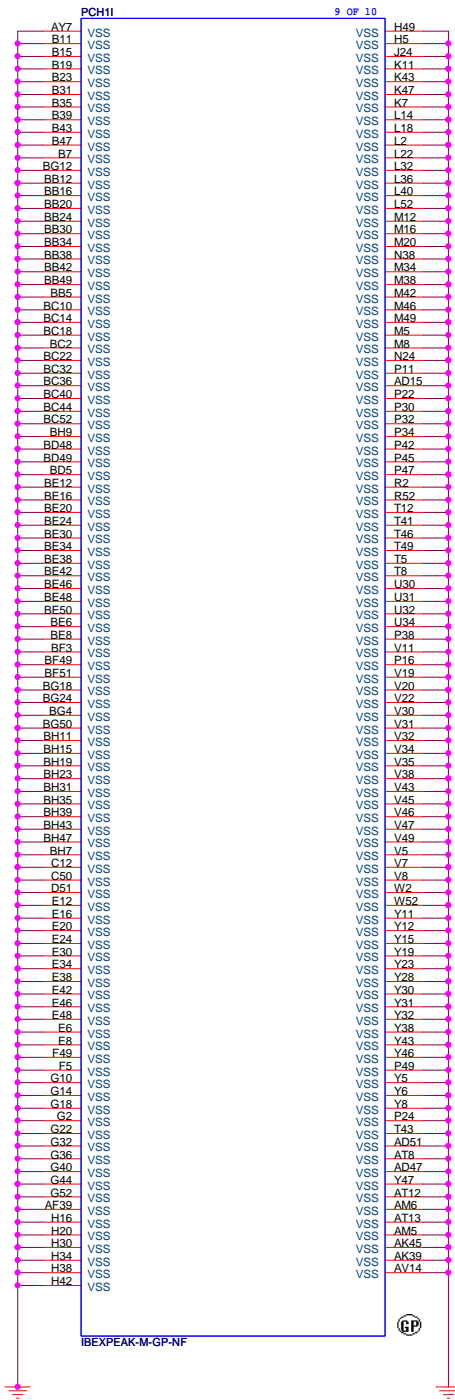
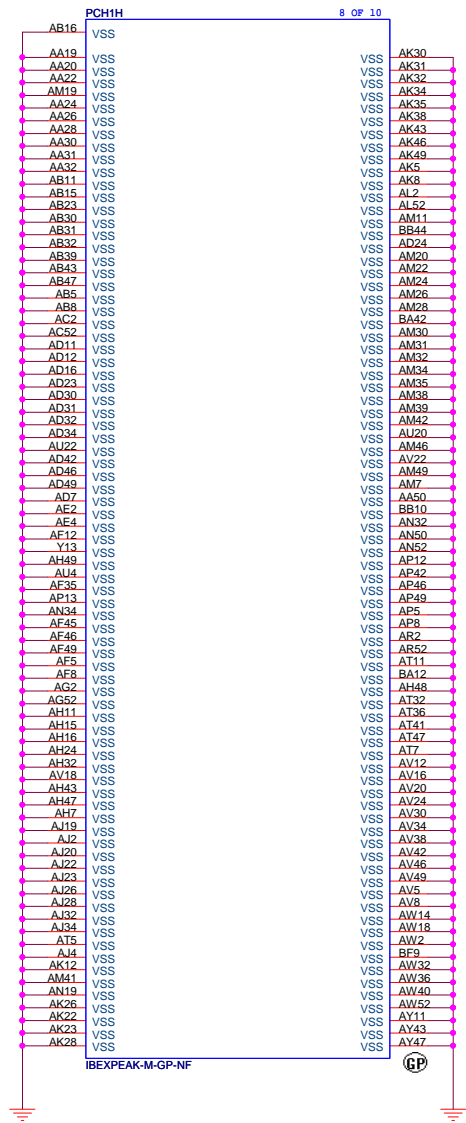
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.







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Title			
PCH (8/9)-PWR_2			
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Size	Document Number		Rev
A3	LA46-UMA		1
Date		Sheet	of
Monday, January 18, 2010		22	48

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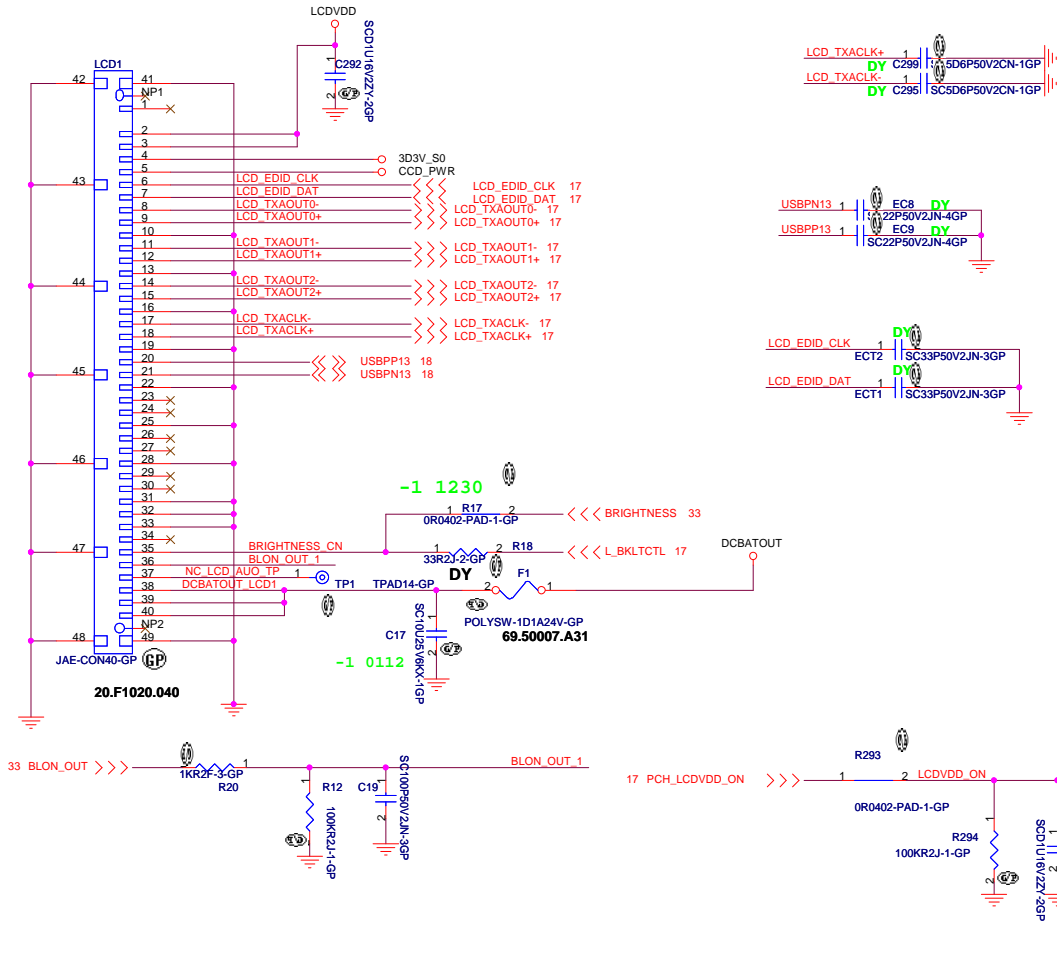
C

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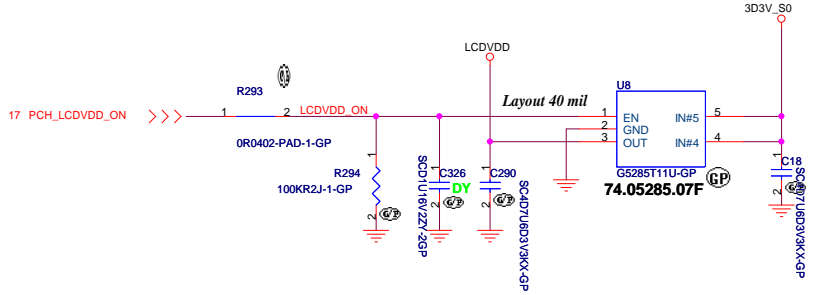
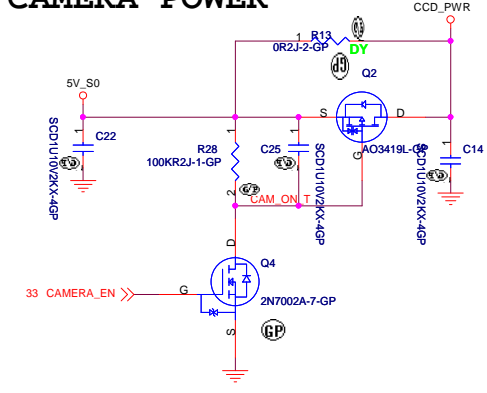
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緯創資通		Wistron Corporation	
<small>21F, 88 Sec. 1, 2nd Fl. Tai Wu Rd., Hsinchu,</small>		<small>Taipei Hsien 221, Taiwan, R.O.C</small>	
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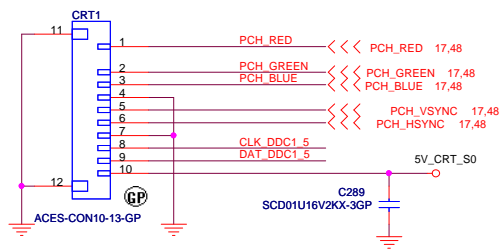
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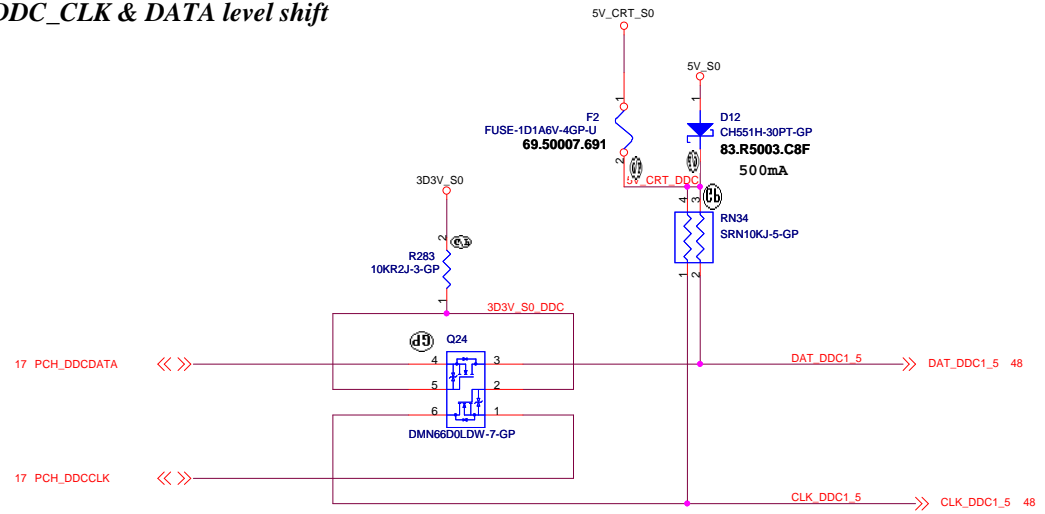
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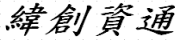


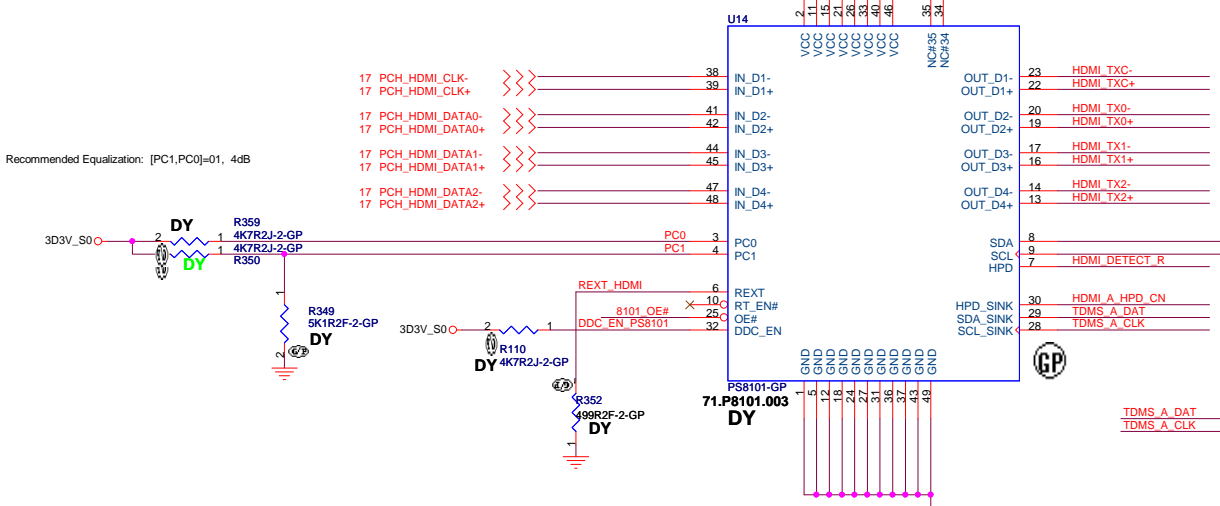
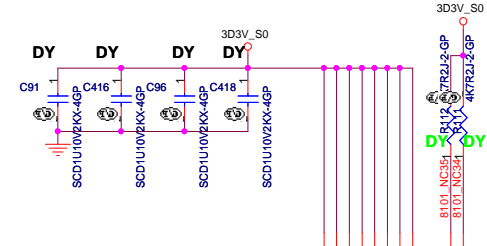
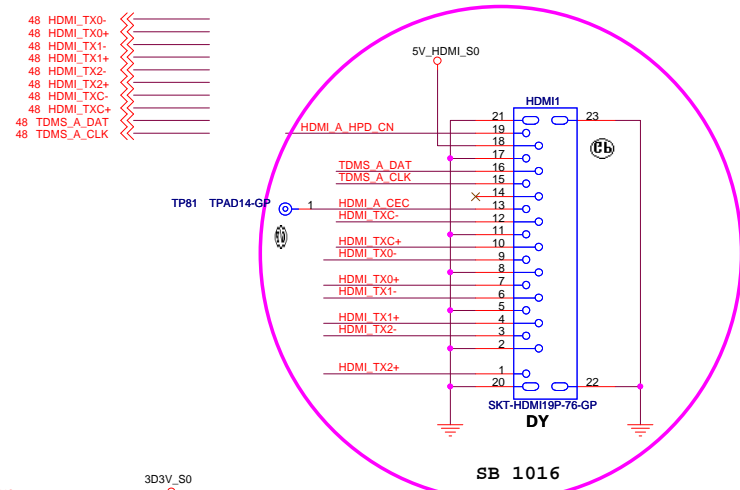
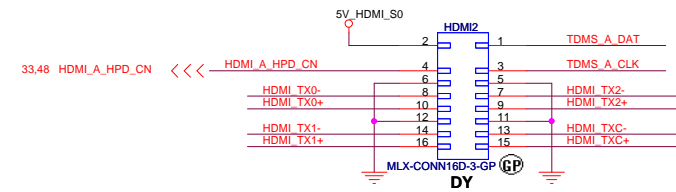
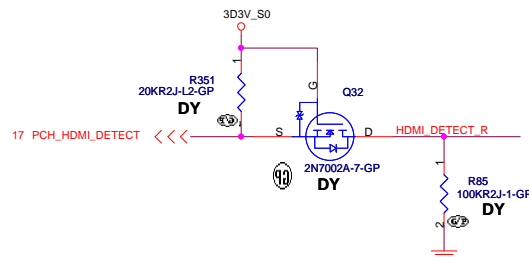
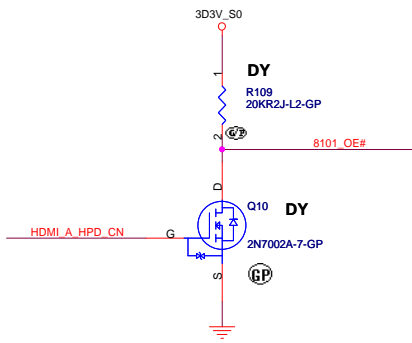
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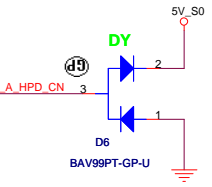
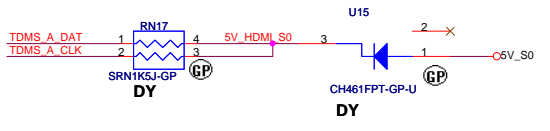
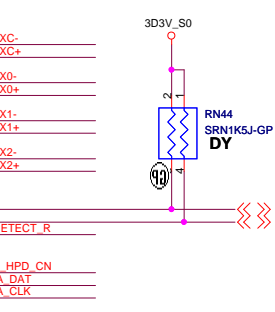
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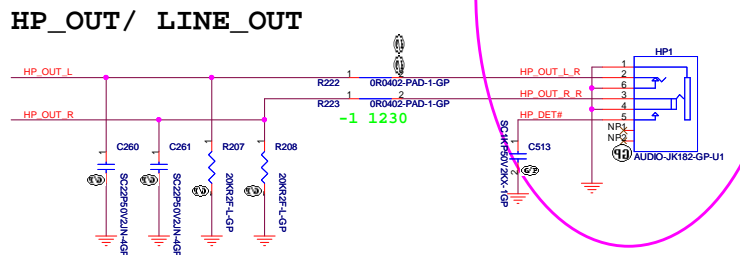
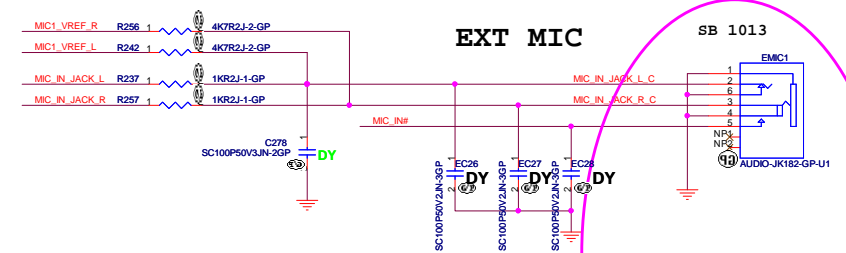
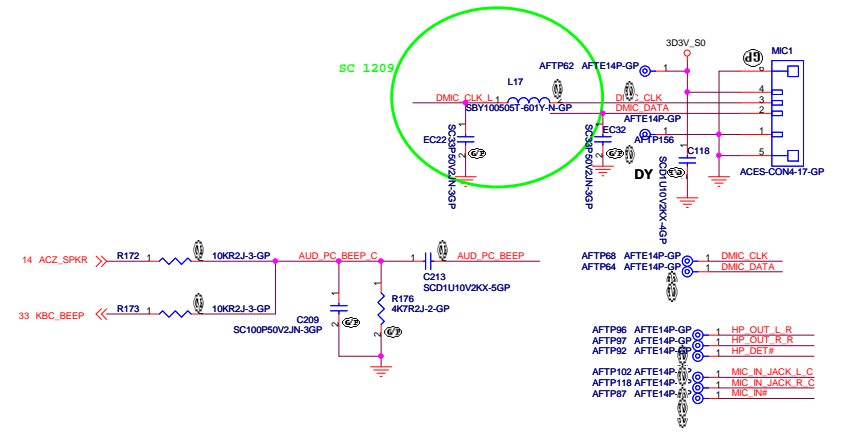
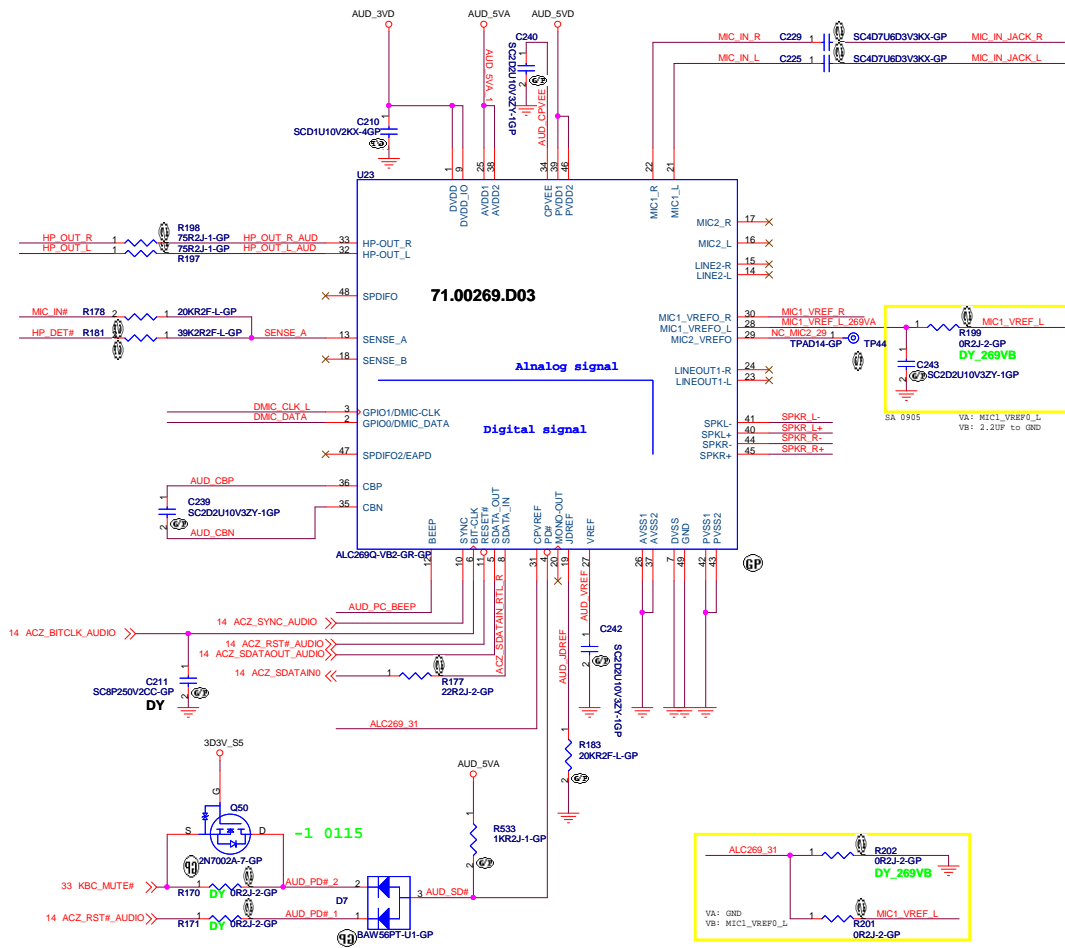
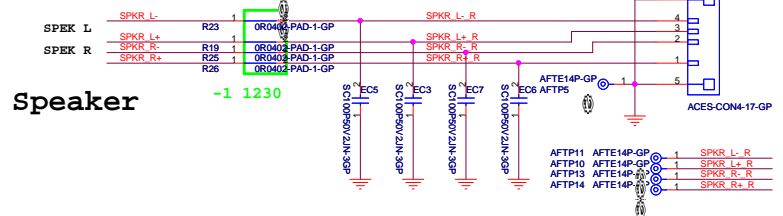
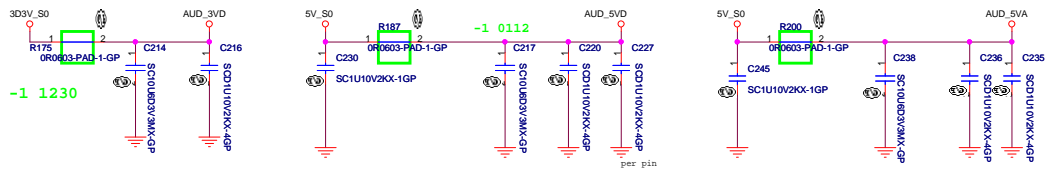
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Title	
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Recommended Equalization: [PC1,PC0]=01, 4dB



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		21F, 88, Sec. 1, Heish Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C	
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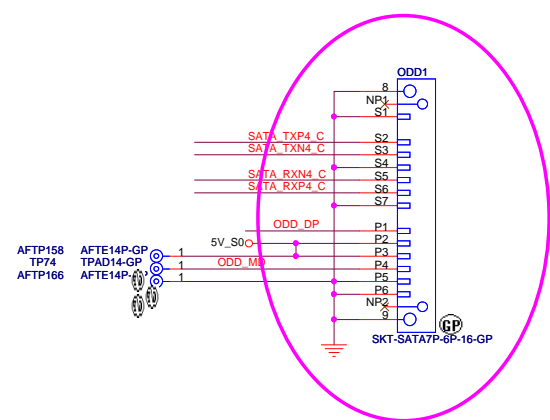
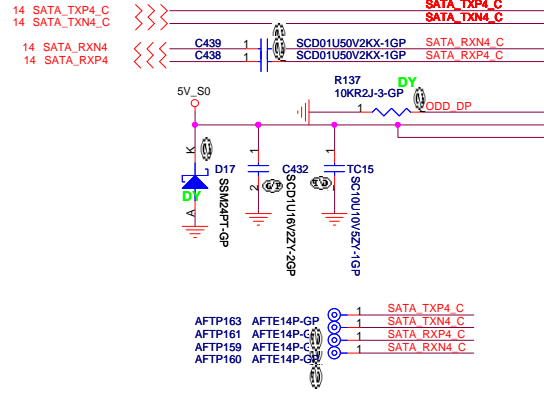
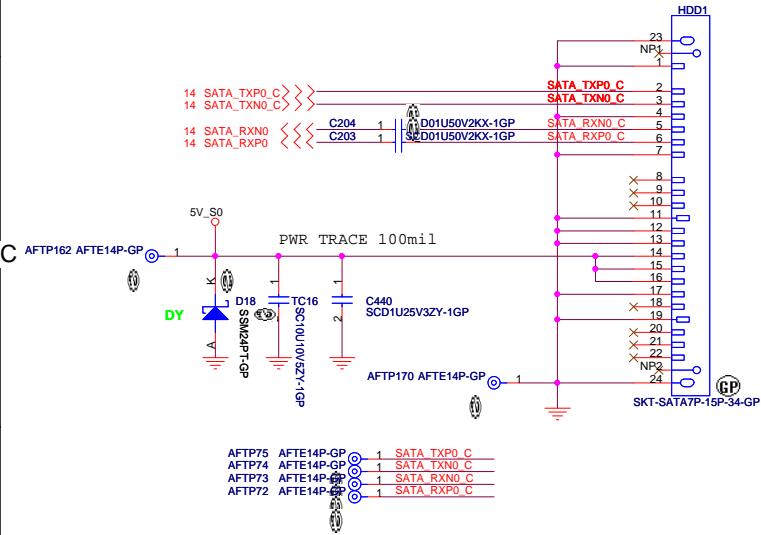
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd, Hsinchu, Taipei Hsin 321, Taiwan, R.O.C.

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SATA Connector

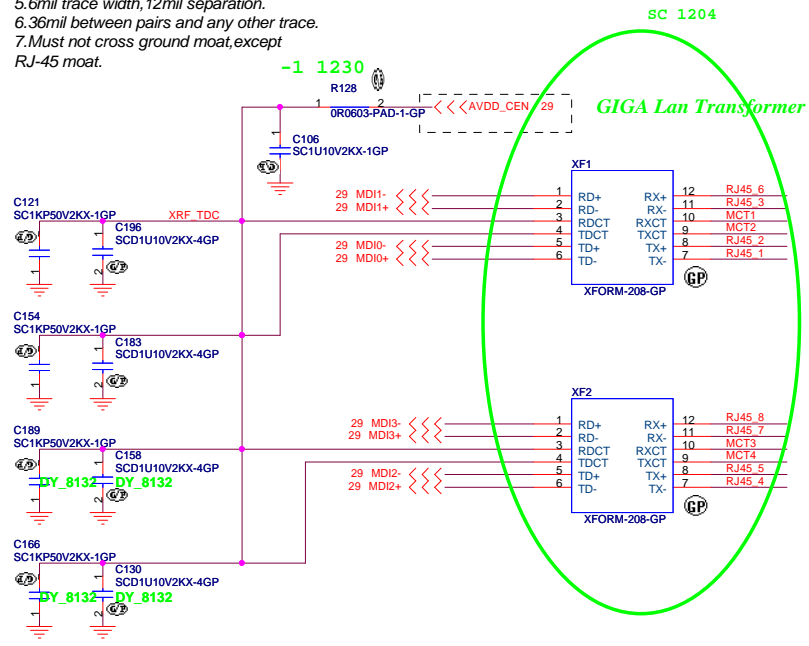
ODD Connector

SB 1016

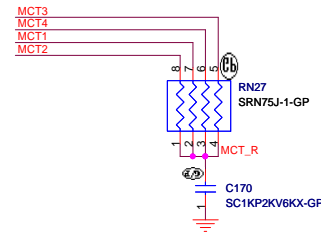
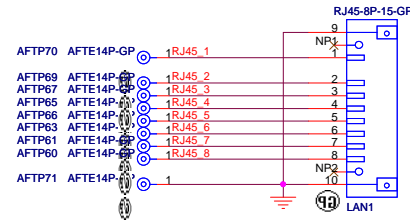


Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



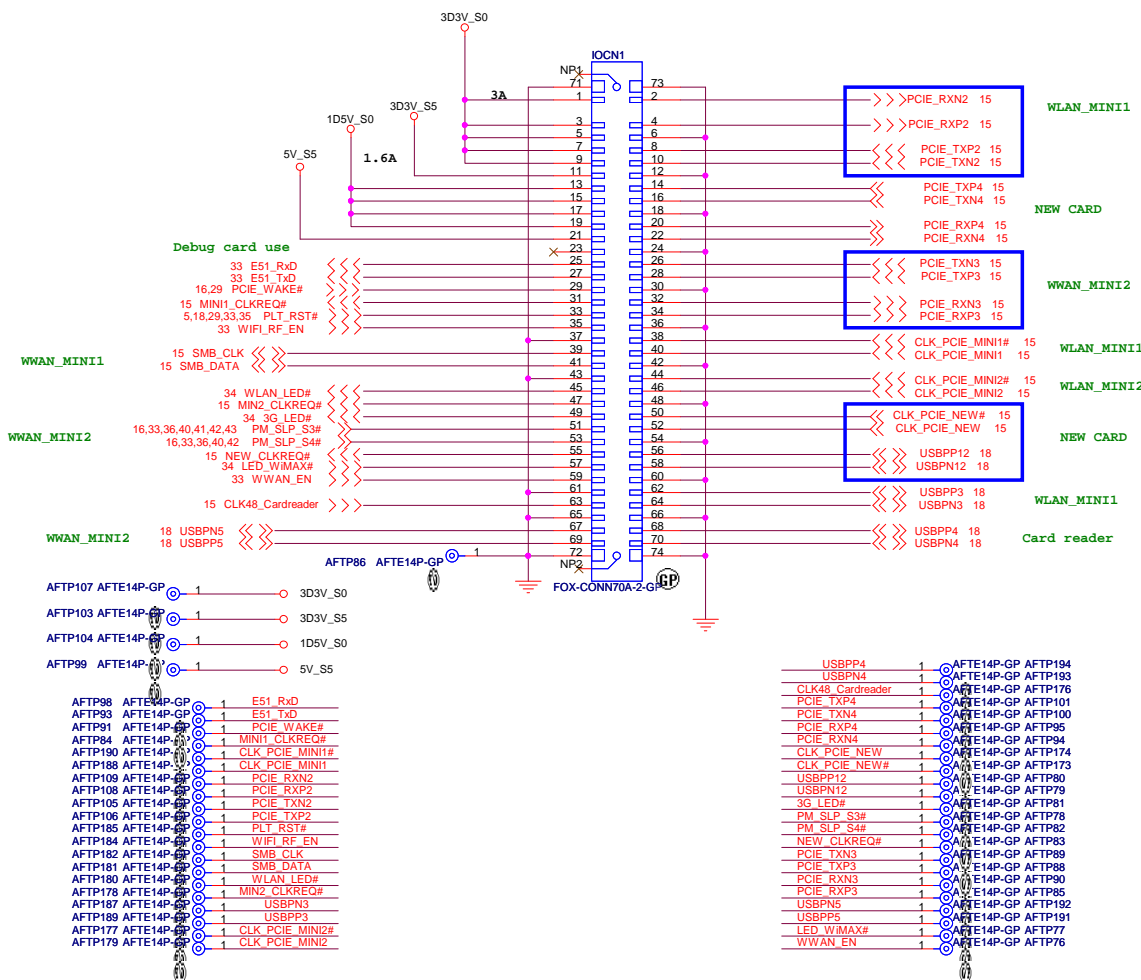
LAN Connector



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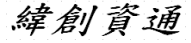
MOVE MINI CARD TO I/O BOARD



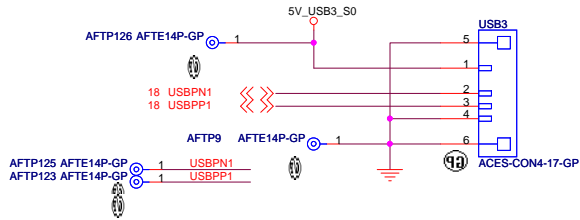
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- AFTP103 AFTE14P-GP 1 3D3V_S5
- AFTP104 AFTE14P-GP 1 1D5V_S0
- AFTP99 AFTE14P-GP 1 5V_S5
- AFTP98 AFTE14P-GP 1 E51_RxD
- AFTP93 AFTE14P-GP 1 E51_TxD
- AFTP91 AFTE14P-GP 1 PCIE_WAKE#
- AFTP84 AFTE14P-GP 1 MINI1_CLKREQ#
- AFTP190 AFTE14P-GP 1 CLK_PCIE_MINI1#
- AFTP188 AFTE14P-GP 1 CLK_PCIE_MINI1
- AFTP109 AFTE14P-GP 1 PCIE_RXN2
- AFTP108 AFTE14P-GP 1 PCIE_RXP2
- AFTP105 AFTE14P-GP 1 PCIE_TXN2
- AFTP106 AFTE14P-GP 1 PCIE_TXP2
- AFTP185 AFTE14P-GP 1 PLT_RST#
- AFTP184 AFTE14P-GP 1 WIFL_RF_EN
- AFTP182 AFTE14P-GP 1 SMB_CLK
- AFTP181 AFTE14P-GP 1 SMB_DATA
- AFTP180 AFTE14P-GP 1 WLAN_LED#
- AFTP178 AFTE14P-GP 1 MIN2_CLKREQ#
- AFTP187 AFTE14P-GP 1 USBPN3
- AFTP189 AFTE14P-GP 1 USBPP3
- AFTP177 AFTE14P-GP 1 CLK_PCIE_MINI2#
- AFTP179 AFTE14P-GP 1 CLK_PCIE_MINI2

- USBPP4 1 AFTE14P-GP AFTP194
- USBPN4 1 AFTE14P-GP AFTP193
- CLK48_Cardreader 1 AFTE14P-GP AFTP176
- PCIE_TXP4 1 AFTE14P-GP AFTP101
- PCIE_TXN4 1 AFTE14P-GP AFTP100
- PCIE_RXP4 1 AFTE14P-GP AFTP95
- PCIE_RXN4 1 AFTE14P-GP AFTP94
- CLK_PCIE_NEW 1 AFTE14P-GP AFTP174
- CLK_PCIE_NEW# 1 AFTE14P-GP AFTP173
- USBPN12 1 AFTE14P-GP AFTP90
- USBPN12 1 AFTE14P-GP AFTP79
- 3G_LED# 1 AFTE14P-GP AFTP81
- PM_SLP_S3# 1 AFTE14P-GP AFTP78
- PM_SLP_S4# 1 AFTE14P-GP AFTP82
- NEW_CLKREQ# 1 AFTE14P-GP AFTP83
- PCIE_RXN3 1 AFTE14P-GP AFTP89
- PCIE_TXN3 1 AFTE14P-GP AFTP88
- PCIE_RXN3 1 AFTE14P-GP AFTP90
- PCIE_RXP3 1 AFTE14P-GP AFTP85
- USBPN5 1 AFTE14P-GP AFTP192
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- LED_WIMAX# 1 AFTE14P-GP AFTP77
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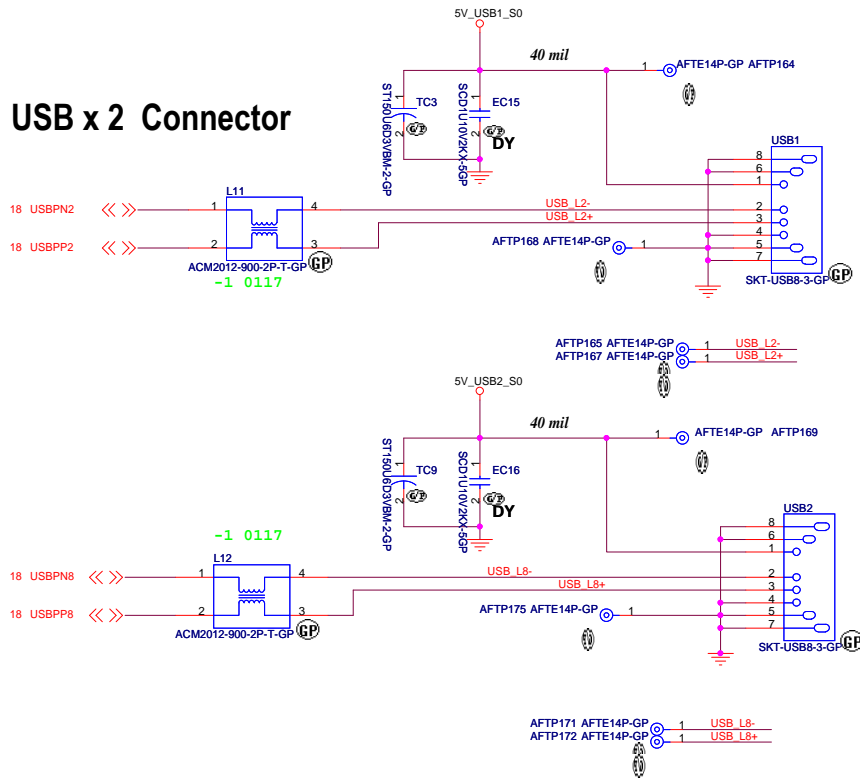
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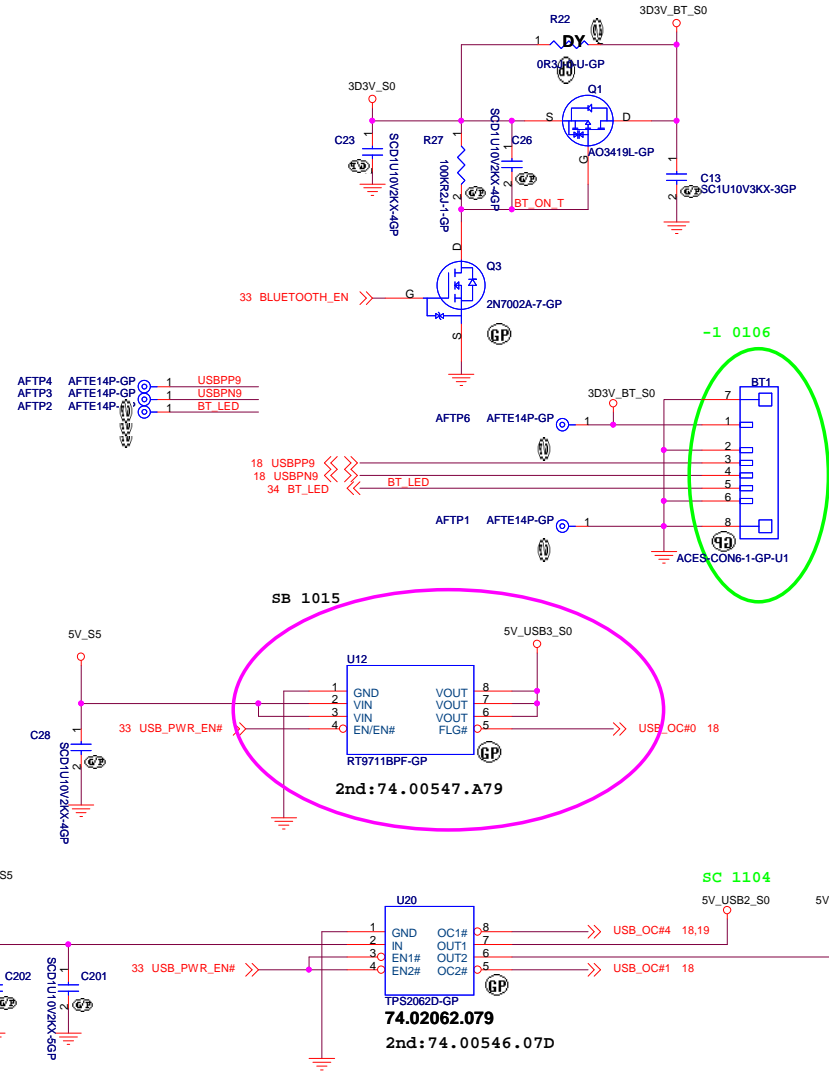
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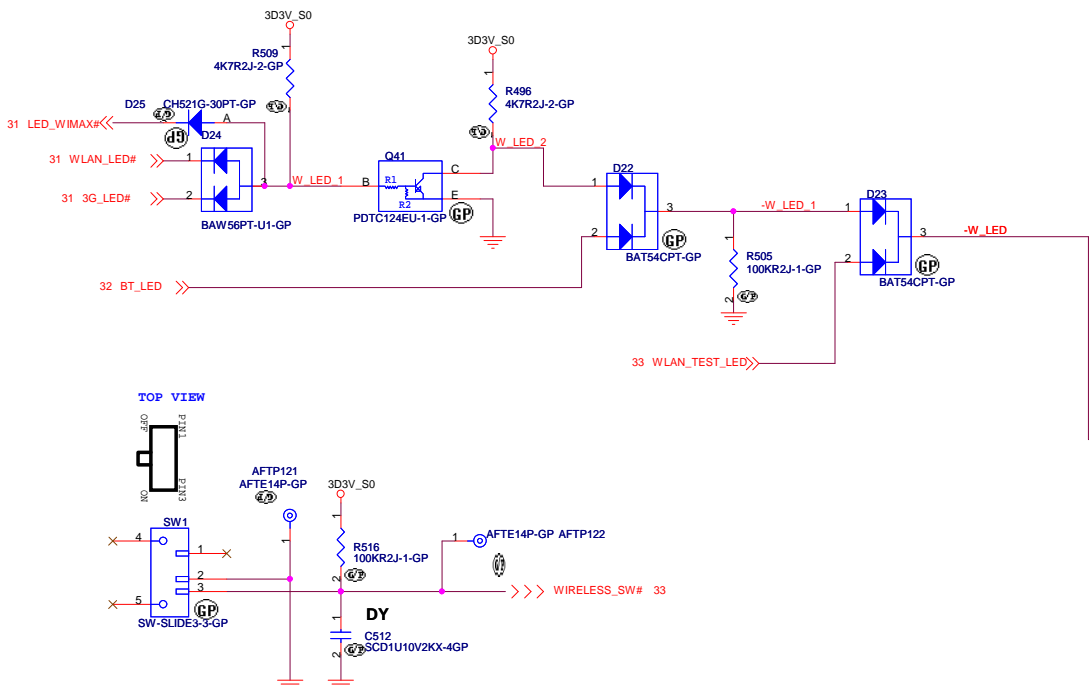
USB x 2 Connector



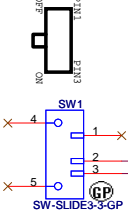
Bluetooth Power



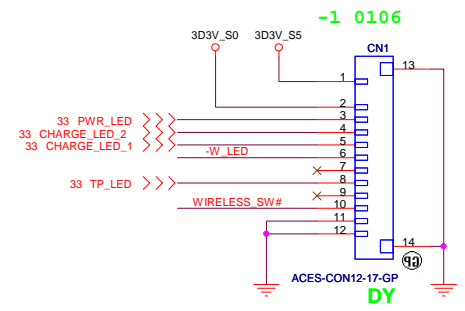
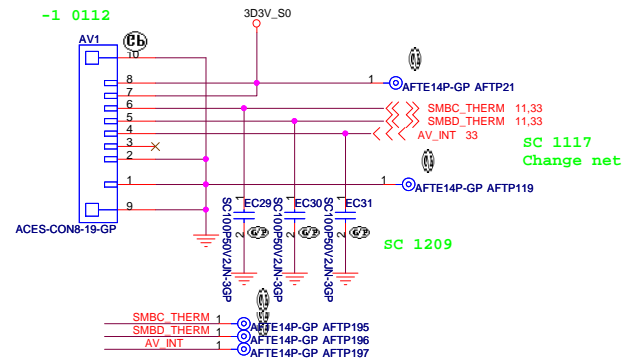
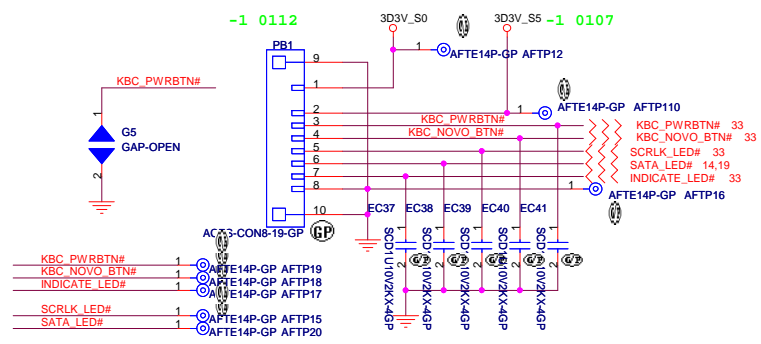
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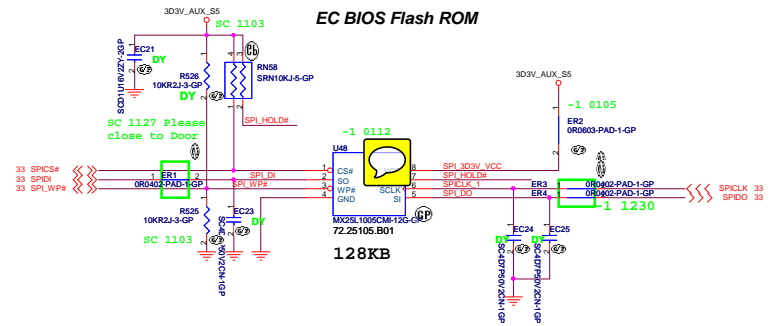
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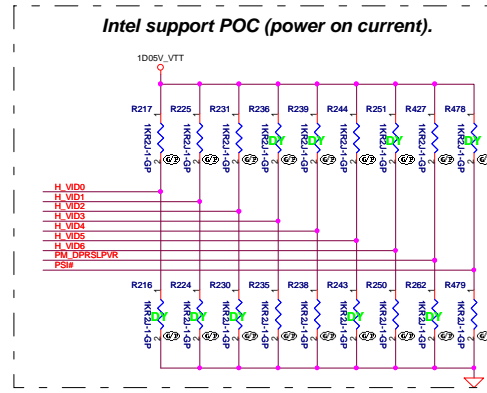
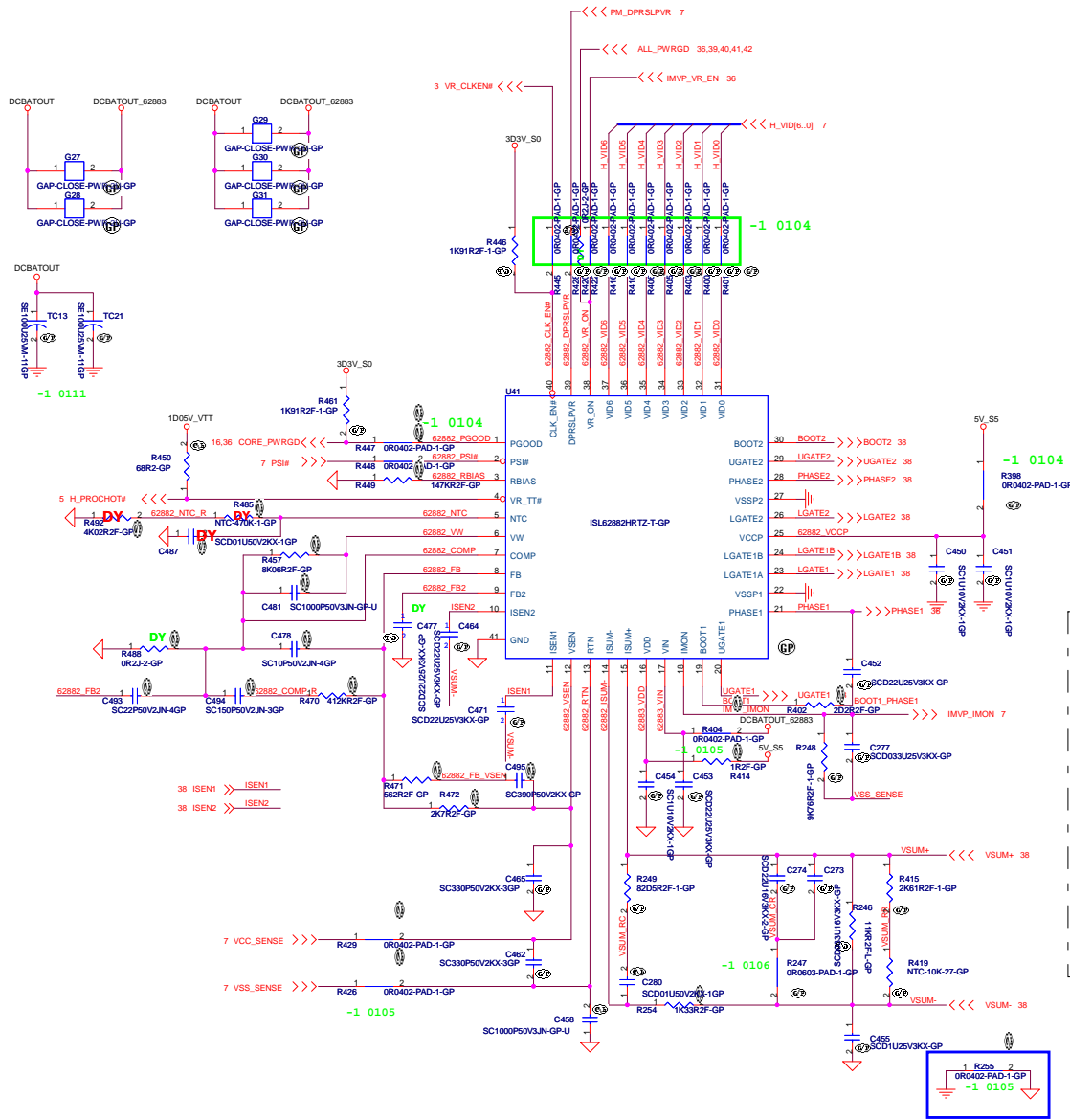


Power and LED Board



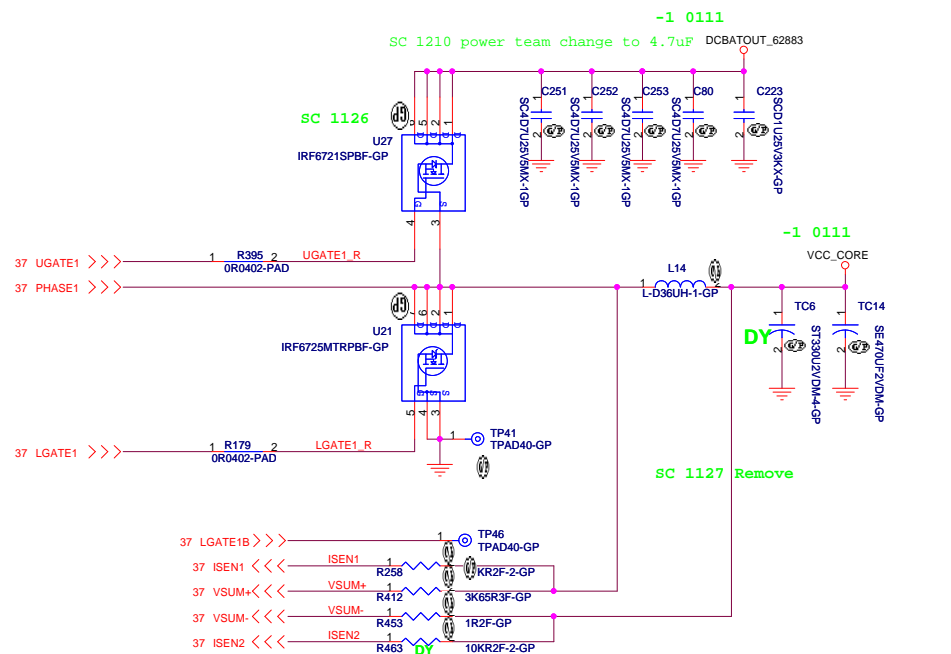
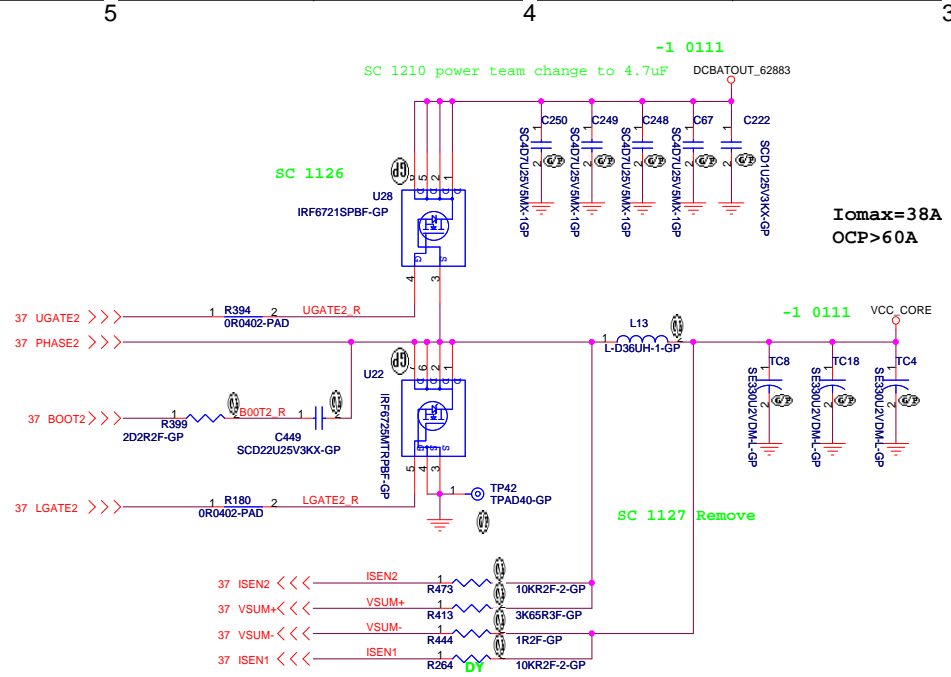
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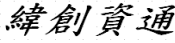


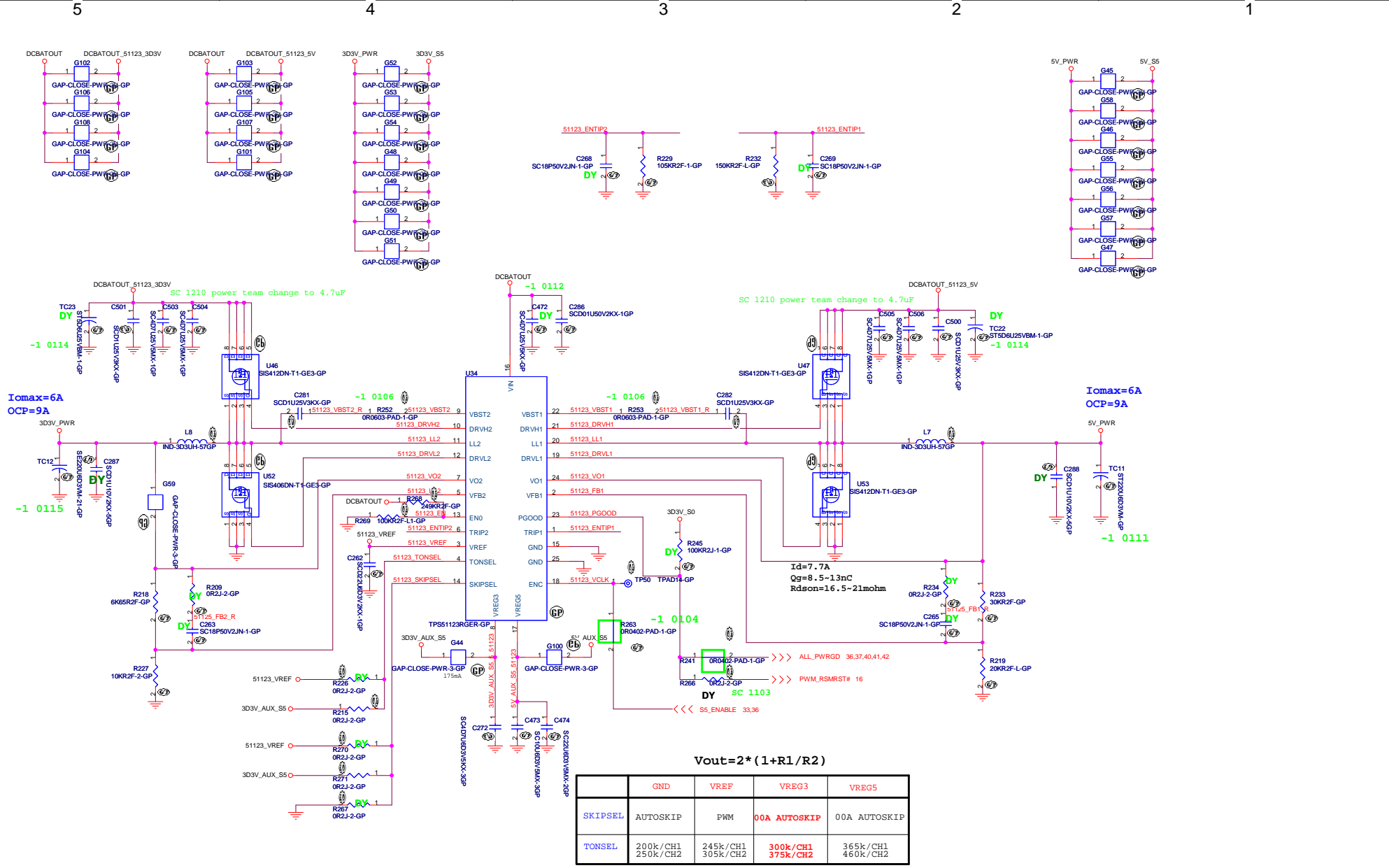
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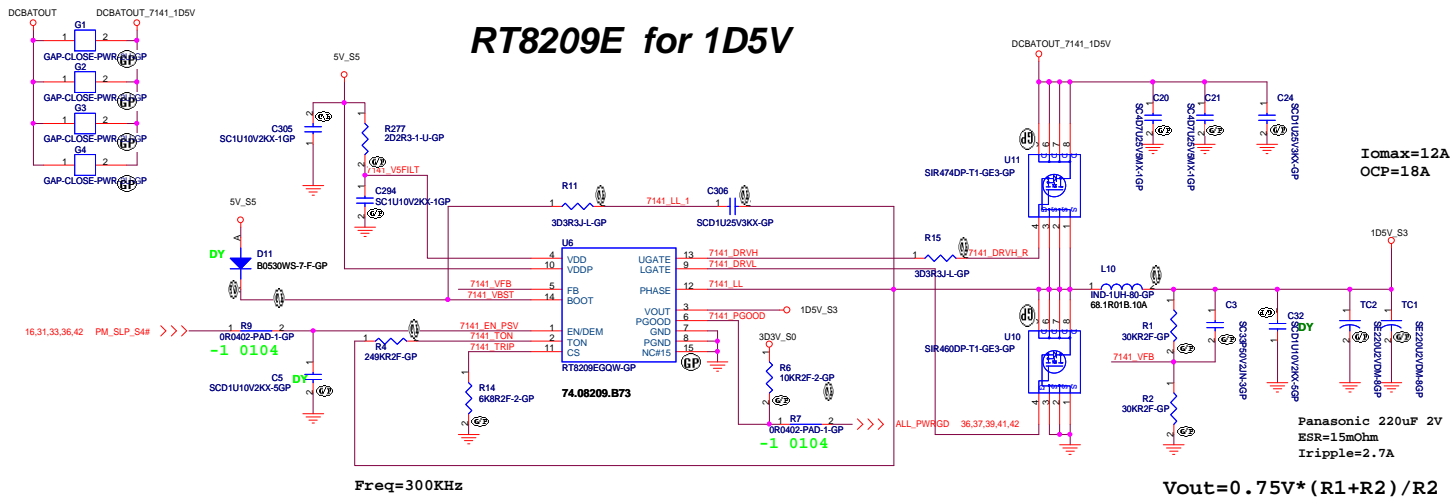


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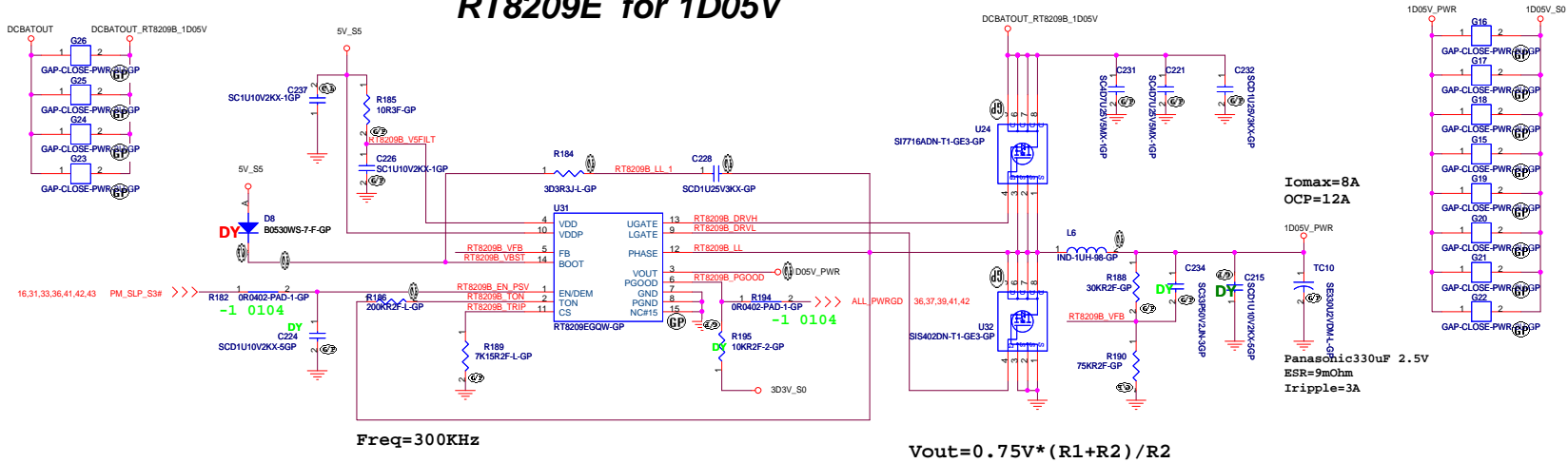
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RT8209E for 1D5V



RT8209E for 1D05V

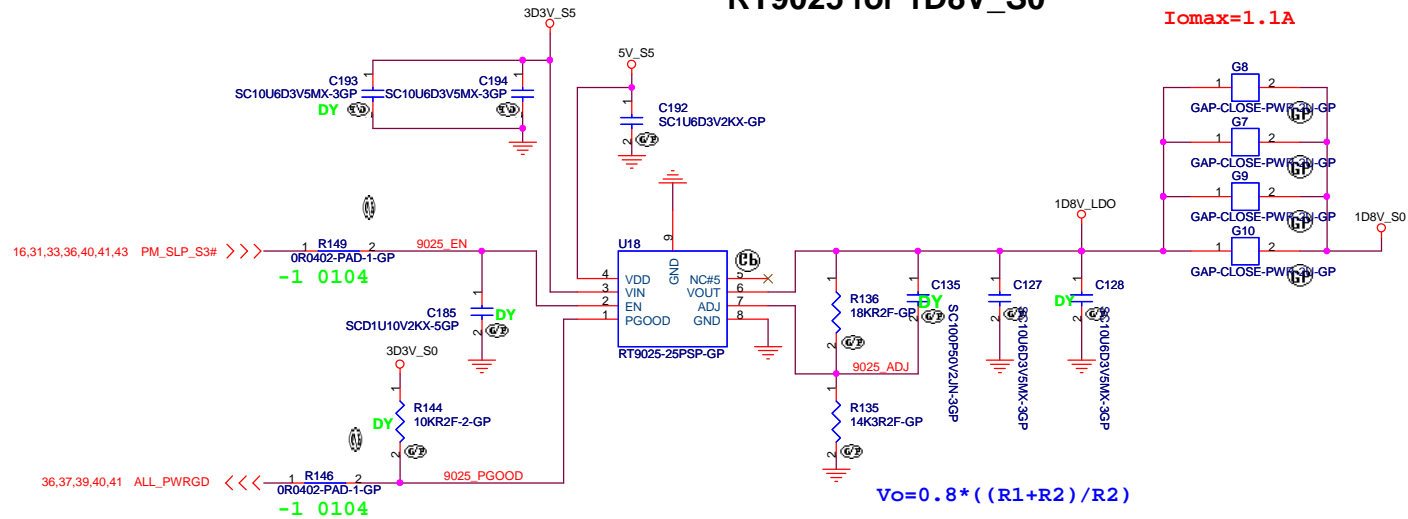


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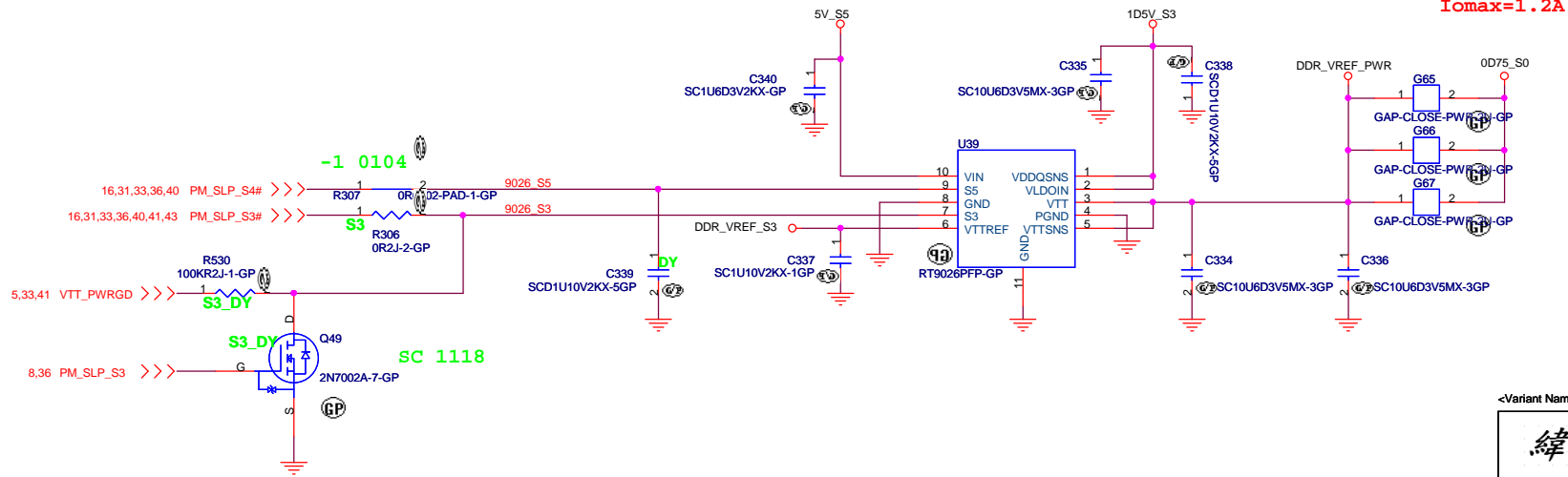
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RT9025 for 1D8V_S0

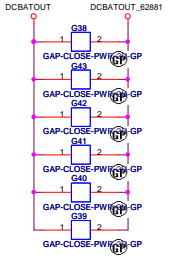
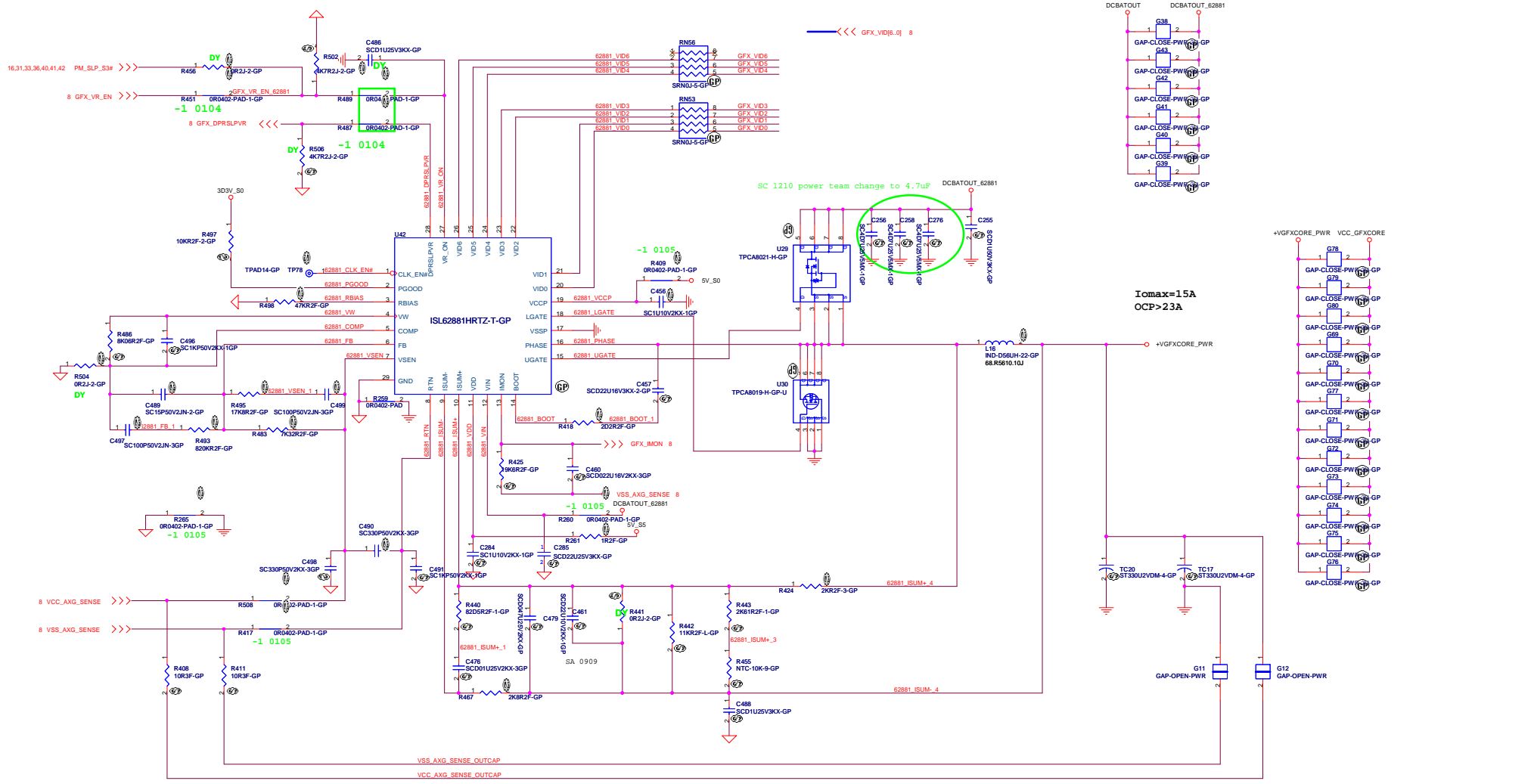


RT9026 for 0D75V_S3

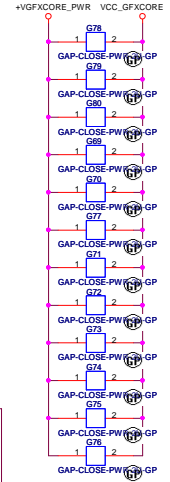


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緯創資通		Wistron Corporation	
<small>21F, 88 Sec. 1, 24th Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C</small>		<small>21F, 88 Sec. 1, 24th Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C</small>	
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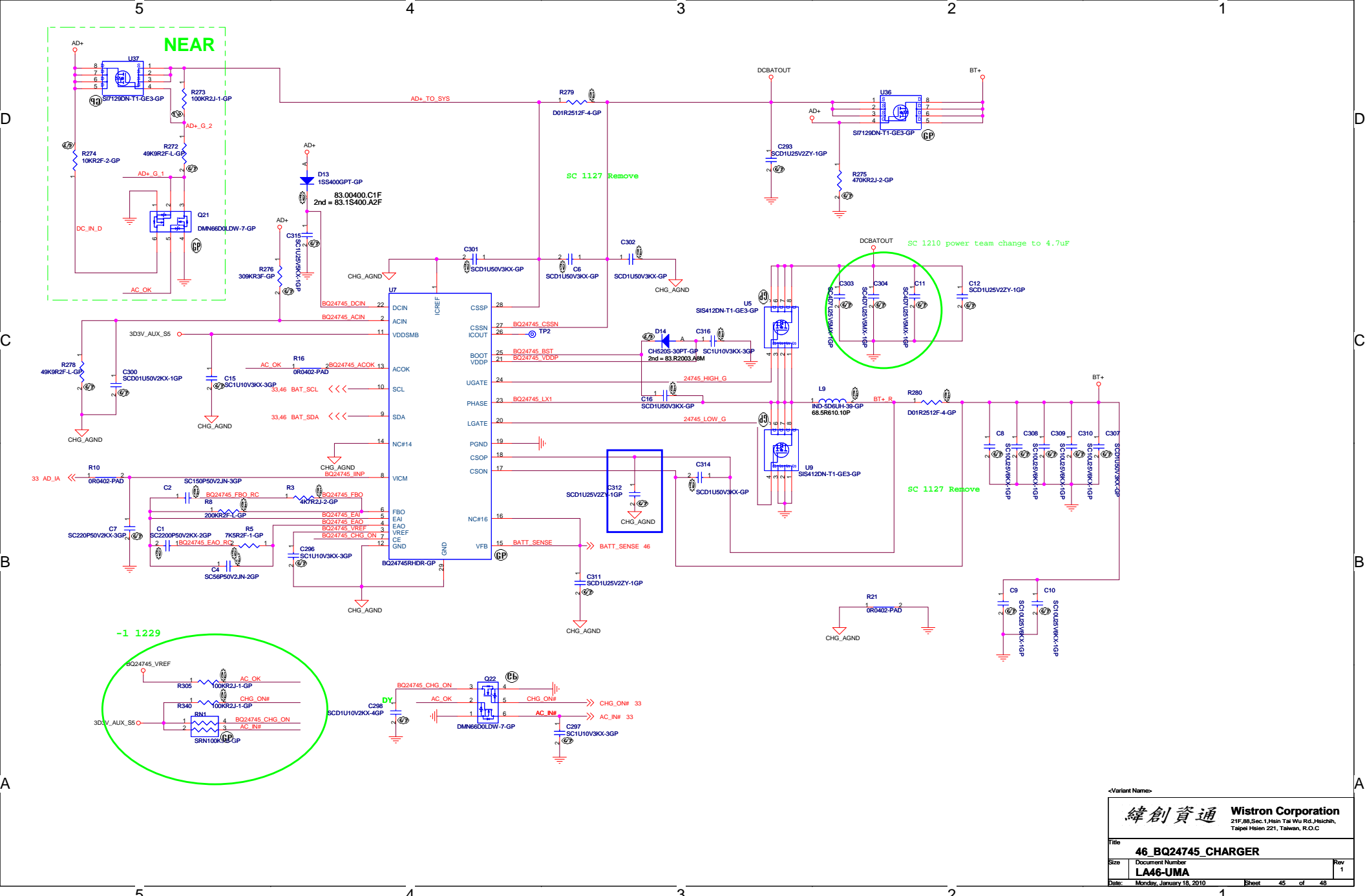
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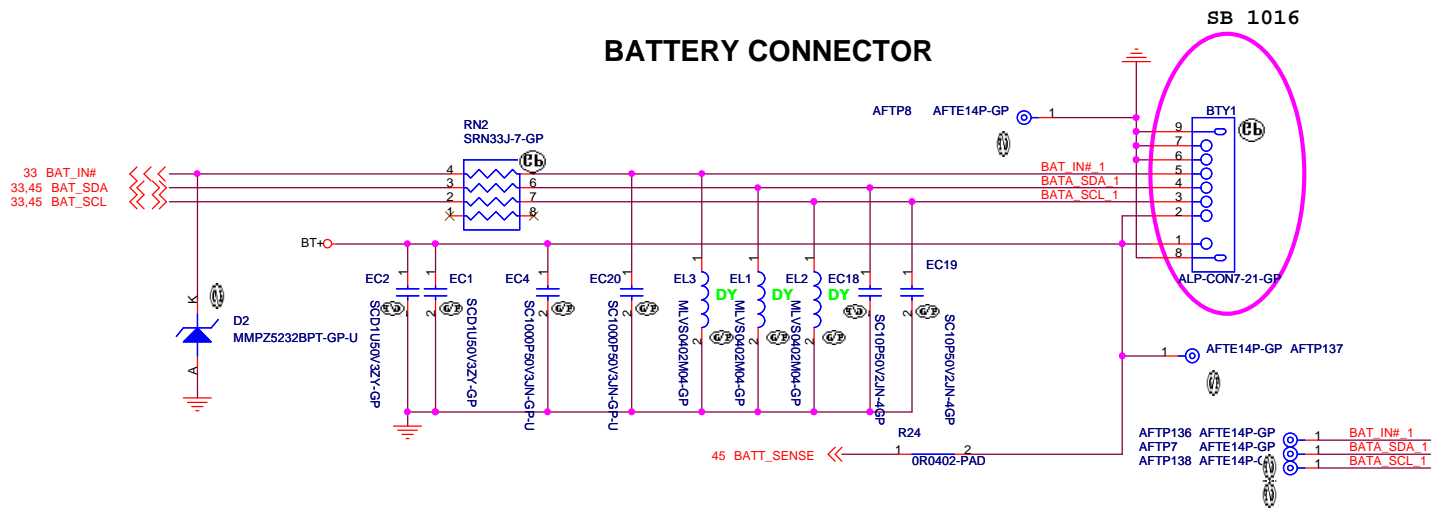
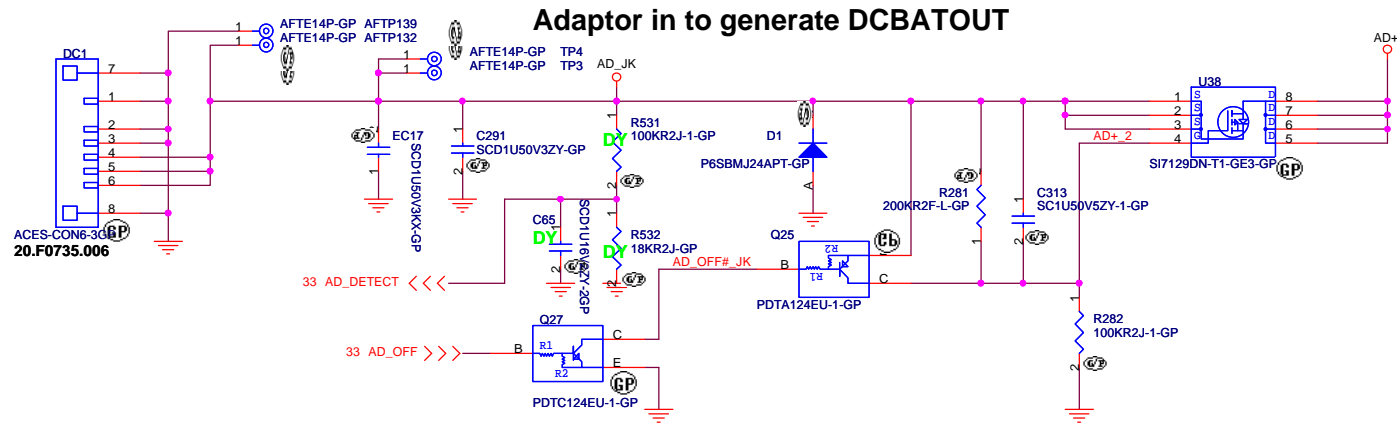
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