

# UMA & Optimus Schematics Document



## IVY Bridge(rPGA989)

### Intel PCH(Panther Point)

***DY :NotInstalled***

***UMA:UMA platform installed***

***OPS:Optimus***

***HR:Huron River***

***CR:Chief River***

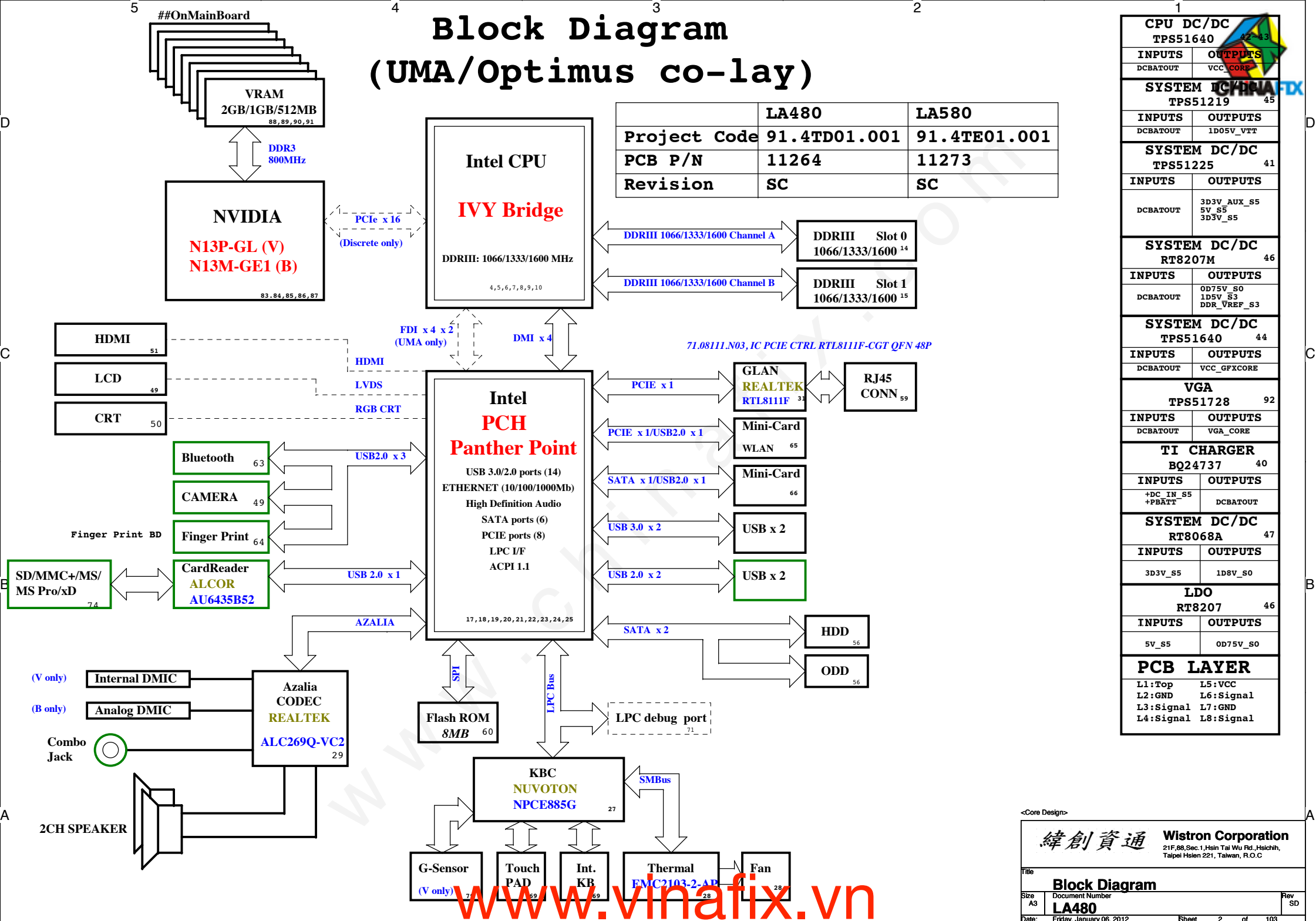
***V: V-Series installed***

<Core Design>

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Title			
<b>Cover Page</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		SD
Date:	Friday, January 06, 2012	Sheet	1 of 103

# Block Diagram (UMA/Optimus co-lay)

	LA480	LA580
Project Code	91.4TD01.001	91.4TE01.001
PCB P/N	11264	11273
Revision	SC	SC



<b>CPU DC/DC</b> TPS51640 42-43	
INPUTS DCBATOUT	OUTPUTS VCC_CORE
<b>SYSTEM DC/DC</b> TPS51219 45	
INPUTS DCBATOUT	OUTPUTS 1D05V_VTT
<b>SYSTEM DC/DC</b> TPS51225 41	
INPUTS DCBATOUT	OUTPUTS 3D3V_AUX_S5 5V_S5 3D3V_S5
<b>SYSTEM DC/DC</b> RT8207M 46	
INPUTS DCBATOUT	OUTPUTS 0D75V_S0 1D5V_S3 DDR_VREF_S3
<b>SYSTEM DC/DC</b> TPS51640 44	
INPUTS DCBATOUT	OUTPUTS VCC_GFXCORE
<b>VGA</b> TPS51728 92	
INPUTS DCBATOUT	OUTPUTS VGA_CORE
<b>TI CHARGER</b> BQ24737 40	
INPUTS +DC_IN_S5 +PBATT	OUTPUTS DCBATOUT
<b>SYSTEM DC/DC</b> RT8068A 47	
INPUTS 3D3V_S5	OUTPUTS 1D8V_S0
<b>LDO</b> RT8207 46	
INPUTS 5V_S5	OUTPUTS 0D75V_S0
<b>PCB LAYER</b>	
L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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File: **Block Diagram**

Size: A3 Document Number: **LA480** Rev: SD

Date: Friday, January 06, 2012 Sheet: 2 of 103



# PCH Strapping Chief River Schematic Checklist Rev0.72

# Processor Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> Default Mode: Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] <b>Disable Danbury:</b> Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	<b>PCI-Express Static Lane Reversal</b>	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port 0: connect to the EMBEDDED display Port	0
CFG[6:5]	<b>PCI-Express Port Bifurcation Straps</b>	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	<b>PEG DEFER TRAINING</b>	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails		DESCRIPTION
		ACTIVE IN		
5V_S0 3D3V_S0 1D8V_S0 1D3V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0		CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S7 DDR_VREF_S3	5V 1.5V 0.75V	S3		
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states		AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3		ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN		ON for iAMTLegacy WOL
3D3V_AUX_RBC	3.3V	DSW, Sx		ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx		Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

## PCIe Routing

LANE	Routing
LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

## USB Table port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

## SMBus ADDRESSES

I 2 C / SMBus Addresses	Ref Des	Chief River CRV		
Device		Address	Hex	Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA		
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA		
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor NI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK		

## SATA Table

Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

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Title: **Table of Content**

Size A3 Document Number **LA480** Rev **SD**

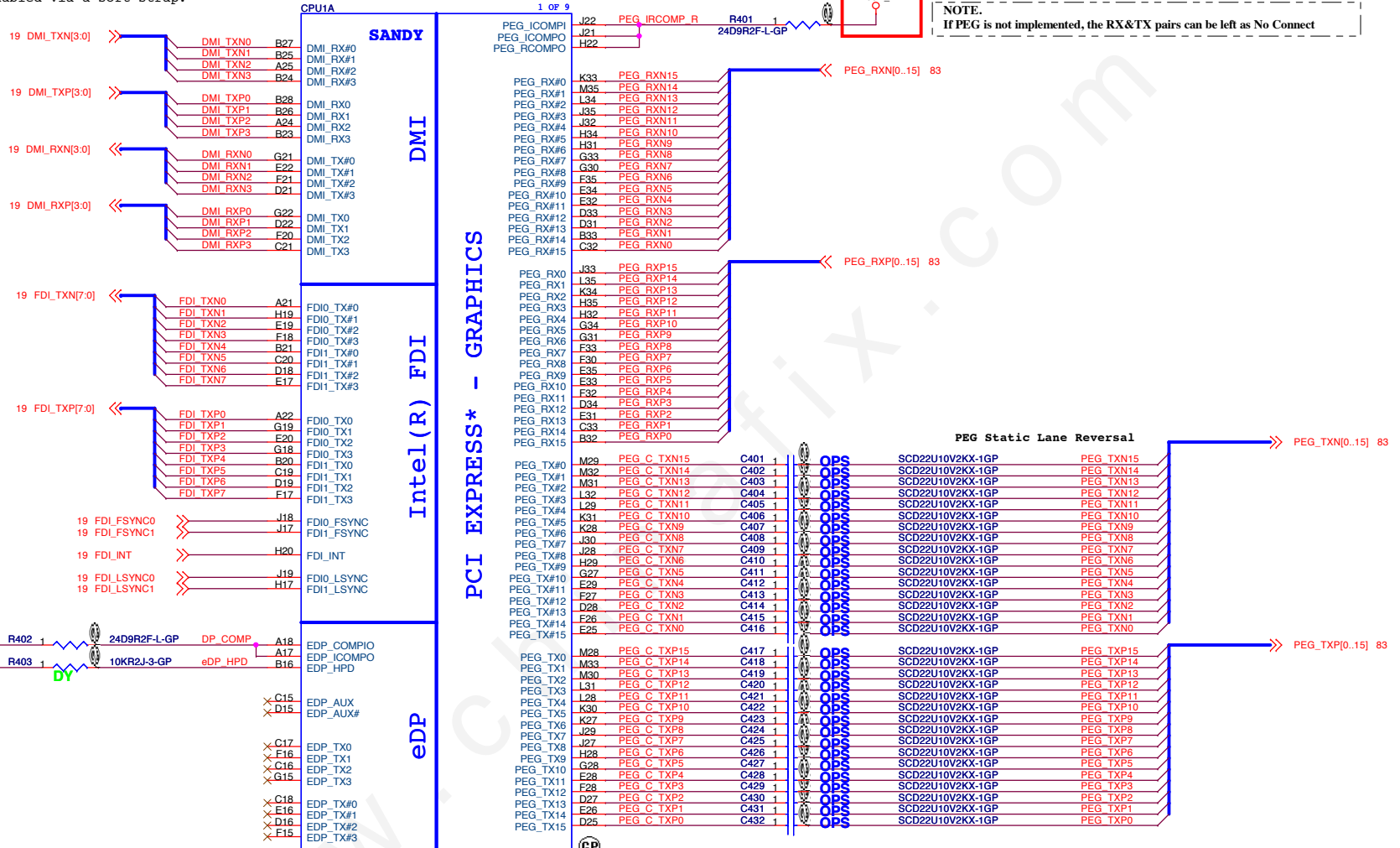
Date: Friday, January 06, 2012 Sheet 3 of 103

**SSID = CPU**

01.001VY.000 IVY BRIDGE ORCAD SYMBOL.

Note:  
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:  
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

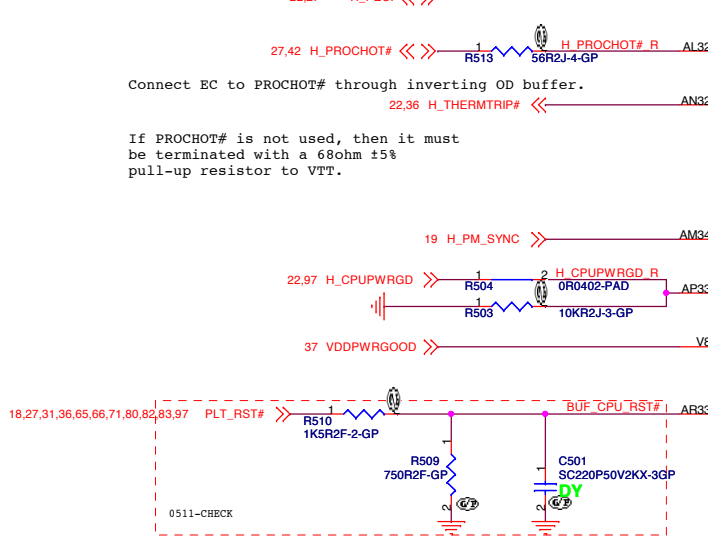
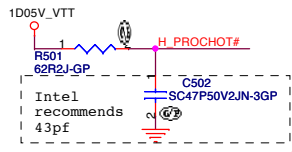
Note:  
Lane reversal does not apply to FDI sideband signals.

**NOTE:**  
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

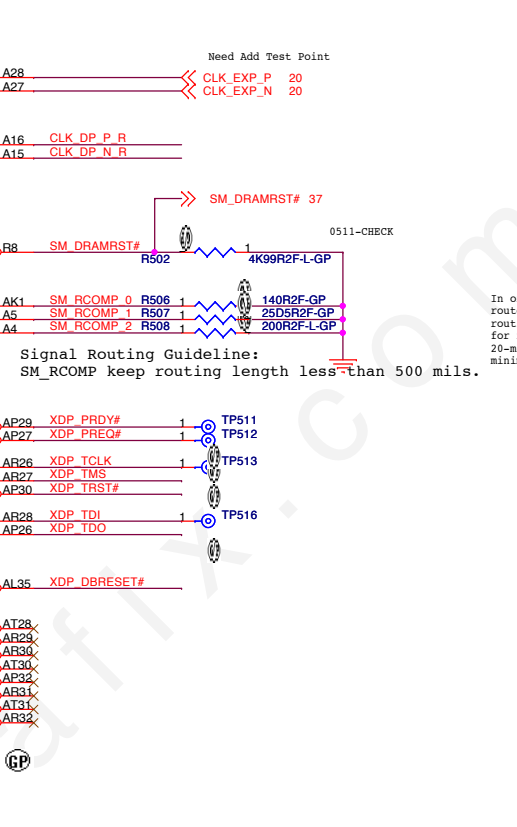
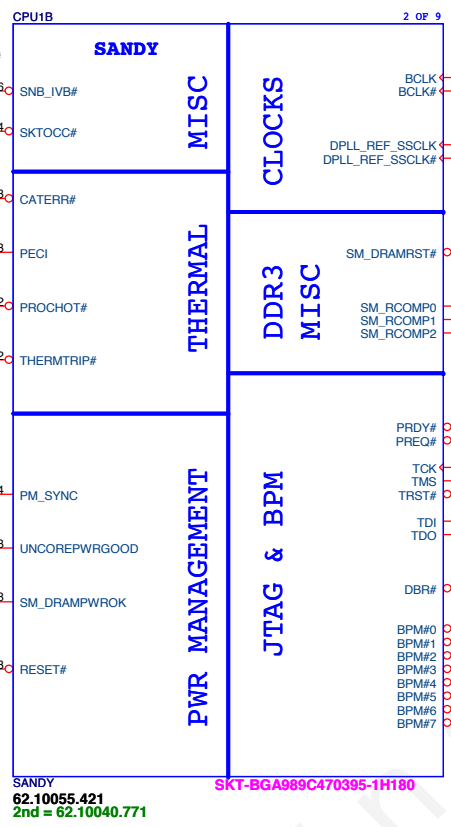
**NOTE:**  
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

**SSID = CPU**

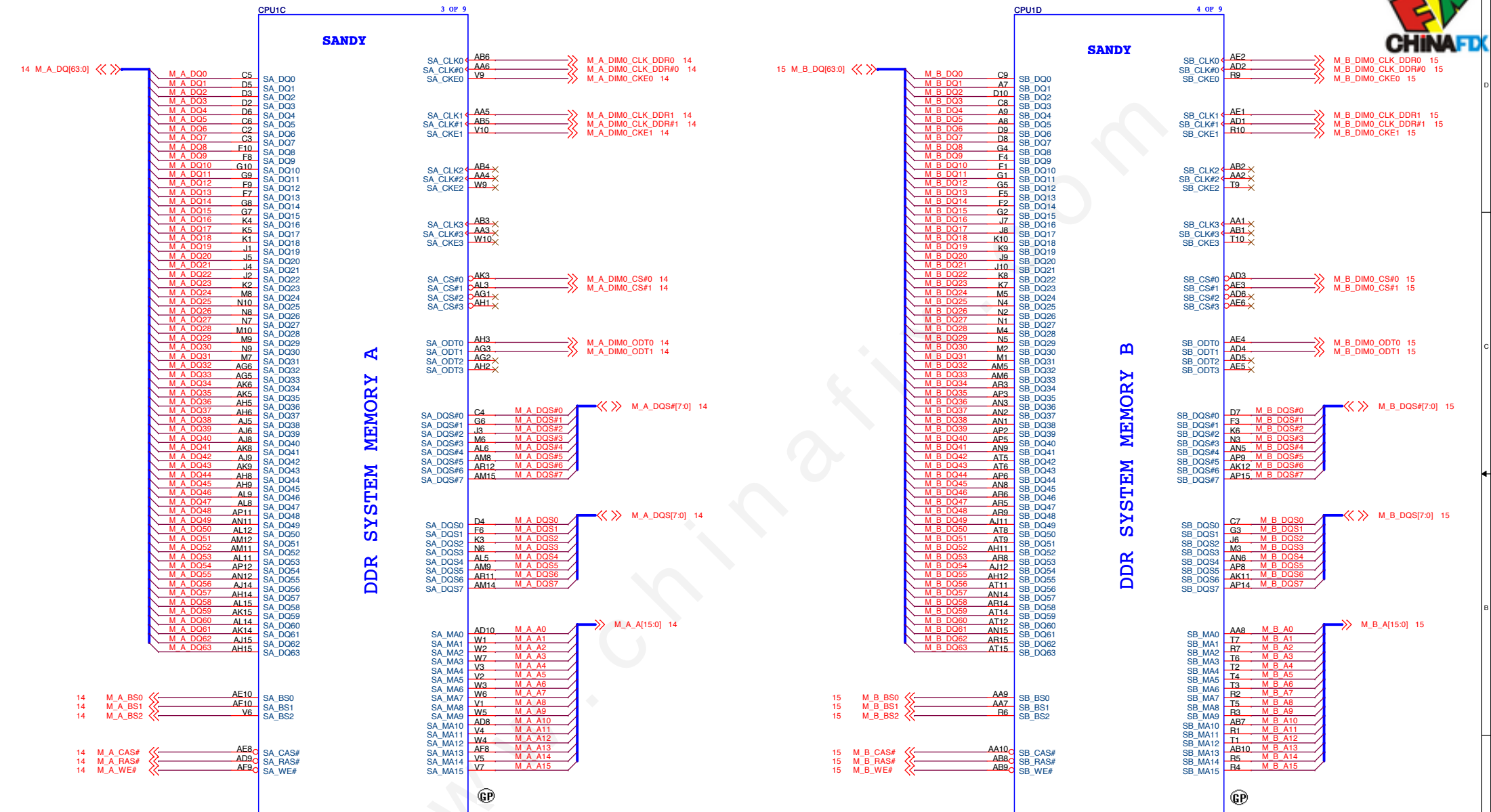


- DEL U501**
- DEL R519**
- DEL C503**
- DEL R517**
- DEL R515**
- ASM R510**
- ASM R509**



**Disabling Guidelines:**  
 If motherboard only supports external graphics:  
 Connect DPLL\_REF\_SSCLK on Processor to GND through 1K +/- 5% resistor.  
 Connect DPLL\_REF\_SSCLK# on Processor to VCCB through 1K +/- 5% resistor (power (~15 mW) may be wasted).

In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.



SANDY  
62.10055.421  
2nd = 62.10040.771

SANDY  
62.10055.421  
2nd = 62.10040.771

<Core Design>

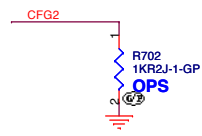
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Title: **CPU (DDR)**

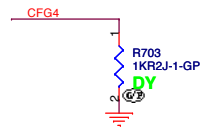
Size: A3 Document Number: **LA480** Rev: SD

Date: Friday, January 06, 2012 Sheet: 6 of 103

# SSID = CPU

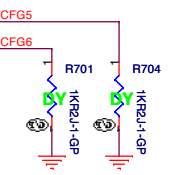


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

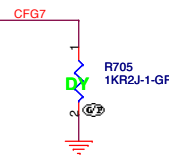


Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

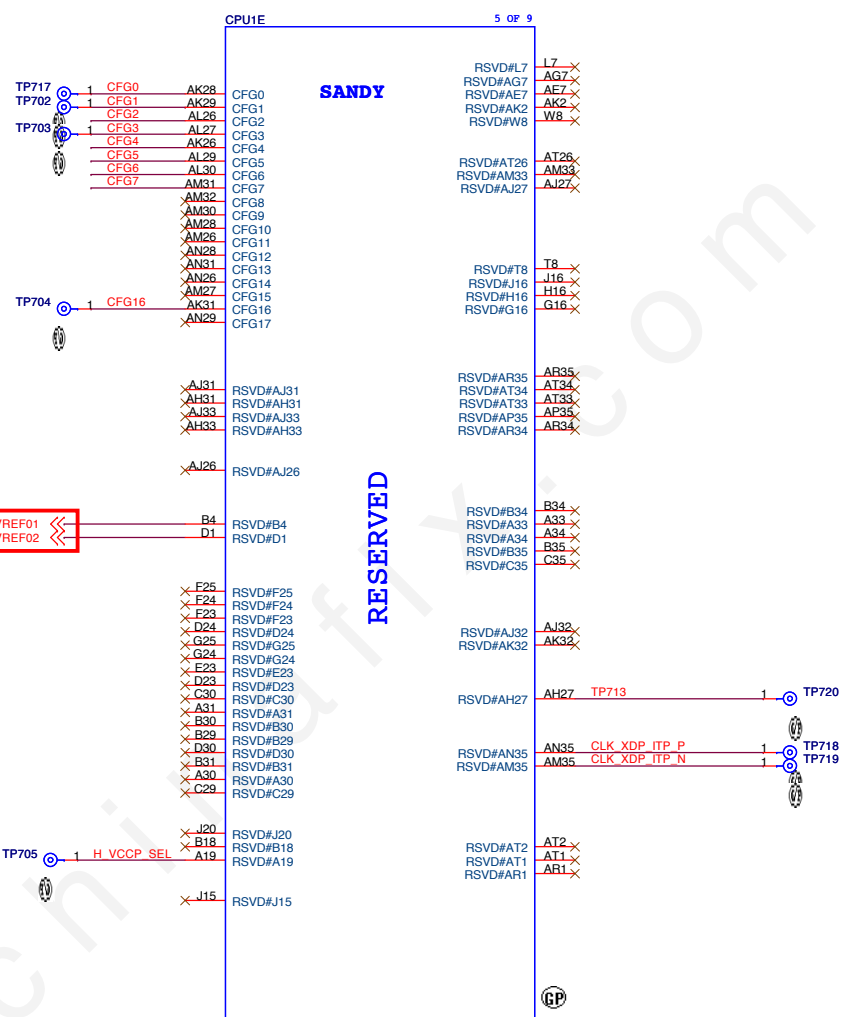
12 DDR\_WR\_VREF01  
12 DDR\_WR\_VREF02



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



SANDY SKT-BGA989C470395-1H180  
62.10055.421  
2nd = 62.10040.771

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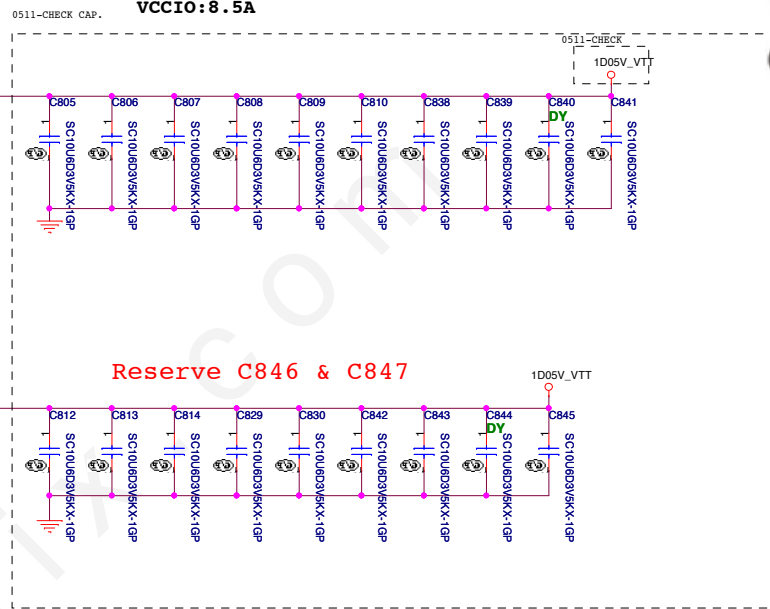
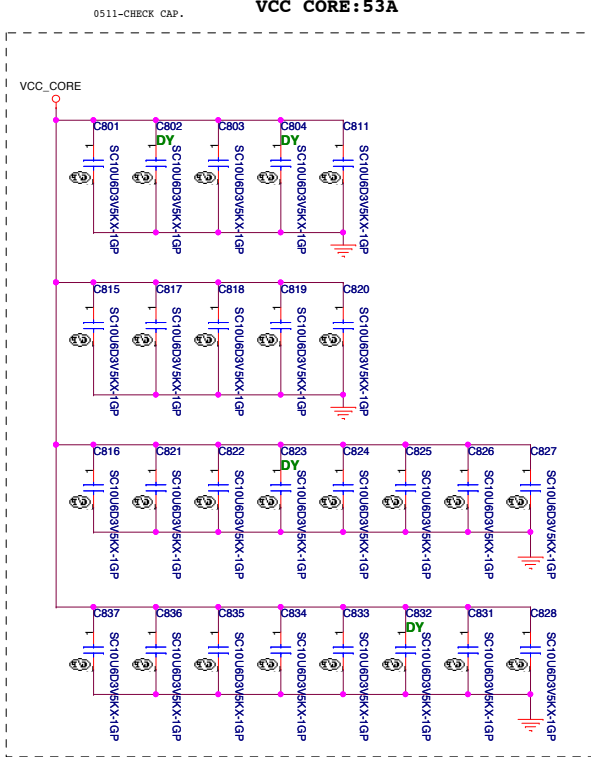
Size A3 Document Number **LA480** Rev SD

Date: Friday, January 06, 2012 Sheet 7 of 103

# POWER

VCC CORE:53A

VCCIO:8.5A



VCC\_CORE

SANDY

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- Y25 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
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- P27 VCC
- P26 VCC

PEG AND DDR

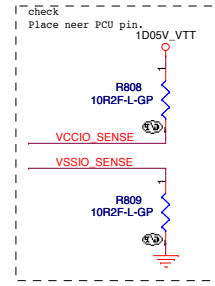
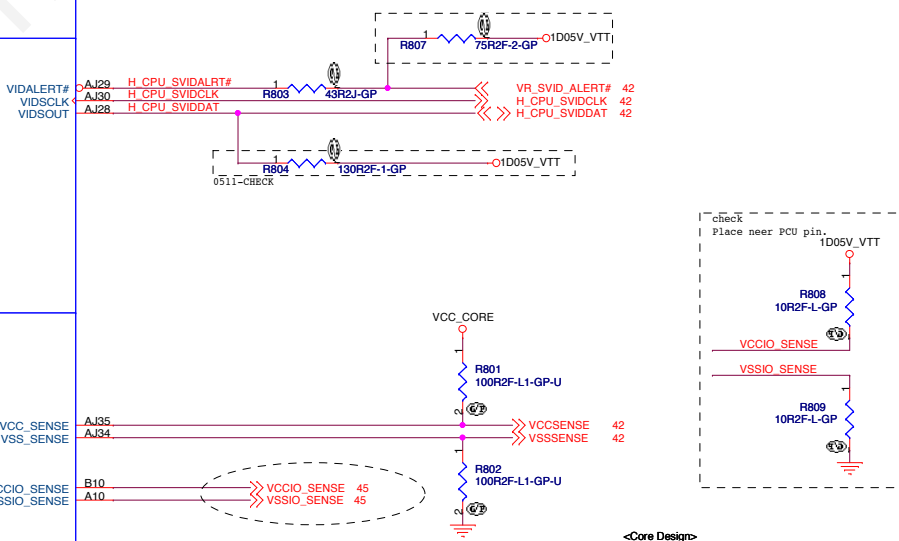
CORE SUPPLY

SVID

SENSE LINES

- VCCIO AH13
- VCCIO AH10
- VCCIO AG10
- VCCIO Y10
- VCCIO U10
- VCCIO P10
- VCCIO L10
- VCCIO J13
- VCCIO J12
- VCCIO H14
- VCCIO H12
- VCCIO H11
- VCCIO G14
- VCCIO G13
- VCCIO F14
- VCCIO F13
- VCCIO F12
- VCCIO E11
- VCCIO E14
- VCCIO E12
- VCCIO E11
- VCCIO D14
- VCCIO D13
- VCCIO D12
- VCCIO D11
- VCCIO C14
- VCCIO C12
- VCCIO C11
- VCCIO B14
- VCCIO B12
- VCCIO A14
- VCCIO A13
- VCCIO A12
- VCCIO A11
- VCCIO J23

For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7  
For CRB VIDALERT# need to pull high 75 ohm close to CPU



<Core Design>

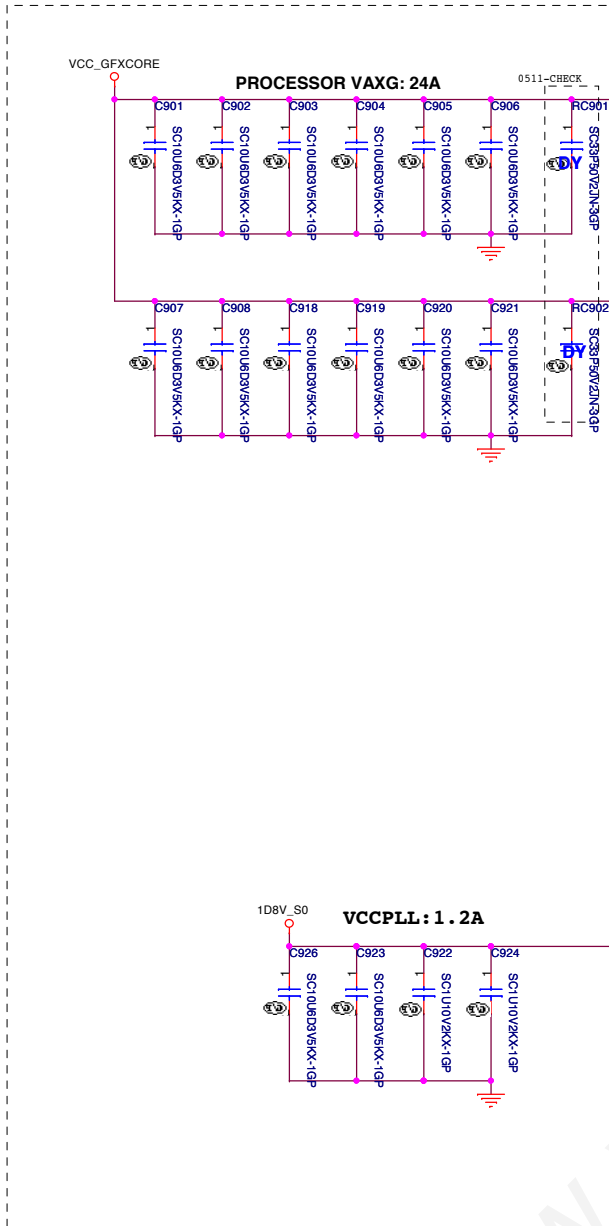
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Title: **CPU (VCC CORE)**

Size	Document Number	Rev
Custom	<b>LA480</b>	SD
Date:	Friday, January 06, 2012	Sheet 8 of 103



0511-CHECK CAP



### POWER

CPU1G 7 OF 9	
SANDY	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
GRAPHICS	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
	VAXG
1.8V RAIL	VCCPLL
	VCCPLL
	VCCPLL
	VCCPLL
	VCCPLL
	VCCPLL
	VCCPLL
	VCCPLL
	VCCPLL
	VCCPLL
SA RAIL	VCCSA
	VCCSA
	VCCSA
	VCCSA
	VCCSA
	VCCSA
	VCCSA
	VCCSA
	VCCSA
	VCCSA
MISC	VCCSA_SENSE
	VCCSA_SELECT0
	VCCSA_SELECT1
	VCCSA_SELECT0
	VCCSA_SELECT1
	VCCSA_SELECT0
	VCCSA_SELECT1
	VCCSA_SELECT0
	VCCSA_SELECT1
	VCCSA_SELECT0

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2nd = 62.10040.771

#### SENSE LINES

#### VREF

#### DDR3 - 1.5V RAILS

#### SA RAIL

#### MISC

VAXG\_SENSE AK35  
VSSAXG\_SENSE AK34

VCC\_AXG\_SENSE 42  
VSS\_AXG\_SENSE 42

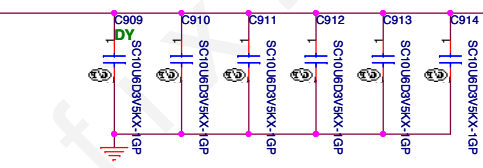
+V\_SM\_VREF\_CNT should have 10 mil trace width

SM\_VREF AL1

Routing Guideline:  
Power from DDR VREF S3 and +V SM\_VREF\_CNT should have 10 mils trace width.

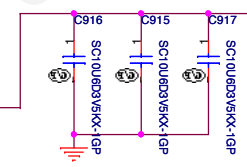
#### VDDQ: 5A

- VDDQ AF7
- VDDQ AF4
- VDDQ AC7
- VDDQ AC4
- VDDQ AC1
- VDDQ Y7
- VDDQ Y4
- VDDQ Y1
- VDDQ LJ7
- VDDQ LJ4
- VDDQ LJ1
- VDDQ P7
- VDDQ P4
- VDDQ P1



#### VCCA: 6A

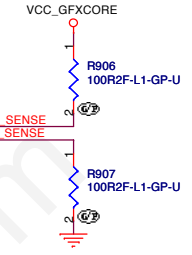
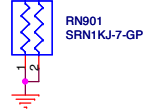
- VCCSA M27
- VCCSA M26
- VCCSA L26
- VCCSA J26
- VCCSA J25
- VCCSA J24
- VCCSA H26
- VCCSA H25



+V0.85S - VCCSA - System Agent rail voltage can be [0.9, 0.725, 0.8, 0.675] V for IVB [0.9, 0.8] V for SNB

VCCSA\_SENSE H23

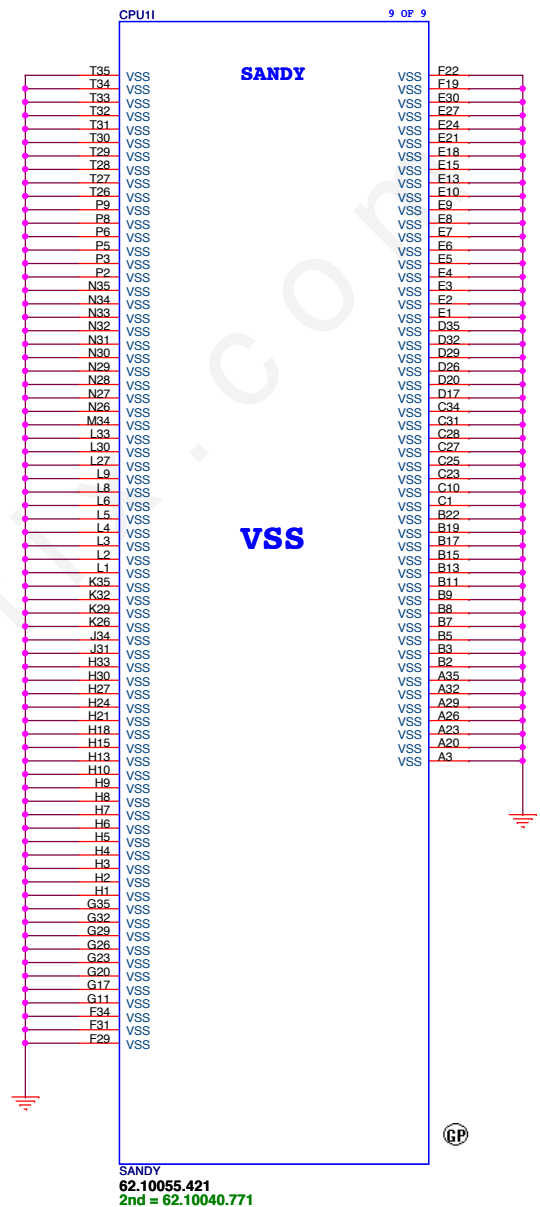
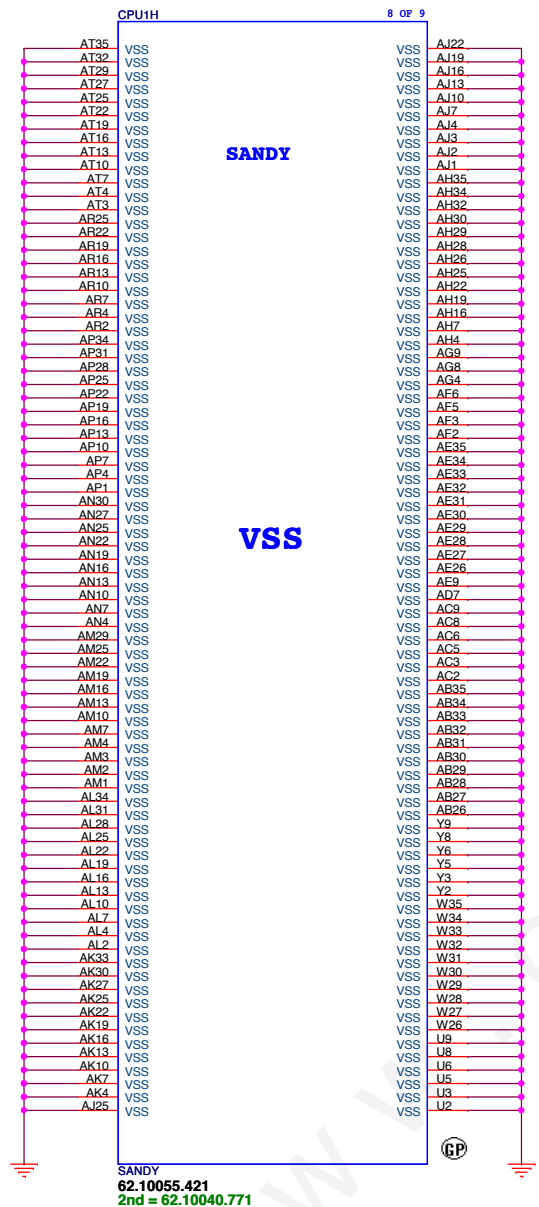
VCCSA\_SELECT0 48  
VCCSA\_SELECT1 48



<Core Design>

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Title <b>CPU (VCC GFXCORE)</b>		
Size A3	Document Number <b>LA480</b>	Rev SD
Date Friday, January 06, 2012	Sheet 9	of 103



<Core Design>

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Title: **CPU (VSS)**

Size: A3	Document Number: LA480	Rev: SD
Date: Friday, January 06, 2012	Sheet: 10	of: 103

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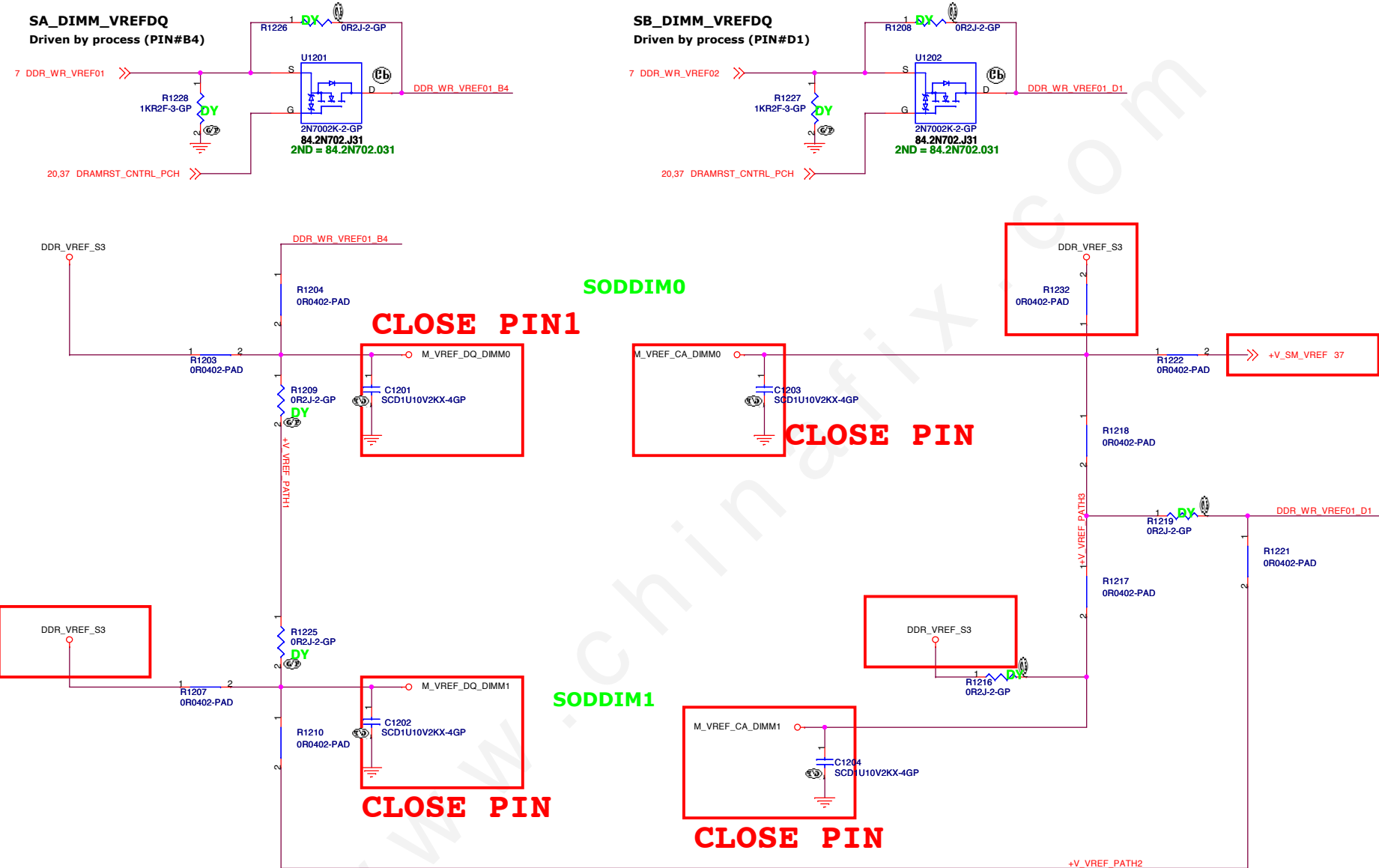
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<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C
Title <Title>		
Size A4	Document Number LA480	Rev SD
Date:	Friday, January 06, 2012	Sheet 11 of 103

# VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations are acceptable if required due to tight routing constraints.



<Core Design>		
緯創資通		Wistron Corporation
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Title		
<b>M3</b>		
Size	Document Number	Rev
A3	LA480	SD
Date:	Friday, January 06, 2012	Sheet 12 of 103



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Title		
<Title>		

Size	Document Number	Rev
A4	LA480	SD

**SSID = MEMORY**

Pin	Signal Name	Pin	Signal Name
M.A.A0	96	NP1	MP1
M.A.A1	97	NP2	MP2
M.A.A2	98	RAS#	M.A.RAS# 6
M.A.A3	99	WE#	M.A.WE# 6
M.A.A4	100	CAS#	M.A.CAS# 6
M.A.A5	101	CS#0	M.A.DIMM_CS#0 6
M.A.A6	102	CS#1	M.A.DIMM_CS#1 6
M.A.A7	103	CKE#	M.A.DIMM_CKE# 6
M.A.A8	104	CKE#1	M.A.DIMM_CKE#1 6
M.A.A9	105	CKE#2	M.A.DIMM_CKE#2 6
M.A.A10	106	CKE#3	M.A.DIMM_CKE#3 6
M.A.A11	107	CKE#4	M.A.DIMM_CKE#4 6
M.A.A12	108	CKE#5	M.A.DIMM_CKE#5 6
M.A.A13	109	CKE#6	M.A.DIMM_CKE#6 6
M.A.A14	110	CKE#7	M.A.DIMM_CKE#7 6
M.A.A15	111	CKE#8	M.A.DIMM_CKE#8 6
M.A.A16	112	CKE#9	M.A.DIMM_CKE#9 6
M.A.A17	113	CKE#10	M.A.DIMM_CKE#10 6
M.A.A18	114	CKE#11	M.A.DIMM_CKE#11 6
M.A.A19	115	CKE#12	M.A.DIMM_CKE#12 6
M.A.A20	116	CKE#13	M.A.DIMM_CKE#13 6
M.A.A21	117	CKE#14	M.A.DIMM_CKE#14 6
M.A.A22	118	CKE#15	M.A.DIMM_CKE#15 6
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M.A.A24	120	CKE#17	M.A.DIMM_CKE#17 6
M.A.A25	121	CKE#18	M.A.DIMM_CKE#18 6
M.A.A26	122	CKE#19	M.A.DIMM_CKE#19 6
M.A.A27	123	CKE#20	M.A.DIMM_CKE#20 6
M.A.A28	124	CKE#21	M.A.DIMM_CKE#21 6
M.A.A29	125	CKE#22	M.A.DIMM_CKE#22 6
M.A.A30	126	CKE#23	M.A.DIMM_CKE#23 6
M.A.A31	127	CKE#24	M.A.DIMM_CKE#24 6
M.A.A32	128	CKE#25	M.A.DIMM_CKE#25 6
M.A.A33	129	CKE#26	M.A.DIMM_CKE#26 6
M.A.A34	130	CKE#27	M.A.DIMM_CKE#27 6
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M.A.A36	132	CKE#29	M.A.DIMM_CKE#29 6
M.A.A37	133	CKE#30	M.A.DIMM_CKE#30 6
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M.A.A64	160	CKE#57	M.A.DIMM_CKE#57 6
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M.A.A70	166	CKE#63	M.A.DIMM_CKE#63 6
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M.A.A73	169	CKE#66	M.A.DIMM_CKE#66 6
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M.A.A77	173	CKE#70	M.A.DIMM_CKE#70 6
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M.A.A119	215	CKE#112	M.A.DIMM_CKE#112 6
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M.A.A122	218	CKE#115	M.A.DIMM_CKE#115 6
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M.A.A145	241	CKE#138	M.A.DIMM_CKE#138 6
M.A.A146	242	CKE#139	M.A.DIMM_CKE#139 6
M.A.A147	243	CKE#140	M.A.DIMM_CKE#140 6
M.A.A148	244	CKE#141	M.A.DIMM_CKE#141 6
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M.A.A150	246	CKE#143	M.A.DIMM_CKE#143 6
M.A.A151	247	CKE#144	M.A.DIMM_CKE#144 6
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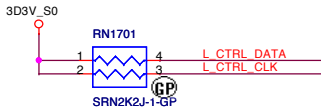
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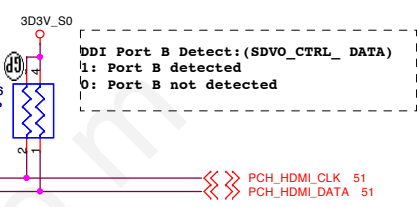
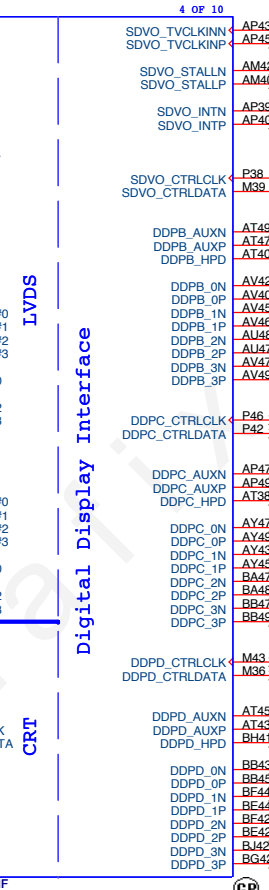
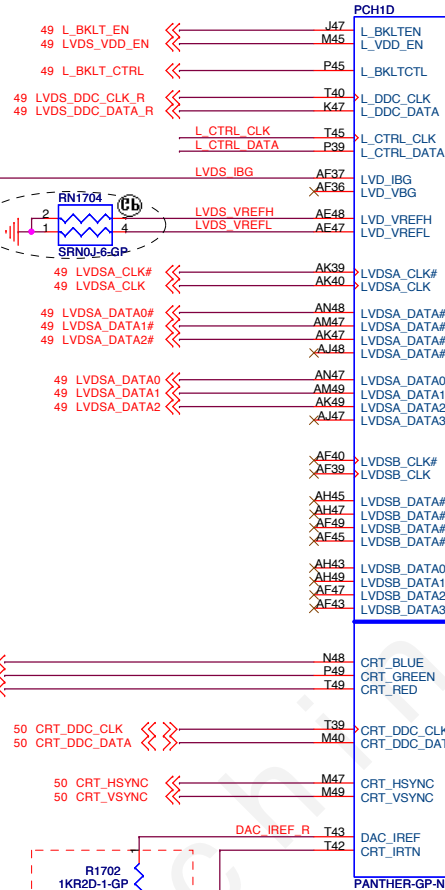
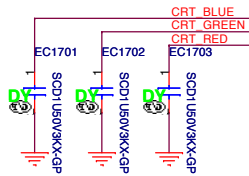
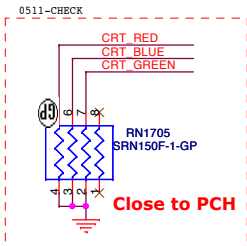
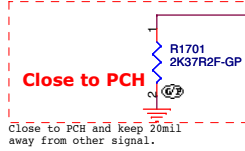
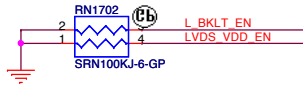
<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>DDR3-SODIMM2</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 16	of 103

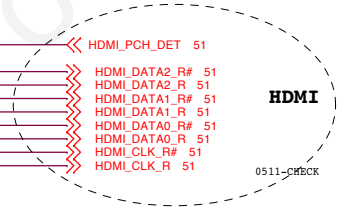




**L\_DDC\_DATA(K47):**  
This signal is on the LVDS interface.  
This signal needs to be left NC if eDP is  
used for the local flat panel display



**DDI Port B Detect: (SDVO\_CTRL\_DATA)**  
1: Port B detected  
0: Port B not detected

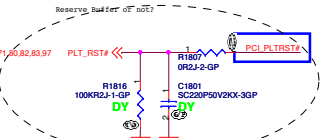
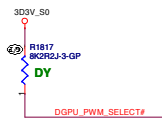
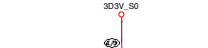
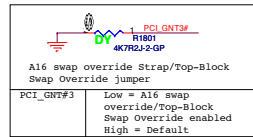


PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_0N	TMDSB_DATA2#
	DDPB_0P	TMDSB_DATA2#
	DDPB_1N	TMDSB_DATA1#
	DDPB_1P	TMDSB_DATA1#
	DDPB_2N	TMDSB_DATA0#
	DDPB_2P	TMDSB_DATA0#
	DDPB_3N	TMDSB_CLK#
	DDPB_3P	TMDSB_CLK#
	DDPB_AUXN	NA
	DDPB_AUXP	NA
	DDPB_HPD	HDMI_B_HPD
	SDVO_CTRLCLK	HDMI_B_CTRLCLK
SDVO_CTRLDATA	HDMI_B_CTRLDATA	

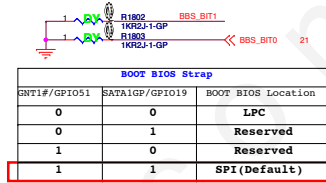
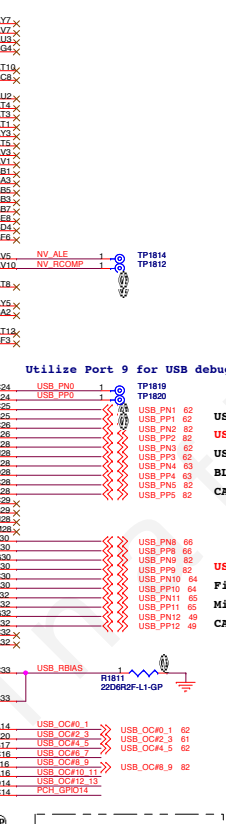
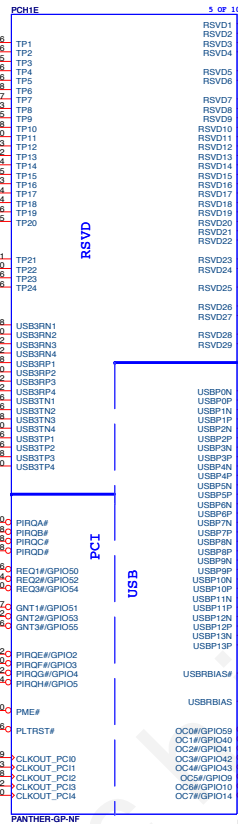
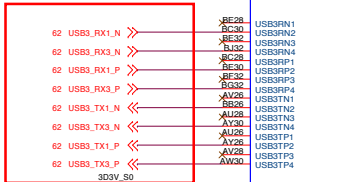
**Notes:**  
1K 0.5% 0402

The recommended value for this external resistor is 1.0 k ±0.5%. The CRT DAC outputs may be measured when the display is completely white. If CRT DAC signal voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the reference resistor value is optimal for the motherboard design.

**SSID = PCH**



**For PPT USB3.0 feature**



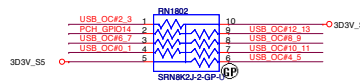
**Gx8 USB Table**

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	CARD READER
6	X
7	X
8	3G
9	USB2.0, ext. port 3
10	Fingerprint
11	Mini Card1 (WLAN)
12	CAMERA
13	X

- USB3.0 ext port 1
- USB2.0 ext port 4
- USB3.0 ext port 2
- BLUETOOTH
- CARD READER
- USB2.0 ext port 3
- Fingerprint
- Mini Card1 (WLAN)
- CAMERA

Pin	Default Port Mapping	Pin	Default Port Mapping
OC#F	Port 8, Port 3	OC#F	Port 8, Port 9
OC#F	Port 2, Port 3	OC#F	USB_OC#2_3 61
OC#F	Port 4, Port 5	OC#F	USB_OC#4_5 62
OC#F	Port 6, Port 7	OC#F	Port 10, Port 11
		OC#F	Port 12, Port 13
			Not Used

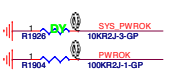
OC[3:0]# for Device 29 (Ports 0-7)  
OC[7:4]# for Device 26 (Ports 8-13)



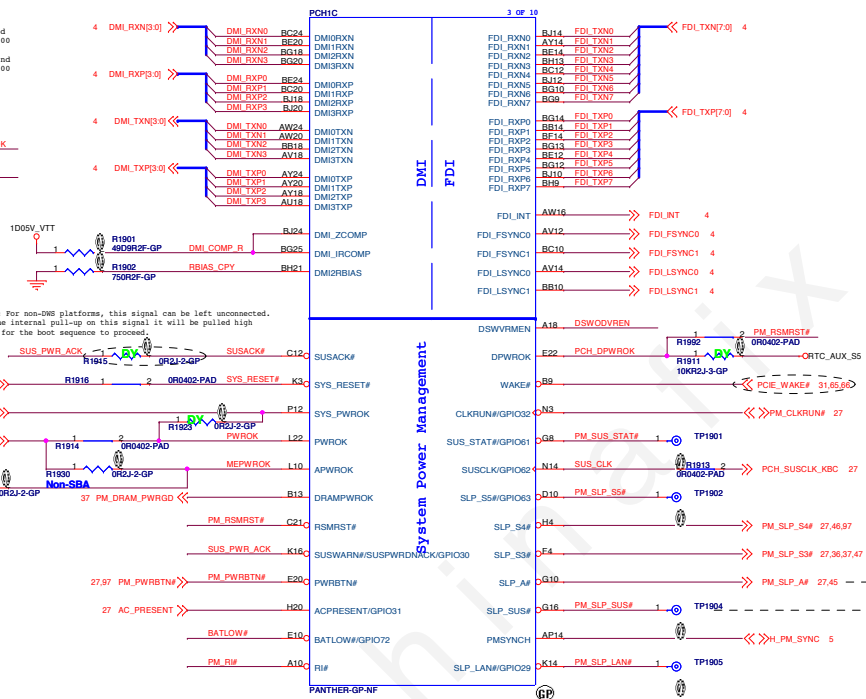


For platforms not supporting Deep S4/S5  
 1.VccSUS3\_3 and VccDSW3\_3 will rise at the same time (connected on board)  
 2.DPWROK and RSMRST# will rise at the same time (connected on board)  
 3.SLP\_SUS# and SUSACK# are left as 'no connect'  
 4.SUSWRN# used as SUSWRDNACK/GPIO30

Signal Routing Guideline:  
 DMI\_ZCOMP keep W#4 mils and routing length less than 300 mils.  
 DMI\_IRCOMP keep W#4 mils and routing length less than 300 mils.



Platforms supporting Deep S4/S5, but not 10KR2J-3-GP to participate in the handshake during wake and Deep S4/S5 entry may tie SUSACK# to SUSWRN#.



DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

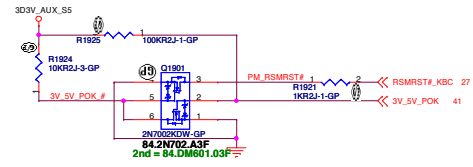
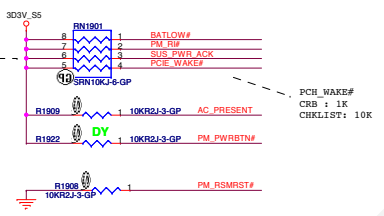
SUS\_PWRCK: the system is ready to start the exit from reset (de-asserts PC\_RST# to the processor)  
 PWRROK: it indicates to PCH that its CORE well power is stable.

Active Sleep Well (ASW) Power OK  
 80\_PWR\_GOOD after PM\_SLP\_S3F delay 200 ms

This signal is used to control power planes to the Intel® ME sub-system. This signal will be asserted in M-off state. If M3 is not supported then SLP\_A# will have the same timings as SLP\_S3F.

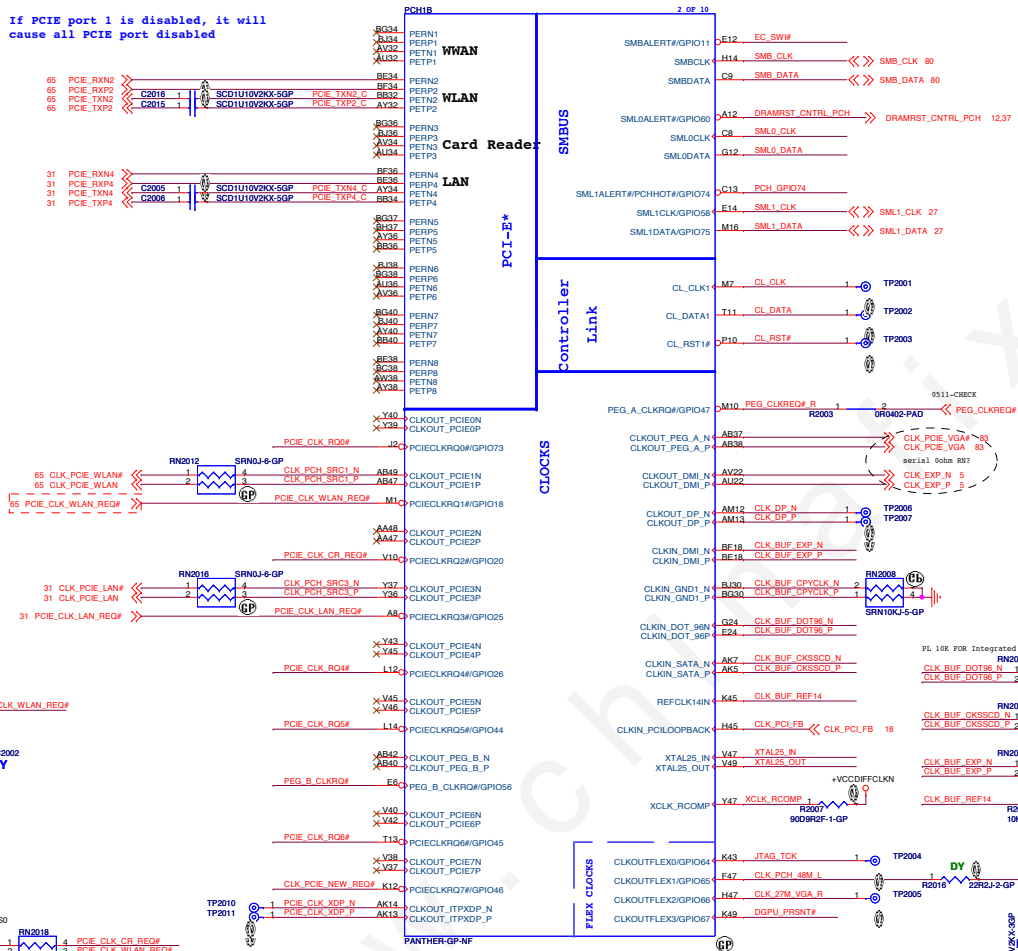
For platforms supporting Deep S4/S5 state, a low on this signal indicates that PCH is in Deep Sleep state and that EC/platform logic does not need to keep the Suspend Rails ON.  
 If high means EC must keep SUS rails ON.  
 If Deep S4/S5 is not supported, then this pin can be left unconnected.

SUSWRDNACK: No longer requires a 10-K pull-up to VccSUS3 (3.3 V).

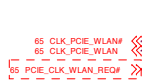


**SSID = PCH**

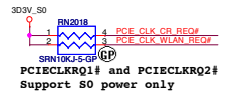
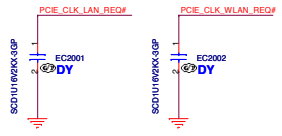
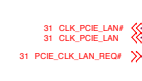
If PCIe port 1 is disabled, it will cause all PCIe port disabled



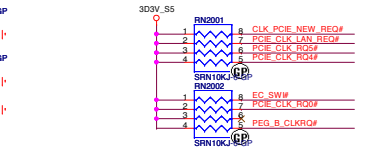
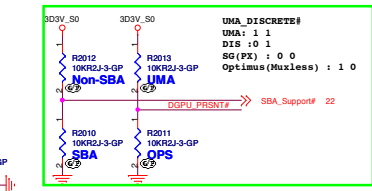
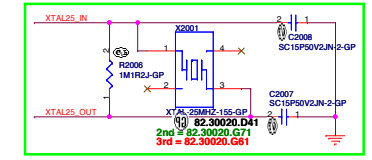
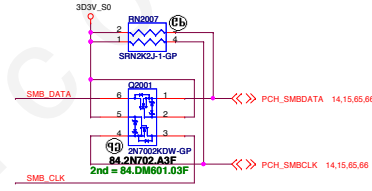
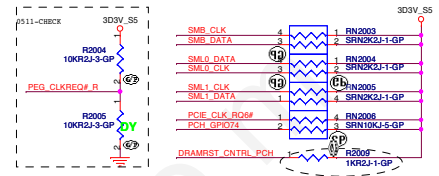
**WLAN CLK**

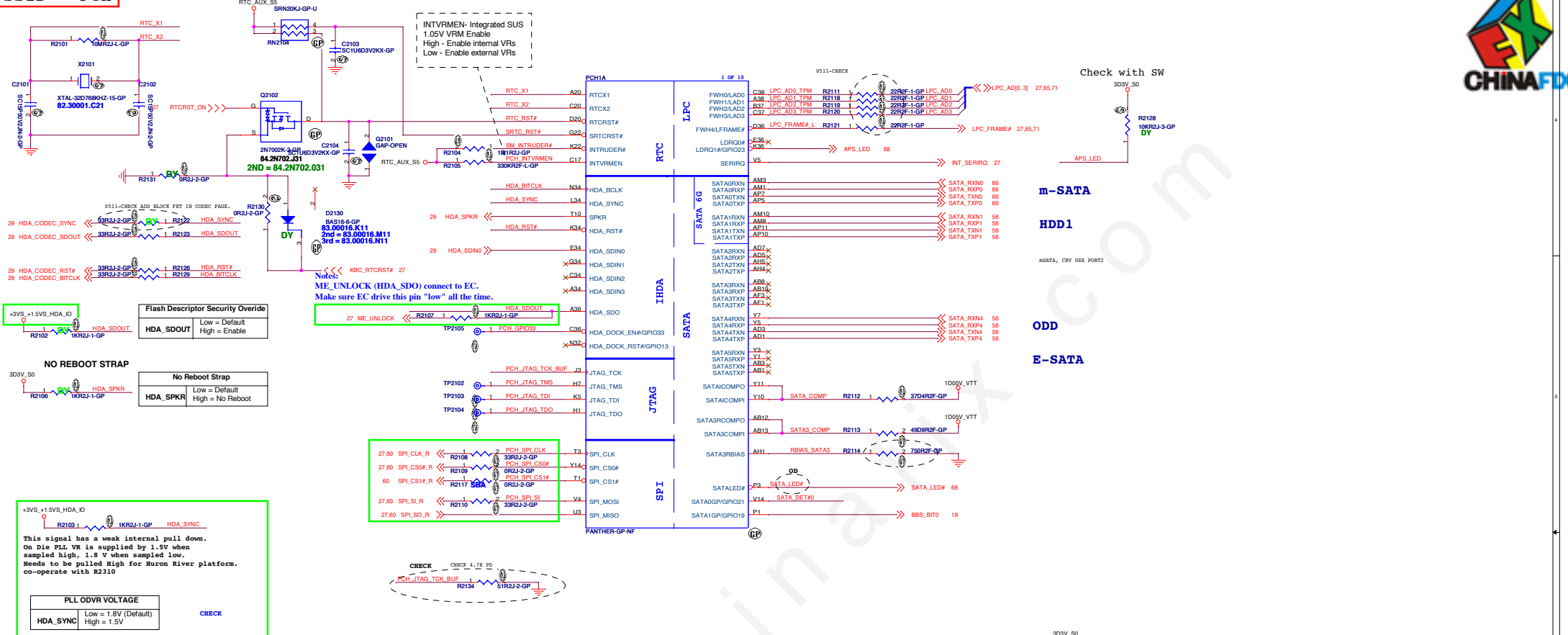


**LAN CLK**



- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3  
 - Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.





29 HDA\_CODEC\_SYNC << 33R2J-2-GP << 1 R2122 HDA\_SYNC  
 29 HDA\_CODEC\_SDOOUT << 33R2J-2-GP << 1 R2123 HDA\_SDOOUT  
 29 HDA\_CODEC\_RST# << 33R2J-2-GP << 1 R2128 HDA\_RST#  
 29 HDA\_CODEC\_BITCLK << 33R2J-2-GP << 1 R2129 HDA\_BITCLK

**Flash Descriptor Security Override**

HDA_SDOOUT	Low = Default High = Enable
------------	--------------------------------

**NO REBOOT STRAP**

HDA_SPKR	Low = Default High = No Reboot
----------	-----------------------------------

**+3VS\_+1.5VS\_HDA\_ID**

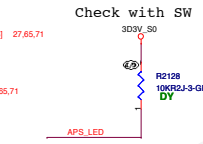
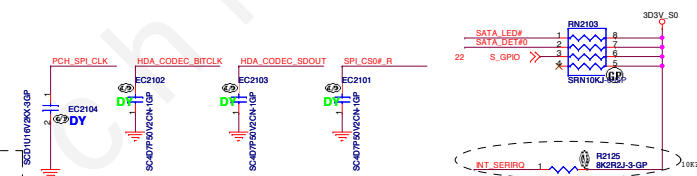
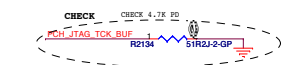
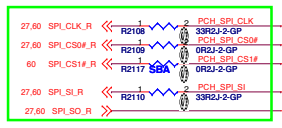
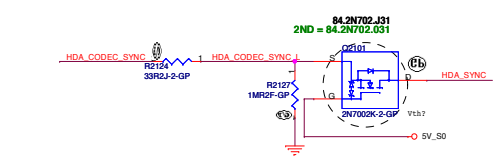
This signal has a weak internal pull down.  
 On Die PLL VR is supplied by 1.5V when sampled high, 1.8V when sampled low.  
 Needs to be pulled High for Huron River platform.  
 co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.5V (Default) High = 1.5V

CHECK

This signal has a weak internal pull-down.  
 On Die PLL VR is supplied by 1.5V from VccVRM when sampled high, 1.8V from VccVRM when sampled low.

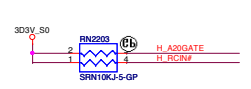
**HDA\_SYNC**: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.



Check with SW

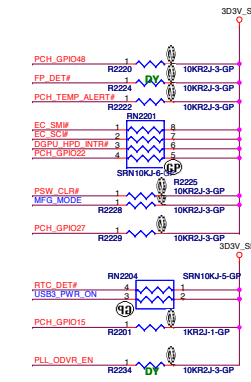
m-SATA  
 HDD1  
 #SATA, CRV USE PORT2  
 ODD  
 E-SATA

R2202  
HR:200K (64.20035.6DL)  
CRV:10K (63.10334.1DL)

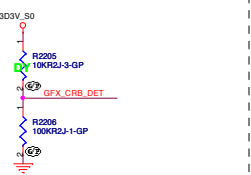


GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.

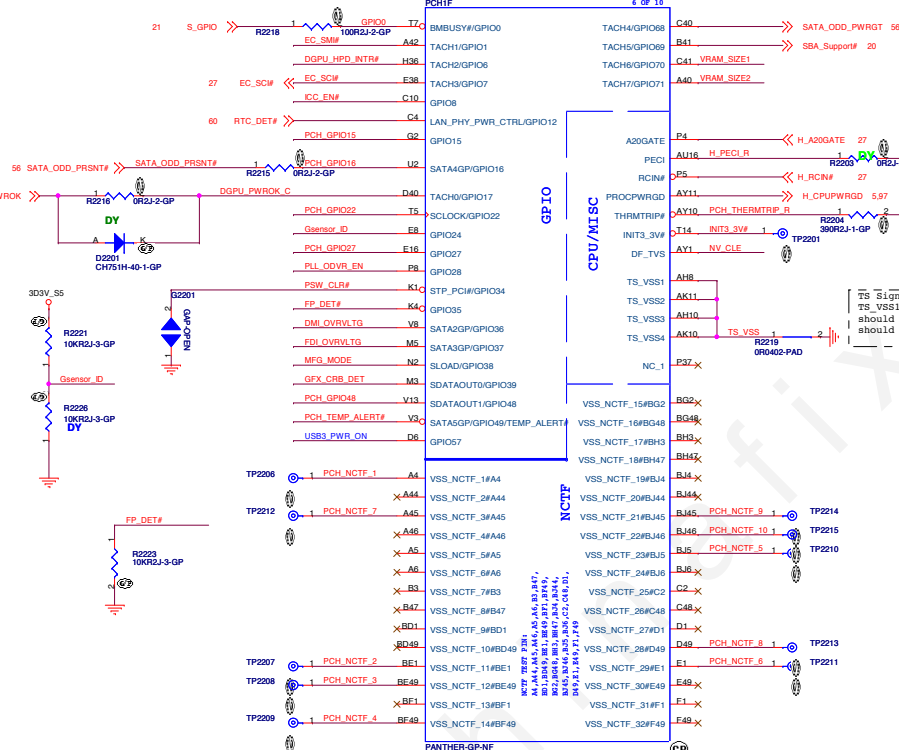
G-Sensor	ST	KIXNOK
R2226	DY	10K
R2221	10K	DY



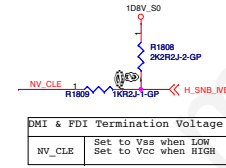
	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



Note:  
For PCH debug with XDP, need to NO STUFF R2218



PLL ON DIE VR ENABLE  
NOTE: This signal has a weak internal pull-up 20K  
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT  
DISABLED -- LOW (R2212 STUFFED)



DMI & FDI Termination Voltage  
NV\_CLE Set to Vss when LOW  
Set to Vcc when HIGH

TS Signal Disable Guideline:  
TS\_VSS1, TS\_VSS2, TS\_VSS3 and TS\_VSS4  
should not float on the motherboard. They  
should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE  
GPIO37 (FDI\_OVRVLTG) LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE  
GPIO36 (DMI\_OVRVLTG) LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

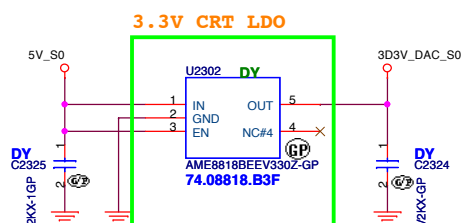
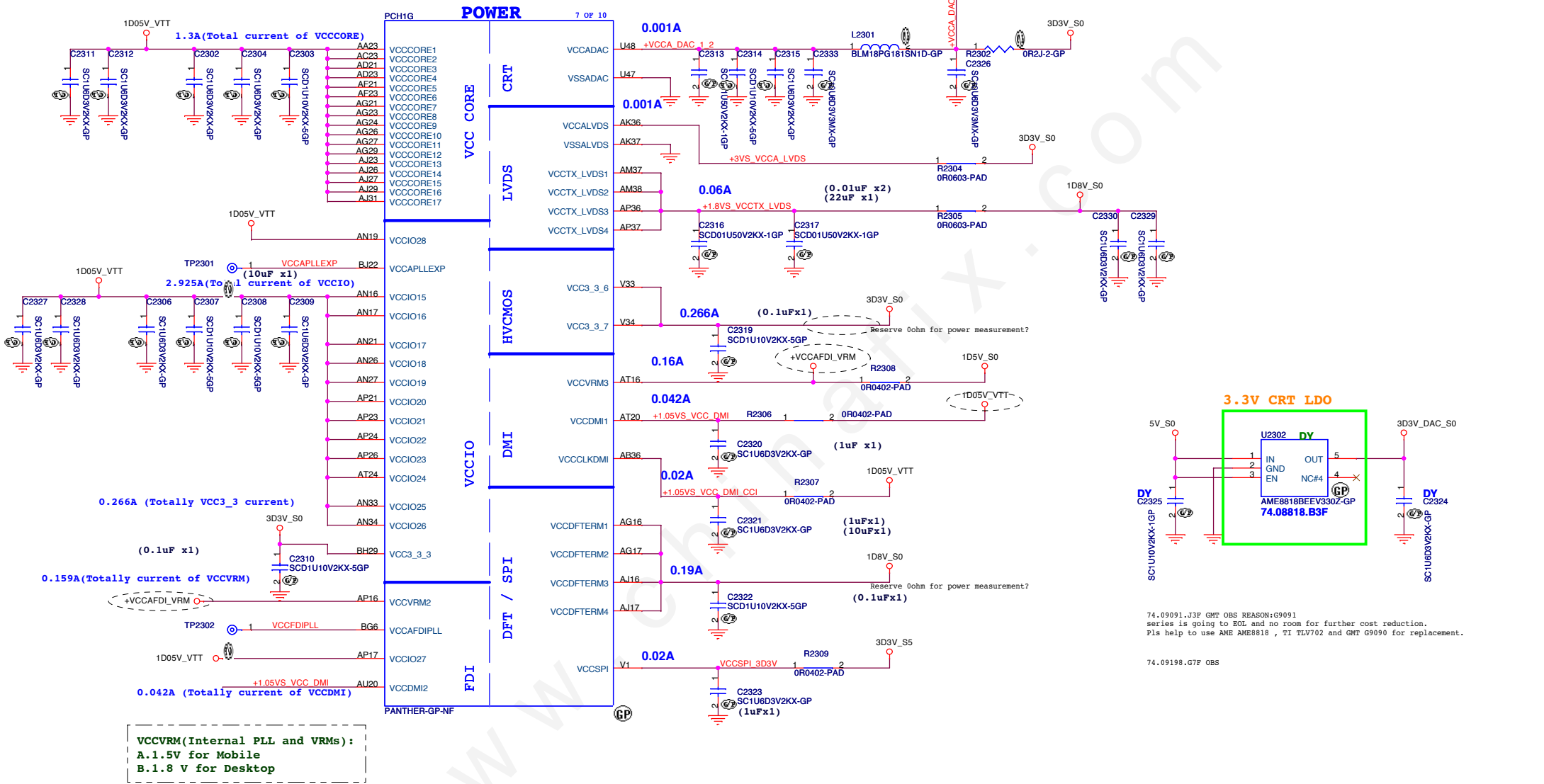
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable  
ICC\_EN# HIGH (R2211 DY) - DISABLED [DEFAULT]  
LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up.  
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

R2211 BOM CTRL  
HR:1K  
CRV:DY

6A

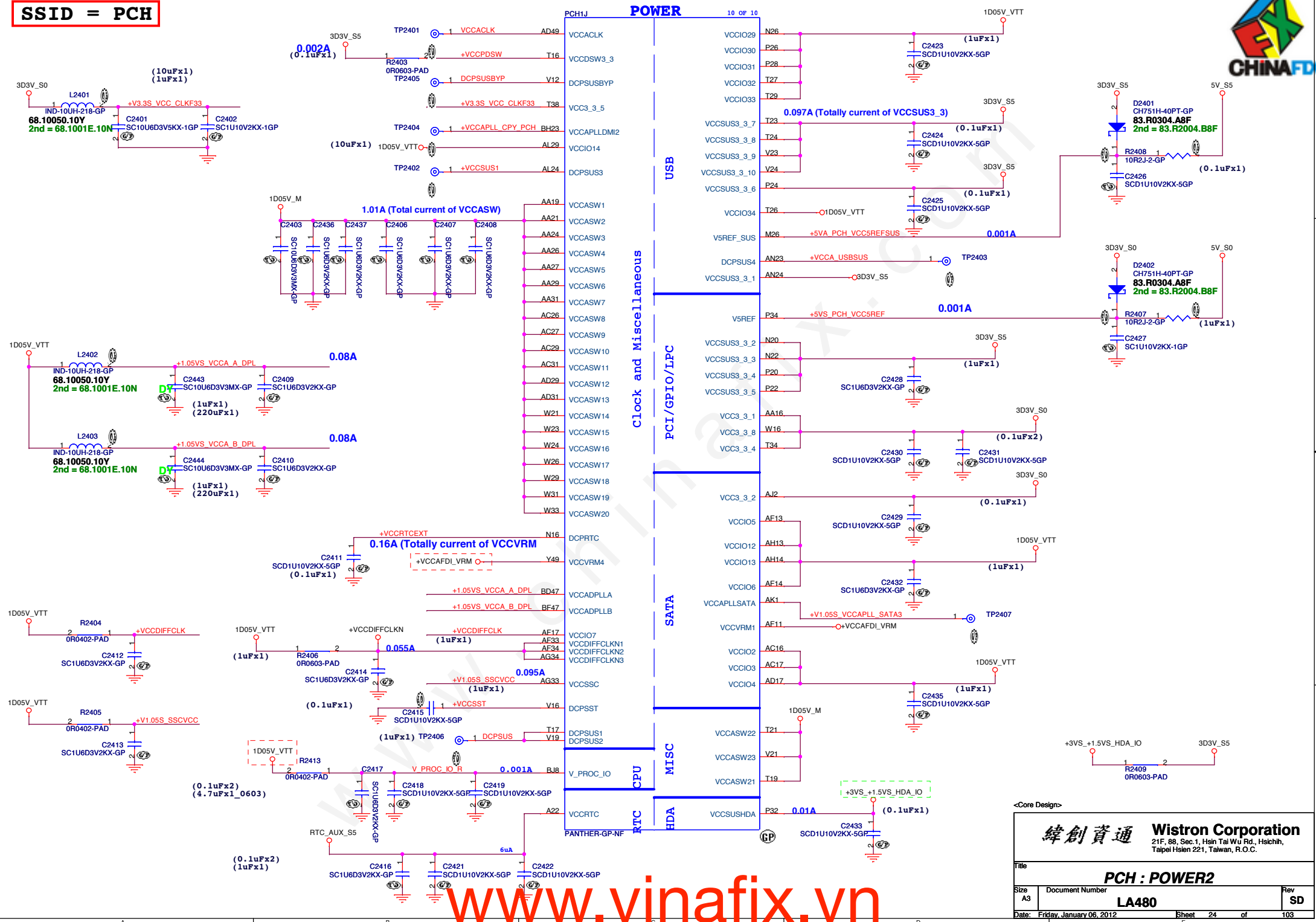


74.09091.J3F GMT OBS REASON:G9091 series is going to EOL and no room for further cost reduction. Pls help to use AME AME8818 , TI TLV702 and GMT G9090 for replacement.

74.09198.G7F OBS

Refer to NPCE795 shared SPI flash architecture

SSID = PCH

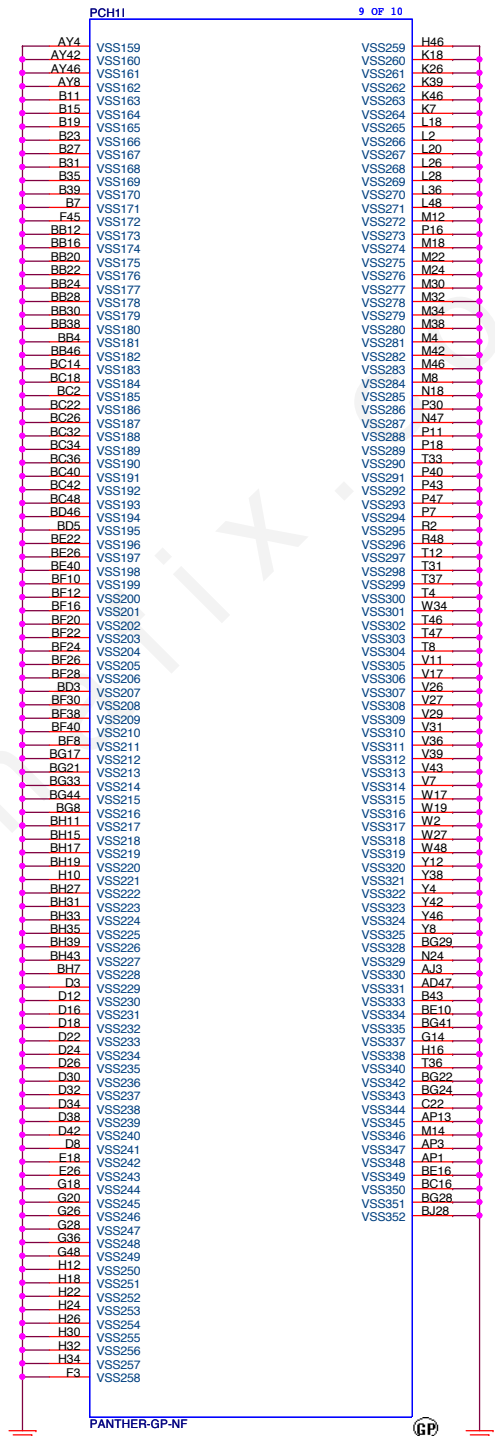
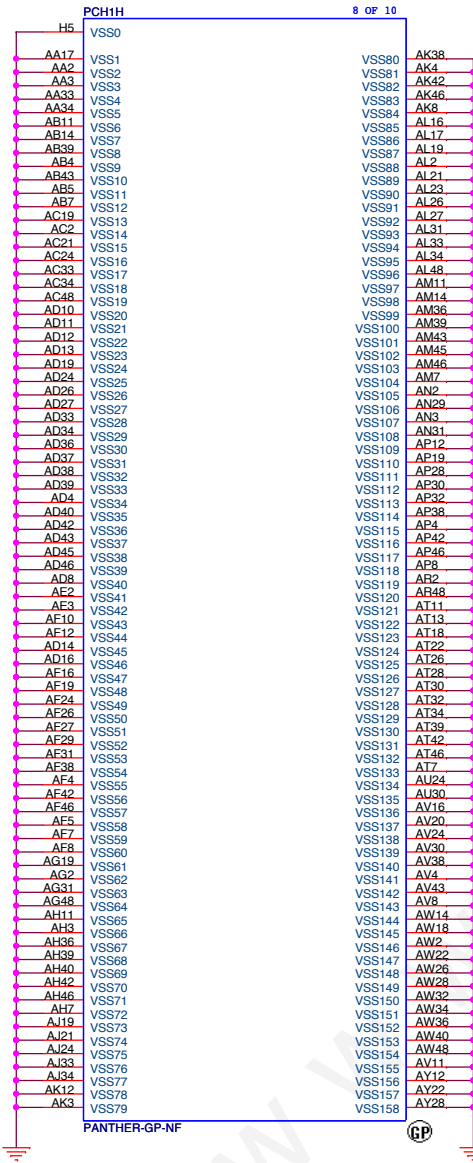


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<p>Title: <b>PCH : POWER2</b></p>		
Size: A3	Document Number: <b>LA480</b>	Rev: <b>SD</b>
Date: Friday, January 06, 2012	Sheet: 24	of 103



SSID = PCH



<Core Design>

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH : VSS**

Size: A3 Document Number: **LA480** Rev: **SD**

Date: Friday, January 06, 2012 Sheet 25 of 103

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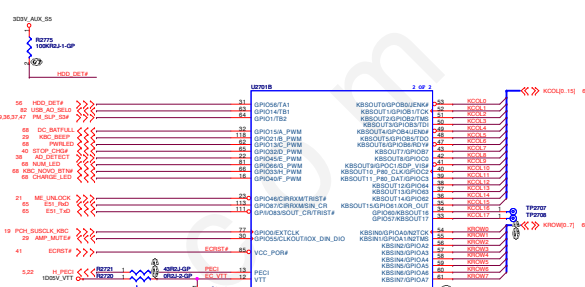
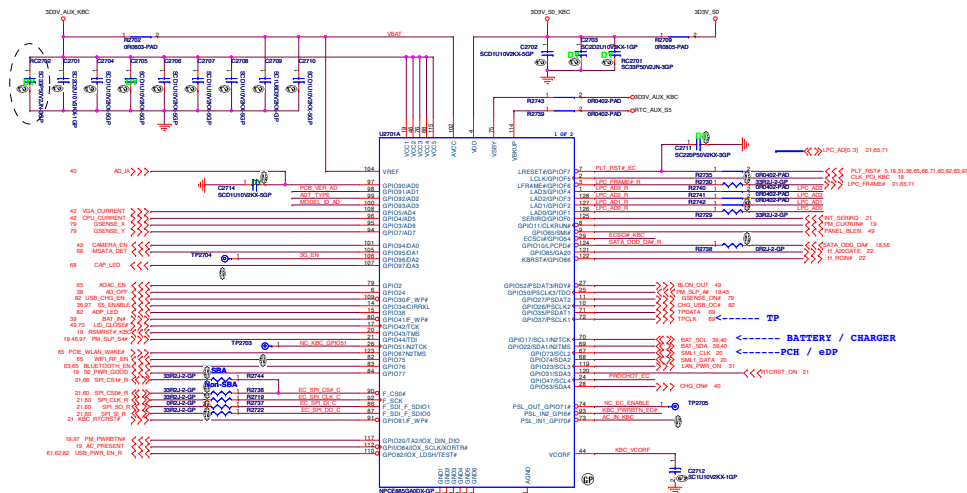
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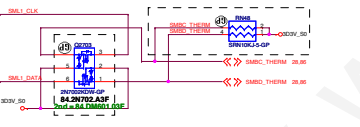
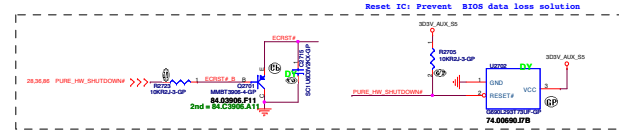
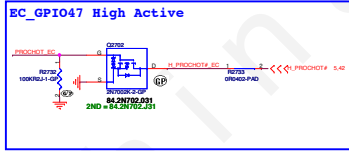
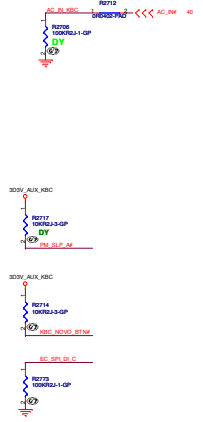
<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 26	of 103

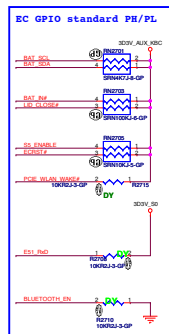
SSID = KBC



Code change to Low Active on 8/19



MODEL_ID_AD (Pin100)	Pull Down	Pull High	Voltage
UMA	100.0K	33.0K	2.481V
OPTI00B	100.0K	47.0K	2.245V

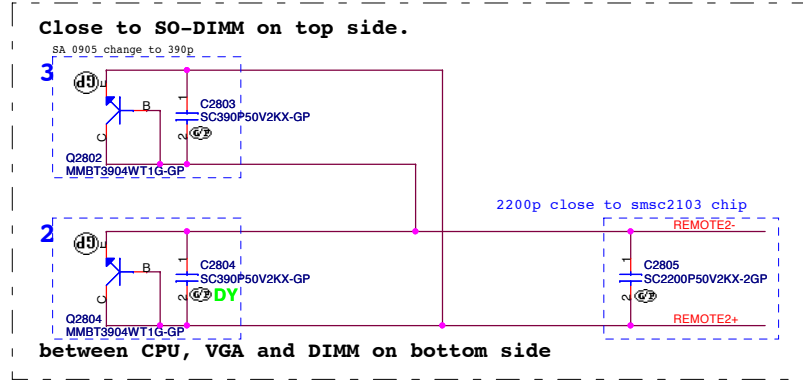


PCB Version A/B (Pin#)	Full-Low Resistor	Full-High Resistor (303V_AUX_85)	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.45V
+L	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

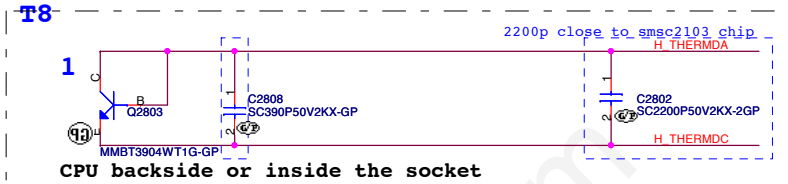
71.00885.A0G  
IC EMB CTRL NPCE885PA0DX LQFP 128P

**SSID = Thermal**

# Thermal sensor

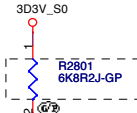
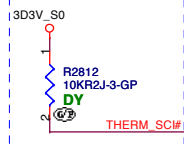


20110718 Carrey:  
For Vendor suggestion, add 390pF Cap. as closed to pin B/C and E of Q2803

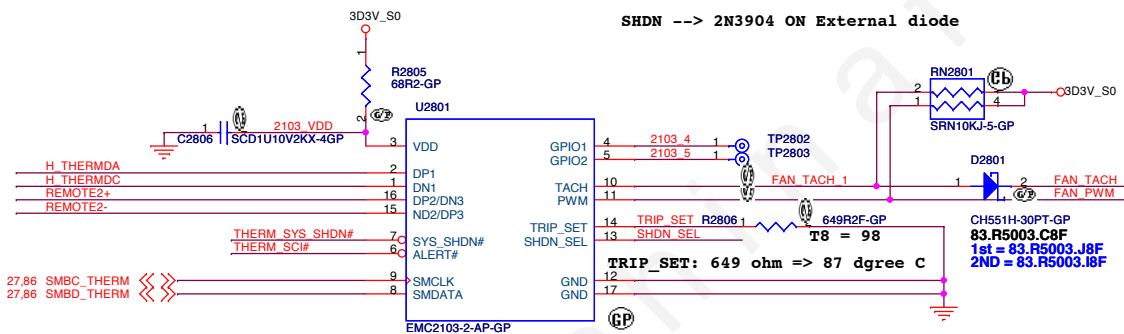


**CPU TEMP:**  
H\_THERMDA and H\_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

20110718 Carrey:  
For Vendor suggestion, add 10k pull high to 3D3V\_S0

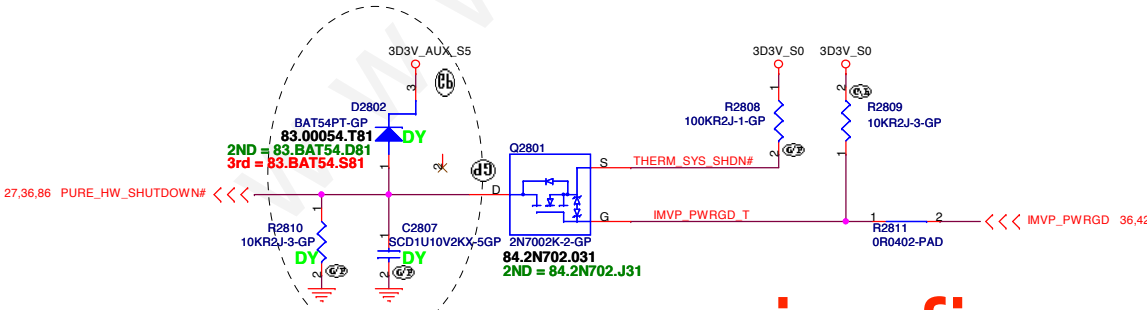
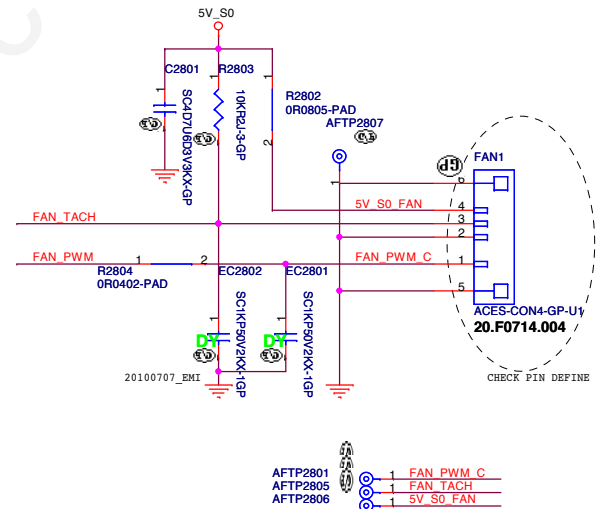


SHDN --> 2N3904 ON External diode



pin6, ALERT# OD  
pin7, SYS\_SHDN# OD

## 4 WIRE PWM Fan Control circuit



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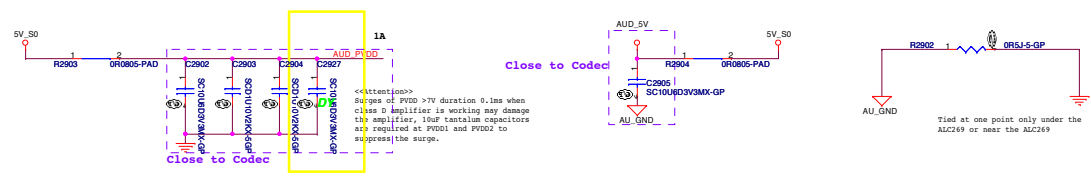
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**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

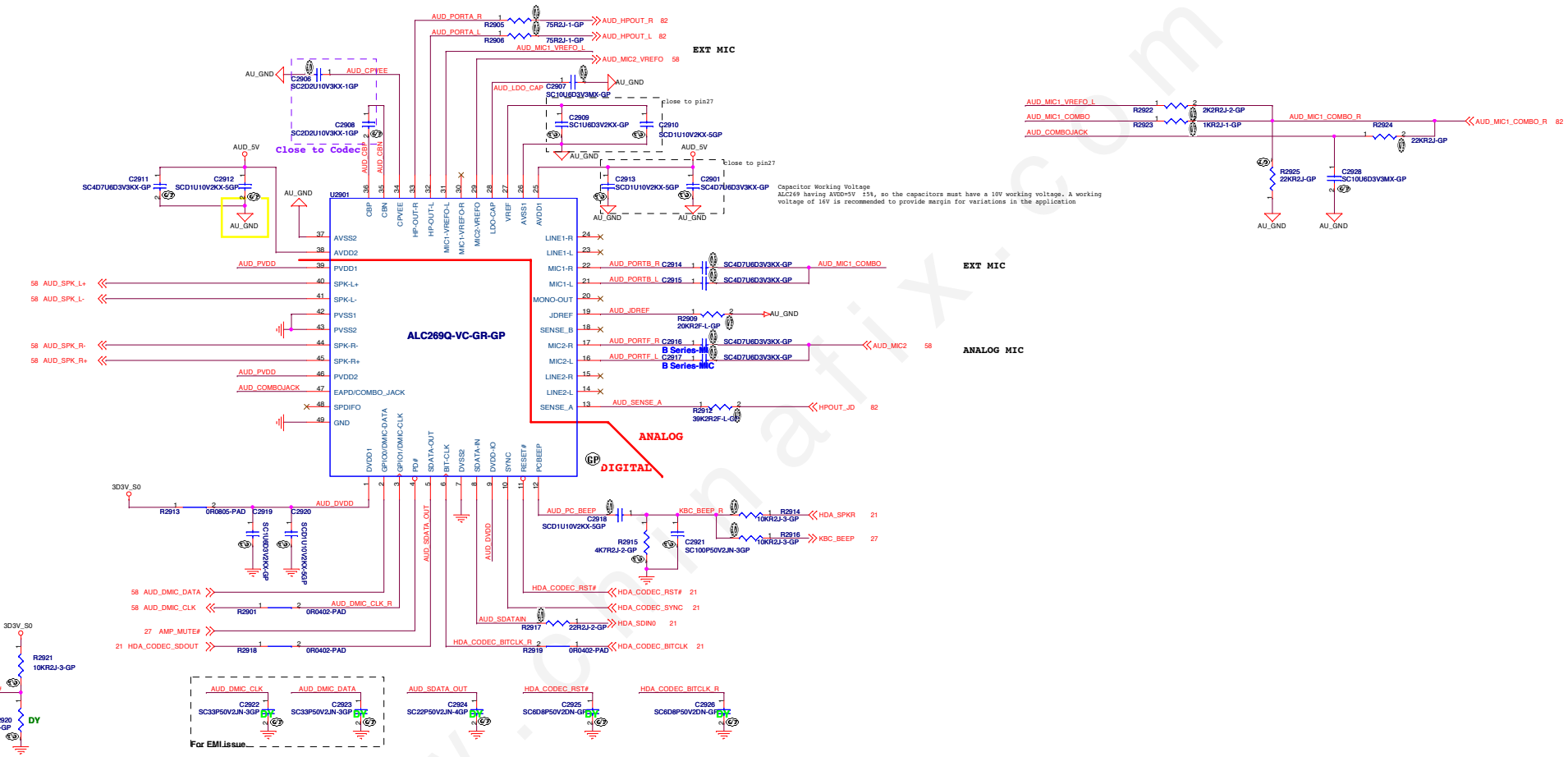
Title: **THERMAL SENSOR SMSC EMC2103**

Size A3 Document Number: **LA480** Rev: **SD**

Date: Friday, January 06, 2012 Sheet 28 of 103



<<Attention>>  
 Burges of PVD >TV duration 0.1ms when class D amplifier is working may damage the amplifier. 10uF tantalum capacitors are required at PVD01 and PVD02 to suppress the surge.



For EMI Issue

20100705\_AUD

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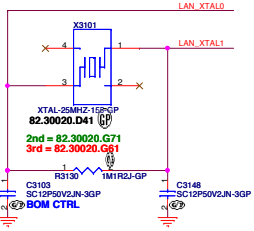
www.chinafix.com

www.vinafix.vn

<Core Design>

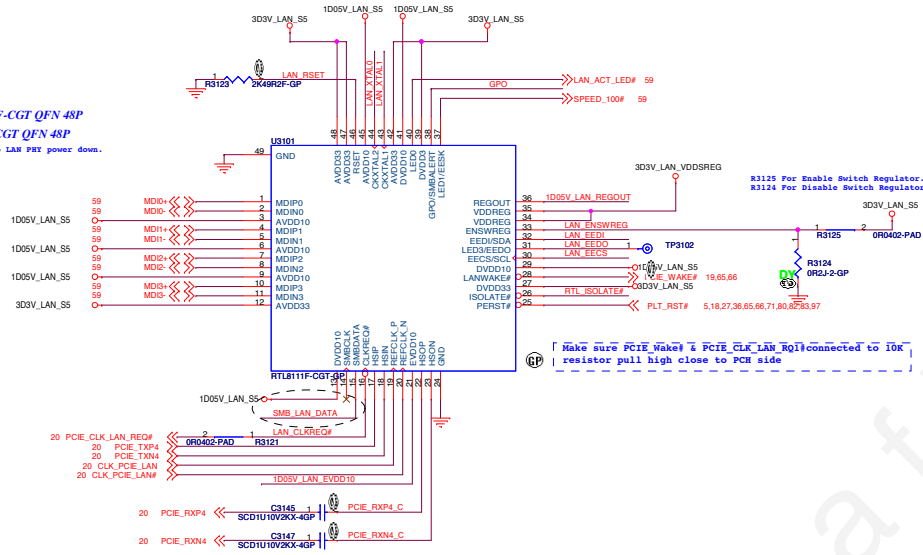
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date:	Friday, January 06, 2012	Sheet	30 of 103

**25MHz XTAL**



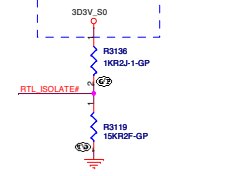
	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF

71.08111.N03\_IC PCIE CTRL.RTL8111F-CGT QFN 48P  
 71.08111.J03\_IC PCIE-E.RTL8111E-VL-CGT QFN 48P  
 8111F can use GPIO to inform system to do LAN PWR power down.

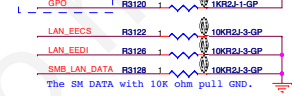


Make sure PCIE\_Wake# & PCIE\_CLK\_LAN\_Roll connected to 10K resistor pull high close to PCH side

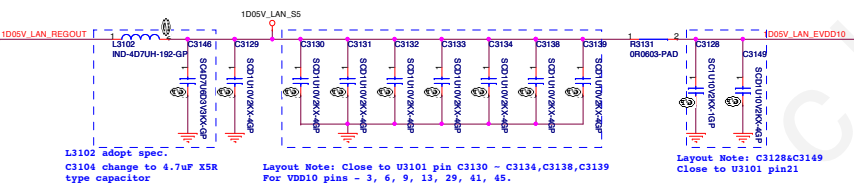
main pwr if have no ASF



High:Link up  
Low:Link down



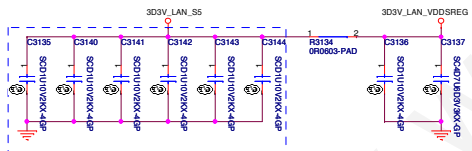
The SM DATA with 10K ohm pull GND.



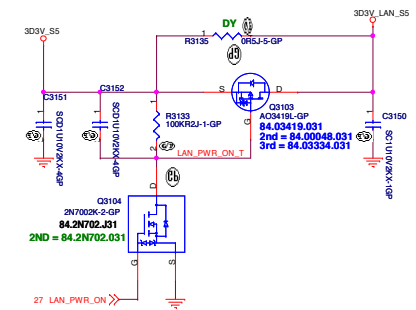
L3102 300pF spec.  
C3104 change to 4.7uF XSR type capacitor

Layout Note: Close to U3101 pin C3130 - C3134, C3138, C3139 For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149 Close to U3101 pin21



Layout Note: C3135, C3140-C3144 Close to U3101 pin For VDD33 pins - 12, 27, 39, 42, 47, 48.



2ND = 84.2N702.031



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<Core Design>

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **Reserved**

Size A4	Document Number <b>LA480</b>	Rev <b>SD</b>
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Date: Friday, January 06, 2012 Sheet 33 of 103

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<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 34	of 103



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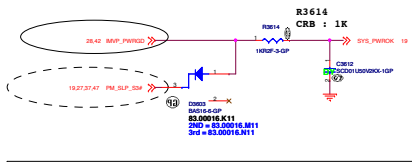
www.chinafix.com

www.vinafix.vn

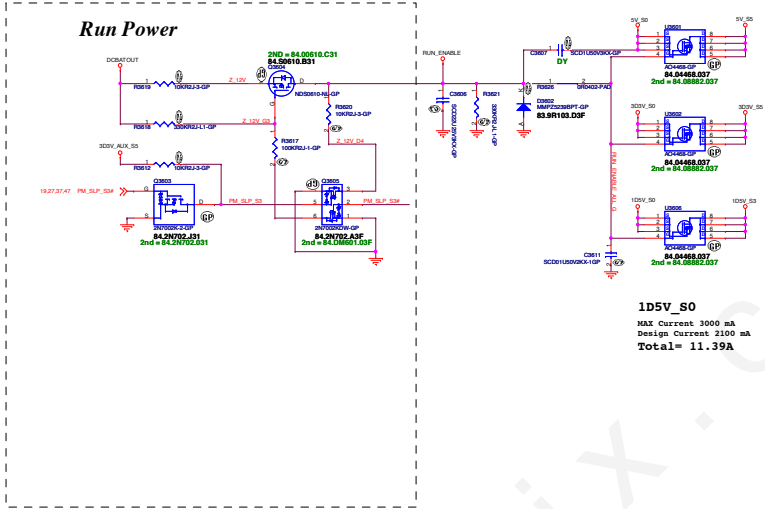
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>USB 3.0 Controller</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 35	of 103

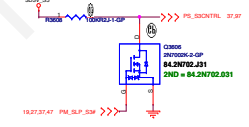
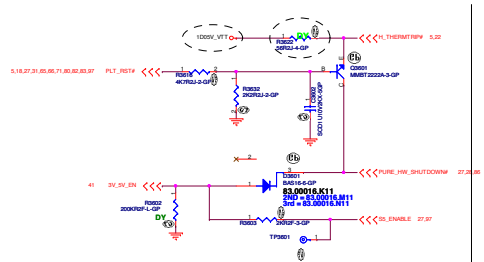
### Power Sequence

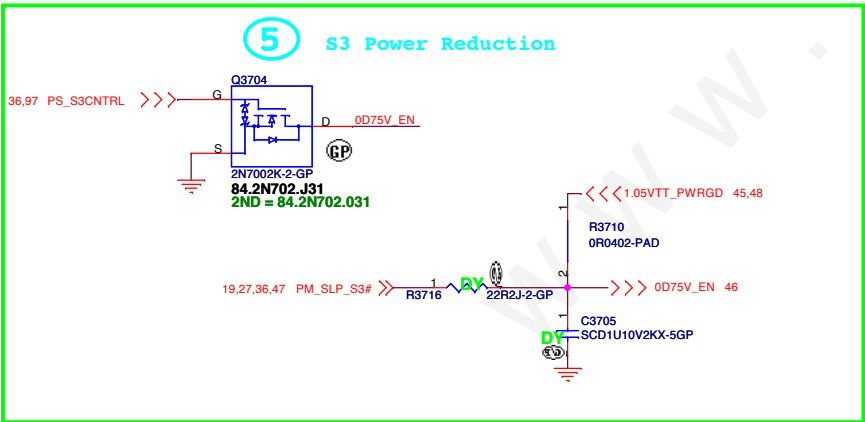
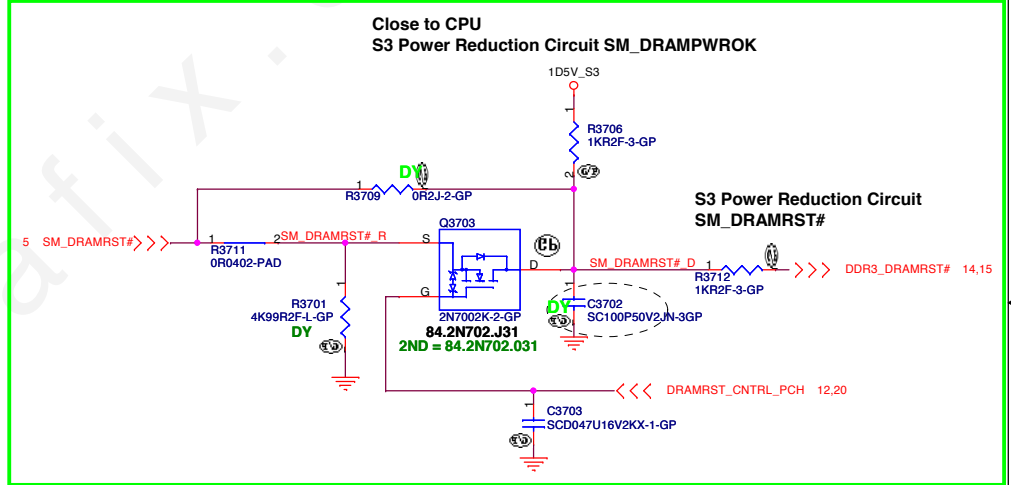
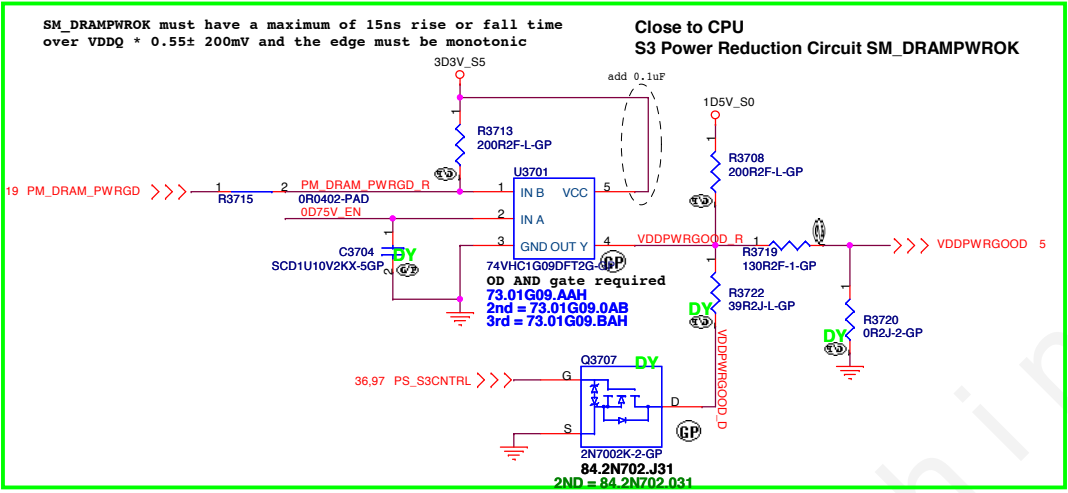
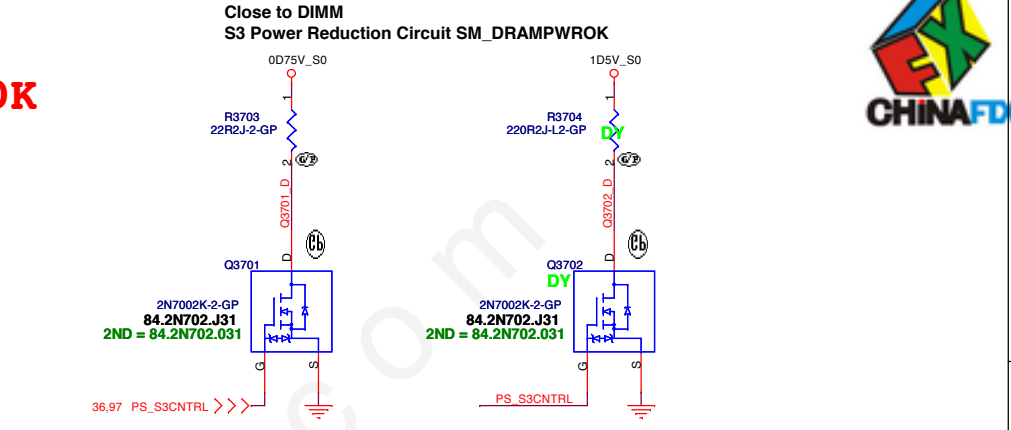
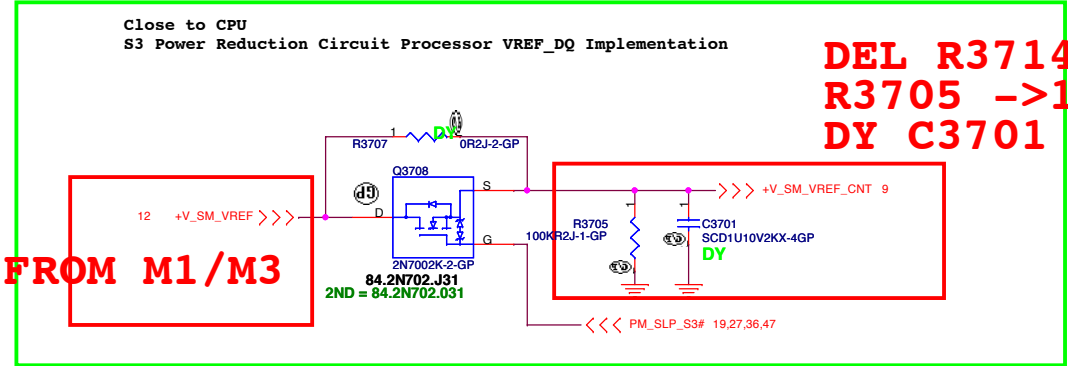


### Run Power

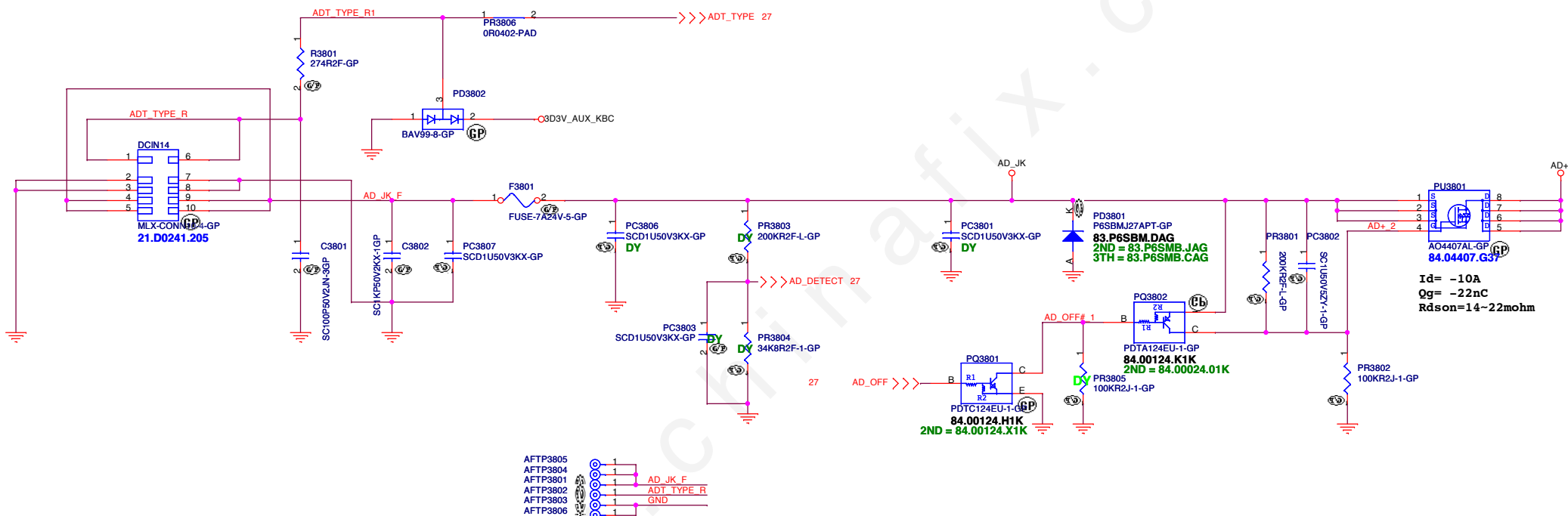


1D5V\_S0  
MAX Current 3000 mA  
Design Current 2100 mA  
Total = 11.39A

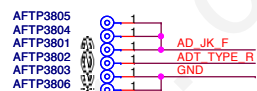




# Adaptor in to generate DCBATOUT

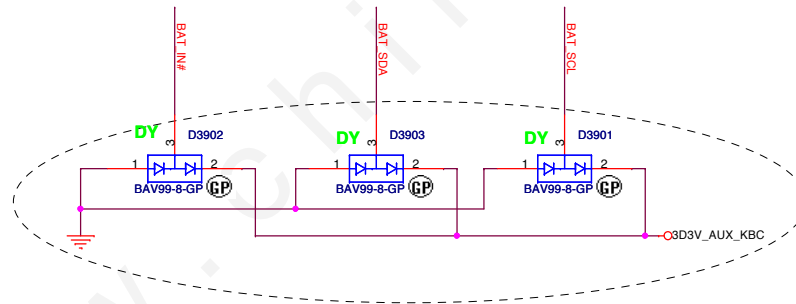
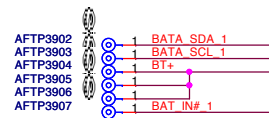
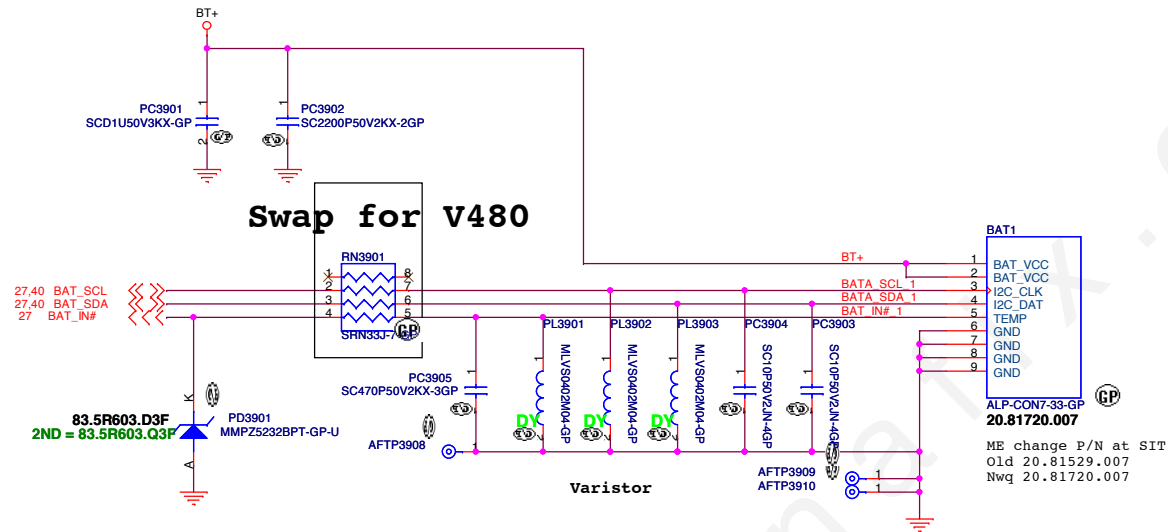


DCIN14 for 14" VB480 & VB485  
 DCIN15 for 15" VB580 & VB585



<Core Design>		
<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Title DCIN_JACK</b>		
Size A3	Document Number <b>LA480</b>	Rev <b>SD</b>
Date: Friday, January 06, 2012	Sheet 38	of 103

## BATTERY CONNECTOR



## DY on LAB stage

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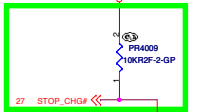
緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>BATT_CONN</b>	
Size	Document Number	LA480	Rev
			<b>SD</b>
Date:	Friday, January 06, 2012	Sheet	39 of 103

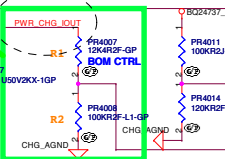
**SSID = Charger**

A8 ( ANNIE/ASTRO)  
PR4007, PR4008

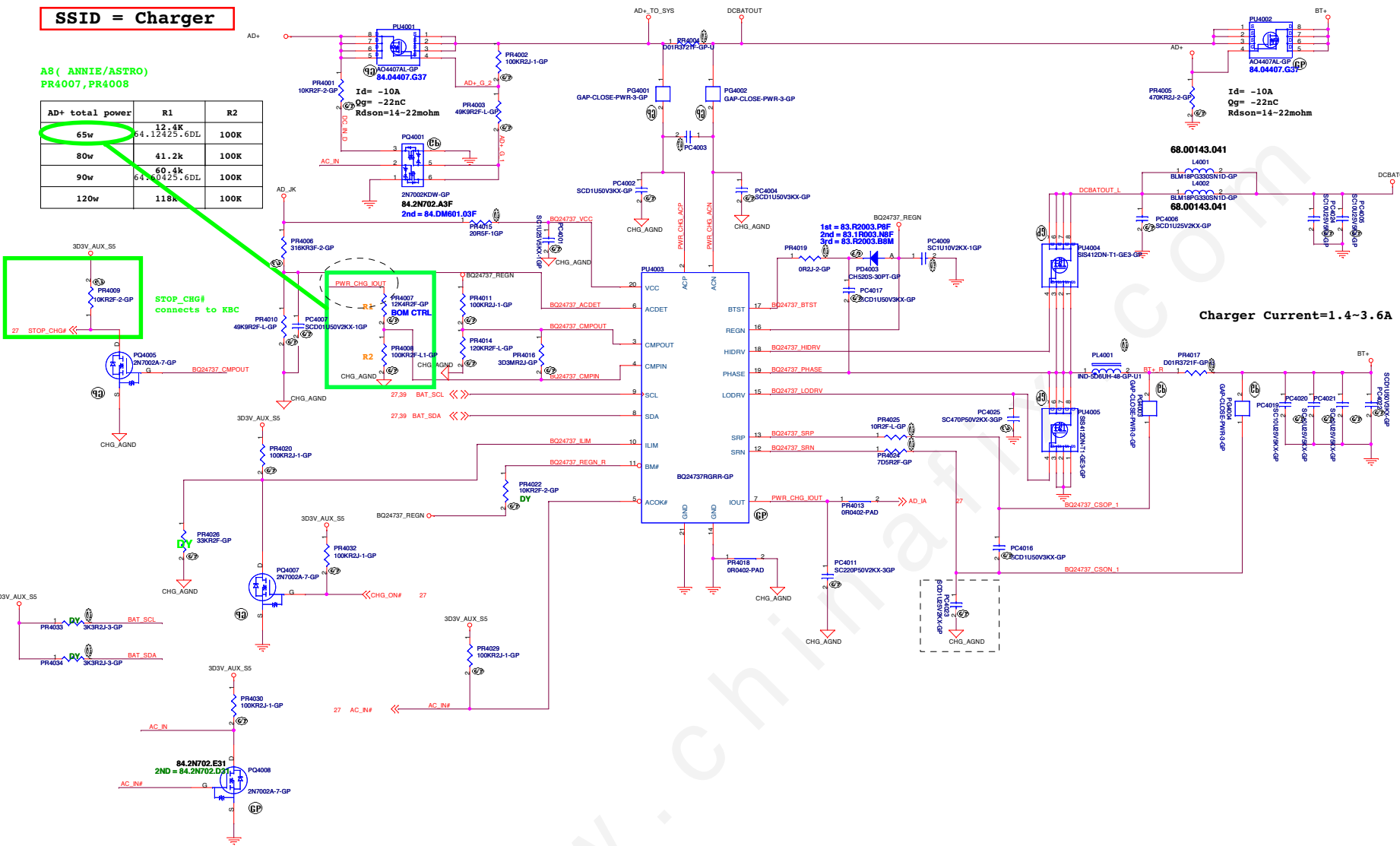
AD+ total power	R1	R2
65w	64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k	100K
120w	118k	100K



STOP\_CHG# connects to KBC



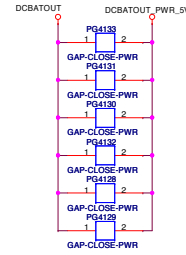
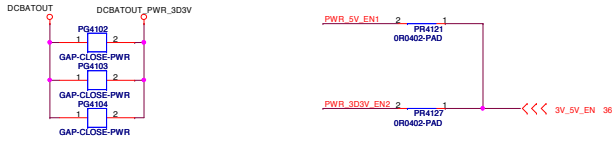
BOM\_CTRL



Charger Current=1.4~3.6A

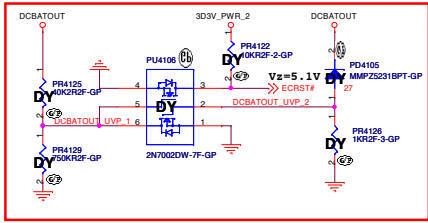
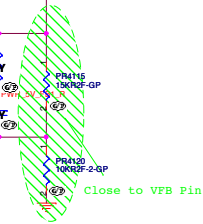
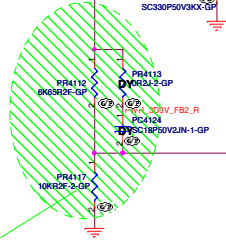
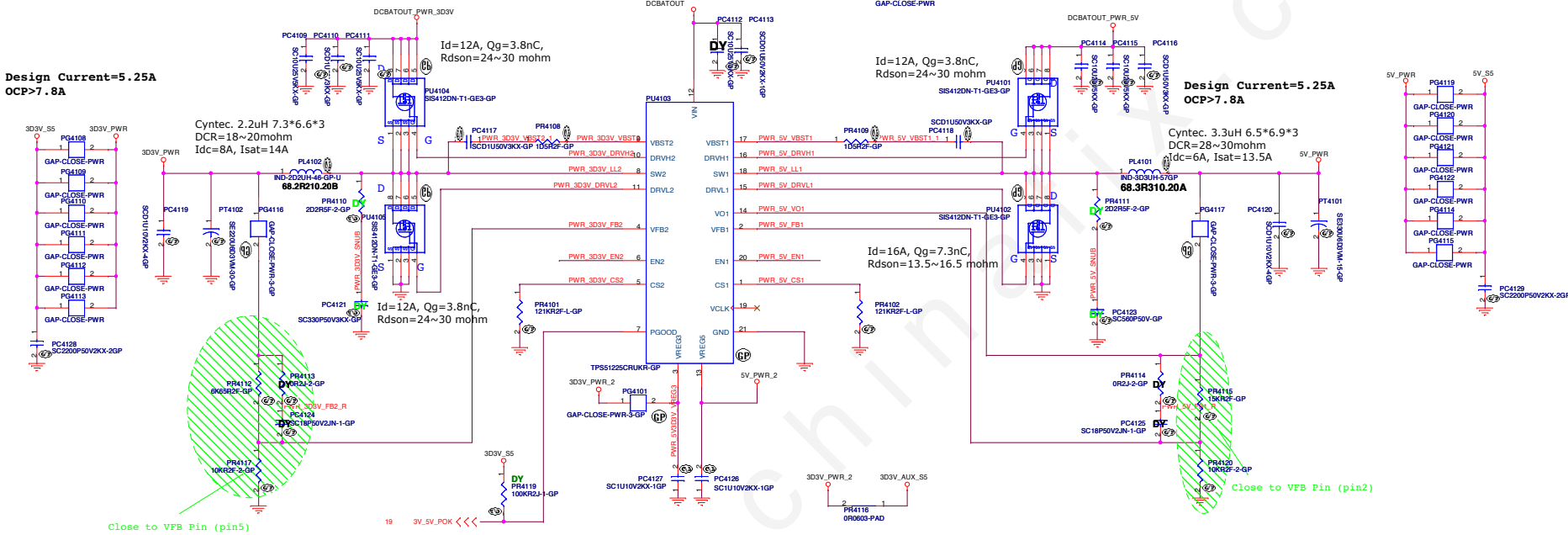


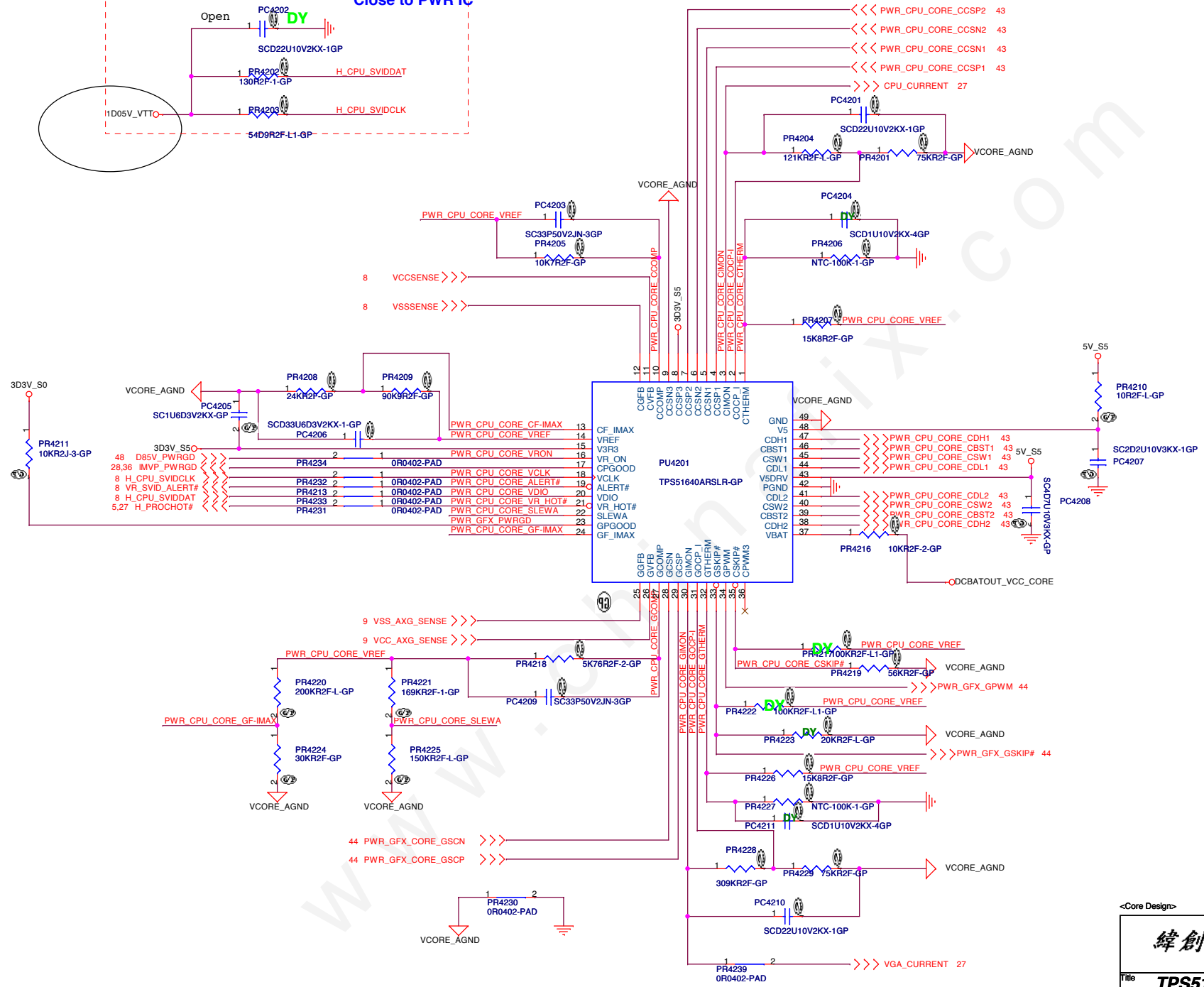
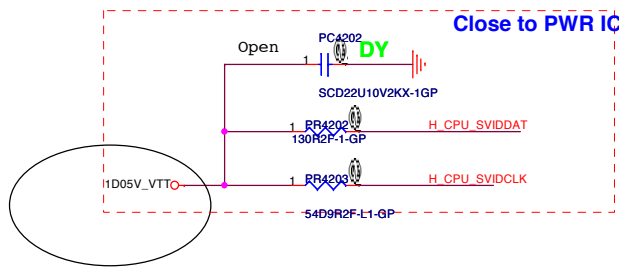




Design Current=5.25A  
OCP>7.8A

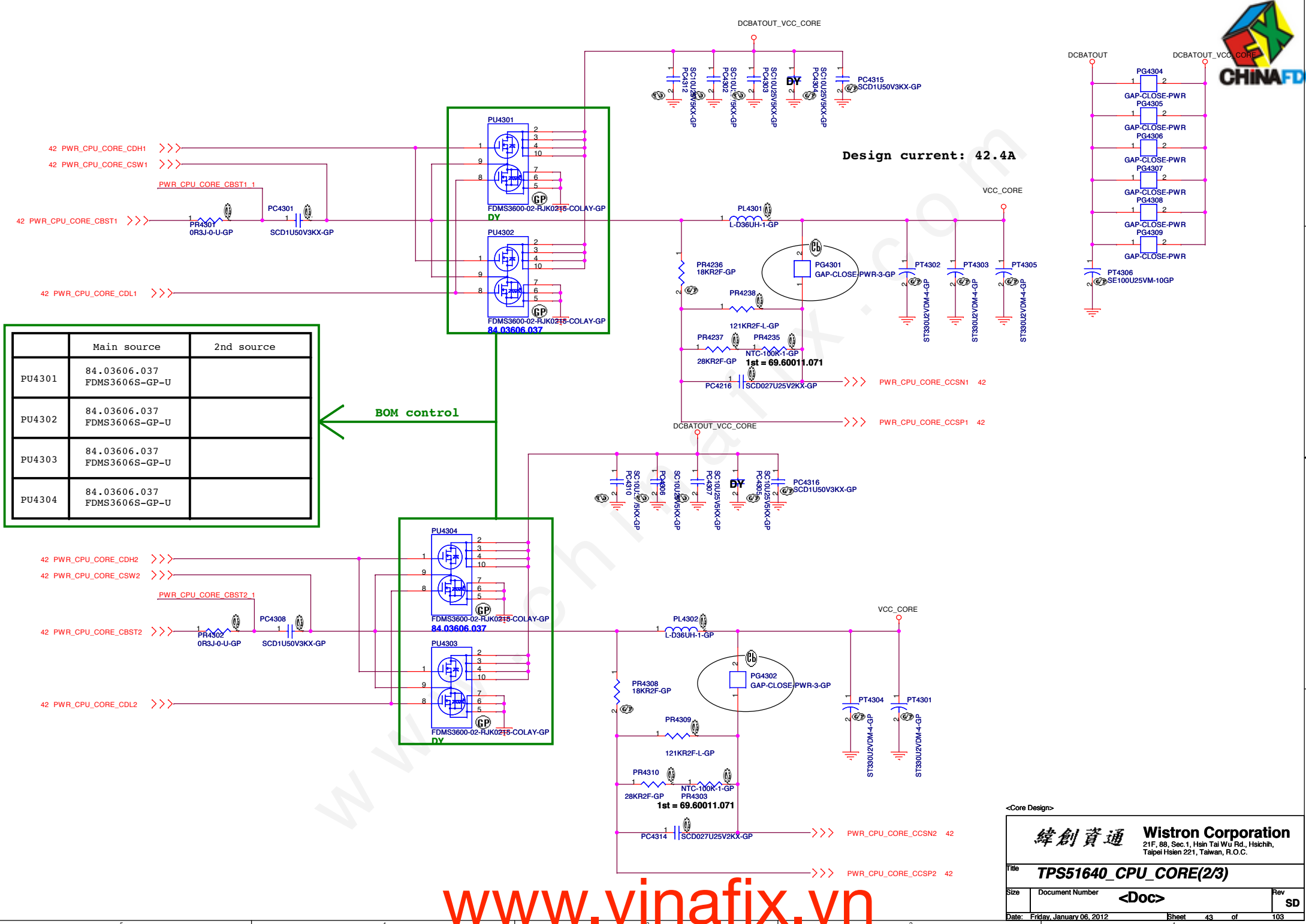
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OCP>7.8A





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<p><b>緯創資通 Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
Title	TPS51640_CPU_CORE(1/3)
Size	Document Number <Doc>
Date	Friday, January 06, 2012
Rev	SD
Sheet	42 of 103



Design current: 42.4A

	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

BOM control

<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

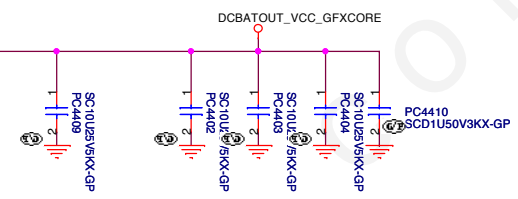
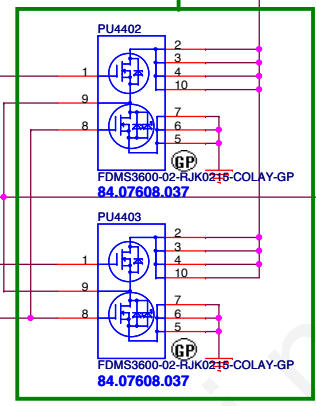
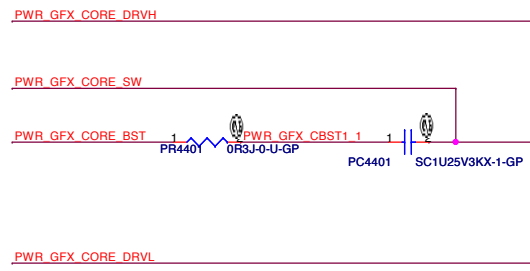
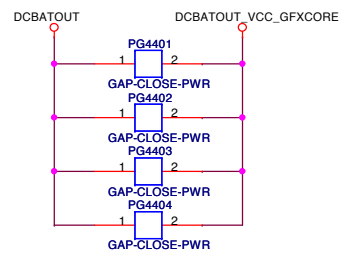
Title: **TPS51640\_CPU\_CORE(2/3)**

Size: Document Number **<Doc>** Rev: **SD**

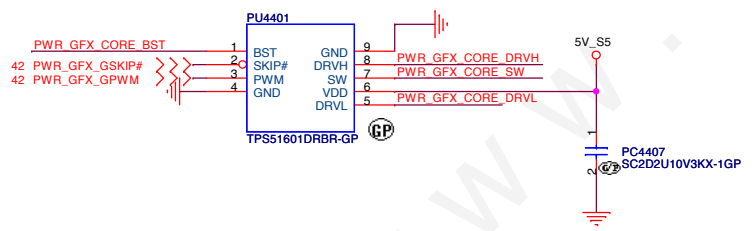
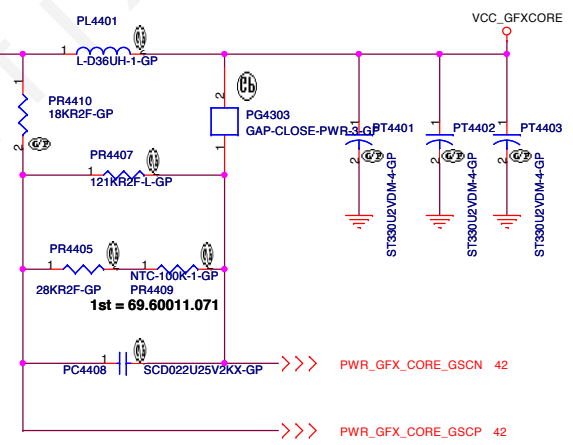
Date: Friday, January 06, 2012 Sheet 43 of 103

	Main source	2nd source
PU4402	84.07608.037 FDMS7608S-GP	
PU4403	84.07608.037 FDMS7608S-GP	

BOM control

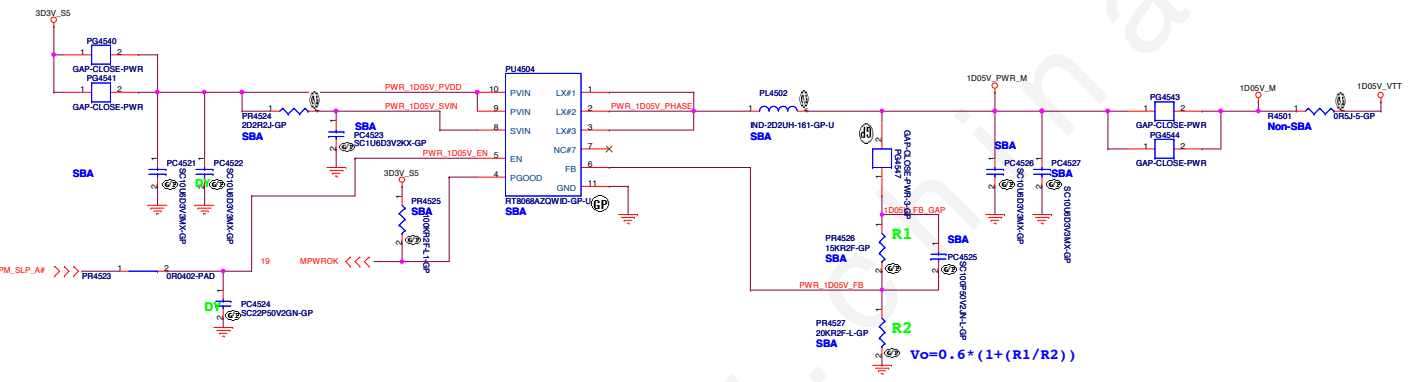
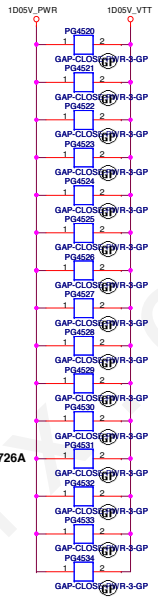
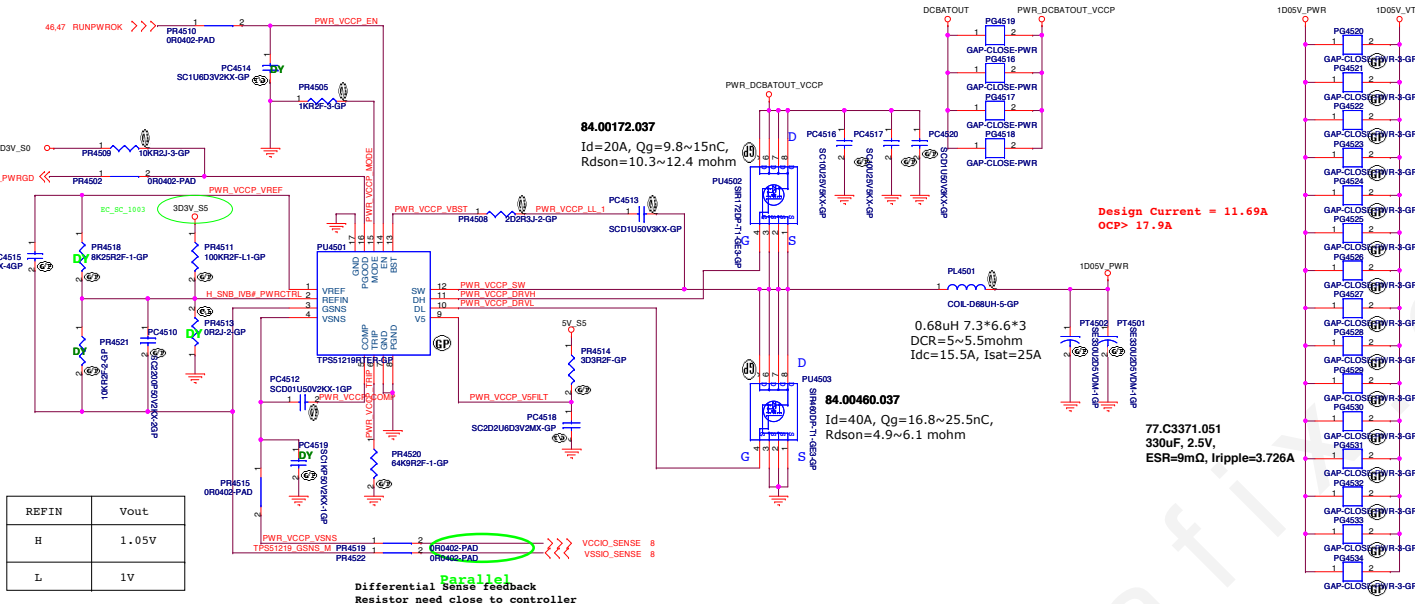


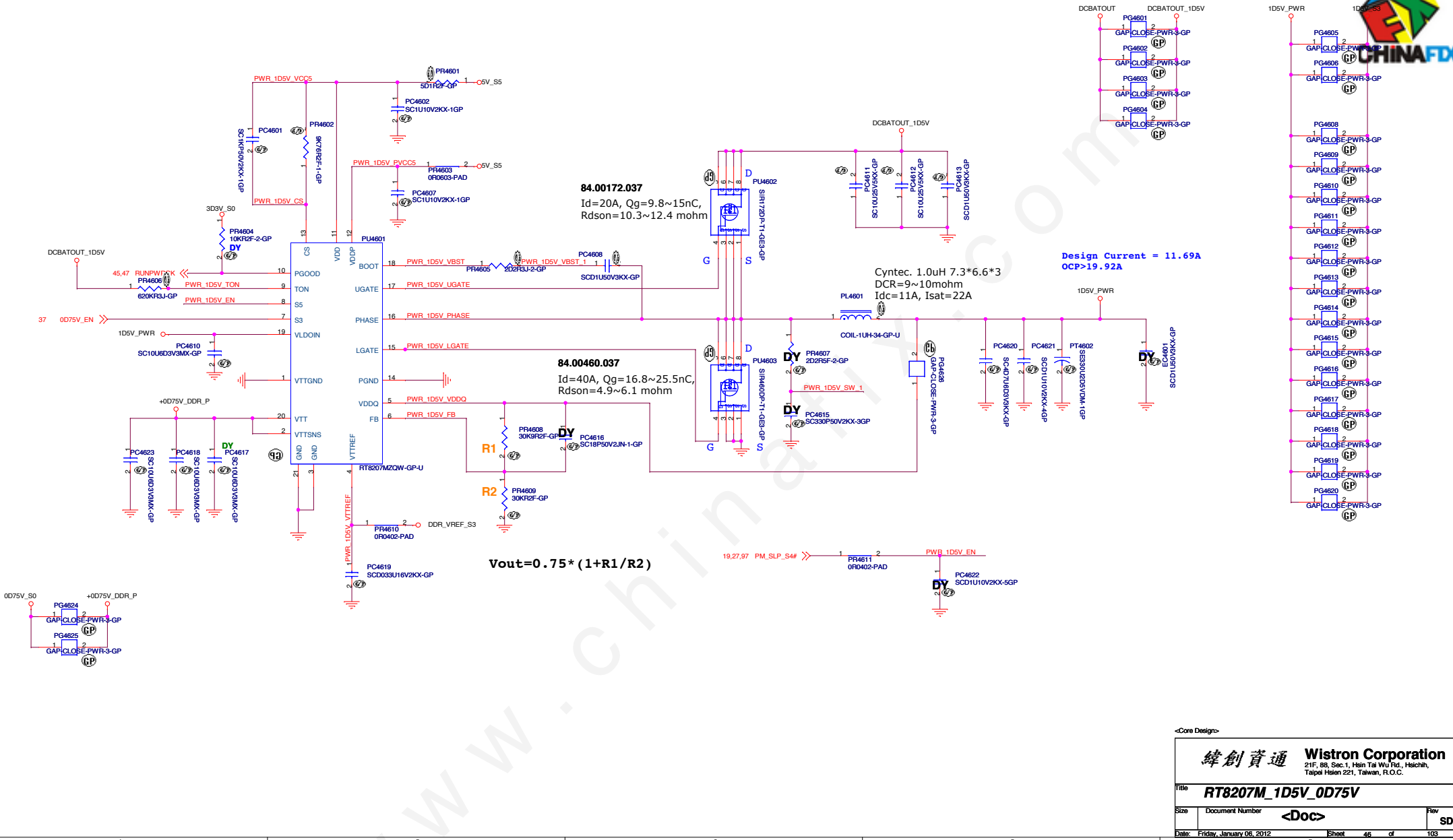
Design current: 22A



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<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<b>TPS51640_CPU_CORE(3/3)</b>
Size	Document Number <b>&lt;Doc&gt;</b> Rev <b>SD</b>
Date	Friday, January 06, 2012 Sheet 44 of 103

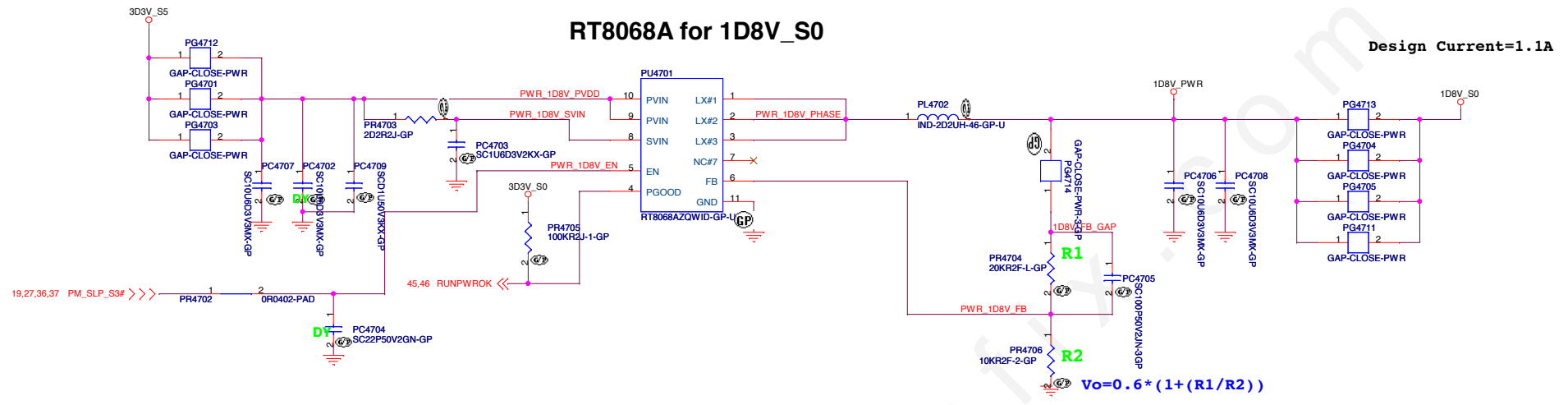




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緯創資通		Wistron Corporation	
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Title	RT8207M_1D5V_0D75V		
Size	Document Number	<Doc>	Rev
			SD
Date:	Friday, January 06, 2012	Sheet	46 of 103

**SSID = PWR.Plane.Regulator\_1p8v**

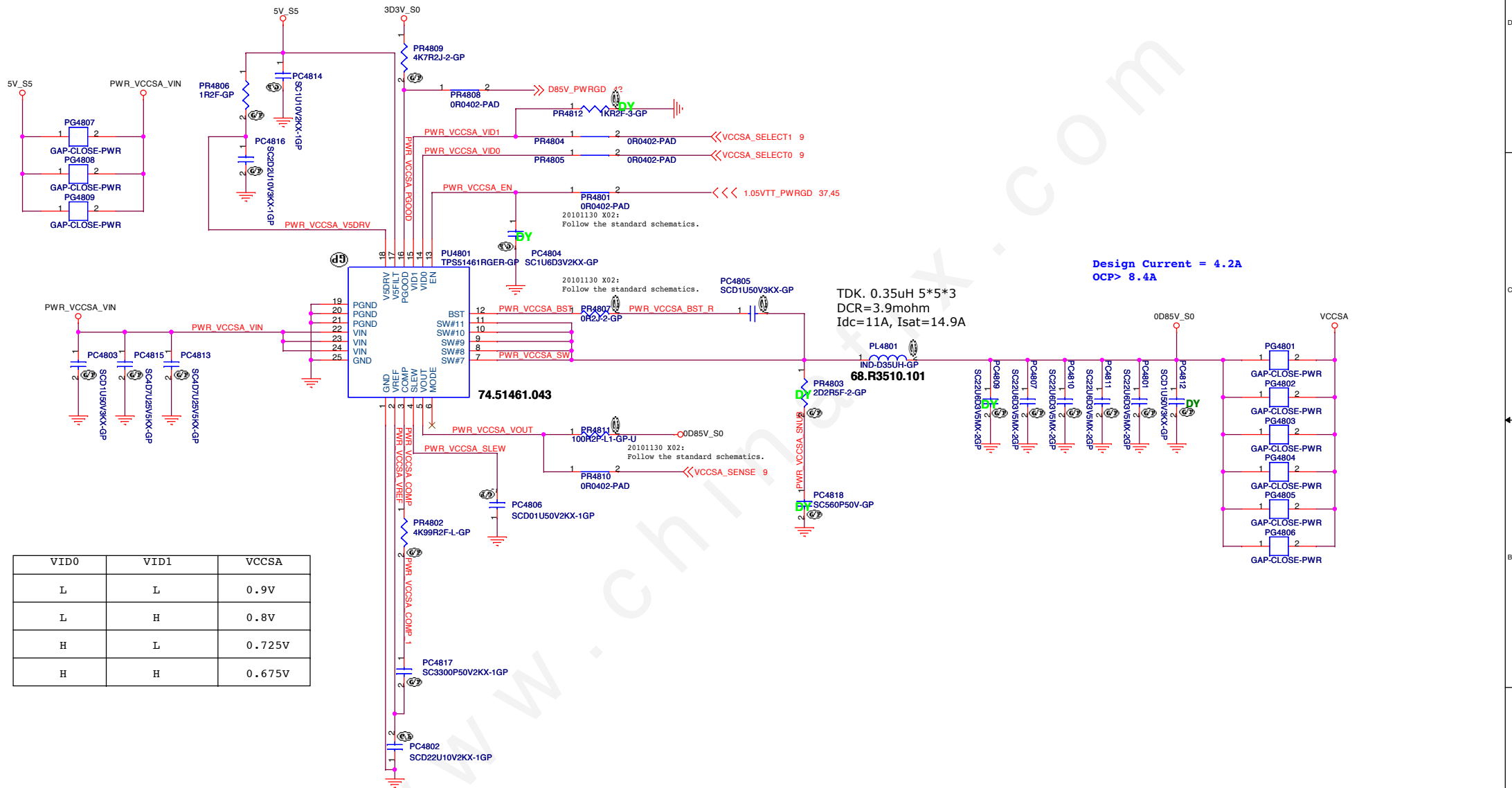


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<Core Design>

<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title PWM_1D8V_RT8015B</b>	
<b>Size</b> Document Number	<b>Rev</b> SD
Date: Friday, January 06, 2012	Sheet 47 of 103

# TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

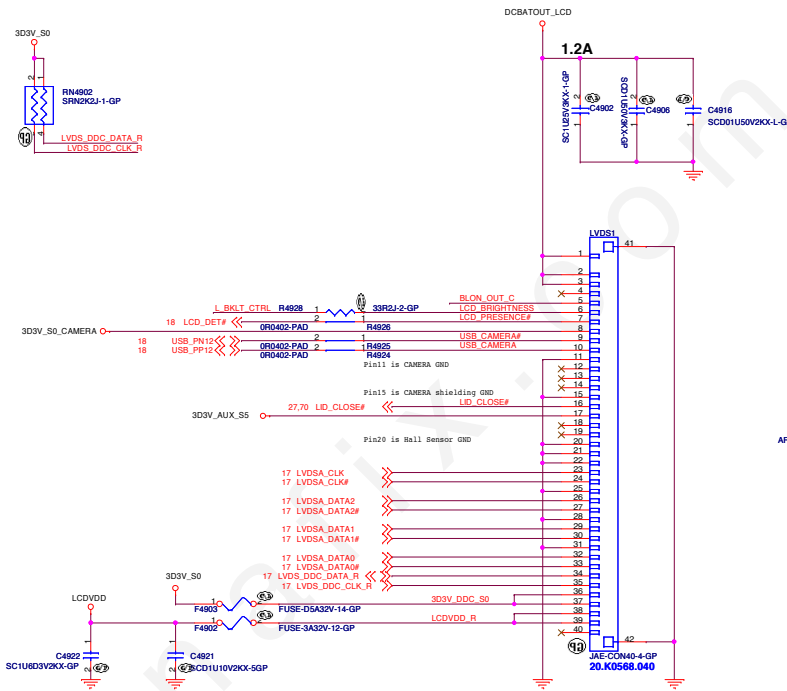
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Size: Document Number **<Doc>** Rev: **SD**

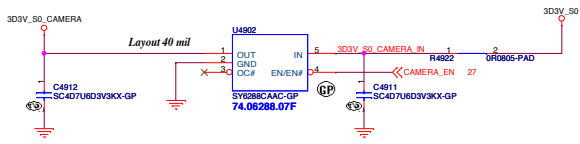
Date: Friday, January 06, 2012 Sheet 48 of 103



LCD / Inverter Connector

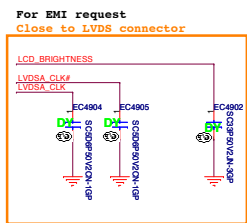
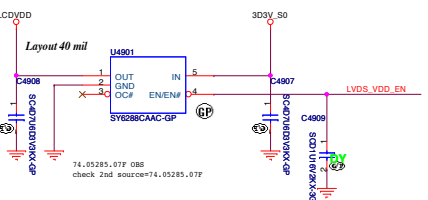
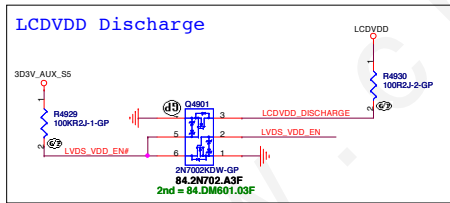
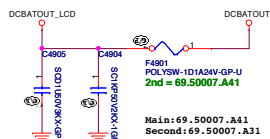


CAMERA POWER

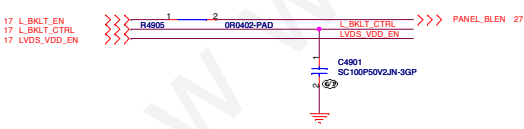


SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

LCD POWER



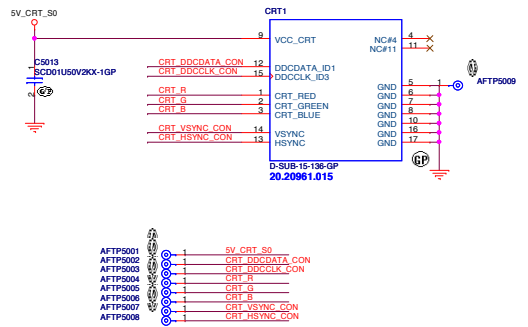
Panel BL brightness/Power En/BL En



<Core Design>

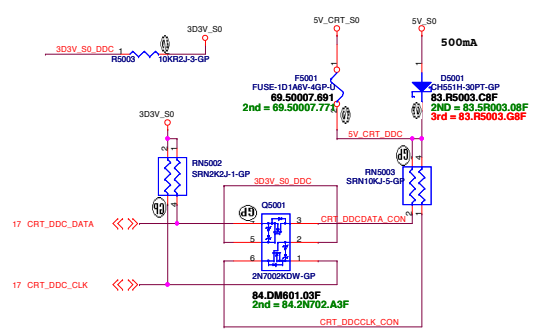
<p>緯創資通 Wistron Corporation</p> <p>21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
Rev	<p><b>LCD Connector</b></p>
Size	Document Number
A2	<b>LA480</b>
Date	Friday, 18 January 2012
Sheet	49 of 103

### CRT connector

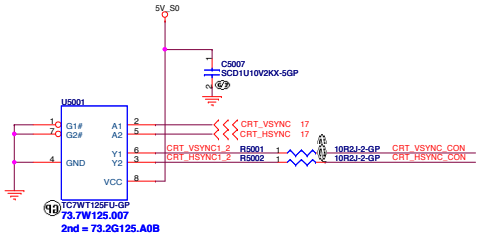


### CRT DDCDATA & DDCCLK level shift

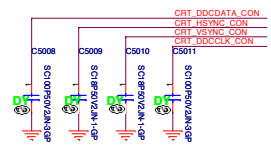
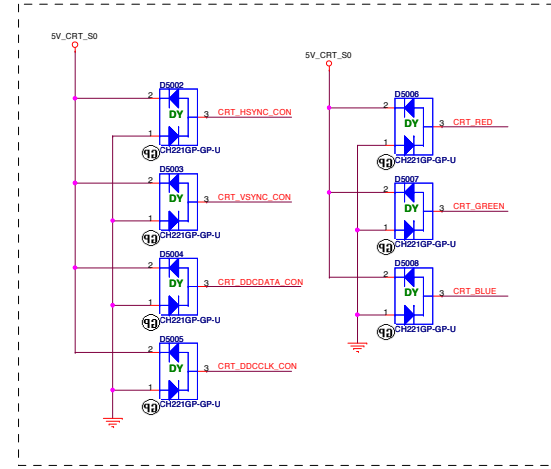
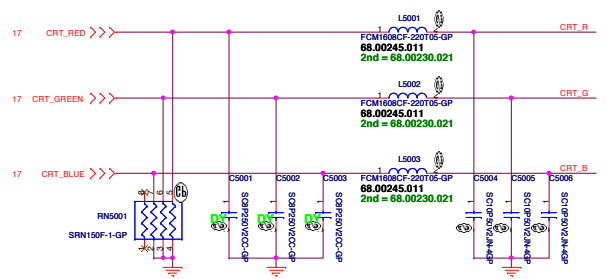
Pull High 5V Design on CRT Board



### CRT Hsync & Vsync level shift

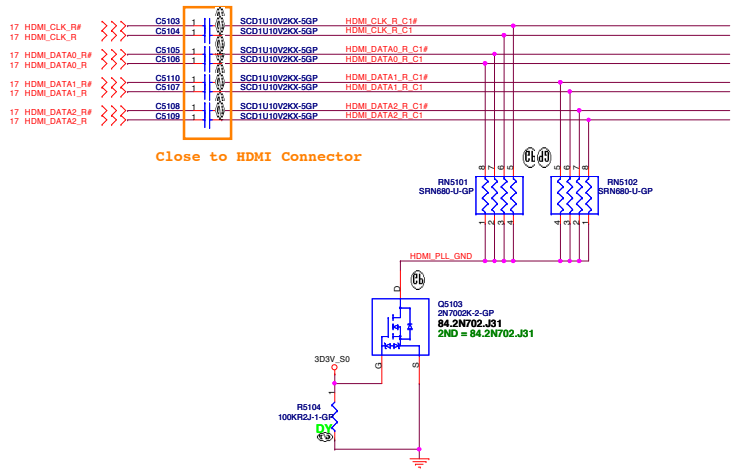


### CRT RGB

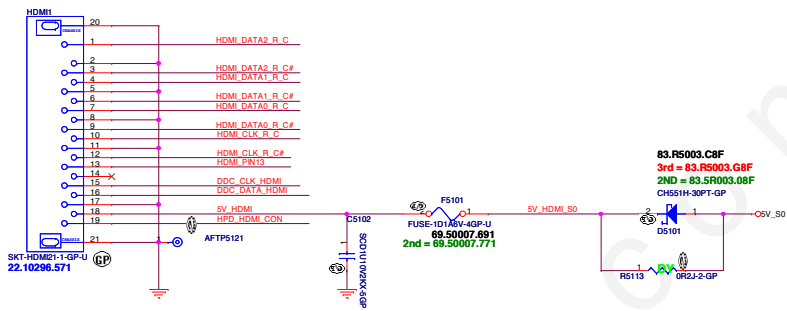


### HDMI Passive Level Shifter

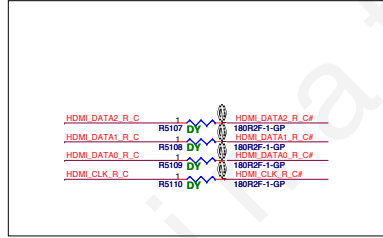
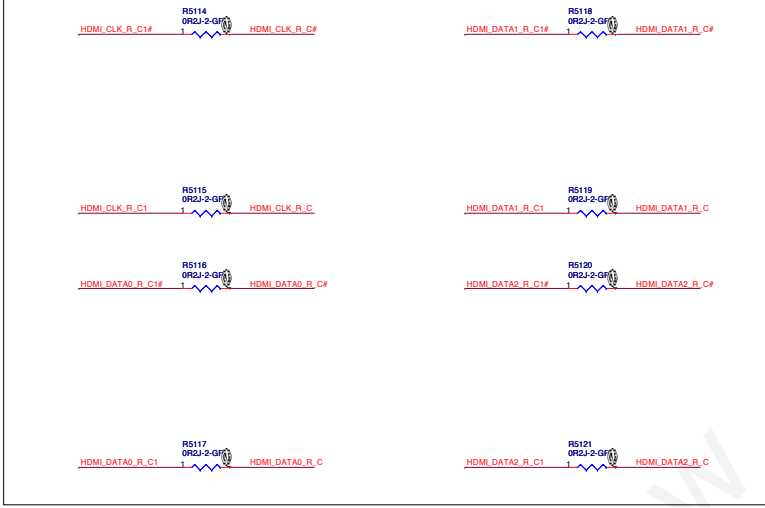
Close to HDMI Connector



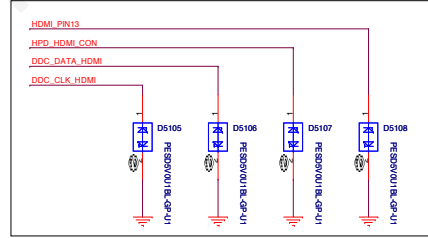
### HDMI CONNECTOR



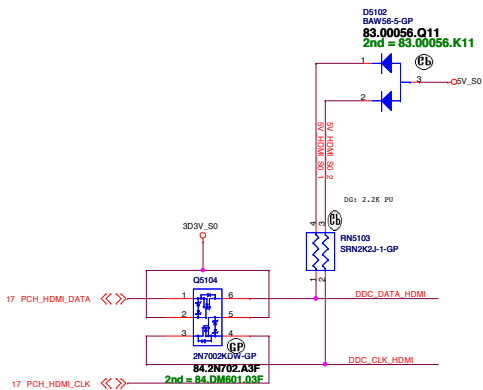
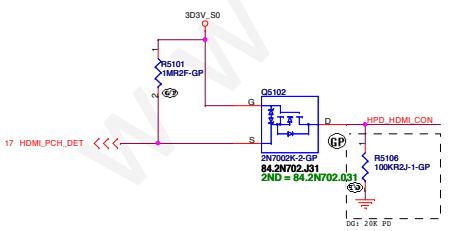
### EMI's request



### ESD Request



### HDMI DDC Passive Level Shifter



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www.vinafix.vn

<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>eDP</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 52	of 103

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<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>S-VIDEO</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date:	Friday, January 06, 2012	Sheet 53	of 103



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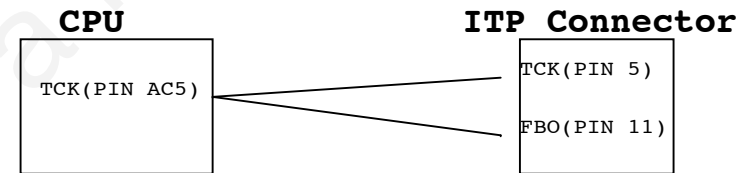
<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date:	Friday, January 06, 2012	Sheet	54 of 103

**SSID = User.Interface**

# ITP Connector

H\_CPURST# use pull-up Resistor close  
 ITP connector 500 mil ( max ),  
 others place near CPU side.



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<Core Design>

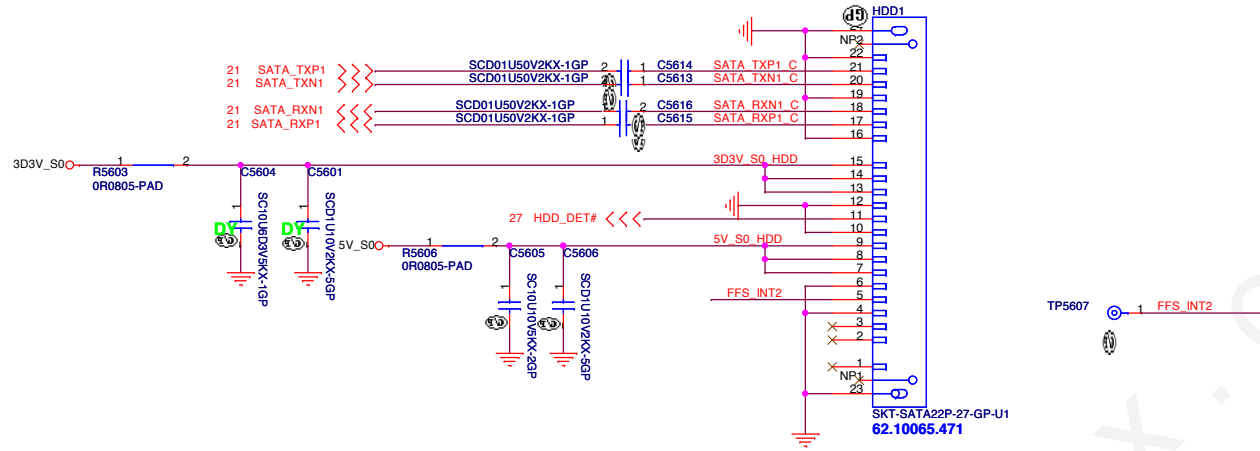
**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title **ITP**

Size A4	Document Number <b>LA480</b>	Rev <b>SD</b>
------------	---------------------------------	------------------

Date: Friday, January 06, 2012 Sheet 55 of 103

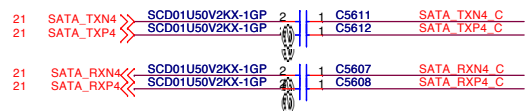
# SATA HDD Connector



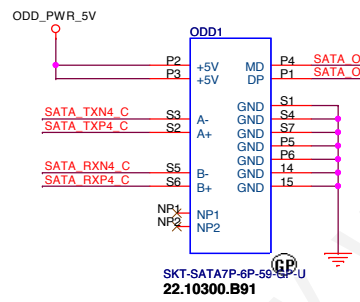
# ODD Connector

SATA\_RX- and SATA\_RX+ Trace  
Length match within 20 mil

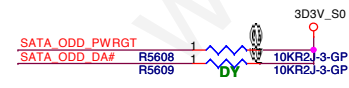
Mars:  
Exchange ODD and ESATA differential pair each other.



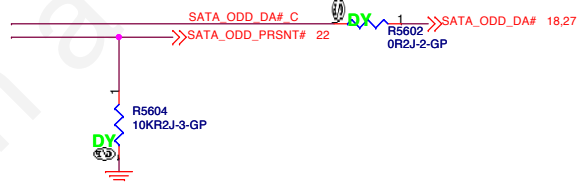
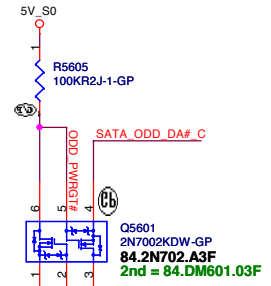
- 74.02069.079 TI TPS2069DGNR MSOP 8P
- 74.07534.D79 UPI UP7534PRA8-15 MSOP 8P
- 74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
- 74.07534.A79 UPI UP7534ARA8-15 MSOP8P



When the drive is powered on, the FET to the MD/DA pin drive is OFF.  
When the drive is powered off, the FET to the MD/DA pin is ON

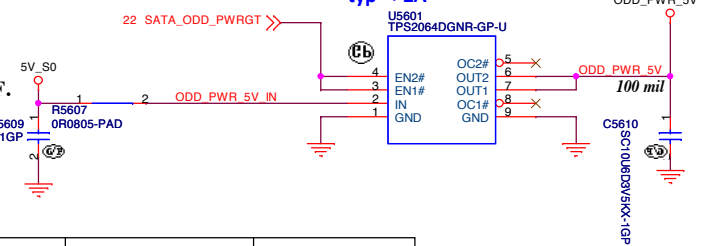


SUPPORT ZERO SATA ODD



## SATA Zero Power ODD

Current limit  
Active High  
typ => 2A



TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active

<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

**HDD/ODD**  
 Title  
 Size A3 Document Number LA480 Rev SD  
 Date: Friday, January 06, 2012 Sheet 56 of 103





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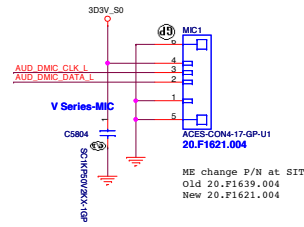
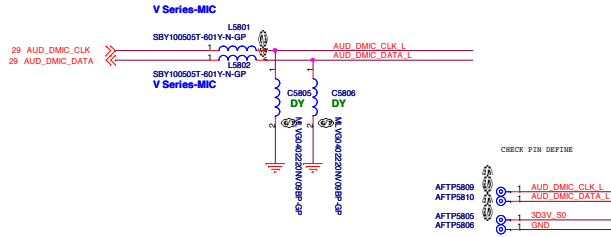
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www.vinafix.vn

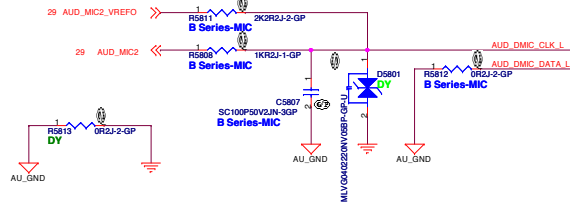
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>E-SATA+USB</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date:	Friday, January 06, 2012	Sheet	57 of 103

## Int. Digital MIC for V series



## Int. Mono Analog MIC for B series



## INTERNAL STEREO SPEAKERS

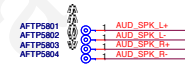
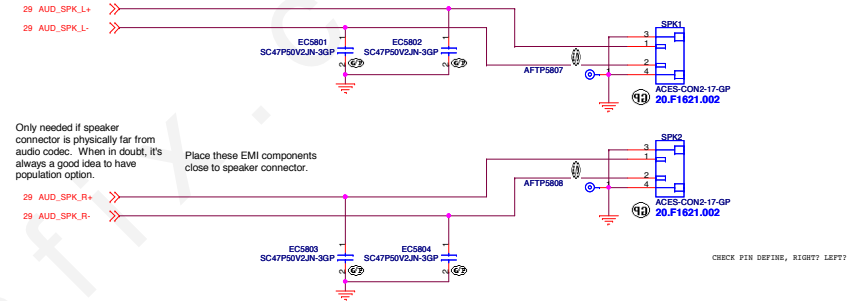


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

<Core Design>

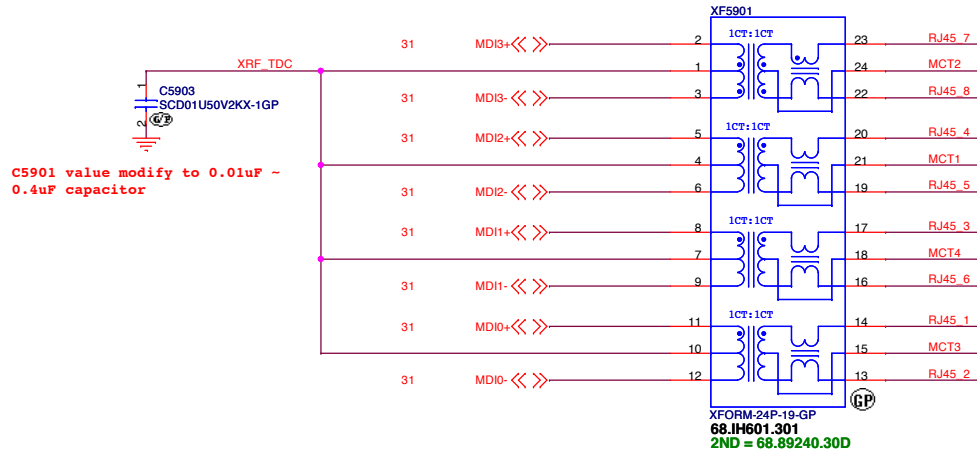
FOR CO-LAY

# GIGA Lan Transformer

TVS

83.00005.BAE

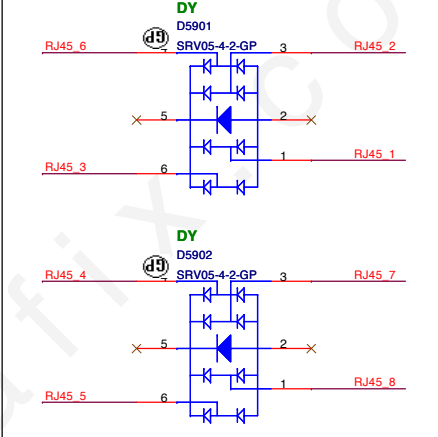
DIODE ARR SRV05-4.TCT SOT23-6L



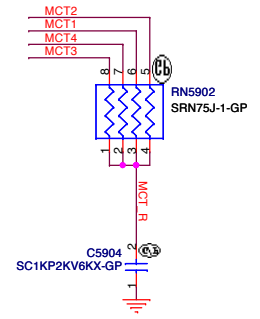
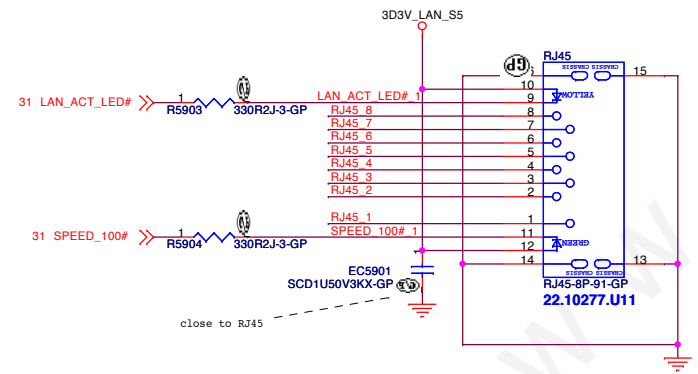
C5901 value modify to 0.01uF ~ 0.4uF capacitor

- 1st  
68.IH601.301(Taimag) for 1000  
68.HH035.301(Taimag) for 10/100
- 2nd  
68.2413S.30A(Lankom) for 1000  
68.H6441.301(Lankom) for 10/100

## Swap for V480

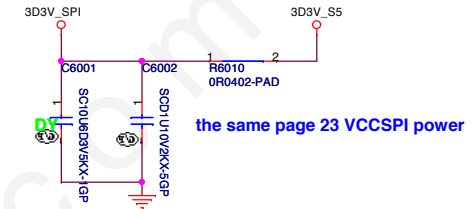
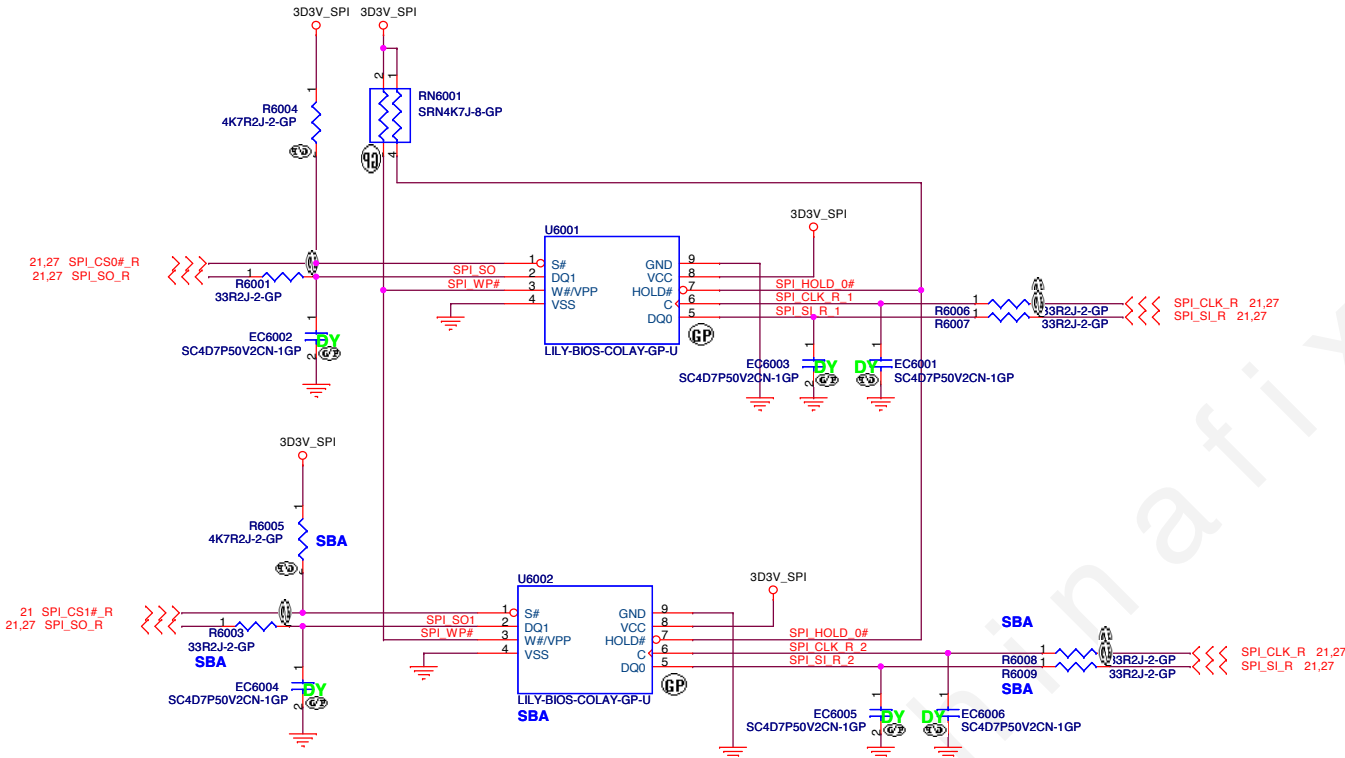


## LAN Connector



**SSID = Flash.ROM**

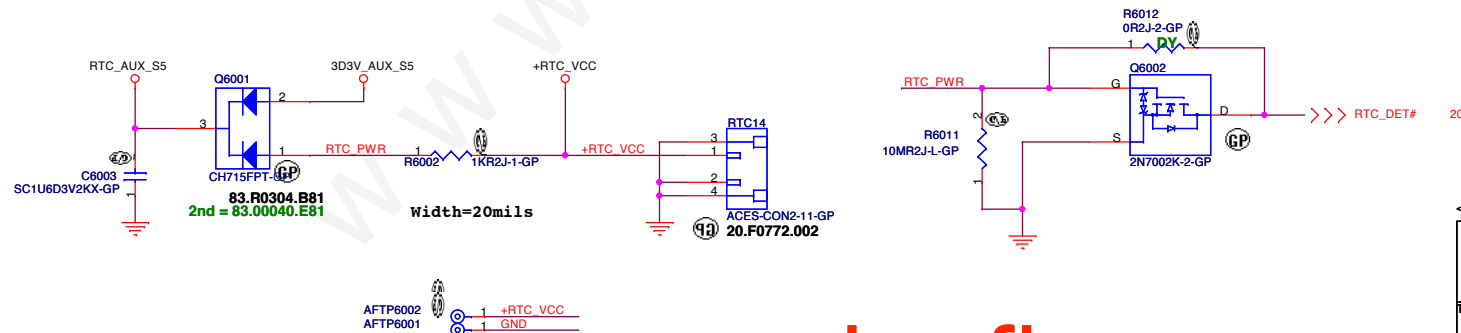
**SPI FLASH ROM (8M byte) for PCH**



the same page 23 VCCSPI power

4MB			
SO8	Marconix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marconix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSON	Marconix	MX25L12836EZNI-10G	72.25128.X01
	Marconix	MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
Numonyx	N25Q128A13EF840	72.25128.B03	

**SSID = RBATT**

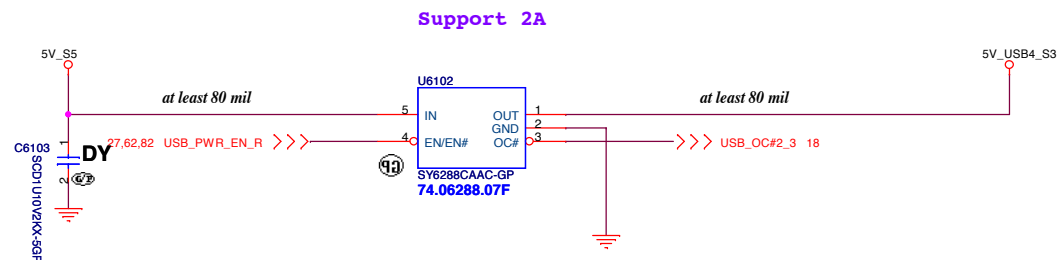


<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 102, Taiwan, R.O.C.

Title		<b>Flash/RTC</b>	
Size A3	Document Number	Rev SD	
Date: Friday, January 06, 2012		Sheet 60 of 103	

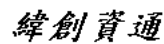
# USB Board CONN.



Place U6102 close to USBCN1

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<Core Design>

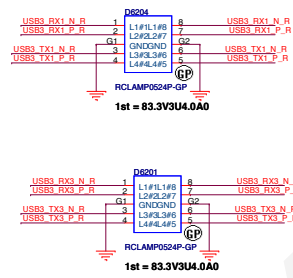
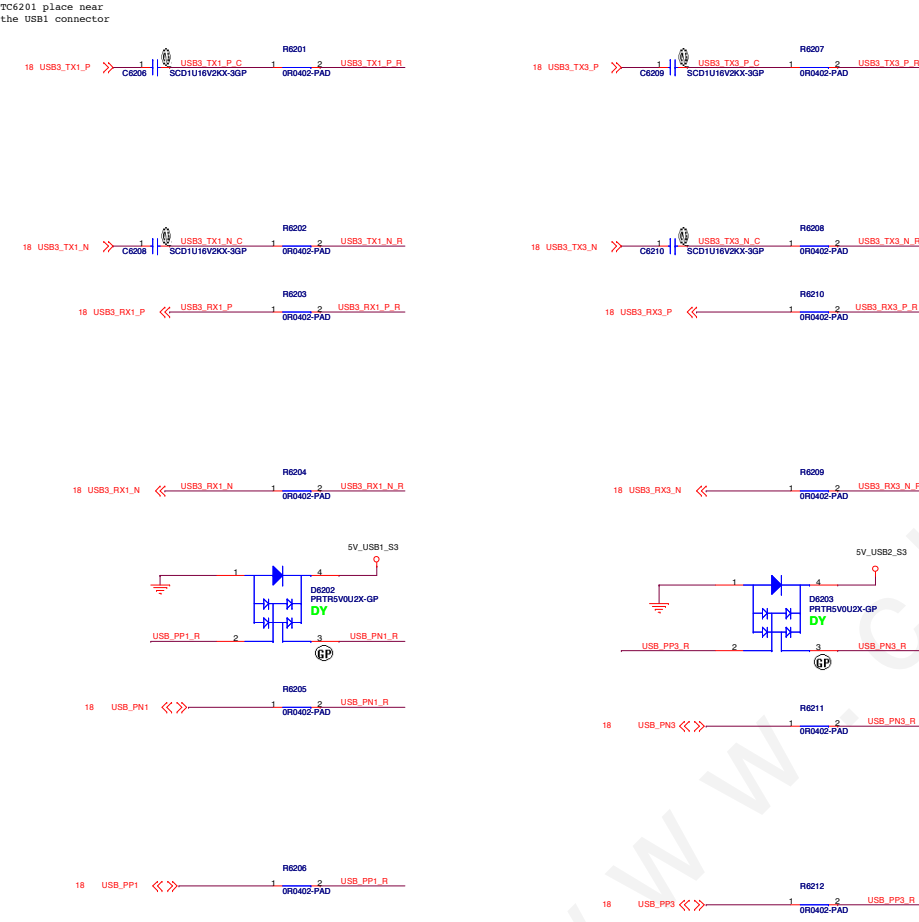
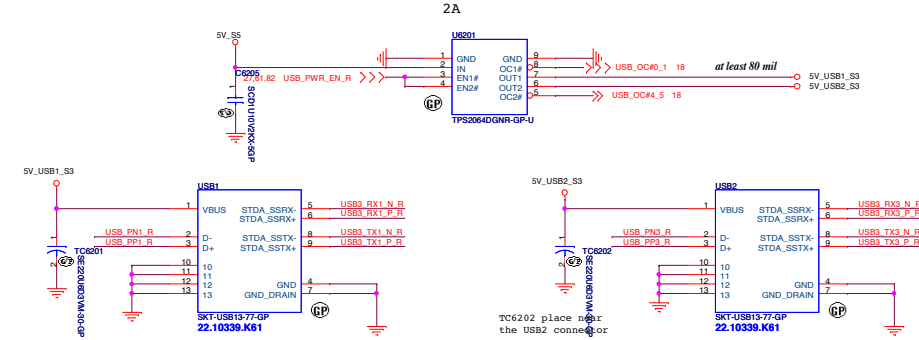
 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>USB Connector</b>	
Size A3	Document Number <b>LA480</b>
Date: Friday, January 06, 2012	Rev <b>SD</b>
Sheet 61 of 103	

USB3.0 Port1

USB3.0 Port2

USB3.0 Port3

USB3.0 Port4

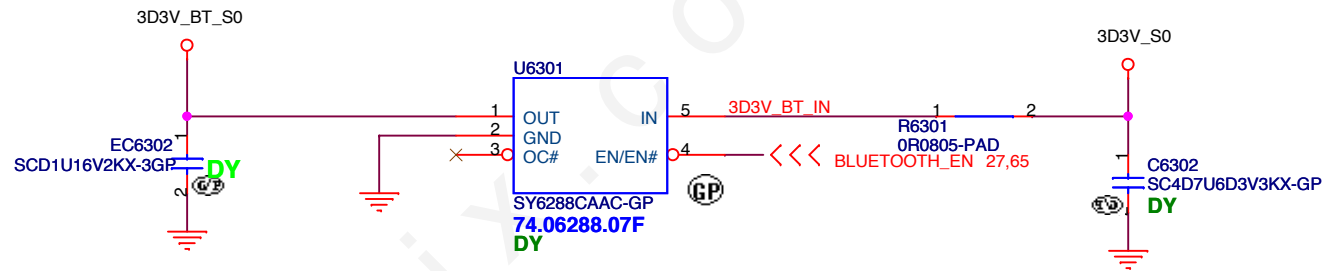


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-Core Design-		
<b>緯創資通 Wistron Corporation</b>		
21F, 8F, 5th Fl., Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.		
<b>USB 3.0 Port*2</b>		
Title		
Size A2	Document Number	Rev
	<b>LA480</b>	<b>SD</b>
Date: Friday, January 06, 2012	Sheet 62 of 100	

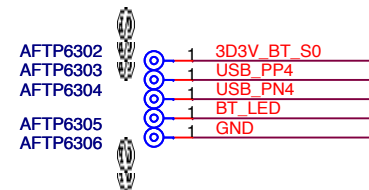
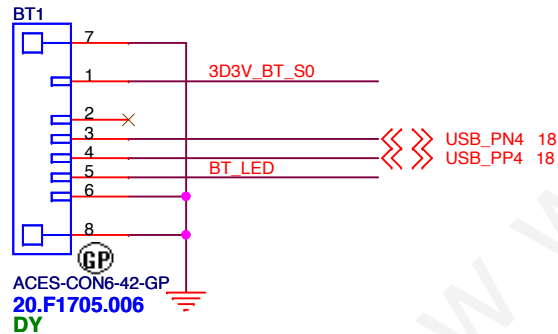
**SSID = User.Interface**

**Bluetooth conn.**



BT Module pin definition is same as LA470

SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active



<Core Design>

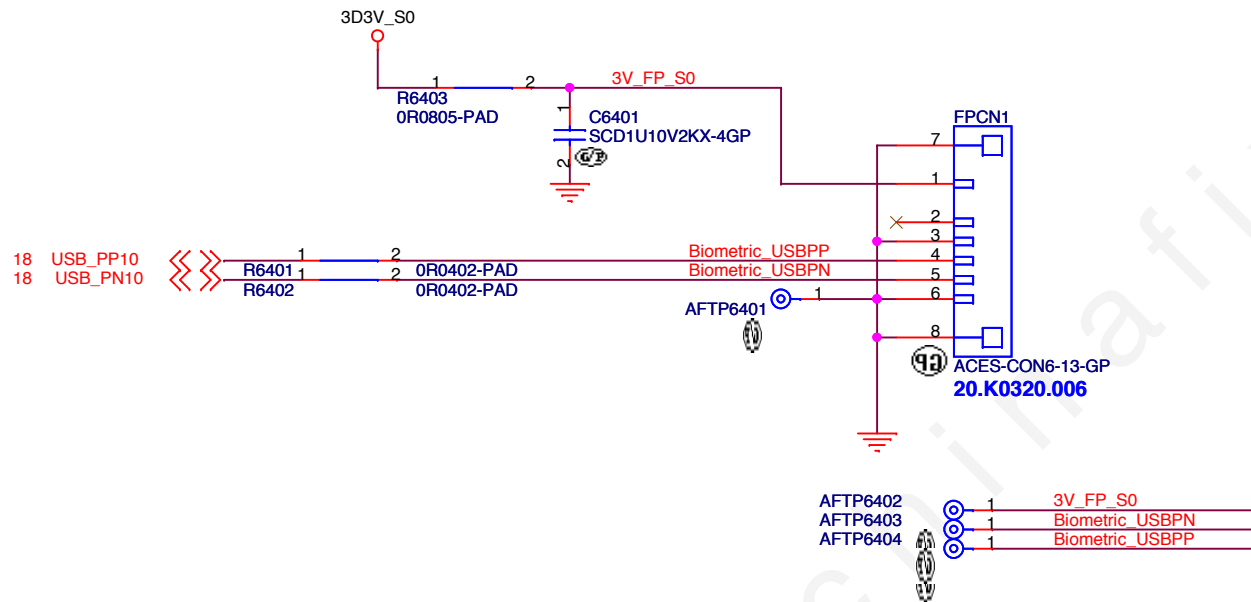
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Bluetooth**

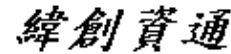
Size: A4 | Document Number: **LA480** | Rev: **SD**

Date: Friday, January 06, 2012 | Sheet: 63 of 103

# Finger Printer Connector



<Core Design>

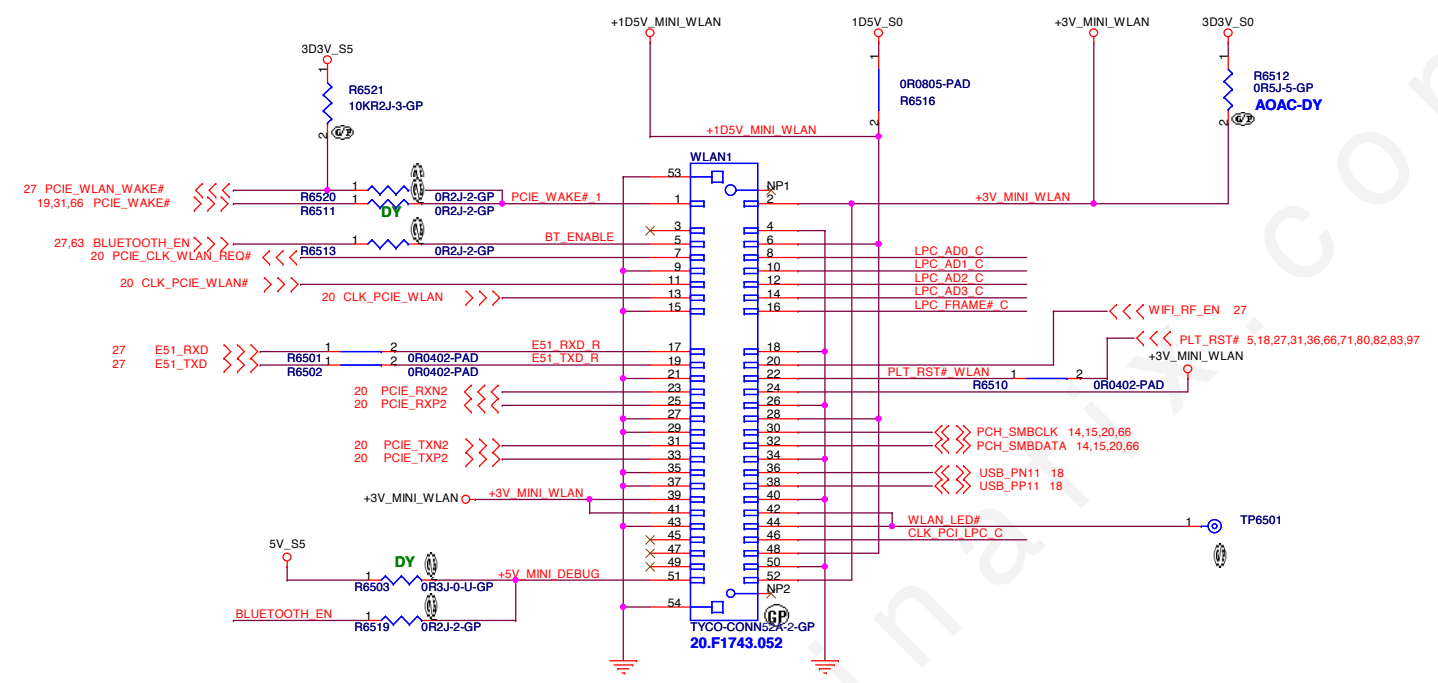
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Finger Printer Connector</b>		
Size A4	Document Number <b>LA480</b>	Rev <b>SD</b>
Date: Friday, January 06, 2012		Sheet 64 of 103



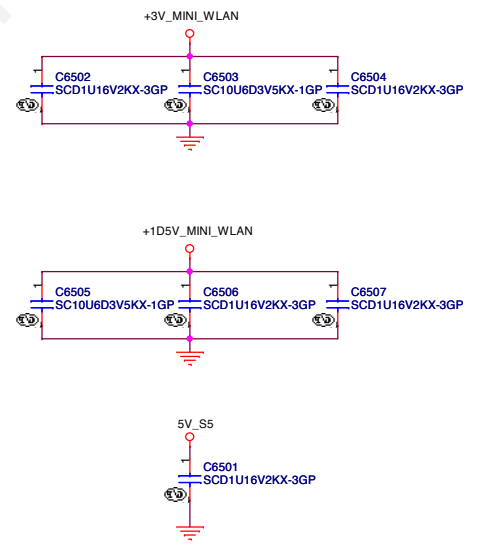
**SSID = Wireless**



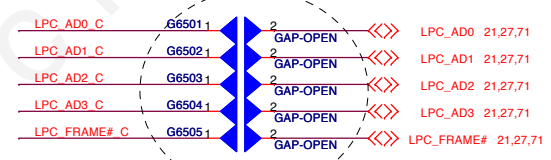
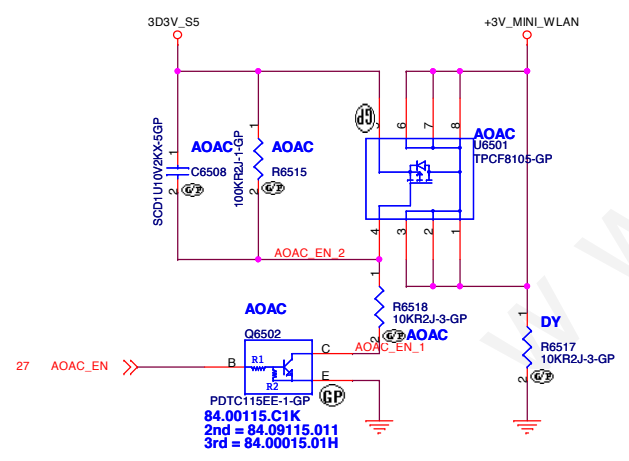
# Mini Card Connector(802.11a/b/g/n)



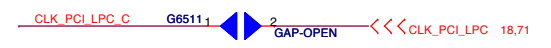
Place near MINI Card CONN



Reserve for AOAC



**G6506~G6511  
placement close close WLAN1  
in bottom side**



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

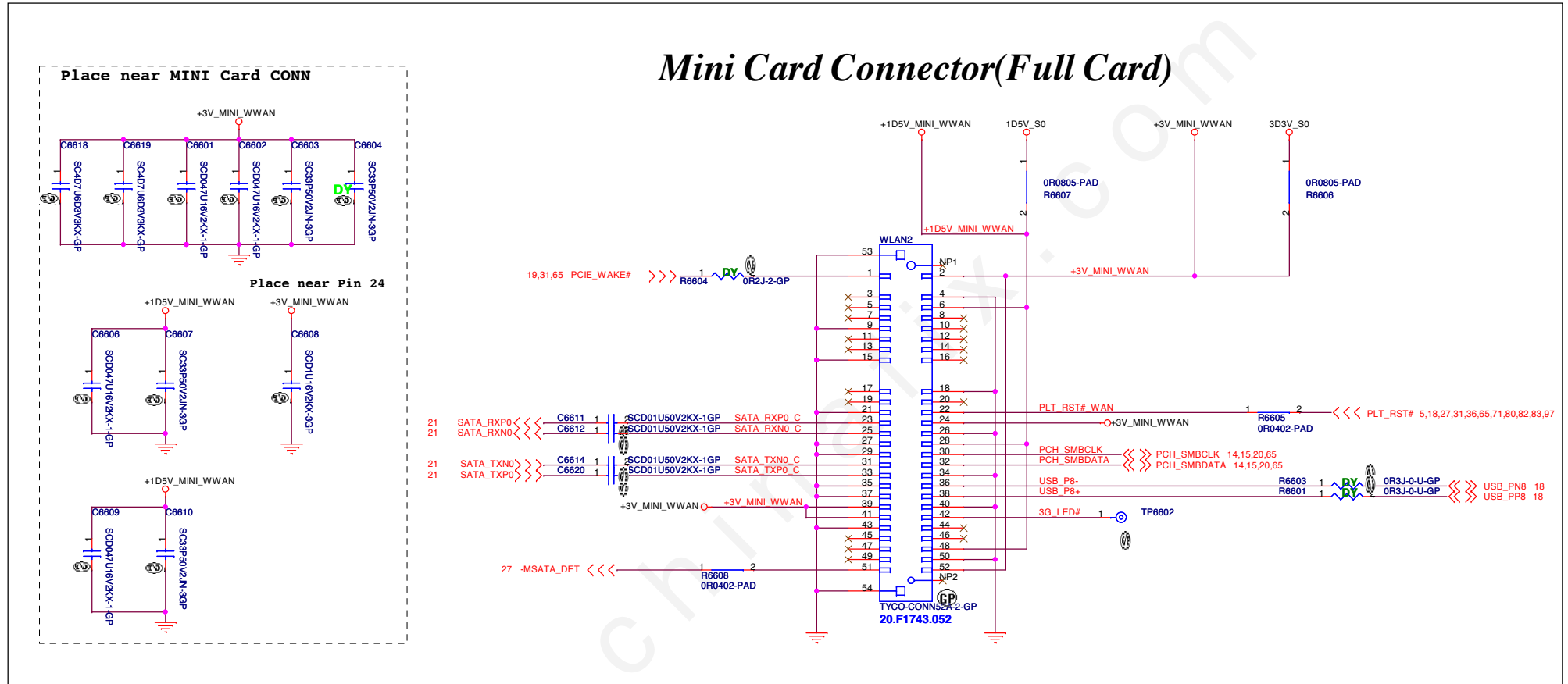
Title: **MINICARD(WLAN)/TP CONN**

Size A3 Document Number: **LA480** Rev: **SD**

Date: Friday, January 06, 2012 Sheet 65 of 103

mSATA for V Series Only

Mini Card Connector(Full Card)





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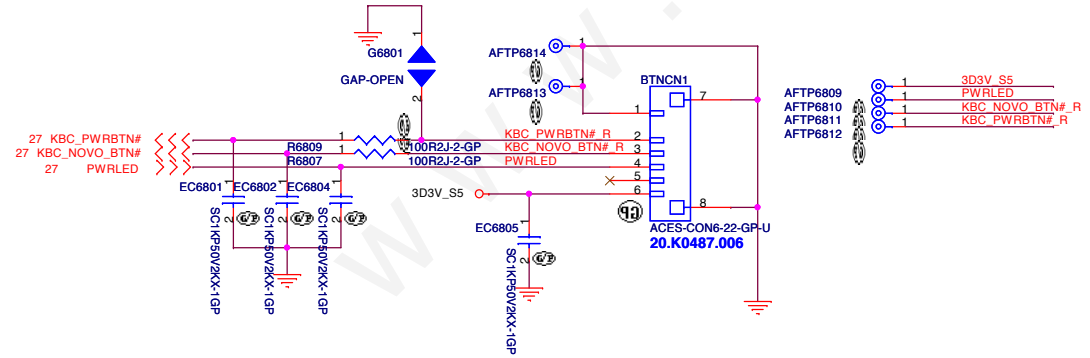
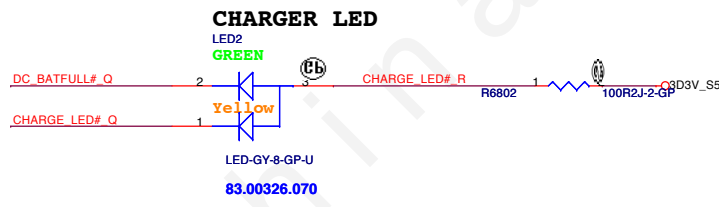
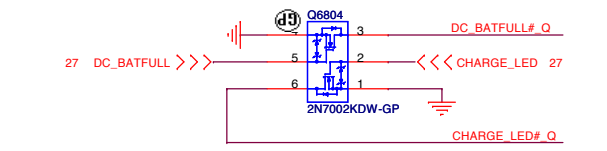
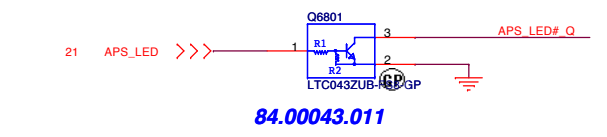
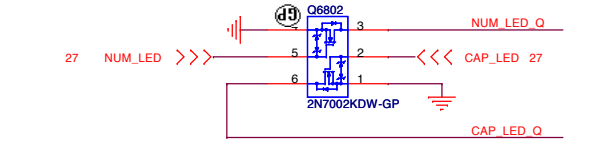
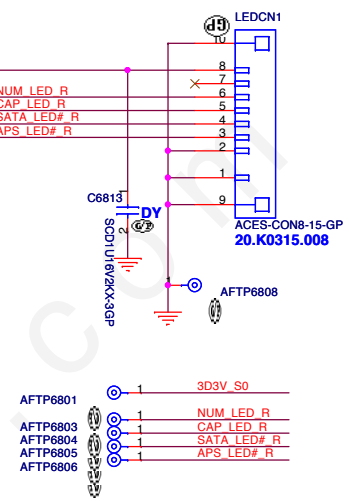
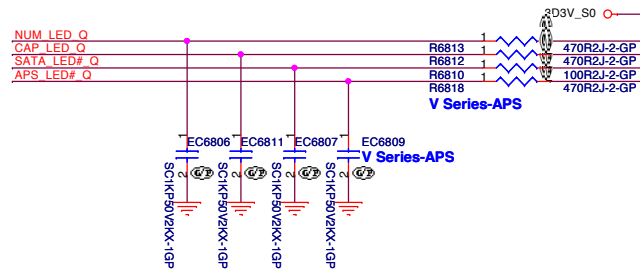
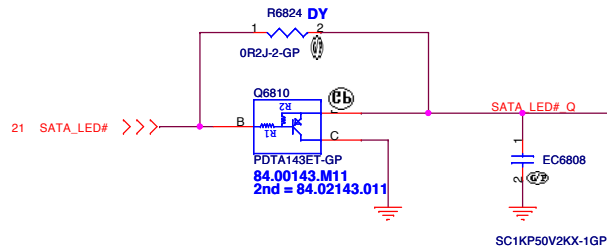
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<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 67	of 103

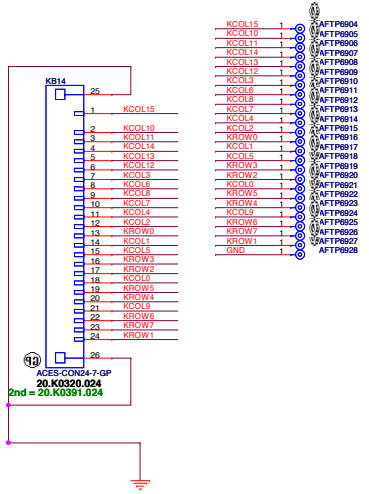
# SSID = User.Interface



**SSID = KBC**

**Internal Keyboard Connector**

<< KROW[8..7] 27  
>> KCOL[0..15] 27

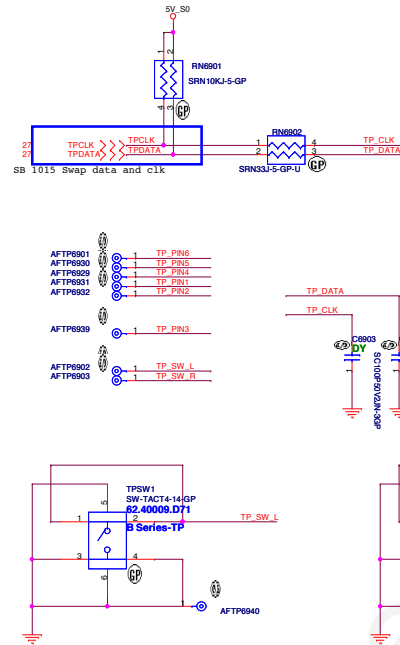


**KB14 for 14" VB480 & VB485**  
**KB15 for 15" VB580 & VB585**

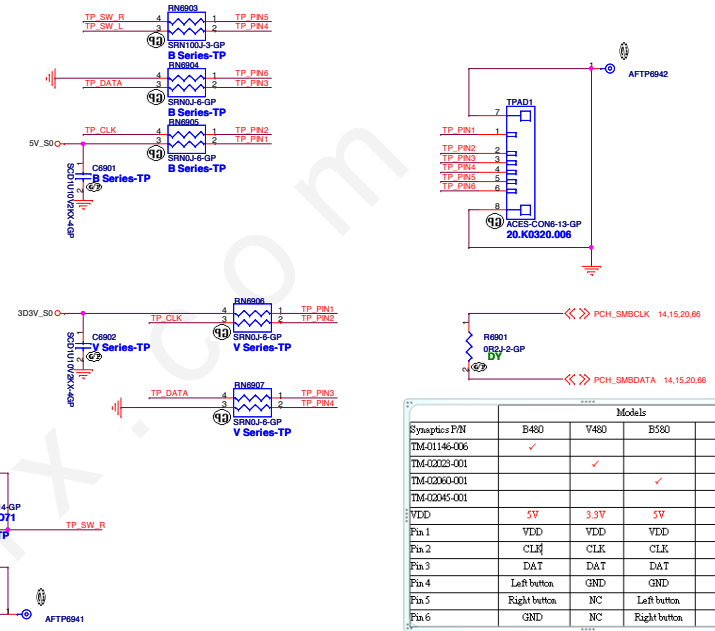
\* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

**SSID = Touch.Pad**



**Normal Pad for B Series 5V**  
**ClickPad for V Series 3.3V**



	Models			
Synaptics P/N	B480	V480	B580	V580
TM-01146-006	✓			
TM-02022-001		✓		
TM-02060-001			✓	
TM-02045-001				✓
VDD	5V	3.3V	5V	3.3V
Pin 1	VDD	VDD	VDD	VDD
Pin 2	CLK	CLK	CLK	CLK
Pin 3	DAT	DAT	DAT	DAT
Pin 4	Left button	GND	GND	GND
Pin 5	Right button	NC	Left button	NC
Pin 6	GND	NC	Right button	NC



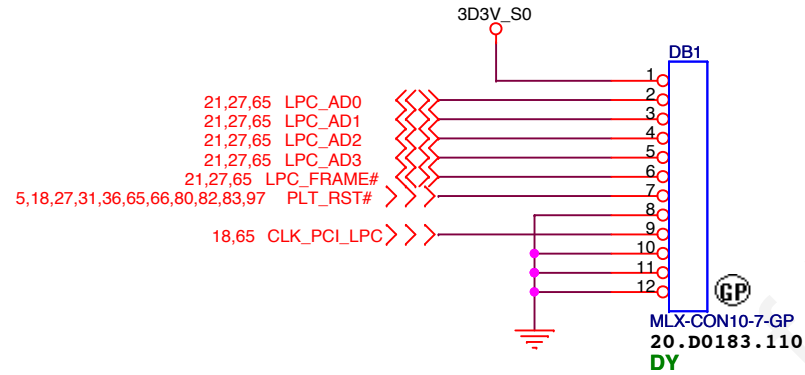


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<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Hall Sensor</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date:	Friday, January 06, 2012	Sheet 70	of 103



<Core Design>

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Dubug connector**

Size  
A4

Document Number

**LA480**

Rev  
**SD**

Date: Friday, January 06, 2012

Sheet 71 of 103



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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 72	of 103



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Title			
<b>Reserved</b>			
Size	Document Number		Rev
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Title			
CARD Reader CONN			
Size	Document Number	Rev.	SD
A2	LA480		
Date	Friday, January 06, 2012	Sheet	74 of 100

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Title			
<b>New Card</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date:	Friday, January 06, 2012	Sheet	75 of 103



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<b>Reserved</b>			
Size A4	Document Number <b>LA480</b>		Rev <b>SD</b>
Date: Friday, January 06, 2012		Sheet 76	of 103



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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size	Document Number	Rev	
A4	<b>LA480</b>	<b>SD</b>	
Date: Friday, January 06, 2012		Sheet 77 of	103

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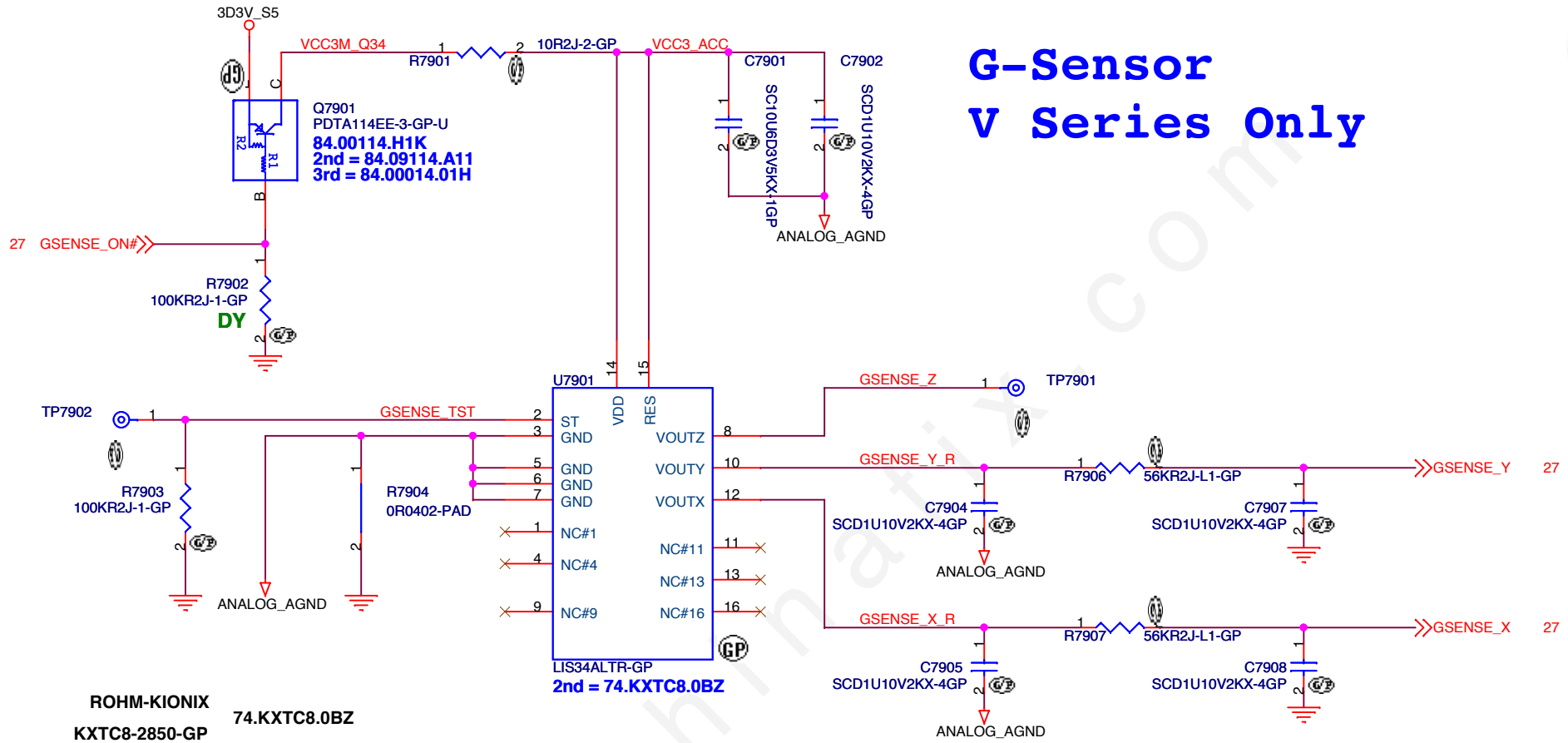
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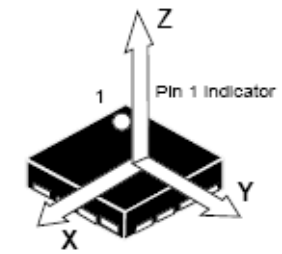
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Title			
<b>Reserved</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date:	Friday, January 06, 2012	Sheet	78 of 103

# G-Sensor V Series Only



ROHM-KIONIX  
KXTC8-2850-GP 74.KXTC8.0BZ



**Layout Comment :**

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>G-Sensor</b>			
Size A4	Document Number <b>LA480</b>		Rev <b>SD</b>
Date: Friday, January 06, 2012	Sheet	79 of	103

# RFID

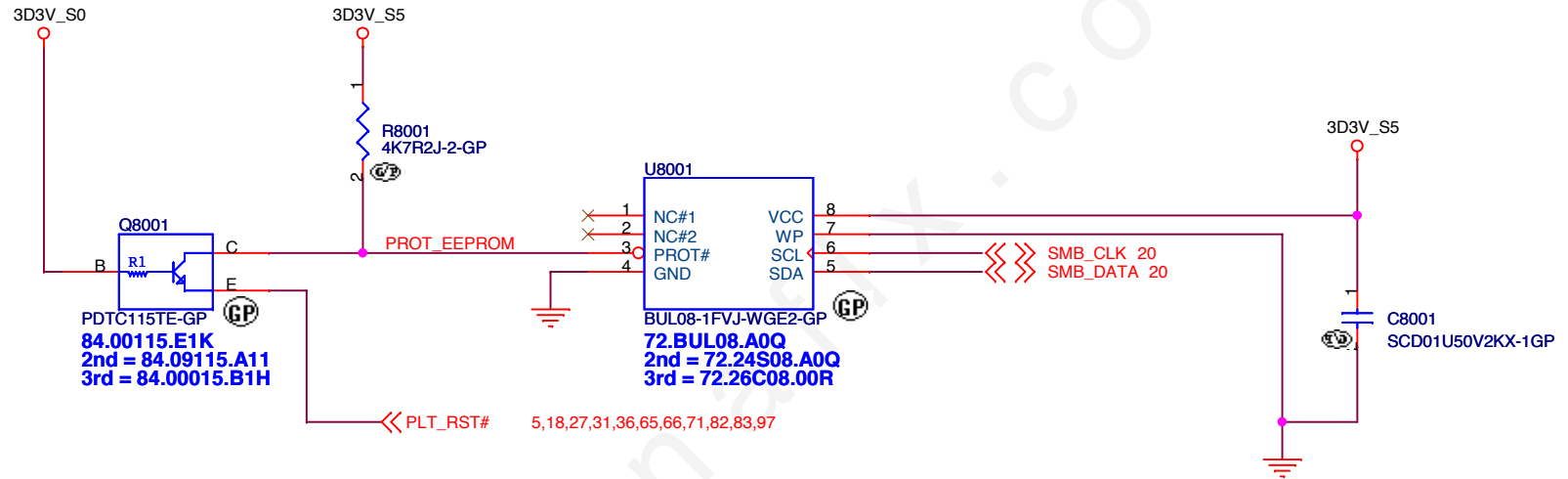


Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>RF ID</b>			
Size A4	Document Number <b>LA480</b>		Rev <b>SD</b>
Date: Friday, January 06, 2012	Sheet 80	of 103	



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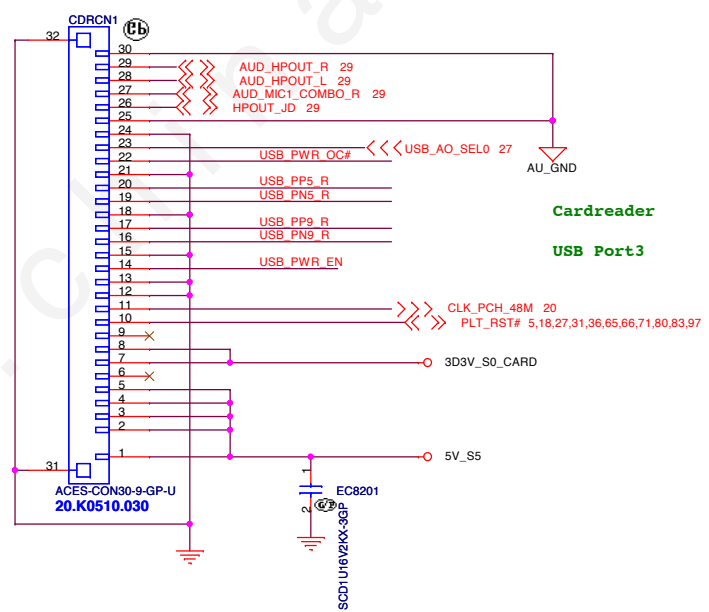
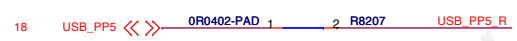
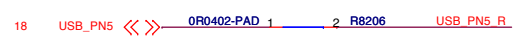
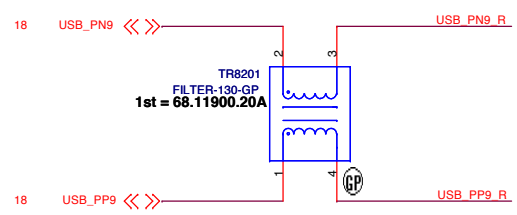
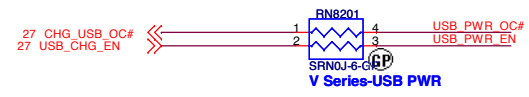
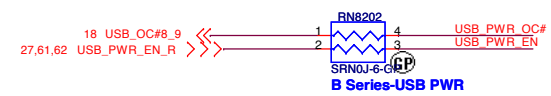
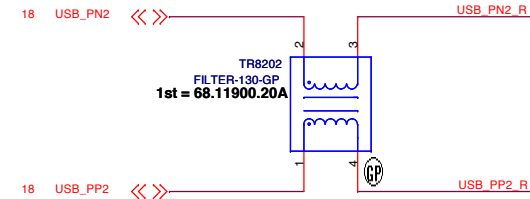
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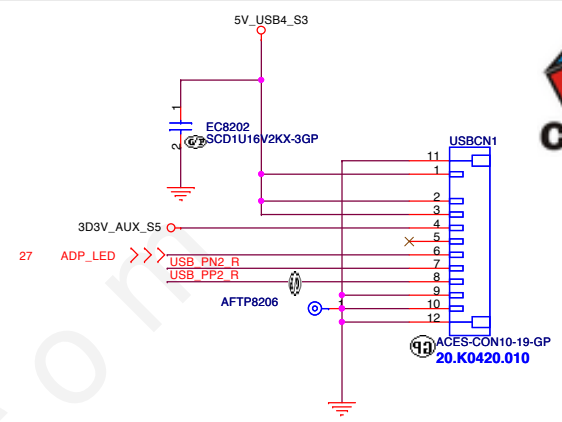
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 81	of 103

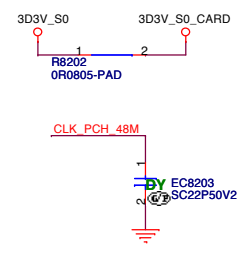
R8201 and R8203 Dual layout with TR8201



Cardreader  
USB Port3



- AFTP8201 1 5V\_USB4\_S3
- AFTP8202 1 3D3V\_AUX\_S5
- AFTP8203 1 ADP\_LED
- AFTP8204 1 USB\_PN2\_R
- AFTP8205 1 USB\_PP2\_R
- AFTP8210 1 HPOUT\_JD
- AFTP8213 1 USB\_PWR\_OC#
- AFTP8223 1 USB\_PWR\_EN
- AFTP8212 1 USB\_AO\_SEL0
- AFTP8209 1 AUD\_MIC1\_COMBO
- AFTP8207 1 AUD\_HPOUT\_R
- AFTP8208 1 AUD\_HPOUT\_L
- AFTP8211 1 AU\_GND
- AFTP8214 1 USB\_PP5\_R
- AFTP8215 1 USB\_PN5\_R
- AFTP8216 1 USB\_PP9\_R
- AFTP8217 1 USB\_PN9\_R
- AFTP8218 1 CLK\_PCH\_48M
- AFTP8219 1 PLT\_RST#
- AFTP8220 1 3D3V\_S0\_CARD
- AFTP8221 1 5V\_S5
- AFTP8224 1 GND
- AFTP8222 1 GND
- AFTP8225 1 GND



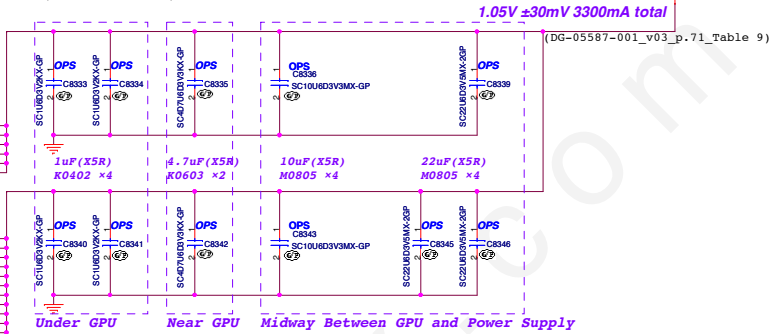
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<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>IO Board Connector</b>	
Title	SD
Size A3	Document Number LA480
Date: Friday, January 06, 2012	Sheet 82 of 103

PCI Express PEX\_IOVVD/Q Combined (DG-05587-001\_v03\_p.72\_Table 10)

Capacitor Type	Footprint	Population	Location
1.0uF	X6S 0402	4	Under GPU
4.7uF	X6S 0603	2	Near GPU
10uF	X5R 0805	4	Midway Between GPU and Power Supply
22uF	X5R 0805	4	Midway Between GPU and Power Supply

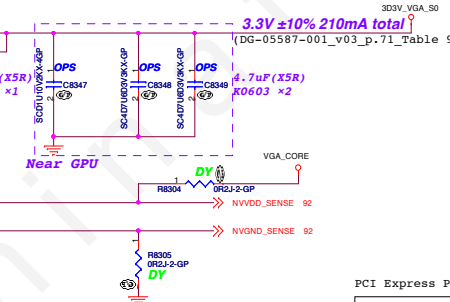
X6S (+/-22% -55-105°C)  
X5R (+/-15% -55-85°C)



PCI Express PEX\_SVDD/PLLHVDD Connected to NV3V3 (DG-05587-001\_v03\_p.72\_Table 12)

Capacitor Type	Footprint	Population	Location
0.1uF	X5R 0402	1	Near GPU
4.7uF	X5R 0603	2	Near GPU

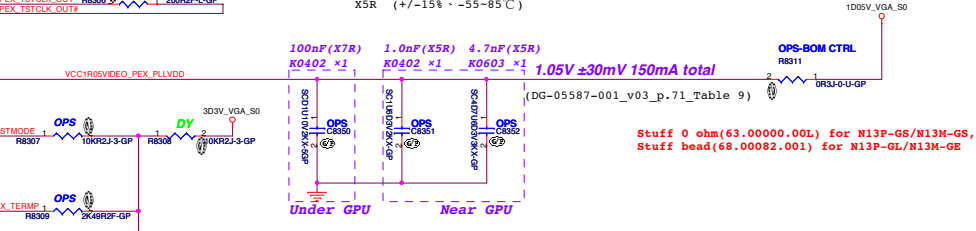
X5R (+/-15% -55-85°C)



PCI Express PEX\_PLLVDD (DG-05587-001\_v03\_p.72\_Table 11)

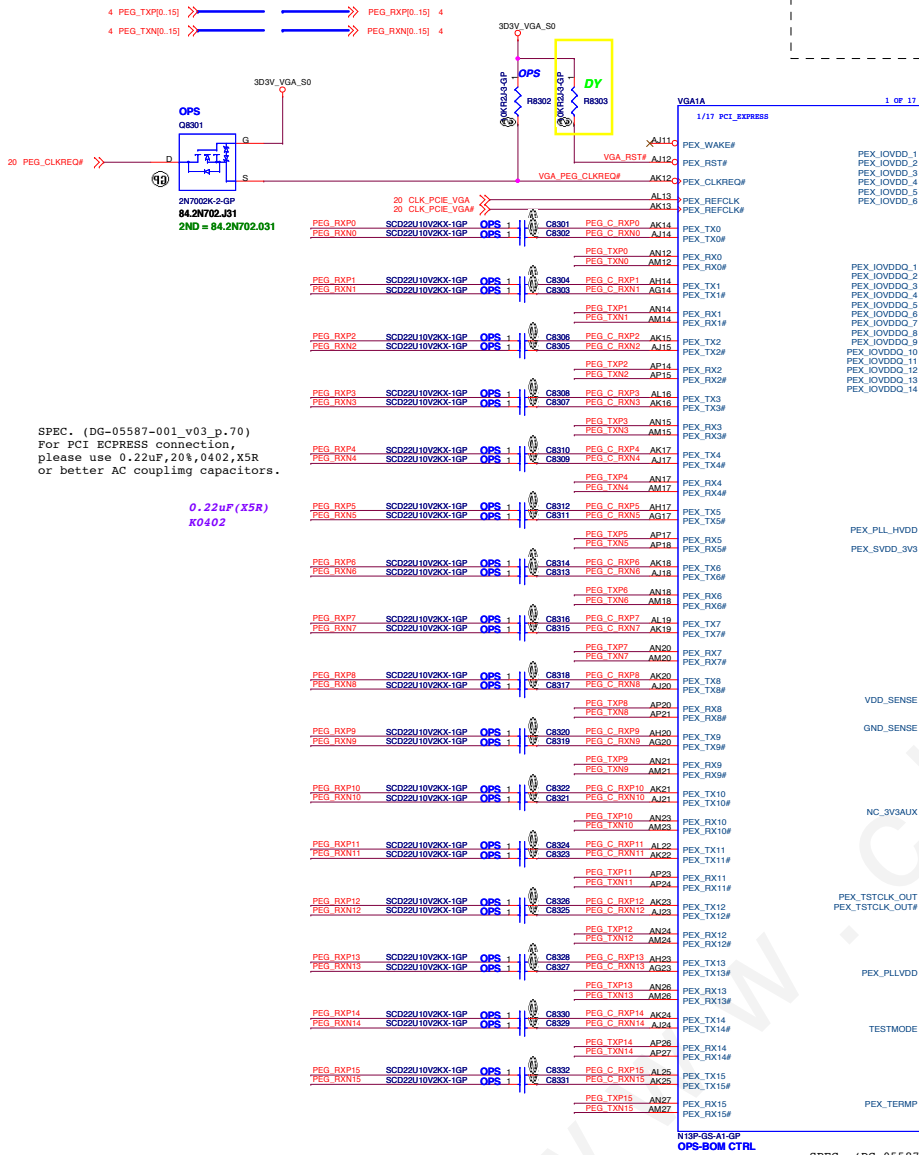
Capacitor Type	Footprint	Population	Location
100nF	X6S 0402	1	Under GPU
1.0uF	X5R 0603	1	Near GPU
4.7uF	X5R 0805	1	Near GPU

X6S (+/-22% -55-105°C)  
X5R (+/-15% -55-85°C)



Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,  
Stuff bead(68.00082.001) for N13P-GL/N13M-GE

SPEC. (DG-05587-001\_v03\_p.70)  
PEX\_CLK\_REQ\_N is an open-drain bi-directional signal;  
by default it should have a 10 kΩ pull-up to 3.3V.  
This signal is an active low signal.



SPEC. (DG-05587-001\_v03\_p.70)  
For PCI EXPRESS connection,  
please use 0.22uF, 20%, 0402, X5R  
or better AC coupling capacitors.

0.22uF (X5R)  
K0402

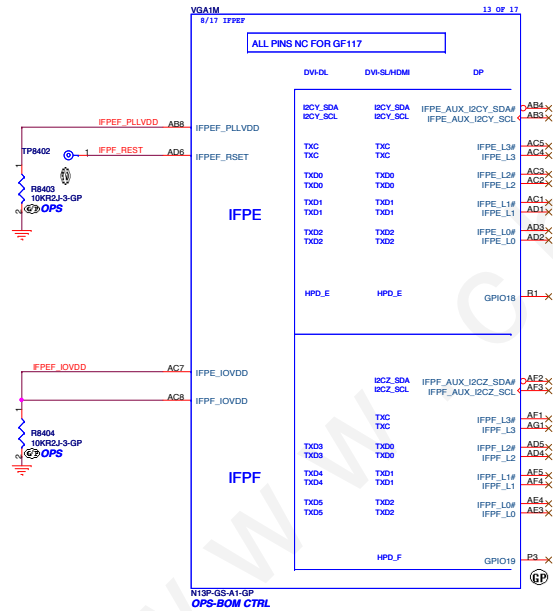
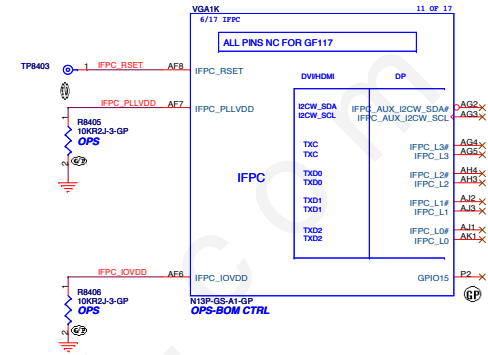
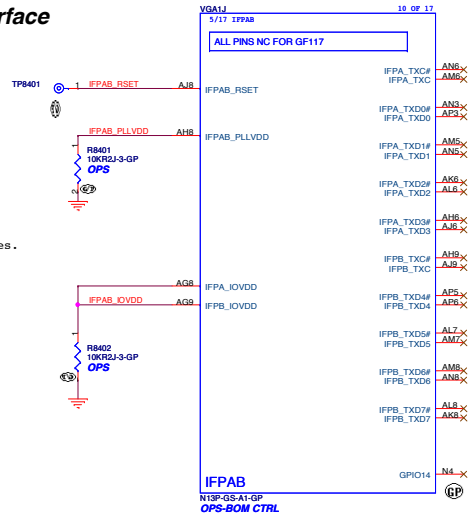
SPEC. (DG-05587-001\_v03\_p.214)  
By default, pull-down the TESTMODE pin to GND with a 10kΩ resistor.  
For XOR tree testing, TESTMODE should be pulled up to 3v3 with a 10 kΩ resistor.

SPEC. (DG-05587-001\_v03\_p.70)  
PEX\_TERM is used for internal calibration;  
pull-down this signal with 2.49 kΩ, 1% resistor.

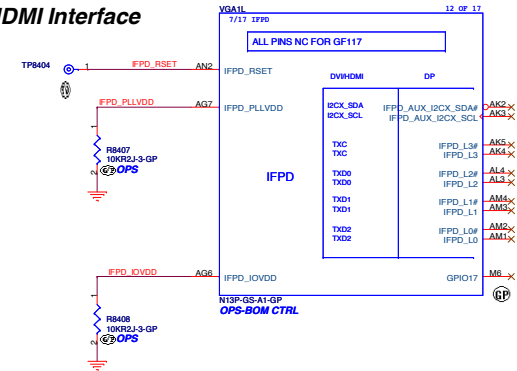
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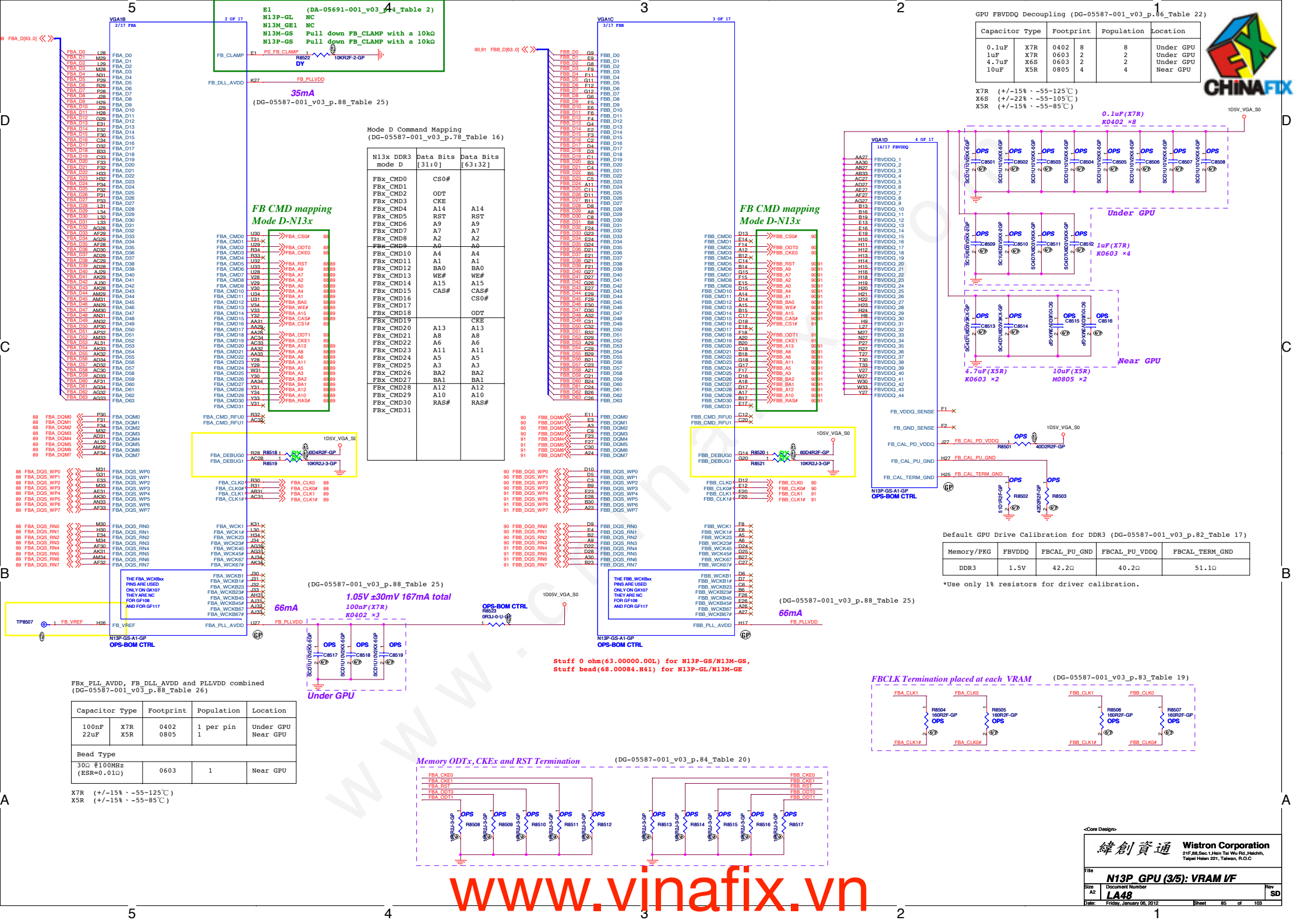
### LVDS Interface

SPEC. (DG-05587-001\_v03\_p.160)  
 Pull down IFPxy IOVDD with 10kΩ resistor.  
 Pull down IFPxy PLLVDD with 10kΩ resistor.  
 The other IO pins can be NC, this includes unused data lines.



### HDMI Interface

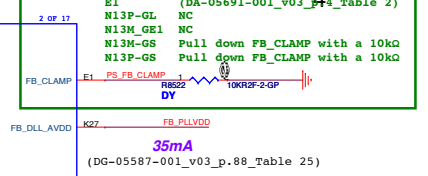




GPU FBVDDQ Decoupling (DG-05587-001\_v03\_p.66\_Table 2)

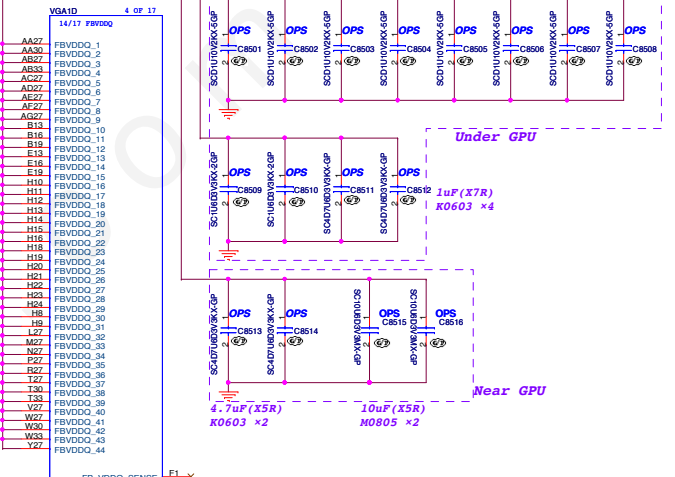
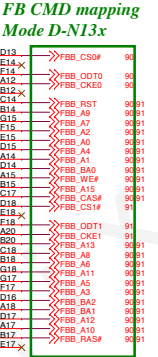
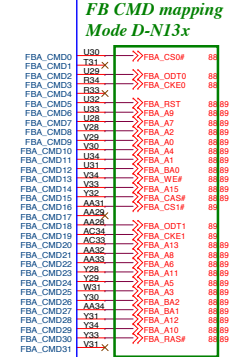
Capacitor Type	Footprint	Population	Location
0.1uF	X7R 0402	8	Under GPU
1uF	X7R 0603	2	Under GPU
4.7uF	X6S 0603	2	Under GPU
10uF	X5R 0805	4	Near GPU

X7R (+/-15% -55-125°C)  
X6S (+/-22% -55-105°C)  
X5R (+/-15% -55-85°C)



Mode D Command Mapping (DG-05587-001\_v03\_p.78\_Table 16)

N13x DDR3 mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0#	
FBx_CMD1	ODT	
FBx_CMD2	CKE	
FBx_CMD3	RST	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	B0	B0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CAS#	CS0#
FBx_CMD17		
FBx_CMD18	ODT	
FBx_CMD19	CKE	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		

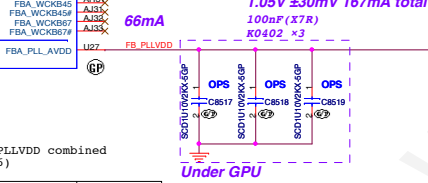


Default GPU Drive Calibration for DDR3 (DG-05587-001\_v03\_p.82\_Table 17)

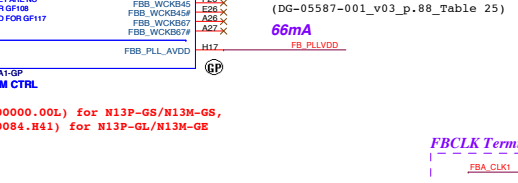
Memory/PKG	FBVDDQ	FBCL_PU_GND	FBCL_PU_VDDQ	FBCL_TERM_GND
DDR3	1.5V	42.2Ω	40.2Ω	51.1Ω

\*Use only 1% resistors for driver calibration.

THE FBV\_WCKBxx PINS ARE USED ONLY ON 6817 THEY ARE NC FOR GF117 AND FOR GF117



THE FBV\_WCKBxx PINS ARE USED ONLY ON 6817 THEY ARE NC FOR GF117 AND FOR GF117

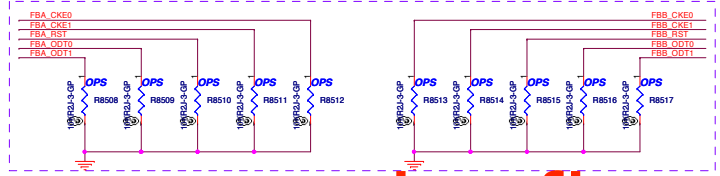


Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS, Stuff bead(68.00084.H41) for N13P-GL/N13M-GE

FBCLK Termination placed at each VRAM (DG-05587-001\_v03\_p.83\_Table 19)



Memory ODTx,CKEx and RST Termination (DG-05587-001\_v03\_p.84\_Table 20)

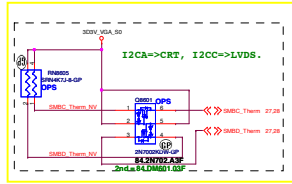
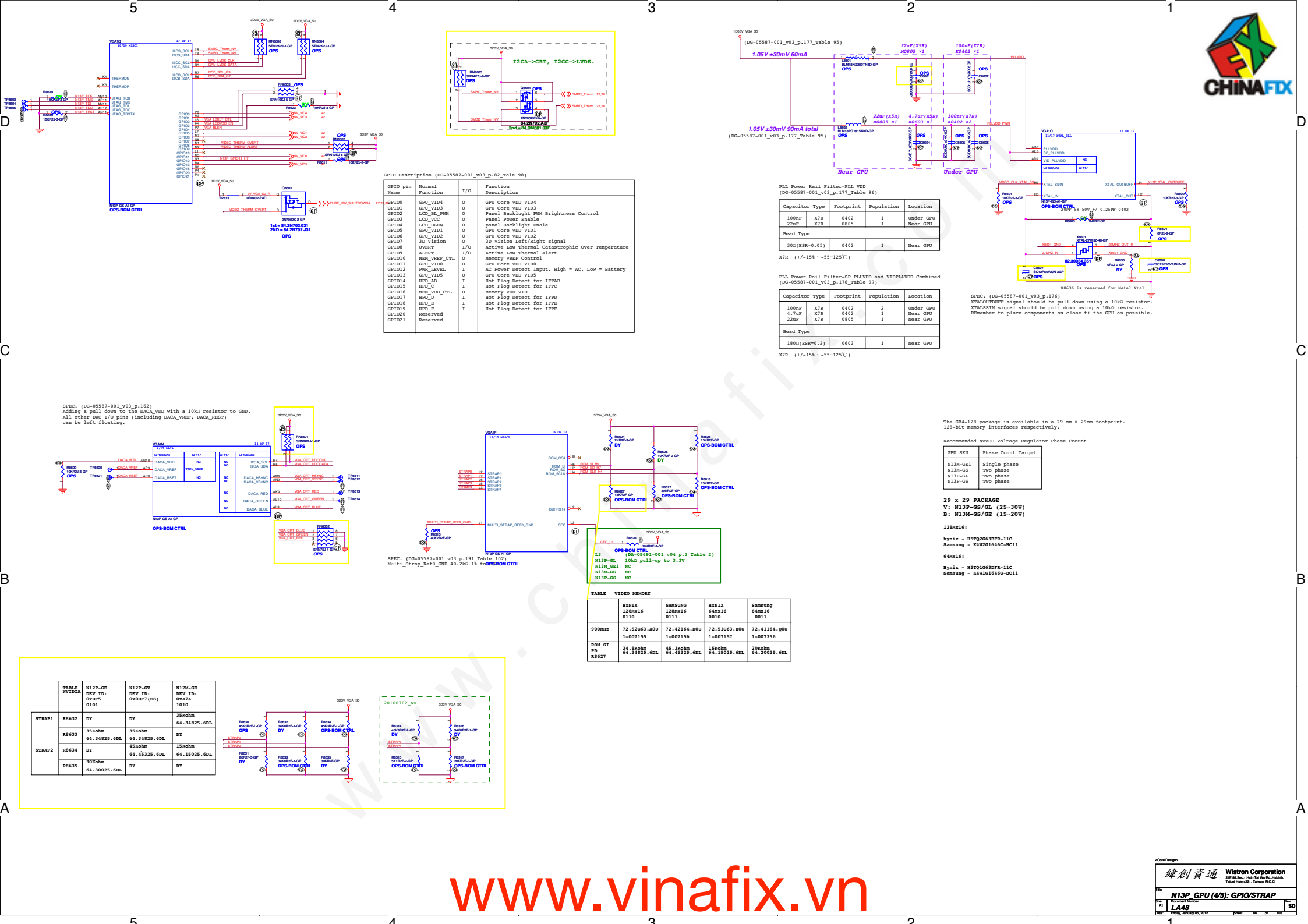


FBx\_PLL\_AVDD, FB\_DLL\_AVDD and PLLVDD combined (DG-05587-001\_v03\_p.88\_Table 26)

Capacitor Type	Footprint	Population	Location
100nF	X7R 0402	1 per pin	Under GPU
22uF	X7R 0805	1	Near GPU

Bead Type	Population	Location
30Ω @100MHz (ESR=0.01Ω)	0603	1

X7R (+/-15% -55-125°C)  
X5R (+/-15% -55-85°C)



GPIO Description (DG-05587-001\_v03\_p.82\_Table 98)

GPIO pin Name	Normal Function	I/O	Function Description
GPIO0	GPU_VID4	0	GPU Core VDD VID4
GPIO1	GPU_VID3	0	GPU Core VDD VID3
GPIO2	LCD_BK_PWM	0	Panel backlight PWM Brightness Control
GPIO3	LCD_VCC	0	Panel Power Enable
GPIO4	LCD_BLEN	0	panel backlight Enable
GPIO5	GPU_VID1	0	GPU Core VDD VID1
GPIO6	GPU_VID2	0	GPU Core VDD VID2
GPIO7	JD_Vision	0	JD Vision Left/Right signal
GPIO8	OVSTRT	1/0	Active Low Thermal Catastrophic Over Temperature
GPIO9	ALERT	1/0	Memory VREF Alert
GPIO10	MEM_VREF_CTL	0	Memory VREF Control
GPIO11	GPU_VDD0	0	GPU Core VDD VID0
GPIO12	PWR_LEVEL	0	AC Power Detect Input. High = AC, Low = Battery
GPIO13	GPU_VID5	0	GPU Core VDD VID5
GPIO14	HPD_AB	1	Hot Plug Detect for IPPAB
GPIO15	HPD_C	1	Hot Plug Detect for IPPC
GPIO16	MEM_VDD_CTL	0	Memory VDD VID
GPIO17	HPD_D	1	Hot Plug Detect for IPPD
GPIO18	HPD_E	1	Hot Plug Detect for IPPE
GPIO19	HPD_F	1	Hot Plug Detect for IPPF
GPIO20	Reserved		
GPIO21	Reserved		
GPIO22	Reserved		

PLL Power Rail Filter-PLL\_VDD (DG-05587-001\_v03\_p.177\_Table 96)

Capacitor Type	Footprint	Population	Location
100nF	X7R	0402	Under GPU
22uF	X7R	0805	Near GPU

Read Type  
300(ESR=0.05) 0402 1 Near GPU

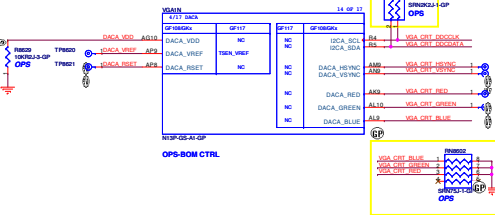
PLL Power Rail Filter-SP\_PLLVDD and VIDPLLVDD Combined (DG-05587-001\_v03\_p.178\_Table 97)

Capacitor Type	Footprint	Population	Location
100nF	X7R	0402	Under GPU
4.7uF	X7R	0402	1 Under GPU
22uF	X7R	0805	1 Near GPU

Read Type  
180(ESR=0.2) 0603 1 Near GPU

X7R (+/-15% -55-125°C)

SPEC. (DG-05587-001\_v03\_p.162)  
Adding a pull down to the DACA\_VDD with a 10k resistor to GND.  
All other I/O pins (including DACA\_VREF, DACA\_RESET) can be left floating.



SPEC. (DG-05587-001\_v03\_p.191\_Table 102)  
Multi Strap Ref0\_GND 40.2kΩ 1V to OPS-BOM CTRL

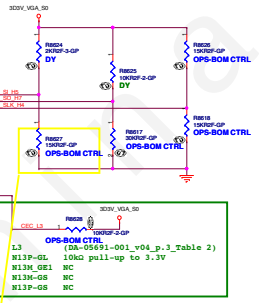


TABLE VIDEO MEMORY

	HYNIX	SAMSUNG	HYNIX	Samsung
900MRx	72.53063.A0U 1-007155	72.42164.D0U 1-007156	640616.0010	640616.0011
ROM_R1	34.8906h 64.14925.6DL	48.3606h 64.14925.6DL	15K020 64.14925.6DL	20K020 64.14925.6DL

The GB4-128 package is available in a 29 mm x 29mm footprint.  
128-bit memory interfaces respectively.

Recommended NVDD Voltage Regulator Phase Count

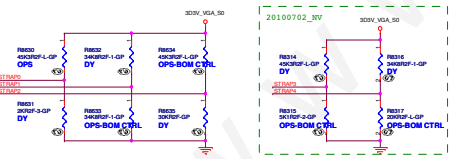
GPU SKU	Phase Count Target
N13M-GE1	Single phase
N13M-GS	Two phase
N13P-GL	Two phase
N13P-GS	Two phase

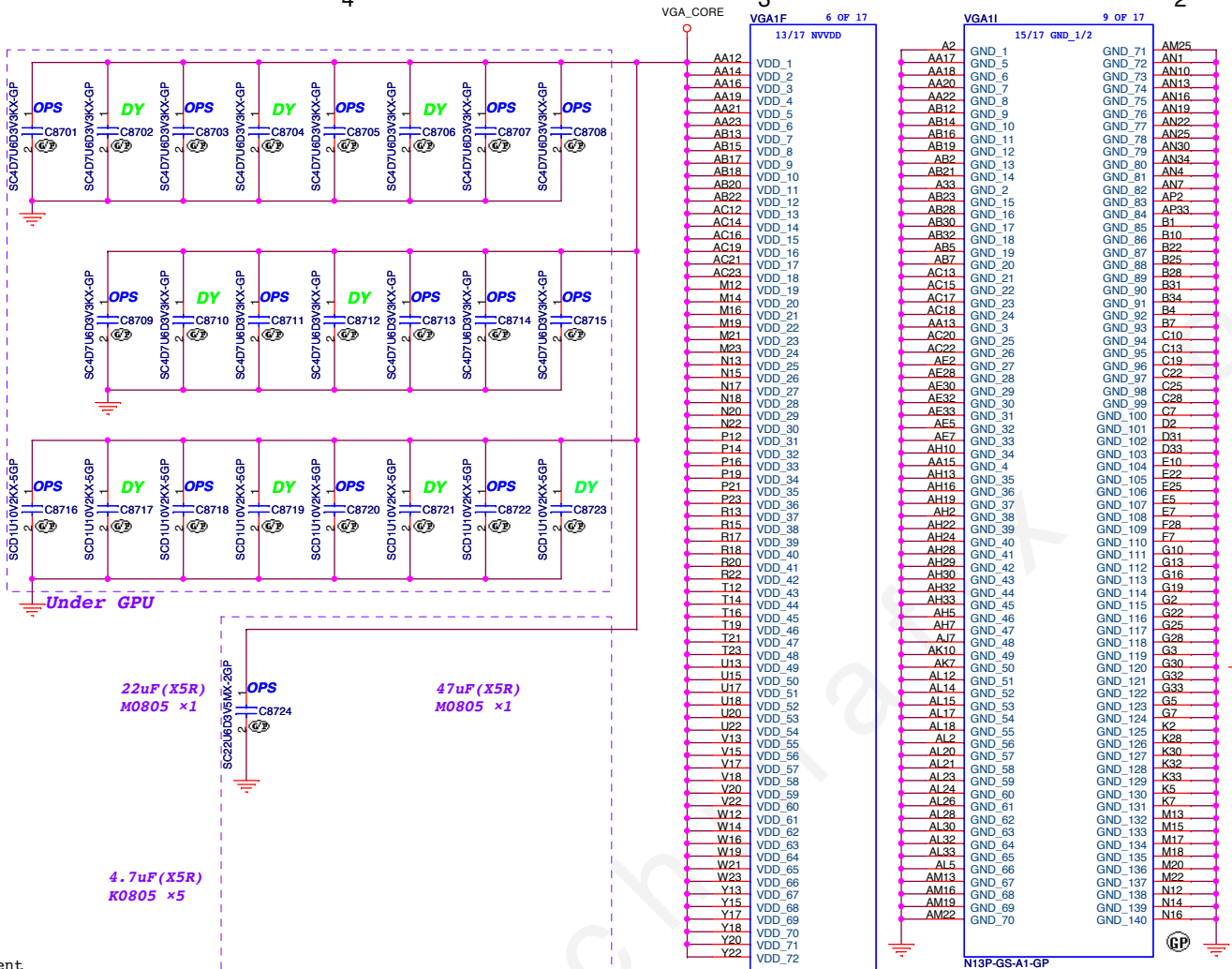
128bit16:

hynix - H57020618P8-11C  
Samsung - K4U201646C-BC11  
640x16:  
hynix - H57010610P8-11C  
Samsung - X4U101646C-BC11

TABLE N13P

STRAP1	R8632	DY	DY	35Kohm
	R8633	35Kohm	35Kohm	64.14825.6DL
	R8634	64.14825.6DL	64.14825.6DL	35Kohm
STRAP2	R8634	DY	45Kohm	15Kohm
	R8635	30Kohm	64.45325.6DL	64.15025.6DL
	R8635	64.30025.6DL	DY	DY





VNDD Decoupling Requirement (DG-05587-001\_v03\_p.56\_Table 7)

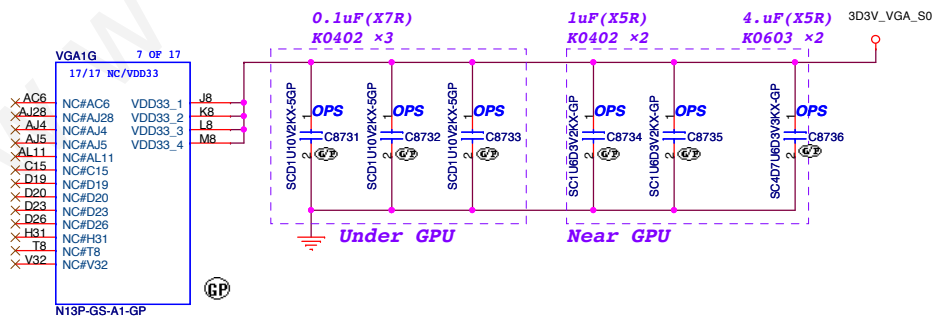
Capacitor Type	Footprint	Population	Location
4.7uF	X6S 0603	15	Under GPU
0.1uF	X7R 0402	8	Under GPU
47uF	X5R 0805	1	Near GPU
22uF	X5R 0805	1	Near GPU
4.7uF	X5R 0805	5	Near GPU

X7R (+/-15%、-55-125°C)  
 X6S (+/-22%、-55-105°C)  
 X5R (+/-15%、-55-85°C)

VDD33 Decoupling (DG-05587-001\_v03\_p.57\_Table 8)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R 0402	3	Under GPU
1uF	X5R 0402	2	Near GPU
4.7uF	X5R 0603	1	Near GPU

X7R (+/-15%、-55-125°C)  
 X5R (+/-15%、-55-85°C)



<Core Design>

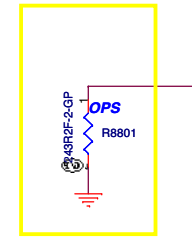
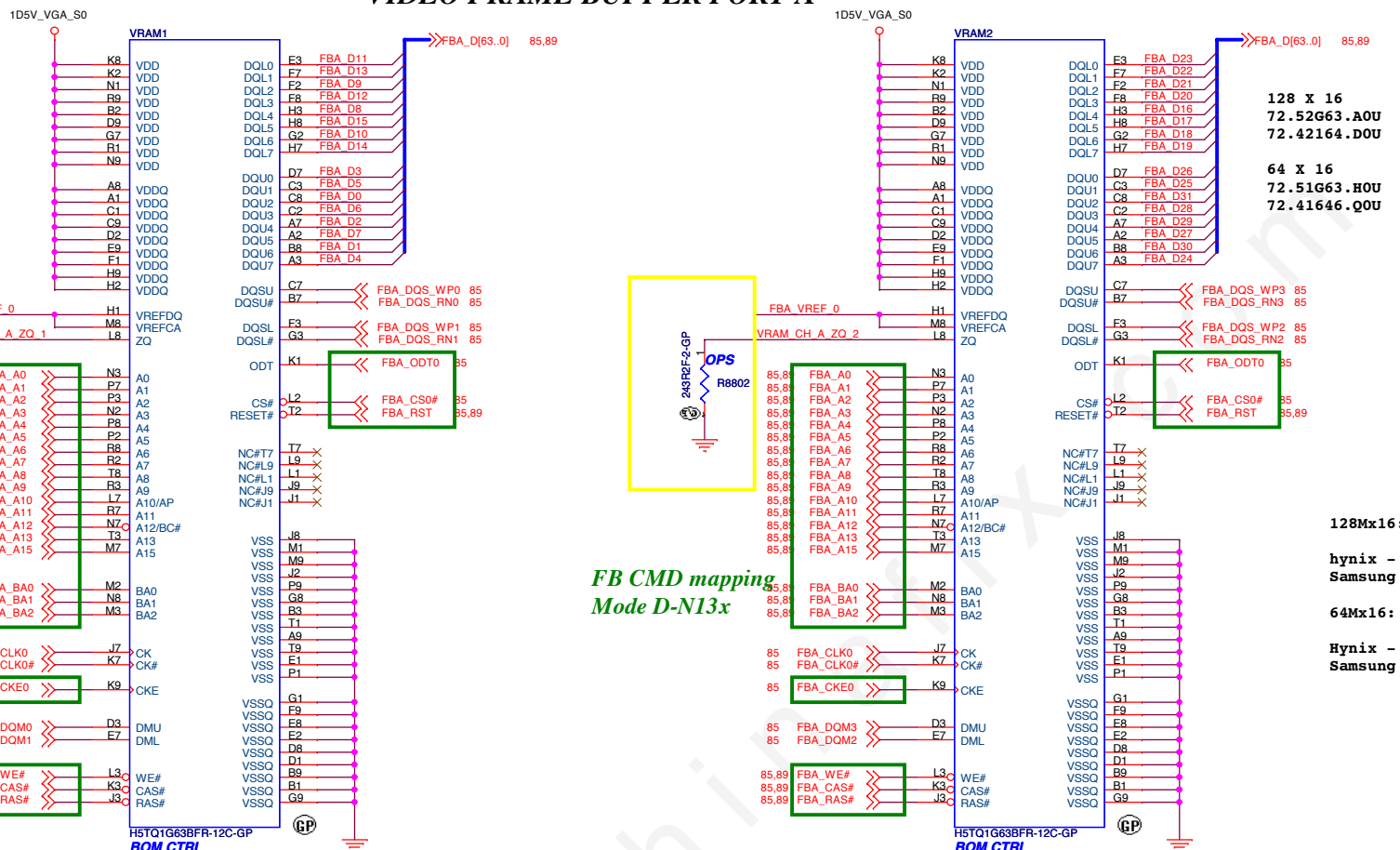
**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C

Title: **N13P GPU (5/5): PWR/GND**

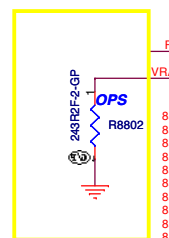
Size A3 Document Number **LA48** Rev **SD**

Date: Friday, January 06, 2012 Sheet 87 of 103

# VIDEO FRAME BUFFER PORT A



**FB CMD mapping Mode D-N13x**



**FB CMD mapping Mode D-N13x**

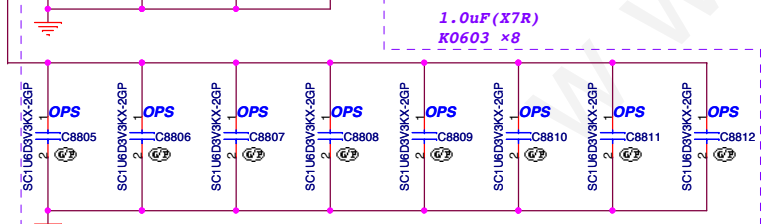
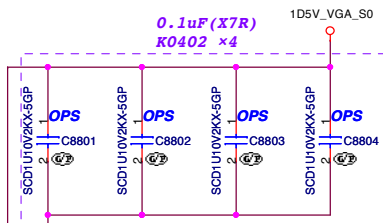
- 128 X 16  
72.52G63.A0U IC VRAM K4W2G1646C-HC11 FBGA96
- 64 X 16  
72.51G63.H0U IC VRAM H5TQ1G63DFR-11C FBGA 96BALLS
- 72.41646.Q0U IC VRAM K4W1G1646G-BC11 FBGA 96BALLS

- 128Mx16:  
hynix - H5TQ2G63BFR-11C  
Samsung - K4W2G1646C-HC11
- 64Mx16:  
Hynix - H5TQ1G63DFR-11C  
Samsung - K4W1G1646G-BC11

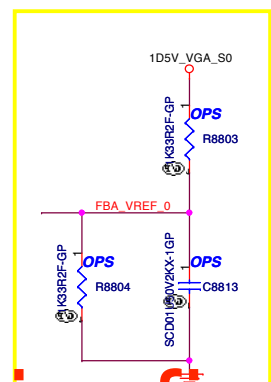
Combined Memory FBVDD/Q Decoupling DDR3\*16 with Clamshell Layout (DG-05587-001\_v03\_p.87\_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)  
\*Per clamshell pair



Close to VRAM(For VRAM1 & VRAM2)



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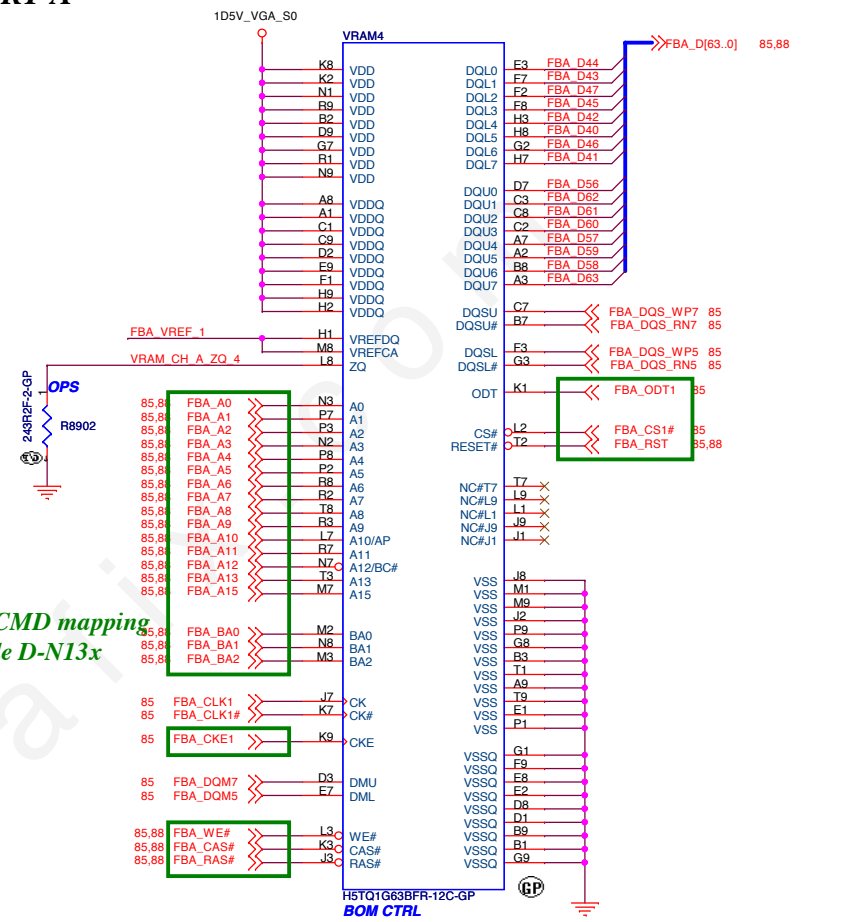
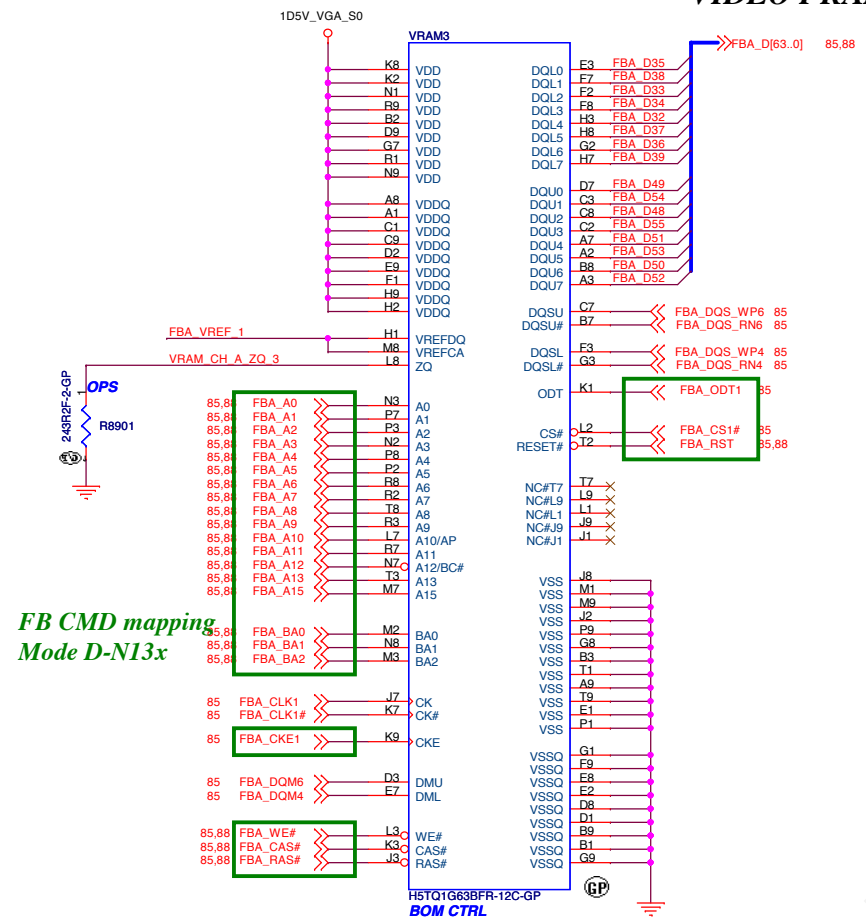
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Size A3 Document Number **LA48** Rev SD

Date: Friday, January 06, 2012 Sheet 88 of 103



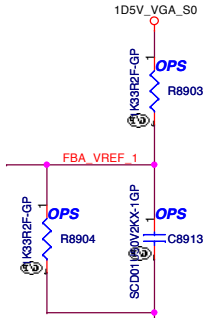
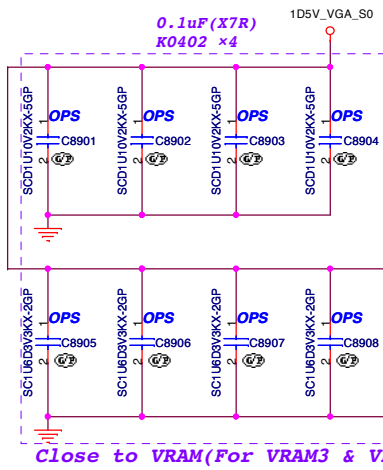
# VIDEO FRAME BUFFER PORT A



Combined Memory FBVDD/Q Decoupling DDR3\*16 with Clamshell Layout (DG-05587-001\_v03\_p.87\_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)  
\*Per clamshell pair



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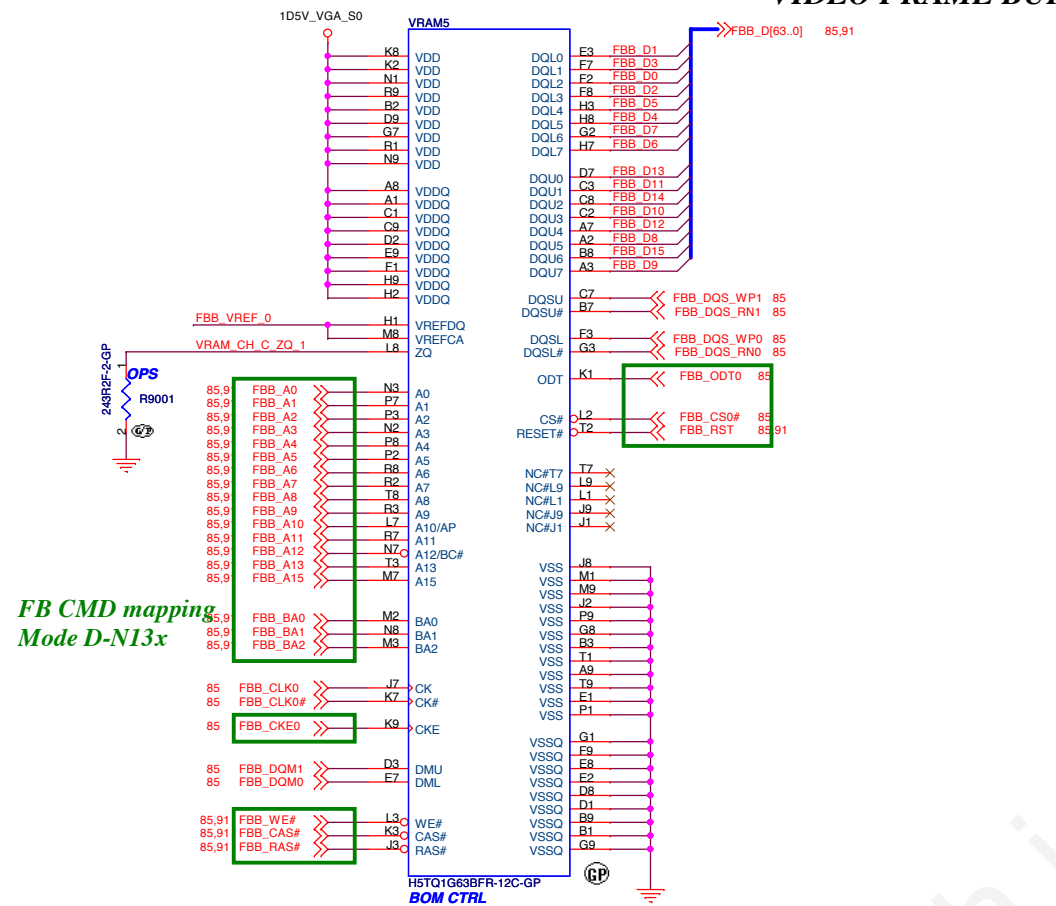
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Title: **CHANNEL-A\_VRAM3,4 (2/4)**

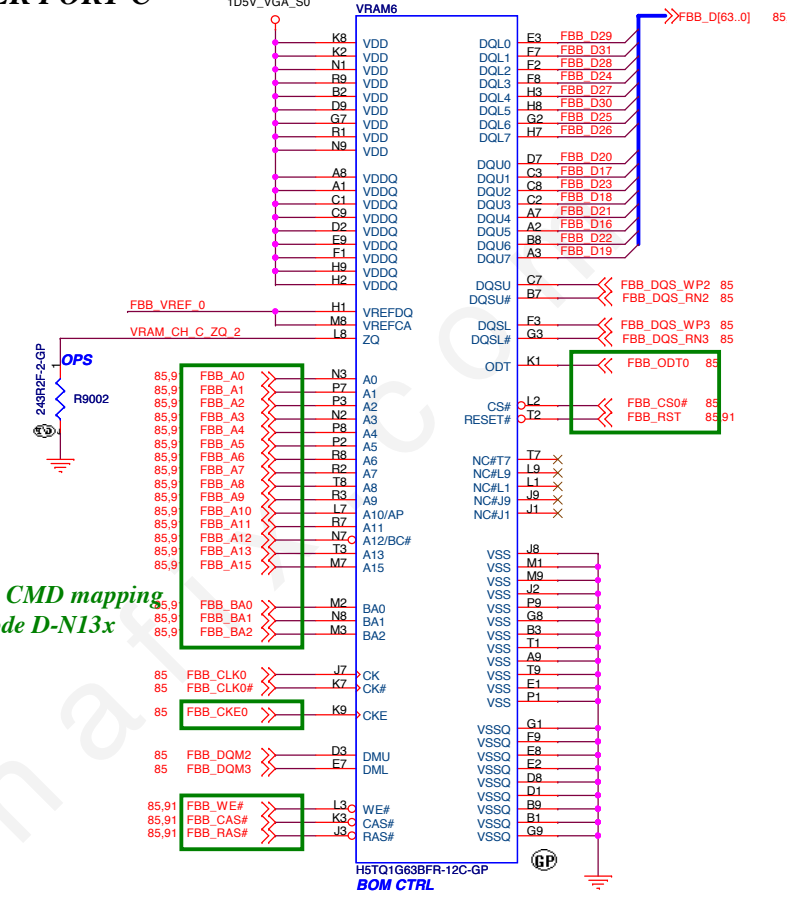
Size A3 Document Number **LA48** Rev SD

Date: Friday, January 06, 2012 Sheet 89 of 103

# VIDEO FRAME BUFFER PORT C



**FB CMD mapping  
Mode D-N13x**

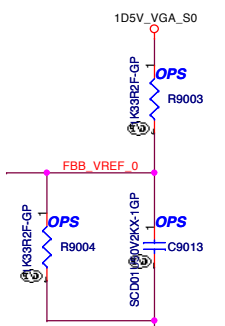
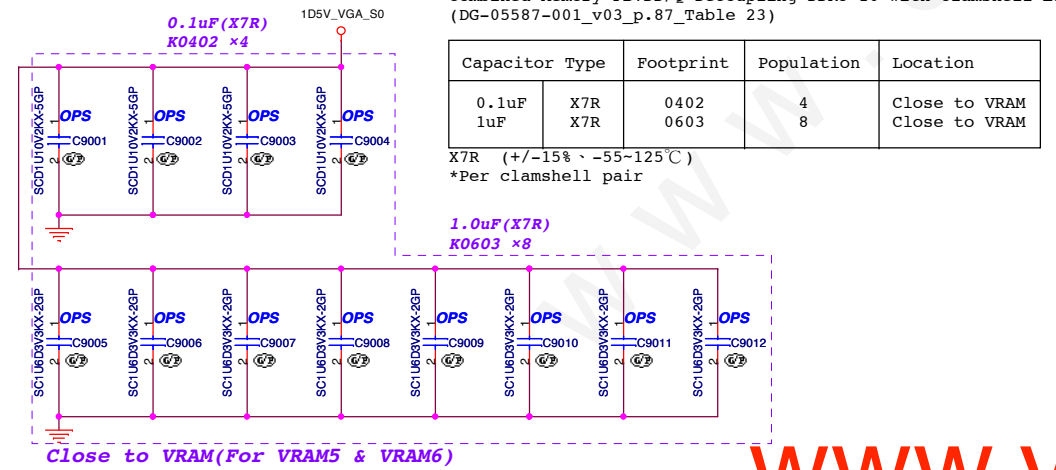


**FB CMD mapping  
Mode D-N13x**

Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001\_v03\_p.87\_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF X7R	X7R	0402	4
1uF	X7R	0603	8
			Close to VRAM
			Close to VRAM

X7R (+/-15%、-55-125°C)  
\*Per clamshell pair



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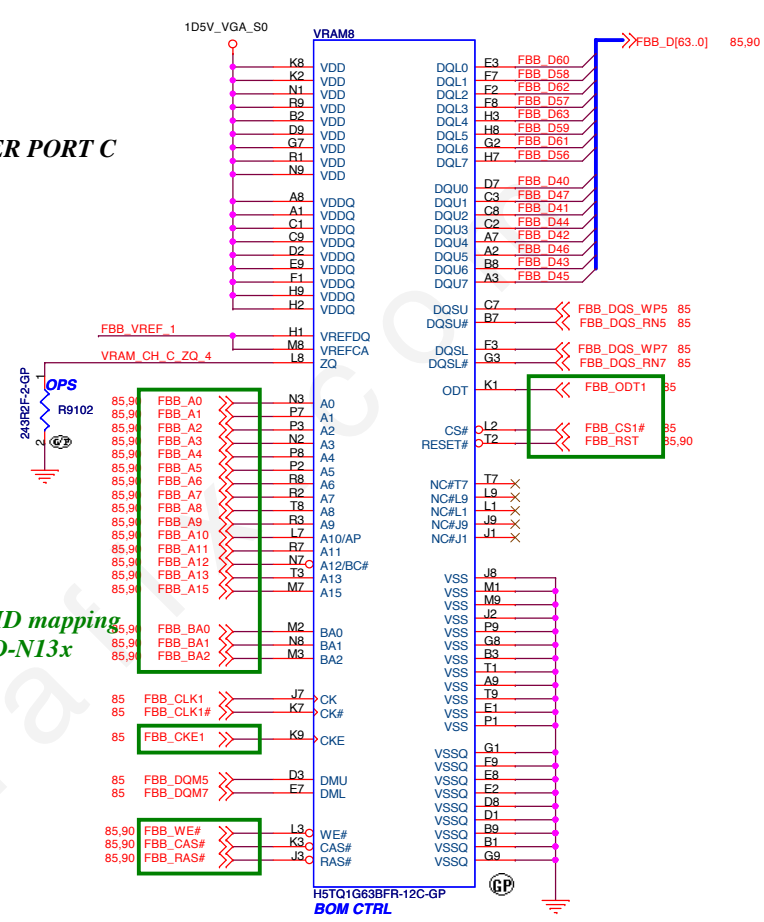
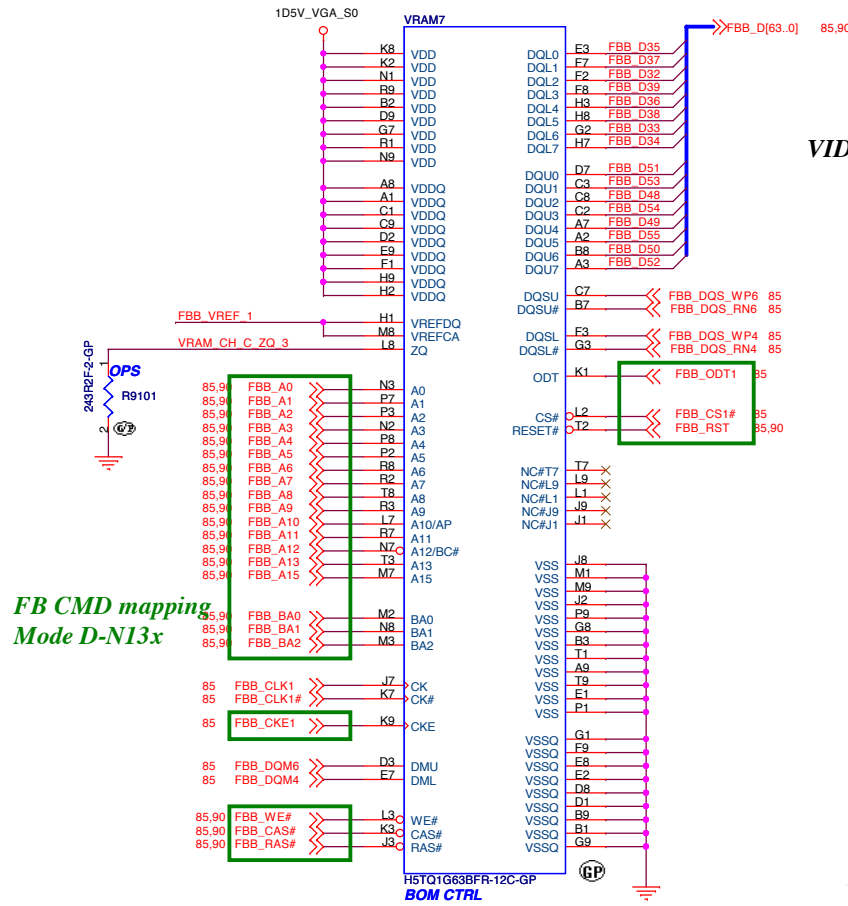
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Title: **CHANNEL-C\_VRAM5,6 (3/4)**

Size A3 Document Number **LA48** Rev **SD**

Date: Friday, January 06, 2012 Sheet 90 of 103

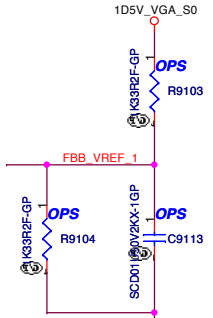
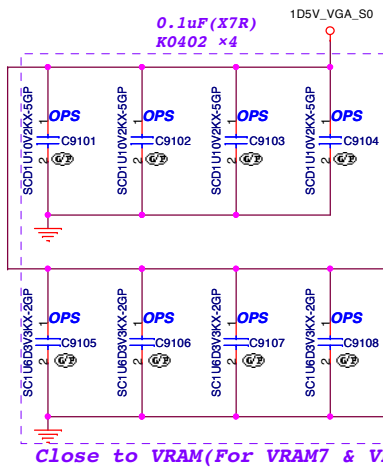
### VIDEO FRAME BUFFER PORT C



Combined Memory FBVDD/Q Decoupling DDR3\*16 with Clamshell Layout (DG-05587-001\_v03\_p.87\_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)  
\*Per clamshell pair

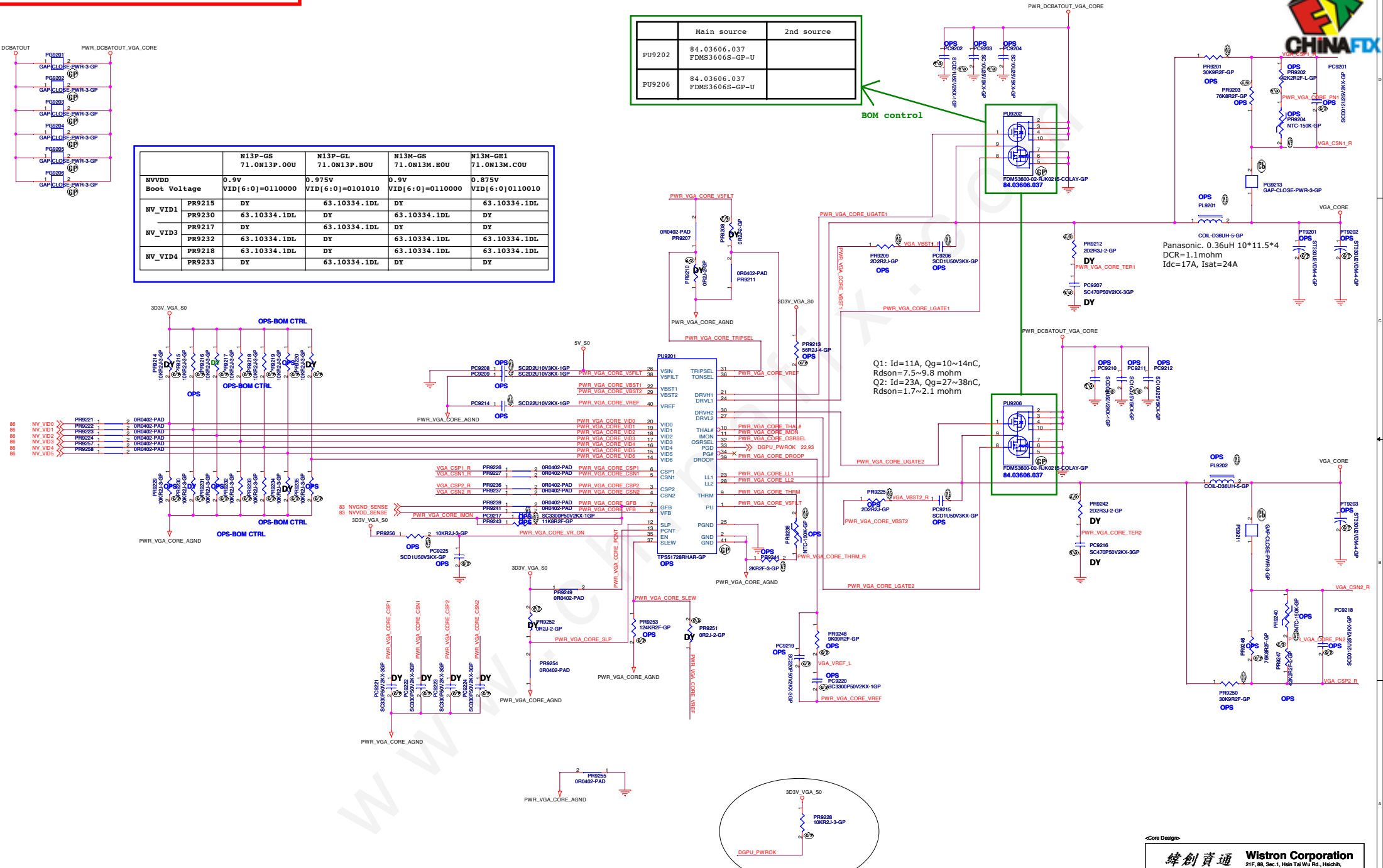




SSID = PWR.Plane.Regulator\_GFX

	Main source	2nd source
PU9202	84.03606.037 FDMS3606S-GP-U	
PU9206	84.03606.037 FDMS3606S-GP-U	

	N13P-GS 71.0N13P.00U	N13P-GL 71.0N13P.B0U	N13M-GS 71.0N13M.E0U	N13M-GE1 71.0N13M.C0U
NV_VDD Boot Voltage	0.9V VID[6:0]=0110000	0.975V VID[6:0]=0101010	0.9V VID[6:0]=0110000	0.875V VID[6:0]=0110010
NV_VID1	PR9215 DY PR9230 63.10334.1DL	63.10334.1DL DY	63.10334.1DL DY	63.10334.1DL DY
NV_VID3	PR9217 DY PR9232 63.10334.1DL	63.10334.1DL DY	63.10334.1DL DY	63.10334.1DL DY
NV_VID4	PR9218 DY PR9233 63.10334.1DL	63.10334.1DL DY	63.10334.1DL DY	63.10334.1DL DY



BOM control

Q1: Id=11A, Qg=10~14nC,  
Rdson=7.5~9.8 mohm  
Q2: Id=23A, Qg=27~38nC,  
Rdson=1.7~2.1 mohm

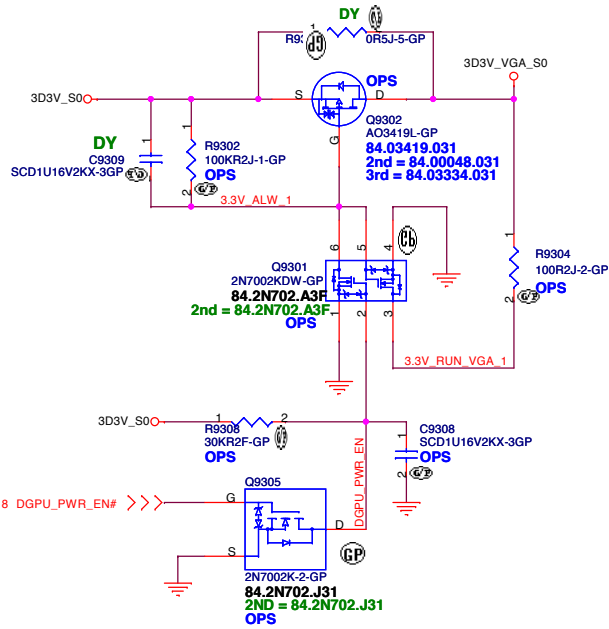
Panasonic. 0.36uH 10\*11.5\*4  
DCR=1.1mohm  
Idc=17A, Isat=24A

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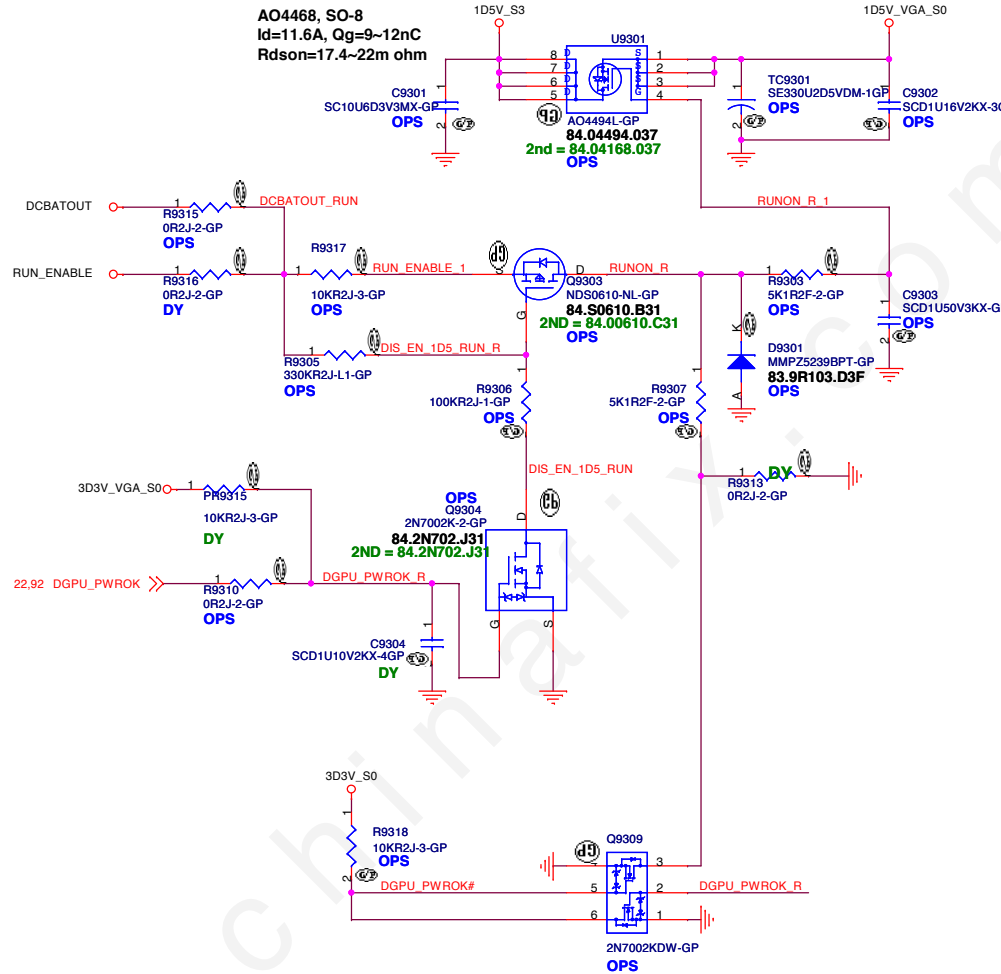
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Date	Friday, January 06, 2012
Sheet	2 of 2
Rev	SD

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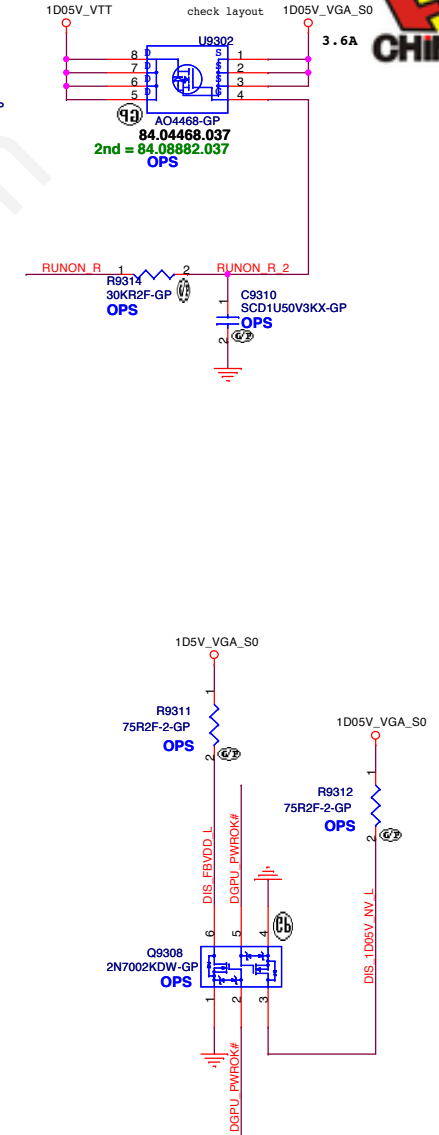
**+3VS to 3.3V\_DELAY Transfer**



**1D5V\_VGA\_S0**



**1.05V to 1.05V\_VGA\_S0 Transfer**



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<p><b>緯創資通 Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
Title	<b>DISCRETE VGA POWER</b>
Size A3	Document Number <b>LA480</b>
Date: Friday, January 06, 2012	Rev <b>SD</b>
Sheet 93	of 103

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Size A4	Document Number LA480	Rev SD
Date:	Friday, January 06, 2012	Sheet 94 of 103

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Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 95	of 103

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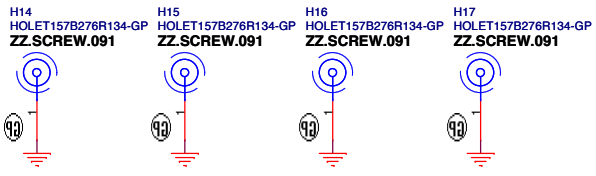
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Title			
<b>TOUCH PANEL</b>			
Size	Document Number		Rev
A4	<b>LA480</b>		<b>SD</b>
Date: Friday, January 06, 2012		Sheet 96	of 103

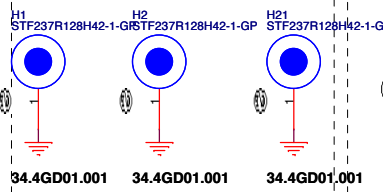




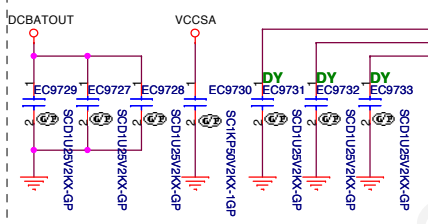
### CPU Plate



### VGA Std-Off

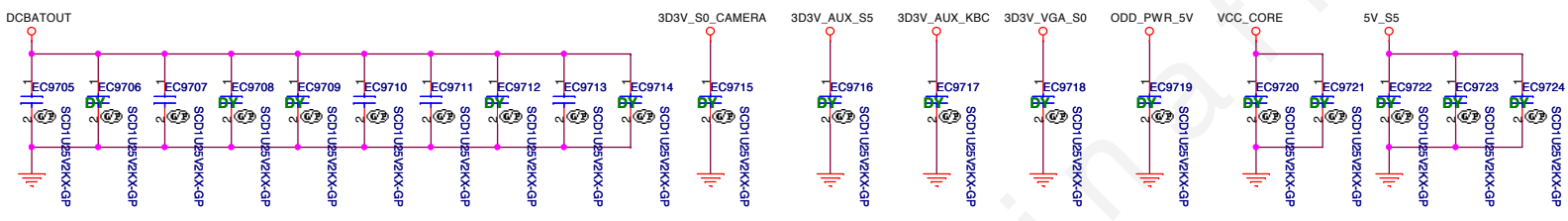
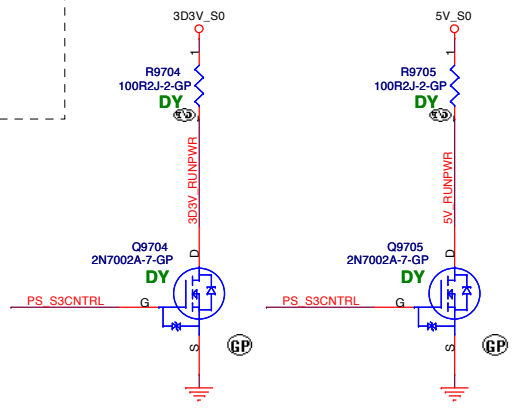
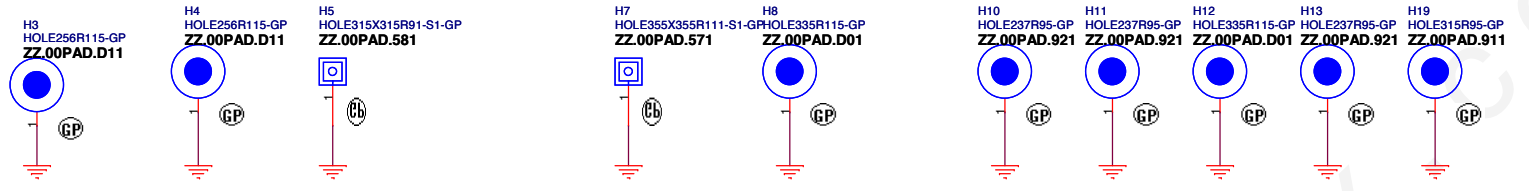


### MINI PCIE

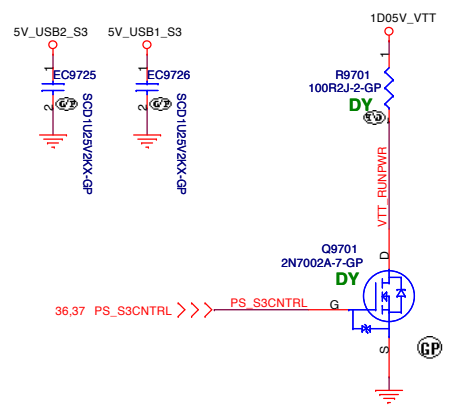
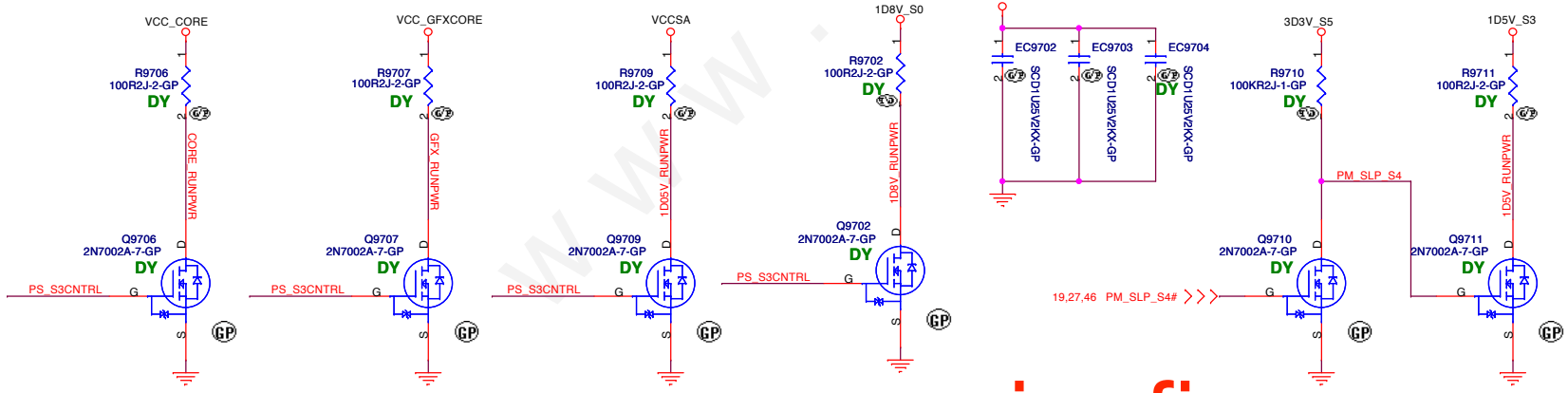


XDP\_DBRESET# 5,19  
H\_CUPW/RGD 5,22  
PLT\_RST# 5,18,27,31,36,65,66,71,80,82,83

### 14" Structure boss



### For Discharge



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Title	<b>UNUSED PARTS/EMI Capacitors</b>		Rev	<b>SD</b>
Size	Document Number	LA480		
A3				
Date:	Friday, January 06, 2012	Sheet	97	of 103

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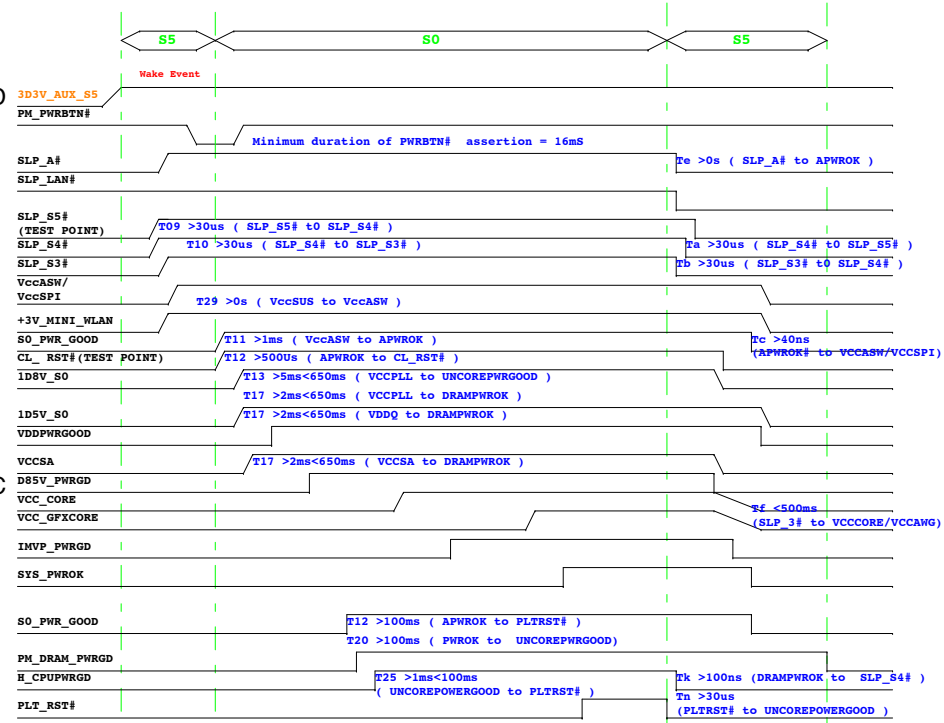
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<b>緯創資通</b>	<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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Title		
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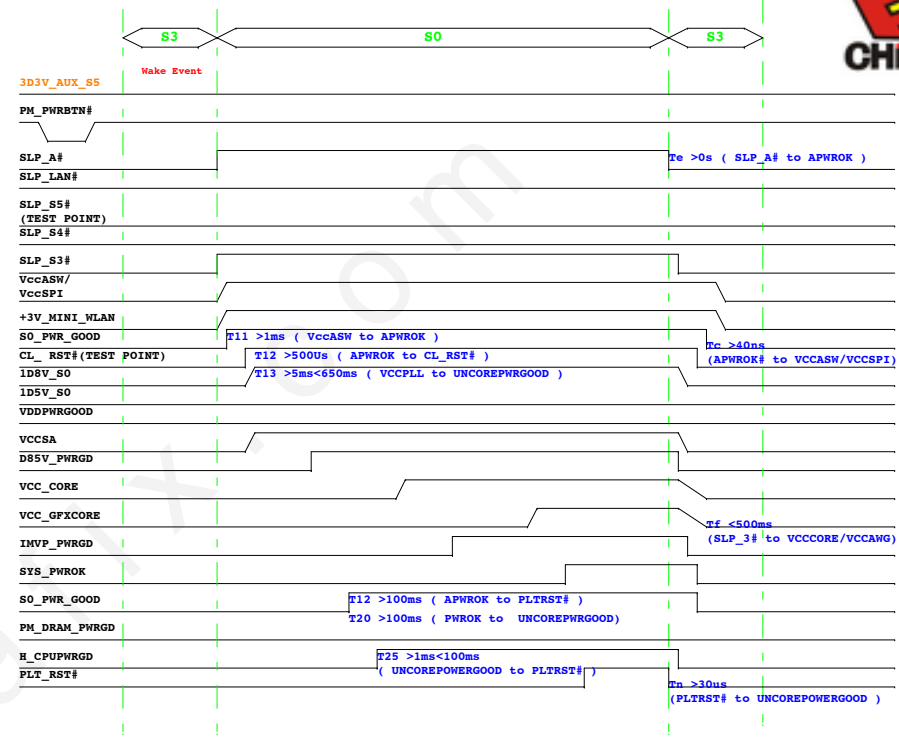
Size A4	Document Number <b>LA480</b>	Rev <b>SD</b>
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# Intel-Power Sequence (S5-to-S0-to-S5)



Intel PCH Pin Name	Main board PCH Pin Name
VccSUS (5V/3V )	3D3V_AUX_S5
PWRBTN#	PM_PWRBTN#
SLP_A#	SLP_A#
SLP_LAN#	SLP_LAN#
SLP_S5#	PM_SLP_S5#
SLP_S4#	PM_SLP_S4#
SLP_S3#	PM_SLP_S3#
VccASW/VccSPI	VccASW/VccSPI
Vcc_WLAN	+3V_MINI_WLAN
PWROK/APWROK	SO_PWR_GOOD
CL_RST#	CL_RST#
VCCPLL	ID8V_S0
VDDQ	ID5V_S0
VR_VDDQ/PWRGOOD	VDDPWRGOOD
VCCSA	VCCSA
IMVP7_VR_EN	D85V_PWRGD
VccCore	VCC_CORE
VccAXG	VCC_GFXCORE
IMVP7_PWRGD	IMVP_PWRGD
SYS_PWRGD	SYS_PWRGD
PWRGD	SO_PWR_GOOD
DRAMPWRGD	PM_DRAM_PWRGD
UNCOREPWRGOOD	H_CPUPWRGD
PLTRST#	PLT_RST#

# (S3-to-S0-to-S3)

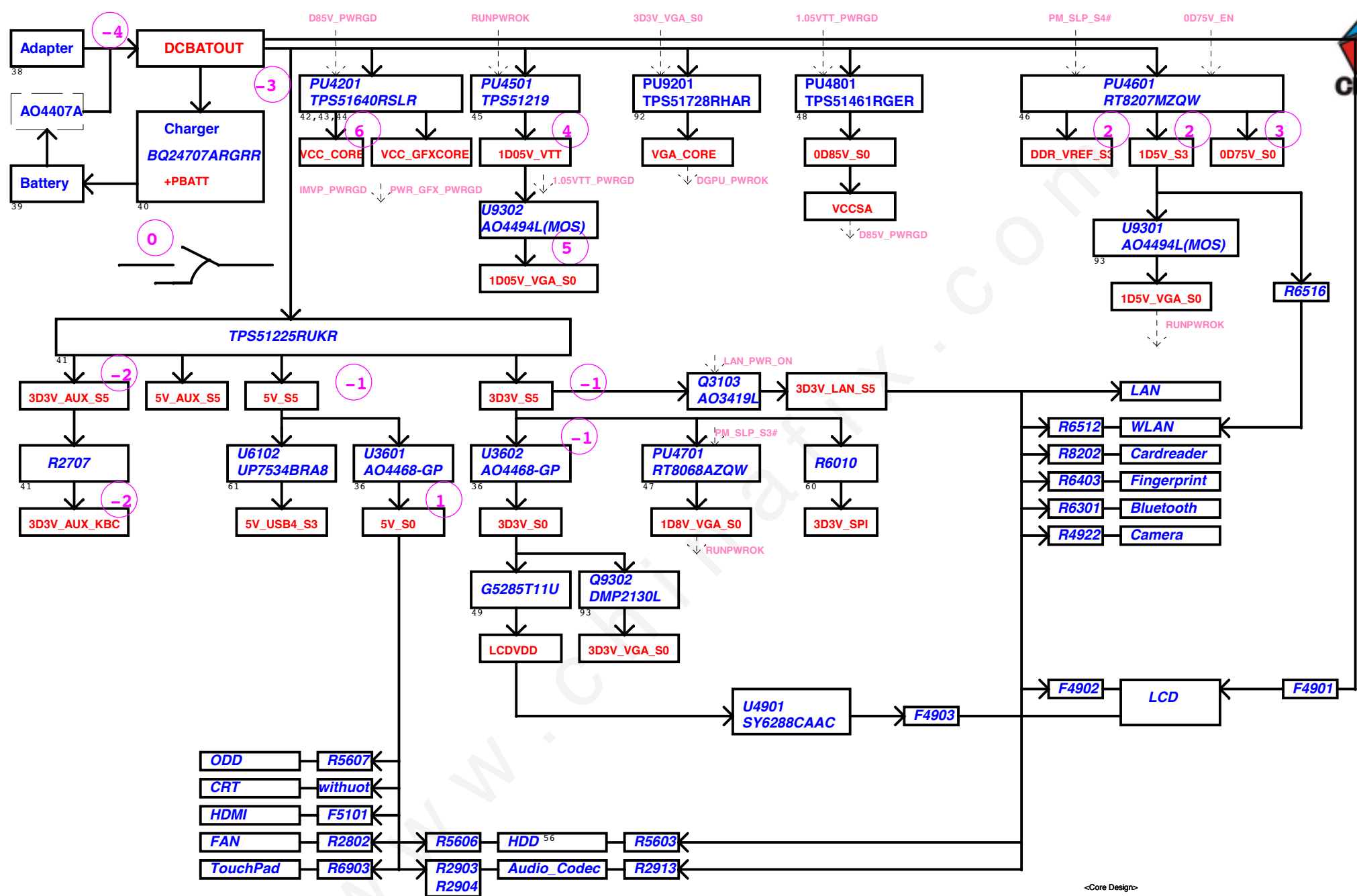


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Title	Change History		Rev
Size	Document Number:	LA480	SD
Date:	Friday, January 05, 2012	Sheet 99 of 103	



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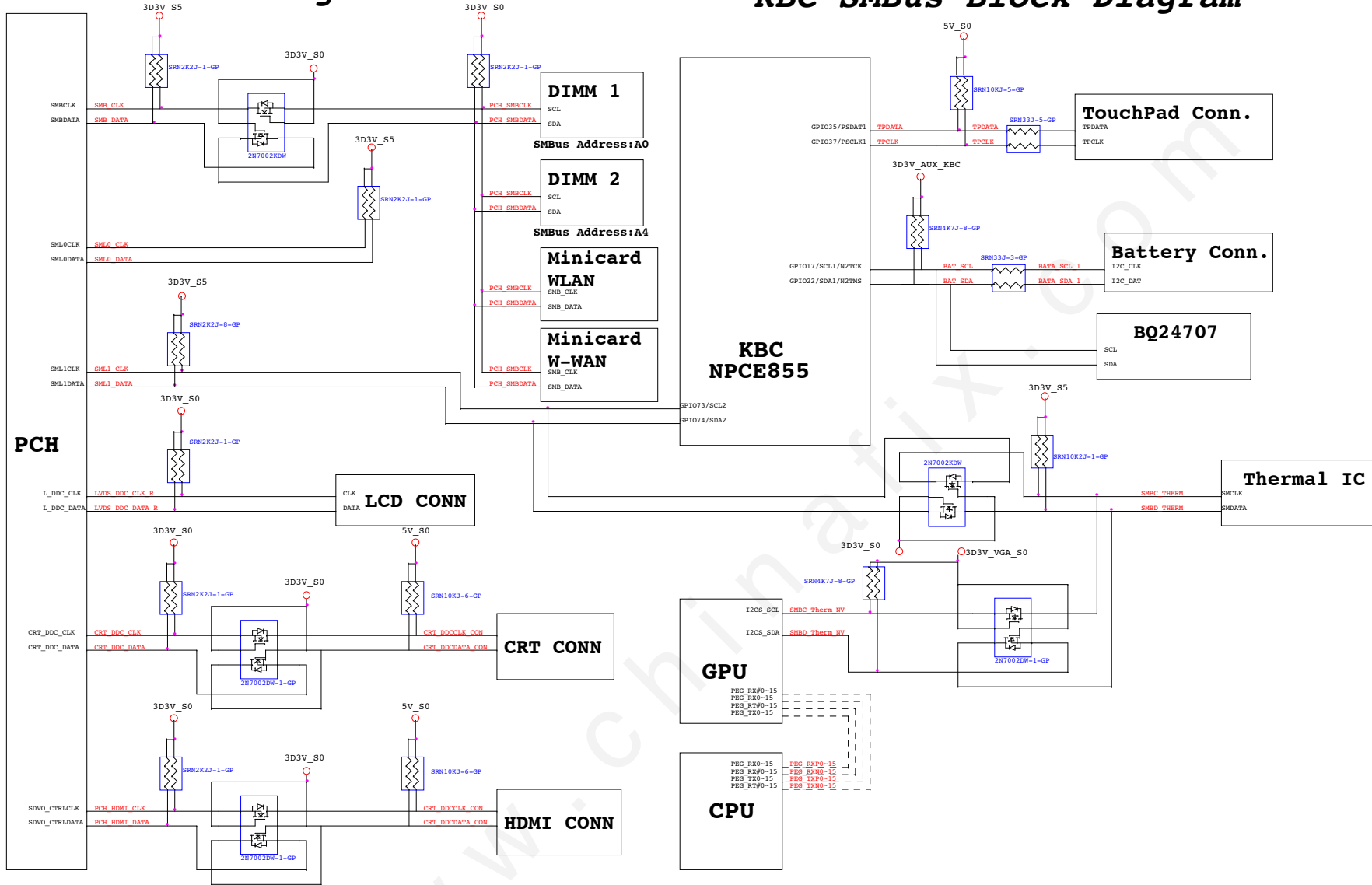
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Size: A3 Document Number: **LA480** Rev: **SD**

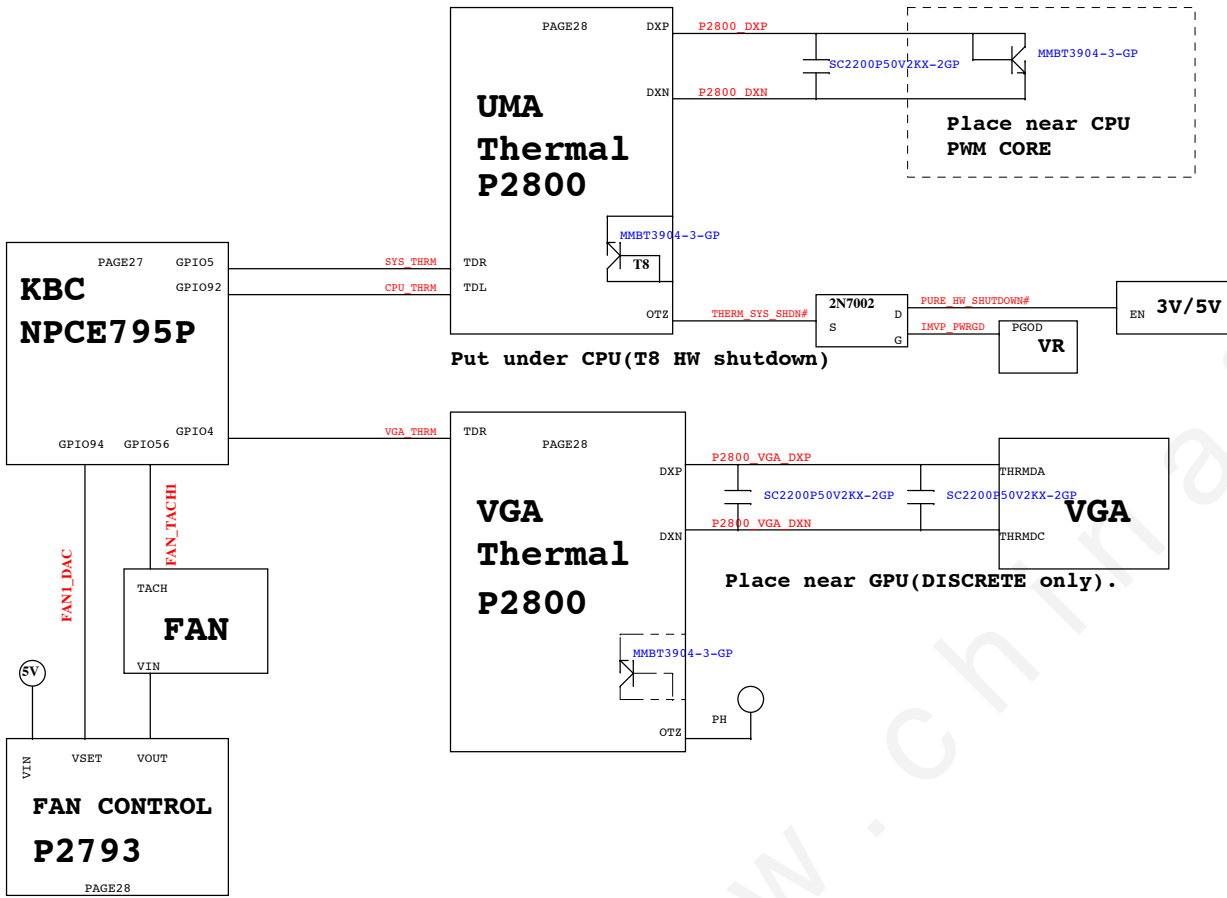
Date: Friday, January 06, 2012 Sheet: 100 of 103

# PCH SMBus Block Diagram

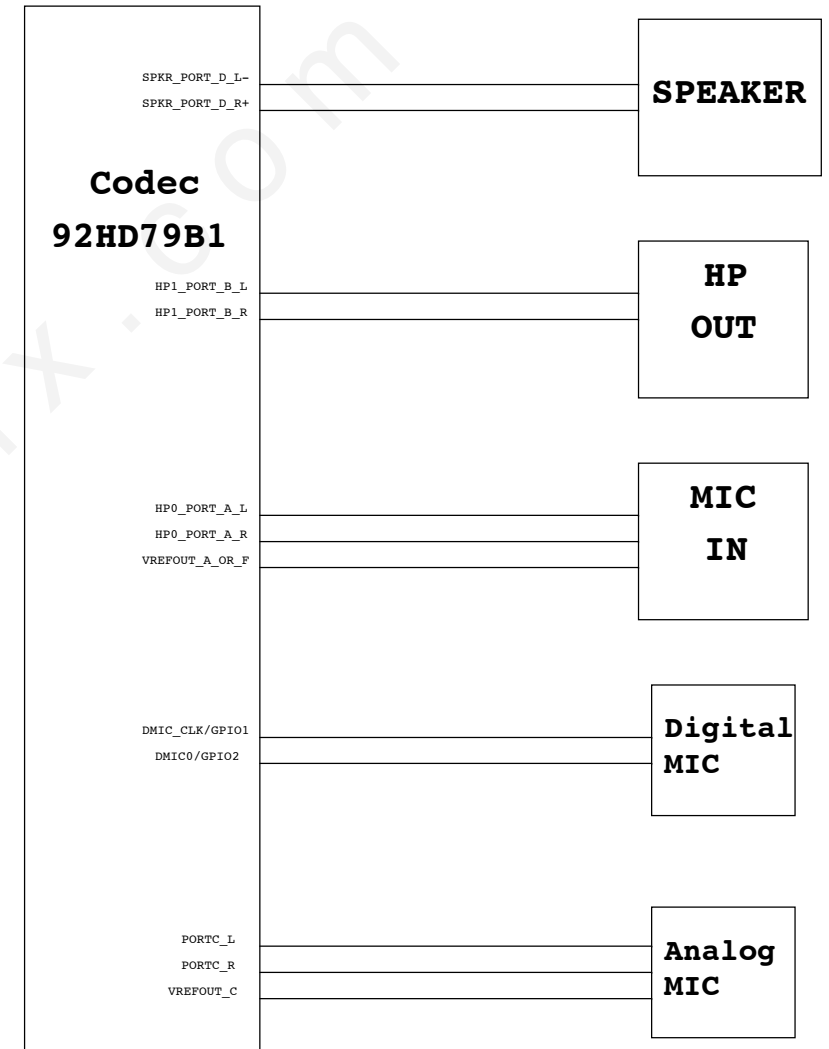
# KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title <b>Thermal/Audio Block Diagram</b>		
Size Custom	Document Number <b>LA480</b>	Rev <b>SD</b>
Date: Friday, January 06, 2012	Sheet 102 of	103

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Title **Change History**

Size A4	Document Number <b>LA480</b>	Rev <b>SD</b>
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