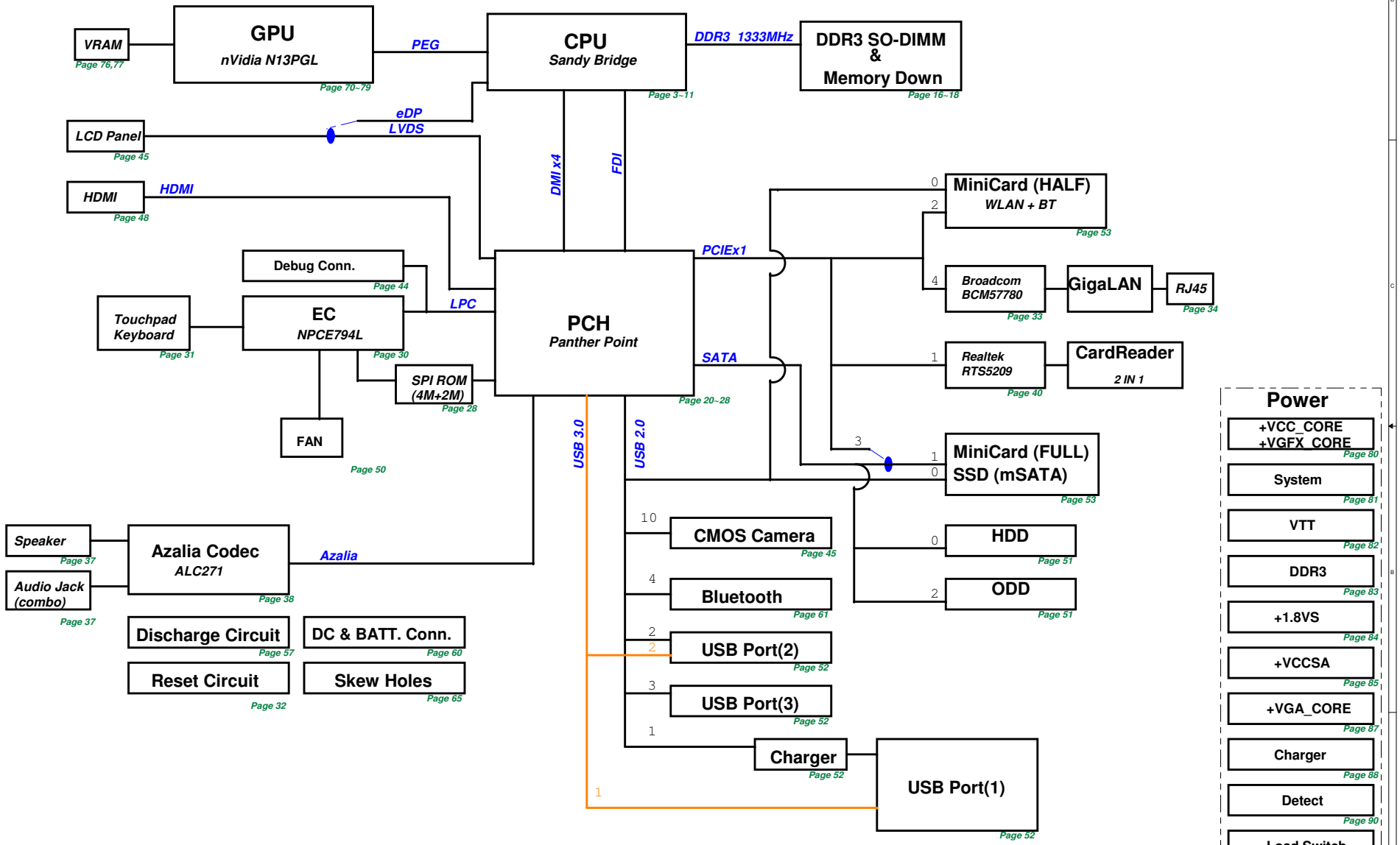
JM50 Ultrabook Block Diagram Rev 1.0



PEGATRON Title : Block Diagram

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 1 of 93

PCH_CPT GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
GPIO 37				
GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
GPIO 46				
GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

EC NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
GPG0		
GPG1		
GPG2		
GPG6		
GPH0		
GPH1		
GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

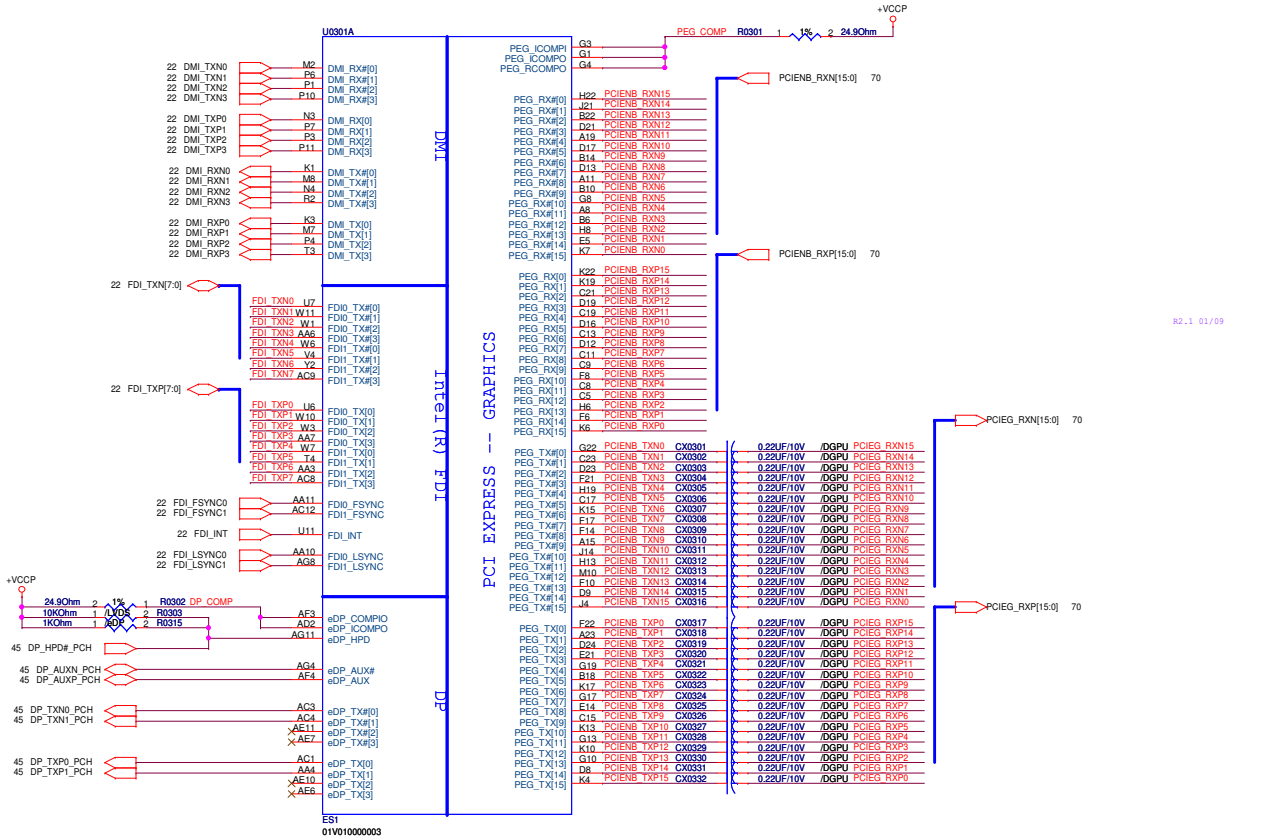
USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A

PEGATRON Title : System Setting

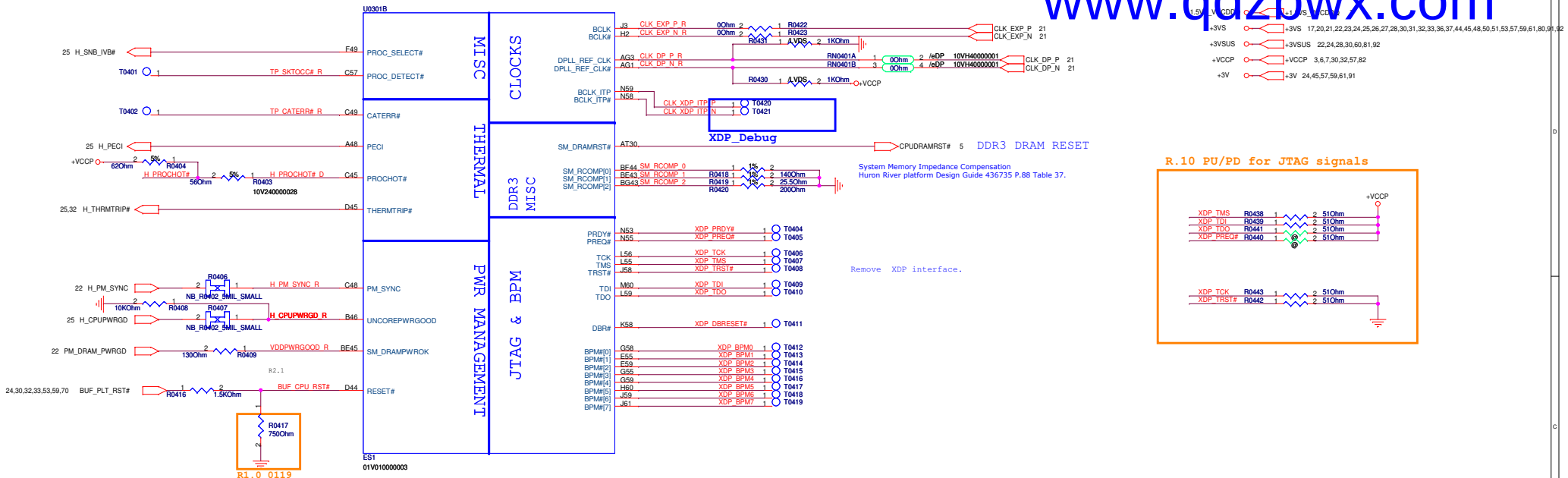
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 2 of 93



PEGATRON	Title : CPU(1)_DMI,DP,PEG,FDI	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 3 of 93	

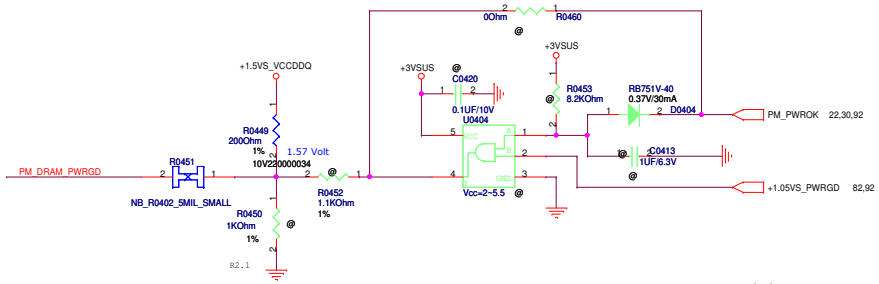


R1.0 0119
Sandy Bridge:R0417 = 750 ohm (10V220000093)
Ivy Bridge:R0417 = 680 ohm (10V240000041)

R.10 PU/PD for JTAG signals

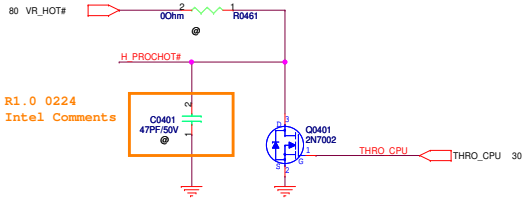
PM_SYS_PWRGD is the power good for +1.5V_VCCDQ

Different from EVEREST



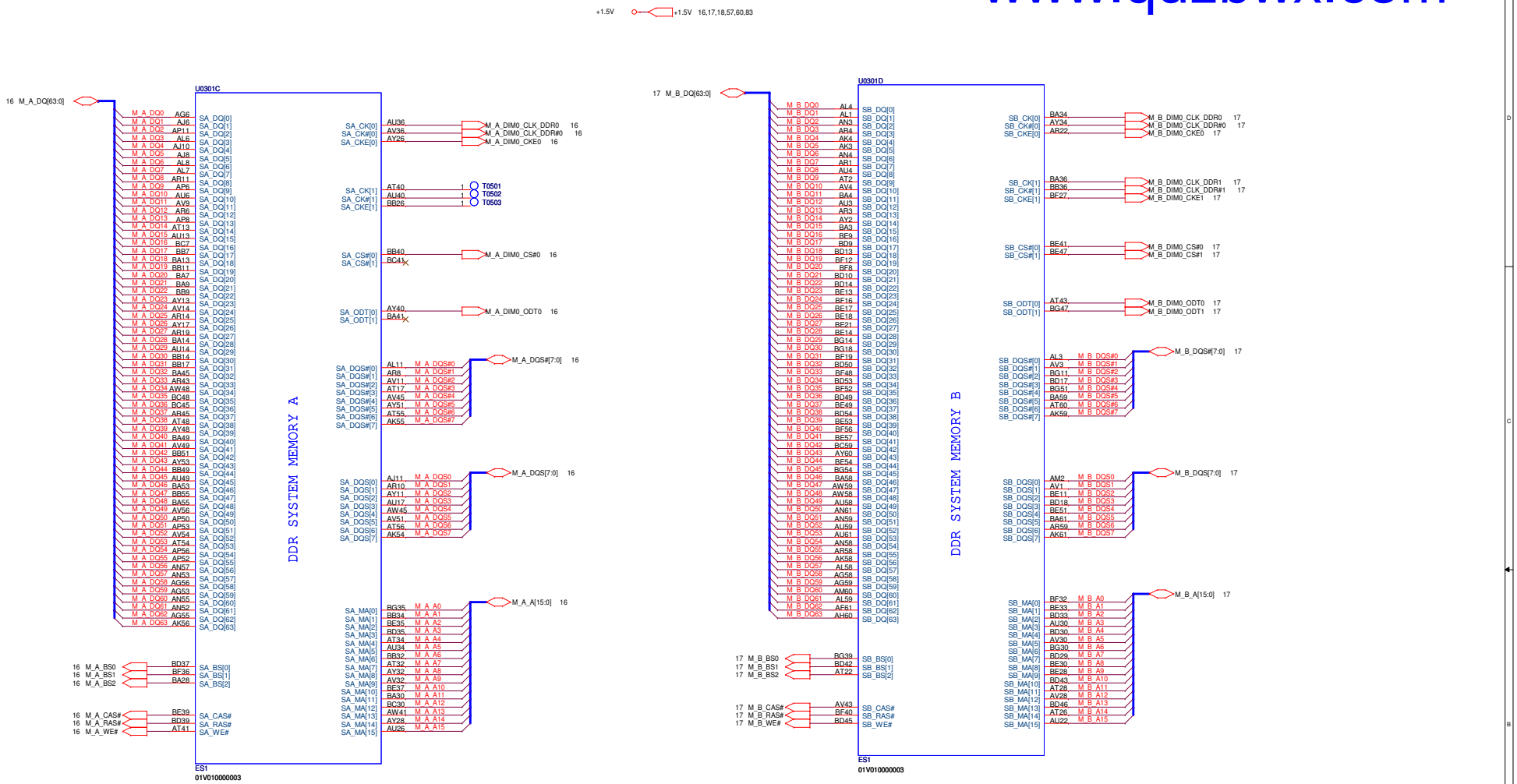
R1.1
add S3 power reduction

If support S3 power reduction with power good.
1. Mount U0404, D0404, C0413, C0420, R0450, R0452, R0453,
   Unmount R0460
2. Change R0449 to 1kohm from 200ohm, change R0409 to 0ohm from 130ohm - Design Guide 1.0 page 106

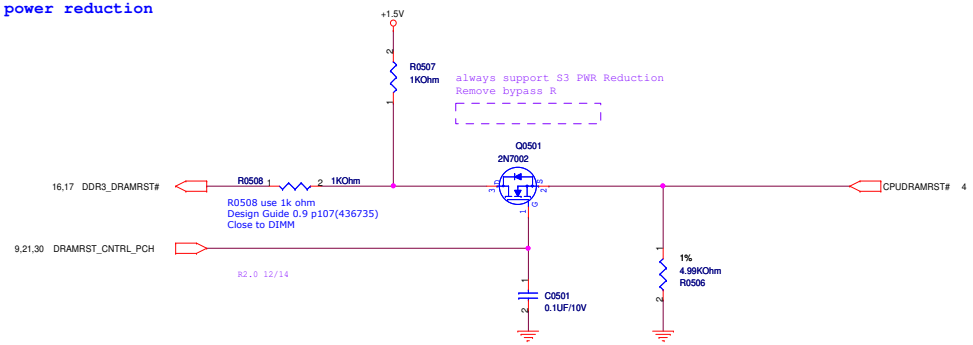


R1.0 0224
Intel Comments

PEGATRON Title : CPU(2)_CLK,MISC,JTAG
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 4 of 93



R1.0 S3 circuit: DRAM_RST# to memory should be high during S3
R1.1 add S3 power reduction

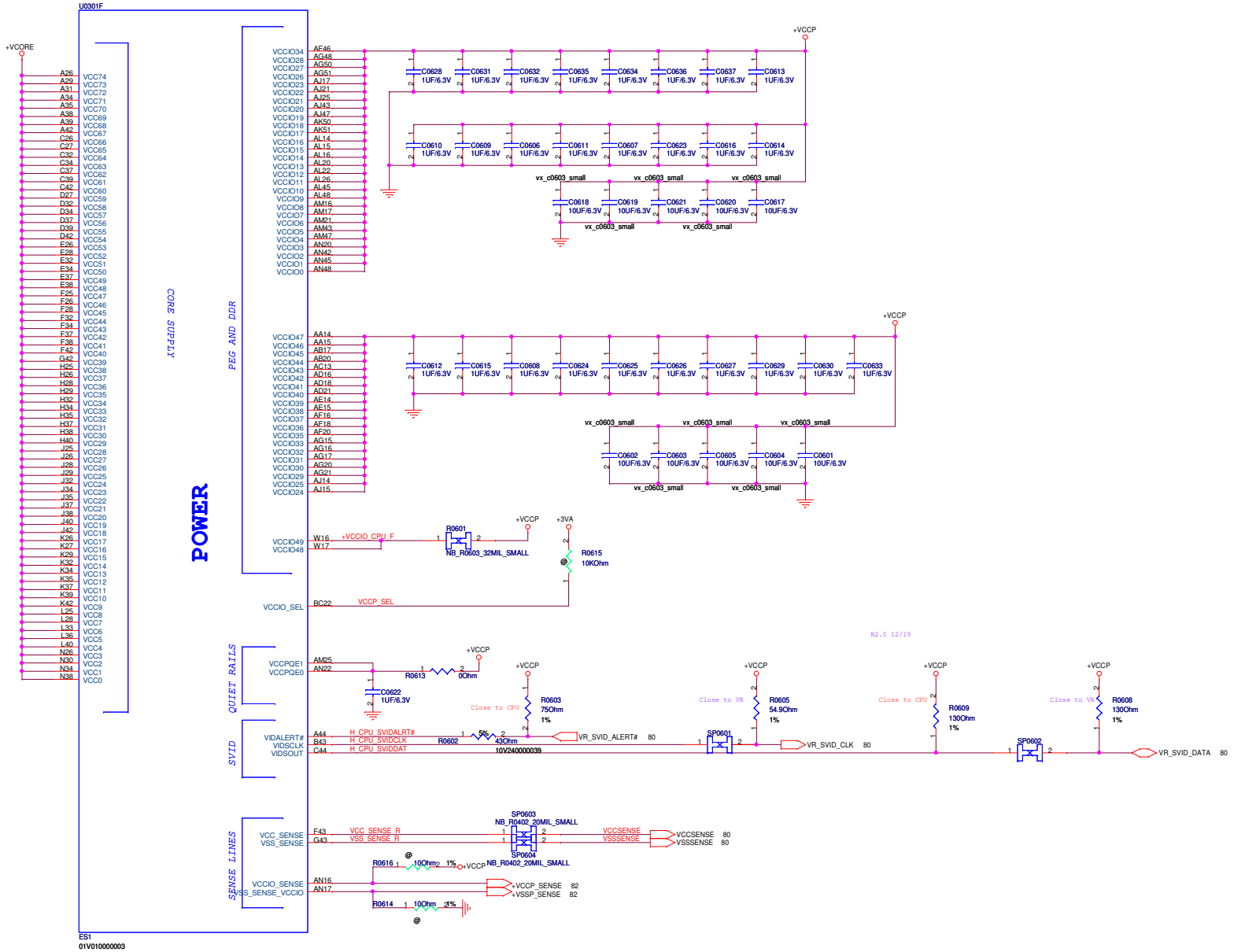


PEGATRON Title : CPU(3)_DDR3

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 5 of 93



PEGATRON	Title : CPU(4)_PWR	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 6 of 93	

Decoupling guide from Intel PDDG R0.8
+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 8pcs(power request)

+VCCP +VCCP 3,4,6,30,32,57,82
+1.5V +1.5V 5,16,17,18,57,60,83
+VCCSA +VCCSA 85
+1.8VS +1.8VS 25,26,57,80,84
+VGFX_CORE +VGFX_CORE 9,80
+1.5VS +1.5VS 26,53,57,91
+V_SM_VREF +V_SM_VREF 83

Graphics core voltage
Voltage range: 0 ~ 1.52V

+VGFX_CORE
C0725 1UF/6.3V C0727 1UF/6.3V C0731 1UF/6.3V C0726 1UF/6.3V C0732 1UF/6.3V C0729 1UF/6.3V C0730 1UF/6.3V C0728 1UF/6.3V
C0717 1UF/6.3V C0719 1UF/6.3V C0722 1UF/6.3V
vx_c0603_small: C0790 10UF/6.3V C0791 10UF/6.3V C0788 10UF/6.3V C0789 10UF/6.3V C0787 10UF/6.3V C0786 10UF/6.3V
vx_c0603_small: C0738 22UF/6.3V C0739 22UF/6.3V C0740 22UF/6.3V C0741 22UF/6.3V C0742 22UF/6.3V C0743 22UF/6.3V C0744 22UF/6.3V C0745 22UF/6.3V

U0301G

VAXG21 VAXG20 VAXG19 VAXG18 VAXG17 VAXG16 VAXG15 VAXG14 VAXG13 VAXG12 VAXG11 VAXG10 VAXG9 VAXG8 VAXG7 VAXG6 VAXG5 VAXG4 VAXG3 VAXG2 VAXG1 VAXG0 VAXG55 VAXG54 VAXG53 VAXG52 VAXG51 VAXG50 VAXG49 VAXG48 VAXG47 VAXG46 VAXG45 VAXG44 VAXG43 VAXG42 VAXG41 VAXG40 VAXG39 VAXG38 VAXG37 VAXG36 VAXG35 VAXG34 VAXG33 VAXG32 VAXG31 VAXG30 VAXG29 VAXG28 VAXG27 VAXG26 VAXG25 VAXG24 VAXG23 VAXG22

GRAPHICS

POWER

DDR3 - 1.5V RAILS

SM_VREF AY43 +V_SM_VREF
VDDQ25 AJ28 VDDQ24 AJ33 VDDQ23 AJ36 VDDQ22 AJ40 VDDQ21 AL30 VDDQ20 AL34 VDDQ19 AL38 VDDQ18 AL42 VDDQ17 AM33 VDDQ16 AM36 VDDQ15 AM40 VDDQ14 AN30 VDDQ13 AN34 VDDQ12 AN38 VDDQ11 AR26 VDDQ10 AR28 VDDQ9 AR30 VDDQ8 AR32 VDDQ7 AR34 VDDQ6 AR36 VDDQ5 AR40 VDDQ4 AV41 VDDQ3 AW26 VDDQ2 BA40 VDDQ1 BB28 VDDQ0 BG33

DDR3 Reference Voltage
+1.5VS_VCCDDQ
R1.1
add S3 power reduction
+V_SM_REF 10mil
R0703 1KOhm
R0710 1KOhm
C0794 0.1UF/10V

Processor I/O supply voltage for DDR3 (DC + AC specification)
MAX:5A
C0704 1UF/6.3V C0709 1UF/6.3V C0705 1UF/6.3V C0706 1UF/6.3V C0707 1UF/6.3V C0708 1UF/6.3V C0713 1UF/6.3V C0710 1UF/6.3V C0712 1UF/6.3V C0711 1UF/6.3V
+1.5VS_VCCDDQ +1.5VS JP0701 @ 3MM_OPEN_5MIL
ICCMAX_VDDQ 5A
vx_c0603_small: C0775 10UF/6.3V C0774 10UF/6.3V C0772 10UF/6.3V C0769 10UF/6.3V C0767 10UF/6.3V C0765 10UF/6.3V C0770 10UF/6.3V C0768 10UF/6.3V
CE0702 330UF/2V
R1.1
add S3 power reduction

Chief River

Decoupling guide from Intel (EE)
+1.5VS_VCCDDQ
1uF * 10pcs
10uF * 8pcs
330uF * 1pcs

SENSE LINES

SP0701 NB_R0402_20MIL_SMALL
80 VCCGT_SENSE
80 VSSGT_SENSE
SP0702 NB_R0402_20MIL_SMALL
VAXG_SENSE F45
VSSAXG_SENSE G45

PLL supply voltage
(DC + AC specification)
+1.8VS
MAX:1.2A
TDC: 1.2A
CE0701 330UF/2V C0761 1UF/6.3V C0764 1UF/6.3V
VCCPLL2 BB3 VCCPLL1 BC1 VCCPLL0 BC4

1.8V RAIL

QUIET RAILS

Filtered(BGA Only)
VCCDQ1 AM28 VCCDQ0 AN26
+1.5VS_VCCDDQ
R0707 0Ohm
C0714 1UF/6.3V

+VCCSA
MAX:10A
TDC: 6A
vx_c0603_small: C0783 10UF/6.3V C0781 10UF/6.3V C0792 10UF/6.3V C0777 10UF/6.3V C0793 10UF/6.3V
vx_c0603_small: C0735 1UF/6.3V C0736 1UF/6.3V C0733 1UF/6.3V C0734 1UF/6.3V C0737 1UF/6.3V
VCCSA15 L17 VCCSA14 L21 VCCSA13 N16 VCCSA12 N20 VCCSA11 N22 VCCSA10 P17 VCCSA9 P20 VCCSA8 R16 VCCSA7 R18 VCCSA6 R21 VCCSA5 U15 VCCSA4 V16 VCCSA3 V17 VCCSA2 V18 VCCSA1 V21 VCCSA0 W20

SA RAIL

SENSE LINES
VDDQ_SENSE BC43 VSS_SENSE_VDDQ BA43
T0701 T0702
VCCSA_SENSE U10
R0704 0Ohm Close to CPU
VCCSA_SENSE 85
VCCSA_VID[0] D48 VCCSA_VID[1] D49
VCCSA_SEL0 VCCSA_SEL1
VCCSA_SEL0 85 VCCSA_SEL1 85

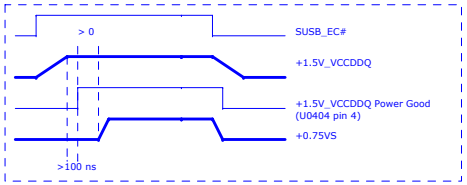
Chief River

R2.2, 03/05

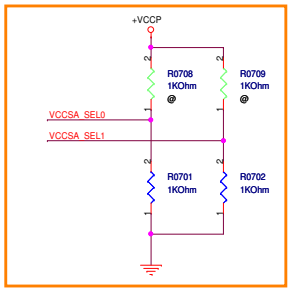
+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

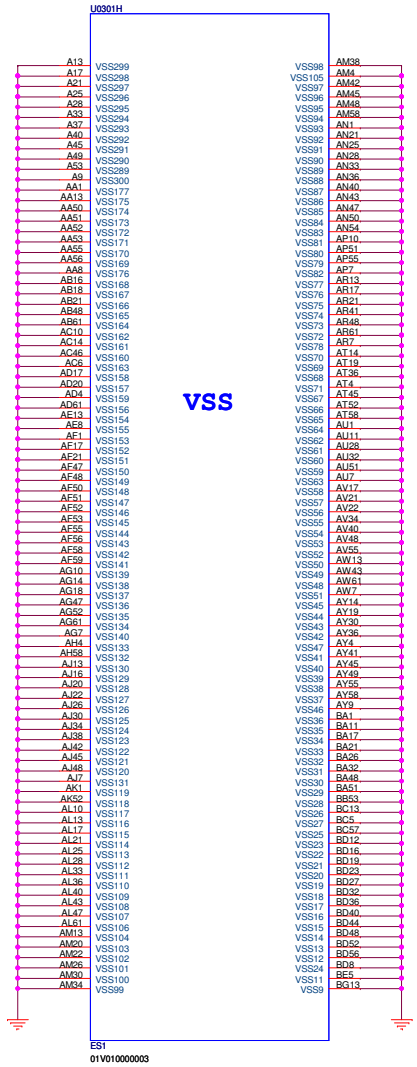
ES1
01V010000003

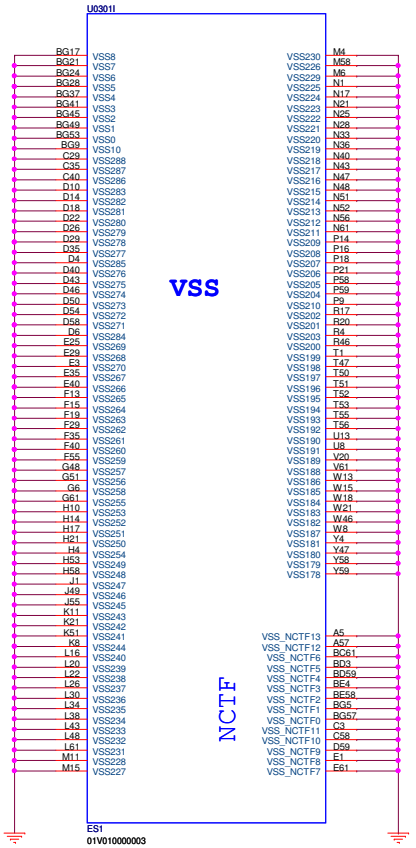


R1.0 0209
Intel Comments



PEGATRON Title : CPU(5)_GFX_PWR
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 7 of 93





PEGATRON	Title : CPU(6)_GND		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 8 of 93		

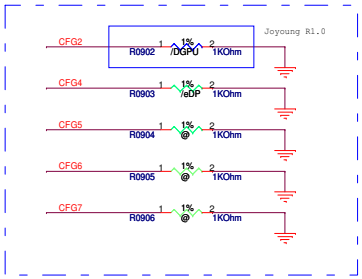
CFG strapping information:

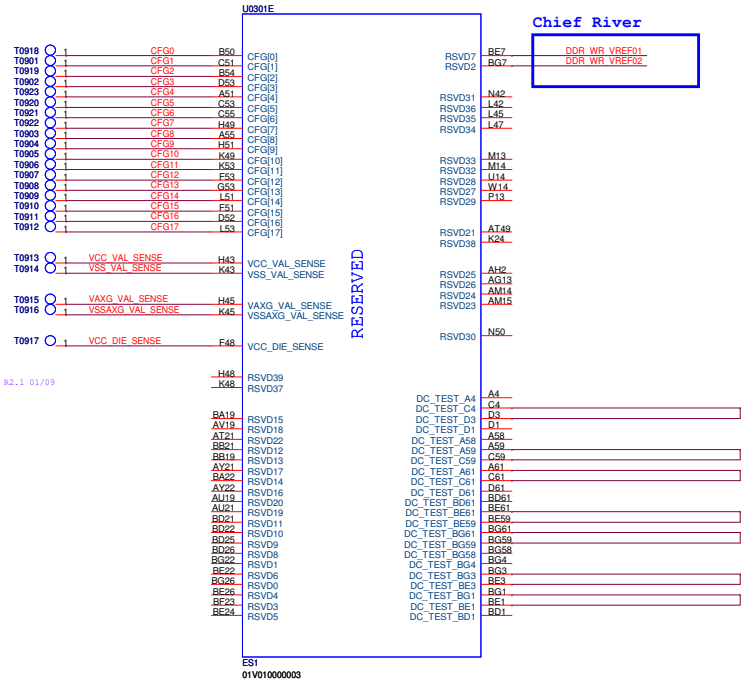
CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x
- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

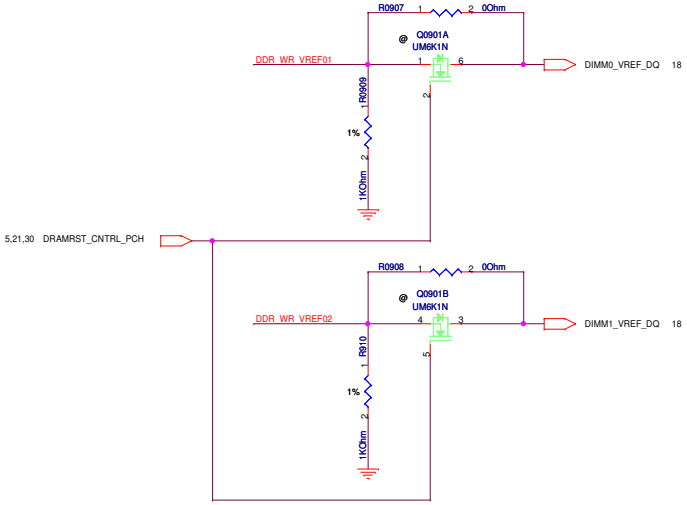
CFG[6:5]: PCI Express Port Bifurcation Straps
- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING
- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training



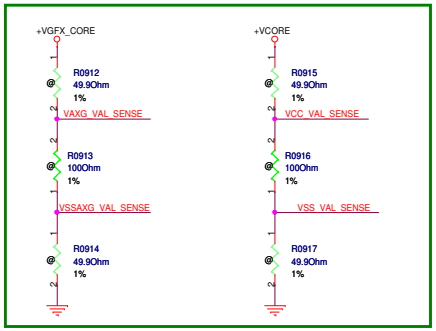


PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



For iFDIM testing
R0912~ R0917 close to pin < 1 inch

R1.1 0512



PEGATRON Title : CPU(7)_RSVD

BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 9 of 93

Check Connector

CPU XDP connector

PCH XDP connector

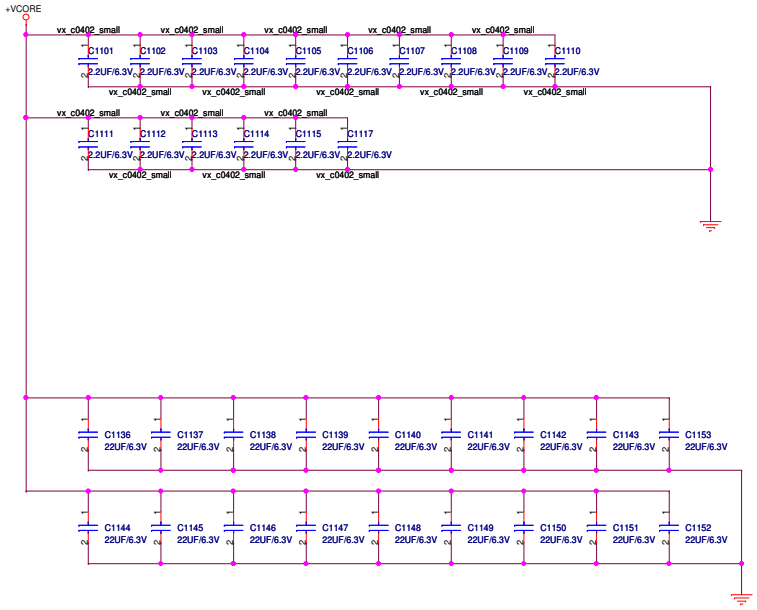
PEGATRON	Title : CPU_PCH_XDP		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 10 of 93		

Chief River

Decoupling guide from Intel PDDG R0.8
+VCORE 2.2uF * 16 pcs
22uF * 12 pcs

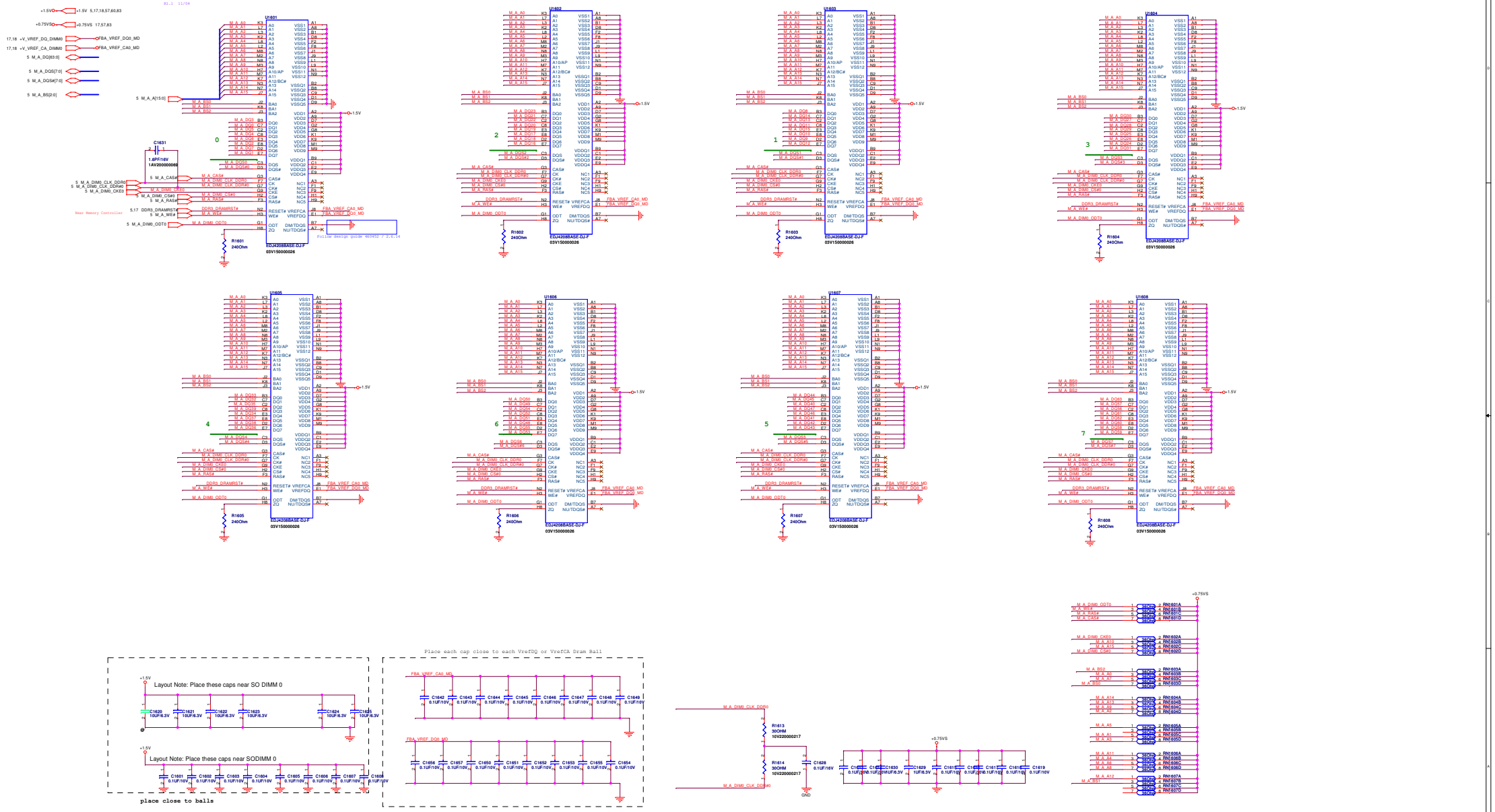
Chief River

+VCORE 2.2uF * 16 pcs
22uF * 18 pcs (power request)



PEGATRON	Title : CPU DECOUPLING	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 11 of 93	

Memory Down CH A



PEGATRON Title : DDR3(1) SO-DIMM0

SG1-HW RD Div.2-MB RD Dept.5 Engineer: Joyoung_Chienhg

Size: D | Project Name: JM50 | Rev: 3.1

Date: Thursday, August 23, 2012 | Sheet 16 of 93

+1.5V +1.5V 5,16,18,57,60,83

+0.75VS +0.75VS 16,57,83

+3VS +3VS 20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+V_VREF_CA_DIMM1 +V_VREF_CA_DIMM1 16,18

+V_VREF_DQ_DIMM1 +V_VREF_DQ_DIMM1 16,18

+1.5V CE1703 220UF/4V @

+1.5V Layout Note: Place these caps near SO DIMM 1

C1709 10UF/6.3V @ C1710 10UF/6.3V C1711 10UF/6.3V @ C1712 10UF/6.3V C1713 10UF/6.3V @ C1718 10UF/6.3V

+0.75VS C1716 1UF/6.3V C1717 1UF/6.3V C1719 1UF/6.3V @ C1730 1UF/6.3V

5 M_B_A[15:0]

M_B_DQ[63:0] 5

J1701A

M_B_A0 98 A0 | M_B_A1 97 A1 | M_B_A2 96 A2 | M_B_A3 95 A3 | M_B_A4 92 A4 | M_B_A5 91 A5 | M_B_A6 90 A6 | M_B_A7 86 A7 | M_B_A8 89 A8 | M_B_A9 85 A9 | M_B_A10 107 A10/AP | M_B_A11 84 A11 | M_B_A12 83 A12/BC# | M_B_A13 119 A13 | M_B_A14 80 A14 | M_B_A15 78 A15

M_B_DQ1 5 DQ0 | M_B_DQ5 7 DQ1 | M_B_DQ7 15 DQ2 | M_B_DQ2 17 DQ3 | M_B_DQ4 4 DQ4 | M_B_DQ0 6 DQ5 | M_B_DQ6 16 DQ6 | M_B_DQ3 18 DQ7 | M_B_DQ8 21 DQ8 | M_B_DQ12 23 DQ9 | M_B_DQ10 33 DQ10 | M_B_DQ15 35 DQ11 | M_B_DQ9 22 DQ12 | M_B_DQ13 24 DQ13 | M_B_DQ11 34 DQ14 | M_B_DQ14 36 DQ15 | M_B_DQ16 39 DQ16 | M_B_DQ20 41 DQ17 | M_B_DQ21 51 DQ18 | M_B_DQ17 53 DQ19 | M_B_DQ23 40 DQ20 | M_B_DQ22 42 DQ21 | M_B_DQ19 50 DQ22 | M_B_DQ18 52 DQ23 | M_B_DQ25 57 DQ24 | M_B_DQ28 59 DQ25 | M_B_DQ30 67 DQ26 | M_B_DQ26 69 DQ27 | M_B_DQ29 56 DQ28 | M_B_DQ24 58 DQ29 | M_B_DQ27 68 DQ30 | M_B_DQ31 70 DQ31 | M_B_DQ32 129 DQ32 | M_B_DQ33 131 DQ33 | M_B_DQ38 141 DQ34 | M_B_DQ34 143 DQ35 | M_B_DQ36 130 DQ36 | M_B_DQ37 132 DQ37 | M_B_DQ39 140 DQ38 | M_B_DQ35 142 DQ39 | M_B_DQ44 147 DQ40 | M_B_DQ40 149 DQ41 | M_B_DQ46 157 DQ42 | M_B_DQ41 159 DQ43 | M_B_DQ42 146 DQ44 | M_B_DQ45 148 DQ45 | M_B_DQ47 158 DQ46 | M_B_DQ43 160 DQ47 | M_B_DQ53 163 DQ48 | M_B_DQ52 165 DQ49 | M_B_DQ55 175 DQ50 | M_B_DQ54 177 DQ51 | M_B_DQ49 164 DQ52 | M_B_DQ48 166 DQ53 | M_B_DQ50 174 DQ54 | M_B_DQ51 176 DQ55 | M_B_DQ63 181 DQ56 | M_B_DQ61 183 DQ57 | M_B_DQ57 191 DQ58 | M_B_DQ59 193 DQ59 | M_B_DQ60 180 DQ60 | M_B_DQ56 182 DQ61 | M_B_DQ58 192 DQ62 | M_B_DQ62 194 DQ63

0~7 8~15 16~23 24~31 32~39 40~47 48~55 56~63

5 M_B_DIM0_CLK_DDR1 | 5 M_B_DIM0_CLK_DDR#1 | 5 M_B_DIM0_CLK_DDR0 | 5 M_B_DIM0_CLK_DDR#0 → CK1 102 | CK1# 104 | CK0 101 | CK0# 103

5 M_B_DIM0_CS#1 | 5 M_B_DIM0_CS#0 → S1# 121 | S0# 114

5 M_B_DIM0_ODT1 | 5 M_B_DIM0_ODT0 → ODT1 120 | ODT0 116

5 M_B_WE# | 5 M_B_RAS# | 5 M_B_CAS# → WE# 113 | RAS# 110 | CAS# 115

5 M_B_BS2 | 5 M_B_BS1 | 5 M_B_BS0 → BA2 79 | BA1 108 | BA0 109

5 M_B_DIM0_CKE1 | 5 M_B_DIM0_CKE0 → CKE1 74 | CKE0 73

SA1 201 | SA0 197

5 M_B_DQS[7:0] | 5 M_B_DQS#[7:0] → DQS7 188 | DQS#7 186 | DQS6 171 | DQS#6 169 | DQS5 154 | DQS#5 152 | DQS4 137 | DQS#4 135 | DQS3 64 | DQS#3 62 | DQS2 47 | DQS#2 45 | DQS1 29 | DQS#1 27 | DQS0 12 | DQS#0 10

DM7 187 | DM6 170 | DM5 153 | DM4 136 | DM3 63 | DM2 46 | DM1 28 | DM0 11

SCL 202 | SDA 200 | RESET# 30 → DDR3_DRAMRST# 5,16

M_B_DIM0_CLK_DDR0 — C1720 10PF/50V @ — 150Ohm R1707 — M_B_DIM0_CLK_DDR#0

M_B_DIM0_CLK_DDR1 — C1721 10PF/50V @ — 150Ohm R1708 — M_B_DIM0_CLK_DDR#1

PLACE CLOSE TO SODIMM

SMBus Slave Address: A4H

+3VS R1709 SP1703 2.10KOhm

take care if can't boot or S3 issue

DM should connect to GND directly
Design Guide 1.0 P.88 (436735)

28,53,59 SMB_CLK_S — SP1701 R0402 SMB_CLK_S_CHB

28,53,59 SMB_DAT_S — SP1702 R0402 SMB_DAT_S_CHB

DDR3_DIMM_204P
12V02GBRM000

H:5.2mm

+1.5V C1705 0.1UF/16V C1706 0.1UF/16V

Layout Note: Place these caps near SO DIMM 1

J1701B

VDD1 75 | VDD3 81 | VDD5 87 | VDD7 93 | VDD9 99 | VDD11 105 | VDD13 111 | VDD15 117 | VDD17 123

VDD2 76 | VDD4 82 | VDD6 88 | VDD8 94 | VDD10 100 | VDD12 106 | VDD14 112 | VDD16 118 | VDD18 124

+1.5V C1707 0.1UF/16V C1708 0.1UF/16V

VSS1 2 | VSS3 8 | VSS5 13 | VSS7 19 | VSS9 25 | VSS11 31 | VSS13 37 | VSS15 43 | VSS17 48 | VSS19 54 | VSS21 60 | VSS23 65 | VSS25 71 | VSS27 127 | VSS29 133 | VSS31 138 | VSS33 144 | VSS35 150 | VSS37 155 | VSS39 161 | VSS41 167 | VSS43 172 | VSS45 178 | VSS47 184 | VSS49 189 | VSS51 195

VSS2 3 | VSS4 9 | VSS6 14 | VSS8 20 | VSS10 26 | VSS12 32 | VSS14 38 | VSS16 44 | VSS18 49 | VSS20 55 | VSS22 61 | VSS24 66 | VSS26 72 | VSS28 128 | VSS30 134 | VSS32 139 | VSS34 145 | VSS36 151 | VSS38 156 | VSS40 162 | VSS42 168 | VSS44 173 | VSS46 179 | VSS48 185 | VSS50 190 | VSS52 196

GND1 207 | GND2 208

T1701 PM_EXTTS#0_DIM_B — Reserve

EVENT# 198 | TEST 125 | NC1 77 | NC2 122

NP_NC1 205 | NP_NC2 206

VTT1 203 | VTT2 204 → +0.75VS

+V_VREF_CA_DIMM1 — C1724 2.2UF/6.3V @ — C1723 0.1UF/16V

+V_VREF_DQ_DIMM1 — C1722 2.2UF/6.3V @ — C1725 0.1UF/16V

VREFCA 126 | VREFDQ 1

VDDSPD 199

+3VS C1715 0.1UF/16V C1714 2.2UF/6.3V @

Frank
20110513 VREFCA and VREFDQ need to separate
It follow EVEREST and Intel spec.

DDR3_DIMM_204P
12V02GBRM000

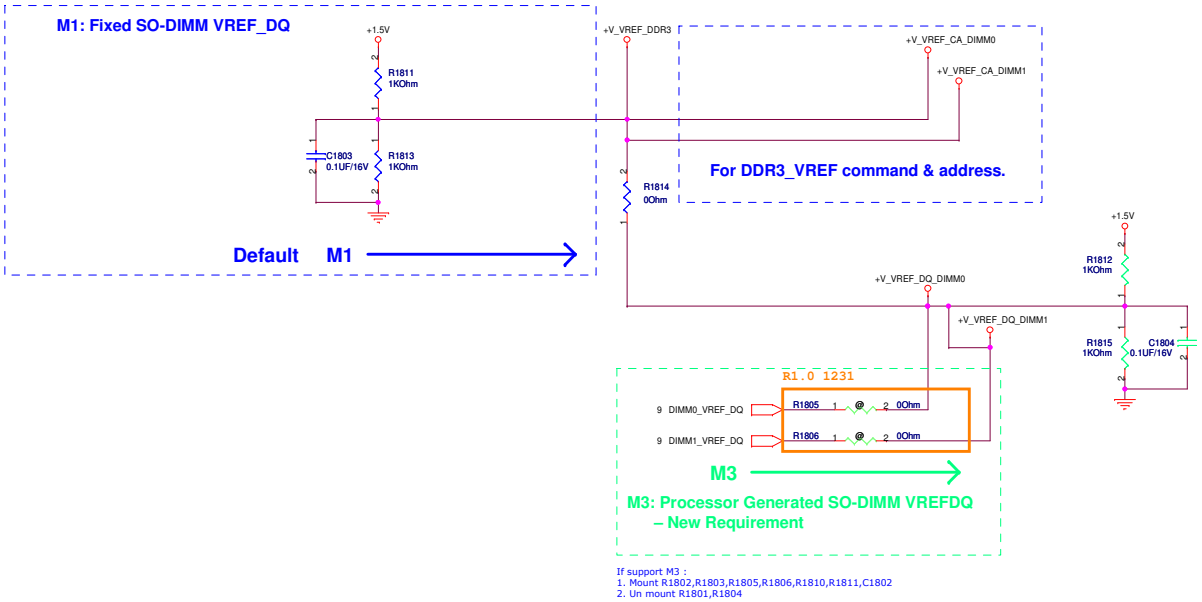
PEGATRON Title : DDR3(2)_SO-DIMM1

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 17 of 93

DDR3 Vref



If support M3 :
1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804

PEGATRON	Title : DDR3(3)_CA/DQ Voltage	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 18 of 93	

R1.4--2

PEGATRON Title : VID Controller

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 19 of 93

RTC battery

PR2.1

+3VA, T2030, +VCC_RTC, D2002, +RTCBAT, R2001 1KOhm, +RTC_BAT, 59,60 +RTCBAT, 1V/0.2A, C2003 1UF/10V, GND

Request by CSC for CMOS clear function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

+VCC_RTC RTCRST# RC delay should be 18ms~25ms

R2003 20KOhm 5%, C2004 1UF/10V, JRST2001 SGL_JUMP @, GND

R2004 20KOhm 5%, R2005 1MOhm, C2005 1UF/10V, JRST2002 SGL_JUMP @, GND

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

PCH_INTVRMEN R2030 @ 1% 200KOhm GND

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Intel 1.5 Design Guide, page 260

isolate schematic for ACZ _SYNC and SDOUT follow EIH31

R1.0
For JTAG to pull high and low.

Remove JTAG schematic

+VCC_RTC +VCC_RTC 22,27 — R1.0 Delete +RTCBAT
+3VA +3VA 6,26,27,30,31,57,59,60,81,88,93
+3VS +3VS 17,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3VSUS_ORG +3VSUS_ORG 21,22,24,25,26,27,33
+VTT_PCH_VCCIO +VTT_PCH_VCCIO 26,27

C2001 15PF/50V, X2001 32.768KHZ, SP2005, R2002 10MOhm, C2002 15PF/50V, T2015, T2012

20110718 Frank add C2006 for EMI request
+VCC_RTC 330KOhm C2006 @ 1% 33PF/50V R2006 GND

U2001A

RTC_X1	A20	RTCX1	RTC	
RTC_X2	C20	RTCX2		
RTC_RST#	D20	RTCRST#		
SRTC_RST#	G22	SRTCRST#		
SM_INTRUDER#	K22	INTRUDER#		
PCH_INTVRMEN	C17	INTVRMEN		
ACZ_BCLK	N34	HDA_BCLK	IHDA	
ACZ_SYNC	L34	HDA_SYNC		
	T10	SPKR		
ACZ_RST#	K34	HDA_RST#		
	E34	HDA_SDIN0		
Remove TP	G34	HDA_SDIN1		
ACZ_SDIN2_AUD	C34	HDA_SDIN2		
ACZ_SDIN3_AUD	A34	HDA_SDIN3		
ACZ_SDOUT	A36	HDA_SDO		
HDA_DOCK_EN#	C36	HDA_DOCK_EN#/GPIO33		
CARDREADER_RESET	N32	HDA_DOCK_RST#/GPIO13		
PCH_JTAG_TCK_BUF	J3	JTAG_TCK	JTAG	
PCH_JTAG_TMS	H7	JTAG_TMS		
PCH_JTAG_TDI	K5	JTAG_TDI		
PCH_JTAG_TDO	H1	JTAG_TDO		
SPI_CLK	T3	SPI_CLK	SPI	
SPI_CS0#	Y14	SPI_CS0#		
SPI_CS1#	T1	SPI_CS1#		
SPI_MOSI	V4	SPI_MOSI		
SPI_MISO	U3	SPI_MISO		

COUGAR_POINT_ES1
02V000000001

FWH0/LAD0	C38	LPC	LPC_AD0 30,44,59	
FWH1/LAD1	A38		LPC_AD1 30,44,59	
FWH2/LAD2	B37		LPC_AD2 30,44,59	
FWH3/LAD3	C37		LPC_AD3 30,44,59	
FWH4/LFRAME#	D36		LPC_FRAME# 30,44,59	
LDRQ0#	F36		SNN_PCH_DRQ#0 T2032	R1.0
LDRQ1#/GPIO23	K36		SNN_LPC_DRQ#1 T2033	
SERIRQ	V5		Serial Interrupt Request — INT_SERIRQ 30,44,59	
SATA0RXN	AM3	SATA 6G	SATA_RXN0 51	HDD1
SATA0RXP	AM1		SATA_RXP0 51	
SATA0TXN	AP7		SATA_TXN0 51	
SATA0TXP	AP5		SATA_TXP0 51	
SATA1RXN	AM10		SATA_RXN1 53	HDD2
SATA1RXP	AM8		SATA_RXP1 53	
SATA1TXN	AP11		SATA_TXN1 53	
SATA1TXP	AP10		SATA_TXP1 53	
SATA2RXN	AD7	SATA	SATA_RXN2 51	ODD
SATA2RXP	AD5		SATA_RXP2 51	
SATA2TXN	AH5		SATA_TXN2 51	
SATA2TXP	AH4		SATA_TXP2 51	
SATA3RXN	AB8			mSATA
SATA3RXP	AB10			
SATA3TXN	AF3			
SATA3TXP	AF1			
SATA4RXN	V7			
SATA4RXP	Y5			
SATA4TXN	AD3			
SATA4TXP	AD1			
SATA5RXN	Y3			
SATA5RXP	Y1			
SATA5TXN	AB5			
SATA5TXP	AB1			
SATAICOMPO	Y11			
SATAICOMPI	Y10		SATA_COMP R2007 1% 37.4Ohm +VTT_PCH_VCCIO	
SATA3RCOMPO	AB12			
SATA3COMPI	AB13		SATA3_COMP R2047 1% 49.9Ohm +VTT_PCH_VCCIO	
SATA3RBIAS	AH1		RBIAS_SATA3 R2048 1% 750Ohm GND	
SATALED#	P3		R2025 10KOhm +3VS; SATA_LED#	
SATA0GP/GPIO21	V14		SATA0GP T2034	
SATA1GP/GPIO19	P1		BBS_BIT0 24	

R1.0

R1.1 11/04

28 SPI_CLK, 28 SPI_CS#0, 28 SPI_CS#1 (SPI_CS#1), 28 SPI_SI, 28 SPI_SO

36 ACZ_BCLK_AUD, 36 ACZ_SYNC_AUD, 36 SB_SPKR, 36,37 ACZ_RST#_AUD, 36 ACZ_SDIN0_AUD, T2021, T2022, R1.1 10/31 IOAC 36 ACZ_SDOUT_AUD, T2001, T2002, T2004, T2005, T2006, T2007

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High:Enable
SB_SPKR R2020 @ 1KOhm +3VS

ACZ_SDOUT:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2.ACZ_SDOUTwhich sample high on the rising edge of PWROK
Will also disable Intel ME.
ACZ_SDOUT R2034 @ 1KOhm +3VSUS_ORG

ACZ_SYNC: On Die PLL VR voltage selector
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hrron River Platform Schematic Design Checklist (438390 page 48)
ACZ_SYNC R2036 1KOhm +3VSUS_ORG
VCCVRAM use +1.5VS in mobile

Pull High
+3VS
INT_SERIRQ R2026 10KOhm
SATA0GP R2027 10KOhm

PEGATRON COMPUTER INC
Title : PCH(1)_SATA,IHDA,RTC,LPC
Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 20 of 93

Frank
0513_Add USB3.0 and Card Reader PCIE and CLKRQ

Frank
0517_Add 3G PCIE and CLKRQ in Port3.

+3VS +3VS 17,20,22,23,24,25,26,27,28,30,...,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+VTT_PCH_ORG +VTT_PCH_ORG 22,26,27
+3VSUS_ ORG +3VSUS_ORG 20,22,24,25,26,27,33

Joyoung R1.0

U2001B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

COUGAR_POINT_ES1

R1.1
remove /niAMT remark

R1.1
S3 RAM reset CTRL

To EC

Joyoung R1.0
modify CLK_REQ

25-MHz is required in:
1. FCIM
2. BTM for PCH Display Clock gereration in Integrated Graphics platforms

CLOCK TERMINATION for FCIM
Default power-on mode is ICC.

PCH CLKREQ Setting:
Not connected to device.
R1.0 0118

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.
Eric Fang to Alan Chien on 11/15/2010

Remove XDP.

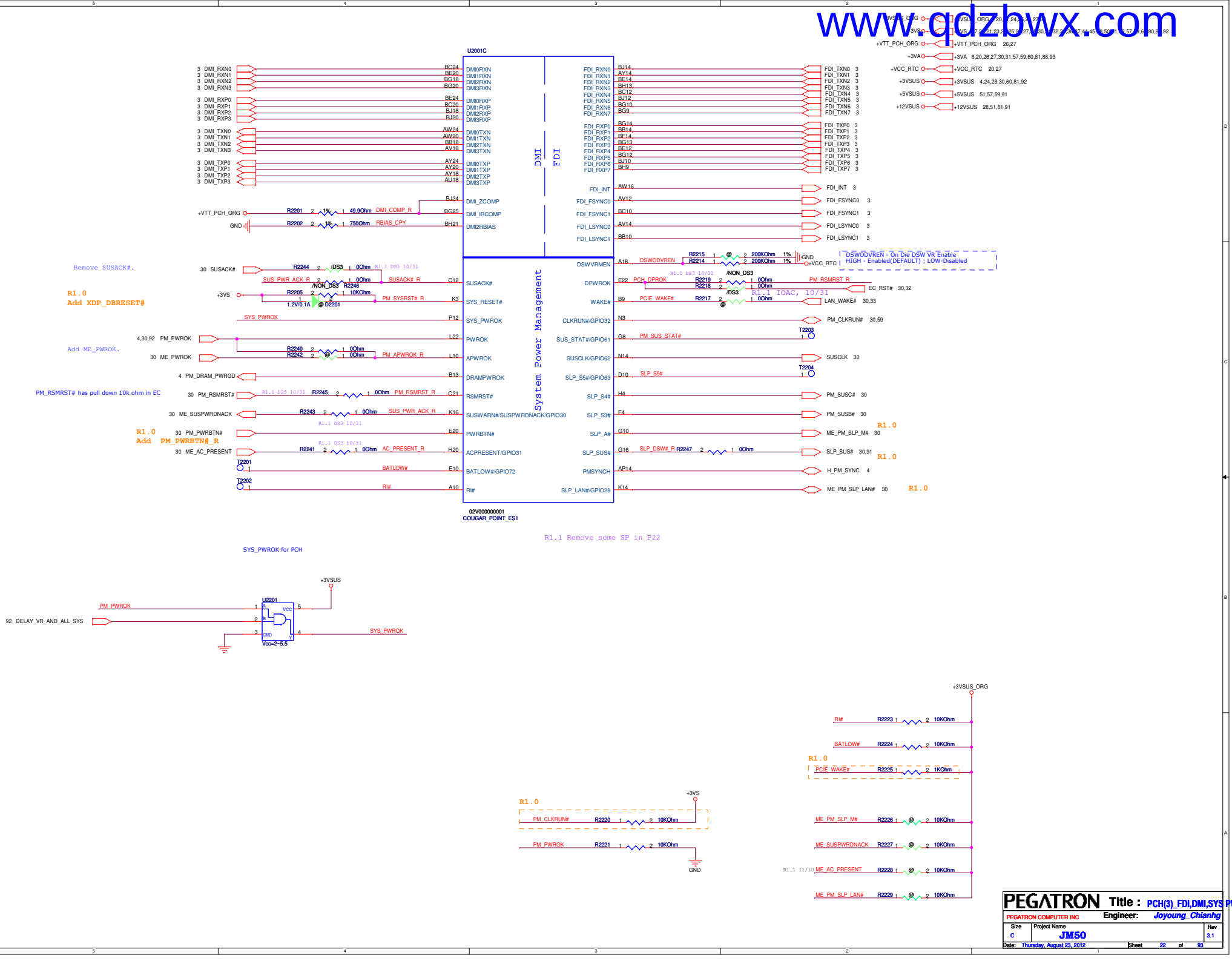
R2.0
Modify RAM Strap PIN

Joyoung R2.0
add GPIO Table for on board RAM Strap

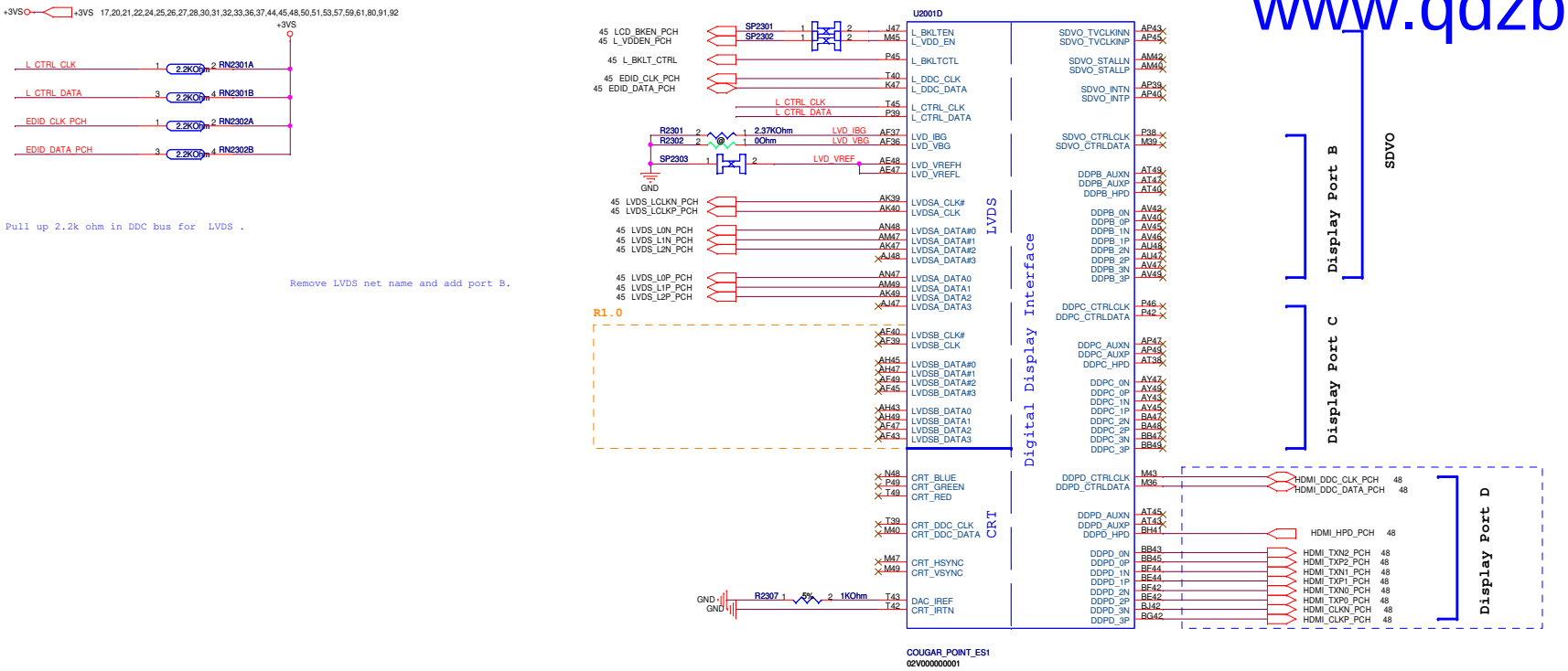
On Board RAM Setting

GPIO67 GPIO66 GPIO65 GPIO64	On Board RAM Setting
0000	No on board RAM
0001	Micron 1333MHz 4GB
0010	Elpida 1333MHz 4GB
0110	Elpida 1333MHz 2GB
0101	Micron 1333MHz 2GB
0100	Hynix 1333MHz 2GB
XXXX	TBD
1000	Common Definition 1333MHz 4GB
1001	Common Definition 1600MHz 4GB
0111	Elpida 1600MHz 2GB

PEGATRON Title : PCH(2)_PCIE,CLK,SMB,PEG
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 21 of 93



PEGATRON	Title :	PCH(3)_FDI,DMI,SYS PWR	
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg	
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 22 of 93		



CRT Disable: (For discrete graphic)

1. NC:
   CRT_RED,CRT_GREEN,CRT_BLUE
   CRT_HSYCN,CRT_VSYNC
2. 1-kΩ ±0.5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

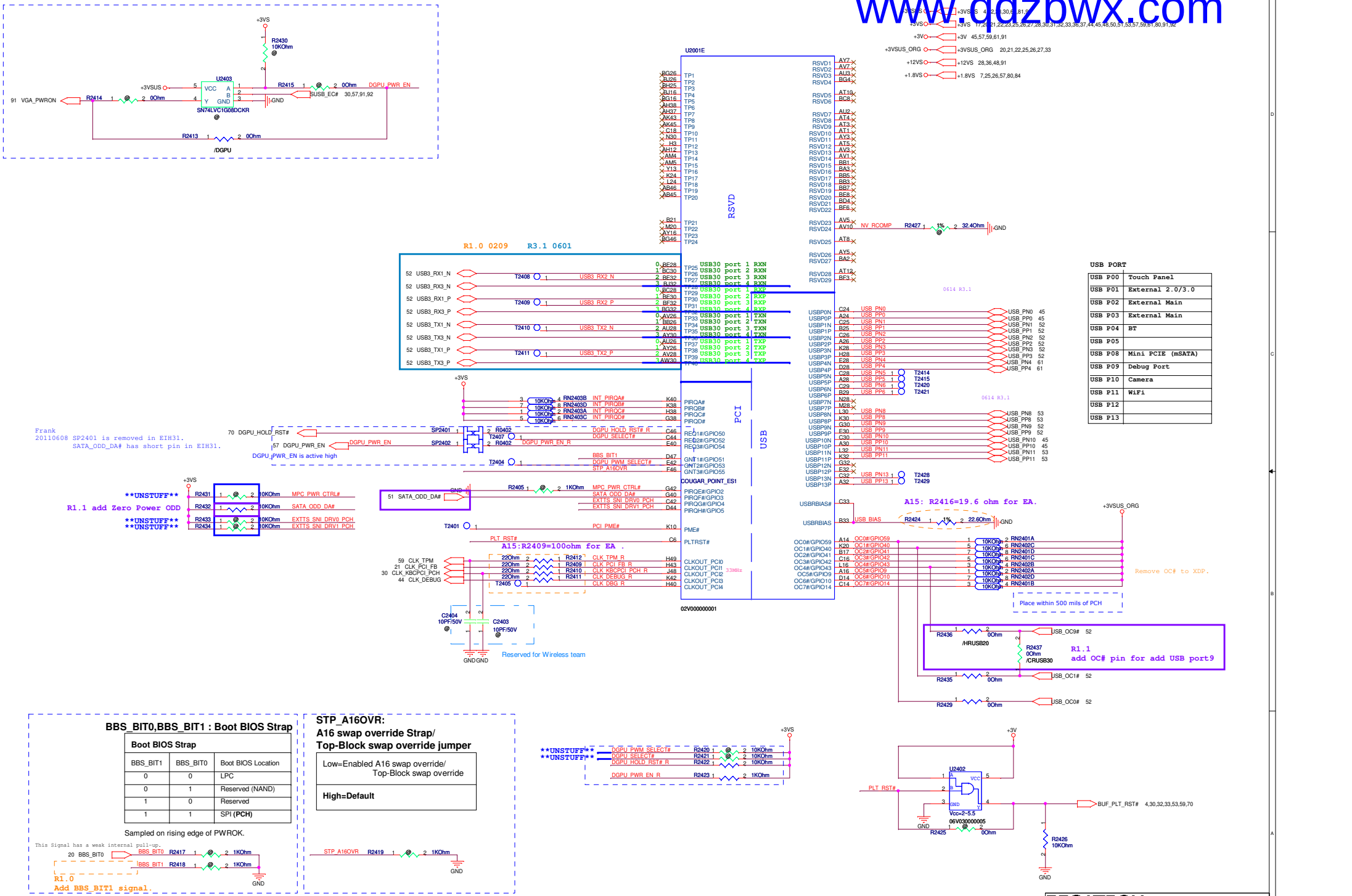
DisPlay Port Disable: (For discrete graphic)

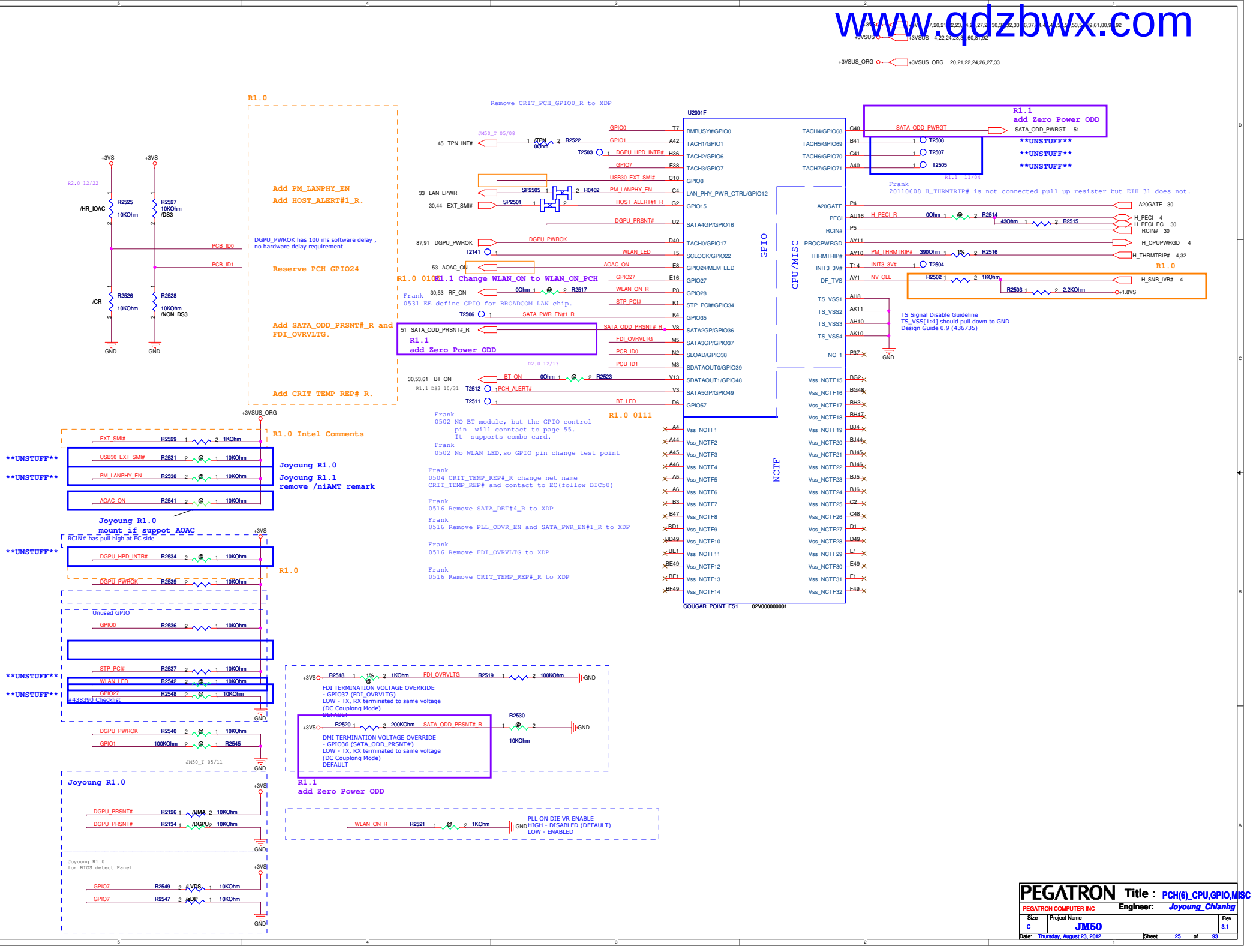
1. NC:
   ALL

LVDS Disable: (For discrete graphic)

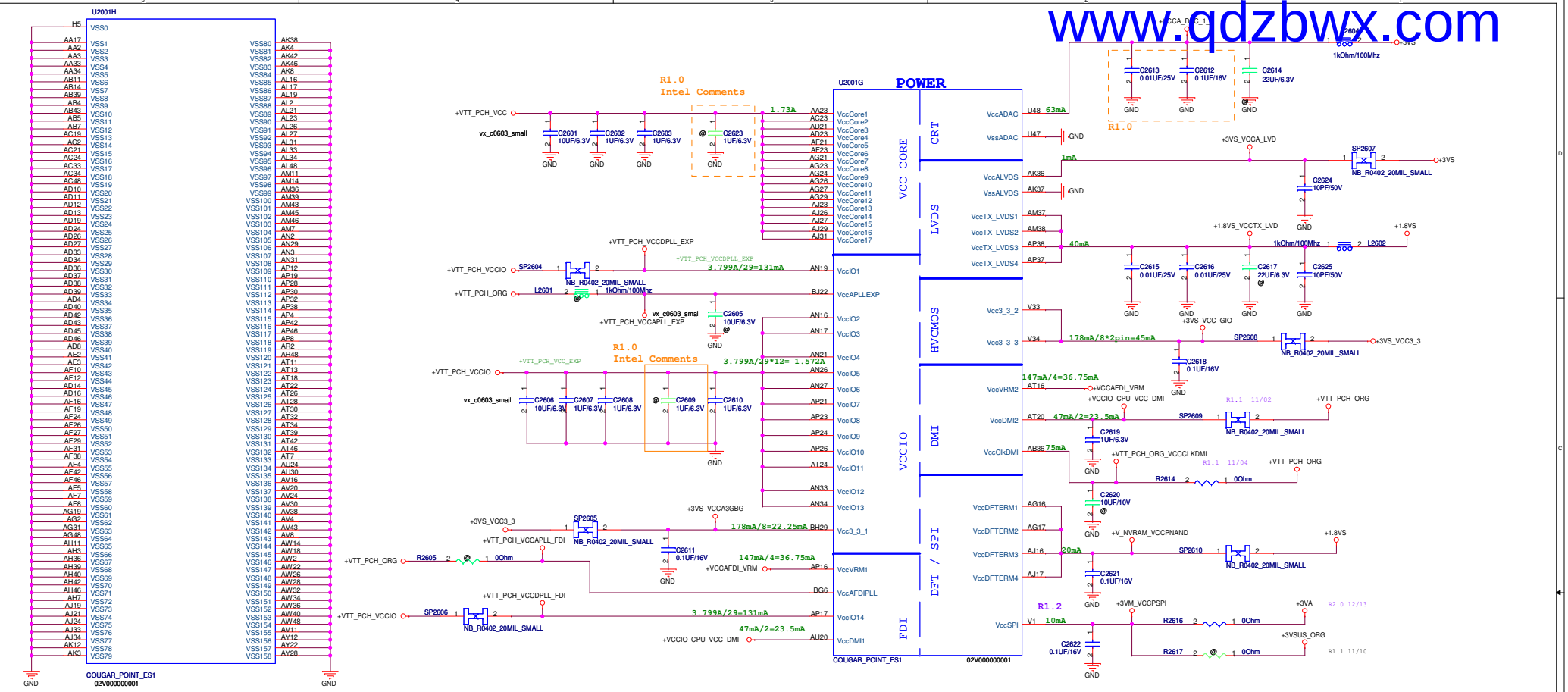
1. NC:
   LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
   LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
   LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
   L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
   LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
   VccALVDS,VccTX_LVDS

PEGATRON Title : PCH(4)_DP,LVDS,CRT
PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 23 of 93

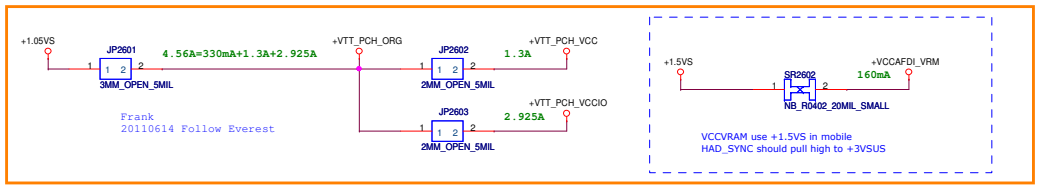




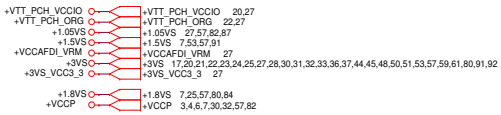
PEGATRON	Title :	PCH(6)_CPU,GPIO,MISC	
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1	
Date: Thursday, August 23, 2012	Sheet 25 of 93		



R1.0



Frank
20110608 EVERST remove 1.8VS and +VTT_PCH_ORG



R1.0
Delete
+VTT_PCH_VCC
+VTT_PCH_VCCDPLL_EXP
+VTT_PCH_VCCAPLL_EXP
+VTT_PCH_VCCDPLL_FDI
+VTT_PCH_VCCAPLL_FDI
+3VS_VCCA3GBG
+3VS_VCC_GIO
+VCCA_DAC_1_2
+3VS_VCCA_LVDS
+3VM_VCCPSPI
+V_NVRAM_VCCPNAND
+1.8VS_VCCTX_LVD
+VCCIO_CPU_VCC_DMI
+VTT_PCH_ORG_VCCCLKDMI

PEGATRON	Title :	PCH(7)_POWER,GND
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 26 of 93	

U2001I

VSS159 VSS160 VSS161 VSS162 VSS163 VSS164 VSS165 VSS166 VSS167 VSS168 VSS169 VSS170 VSS171 VSS172 VSS173 VSS174 VSS175 VSS176 VSS177 VSS178 VSS179 VSS180 VSS181 VSS182 VSS183 VSS184 VSS185 VSS186 VSS187 VSS188 VSS189 VSS190 VSS191 VSS192 VSS193 VSS194 VSS195 VSS196 VSS197 VSS198 VSS199 VSS200 VSS201 VSS202 VSS203 VSS204 VSS205 VSS206 VSS207 VSS208 VSS209 VSS210 VSS211 VSS212 VSS213 VSS214 VSS215 VSS216 VSS217 VSS218 VSS219 VSS220 VSS221 VSS222 VSS223 VSS224 VSS225 VSS226 VSS227 VSS228 VSS229 VSS230 VSS231 VSS232 VSS233 VSS234 VSS235 VSS236 VSS237 VSS238 VSS239 VSS240 VSS241 VSS242 VSS243 VSS244 VSS245 VSS246 VSS247 VSS248 VSS249 VSS250 VSS251 VSS252 VSS253 VSS254 VSS255 VSS256 VSS257 VSS258

VSS259 VSS260 VSS261 VSS262 VSS263 VSS264 VSS265 VSS266 VSS267 VSS268 VSS269 VSS270 VSS271 VSS272 VSS273 VSS274 VSS275 VSS276 VSS277 VSS278 VSS279 VSS280 VSS281 VSS282 VSS283 VSS284 VSS285 VSS286 VSS287 VSS288 VSS289 VSS290 VSS291 VSS292 VSS293 VSS294 VSS295 VSS296 VSS297 VSS298 VSS299 VSS300 VSS301 VSS302 VSS303 VSS304 VSS305 VSS306 VSS307 VSS308 VSS309 VSS310 VSS311 VSS312 VSS313 VSS314 VSS315 VSS316 VSS317 VSS318 VSS319 VSS320 VSS321 VSS322 VSS323 VSS324 VSS325 VSS326 VSS327 VSS328 VSS329 VSS330 VSS331 VSS332 VSS333 VSS334 VSS335 VSS336 VSS337 VSS338 VSS339 VSS340 VSS341 VSS342 VSS343 VSS344 VSS345 VSS346

02V000000001

COUGAR_POINT_ES1

GND

U2001J

POWER

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

RTC

HDA

VccACIk VccDSW3_3 DcpSusByp Vcc3_3_4 VccAPLLDMI2 VccIO15 DcpSus1 VccASW1 VccASW2 VccASW3 VccASW4 VccASW5 VccASW6 VccASW7 VccASW8 VccASW9 VccASW10 VccASW11 VccASW12 VccASW13 VccASW14 VccASW15 VccASW16 VccASW17 VccASW18 VccASW19 VccASW20 DcpRTC VccVRM3 VccADPLLA VccADPLLB VccIO16 VccDIFFCLKN1 VccDIFFCLKN2 VccDIFFCLKN3 VccSSC DcpSST DcpSus2 DcpSus3 V_PROC_IO VccRTC

COUGAR_POINT_ES1

VccIO17 VccIO18 VccIO19 VccIO20 VccIO21 VccSus3_3_1 VccSus3_3_2 VccSus3_3_3 VccSus3_3_4 VccSus3_3_5 VccIO22 V5REF_Sus DcpSus4 VccSus3_3_6 V5REF VccSus3_3_7 VccSus3_3_8 VccSus3_3_9 VccSus3_3_10 Vcc3_3_5 Vcc3_3_6 Vcc3_3_7 Vcc3_3_8 VccIO23 VccIO24 VccIO25 VccIO26 VccAPLLSATA VccVRM4 VccIO27 VccIO28 VccIO29 VccASW21 VccASW22 VccASW23 VccSusHDA

Frank
20110608 C2741,C2713, C2740 is mounted in EIH31

R1.0
Intel Comments
0.803A/23*20= 698mA

Frank
20110608 R2701 is un-mounted and L2701 is mounted in EIH31

R1.0
Intel Comments

R1.0
Intel Comments

R1.0
Intel Comments

R1.0
Intel Comments

Frank
20110608 Remove short pins but EIH31 does not.

Frank
0503 Remove Remove +1.05VM.

Frank
20110614 Follow Everest

R1.0
Delete
+VTT_PCH_VCCUSBCORE
+VTT_PCH_VCCIO_SATA3
+VTT_PCH_ORG_VCCAPLL_SATA3
+VTT_PCH_VCCA_A_DPL
+VTT_PCH_VCCA_B_DPL
+VTT_PCH_ORG_SSCVCC
+VCCDPLL_CPY
+VTT_PCH_VCCIO_VCC_SATA
+3VS_VCC_CLKF33
+3VS_VCCPCORE
+3VS_VCCPPCI
+VTT_CPU_VCCPCPU
+5VSUS_ORG
+5VSUS_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+3VSUS_ORG_VCCPAZSUS
+3VSUS_ORG_VCCPSUS

PEGATRON Title : PCH(8)_POWER,GND

PEGATRON COMPUTER INC Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 27 of 93

PCH SPI ROM

SHARE ROM CONFIG1

U2801	@	
U2802	@	
U2803	ME+BIOS+EC	4MB

ummount:
R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802,R2869, R2870, R2868, D2802, U2801

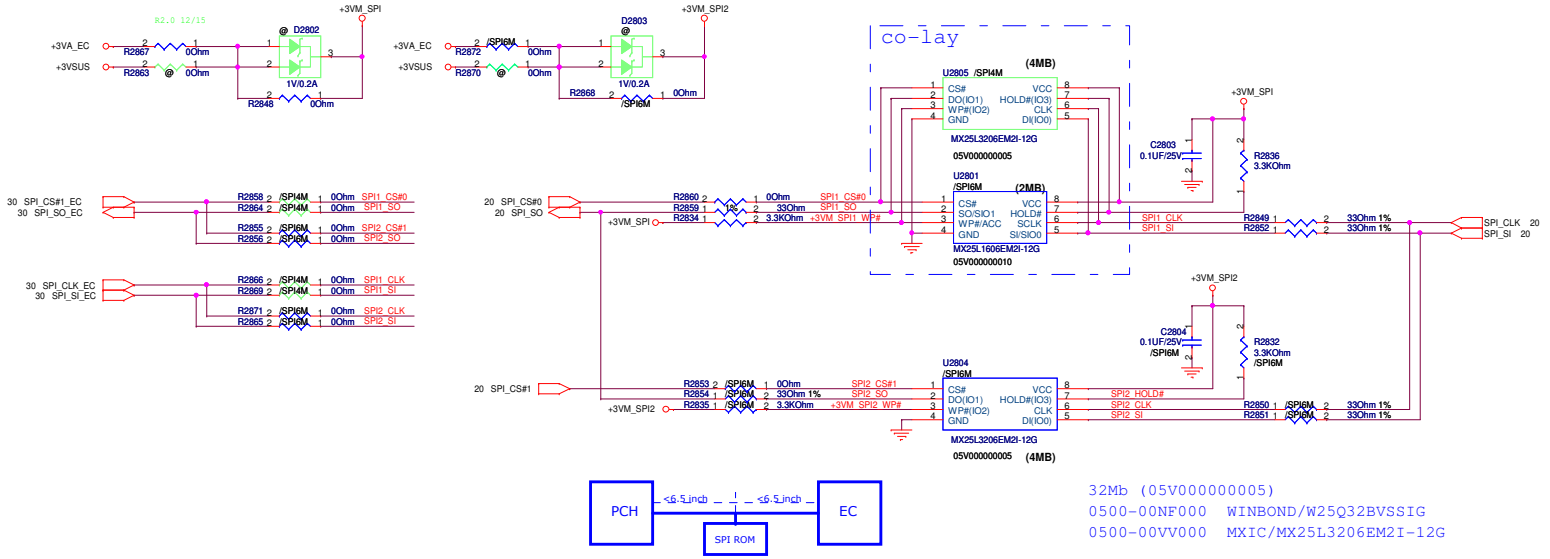
SHARE ROM CONFIG2

U2801	ME Firmware	2MB
U2802	EC+BIOS	4MB

ummount:
R2858, R2862, R2866, R2867, U2803

PCH SPI ROM

+3VA_EC reserved for share ROM

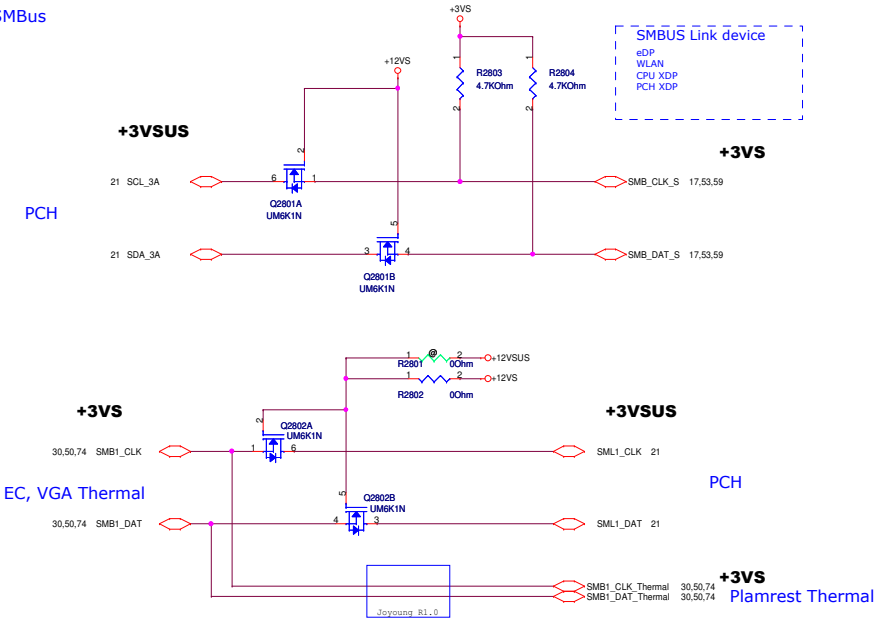


32Mb (05V000000005)
0500-00NF000 WINBOND/W25Q32BVSSIG
0500-00VV000 MXIC/MX25L3206EM2I-12G

SPI Debug Connector

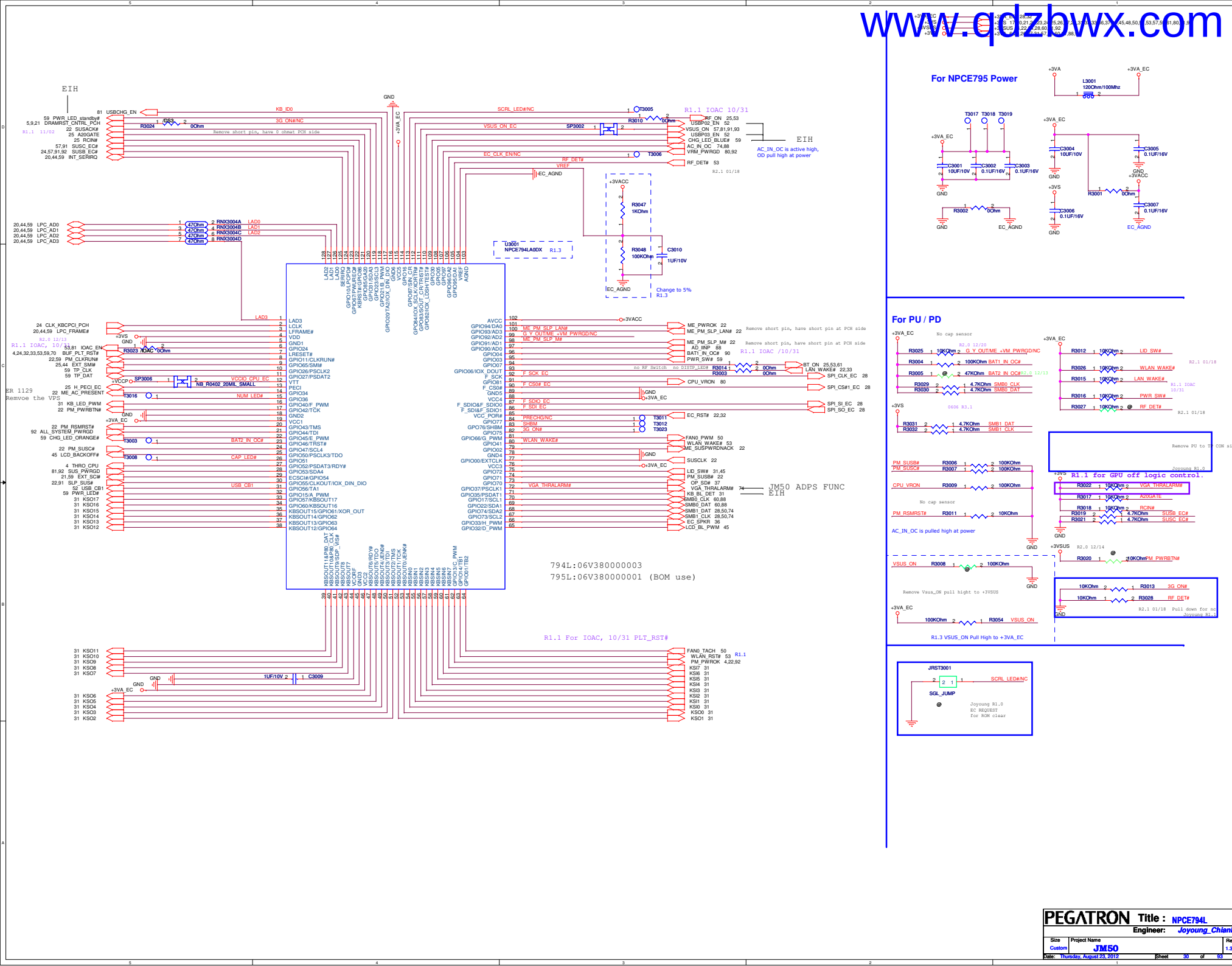
layout space issue, so remove J2801.

PCH SMBus



PEGATRON	Title :	PCH(9)_SPI,SMB	
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg	
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 28 of 93		

PEGATRON	Title :	CLK_ICS9LRS3197
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg
Size: Custom	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 29 of 93	

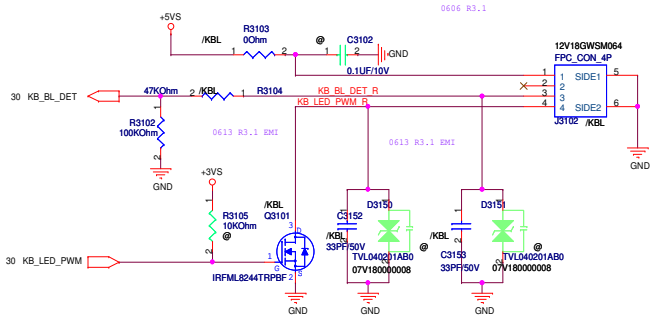


PEGATRON	Title : NPCE794L		
	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 1.3
Date: Thursday, August 23, 2012	Sheet 30 of 93		

+5VS +5VS 27,36,37,45,48,50,51,57,80,87,91
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3VA +3VA 6,20,26,27,30,57,59,60,81,88,93

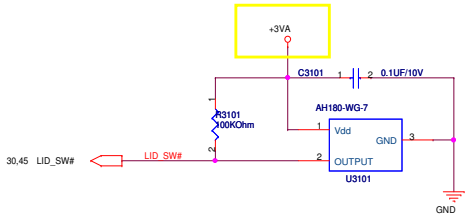
KB backlight

R3.1 Add 4P CON for KB Backlight Kevin 0601

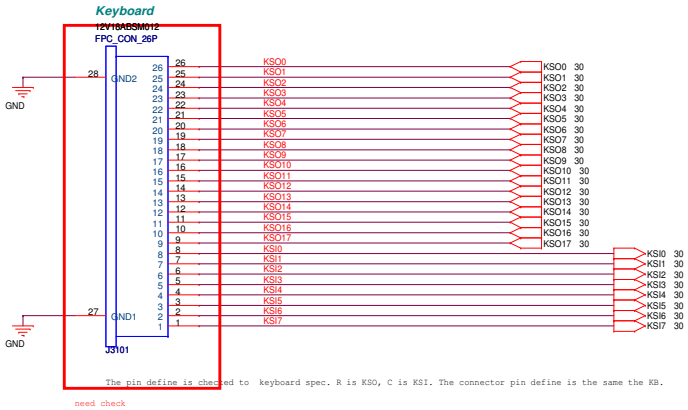


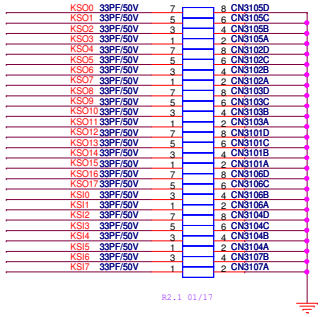
LID Switch

SR-85
R1.0 change net name. Joyoung 0630



Keyboard





PEGATRON	Title : EC_IT8512(2)KB, TP,FP		
	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 31 of 93		

+VCCP +VCCP 3,4,6,7,30,57,82
+3VA_EC +3VA_EC 28,30
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

R1.1
add for NV FAE request
choke temp sense.

Thermal Policy

+3VS
R3208
10KOhm
@
Q3203B
UM6K1N
@
Q3203A
UM6K1N
@
87 VGA_HOT#
+3VS
R3206
10KOhm
JM50_I 05/08
JM50_I 05/24

74 VGA_OVERTEMP# SP3202 R0402

50 PR_OVERTEMP# 0Ohm @ R3207 PR_OVERTEMP# R

50,92 CPU_THERM# SP3201 NB_R0402_20MIL_SMALL

NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of POR is less than 10us

+3VA_EC
R3204 47KOhm
D3202 1.2V/0.1A
D3203 1.2V/0.1A
EC_RST# 22,30
C3201
4.7UF/6.3V
@
Q3202A
UM6K1N

81,92 FORCE_OFF#

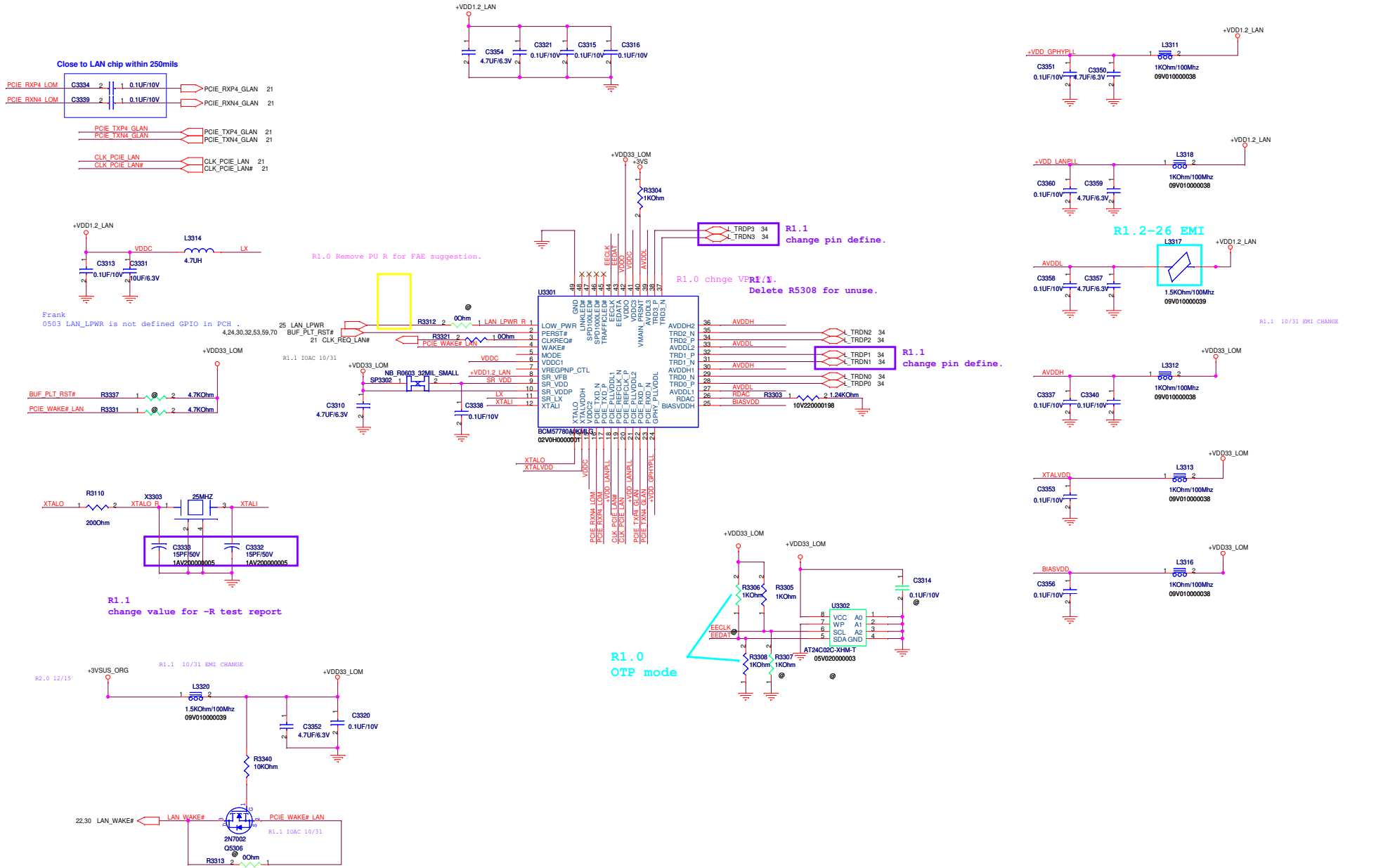
Q3202B
UM6K1N

4,24,30,33,53,59,70 BUF_PLT_RST#

+VCCP
R3201
330Ohm
Q3201
PMBS3904

4,25 H_THRMTRIP#

PEGATRON	Title : RST_Reset Circuit	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: Custom	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 32 of 93	



PEGATRON	Title : LAN_BCM57780		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50	Rev: 3.1	
Date: Thursday, August 23, 2012	Sheet 33 of 93		

Joyoung R1.0
FAE suggest common mode choke is on chip side.

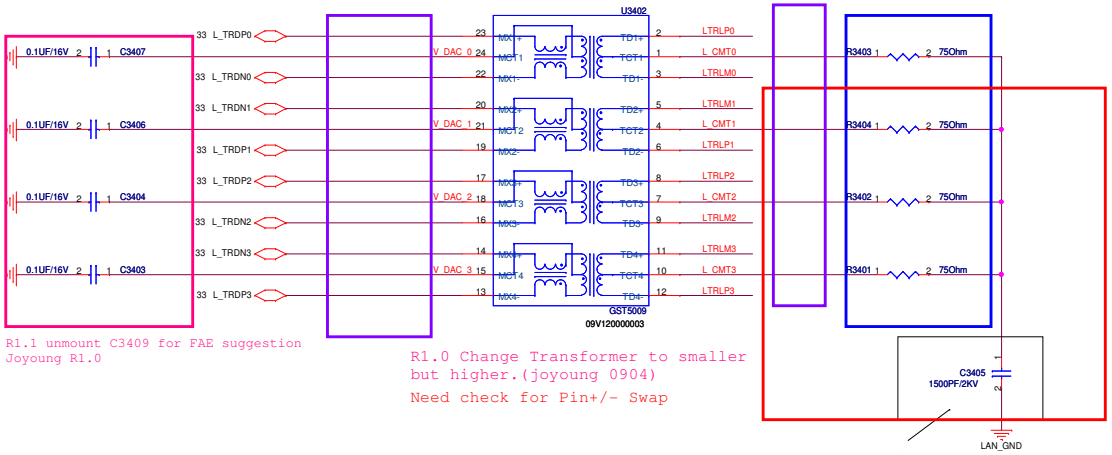
R1.1 Add 0 OHM for FAE suggestion 0809
JM50: FAE suggest remove

R1.1 Swap L_TRDP3 L_TRDN3 & L_TRDP1 L_TRDN1

R1.1 remove CAP of V_DAC_3, V_DAC_2 and V_DAC_1 for FAE suggestion

R1.1 Remove R3405~R3407 & C3409

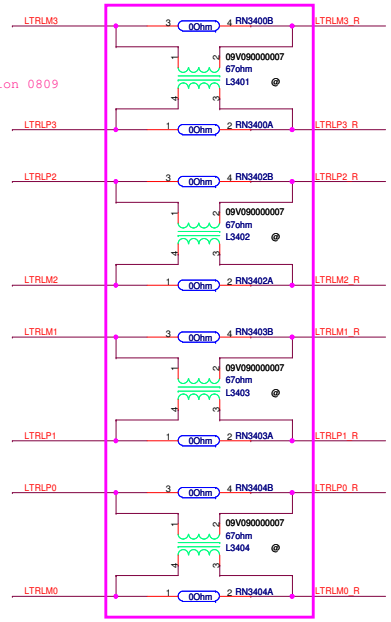
R1.1 Mount R3401~R3403 for FAE suggestion 0809

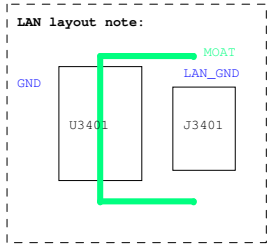


R1.1 unmount C3409 for FAE suggestion
Joyoung R1.0

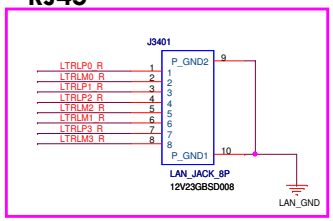
R1.0 Change Transformer to smaller but higher.(joyoung 0904)

Need check for Pin+/- Swap



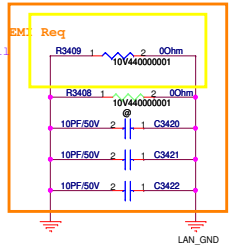


RJ45



Change RJ45 CON3401

R1.1 EMI Request 4.7PF & Set Close to Connector, then removed all



R1.0 Reserve D3401 for EMI.

R1.0 Mount R3408 for FAE suggestion

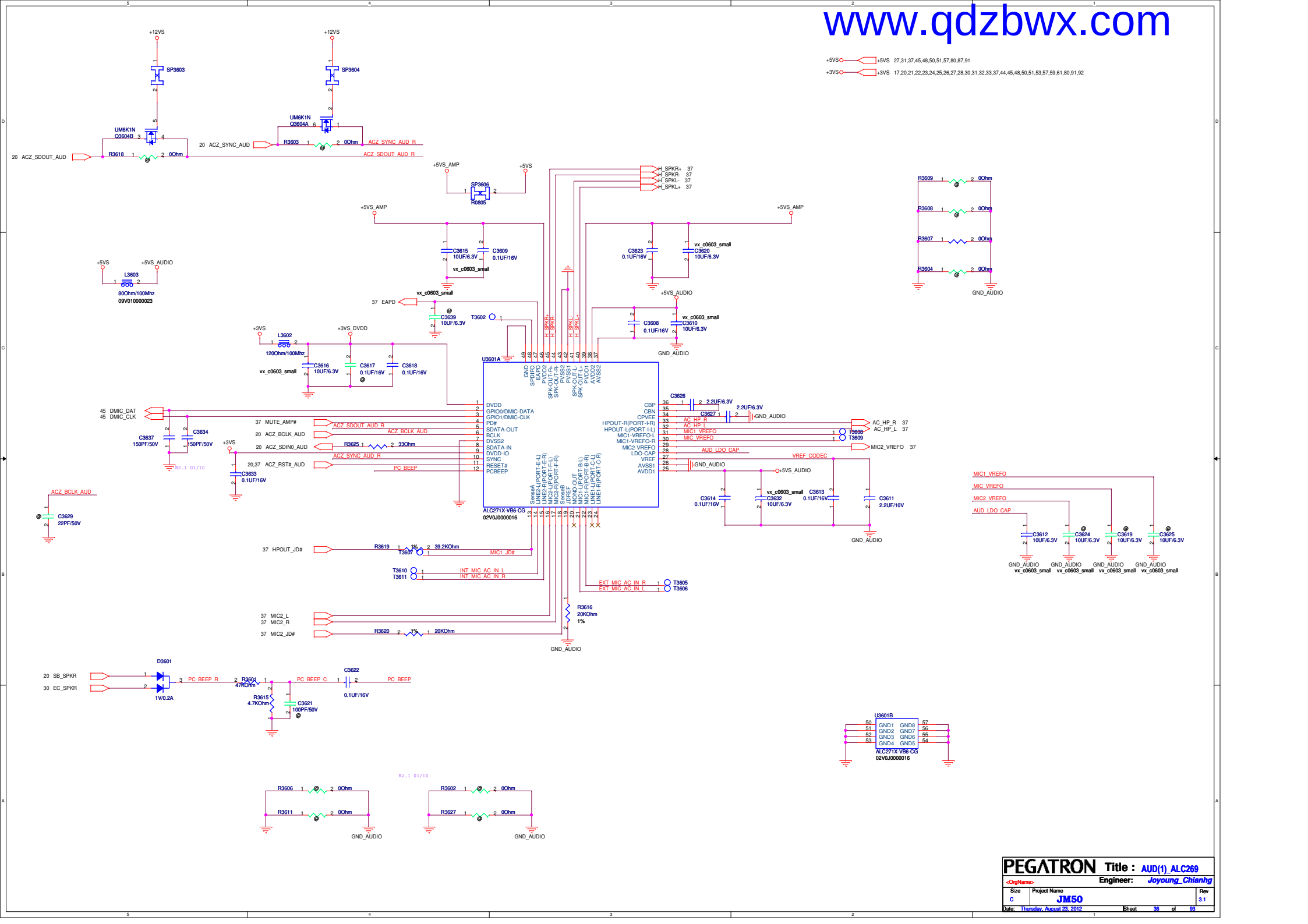
PEGATRON Title : RJ45
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 34 of 93

PEGATRON Title : MDC CONN

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 35 of 93



PEGATRON	Title : AUD(1)_ALC269		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 36 of 93		

+5VS +5VS 27,31,36,45,48,50,51,57,80,87,91
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,44,45,48,50,51,53,57,59,61,80,91,92
+5VS_AUDIO +5VS_AUDIO 36

Internal Speaker Conn.

add R3706, R3707, R3708, R3709 for EMI request

36 H_SPKR+
36 H_SPKR-
36 H_SPKL+
36 H_SPKL-
R3706 0Ohm
R3707 0Ohm
R3708 0Ohm
R3709 0Ohm
J3704 SIDE1 SIDE2
WtoB_CON_4P
12V17GIRM002
C3710 1000PF/50V
C3711 1000PF/50V
C3712 1000PF/50V
C3713 1000PF/50V
R1.1 Reserved for EMI & Change to 1000PF

MIC2_JD# 36
COMBO_MIC
R3701 22KOhm R1.1 10/31 KEVIN
Q3701 2N7002
C3701 10UF/6.3V
GND_AUDIO
Need change 0702-0028000 in next stage

R2.0 12/16
R1.1 10/31 KEVIN
36 MIC2_VREFO
R3710 2.2KOhm
R3714 1KOhm
C3702 2.2UF/10V
C3703 2.2UF/10V
MIC2_R 36
MIC2_L 36
R3711 22KOhm 10V240000016

add R3722, R3723 and C3723, C3725 change 100pFfor EMI request

ER1.11
COMBO_MIC
L3701 120Ohm/100Mhz
L3703 120Ohm/100Mhz
L3702 120Ohm/100Mhz
COMBO_MIC_CON
HP_L_CON
HP_R_CON
HPOUT_JD#
36 AC_HP_L
36 AC_HP_R
36 HPOUT_JD#
R3713 62Ohm
R3712 62Ohm
R3716 1KOhm
R3715 1KOhm
C3704 100PF/50V
C3705 100PF/50V
C3709 100PF/50V
J3701 PHONE_JACK_7P
12V14GBSD015
need check
Close J6701

JM50_T 05/11
+3VS
+5VS
R3704 10KOhm
R3702 1KOhm
D3702 RB751V-40
36 EAPD
D3701 BAT54AW
20,36 ACZ_RST#_AUD
30 OP_SD#
1V/0.1A
MUTE_AMP# 36
+5VA
R3705 100KOhm
R3703 10KOhm
MUTE_AMP#
Q3704 2N7002
Q3705A UM6K1N
OP_SD#
Q3705B UM6K1N
ACZ_RST#_AUD
GND

C3706 10PF/50V
C3707 33PF/50V
ER1.32
D3706 AZ2025-01H.R7G 07V220000006
GND_AUDIO

R2.1 01/17
HP_R_CON
D3705 AZ2025-01H.R7G 07V220000006
HPOUT_JD#
D3704 AZ2025-01H.R7G 07V220000006
HP_L_CON
D3703 AZ2025-01H.R7G 07V220000006
EMI request
C3708 0.1UF/16V
GND

PEGATRON Title : AUD(2)_AMP,JACK
<OrgName> Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 37 of 93

PEGATRON Title : AUD(3)_FM2010

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 38 of 93

PEGATRON	Title : AUD(4)_****		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 39 of 93		

PEGATRON Title : TPM_****

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 40 of 93

PEGATRON Title : CB(2)_R5C833

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 41 of 93

PEGATRON Title : CB(3)_4in1 CardReader

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 42 of 93

PEGATRON Title : CB(4)_NewCard

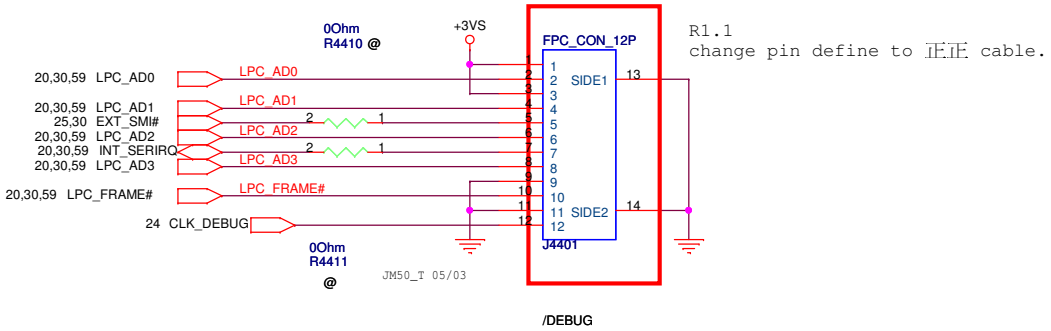
<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 43 of 93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,45,48,50,51,53,57,59,61,80,91,92

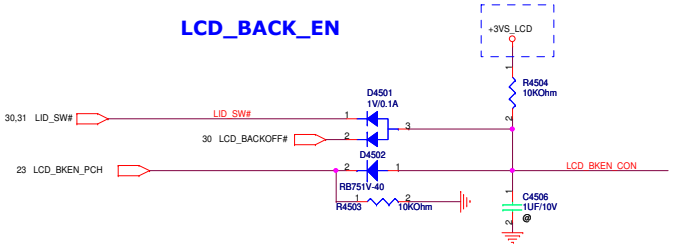
LPC Debug Port



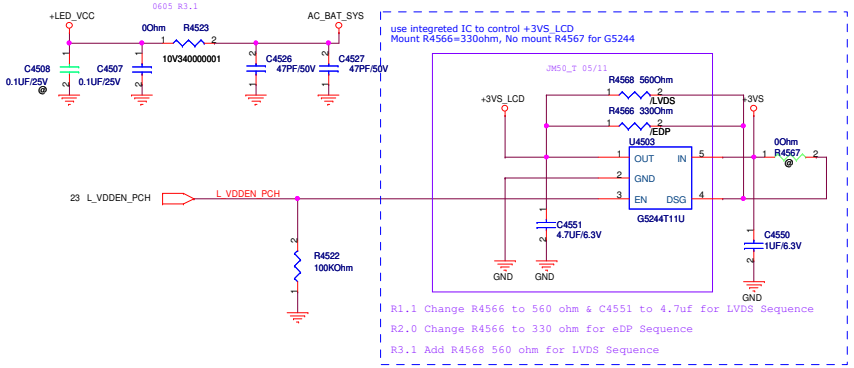
R1.1
change pin define to IEIE cable.

PEGATRON	Title : BUG_Debug	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: B	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 44 of 93	

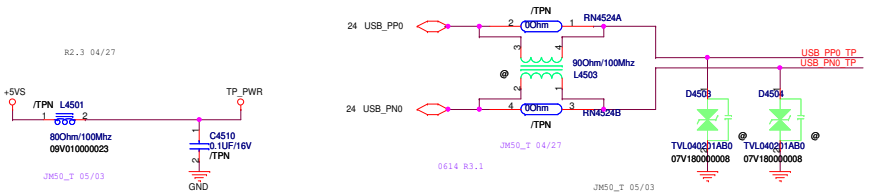
LCD_BACK_EN



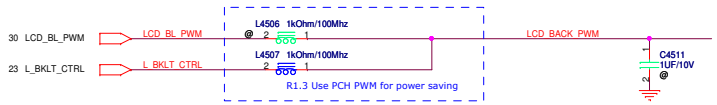
LCD VDDEN / +LED_VCC



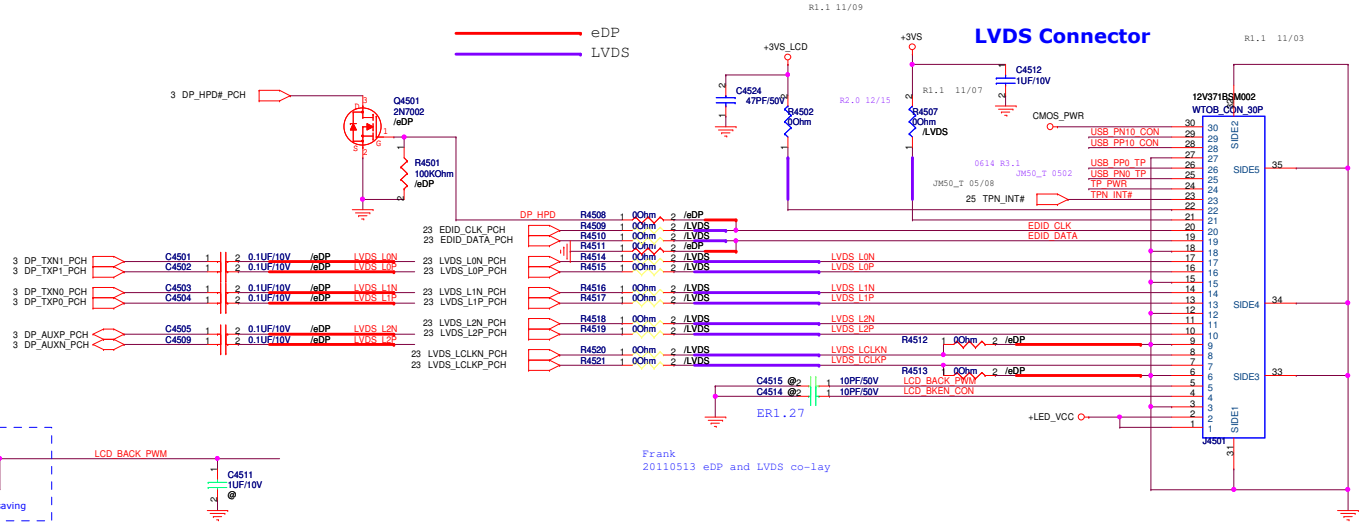
Touch Panel



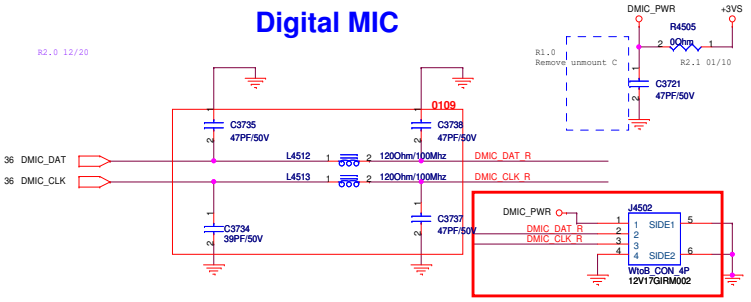
LCD_BL_PWM



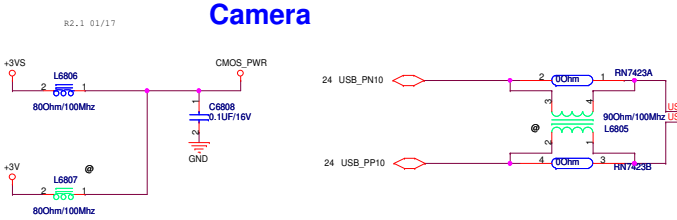
LVDS Connector



Digital MIC



Camera



PEGATRON	Title : CRT(1)_LVDS	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 45 of 93	

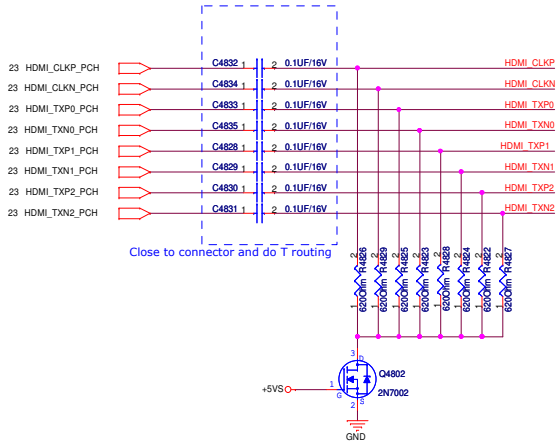
PEGATRON	Title : CRT		
BU1-RD Div.1-HW RD Dept.1	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 46 of 93		

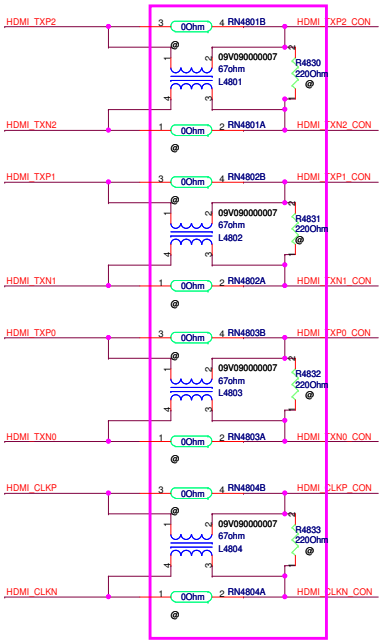
PEGATRON Title : CRT(3)_Display Port

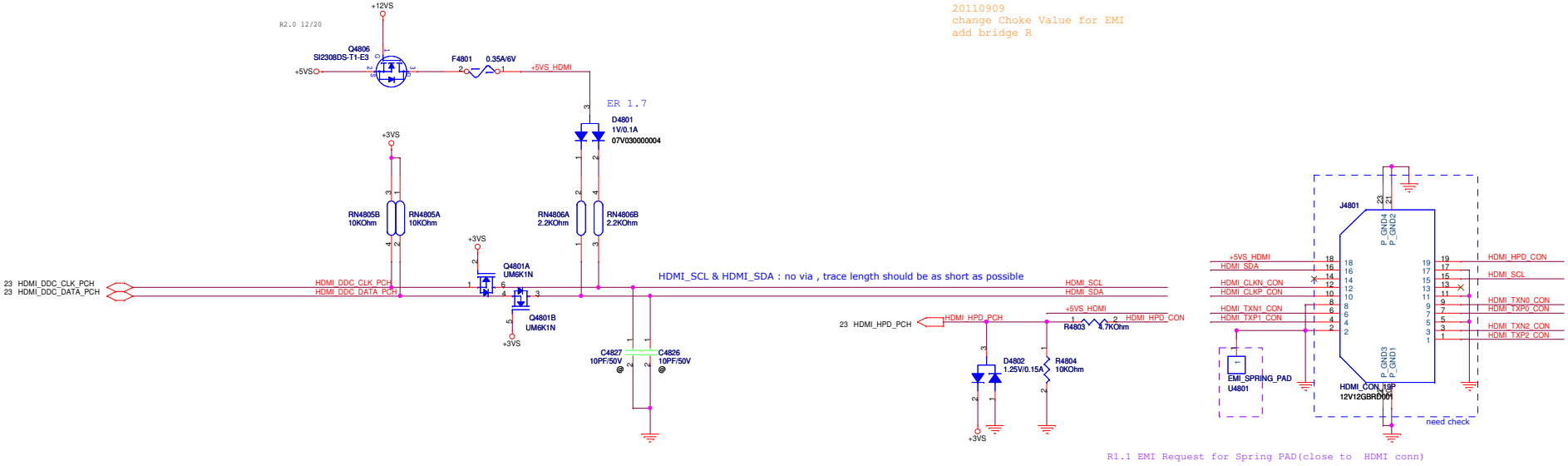
<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 47 of 93







+12VS +12VS 28,36,91

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,50,51,53,57,59,61,80,91,92

+5VS +5VS 27,31,36,37,45,50,51,57,80,87,91

PEGATRON	Title : TV(1)_HDMI	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 48 of 93	

PEGATRON Title : TV(2)_****

<OrgName> Engineer: Joyoung_Chianhg

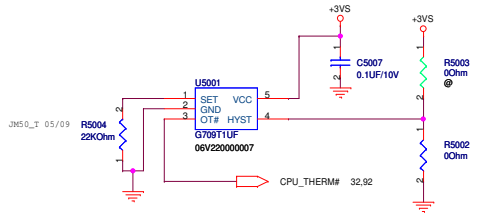
Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 49 of 93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,51,53,57,59,61,80,91,92

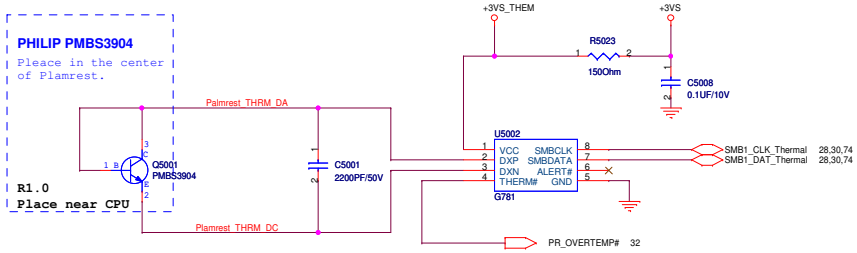
+5VS +5VS 27,31,36,37,45,48,51,57,80,87,91

CPU Thermal Sensor



(10°C for HYST =VCC)
(2°C for HYST = GND)
Hysteresis prevents the output from oscillating when the temperature is near the trip point.

DIMM Thermal Sensor

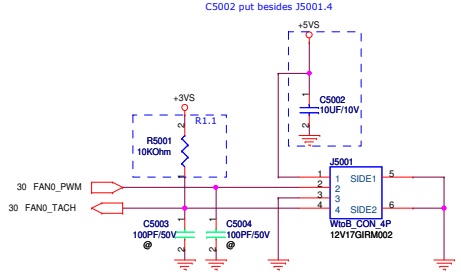


U5002 place neer power, CPU, PCH area,

SMBUS addr=1001100x (98)

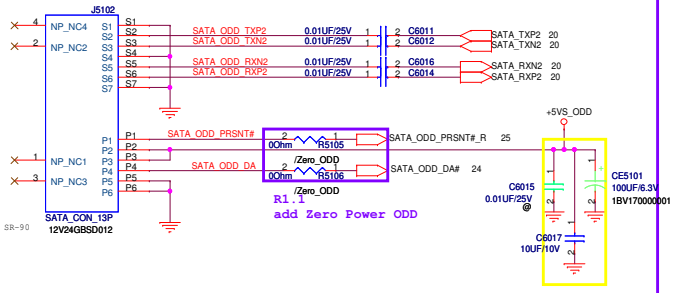
U5002: Remote(Local) thermal sensor,use remote mode.

PWM Fan



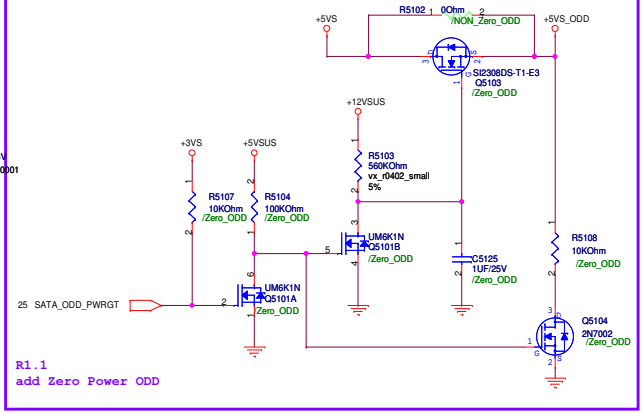
PEGATRON	Title : FAN_Fan,Sensor		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 50 of 93		

ODD

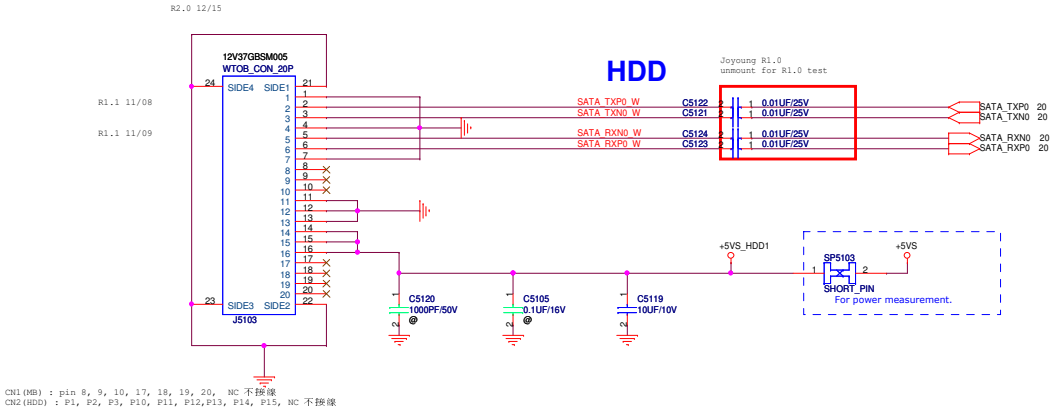


ZERO POWER ODD SUPPORT

support Hokey turn off ODD power

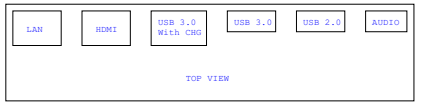


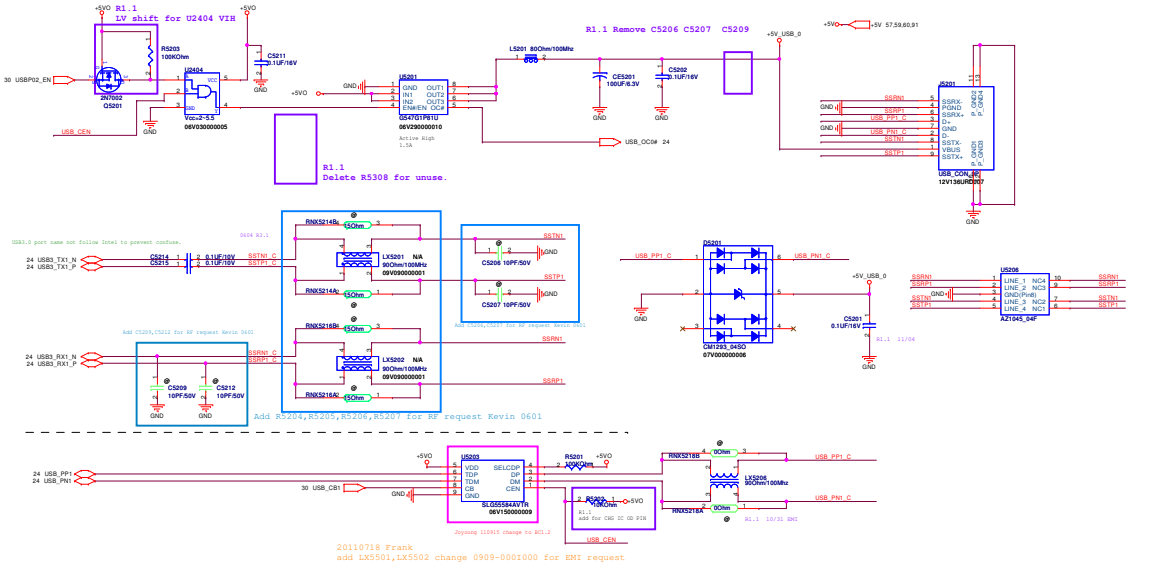
Connector for Cable

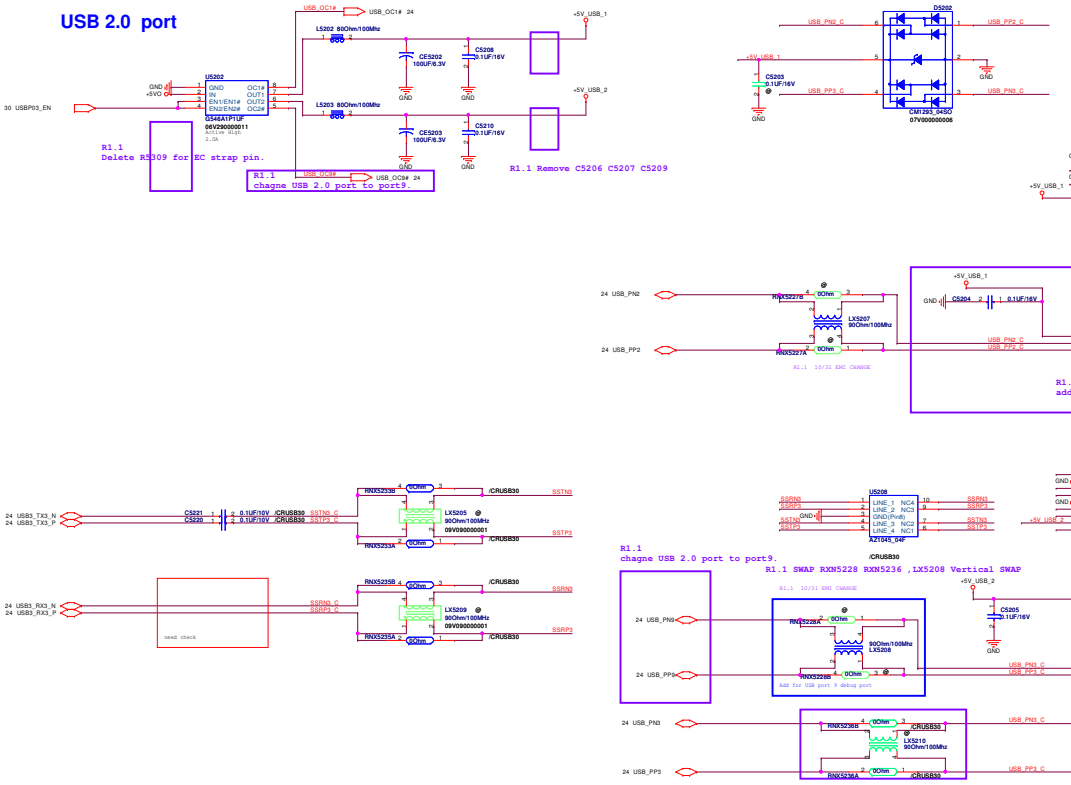


R1.1 11/02 Remove HDD SATA CONN PART

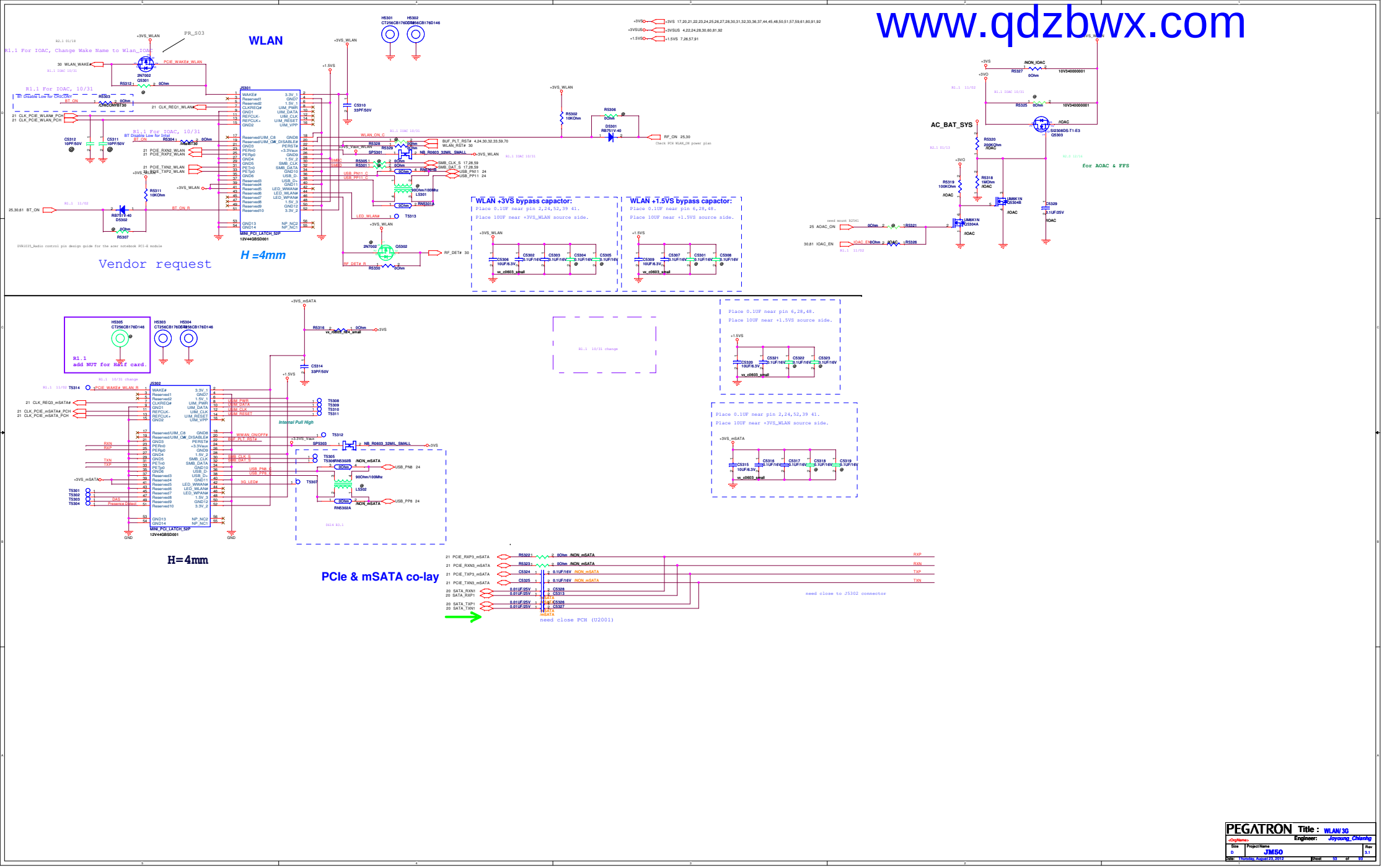
PEGATRON	Title : XDD_HDD,ODD	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 51 of 93	







PEGATRON	Title : USB_USB Port		
<OrgName>	Engineer: Joyoung_Chiang		
Size: D	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 52 of 93		



PEGATRON	Title : WLAN/ 3G	
<OrgName>	Engineer: Joyoung_Chiang	
Size: D	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 53 of 93	

PEGATRON Title : USB3.0

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 54 of 93

PEGATRON Title : Fersco USB 3.0

BG1-CSC-HW R&D Dept.5 Engineer: Joyoung_Chianhg

Size	Project Name	Rev
A2	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 55 of 93

+3VA +3VA 6,20,26,27,30,31,57,59,60,81,88,93

+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

+5VSUS +5VSUS 51,57,59,91

+5VA +5VA 37,60,81,91

+5V +5V 57,59,60,91

+5VS +5VS 27,31,36,37,45,48,50,51,57,80,87,91

AC_BAT_SYS AC_BAT_SYS 45,53,81,87,88

+3V +3V 24,45,57,59,61,91

30,59 PWR_LED#

30,59 PWR_LED_standby#

30,59 CHG_LED_BLUE#

30,59 CHG_LED_ORANGE#

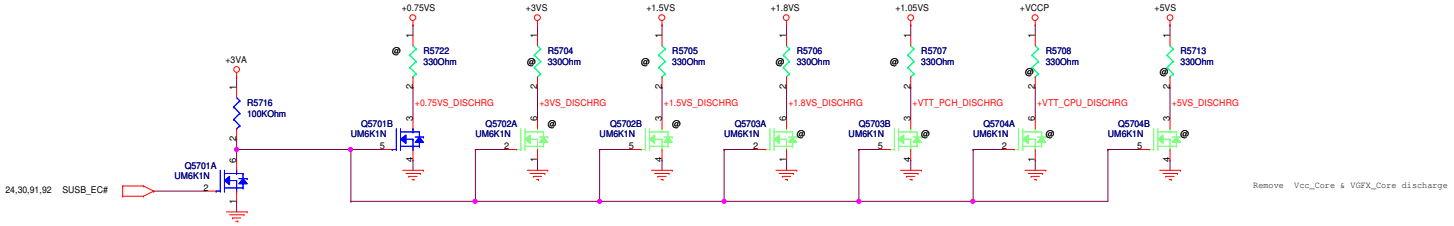
PEGATRON Title : LED_Indicator

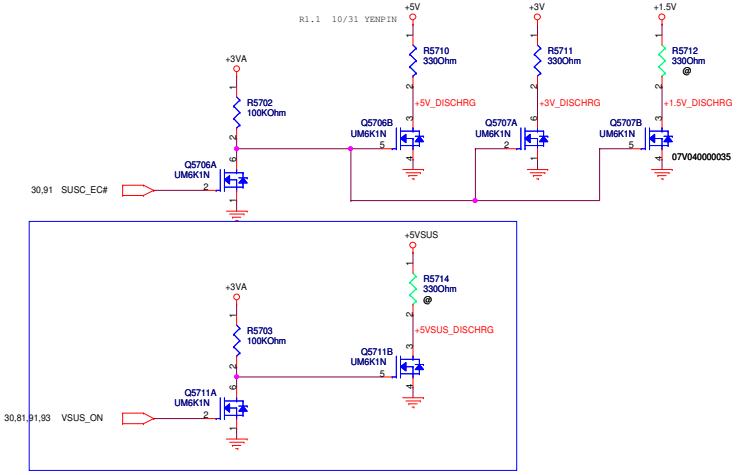
<OrgName> Engineer: Joyoung_Chianhg

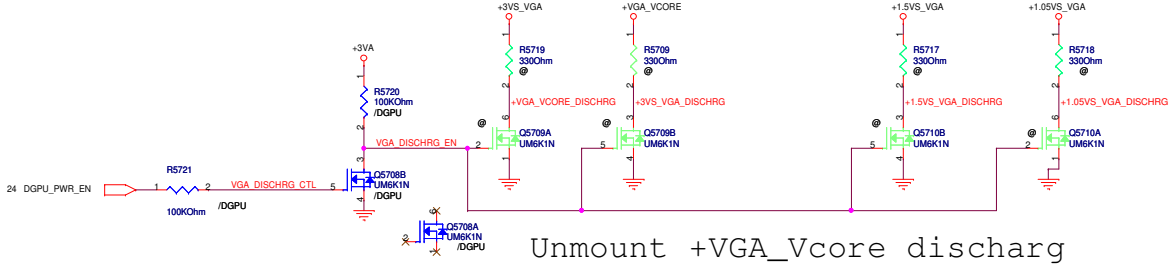
Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 56 of 93

+3VA +3VA 6,20,26,27,30,31,59,60,81,88,93
+VCORE +VCORE 6,9,11,80
+VGFX_CORE +VGFX_CORE 7,9,80
+VCCP +VCCP 3,4,6,7,30,32,82
+0.75VS +0.75VS 16,17,83
+1.05VS +1.05VS 26,27,82,87
+1.5VS +1.5VS 7,26,53,91
+1.8VS +1.8VS 7,25,26,80,84
+3VS +3VS 17,20,21,22,23,24,25,26,27,28,30,31,32,33,36,37,44,45,48,50,51,53,59,61,80,91,92
+5VS +5VS 27,31,36,37,45,48,50,51,80,87,91
+1.5V +1.5V 5,16,17,18,60,83
+3V +3V 24,45,59,61,91
+5V +5V 59,60,91







Unmount +VGA_Vcore discharg

PEGATRON Title : DSG_Discharge
<OrgName> Engineer: Joyoung_Chianhg
Size C | Project Name JM50 | Rev 3.1
Date: Thursday, August 23, 2012 | Sheet 57 of 93

PEGATRON	Title : System Setting		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: Custom	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 58 of 93		

12V371BSM002
WTOB_CON_30P
J5901

R1.1 11/03

22,30 PM_CLKRUN#
20,30,44 INT_SERIRQ
20,30,44 LPC_FRAME#
20,30,44 LPC_AD3
20,30,44 LPC_AD2
20,30,44 LPC_AD1
20,30,44 LPC_AD0
24 CLK_TPM
+3V
+3VS
GND
C5902 10UF/10V
+RTCBAT
20,60 +RTCBAT
4,24,30,32,33,53,70 BUF_PLT_RST#
21 CLK_REQ_CR#
21 PCIE_TXP1_CR
21 PCIE_TXN1_CR
21 CLK_PCIE_CR
21 CLK_PCIE_CR#
21 PCIE_RXP1_CR
21 PCIE_RXN1_CR
SIDE1
SIDE2
SIDE3
SIDE4
SIDE5

Card Reader

TP_CLK @C5916 1000PF/50V
TP_DAT @C5915 1000PF/50V
SMB_DAT_S @C5914 1000PF/50V
SMB_CLK_S @C5913 1000PF/50V
GND

Power BTN and LED

R2.0 12/19

30 PWR_SW#
30 PWR_LED#
30 PWR_LED_standby#
30 CHG_LED_BLUE#
30 CHG_LED_ORANGE#
PWR_SW#
PWR_LED#
PWR_LED_standby#
CHG_LED_BLUE#
CHG_LED_ORANGE#
+5VSUS
+5V
+3VA
GND
J5904
FPC_CON_10P
12V18AWSM001

R1.1
change power plane

R2.0 12/20

C5905 0.01UF/25V PWR_LED#
C5906 0.01UF/25V PWR_LED_standby#
C5907 0.01UF/25V CHG_LED_BLUE#
C5908 0.01UF/25V CHG_LED_ORANGE#

R1.1
change for TP

R2.0 12/19

R2.0
change for Elan click pad

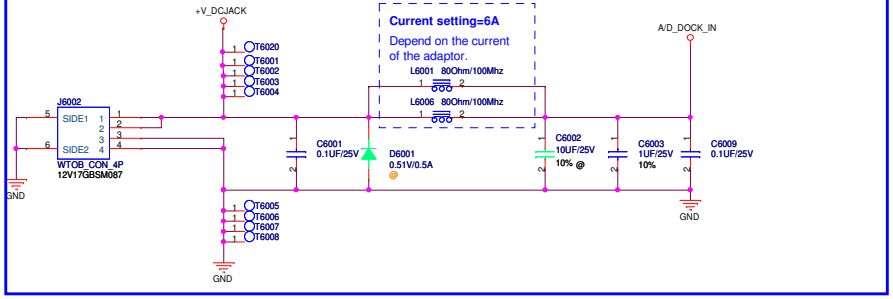
+3VS
RN5901A 4.7KOhm TP_CLK
RN5901B 4.7KOhm TP_DAT
C5901 10UF/10V
30 TP_CLK
30 TP_DAT
17,28,53 SMB_DAT_S
17,28,53 SMB_CLK_S
R5901 10KOhm
R5915 100KOhm
21,30 EXT_SCI#
Q5901 @2N7002
J5906
SIDE1
SIDE2
FPC_CON_8P
12V18GWSM059

R1.1 11/10

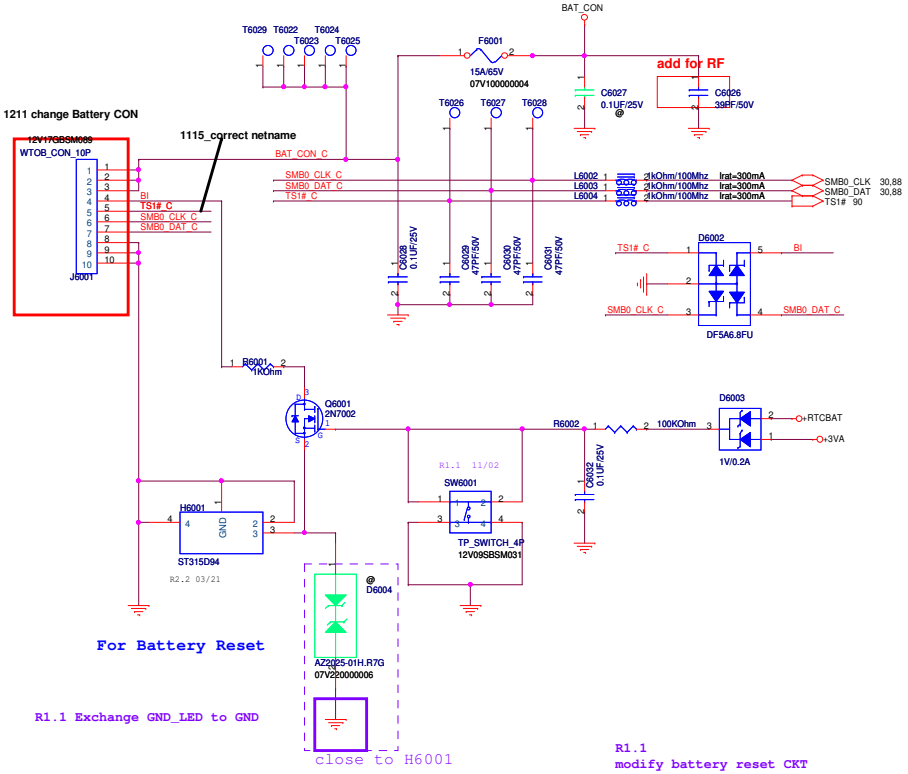
R3.1 Unmount for SMBus INT pin Kevin 0601

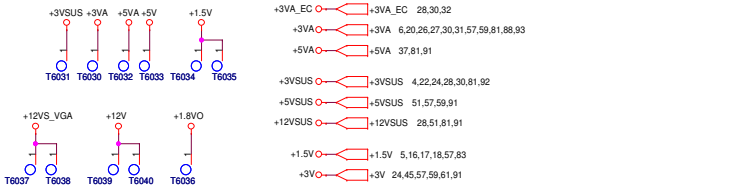
PEGATRON	Title : B to B		
<OrgName>	Engineer: Joyoung_Chianhg		
Size: A	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 59 of 93		

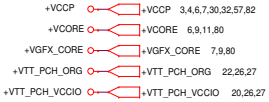
DC Jack WtoB CONN



Battery Connector







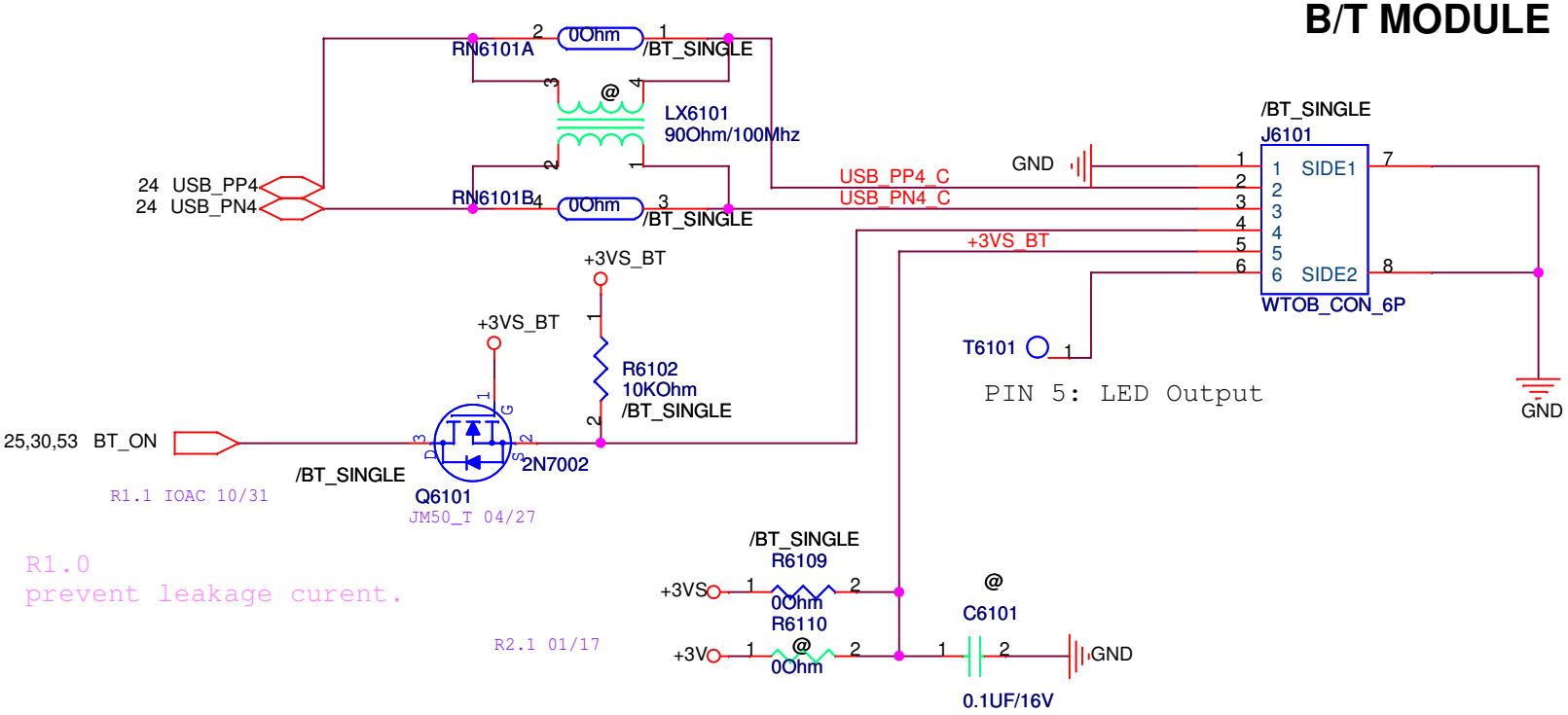
PEGATRON Title : DC_DC/BAT CONN

<OrgName> Engineer: Joyoung_Caianhg

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 60 of 93

B/T MODULE



PEGATRON	Title : Fersco USB 3.0		
Pegatron Corp.	Engineer: Joyoung_Chianhg		
Size: A	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 61 of 93		

PEGATRON	Title : System Setting	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: Custom	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 62 of 93	

PEGATRON	Title : B to B	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: A	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 63 of 93	

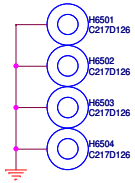
PEGATRON Title : B to B

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

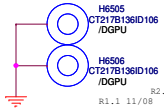
Date: Thursday, August 23, 2012 Sheet 64 of 93

CPU Bracket Hole

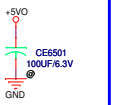


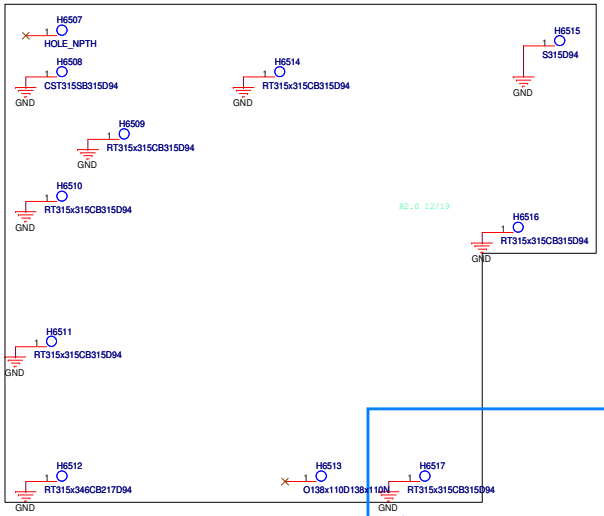
ME B Type

VGA Bracket Hole



place between J5204 /J5205

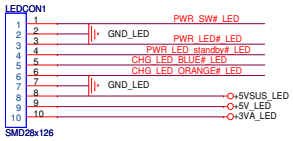


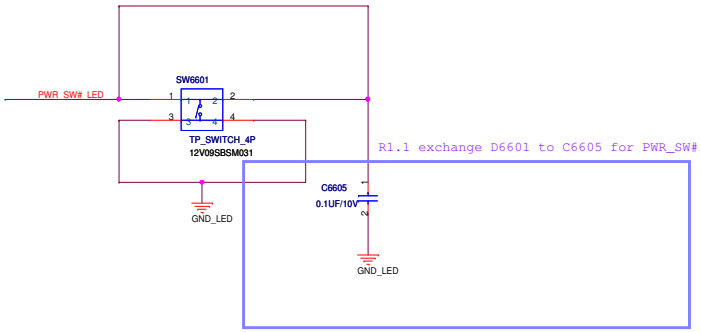


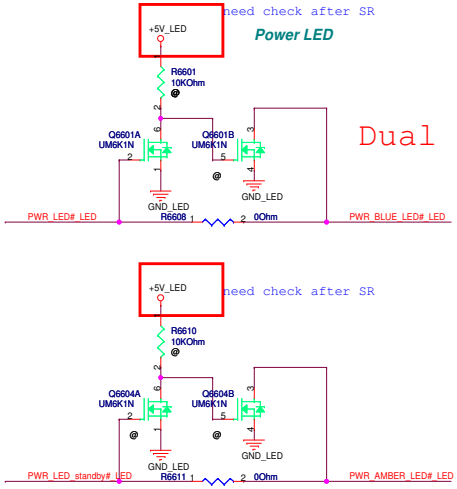
This screw hole should be Upside down(TOP and BOTTOM).

PEGATRON	Title : ME_CONN,Skew Hole	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 65 of 93	

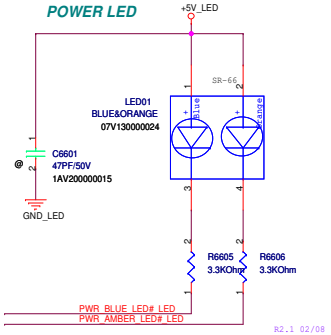
Power Button

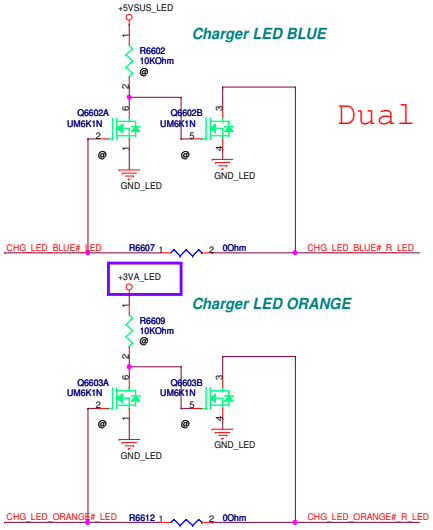




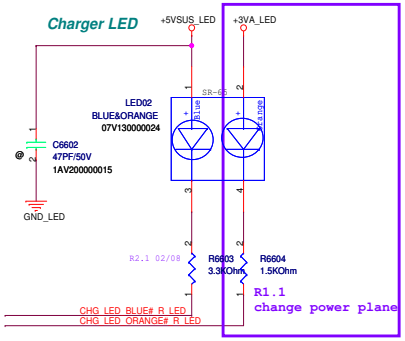


Dual Color





Dual Color



PEGATRON	Title : TP_M	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 66 of 93	

From System's PCIE interface

R1.1 change to 30P

R2.0 move back

R2.0 12/13

RTC

12V20GBSM000

Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

SDCLK trace length shorter,surround with GND.

20110909 Joyoung EMI request

C4008 C4002 SD CARD CAP

Close to connector

trace width 60mils

trace width 40mils

Part number:020J-007D000

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

PEGATRON Title : RTS5209

Engineer: JAY TSAI

Size	Project Name	Rev
C	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 67 of 93

PEGATRON Title : USB_USB Port

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
B	JM50	3.1

Date: Thursday, August 23, 2012 Sheet 69 of 93

Frank
20110513 Change N13P GPU.

PEX=> From NB
EXP: VGA Card to NB

3 PCIENB_RXP[0..15]
3 PCIENB_RXN[0..15]
3 PCIEG_RXP[0..15]
3 PCIEG_RXN[0..15]

+3VS_VGA
24 DGPU_HOLD_RST#
4,24,30,32,33,53,59 BUF_PLT_RST#
U7002
SN74LVC1G08DCKR
/DGPU
T7022
PEX_RST
R7020 0Ohm @
R7009 100KOhm /DGPU
R7008 10KOhm /DGPU
21 CLKREQ_PEG#
CLKREQ_PEG# R
Q7001 2N7002 /DGPU
21 CLK_PCIE_PEG_PCH
21 CLK_PCIE_PEG#_PCH

U7001A
1/19 PCI_EXPRESS

PEX_WAKE_N AJ11
PEX_RST_N AJ12
PEX_CLKREQ_N AK12
PEX_REFCLK AL13
PEX_REFCLK_N AK13

PCIENB_RXP0 C7032 0.22UF/10V PEX_TX0+ AK14
PCIENB_RXN0 C7021 0.22UF/10V PEX_TX0- AJ14
PCIEG_RXP0 AN12
PCIEG_RXN0 AM12
PEX_RX0 / PEX_RX0_N
PCIENB_RXP1 C7018 0.22UF/10V PEX_TX1+ AH14
PCIENB_RXN1 C7019 0.22UF/10V PEX_TX1- AG14
PCIEG_RXP1 AN14
PCIEG_RXN1 AM14
PEX_RX1 / PEX_RX1_N
PCIENB_RXP2 C7024 0.22UF/10V PEX_TX2+ AK15
PCIENB_RXN2 C7031 0.22UF/10V PEX_TX2- AJ15
PCIEG_RXP2 AP14
PCIEG_RXN2 AP15
PEX_RX2 / PEX_RX2_N
PCIENB_RXP3 C7020 0.22UF/10V PEX_TX3+ AL16
PCIENB_RXN3 C7022 0.22UF/10V PEX_TX3- AK16
PCIEG_RXP3 AN15
PCIEG_RXN3 AM15
PEX_RX3 / PEX_RX3_N
PCIENB_RXP4 C7023 0.22UF/10V PEX_TX4+ AK17
PCIENB_RXN4 C7028 0.22UF/10V PEX_TX4- AJ17
PCIEG_RXP4 AN17
PCIEG_RXN4 AM17
PEX_RX4 / PEX_RX4_N
PCIENB_RXP5 C7036 0.22UF/10V PEX_TX5+ AH17
PCIENB_RXN5 C7030 0.22UF/10V PEX_TX5- AG17
PCIEG_RXP5 AP17
PCIEG_RXN5 AP18
PEX_RX5 / PEX_RX5_N
PCIENB_RXP6 C7026 0.22UF/10V PEX_TX6+ AK18
PCIENB_RXN6 C7025 0.22UF/10V PEX_TX6- AJ18
PCIEG_RXP6 AN18
PCIEG_RXN6 AM18
PEX_RX6 / PEX_RX6_N
PCIENB_RXP7 C7029 0.22UF/10V PEX_TX7+ AL19
PCIENB_RXN7 C7027 0.22UF/10V PEX_TX7- AK19
PCIEG_RXP7 AN20
PCIEG_RXN7 AM20
PEX_RX7 / PEX_RX7N
PCIENB_RXP8 C7034 0.22UF/10V PEX_TX8+ AK20
PCIENB_RXN8 C7033 0.22UF/10V PEX_TX8- AJ20
PCIEG_RXP8 AP20
PCIEG_RXN8 AP21
PEX_RX8 / PEX_RX8_N
PCIENB_RXP9 C7046 0.22UF/10V PEX_TX9+ AH20
PCIENB_RXN9 C7035 0.22UF/10V PEX_TX9- AG20
PCIEG_RXP9 AN21
PCIEG_RXN9 AM21
PEX_RX9 / PEX_RX9_N
PCIENB_RXP10 C7038 0.22UF/10V PEX_TX10+ AK21
PCIENB_RXN10 C7037 0.22UF/10V PEX_TX10- AJ21
PCIEG_RXP10 AN23
PCIEG_RXN10 AM23
PEX_RX10 / PEX_RX10_N
PCIENB_RXP11 C7040 0.22UF/10V PEX_TX11+ AL22
PCIENB_RXN11 C7039 0.22UF/10V PEX_TX11- AK22
PCIEG_RXP11 AP23
PCIEG_RXN11 AP24
PEX_RX11 / PEX_RX11_N
PCIENB_RXP12 C7042 0.22UF/10V PEX_TX12+ AK23
PCIENB_RXN12 C7041 0.22UF/10V PEX_TX12- AJ23
PCIEG_RXP12 AN24
PCIEG_RXN12 AM24
PEX_RX12 / PEX_RX12_N
PCIENB_RXP13 C7047 0.22UF/10V PEX_TX13+ AH23
PCIENB_RXN13 C7043 0.22UF/10V PEX_TX13- AG23
PCIEG_RXP13 AN26
PCIEG_RXN13 AM26
PEX_RX13 / PEX_RX13_N
PCIENB_RXP14 C7049 0.22UF/10V PEX_TX14+ AK24
PCIENB_RXN14 C7048 0.22UF/10V PEX_TX14- AJ24
PCIEG_RXP14 AP26
PCIEG_RXN14 AP27
PEX_RX14 / PEX_RX14_N
PCIENB_RXP15 C7051 0.22UF/10V PEX_TX15+ AL25
PCIENB_RXN15 C7050 0.22UF/10V PEX_TX15- AK25
PCIEG_RXP15 AN27
PCIEG_RXN15 AM27
PEX_RX15 / PEX_RX15_N

N13P-GS
02V0A0000011
/DGPU

+1.05VS_VGA
PEX_IOVDD AG19 AG21 AG22 AG24 AH21 AH25
C7052 0.1UF/16V /DGPU
C7001 1UF/6.3V /DGPU
C7002 1UF/6.3V /DGPU
C7003 4.7UF/6.3V /DGPU
PLACE UNDER BGA
C7009 10UF/6.3V /DGPU
C7004 10UF/6.3V /DGPU
C7005 22UF/6.3V /DGPU
C7010 22UF/6.3V /DGPU
PLACE BETWEEN BGA AND POWER SUPPLY
PEX_IOVDDQ AG13 AG15 AG16 AG18 AG25 AH15 AH18 AH26 AH27 AJ27 AK27 AL27 AM28 AN28
C7053 0.1UF/16V /DGPU
C7008 1UF/6.3V /DGPU
C7006 1UF/6.3V /DGPU
C7007 4.7UF/6.3V /DGPU
C7011 10UF/6.3V /DGPU
20110909 Joyoung EMI Request

0928 Alfie **PEX_PLL_HVDD**

N13P-GL	N13P-GS
NC	PEX_PLL_HVDD (3.3V)

PEX_PLL_HVDD AH12
PEX_SVDD_3V3 AG12
R7021 0Ohm /GS
C7016 0.1UF/16V /DGPU
C7017 4.7UF/6.3V /DGPU
C7015 4.7UF/6.3V /DGPU

VDD_SENSE L4 NVDD_SENSE 87
GND_SENSE L5 NVDD_GND_SENSE 87
NC P8

PEX_TSTCLK_OUT R7007 200Ohm @
PEX_TSTCLK_OUT AJ26
PEX_TSTCLK_OUT# AK26

0928 Alfie **PEX_PLLVDD**

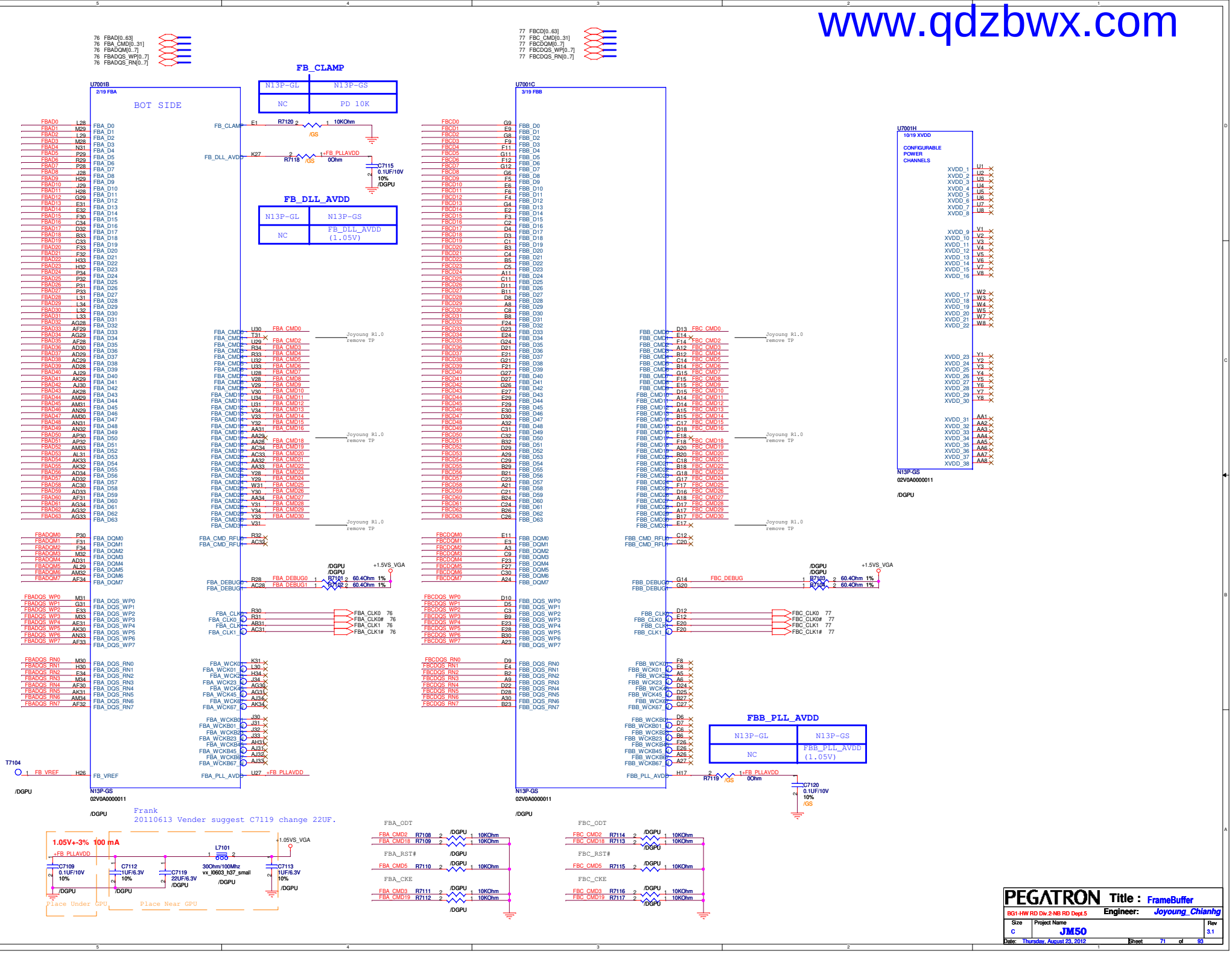
N13P-GL	N13P-GS
L7001	R7022

PEX_PLLVDD AG26
PLACE NEAR
C7061 0.1UF/16V /DGPU
PLACE NEAR BGA
C7044 1UF/6.3V /DGPU
C7045 4.7UF/6.3V /DGPU
L7001 600 30Ohm/100Mhz /GL
R7022 0Ohm /GS
+1.05VS_VGA

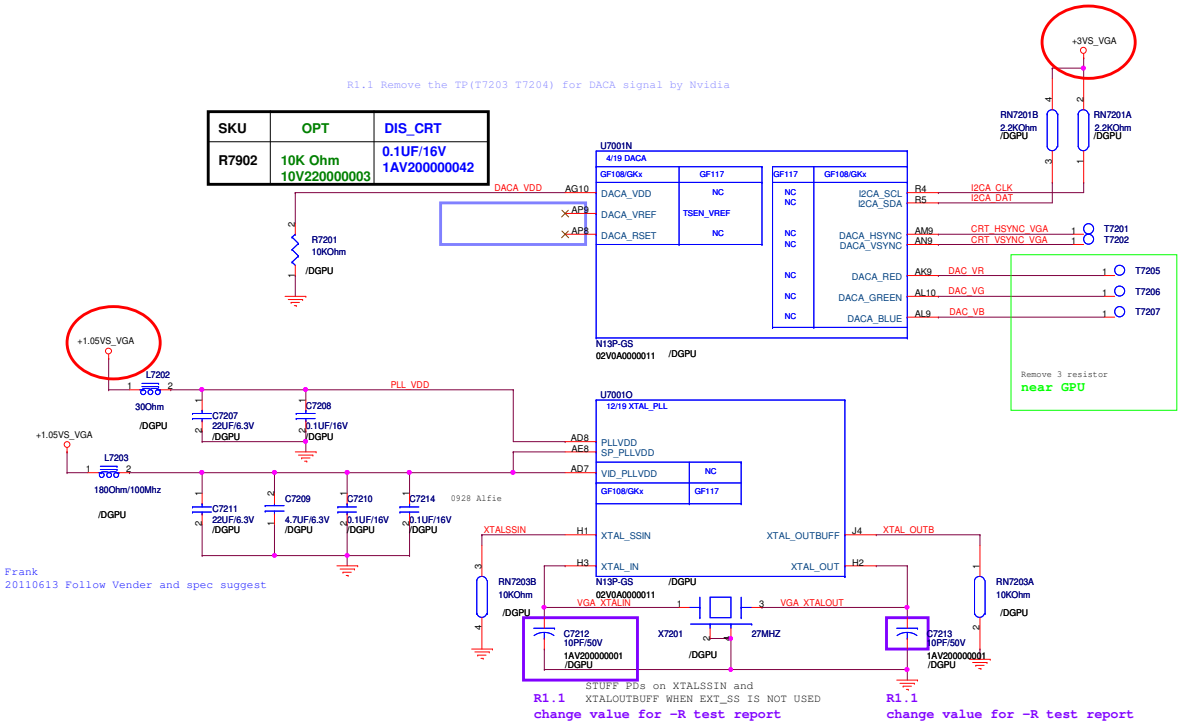
TESTMODE AK11
R7004 10KOhm /DGPU

PEX_TERMP AP29
R7003 2.49KOhm 1% /DGPU

PEGATRON	Title : PEG		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size C	Project Name JM50		Rev 3.1
	P/N <OrgAddr2>		
Date: Thursday, August 23, 2012	Sheet 70 of 93		



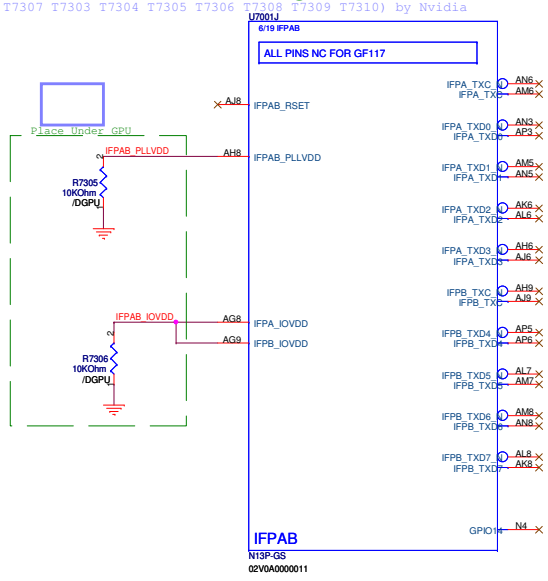
PEGATRON	Title : FrameBuffer
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg
Size: C	Project Name: JM50
Rev: 3.1	
Date: Thursday, August 23, 2012	Sheet 71 of 93



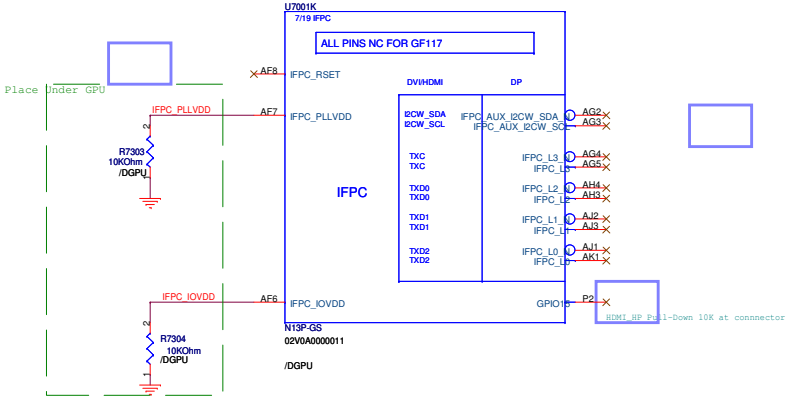
PEGATRON	Title :	FRAME BUFFER C
PEGATRON COMPUTER INC	Engineer:	Joyoung_Chianhg
Size: C	Project Name: JM50	Rev: 3.1
	P/N: <OrgAddr2>	
Date: Thursday, August 23, 2012	Sheet 72 of 93	

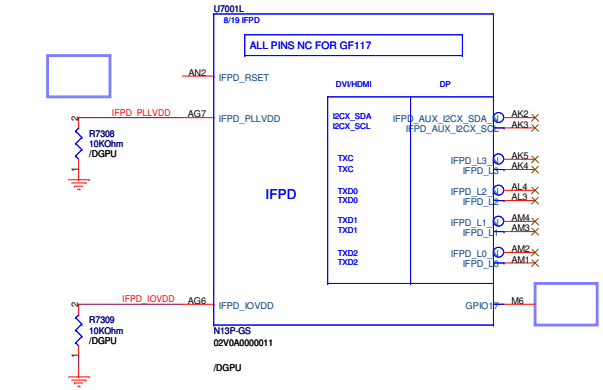
R1.1 Remove the TP (T7301 T7311 T7302 T7307 T7303 T7304 T7305 T7306 T7318 T7309 T7310) by Nvidia

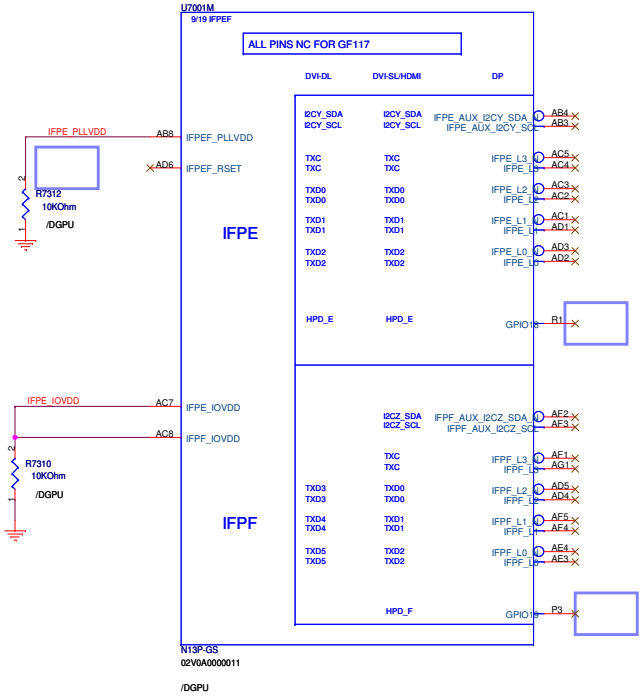
LVDS



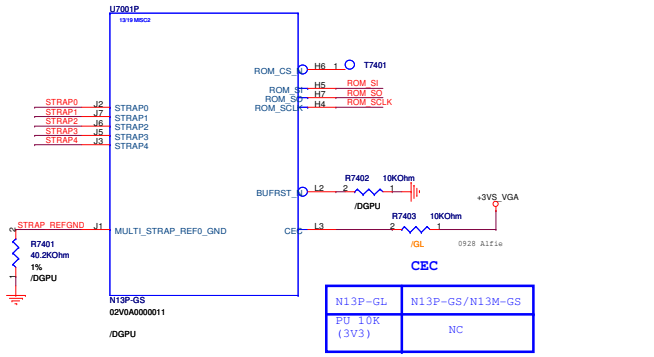
HDMI







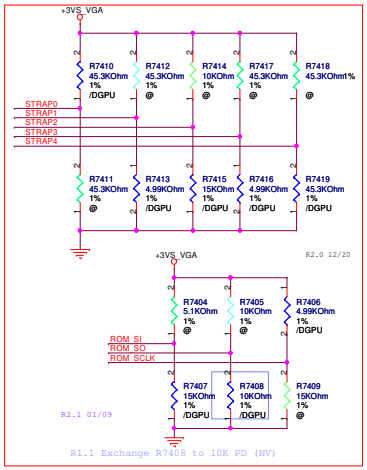
PEGATRON	Title : FRAME BUFFER C		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
	P/N: <OrgAddr2>		
Date: Thursday, August 23, 2012	Sheet 73 of 93		



CEC

N13P-GL	N13P-GS/N13M-GS
PU 10K (3V3)	NC

0928 Alfie change to N13P-GL strap



TERMINATION RESISTANCE	TERMINATION VOLTAGE 3V3 [3:0]	GND [3:0]
5K	1000 8	0000 0
10K	1001 9	0001 1
15K	1010 A	0010 2
20K	1011 B	0011 3
25K	1100 C	0100 4
30K	1101 D	0101 5
35K	1110 E	0110 6
45K	1111 F	0111 7

STRAP0

USER[3:0]

3	2	1	0	PANEL	VS/HS
0	0	0	0	XGA	-/-
0	0	0	1	XGA	+/+
0	0	1	0	SXGA	+/+
0	0	1	1	SXGA+	-/-
0	1	0	0	UXGA	+/+
1	1	1	1	FDTD	N/A

STRAP1

3GIO_PAD_CFG_ADR[3:0]

3	2	1	0	PANEL
0	0	0	0	RESERVED
0	1	1	0	NOTEBOOK
.				
.				
1	1	1	1	RESERVED

STRAP2

LOGICAL BIT	
0	PCI_DEVID[0]
1	PCI_DEVID[1]
2	PCI_DEVID[2]
3	PCI_DEVID[3]

ROM_SI_RAMCONFIG (MONO RANK)

Hynix 64Mx16 -> ram_cfg = 0x2
Samsung 64Mx16 -> ram_cfg = 0x3
Hynix 128Mx16 -> ram_cfg = 0x6
Samsung 128Mx16 -> ram_cfg = 0x7

ROM_SO

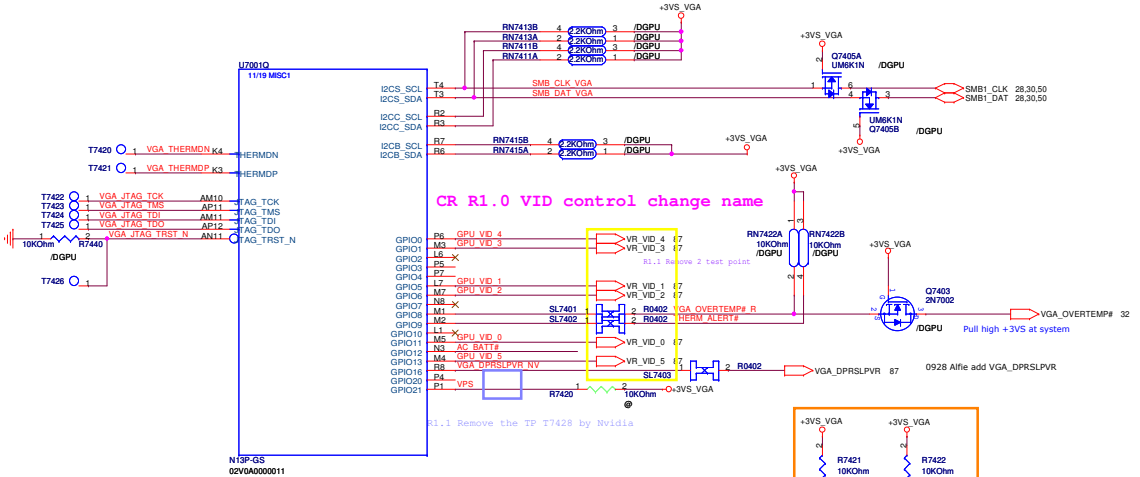
LOGICAL BIT	
3	XCLK_417
2	FB_0_BAR_SIZE
1	SMB_ALT_ADDR
0	VGA_DEVICE

ROM_SCLK

LOGICAL BIT	
3	PCI_DEVID[4]
2	SUB_VENDER
1	SLOT_CLK_CFG
0	PEX_PLL_EN_TERM

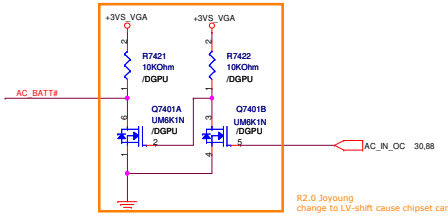
N13P-GL					
DEVICE ID	0xDE9				
STRAP0	45K PU	ROM_SCLK			15K PD
STRAP1	45K PD	ROM_SI	64x16		
STRAP2	10K PU			Hynix	15KPD
STRAP3	NC		128X16		
STRAP4	NC			Hynix	35KPD
		ROM_SO			30K PD

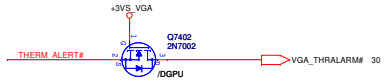
VRAM need change BOM



CR R1.0 VID control change name

R1.1 Remove L_VDDEN_VGA & LCD_BKEN_VGA signals, No function request on the pin (NV)





PEGATRON

Title : FRAME BUFFER A

PEGATRON COMPUTER INC

Engineer: Joyoung_Chianhg

Size	Project Name	Rev
A2	JM50	3.1
	P/N <OrgAddr2>	

Date: Thursday, August 23, 2012 Sheet 74 of 93

+VGA_VCORE

U7001E
14/19 NVVDD

PLACE UNDER GPU

C7511 C7510 C7513 C7512 C7515 C7514 C7517 C7516 — 0.1UF/16V /DGPU

C7519 C7518 C7521 C7520 C7523 C7522 C7525 C7524 — 4.7UF/6.3V /DGPU

C7527 C7526 C7528 C7529 C7531 C7530 C7532 — 4.7UF/6.3V /DGPU

GND

0928 Alfie change 15pcs 10uF to 4.7uF , follow NV suggest

CE7501 330UF/2V 1BV080000010

C7534 C7533 C7535 C7536 C7537 — 4.7UF/6.3V /DGPU

C7552 — 22UF/6.3V /DGPU

C7553 — 47UF/4V /DGPU

PLACE NEAR GPU

0929 Alfie change 5pcs 10uF to 4.7uF , follow NV suggest

N13P-GS
02V0A0000011
/DGPU

U7001F
18/19 NC/VDD33

C7507 C7501 C7504 C7505 — 0.1UF/16V /DGPU — PLACE NEAR BALLS

C7502 — 1UF/6.3V /DGPU

C7503 — 4.7UF/6.3V /DGPU — PLACE NEAR BGA

+3VS_VGA

R7501 0Ohm /DGPU

N13P-GS
02V0A0000011
/DGPU

Frank
20110613 Follow Vender and spec suggest=>Remove C7506, C7508

Frank
20110613 Follow Vender and spec suggest
=> Add C7542, C7543, C7544, C7545 and C7556 mount
Remove C7540, C7561, C7558, C7649
Change C7541, C7557 to 10uF

+1.5VS_VGA

U7001D
15/19 FBVDDQ

C7539 C7559 C7542 C7544 C7538 C7555 C7554 C7541 — 0.1UF/16V /DGPU — 1UF/6.3V /DGPU — 4.7UF/6.3V /DGPU — 10UF/6.3V /DGPU

C7551 C7556 C7543 C7545 C7560 C7562 C7550 C7557 — 0.1UF/16V /DGPU — 1UF/6.3V /DGPU — 4.7UF/6.3V /DGPU — 10UF/6.3V /DGPU

CALIBRATION PIN	GDDR5
FB_CALx_PD_VDDQ	40
FB_CALx_PU_GND	40
FB_CALx_TERM_GND	60

FB_VDDQ_SENSE — F1 — FBVDDQ_SENSE — T7508
FB_GND_SENSE — F2 — FBVDDQ_GND_SENSE — T7509
FB_CAL_PD_VDDQ — J27 — FB_CAL_PD_VDDQ
FB_CAL_PU_GND — H27 — FB_CAL_PU_GND
FB_CAL_TERM_GND — H25 — FB_CAL_TERM_GND

PLACE CLOSE TO GPU BALLS
/DGPU R7507 40.2Ohm
/DGPU R7509 42.2Ohm
/DGPU R7510 51.1Ohm 10V220000319
+1.5VS_VGA
GND

N13P-GS
02V0A0000011
/DGPU

Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm
Joyoung
20110913 Follow Vendor spec PUN-05893-001_v02=>Change R7510 to 51.1 ohm

U7001G
18/19 GND_1/2

U7001I
17/19 GND_2/2

GND_OPT1 — C16
GND_OPT2 — W32
Optional CMO GNDs (2)
NC for 4-Lyr cards

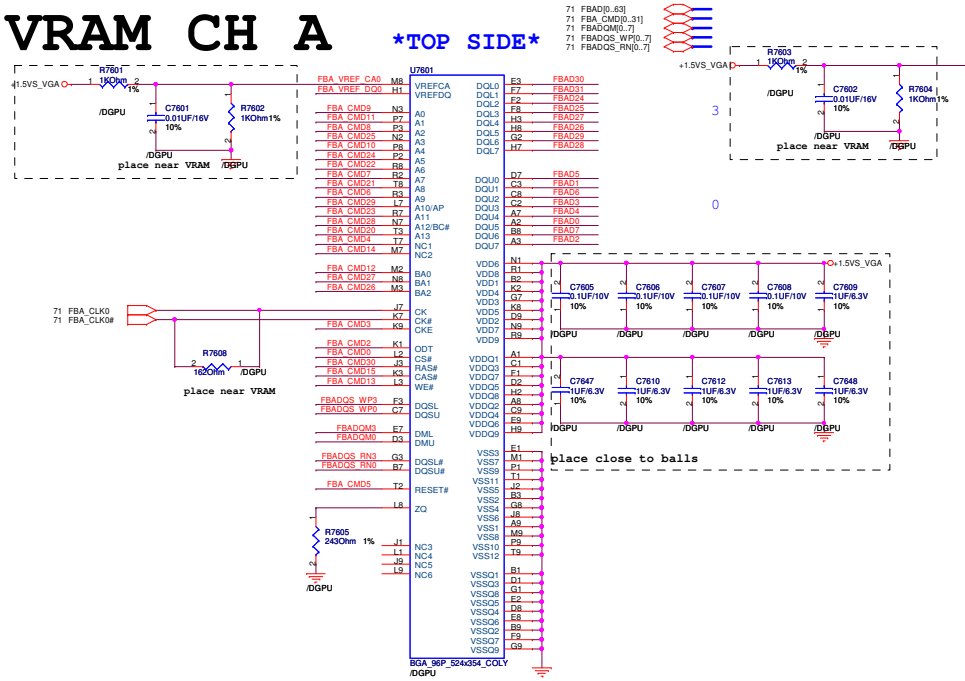
N13P-GS
02V0A0000011
/DGPU

0612 R3.1 EMI

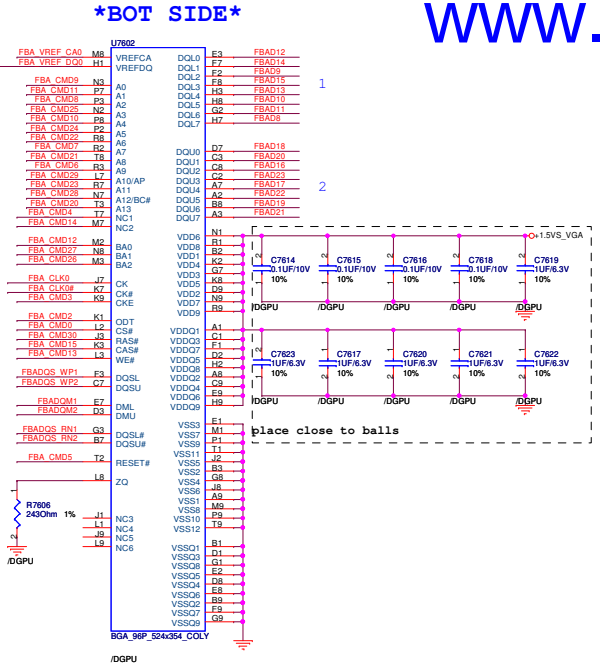
PEGATRON	Title : FRAME BUFFER C	
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 75 of 93	

VRAM CH A

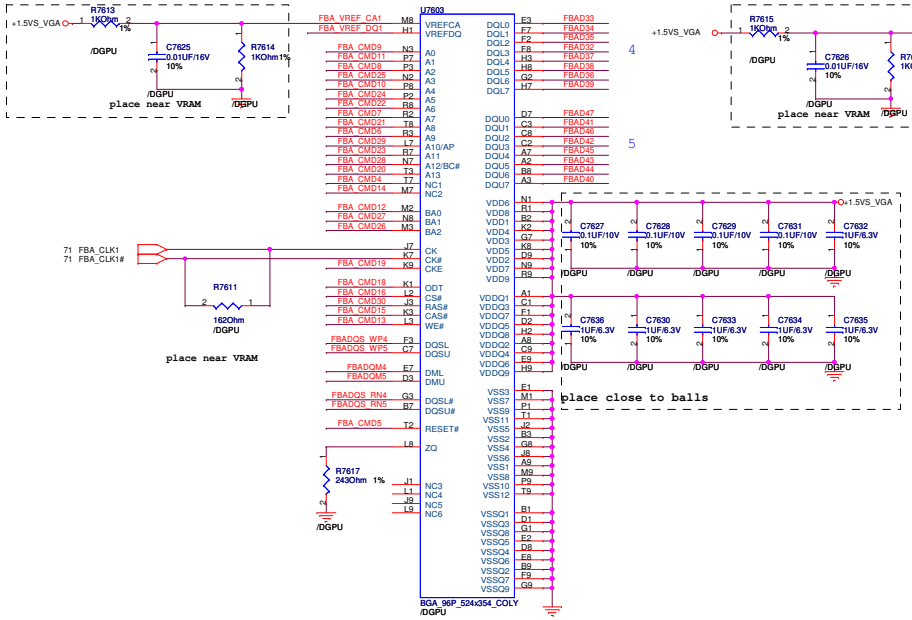
TOP SIDE



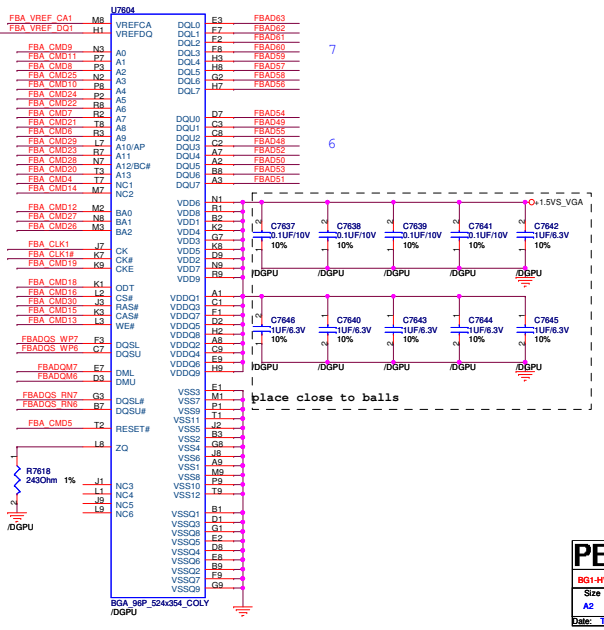
BOT SIDE



TOP SIDE



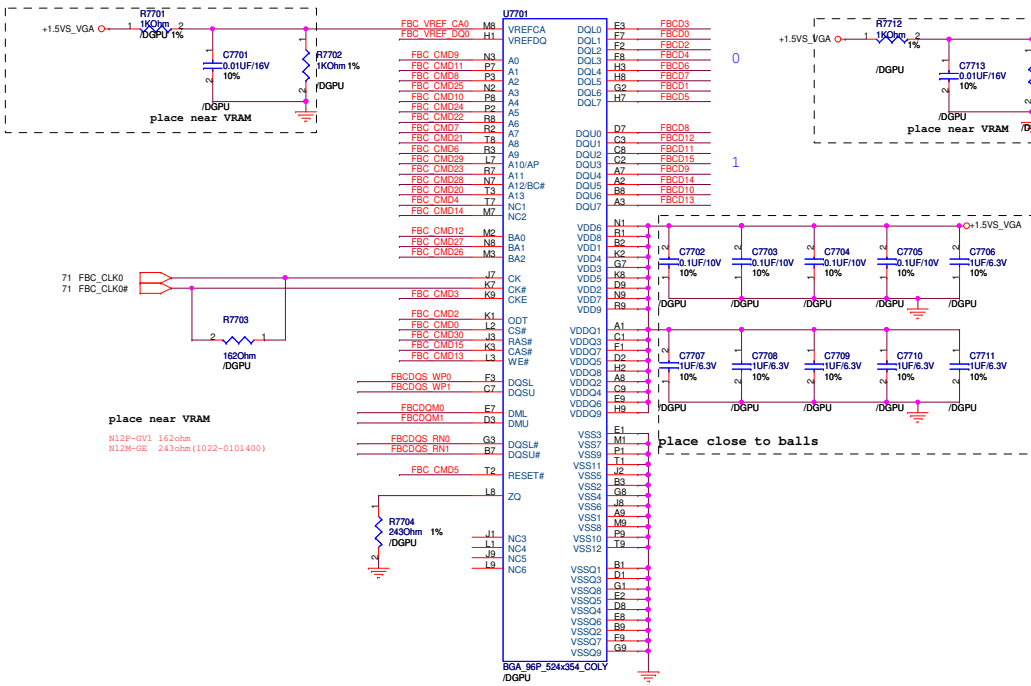
BOT SIDE



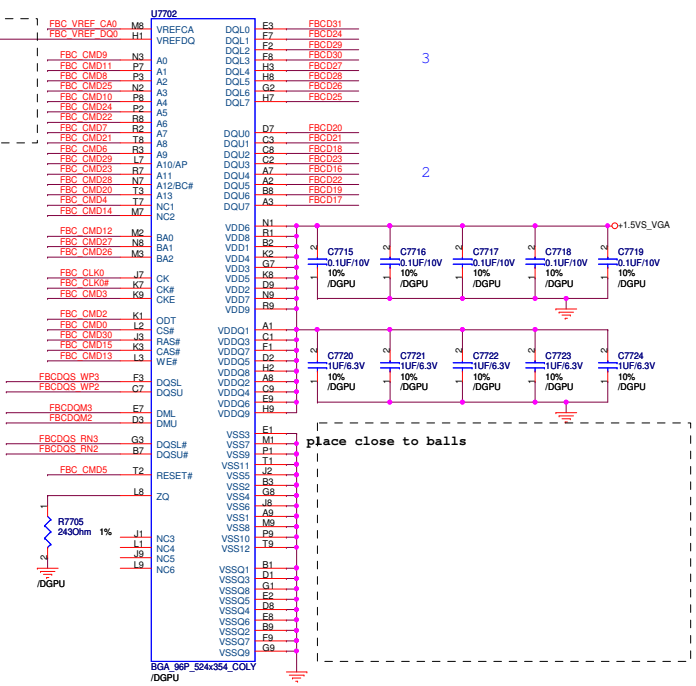
PEGATRON	Title : FRAME BUFFER A		
BG1-HW RD Div.2-NB RD Dep15	Engineer: Joyoung_Chianhg		
Size: A2	Project Name: JM50	Rev: 3.1	
Date: Thursday, August 23, 2012	Sheet 76 of 93		

VRAM CH C

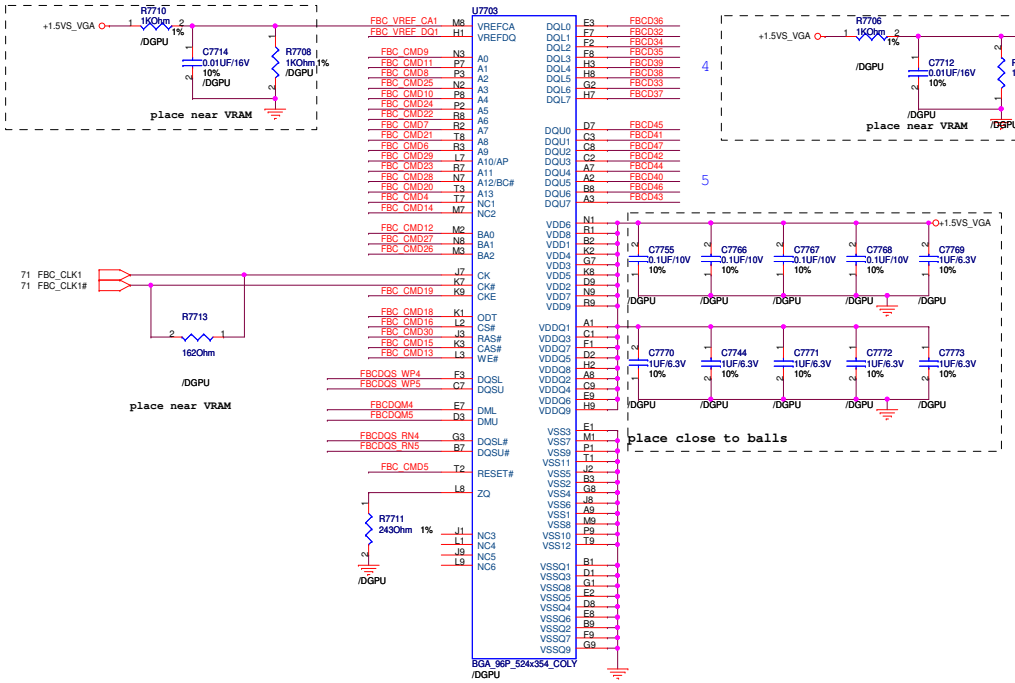
TOP SIDE



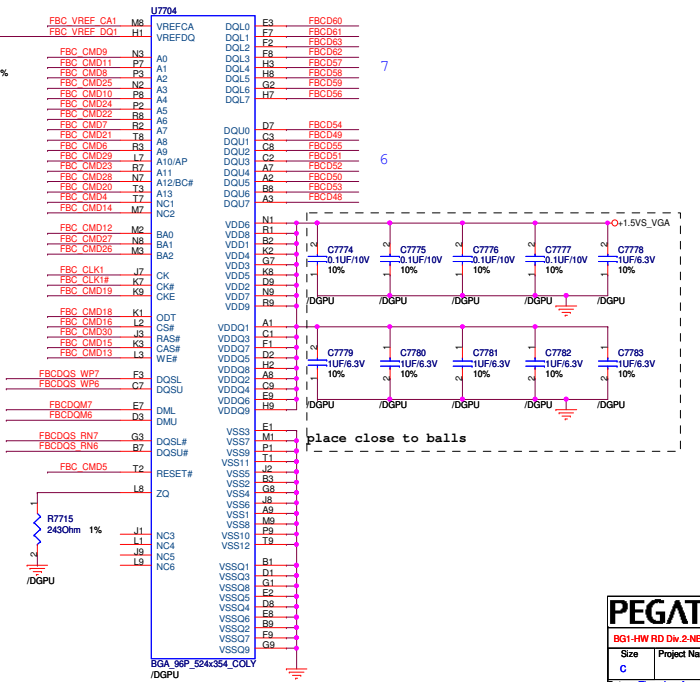
BOT SIDE



TOP SIDE



BOT SIDE

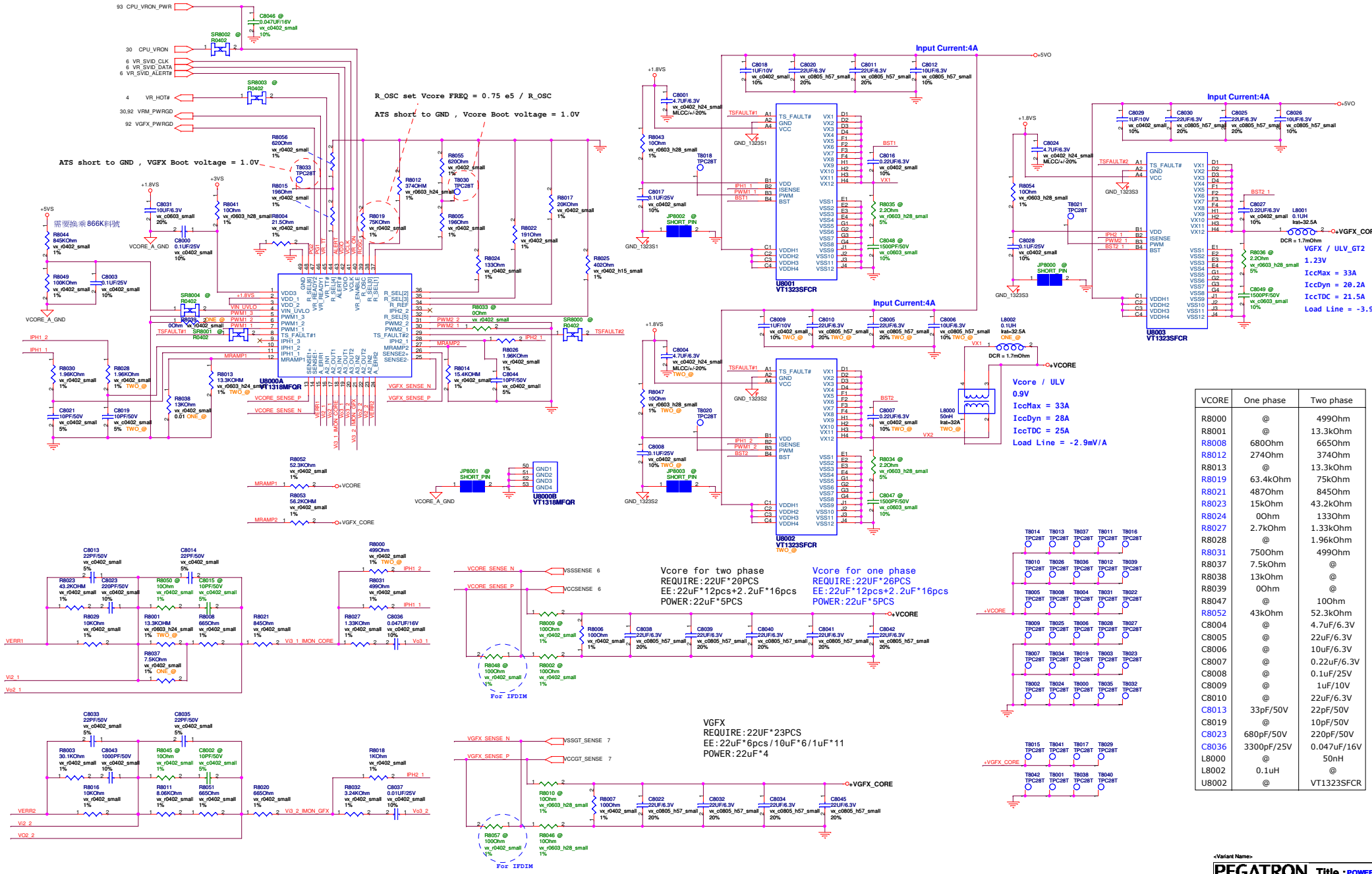


PEGATRON	Title : FRAME BUFFER B		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 77 of 93		

PEGATRON	Title : Connector, LED		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50	P/N: <OrgAddr2>	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 78 of 93		

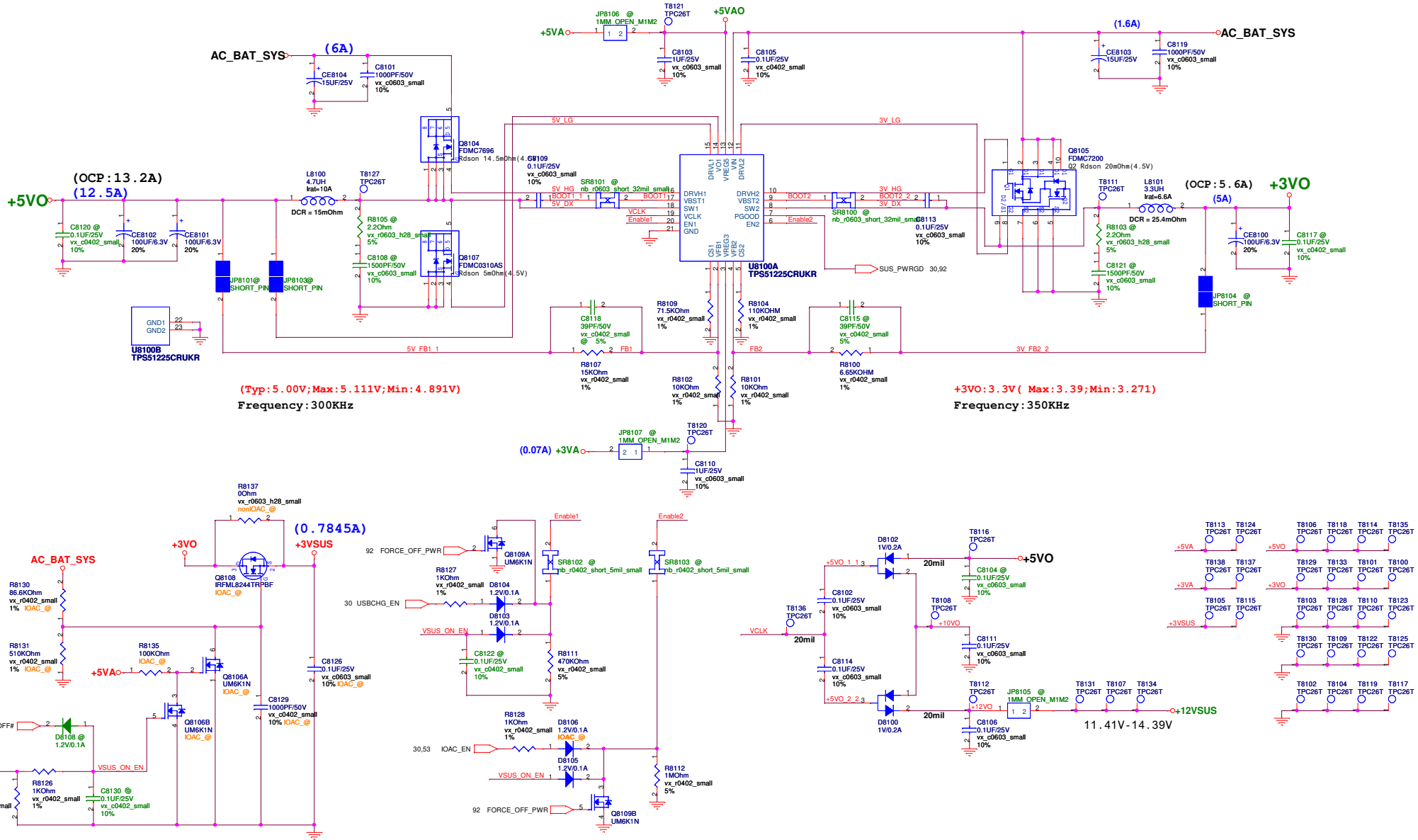
PEGATRON	Title : GPU PWR/GND		
PEGATRON COMPUTER INC	Engineer: Joyoung_Chianhg		
Size: C	Project Name: JM50		Rev: 3.1
	P/N: <OrgAddr2>		
Date: Thursday, August 23, 2012	Sheet 79 of 93		

+VCORE & +VGFX POWER SUPPLY



VCORE	One phase	Two phase
R8000	@	499Ohm
R8001	@	13.3kOhm
R8008	680Ohm	665Ohm
R8012	274Ohm	374Ohm
R8013	@	13.3kOhm
R8019	63.4kOhm	75kOhm
R8021	487Ohm	845Ohm
R8023	15kOhm	43.2kOhm
R8024	0Ohm	133Ohm
R8027	2.7kOhm	1.33kOhm
R8028	@	1.96kOhm
R8031	750Ohm	499Ohm
R8037	7.5kOhm	@
R8038	13kOhm	@
R8039	0Ohm	@
R8047	@	10Ohm
R8052	43kOhm	52.3kOhm
C8004	@	4.7uF/6.3V
C8005	@	22uF/6.3V
C8006	@	10uF/6.3V
C8007	@	0.22uF/6.3V
C8008	@	0.1uF/25V
C8009	@	1uF/10V
C8010	@	22uF/6.3V
C8013	33pF/50V	22pF/50V
C8019	@	10pF/50V
C8023	680pF/50V	220pF/50V
C8036	3300pF/25V	0.047uF/16V
L8000	@	50nH
L8002	0.1uH	@
U8002	@	VT1323SFCR

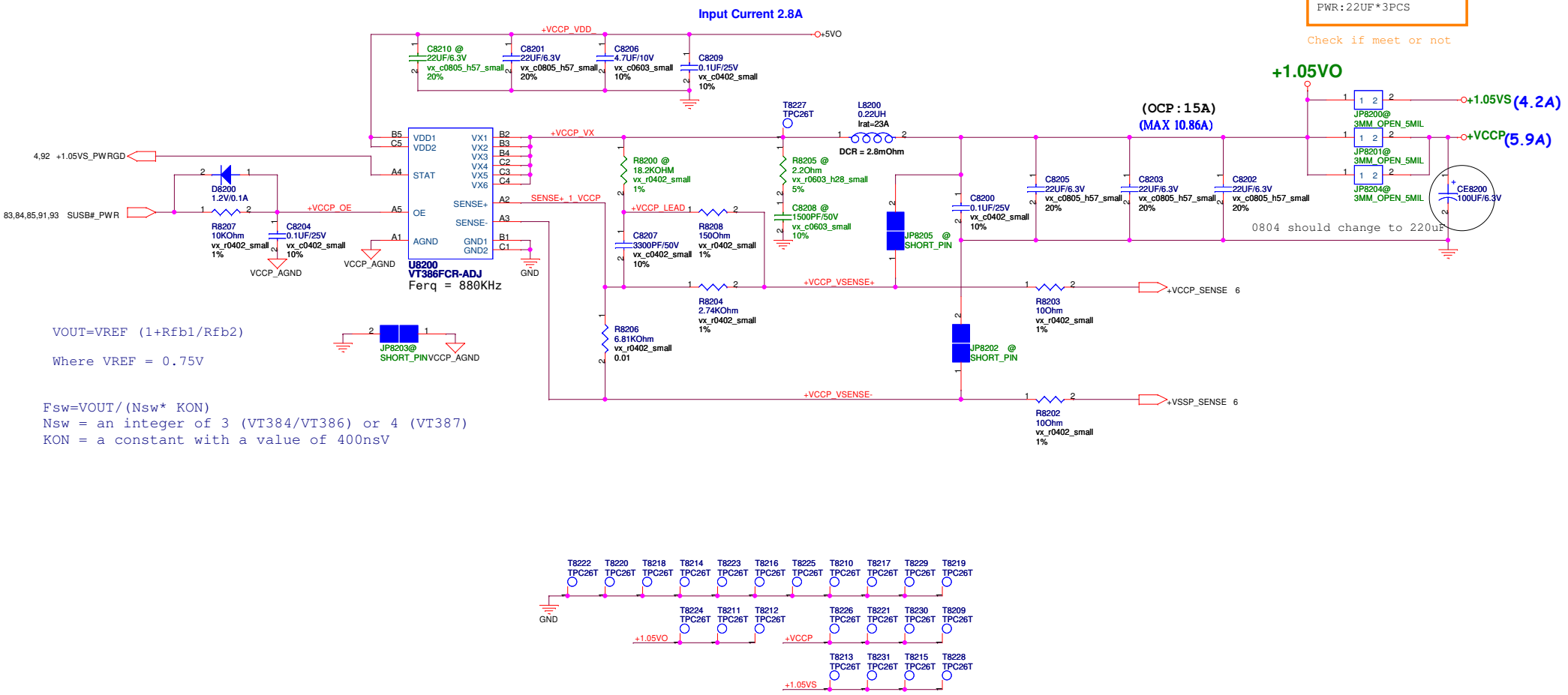
+5VO & +3VO POWER SUPPLY



+1.05VO POWER SUPPLY

11/07/21
+1.05VS & +VCCP
REQUIRE:22UF*18PCS
EE:10UF*10PCS/1uF*26
PWR:22UF*3PCS

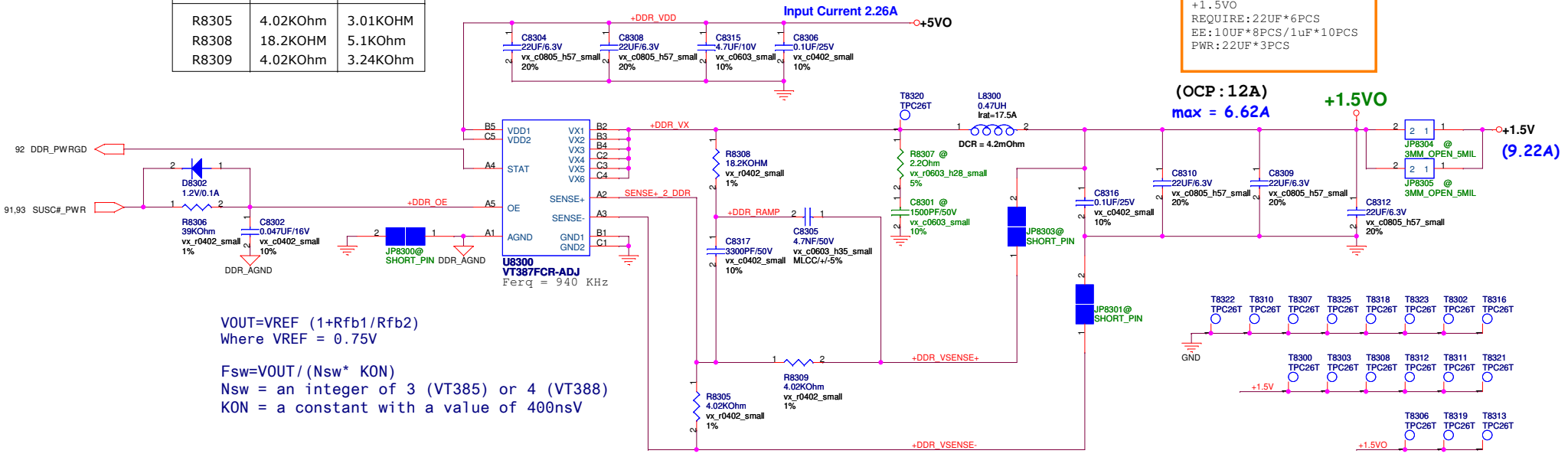
Check if meet or not



+1.5VO POWER SUPPLY

1.5VO	UMA	DSC
Vout	1.5V	1.557V
R8305	4.02KOhm	3.01KOHM
R8308	18.2KOHM	5.1KOhm
R8309	4.02KOhm	3.24KOhm

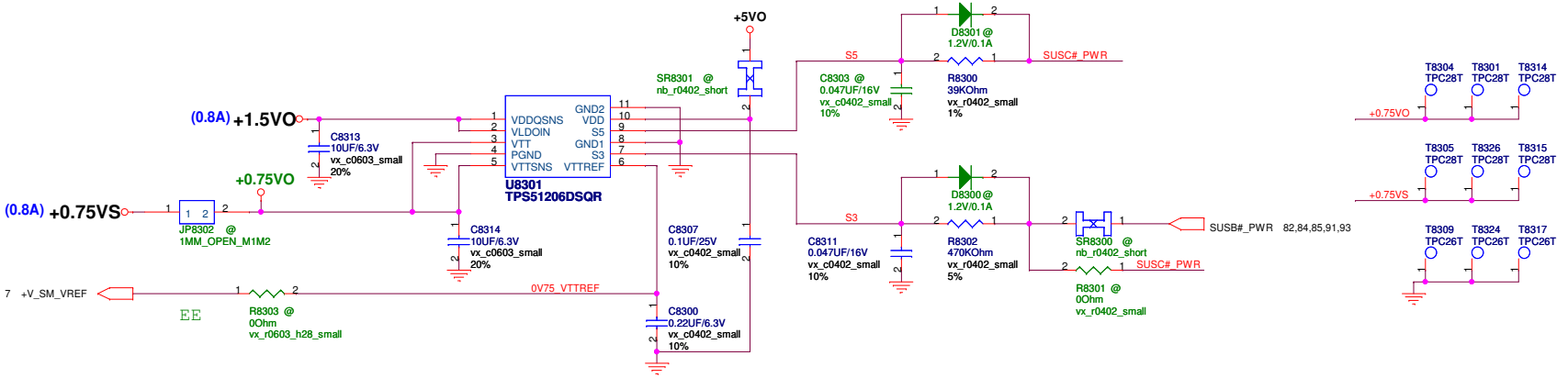
11/07/21
+1.5VO
REQUIRE:22UF*6PCS
EE:10UF*8PCS/1uF*10PCS
PWR:22UF*3PCS



VOUT=VREF (1+Rfb1/Rfb2)
Where VREF = 0.75V

Fsw=VOUT/(Nsw* KON)
Nsw = an integer of 3 (VT385) or 4 (VT388)
KON = a constant with a value of 400nsV

+0.75VS POWER SUPPLY



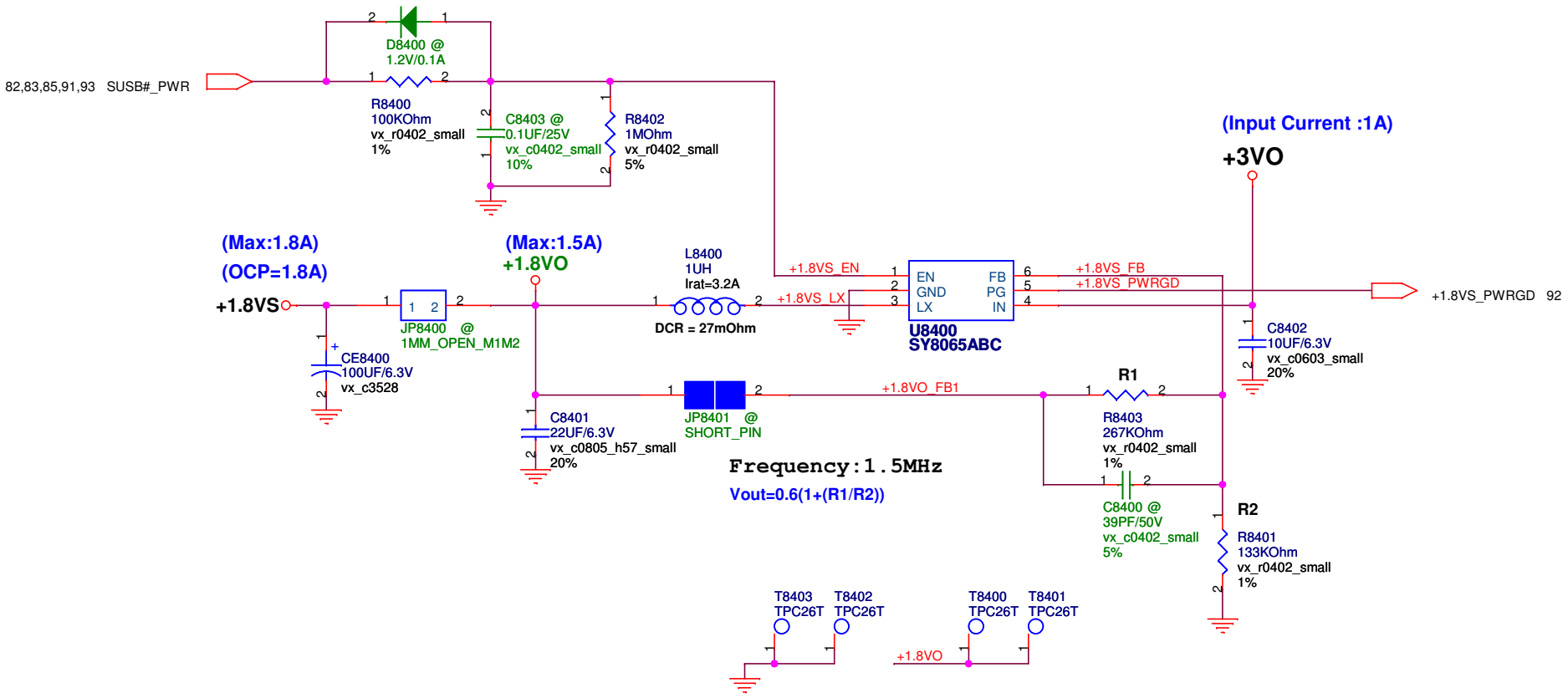
<Variant Name>

PEGATRON Title : POWER_DDR & VTT
Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 83 of 94

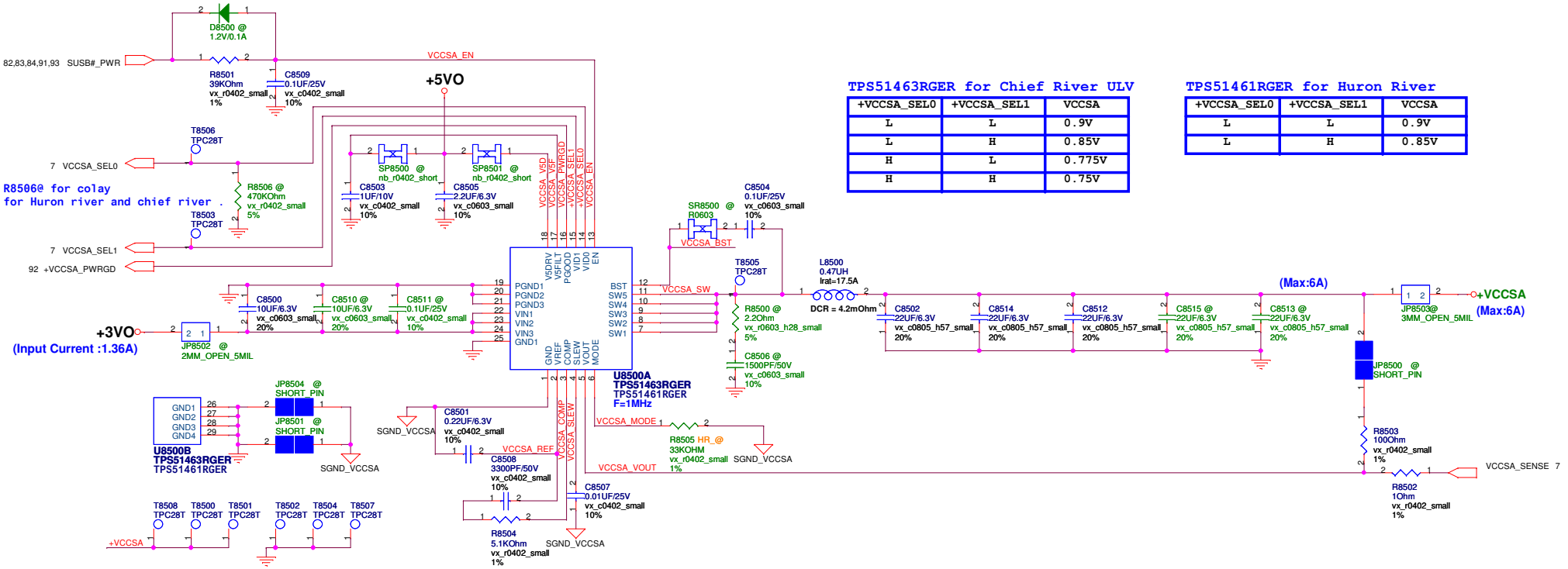
+1.8VS POWER SUPPLY



<Variant Name>

PEGATRON	Title : POWER_+1.8VS	
	Engineer: Clark Liang	
Size: Custom	Project Name: JM50	Rev: 1.0
Date: Thursday, August 23, 2012	Sheet 84 of 94	

VCCSA POWER SUPPLY



TPS51463RGER for Chief River ULV

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

TPS51461RGER for Huron River

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.85V

<Variant Name>

PEGATRON Title :POWER_+VCCSA_0.85VS

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 85 of 94

<Variant Name>

PEGATRON

Title : POWER_N/A

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

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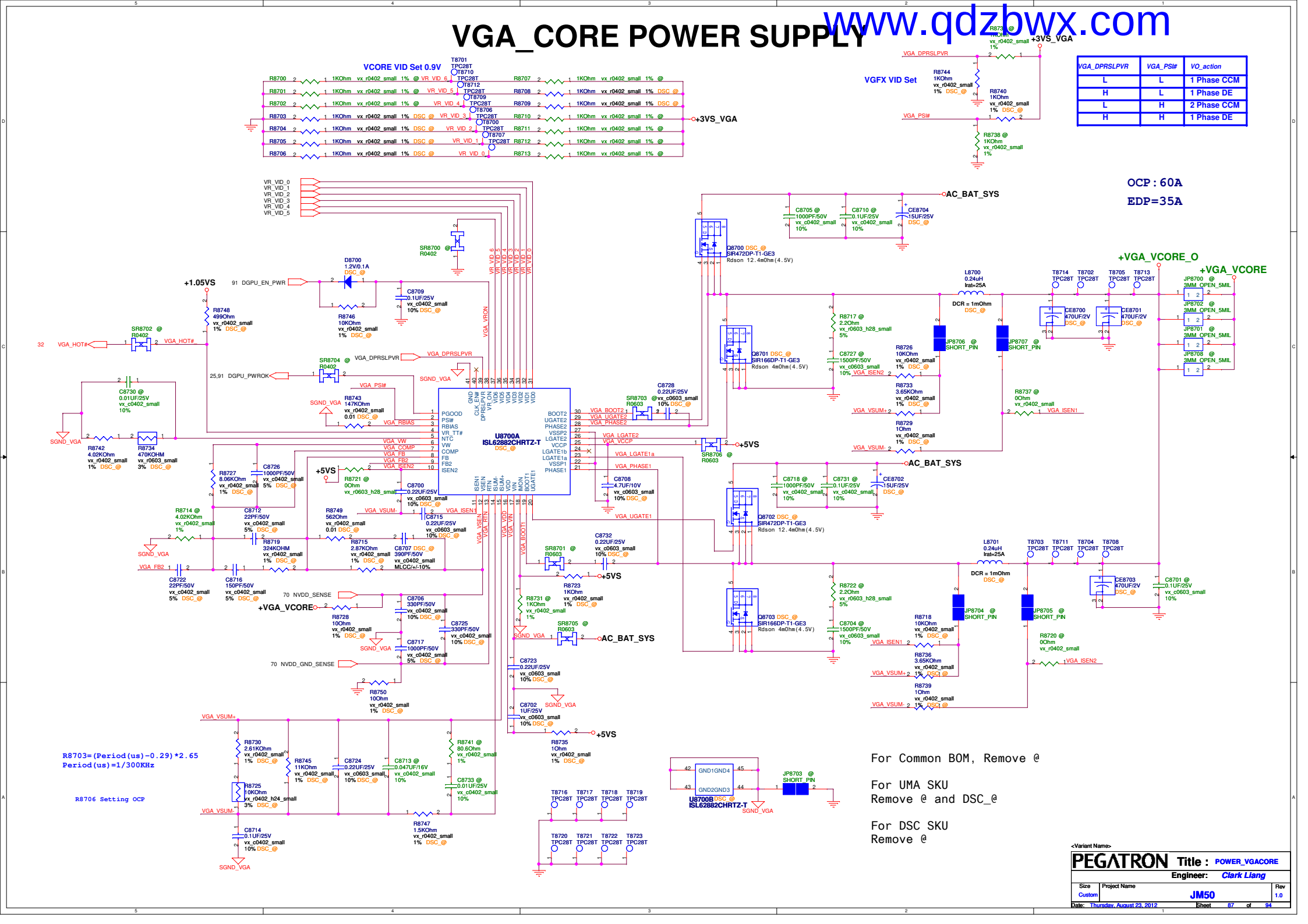
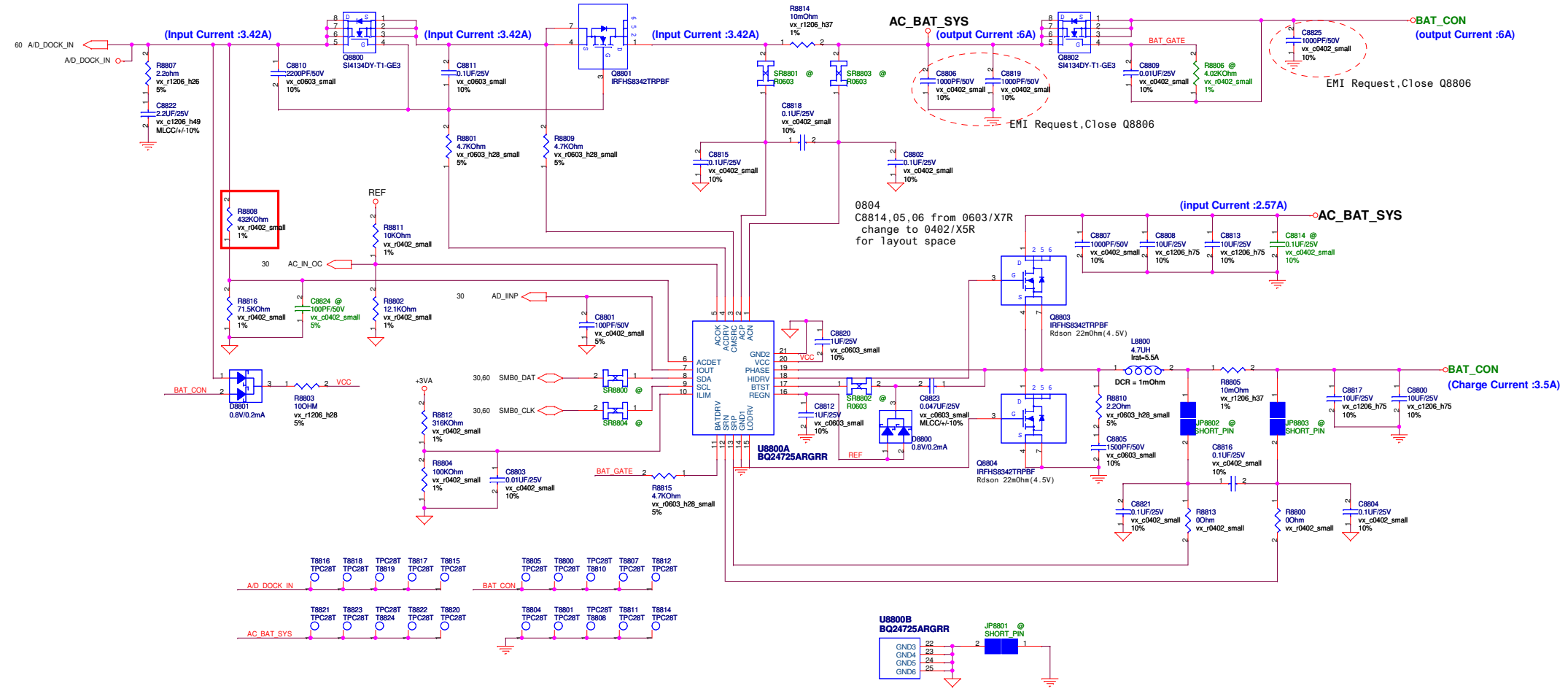
VGA_CORE POWER SUPPLY



VGA_DPRSLPVR	VGA_PSI#	VO_action
L	L	1 Phase CCM
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

BATTERY CHARGER



<variant_name>

PEGATRON Title : POWER_CHARGER

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 88 of 94

<Variant Name>

PEGATRON

Title : POWER_N/A

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 89 of 94

BATTERY IN DETECT

<Variant Name>

PEGATRON

Title : POWER_DETECT

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

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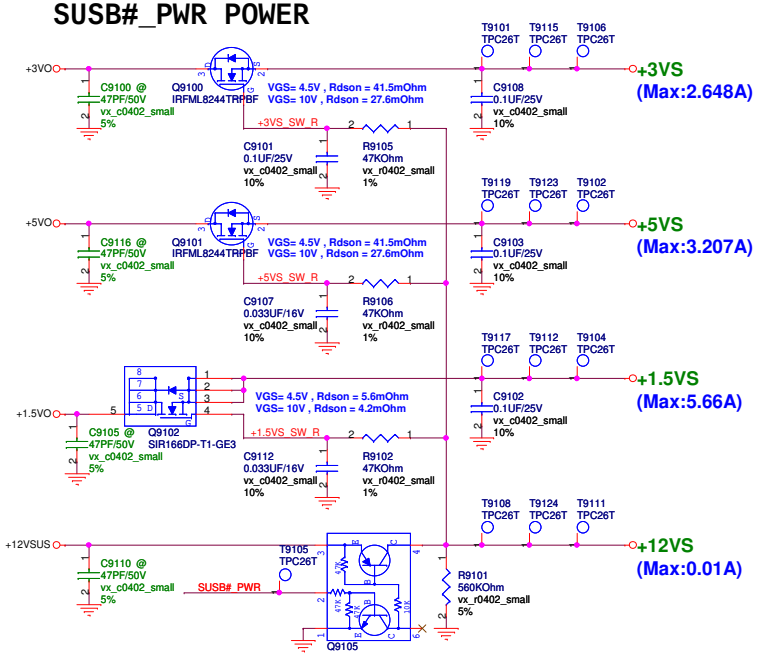
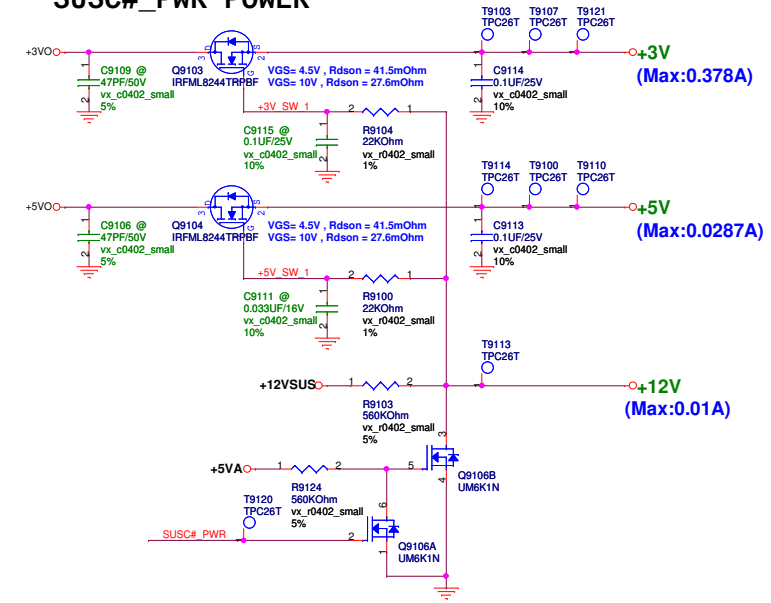
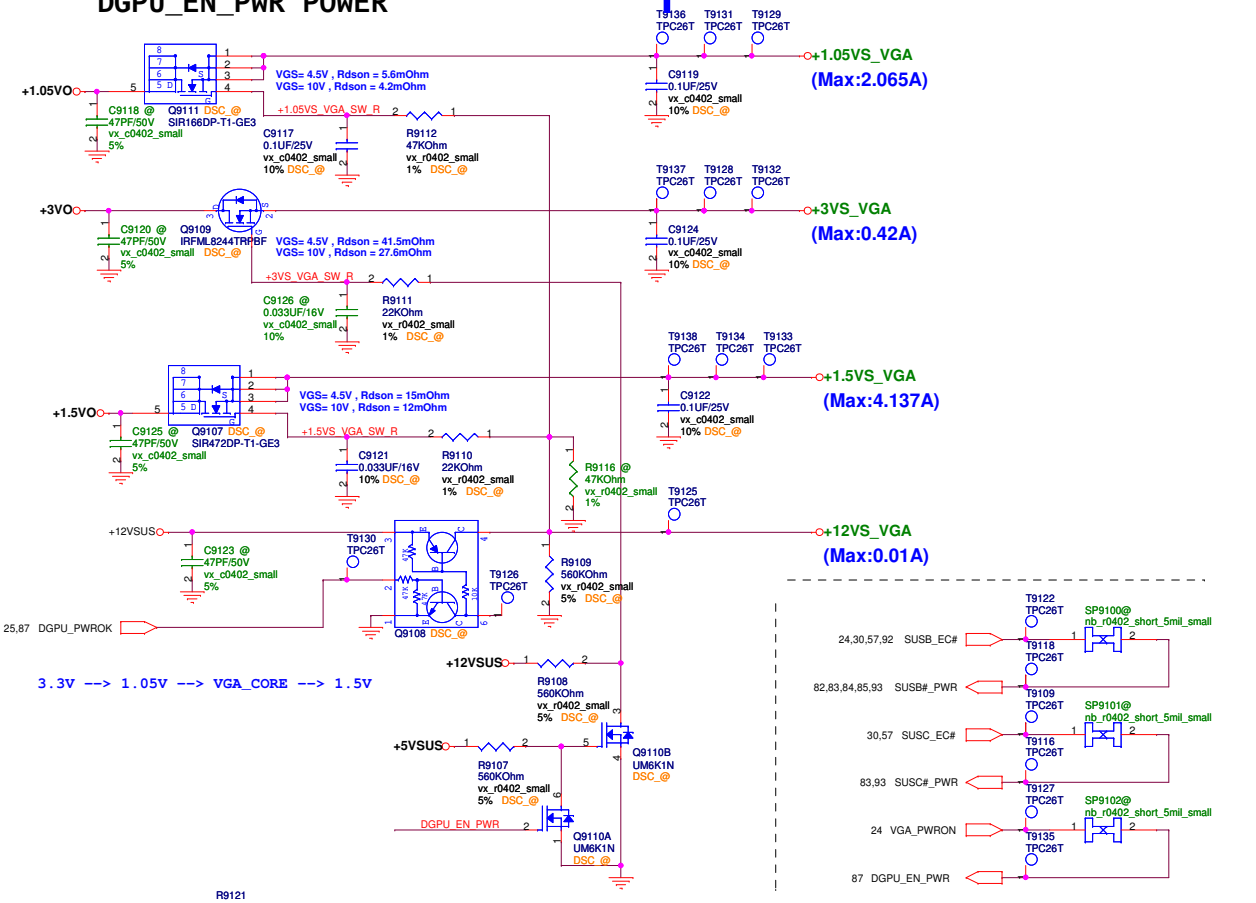
SUSB#_PWR POWER



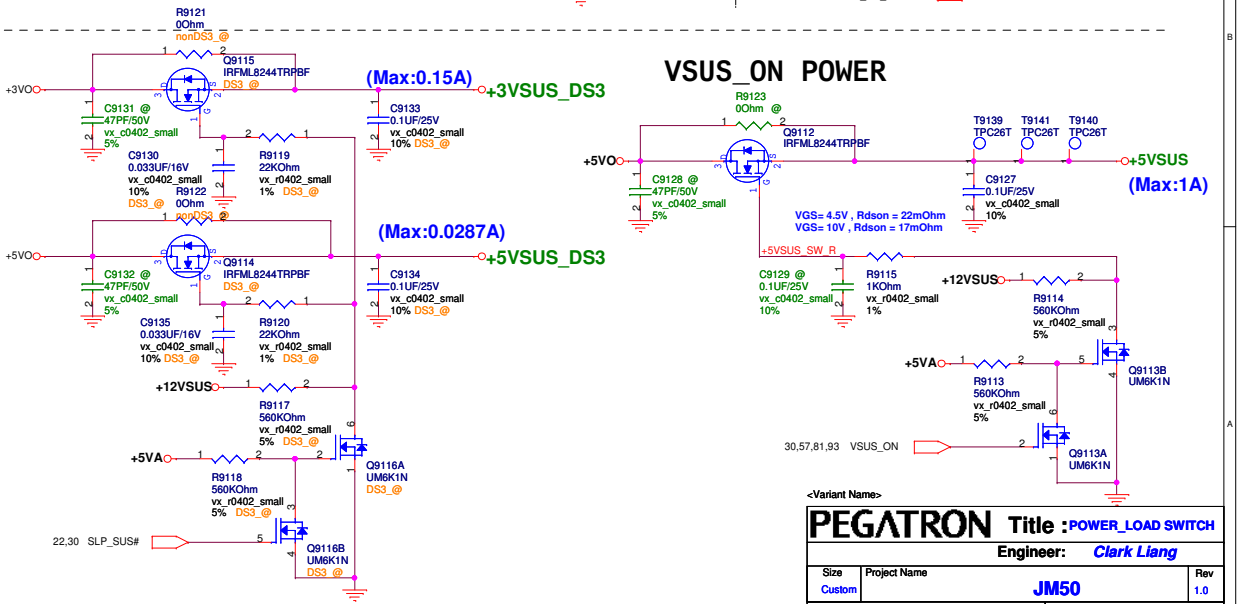
SUSC#_PWR POWER



DGPU_EN_PWR POWER



VSUS_ON POWER



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

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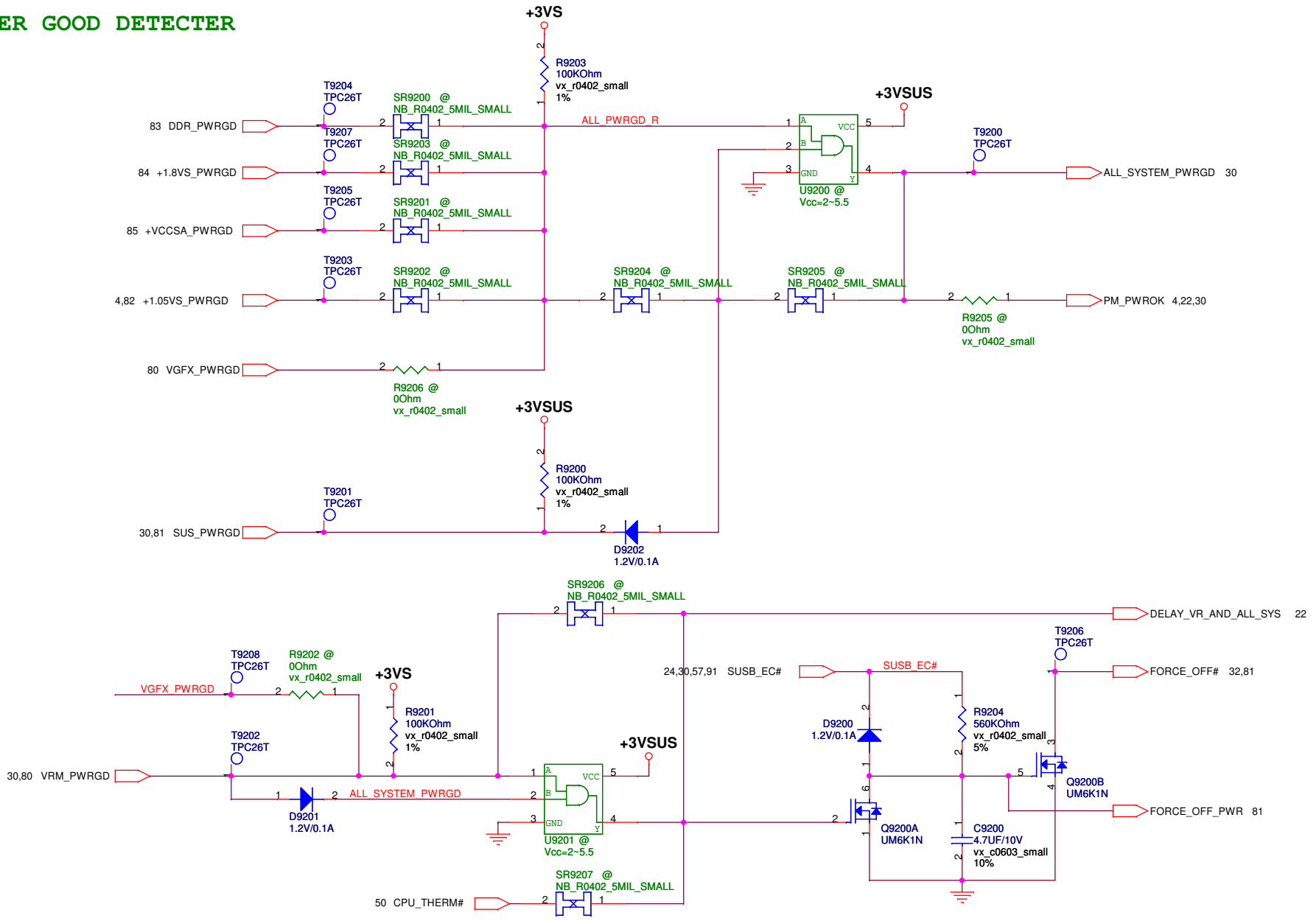
POWER GOOD DETECTER



<Variant Name>

PEGATRON Title : POWER_PROTECT

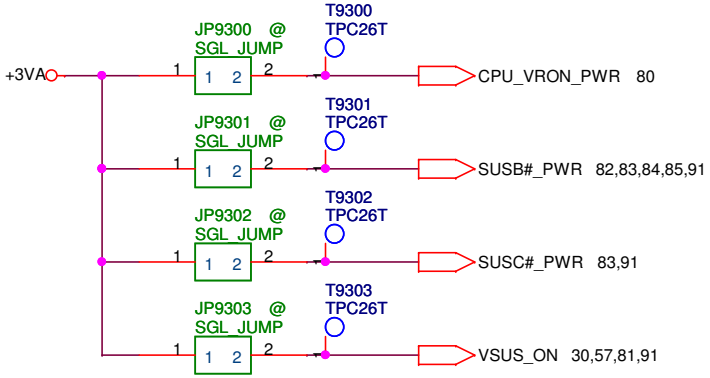
Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

Date: Thursday, August 23, 2012 Sheet 92 of 94

AC_BAT_SYS	AC_BAT_SYS	45,53,81,87,88
BAT_CON	BAT_CON	60,88
+5VA	+5VA	37,60,81,91
+3VA	+3VA	6,20,26,27,30,31,57,59,60,81,88
+5VO	+5VO	52,65,80,81,82,83,85,91
+3VO	+3VO	53,81,84,85,91
+1.8VO	+1.8VO	60,84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+0.75VO	+0.75VO	83
+12VSUS	+12VSUS	28,51,81,91
+5VSUS	+5VSUS	51,57,59,91
+3VSUS	+3VSUS	4,22,24,28,30,60,81,92
+12V	+12V	60,91
+5V	+5V	57,59,60,91
+3V	+3V	24,45,57,59,61,91
+1.5V	+1.5V	5,16,17,18,57,60,83
+12VS	+12VS	28,36,48,91
+5VS	+5VS	27,36,37,48,50,51,57,80,87,91
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+1.8VS	+1.8VS	7,25,26,57,80,84
+1.5VS	+1.5VS	7,26,53,57,91
+1.05VS	+1.05VS	26,27,57,82,87
+VCCSA	+VCCSA	7,85
+0.75VS	+0.75VS	16,17,57,83
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+12VS_VGA	+12VS_VGA	60,91
+3VS_VGA	+3VS_VGA	57,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	57,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	57,70,71,72,91

FOR POWER TEST



<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Clark Liang

Size	Project Name	Rev
Custom	JM50	1.0

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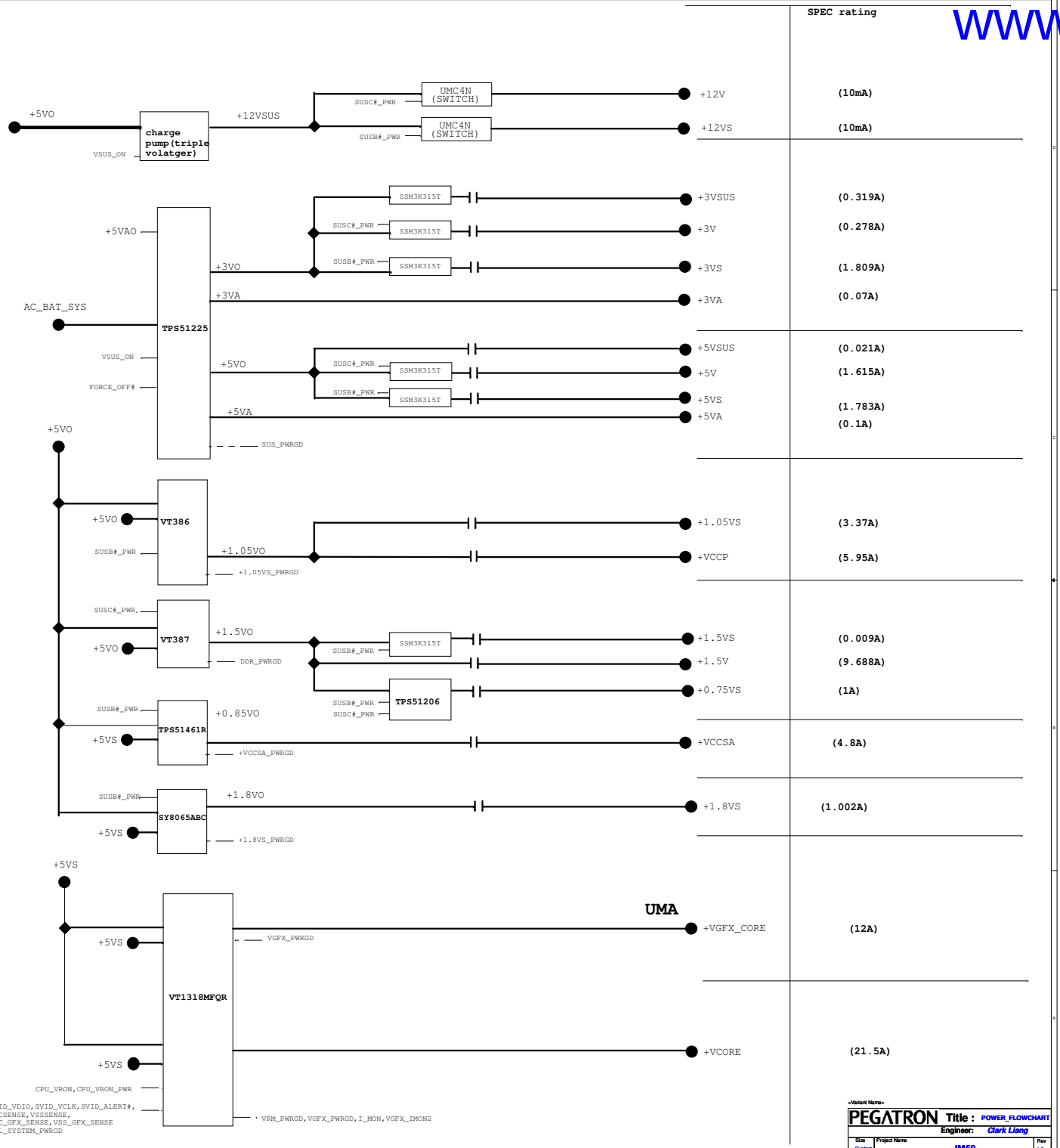

PEGATRON	Title : ****	
BG1\HW1	Engineer: *Joyoung_Chianhg*	
Size: A	Project Name: **JM50**	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 96 of 93	

SR BOM change

SR1.1 Un-mount Q5602, Q5601 and mount R5323 and R5310

SR1.2 CE5001 un-mount

SR1.3 L3602 mount

SR1.4 R7005 un-mount

SR1.5 R7410 change 10K ohm

SR1.6 R4504 change 10K ohm for LVDS backlight

SR1.7 R7430, R7432, R7433 un-mount

SR1.8 R7608, R7611 change 162 ohm

ER

ER1.1 PI pin connect to ESD and VDD pin reserve 0.1 uF cap
ER1.2 Add diode and reserve 0 ohm for AC adapter plug in /out voice
ER1.3 U5201 change G547G1P81U for Desing IP
ER1.4 Add Card Reader LED
ER1.5 J3701, J3702, J4601, J5201, J5304,J5001 chang connector
ER1.6 R6505~R6508 change 0603 size
ER1.7 D4801 contact to 2.2K ohm for EA solution in HDMI issue
ER1.8 CPU_THERM# contact to FORCE_OFF#
ER1.9 RTC battery connector (J2001)Pin1, Pin2 swap
ER1.10 D3707, D4618, D5201, D5301, D6502, D6503, D6802 VDD pin reserve 0.1 uF cap
ER1.11 R3720 R3721 change 51ohm for consumer spec in HP
ER1.12 L4601, L4602, L4603 change 27nH and add C4622, C4623, C4624 for EA solution in CRT
ER1.13 L5301, L5302, L5306 change 0 ohm and L5305 change short pin,
C5321, C5327,C5307, C5322, C5315, C5305, C5313 change umount
ER1.14 Change R4566 from 300(0603) to 150(0402) for LVDS power sequence solution
ER1.15 USB port 0 and port 1 swap
ER1.16 Vcore_add CE8002&CE8006 to replace CE0601&CE0602
ER1.17 VGFX_CORE(IGPU) add CE8007 to replace CE0705
ER1.18 reserve M_VREF schematic
ER1.19 Reserve C2623, C2624, C4514, C4515 for WLAN solution
ER1.20 Reserve C4510, C4512, C4513 for 3G and L6002~L6004, L4502 change 47 ohm Bead
ER1.21 C6007, C6006 mount for WLAN
ER1.22 RN3002 change 2R4P
ER1.23 LED and BT schematic change to LED board
ER1.24 LED power change 5VSUS, so R5618, R5616, R5623 change 560 ohm
ER1.25 VRAM change co-lay footprint
ER1.26 Reserve C5601, C5602, C5603, C6356, C6357 to 47pF for RF request
ER1.27 Reserve C4516, C4517 to 10pF for RF request
ER1.28 U6504,U6505 change AZ3028 for EMI request
ER1.29 D6401, D6501, D6502 change ESD AZ5023 in for EMI request in LAN function
ER1.30 Add C6010 C6011 for EMI request
ER1.31 Merge Q6704 and remove U6704
ER1.32 D3720 change to mount for EMI request
ER1.34 Reserve C6913(47PF), C6902(0.1uF), C6623(47PF), C6606(22uF) for 3G
ER1.35 L6601=>0901-00HI000 FERRITE BEAD(1206)390 OHM/2A

PR

PR2.1 RTC pin define swap

PR_S01:Change C3627,C3626 from X5R to Y5V

PR_S02:According with INTEL datasheet suggest.(Power circuit mount)

PR_S03:To prevent 誤動作 PCIE Wake.

PR_S04:To change WLAN LED control by MODULE then gate control by 3G LED.

PR_S05:To change 3G LED control by MODULE.

PR_S06:To prevent leakage current and mount R for cost down.

PR_S07:RF reserve.

PR_S08:Move P.U 10K near 3G connector.

PR_S09:Change LED POWER rail from +5VSUS_LEDDB(+5VSUS) to
+5VA_LEDDB(+5VA) .(To resolve Battery LL issue)

PR_S10:Change LED POWER rail from
+5VSUS_LEDDB(+5VSUS) to +5V_LEDDB(+5V)

PR_S11:Del JP, +3VS_CR change Net name to +3VS

PR_S12:ESD change solution ,Add U6512 ,Del C6509,D6501~3,U6502,U6503,D6401

PR_S13:Change NET name to +3VS

PR_S14:Change 10uF to 22uF for wave of CRT display.

PR_S15:Add 10uF (C6803)for USB droop test.

PR_S16:D5201 PIN Swap

PR_S17:ME modify.(H6532,8,1,9,4,3,5,H6945),DEL H6944

PR_S18:EMI add.

PR_S19:Change to unmount for ME

PR_S20:RF request.

PR_S21:LED light fine-tune.

PR_S22:BIOS request for UMA and DSC platform identifying.

PEGATRON Title : ****

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

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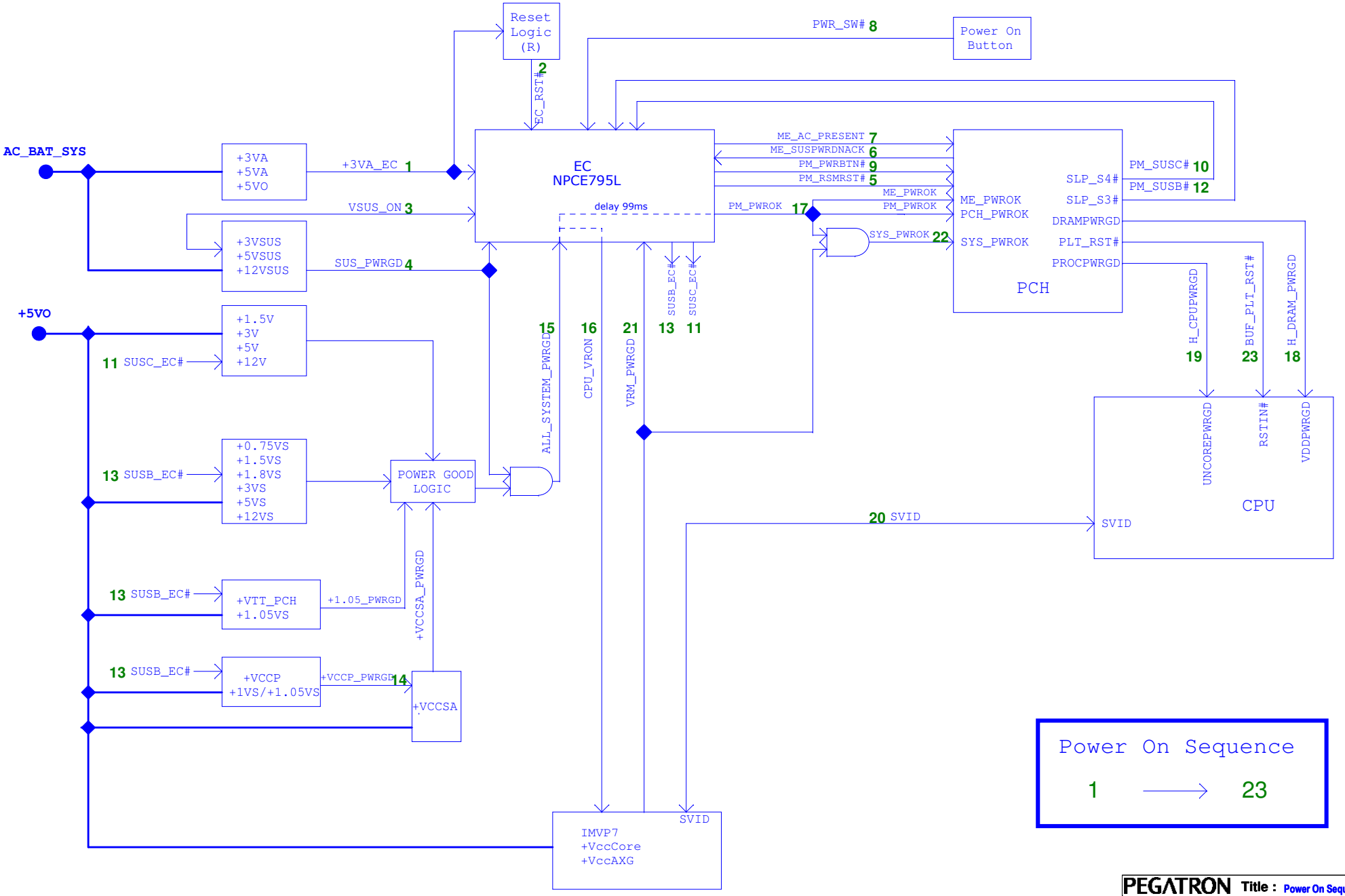
Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON Title : Power On Sequence

<OrgName> Engineer: Joyoung_Chianhg

Size	Project Name	Rev
C	JM50	3.1

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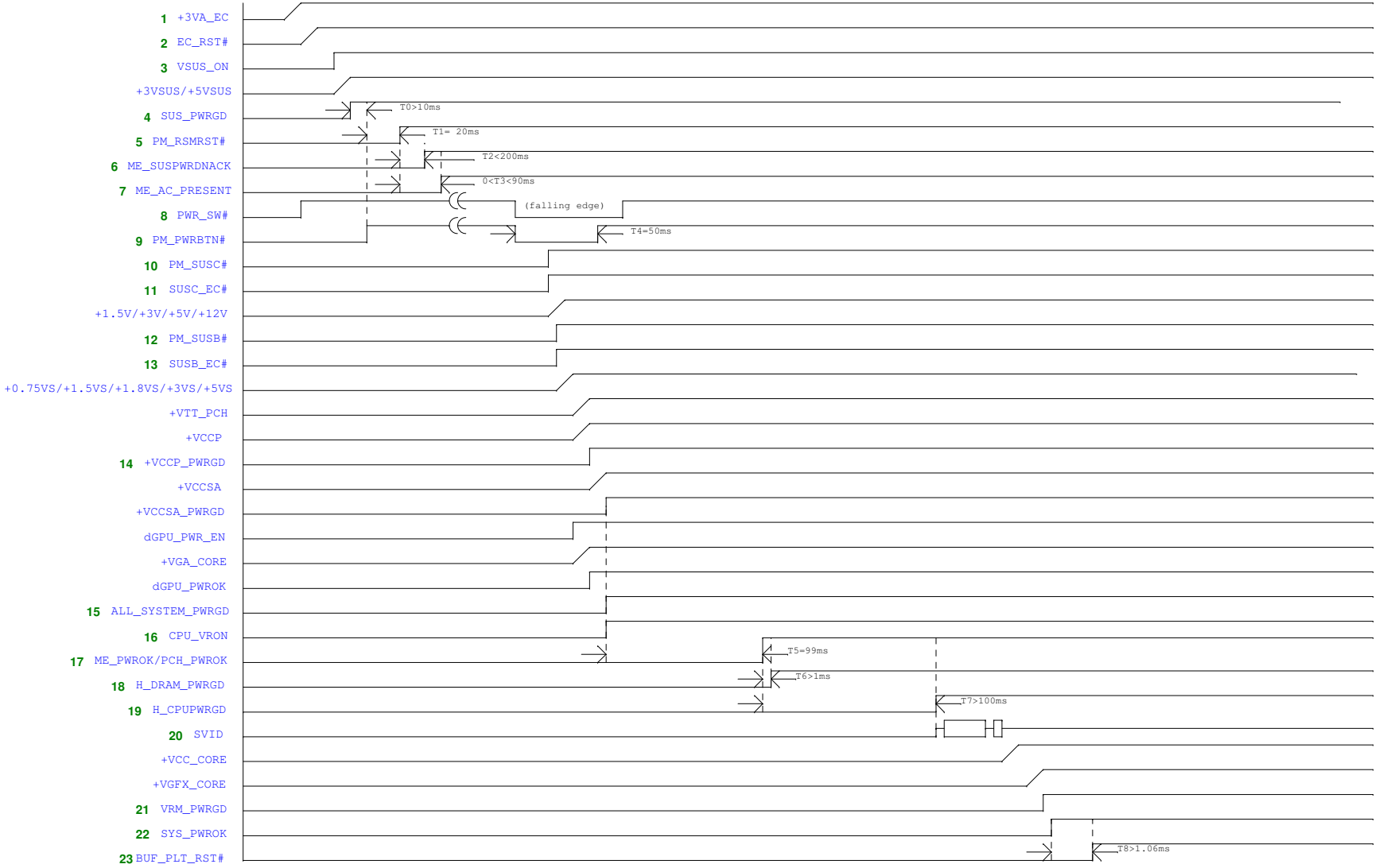
Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



PEGATRON	Title : Power On Timing	
<OrgName>	Engineer: Joyoung_Chianhg	
Size: C	Project Name: JM50	Rev: 3.1
Date: Thursday, August 23, 2012	Sheet 99 of 93	