

JIWA3/A4

Compal Schematics Document

Mobile Penryn uFCPGA

Intel Cantiga_GM/PM+ICH9-M

Wednesday, May 14, 2008

REV:1.0

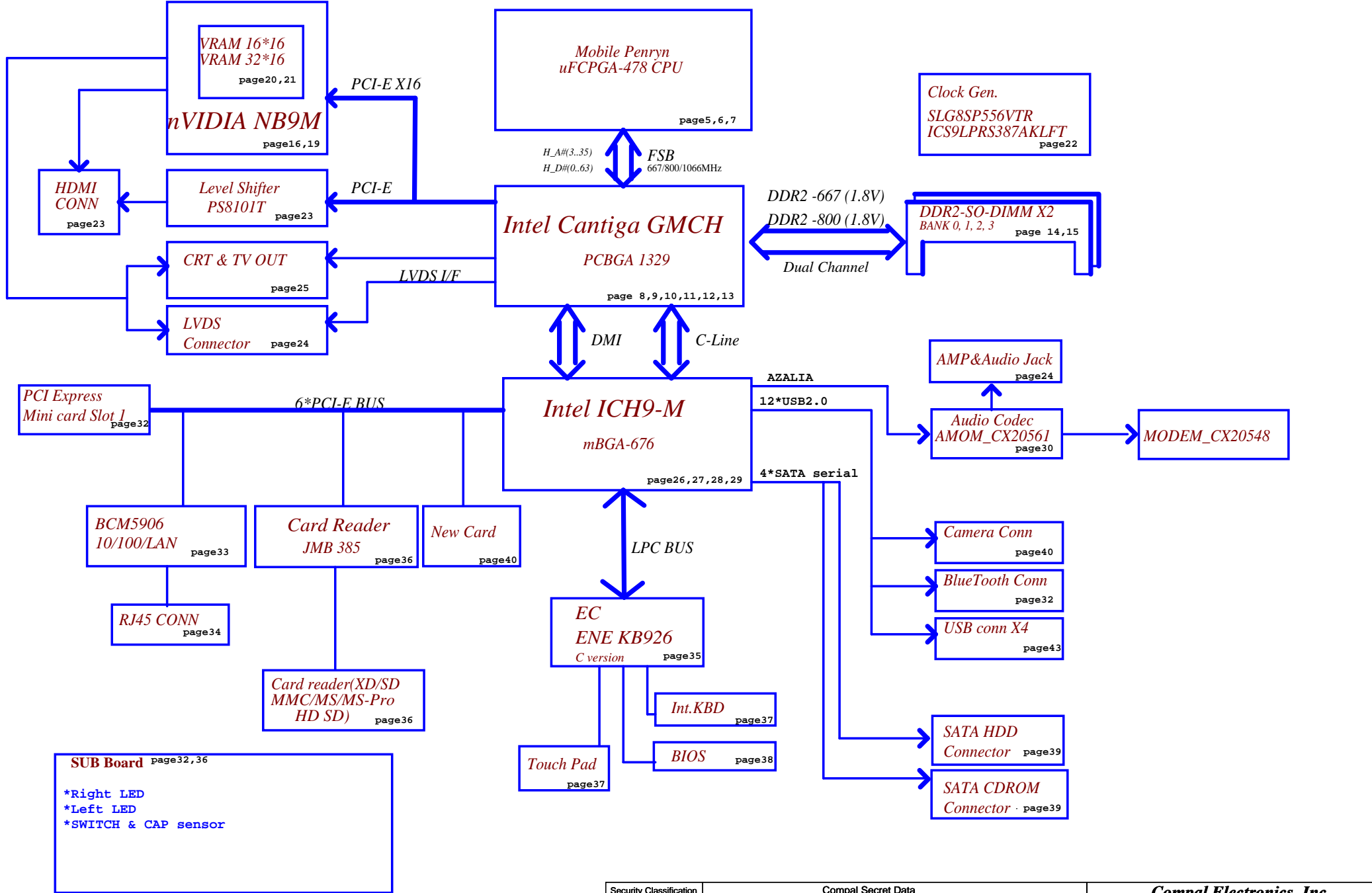
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	<i>Compal Electronics, Inc.</i>
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				Document Number
Date:				Rev
				1.0
				Sheet 1 of 53



Right LED Board

Switch & CAP SENSE LEDs Board

Left LED Board



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Size	Document Number	Date		Rev	1.0
Custom	J1WA3/A4_LA-4212P	Monday, May 12, 2008		Sheet	2 of 53

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD	CAP BRD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@
GM@
X76@
CARD@
WLAN@
HDMI@
HDMI_PM@
HDMI_GM@
BT@

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				Size B Rev 1.0 Sheet 3 of 53

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

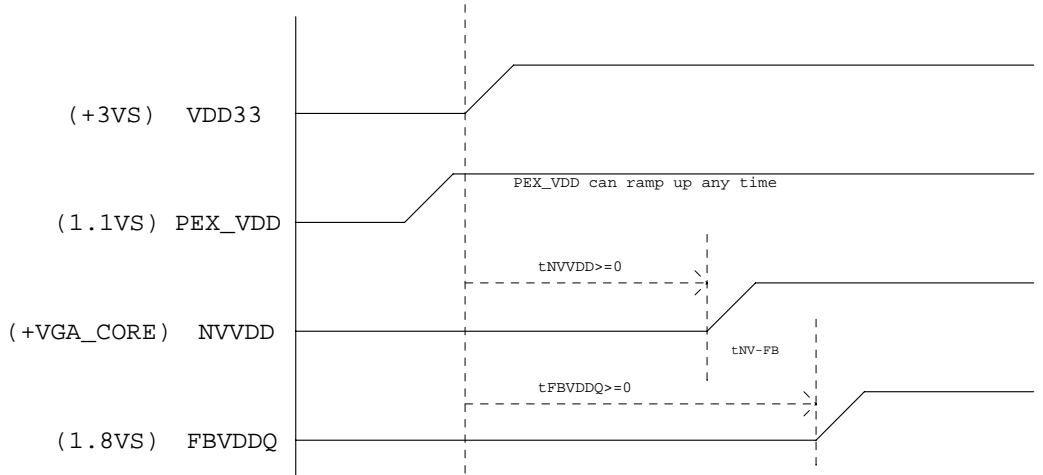
EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1		25mA		
FB_PLLAVDD	1.1		10mA		
IFPC_IOVDD	1.1		385mA		
IFPD_IOVDD	1.1		385mA		
IFPE_IOVDD	1.1		385mA		
IFPF_IOVDD	1.1		385mA		
PEX_IOVDD/Q	1.1		1400mA		
PEX_PLLVDD	1.1		110mA		
PLLVDD	1.1		65mA		
SP_PLLVDD	1.1		25mA		
VID_PLLVDD	1.1		50mA		
TOTAL	1.1		3.225A		
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8		50mA		
IFPB_IOVDD	1.8		50mA		
IFPAB_PLLVDD	1.8		100mA		
IFPCD_PLLVDD	1.8		160mA		
IFPEF_PLLVDD	1.8		160mA		
TOTAL	1.8	3.6A	2.24A	3.53A	2.2A
DACA_VDD	3.3		130mA		
DACB_VDD	3.3		255mA		
DACC_VDD	3.3		130mA		
MIOA_VDDQ	3.3		10mA		
MIOB_VDDQ	3.3		10mA		
VDD33	3.3		110mA		
TOTAL	3.3		0.645A		

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

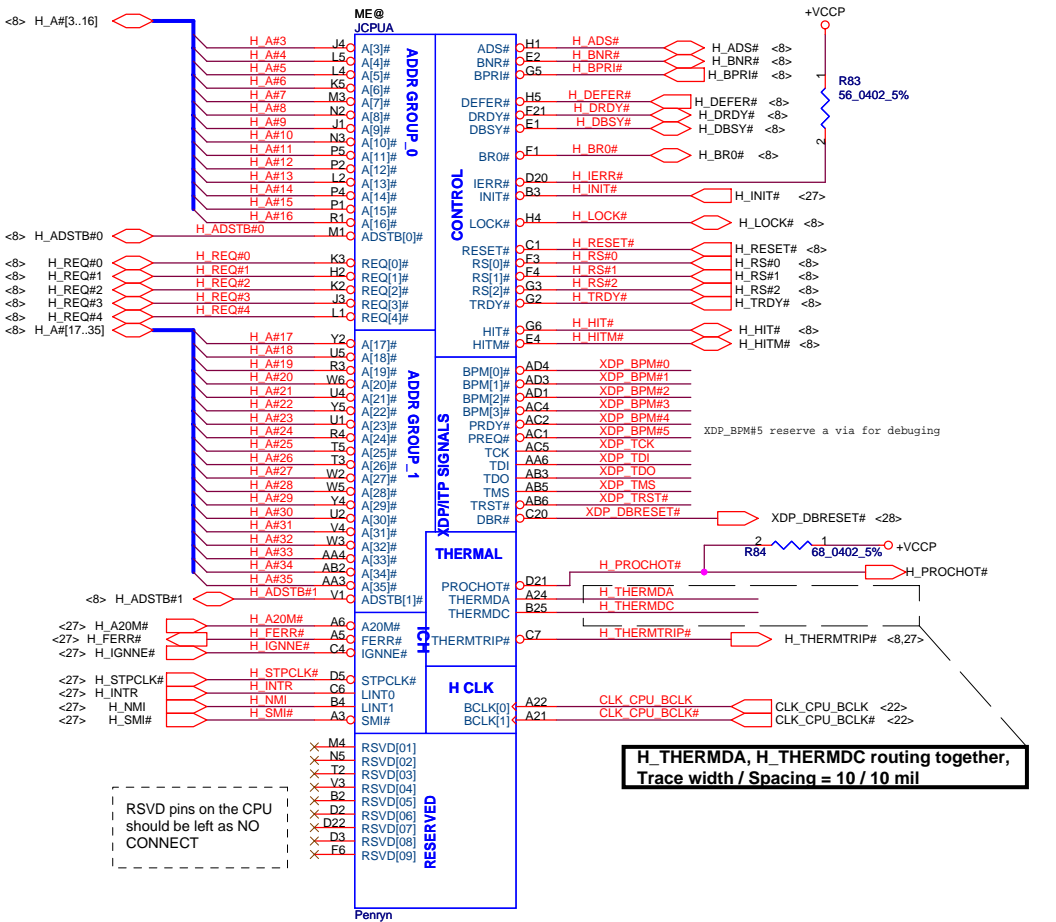
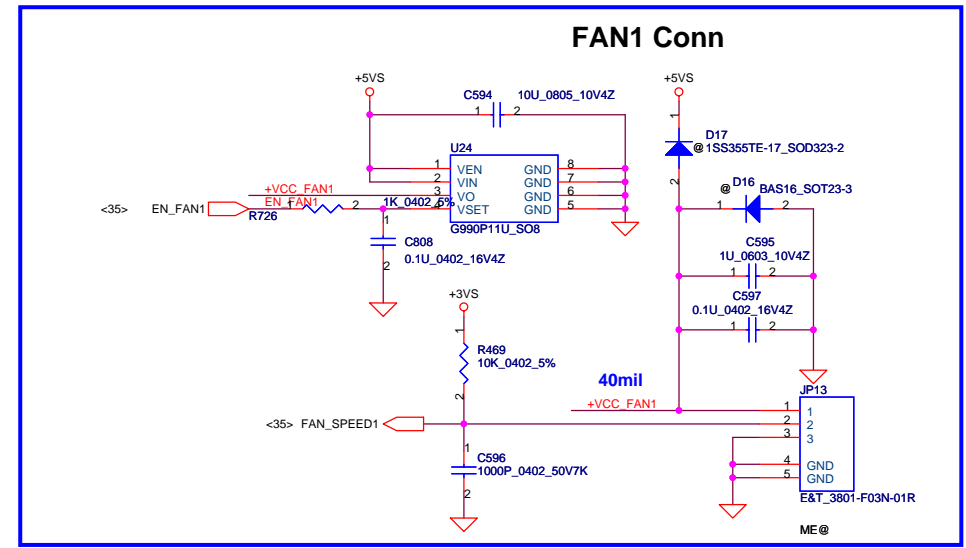
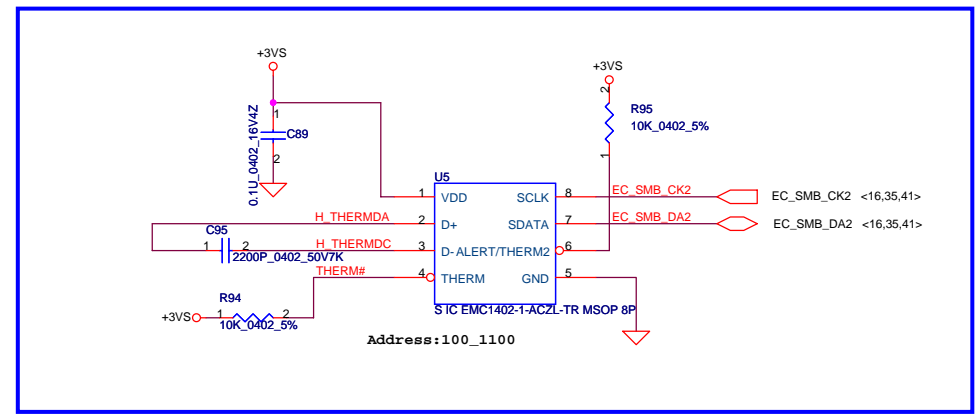
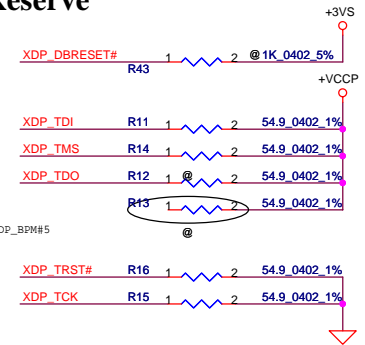
POWER SEQUENCE

The ramp time for any rail must be more than 40us



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				Date:	Monday, May 12, 2008
				Sheet	4 of 53
				Rev	1.0

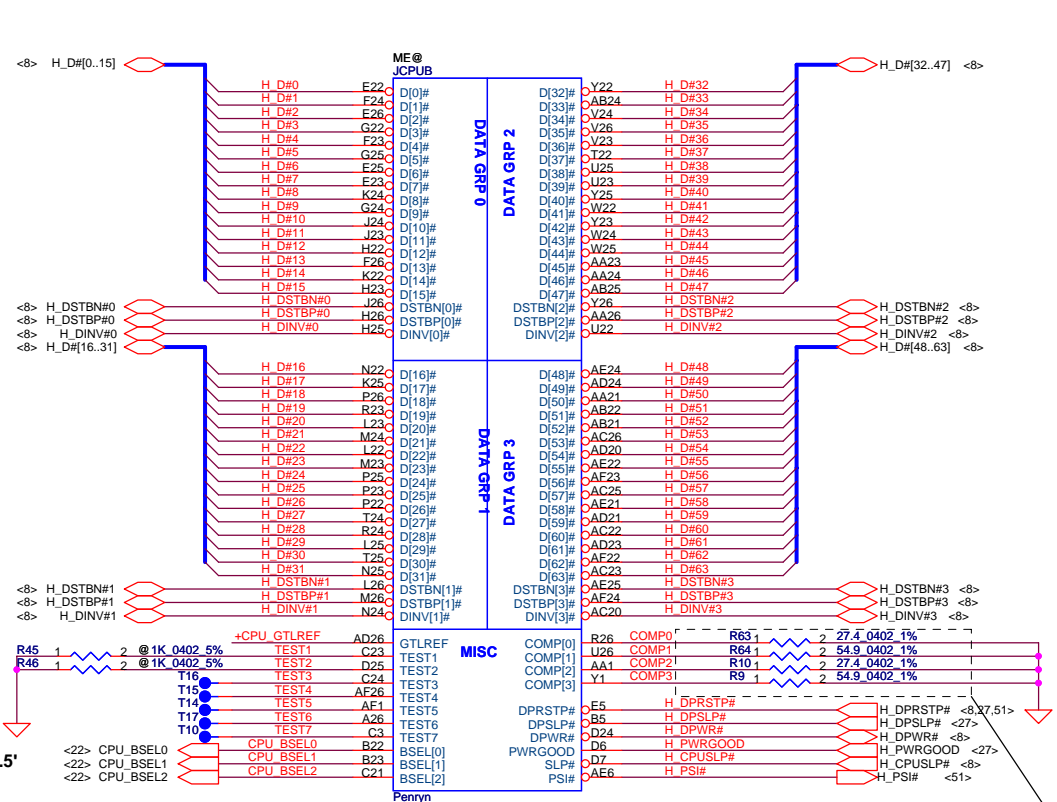
XDP Reserve



H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

RSVD pins on the CPU should be left as NO CONNECT

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Size B	Document Number	Date		Sheet	Rev
	J1WA3/A4_LA4212P	Wednesday, May 14, 2008		5	1.0
				of	53



Trace Close CPU < 0.5'

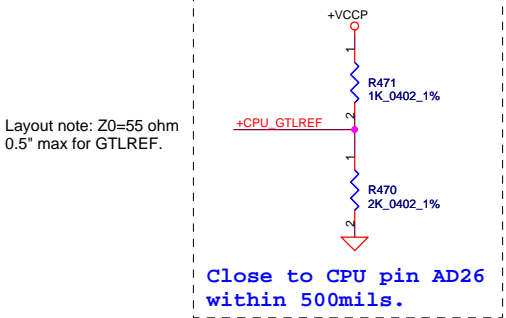
Width=4 mil ,
Spacing: 15mil
(55Ohm)

TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)

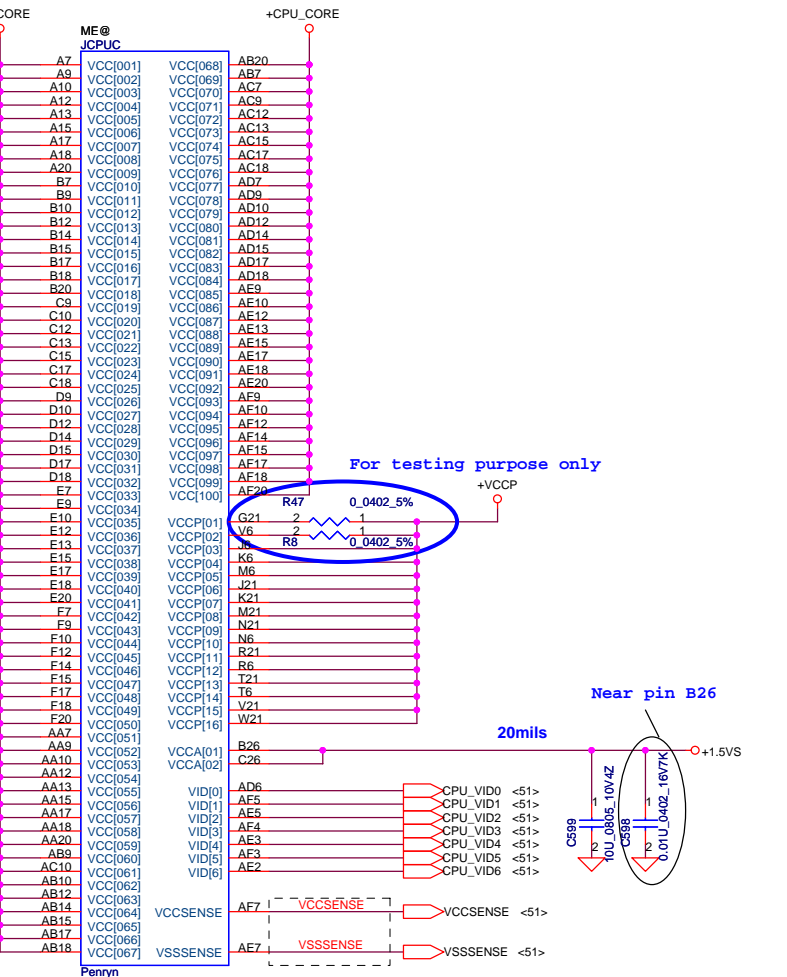
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs



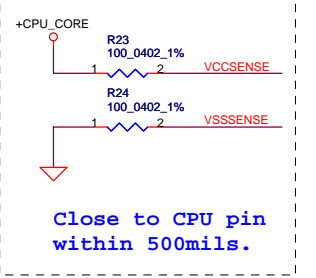
Layout note: Z0=55 ohm
0.5" max for GTLREF.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

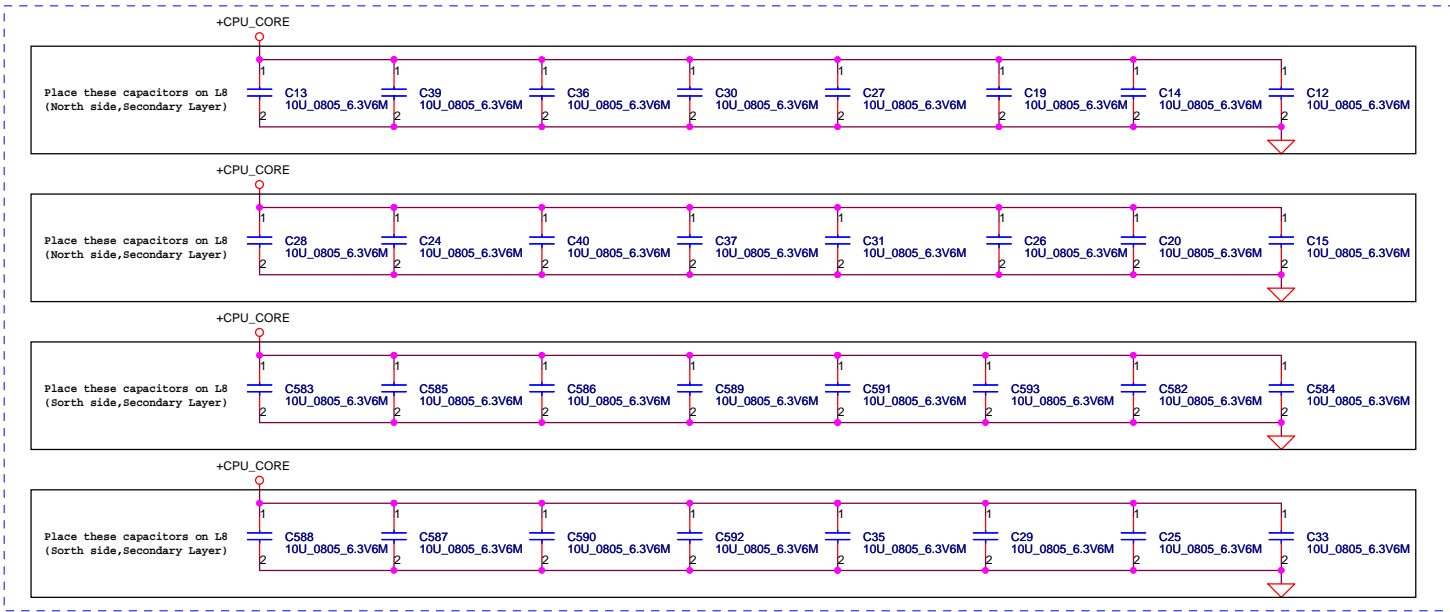


Length match within 25 mils.
The trace width/space/other is 16/7/25.

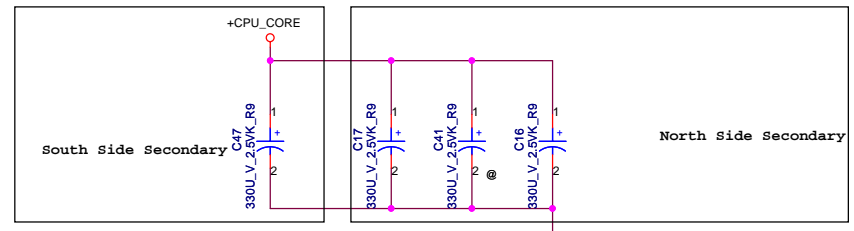
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



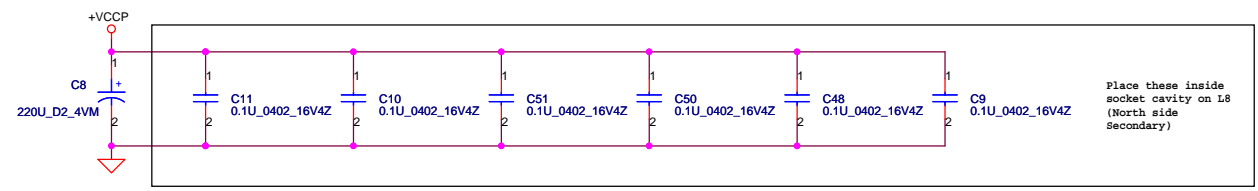
ME@	JCPU	VSS	P
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B8	VSS[009]	VSS[090]	T4
B11	VSS[010]	VSS[091]	T23
B13	VSS[011]	VSS[092]	T26
B16	VSS[012]	VSS[093]	U3
B19	VSS[013]	VSS[094]	U6
B21	VSS[014]	VSS[095]	U21
B24	VSS[015]	VSS[096]	U24
C5	VSS[016]	VSS[097]	V2
C8	VSS[017]	VSS[098]	V5
C11	VSS[018]	VSS[099]	V22
C14	VSS[019]	VSS[100]	V25
C16	VSS[020]	VSS[101]	W1
C19	VSS[021]	VSS[102]	W4
C2	VSS[022]	VSS[103]	W23
C22	VSS[023]	VSS[104]	W26
C25	VSS[024]	VSS[105]	Y3
D1	VSS[025]	VSS[106]	Y6
D4	VSS[026]	VSS[107]	Y21
D8	VSS[027]	VSS[108]	Y24
D11	VSS[028]	VSS[109]	AA2
D13	VSS[029]	VSS[110]	AA5
D16	VSS[030]	VSS[111]	AA8
D19	VSS[031]	VSS[112]	AA11
D23	VSS[032]	VSS[113]	AA14
D26	VSS[033]	VSS[114]	AA16
E3	VSS[034]	VSS[115]	AA19
E6	VSS[035]	VSS[116]	AA22
E8	VSS[036]	VSS[117]	AA25
E11	VSS[037]	VSS[118]	AB1
E14	VSS[038]	VSS[119]	AB4
E16	VSS[039]	VSS[120]	AB8
E19	VSS[040]	VSS[121]	AB11
E21	VSS[041]	VSS[122]	AB13
E24	VSS[042]	VSS[123]	AB16
F5	VSS[043]	VSS[124]	AB19
F8	VSS[044]	VSS[125]	AB23
F11	VSS[045]	VSS[126]	AB26
F13	VSS[046]	VSS[127]	AC3
F16	VSS[047]	VSS[128]	AC6
F19	VSS[048]	VSS[129]	AC8
F2	VSS[049]	VSS[130]	AC11
F22	VSS[050]	VSS[131]	AC14
F25	VSS[051]	VSS[132]	AC16
G4	VSS[052]	VSS[133]	AC19
G1	VSS[053]	VSS[134]	AC21
G23	VSS[054]	VSS[135]	AC24
H3	VSS[055]	VSS[136]	AD2
H6	VSS[056]	VSS[137]	AD5
H21	VSS[057]	VSS[138]	AD8
H24	VSS[058]	VSS[139]	AD11
J2	VSS[059]	VSS[140]	AD13
J5	VSS[060]	VSS[141]	AD16
J22	VSS[061]	VSS[142]	AD19
J25	VSS[062]	VSS[143]	AD22
K1	VSS[063]	VSS[144]	AD25
K4	VSS[064]	VSS[145]	AE1
K23	VSS[065]	VSS[146]	AE4
K26	VSS[066]	VSS[147]	AE8
L3	VSS[067]	VSS[148]	AE11
L6	VSS[068]	VSS[149]	AE14
L21	VSS[069]	VSS[150]	AE16
L24	VSS[070]	VSS[151]	AE19
M2	VSS[071]	VSS[152]	AE23
M5	VSS[072]	VSS[153]	AE26
M22	VSS[073]	VSS[154]	A2
M25	VSS[074]	VSS[155]	AF6
N1	VSS[075]	VSS[156]	AF8
N4	VSS[076]	VSS[157]	AF11
N23	VSS[077]	VSS[158]	AF13
N26	VSS[078]	VSS[159]	AF16
P3	VSS[079]	VSS[160]	AF19
	VSS[080]	VSS[161]	AF21
	VSS[081]	VSS[162]	A25
	VSS[082]	VSS[163]	AF25



Mid Frequency Decoupling

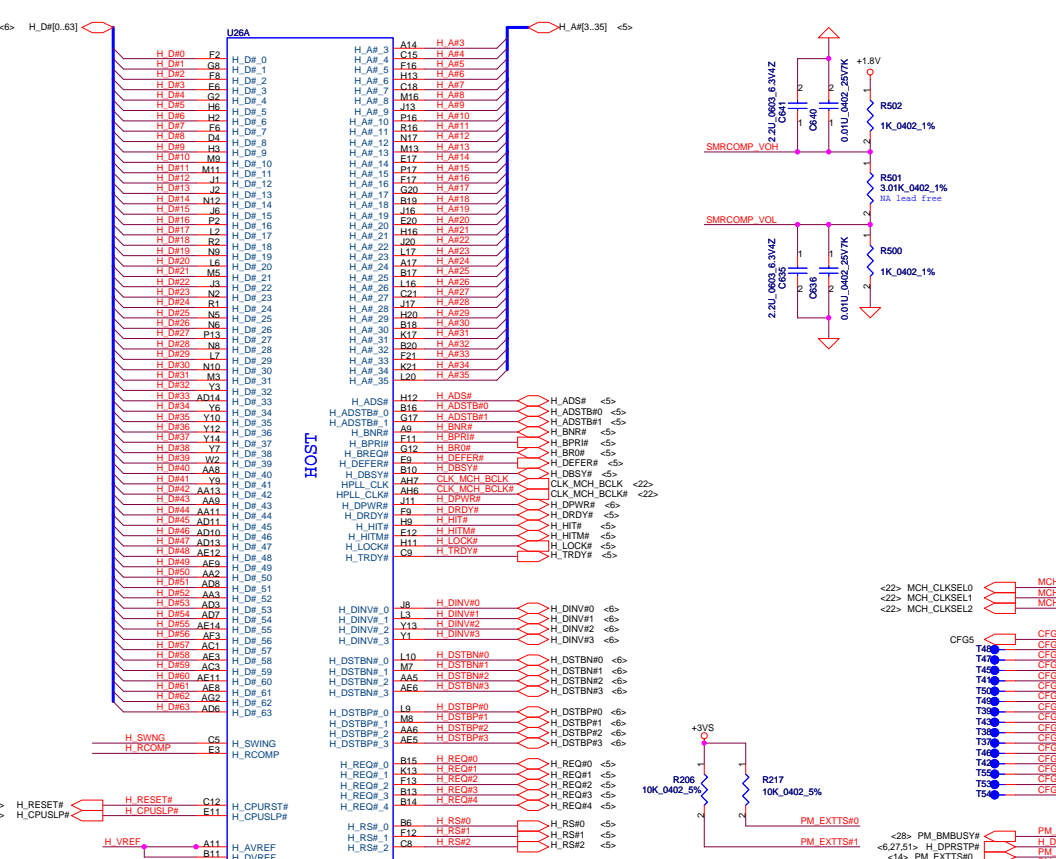


ESR <= 1.5m ohm
Capacitor > 1980uF



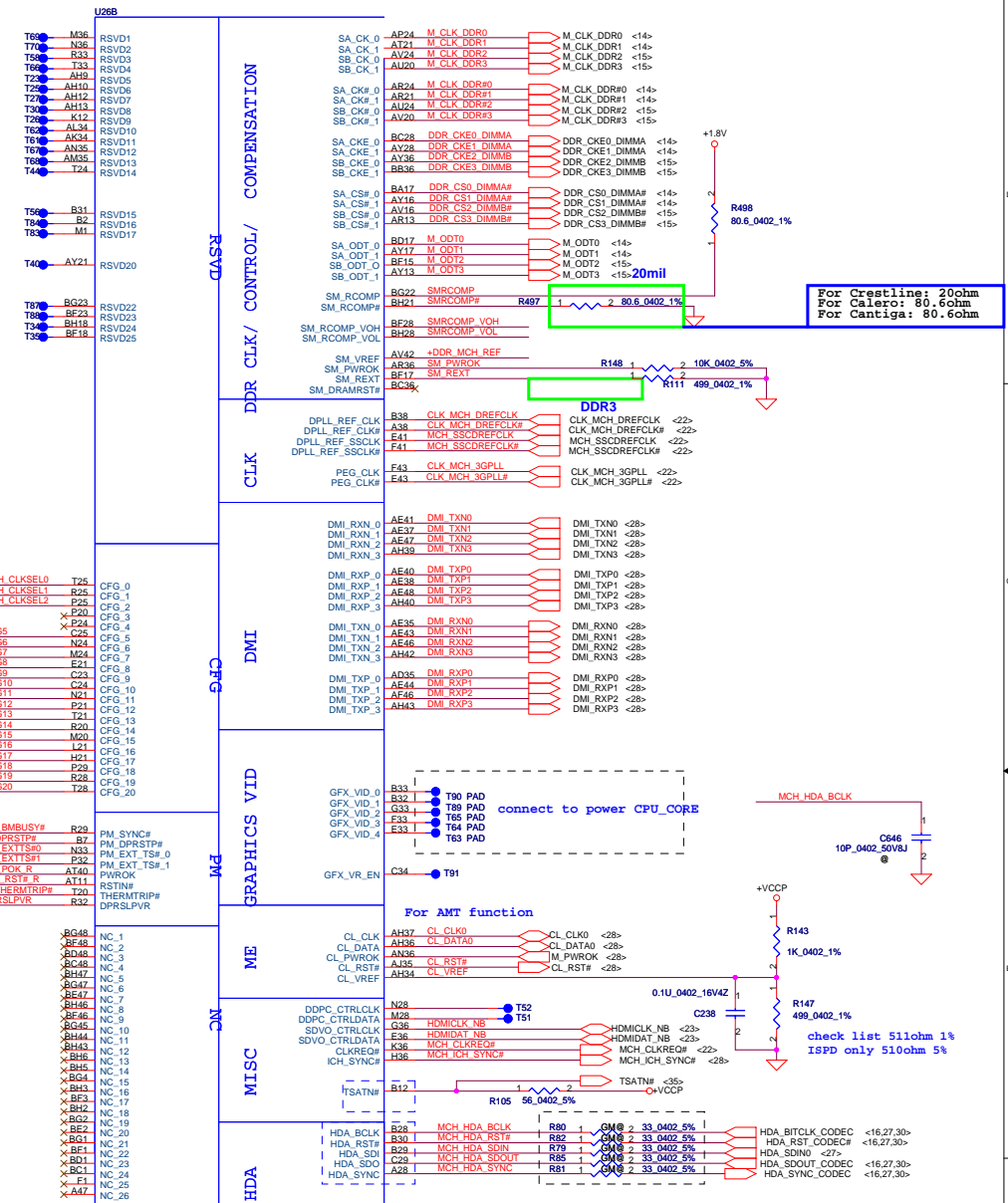
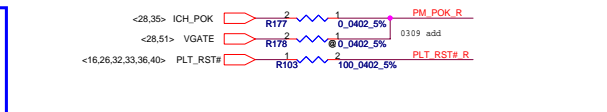
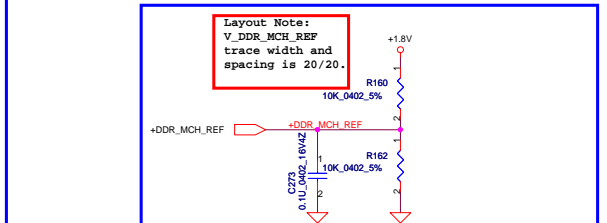
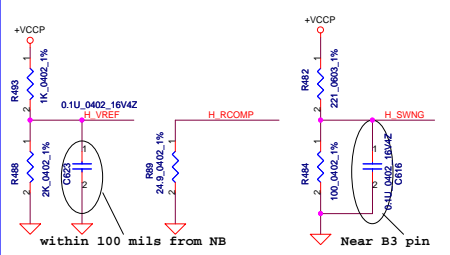
Place these inside socket cavity on L8 (North side Secondary)

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Size B	Document Number	Date		Rev	1.0
	J1WA3/A4_LA4212P	Monday, May 12, 2008	Sheet 7 of 53		

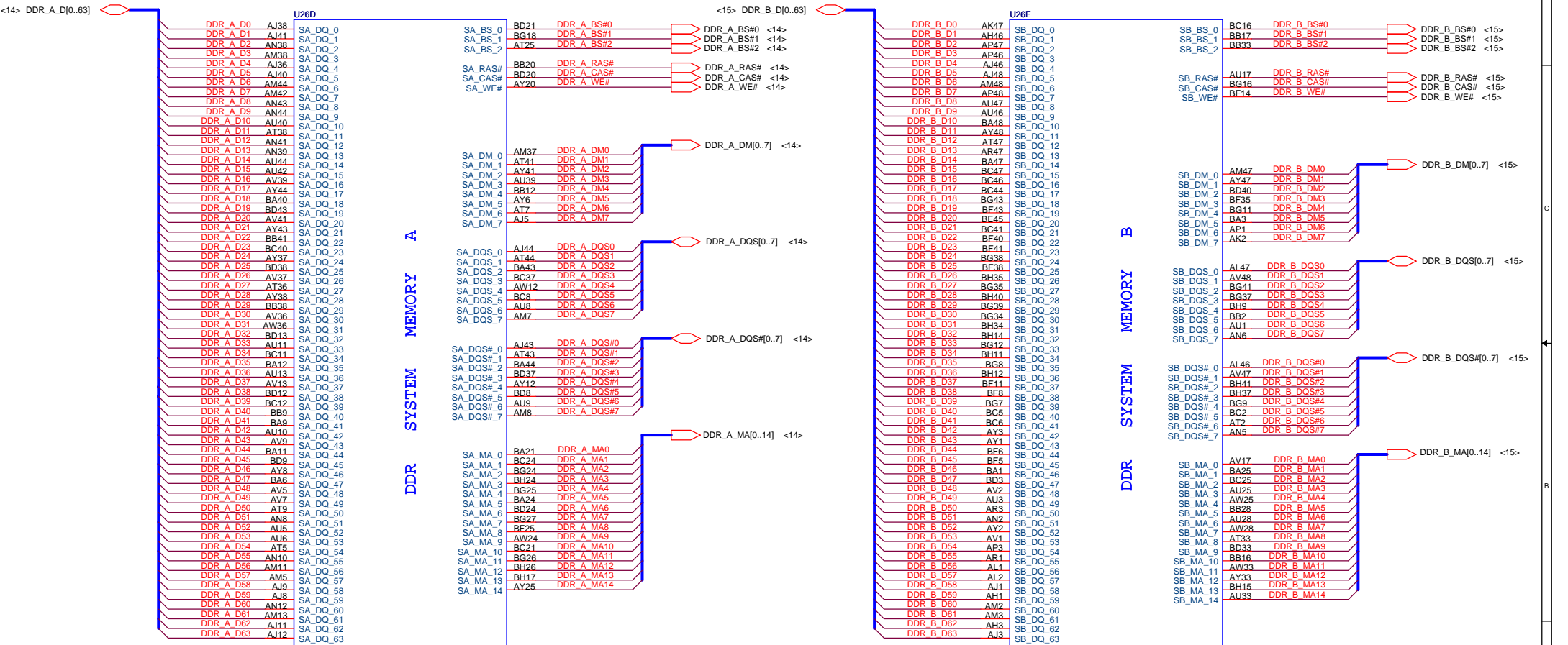


layout note:
Route H_SCOMP and H_SCOMP# with trace width spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCAMP / H_VREF / H_SWING
trace width and spacing is 10/20



Notice: Please check HDA power rail to select HDA controller.



CANTIGA ES_FCBGA1329

CANTIGA ES_FCBGA1329

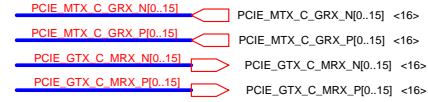
GM@

GM@

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Size	Document Number	Date		Sheet	Rev
B	J1WA3/A4_LA4212P	Wednesday, May 14, 2008		9	1.0
				of	53

Strap Pin Table

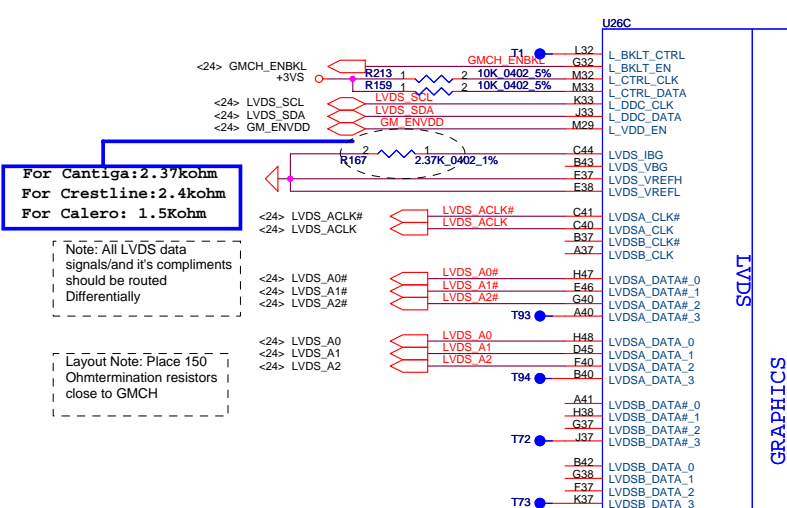
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chipset suite with no confidentiality 1=(TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *



Place the resistor within 500mils (1.27mm) of the (G)MCH
PEGCOMP trace width and spacing is 20/25 mils.



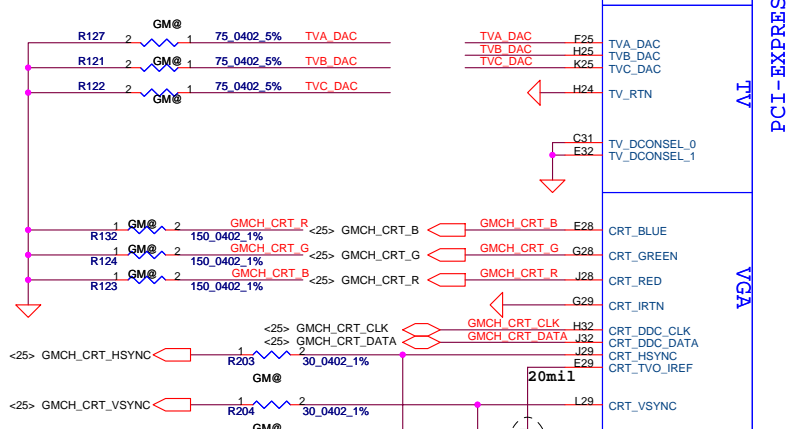
Please check Power source if want support IAMT



For Cantiga: 2.37kohm
For Crestline: 2.4kohm
For Calero: 1.5kohm

Note: All LVDS data signals/and it's compliments should be routed Differentially

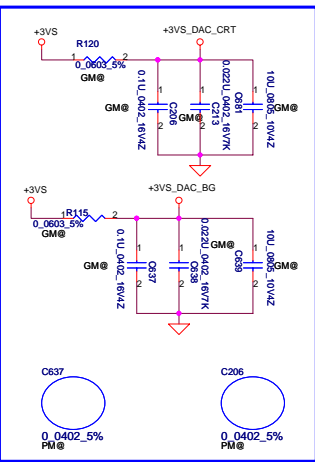
Layout Note: Place 150 Ohm termination resistors close to GMCH



For Cantiga: 1.02kohm
For Crestline: 1.3kohm
For Calero: 255ohm

PEG_RX#_0	H44	PCIE GTX C MRX N0				
PEG_RX#_1	L46	PCIE GTX C MRX N1				
PEG_RX#_2	L44	PCIE GTX C MRX N2				
PEG_RX#_3	L40	PCIE GTX C MRX N3				
PEG_RX#_4	N41	PCIE GTX C MRX N4				
PEG_RX#_5	P48	PCIE GTX C MRX N5				
PEG_RX#_6	N44	PCIE GTX C MRX N6				
PEG_RX#_7	T43	PCIE GTX C MRX N7				
PEG_RX#_8	U43	PCIE GTX C MRX N8				
PEG_RX#_9	Y43	PCIE GTX C MRX N9				
PEG_RX#_10	Y36	PCIE GTX C MRX N10				
PEG_RX#_11	AA43	PCIE GTX C MRX N11				
PEG_RX#_12	AD37	PCIE GTX C MRX N12				
PEG_RX#_13	AC47	PCIE GTX C MRX N13				
PEG_RX#_14	AD39	PCIE GTX C MRX N14				
PEG_RX#_15	AD39	PCIE GTX C MRX N15				
PEG_RX_0	H43	PCIE GTX C MRX P0				
PEG_RX_1	J44	PCIE GTX C MRX P1				
PEG_RX_2	L43	PCIE GTX C MRX P2				
PEG_RX_3	L41	PCIE GTX C MRX P3				
PEG_RX_4	N40	PCIE GTX C MRX P4				
PEG_RX_5	P47	PCIE GTX C MRX P5				
PEG_RX_6	N43	PCIE GTX C MRX P6				
PEG_RX_7	T42	PCIE GTX C MRX P7				
PEG_RX_8	U42	PCIE GTX C MRX P8				
PEG_RX_9	Y42	PCIE GTX C MRX P9				
PEG_RX_10	W47	PCIE GTX C MRX P10				
PEG_RX_11	Y37	PCIE GTX C MRX P11				
PEG_RX_12	AA42	PCIE GTX C MRX P12				
PEG_RX_13	AD36	PCIE GTX C MRX P13				
PEG_RX_14	AC48	PCIE GTX C MRX P14				
PEG_RX_15	AD40	PCIE GTX C MRX P15				
PEG_TX#_0	J41	PCIE MTX GRX N0 C277	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N0
PEG_TX#_1	M46	PCIE MTX GRX N1 C303	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N1
PEG_TX#_2	M47	PCIE MTX GRX N2 C317	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N2
PEG_TX#_3	M40	PCIE MTX GRX N3 C315	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N3
PEG_TX#_4	M42	PCIE MTX GRX N4 C325	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N4
PEG_TX#_5	R48	PCIE MTX GRX N5 C343	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N5
PEG_TX#_6	N38	PCIE MTX GRX N6 C358	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N6
PEG_TX#_7	T40	PCIE MTX GRX N7 C349	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N7
PEG_TX#_8	U37	PCIE MTX GRX N8 C364	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N8
PEG_TX#_9	U40	PCIE MTX GRX N9 C354	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N9
PEG_TX#_10	Y40	PCIE MTX GRX N10 C371	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N10
PEG_TX#_11	AA46	PCIE MTX GRX N11 C356	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N11
PEG_TX#_12	AA40	PCIE MTX GRX N12 C372	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N12
PEG_TX#_13	AD43	PCIE MTX GRX N13 C364	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N13
PEG_TX#_14	AD43	PCIE MTX GRX N14 C375	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N14
PEG_TX#_15	AC46	PCIE MTX GRX N15 C348	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_N15
PEG_TX_0	J42	PCIE MTX GRX P0 C271	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P0
PEG_TX_1	L46	PCIE MTX GRX P1 C296	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P1
PEG_TX_2	M48	PCIE MTX GRX P2 C314	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P2
PEG_TX_3	M39	PCIE MTX GRX P3 C311	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P3
PEG_TX_4	M43	PCIE MTX GRX P4 C322	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P4
PEG_TX_5	R47	PCIE MTX GRX P5 C336	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P5
PEG_TX_6	N37	PCIE MTX GRX P6 C352	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P6
PEG_TX_7	T39	PCIE MTX GRX P7 C344	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P7
PEG_TX_8	U36	PCIE MTX GRX P8 C363	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P8
PEG_TX_9	U39	PCIE MTX GRX P9 C346	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P9
PEG_TX_10	Y39	PCIE MTX GRX P10 C366	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P10
PEG_TX_11	Y46	PCIE MTX GRX P11 C351	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P11
PEG_TX_12	AA36	PCIE MTX GRX P12 C367	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P12
PEG_TX_13	AA39	PCIE MTX GRX P13 C359	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P13
PEG_TX_14	AD42	PCIE MTX GRX P14 C373	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P14
PEG_TX_15	AD46	PCIE MTX GRX P15 C347	1	2	PM@ 0.1U 0402 10V7K	PCIE MTX_C GRX_P15
PCIE MTX GRX P3	C670	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_CLK <23>	
PCIE MTX GRX N3	C674	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_CLK# <23>	
PCIE MTX GRX P2	C669	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_DATA0 <23>	
PCIE MTX GRX N2	C673	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_DATA0# <23>	
PCIE MTX GRX P1	C662	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_DATA1 <23>	
PCIE MTX GRX N1	C663	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_DATA1# <23>	
PCIE MTX GRX P0	C658	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_DATA2 <23>	
PCIE MTX GRX N0	C661	1	2	HDMI GM@ 0.1U 0402 10V7K	TMDS_B_DATA2# <23>	
PCIE GTX_C MRX P3	C306	1	2	HDMI GM@ 0.0402 5%	TMDS_B_HPD# <23>	

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Size	Document Number	Rev		1.0	
Custom	JTWA3/A4 LA4212P				
Date:	Wednesday, May 14, 2008	Sheet	10	of 53	



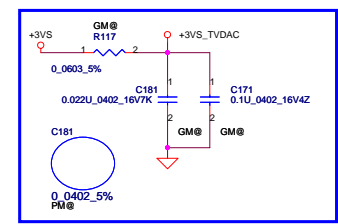
VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
 +3VS_DAC_CRT → B27 → A26 → VCCA_CRT_DAC_1
 VCCA_CRT_DAC_2

VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)
 +3VS_DAC_BG → A25 → B25 → VSSA_DAC_BG

+1.5VS_PEG_BG: 0.414mA (0.1UF*1)
 +1.5VS → R166 → Node → C301 → GND
 +1.5VS → R166 → Node → +1.5VS_PEG_BG

VCCA_SM: 720mA (22UF*1, 4.7UF*1, 1UF*1)
 +VCCP → R108 → Node → C605 → GND
 +VCCP → R108 → Node → C87 → GND
 +VCCP → R108 → Node → C87 → Node → 4.7U_0805_10V4Z → C36 → GND
 +VCCP → R108 → Node → C87 → Node → 1U_0603_10V4Z → C102 → GND

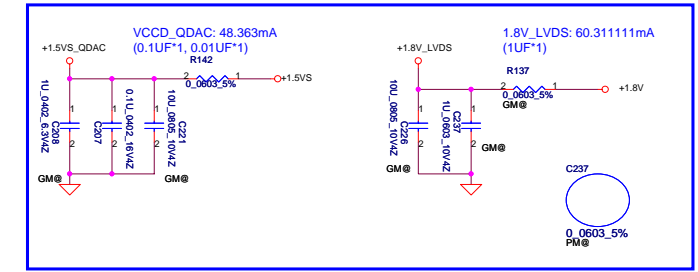
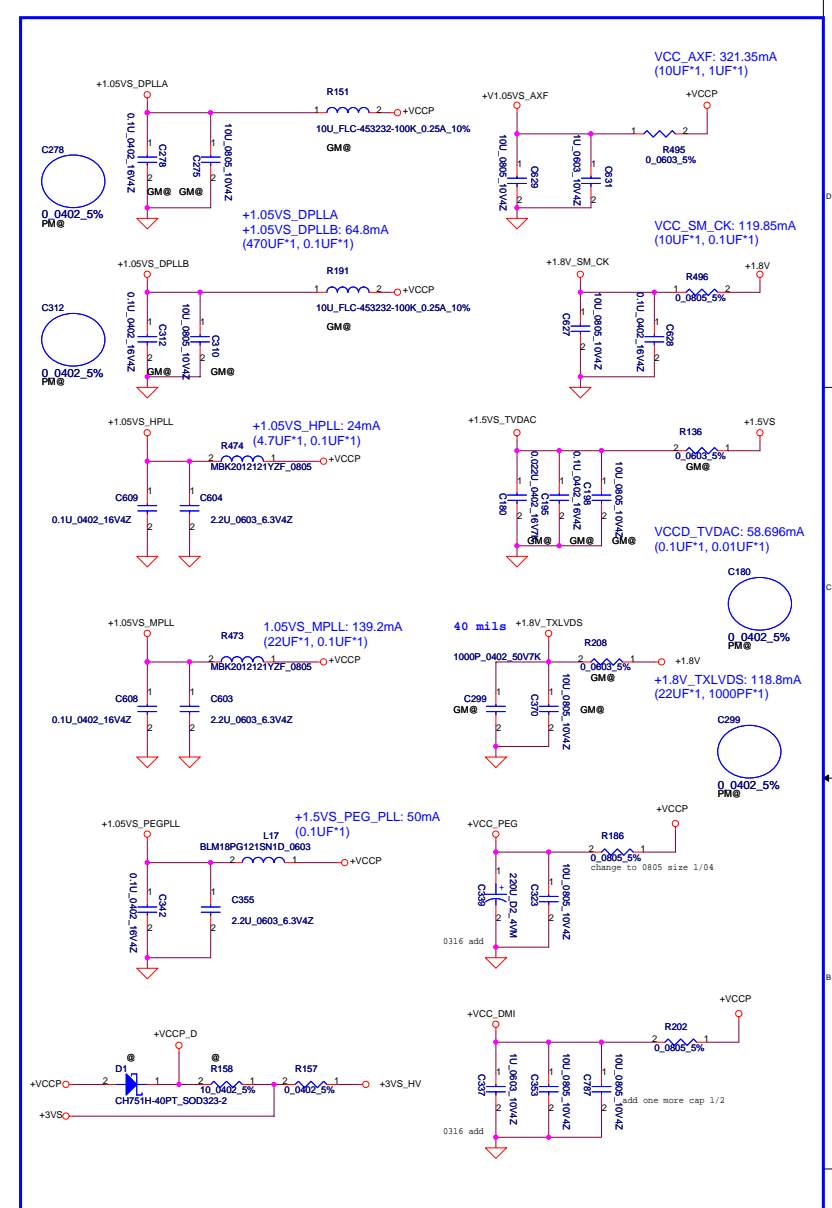
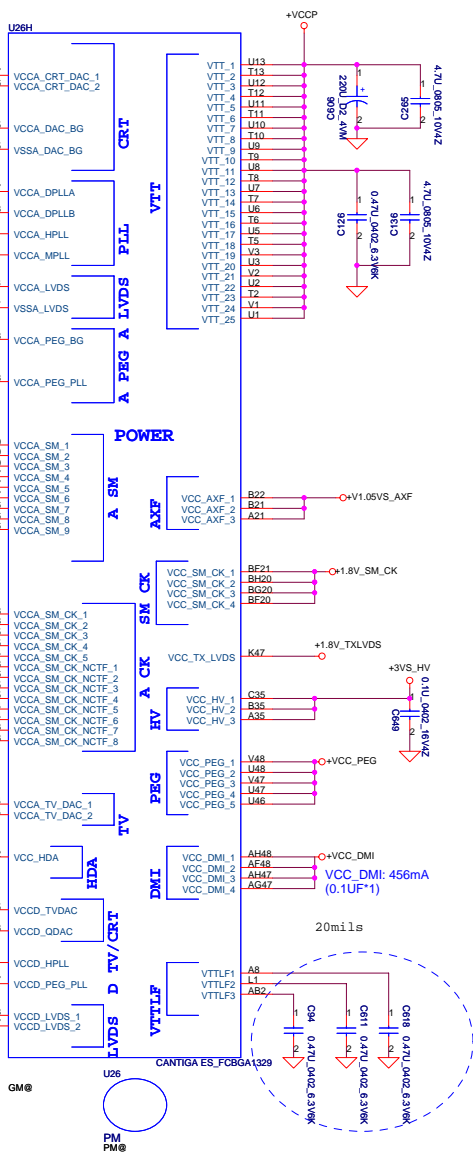
VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)
 +VCCP → R134 → Node → C608 → GND
 +VCCP → R134 → Node → C604 → GND
 +VCCP → R134 → Node → C604 → Node → 2.2U_0603_6.3V4Z → C102 → GND

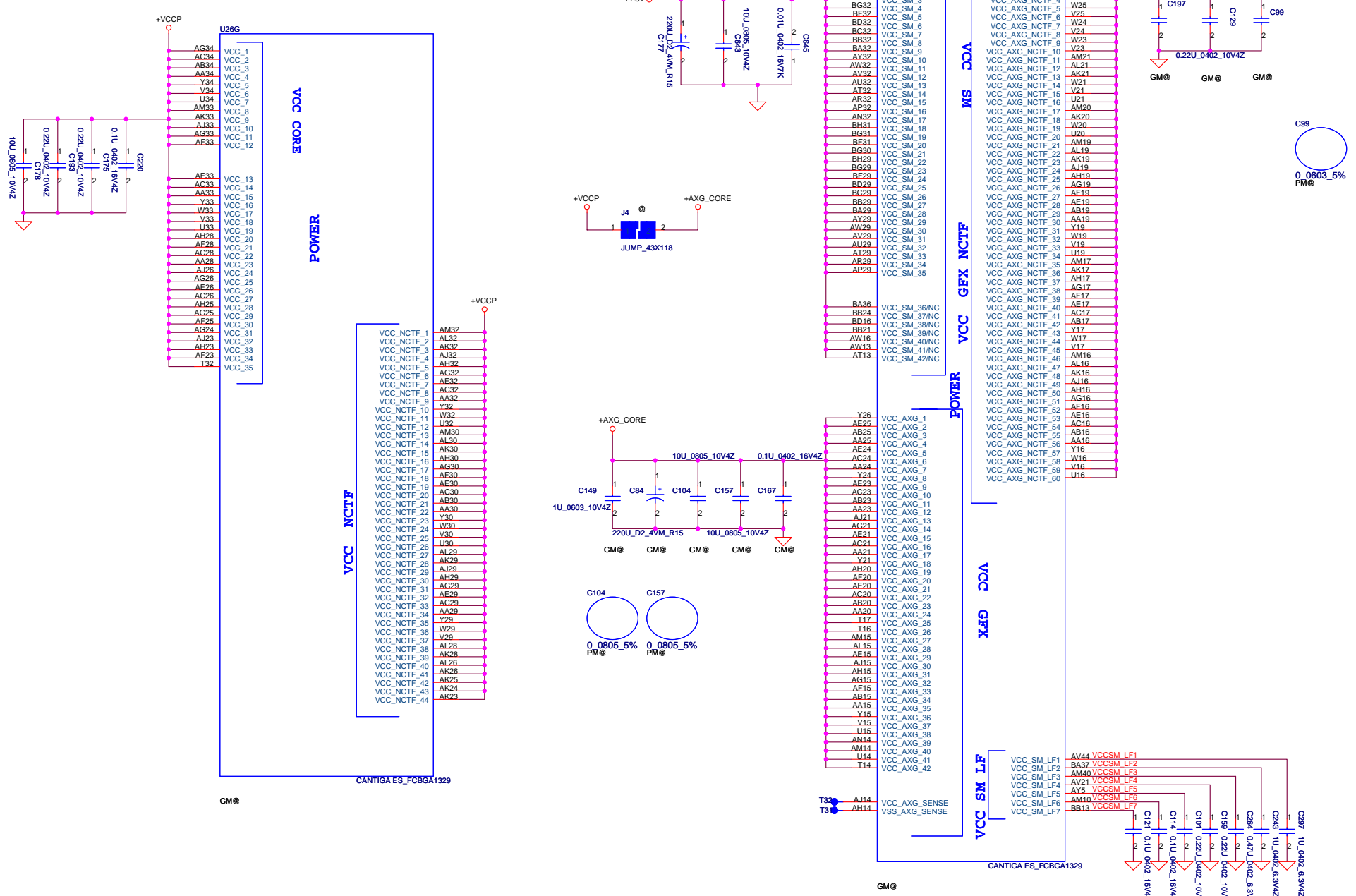


+3VS_TVDAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)
 +3VS_TVDAC → B24 → A24 → VCCA_TV_DAC_1
 VCCA_TV_DAC_2

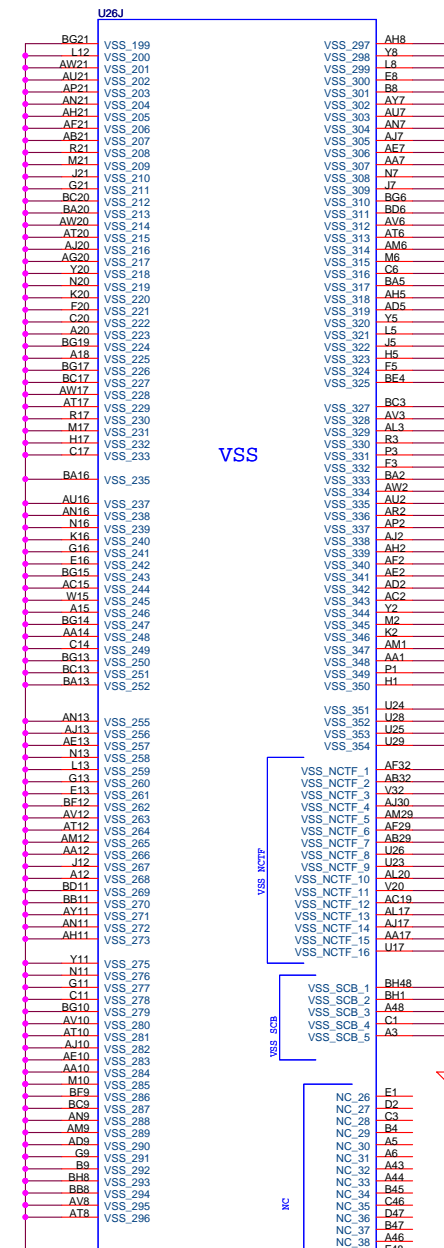
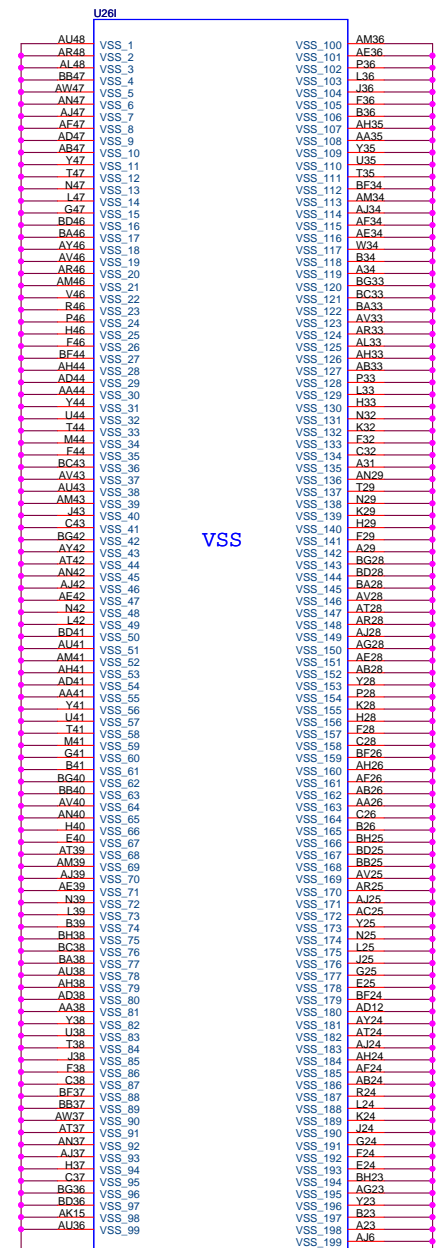
VCC_HDA: 50mA (0.1UF*1)
 +1.5VS → A32 → VCC_HDA

+1.5VS_TVDAC: M25
 +1.5VS_QDAC: L28
 +1.05VS_HPLL: AF1
 +1.05VS_PEGPLL: AA47
 +1.8V_LVDS: M38
 L37



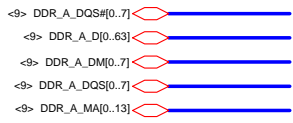


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Size	Document Number	Rev		Date	
Custom	J1WA3/A4 LA4212P	1.0		Wednesday, May 14, 2008	
				Sheet 12 of 53	

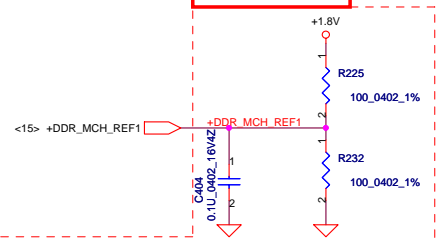


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Issued Date	2007/10/15	Deciphered Date	2008/10/15
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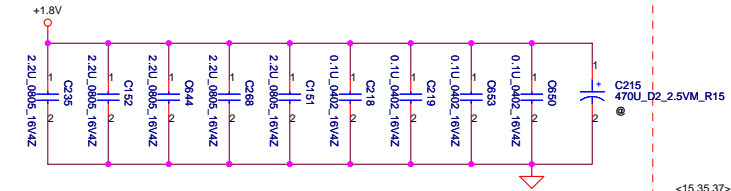
Compal Electronics, Inc.			
Cantiga GMCH (6/6)-GND			
Size	Document Number	Rev	
Custom	JJWA3/A4_LA4212P	1.0	
Date:	Wednesday, May 14, 2008	Sheet	13 of 53



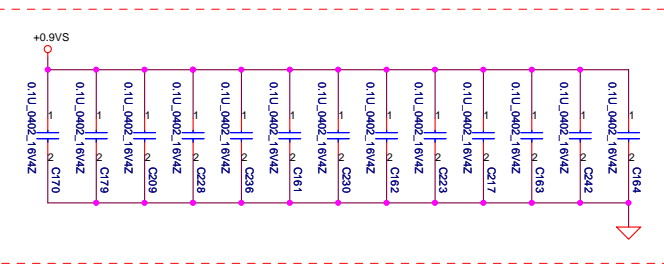
Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.



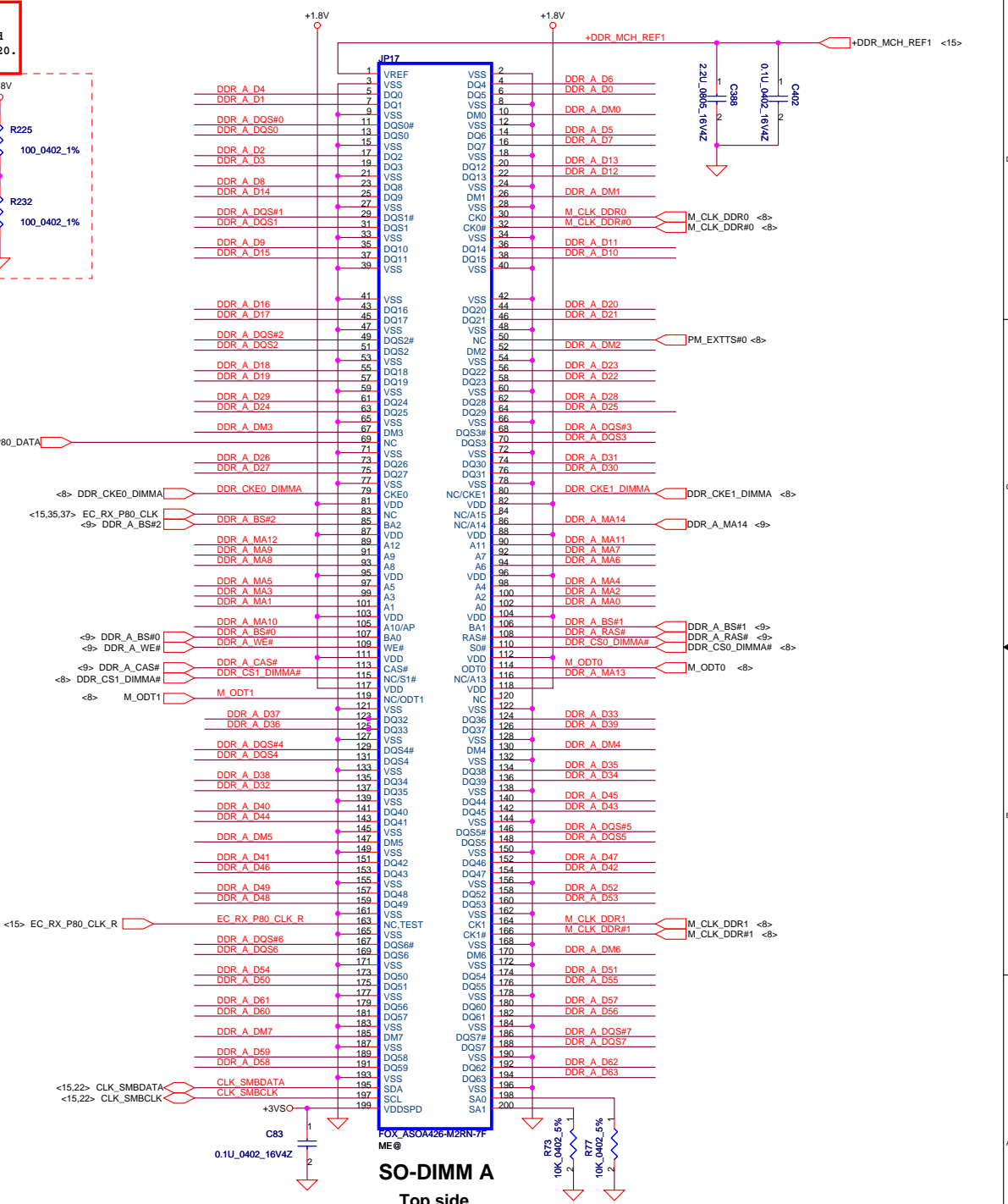
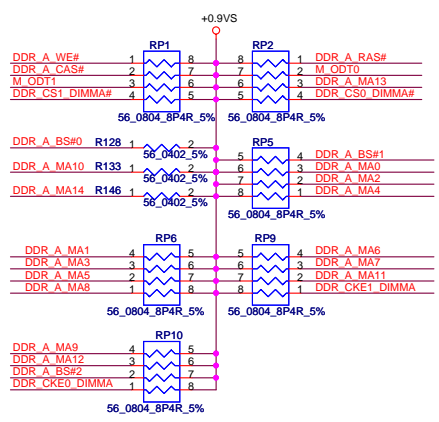
Layout Note:
Place near JP41



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



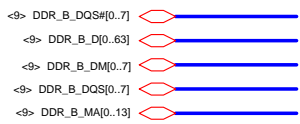
Layout Note:
Place these resistor closely JP41, all trace length Max=1.5"



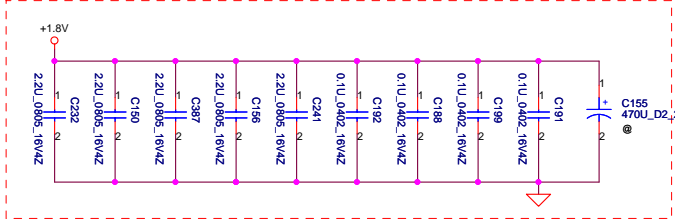
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Date: Monday, May 12, 2008				Sheet 14 of 53

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DDRII-SODIMM SLOT1

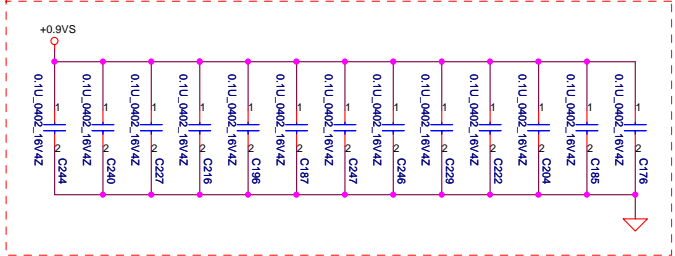
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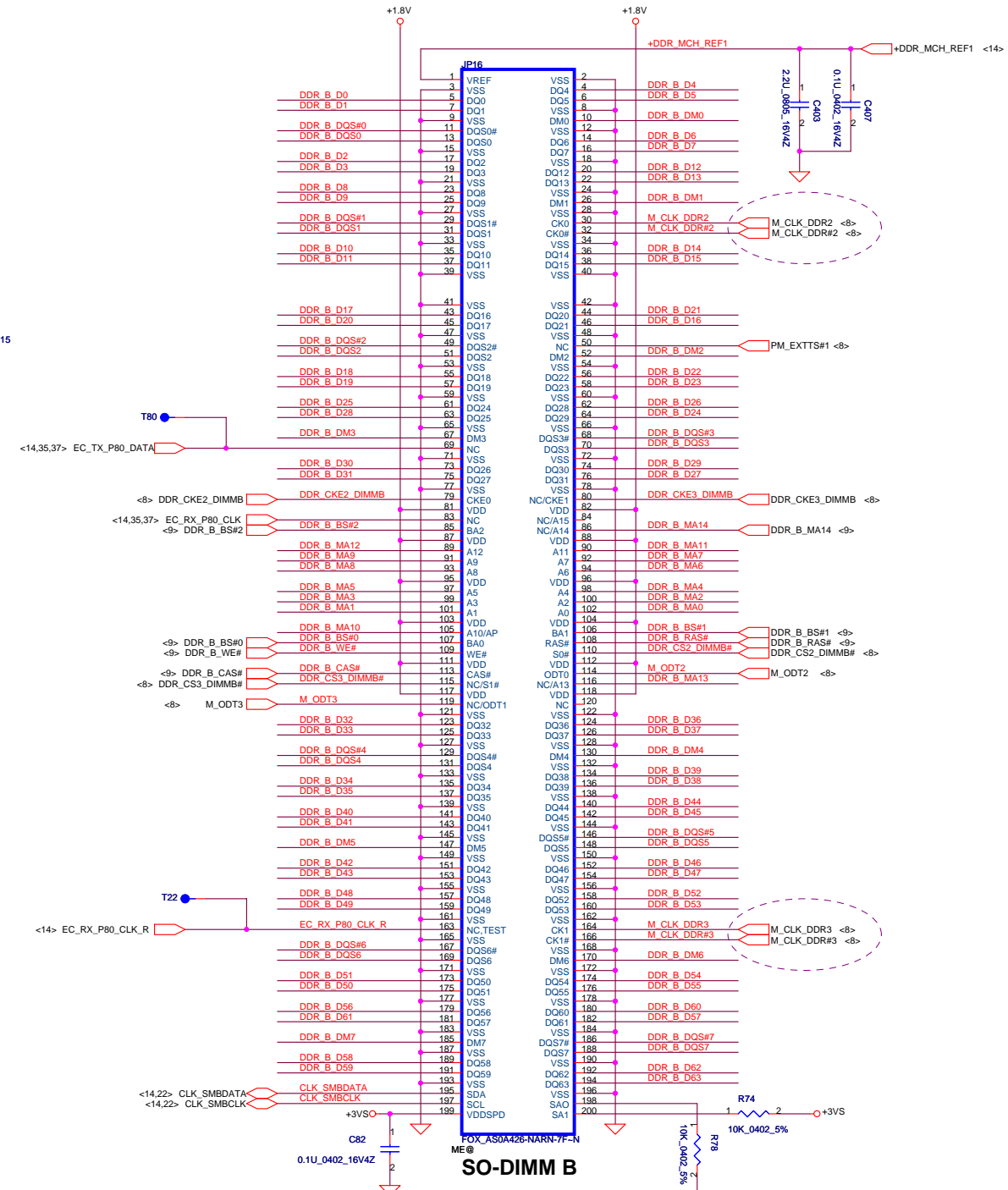
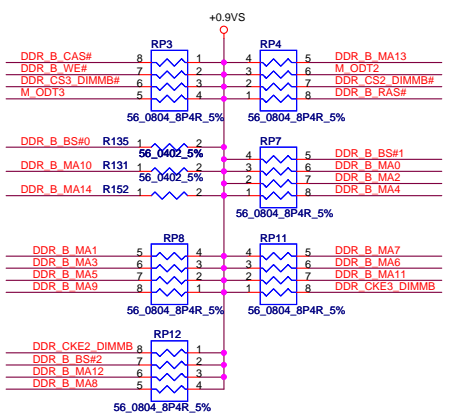
Layout Note:
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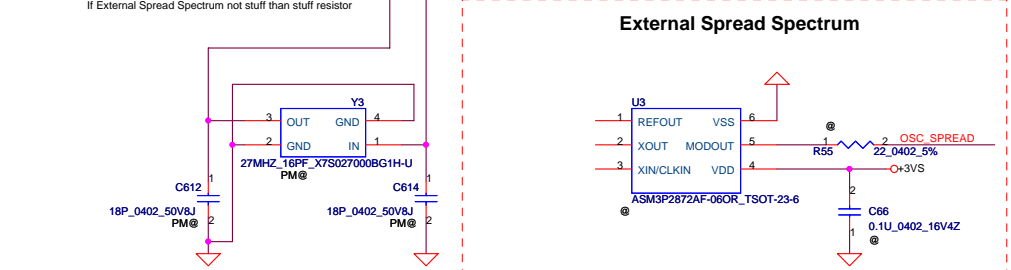
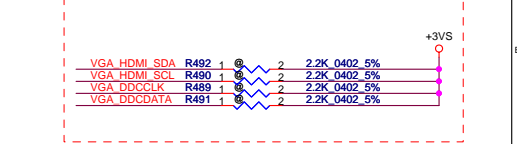
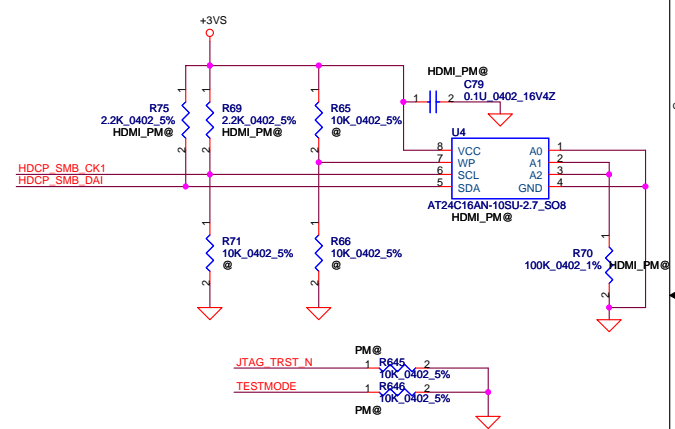
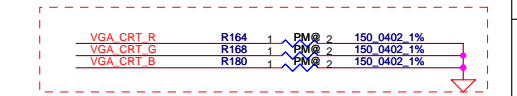
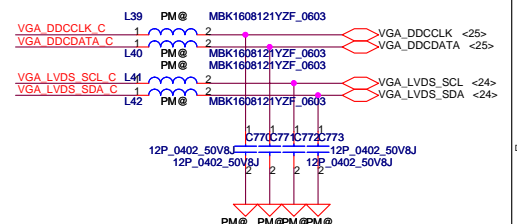
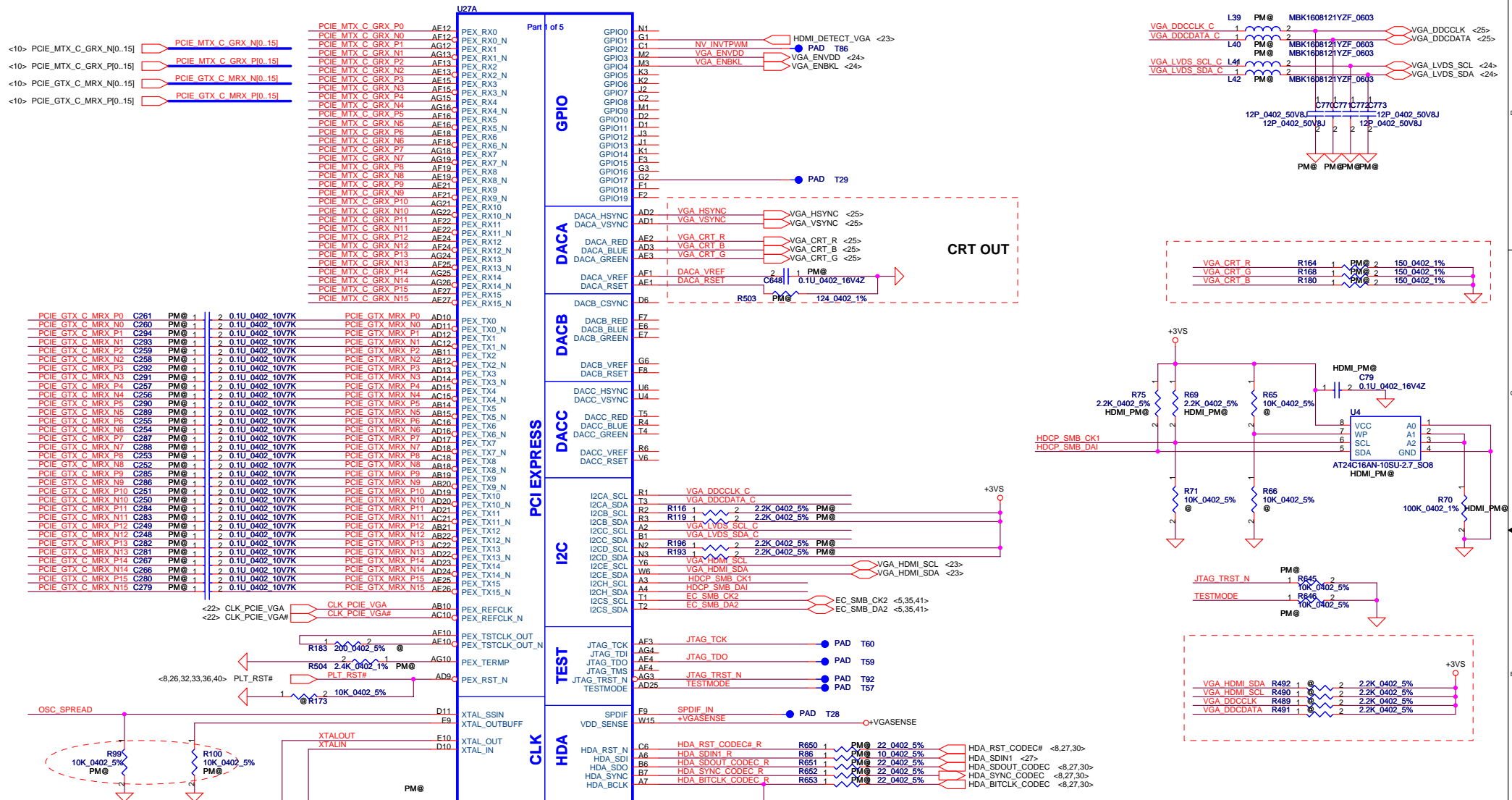


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

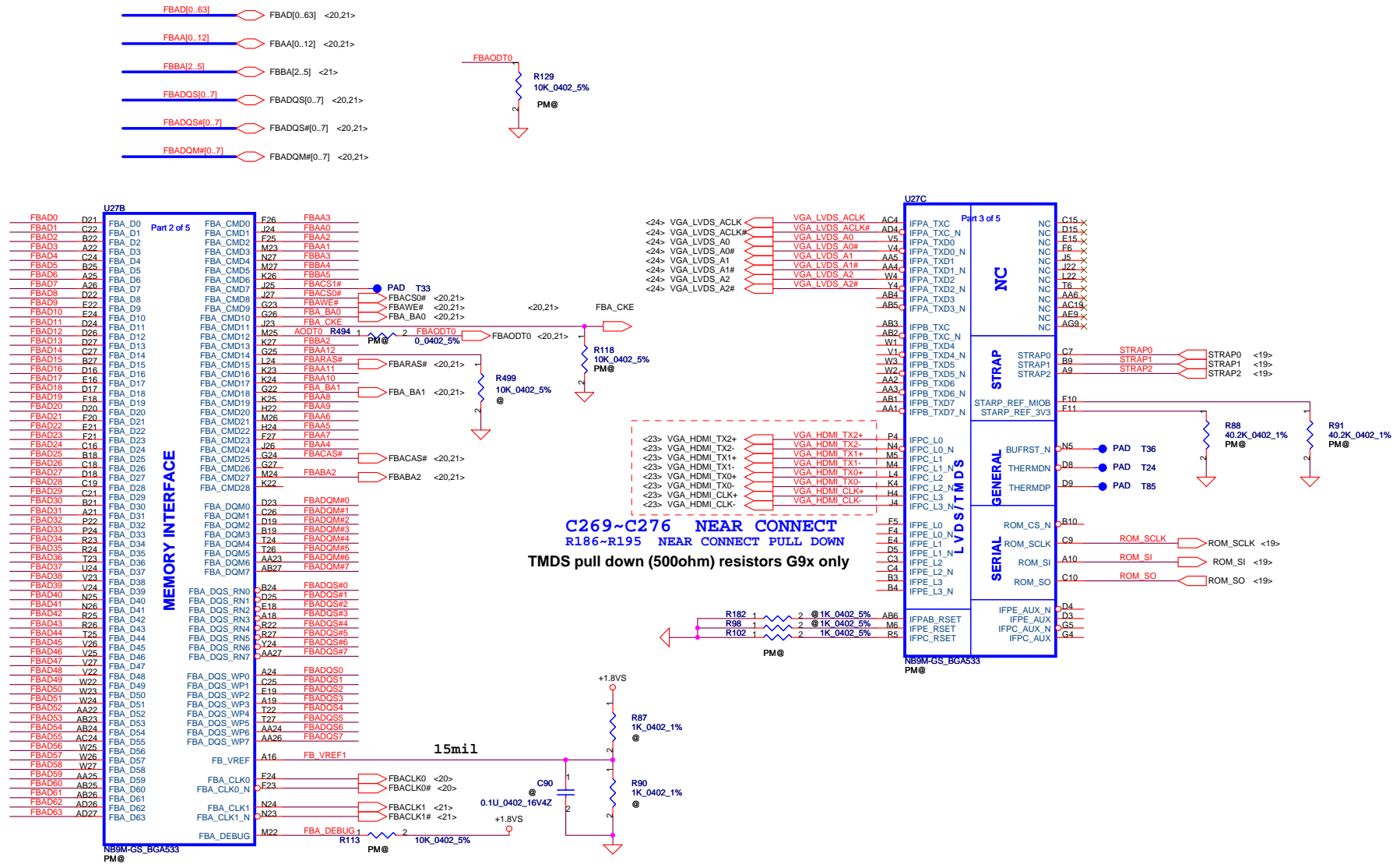


Layout Note:
Place these resistor closely JP42, all trace length Max=1.5"

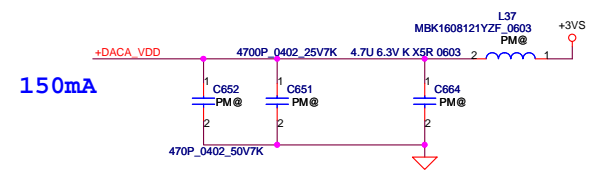
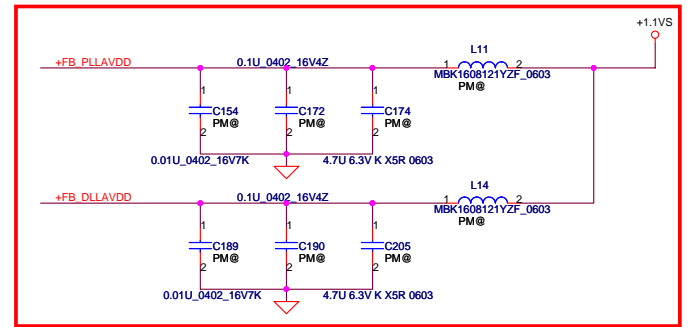
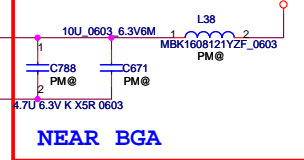
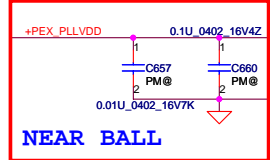
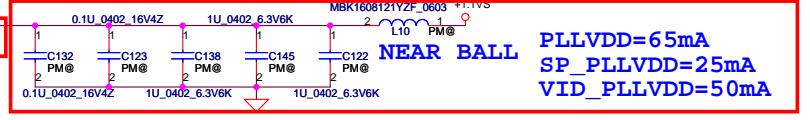
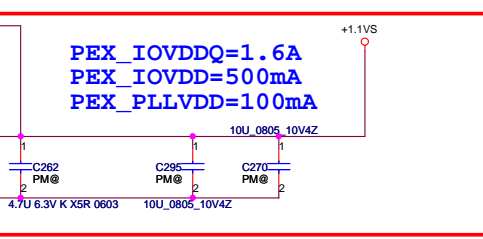
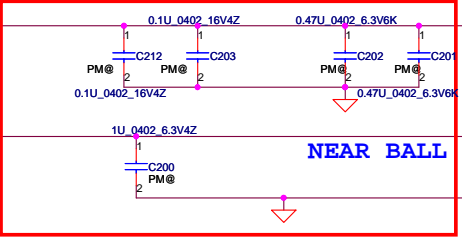
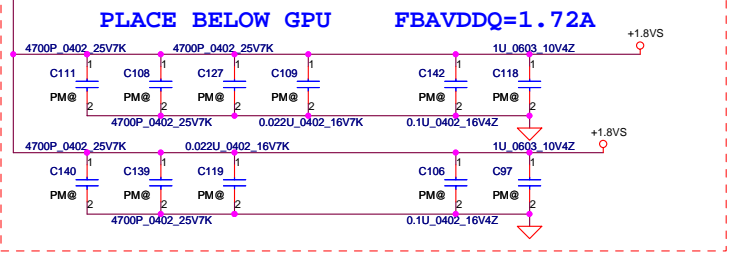
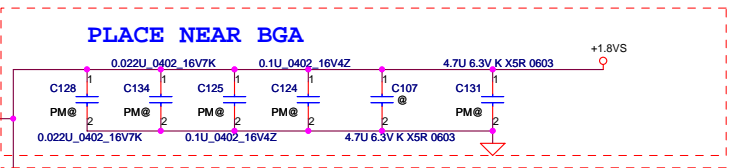
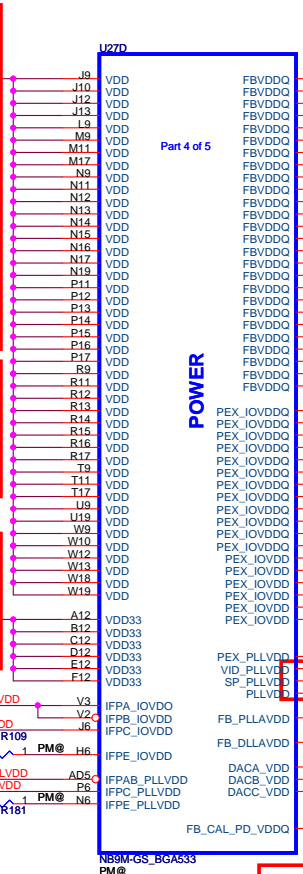
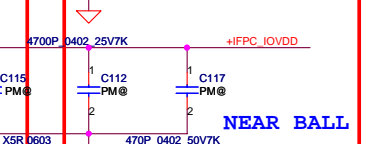
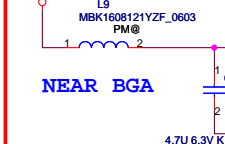
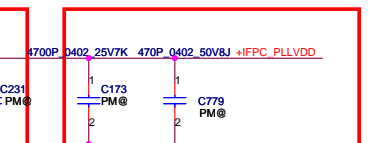
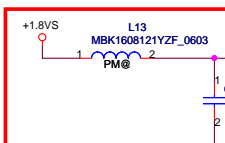
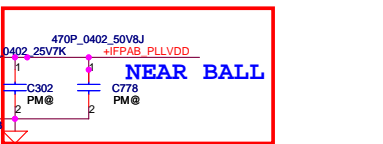
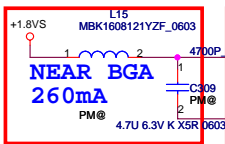
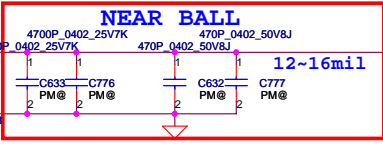
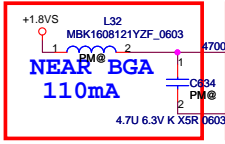
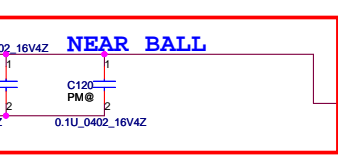
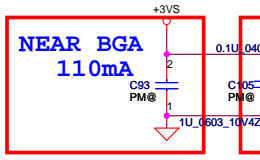
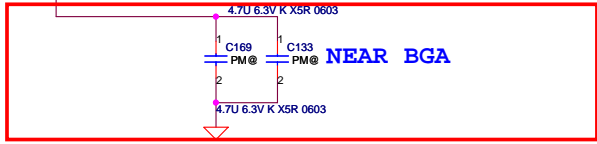
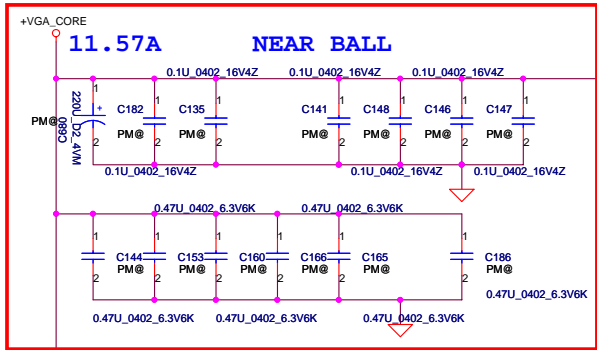




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Size B	Document Number	J1WA3/A4_LA4212P	Rev	1.0
Date:	Wednesday, May 14, 2008	Sheet	16	of 53



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Date: Monday, May 12, 2008				Sheet 17 of 53



Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	NB9M-GS Power	
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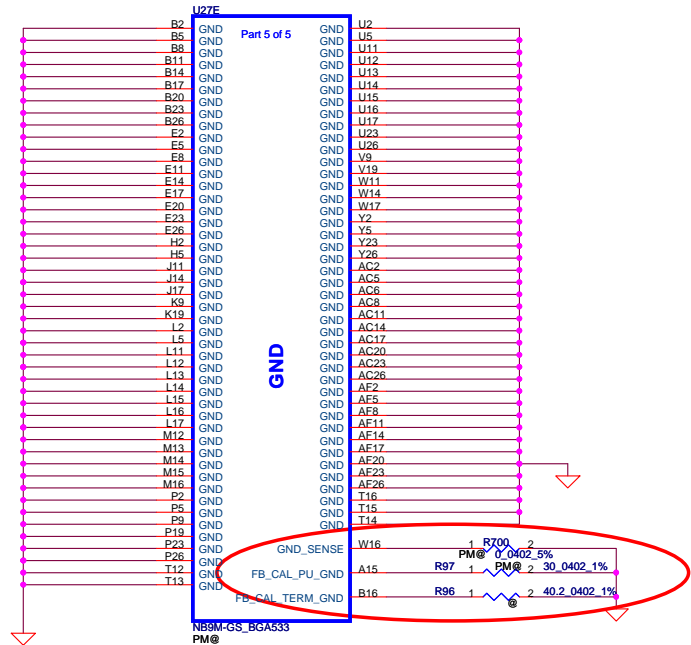
A total of 8 signals are required for GB1 strapping this includes

2 reference signals

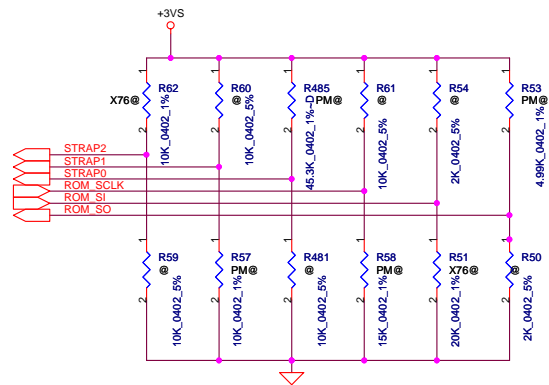
6 physical strapping pins

4 logical strapping bits

A total of 24 logical strapping bits are available



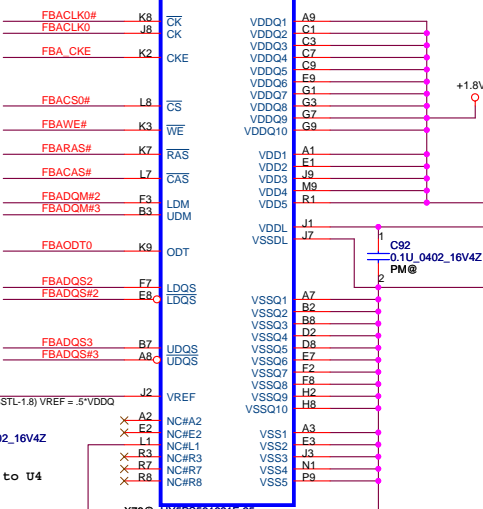
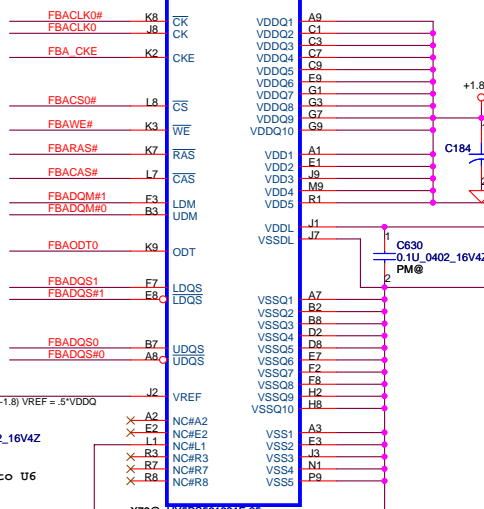
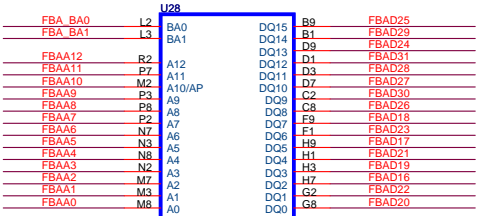
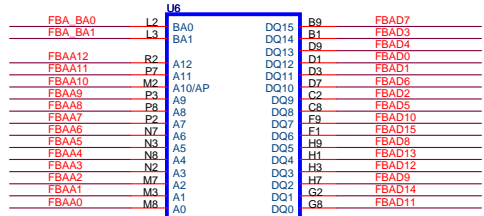
<17> STRAP2
<17> STRAP1
<17> STRAP0
<17> ROM_SCLK
<17> ROM_SI
<17> ROM_SO



GB1 Family GPU Strap Options

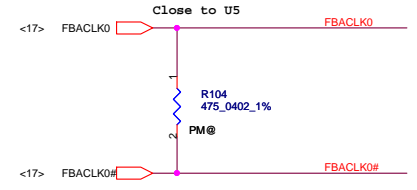
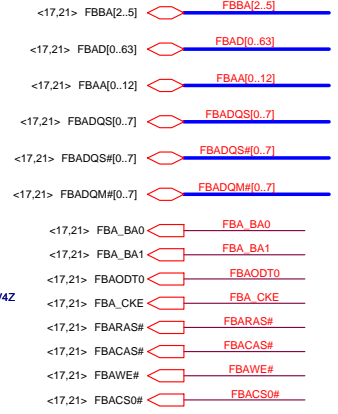
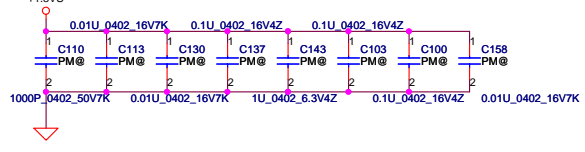
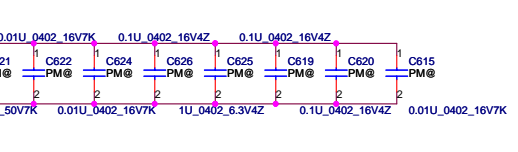
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
NB9M-GS (0x06E9)	Samsung	32Mx16 (5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K	PU 45K
		64Mx16	PU 5K	PD 15K	PD 5K	PU 10K	PD 10K	PU 45K
	Hynix	32Mx16 (7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K	PU 45K
		64Mx16	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K	PU 45K
	Qimonda	32Mx16 (6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K	PU 45K

Component	Manufacturer	Compal PN
DDR2 VRAM (32M*16)	Hynix	SA00000FF30
	Qimonda	SA00000S820
	Samsung	SA00001VX10



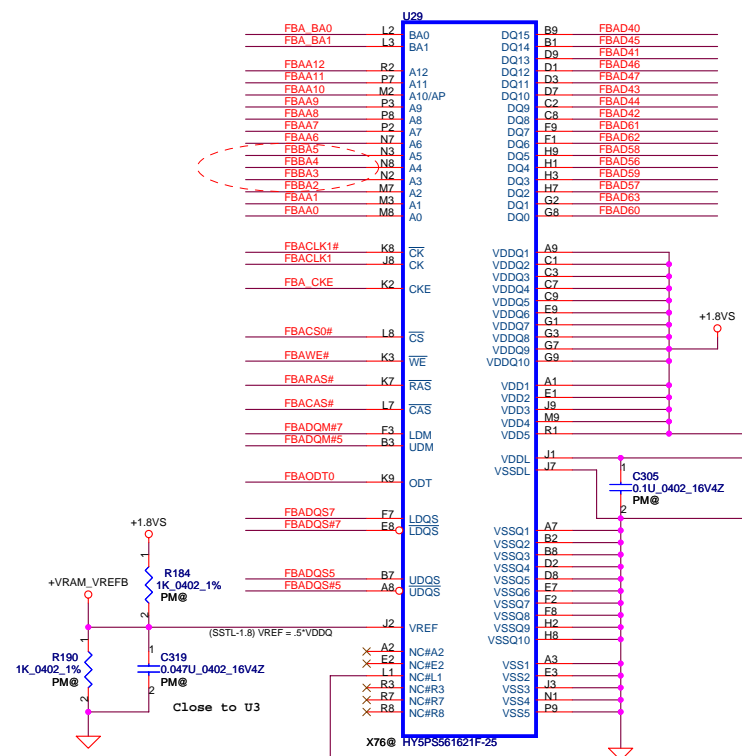
DDR2 BGA MEMORY

DDR2 BGA MEMORY

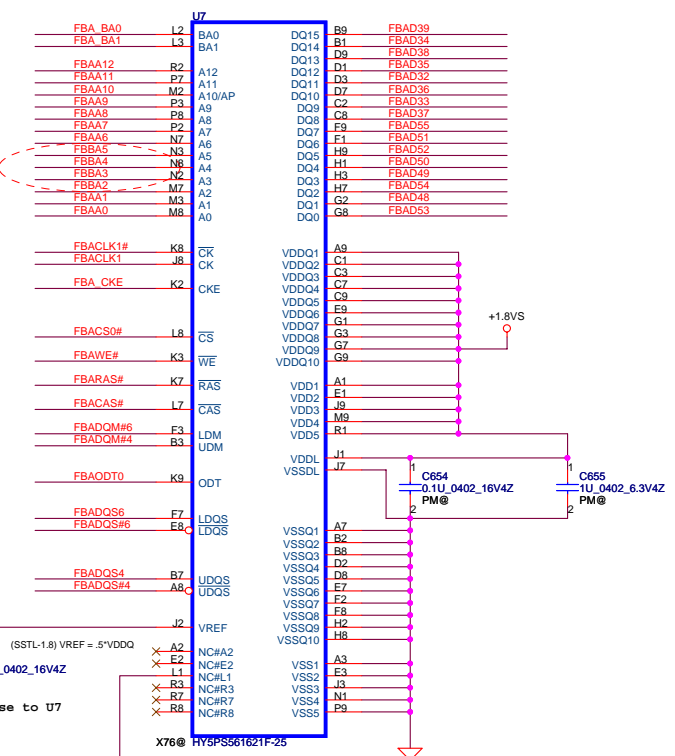


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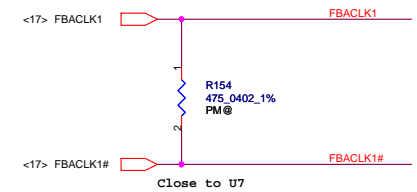
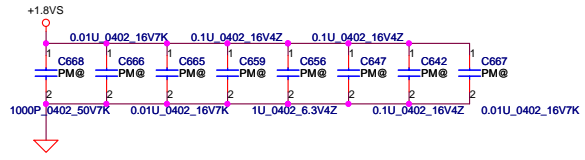
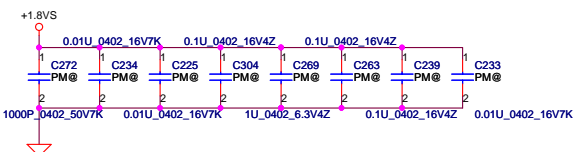
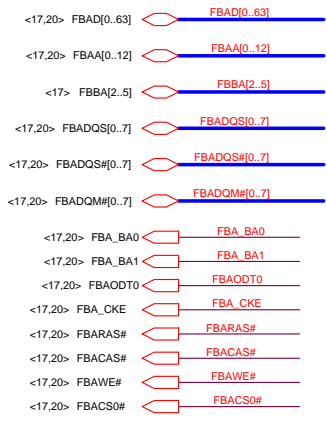
<p align="center">Compal Electronics, Inc.</p> <p align="center">VRAM DDRA</p>		
Title	Size	Rev
	Custom	1.0
Date:	Monday, May 12, 2008	Sheet 20 of 53



DDR2 BGA MEMORY



DDR2 BGA MEMORY

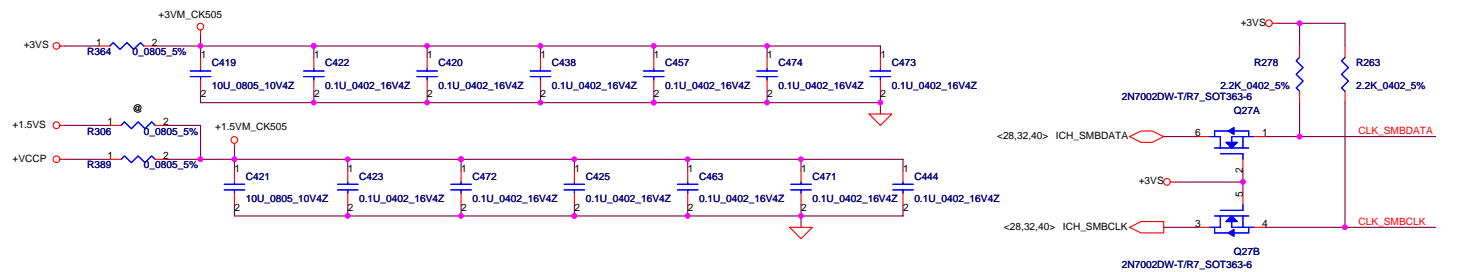


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		2008/10/15

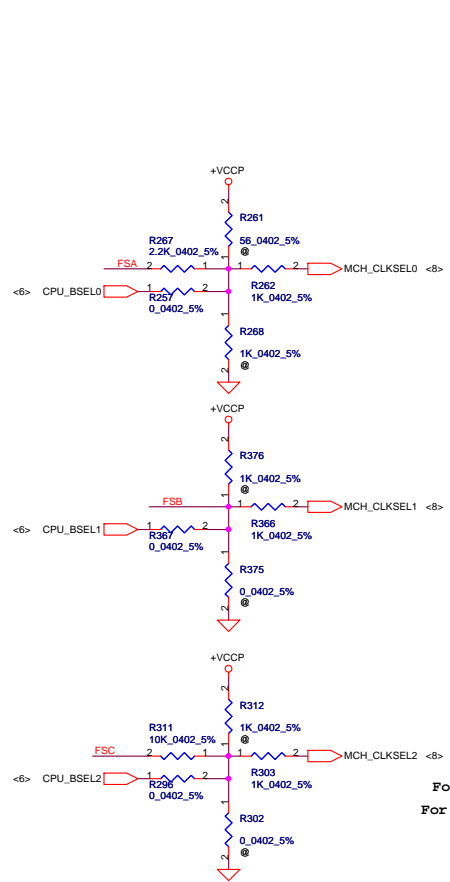
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Title			Compal Electronics, Inc.	
			VRAM DDRB	
Size	Document Number		Rev	
Custom	J1WA3/A4_LA4212P		1.0	
Date:	Monday, May 12, 2008	Sheet	21	of 53

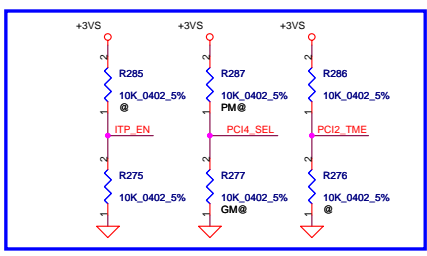
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



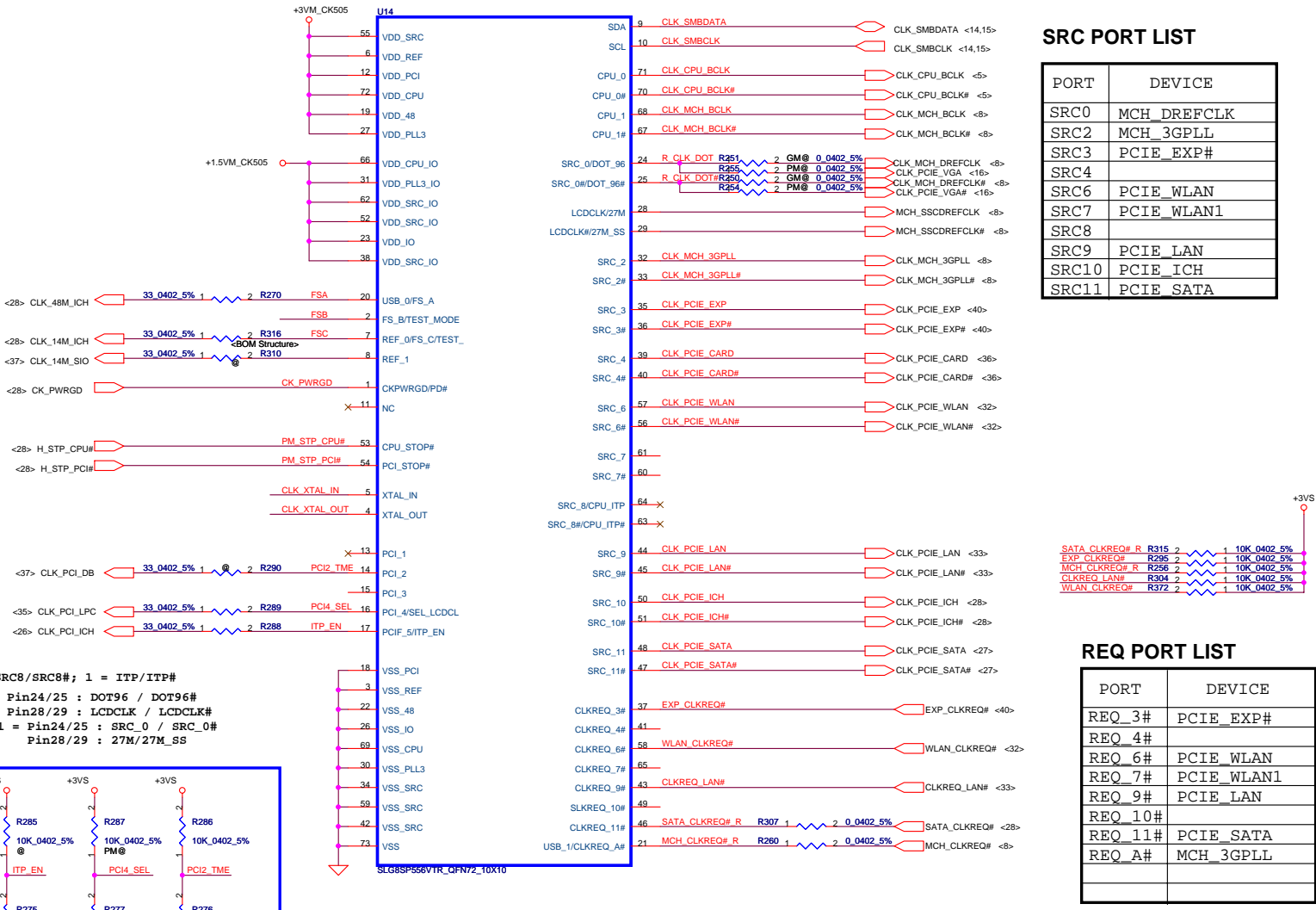
SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 = SRC8 / SRC8#; 1 = ITP / ITP#
 For PCI4_SEL, 0 = Pin24 / 25 : DOT96 / DOT96#
 Pin28 / 29 : LCDCLK / LCDCLK#
 1 = Pin24 / 25 : SRC_0 / SRC_0#
 Pin28 / 29 : 27M / 27M_SS



Routing the trace at least 10mil



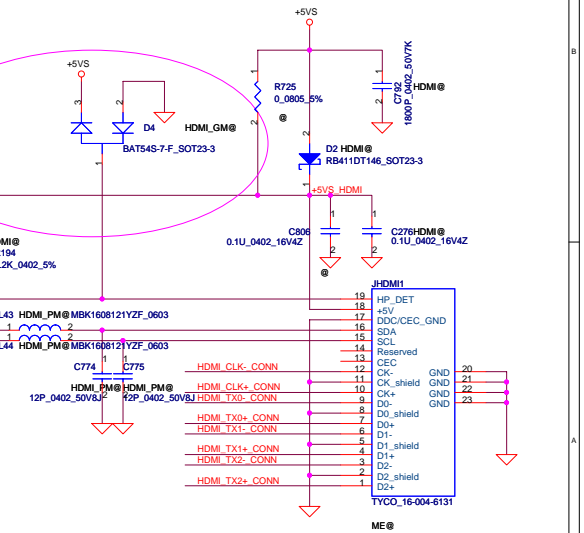
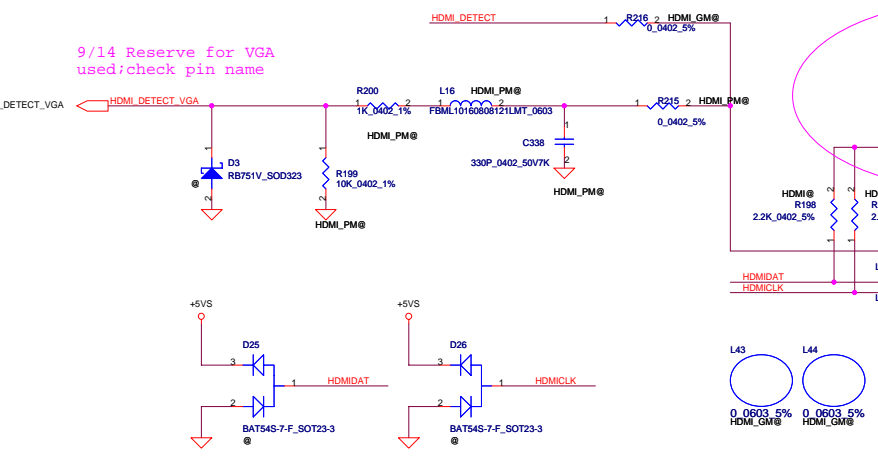
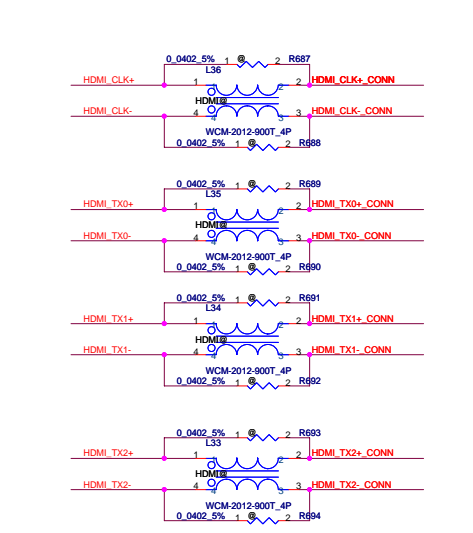
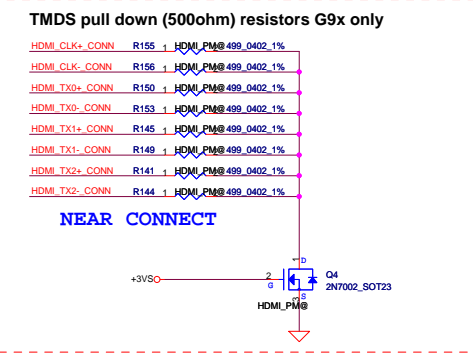
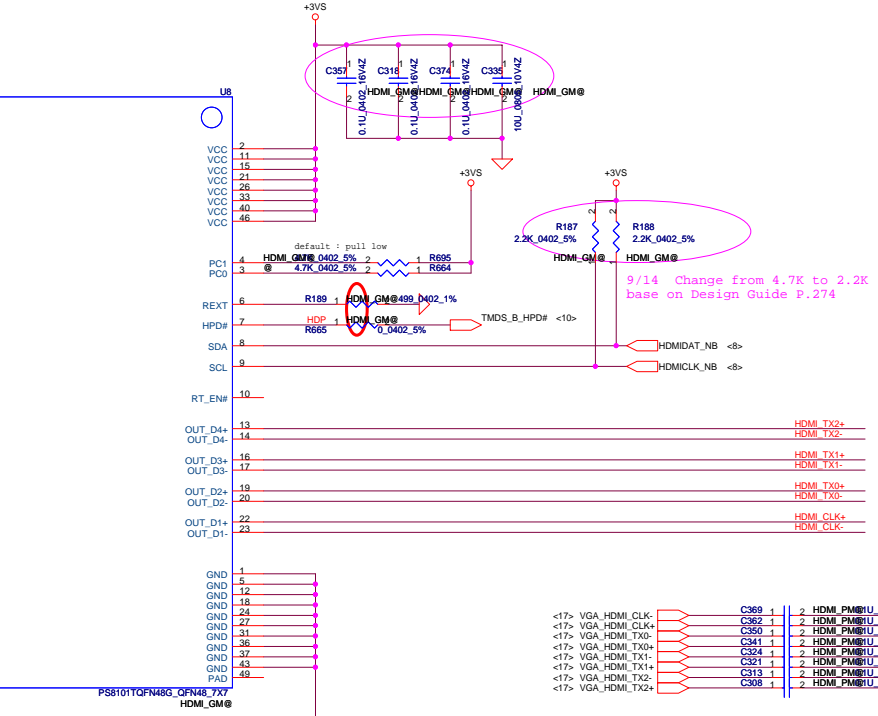
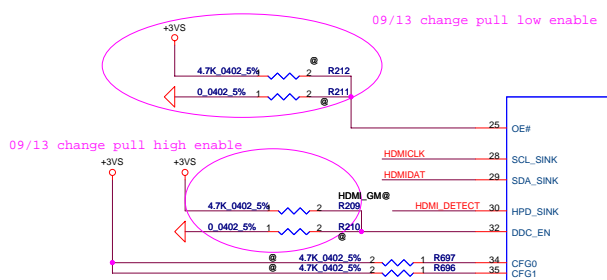
SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3PLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

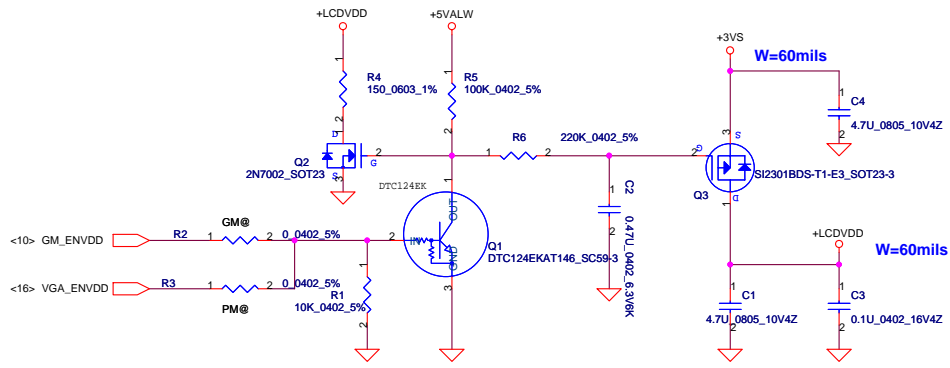
PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3PLL

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Size	Document Number	JIWA3/A4_LA4212P		Rev	1.0
Date:	Monday, May 12, 2008	Sheet	22	of	53

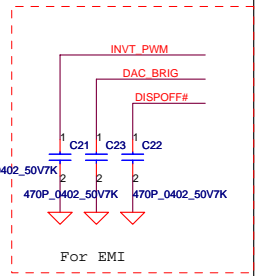
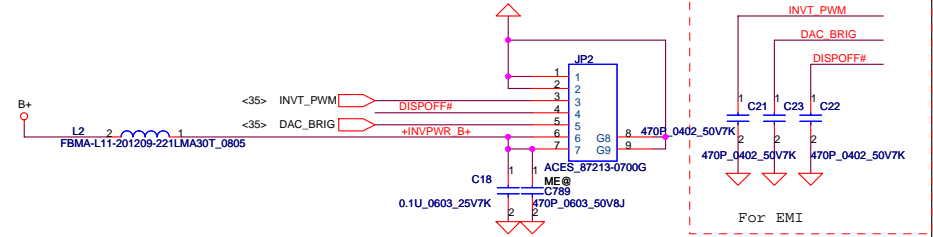


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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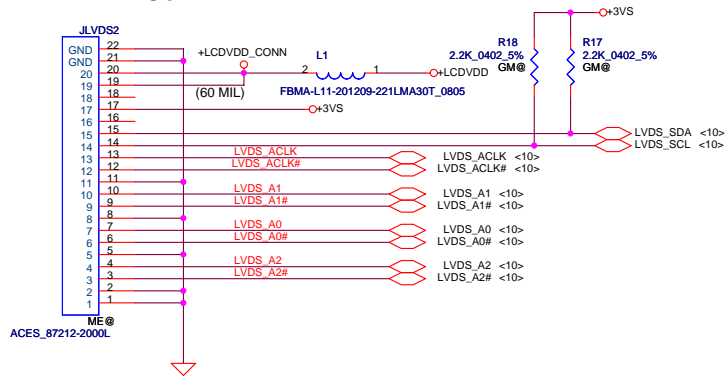
LCD POWER CIRCUIT



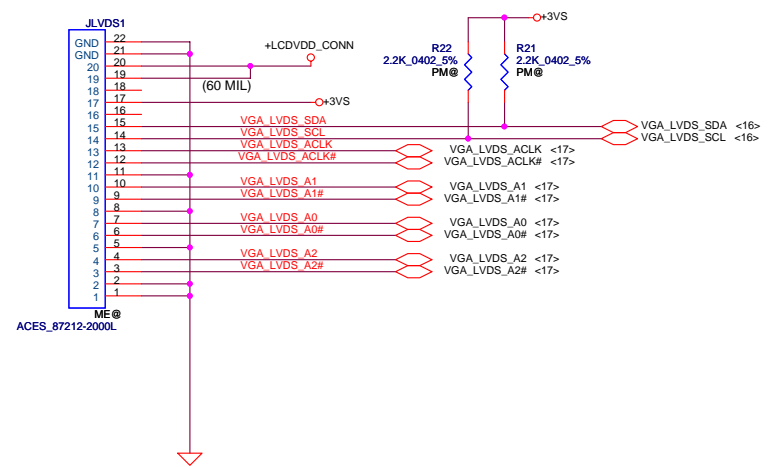
INVERTER Conn.



LCD/PANEL BD. Conn.



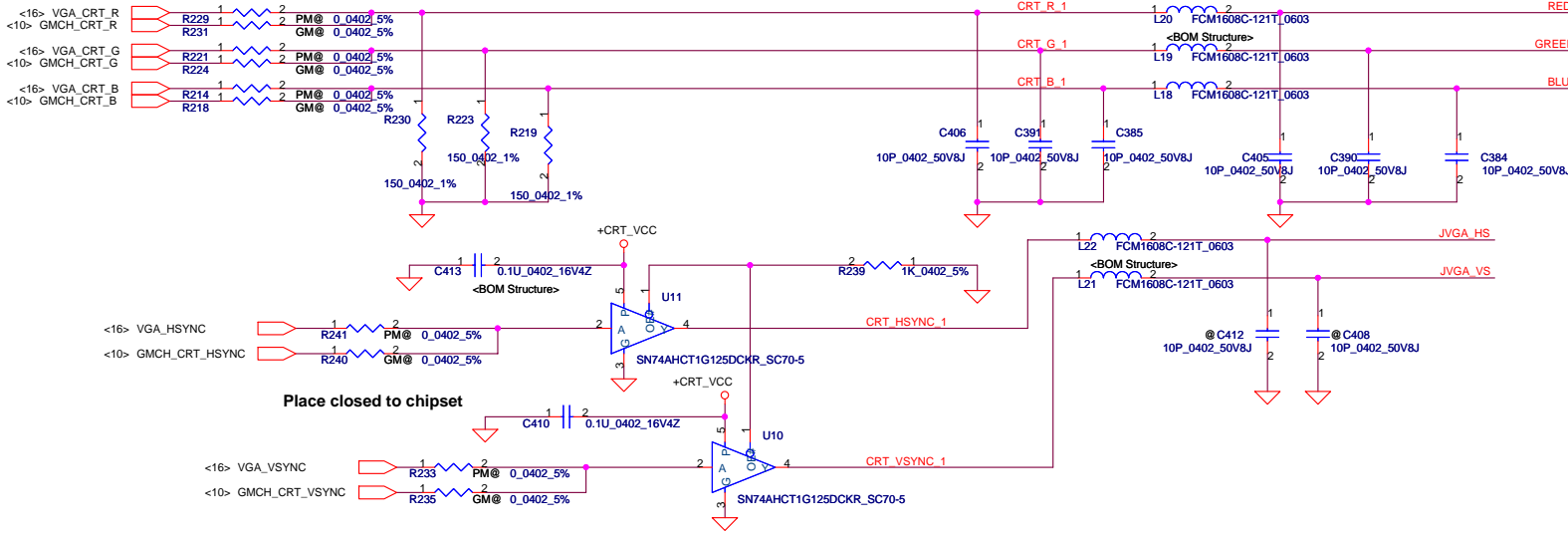
LCD/PANEL BD. Conn.



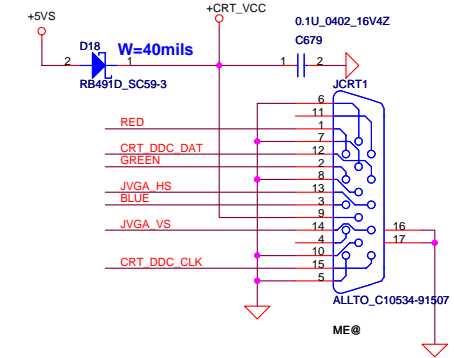
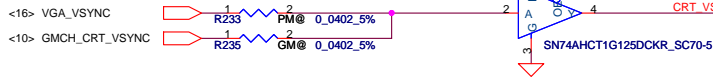
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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Size B	Document Number	Date: Monday, May 12, 2008		J1WA3/A4_LA4212P	Rev 1.0
				Sheet 24	of 53

CRT Connector

Place closed to chipset



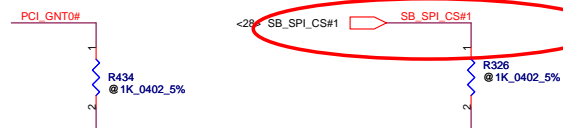
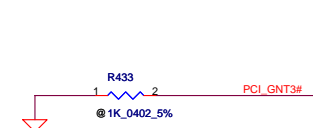
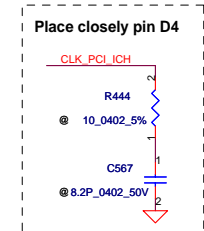
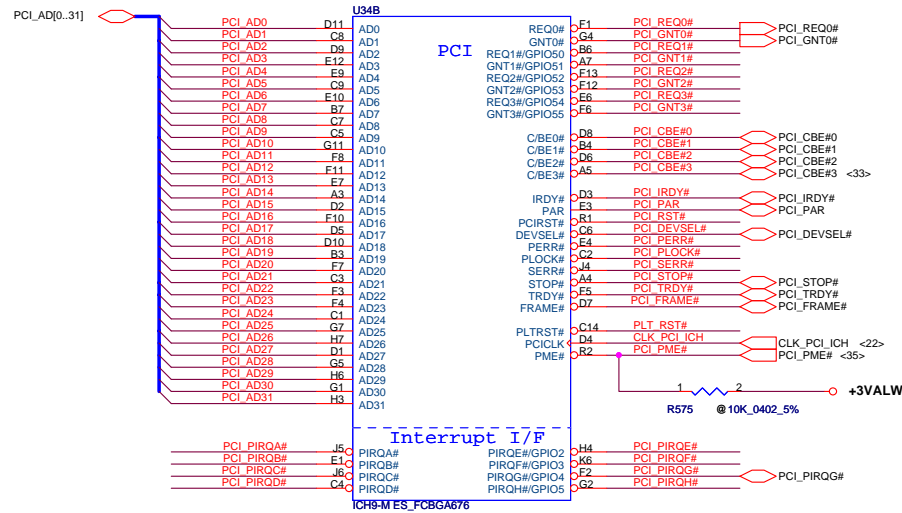
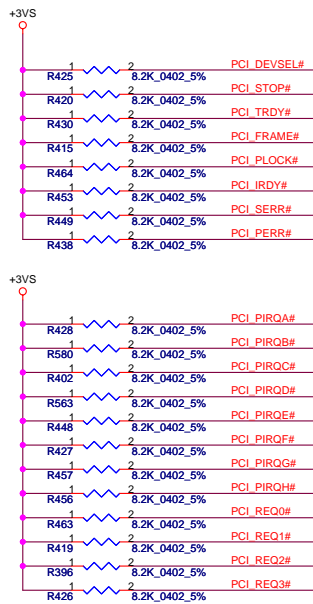
Place closed to chipset



PIN ASSIGNMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

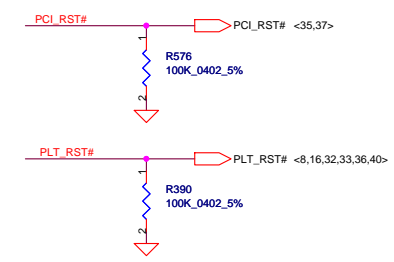
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	
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Size	Document Number	Rev		1.0
Custom	J1WA3/A4_LA4212P	Date:		Monday, May 12, 2008
		Sheet	25 of 53	

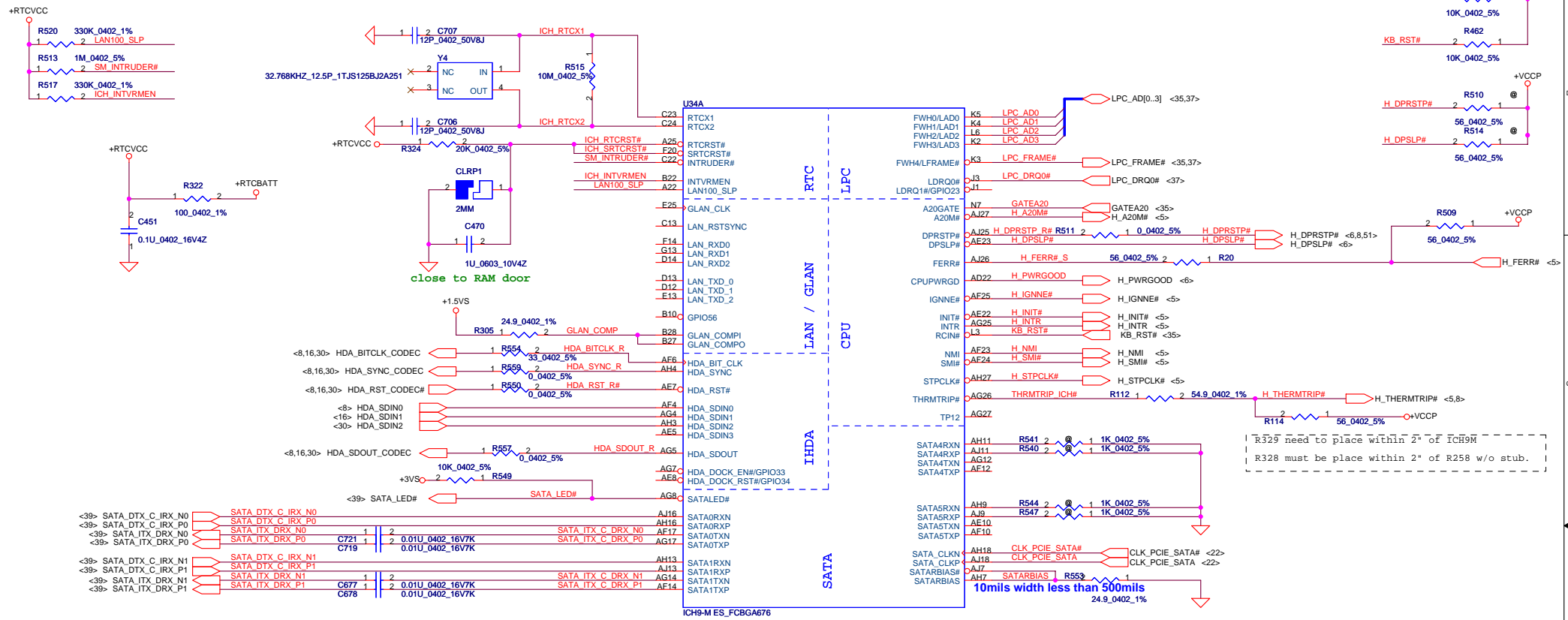


Pull high?

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

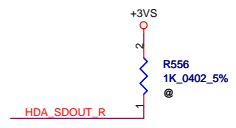
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



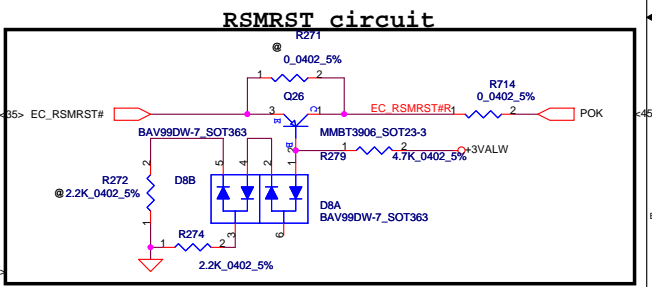
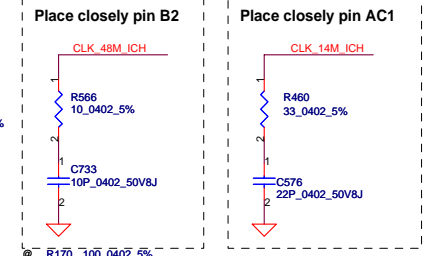
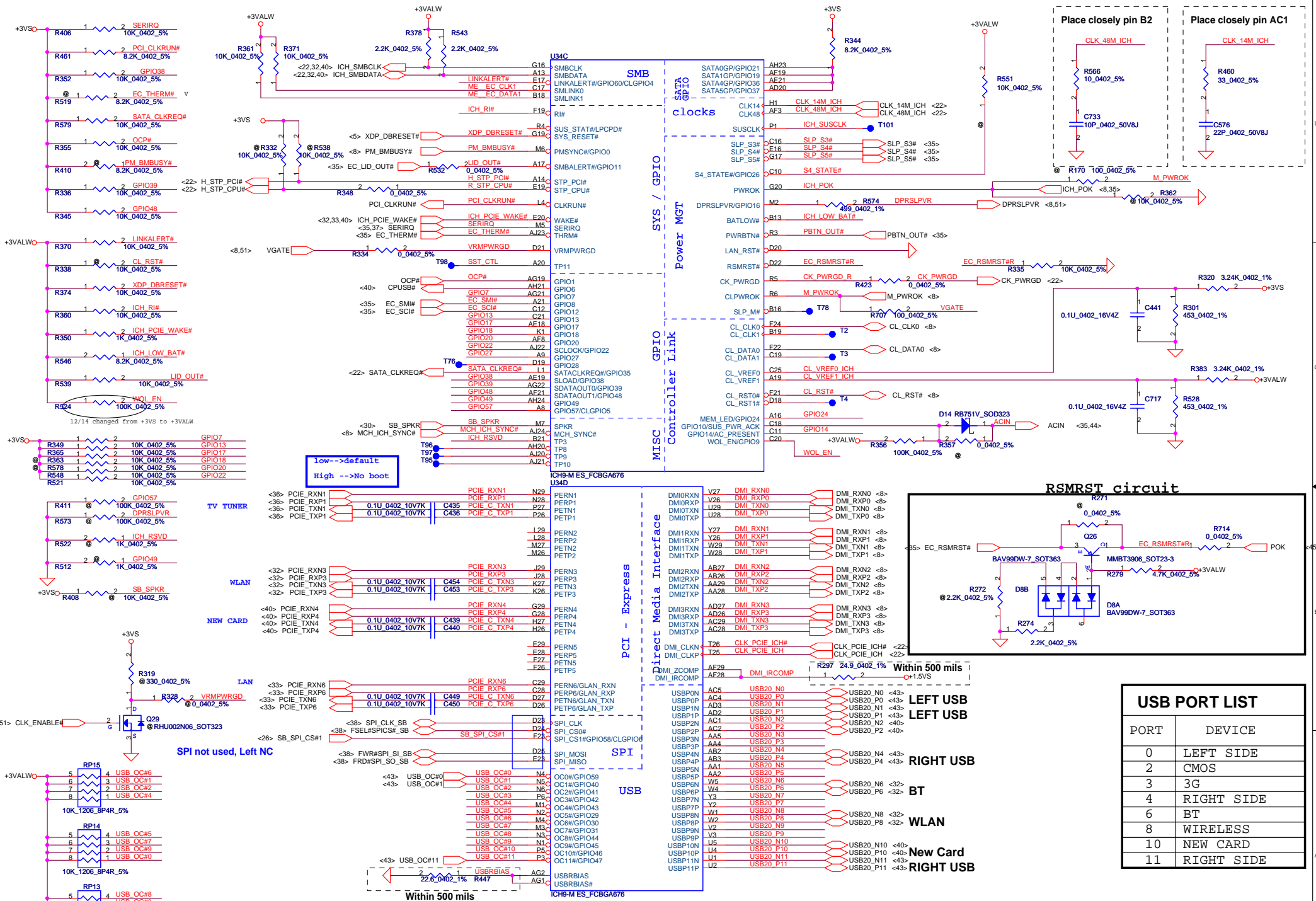


R329 need to place within 2" of ICH9M
 R328 must be place within 2" of R258 w/o stub.

Need check



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1



USB PORT LIST	
PORT	DEVICE
0	LEFT SIDE
2	CMOS
3	3G
4	RIGHT SIDE
6	BT
8	WIRELESS
10	NEW CARD
11	RIGHT SIDE

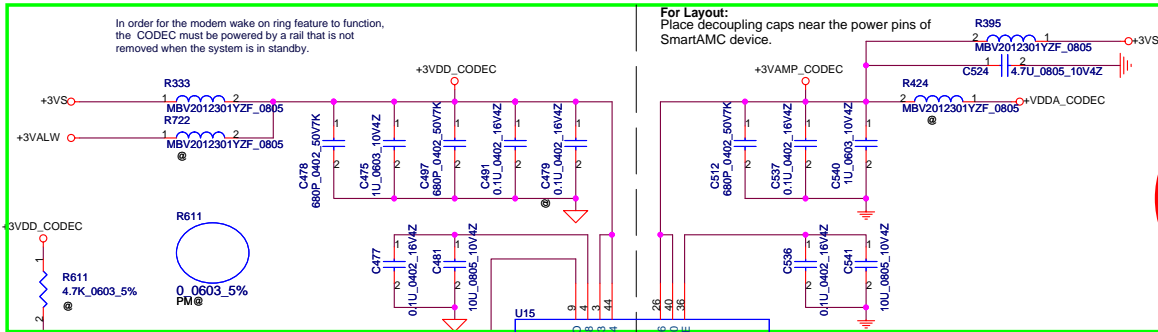
Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15

Compal Electronics, Inc.		
Title		
ICH9M(3/4)-USB,GPIO,PCIE		
Size	Document Number	Rev
Custort	J1WA3/A4_LA421P	1.0
Date:	Wednesday, May 14, 2008	Sheet 28 of 53

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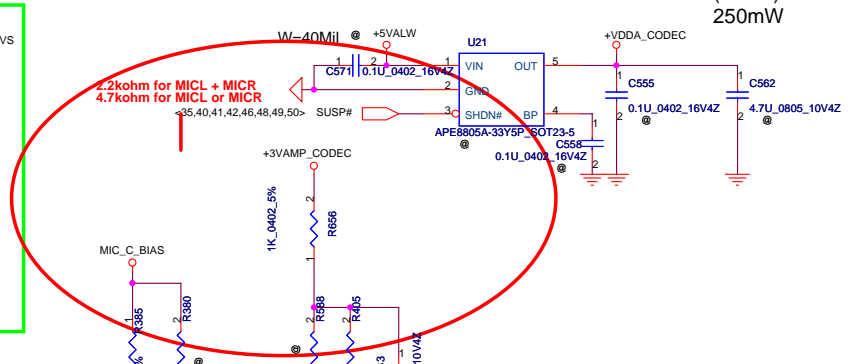
AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

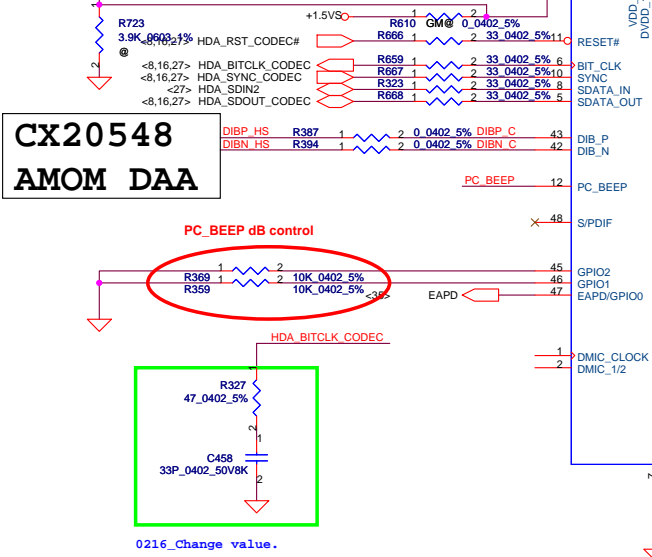


CODEC POWER

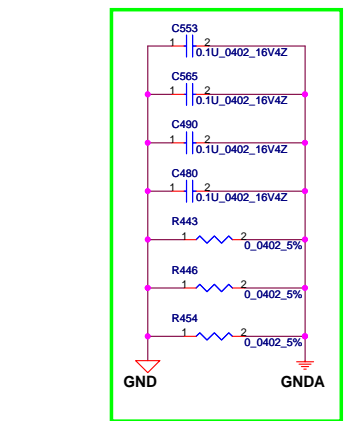
(3.33V)
250mW



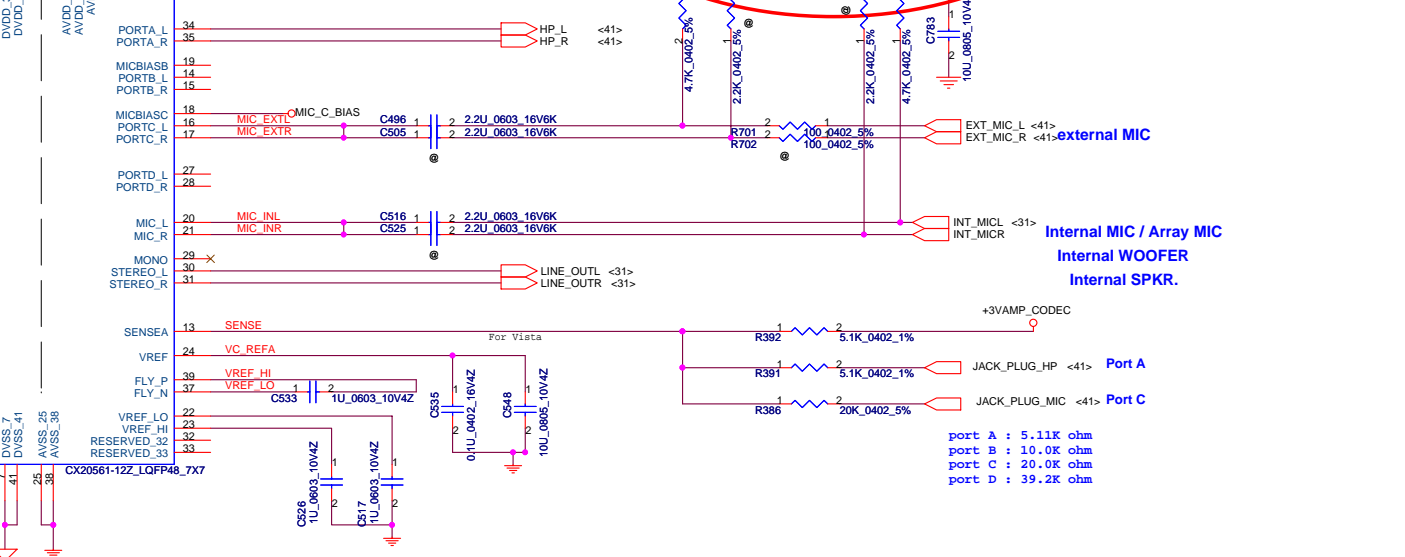
CX20548 AMOM DAA



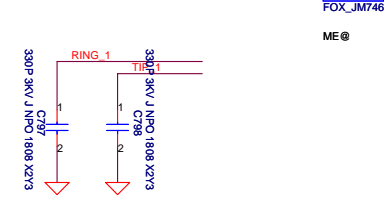
DIGITAL ANALOG



Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate



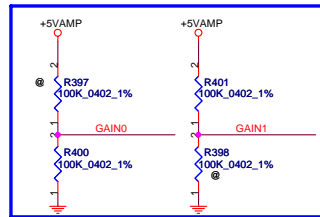
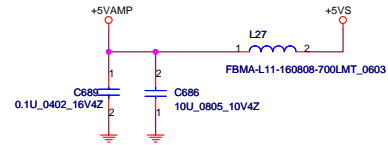
CX20548 AMOM DAA



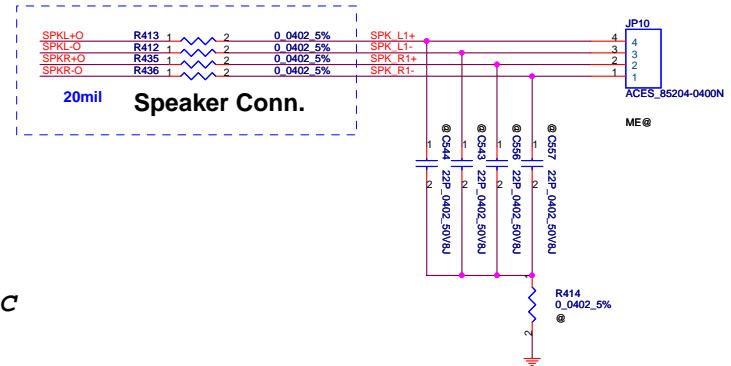
Security Classification		Compal Secret Data		Title	
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Size	Document Number	Date		Rev	
	JJWA3/A4_LA4212P	Monday, May 12, 2008		1.0	
				Sheet 30 of 53	

Speaker Amplifier

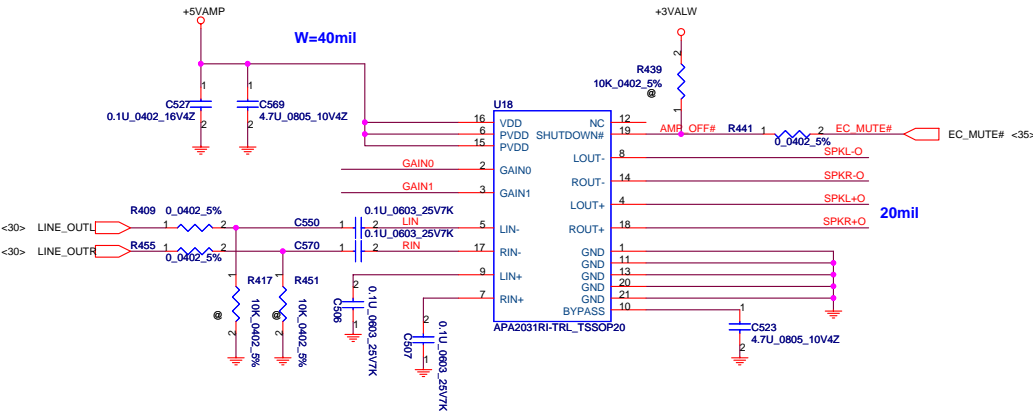
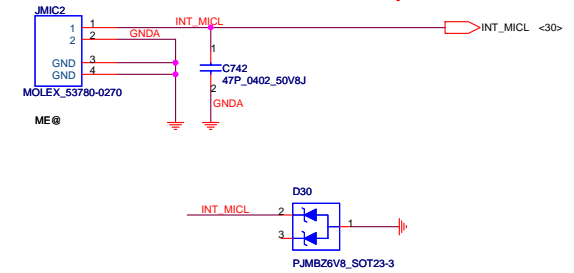
1nd = APA2031 (SA00001RZ00)
 2nd = G1431F2U (SA000012Y00)



	GAIN0	GAIN1	
	0	0	6dB
	0	1	10dB
	1	0	15.6dB
	1	1	21.6dB



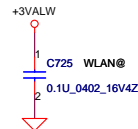
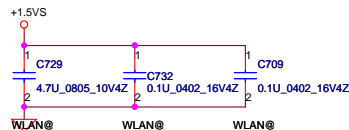
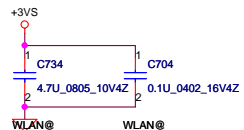
INT MIC



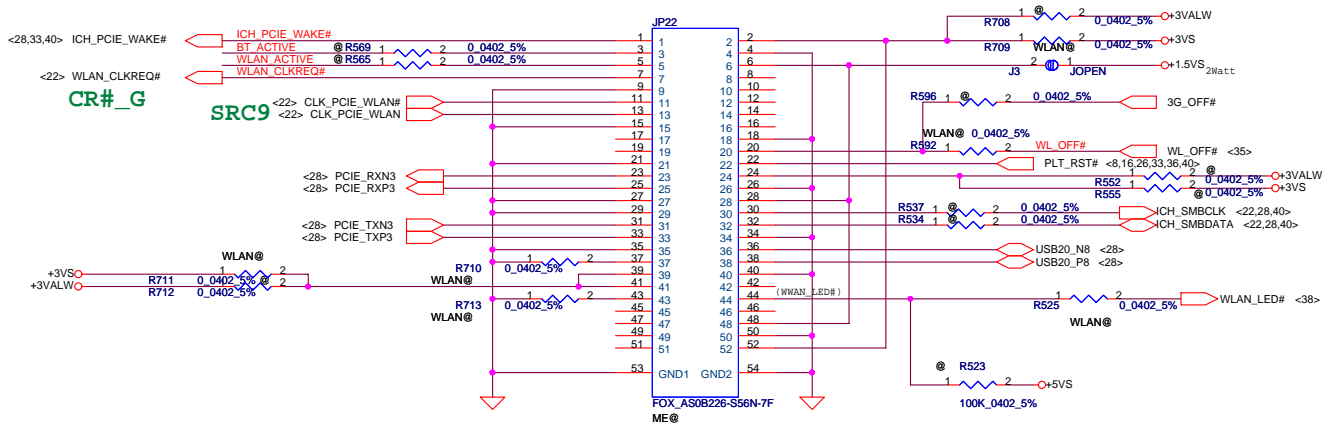
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	
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			JIWA3/A4_LA4212P	1.0
Date:	Monday, May 12, 2008	Sheet	31	of 53

Mini-Express Card for 3G Or TV Tuner

Mini-Express Card for WLAN

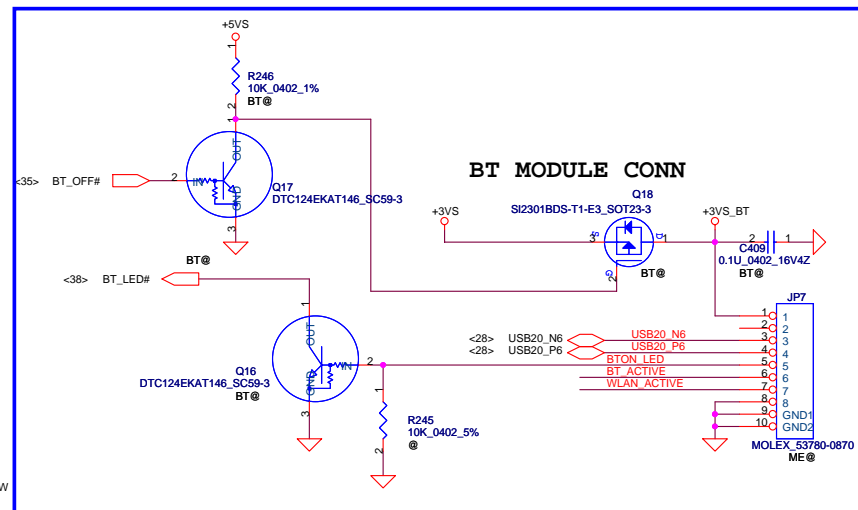


Mini-Express Card (Slot 1-WLAN)



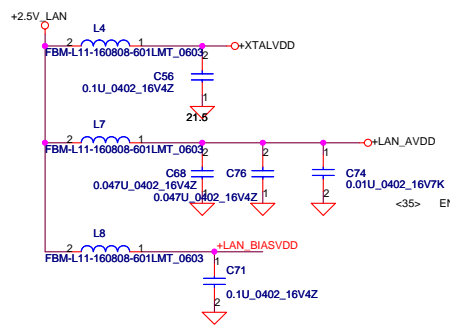
2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

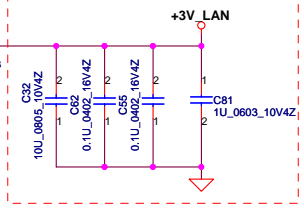


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Mini-Card/3G/FeliCa/BT	
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Size	Document Number	J1WA3/A4_LA4212P		Rev	1.0
Date:	Tuesday, May 20, 2008	Sheet	32	of	53

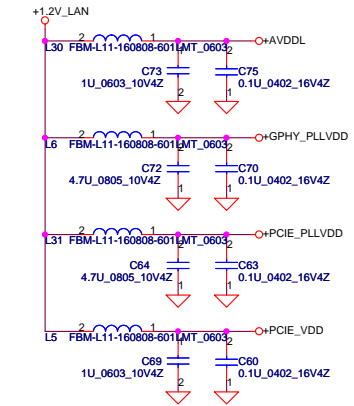
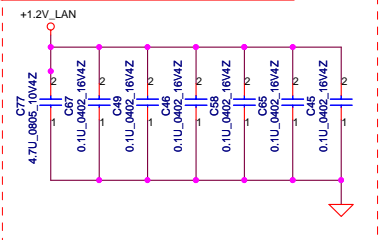
Layout Notice : Filter place as close chip as possible.



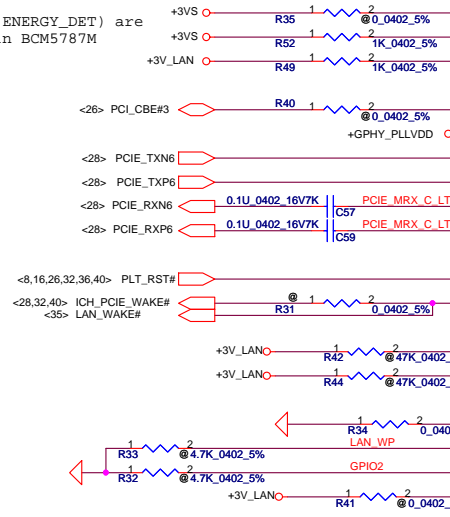
Layout Notice : Place as close chip as possible.



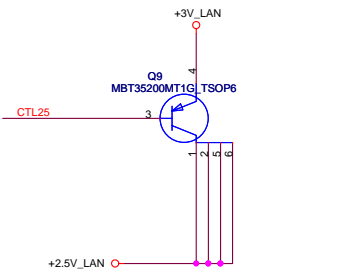
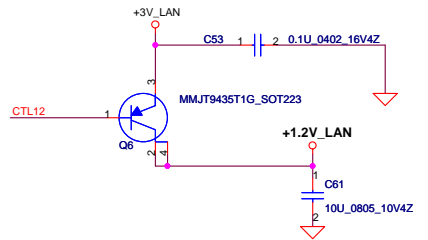
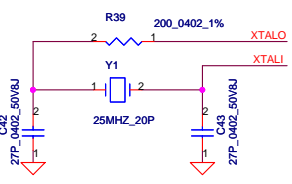
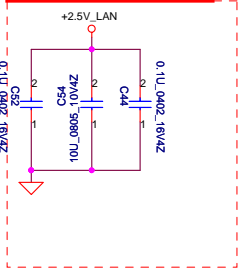
Layout Notice : 1.2V filter. Place as close chip as possible.



(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M

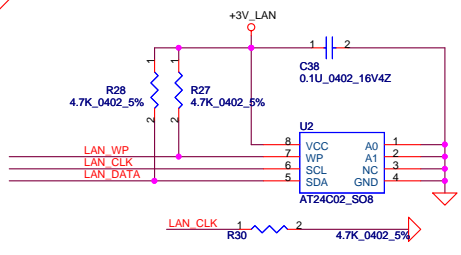


Layout Notice : Place as close chip as possible.



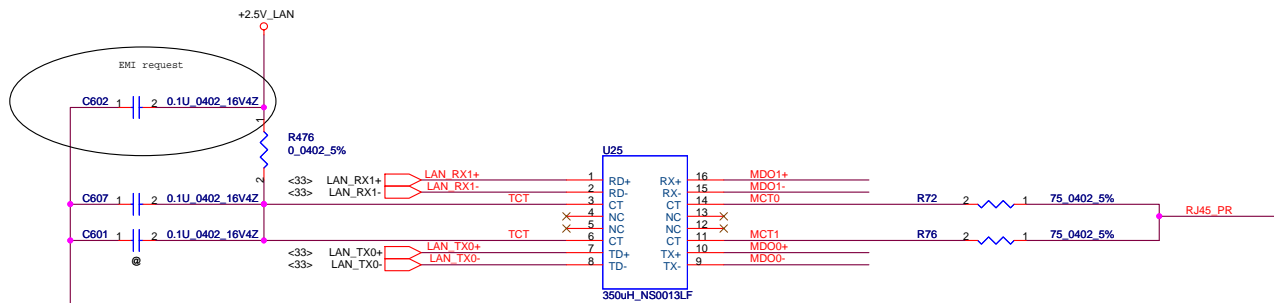
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

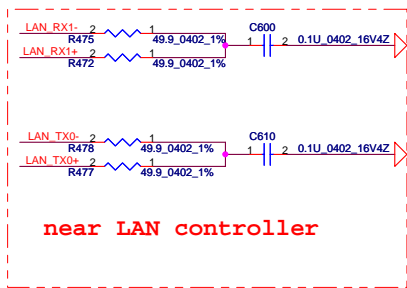


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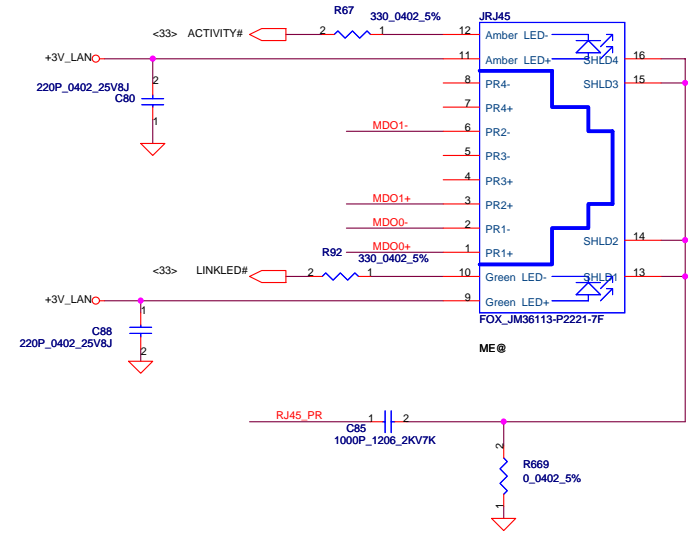
Compal Electronics, Inc.			
Title			
BCM5787MKML			
Size	Document Number	Rev	
Custom	J1WA3/A4_LA4212P	1.0	
Date:	Monday, May 12, 2008	Sheet	33 of 53



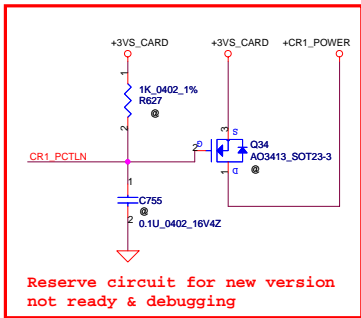
Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



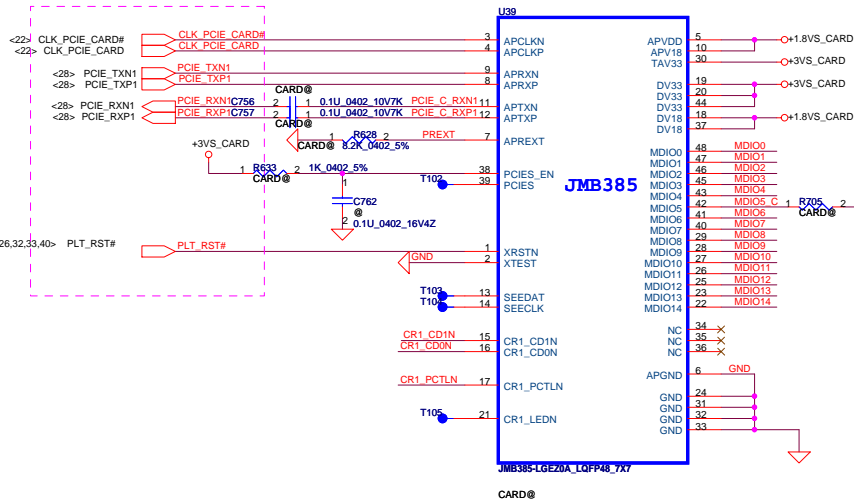
RJ45 CONN



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				Document Number	1.0
				J1WA3/A4_LA4212P	
				Date: Monday, May 12, 2008	Sheet 34 of 53

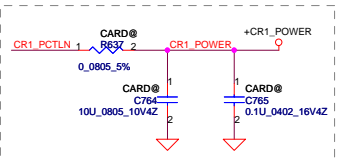
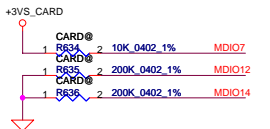
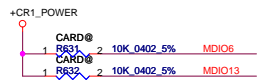


Need check CLK GEN & SB select pin & page



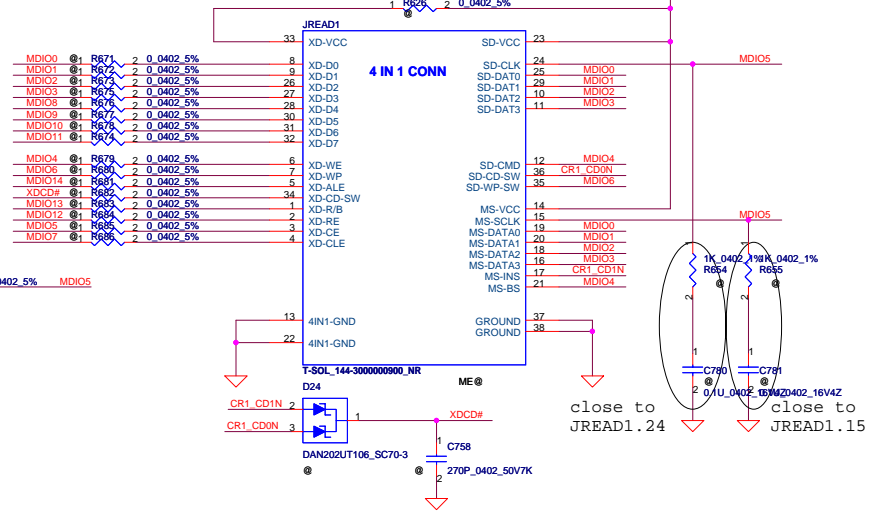
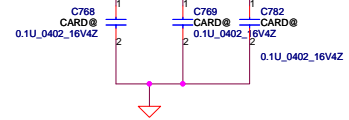
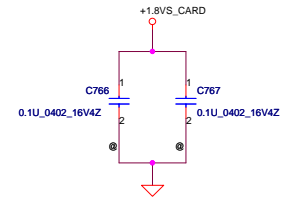
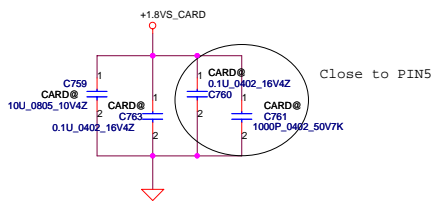
JMB385 Operation Modes

	Normal
XTEST	0
CR1_CD0N	X
CR1_CD1N	X



Use 0805 type and over 20 mils trace width on both side

Card Reader power circuit

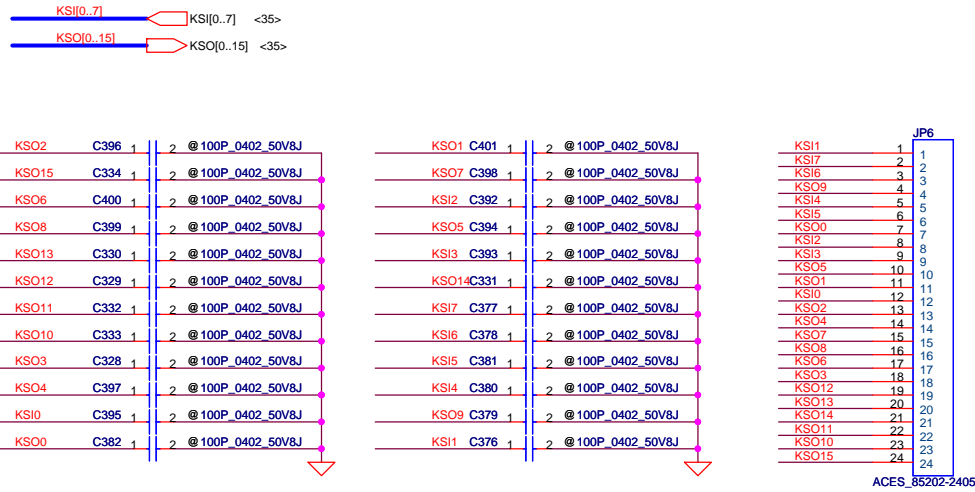


SD,MMC,MS,XD multi-function pin define

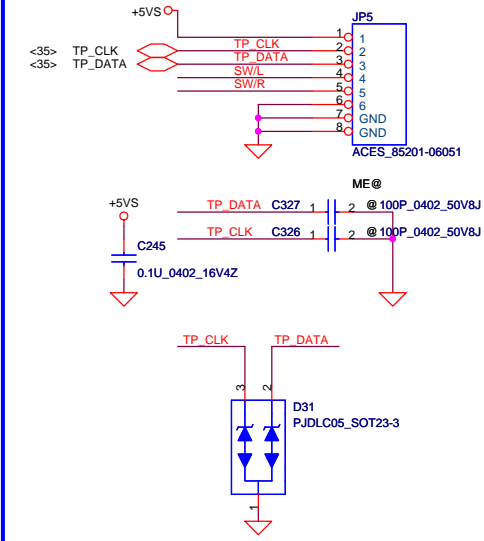
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SD_DAT0	MMC_DAT0	MS_DAT0	XD_DAT0
MDIO01	SD_DAT1	MMC_DAT1	MS_DAT1	XD_DAT1
MDIO02	SD_DAT2	MMC_DAT2	MS_DAT2	XD_DAT2
MDIO03	SD_DAT3	MMC_DAT3	MS_DAT3	XD_DAT3
MDIO04	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO05	SDCLK1	MMCCLK	MSCCLK	XD_CE#
MDIO06	SD_WP#	MMC_WP#		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_DAT4	MS_DAT4	XD_DAT4
MDIO09		MMC_DAT5	MS_DAT5	XD_DAT5
MDIO10		MMC_DAT6	MS_DAT6	XD_DAT6
MDIO11		MMC_DAT7	MS_DAT7	XD_DAT7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE

Cardreader contactor not support MMC & MS Bit 4~7

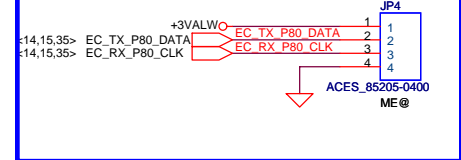
INT_KBD Conn.



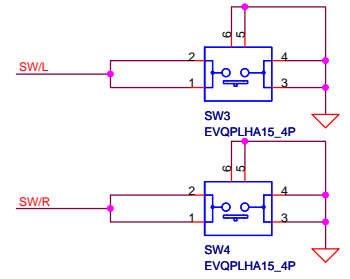
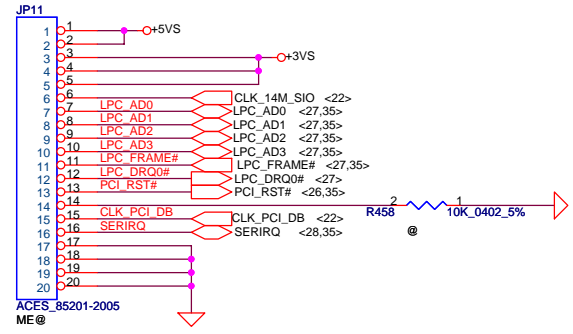
To TP/B Conn.



EC DEBUG PORT

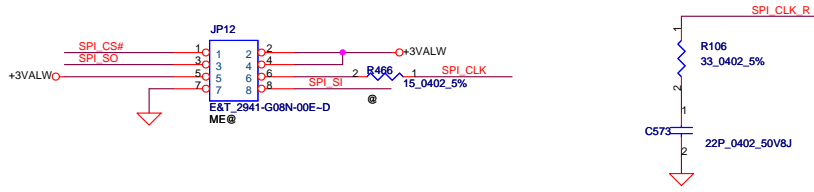
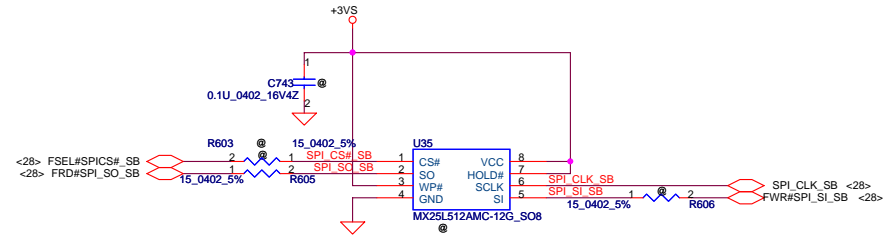
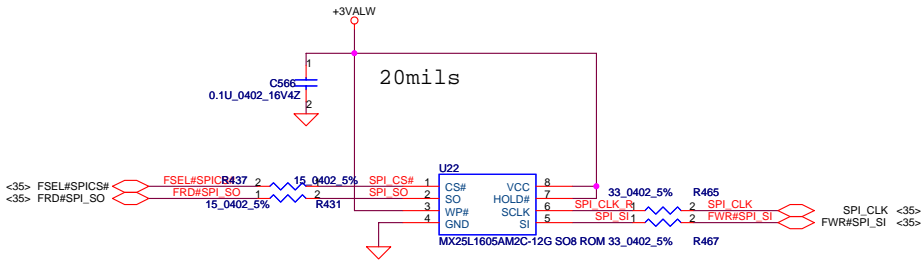


FOR LPC SIO DEBUG PORT

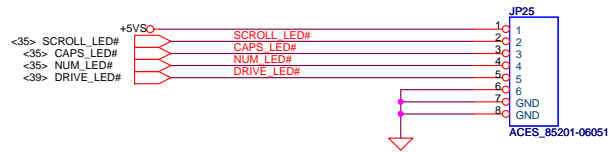
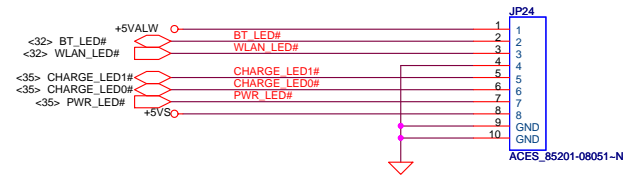
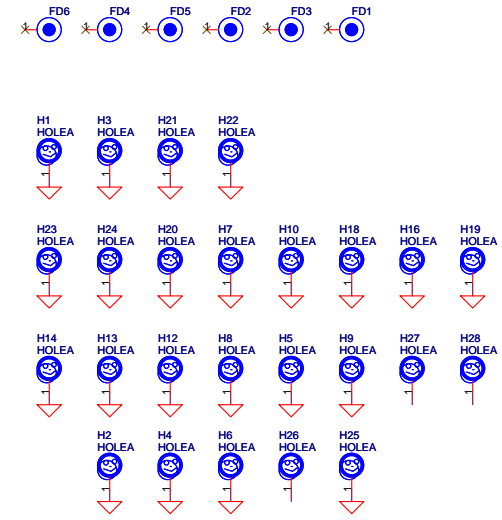
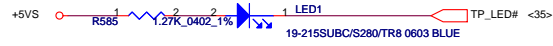


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Size	Document Number	Date		Rev	1.0
B	JJWA3/A4_LA4212P	Monday, May 12, 2008		Sheet	37 of 53

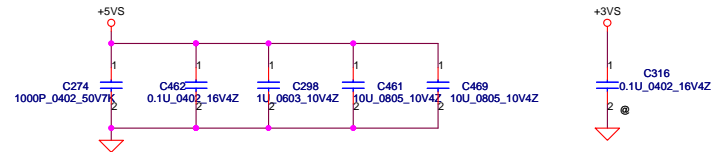
FOR EC 8M SPI ROM



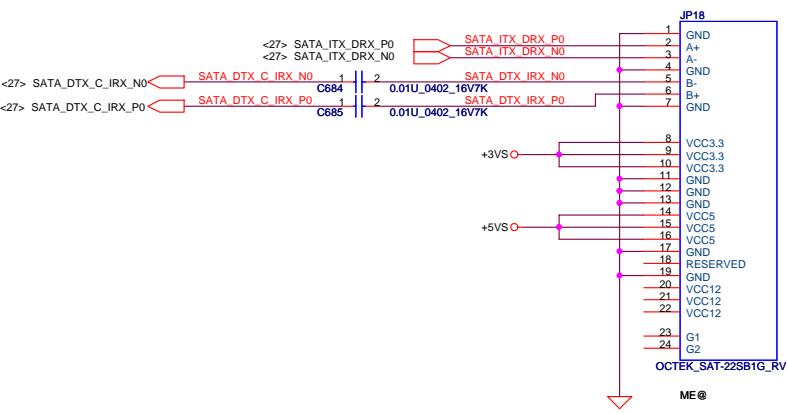
LED



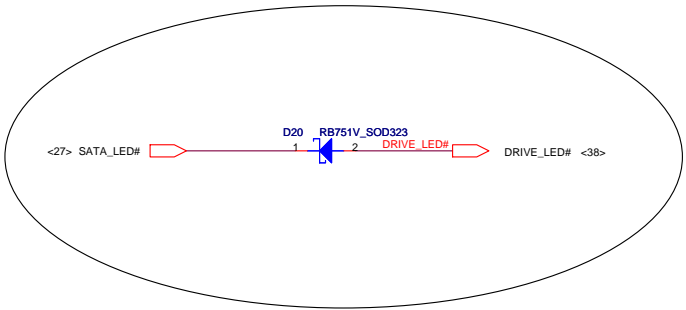
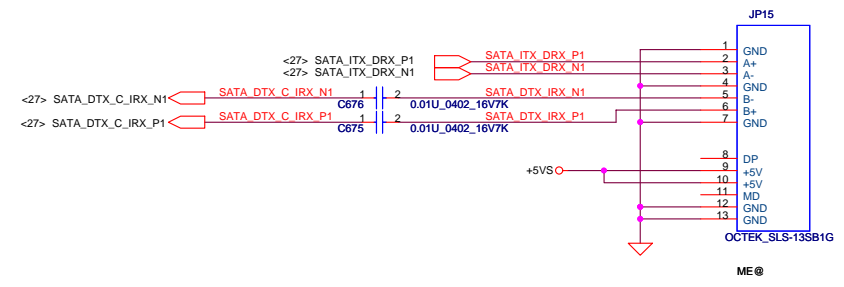
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Issued Date	2007/10/15	Deciphered Date	2008/10/15		
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				Date: Wednesday, May 14, 2008	Rev 1.0
				Sheet 38	of 53



SATA HDD Conn.

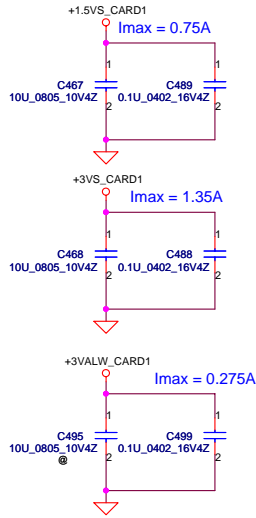
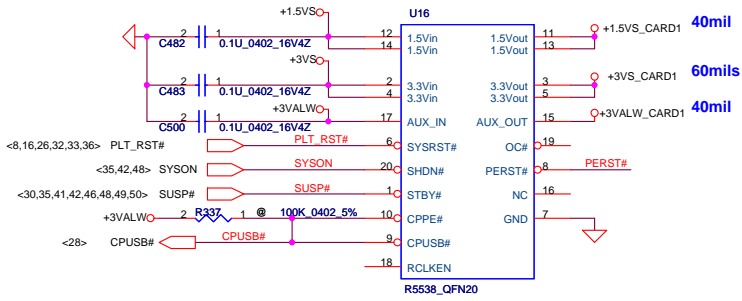


SATA ODD Conn.

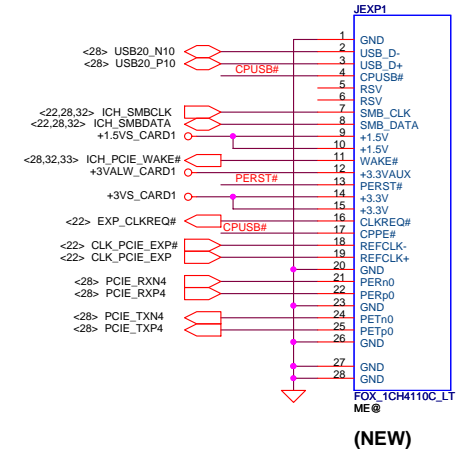


Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	HDD & ODD Connector		
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			Date:	Monday, May 12, 2008	Sheet 39 of 53

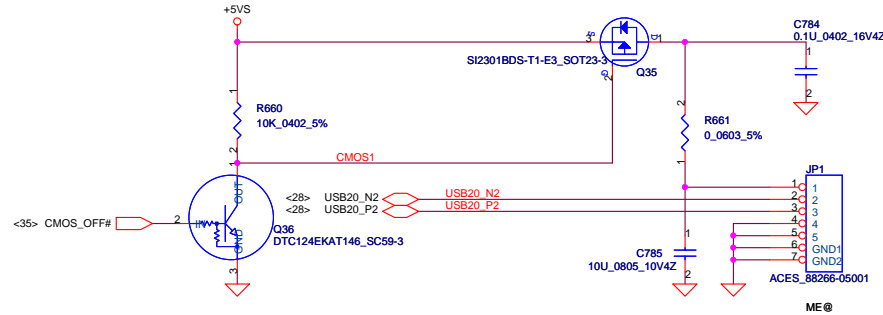
Express Card Power Switch



New Card Socket (Left/TOP)



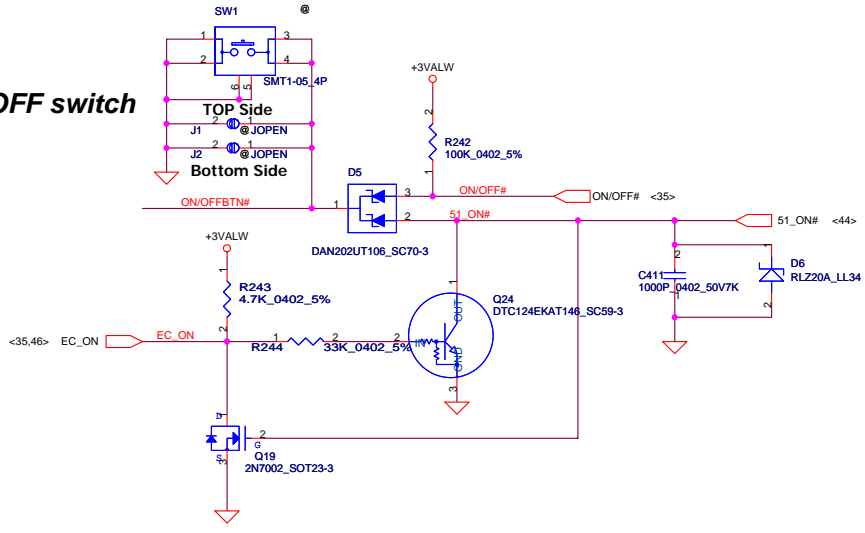
CMOS Camera Conn



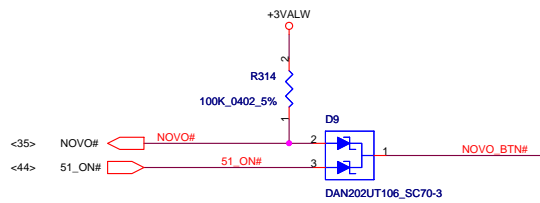
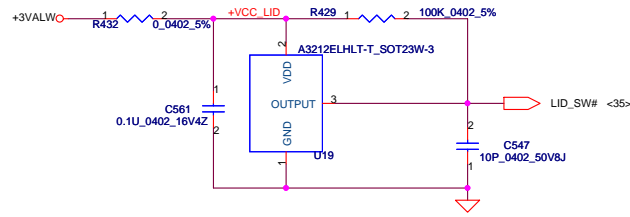
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc. NEW CARD & CMOS Connector	
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				JIWA3/A4_LA4212P Date: Monday, May 12, 2008	Rev 1.0 Sheet 40 of 53

Power Button

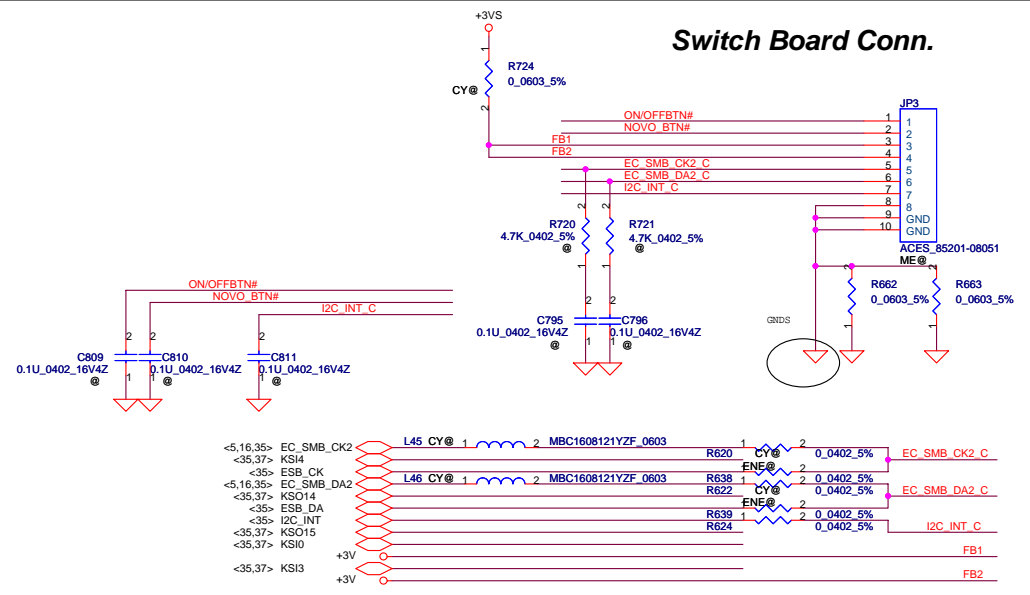
ON/OFF switch



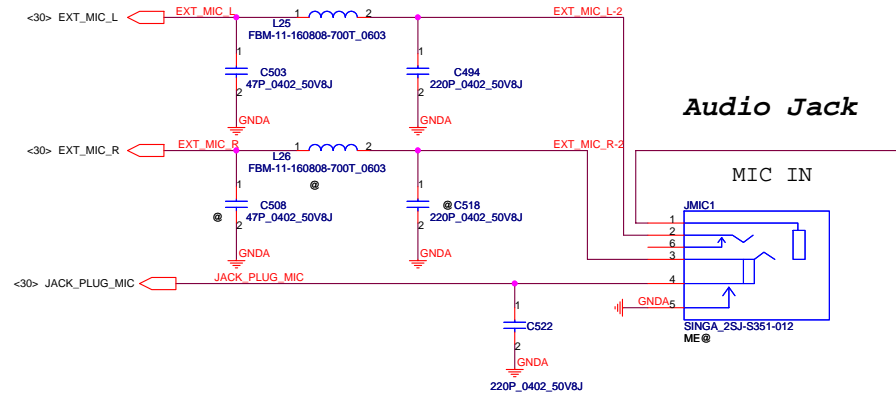
Lid Switch



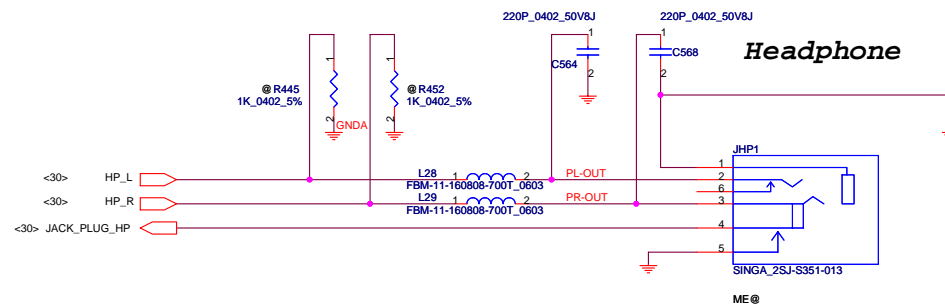
Switch Board Conn.



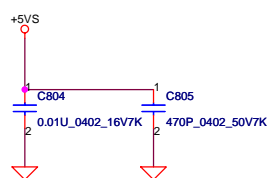
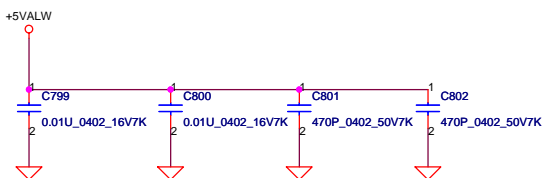
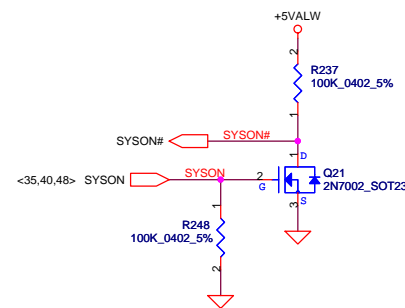
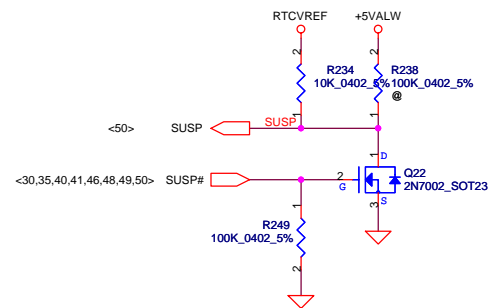
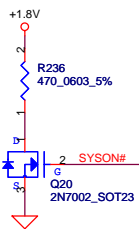
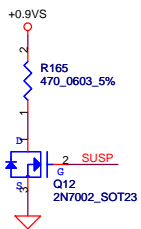
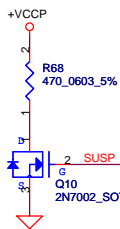
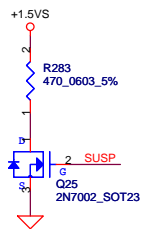
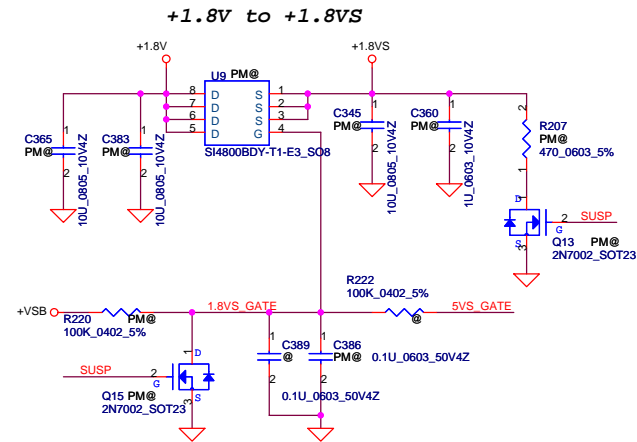
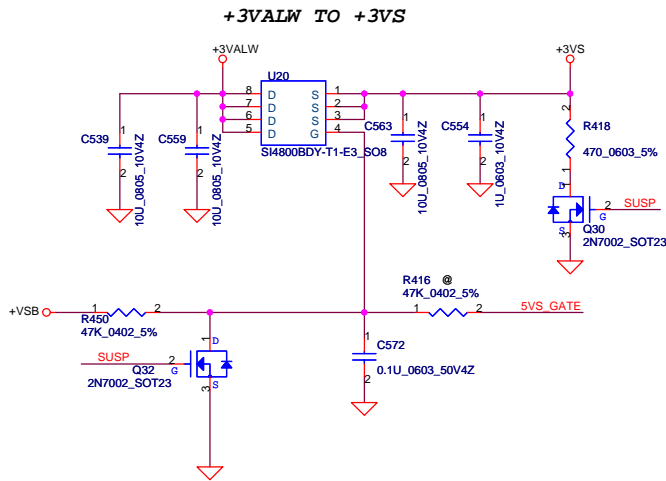
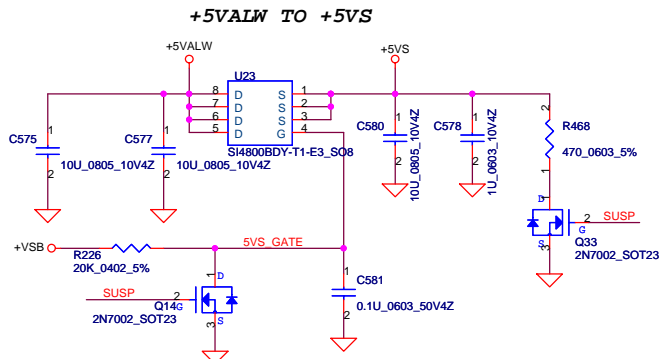
Audio Jack



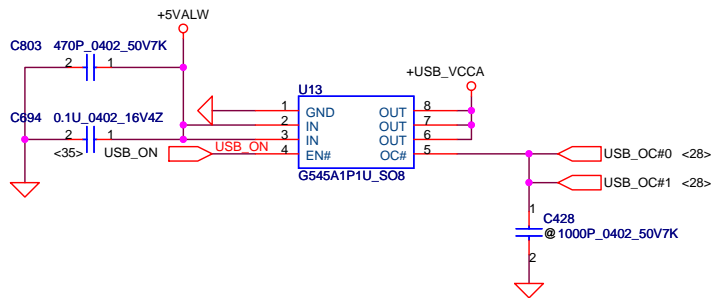
Headphone



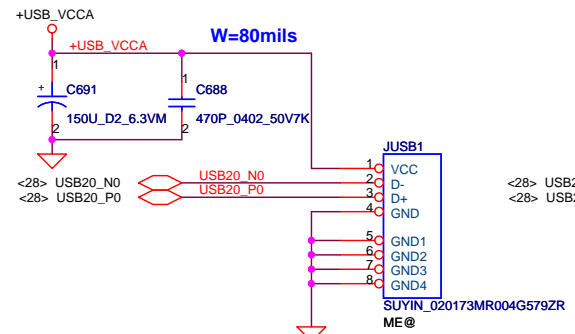
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				J1WA3/A4_LA4212P	
				Rev 1.0	
				Date: Monday, May 12, 2008	
				Sheet 41 of 53	



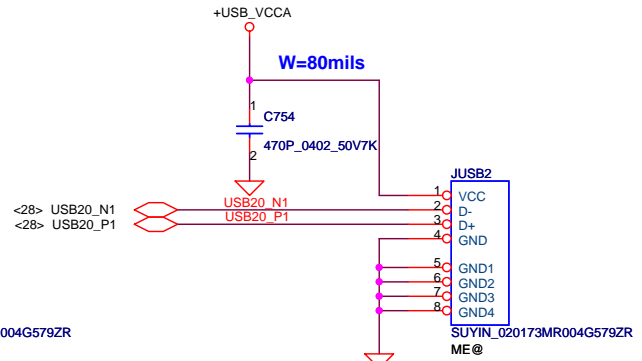
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Size	Document Number			Rev	1.0
Custom	J1WA3/A4_LA4212P			Date:	Monday, May 12, 2008
				Sheet	42 of 53



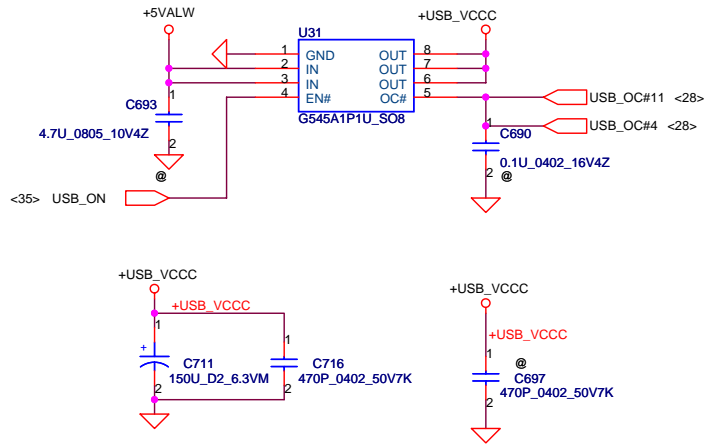
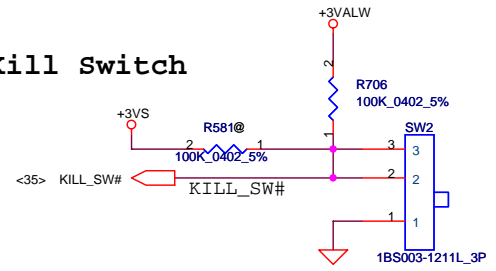
LIFT USB CONN. 1



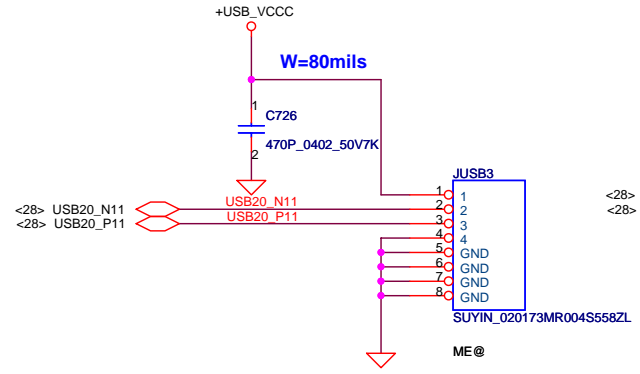
LIFT USB CONN. 2



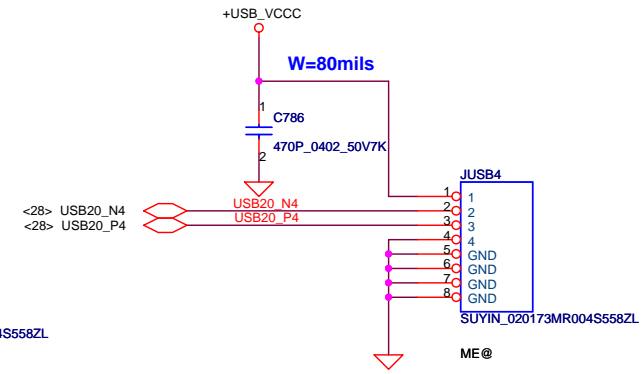
Kill Switch



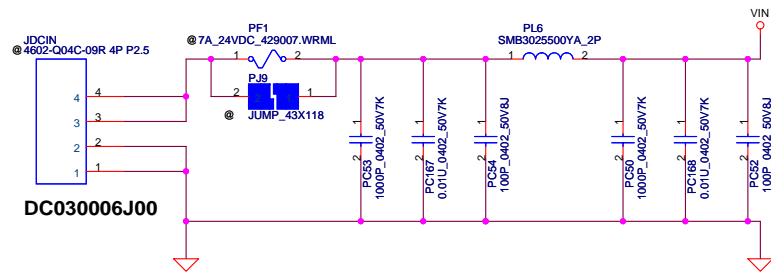
RIGHT USB CONN. 3



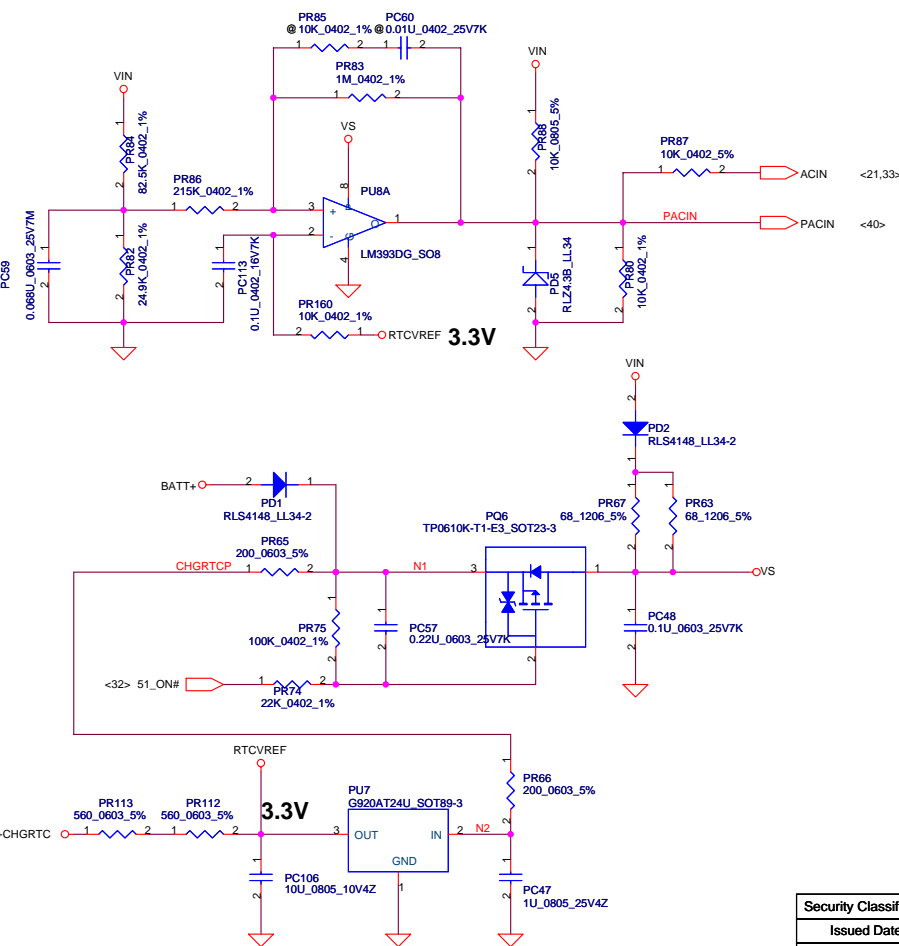
RIGHT USB CONN. 4



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Size	Document Number	Rev		Date	
Custom	JWA3/A4_LA4212P	1.0		Wednesday, May 14, 2008	
				Sheet 43 of 53	

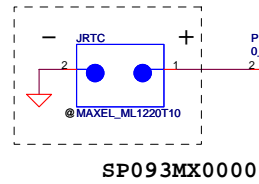
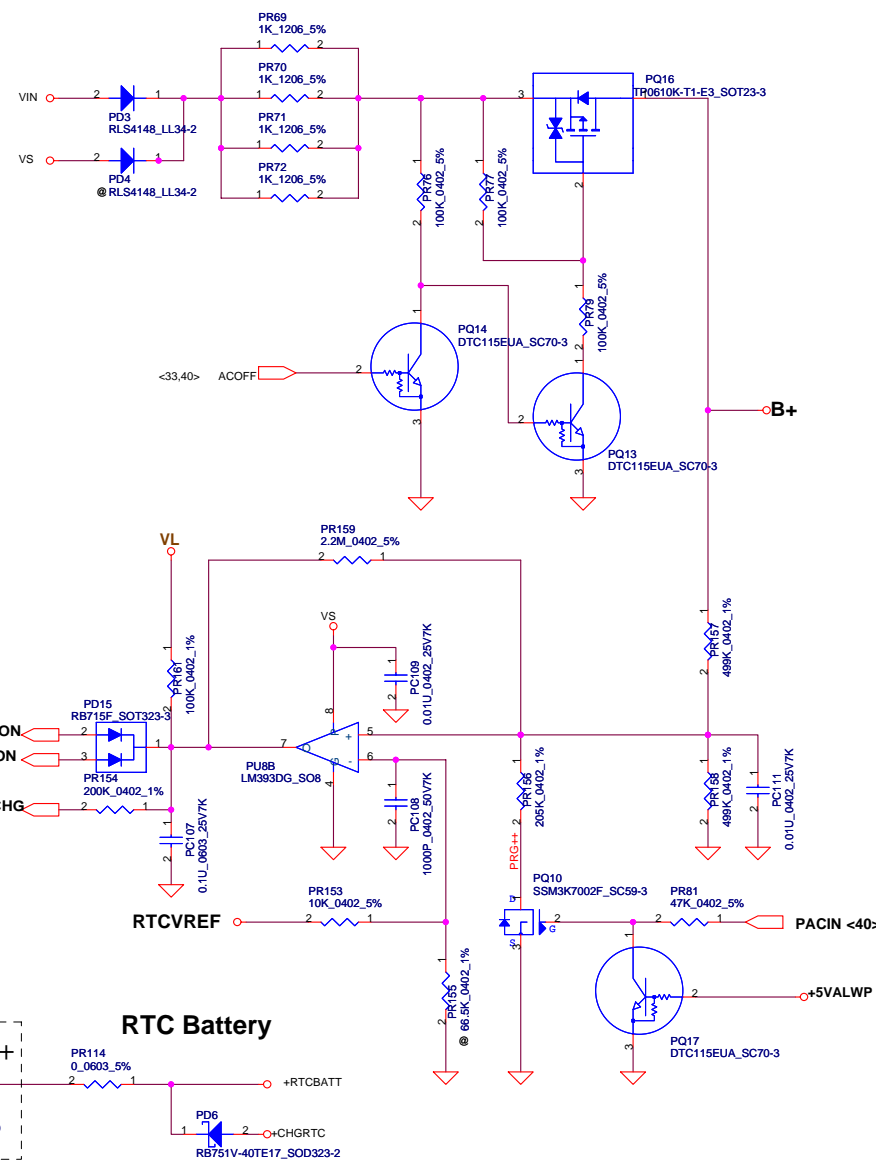


Vin Detector			
High	18.135	17.566	17.011
Low	14.866	14.355	14.063

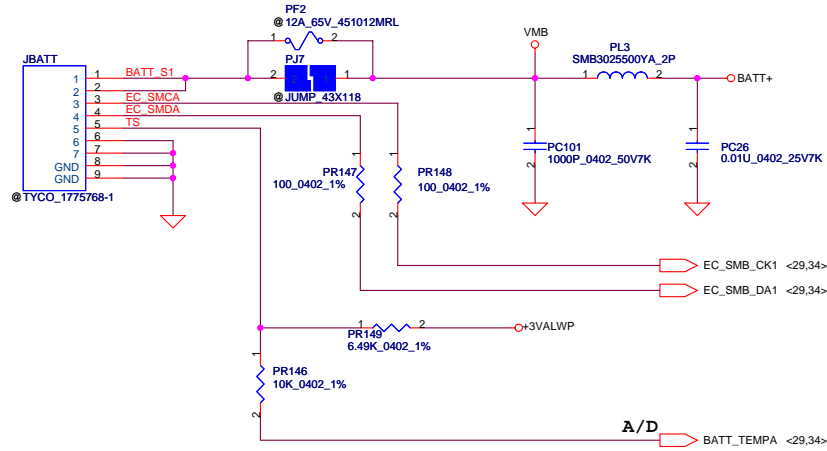


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	13.843V	14.247V	14.636V
L->H	14.936V	15.381V	15.814V

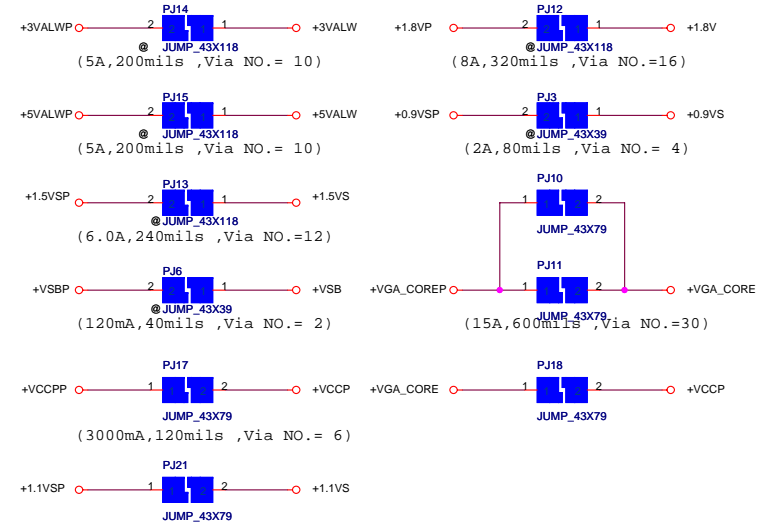
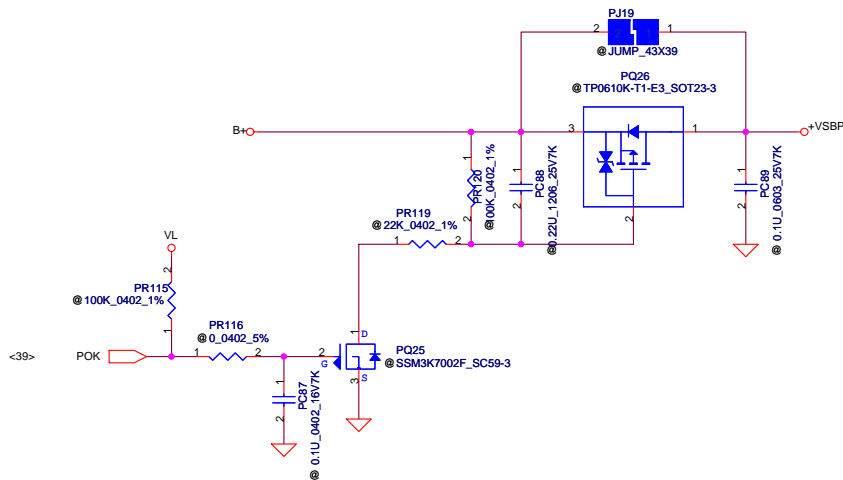
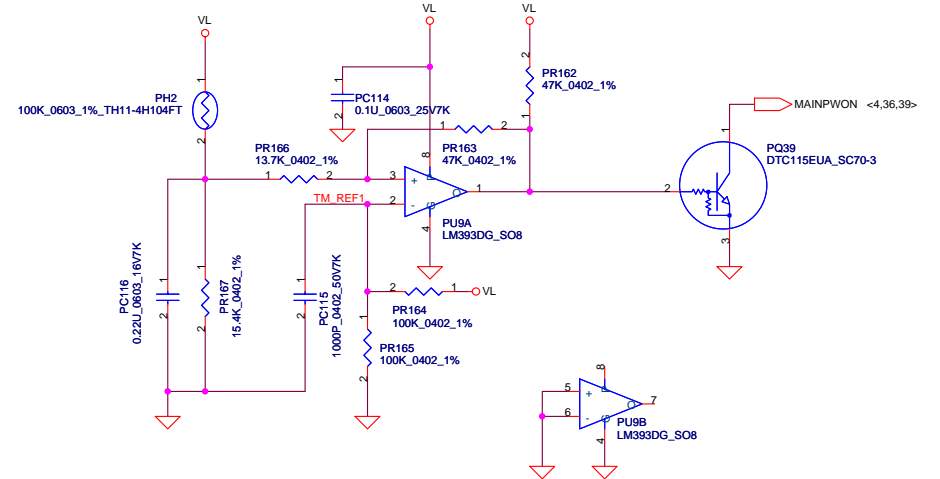
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



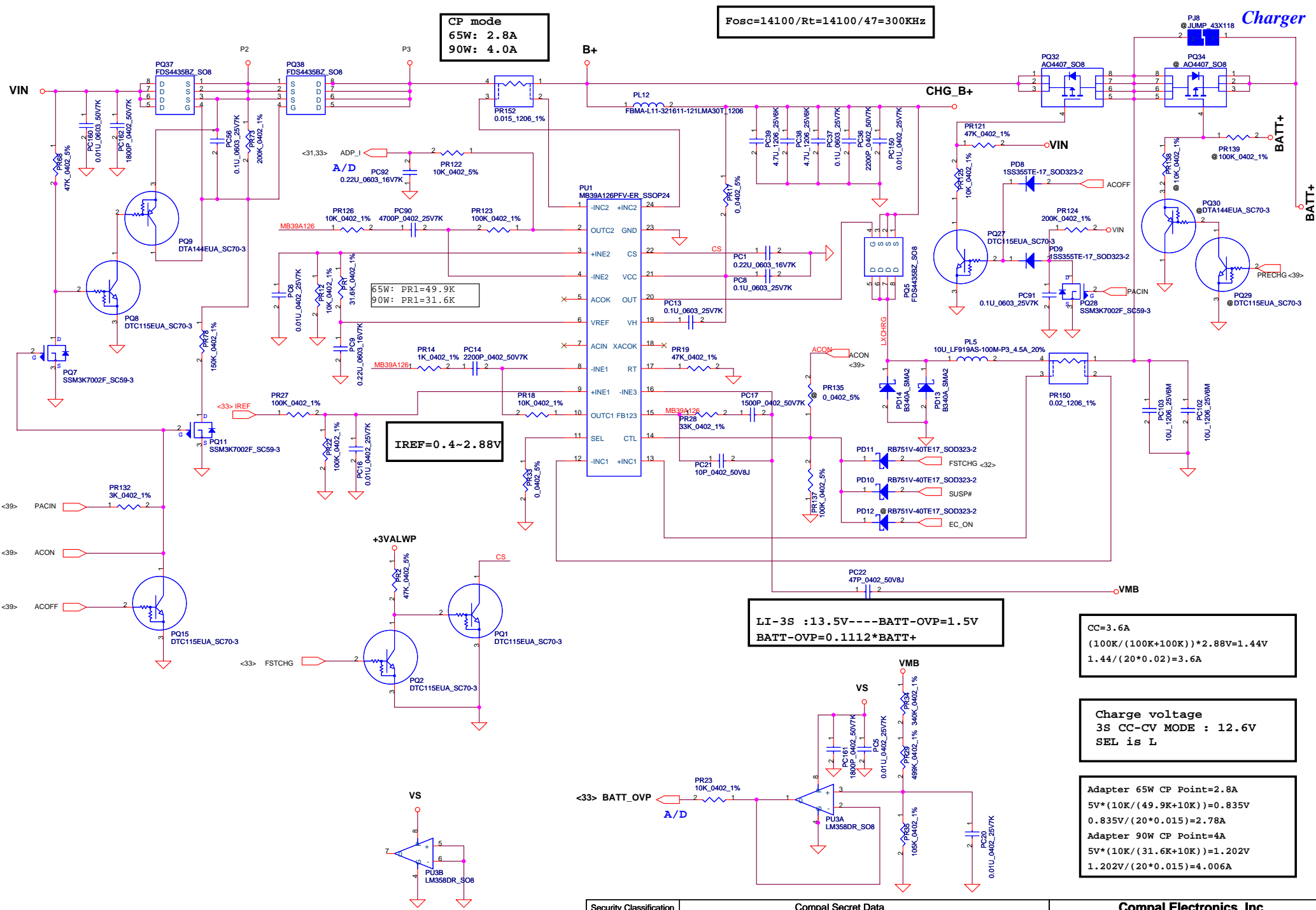
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Issued Date	2007/06/22	Deciphered Date	2008/06/22	Title
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Size	Document Number		Rev	1.0
Date:	Monday, May 12, 2008	Sheet	44	of 53



PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Size	Document Number				Rev 1.0
Date:	Monday, May 12, 2008	Sheet	45	of	53



CP mode
65W: 2.8A
90W: 4.0A

Fosc=14100/Rt=14100/47=300KHz

IREF=0.4~2.88V

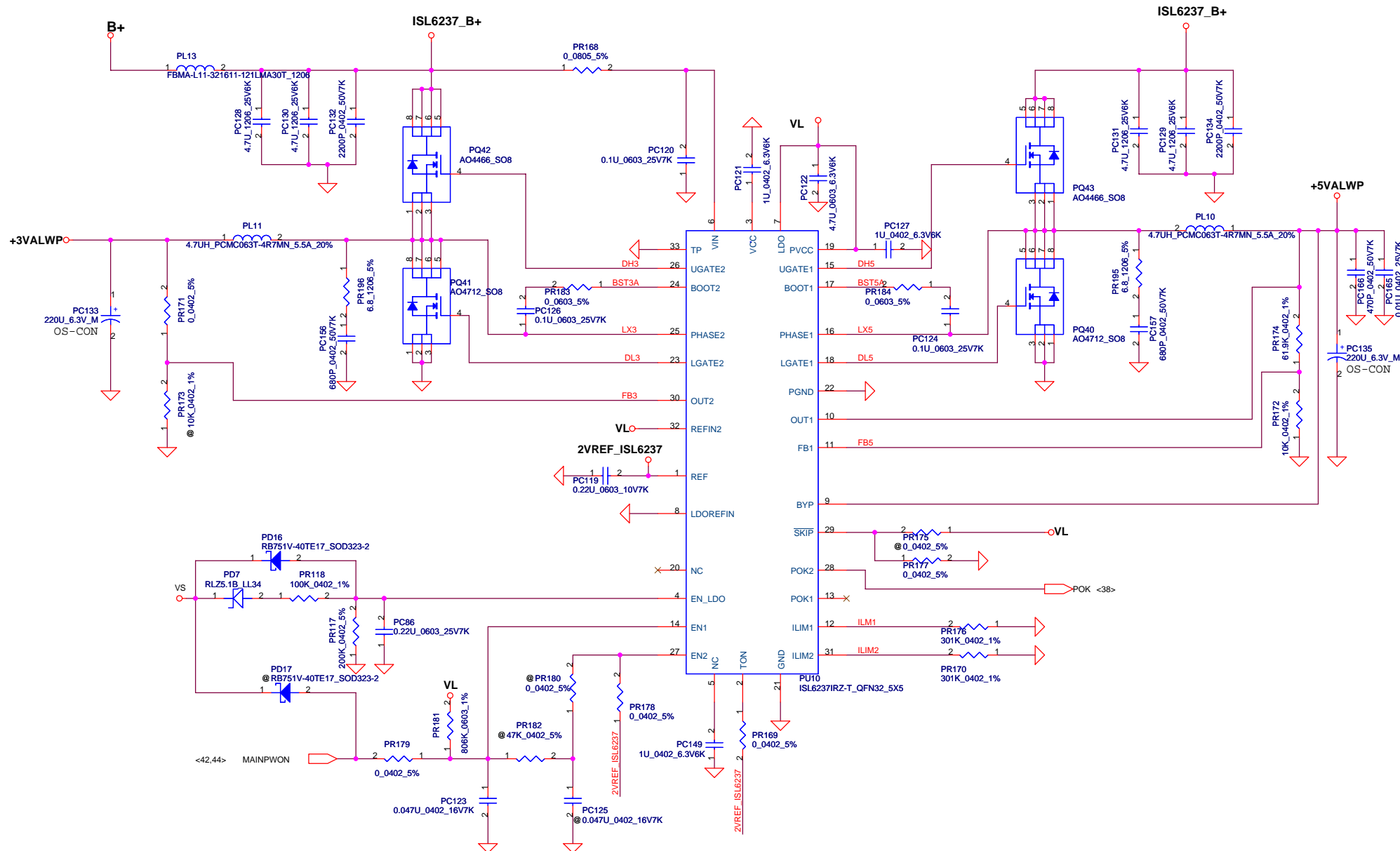
LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

CC=3.6A
 $(100K/(100K+100K))*2.88V=1.44V$
 $1.44V/(20*0.02)=3.6A$

Charge voltage
3S CC-CV MODE : 12.6V
SEL is L

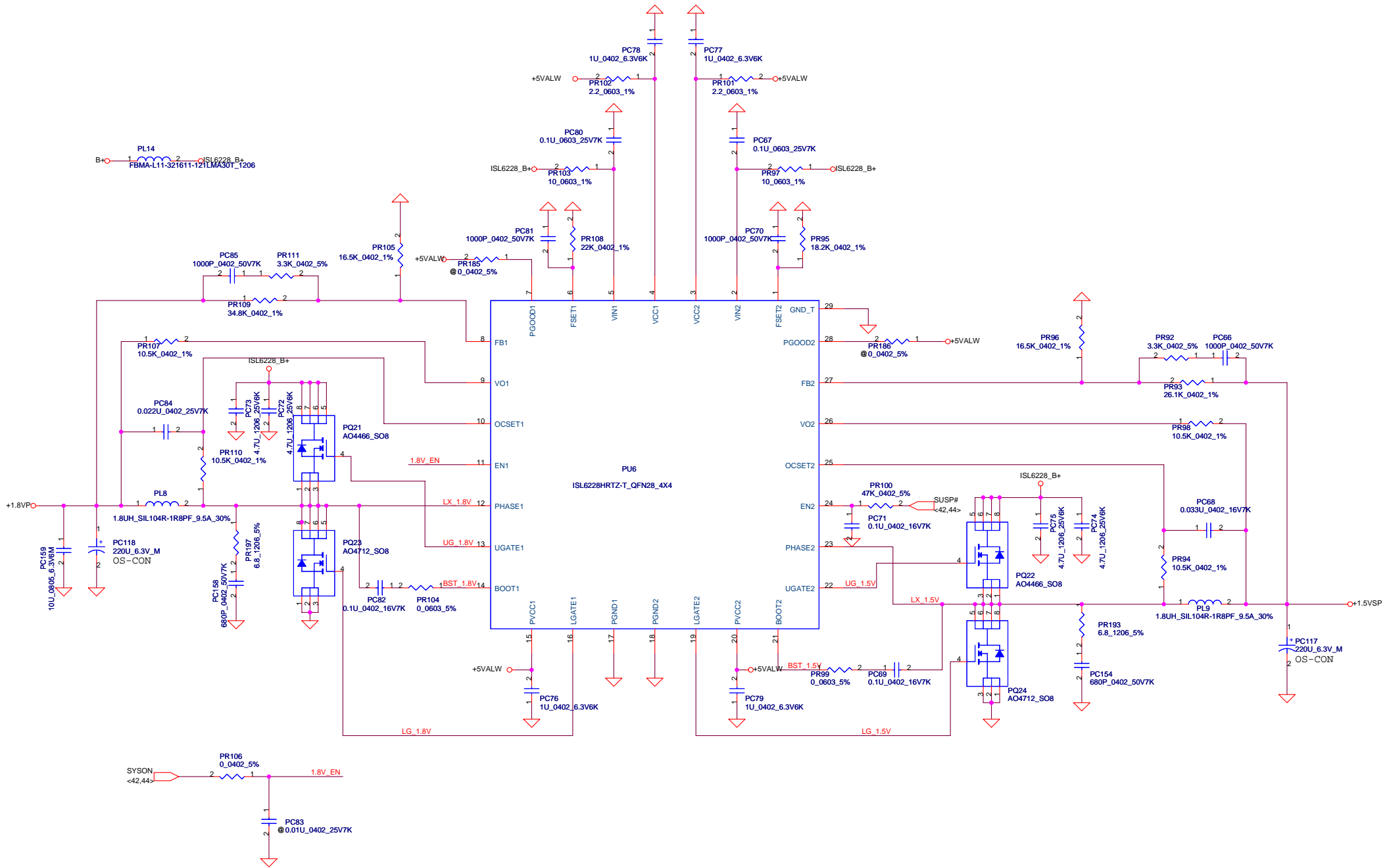
Adapter 65W CP Point=2.8A
 $5V*(10K/(49.9K+10K))=0.835V$
 $0.835V/(20*0.015)=2.78A$
Adapter 90W CP Point=4A
 $5V*(10K/(31.6K+10K))=1.202V$
 $1.202V/(20*0.015)=4.006A$

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Date:	Monday, May 12, 2008	Sheet	46	of 53							

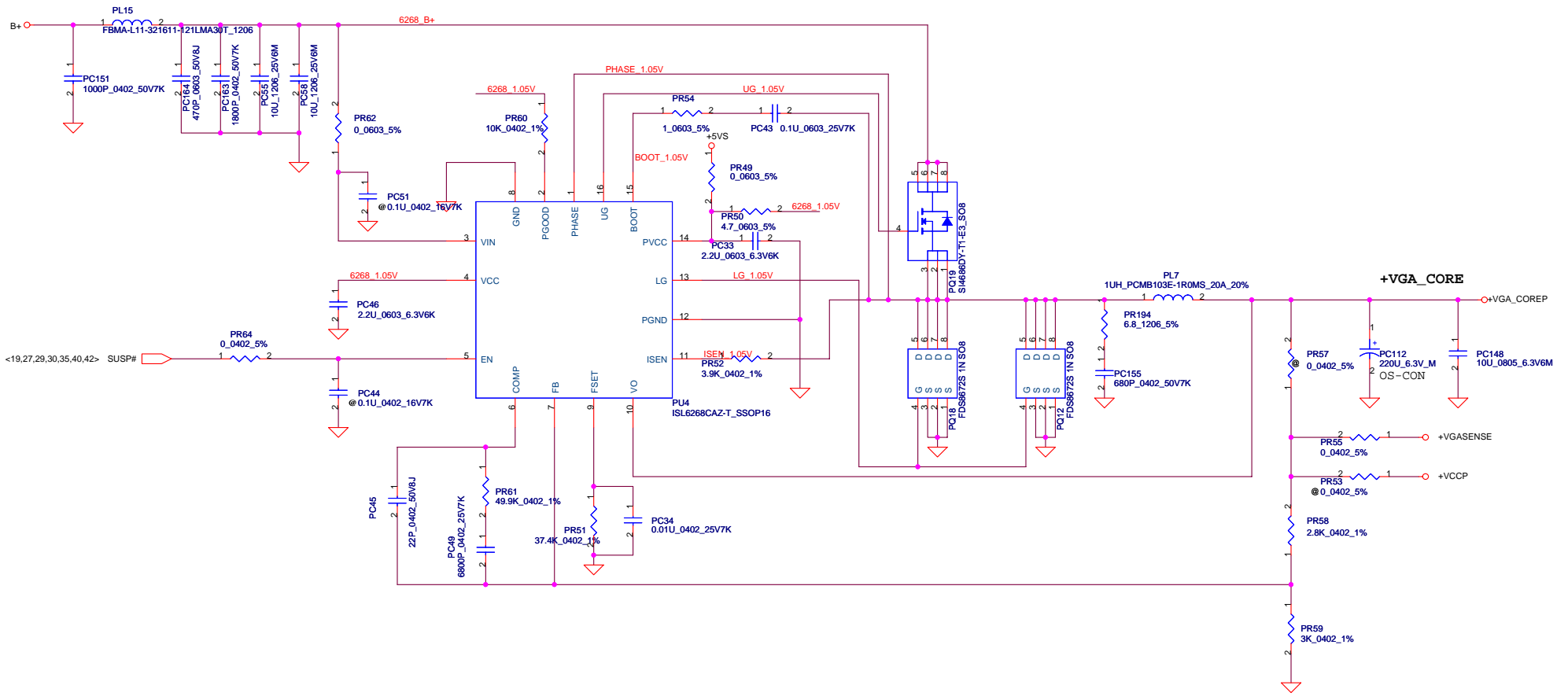


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Size	Document Number	Date		Rev	1.0
Custom		Monday, May 12, 2008		Sheet	47 of 53

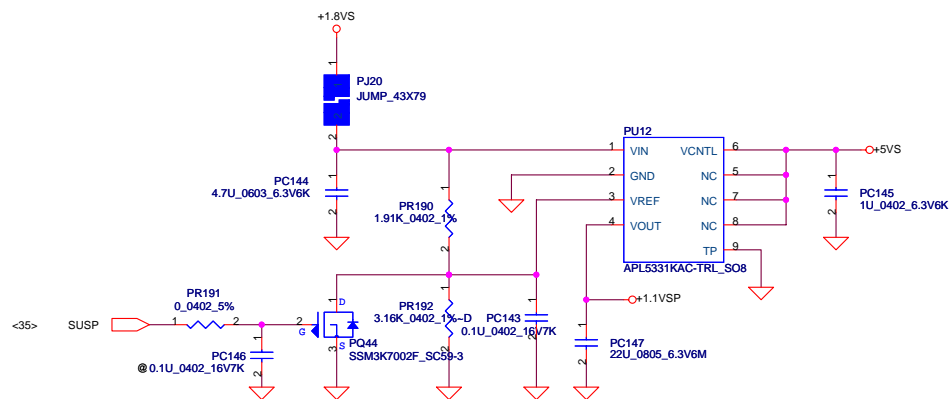
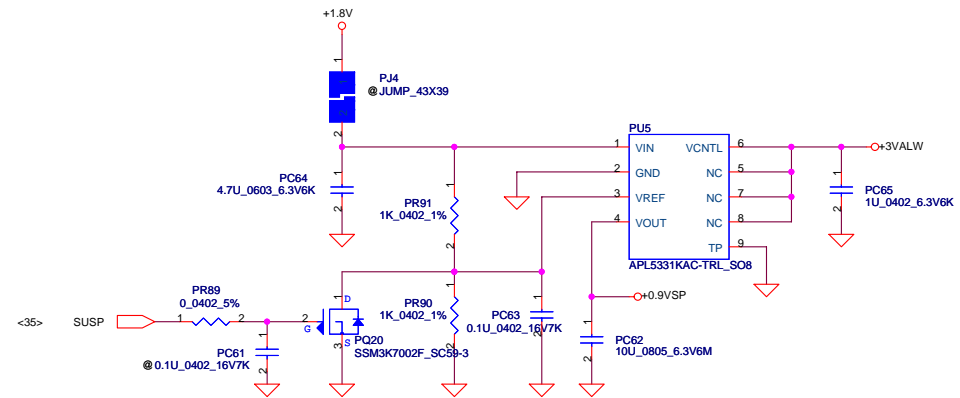
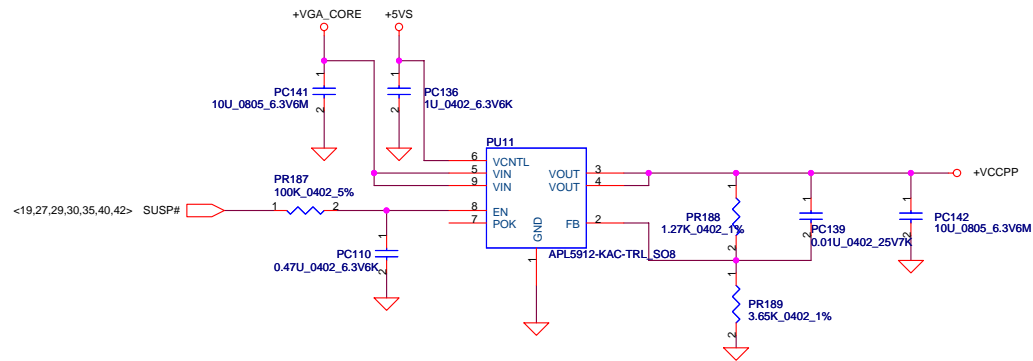
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Date:	Monday, May 12, 2008	Sheet	48	of	53



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Size	Document Number			Rev	1.0
Date: Monday, May 12, 2008		Sheet 49 of 53			



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				VCCP/0.9V/1.1V	
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				Date: Monday, May 12, 2008	Rev 1.0
				Sheet 50	of 53

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

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				Document Number	
Date: Monday, May 12, 2008				Sheet 51 of 51	
				Power PIR	
				J1WA3/A4 LA4212P	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/10	P29	C615 change to R615 and BOM Structure change to PM@	Fix DIS Audio issue
2	12/10	P20, P21	R104 & R154 BOM Structure change to PM@	Reduce cost
3	12/10	P16	R86, R645, R646, R650, R651, R652 & R653 BOM Structure change to PM@	Reduce cost
4	12/10	P29	R614 change from 10K to 45.3ohm R615 change from 12K to 54.9ohm	Fix UMA Audio issue
5	12/10	P08	R79 change from 33 to 10ohm R80, R81, R82 & R85 change from 0 to 22 ohm	Fix UMA Audio issue
6	12/10	P30	The C783 links to GND	Fix Internal MIC issue
7	12/10	P41	Add L45 & L46 MBCL608121Y2F Bead	Fix F/B issue
8	01/02	P11	Change C126 package	
9	01/02	P28	Add R707 to connect VGATE to M_PWROK	Modify power sequence
10	01/02	P16	Add R699 to connect +VGASENSE	
11	01/02	P16	Remove U3.P1	
12	01/02	P19	Add R700 to connect GND	
13	01/02	P11	Add C707	for +VCC_DMI
14	01/02	P16	Add C788	for nvidia request for +PEX_PLLVDD
15	02/27	P08	change R147 from 511 ohm 1% to 499 ohm 1%	
16	02/27	P23	change D4 location	
17	02/27	P23	Add D25 , D26 for ESD	
18	02/27	P25	Add D27 , D28 & D29 for ESD	
19	02/27	P29	Add R713 connect to 1.5V	
20	02/27	P31	change C550 , C570 , C506 & C507 to 0.1uF 0603	Fix pop noise issue
21	05/08	P05	Add R726 1k ohm & C808 0.1uF to fix issue.	
22	05/08	P16	Remove R48 for EMI request.	
23	05/08	P27	Change R554 from 0 ohm to 33 ohm for EMI request.	
24	05/08	P28	Add R566 10 ohm & C733 10pF for EMI request.	
25	05/08	P30	Add R327 47 ohm & C458 33pF for EMI request.	
26	05/08	P35	Change C501 & C514 from 15pF to 12pF	
27	05/08	P37	Add D31 (PJDLCO5_SOT23-3) for ESD request.	
28	05/08	P41	Add C494, C522, C564 & C568 220pF for EMI request	

Title			<Title>
Size	Document Number	Rev	
Custm	JWAS3A4_LA4212P	1.0	
Date:	Monday, May 12, 2008	Sheet	53 of 53