

# ROME-1 PLANAR SIT (M9/KINNERETH-R BASE)

VER 0.73 OCT/25/2002

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DESIGNER	T.O	10/25/02	PART NO.	
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CLASS			TITLE	PAGE
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# EC HISTORY

DATE	10/25/02	VER 0.73	PART NO.	
DEVELOPMENT NO.			Q/M	2 / 82

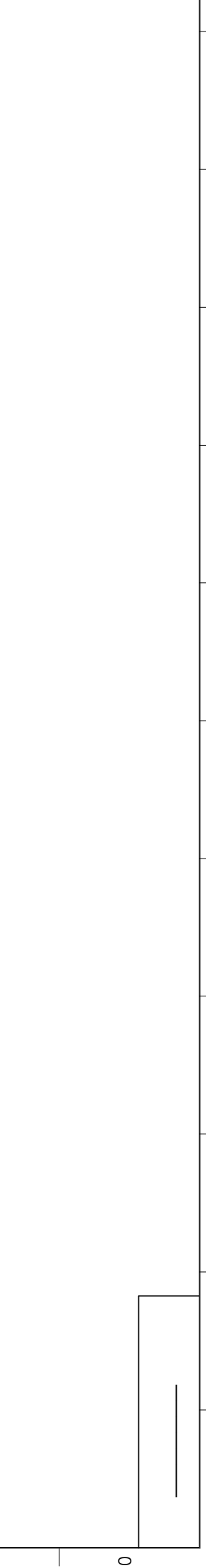
SIV	VER. 0.37	07/16/2002	APPLY RM_EC_SIV01
VER. 0.38	07/17/2002	CHANGE BAY/HDD/AUDIO CONN	
VER. 0.39	07/18/2002	APPLY RM_EC_SIV02	
VER. 0.40	07/22/2002	APPLY RM_EC_SIV03	
VER. 0.41	07/23/2002	CHANGE USB/COMBO/S-VIDEO/DOCK CONN	
VER. 0.42	07/24/2002	APPLY RM_EC_SIV04	
VER. 0.43	07/25/2002	APPLY RM_EC_SIV05	
VER. 0.44	07/25/2002	APPLY RM_EC_SIV06	
VER. 0.45	07/26/2002	APPLY RM_EC_SIV07	
VER. 0.46	07/29/2002	CHANGE AUDIO	
VER. 0.47	07/31/2002	APPLY RM_EC_SIV08	
VER. 0.48	08/01/2002	APPLY RM_EC_SIV09	
VER. 0.49	08/02/2002	APPLY RM_EC_SIV10	
VER. 0.50	08/05/2002	APPLY RM_EC_SIV11	
VER. 0.51	08/07/2002	APPLY RM_EC_SIV12	
VER. 0.52	08/09/2002	APPLY RM_EC_SIV13	
VER. 0.53	08/12/2002	APPLY RM_EC_SIV14	
VER. 0.54	08/13/2002	APPLY RM_EC_SIV15	

SIV DATA RELEASE	VER. 0.55	08/21/2002	APPLY RM_EC_SIV16 (G-SENSOR)
VER. 0.56	08/29/2002	APPLY RM_EC_SIV17/18(VBL16/CHARGER/TSURUMAI)	
VER. 0.57	09/02/2002	APPLY RM_EC_SIV19(PMH4)	

SIT	VER. 0.58	09/18/2002	APPLY RM_EC_SIT01
VER. 0.59	09/24/2002	APPLY RM_EC_SIT02	
VER. 0.60	09/27/2002	APPLY RM_EC_SIT03/04	
VER. 0.61	09/30/2002	APPLY RM_EC_SIT05	
VER. 0.62	10/01/2002	APPLY RM_EC_SIT06	
VER. 0.63	10/02/2002	APPLY RM_EC_SIT07	
VER. 0.64	10/03/2002	APPLY RM_EC_SIT08	
VER. 0.65	10/04/2002	APPLY RM_EC_SIT09	
VER. 0.66	10/08/2002	APPLY RM_EC_SIT10 (W/O L9/L19 CHANGE)	
VER. 0.67	10/09/2002	APPLY RM_EC_SIT11	
VER. 0.68	10/11/2002	APPLY RM_EC_SIT12	
VER. 0.69	10/15/2002	APPLY RM_EC_SIT13	
VER. 0.70	10/16/2002	APPLY RM_EC_SIT14	
VER. 0.71	10/16/2002	APPLY RM_EC_SIT15	

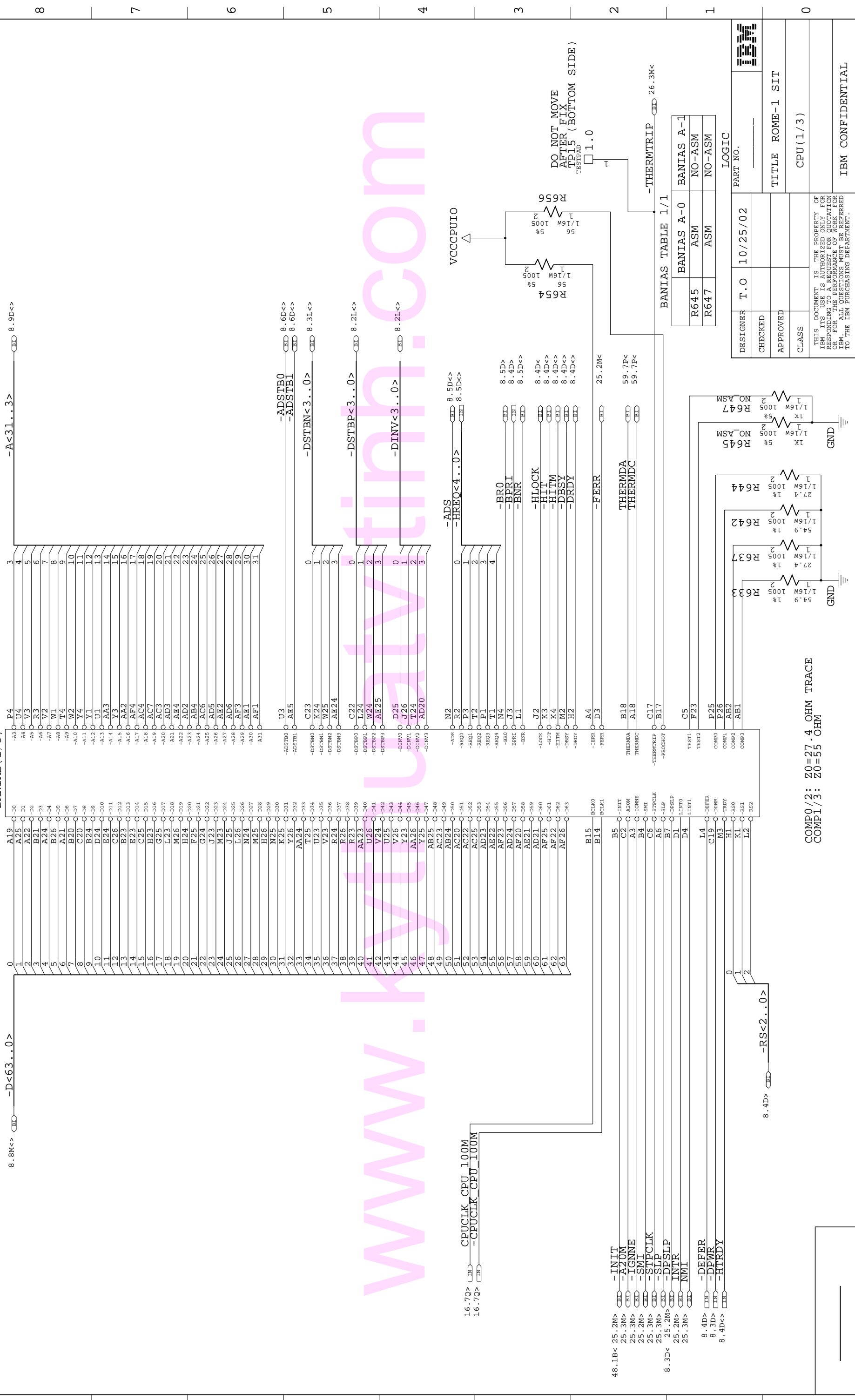
SIT DATA RELEASE (10/17/2002)	VER. 0.72	10/22/2002	APPLY RM_EC_SIT16
VER. 0.73	10/25/2002	APPLY RM_EC_SIT17	

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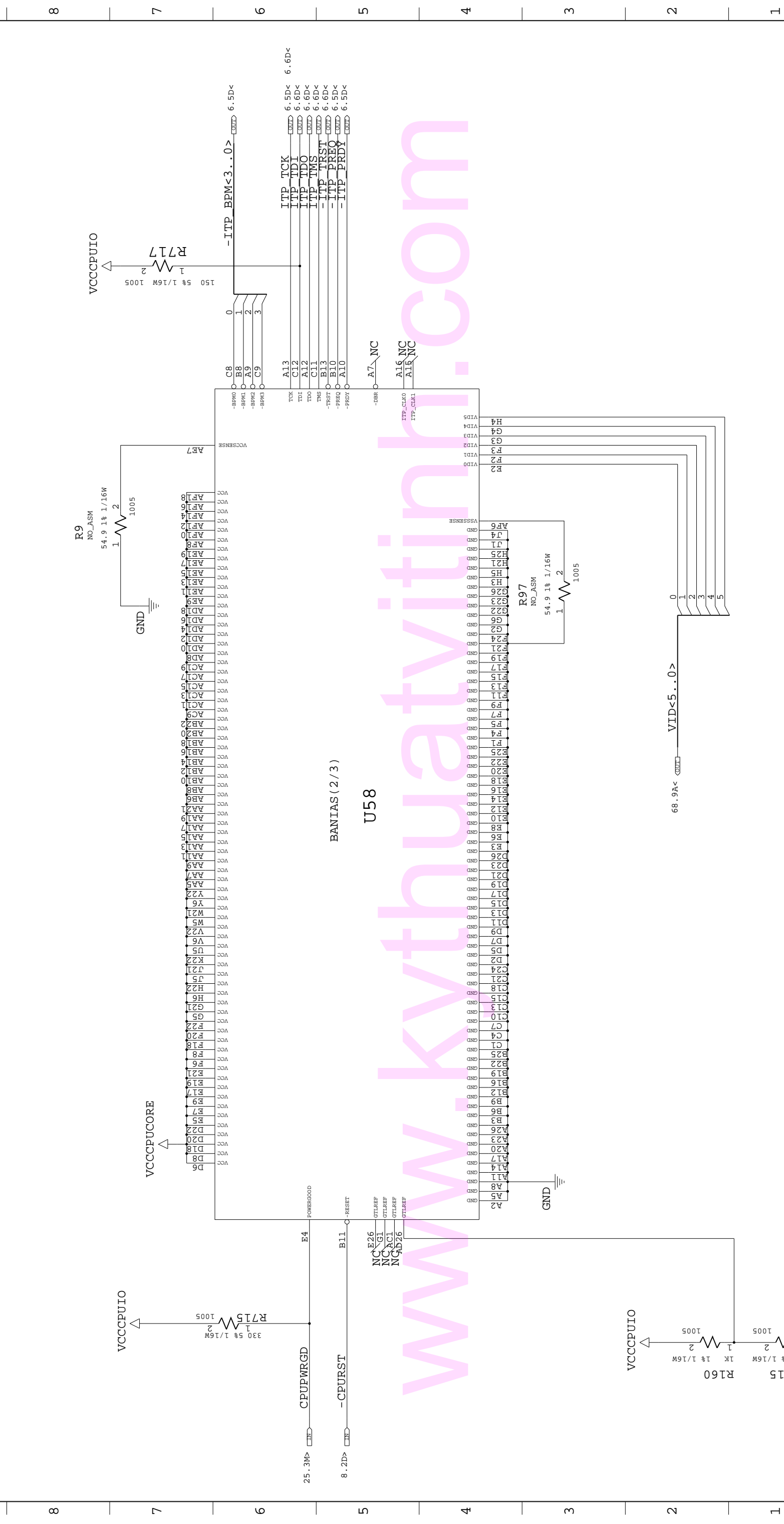
U58

BANIAS(1/3)



COMP0/2: Z0=27.4 OHM TRACE  
COMP1/3: Z0=55 OHM

DATE	EC NO.	PART NO.
10/25/02	VER 0.73	
DEVELOPMENT NO. 4 / 82		
		Q/M



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TITLE	ROME-1 SIT		
CLASS	CPU(2/3)		
IBM CONFIDENTIAL			

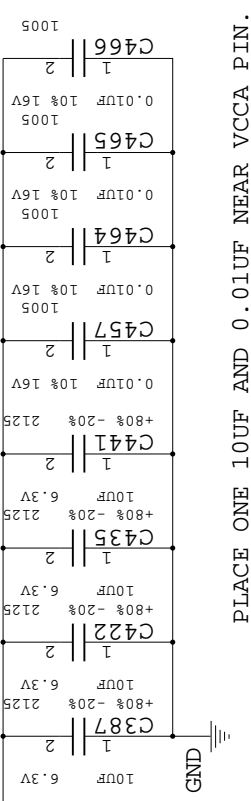
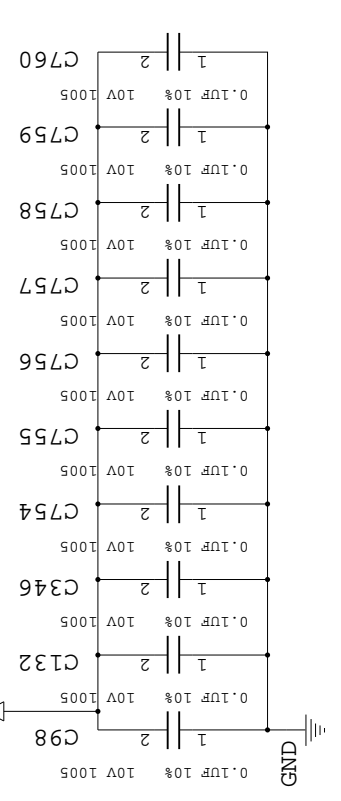
www.kvthwatvitihr.com

BANIAS (2 / 3)

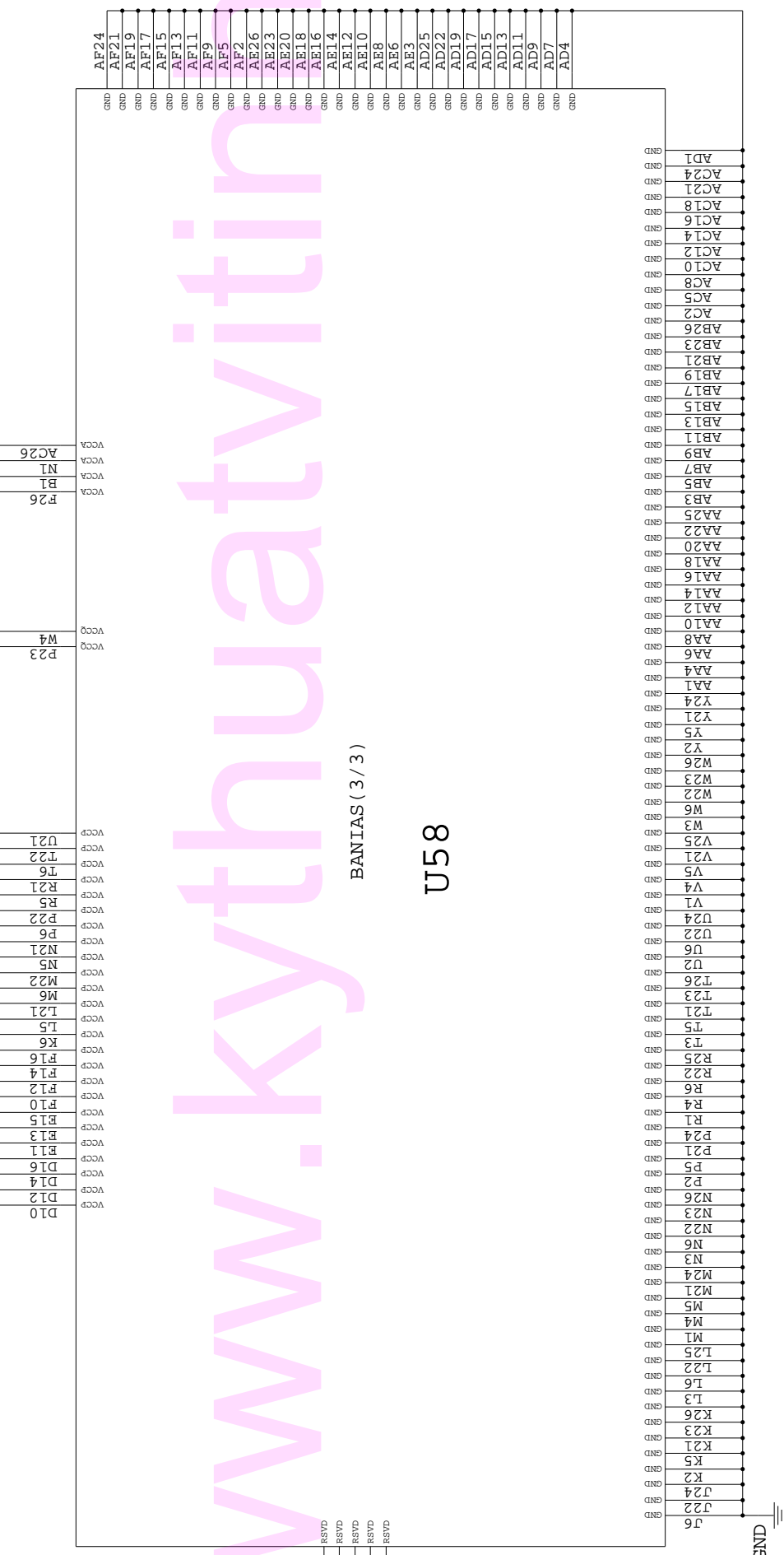
U58

PLACE < 0.5 INCHES FROM BANIAS

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q
DATE												PART NO.		
10/25/02												VER 0.73		
DEVELOPMENT NO.												Q/M		
												5 / 82		



PLACE ONE 10UF AND 0.01UF NEAR VCCA PIN.



BANTAS (3/3)

U58

www.kythatvitin.com

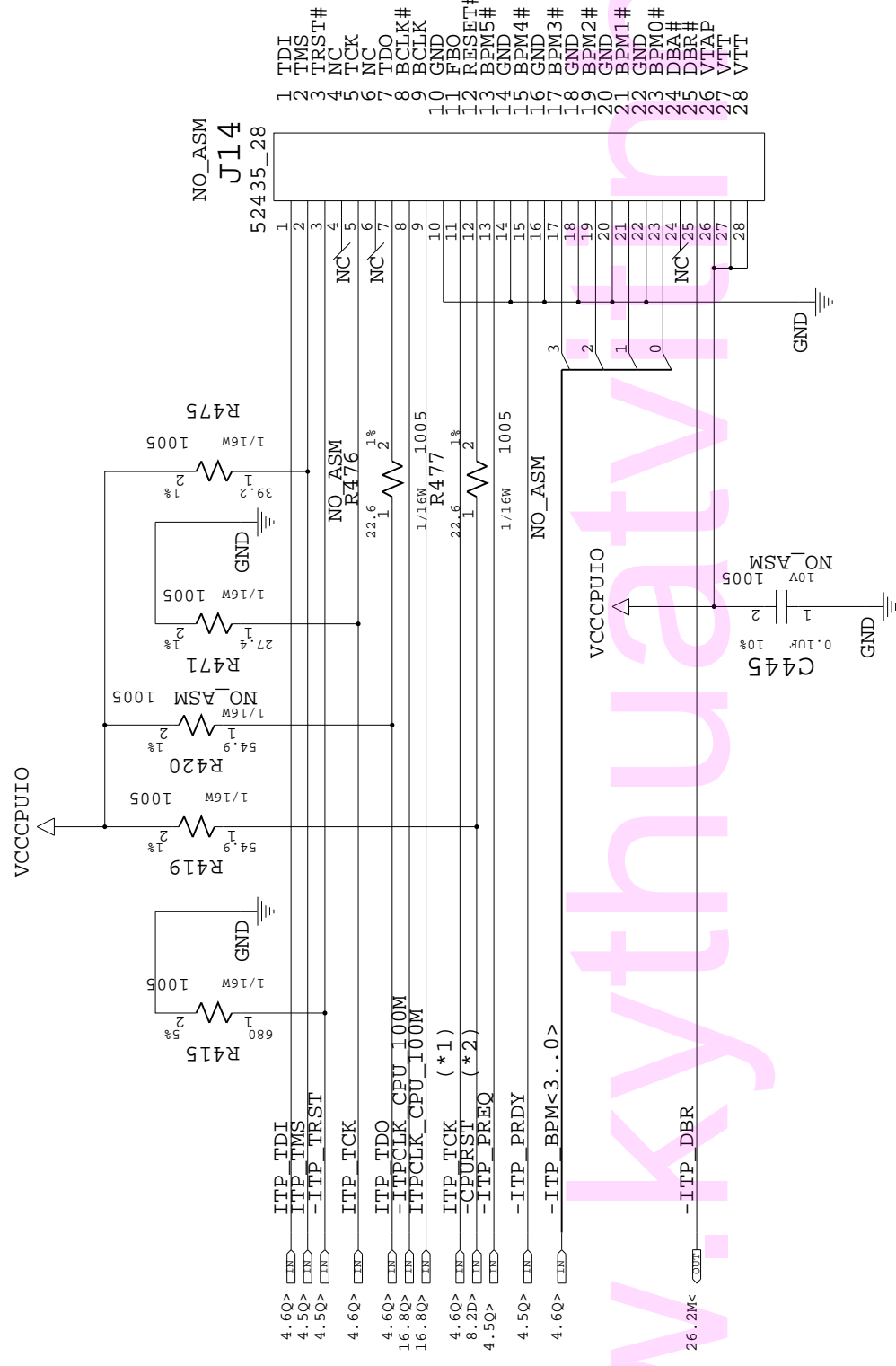
DO NOT MOVE  
AFTER FIX  
TP16  
TESTPAD  
□ 1.0 (BOTTOM SIDE)

-PSI 68.9A<

DESIGNER	T.O	10/25/02	PART NO.	
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CLASS			CLASS	CPU (3/3)
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A B C D E F G H J K L M N P Q

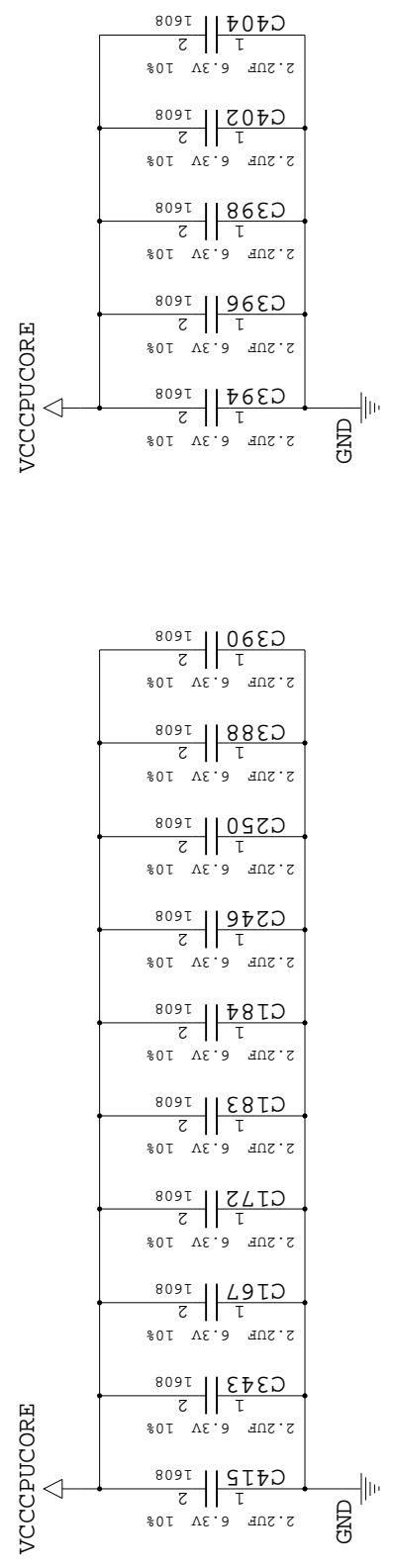
M	N	P	Q
DATE	EC NO.	PART NO.	
10/25/02	VER 0.73		
		DEVELOPMENT NO.	Q/M
			6 / 82



(\*1) TCK SIGNAL IS BRANCHED AT BANIAS PIN  
 (\*2) -CPURST SIGNAL IS BRANCHED AT ODEM PIN

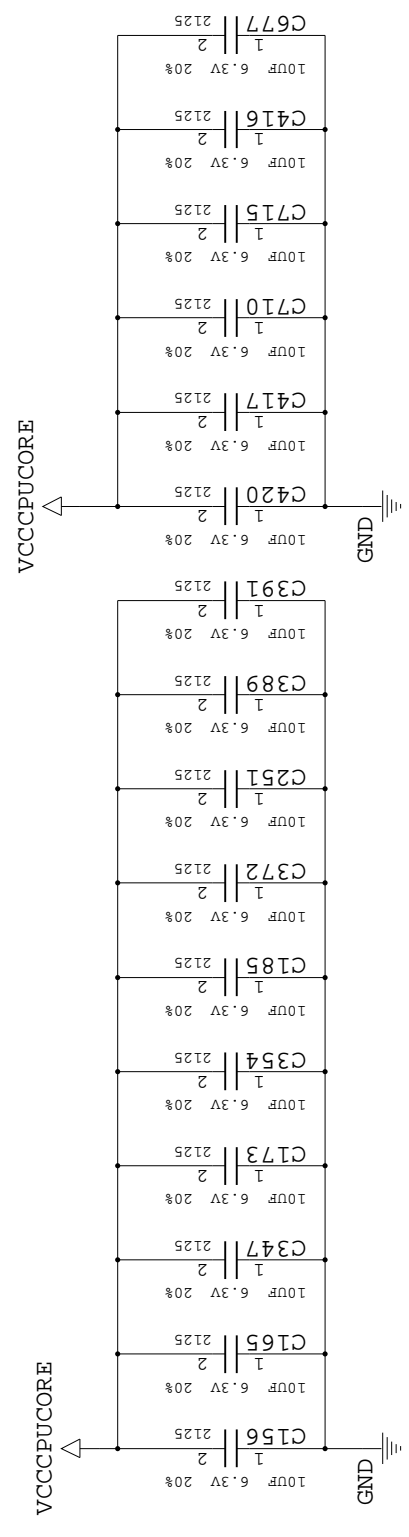
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													DEVELOPMENT NO.	Q/M 7 / 82



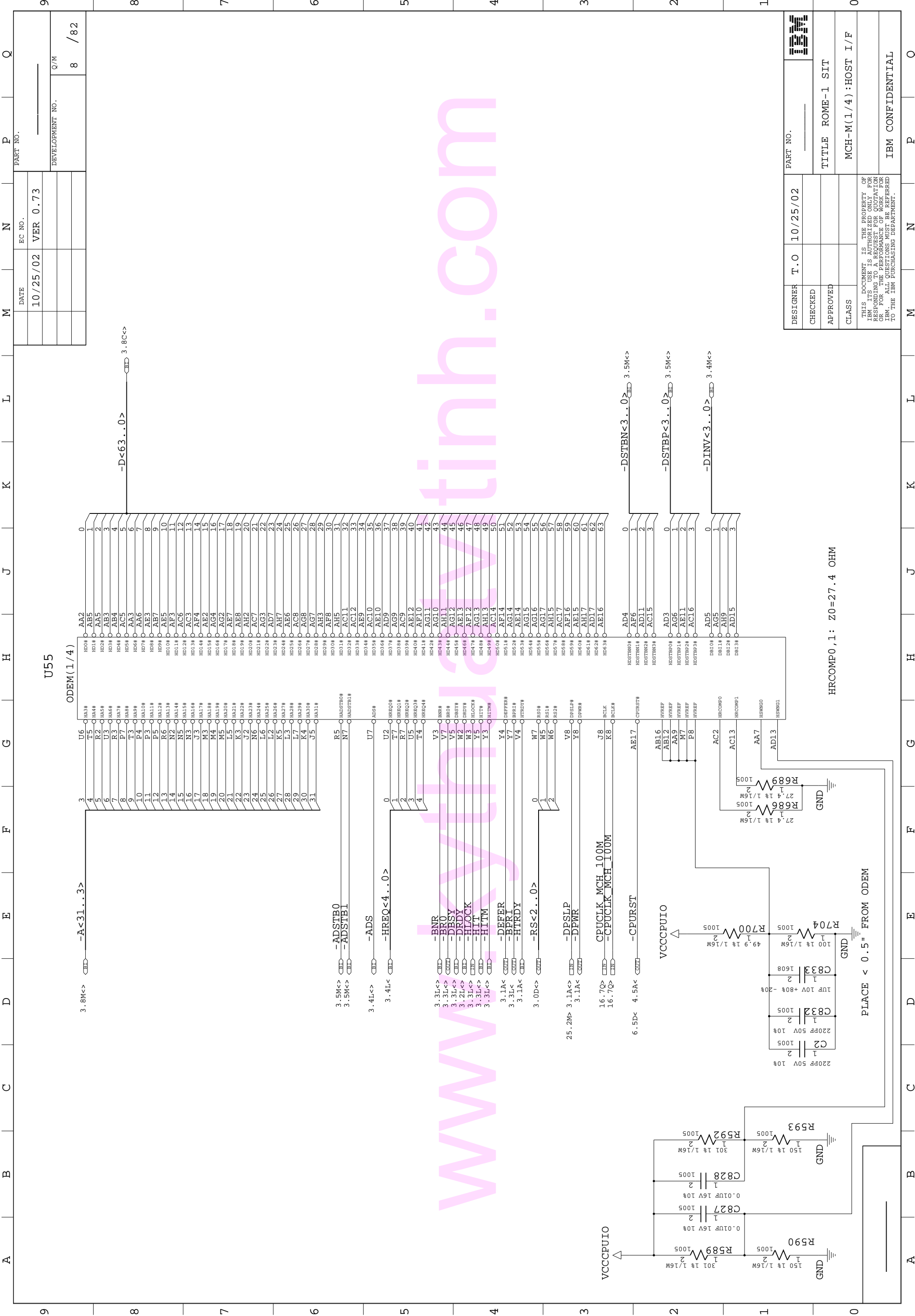
2.2UF X5R 1608 1/16W X15PCS

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10UF X5R 2125 1/16W X16PCS

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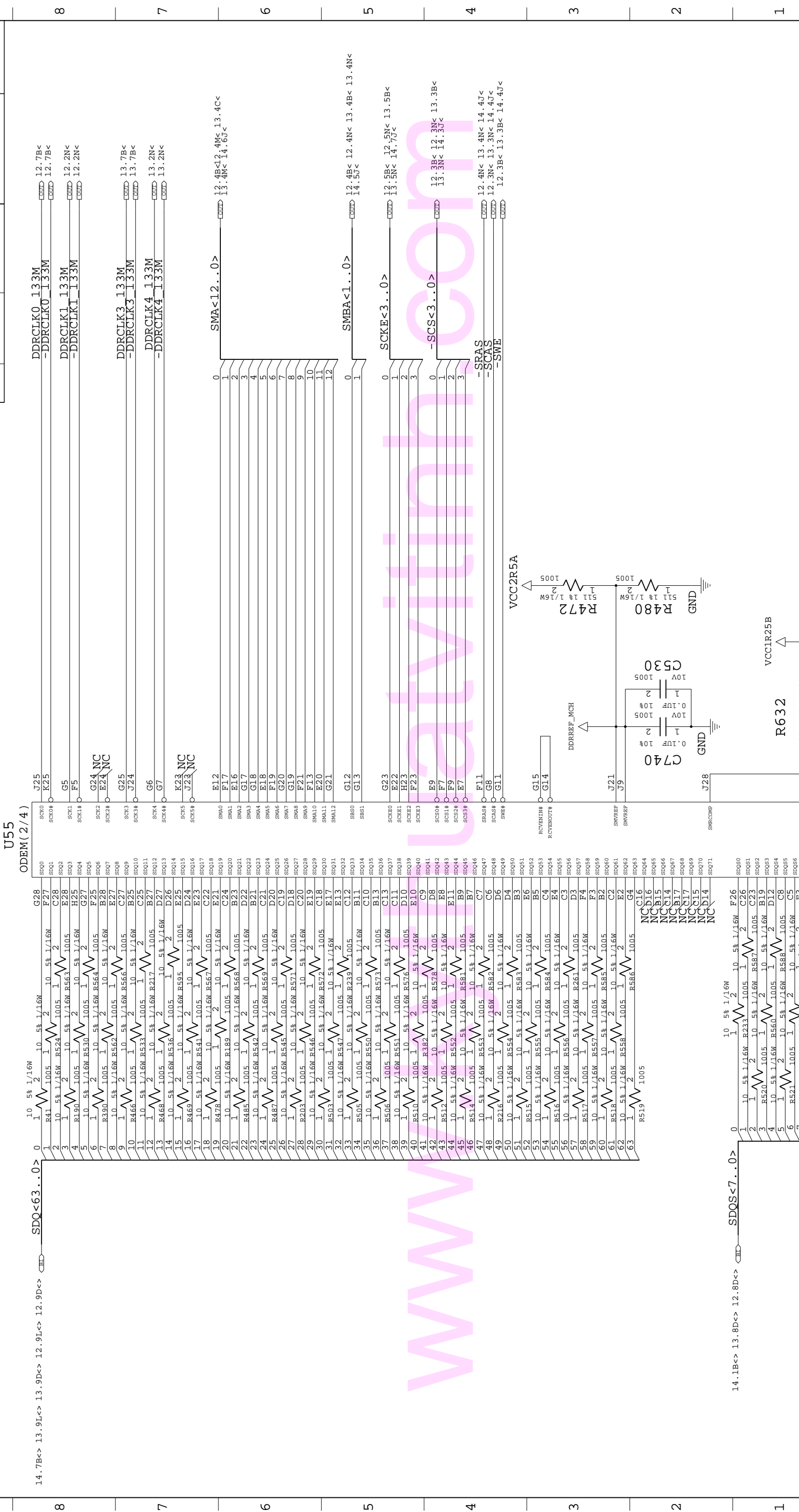
DATE	10/25/02	VER	0.73
PART NO.			
DEVELOPMENT NO.		8 / 82	

DESIGNER	T.O	10/25/02	PART NO.	
CHECKED			TITLE	ROME-1 SIT
APPROVED			MCH-M(1/4):HOST I/F	
CLASS			IBM CONFIDENTIAL	

HRCOMPO, 1: Z0=27.4 OHM

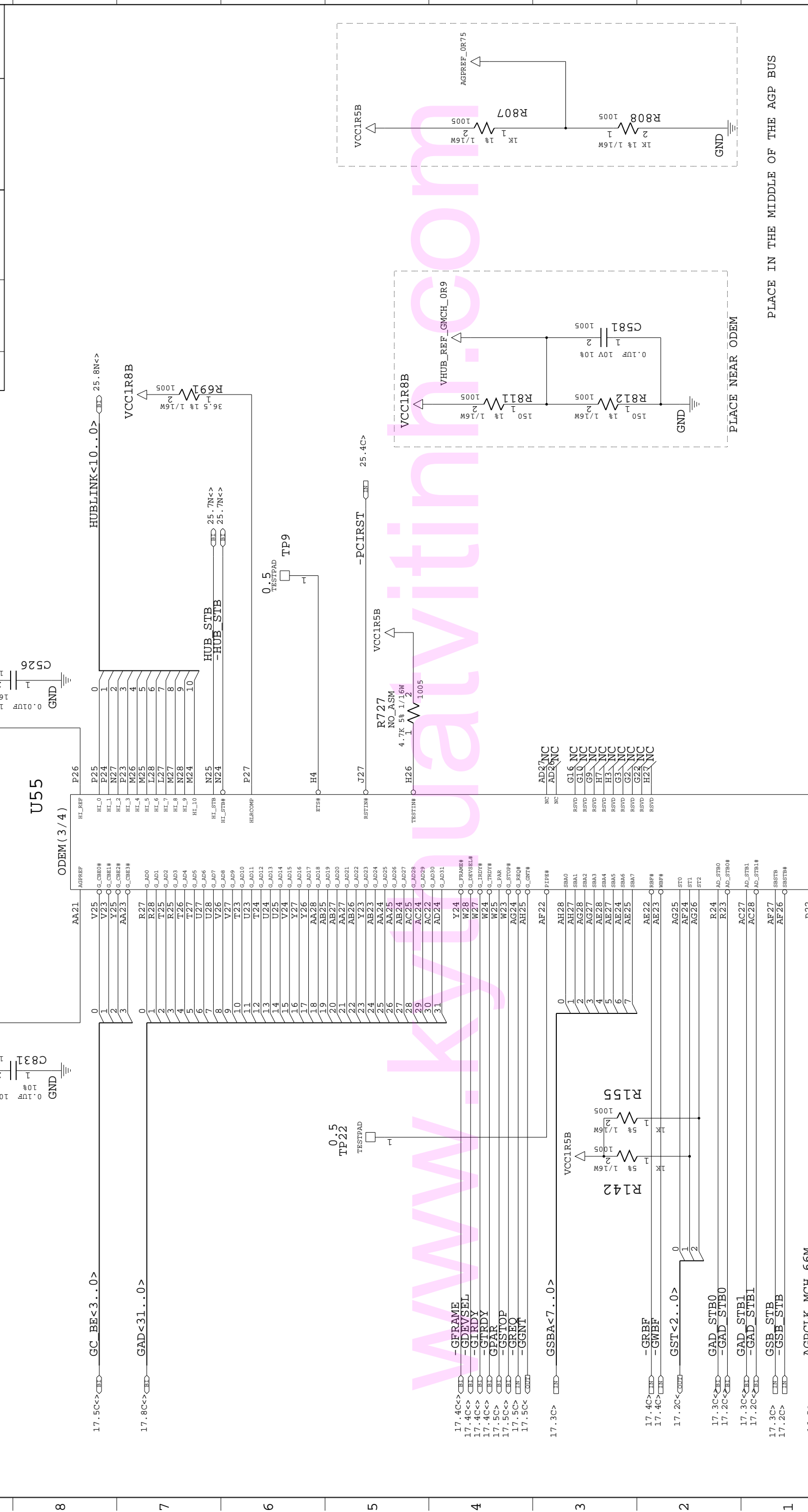
www.tinh.com



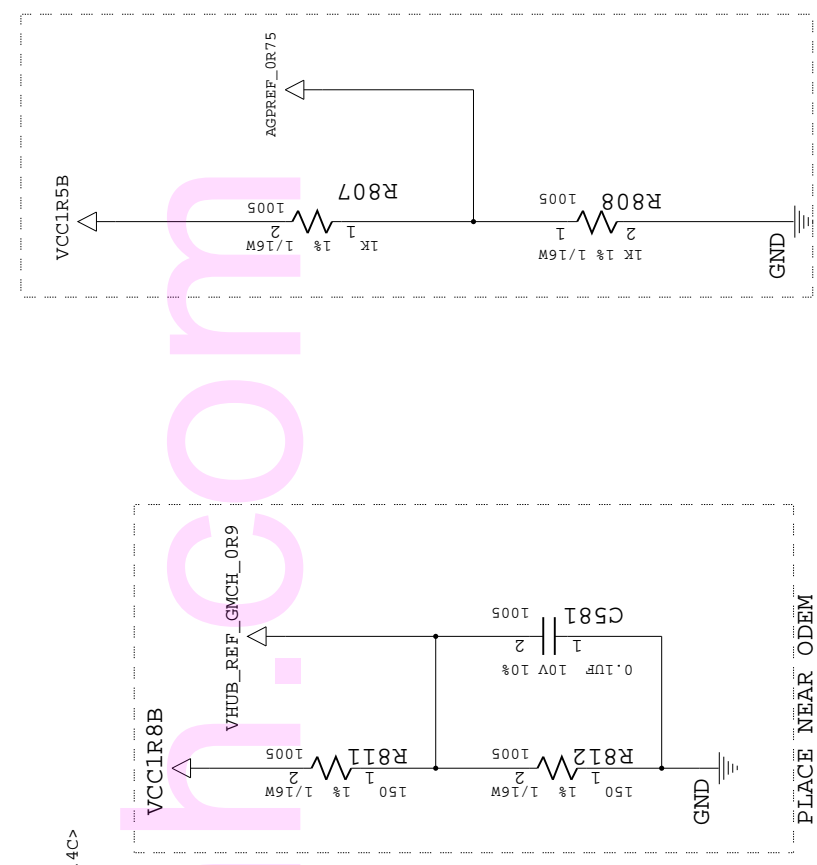


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TITLE		ROME-1 SIT	
MCH-M(2/4)		MEMORY I/F	
IBM CONFIDENTIAL			

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EC NO.			
PART NO.			
DEVELOPMENT NO.			10 / 82

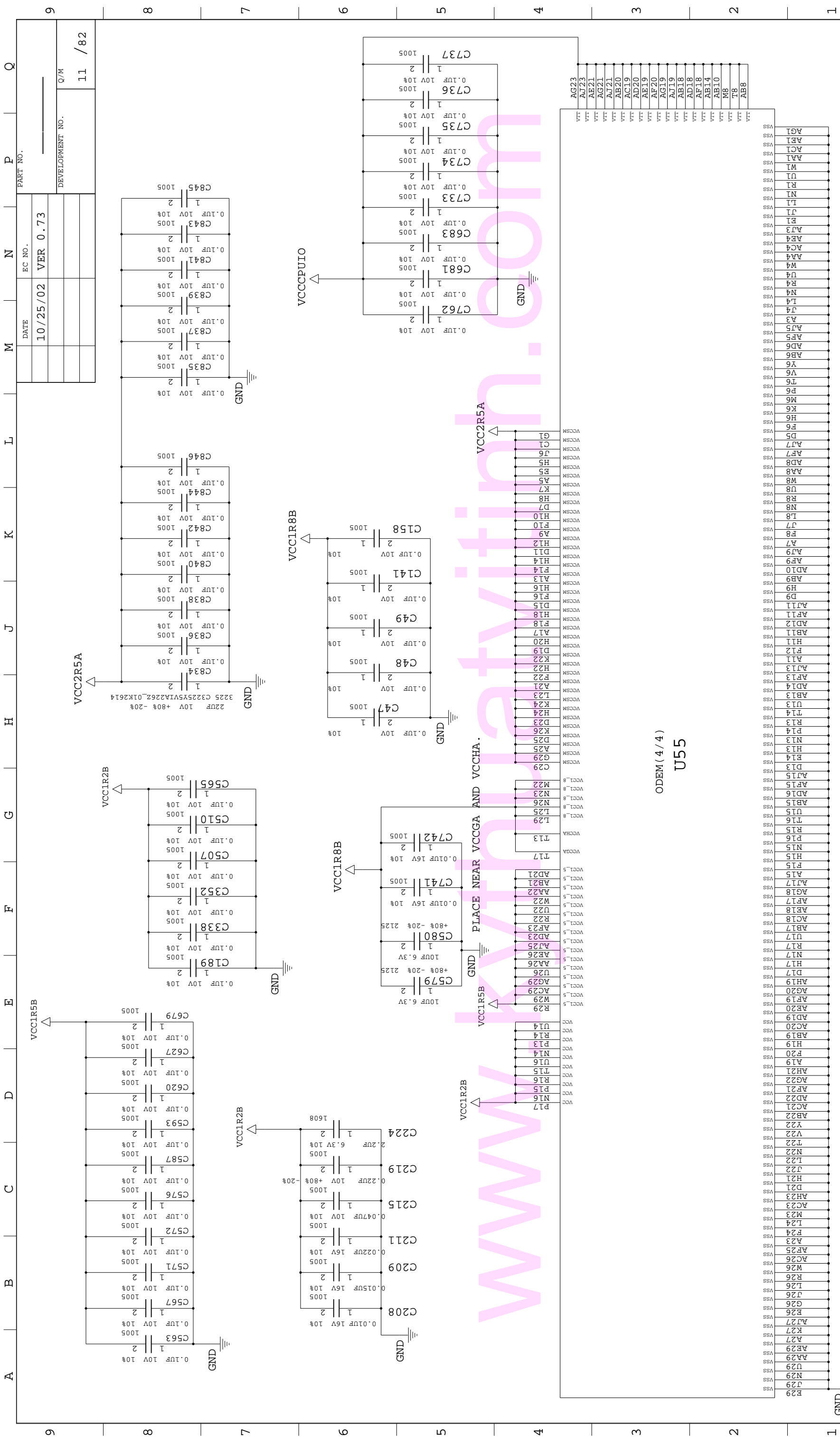


PLACE IN THE MIDDLE OF THE AGP BUS



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APPROVED			TITLE	ROME-1 SIT
CLASS				MCH-M(3/4):AGP/HUB I/F

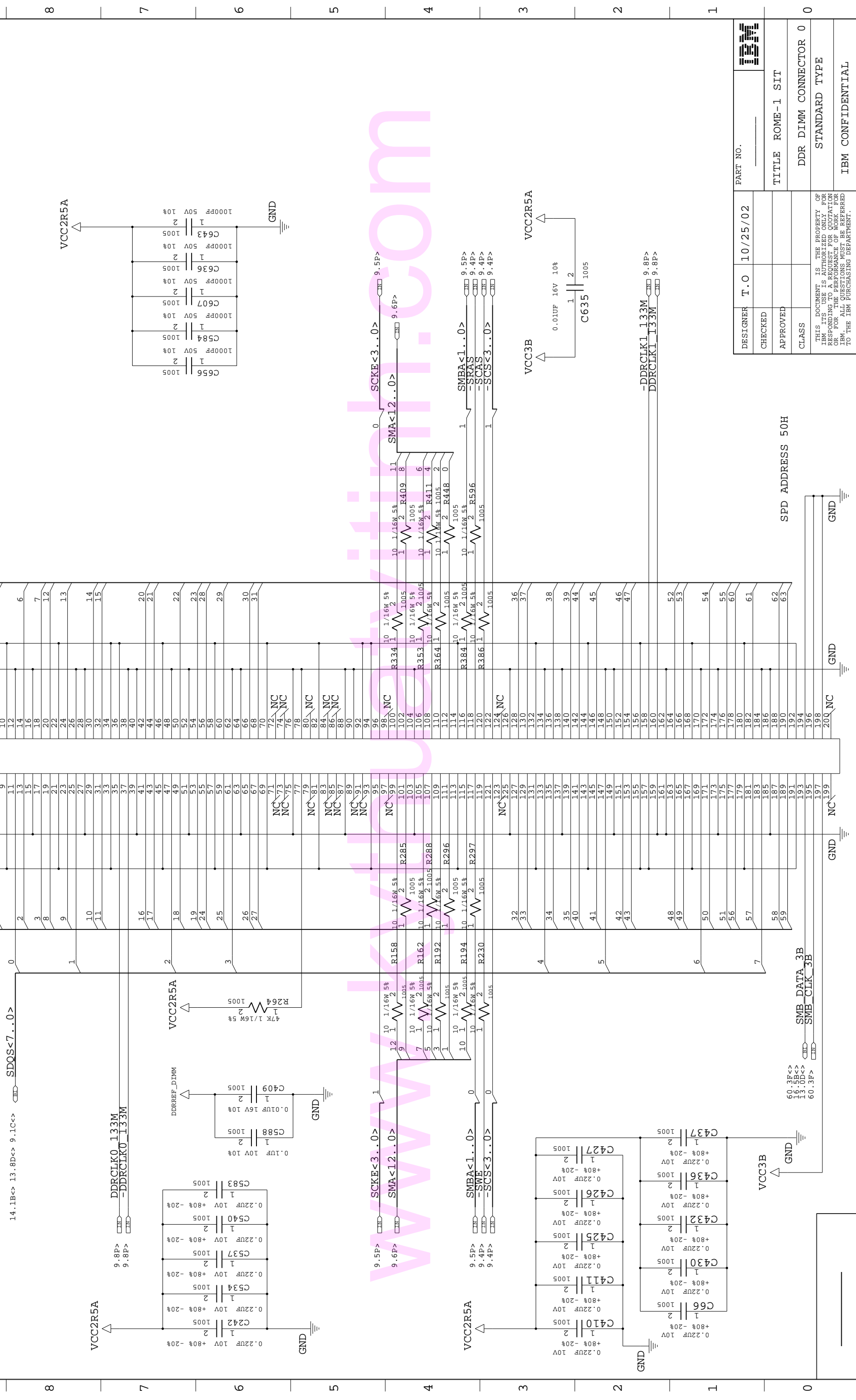
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ODEM ( 4 / 4 )  
U55

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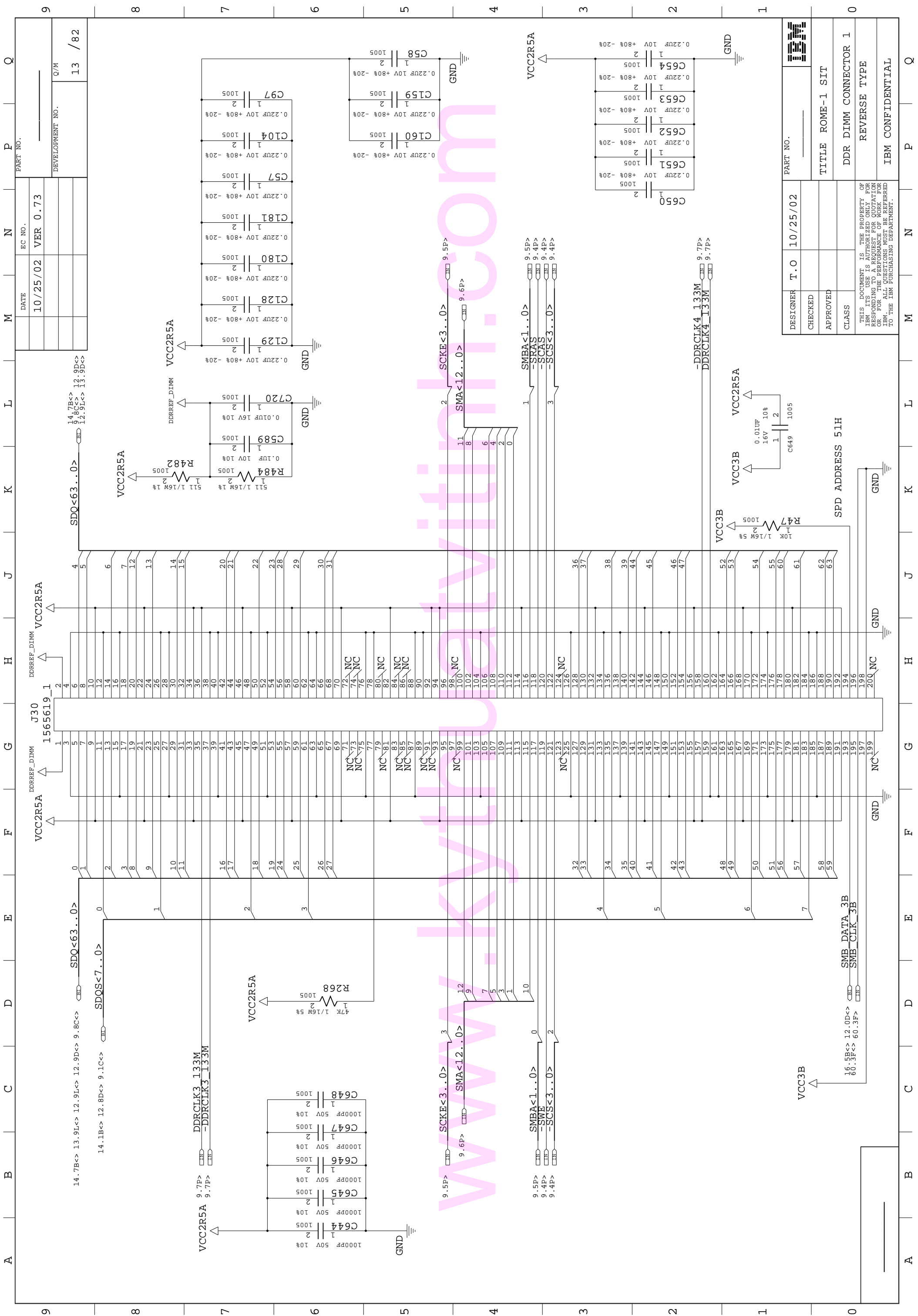
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TITLE ROME-1 SIT				
DDR DIMM CONNECTOR 0				
STANDARD TYPE				
IBM CONFIDENTIAL				

SPD ADDRESS 50H





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CLASS			TITLE	ROME-1 SIT
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				DDR DIMM CONNECTOR 1
				IBM CONFIDENTIAL

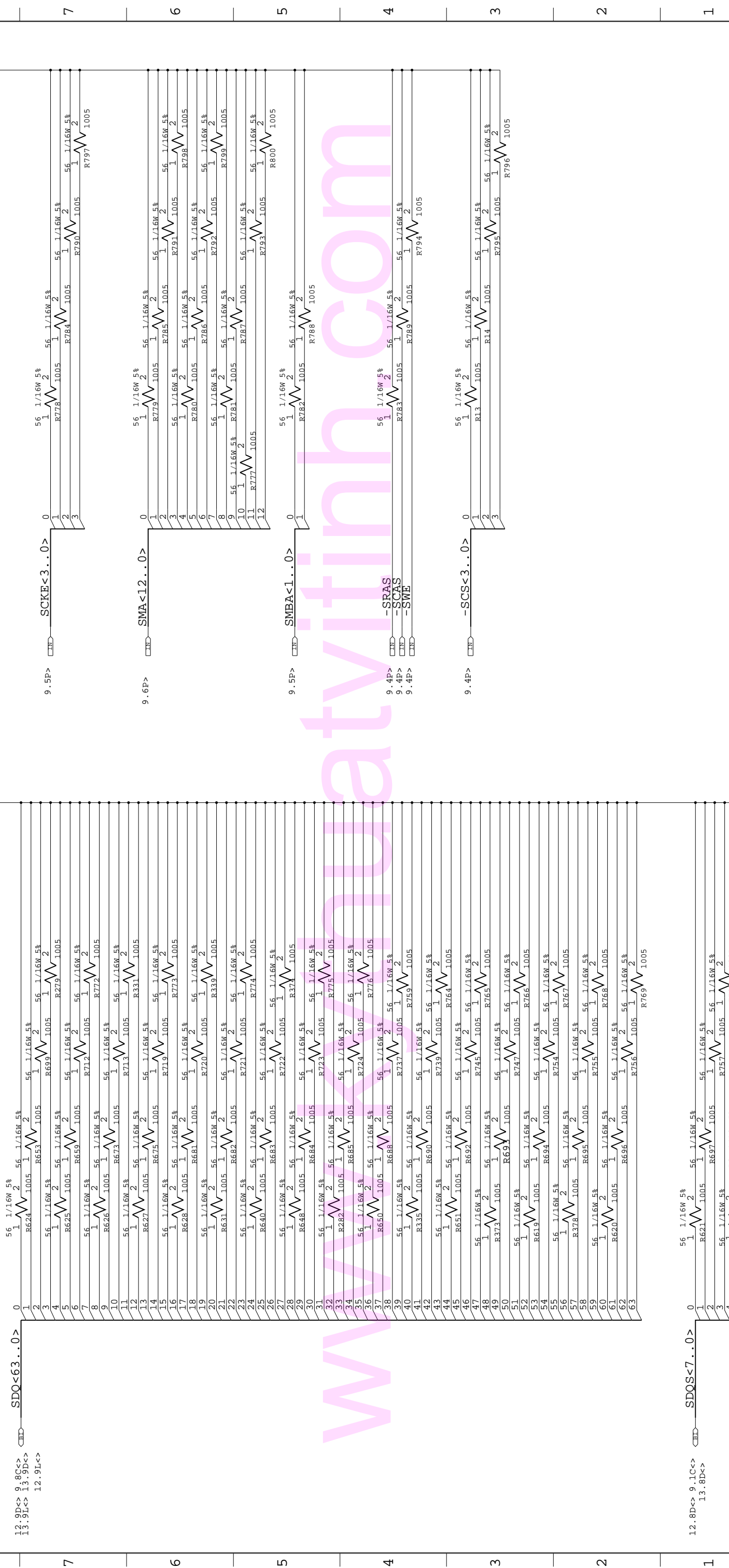
A B C D E F G H J K L M N P Q  
 0 1 2 3 4 5 6 7 8 9

DATE	EC NO.	PART NO.
10/25/02	VER 0.73	
DEVELOPMENT NO.		Q/M
		14 / 82

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CLASS			
TITLE ROME-1 SIT			
SSTL-2 TERMINATION			
IBM CONFIDENTIAL			

VCC1R25B

VCC1R25B



12.9D<> 9.8C<>  
13.9D<> 13.9D<>  
12.9L<>

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9.6P> SMA<12..0>

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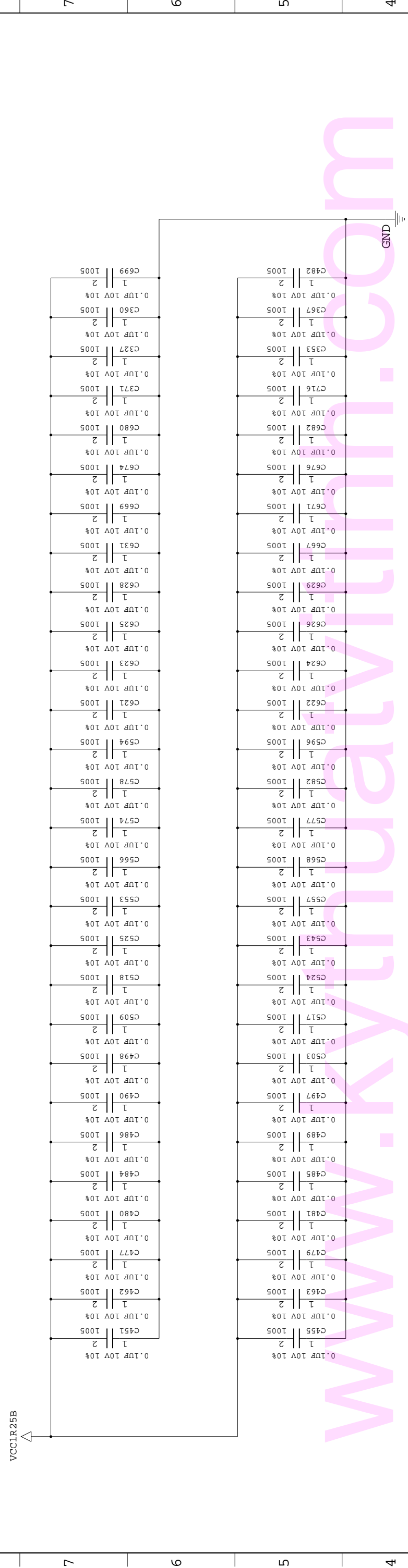
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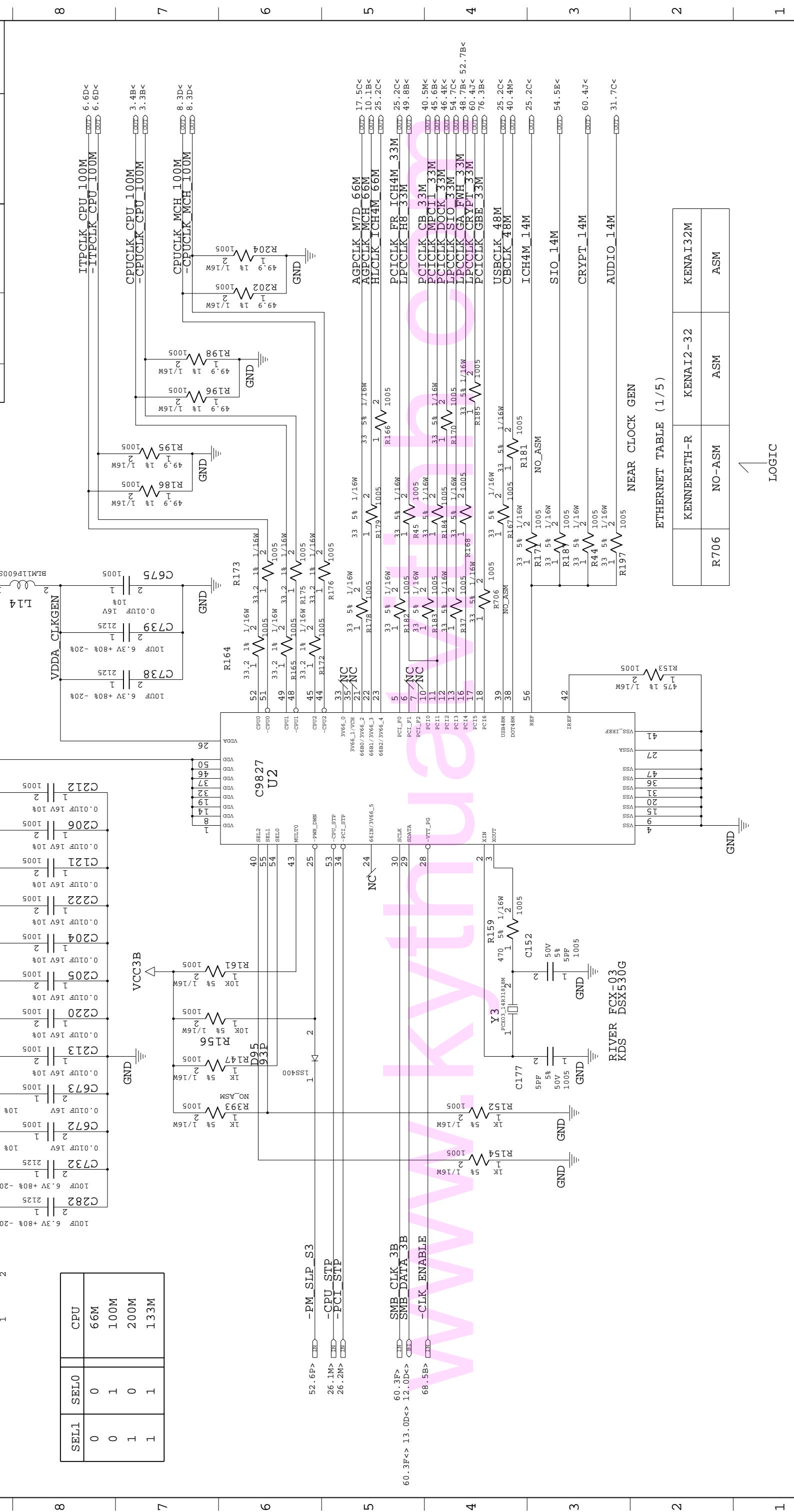
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DATE 10/25/02												PART NO.		
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DEVELOPMENT NO.												Q/M		
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PLACE 1 CAP FOR EVERY 2 BITS TERMINATED TO VCC1R25B.



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A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q
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TITLE ROME-1 SIT			
CLOCK GEN (CK-408)			
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ETHERNET TABLE (1/5)

KENNERETH-R	KENAI2-32	KENAI32M
R706	NO-ASM	ASM

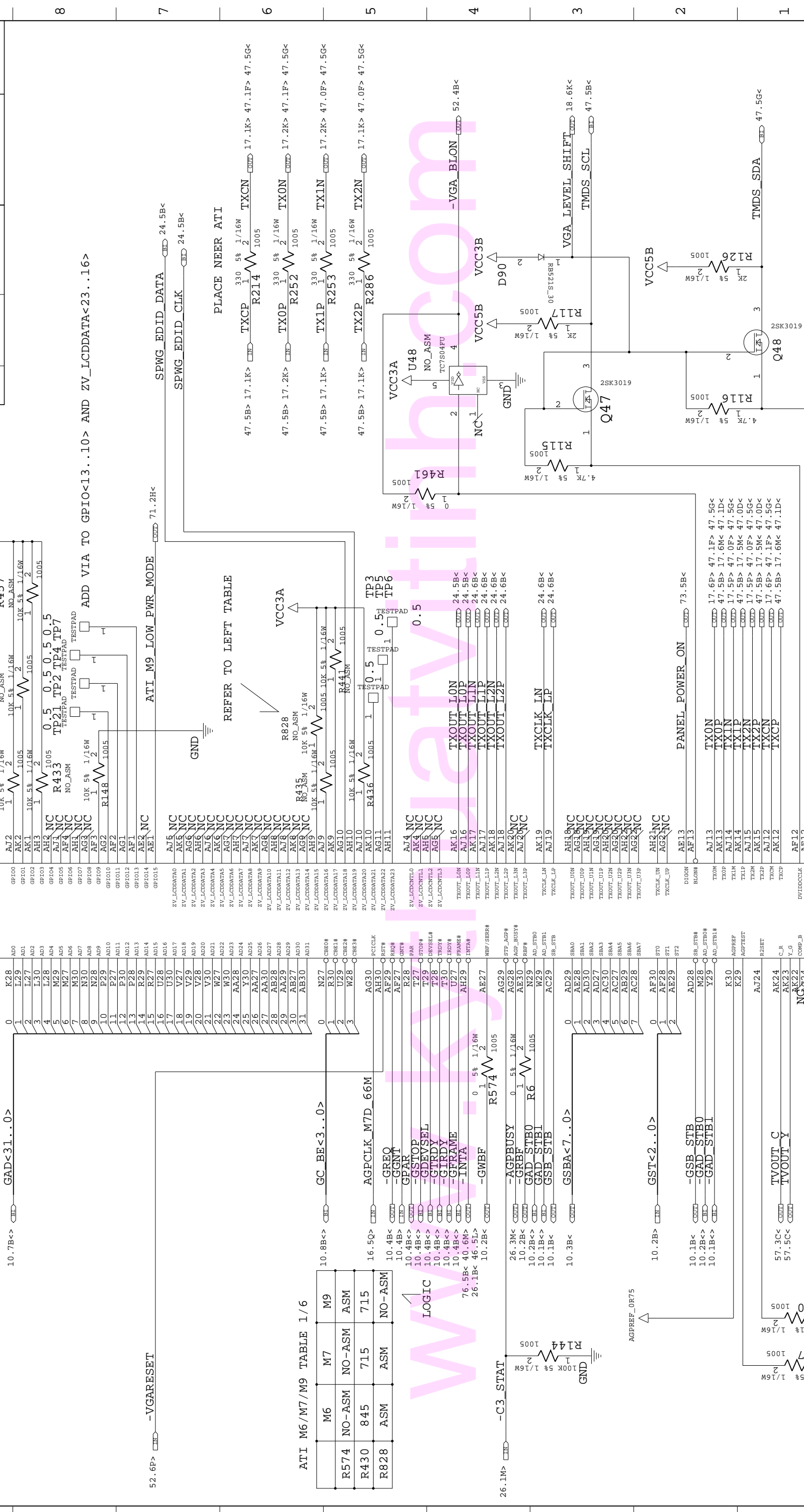
LOGIC

RIVER FCX-03  
KDS DSX530G

SEL1	SEL0	CPU
0	0	66M
0	1	100M
1	0	200M
1	1	133M

PLACE AT LEAST 1 CAP FOR EACH VDD PINS





ATI M6/M7/M9 TABLE 1/6

M6	M7	M9
R574	NO-ASM	ASM
R430	715	715
R828	ASM	NO-ASM

REFER TO ABOVE TABLE

DESIGNER: T.O 10/25/02  
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 APPROVED: \_\_\_\_\_  
 CLASS: \_\_\_\_\_

PART NO. \_\_\_\_\_  
 TITLE: ROME-1 SIT  
 RADEON M9\_CSP (1/7)

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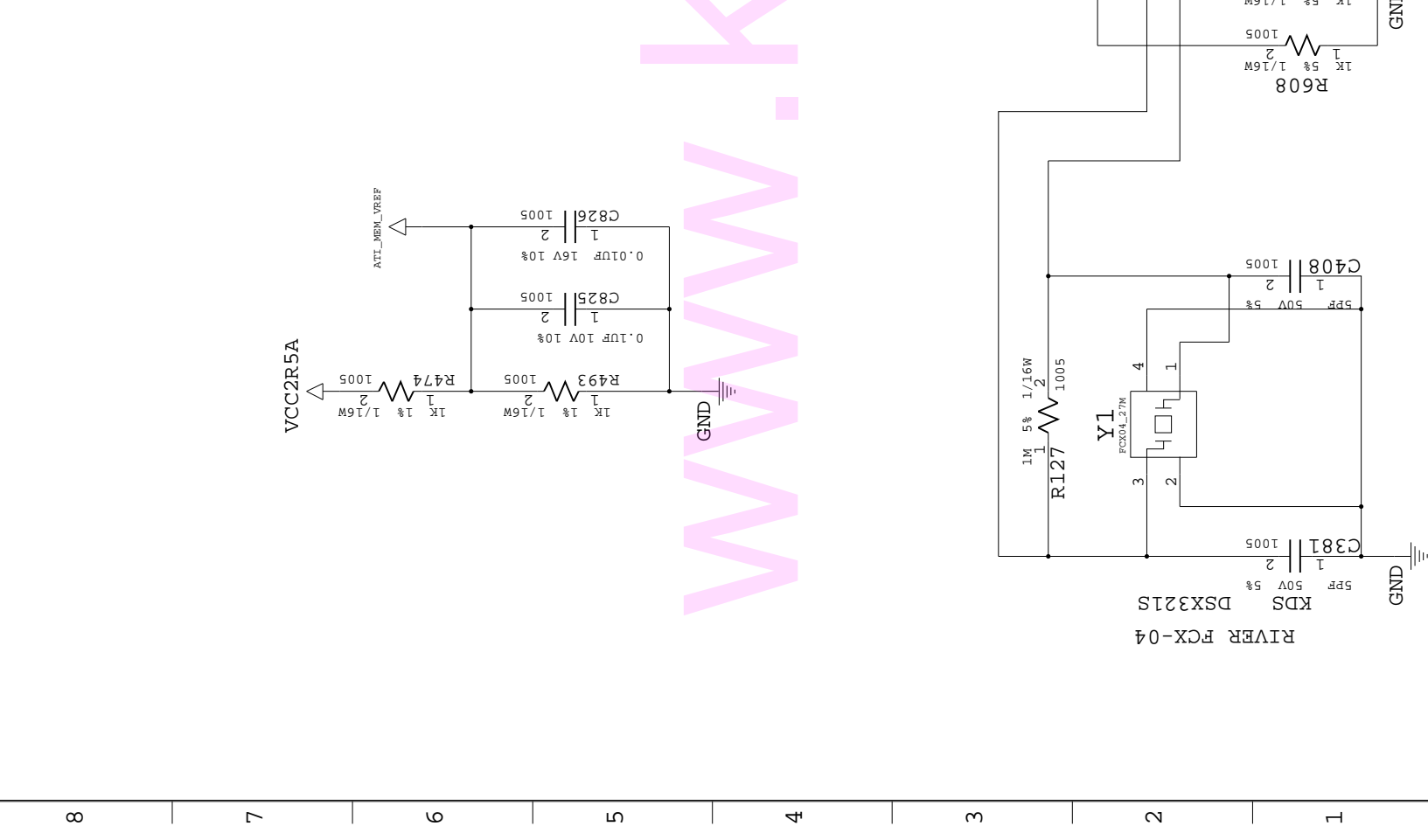
M9\_CSP\_120G\_DI(2/7)

ATI M6/M7/M9 TABLE 2/6

	M6	M7	M9
R481	NO-ASM	ASM	ASM
R464	NO-ASM	ASM	ASM
R54	ASM	NO-ASM	NO-ASM
R494	ASM	NO-ASM	NO-ASM
R896	NO-ASM	ASM	ASM
R897	NO-ASM	ASM	ASM

LOGIC

Pin	Signal	Value
J30	DQ00	NC
J29	DQ01	NC
H30	DQ02	NC
H29	DQ03	NC
F30	DQ04	NC
F29	DQ05	NC
E30	DQ06	NC
E29	DQ07	NC
D30	DQ08	NC
D29	DQ09	NC
C30	DQ10	NC
C29	DQ11	NC
B30	DQ12	NC
B29	DQ13	NC
A30	DQ14	NC
A29	DQ15	NC
A28	DQ16	NC
A27	DQ17	NC
A26	DQ18	NC
A25	DQ19	NC
A24	DQ20	NC
A23	DQ21	NC
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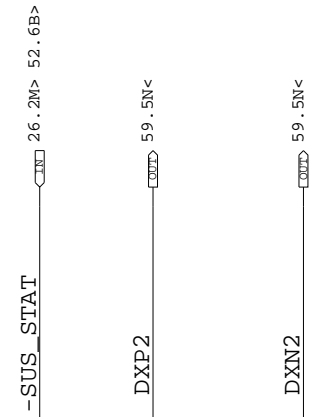
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TITLE		ROME-1 SIT		
CLASS		RADEON M9_CSP (2/7)		
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M9\_CSP\_120G\_DI (3/7)

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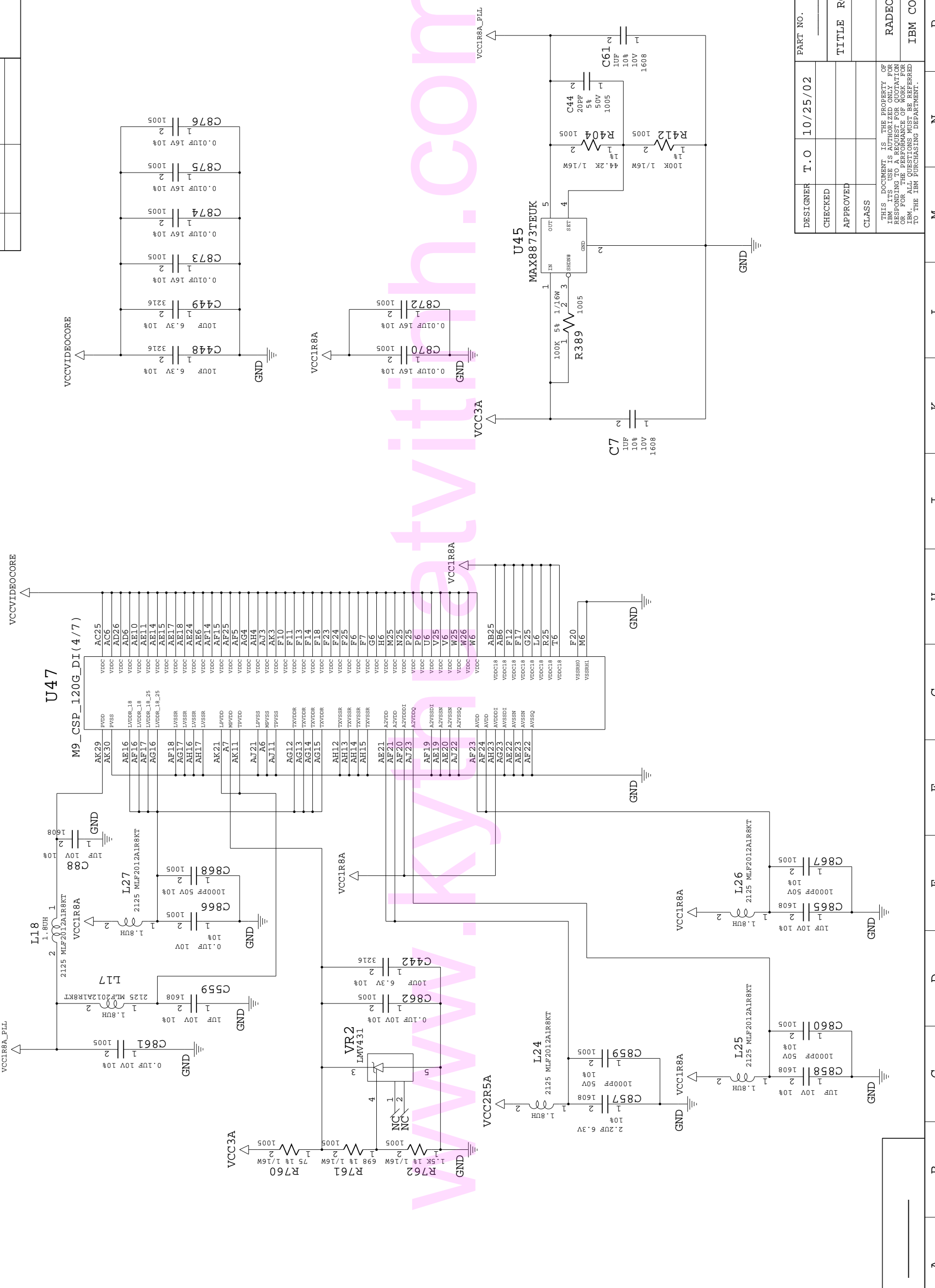
ATI M6/M7/M9 TABLE 4/6

R544	ASM	ASM	M9	NO_ASM
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LOGIC

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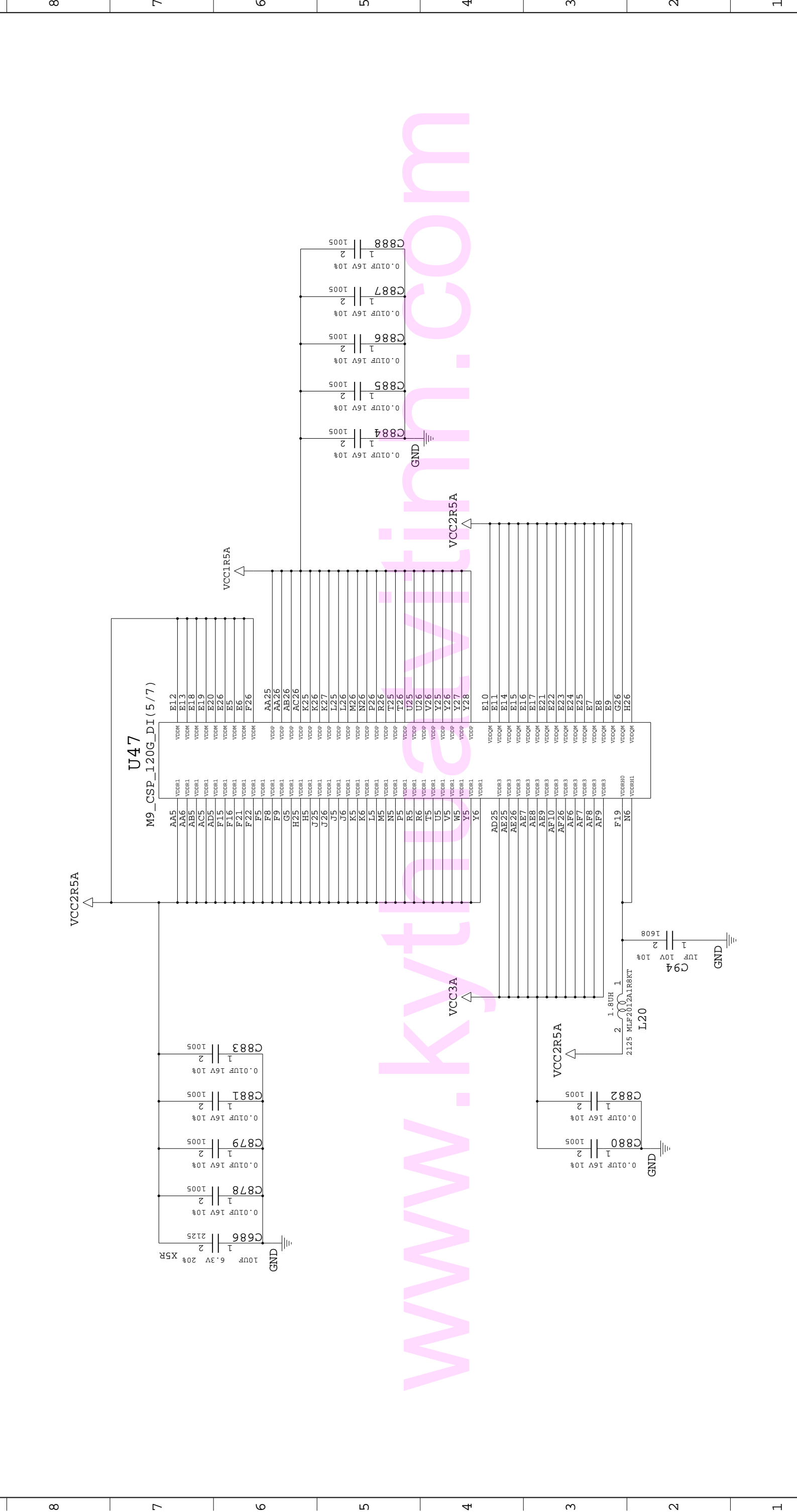
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DATE: 10/25/02 EC NO.: VER 0.73 DEVELOPMENT NO.: Q/M 20 / 82												PART NO.: _____		



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DEVELOPMENT NO.			21 / 82	Q/M	



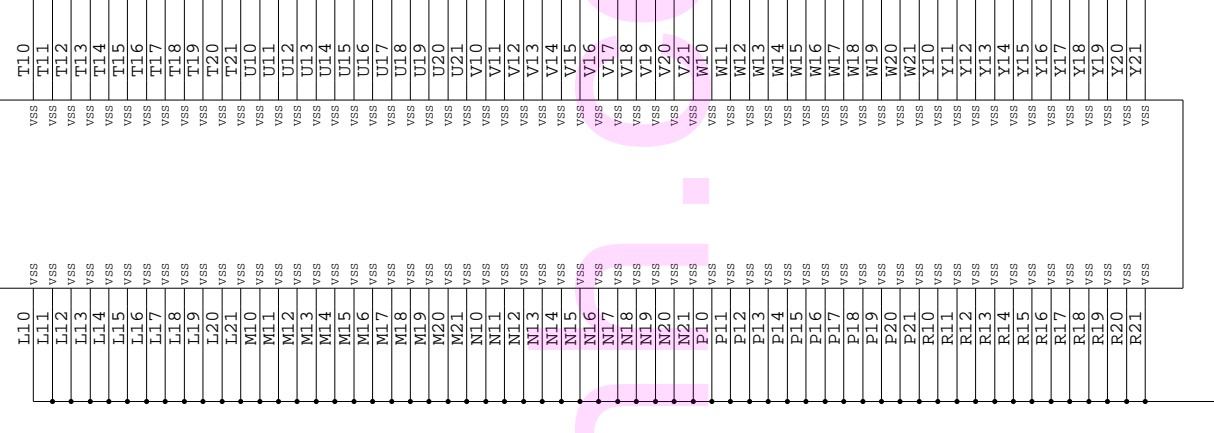
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		22 / 82

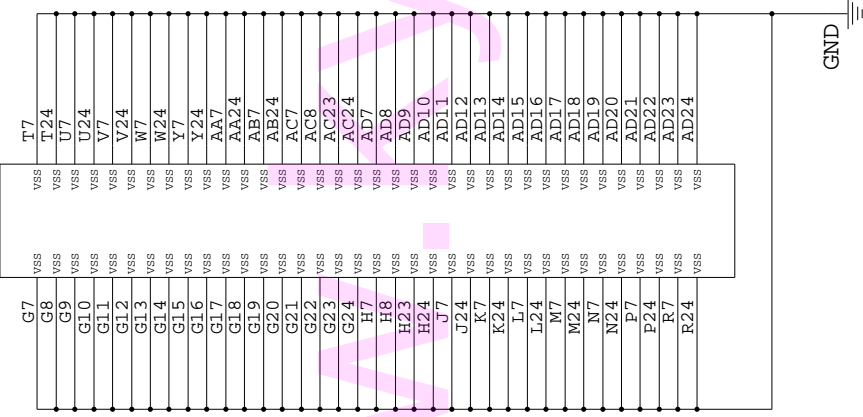
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M9\_CSP\_120G\_DI(7/7)



U47

M9\_CSP\_120G\_DI(6/7)

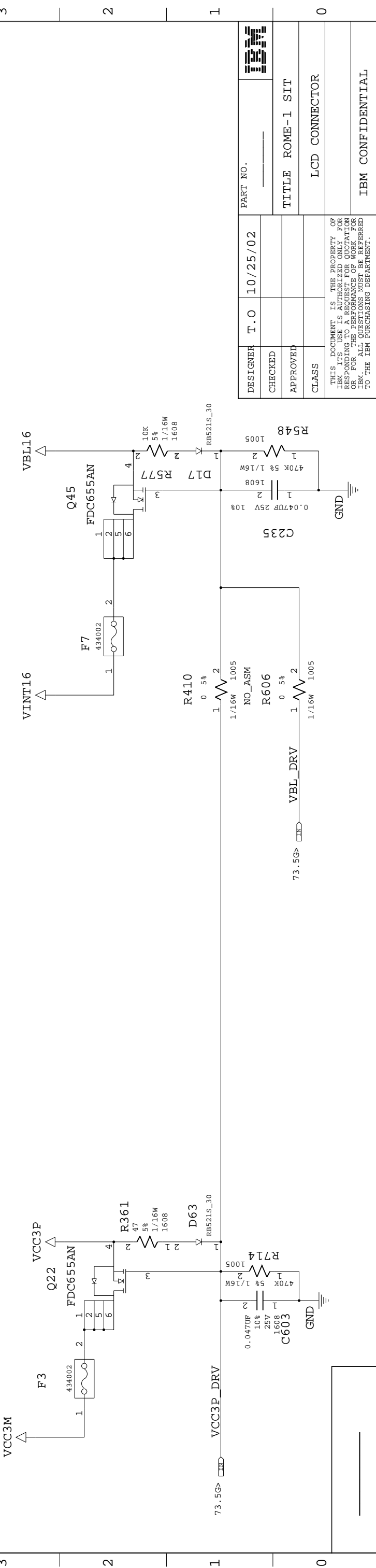
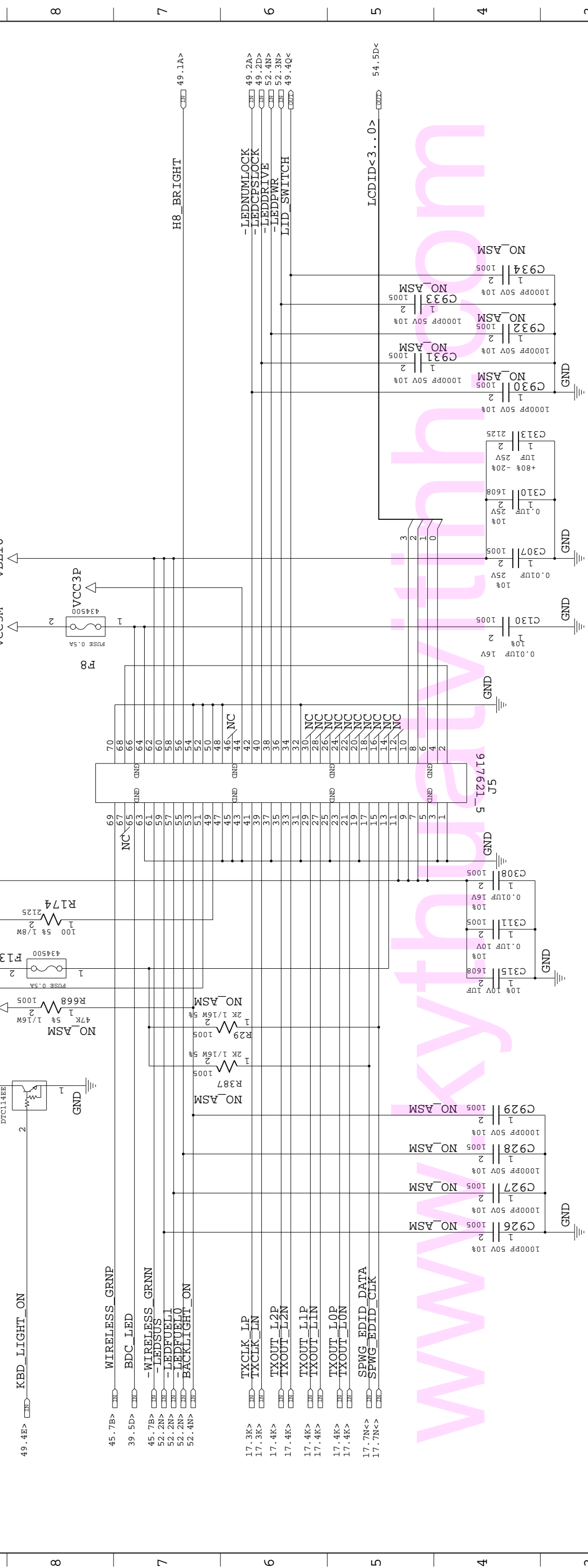


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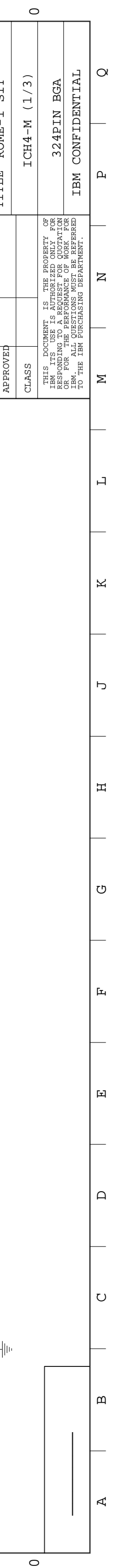
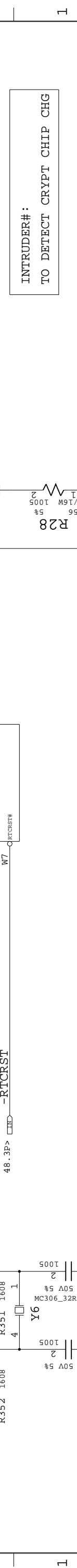
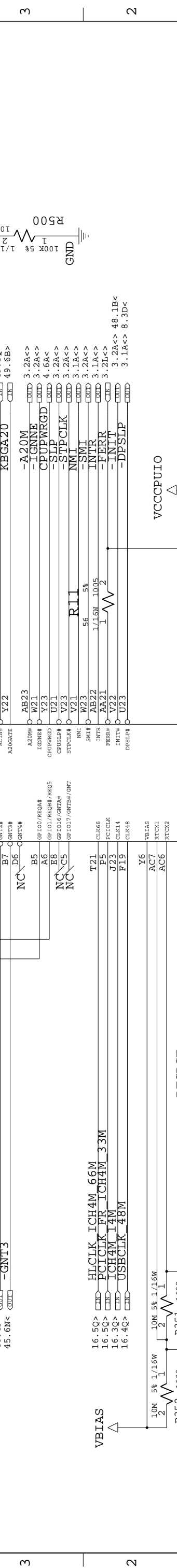
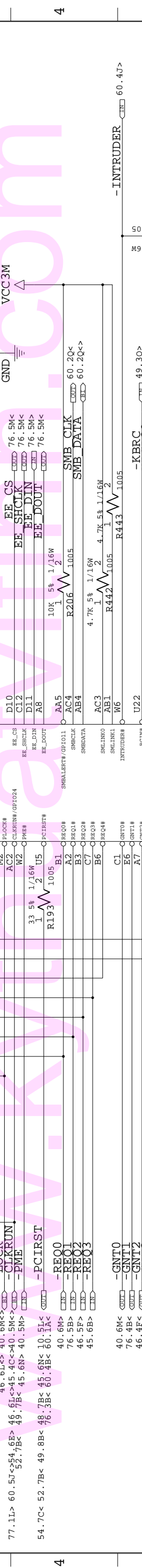
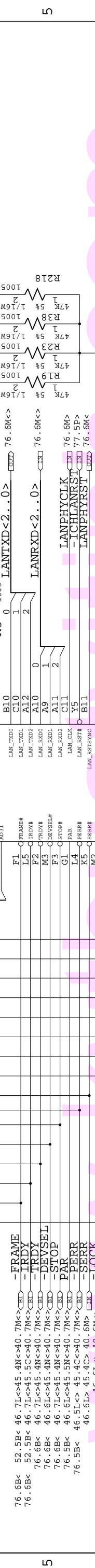
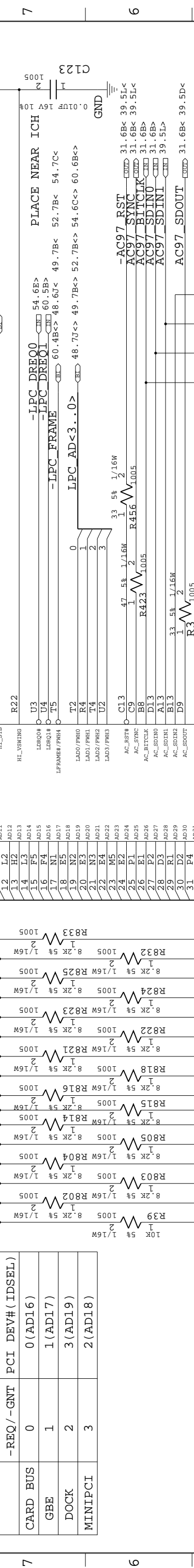
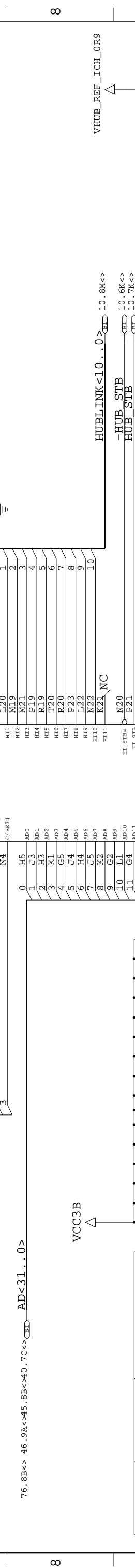


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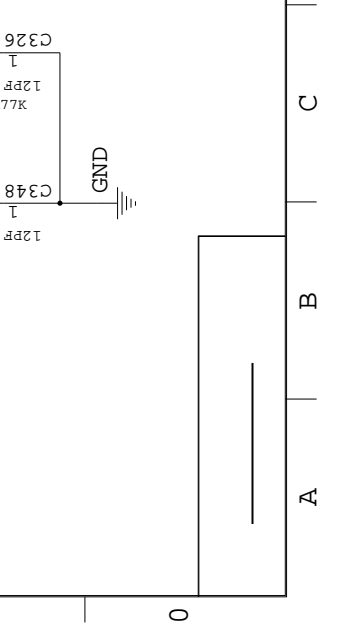
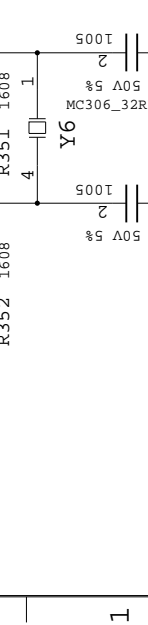
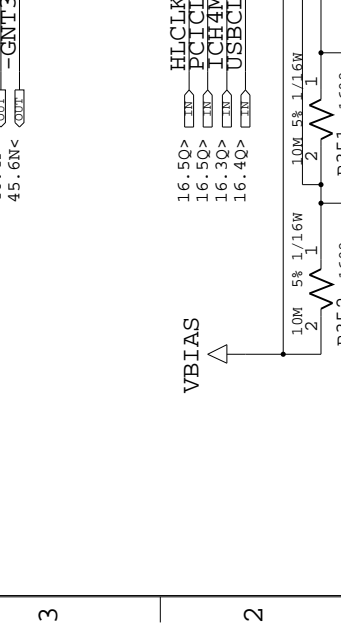


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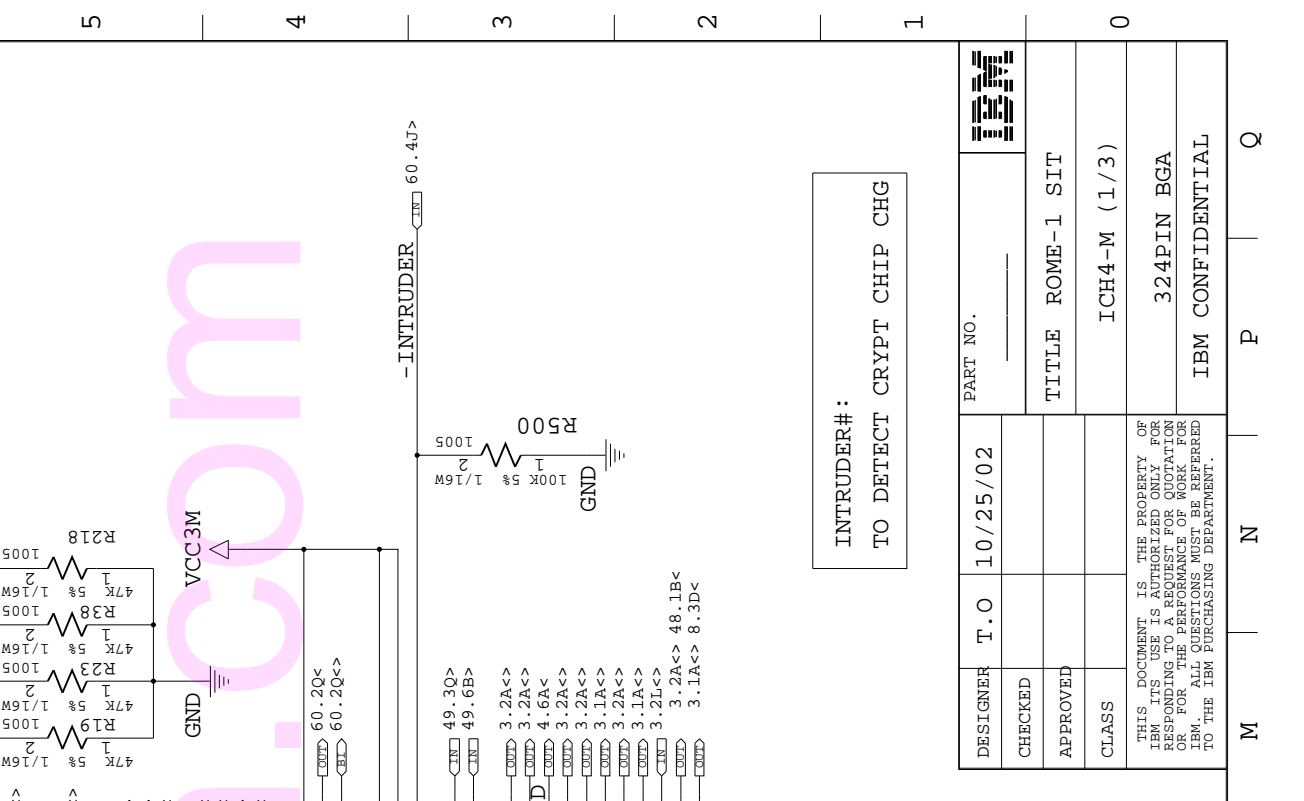
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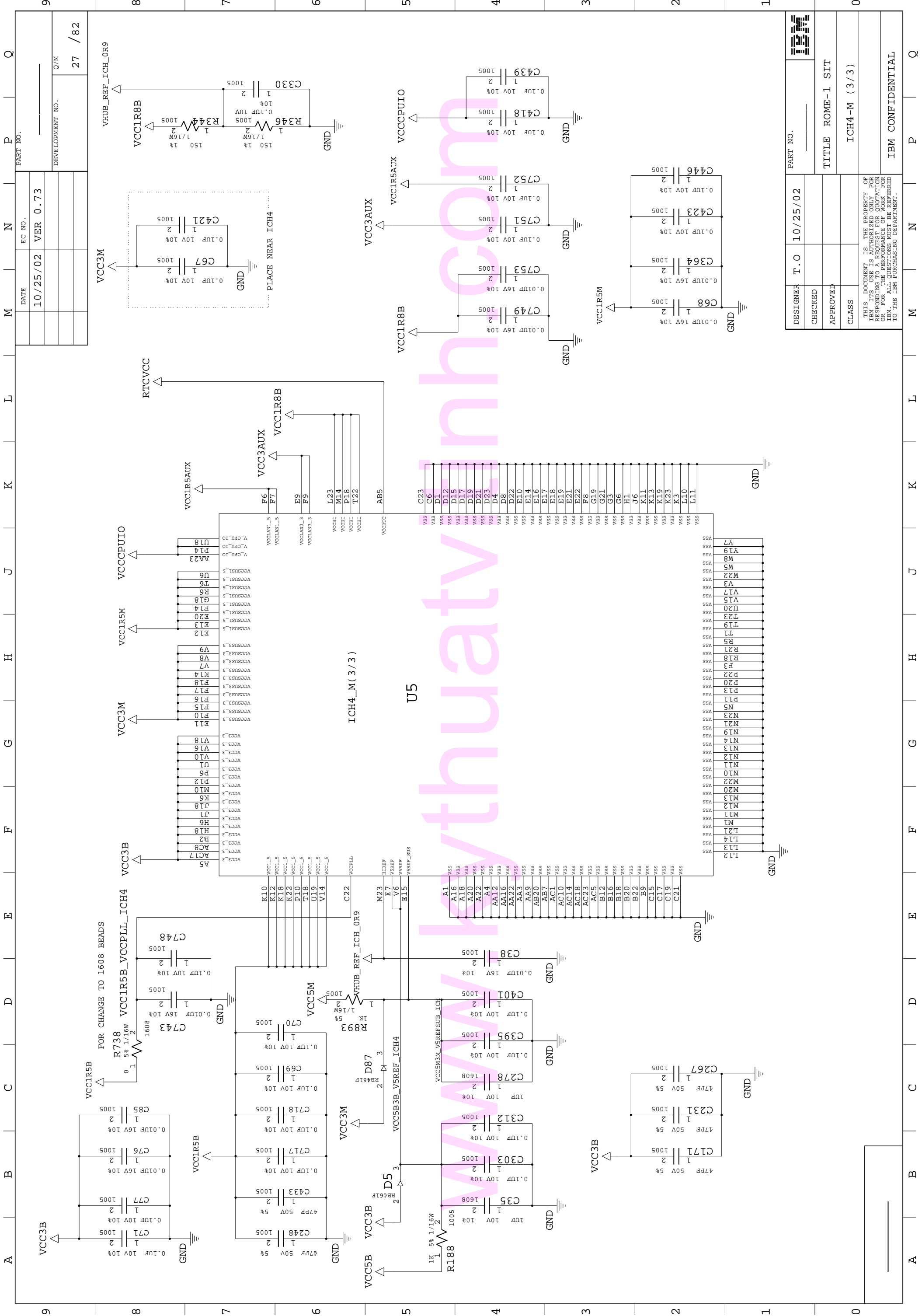
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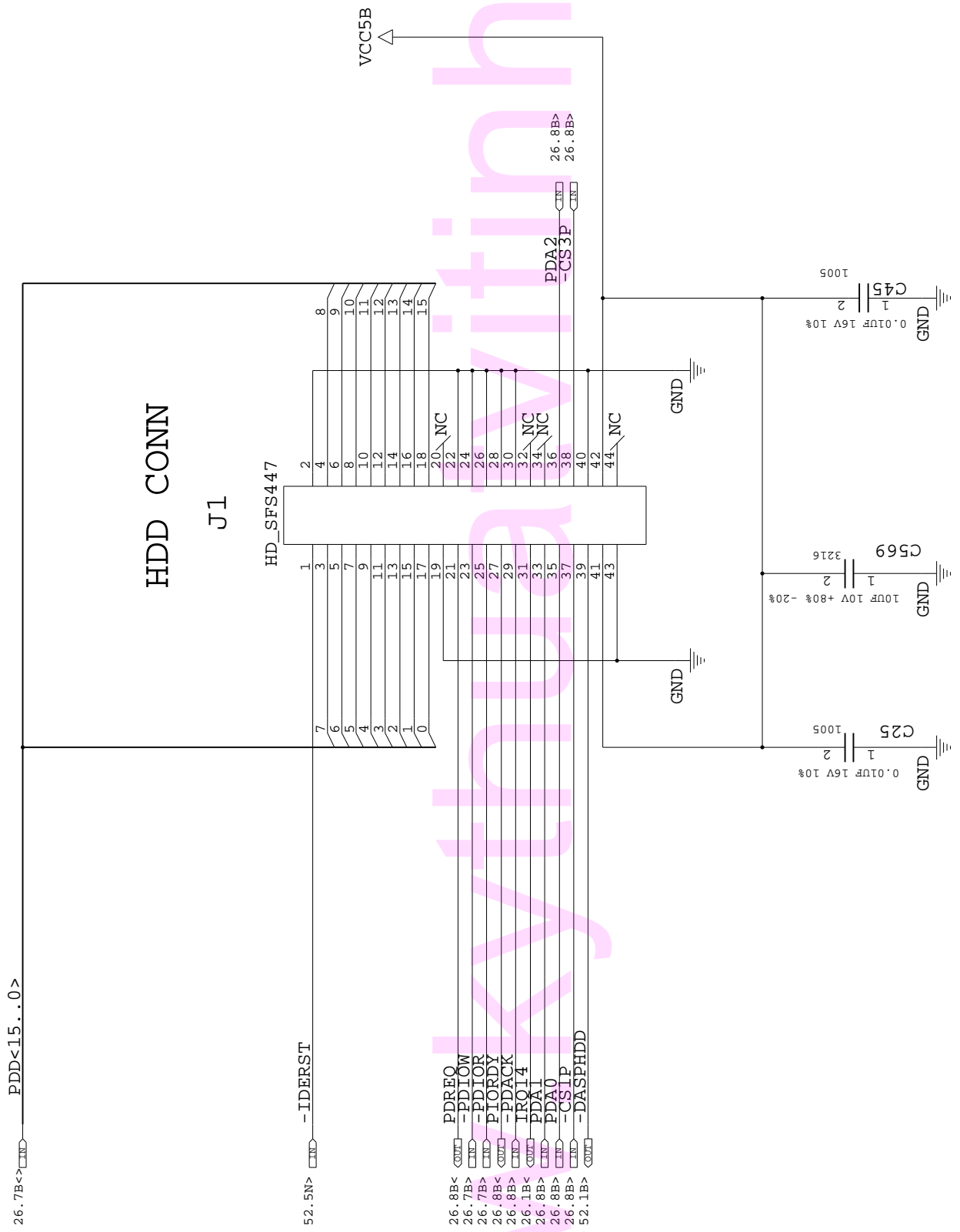




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DEVELOPMENT NO.					
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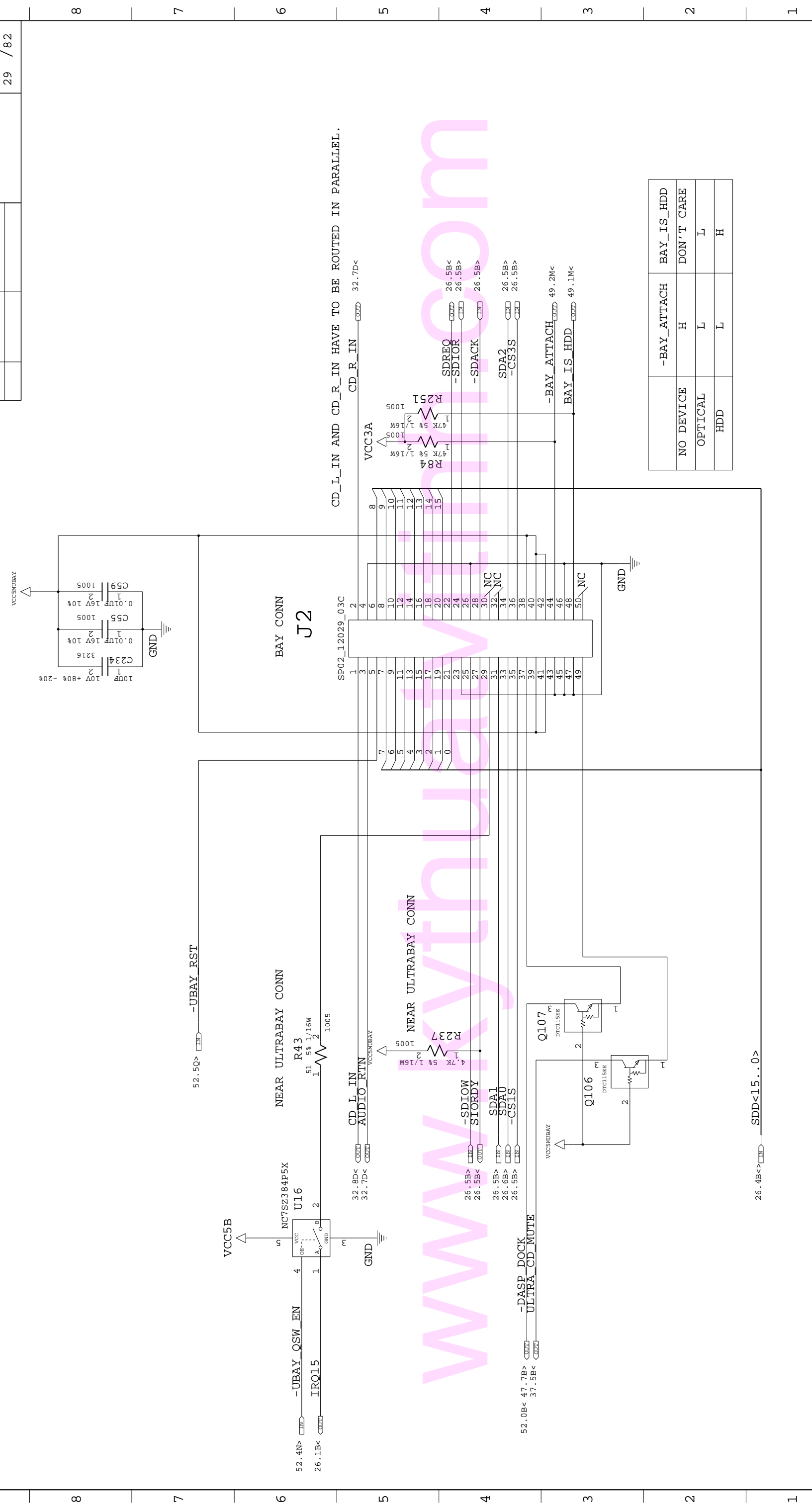
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10/25/02	VER 0.73		
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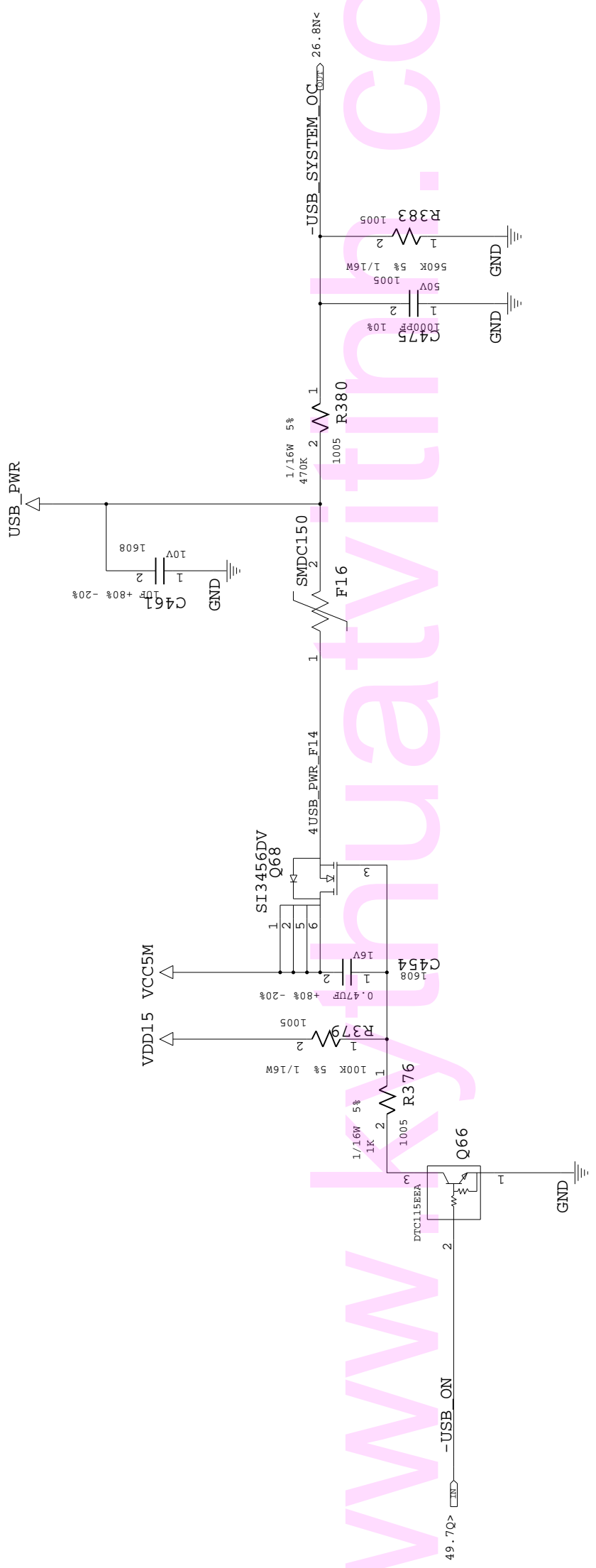


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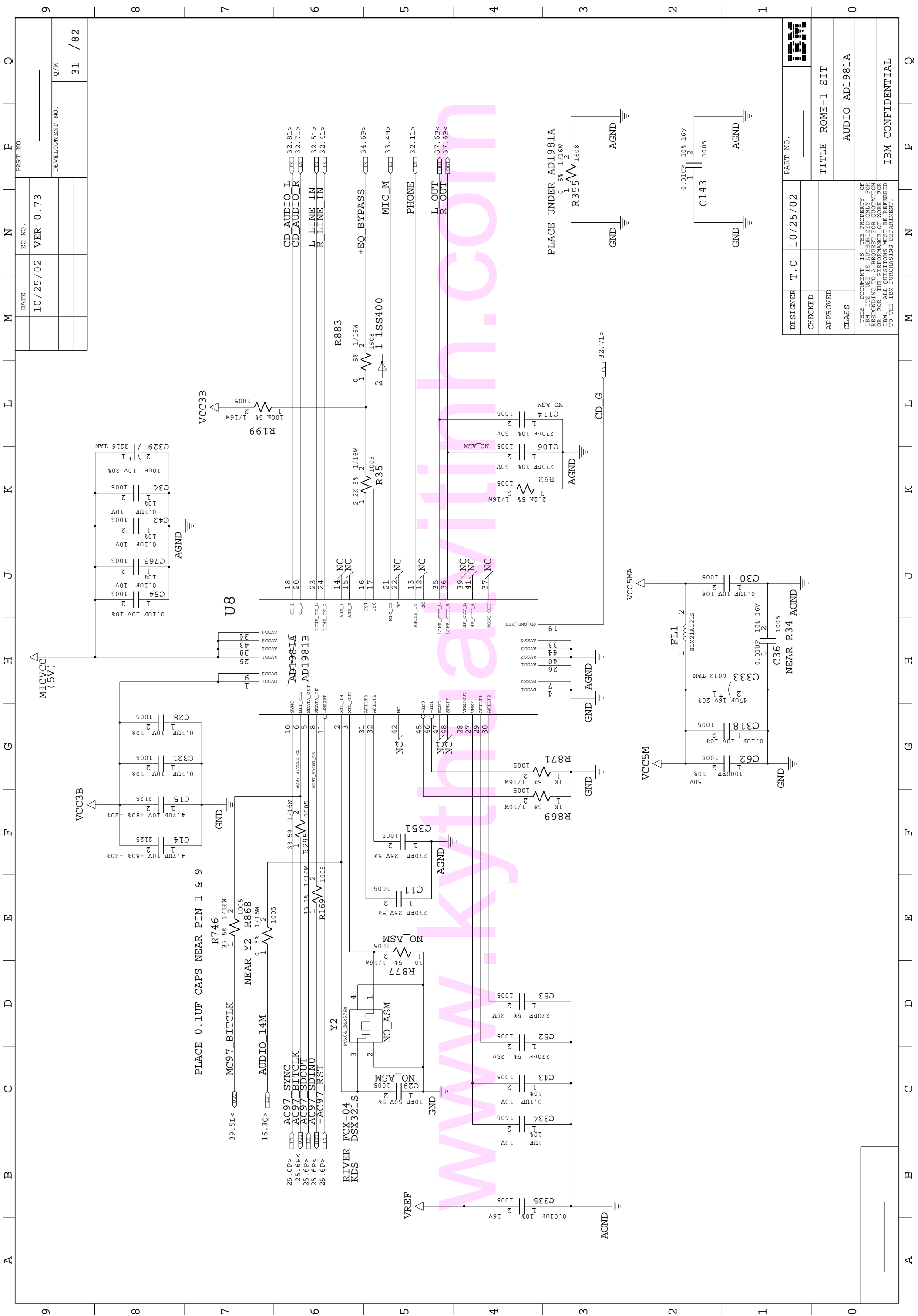
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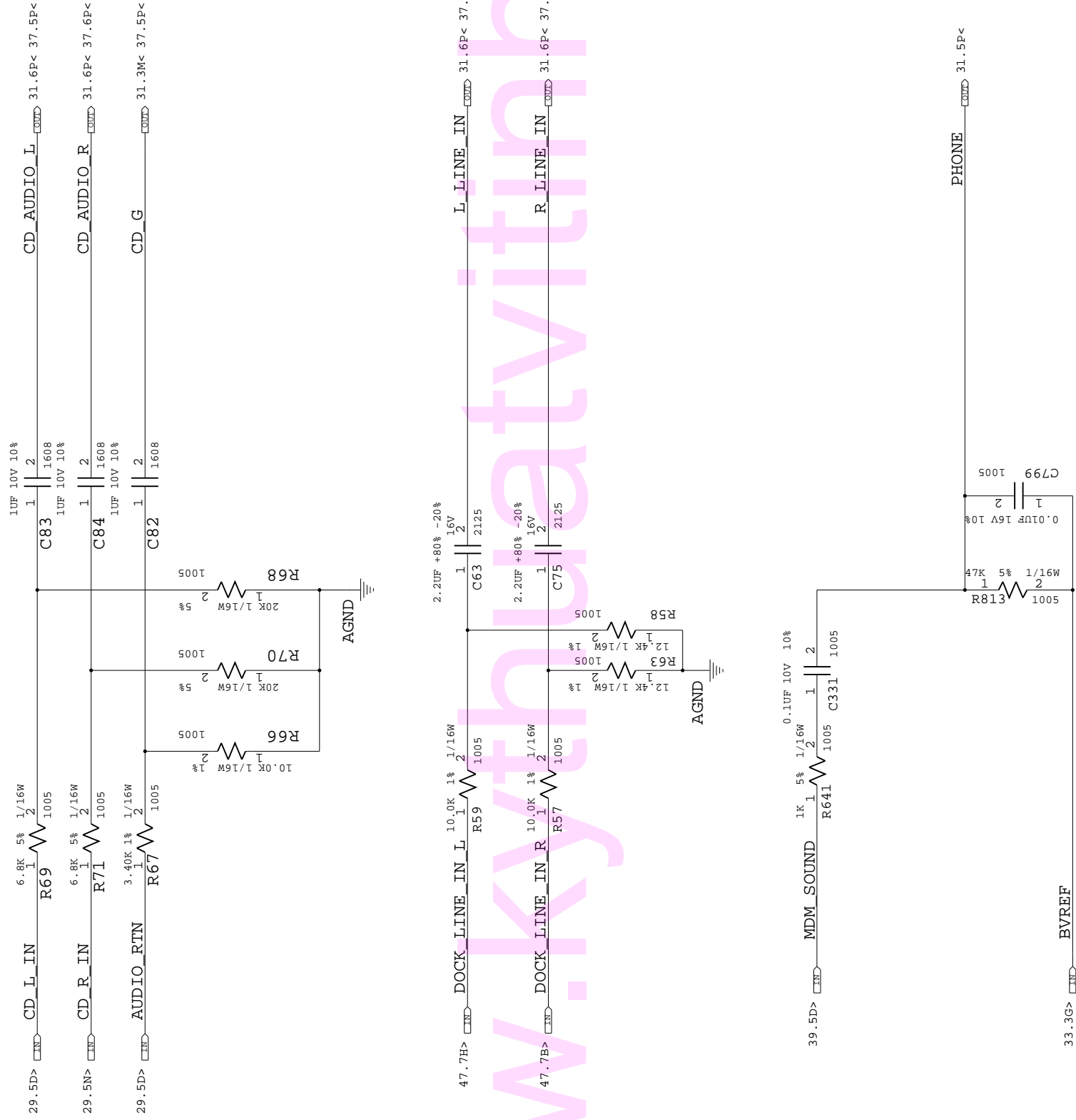
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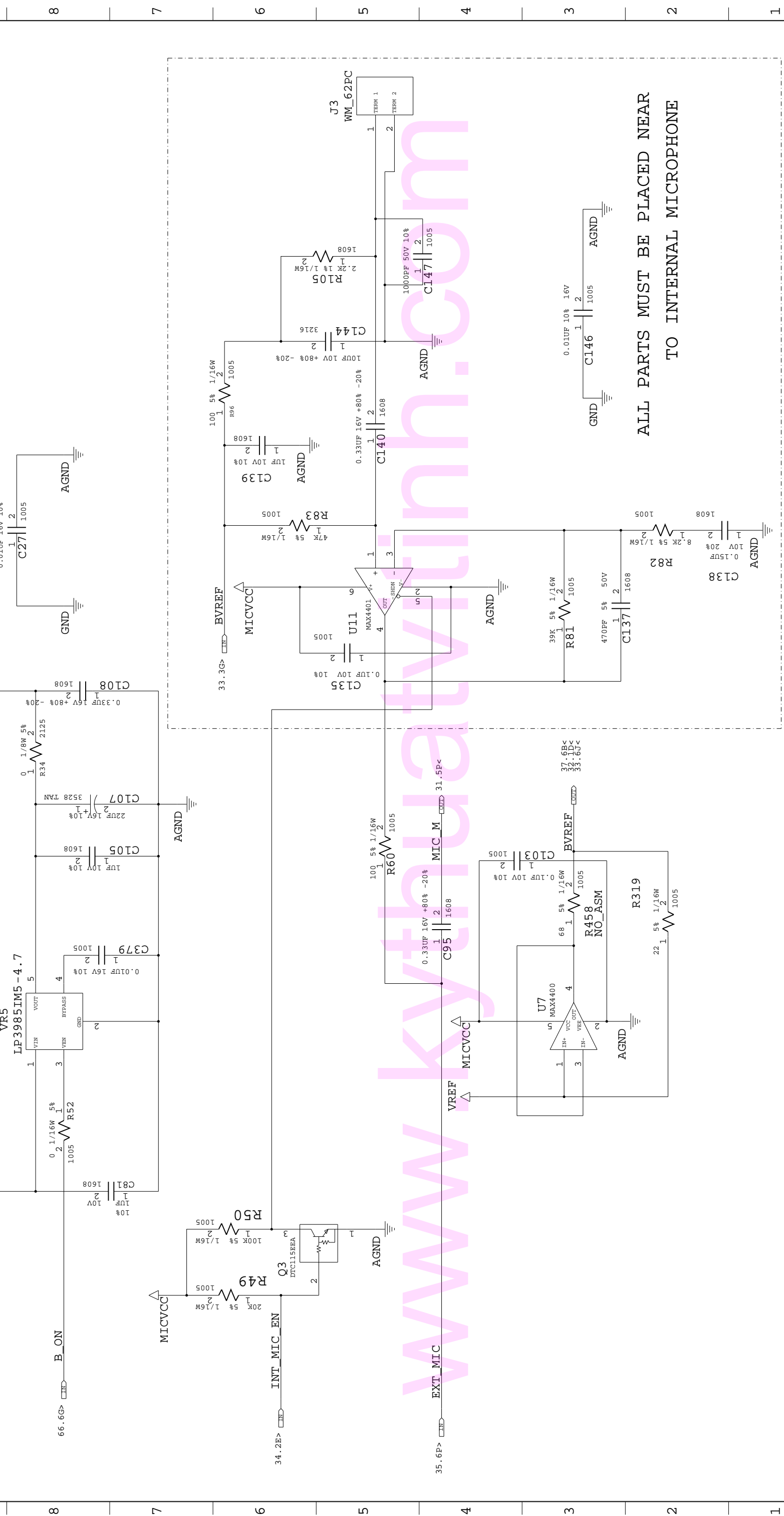


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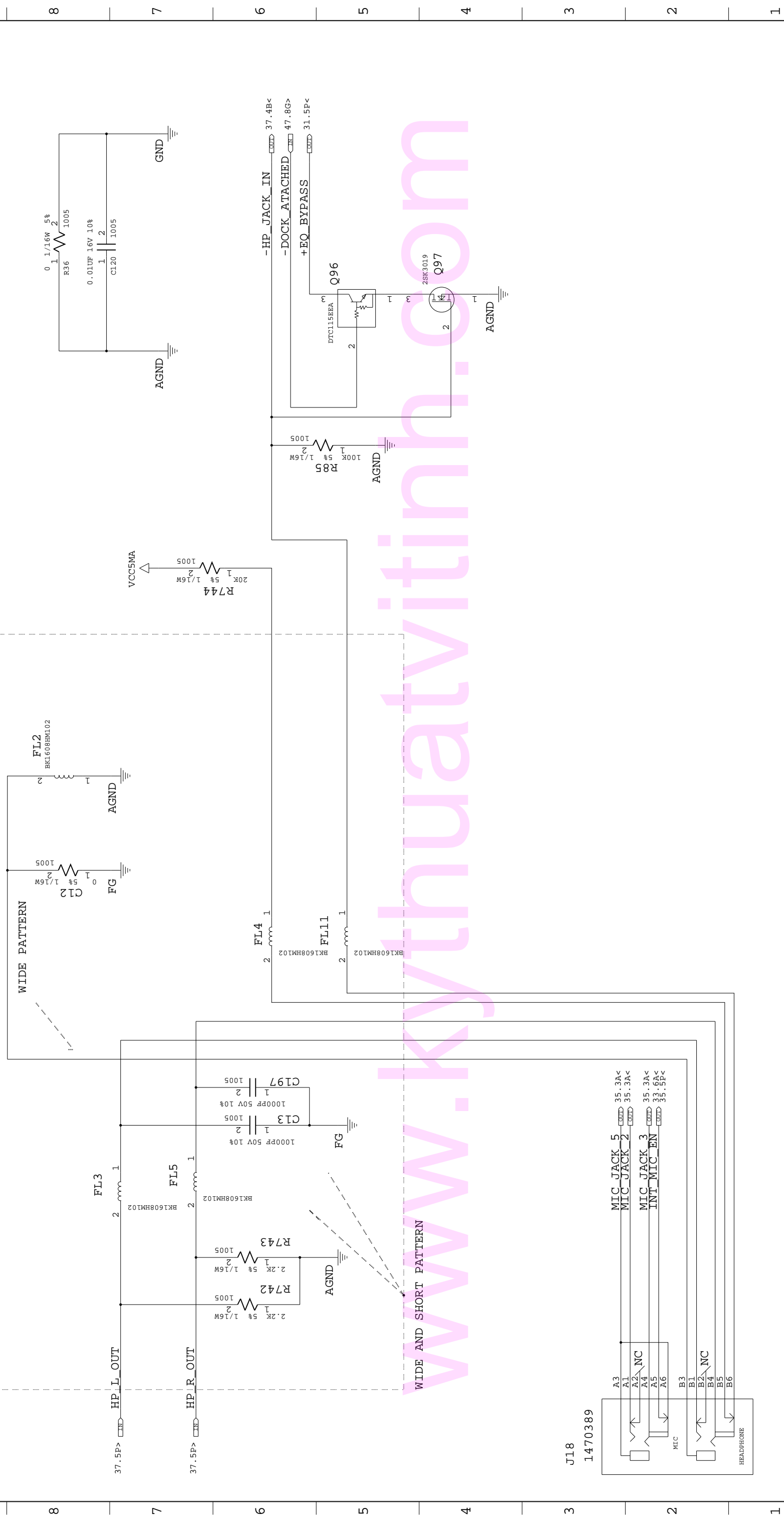
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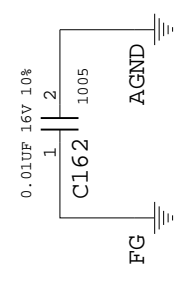
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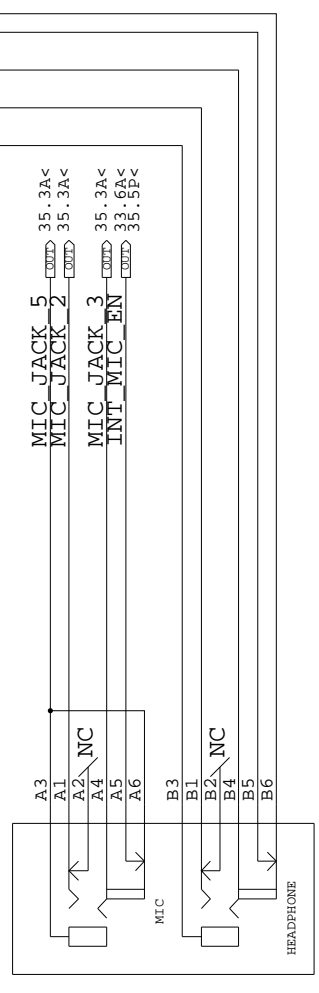
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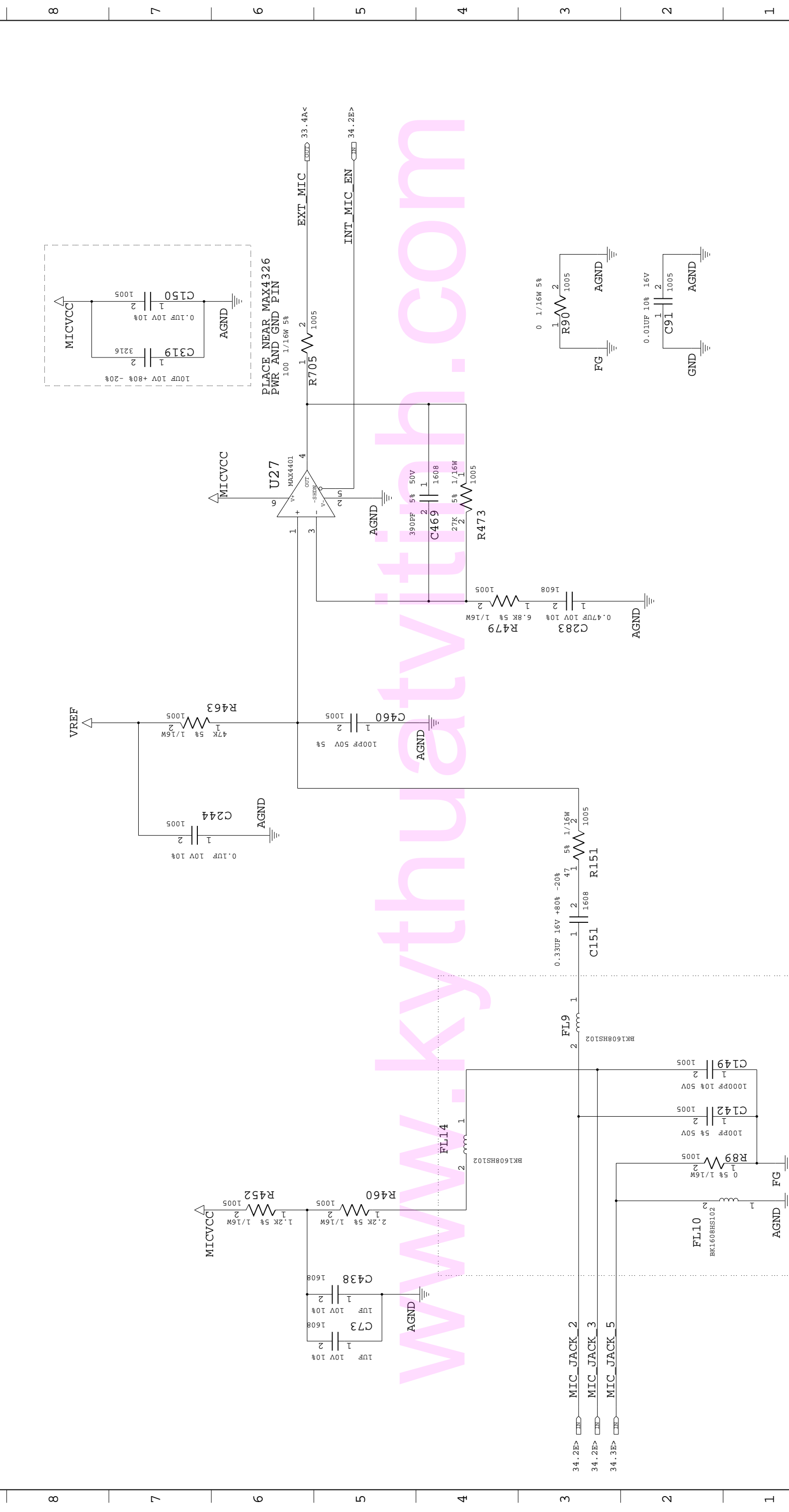


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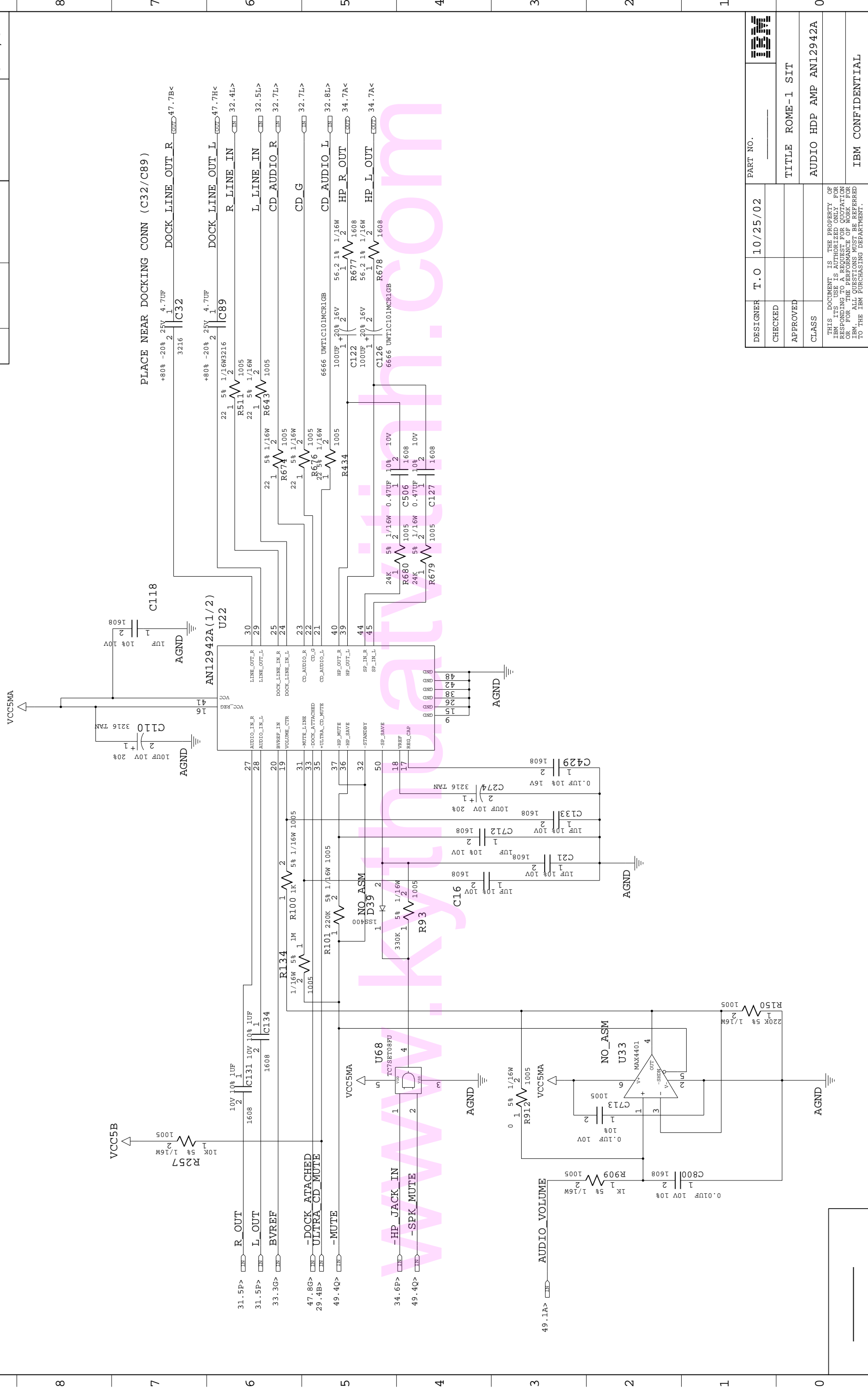
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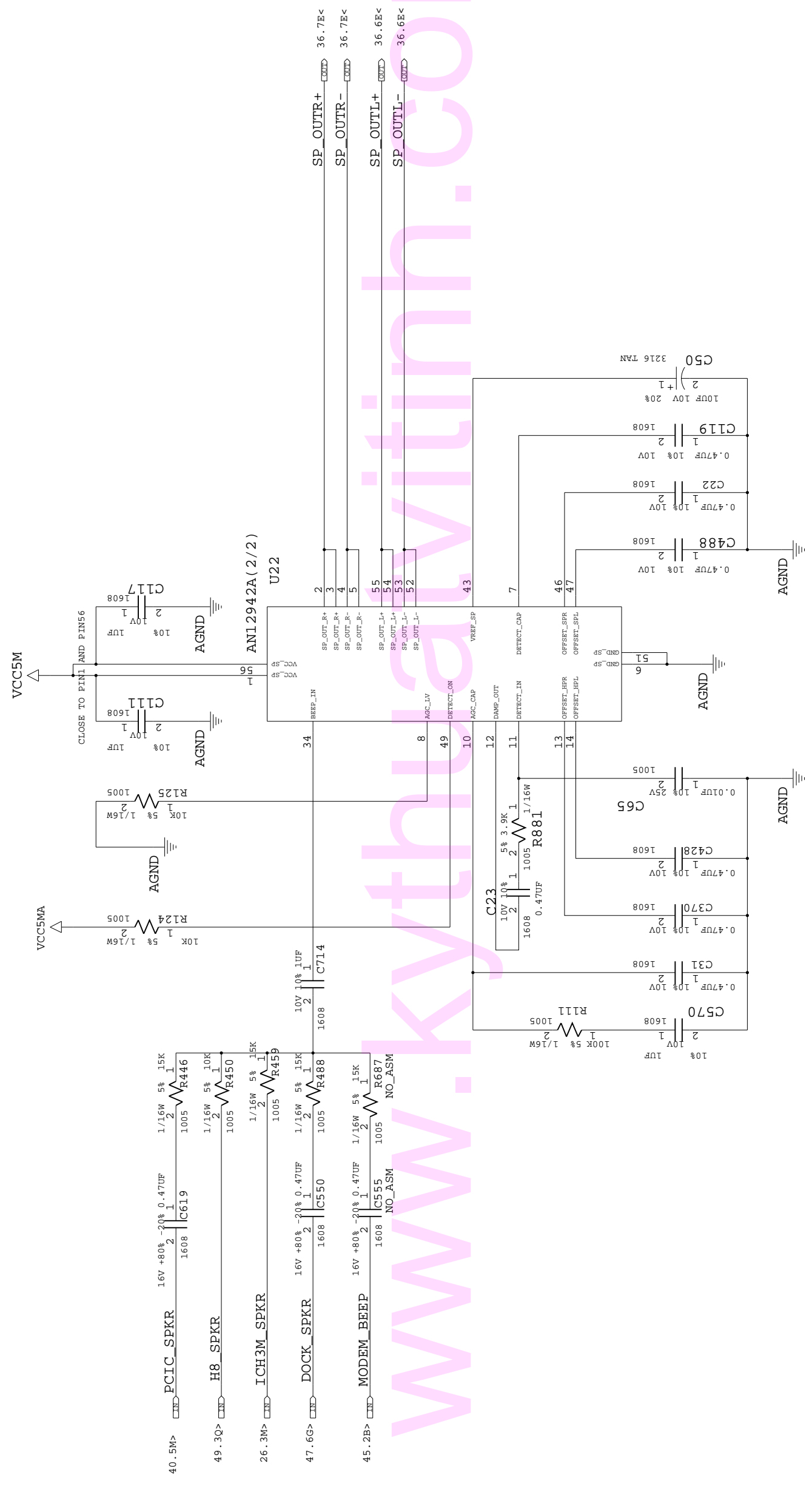


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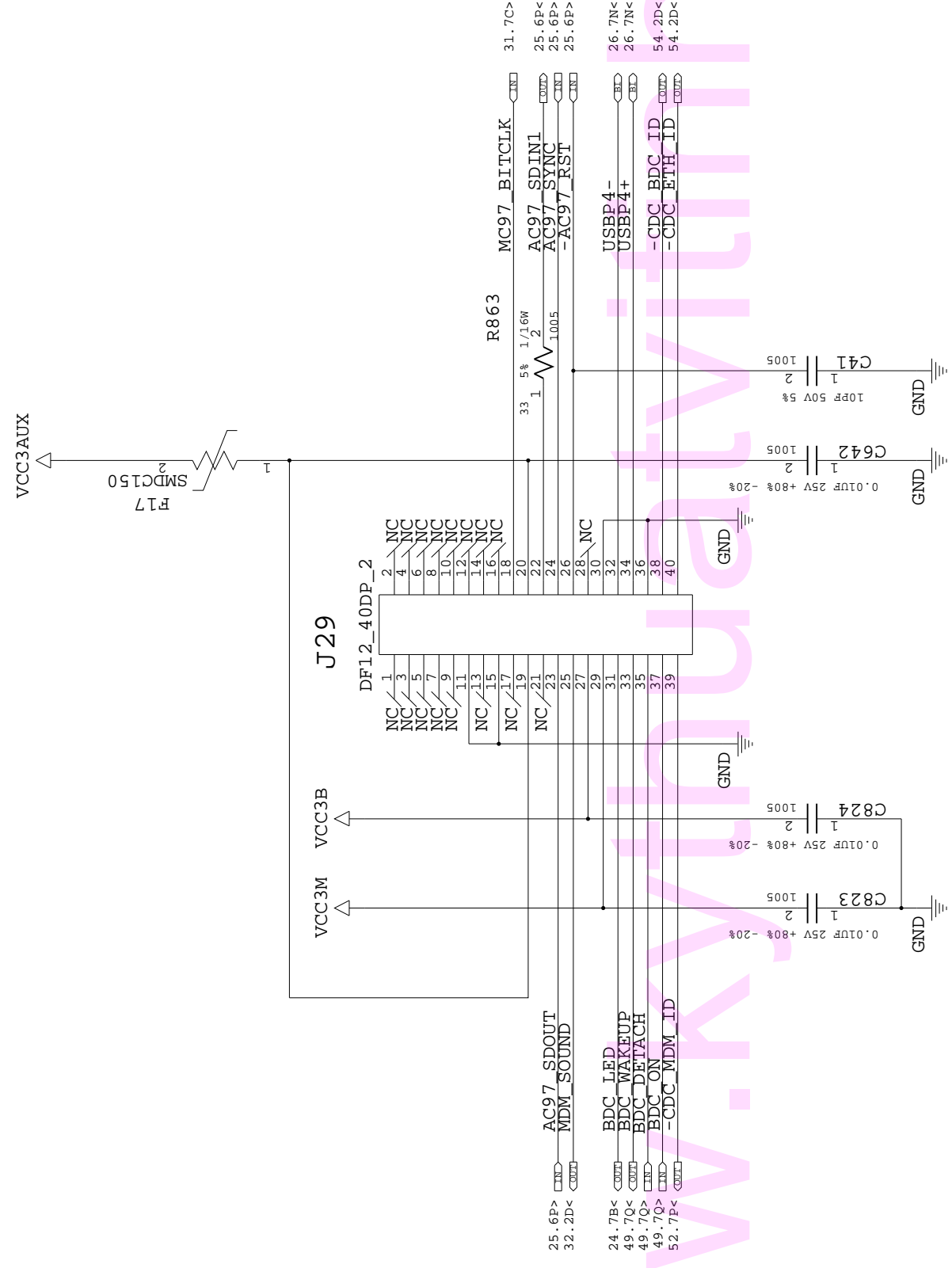


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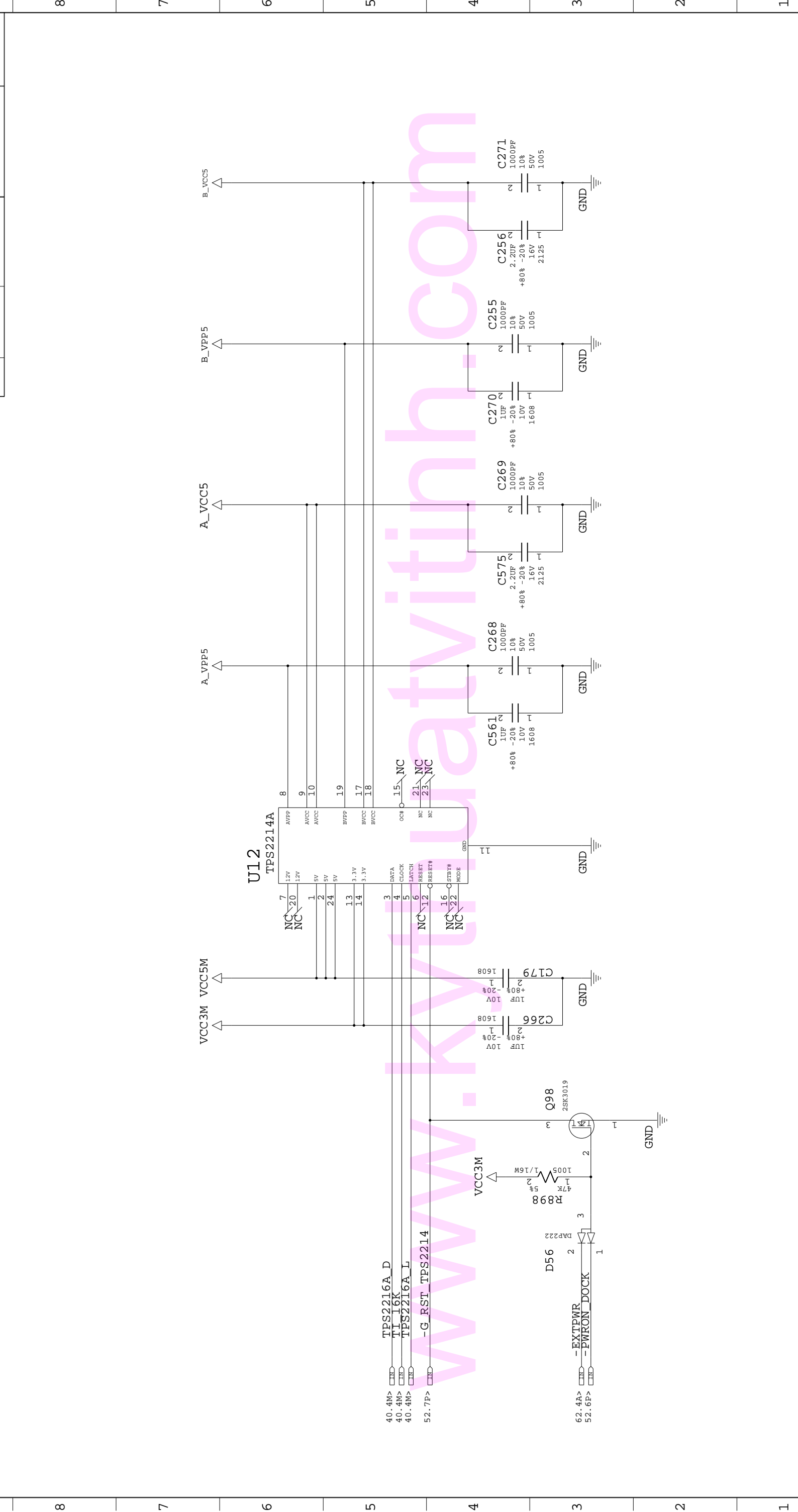
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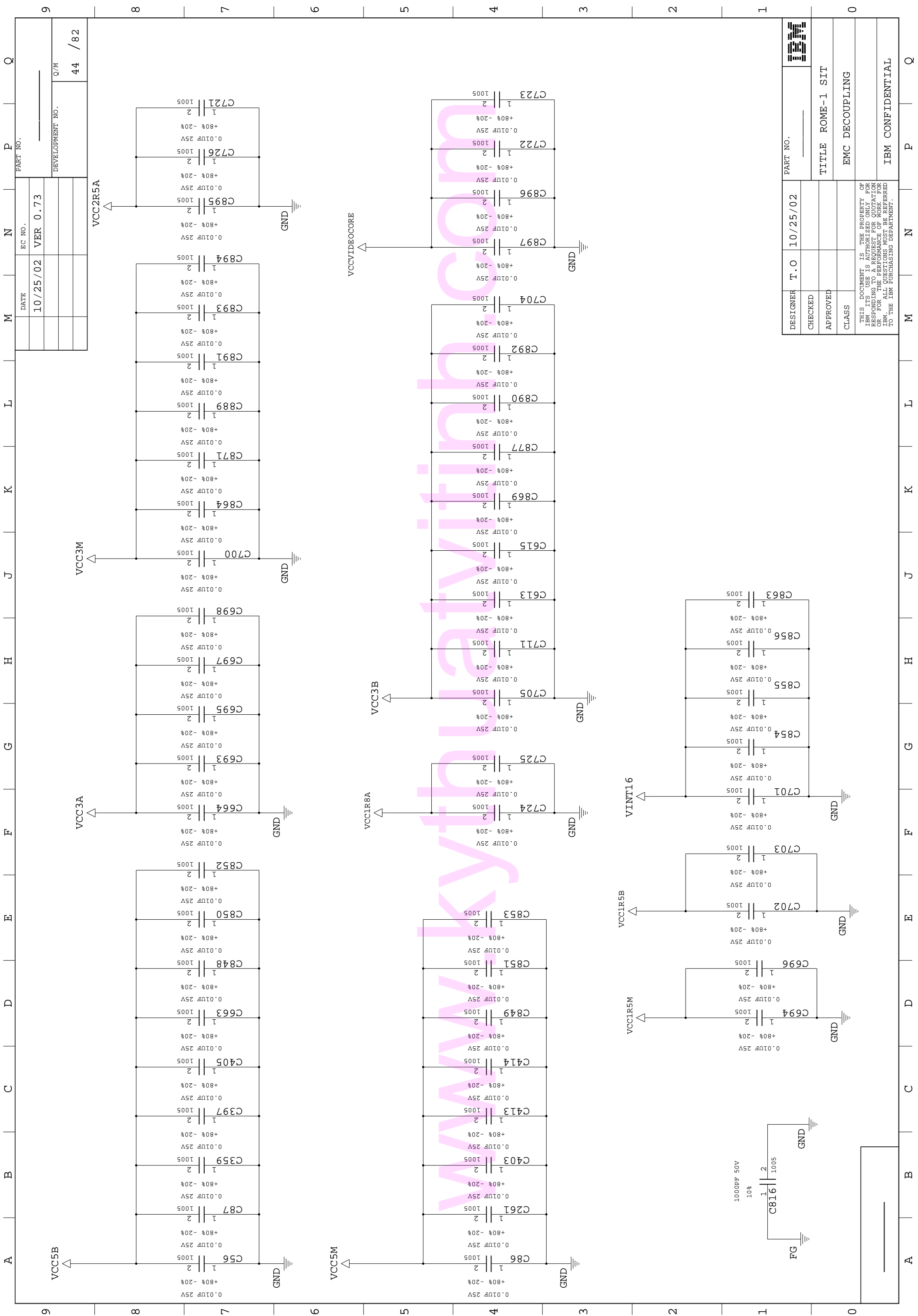


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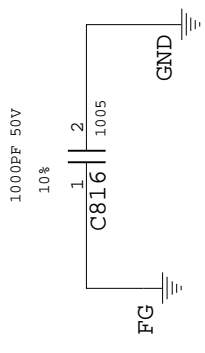


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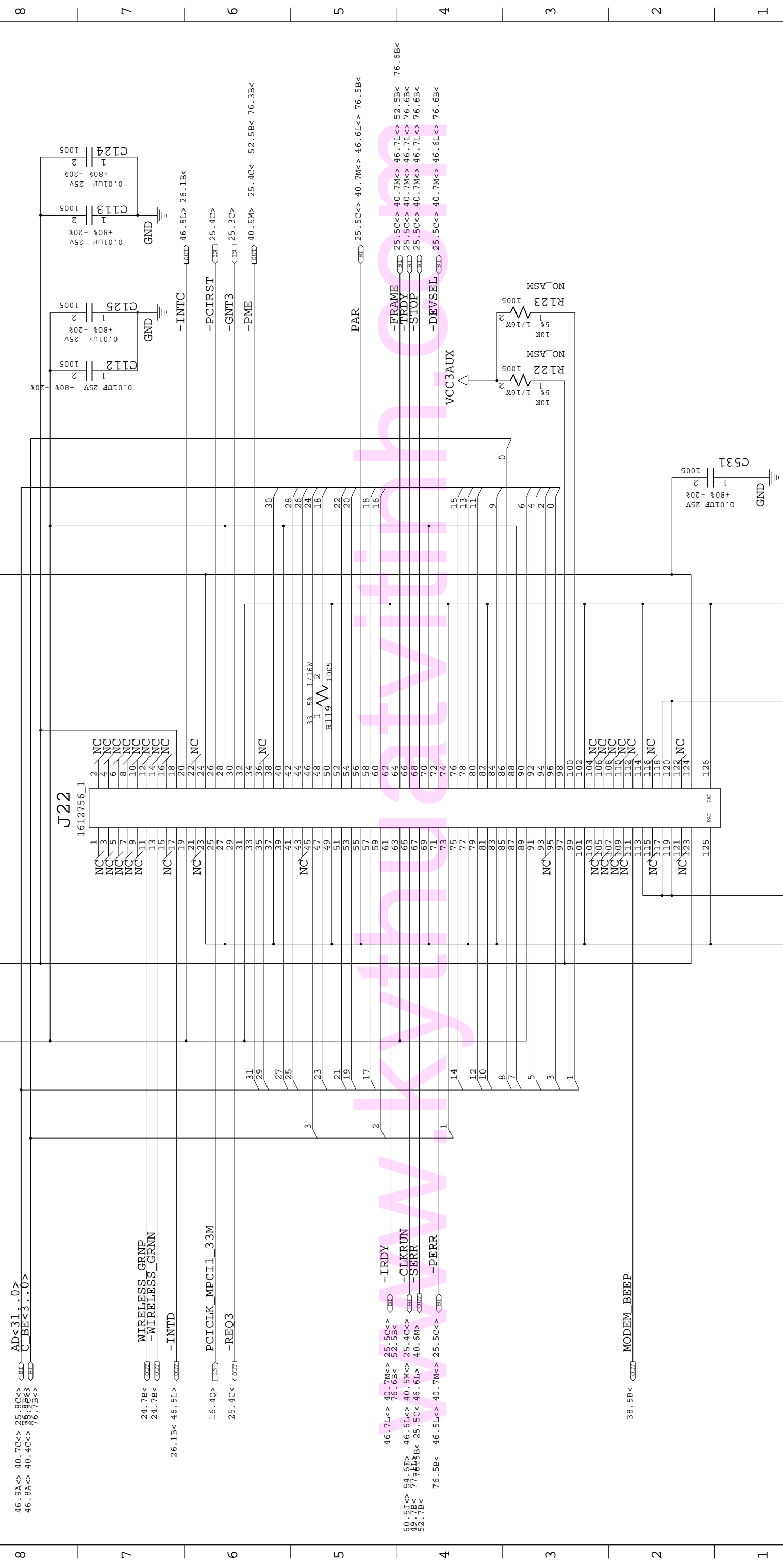
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# MINI PCI

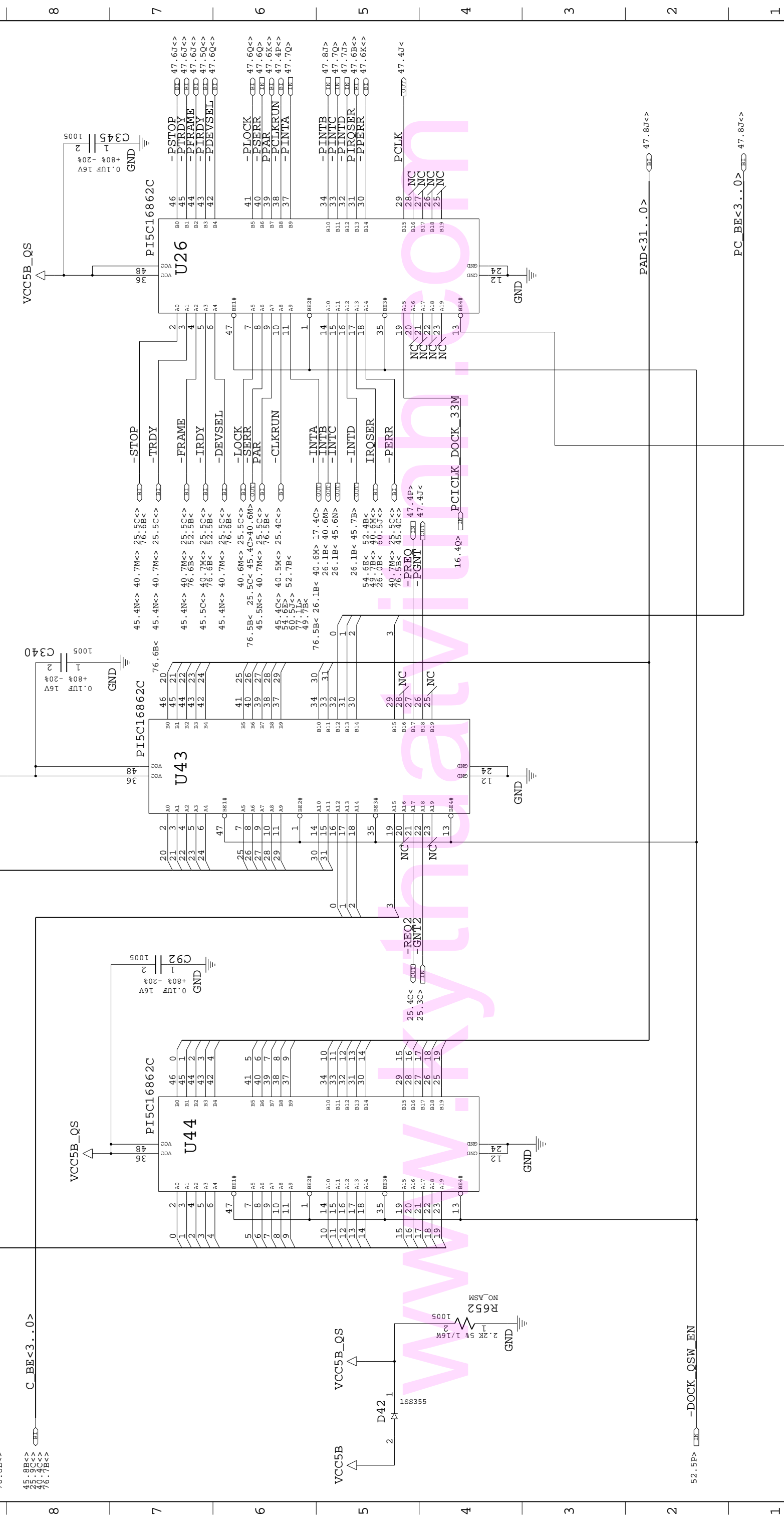


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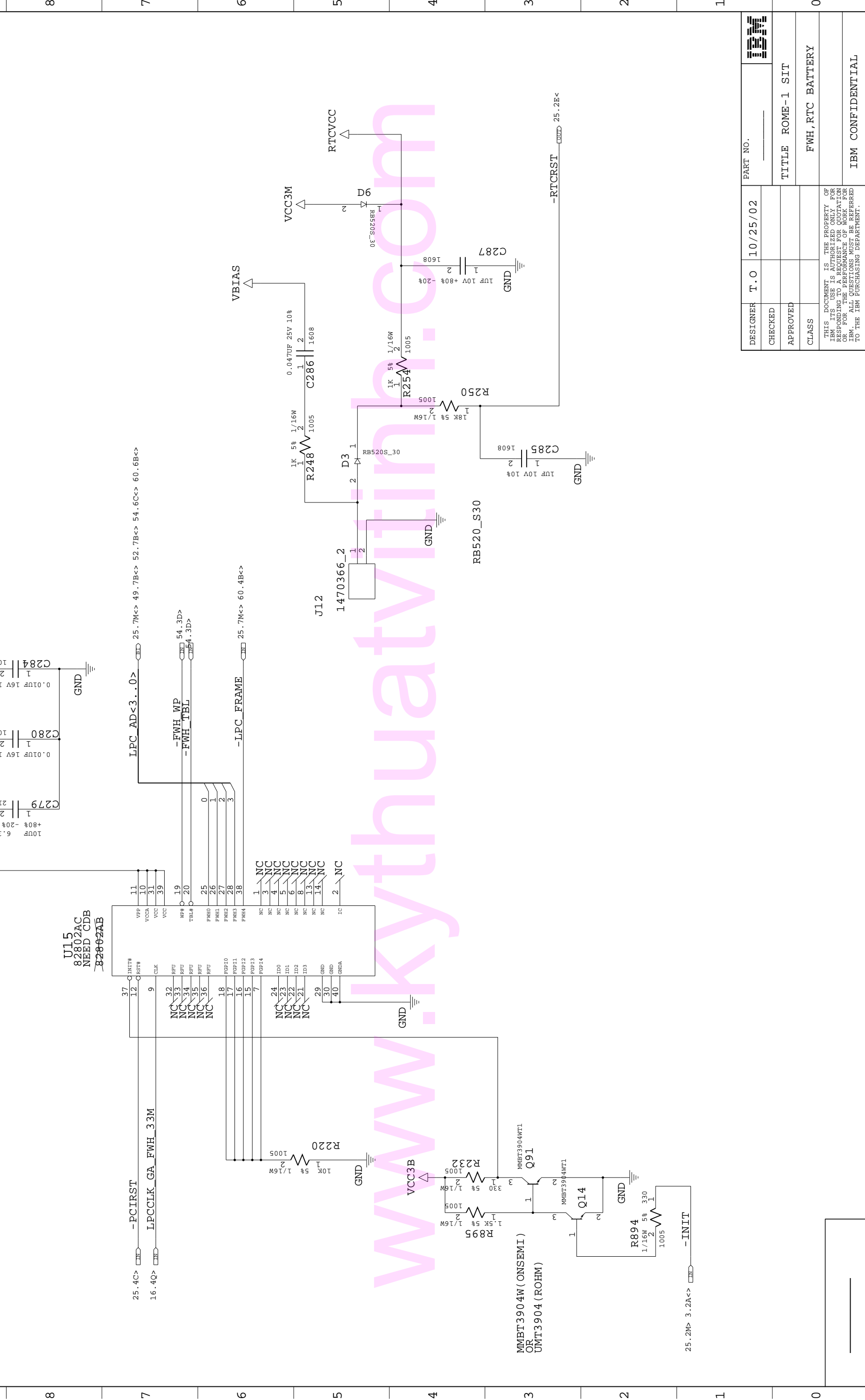
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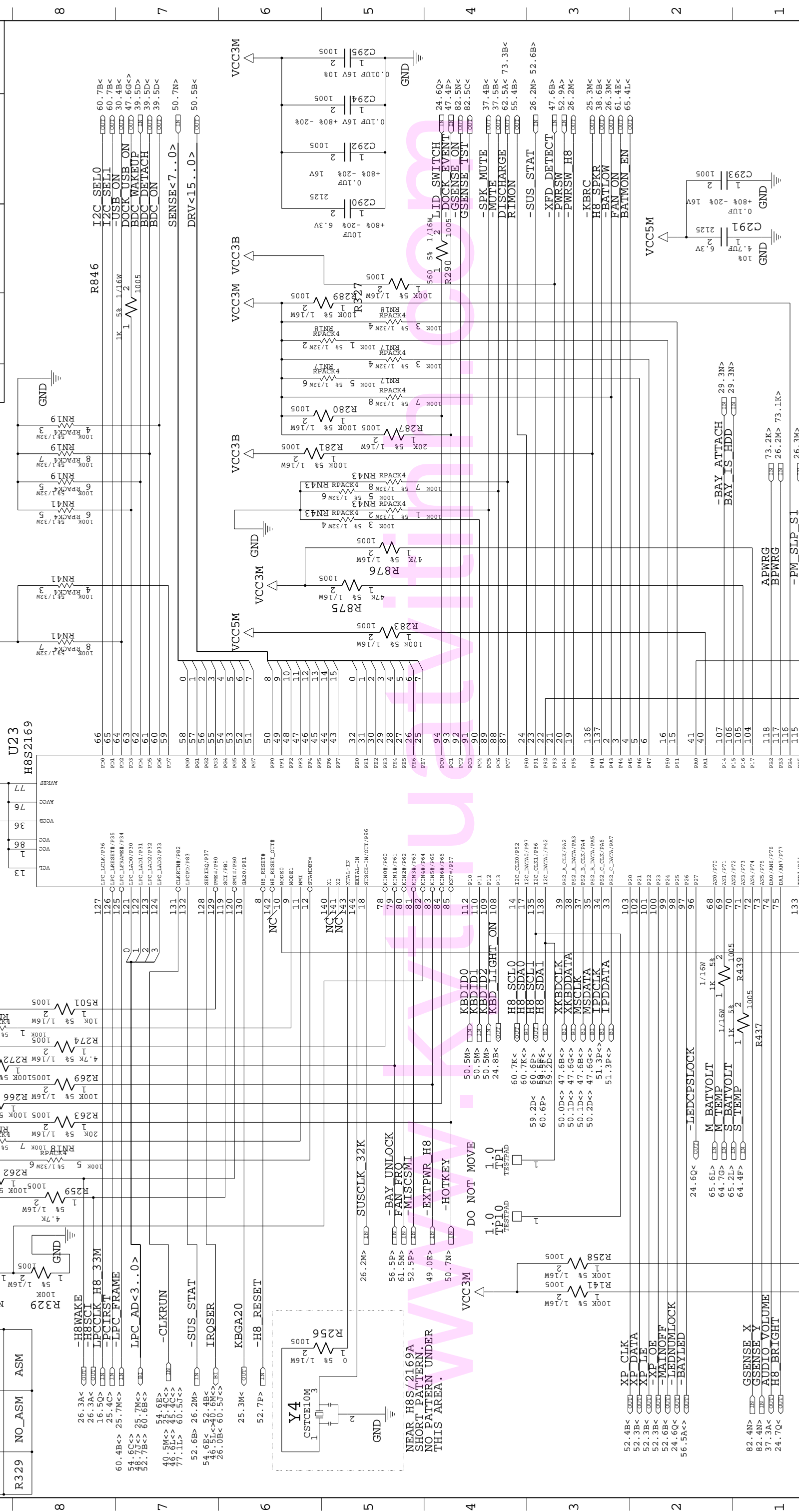


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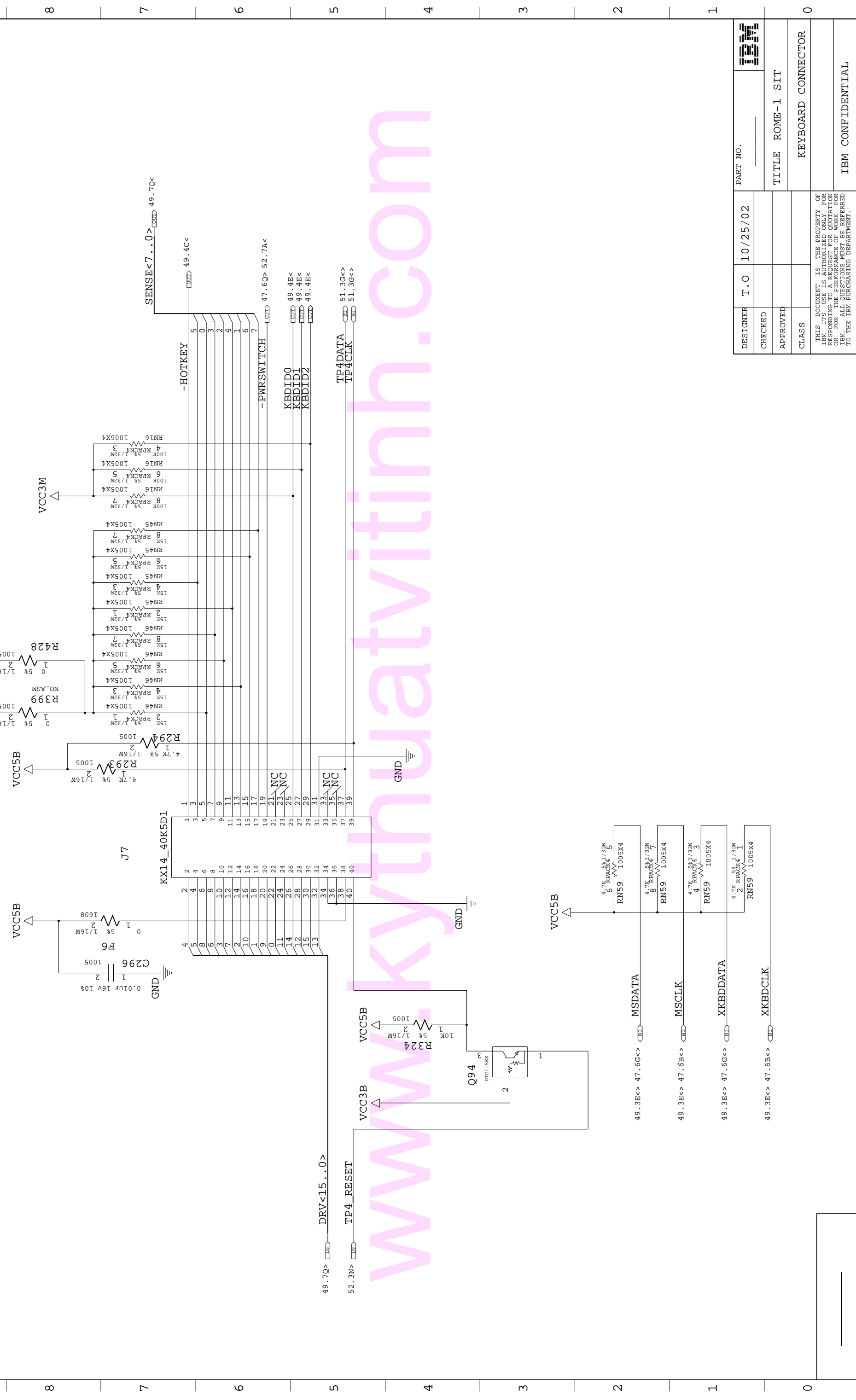


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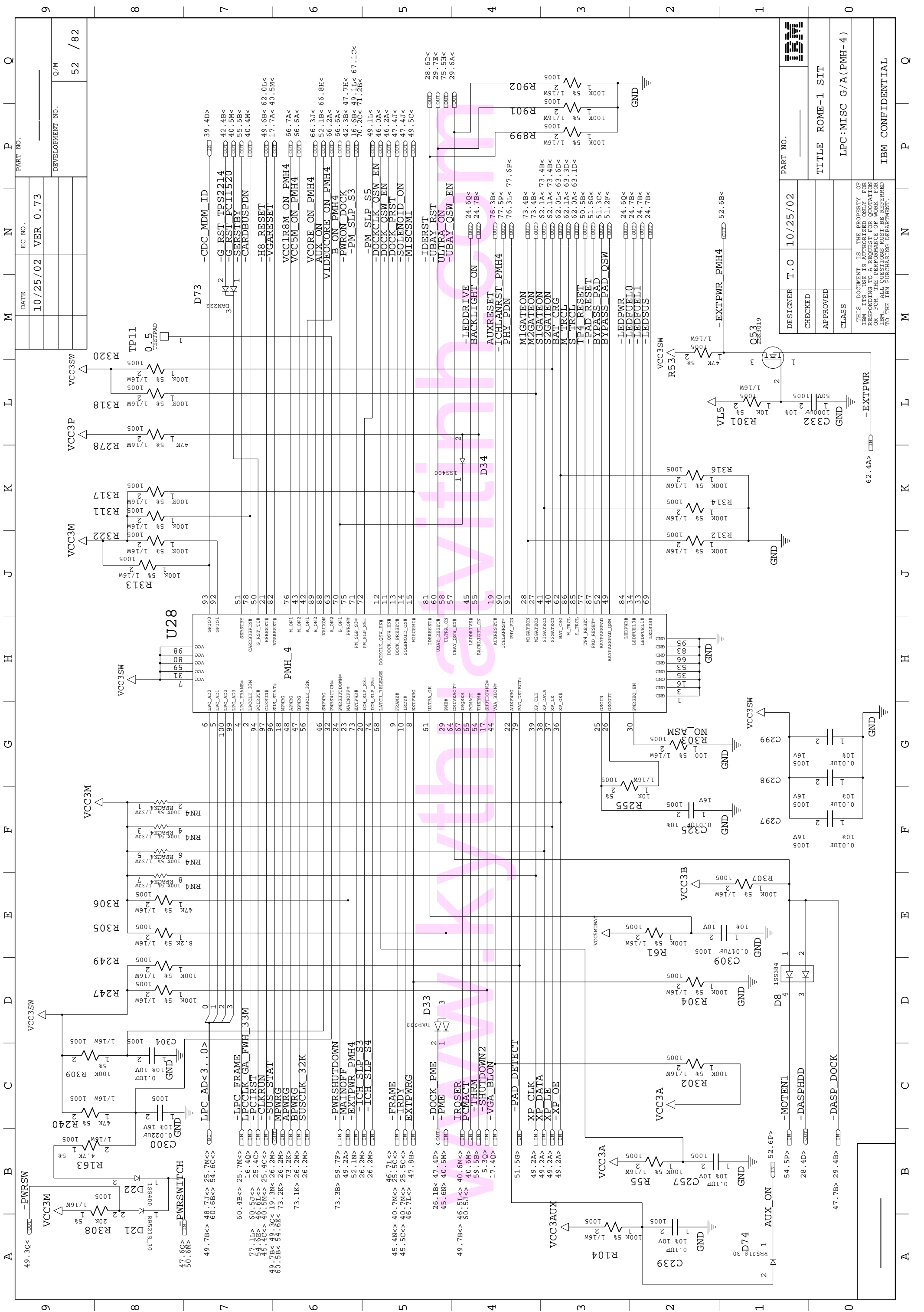
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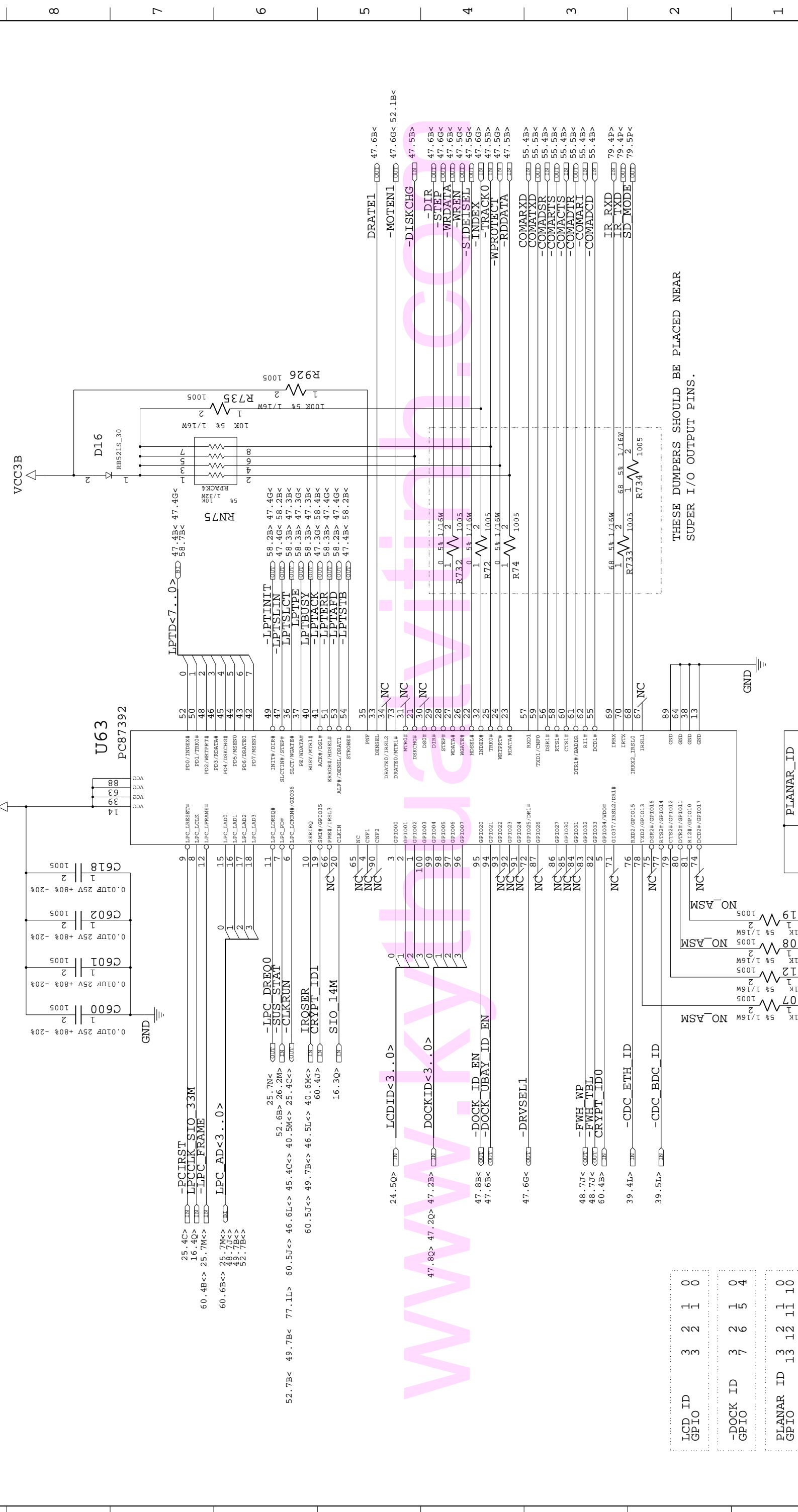
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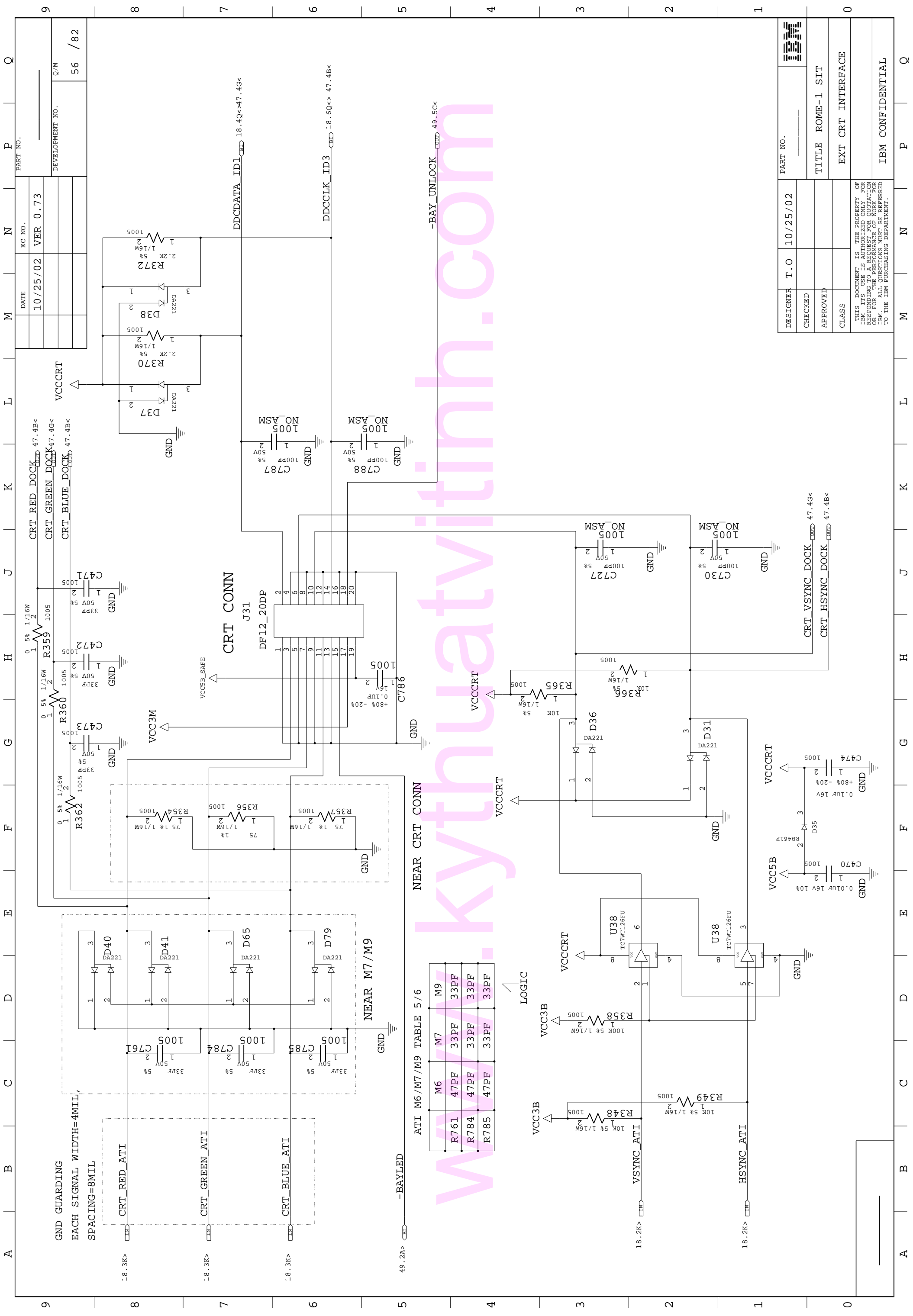
  

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ATI M6/M7/M9 TABLE 5/6

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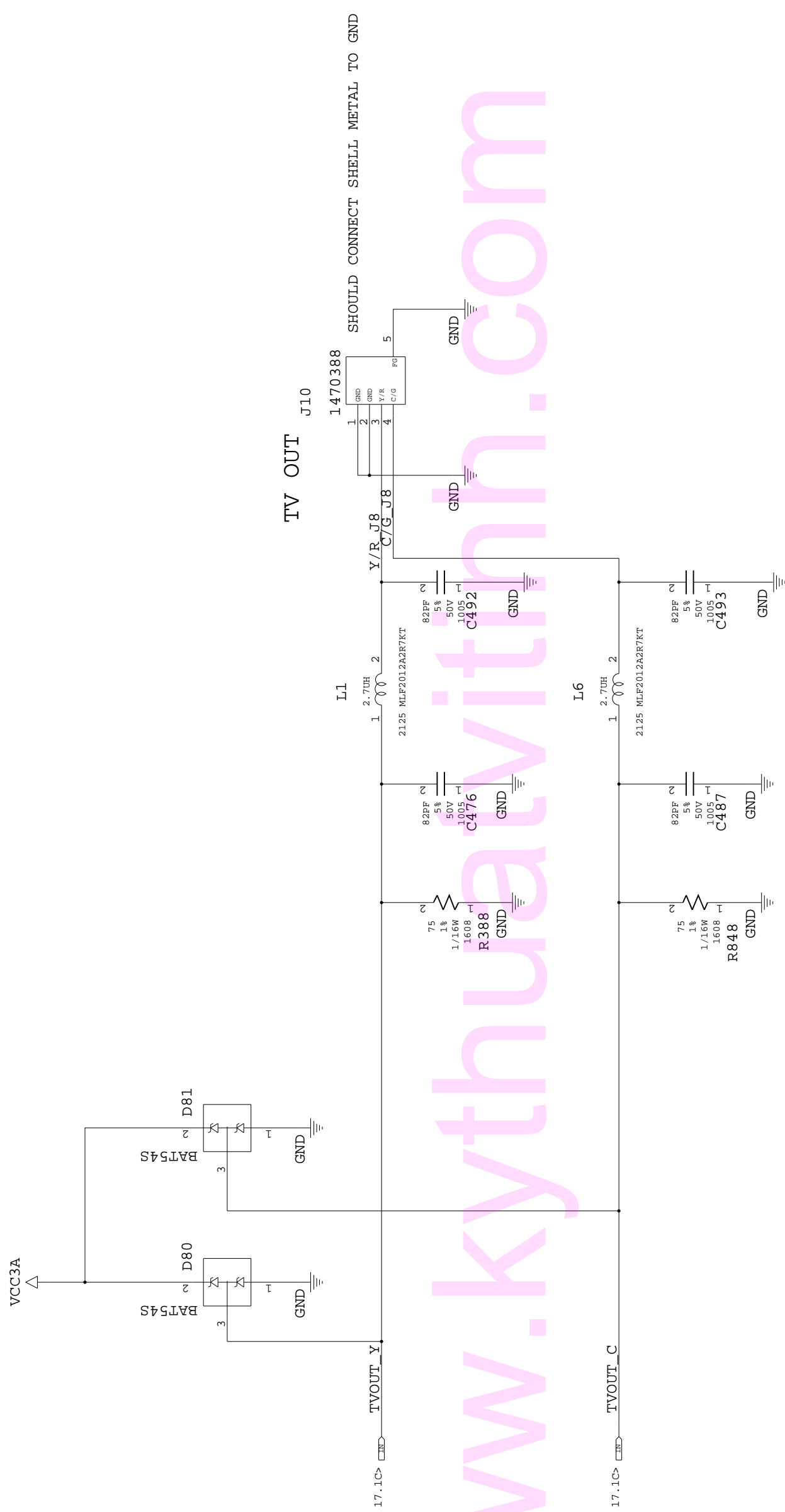
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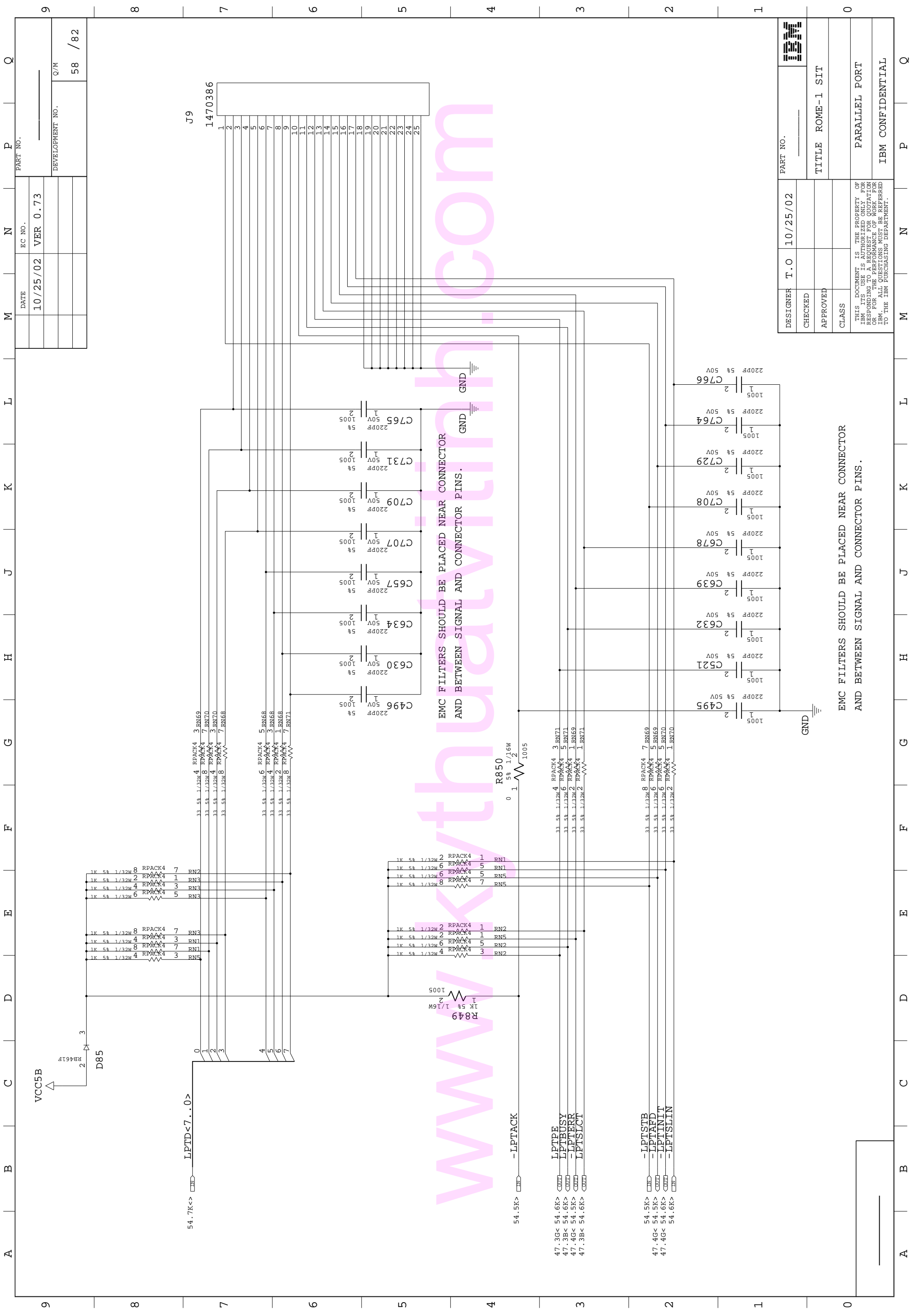


NEAR TO CONNECTOR(J11)

GND GUARDING  
WIDTH:  
MORE THAN 8 MIL

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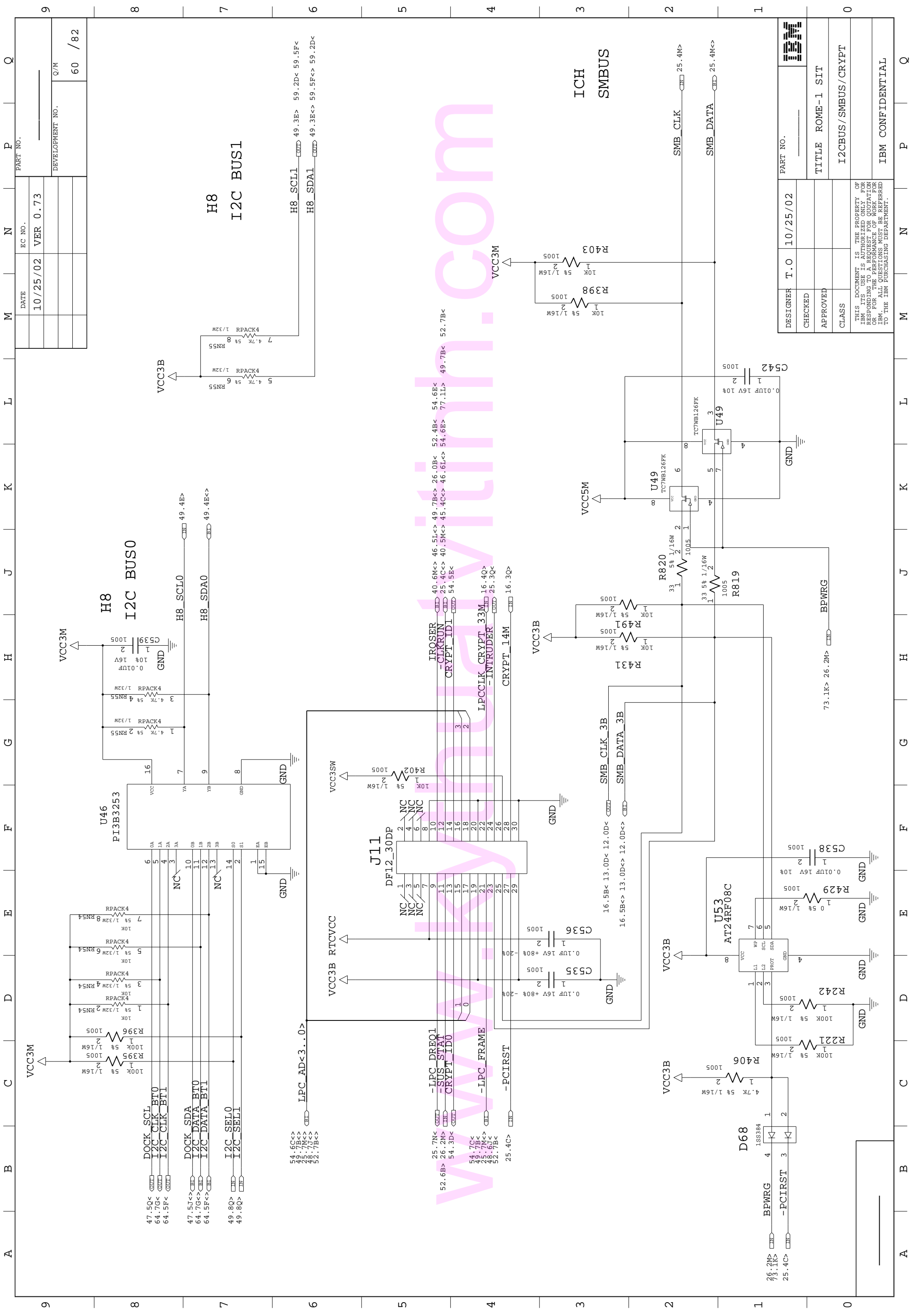
EMC FILTERS SHOULD BE PLACED NEAR CONNECTOR AND BETWEEN SIGNAL AND CONNECTOR PINS.

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A B C D E F G H J K L M N P Q

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DATE	EC NO.	PART NO.
10/25/02	VER 0.73	
		DEVELOPMENT NO.
		60 / 82

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I2C BUS1

H8\_SCL1  
H8\_SDA1

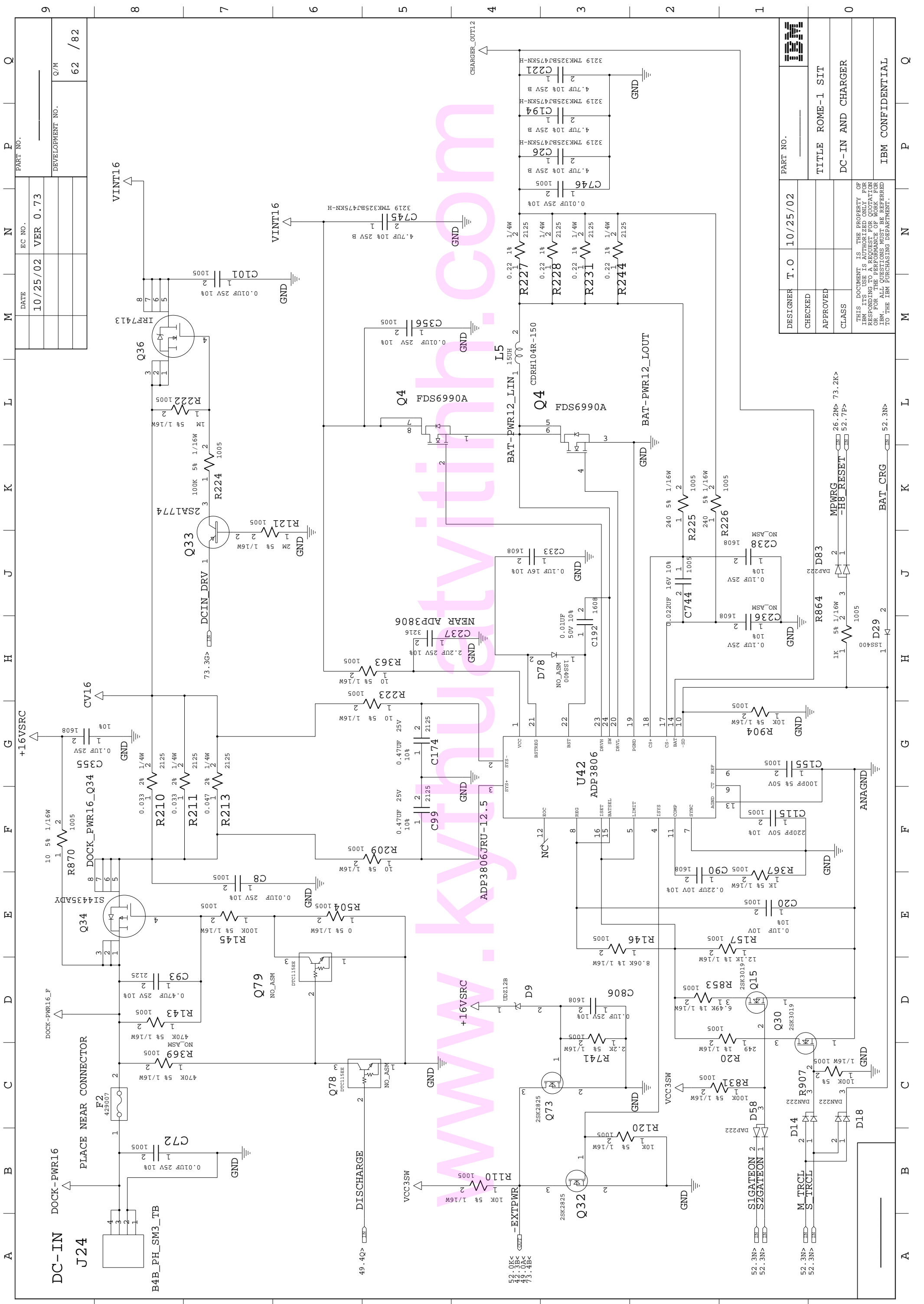
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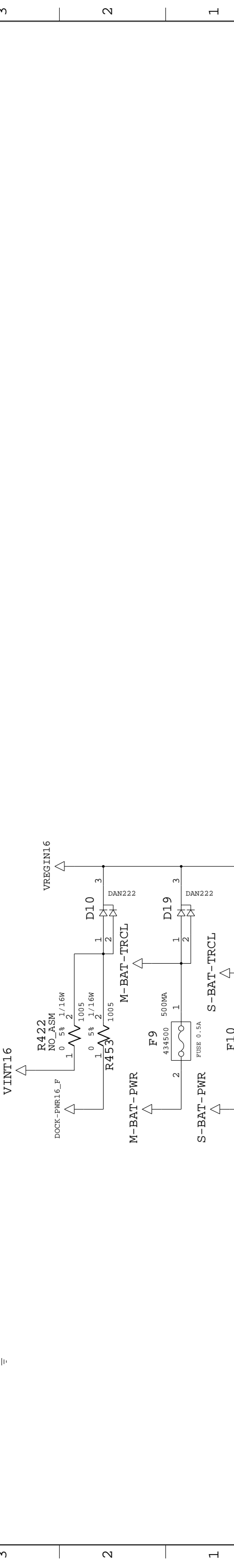
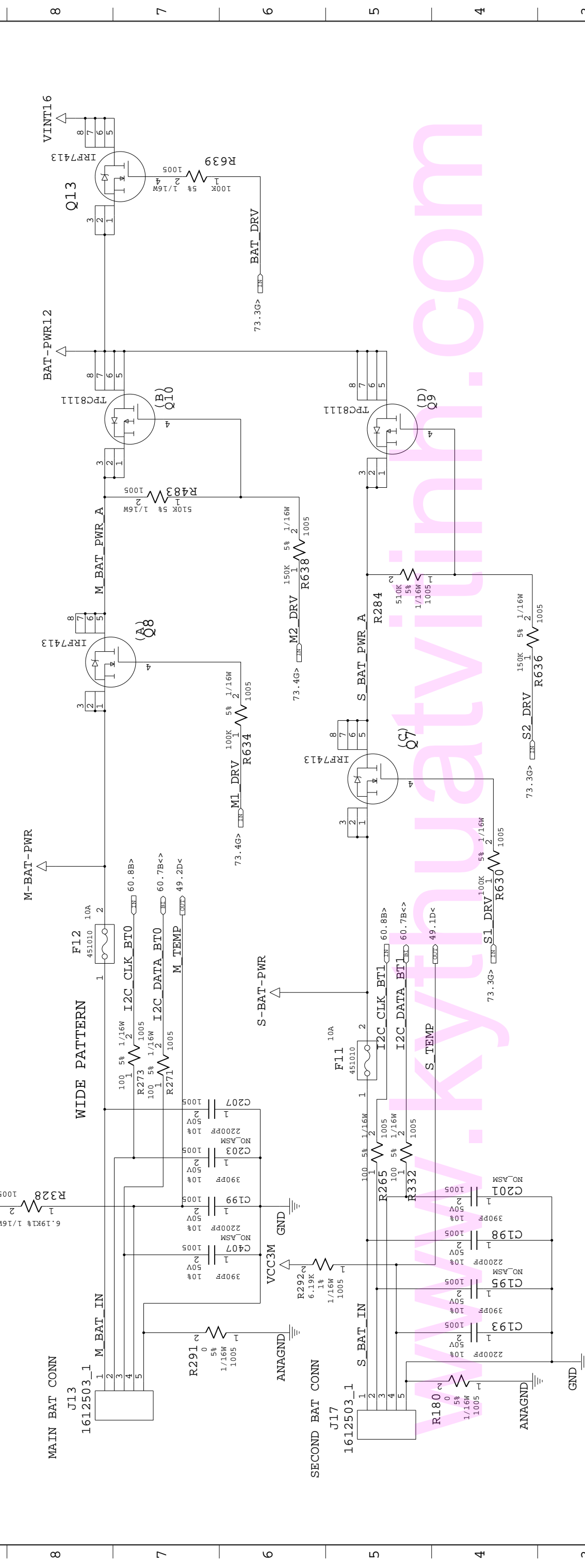
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MPWRG -H8 RESET 26.2M> 73.2K<  
 BAT\_CRG 52.3N>

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DATE	10/25/02	EC NO.	VER 0.73	PART NO.	
DEVELOPMENT NO.					
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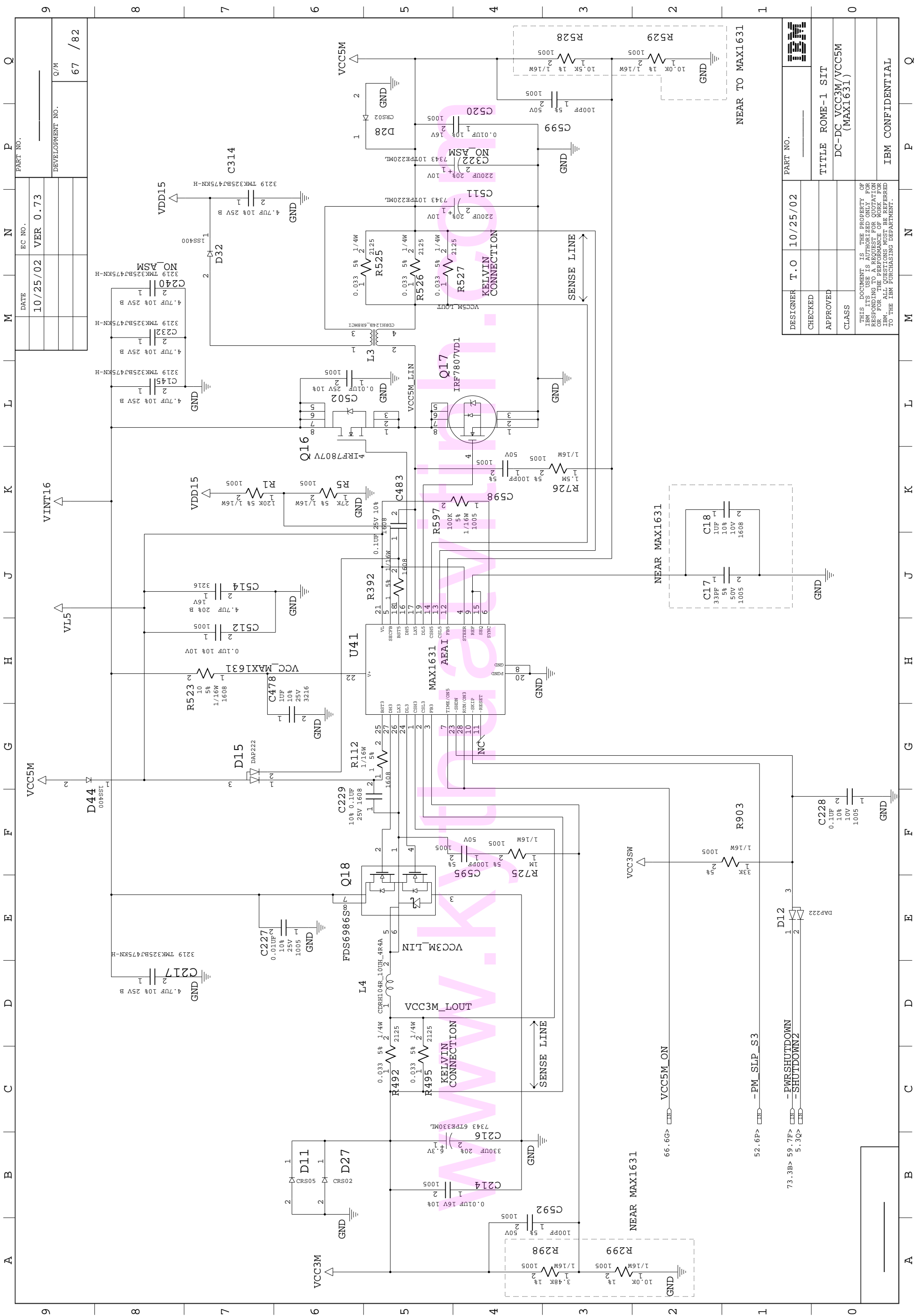


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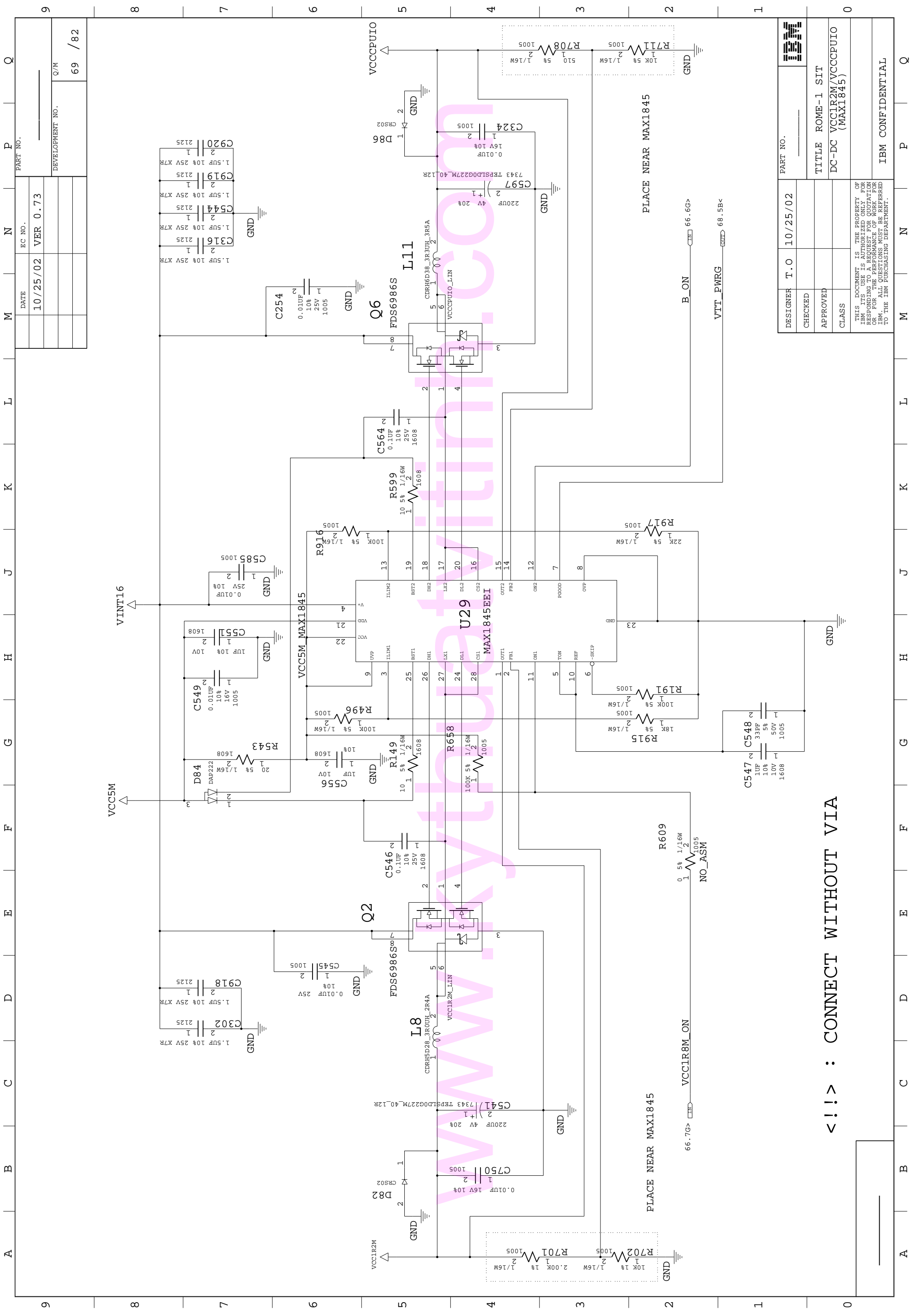
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5.3Q>

52.6P> -PM\_SLP\_S3

66.6G> VCC5M\_ON

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DEVELOPMENT NO.		67 / 82			





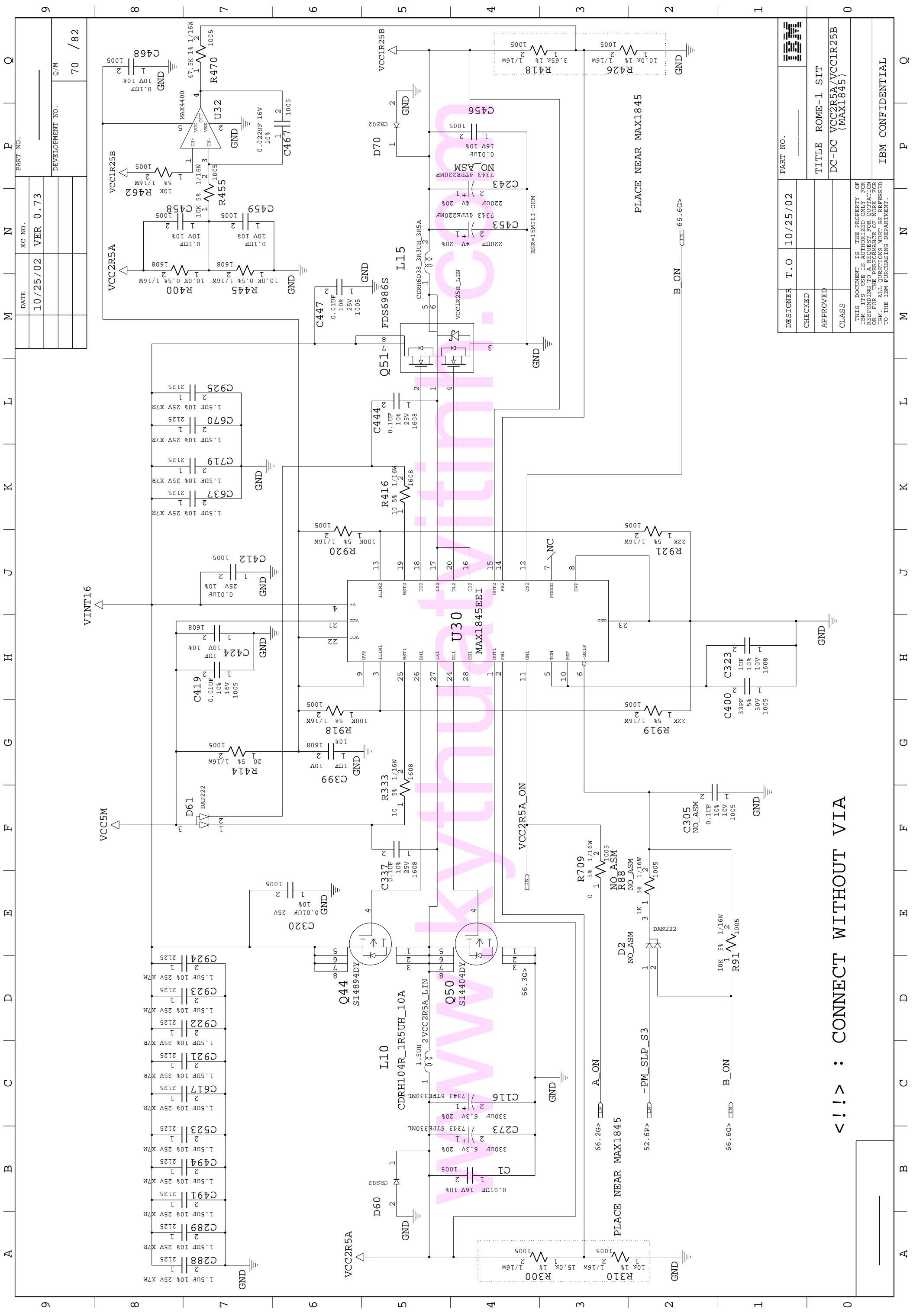
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<!!> : CONNECT WITHOUT VIA

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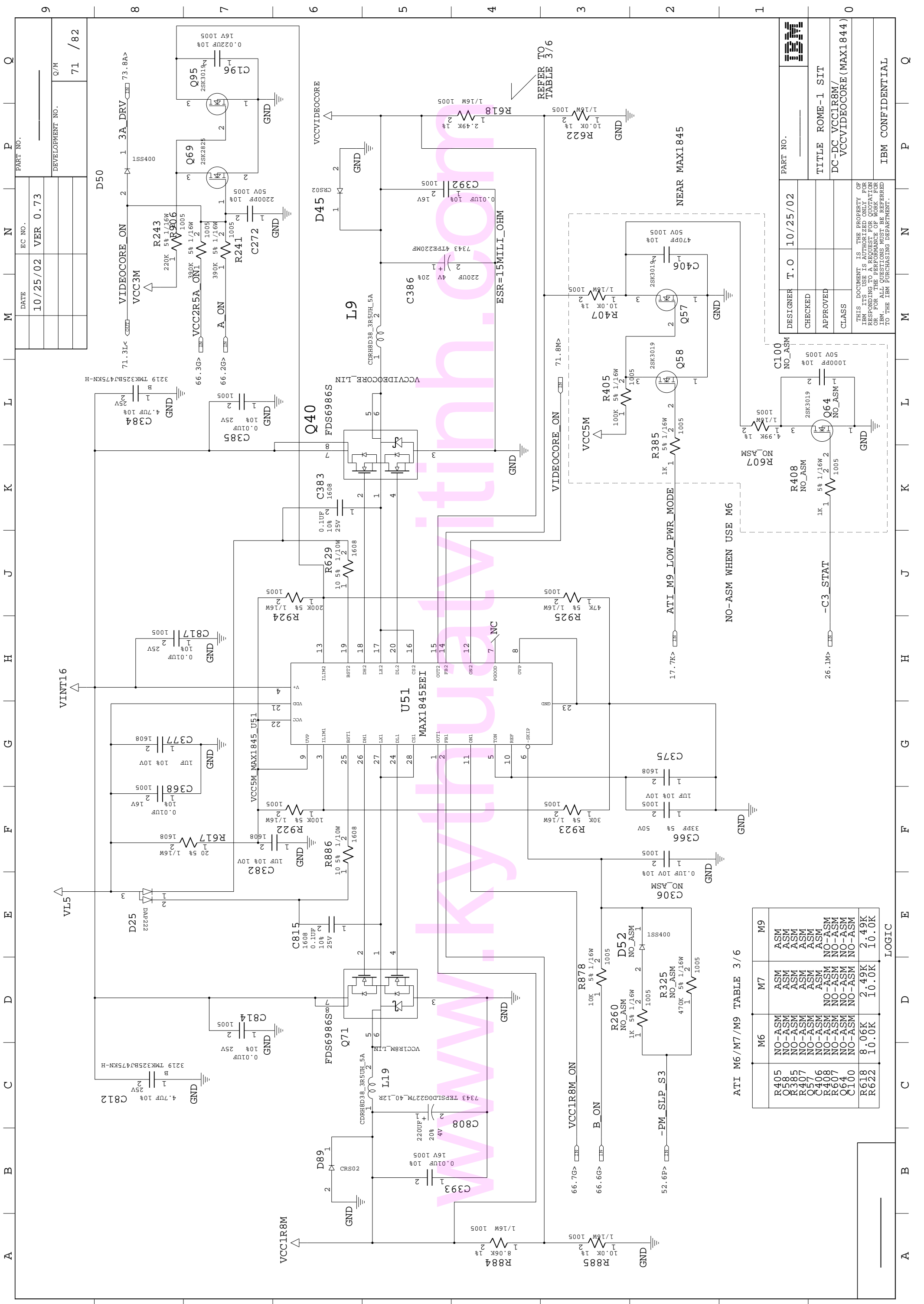
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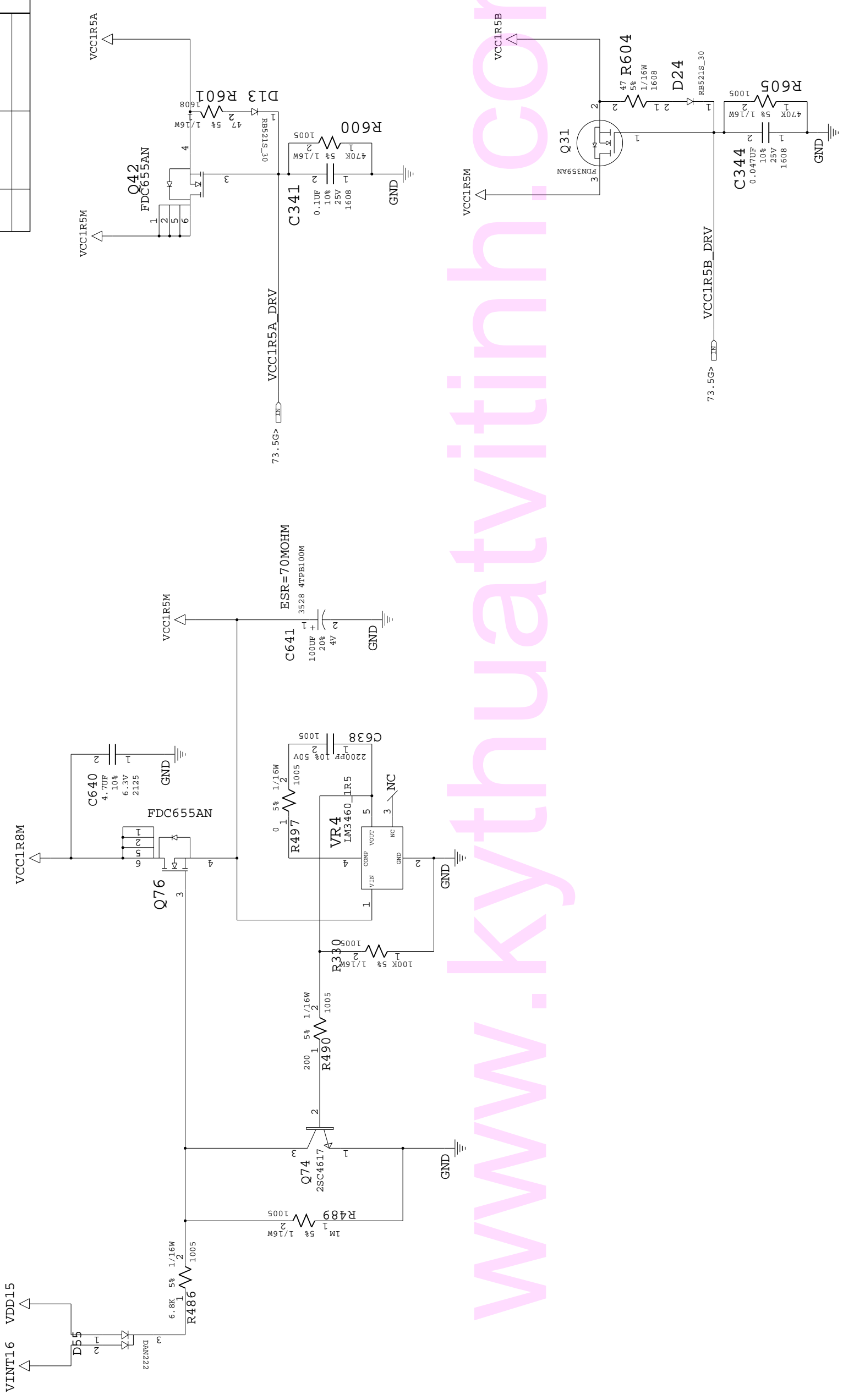
DATE	10/25/02	EC NO.	VER 0.73	PART NO.	
DEVELOPMENT NO.					
					71 / 82

ATI M6/M7/M9 TABLE 3/6

Component	M6	M7	M9	LOGIC
R405	NO-ASM	ASM	ASM	ASM
Q58	NO-ASM	ASM	ASM	ASM
R385	NO-ASM	ASM	ASM	ASM
R407	NO-ASM	ASM	ASM	ASM
Q406	NO-ASM	ASM	ASM	ASM
R408	NO-ASM	NO-ASM	NO-ASM	NO-ASM
R607	NO-ASM	NO-ASM	NO-ASM	NO-ASM
Q64	NO-ASM	NO-ASM	NO-ASM	NO-ASM
C100	NO-ASM	NO-ASM	NO-ASM	NO-ASM
R618	8.06K	2.49K	2.49K	2.49K
R622	10.0K	10.0K	10.0K	10.0K

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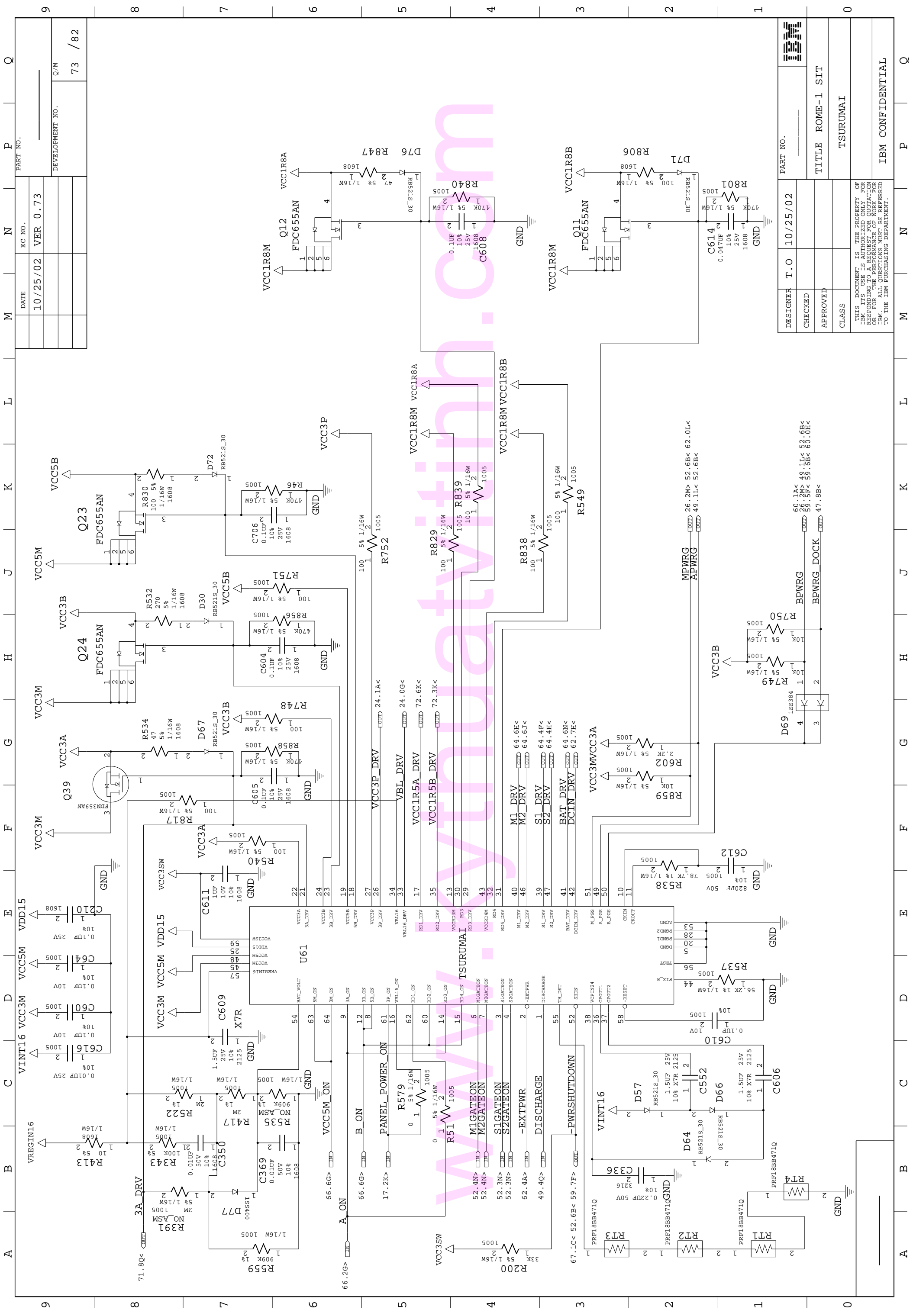


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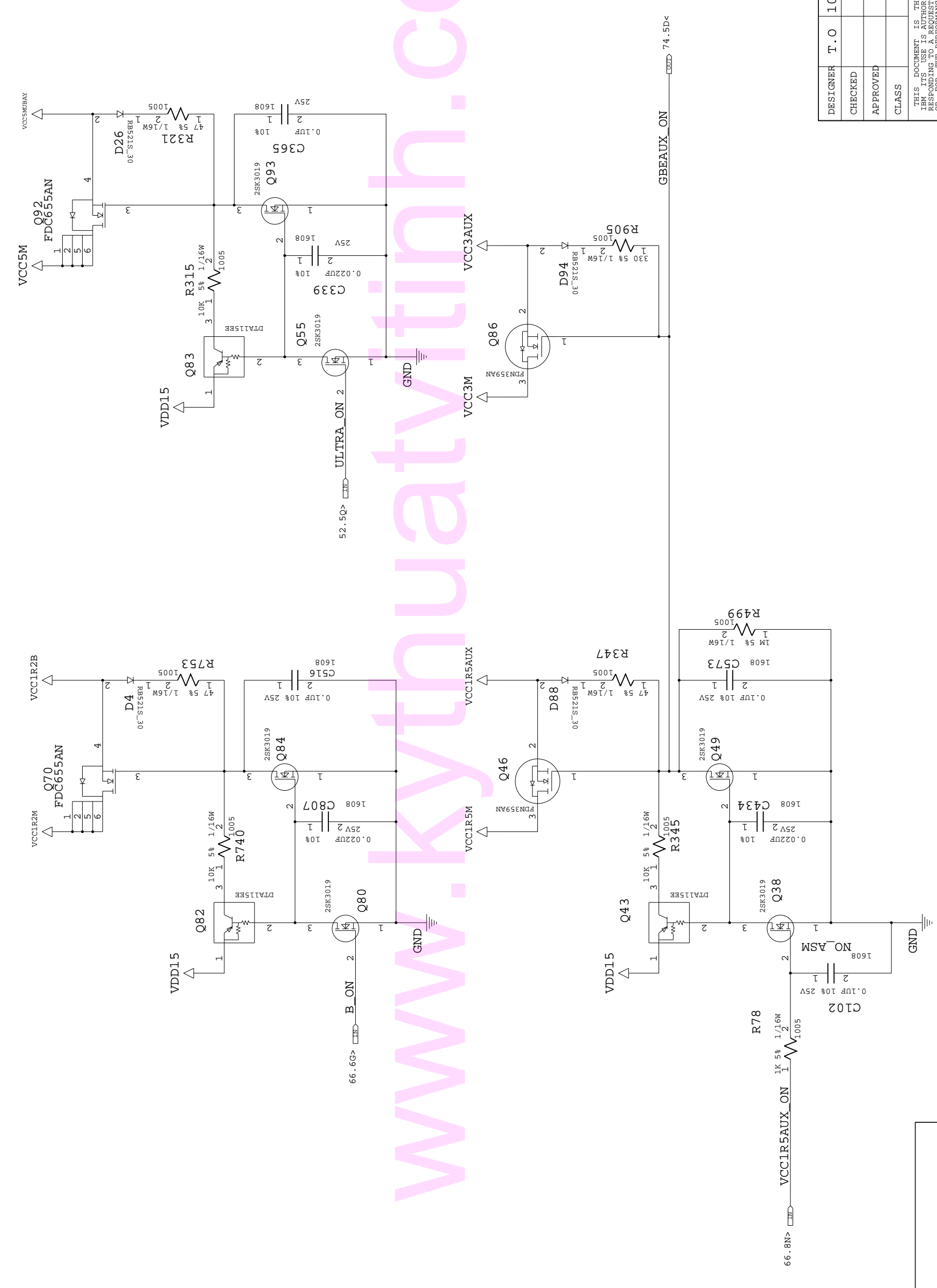


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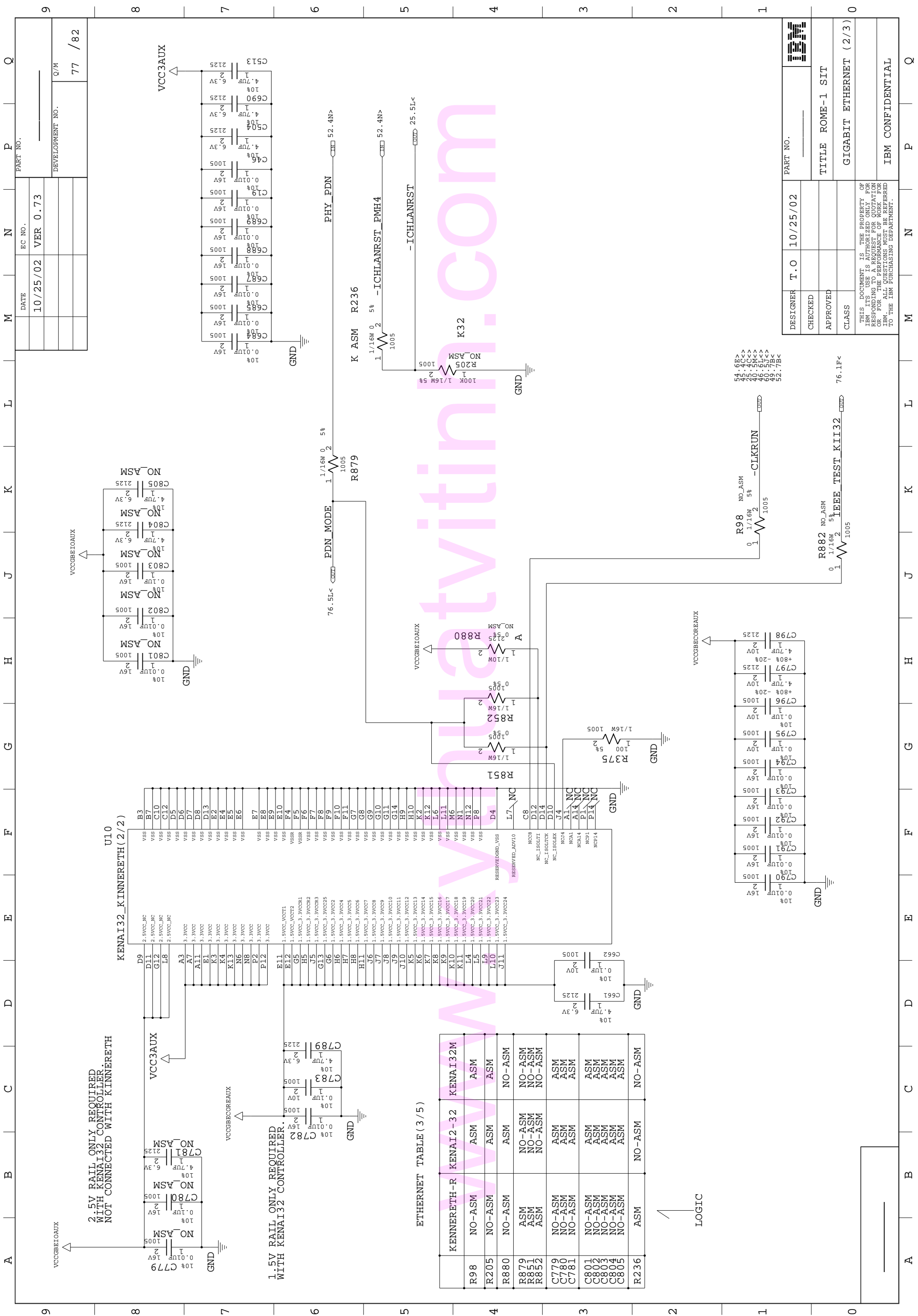
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1.5V RAIL ONLY REQUIRED WITH KENAI32 CONTROLLER.

ETHERNET TABLE (3/5)

KENNERETH-R	KENAI2-32	KENAI32M
R98	NO-ASM	ASM
R205	NO-ASM	ASM
R880	NO-ASM	NO-ASM
R879	ASM	NO-ASM
R851	NO-ASM	NO-ASM
R852	NO-ASM	NO-ASM
C779	NO-ASM	ASM
C780	NO-ASM	ASM
C781	NO-ASM	ASM
C801	NO-ASM	ASM
C802	NO-ASM	ASM
C803	NO-ASM	ASM
C804	NO-ASM	ASM
C805	NO-ASM	ASM
R236	ASM	NO-ASM

LOGIC

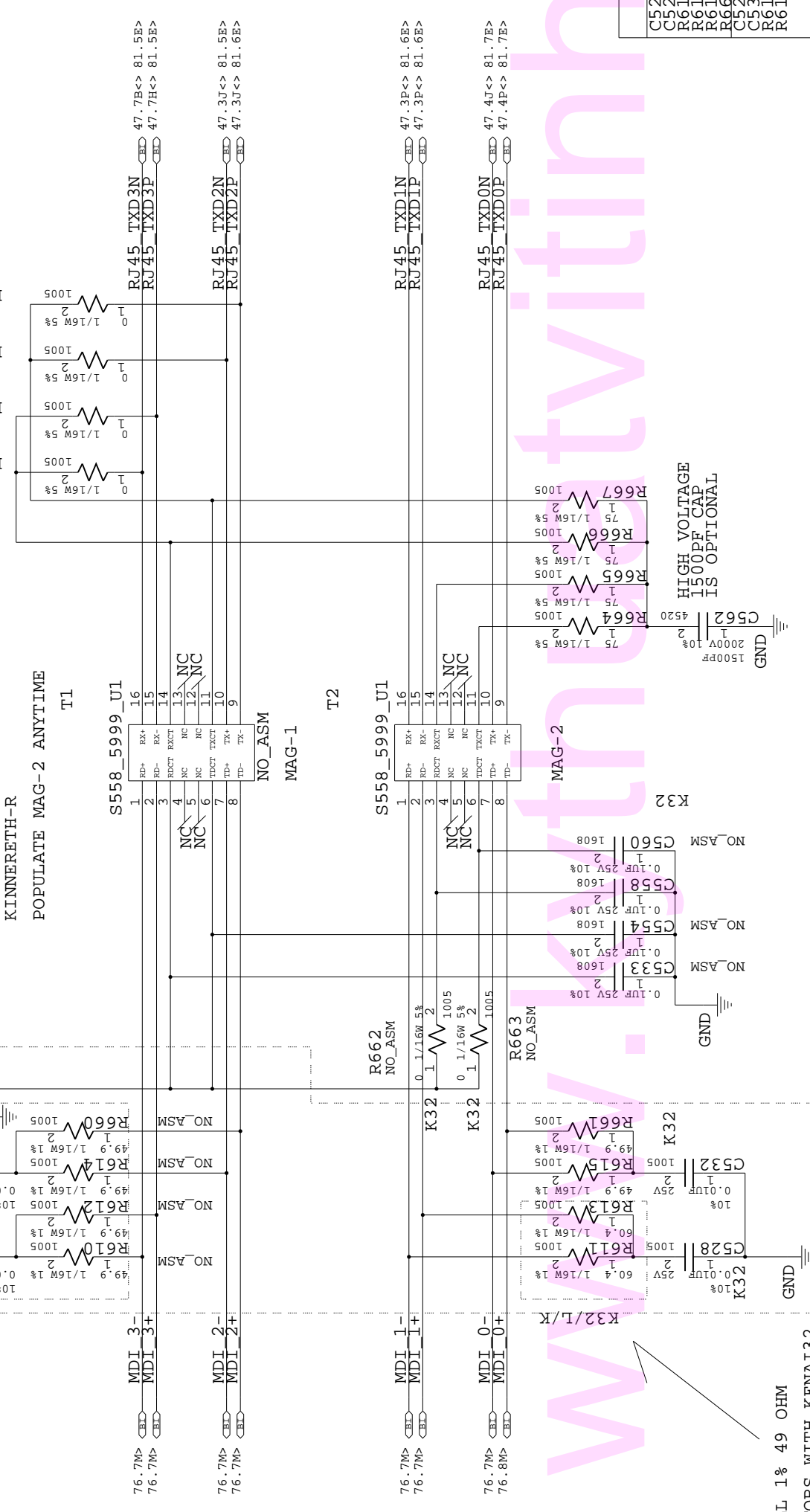
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54.6E>	
45.4C<>	
40.5K<>	
46.6L<>	
60.5J<>	
49.7B<	
52.7B<	
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C560	10%	0.01uF	15V

THESE FOUR RESISTORS ARE POPULATED FOR KINNERETH-R

DO NOT POPULATE MAG-1 WHEN USING KINNERETH-R  
POPULATE MAG-2 ANYTIME



INSTALL 1% 49 OHM RESISTORS WITH KENAI32 AND WITH KENAI II 32, OR 1% 60.4 OHM RESISTORS WITH LAVON AND KINNERETH-R CONTROLLERS.

THESE R AND C SHOULD BE PLACED NEAR PHY CHIP (KENAI32M, KENAI2-32 AND KINNERETH-R)

T1 : S558-599-BD FOR KENAI32M OR KENAI2-32  
T2 : S558-599-BD FOR KENAI32M OR KENAI2-32, S558-599-U1 FOR KINNERETH-R

ETHERNET TABLE (4/5)

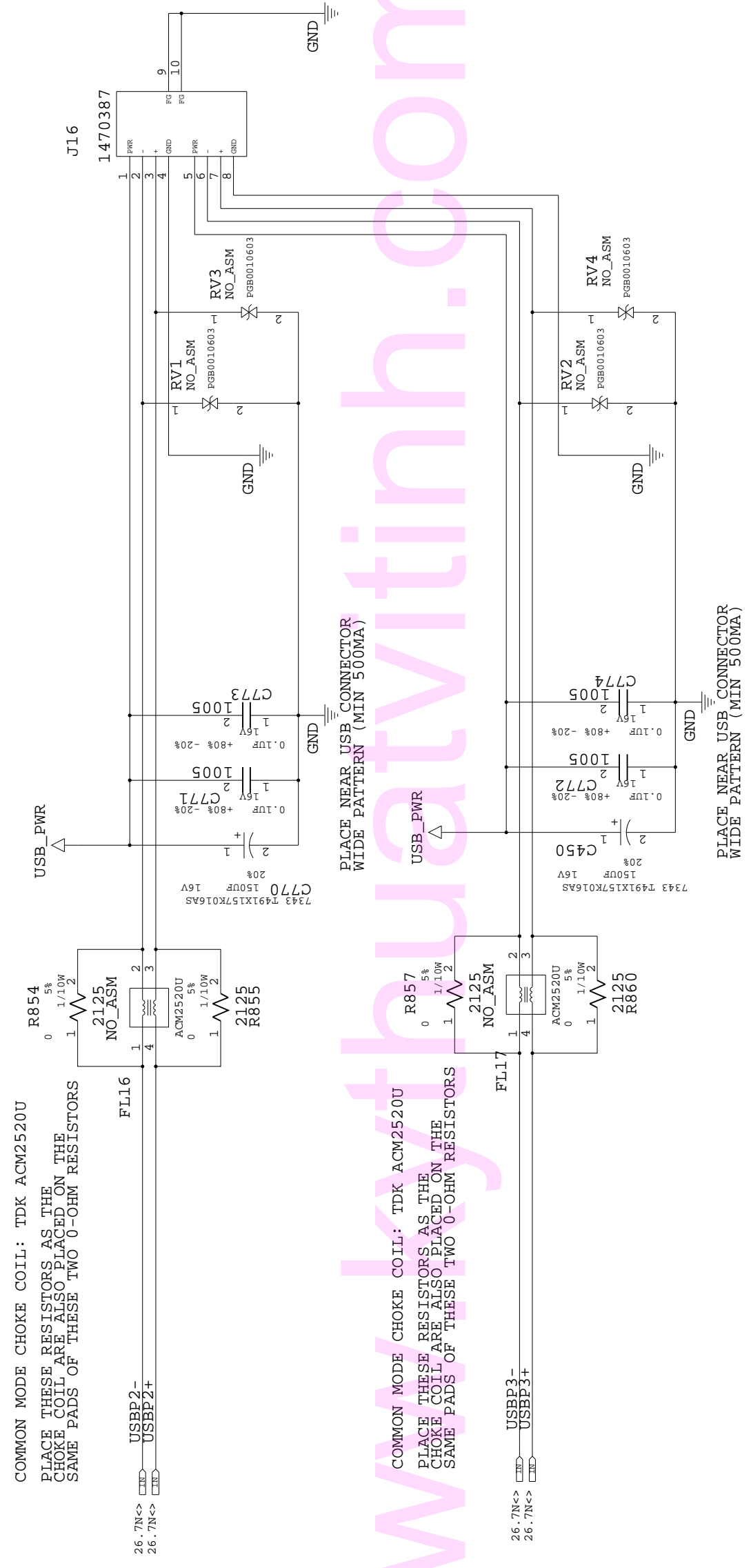
KINNERETH-R		KENAI II-32		KENAI32M	
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C529	NO-ASM	ASM	ASM	ASM	ASM
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R612	NO-ASM	ASM	ASM	ASM	ASM
R614	NO-ASM	ASM	ASM	ASM	ASM
R616	NO-ASM	ASM	ASM	ASM	ASM
R618	NO-ASM	ASM	ASM	ASM	ASM
R620	NO-ASM	ASM	ASM	ASM	ASM
R622	NO-ASM	ASM	ASM	ASM	ASM
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R632	NO-ASM	ASM	ASM	ASM	ASM
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LOGIC

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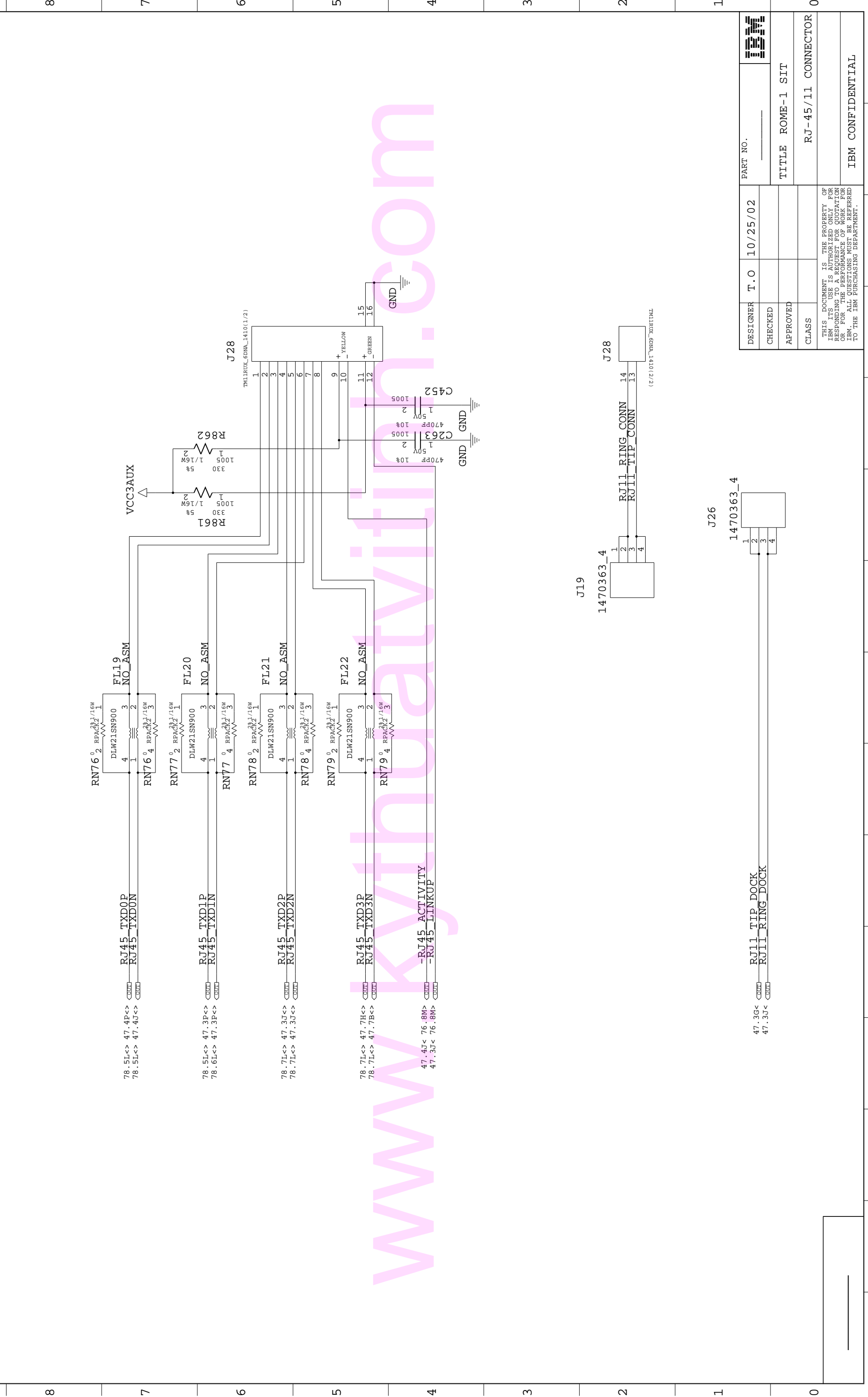
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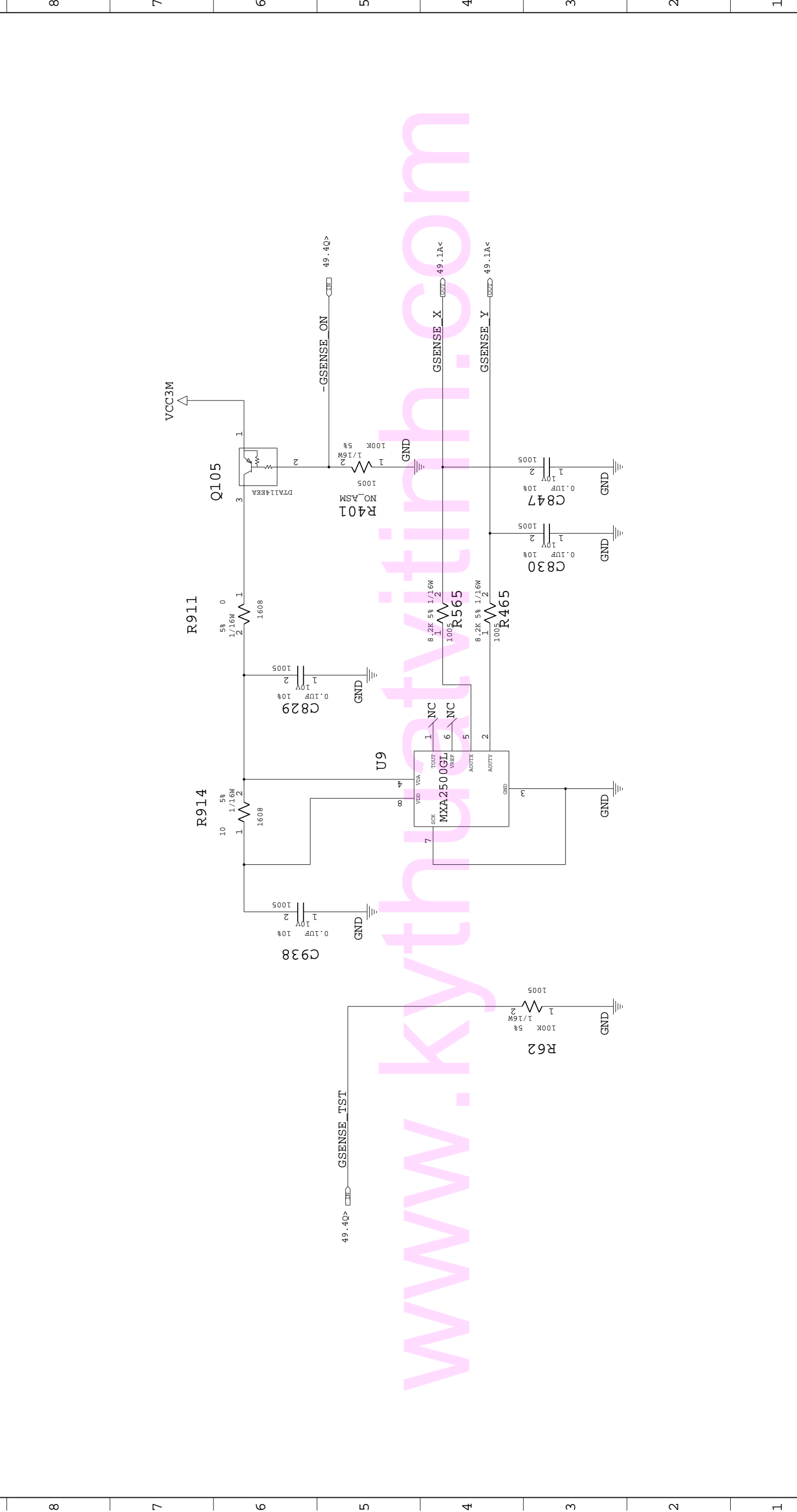


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												81 / 82		



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												82 / 82		



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