Wistron Confidential

PV

2009/10/19 REV :PV-01

<Variant Name>

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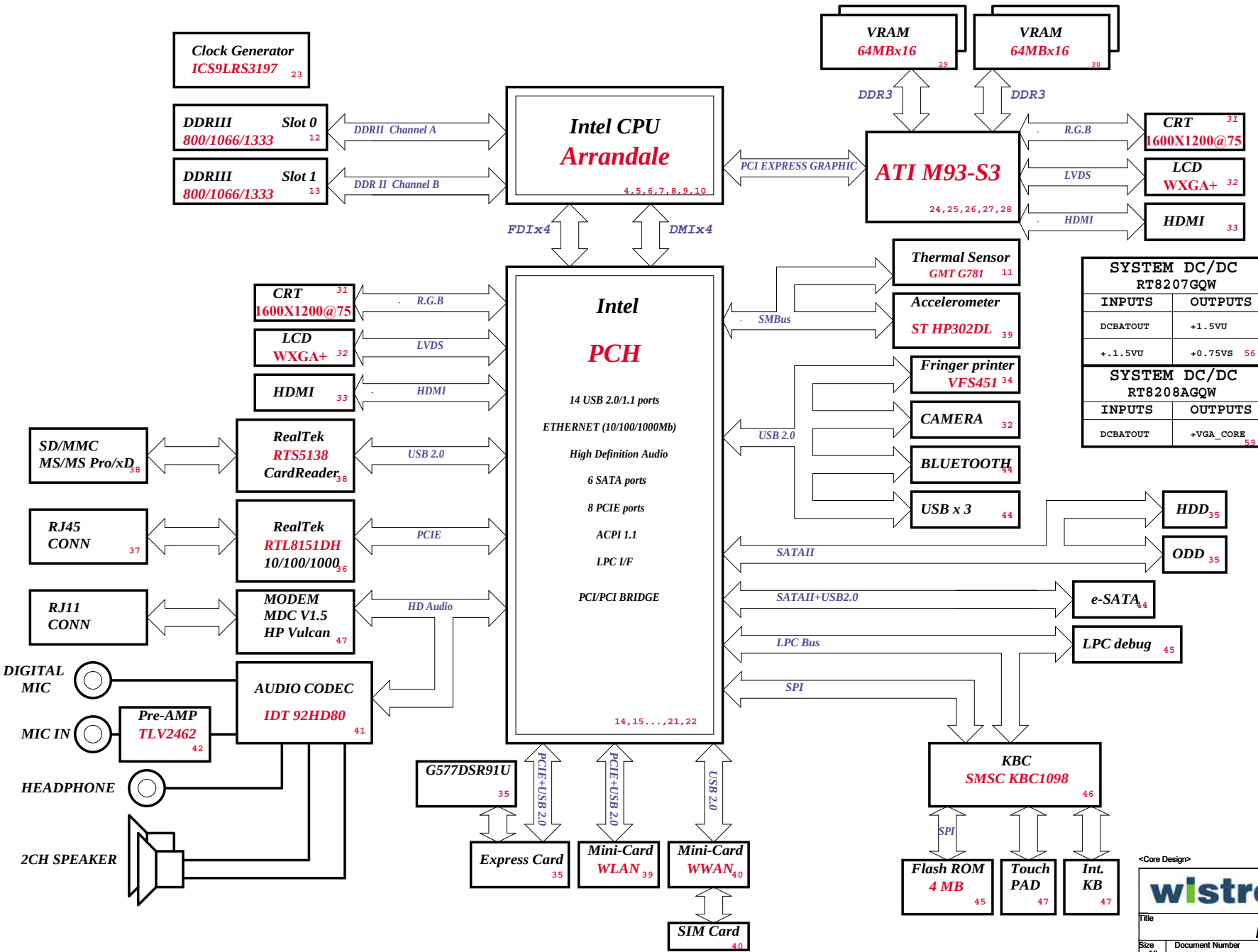
Title: *S-Class Intel*

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 1 of 62

Intel Calpella Arrandale Block Diagram



SYSTEM DC/DC RT8205A	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 53

SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	+1.05VS_VTT +1.05VS 58

SYSTEM DC/DC ADP3211MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_GFX_CORE 55

SYSTEM DC/DC RT8207GQW	
INPUTS	OUTPUTS
DCBATOUT	+1.5VU
+.1.5VU	+0.75VS 56

SYSTEM DC/DC RT8208AGQW	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 59

TI CHARGER BQ24740	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 52

CPU DC/DC ADP3212MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 65A 54

SYSTEM DC/DC APL5930/APL5930	
INPUTS	OUTPUTS
+3VS	+1.8VS_NB +1.8VS_VGA
+1.5VS	+1.1V_REG 57

PCB 6 LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

<Core Design>

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Title: **Block Diagram**

Size: A3 | Document Number: S-Class Intel | Rev: SD

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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing page 15

LANE2	EXP
LANE4	WLAN
LANE6	LAN

USB Table page 18

Pair	Device
0	External USB2
1	USB1 (Debug port)
2	ESATA USB4
3	Card Reader
4	NEW CARD
5	FREE
6	WLAN
7	FREE
8	BLUETOOTH
9	WWAN
10	Fingerprint
11	External USB3
12	CAMERA
13	FREE

091019-1

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

090901-1

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	M93
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	V	V
PCH_SMB_DATA PCH_SMB_CLK	Calpella	X	V	V	V	V	X	X

<Core Design>

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Title: **Notes List**

Size: A3 | Document Number: S-Class Intel | Rev: SD

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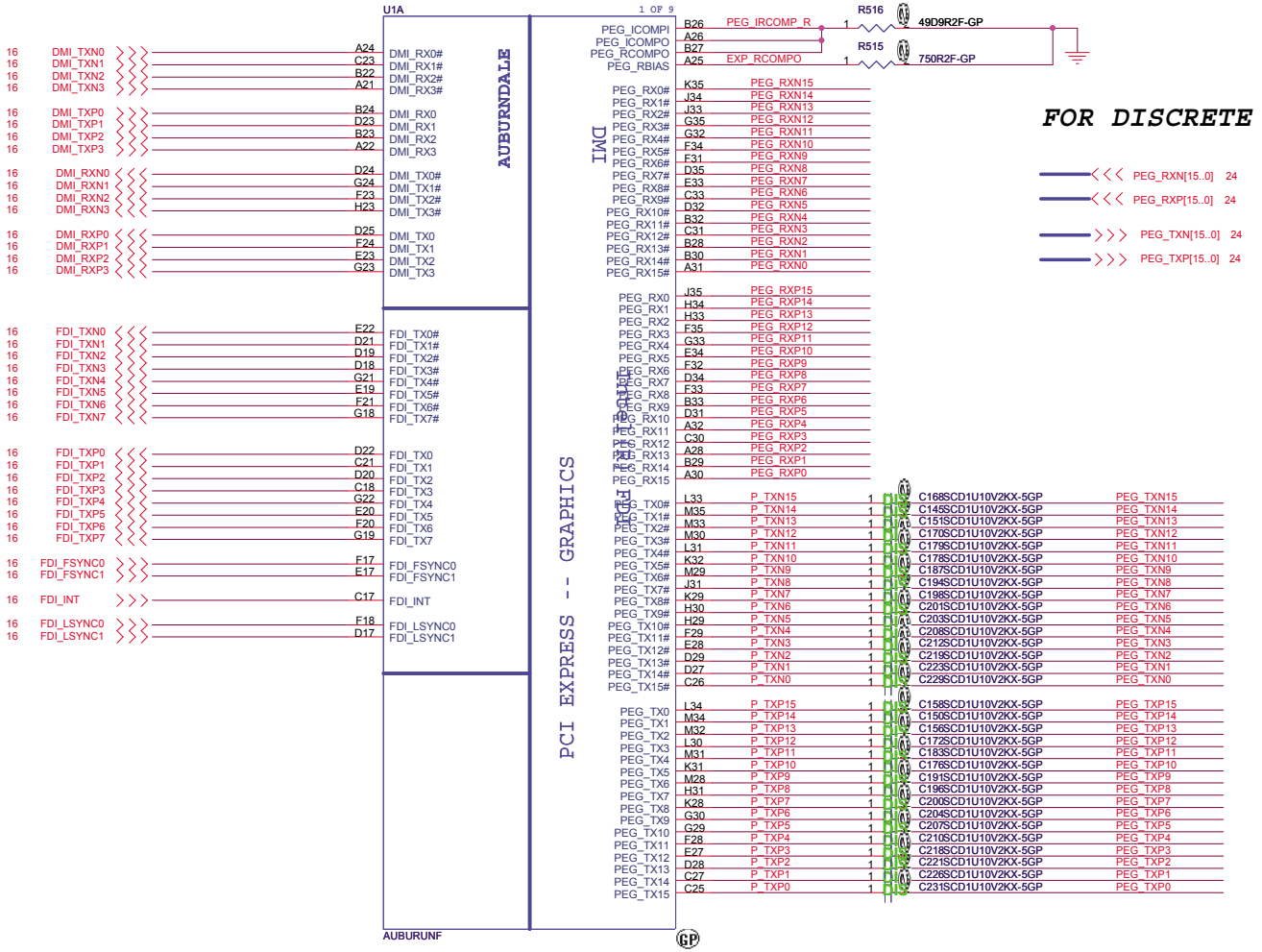
CPU(1/7)



<Core Design>

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Title: CPU (1/7)-PEG / DMI / FDI

Size: A3 | Document Number: S-Class Intel | Rev: SD

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CPU(2/7)

5

Processor Pullups

+1.05VS_VTT

R157 1 49D9R2F-GP H_CATERR#

R171 1 DX 68R2-GP H_CPURST#_R

Processor Compensation Signals

R460 1 20R2F-GP H_COMP3

R462 1 20R2F-GP H_COMP2

R501 1 49D9R2F-GP H_COMP1

R463 1 49D9R2F-GP H_COMP0

TP60 TPAD14-GP 1 SKTOCC#_R

U1B

H_COMP3	AT23	COMP3
H_COMP2	AT24	COMP2
H_COMP1	G16	COMP1
H_COMP0	AT26	COMP0
SKTOCC#_R	AH24	SKTOCC#
H_CATERR#	AK14	CATERR#
H_PECI	AT15	PECI
H_PROCHOT#	AN26	PROCHOT#
H_THRMTRIP-A#	AK15	THERMTRIP#
H_CPURST#_R	AP26	RESET_OBS#
H_PM_SYNC	AL15	PM_SYNC
VCCPWRGOOD	AN14	VCCPWRGOOD_1
VCCPWRGOOD_0	AN27	VCCPWRGOOD_0
VDDPWRGOOD_R	AK13	SM_DRAMPWROK
H_VTTPWRGD	AM15	VTTPWRGOOD
H_PWRGD_XDP	AM26	TAPPWRGOOD
PLT_RST#_R	AL14	RSTIN#
		AUBURUNF

2 OF 9

AUBURNDE CLOCKS

BCLK BCLK#	A16 B16	BCLK_CPU_P_R BCLK_CPU_N_R	RN62 SRN0J-10-GP-U
BCLK_ITP BCLK_ITP#	AR30 AT30	BCLK_ITP_P_R BCLK_ITP_N_R	RN4 SRN0J-10-GP-U
PEG_CLK PEG_CLK#	E16 D16	PEG_CLK_R PEG_CLK#_R	RN60 SRN0J-10-GP-U
DPLL_REF_SSCLK DPLL_REF_SSCLK#	A18 A17	DPLL_REF_SSCLK_R DPLL_REF_SSCLK#_R	RN61 SRN0J-10-GP-U

BCLK_CPU_P_R 19 BCLK_CPU_N_R 19

CLK_CPU_XDP CLK_CPU_XDP# 15

CLK_EXP_P 15 CLK_EXP_N 15

CLK_DP_P 15 CLK_DP_N 15

THERMAL, DDR3 MISC

SM_DRAMRST#	F6	DDR3_DRAMRST#_R
SM_RCOMP0 SM_RCOMP1 SM_RCOMP2	AL1 AM1 AN1	SM_RCOMP_0 SM_RCOMP_1 SM_RCOMP_2
PM_EXT_TS0# PM_EXT_TS1#	AN15 AP15	

RN54 SRN10KJ-5-GP

+1.05VS_VTT

PM_EXTTS#0_R 12 PM_EXTTS#1_R 13

R105 12K4R2F-GP DY R108 12K4R2F-GP DY

PWR MANAGEMENT

PRDY# PREQ#	AT28 AP27	XDP_PRDY# XDP_PREQ#
TCK TMS TRST#	AN28 AP28 AT27	XDP_TCK XDP_TMS XDP_TRST#
TDI TDO TDI_M TDO_M	AT29 AR27 AR29 AP29	XDP_TDI XDP_TDO XDP_TDI_TDO_M XDP_TDI_TDO_M_R
DBR#	AN25	XDP_DBRESET#

091019-1

R461 1 2 0R0402-PAD-1-GP

BPM0# BPM1# BPM2# BPM3#	AJ22 AK22 AK24 AJ24	XDP_BPM#0 XDP_BPM#1 XDP_BPM#2 XDP_BPM#3	
BPM4# BPM5# BPM6# BPM7#	AJ25 AH22 AK23 AH23	XDP_BPM#4_R XDP_BPM#5_R XDP_BPM#6_R XDP_BPM#7_R	R168 R158 R150 R145

0R0402-PAD-1-GP XDP_BPM#4 XDP_BPM#5 XDP_BPM#6 XDP_BPM#7

DDR3 Compensation Signals

SM_RCOMP_0 R136 100R2F-L1-GP-U

SM_RCOMP_1 R135 24D9R2F-L-GP

SM_RCOMP_2 R134 130R2F-1-GP

R252 DX 0R2J-2-GP +1.5VU

R257 1KR2J-1-GP

Q17 BSS138-7F-GP

DDR3_DRAMRST# 12,13

R253 100KR2J-1-GP

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090813-1-SI

R771 0R0402-PAD-1-GP PCH_DDR_RST 19

C978 SC470P50V2KX-3GP

+1.05VS_VTT

XDP_TMS R132 DY 51R2J-2-GP

XDP_PREQ# R141 DY 51R2J-2-GP

R128 1K5R2F-2-GP

R124 750R2F-GP

VCCP_1.5VSPWRGD 49

16 PM_DRAM_PWRGD

49 H_VTTPWRGD

VDDPWRGOOD_R

18,26,35,36,39,45 PLT_RST#

R130 0R0402-PAD-1-GP VDDPWRGOOD_R

R121 0R0402-PAD-1-GP 19 H_PWRGD

R117 0R0402-PAD-1-GP VCCPWRGOOD_0

R176 0R0402-PAD-1-GP H_CPURST#

16 H_PM_SYNC

R127 1K5R2F-2-GP PLT_RST#_R

R129 750R2F-GP

closed to XDP

XDP1

STC-CONN60A-GP 20.F0971.060

XDP_PREQ# XDP_PRDY#	3 5	
XDP_BPM#0 XDP_BPM#1	9 11	
XDP_BPM#2 XDP_BPM#3	13 15	
XDP_BPM#4 XDP_BPM#5	25 27	
XDP_BPM#6 XDP_BPM#7	31 33	
CLK_CPU_XDP	39	
CLK_CPU_XDP#	41	
XDP_RST#_R	45	
XDP_DBRESET#_R	47	
XDP_TRST#	51	
XDP_TDI	53	
XDP_TMS	55	
XDP_TCK	57	

XDP_TRST# R431 51R2J-2-GP

090824-1-SI

16,45,46 PWRBTN_OUT#

+1.05VS_VTT

H_PWRGD XR1 DY 1KR2J-1-GP

H_CPUPWRGD_R

H_PWRGD_XDP

090901-1

TPAD14-GP TP4 TPAD14-GP TP3

XDP1_TP2 XDP1_TP3

XDP_TCK

XDP_RST#_R XR4 DX 1KR2J-1-GP H_CPURST#

XDP_DBRESET#_R XR2 DY 0R2J-2-GP

XDP_DBRESET# 16

XDP_TDO

XDP_RST#_R XR3 DY 0R2J-2-GP PLT_RST# 18,26,35,36,39,45

+1.05VS_VTT +3VS

R432 51R2J-2-GP

R435 10KR2J-3-GP

Place those AFTP at bottom side.

XDP_TDO	TP38	TPAD14-GP
XDP_TRST#	TP37	TPAD14-GP
XDP_TMS	TP40	TPAD14-GP
XDP_TDI	TP36	TPAD14-GP
XDP_TCK	TP2	TPAD14-GP

<Core Design>

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Title: CPU (2/7)-HOST

Size: A3 | Document Number: S-Class Intel | Rev: SD

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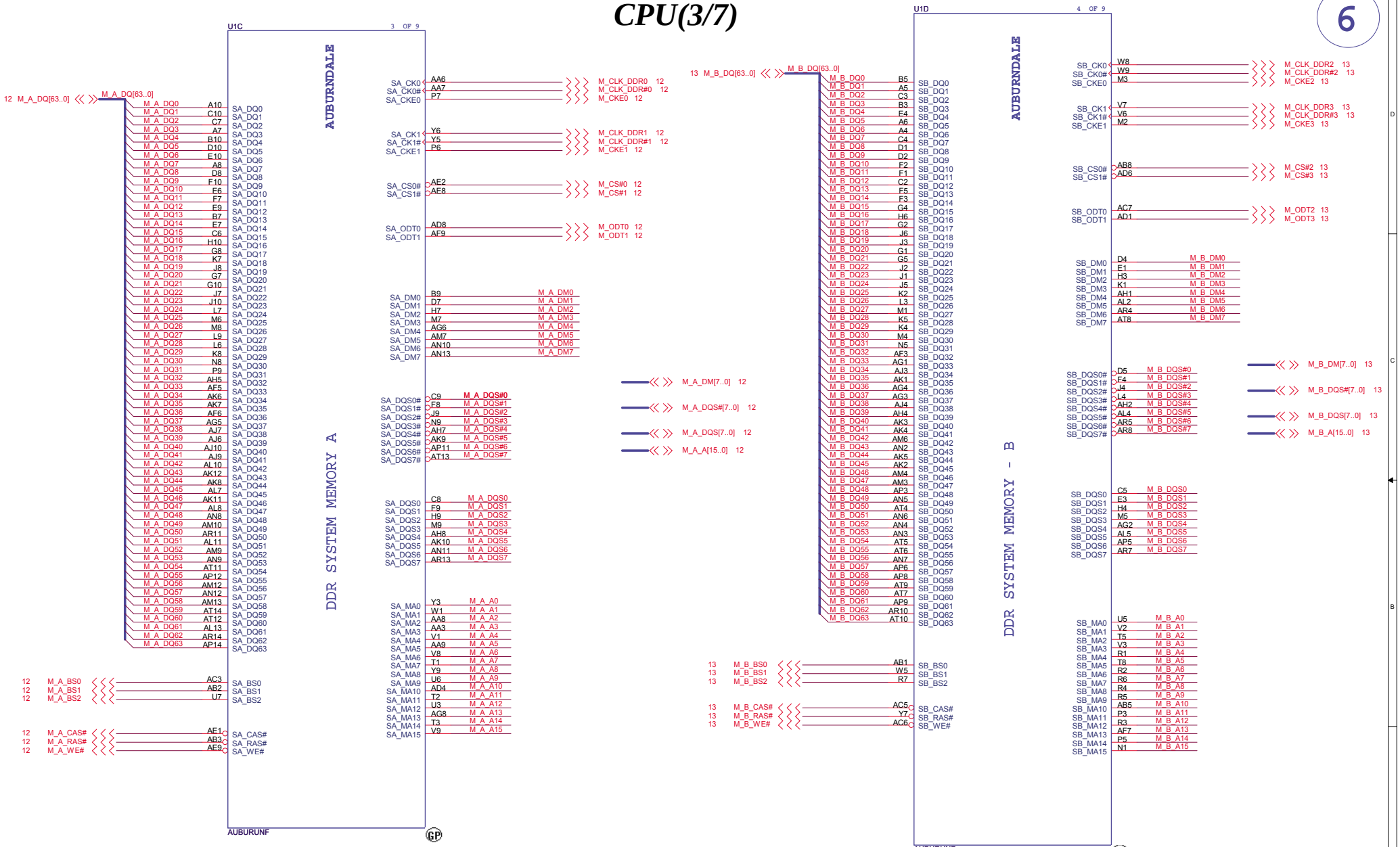
CPU(3/7)



Wistron Incorporated	21F, 88, Hsin Tai Wu Rd, Hsichih, Taipei
Title	CPU (3/7)-MEM INTERFACE
Size A3	Document Number S-Class Intel
Rev	SD
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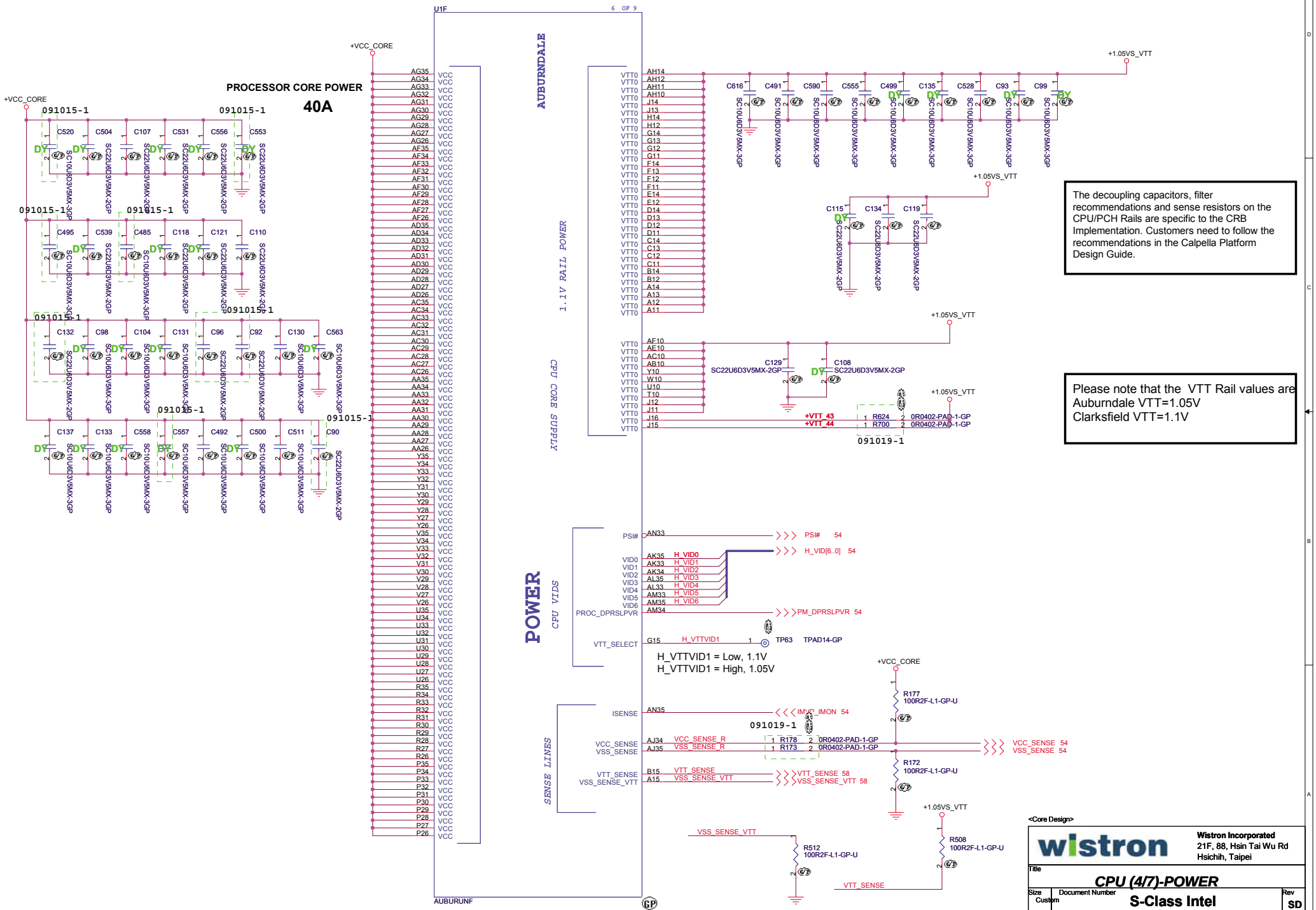
CPU(4/7)


PROCESSOR CORE POWER
40A
+VCC_CORE
091015-1
U1F
6 OF 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
+1.05VS_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V
PSI#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
PROC_DPRSLPVR
VTT_SELECT
H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
AUBURUNF
091019-1
<Core Design>
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CPU (4/7)-POWER
S-Class Intel
SD
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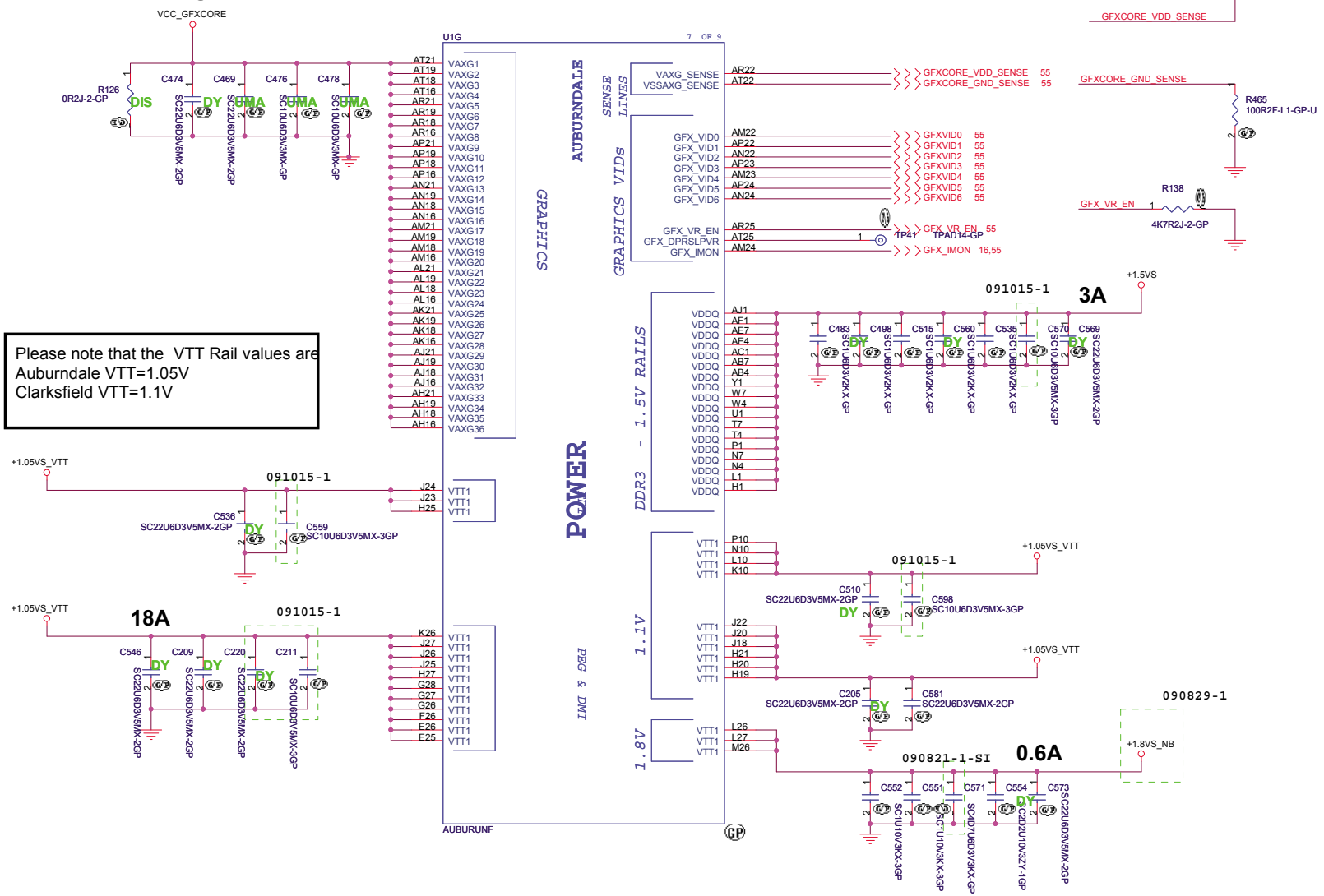
CPU(5/7)

UMA 22A



Please note that the VTT Rail values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

<Core Design>

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Title: CPU (5/7)-Graphic POWER

Size: A3 | Document Number: S-Class Intel | Rev: SD

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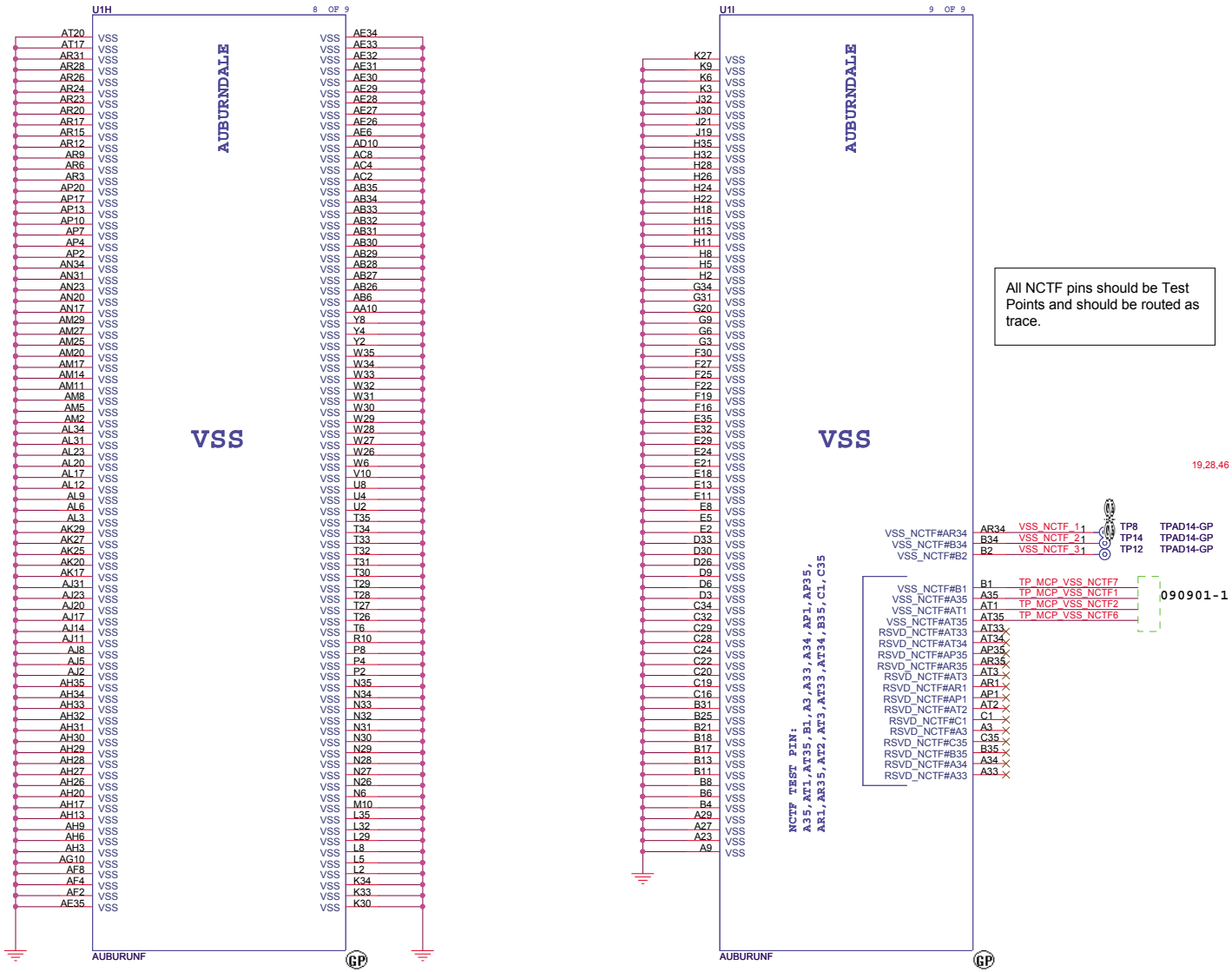
CPU(6/7)



<Core Design>

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Title: CPU (6/7)-VSS		
Size: A3	Document Number: S-Class Intel	Rev: SD
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CPU(7/7)

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

CFG0 — R140 3K01R2F-3-GP (DY)

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 — R149 3K01R2F-3-GP (DY)

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

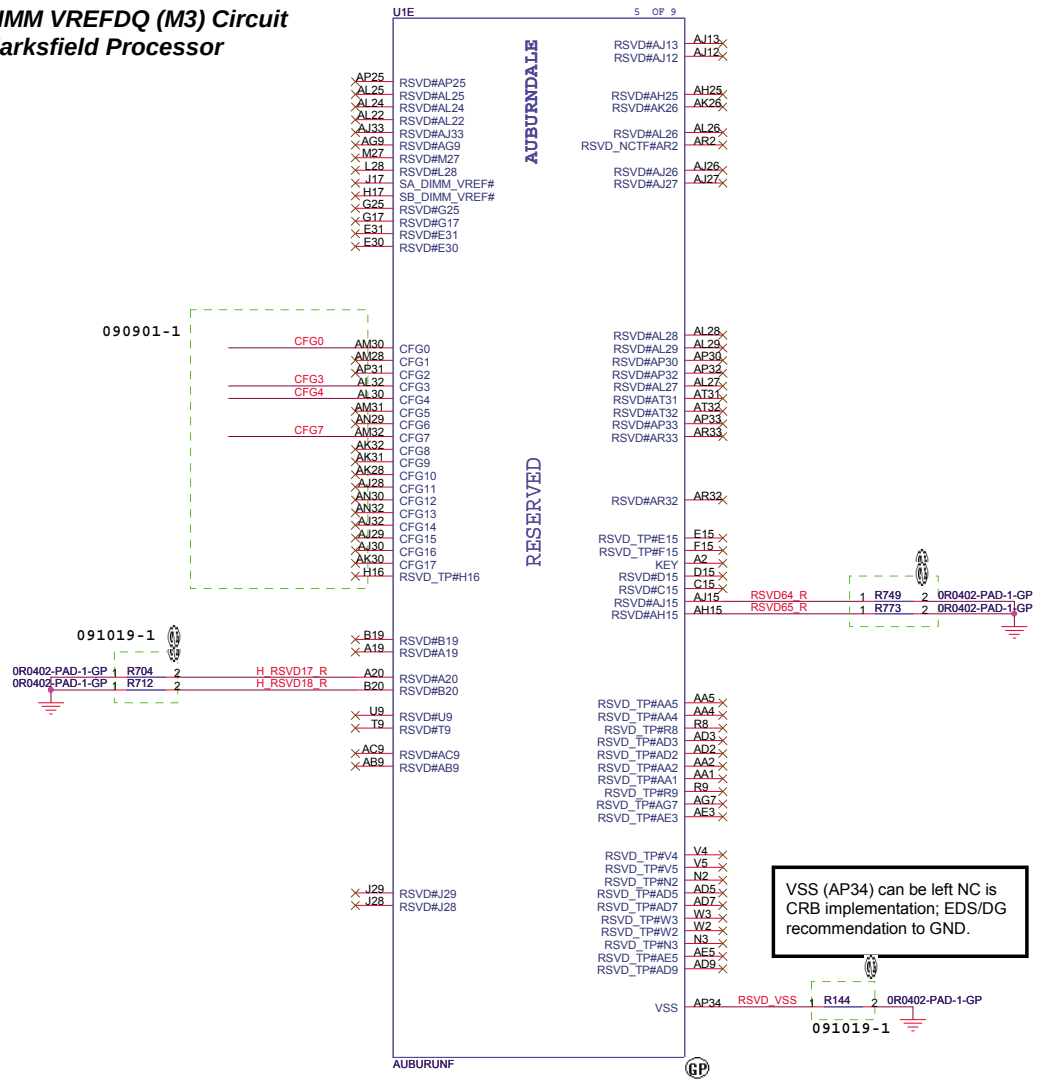
CFG4 — R156 3K01R2F-3-GP (DY)

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

0829 SA

CFG7 — R167 3K01R2F-3-GP (DY)

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



<Core Design>

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Title: CPU (7/7)-RESERVED

Size: A3 | Document Number: S-Class Intel | Rev: SD

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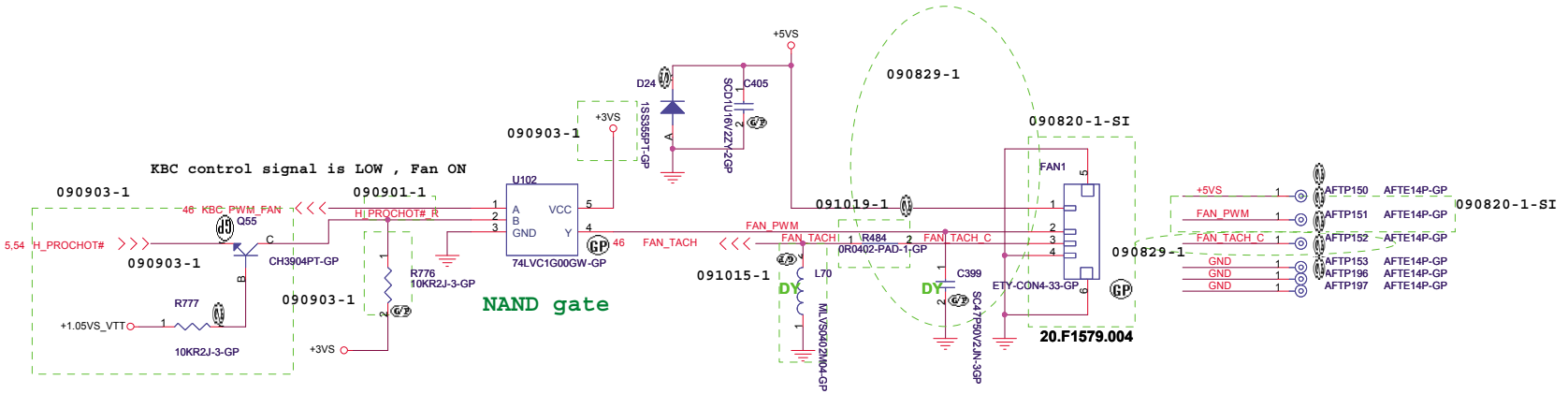
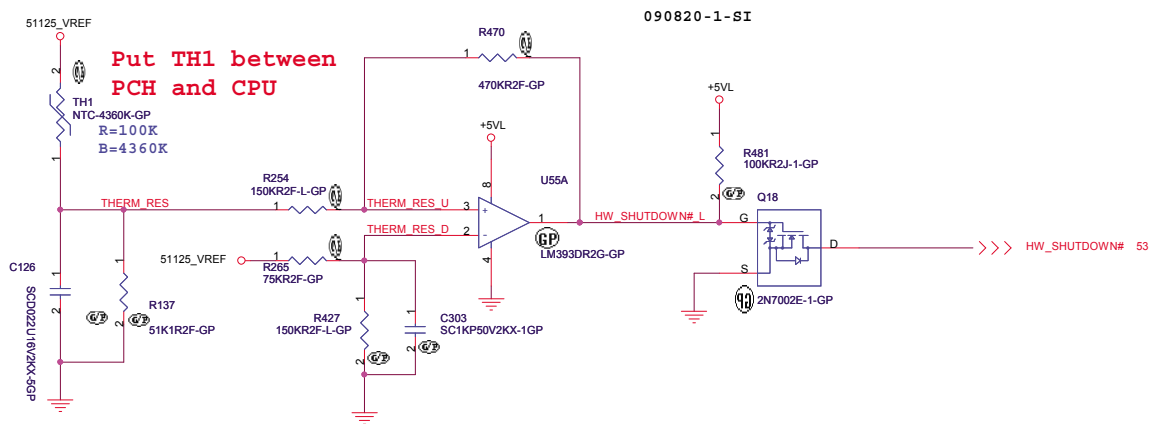
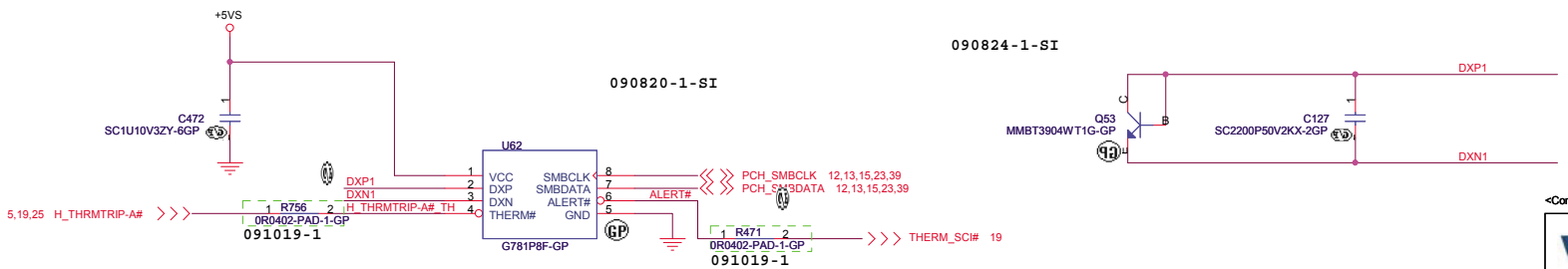
4 WIRE PWM Fan Control circuit



T8 H/W Shutdown Control circuit



Thermal IC Control circuit



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Title: G787S11U-GP THERMAL

Size: A3 | Document Number: S-Class Intel | Rev: SD

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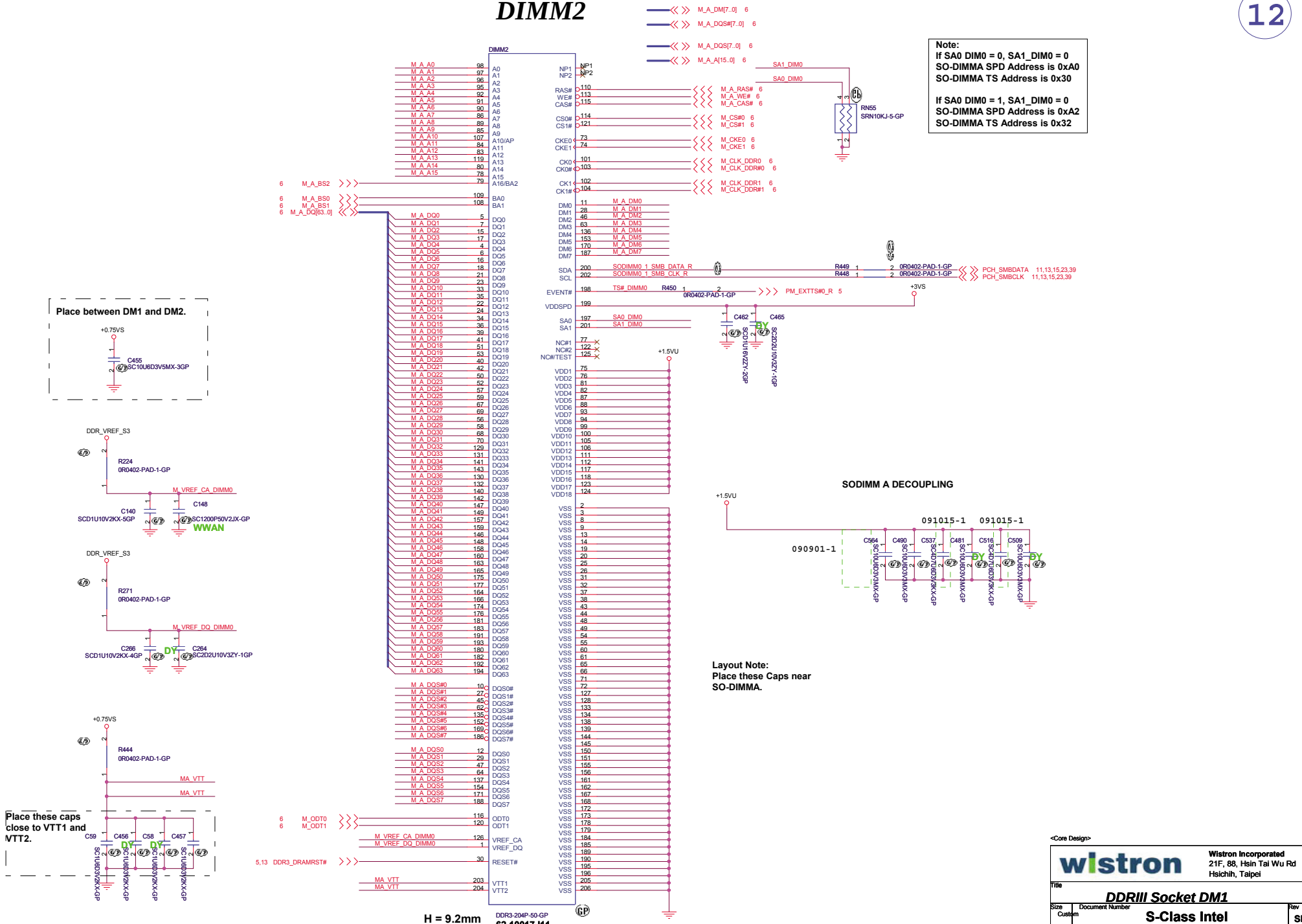
DIMM2



<Core Design>
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Title: DDRIII Socket DM1

Size: Custom | Document Number: S-Class Intel | Rev: SD

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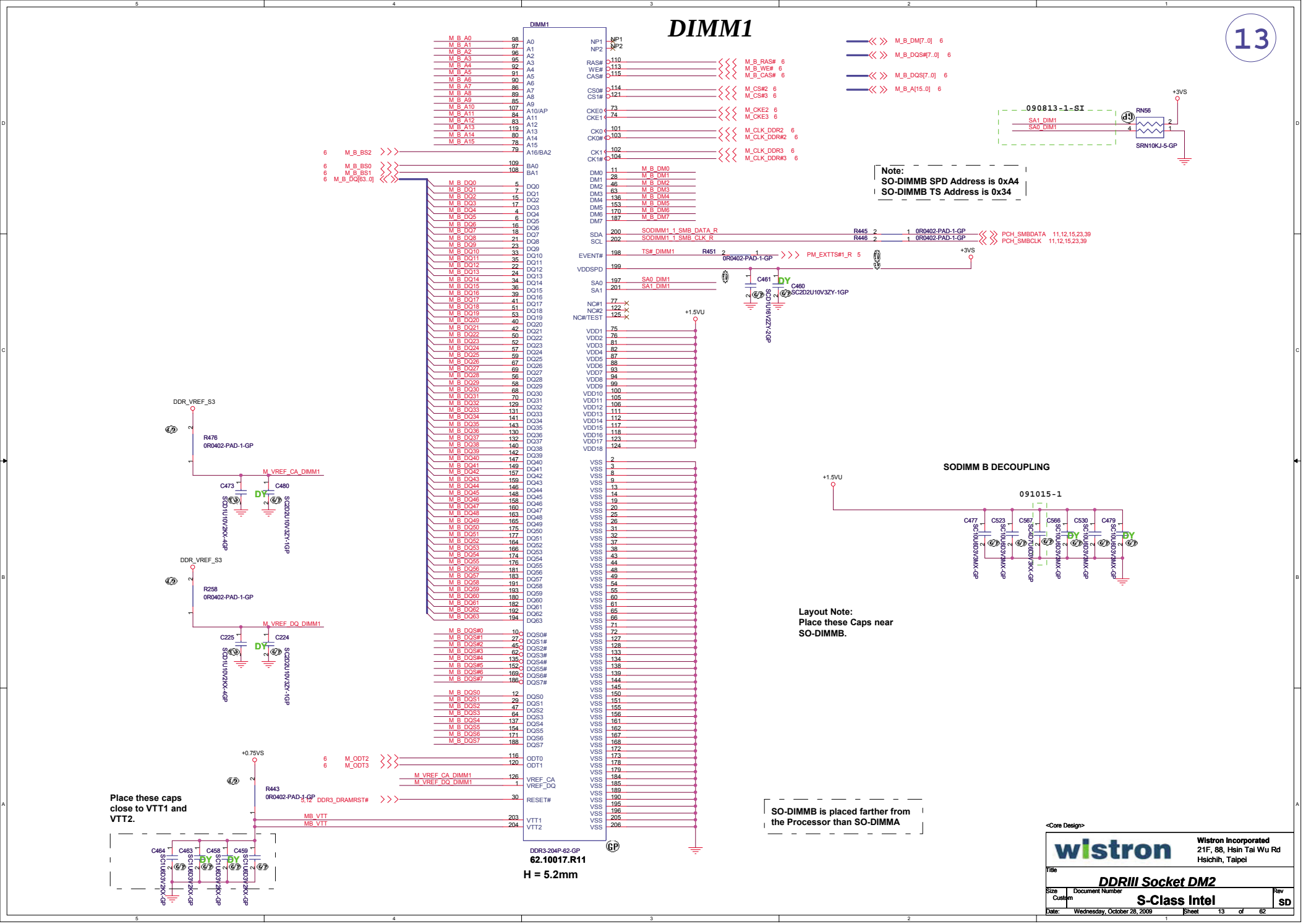
DIMM1



<Core Design>

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Title: DDRIII Socket DM2

Size: Custom | Document Number: S-Class Intel | Rev: SD

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PCH(1/9)

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INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

U3A 1 OF 10

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14
LPC: FWH0/LAD0 D33, FWH1/LAD1 B33, FWH2/LAD2 C32, FWH3/LAD3 A32, FWH4/LFRAME# C34, LDRQ0# A34, LDRQ1#/GPIO23 F34, SERIRQ AB9
IHDA: HDA_BCLK A30, HDA_SYNC D29, SPKR P1, HDA_RST# C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29
SATA: HDA_DOCK_EN#/GPIO33 H32, HDA_DOCK_RST#/GPIO13 J30; SATA0RXN AK7, SATA0RXP AK6, SATA0TXN AK11, SATA0TXP AK9; SATA1RXN AH6, SATA1RXP AH5, SATA1TXN AH9, SATA1TXP AH8; SATA2RXN AF11, SATA2RXP AF9, SATA2TXN AF7, SATA2TXP AF6; SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1; SATA4RXN AD9, SATA4RXP AD8, SATA4TXN AD6, SATA4TXP AD5; SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1; SATAICOMPO AF16, SATAICOMPI AF15
JTAG: JTAG_TCK M3, JTAG_TMS K3, JTAG_TDI K1, JTAG_TDO J2, TRST# J4
SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1; SATALED# T3, SATA0GP/GPIO21 Y9, SATA1GP/GPIO19 V1

IBEXPEAK-M-GP-NF

HDD: SATA_RXN0 35, SATA_RXP0 35, SATA_TXN0 35, SATA_TXP0 35
ODD: SATA_RXN1 35, SATA_RXP1 35, SATA_TXN1 35, SATA_TXP1 35
ESATA: SATA_RXN4 44, SATA_RXP4 44, SATA_TXN4 44, SATA_TXP4 44

LPC_AD[0..3] 45,46; LPC_FRAME# 45,46; PCH_GPIO23; SIRQ 45,46

NO REBOOT STRAP

090829-1

No Reboot Strap R336	
HDA_SPKR	Low = Default High = No Reboot

VTAP Assumed as 1.1V

PCH_JTAG_RST# R347 51R2F-2-GP
PCH_JTAG_TCK R338 4K7R2J-2-GP
PCH_JTAG_TMS R342 51R2F-2-GP
PCH_JTAG_TDO R351 51R2F-2-GP
PCH_JTAG_TDI R345 51R2F-2-GP
PCH_JTAG_RST# R349 10KR2J-3-GP

Place the resistors on RST, TCK, TMS, and TDI near PCH.

Place the resistors on TDO near XDP.

Oscillator

ICH_RTCX1, ICH_RTCX2
R358 10MR2J-L-GP
090903-1
X1 X-32D768KHZ-38GPU 82.30001.691
090825-1-SI
C386 SC15P50V2JN-2GP, C387 SC15P50V2JN-2GP

32.768Khz 12.5pf 10ppm
1st: 82.30001.691 (KDS)

BIOS have Default code & Run code. If we want to flash default code area, we should set GPIO33 be Low when SYS_PWROK assert.

+3VS, R719 10KR2J-3-GP DY, R692 1KR2F-3-GP, GPIO33, Q48 2N7002E-1-GP, R718 0R2J-2-GP, 46,51 WHITE_BATLED#

RTC Battery

+RTCVCC, 091019-1, W=20mils, R352 0R0402-PAD-1-GP, RTC_PWR_L, C372 SC1U10V3KX-3GP
090919-1, U43 CH715FPT-GP, RTC_PWR, R353 1KR2J-1-GP
090829-1, 3D3V_AUX_S5_5_51125, BATT1.1
090819-1-SI, RTC1, BAT-BH-8201-C1401-7H-GP 62.70001.031
090829-1

<Core Design>

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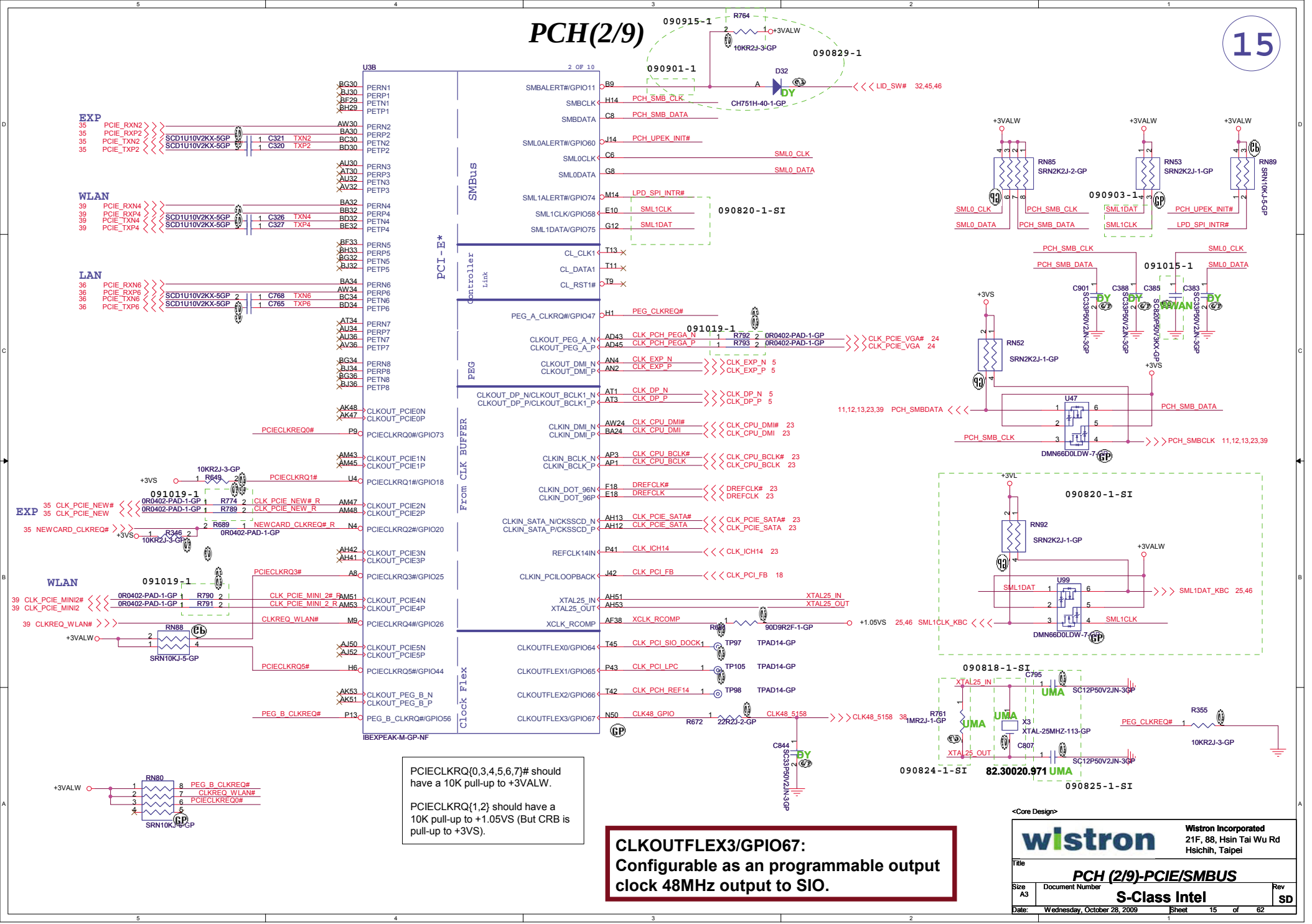
Title: PCH (1/9)-SATA/SPI/LPC
Size: A3 | Document Number: S-Class Intel | Rev: SD
Date: Wednesday, October 28, 2009 | Sheet 14 of 62

PCH(2/9)



<Core Design>
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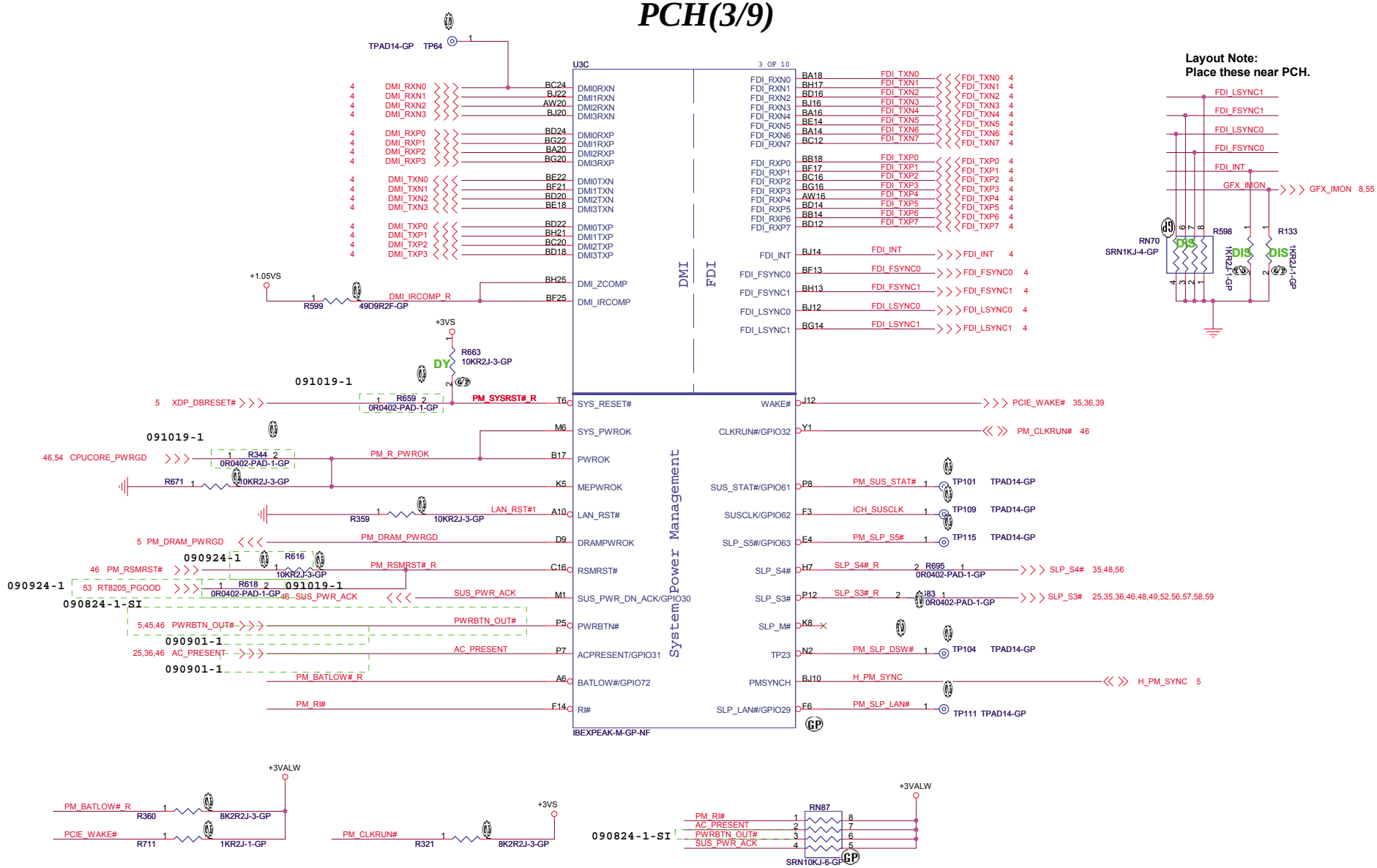
Hsichih, Taipei

Title: PCH (2/9)-PCIE/SMBUS

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 15 of 62

PCH(3/9)



Layout Note:
Place these near PCH.

<Core Design>

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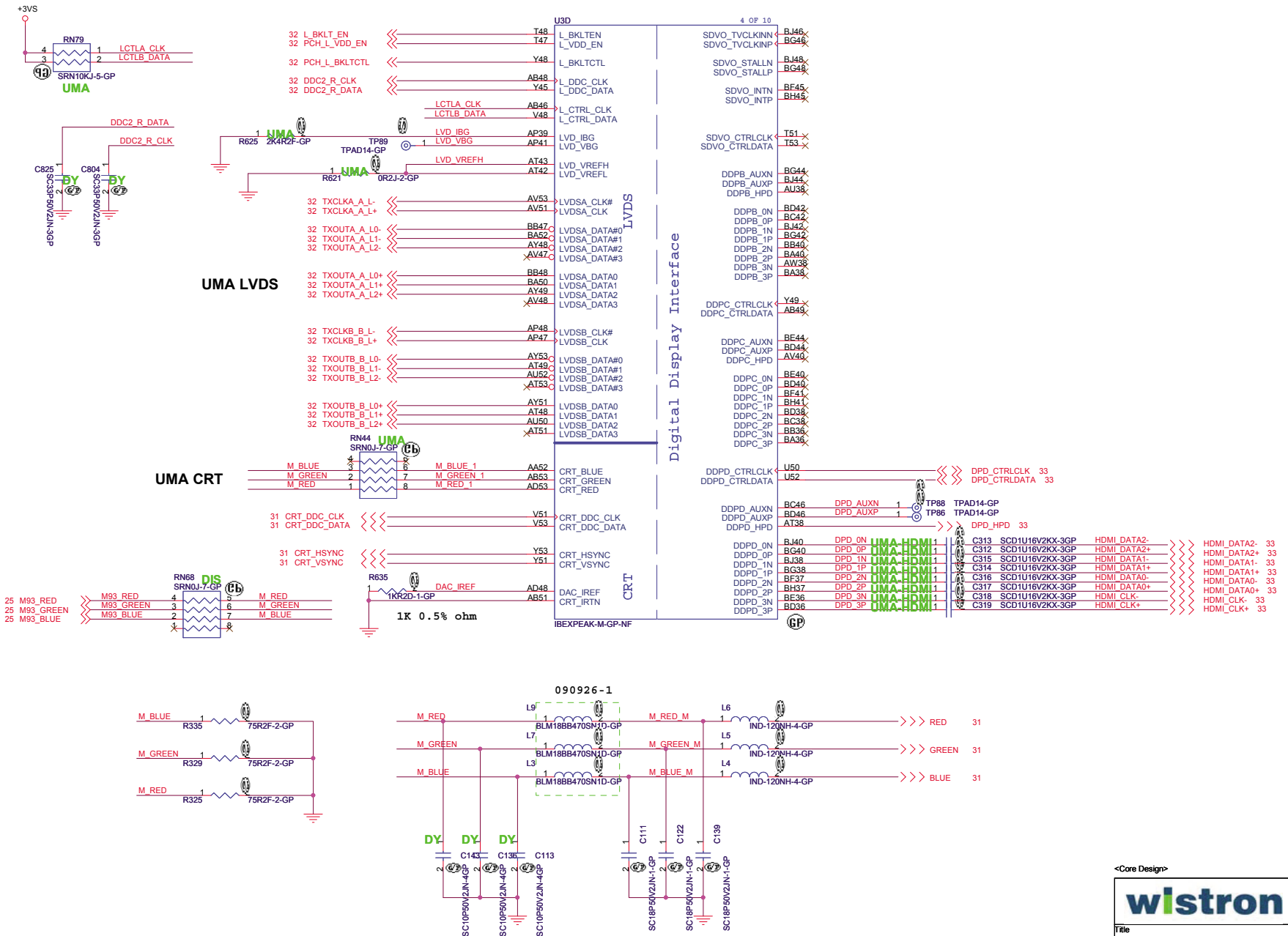
Title: PCH (3/9)-DMI/SYS PWR

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 16 of 62

PCH(4/9)



<Core Design>

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Title: PCH (4/9)-LVDS/CRT

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 17 of 62

PCH(5/9)

U3E — 5 OF 10 — IBEXPEAK-M-GP-NF

PCI

AD0	H40
AD1	N34
AD2	C44
AD3	A38
AD4	C36
AD5	J34
AD6	A40
AD7	D45
AD8	E36
AD9	H48
AD10	E40
AD11	C40
AD12	M48
AD13	M45
AD14	F53
AD15	M40
AD16	M43
AD17	J36
AD18	K48
AD19	F40
AD20	C42
AD21	K46
AD22	M51
AD23	J52
AD24	K51
AD25	L34
AD26	F42
AD27	J40
AD28	G46
AD29	F44
AD30	M47
AD31	H36
C/BE0#	J50
C/BE1#	G42
C/BE2#	H47
C/BE3#	G34
PIRQA#	G38
PIRQB#	H51
PIRQC#	B37
PIRQD#	A44
REQ0#	F51
REQ1#/GPIO50	A46
REQ2#/GPIO52	B45
REQ3#/GPIO54	M53
GNT0#	F48
GNT1#/GPIO51	K45
GNT2#/GPIO53	F36
GNT3#/GPIO55	H53
PIRQE#/GPIO2	B41
PIRQF#/GPIO3	K53
PIRQG#/GPIO4	A36
PIRQH#/GPIO5	A48
PCIRST#	K6
SERR#	E44
PERR#	E50
IRDY#	A42
PAR	H44
DEVSEL#	F46
FRAME#	C46
PLOCK#	D49
STOP#	D41
TRDY#	C48
PME#	M7
PLTRST#	D5
CLKOUT_PCI0	N52
CLKOUT_PCI1	P53
CLKOUT_PCI2	P46
CLKOUT_PCI3	P51
CLKOUT_PCI4	P48

NVRAM

NV_CE#0	AY9
NV_CE#1	BD1
NV_CE#2	AP15
NV_CE#3	BD8
NV_DQS0	AV9
NV_DQS1	BG8
NV_DQ0/NV_IO0	AP7
NV_DQ1/NV_IO1	AP6
NV_DQ2/NV_IO2	AT6
NV_DQ3/NV_IO3	AT9
NV_DQ4/NV_IO4	BB1
NV_DQ5/NV_IO5	AV6
NV_DQ6/NV_IO6	BB3
NV_DQ7/NV_IO7	BA4
NV_DQ8/NV_IO8	BE4
NV_DQ9/NV_IO9	BB6
NV_DQ10/NV_IO10	BD6
NV_DQ11/NV_IO11	BB7
NV_DQ12/NV_IO12	BC8
NV_DQ13/NV_IO13	BJ8
NV_DQ14/NV_IO14	BJ6
NV_DQ15/NV_IO15	BG6
NV_ALE	BD3
NV_CLE	AY6
NV_RCOMP	AU2
NV_RB#	AV7
NV_WR#0_RE#	AY8
NV_WR#1_RE#	AY5
NV_WE#_CK0	AV11
NV_WE#_CK1	BF5

USB

USBP0N	H18
USBP0P	J18
USBP1N	A18
USBP1P	C18
USBP2N	N20
USBP2P	P20
USBP3N	J20
USBP3P	L20
USBP4N	F20
USBP4P	G20
USBP5N	A20
USBP5P	C20
USBP6N	M22
USBP6P	N22
USBP7N	B21
USBP7P	D21
USBP8N	H22
USBP8P	J22
USBP9N	E22
USBP9P	F22
USBP10N	A22
USBP10P	C22
USBP11N	G24
USBP11P	H24
USBP12N	L24
USBP12P	M24
USBP13N	A24
USBP13P	C24
USBRBIAS#	B25
USBRBIAS	D25
OC0#/GPIO59	N16
OC1#/GPIO40	J16
OC2#/GPIO41	F16
OC3#/GPIO42	L16
OC4#/GPIO43	E14
OC5#/GPIO9	G16
OC6#/GPIO10	F12
OC7#/GPIO14	T15

090821-1-SI

090901-1

NV_CLE

NV_ALE

NV_RCOMP 1 R619 32D4R2F-GP

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

+1.8VS_NB — R725 1KR2J-1-GP DY — NV_CLE

Danbury Technology:
Disabled when Low.
Enable when High.

+1.8VS_NB — R748 1KR2J-1-GP DY — NV_ALE

USB

Pair	Device
0	External USB2
1	USB1 (Debug port)
2	ESATA USB4
3	Card Reader
4	NEW CARD
5	FREE
6	WLAN
7	FREE
8	BLUETOOTH
9	WWAN
10	Fingerprint
11	External USB3
12	CAMERA
13	FREE

091019-1

USB20_N0 44 External USB2
USB20_P0 44
USB20_N1 44 USB1
USB20_P1 44
USB20_N2 44 ESATA USB4
USB20_P2 44
USB20_N3 38 Card Reader
USB20_P3 38
USB20_N4 35 NEW CARD
USB20_P4 35
USB20_N5 39 WLAN
USB20_P5 39
USB20_N8 44 BLUETOOTH
USB20_P8 44
USB20_N9 40 WWAN
USB20_P9 40
USB20_N10 34 Fingerprint
USB20_P10 34
USB20_N11 44 External USB3
USB20_P11 44
USB20_N12 32 CAMERA
USB20_P12 32

USB_RBIAS_PN — R367 22D6R2F-L1-GP

USB_OC0# — BT_OFF — OC2# — FPR_OFF — USB_OC4# — ISO_PREP# — LANLINK_STATUS# — GPIO14

091019-1

BT_OFF 44
FPR_OFF 34
LANLINK_STATUS# 36,37,46

USB20_N12 — C871 SC33P50V2JN-3GP — C872 SC33P50V2JN-3GP — USB20_P12

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
0	1	Reserved
1	0	PCI
1	1	SPI

USE SPI

PCI_GNT0# R678 1KR2J-1-GP
PCI_GNT1# R665 1KR2J-1-GP

PCI_GNT3# R676 4K7R2J-2-GP

TPAD14-GP TP116 — INT_PIRQE# INT_PIRQF# INT_PIRQG# ACCEL_INT#
TPAD14-GP TP113

39 ACCEL_INT#

45,46 PCI_SERR#

PCI_IRDY# PCI_DEVSEL# PCI_FRAME# PCI_PLOCK# PCI_STOP# PCI_TRDY#

TPAD14-GP TP106 — ICH_PME#

PCI_PLTRST# — R339 R654 R677 22R2J-2-GP — CLK_PCI_DB_R CLK_PCI_FB_R CLK_PCI_KBC_R CLK_PCI_GOLDF CLK_PCI_TPM
TPAD14-GP TP99
TPAD14-GP TP100

CLK_PCI_DB
CLK_PCI_FB
CLK_PCI_KBC

C857 C854 C862 SC33P50V2JN-3GP — 090903-1

45 CLK_PCI_DB
15 CLK_PCI_FB
46 CLK_PCI_KBC

+3VALW

090821-1-SI U46 AND GATE — 74LVC1G08GW-1-GP

PCI_PLTRST# — PLT_RST# — PLT_RST# 5,26,35,36,39,45

R362 0R2J-2-GP DY
R357 100KR2J-1-GP DY

RP2 SRN10KJ-L3-GP

19,36 CLK_PCIE_LAN_REQ#
091019-1 OC2# USB_OC4#
ISO_PREP#
CLKREQ_WWAN# 19

RP3 SRN10KJ-L3-GP

GPIO14
19,39 WLAN_TRANSMIT_OFF#
PCH_GPIO12 19
PCH_GPIO24 19
USB_OC0#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	

Low = A16 swap override/Top-Block Swap Override enabled
High = Default

<Core Design>

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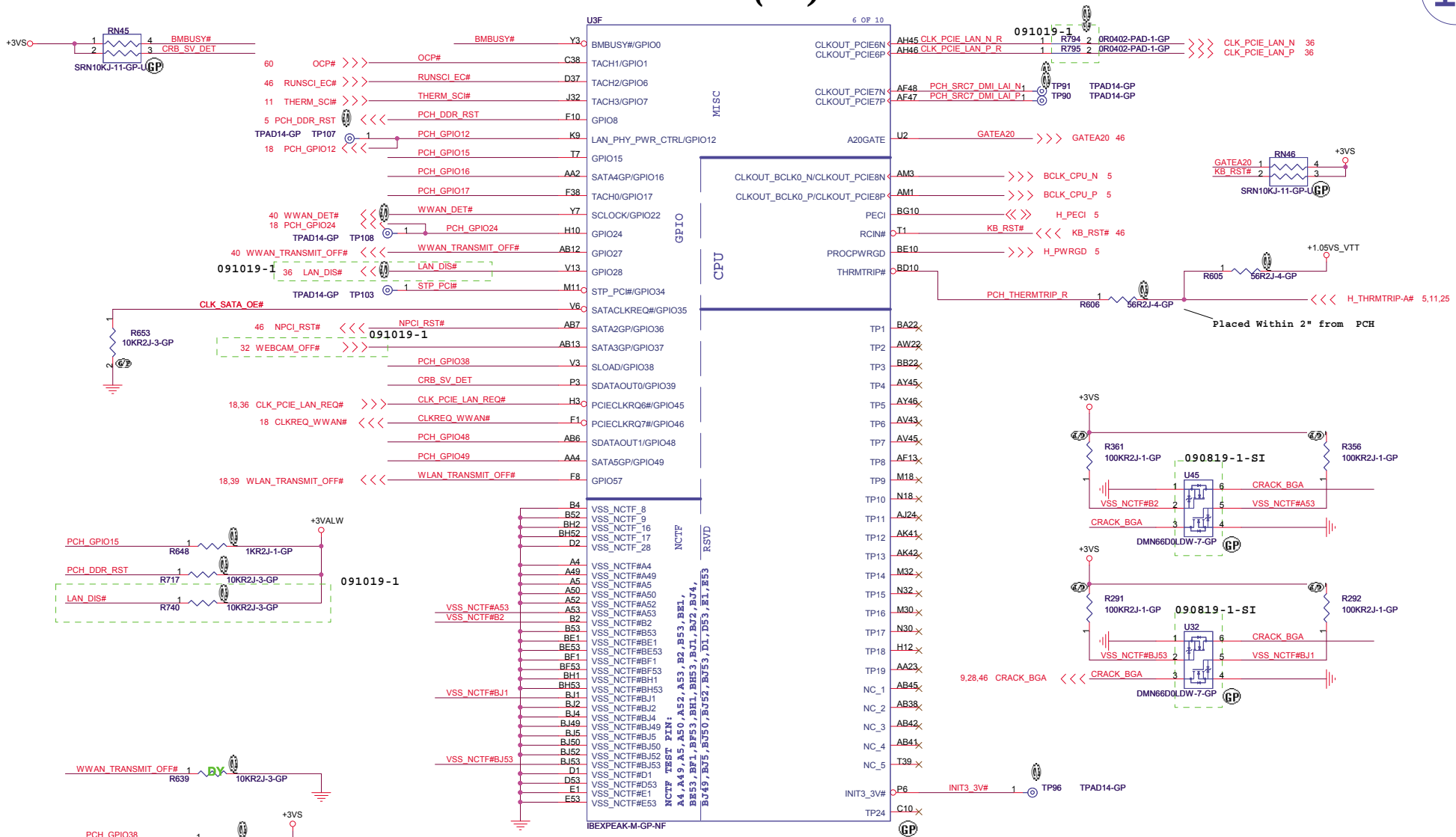
Title: PCH (5/9)-PCI/USB

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 18 of 62

PCH(6/9)



<Core Design>

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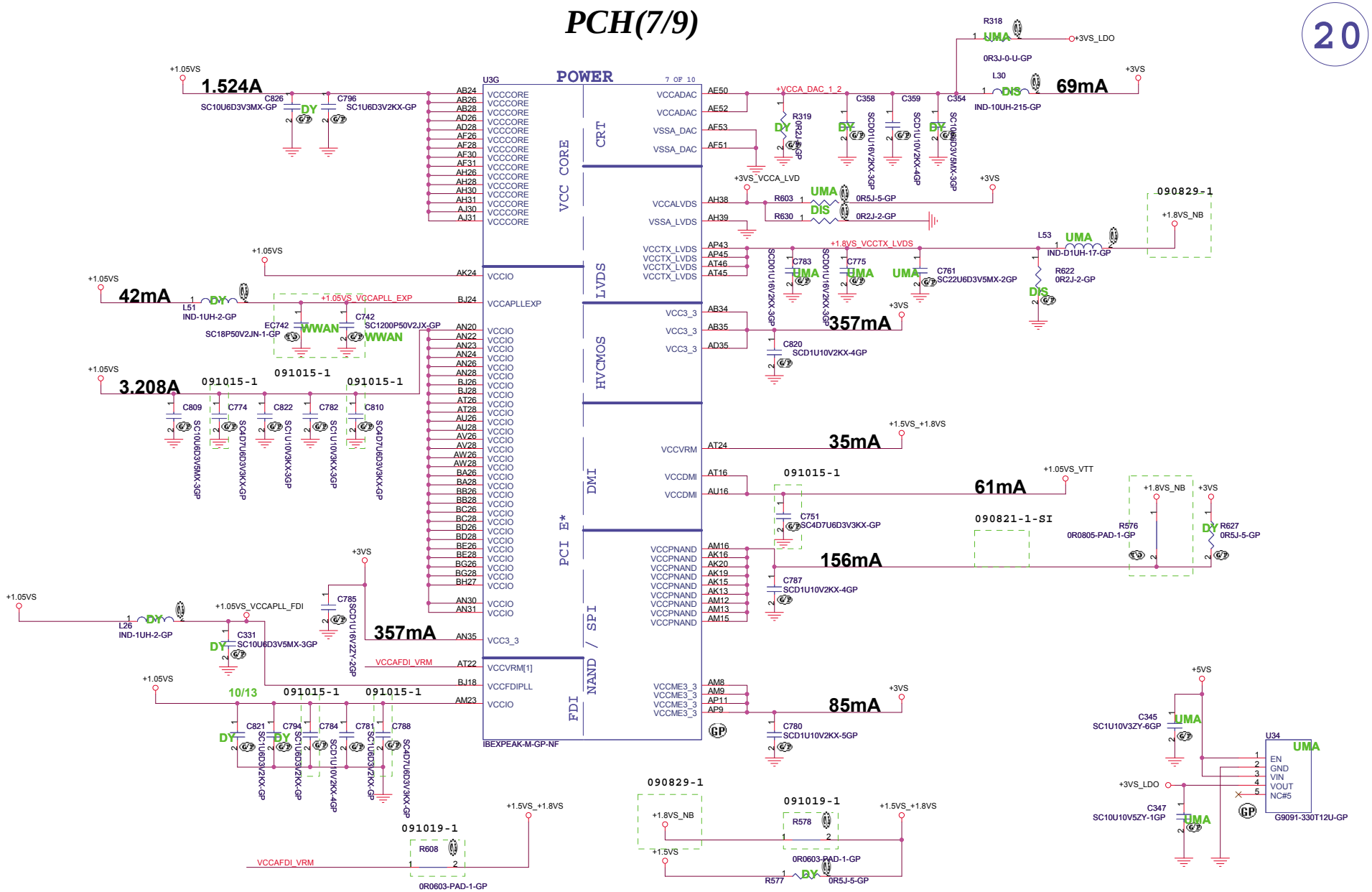
Title: PCH (6/9)-GPIO

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 19 of 62

PCH(7/9)



<Core Design>

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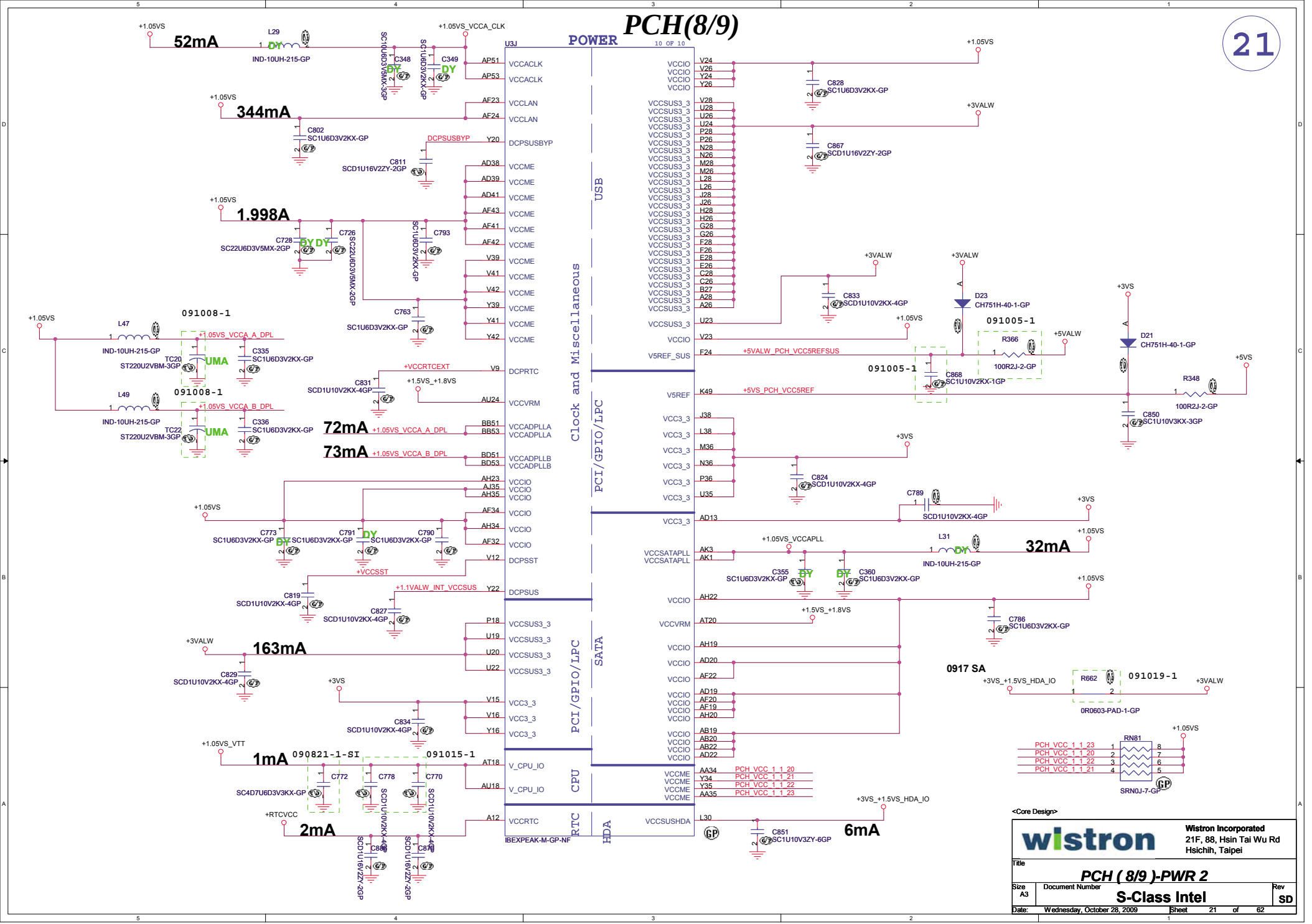
Title: PCH (7/9)-PWR 1

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 20 of 62

PCH(8/9)



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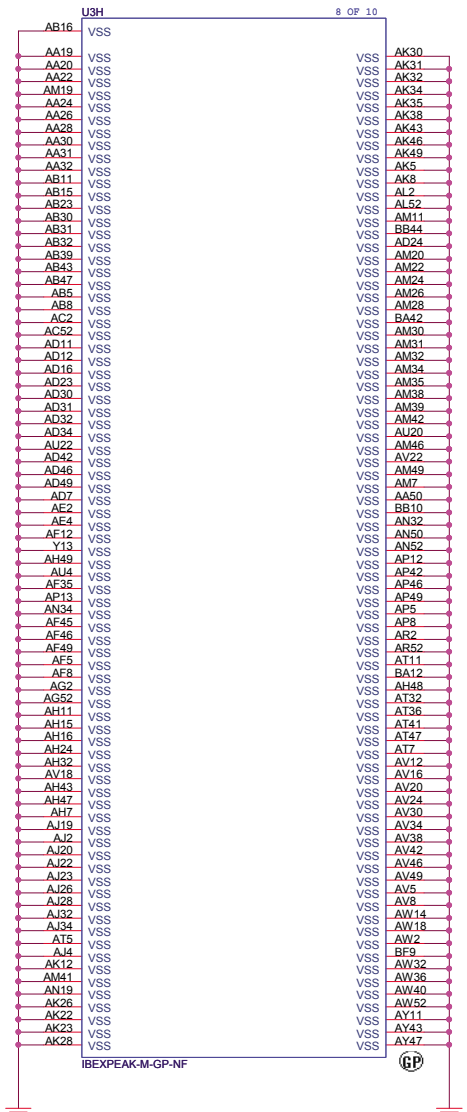
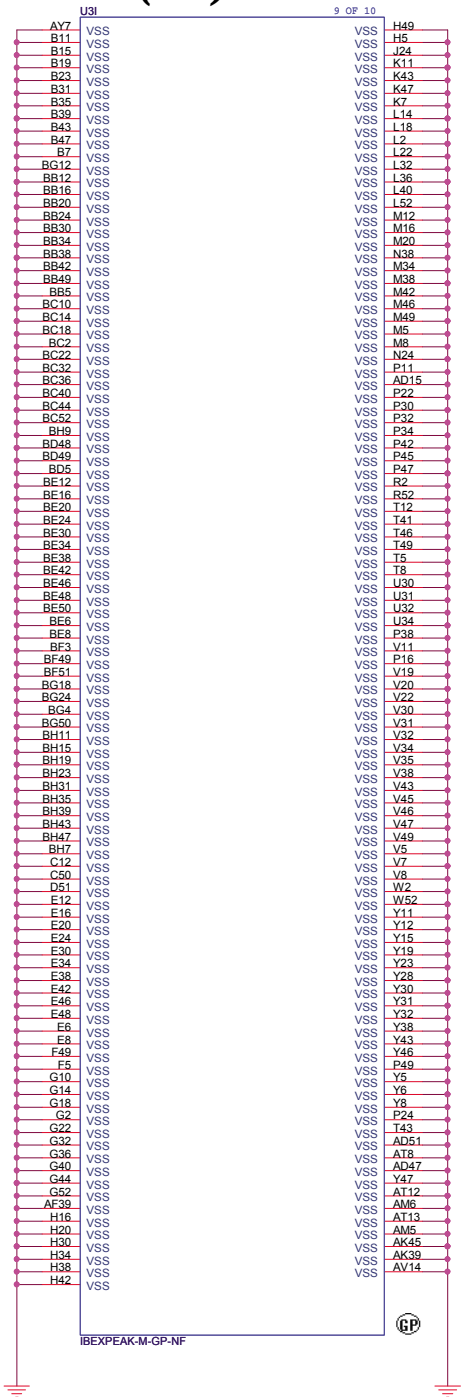
Title	PCH (8/9)-PWR 2
Size A3	Document Number S-Class Intel
Rev	SD
Date: Wednesday, October 28, 2009	Sheet 21 of 62

PCH(9/9)





<Core Design>

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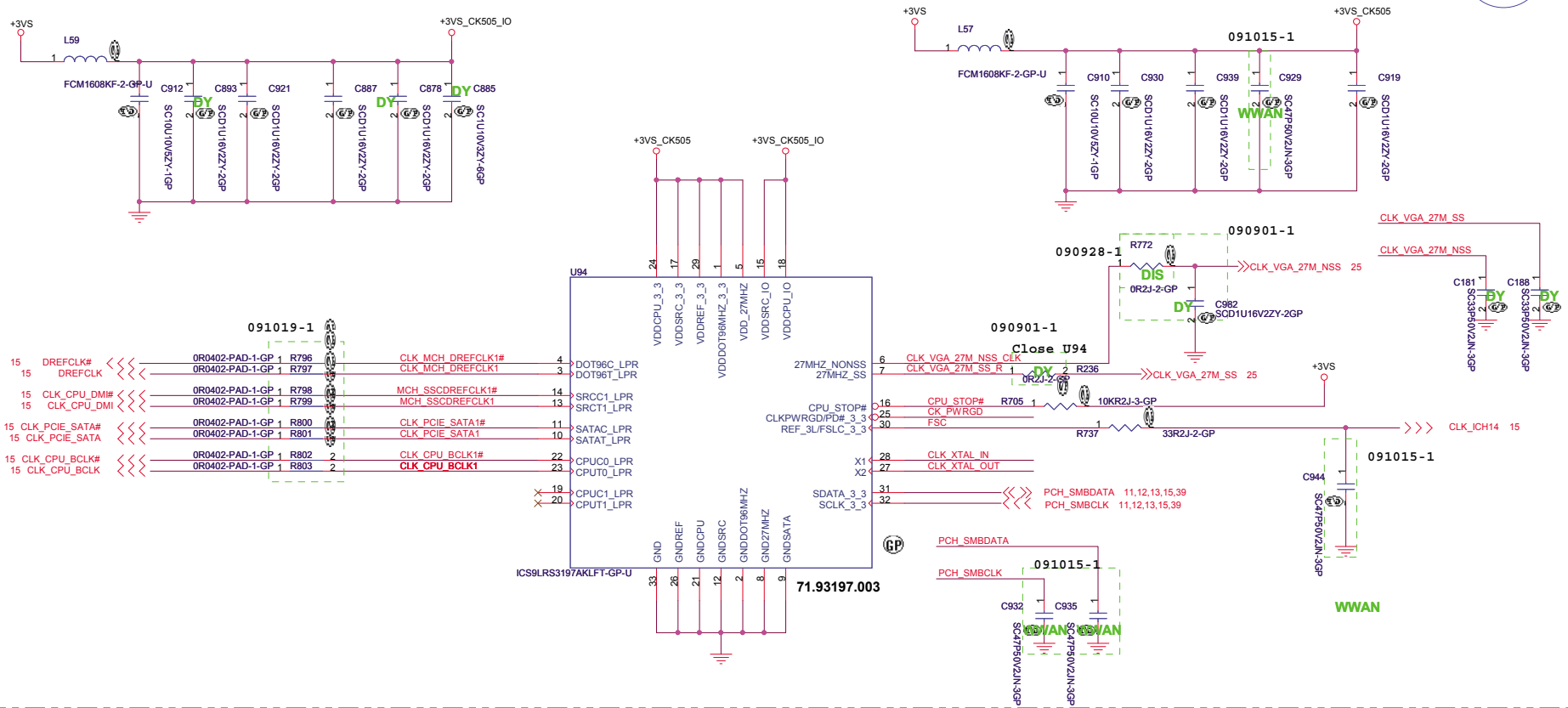
Title: PCH (9/9)-VSS

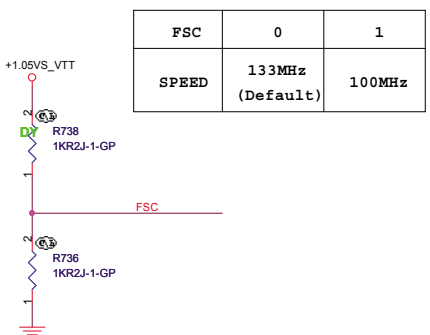
Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 22 of 62

CLOCK GENERATOR

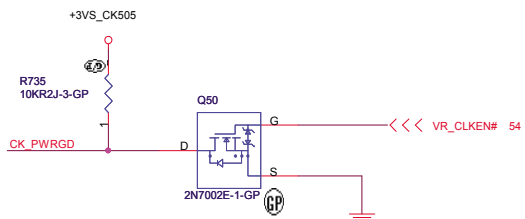


FSB Frequency Select

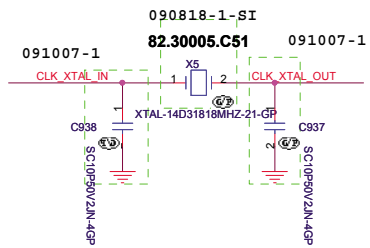


FSC	0	1
SPEED	133MHz (Default)	100MHz

Clock Gen. Eable



Clock Gen. Crystal



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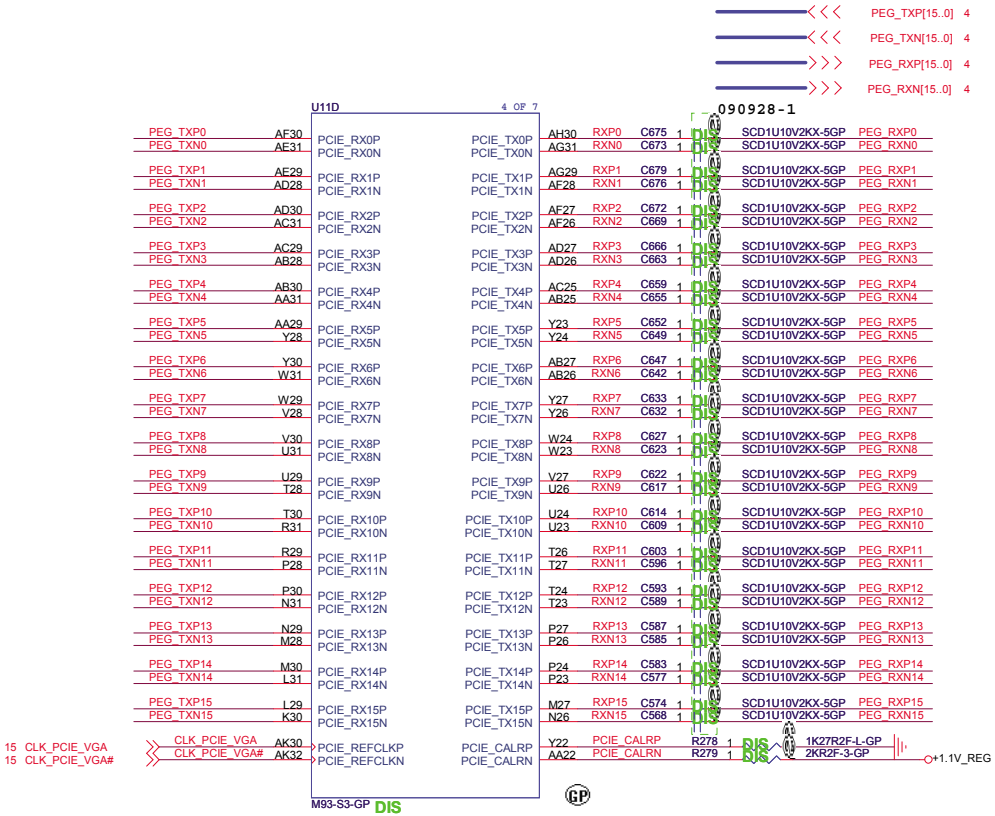
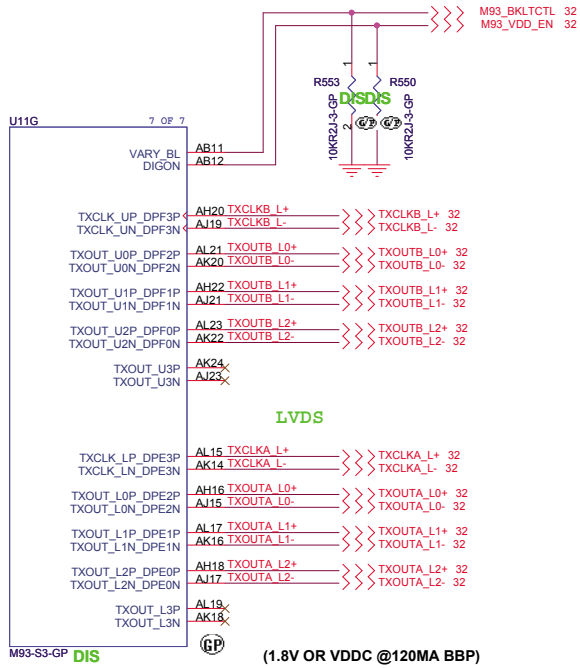
Title: Clock Generator ICS9LRS3197

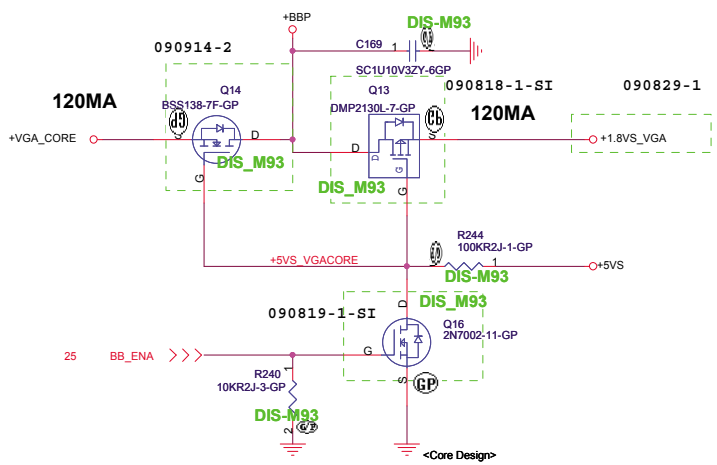
Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 23 of 62

M93 GPU(1/5)







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Hsichih, Taipei

Title: VGA-PCIE/LVDS(1/5)

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 24 of 62

M93 GPU(2/5)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
X = DESIGN DEPENDANT
N/A = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM ID CFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 XX

090824-1-SI

VRAM ID:
BIT0 --> L:Quanta ; H:Wistron
BIT1 --> L:512M ; H:1GB
BIT2 --> L:Samsung ; H:Hynix
BIT3 -->N/A

090829-1 — VRAM ID — 090824-1-SI

+1.8VS_VGA	R283	DIS	10KR2J-3-GP	VRID_0	R570	DIS	10KR2J-3-GP	
	R284	DIS	10KR2J-3-GP	VRID_1	R569	DIS	10KR2J-3-GP	
	R281	DIS	10KR2J-3-GP	VRID_2	R572	DIS	10KR2J-3-GP	
	R282	DIS	10KR2J-3-GP	VRID_3	R571	DIS	10KR2J-3-GP	

M93 LP: VDDC=0.9/1.1V

GPIO20_VID1	GPIO15_VID0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

Aperture Conig. PIN	M93S3 GPIO	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG0	GPIO_11	R243	0	0	1
CONFIG1	GPIO_12	R246	1	0	0
CONFIG2	GPIO_13	R250	0	0	0

VRID 3210	Vendor	Type	Vendor P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12

LVDS — 32 DDC2_CLK, 32 DDC2_DATA — 091019-1 — R0402-PAD-1-GP R804, R805 — GPU_LVDS_SCL, GPU_LVDS_SDA

091008-1 — 090820-1-SI — D39 1SS355PT-GP — 16,36,46 AC_PRESENT — DDC2_CLK, DDC2_DATA — 32 M93_BKLT_EN — C177, C182

090820-1-SI — Q15 2N7002E-1-GP — R245 H_THRMTRIP-A# — 5,11,19 H_THRMTRIP-A# — GPU_CTF — 59 GPIO15_VID0, 23 CLK_VGA_27M_SS, 59 GPIO20_VID1, 24 BB_ENA

090901-1 — 091001-1 — M93_HPD3

GPIO0 GPIO1 GPIO2 GPIO3_SMBDATA GPIO4_SMBCLK GPIO5_ACBATT GPIO6 GPIO7_BLON GPIO8_ROMSO GPIO9_ROMSI GPIO10_ROMSCK GPIO11 GPIO12 GPIO13 GPIO14_HPD2 GPIO15_PWRCNTL0 GPIO16_SSIN GPIO17_THERMAL_INT GPIO18_HPD3 GPIO19_CTF GPIO20_PWRCNTL1 GPIO21_BB_EN GPIO22_ROMCS# GPIO23_CLKREQ#

090903-1 — R243 GPIO11, R246 GPIO12, R250 GPIO13, R237 GPIO23_CLKREQB, R255 GPIO5, R241 GPU_CTF, R552 M93_HPD2, R551 M93_HPD3, R548 M93_HPD4

RN16 — GPIO0 GPIO1 GPIO2 GPIO8 GPIO9 GPIO22 GENERICA — SRN10KJ-L-3-GP

RN15 — GENERICB GENERICC — SRN10KJ-11-GP-U

090829-1 — R565 499R2F-2-GP — VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V) — R561 249R2F-2-GP — C705 SCD1U10V2KX-4GP — 28 GPU_TESTEN#2 — GPU_TESTEN#2

R517 10KR2J-3-GP — JTAG_TRSTB, JTAG_TDI, JTAG_TCK, JTAG_TMS, JTAG_TDO — TPAD14-GP TP71 TP72 TP69 TP67

R277 5K11R2F-L1-GP — TESTEN — R275 5K11R2F-L1-GP

GENERICA GENERICB GENERICC GENERICD GENERICE_HPD4 — M93_HPD4 — 33 HDMI_M93_HPD — HPD1

090829-1 — 23 CLK_VGA_27M_NSS — R232 121R2F-GP — R233 147R2F-GP — VOLTAGE DIVIDER TO MAKE XTALIN VOLTAGE LEVEL OF 1.8V — 3.3V => 147 ohm — CLK_VGA_27M_NSS_R

090824-1-SI — TPAD14-GP TP15 TP16 TP17 — M93_DXP1_R M93_DXN1_R — XTALOUT_M93 — XTALIN XTALOUT — DPLUS DMINUS

DPLL_PVDD, DPLL_VDDC — TSVDD — R5 — TS_FDO TSVDD TSVSS

(1.8V @ 120MA DPLL_PVDD) — 090829-1 — L40 BLM18PG471SN1D-GP — 470R_1000mA — C719 C706 C670 — DPLL_PVSS

(1.1V @300MA DPLL_VDDC) — +1.1V_REG — L17 BLM18PG471SN1D-GP — 470R_1000mA — C277 C268 C661 — DPLL_PVSS

091019-1 — L24 BLM15BD121SS1D-GP — (1.8V @20MA TSVDD) — C307 C300 C298 — TSVSS

090820-1-SI — +3VS — RN93 SRN2KZJ-1-GP — 090903-1 — +3VS — U100 DMN66D0LDW-7-GP — GPIO3_SMBDATA — GPIO3_SMBCLK — SML1DAT_KBC 15,46 — SML1CLK_KBC 15,46

U11E — 5 OF 7

DVCNTL0	AE9	DVCNTL0	
DVCNTL1	L9	DVCNTL1	
DVCNTL2	N9	DVCNTL2	
VRID_0	Y7	DVDATA0	
VRID_1	Y8	DVDATA1	
VRID_2	AB2	DVDATA2	
VRID_3	AB4	DVDATA3	
DVDATA4	AB7	DVDATA4	
DVDATA5	AB8	DVDATA5	
DVDATA6	AB9	DVDATA6	
DVDATA7	AC7	DVDATA7	
DVDATA8	AC8	DVDATA8	
DVDATA9	AD7	DVDATA9	
DVDATA10	AC10	DVDATA10	
DVDATA11	AD9	DVDATA11	
DVDATA12	AE8	DVDATA12	
		SCL	R1
		SDA	R3
		GPIO0	U6
		GPIO1	U10
		GPIO2	T10
		GPIO3_SMBDATA	U8
		GPIO4_SMBCLK	U7
		GPIO5_ACBATT	T9
		GPIO6	T8
		GPIO7_BLON	T7
		GPIO8_ROMSO	P10
		GPIO9_ROMSI	P4
		GPIO10_ROMSCK	P2
		GPIO11	N6
		GPIO12	N5
		GPIO13	N3
		GPIO14_HPD2	Y9
		GPIO15_PWRCNTL0	N1
		GPIO16_SSIN	M4
		GPIO17_THERMAL_INT	R6
		GPIO18_HPD3	W10
		GPIO19_CTF	M2
		GPIO20_PWRCNTL1	P8
		GPIO21_BB_EN	P7
		GPIO22_ROMCS#	N8
		GPIO23_CLKREQ#	N7
		JTAG_TRST#	L6
		JTAG_TDI	L5
		JTAG_TCK	L3
		JTAG_TMS	L1
		JTAG_TDO	K4
		TESTEN	AF24
		GENERICA	AB13
		GENERICB	W8
		GENERICC	W9
		GENERICD	W7
		GENERICE_HPD4	AD10
		HPD1	AC14
		VREFG	AC16
DPLL_PVDD	AF14	DPLL_PVDD	
DPLL_PVSS	AE14	DPLL_PVSS	
DPLL_VDDC	AD14	DPLL_VDDC	
		XTALIN	AM28
		XTALOUT	AK28
		DPLUS	AF17
		DMINUS	AE17
TS_FDO	AD17	TSVDD	
TSVSS	AC17		
		M93-S3-GP	

HDMI

TX2P_DPA0P	AK3	HDMI_DPA0P	33
TX2M_DPA0N	AK1	HDMI_DPA0N	33
TX1P_DPA1P	AH3	HDMI_DPA1P	33
TX1M_DPA1N	AH1	HDMI_DPA1N	33
TX0P_DPA2P	AG3	HDMI_DPA2P	33
TX0M_DPA2N	AG5	HDMI_DPA2N	33
TXCAP_DPA3P	AF2	HDMI_DPA3P	33
TXCAM_DPA3N	AF4	HDMI_DPA3N	33
TX5P_DPB0P	AK8		
TX5M_DPB0N	AL7		
TX4P_DPB1P	AJ7		
TX4M_DPB1N	AH8		
TX3P_DPB2P	AK6		
TX3M_DPB2N	AM5		
TXCBP_DPB3P	AK5		
TXCBM_DPB3N	AM4		
TX2P_DPC0P	AA3		
TX2M_DPC0N	Y2		
TX1P_DPC1P	Y4		
TX1M_DPC1N	W5		
TX0P_DPC2P	W3		
TX0M_DPC2N	V2		
TXCCP_DPC3P	V4		
TXCCM_DPC3N	U5		

CRT

R	AM26	M93_RED	
RB	AK26	M93_RB	
G	AL25	M93_GREEN	
GB	AJ25	M93_GB	
B	AH24	M93_BLUE	
BB	AG25	M93_BB	
HSYNC	AH26	M93_VGA_HSYNC	31
VSYNC	AJ27	M93_VGA_VSYNC	31
RSET	AD22	VGA_RSET	R530 499R2F-2-GP
AVDD	AG24	AVDD	
AVSSQ	AE22		
VDD1DI	AE23	M93_AGND	VDD1_DI
VSS1DI	AD23		

NC#AM12_R2	AM12	R532 0R2J-2-GP	
NC#AK12_R2B	AK12		
NC#AL11_G2	AL11	M93_AGND	
NC#AJ11_G2B	AJ11		
NC#AK10_B2	AK10		
NC#AL9_B2B	AL9		
NC#AH12_C	AH12		
NC#AM10_Y	AM10		
NC#AJ9_COMP	AJ9		
H2SYNC	AL13	DAC2_HSYNC	
V2SYNC	AJ13	DAC2_VSYNC	RN20 SRN10KJ-11-GP-U
NC#AD19_VDD2DI	AD19	VDD2_DI	
NC#AC19_VSS2DI	AC19		
NC#AE20_A2VDD	AE20	A2VDD	
NC#AE17_A2VDDQ	AE17	A2VDDQ	
A2VSSQ	AE19	M93_AGND	
NC#AG13_R2SET	AG13	VGA_R2SET	R544 715R2F-GP
DDC1CLK	AE6	DDC1_CLK	33
DDC1DATA	AE5	DDC1_DATA	33
AUX1P	AD2		
AUX1N	AD4		
DDC2CLK	AC11		
DDC2DATA	AC12		
AUX2P	AD13		
AUX2N	AD11		
RSVD#AB22	AB22	RSVD#AB22	RN86 SRN0J-10-GP-U
RSVD#AC22	AC22	RSVD#AC22	
DDCCLK_AUX5P	AE16		
DDCDATA_AUX5N	AD16		
DDC6CLK	AC1	DDC6_CLK	31
DDC6DATA	AC3	DDC6_DATA	31
DDCCLK_UX3P	AD29		
DDCDATA_AUX3N	AC29		

HDMI — 090820-1-SI

CRT — 090820-1-SI

M93_VGA_HSYNC, M93_VGA_VSYNC — RN18 SRN10KJ-11-GP-U — +3.3V_DELAY

DO NOT INSTALL for M93-S3
Only for PARK-S3

(1.8V @ 70MA AVDD) — AVDD — SCD1U10V2KX-4GP — SC10U6D3V3MX-GP — L25 BLM15BD121SS1D-GP — 091019-1 — 090829-1 — +1.8VS_VGA

(1.8V @ 45MA VDD1DI) — VDD2_DI — VDD1_DI — R568 0R2J-2-GP — DIS_PARK — L41 BLM15BD121SS1D-GP — C696 C703 C714 — SC10U6D3V2KX-GP

(1.8V @ 2MA A2VDDQ) — A2VDDQ — L48 BLM18BD121SS1D-GP — C727 C724 C730 — DIS_PARK

(3.3V @ 65MA A2VDD) — A2VDD — R274 0R2J-2-GP — DIS_PARK — +3.3V_DELAY

M93_RED 17, M93_GREEN 17, M93_BLUE 17 — R546 R547 — 0R2J-2-GP

+3VS — Q23 DMP2130L-7-GP — R298 100KR2J-1-GP — DIS_M93 — +3VS_3.3V_DELAY

R299 0R2J-2-GP — DIS_PARK — 090818-1-SI

090819-1-SI — Q22 2N7002-11-GP — R302 R304 R301 0R2J-2-GP — C342 SCD1U16V2ZY-2GP — DIS_M93

49,58 VTT_EN — SLP_S3# — 16,35,36,46,48,49,52,56,57,58,59

Optional RC network to fine tune PWR SEQ.

<Core Design>

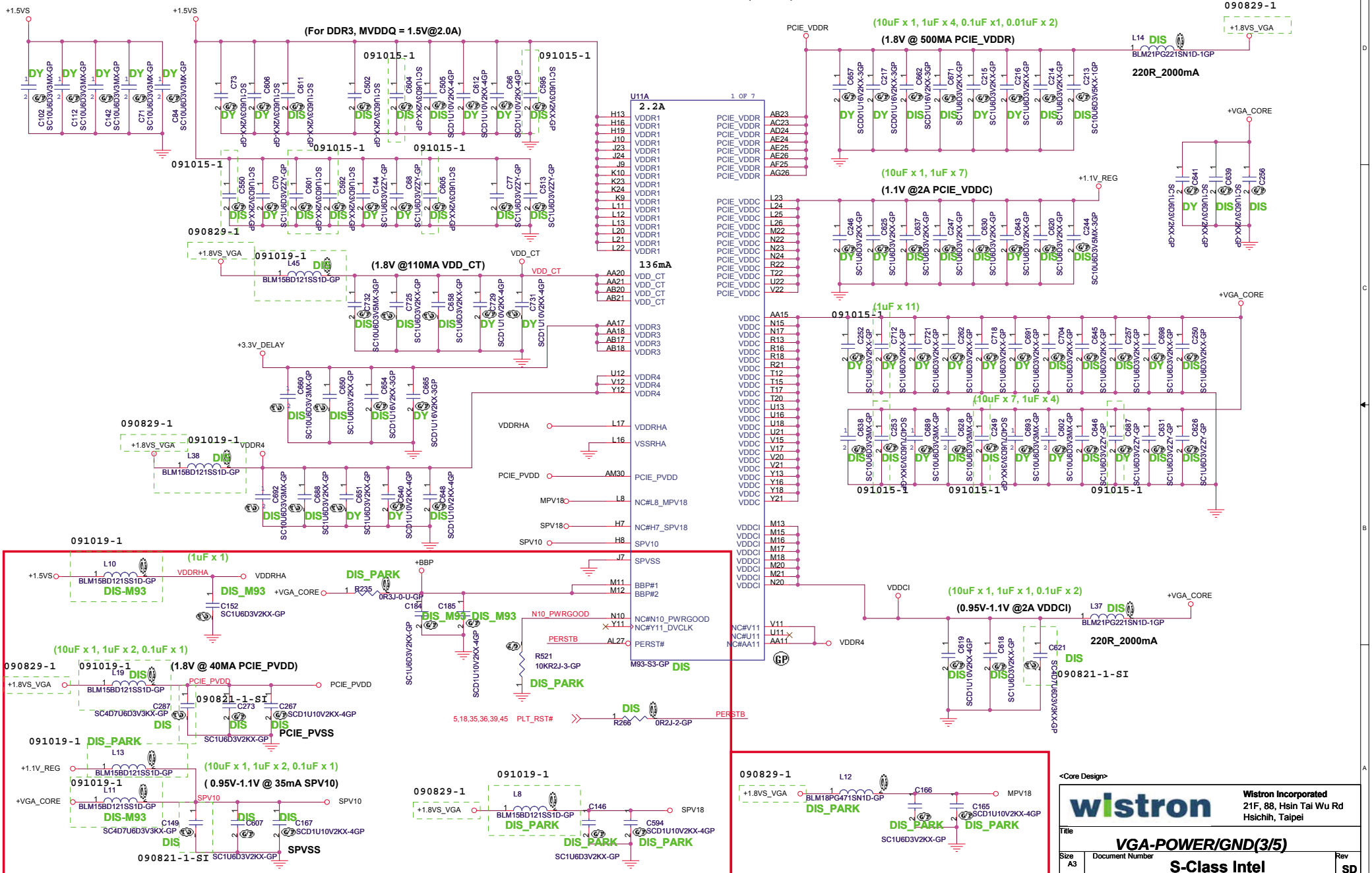
wistron — Wistron Incorporated, 21F, 88, Hsin Tai Wu Rd, Hsichih, Taipei

Title: LCD/CRT/HDMI PORT(2/5)

Size: A2 | Document Number: S-Class Intel | Rev: SD

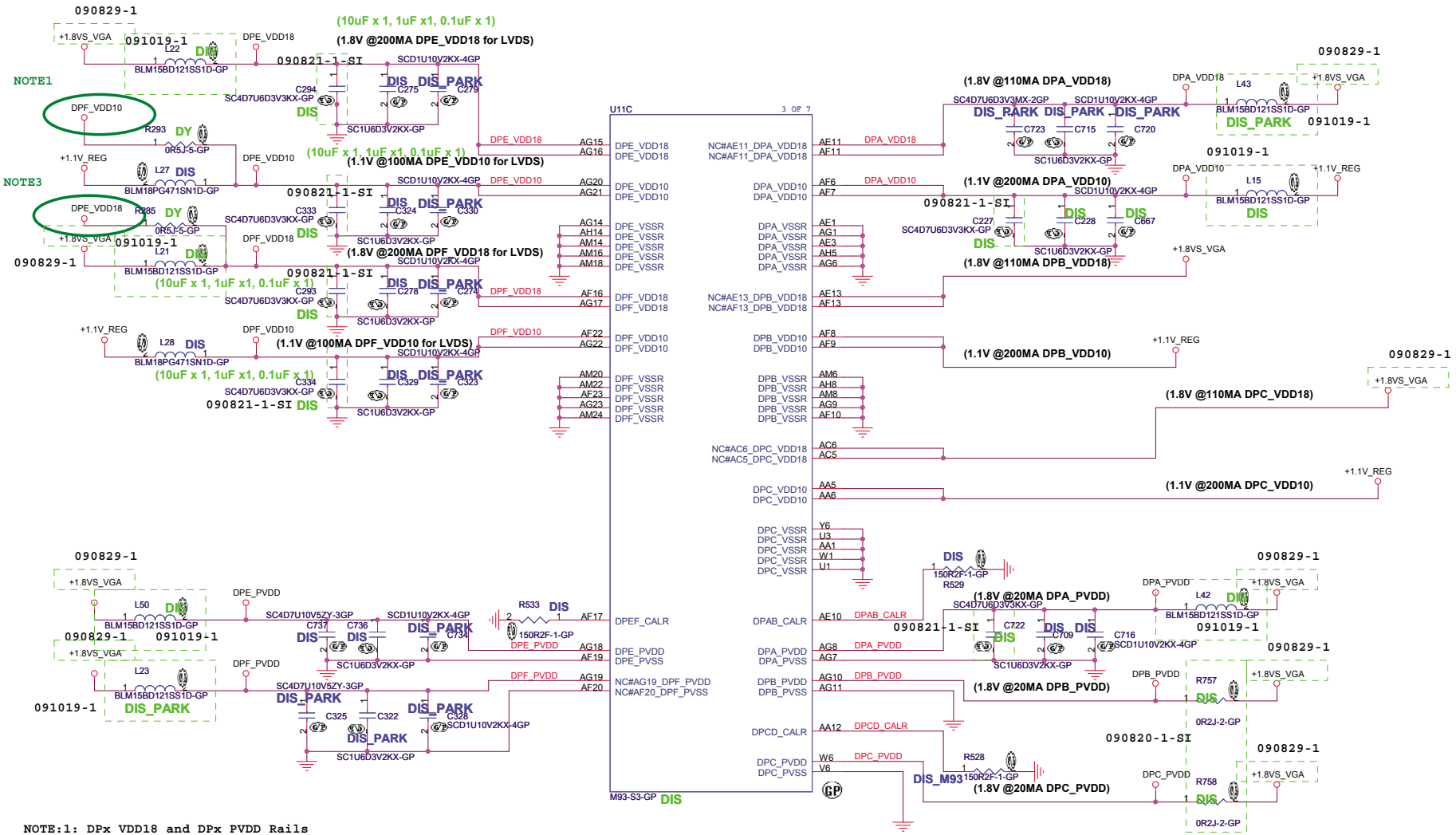
Date: Wednesday, October 28, 2009 | Sheet 25 of 62

M93 GPU(3/5)



Wistron Incorporated	21F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	VGA-POWER/GND(3/5)
Size A3	Document Number S-Class Intel
Rev	SD
Date: Wednesday, October 28, 2009	Sheet 26 of 62

M93 GPU(4/5)



NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEADfor one rail of each pair if signal integrity for DP lanes are OK.
We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove DecouplingCapacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK.
We need at least 500mA Bead to supportjoin rails.

<Core Design>

wistron

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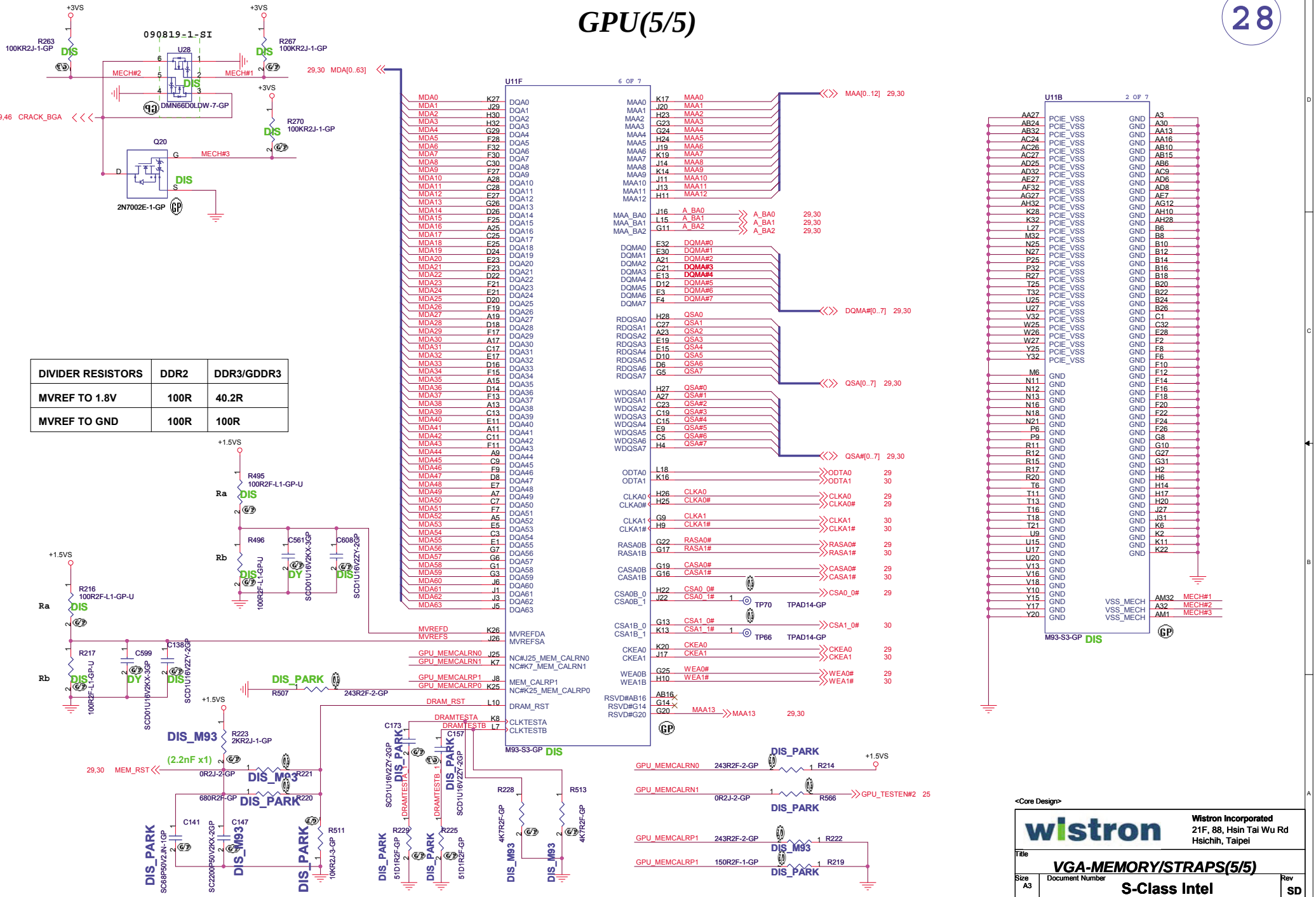
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-POWER/GND(4/5)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 27 of 62

GPU(5/5)



DIVIDER RESISTORS	DDR2	DDR3/GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-MEMORY/STRAPS(5/5)

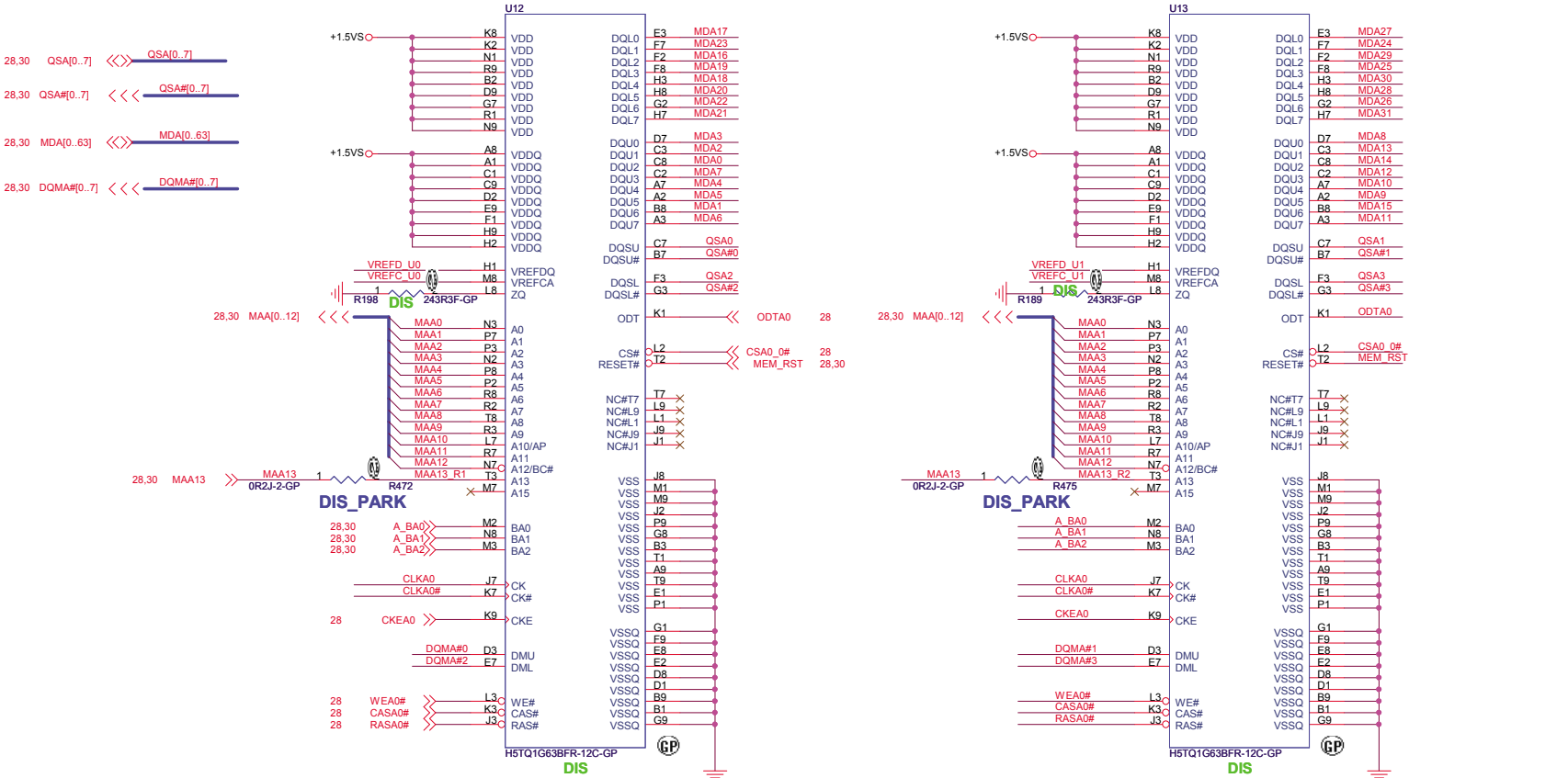
Size: A3 | Document Number: S-Class Intel | Rev: SD

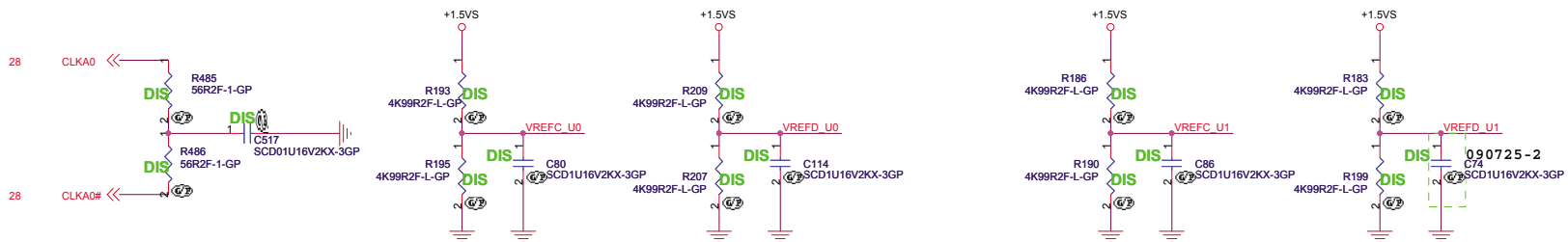
Date: Wednesday, October 28, 2009 | Sheet 28 of 62

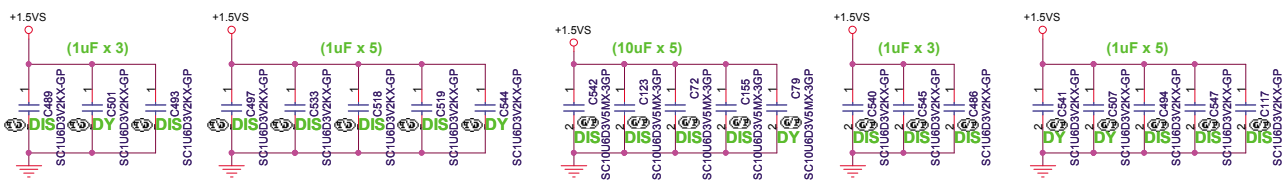
VRAM DDR3 (1/2)

256MB/512MB DDR3

29







<Core Design>

wistron

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VGA-MEMORY/STRAPS(2/4)

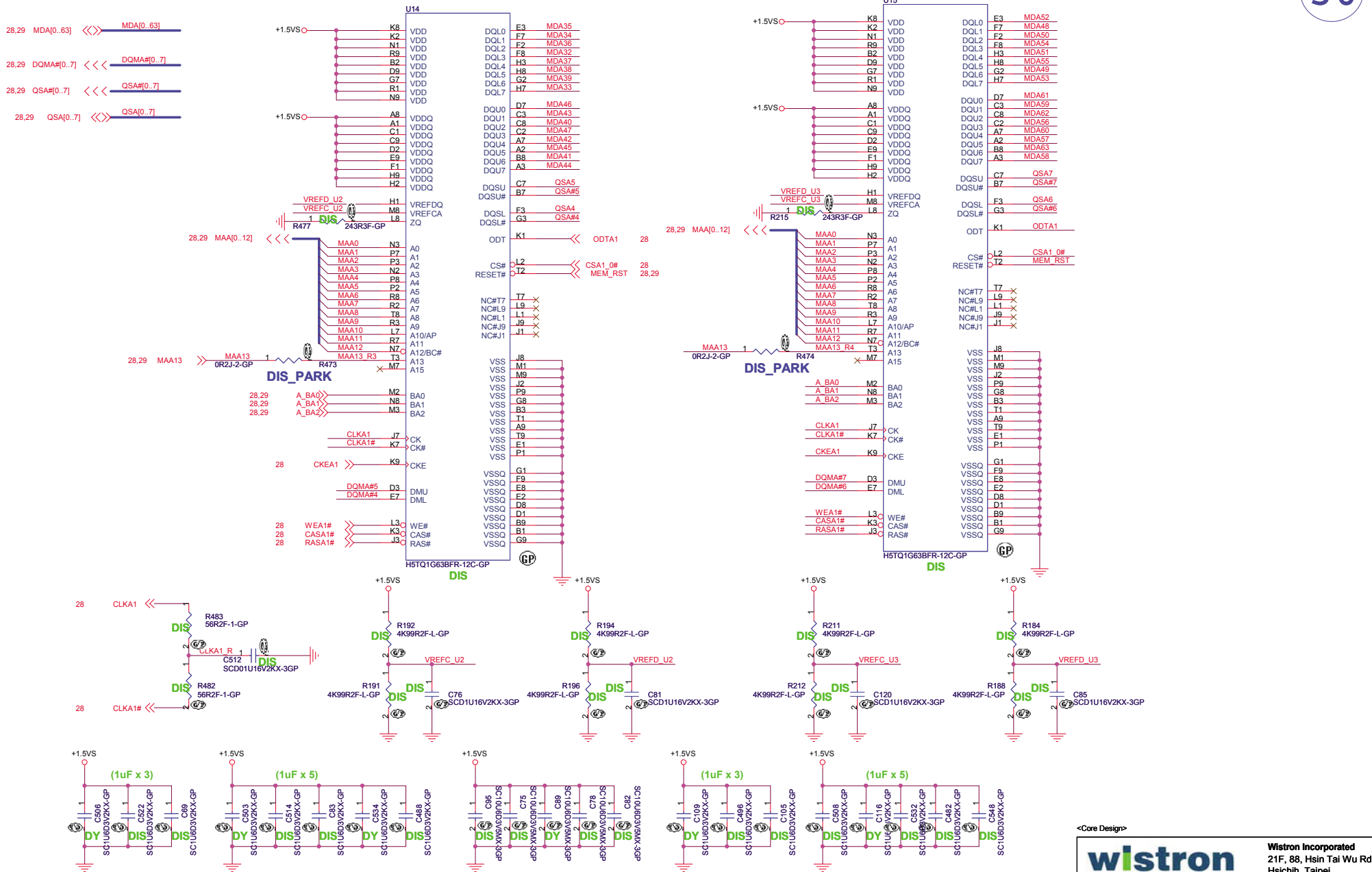
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 29 of 62

VRAM DDR3 (2/2)

256MB/512MB DDR3

30



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

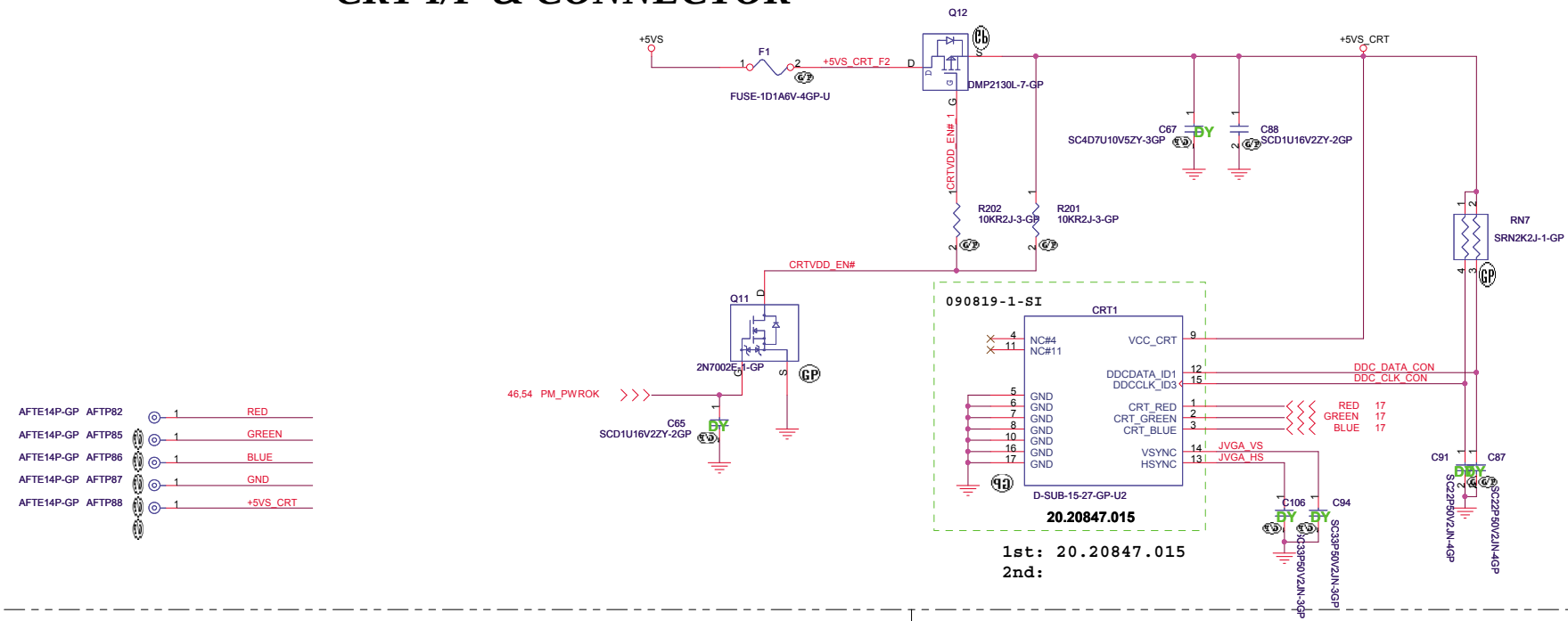
Title: VGA-MEMORY/STRAPS(4/4)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 30 of 62

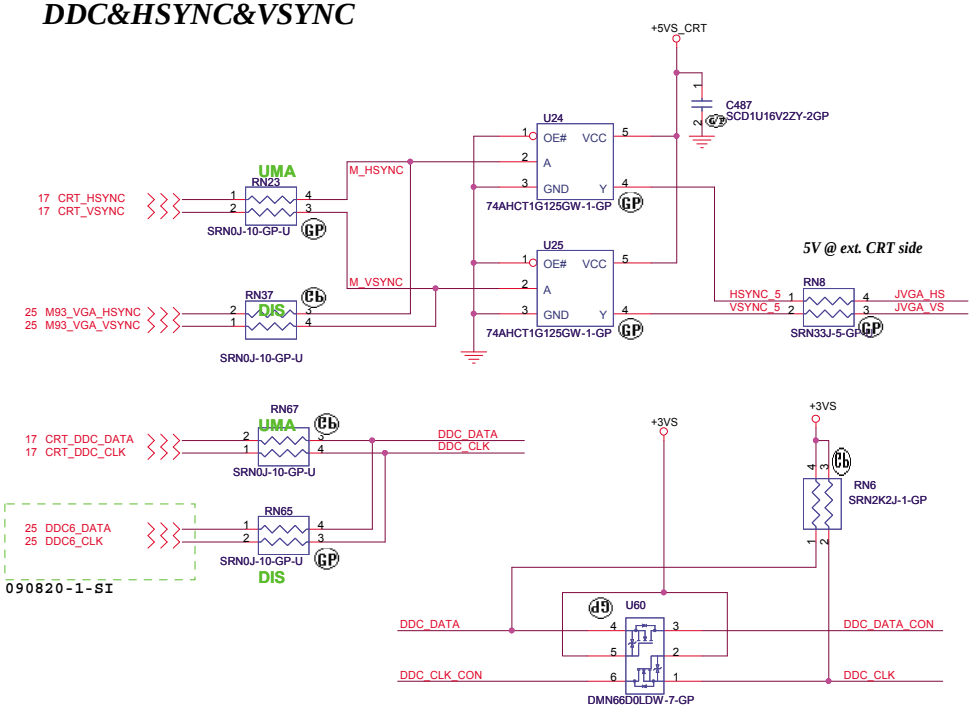
CRT I/F & CONNECTOR

31

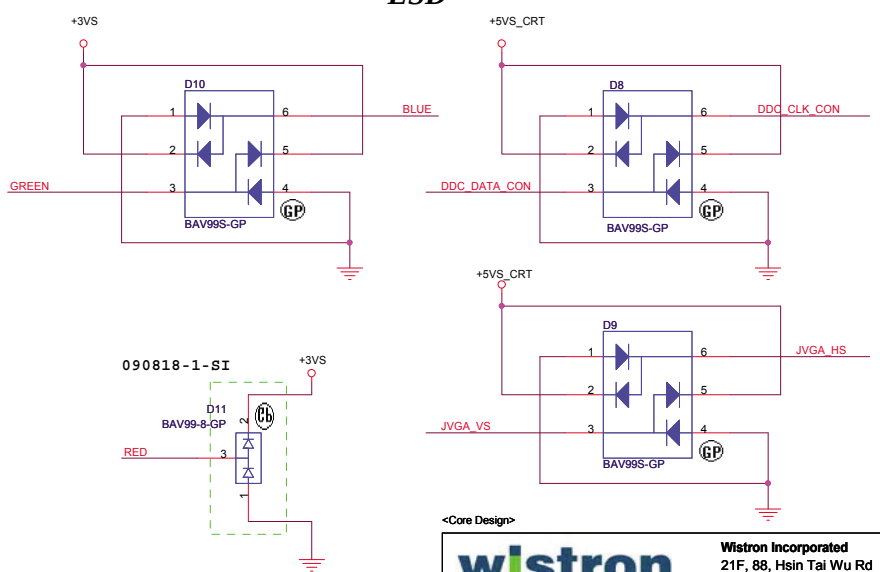


1st: 20.20847.015
2nd:

DDC&HSYNC&VSYNC



ESD



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CRT Connector

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 31 of 62

LVDS CONNECTOR

LCD / INVERTER INTERFACE / CAMERA

20.F1619.040

1st: 20.F1619.040

2nd:

	SIZE_DET0 (Pin17)
17.3"	0
15.6"	1

Camera Power&Interface

LCD Power&Discharge

<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

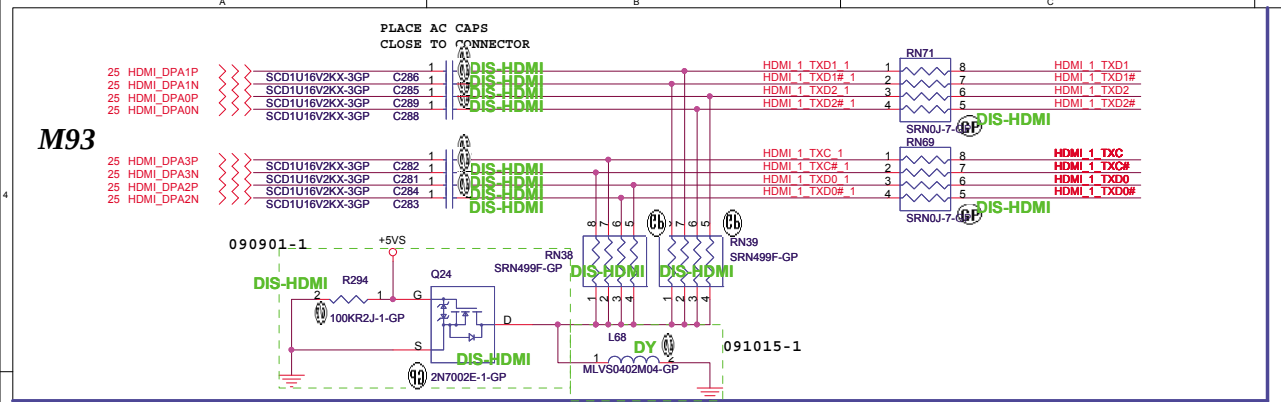
Title: LCD/Inverter Connector/CAM/LED

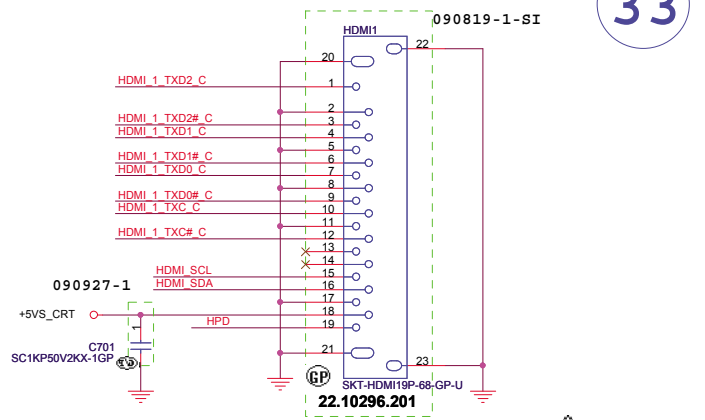
Size: Custom | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 32 of 62

HDMI CONNECTOR

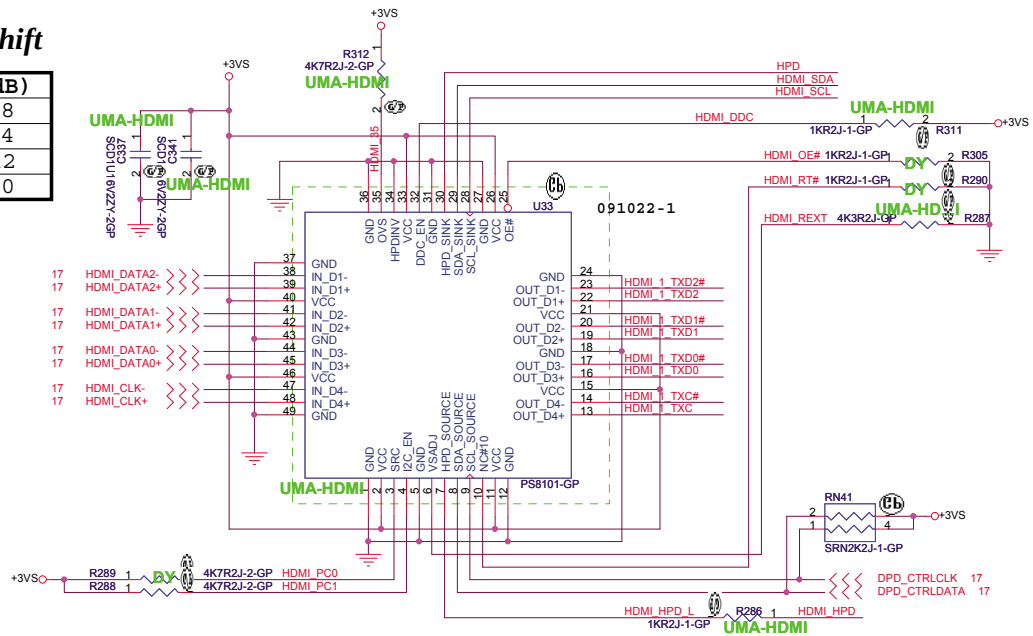
33



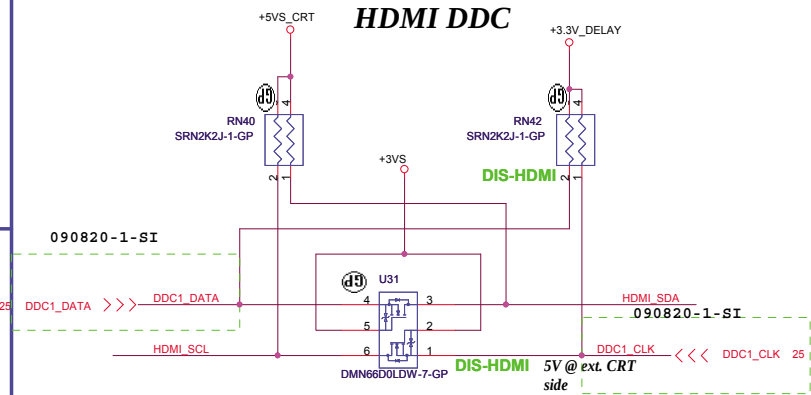


PCH Level Shift

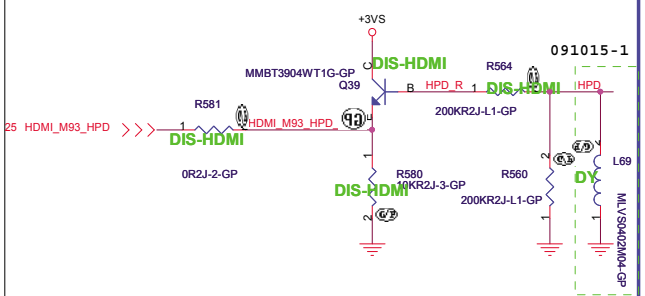
PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0



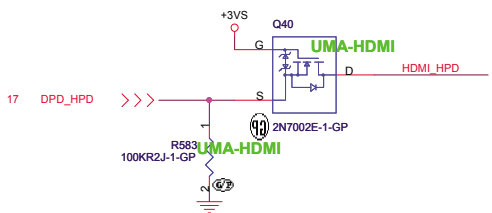
HDMI DDC



DIS HPD



UMA HPD



<Core Design>

wistron

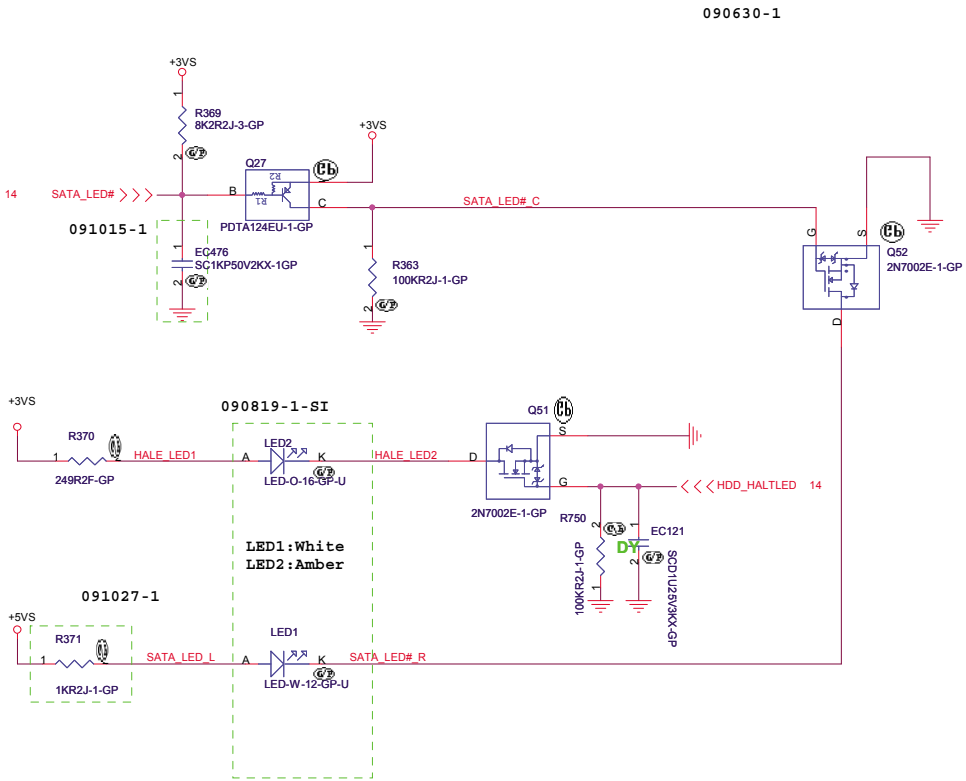
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDMI CONN.

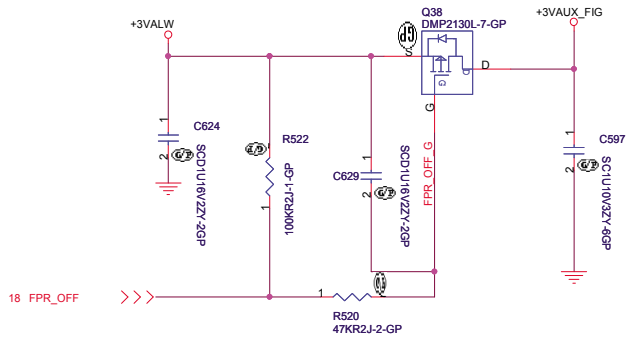
Size	Document Number	Rev
A3	S-Class Intel	SD

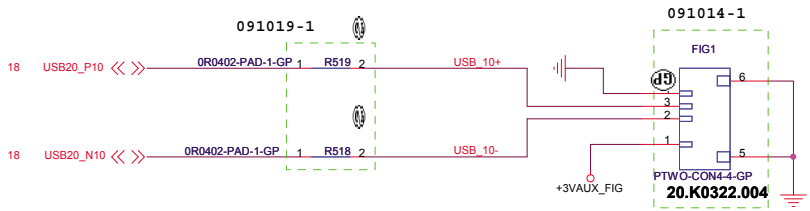
Date: Wednesday, October 28, 2009 Sheet 33 of 62

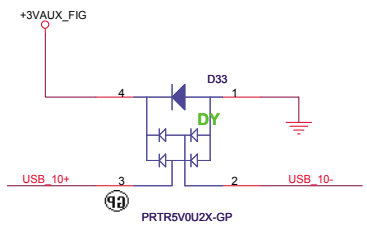
SATA LED FOR HDD

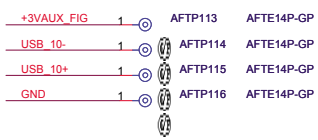


Fingerprint









<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SATA&CAP LED&GOLDEN FINGER

Size: A3 | Document Number: S-Class Intel | Rev: SD

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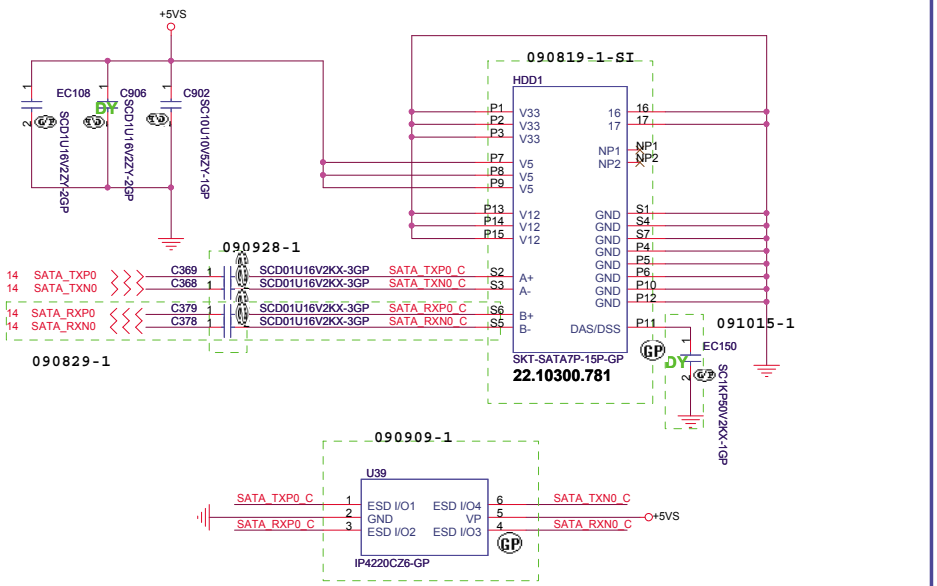
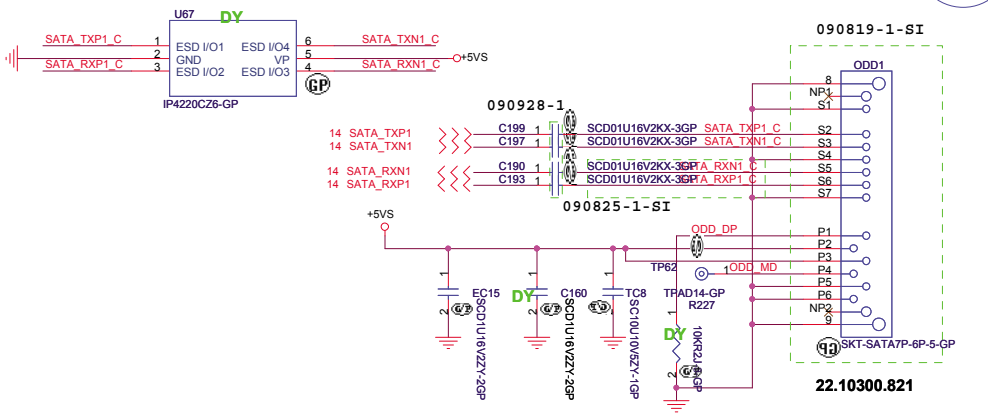
SATA HD Connector

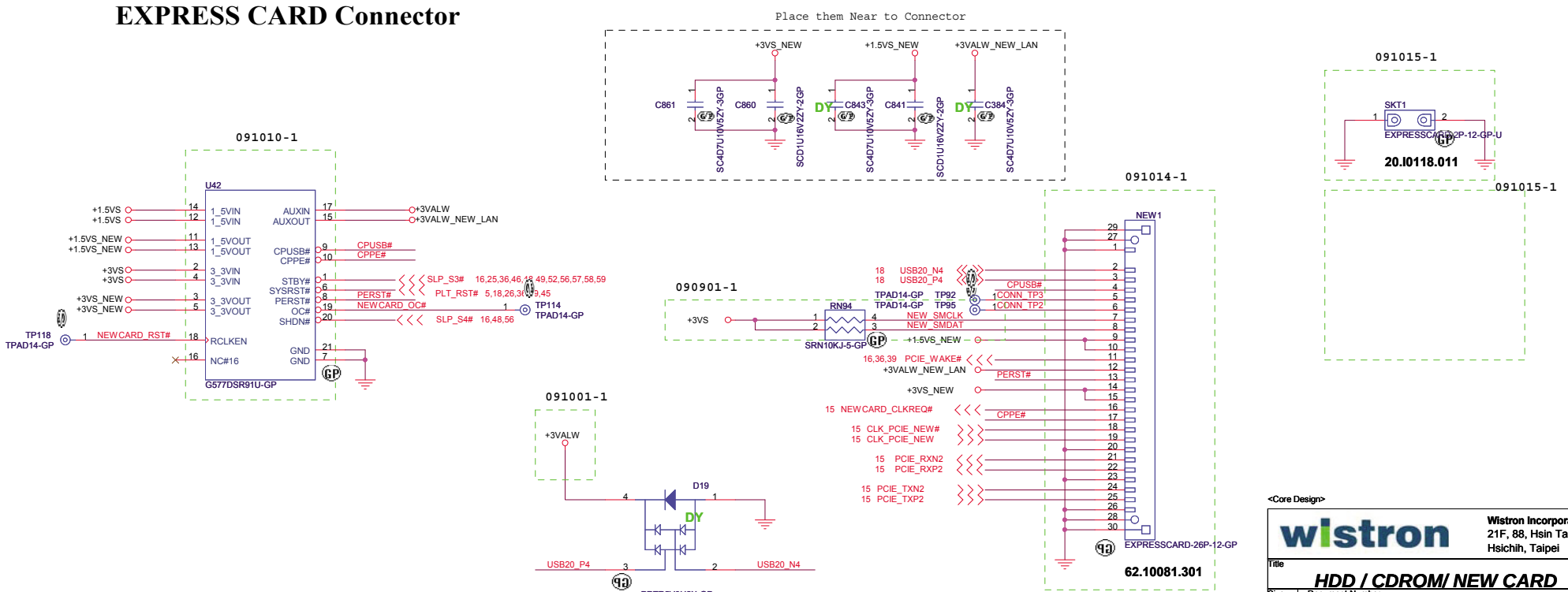


ODD Connector



35

EXPRESS CARD Connector



<Core Design>

wistron

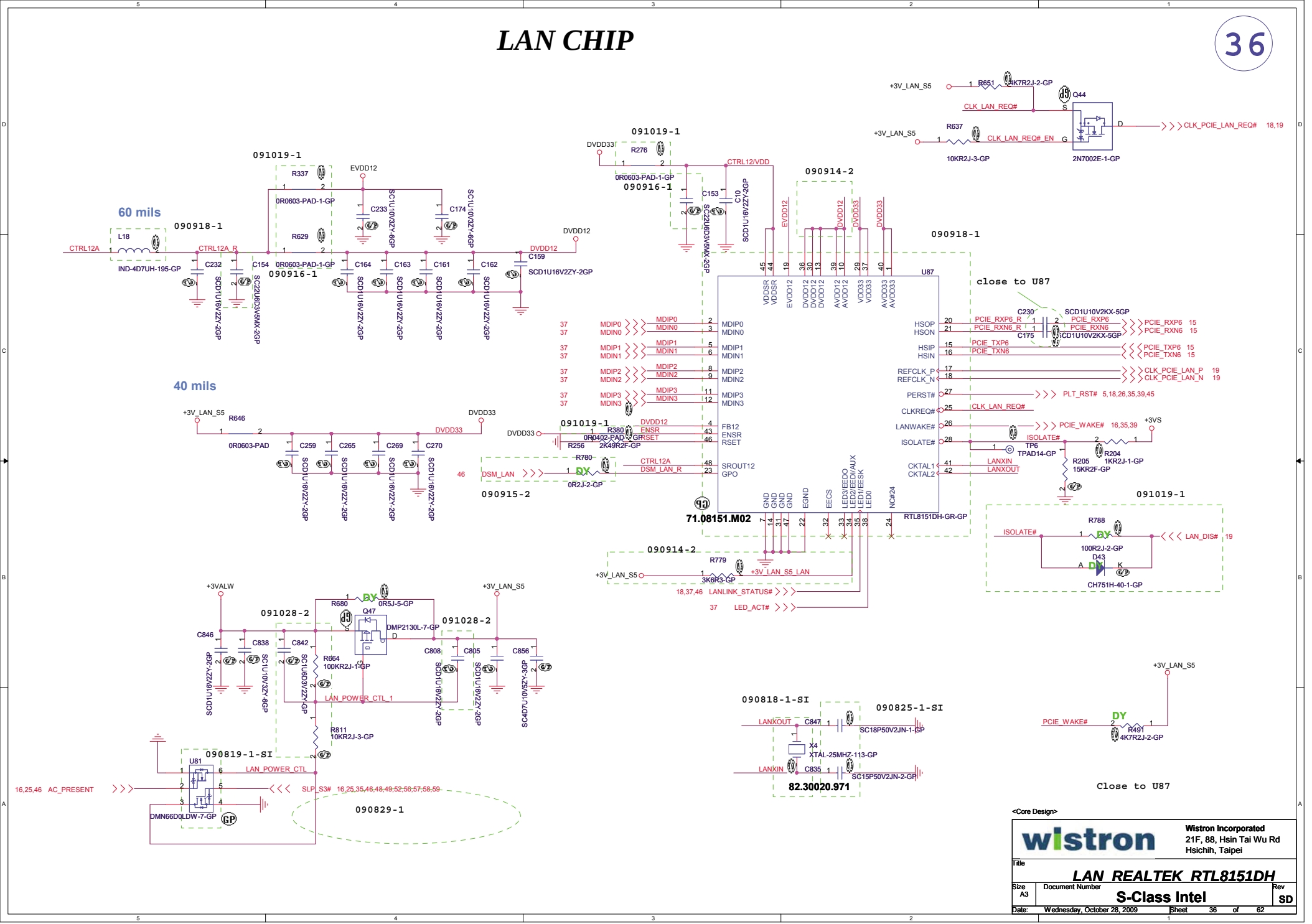
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: HDD / CDROM/ NEW CARD

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 35 of 62

LAN CHIP



<core_design>

wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title	LAN_REALTEK_RTL8151DH	
Size A3	Document Number S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 36 of 62	
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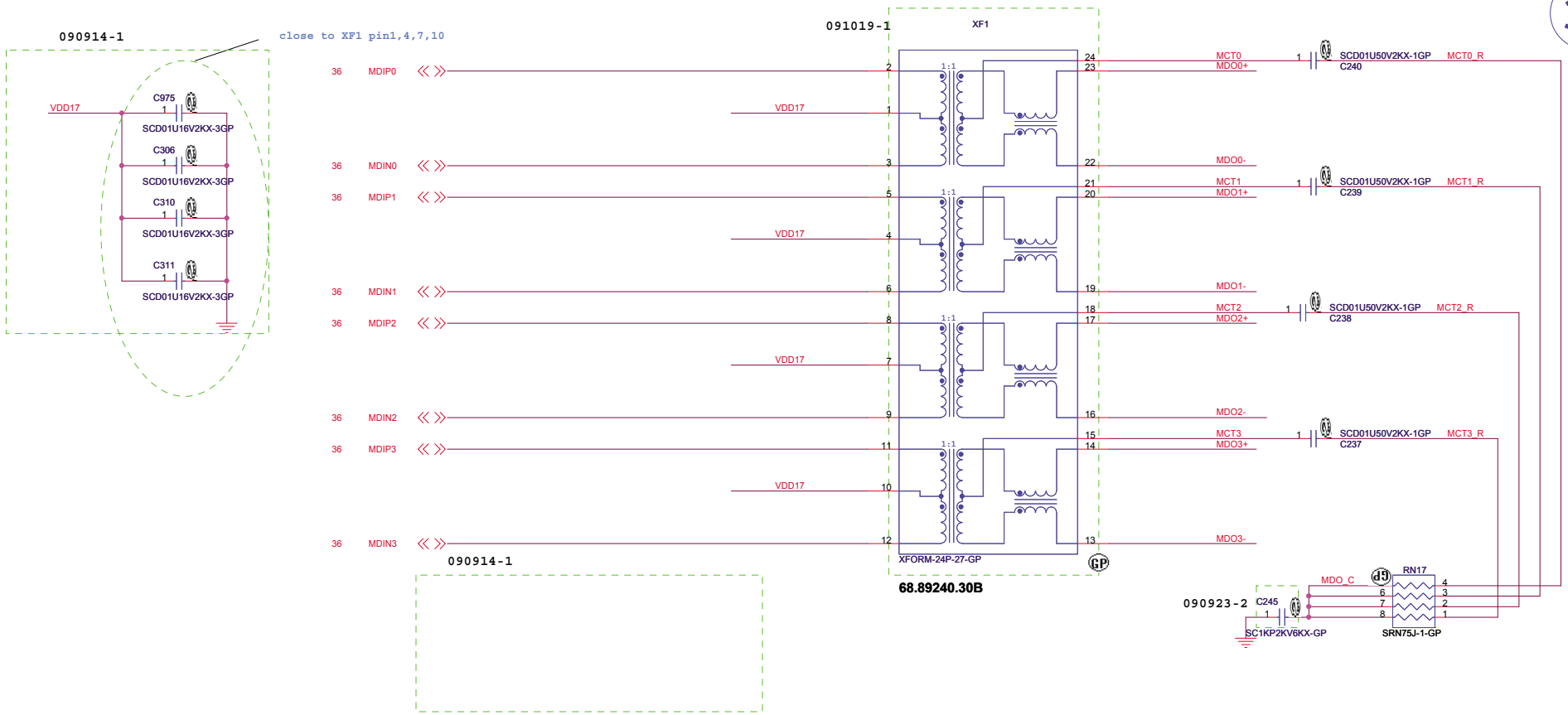
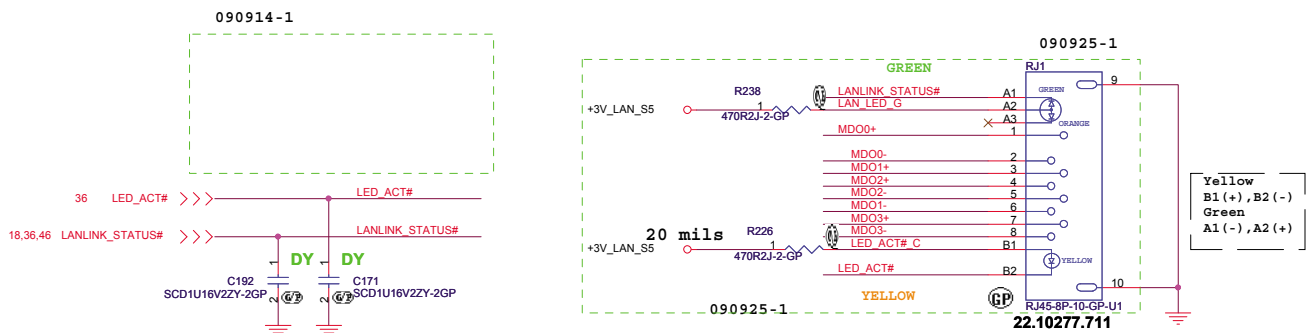




IF NOT OVER CLOCKING, LED_ACT# WILL ACT HIGH

Check LAN chip for LED_ACT# function on RJ45 connector pin define.

<Core Design>

wistron

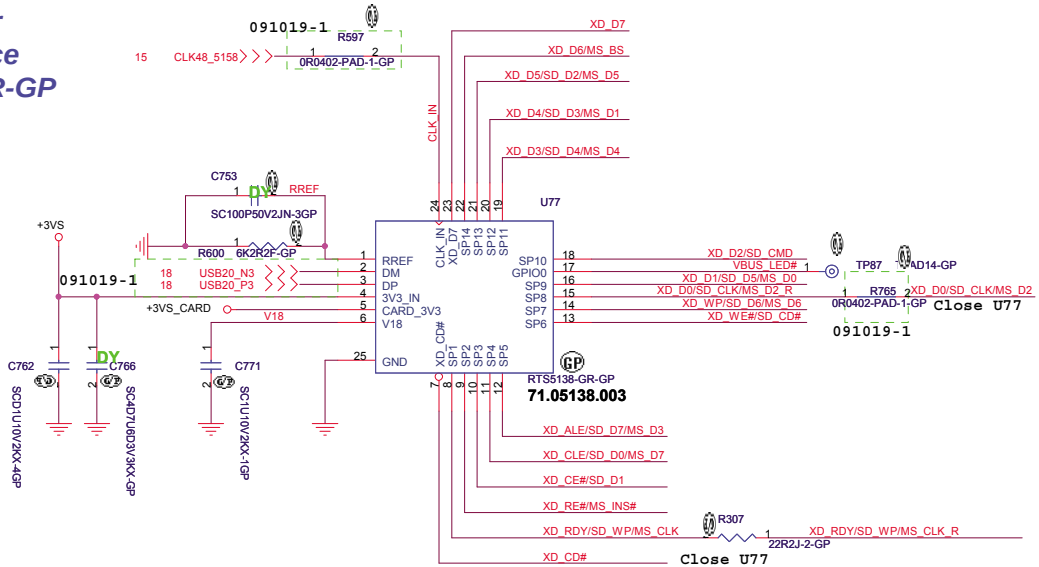
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Magnetic & RJ45

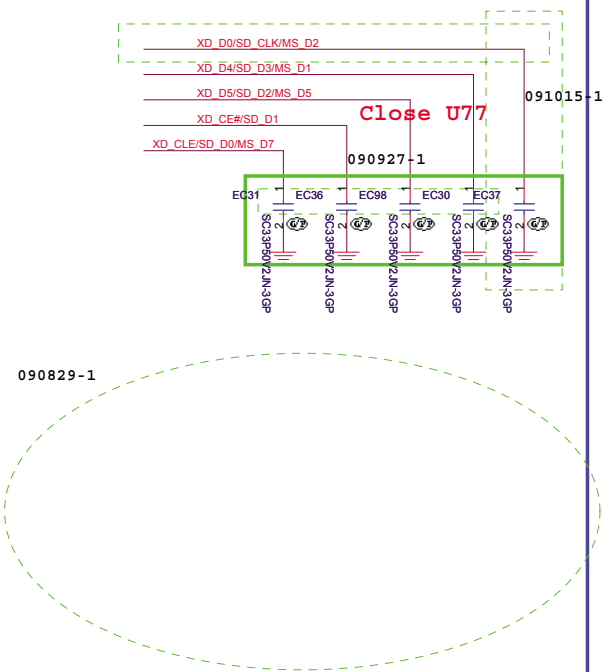
Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 37 of 62

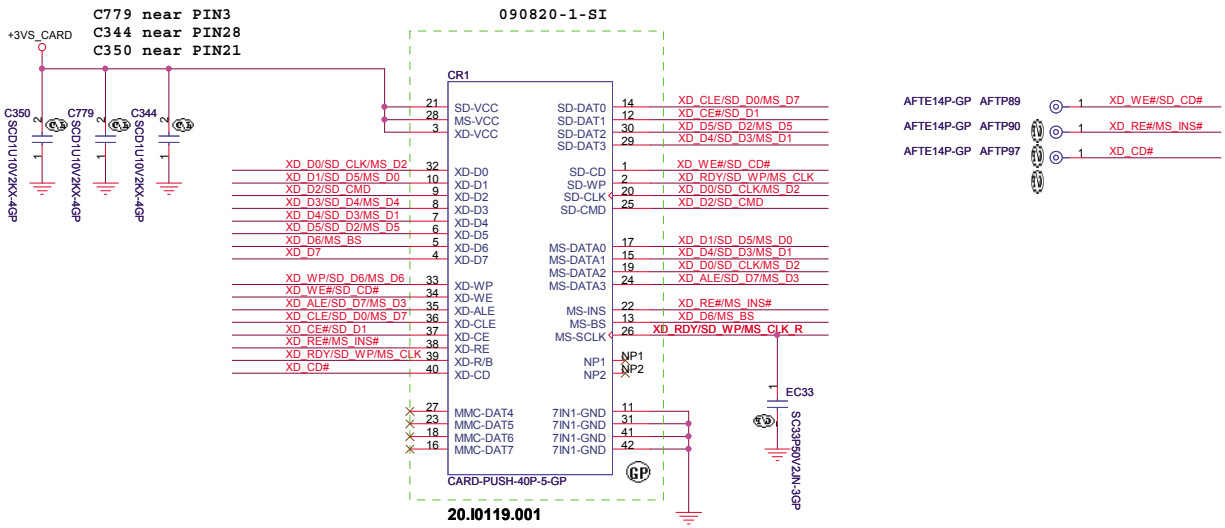
Card Reader
USB Interface
RTS5138-GR-GP



EMI Reserve Cap



4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



<Core Design>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CardReader RTS5138

Size	Document Number	Rev
A3	S-Class Intel	SD

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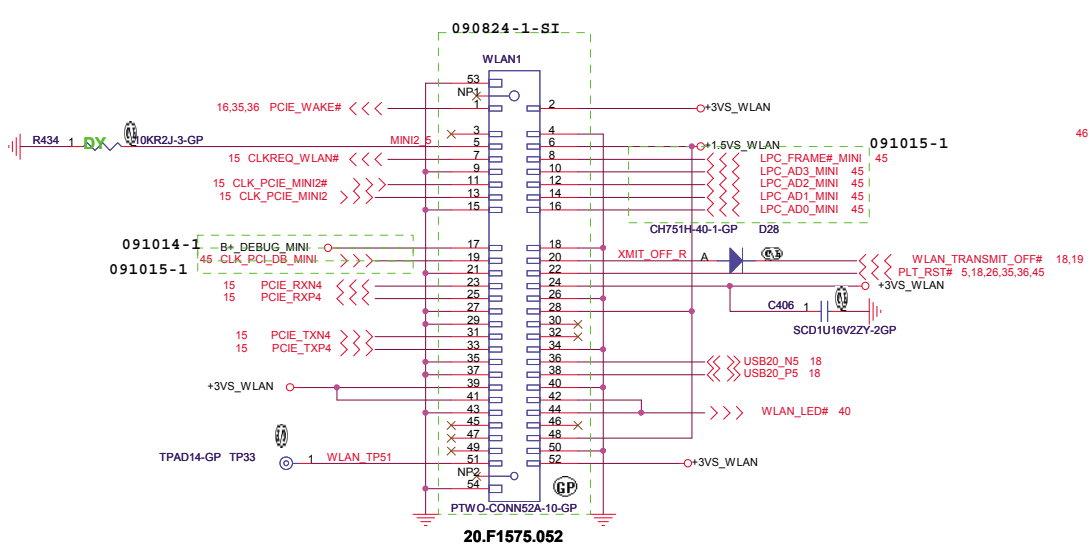
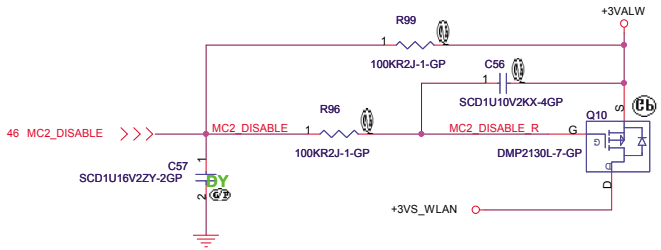
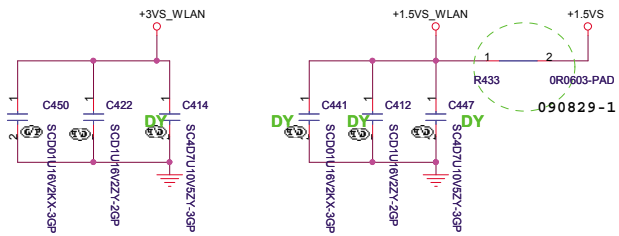
Mini-Card--WLAN

Half minicard

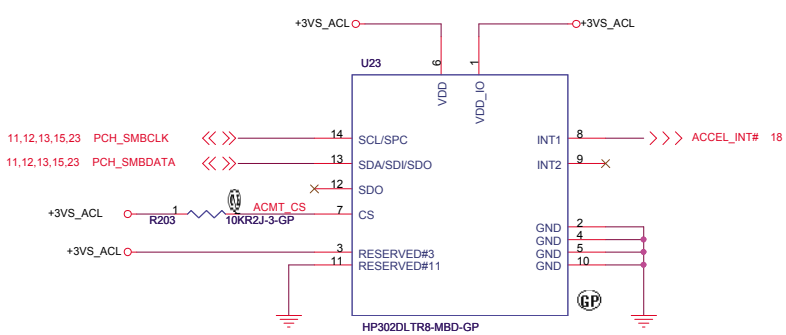


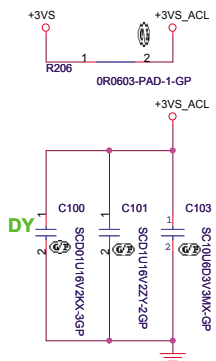
20.F1575.052





ACCELEROMETER





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Title: *Mini-Card/Accelerometer*

Size: A3 | Document Number: S-Class Intel | Rev: SD

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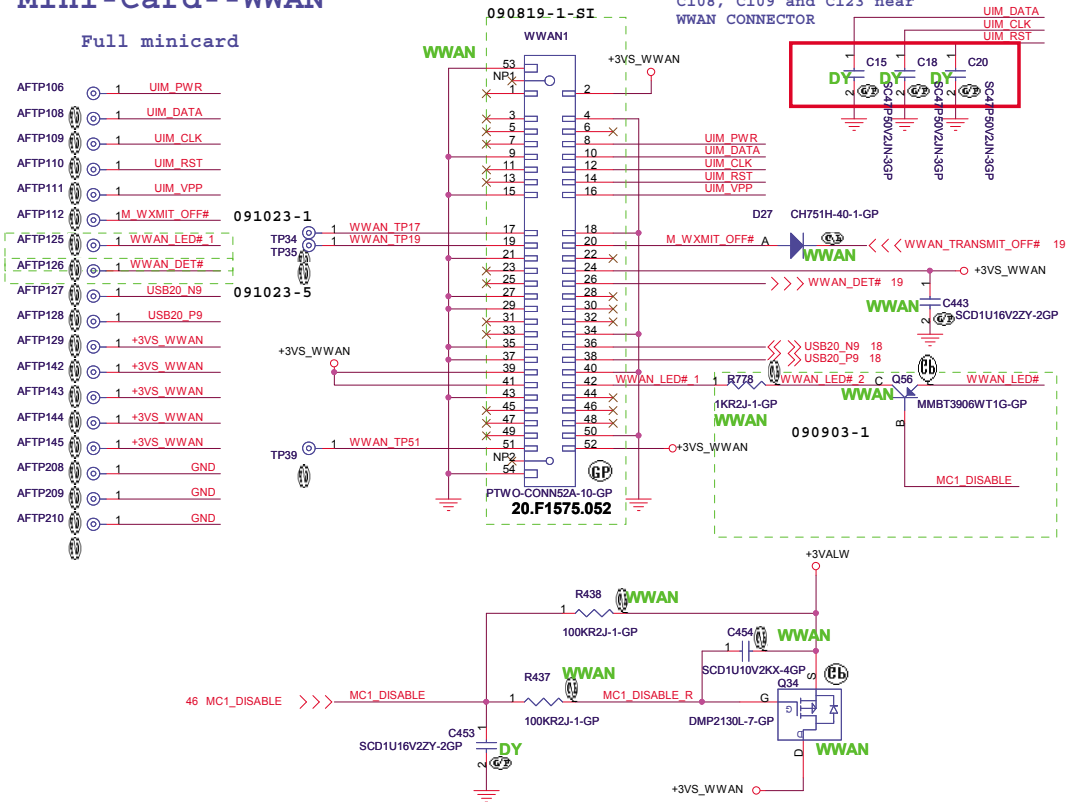
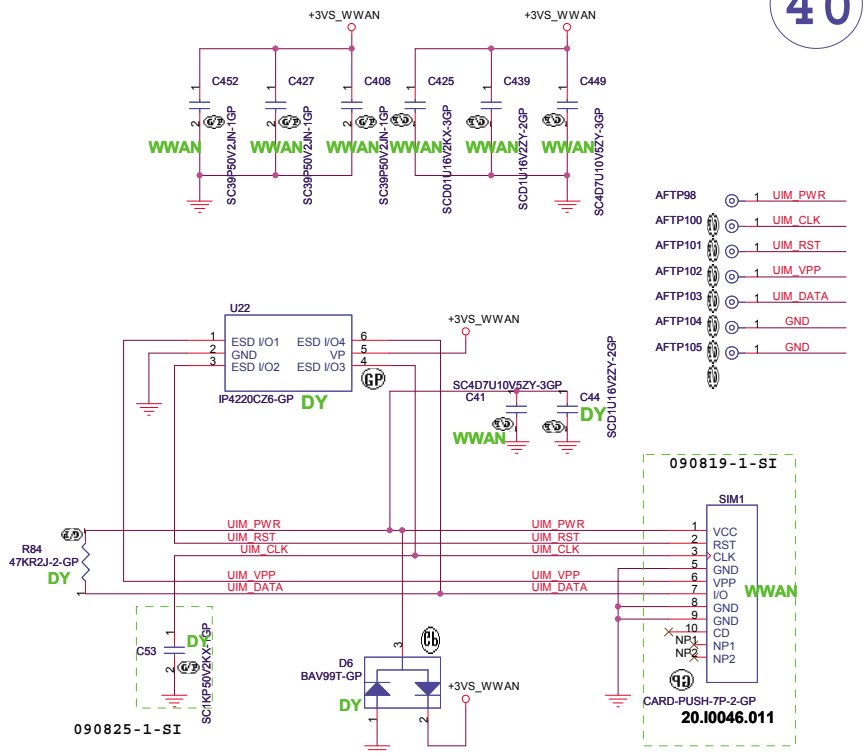
Mini-Card--WWAN

Full minicard

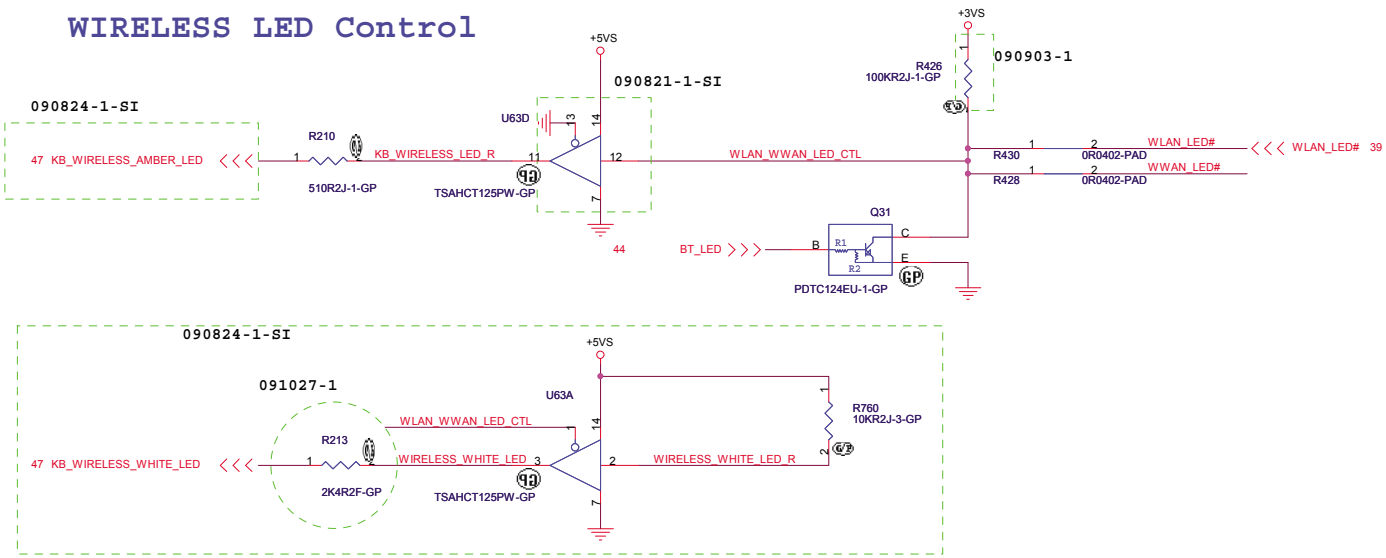


SIM Card Slot

40



WIRELESS LED Control



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AUDIO CODEC(92HD80)

090821-1-SI

Port Arrangement

Port A---> Ext Mic
Port B---> HP
Port C---> Int Mic
Port D---> SPKR
Port E---> FREE
Port F---> FREE

090918-1

U95

092HD80B1X5NLGXYD2-GP

71.92H80.A03

090817-1-SI

090903-1

090829-1

091022-1

091021-1

SENSE Detect

Close to Pin13

Close to Pin14

090829-1

Digital GND & AUD_AGND

Place close to Codec chip

audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP

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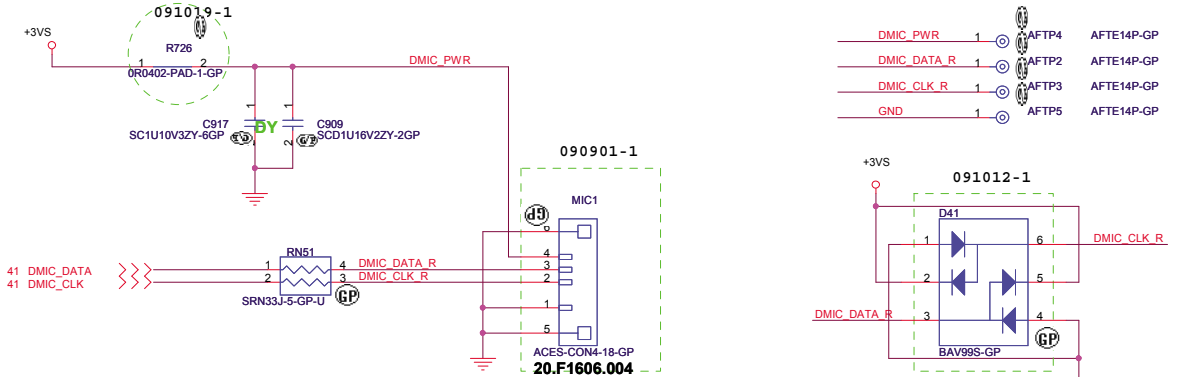
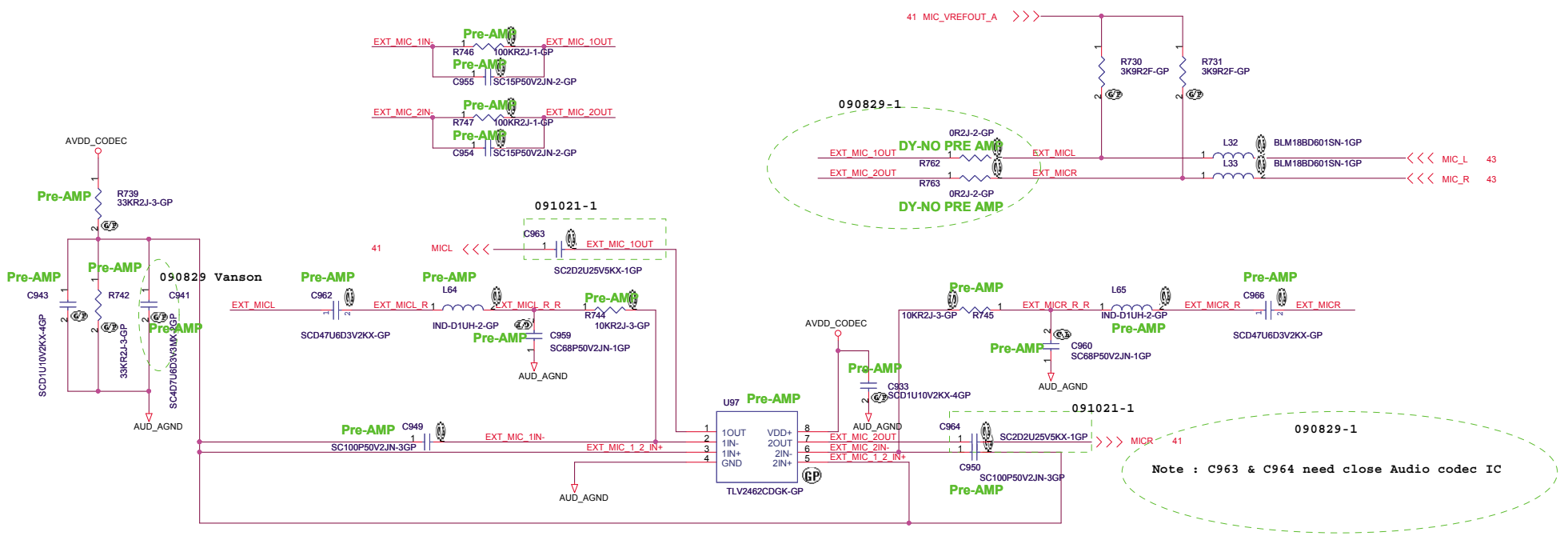
Title: AUDIO_92HD80 / OP AMP		
Size: A3	Document Number: S-Class Intel	Rev: SD
Date: Wednesday, October 28, 2009	Sheet 41 of 62	

Internal Digital MIC



Ppre-AMP. for External MIC



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Title: AUDIO Pre-AMP / CONN

Size: A3 | Document Number: S-Class Intel | Rev: SD

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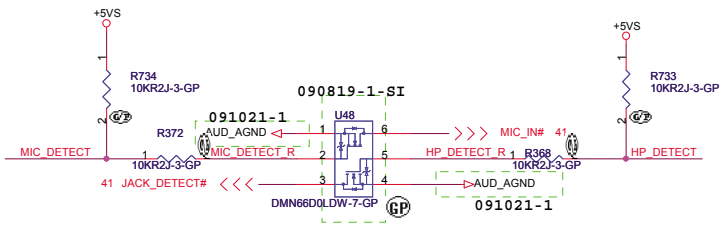
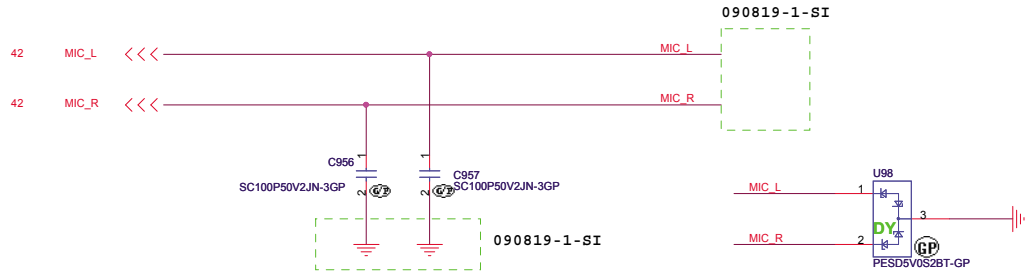
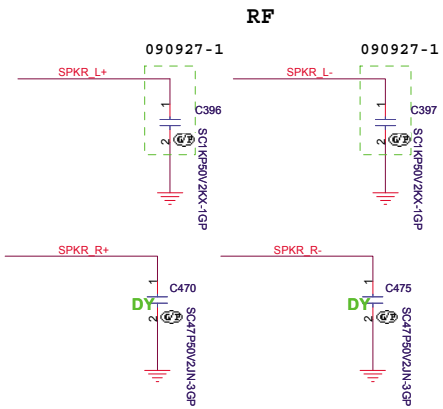
Jack Detect



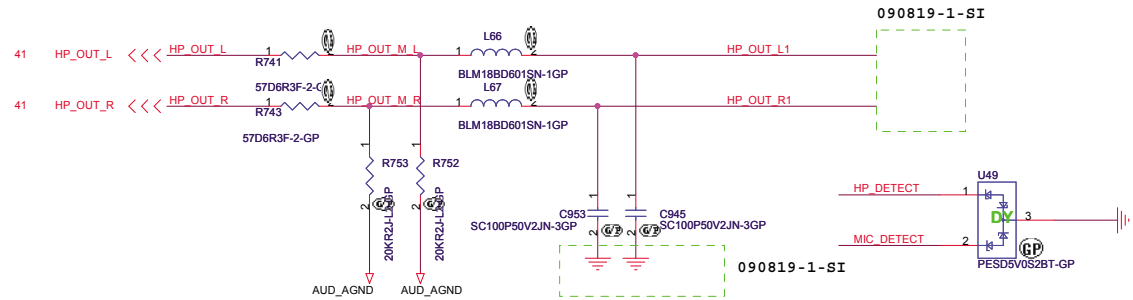
MIC IN



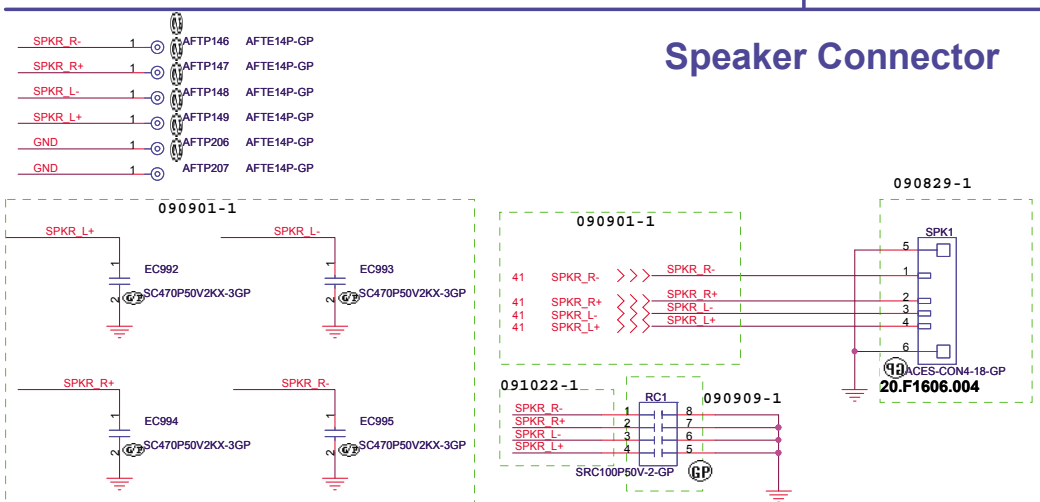
RF Reserver Cap



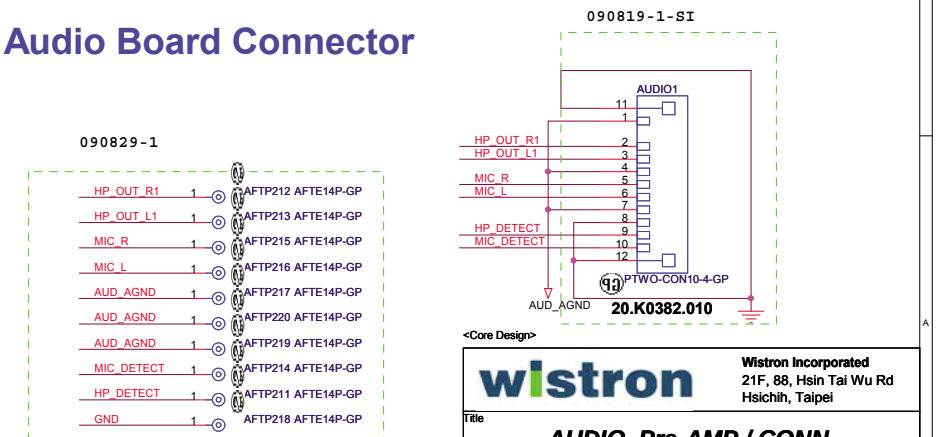
HeadPhone OUT



Speaker Connector



Audio Board Connector



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Title: AUDIO Pre-AMP / CONN

Size: A3 | Document Number: S-Class Intel | Rev: SD

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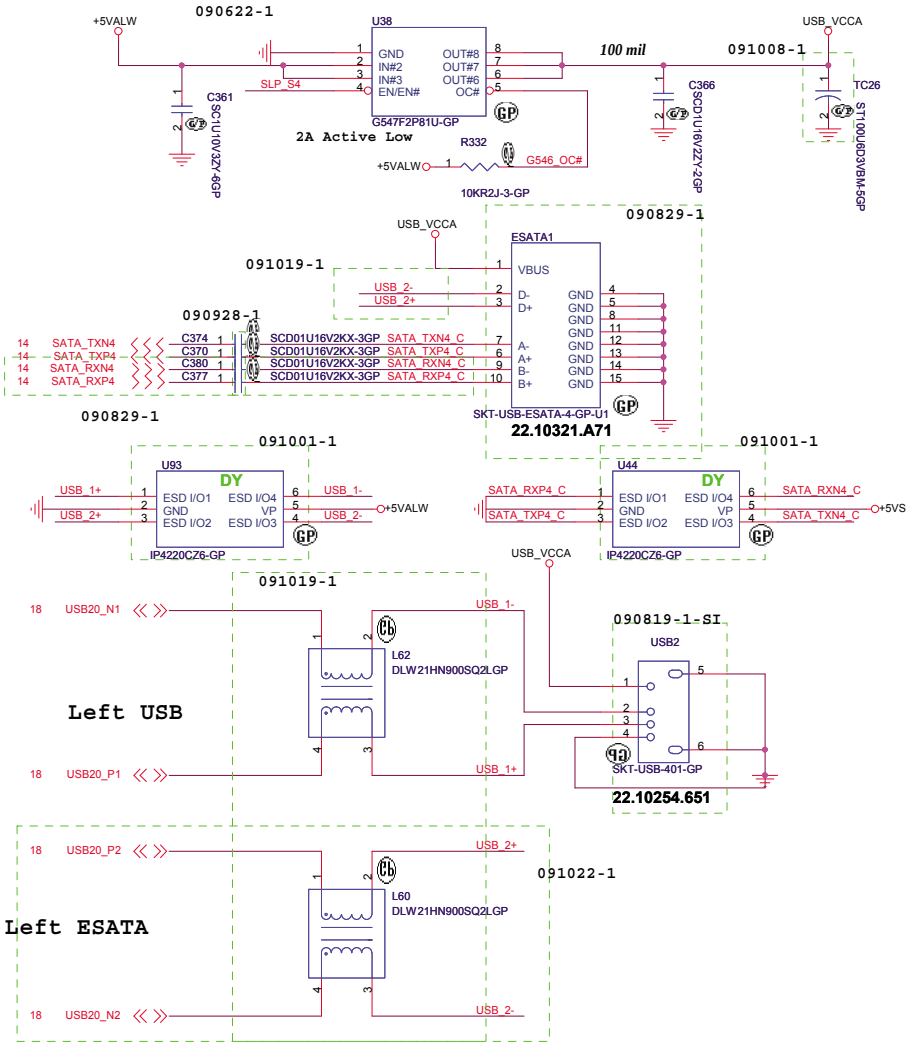
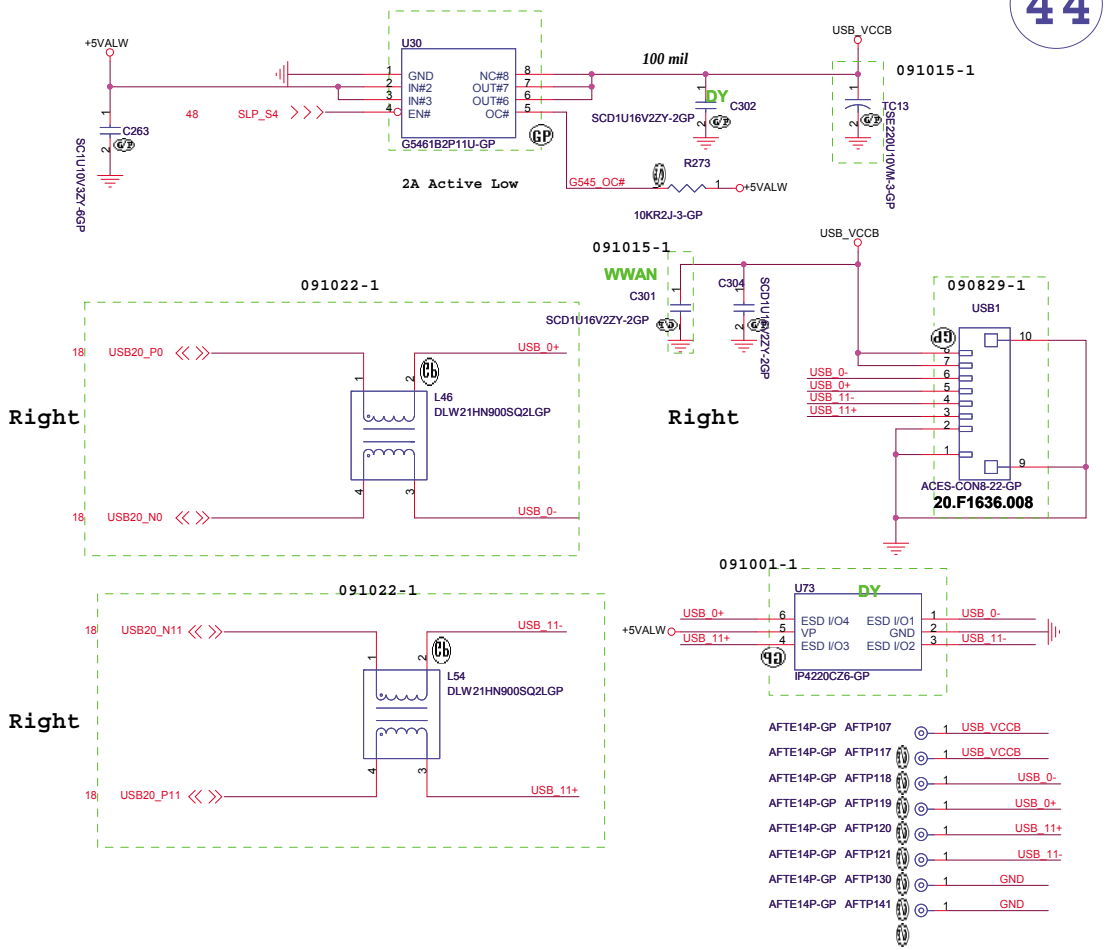
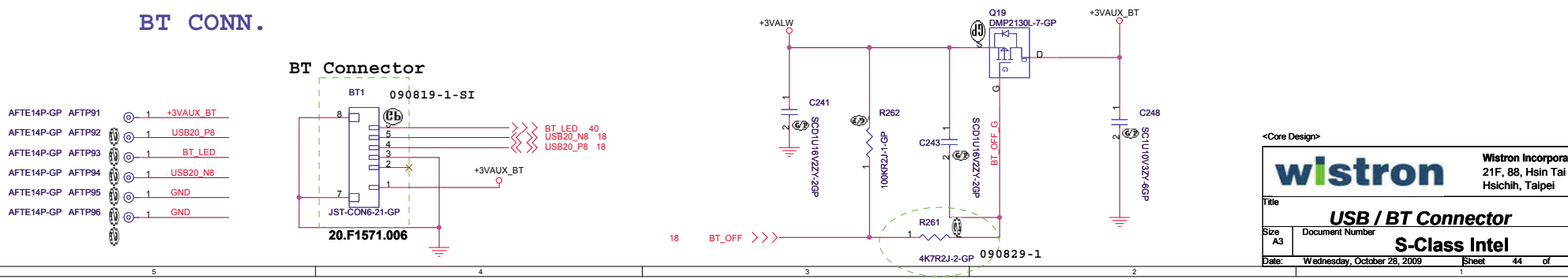
Left Side USB + ESATA Port



Right Side USB x 2



BT CONN.



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Title: USB / BT Connector

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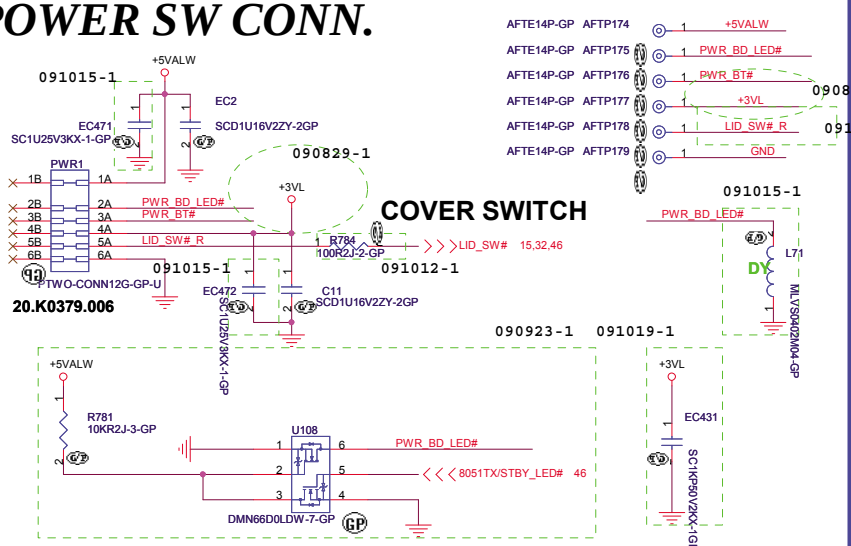
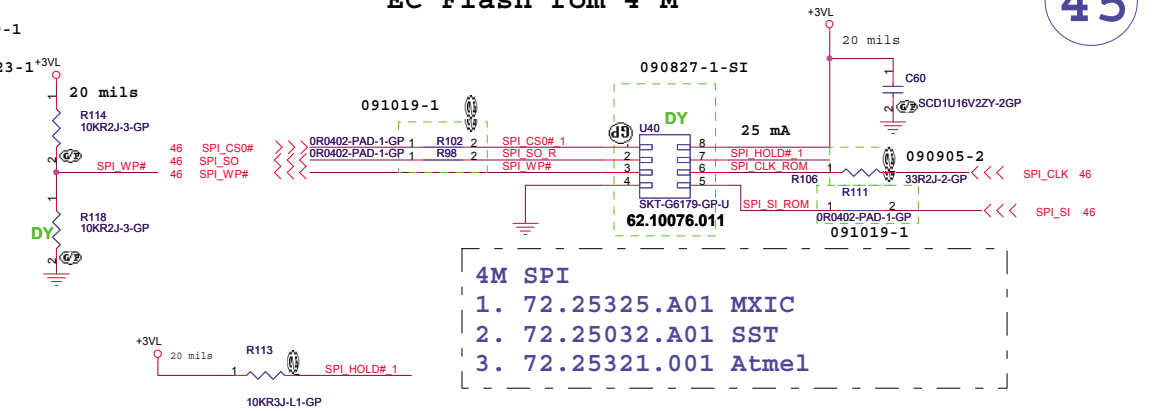
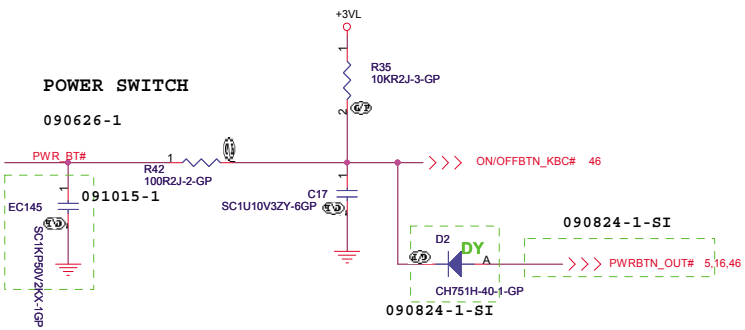
POWER SW CONN.

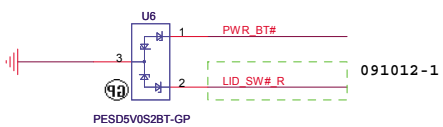


EC Flash rom 4 M

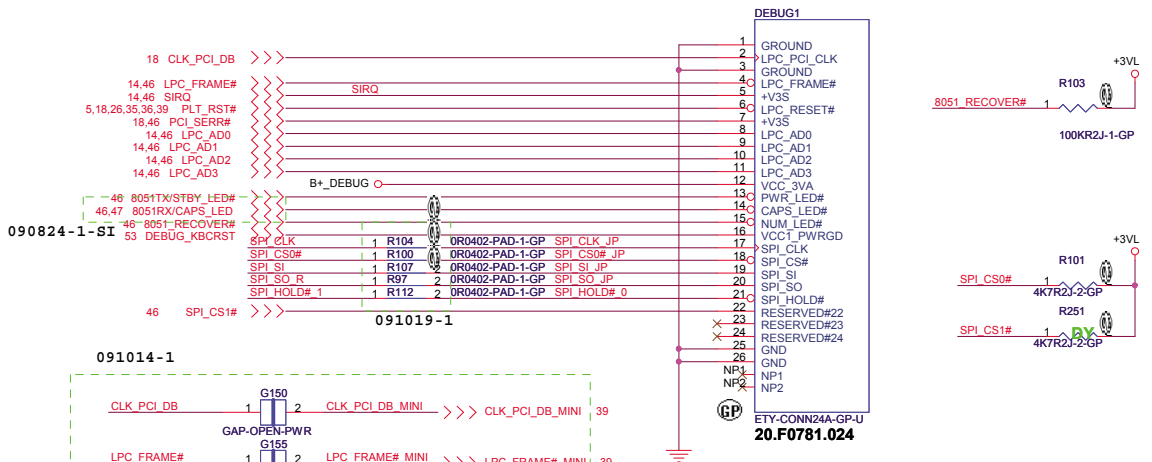


Power SW Circuit





24 PIN LPC DEBUG CONN.



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Title: FWH / BTN / DEBUG CONN.

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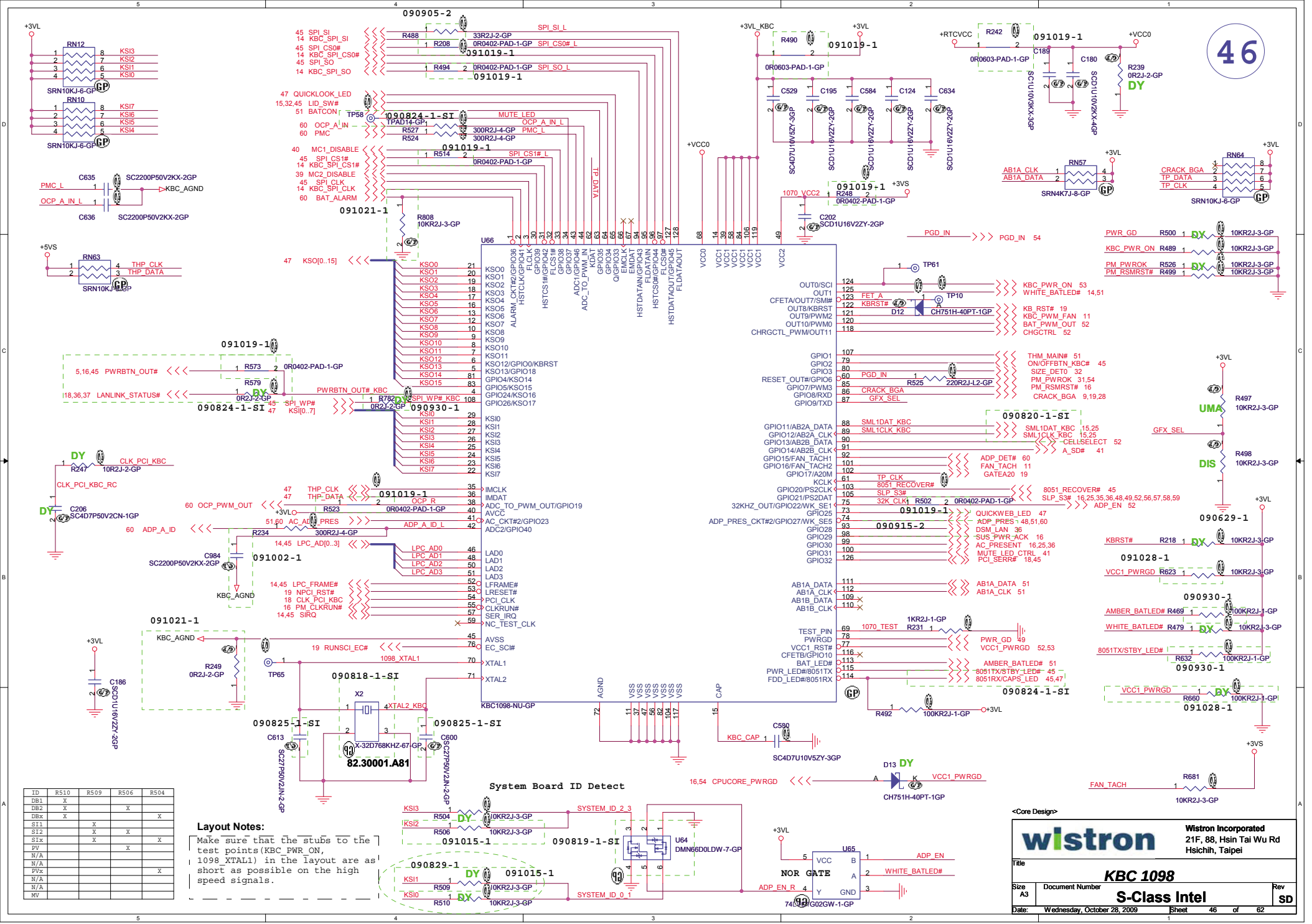
46
U66
KBC1098-NU-GP
090905-2
090824-1-SI
091019-1
091021-1
090930-1
090820-1-SI
090915-2
090824-1-SI
090629-1
091028-1
090818-1-SI
090825-1-SI
090829-1
091015-1
090819-1-SI
091002-1
System Board ID Detect
Layout Notes:
Make sure that the stubs to the test points(KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.
82.30001.A81
NOR GATE
<Core Design>
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Hsichih, Taipei
KBC 1098
S-Class Intel
Size A3
Document Number
Rev SD
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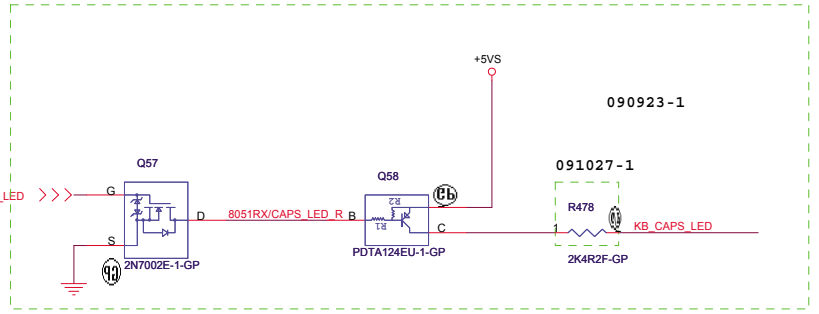
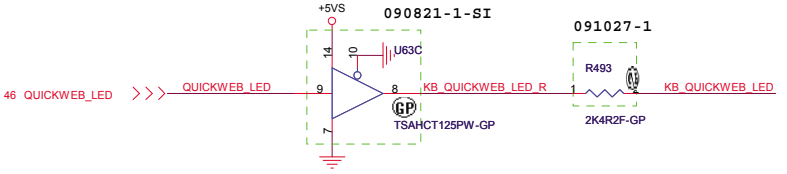
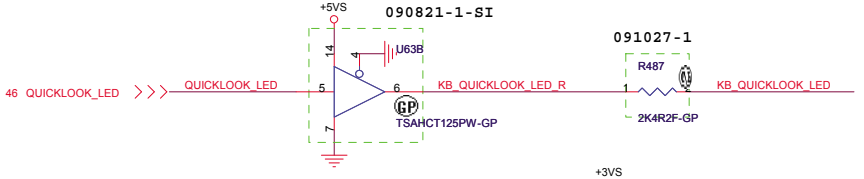
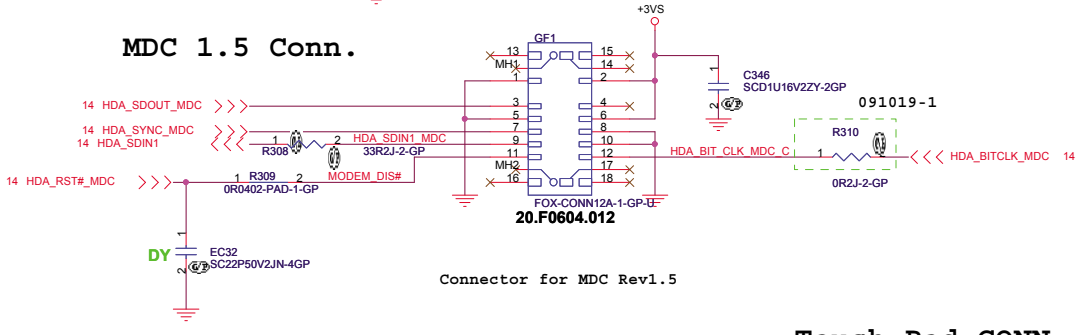




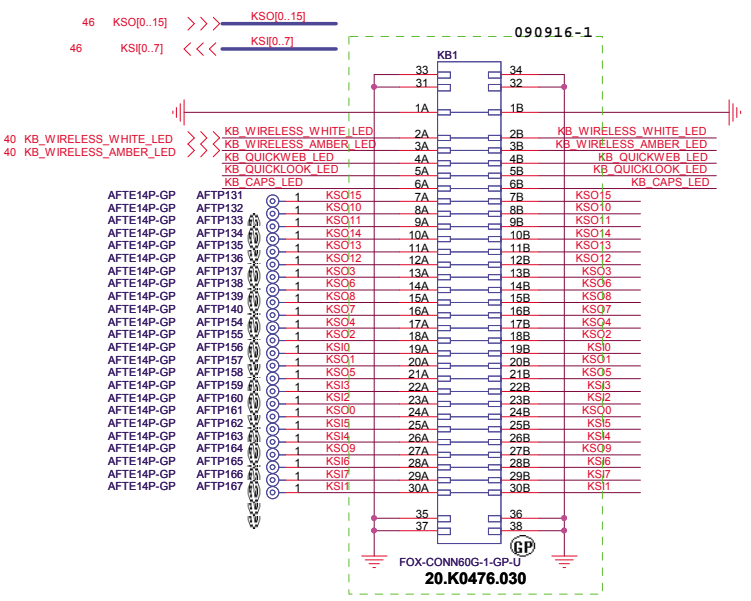


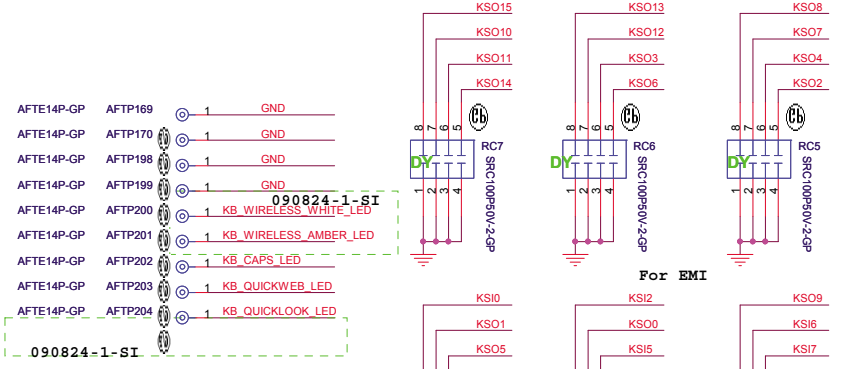
MDC 1.5 Conn.



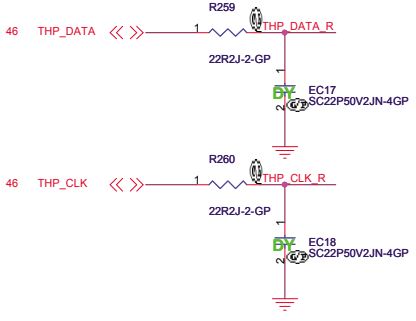
Connector for MDC Rev1.5

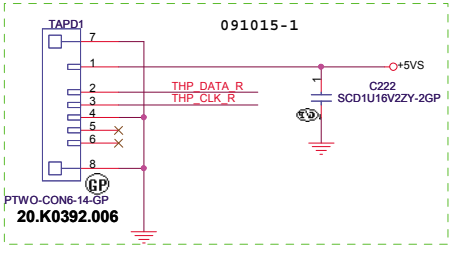
INT_KBD CONN.

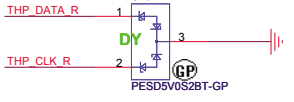


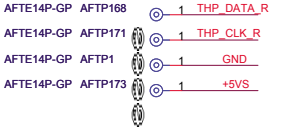


Touch_Pad CONN.









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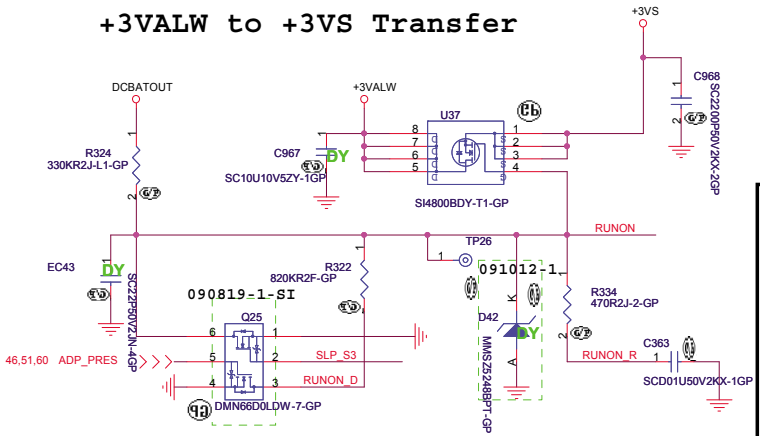
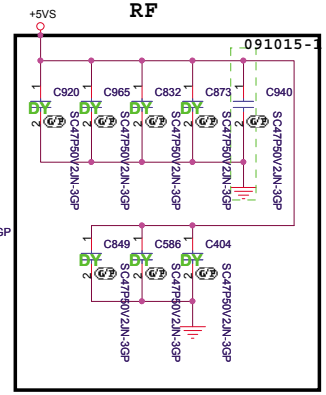
+1.5VU to +1.5VS Transfer

48

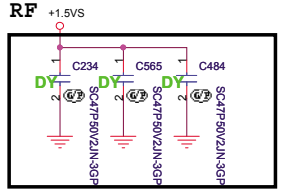
+3VALW to +3VS Transfer

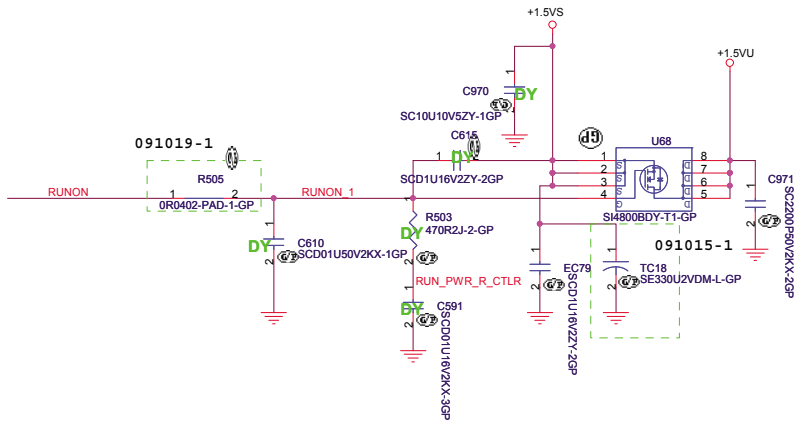


RF

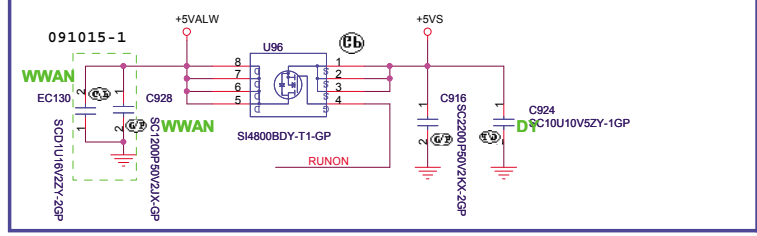


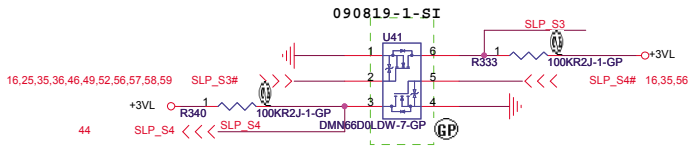
RF



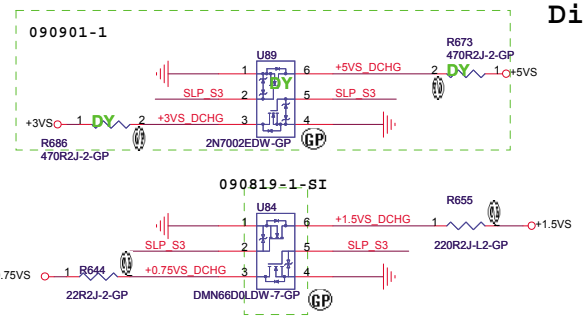


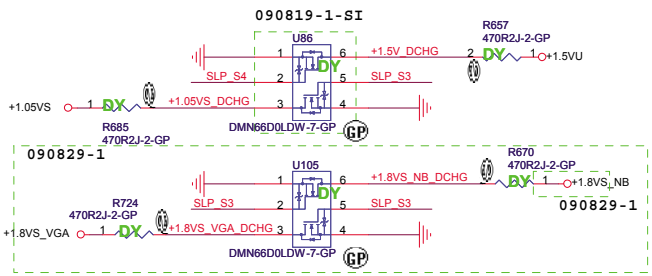
+5VALW to +5VS Transfer





Discharge circuit-1





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Title: DC/DC Circuit

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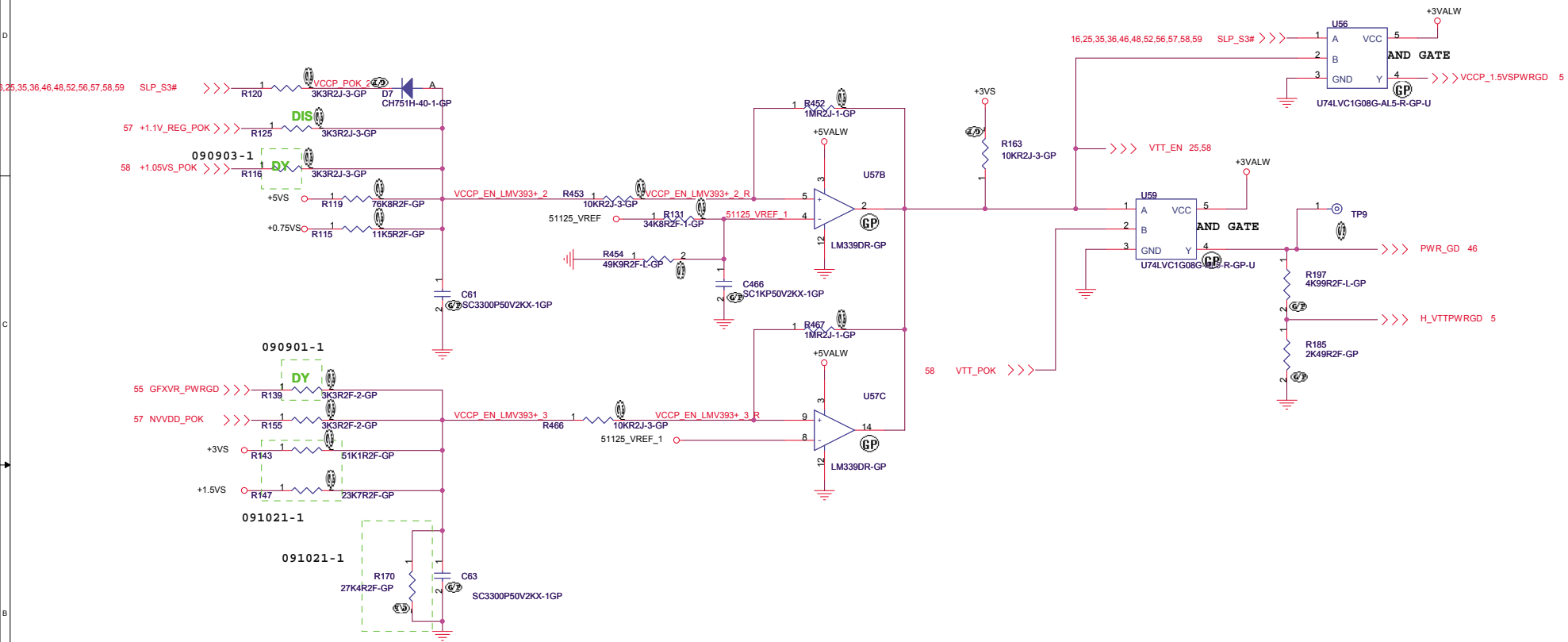

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Hsichih, Taipei

Title: POK CKT

Size: A3 | Document Number: S-Class Intel | Rev: SD

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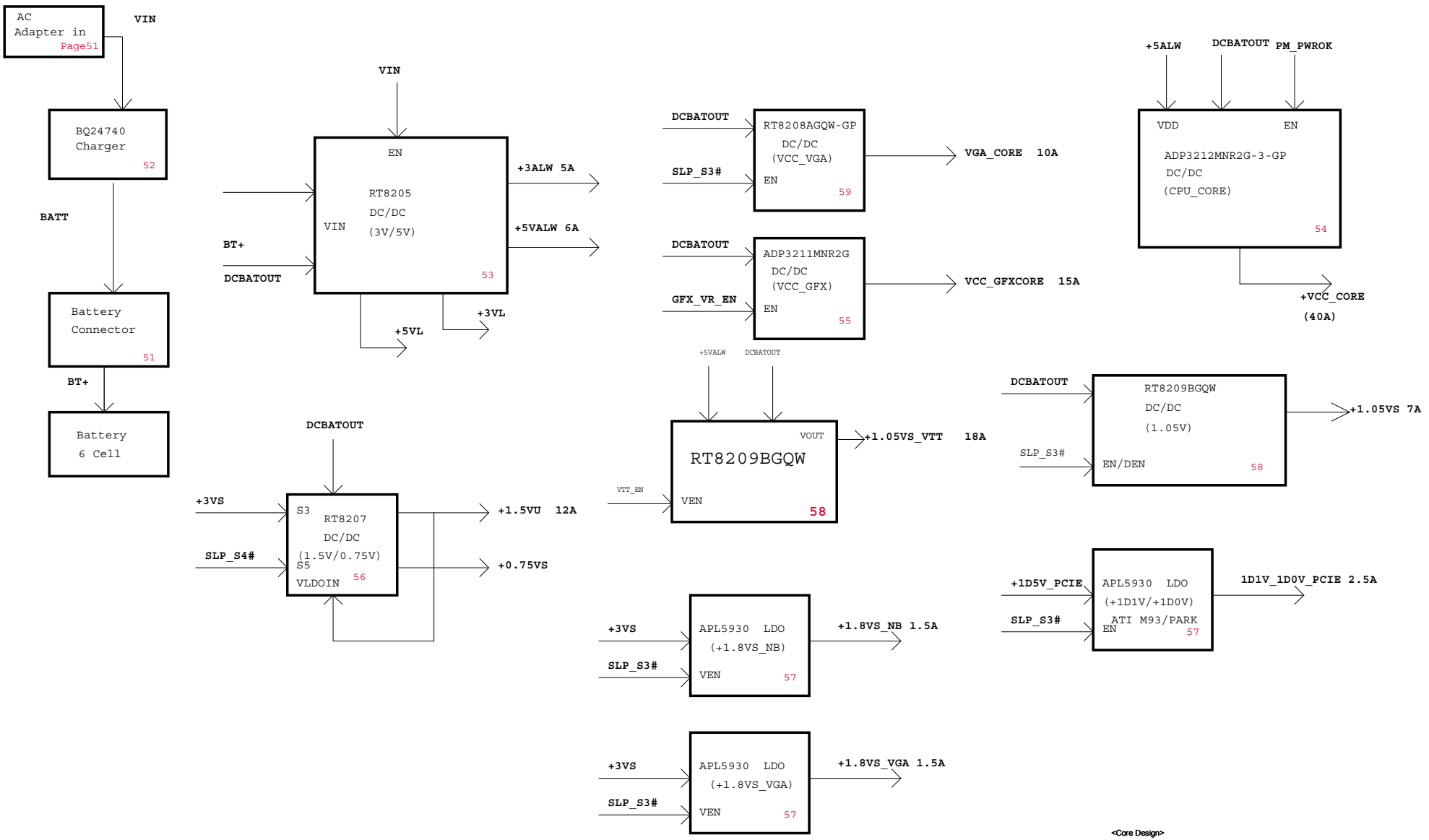
Power Block Diagram



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Title: Power Block Diagram

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A3	S-Class Intel	SD

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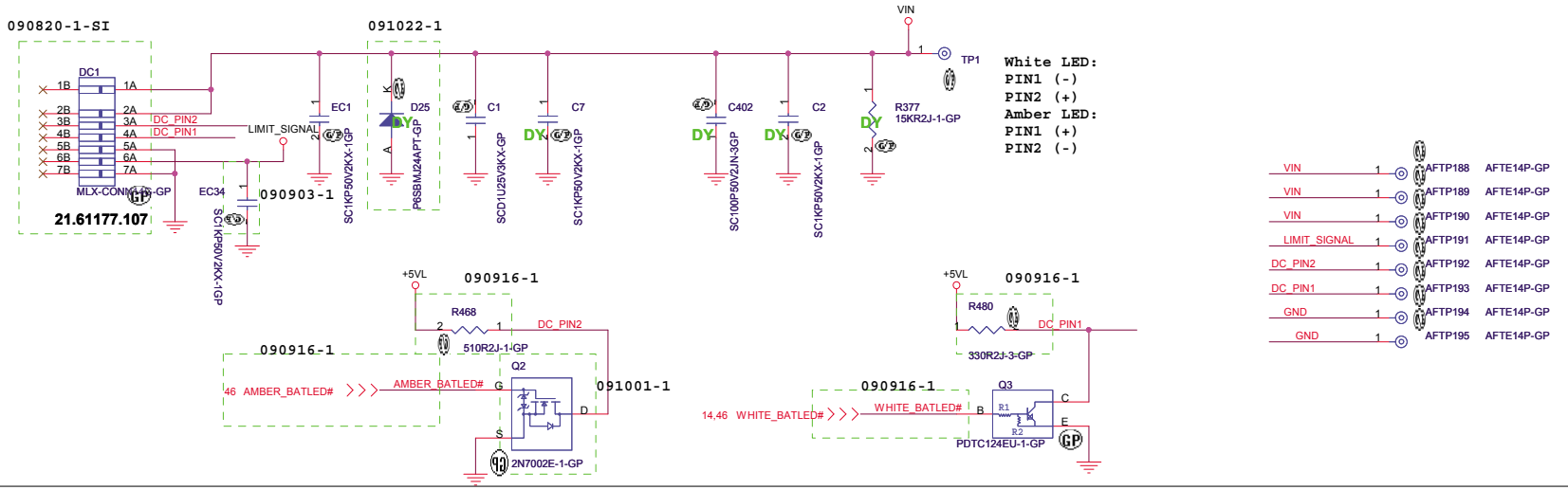
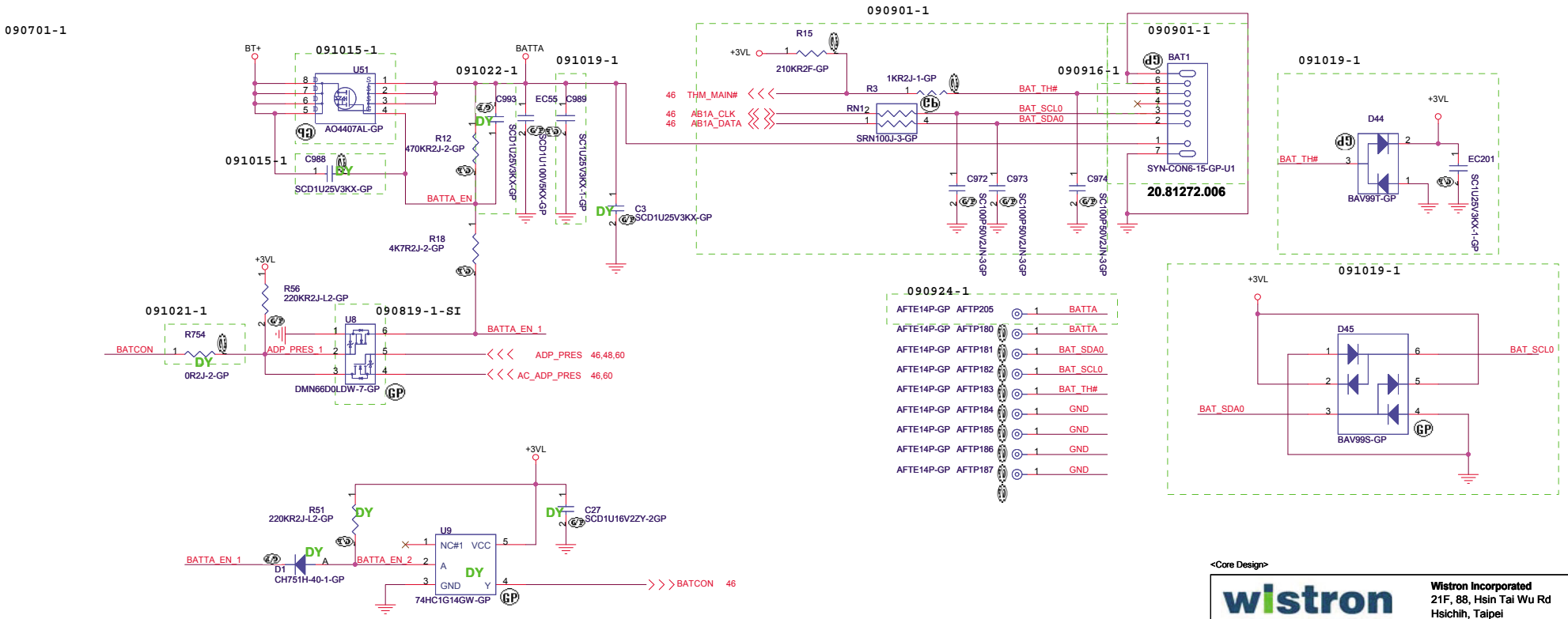
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Hsichih, Taipei

Title: DC & BATTERT CONN.

Size: Custom | Document Number: S-Class Intel | Rev: SD

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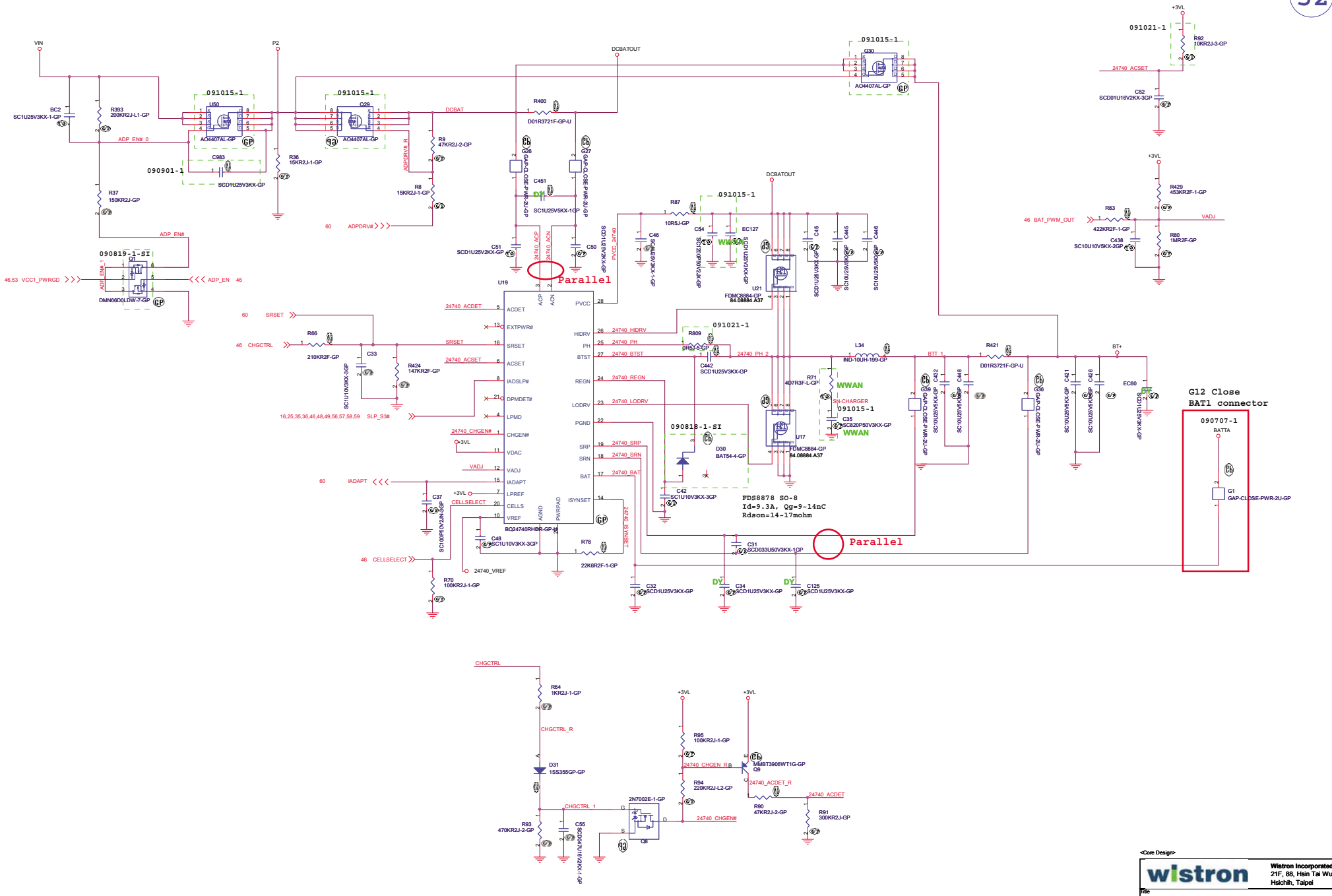

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Title: CHARGER BQ24740

Size: A2 | Document Number: S-Class Intel | Rev: SD

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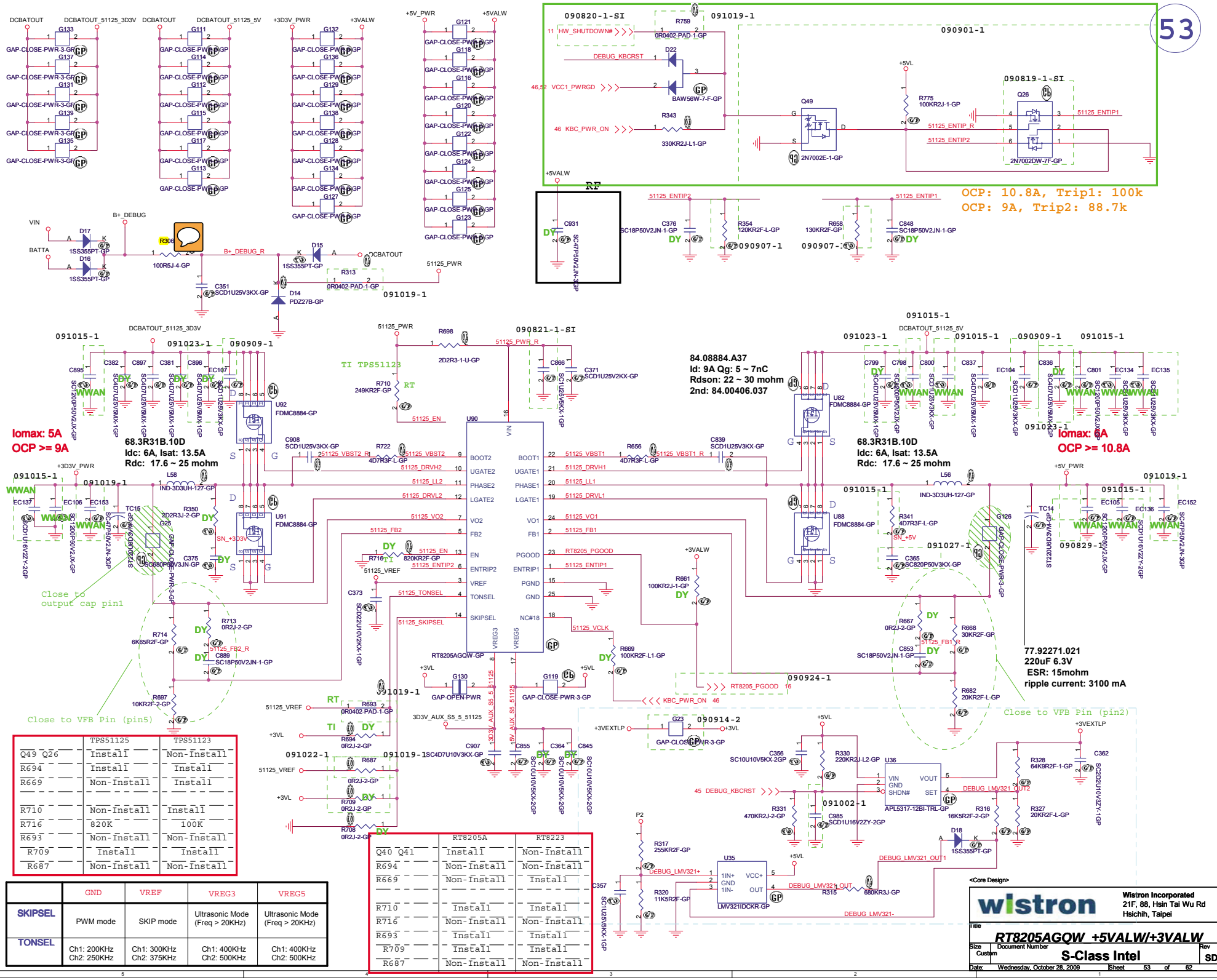
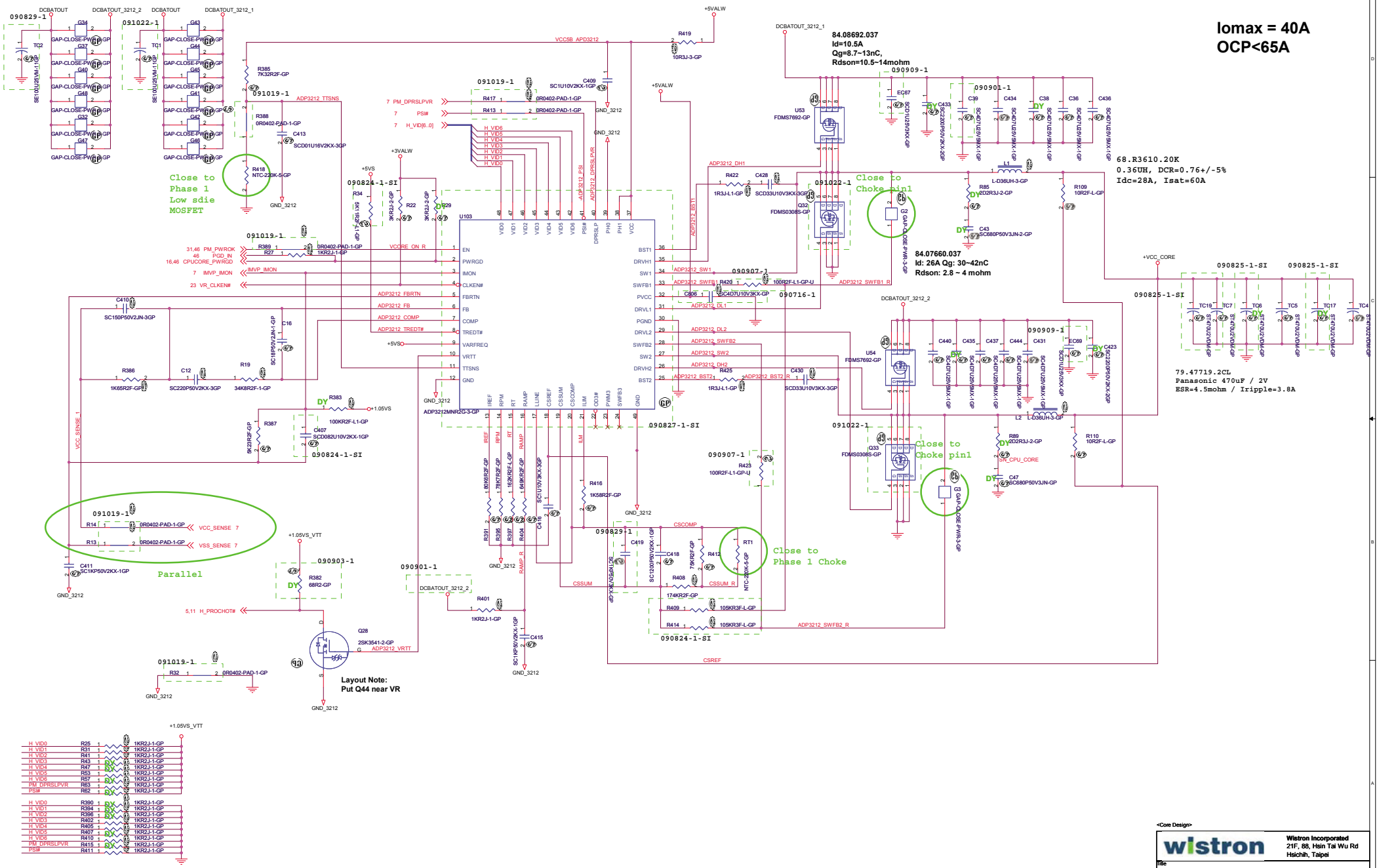


	TPS51125	TPS51123
Q49 Q26	Install	Non-Install
R694	Install	Install
R669	Non-Install	Install
R710	Non-Install	Install
R716	820K	100K
R693	Non-Install	Non-Install
R709	Install	Install
R687	Non-Install	Non-Install

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R694	Non-Install	Non-Install
R669	Non-Install	Install
R710	Install	Install
R716	Non-Install	Non-Install
R693	Install	Install
R709	Install	Install
R687	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz



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Title: ADP3212MNR2G_CPU CORE

Size	Document Number	Rev
A2	S-Class Intel	SD

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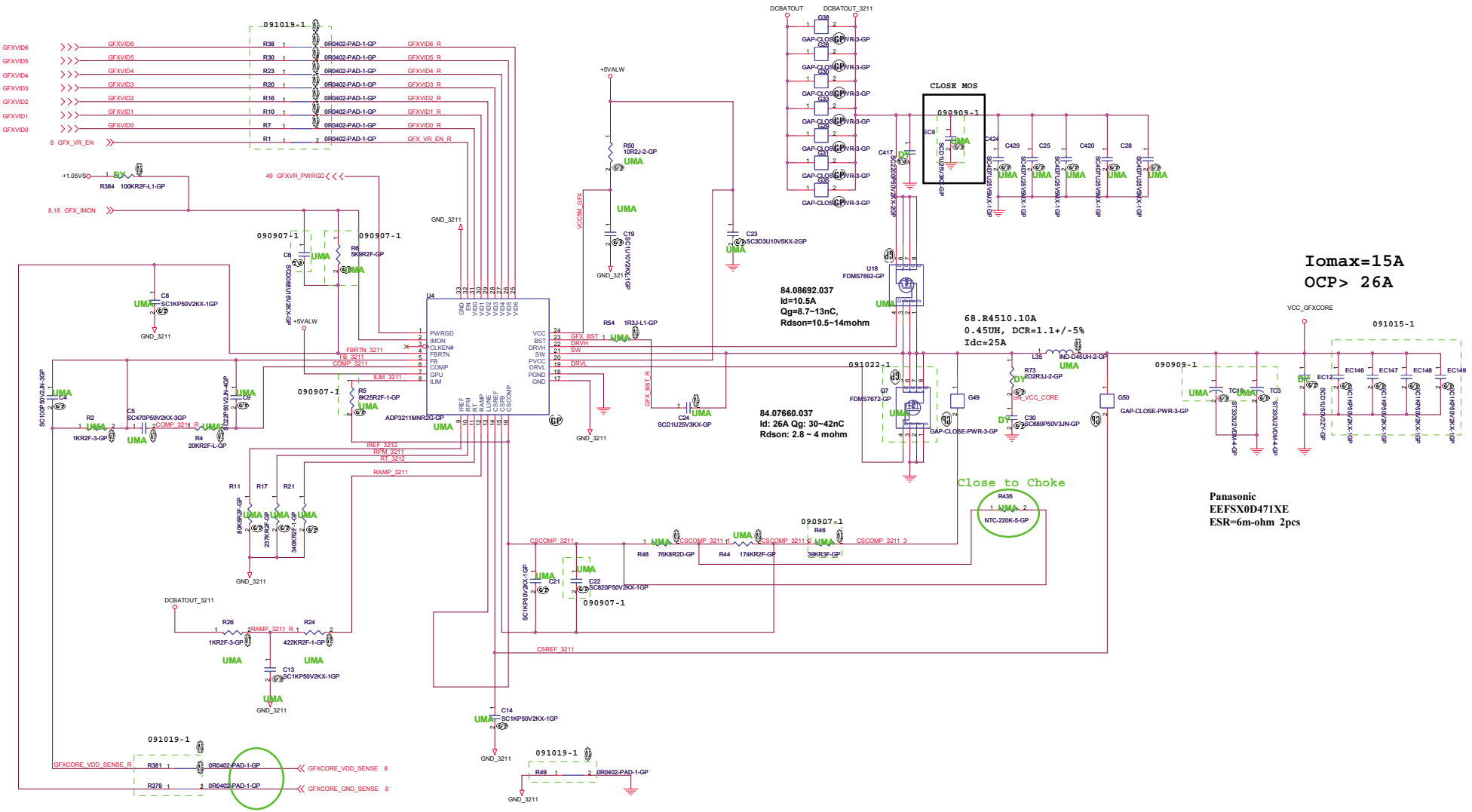

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Title: ADP3211MNR2G_+VCC_GFX_CORE

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A2	S-Class Intel	SD

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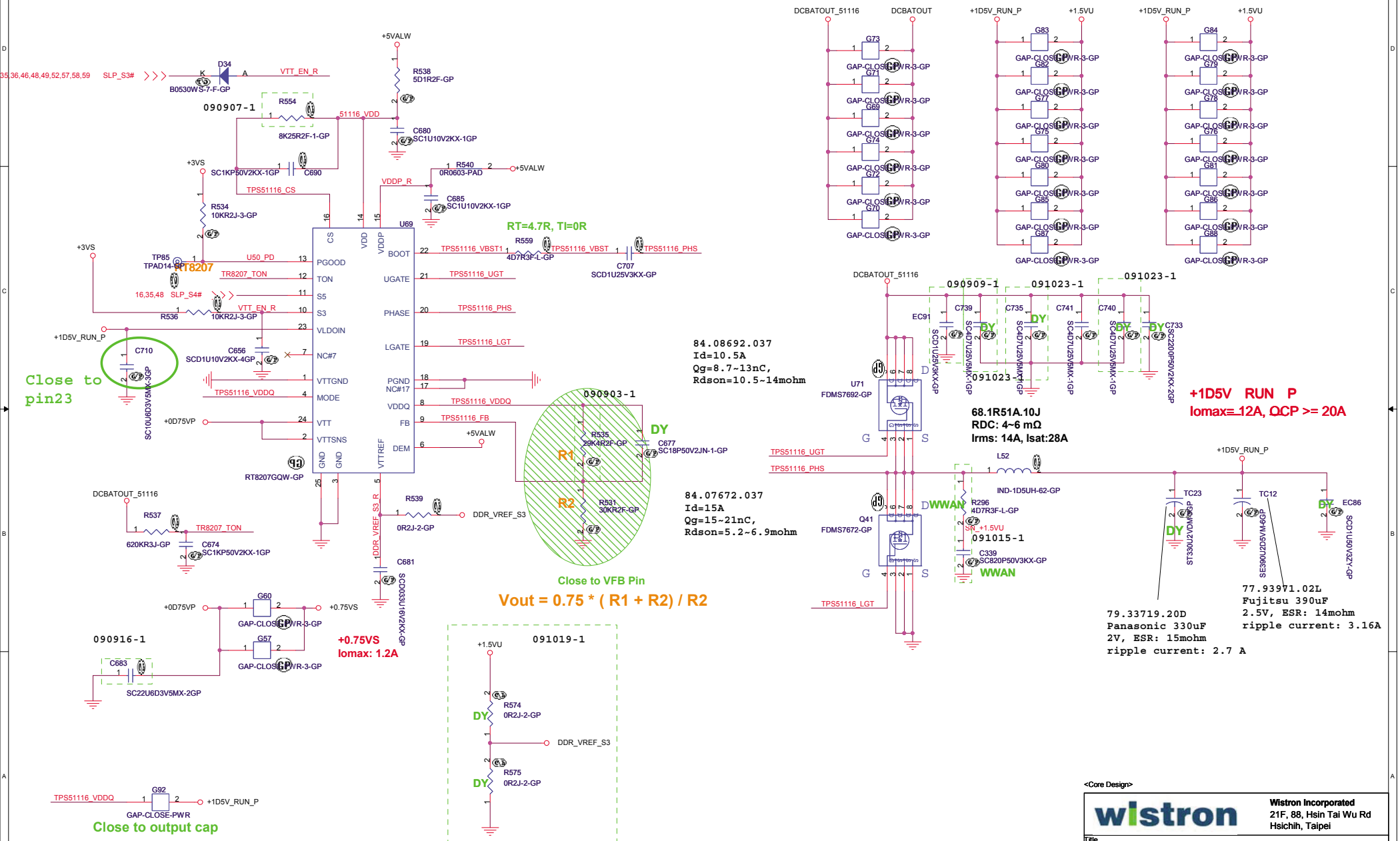
RT8207 for 1D5V and 0D75V



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Title: RT8207GQW +1.5VU / +0.75VS

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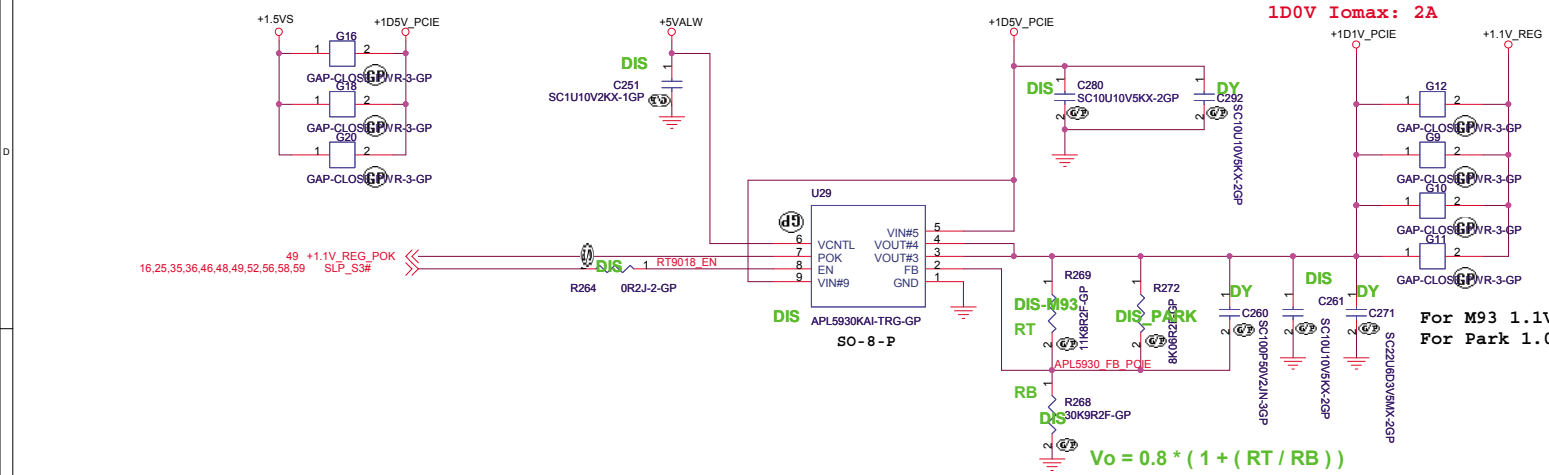
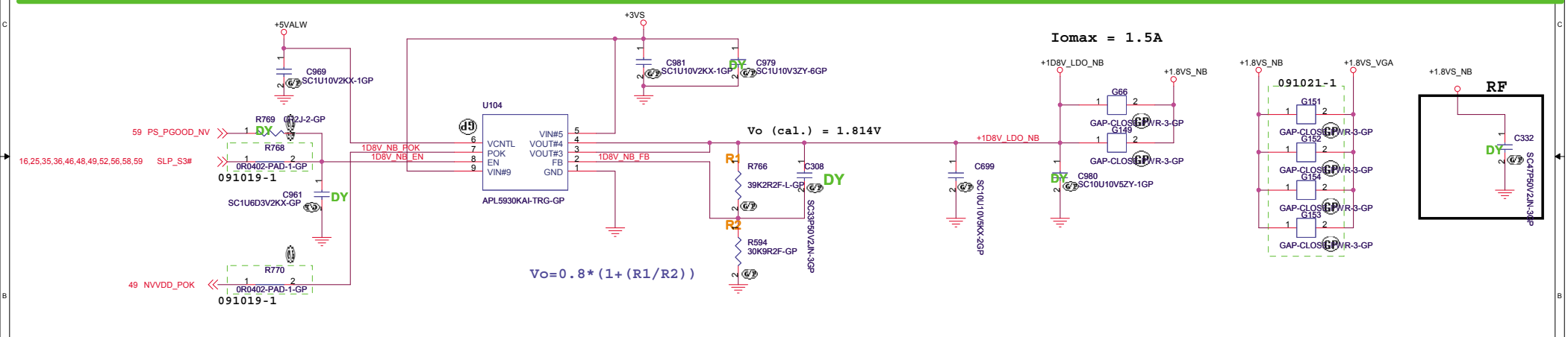
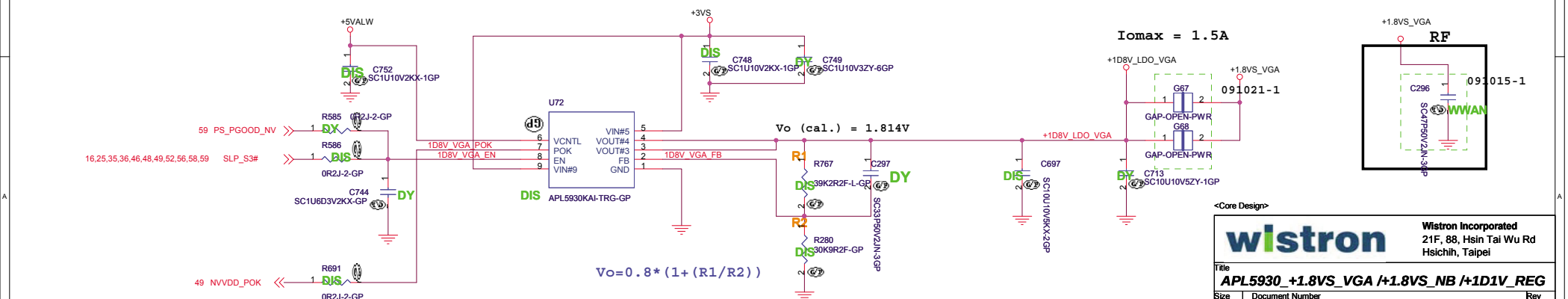
1D1V Iomax: 2.5A
1D0V Iomax: 2A







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Title: APL5930_+1.8VS_VGA /+1.8VS_NB /+1D1V_REG

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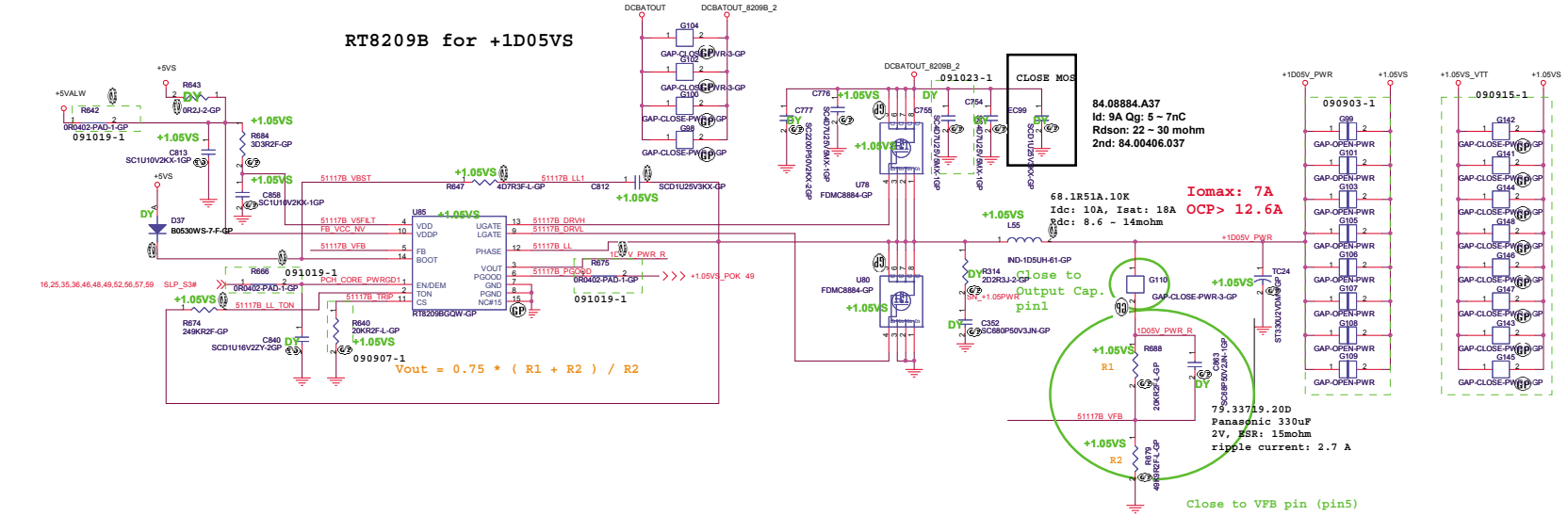

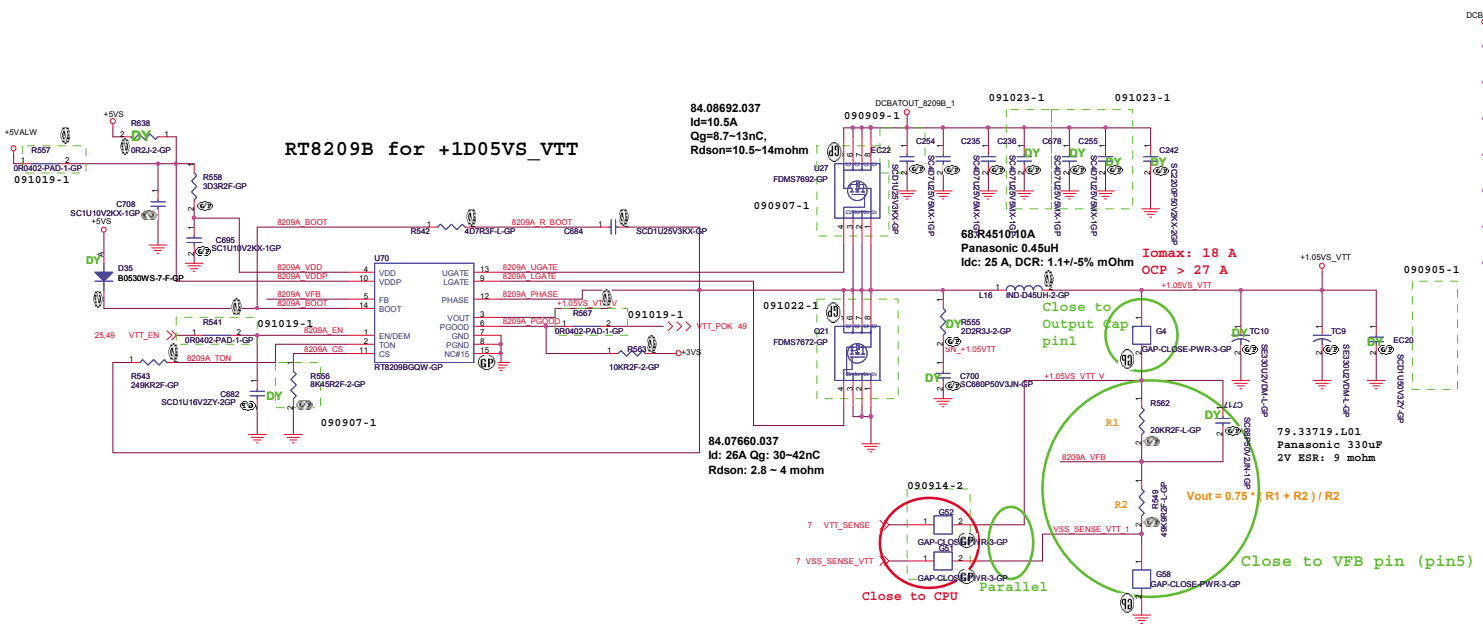

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Title: RT8209B +1.05VS_VTT /+1.05VS

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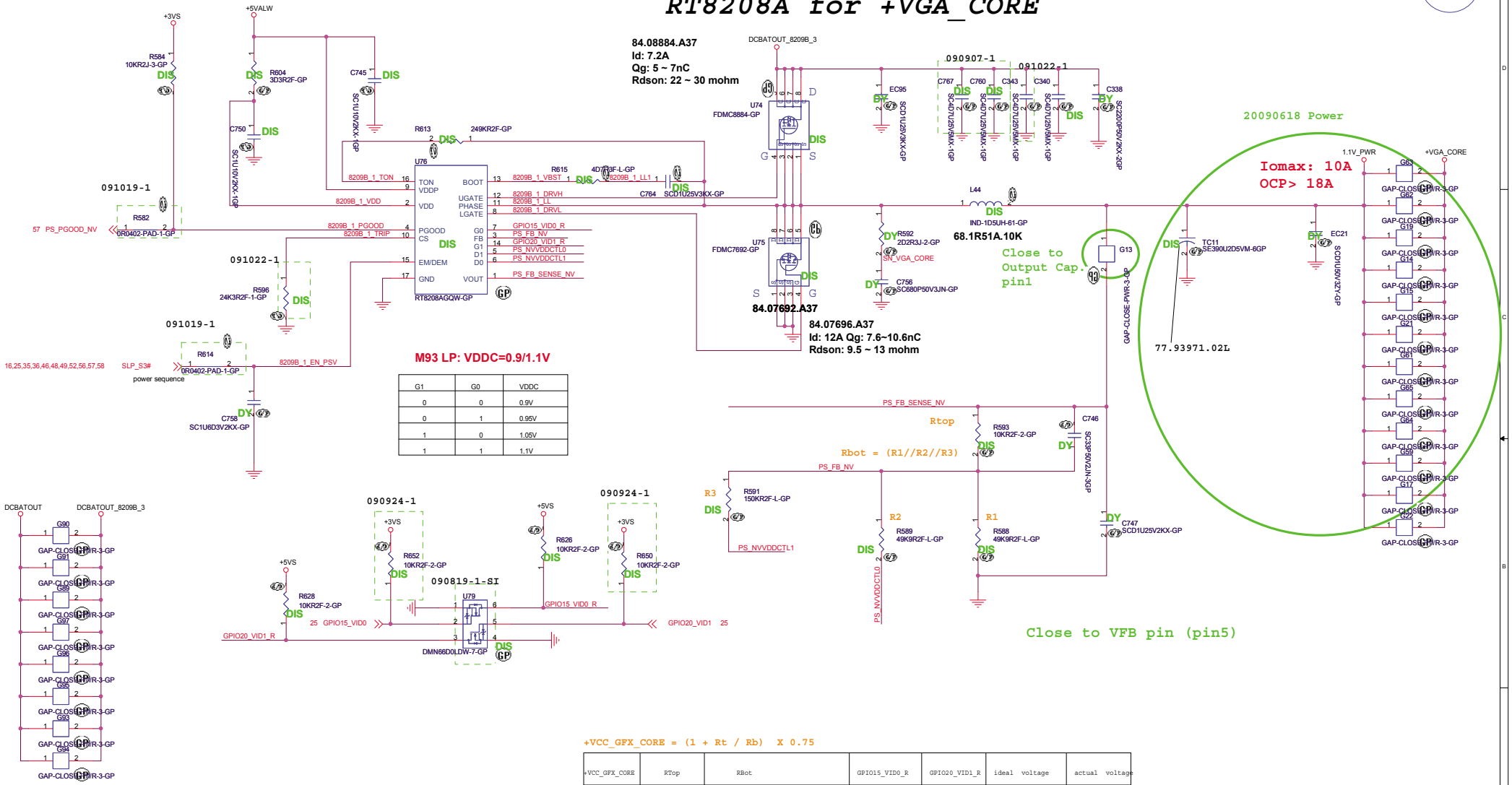
RT8208A for +VGA_CORE



G1	G0	VDDC
0	0	0.9V
0	1	0.95V
1	0	1.05V
1	1	1.1V

+VCC_GFX_CORE = (1 + Rt / Rb) X 0.75

+VCC_GFX_CORE	RTop	RBot	GPIO15_VID0_R	GPIO20_VID1_R	ideal voltage	actual voltage
0.9v	10k	R1 49.9k	LOW	LOW	0.9003	
0.95v	10k	R1 R2 49.9k // 49.9k	LOW	HIGH	0.9493	
1.05v	10k	R1 R3 49.9k // 150k	HIGH	LOW	1.0506	
1.1v	10k	R1 R2 R3 49.9k // 49.9k // 150k	HIGH	HIGH	1.0997	

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Title: RT8208AGQW +VGA_CORE

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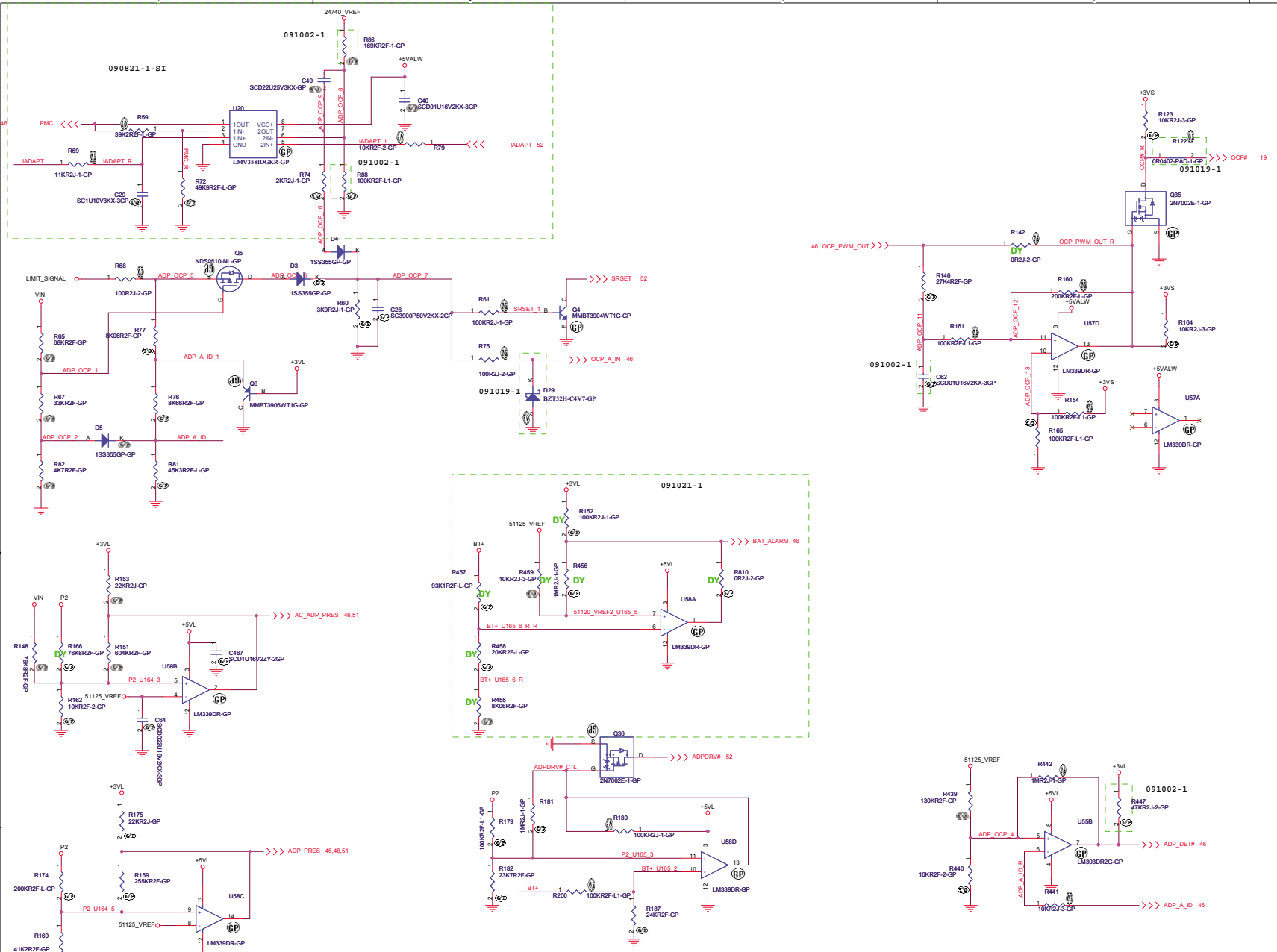

When AC_ADP_PRES=0 -->1
Vin*(R162//R151)/ [(R162//R151)+R148]=51125_VREF
Vin=17.6145V

When AC_ADP_PRES=1 --> 0
[(Vin-51125_VREF)/R148]+[(+3VL-51125_VREF)/(R151+R153)]=51125_VREF/R162

Vin=17.212554V

When ADP_PRES=0->1

P2*(R169//R159)/ [(R169//R159)+R174]=51125_VREF

P2=13.325V

When ADP_PRES=1->0

[(P2-51125_VREF)/R169]+[(+3VL-51125_VREF)/(R175+R159)]=51125_VREF/R169

P2=10.894V

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Title: ADP OCP

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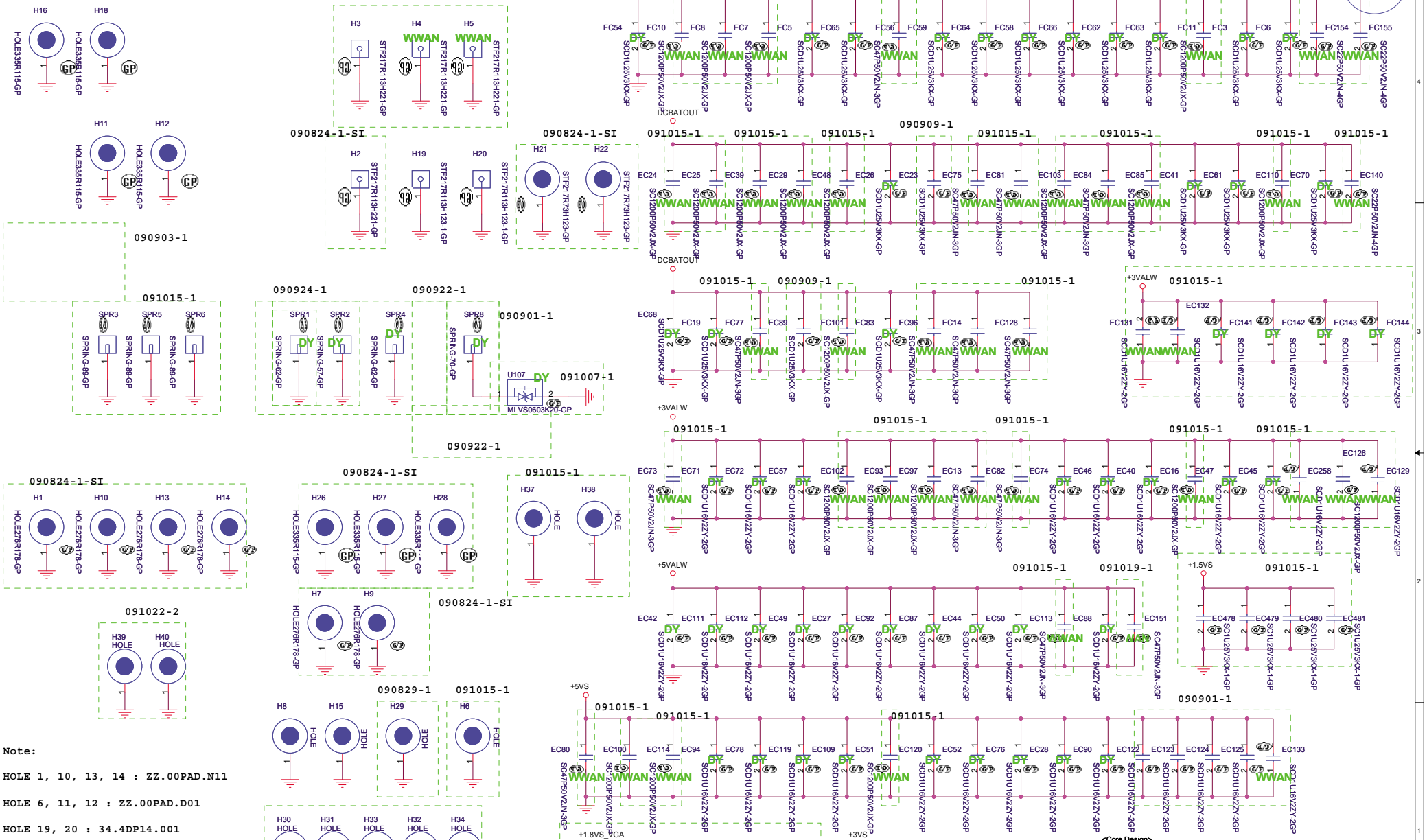
HOLE



Note:

HOLE 1, 10, 13, 14 : ZZ.00PAD.N11

HOLE 6, 11, 12 : ZZ.00PAD.D01

HOLE 19, 20 : 34.4DP14.001

HOLE 17, 25 : ZZ.00PAD.D11

HOLE 2 : 34.4GK01.001

HOLE 3, 4, 5 : 34.4GK01.001

HOLE 21, 22 : 34.4GK02.001

<Core Design>

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Title: HOLE

Size: A3 | Document Number: S-Class Intel | Rev: SD

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