Wistron Confidential

PV

2009/10/19 **REV :PV-01**

<Variant Name>

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Title	*S-Class Intel*	
Size A3	Document Number S-Class Intel	Rev SD
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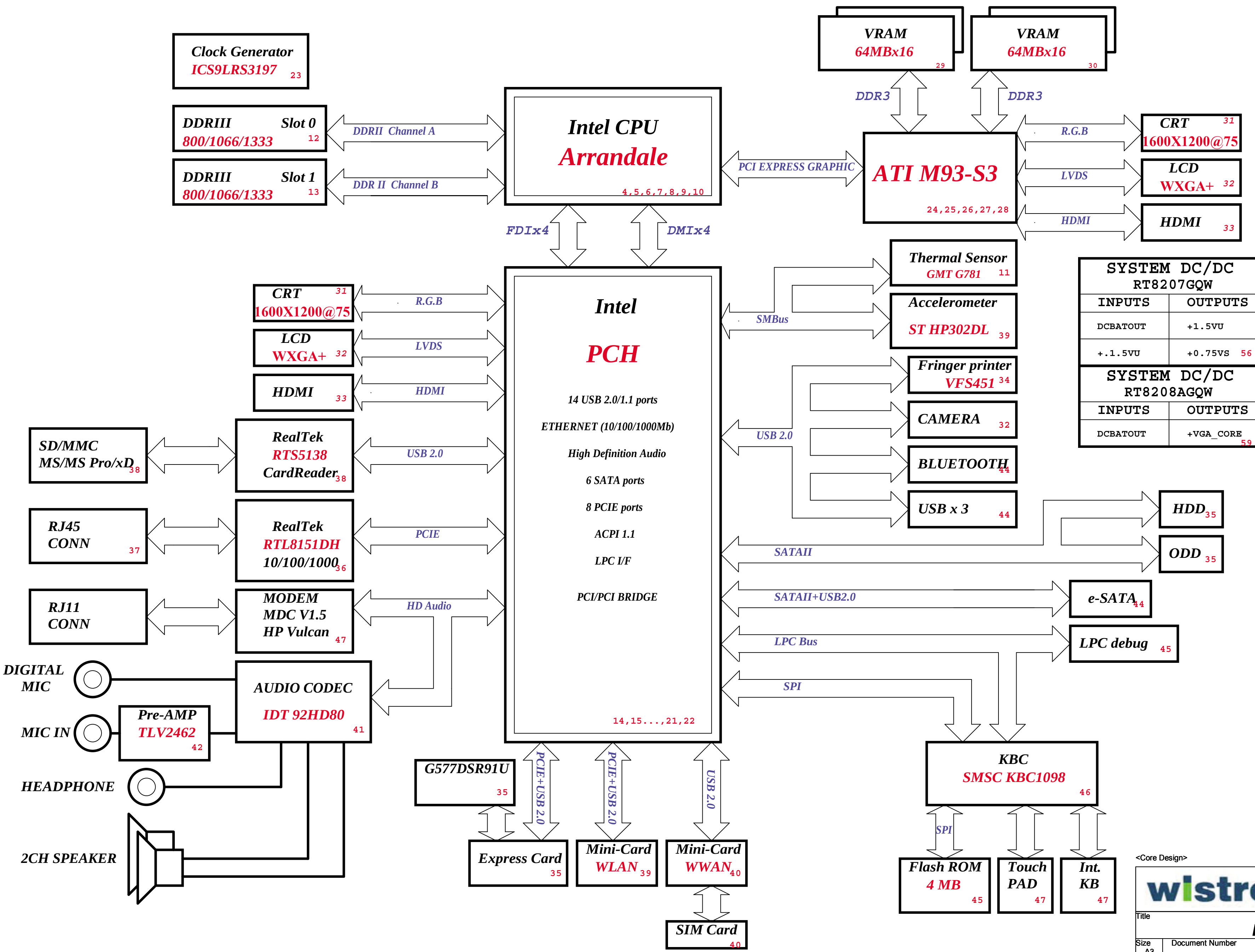
Intel Calpella Arrandale Block Diagram



SYSTEM DC/DC RT8205A

INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 53

SYSTEM DC/DC RT8209B

INPUTS	OUTPUTS
DCBATOUT	+1.05VS_VTT +1.05VS 58

SYSTEM DC/DC ADP3211MNR2G

INPUTS	OUTPUTS
DCBATOUT	+VCC_GFX_CORE 55

SYSTEM DC/DC RT8207GQW

INPUTS	OUTPUTS
DCBATOUT	+1.5VU
+.1.5VU	+0.75VS 56

SYSTEM DC/DC RT8208AGQW

INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 59

TI CHARGER BQ24740

INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 52

CPU DC/DC ADP3212MNR2G

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 65A 54

SYSTEM DC/DC APL5930/APL5930

INPUTS	OUTPUTS
+3VS	+1.8VS_NB +1.8VS_VGA
+1.5VS	+1.1V_REG 57

PCB 6 LAYER

L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

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Title	Block Diagram	
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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

090901-1

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	M93
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	V	V
PCH_SMB_DATA PCH_SMB_CLK	Calpella	X	V	V	V	V	X	X

PCIE Routing page 15

LANE2	EXP
LANE4	WLAN
LANE6	LAN

USB Table page 18

Pair	*Device*
0	*External USB2*
1	*USB1 (Debug port)*
2	*ESATA USB4*
3	*Card Reader*
4	*NEW CARD*
5	*FREE*
6	*WLAN*
7	*FREE*
8	*BLUETOOTH*
9	*WWAN*
10	*Fingerprint*
11	*External USB3*
12	*CAMERA*
13	*FREE*

091019-1

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Title: **Notes List**

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CPU(1/7)

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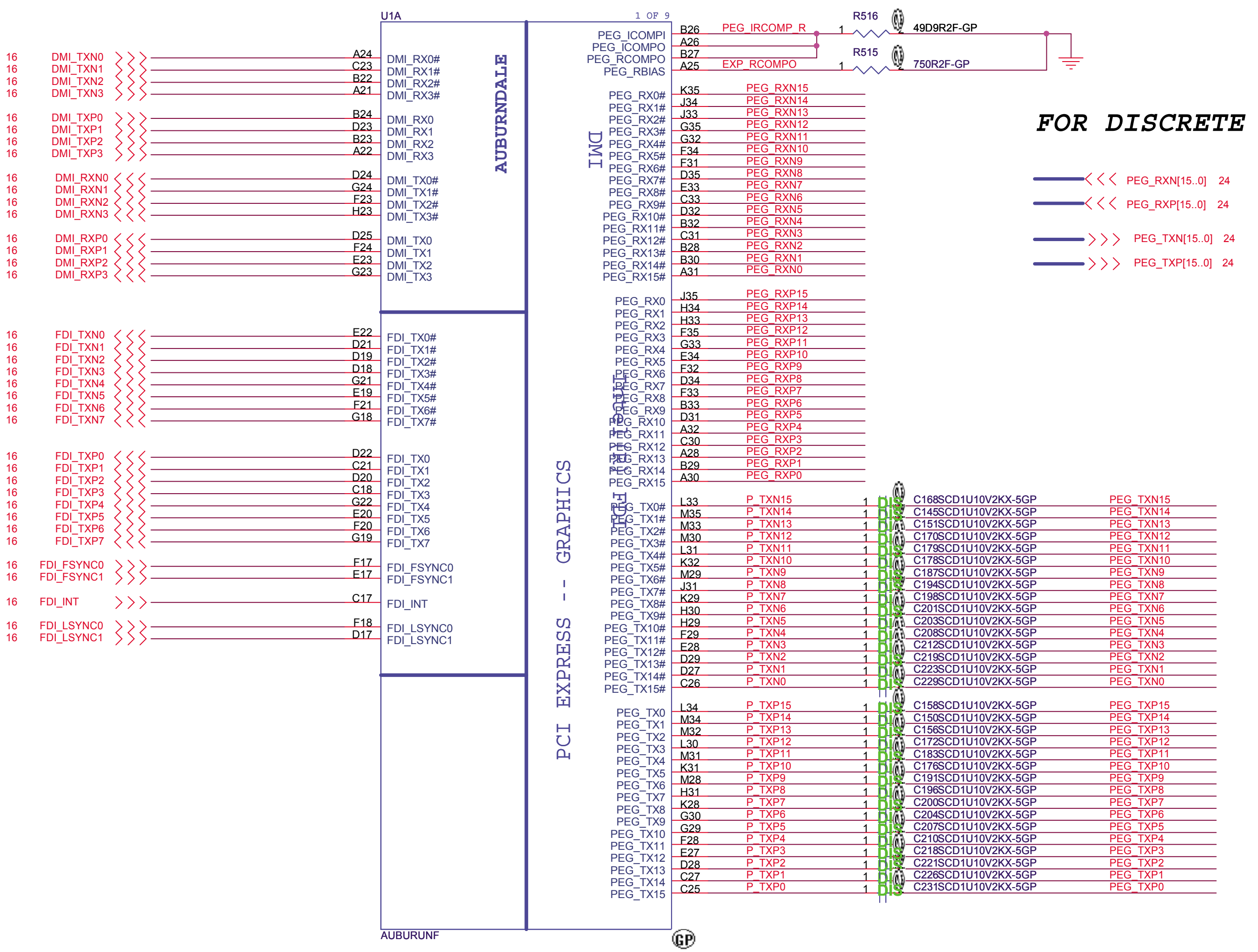

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Title		
CPU (1/7)-PEG / DMI / FDI		
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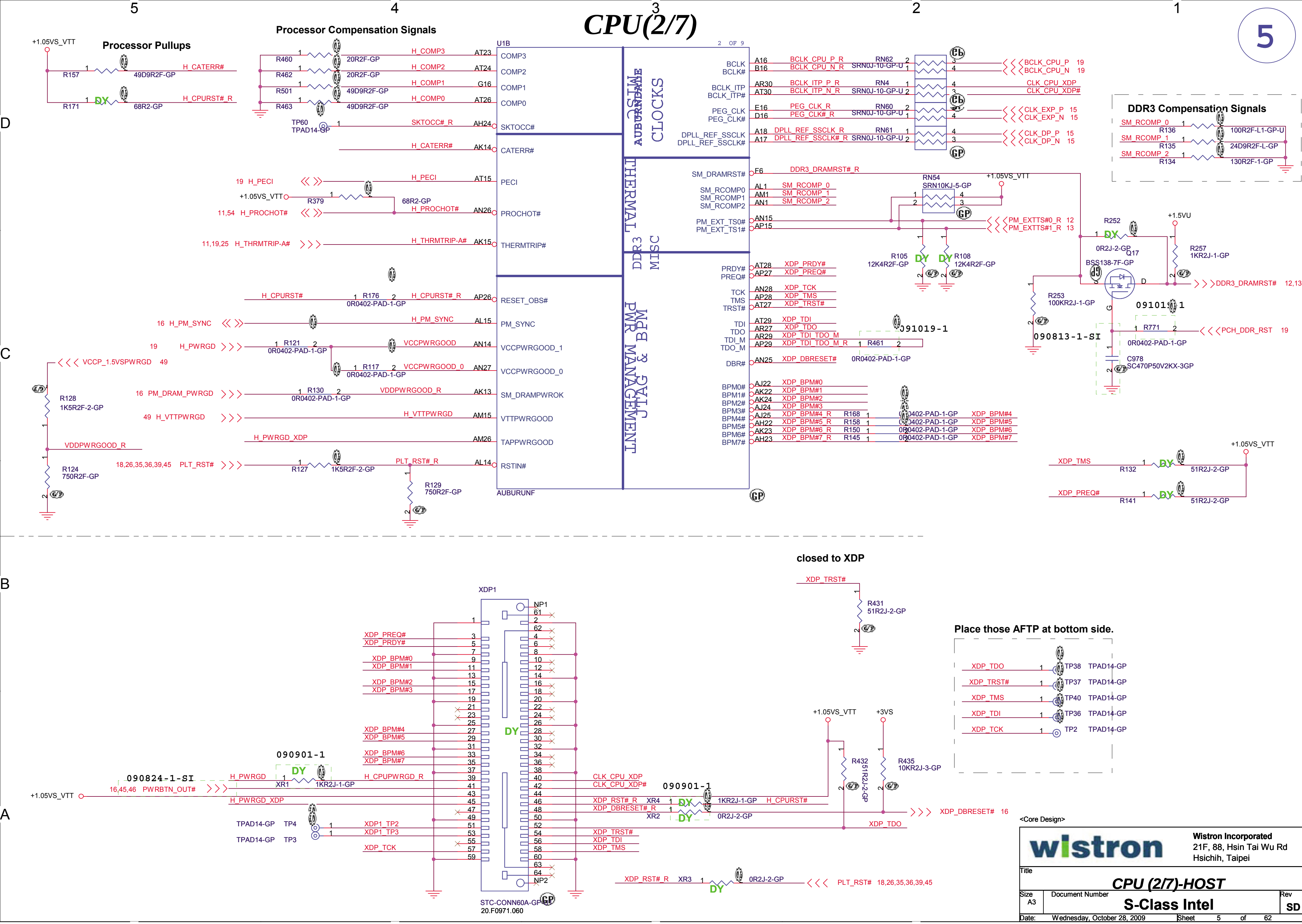
CPU(2/7)



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Title	CPU (2/7)-HOST	
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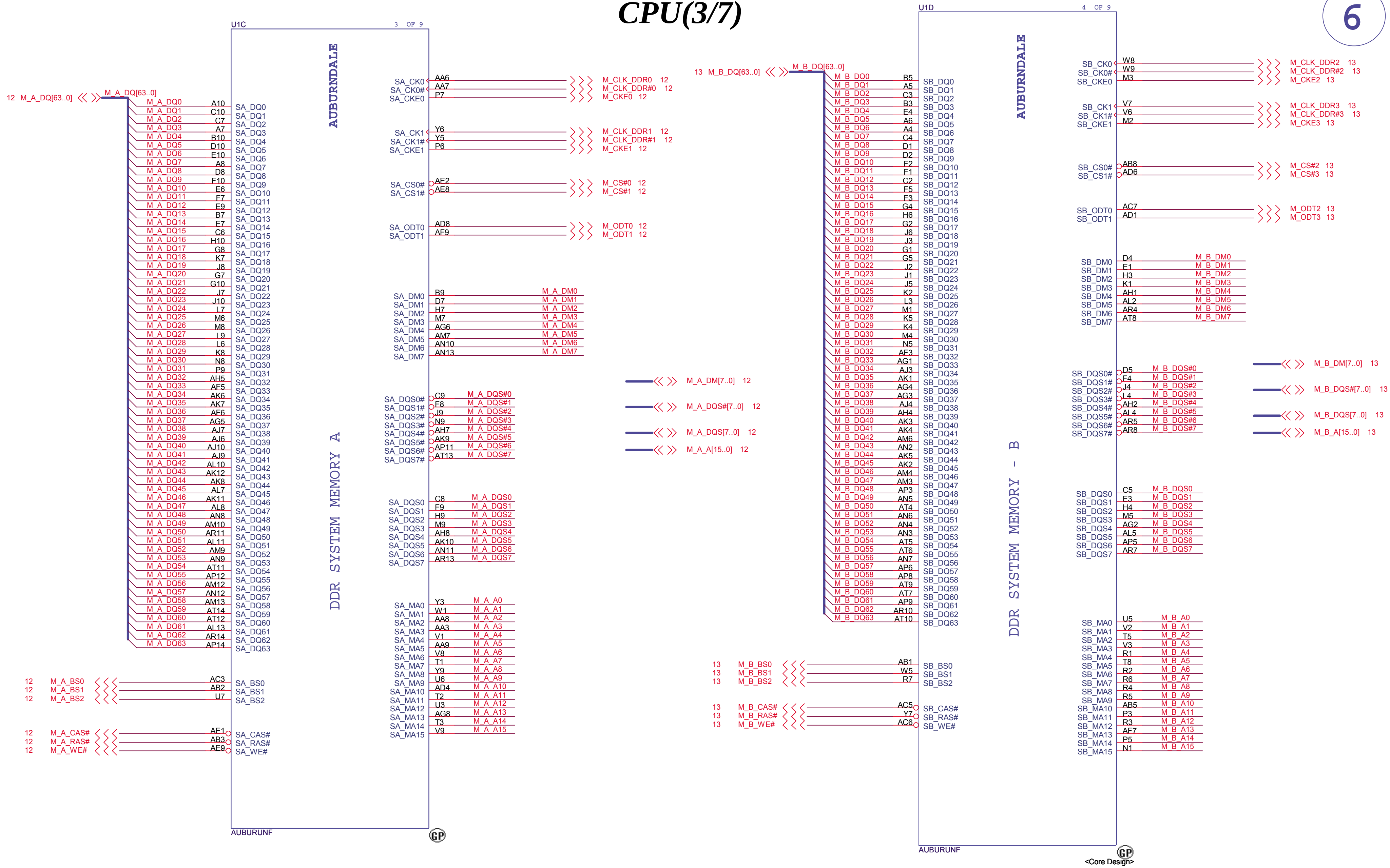
CPU(3/7)



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Title	**CPU (3/7)-MEM INTERFACE**	
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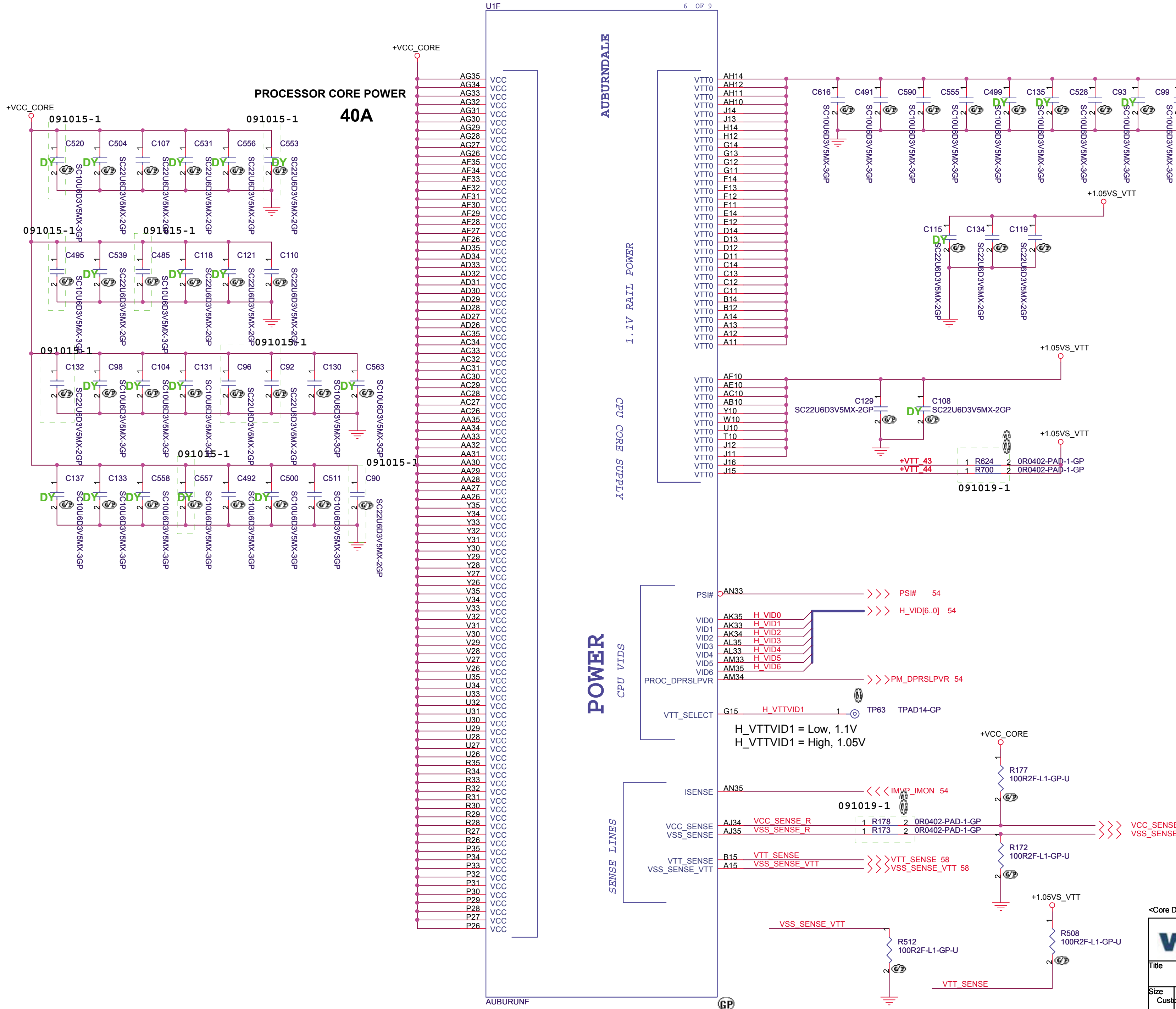
CPU(4/7)



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail values are
Auburndale VTT=1.05V
Clarksfield VTT=1.1V

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Title	CPU (4/7)-POWER
Size	Custom
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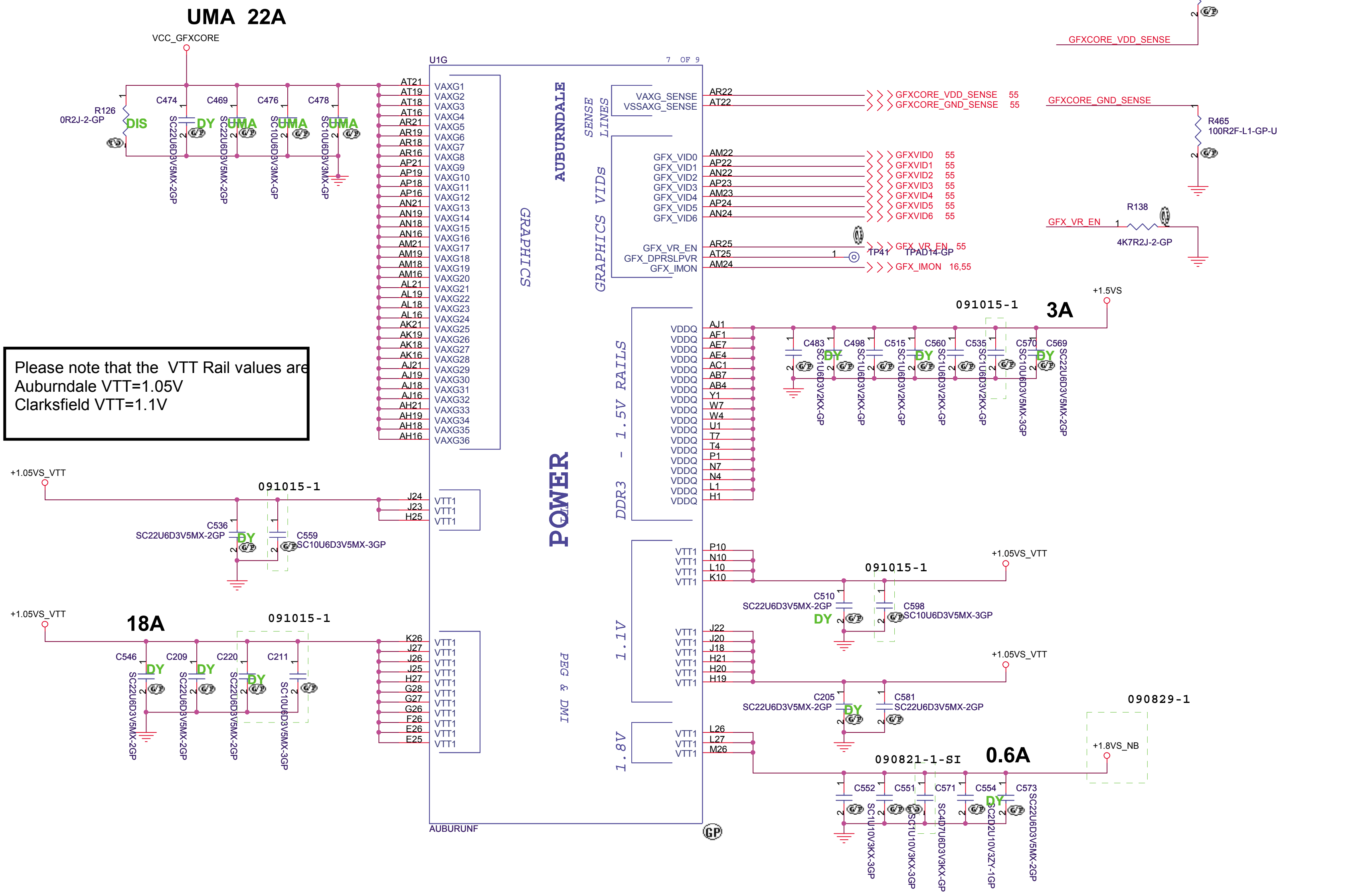
CPU(5/7)



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Title	CPU (5/7)-Graphic POWER	
Size A3	Document Number S-Class Intel	Rev SD
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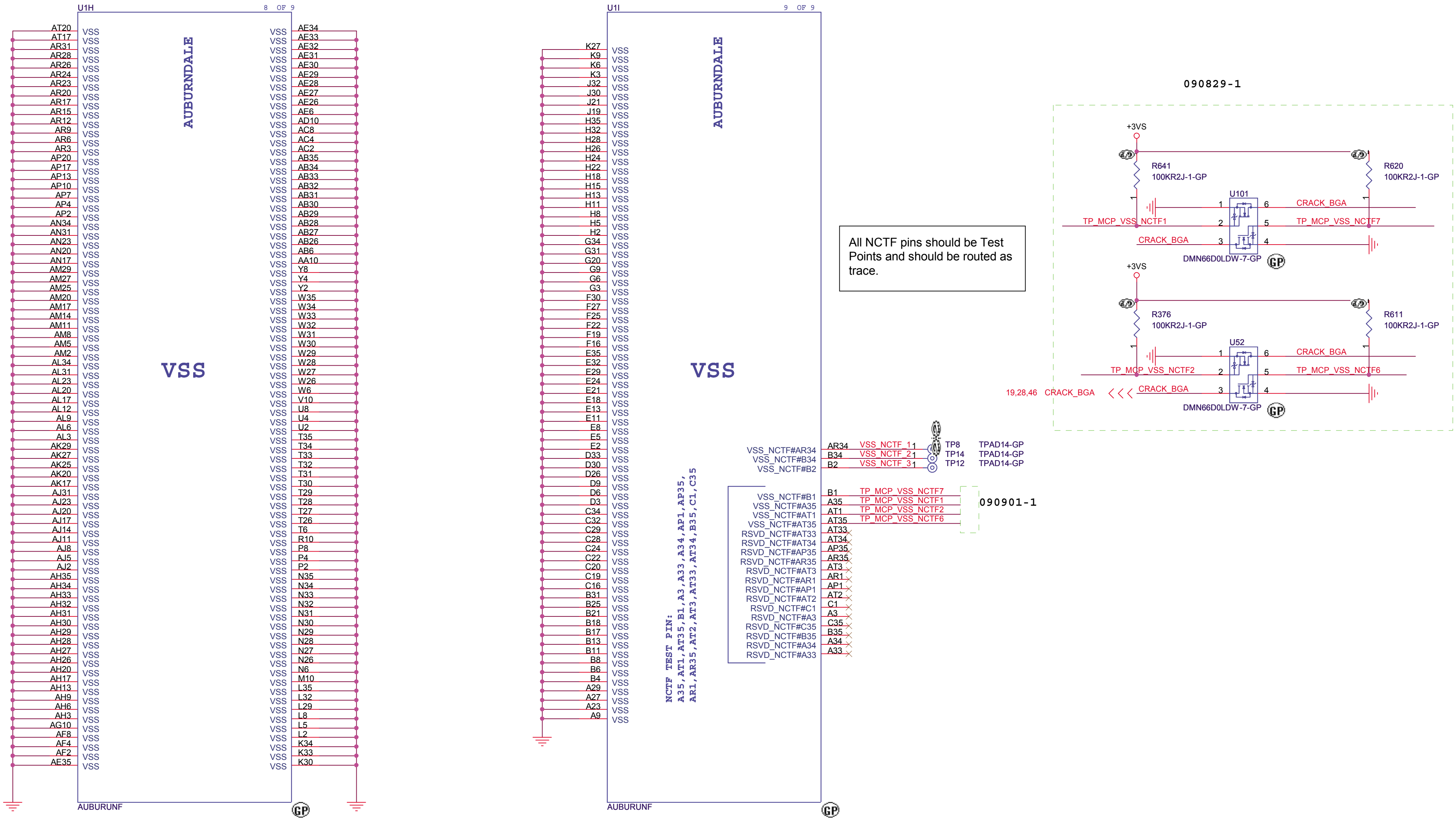
CPU(6/7)



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Title: *CPU (6/7)-VSS*

Size: A3 | Document Number: **S-Class Intel** | Rev: SD

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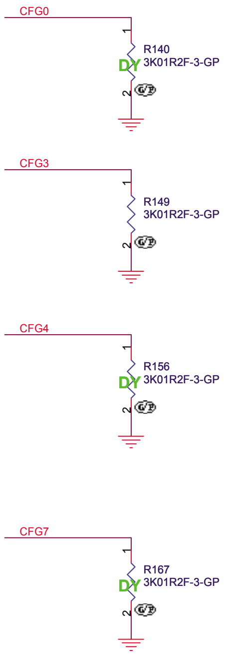
CPU(7/7)

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



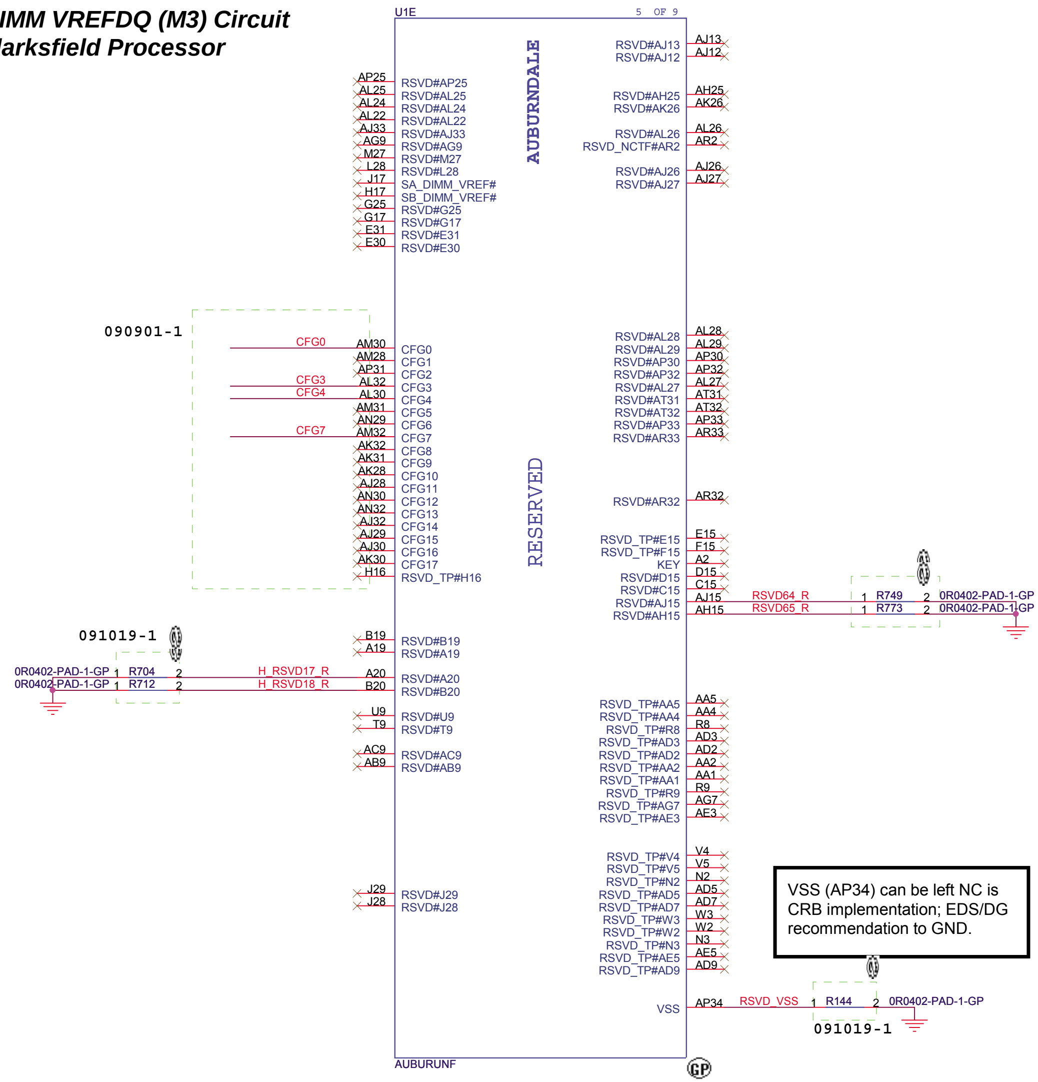
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

0829 SA

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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Title	CPU (7/7)-RESERVED		
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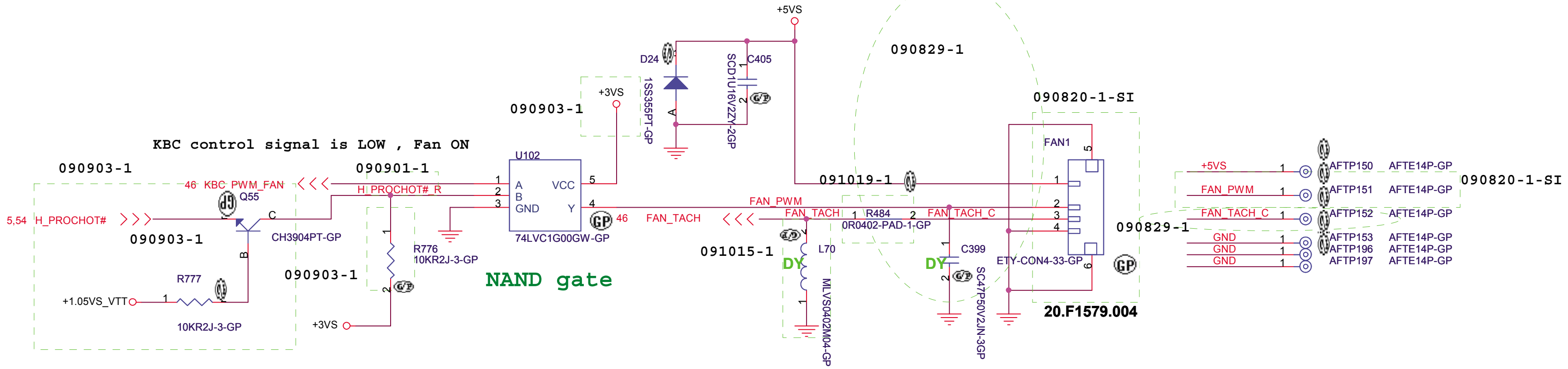
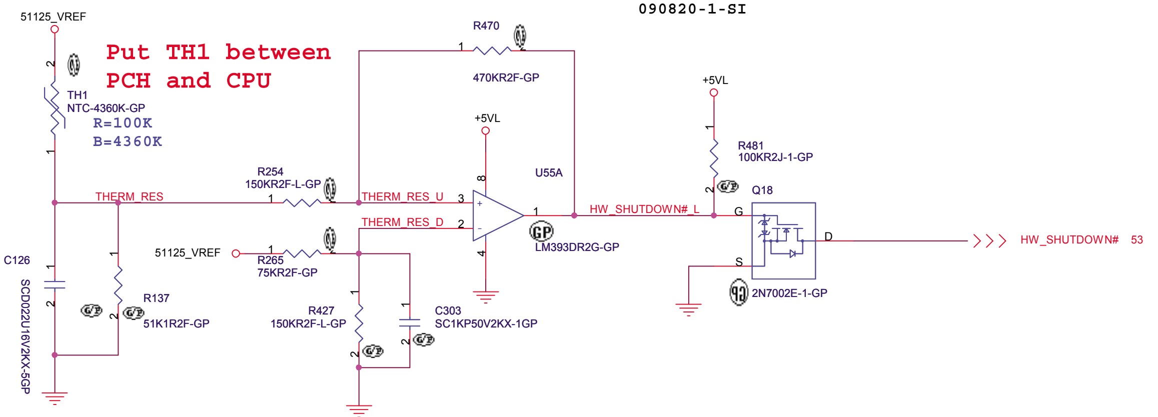
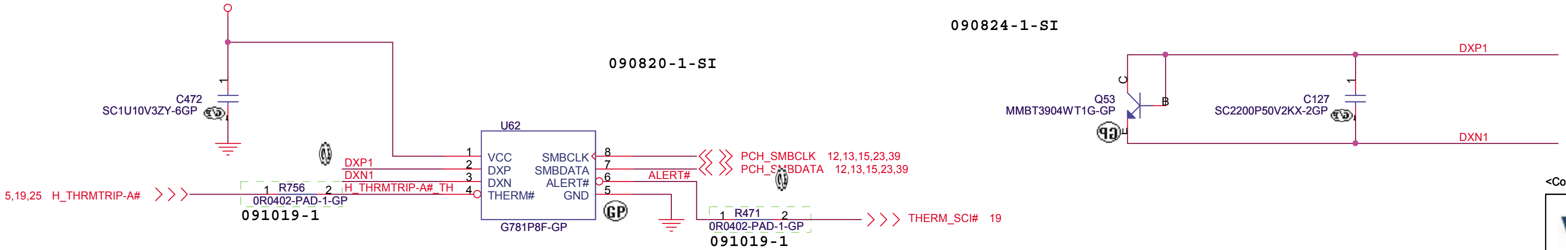
4 WIRE PWM Fan Control circuit



T8 H/W Shutdown Control circuit



Thermal IC Control circuit



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Title	G787S11U-GP THERMAL	
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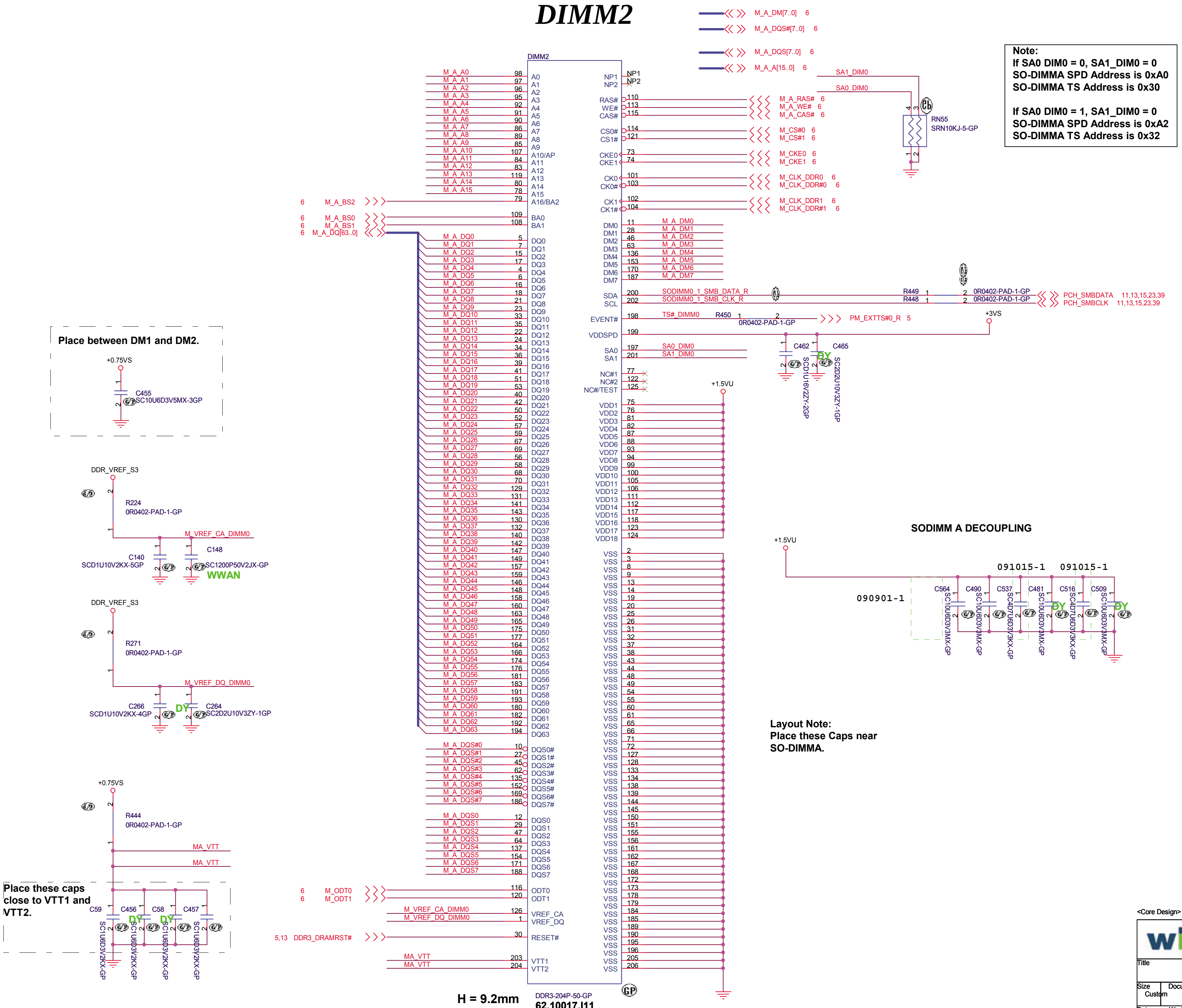
DIMM2



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

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Title	DDRIII Socket DM1	
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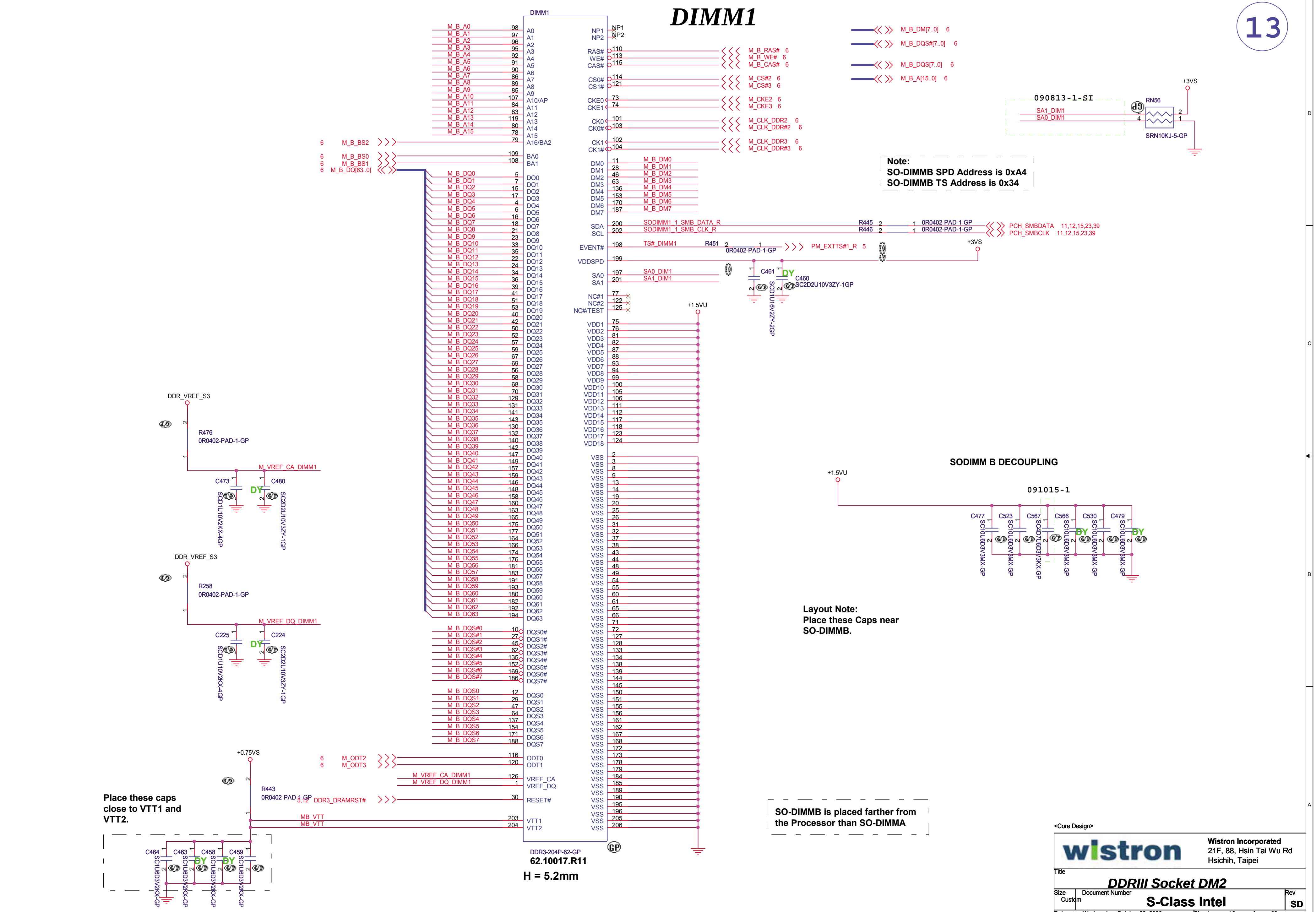
DIMM1



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Title	DDRIII Socket DM2	
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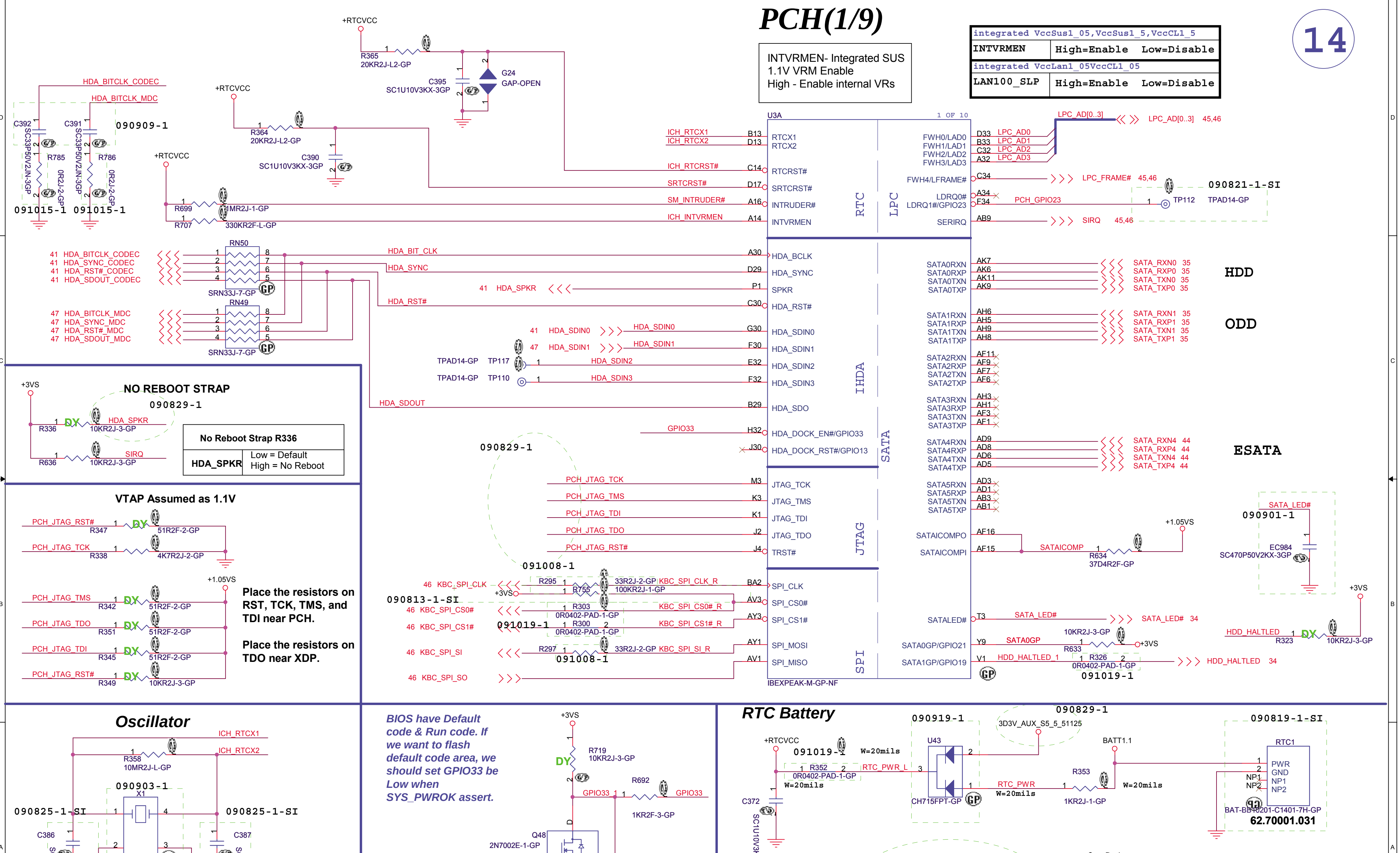
PCH(1/9)



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Title	PCH (1/9)-SATA/SPI/LPC	
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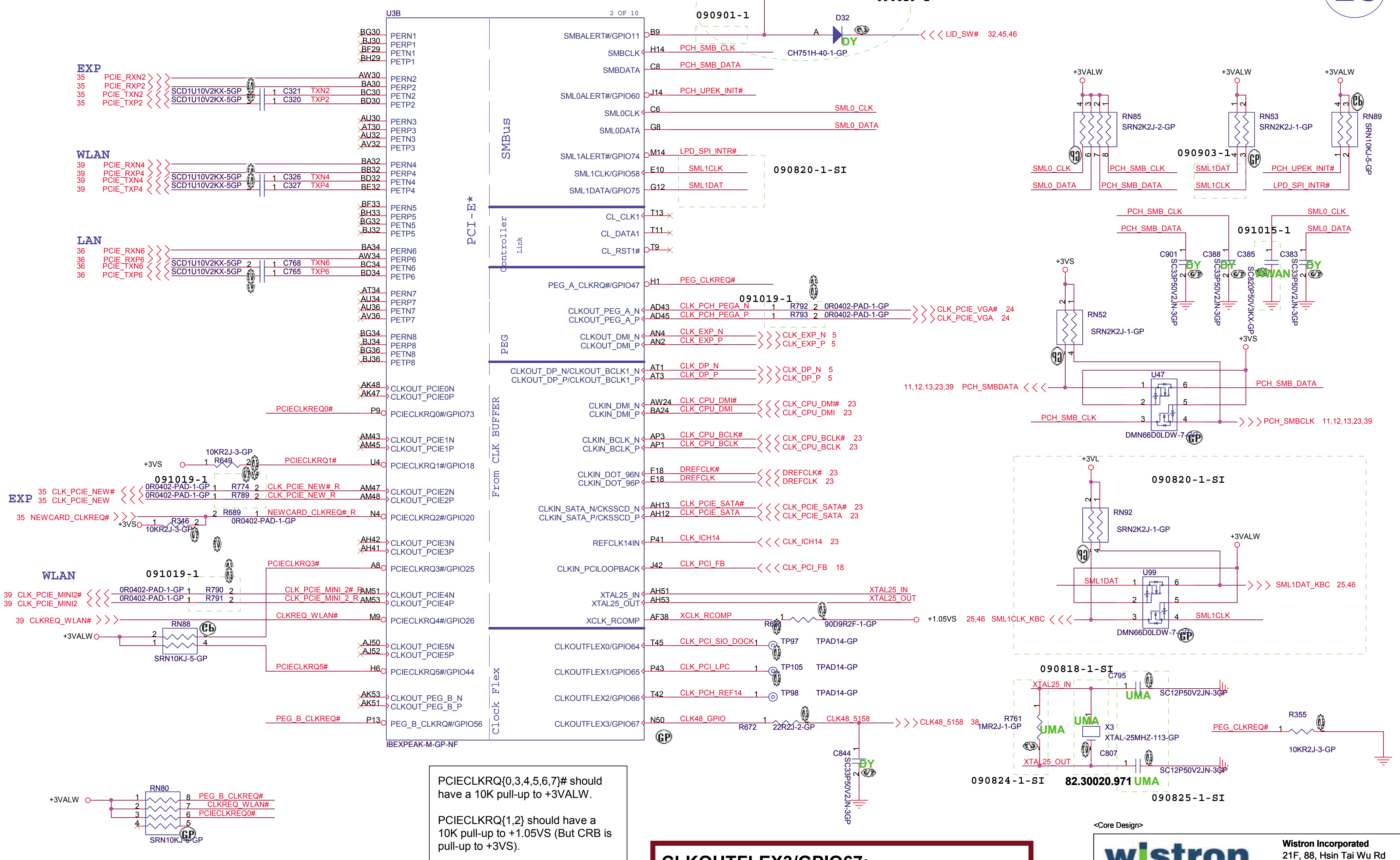
PCH(2/9)



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

CLKOUTFLEX3/GPIO67: Configurable as an programmable output clock 48MHz output to SIO.

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Title: PCH (2/9)-PCIE/SMBUS

Size: A3 | Document Number: S-Class Intel | Rev: SD

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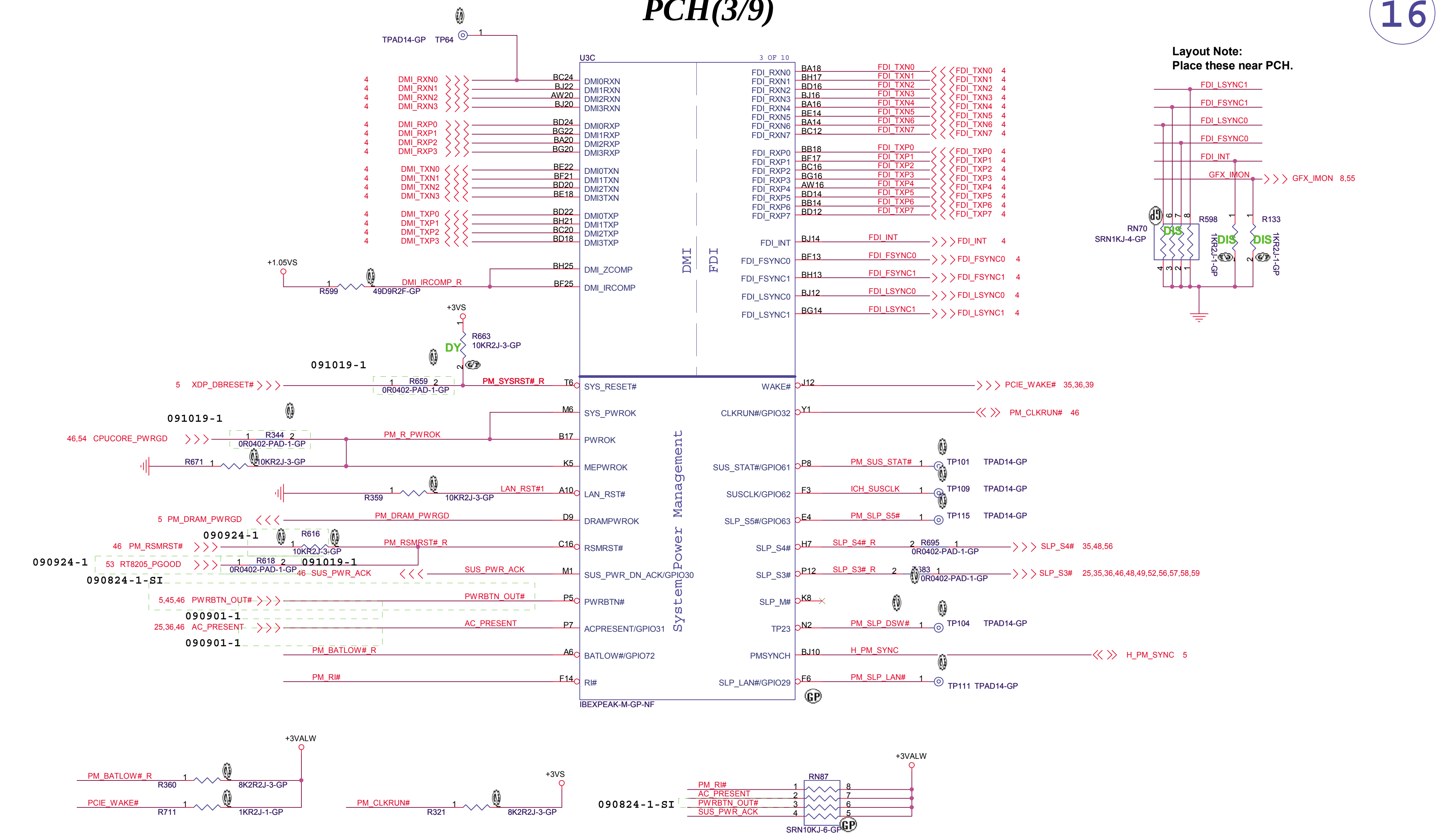
PCH(3/9)

Layout Note:
Place these near PCH.



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Title	PCH (3/9)-DMI/SYS PWR	
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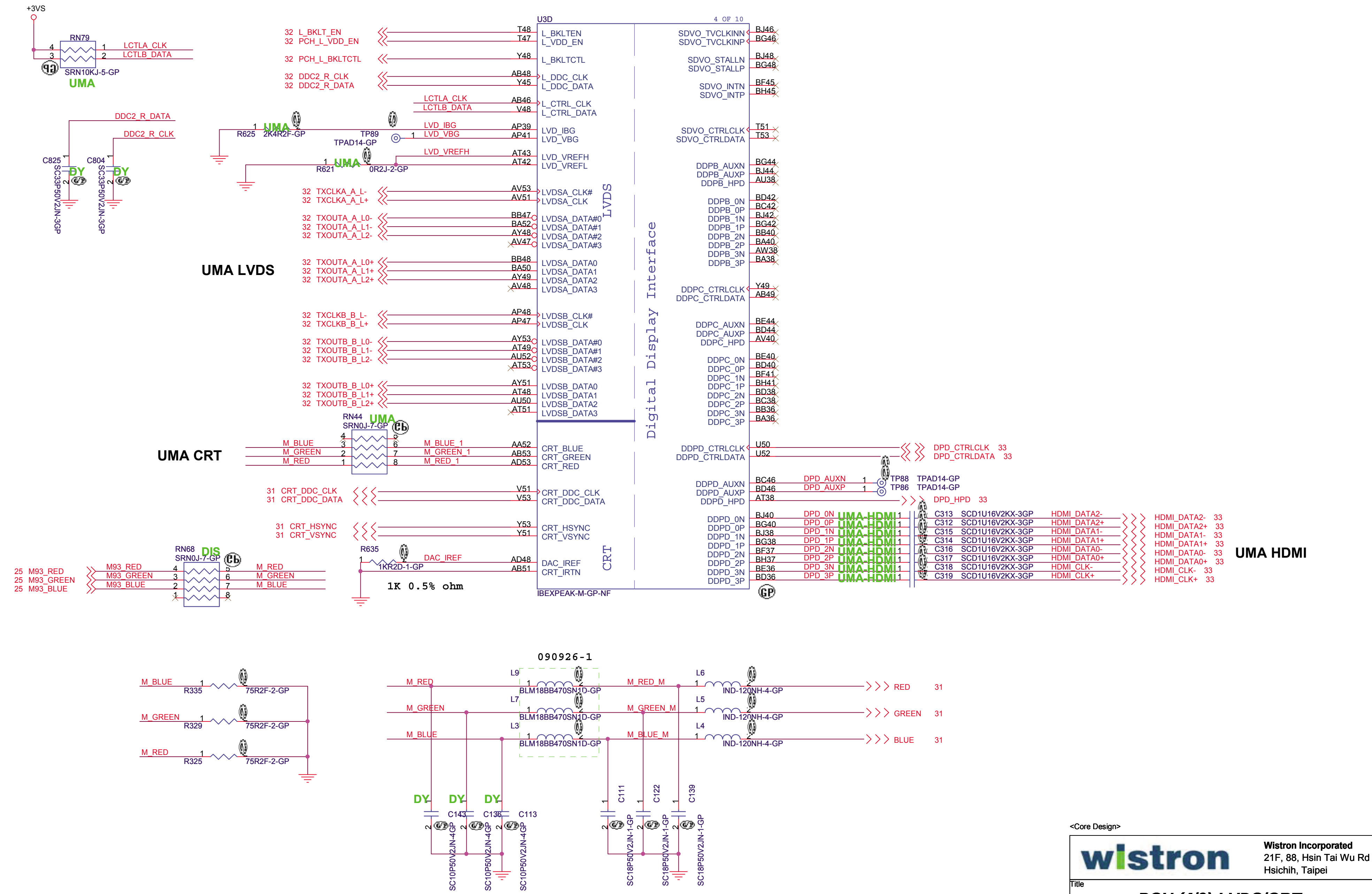
PCH(4/9)



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Title	PCH (4/9)-LVDS/CRT	
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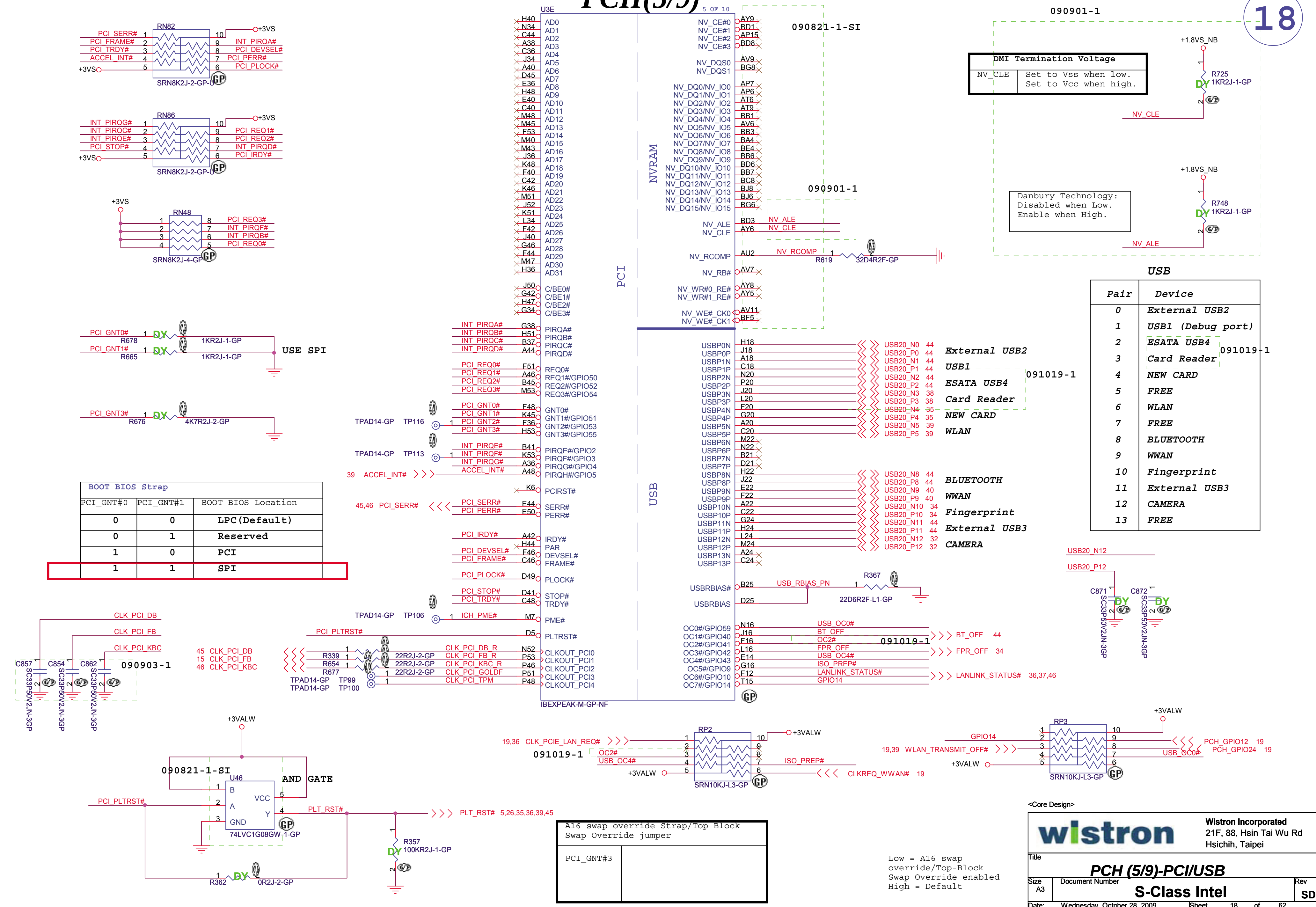
PCH(5/9)



DMI Termination Voltage

NV_CLE	Set to Vss when low. Set to Vcc when high.

USB

Pair	Device
0	External USB2
1	USB1 (Debug port)
2	ESATA USB4
3	Card Reader
4	NEW CARD
5	FREE
6	WLAN
7	FREE
8	BLUETOOTH
9	WWAN
10	Fingerprint
11	External USB3
12	CAMERA
13	FREE

BOOT BIOS Strap

PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
0	1	Reserved
1	0	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper

PCI_GNT#3	

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Title: PCH (5/9)-PCI/USB

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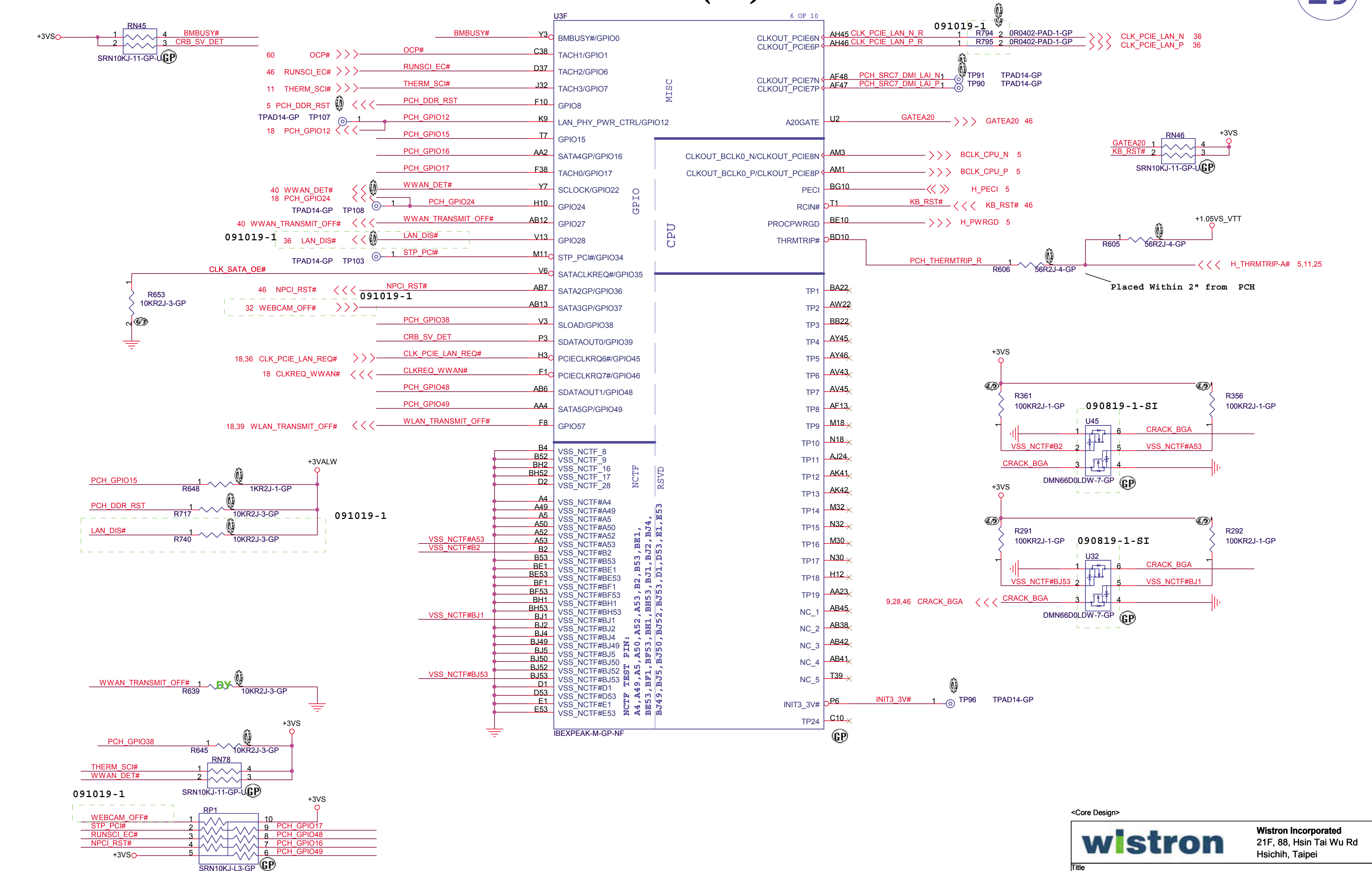

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Title		
PCH (6/9)-GPIO		
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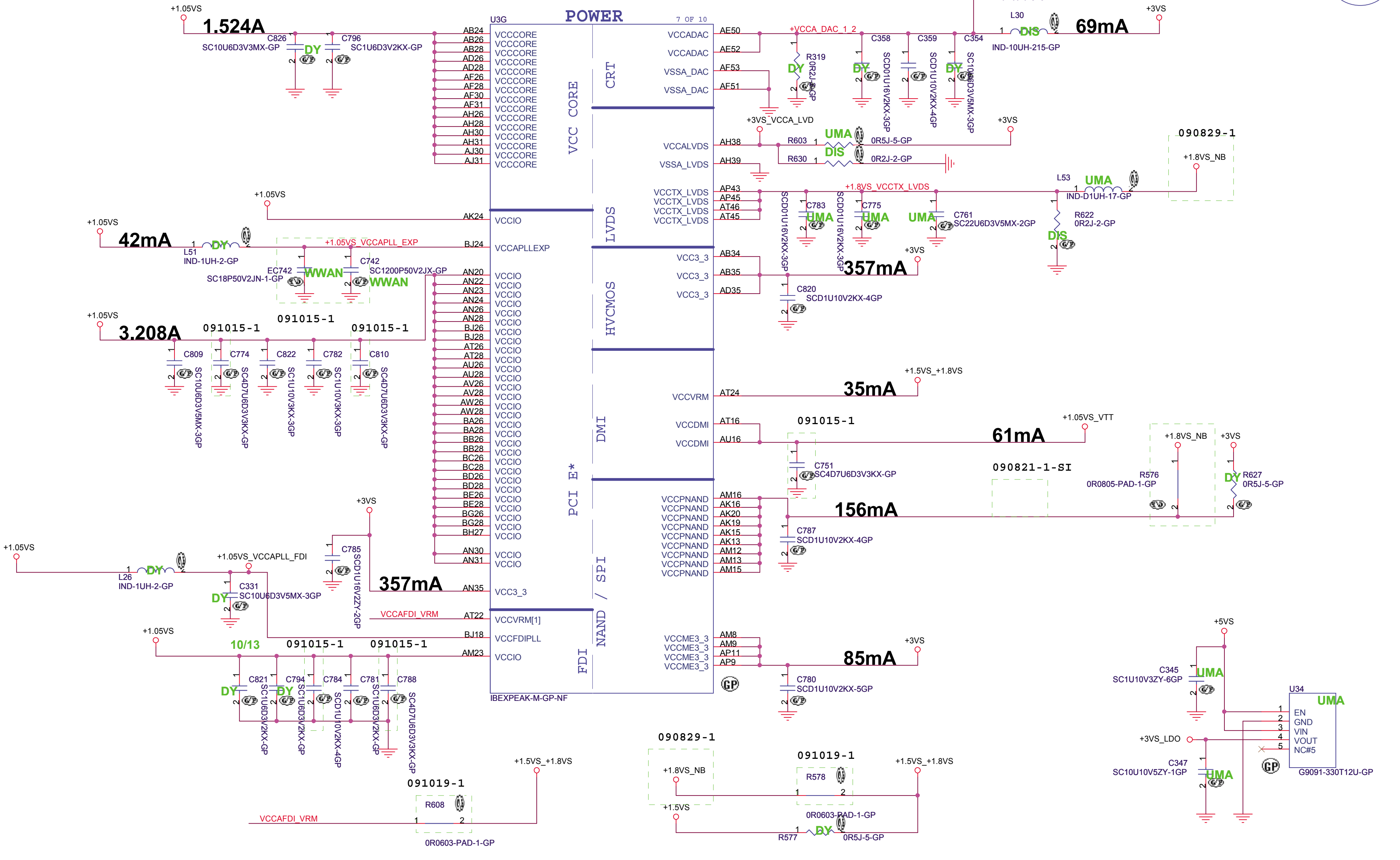

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Title: PCH (7/9)-PWR 1
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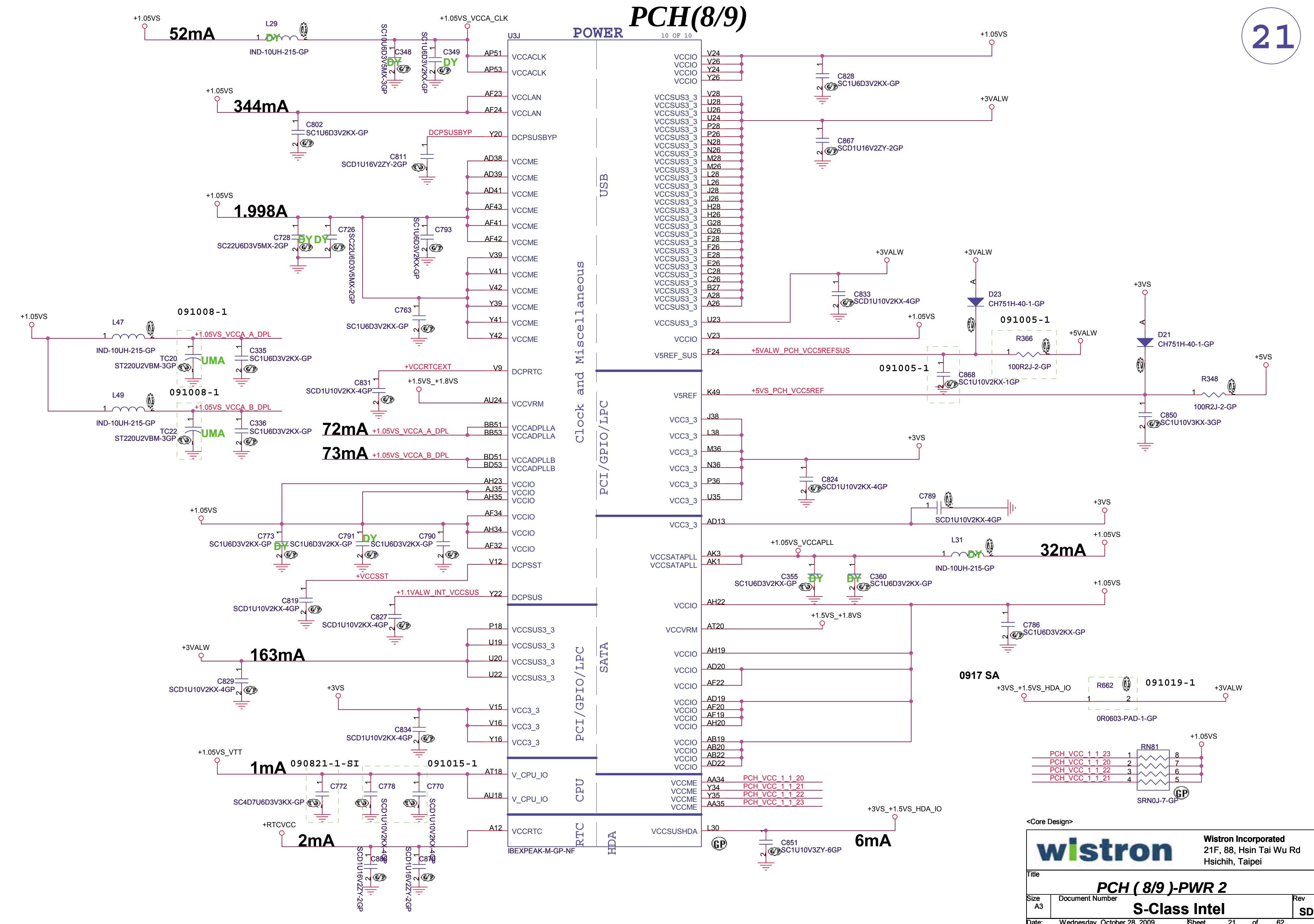

PCH(8/9)
21
U3J
POWER
10 OF 10
IBEXPEAK-M-GP-NF
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
+1.05VS
52mA
L29
IND-10UH-215-GP
DY
+1.05VS_VCCA_CLK
C348
C349
SC10U6D3V5MX-3GP
SC1U6D3V2KX-GP
AP51 VCCACLK
AP53 VCCACLK
344mA
AF23 VCCLAN
AF24 VCCLAN
C802
SC1U6D3V2KX-GP
DCPSUSBYP
Y20 DCPSUSBYP
C811
SCD1U16V2ZY-2GP
AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
1.998A
C728
C726
SC22U6D3V5MX-2GP
C793
SC1U6D3V2KX-GP
C763
091008-1
L47
+1.05VS_VCCA_A_DPL
C335
TC20
ST220U2VBM-3GP
UMA
L49
+1.05VS_VCCA_B_DPL
C336
TC22
+VCCRTCEXT
V9 DCPRTC
C831
SCD1U10V2KX-4GP
+1.5VS_+1.8VS
AU24 VCCVRM
72mA
73mA
BB51 VCCADPLLA
BB53 VCCADPLLA
BD51 VCCADPLLB
BD53 VCCADPLLB
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO
C773
C791
C790
V12 DCPSST
+VCCSST
C819
+1.1VALW_INT_VCCSUS
Y22 DCPSUS
C827
+3VALW
163mA
P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
C829
+3VS
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
C834
+1.05VS_VTT
1mA
090821-1-SI
091015-1
C772
SC4D7U6D3V3KX-GP
C778
C770
SCD1U10V2KX-4GP
AT18 V_CPU_IO
AU18 V_CPU_IO
+RTCVCC
2mA
A12 VCCRTC
C886
C876
SCD1U16V2ZY-2GP
V24 V26 Y24 Y26 VCCIO
C828
+3VALW
VCCSUS3_3
C867
C833
D23
CH751H-40-1-GP
091005-1
R366
100R2J-2-GP
+5VALW
U23 VCCSUS3_3
V23 VCCIO
F24 V5REF_SUS
+5VALW_PCH_VCC5REFSUS
C868
SC1U10V2KX-1GP
+3VS
D21
+5VS
R348
K49 V5REF
+5VS_PCH_VCC5REF
C850
SC1U10V3KX-3GP
J38 L38 M36 N36 P36 U35 VCC3_3
C824
C789
AD13 VCC3_3
L31
+1.05VS_VCCAPLL
AK3 AK1 VCCSATAPLL
C355
C360
32mA
AH22 VCCIO
C786
AT20 VCCVRM
AH19 AD20 AF22 AD19 AF20 AF19 AH20 AB19 AB20 AB22 AD22 VCCIO
0917 SA
+3VS_+1.5VS_HDA_IO
R662
091019-1
0R0603-PAD-1-GP
RN81
PCH_VCC_1_1_23
PCH_VCC_1_1_20
PCH_VCC_1_1_22
PCH_VCC_1_1_21
SRN0J-7-GP
AA34 Y34 Y35 AA35 VCCME
L30 VCCSUSHDA
C851
SC1U10V3ZY-6GP
6mA
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Title
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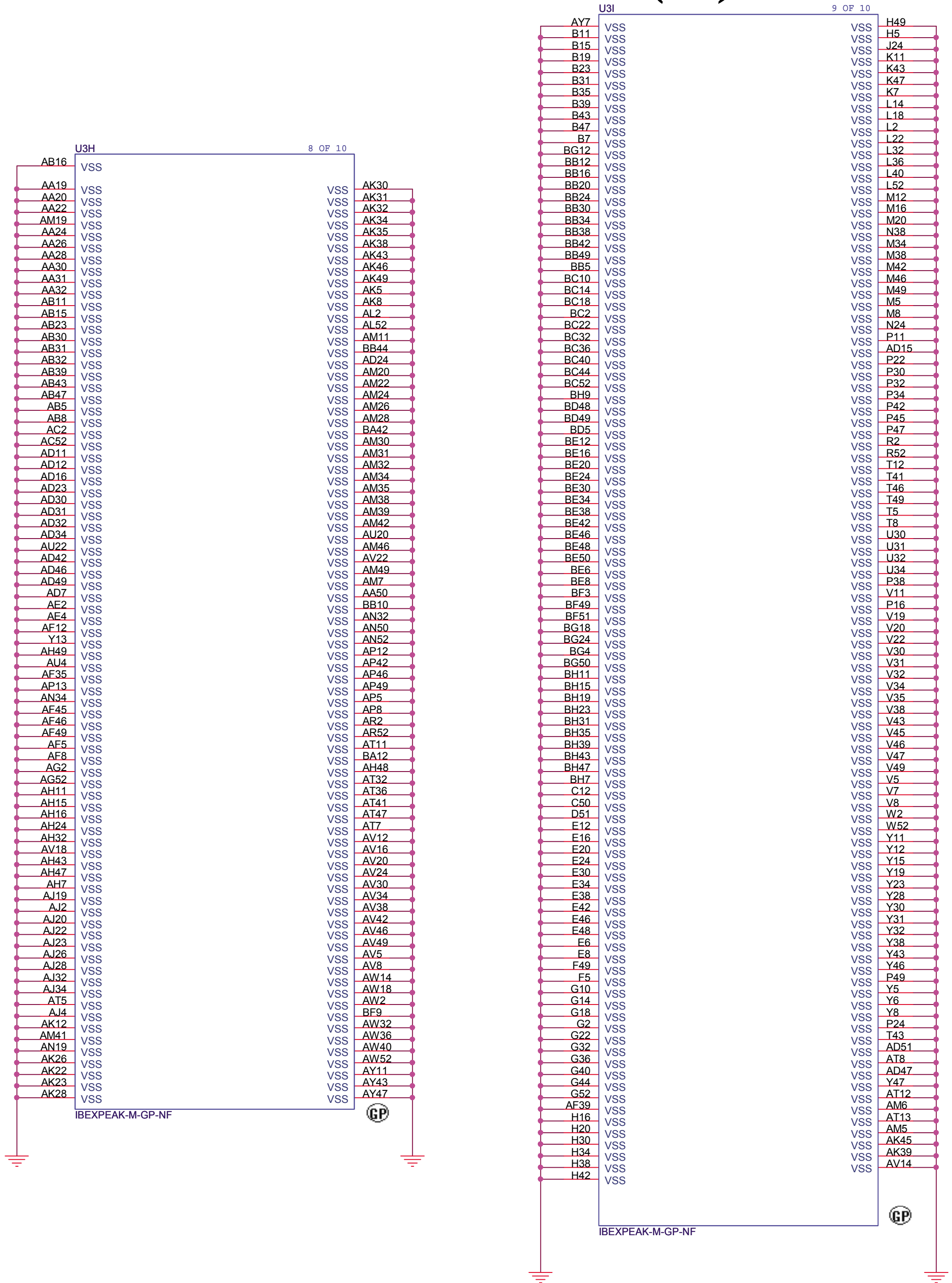
PCH(9/9)



<Core Design>

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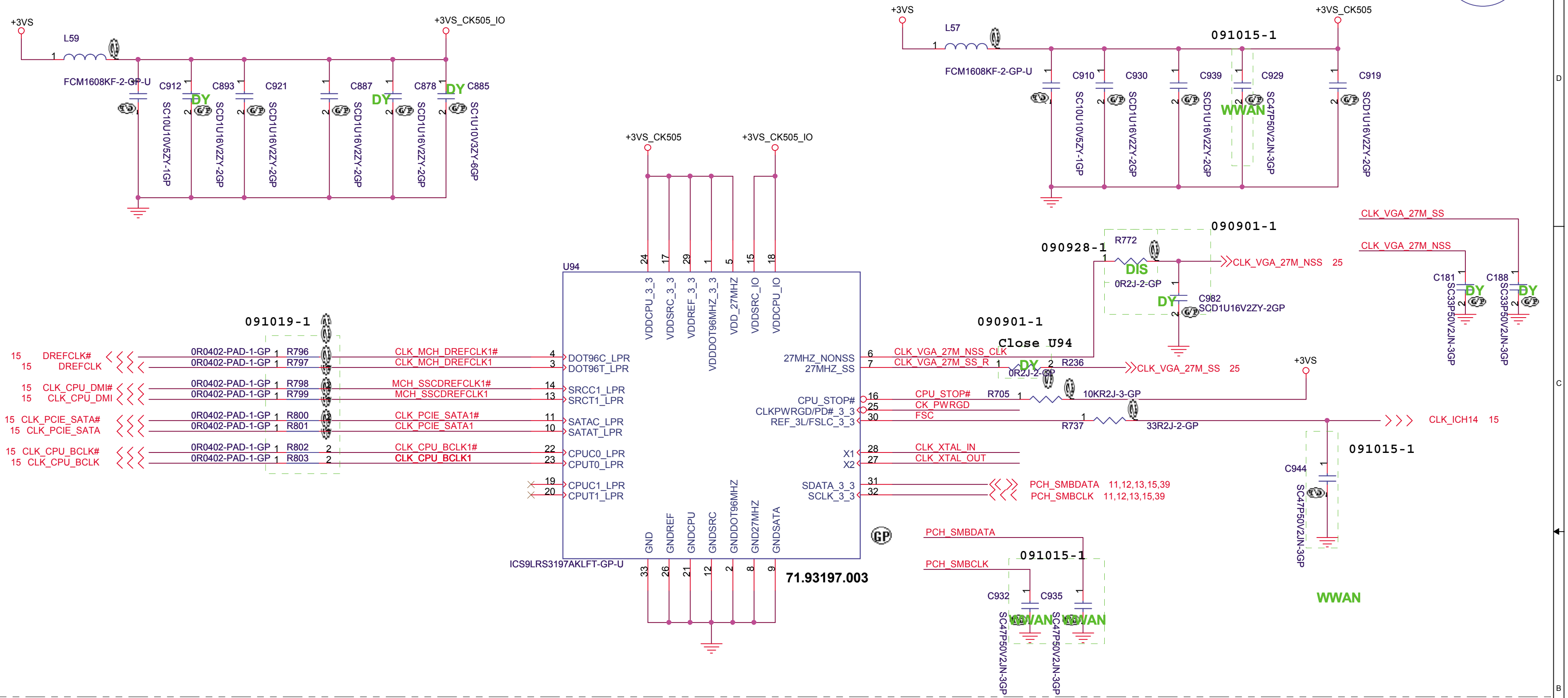
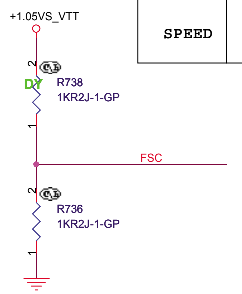
Title	PCH (9/9)-VSS	
Size A3	Document Number S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 22 of 62	

CLOCK GENERATOR

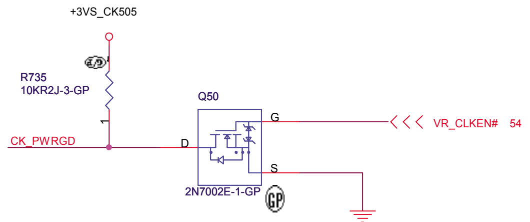


FSB Frequency Select

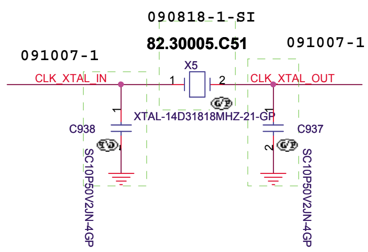
FSC	0	1
SPEED	133MHz (Default)	100MHz



Clock Gen. Eable



Clock Gen. Crystal



<Core Design>

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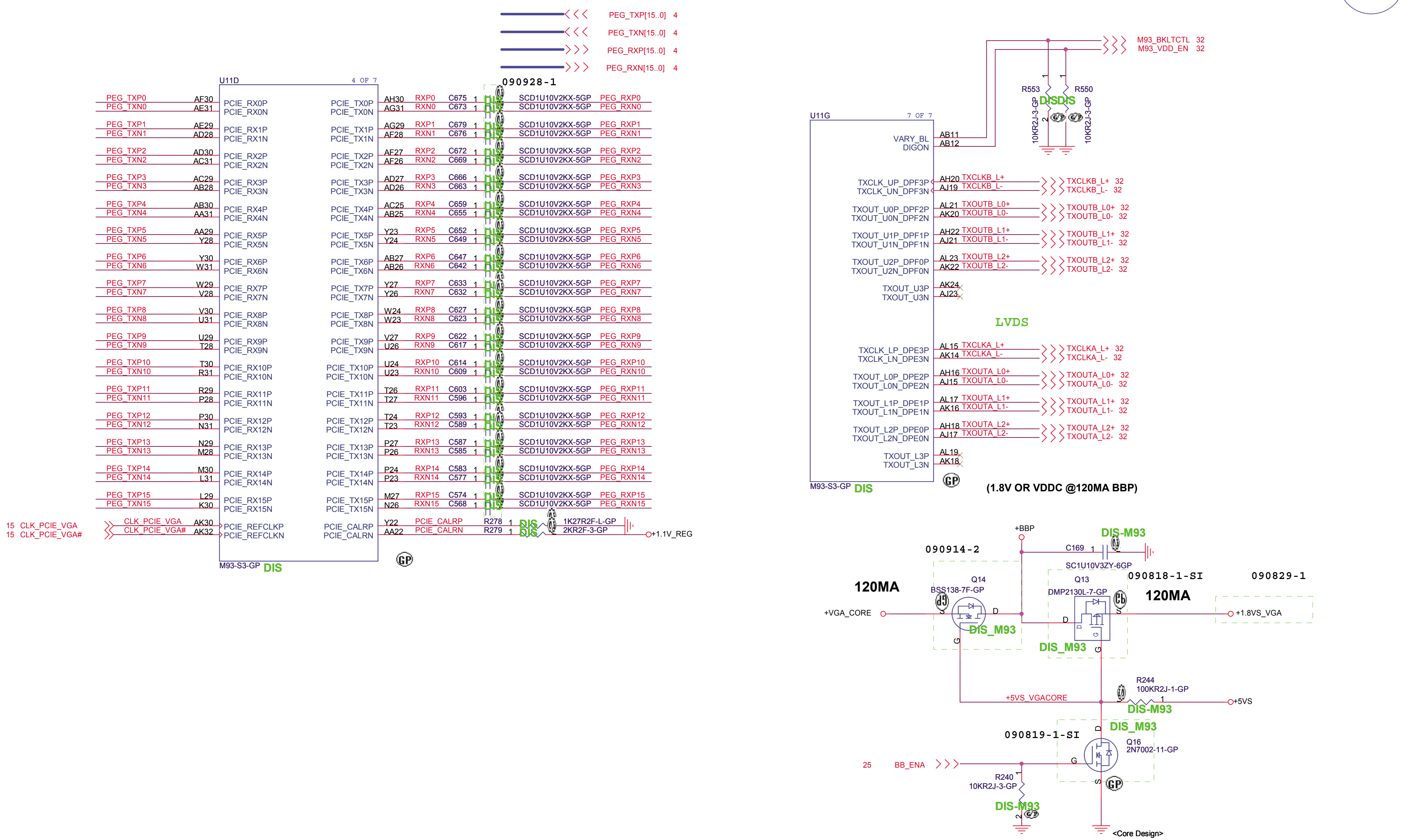
Title	Clock Generator ICS9LRS3197	
Size A3	Document Number: S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 23 of 62	

M93 GPU(1/5)



<Core Design>

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Title	VGA-PCIE/LVDS(1/5)
Size	A3
Document Number	S-Class Intel
Rev	SD
Date	Wednesday, October 28, 2009
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M93 GPU(2/5)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD BIF_VGA DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM ID CFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 XX

Aperture Conig. PIN	M93S3 GPIO	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG0	GPIO_11	R243	0	0	1
CONFIG1	GPIO_12	R246	1	0	0
CONFIG2	GPIO_13	R250	0	0	0

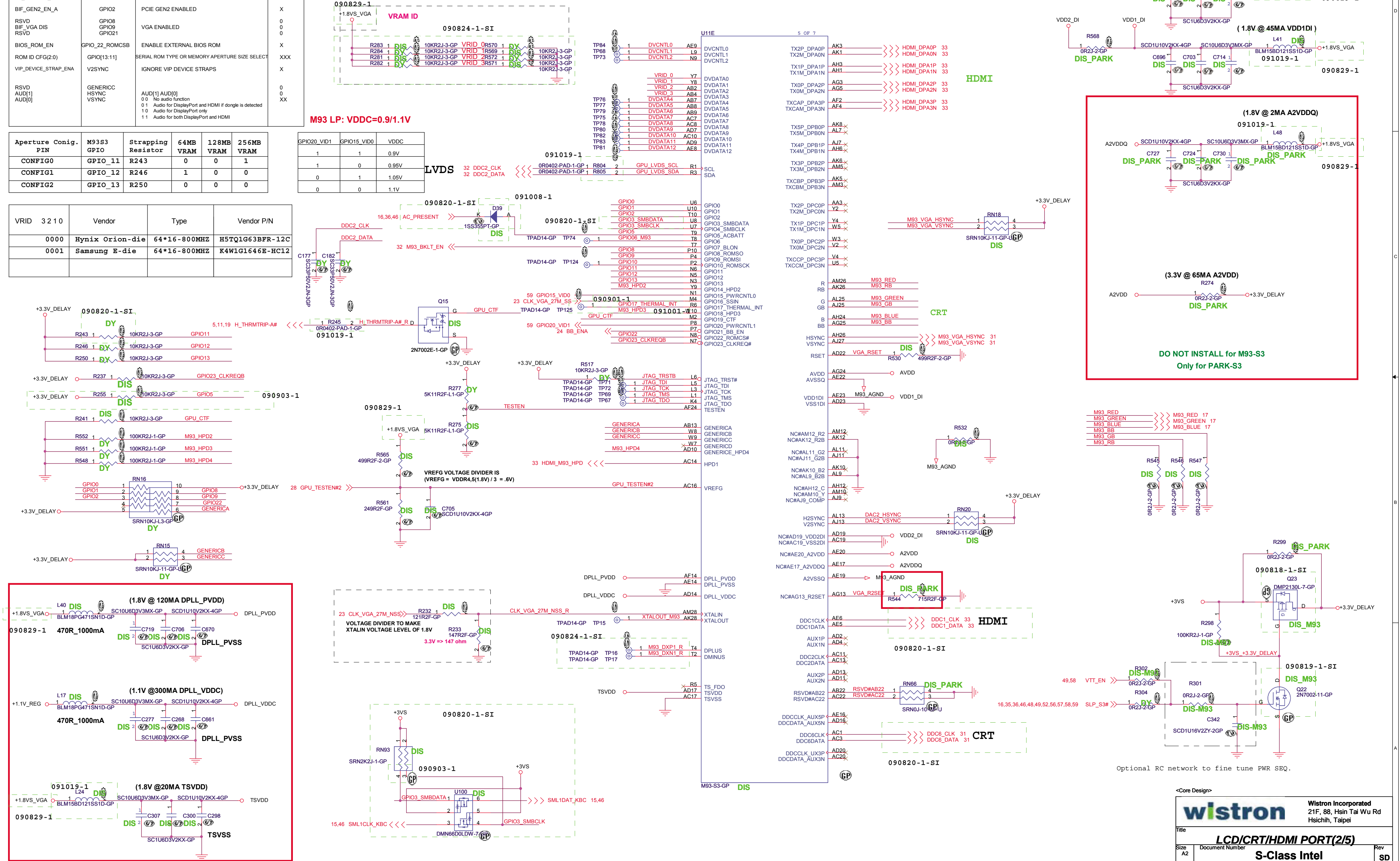
GPIO20_VID1	GPIO15_VID0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

VRID 3210	Vendor	Type	Vendor P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12

090824-1-SI

VRAM ID:
BIT0 --> L:Quanta ; H:Wistron
BIT1 --> L:512M ; H:1GB
BIT2 --> L:Samsung ; H:Hynix
BIT3 -->N/A

M93 LP: VDDC=0.9/1.1V



<Core Design>

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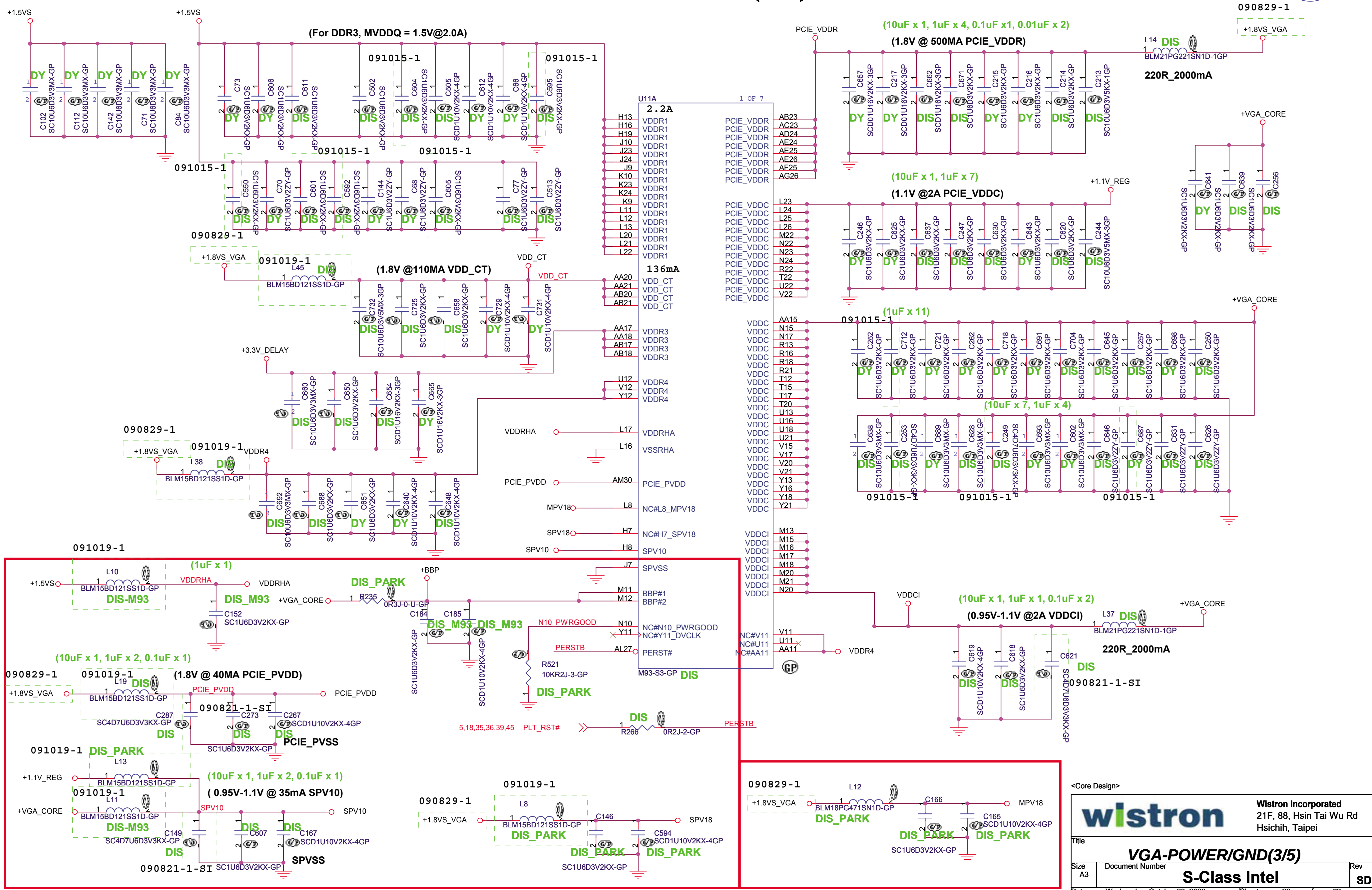
Title: LCD/CRT/HDMI PORT(2/5)

Size: A2 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 25 of 62

M93 GPU(3/5)



<Core Design>

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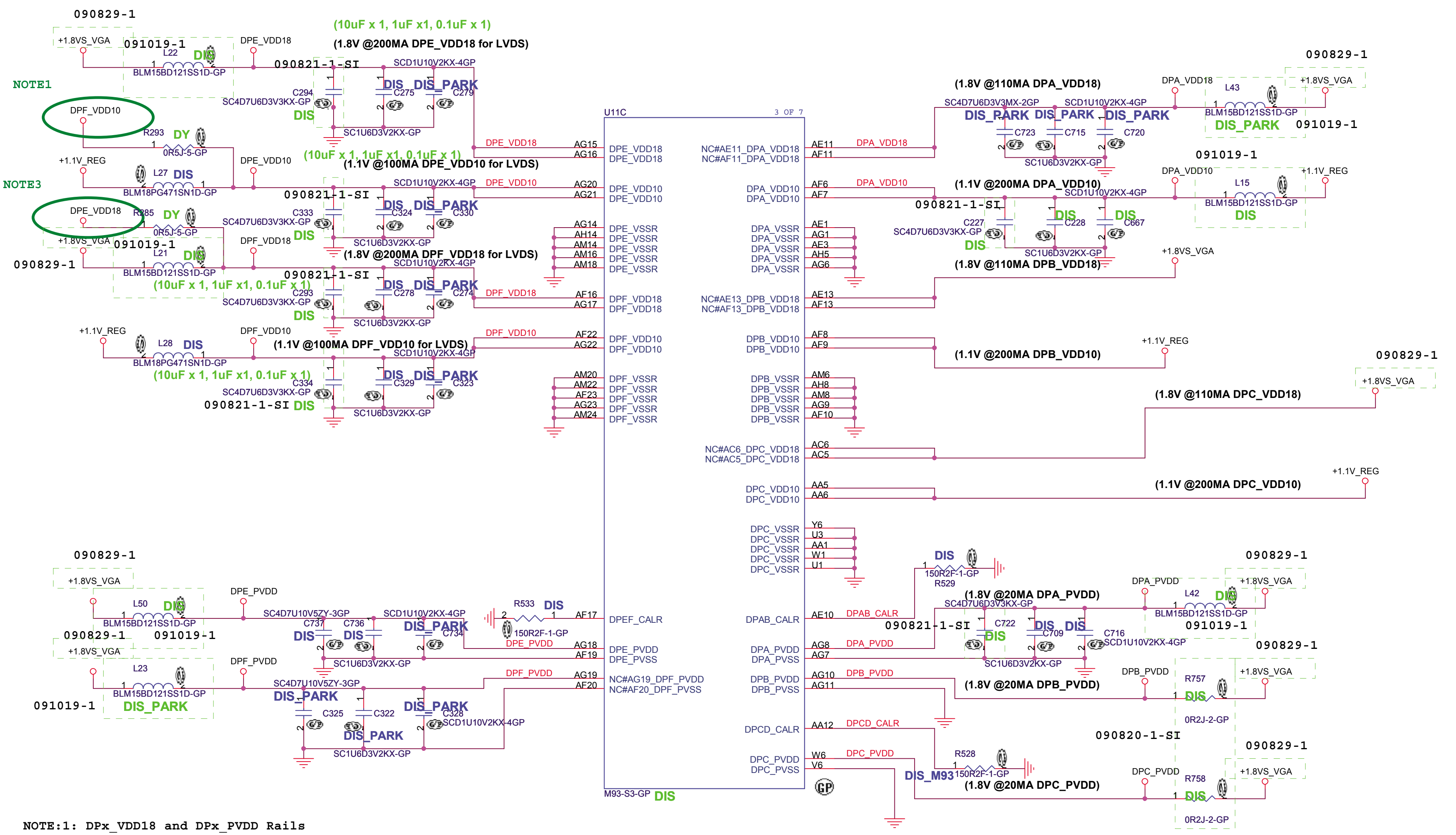
Hsichih, Taipei

Title	VGA-POWER/GND(3/5)	
Size A3	Document Number: S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 26 of 62	

M93 GPU(4/5)



NOTE:1: DPx_VDD18 and DPx_PVDD Rails
can be join together and remove Decoupling
Capacitors and BEAD for DPx_PVDD if
signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 /
DPF_VDD10 Rails can be join together and remove
Decoupling Capacitors and BEADfor one rail of each pair
if signal integrity for DP lanes are OK.
We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown
in schematic for Dual -Link DVI or LVDS setting and
remove DecouplingCapacitors and BEAD of any one rail
of the pair if signal integrity for DP lanes are OK.
We need at least 500mA Bead to supportjoin rails.

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Title	VGA-POWER/GND(4/5)
Size A3	Document Number: S-Class Intel
Rev	SD
Date:	Wednesday, October 28, 2009
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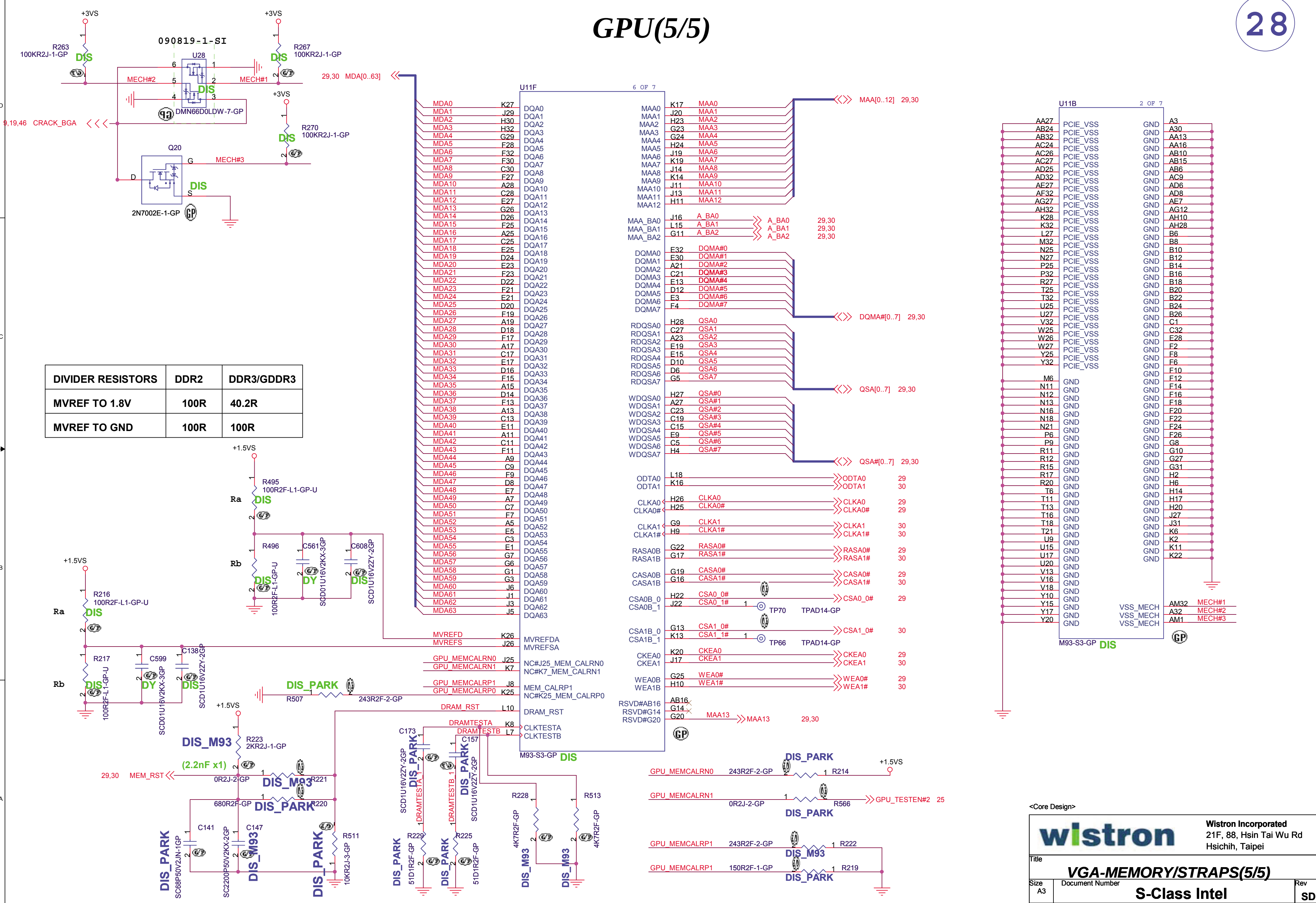
GPU(5/5)



DIVIDER RESISTORS	DDR2	DDR3/GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

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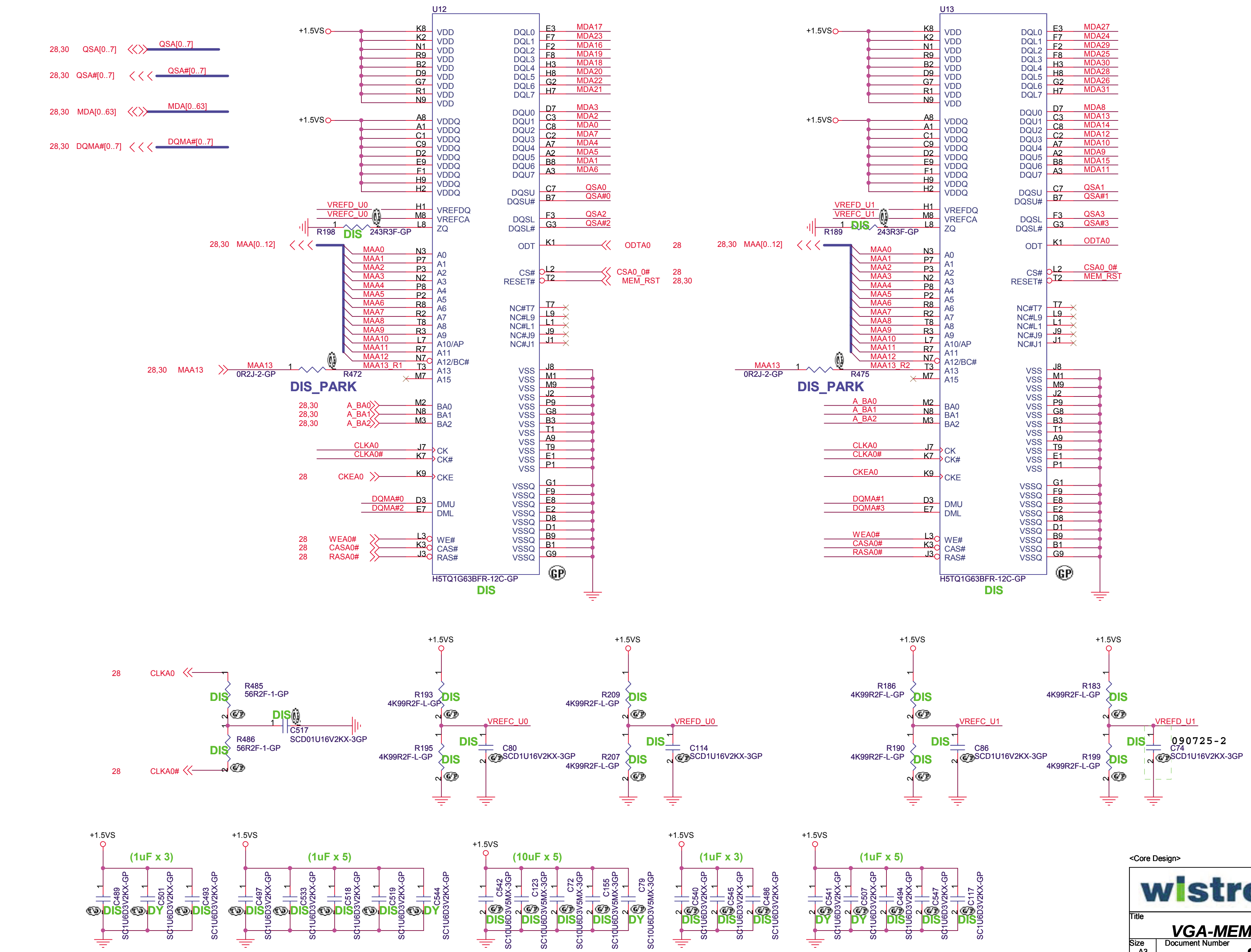
Title: VGA-MEMORY/STRAPS(5/5)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 28 of 62

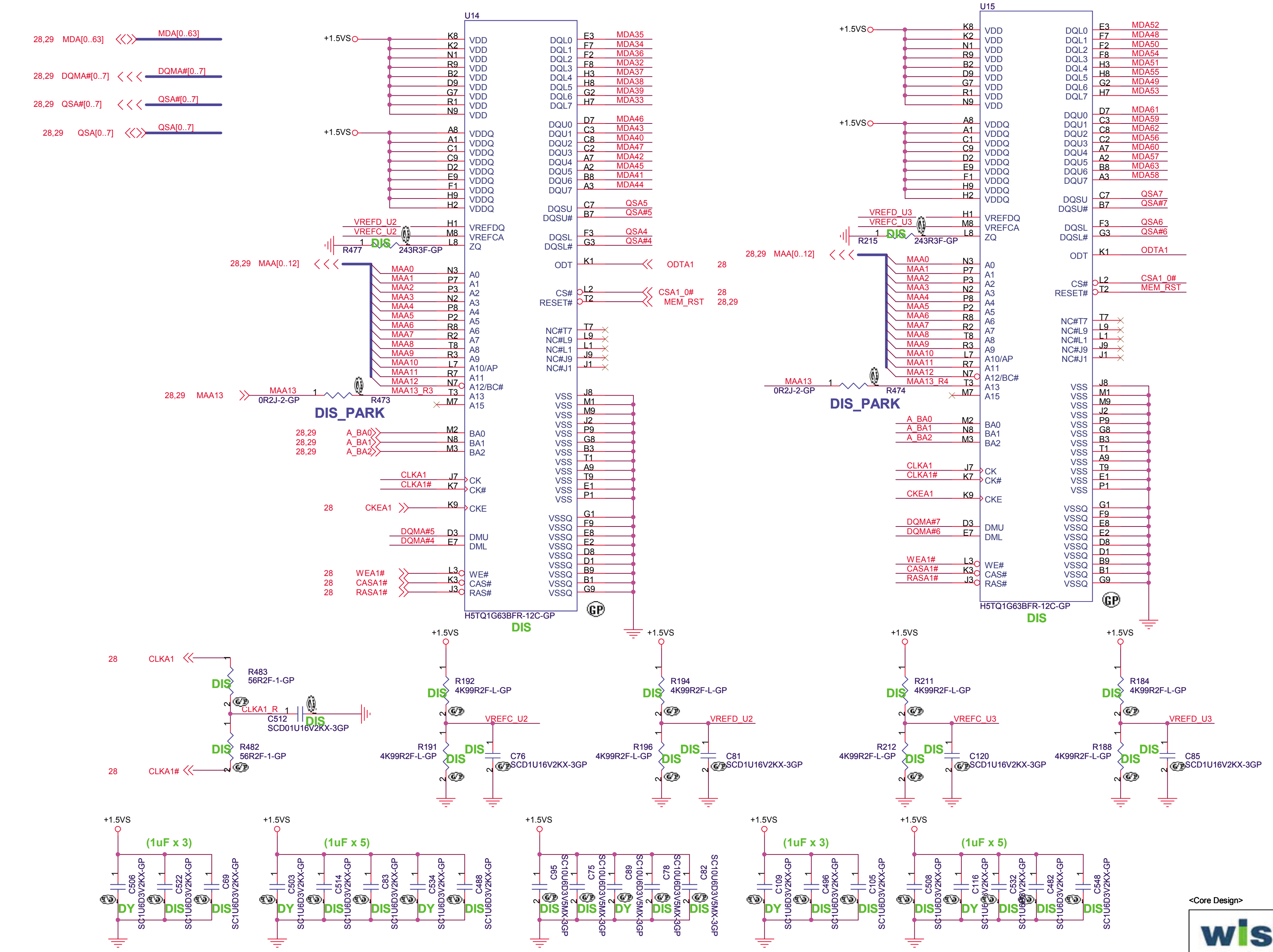
VRAM DDR3 (1/2)

256MB/512MB DDR3



VRAM DDR3 (2/2)

256MB/512MB DDR3



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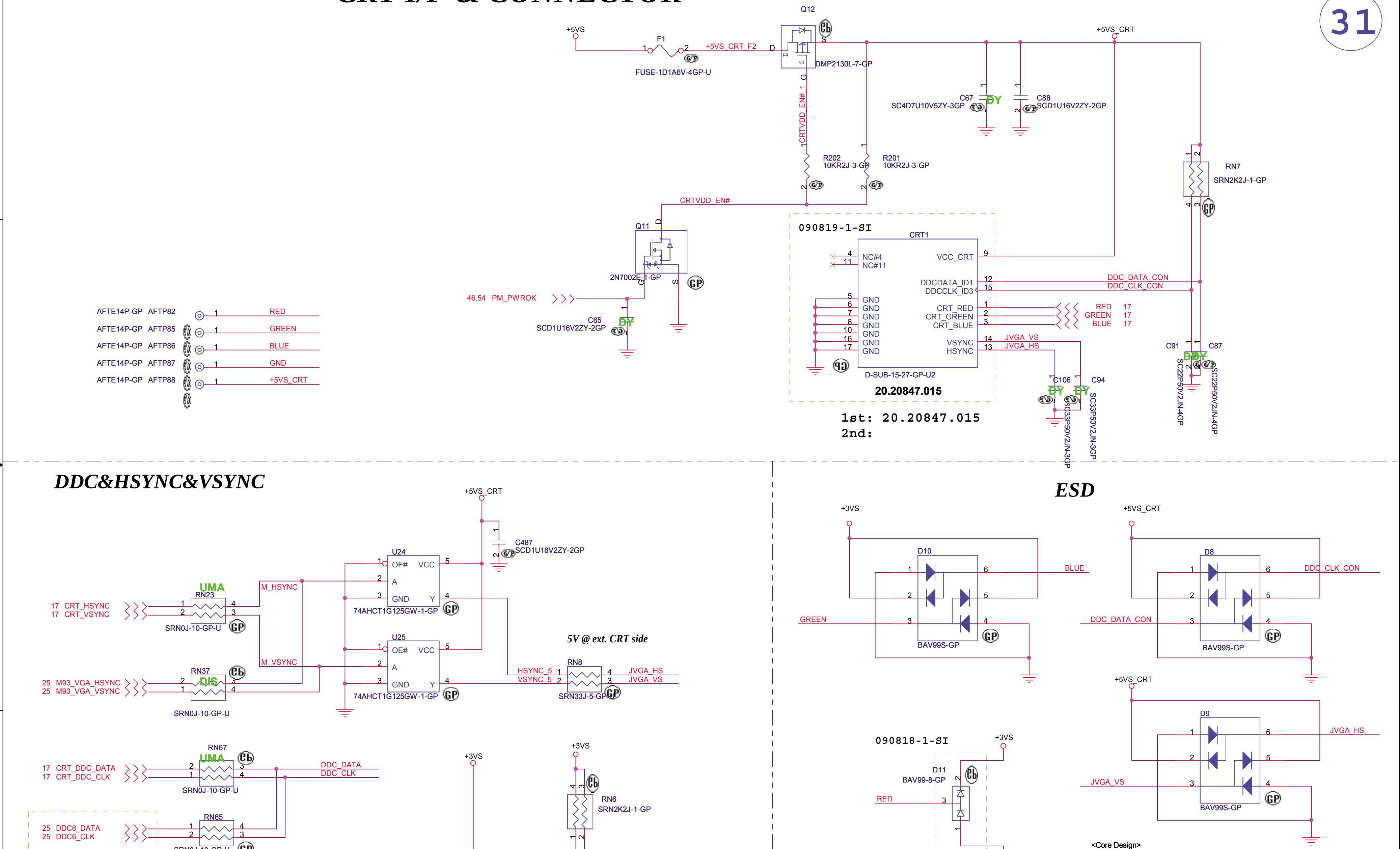
Title: VGA-MEMORY/STRAPS(4/4)

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 30 of 62

CRT I/F & CONNECTOR



<Core Design>

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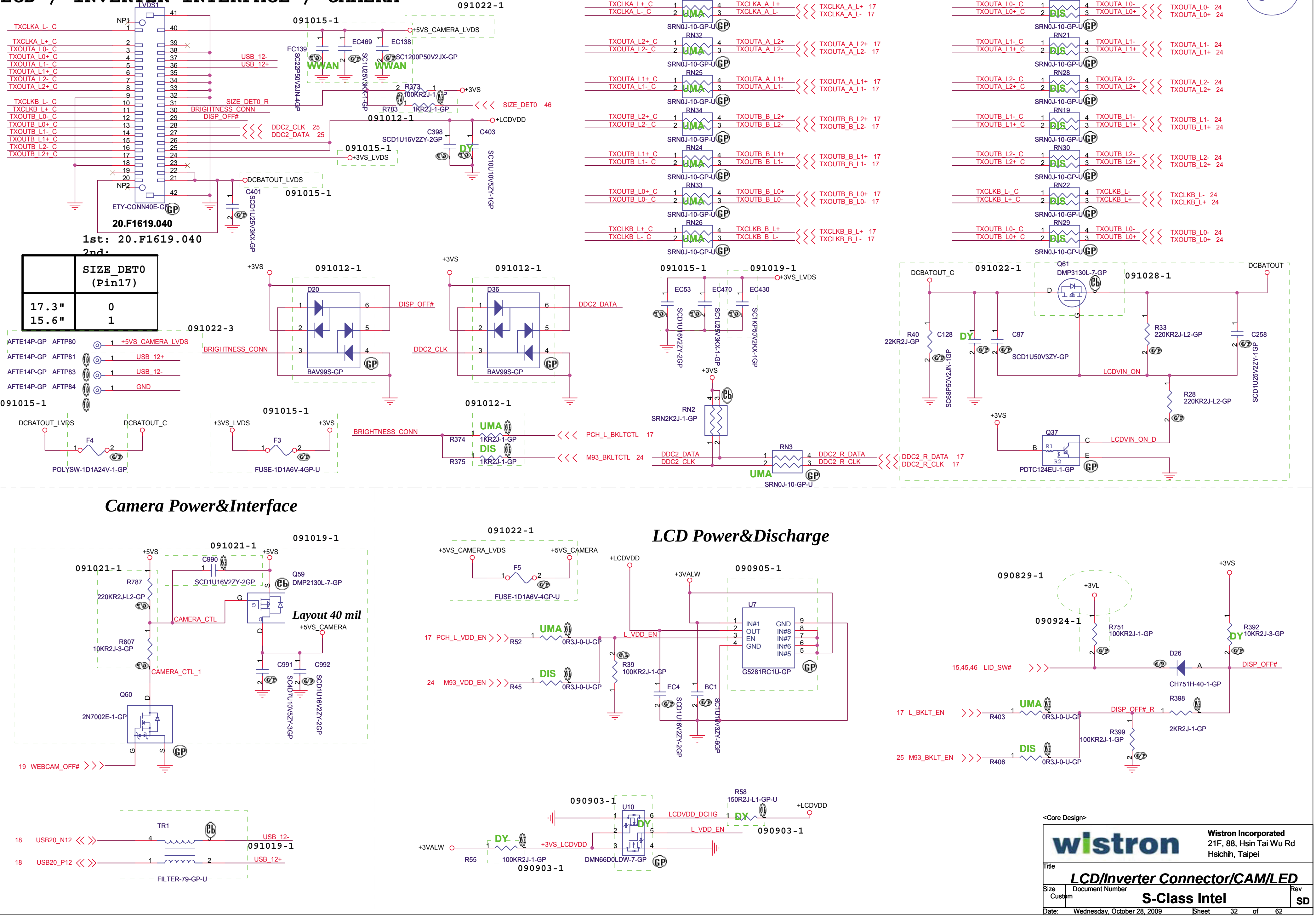
Title	CRT Connector	
Size A3	Document Number: S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 31 of 62	

LVDS CONNECTOR

LCD / INVERTER INTERFACE / CAMERA



	SIZE_DET0 (Pin17)
17.3"	0
15.6"	1

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Title: LCD/Inverter Connector/CAM/LED

Size: Custom | Document Number: S-Class Intel | Rev: SD

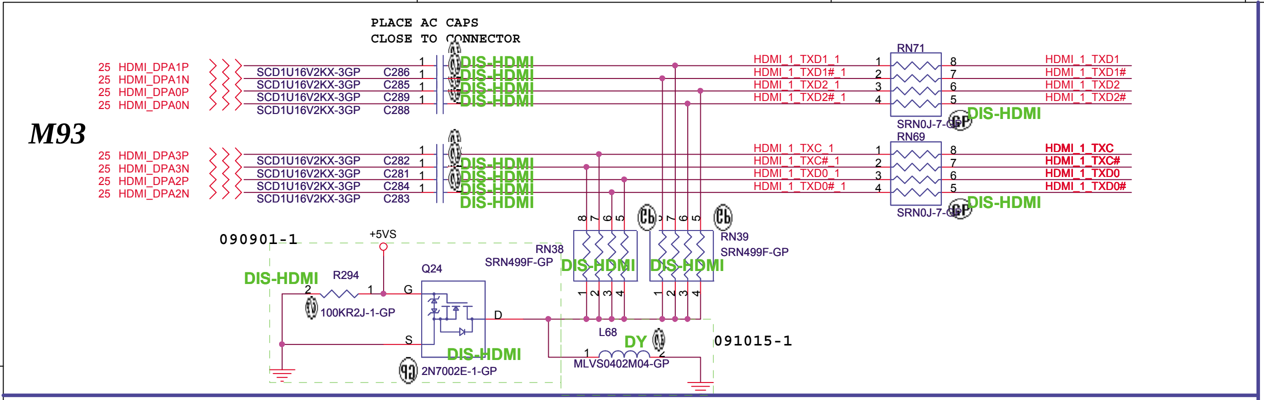
Date: Wednesday, October 28, 2009 | Sheet 32 of 62

HDMI CONNECTOR

33

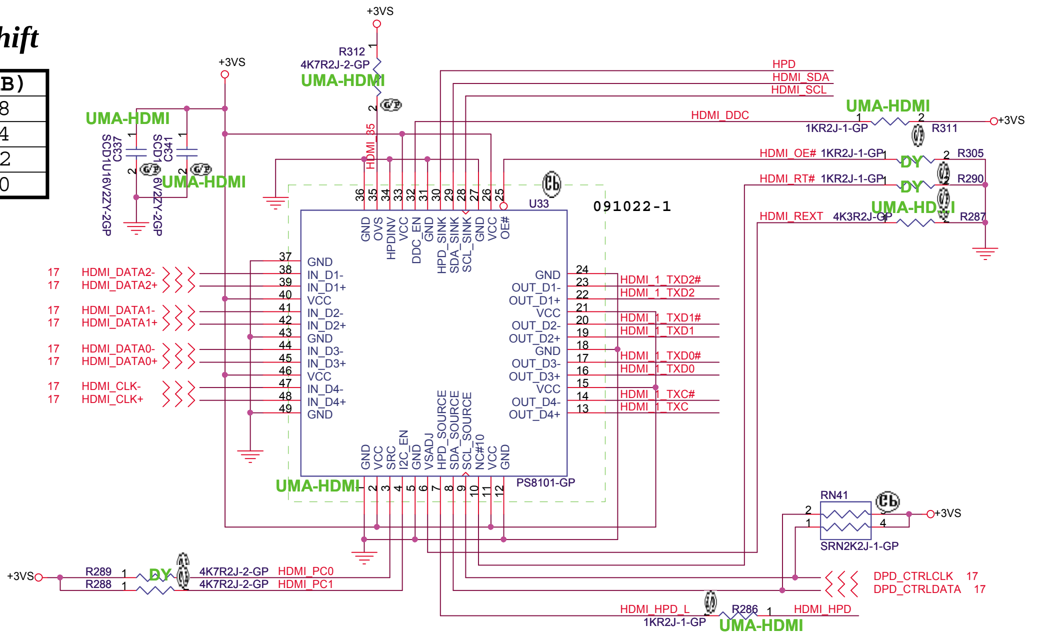
M93

PLACE AC CAPS
CLOSE TO CONNECTOR

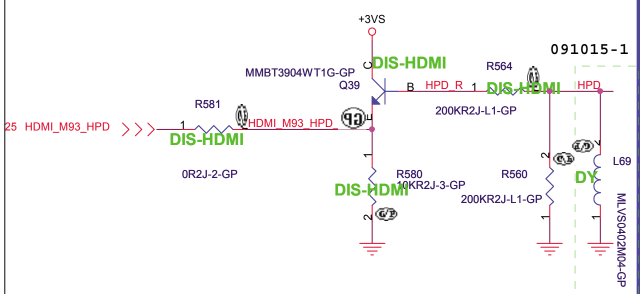


PCH Level Shift

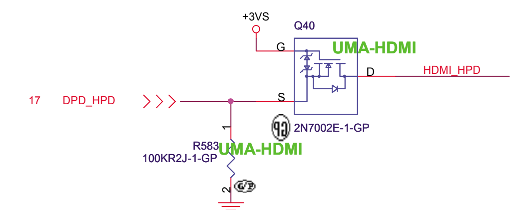
PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0

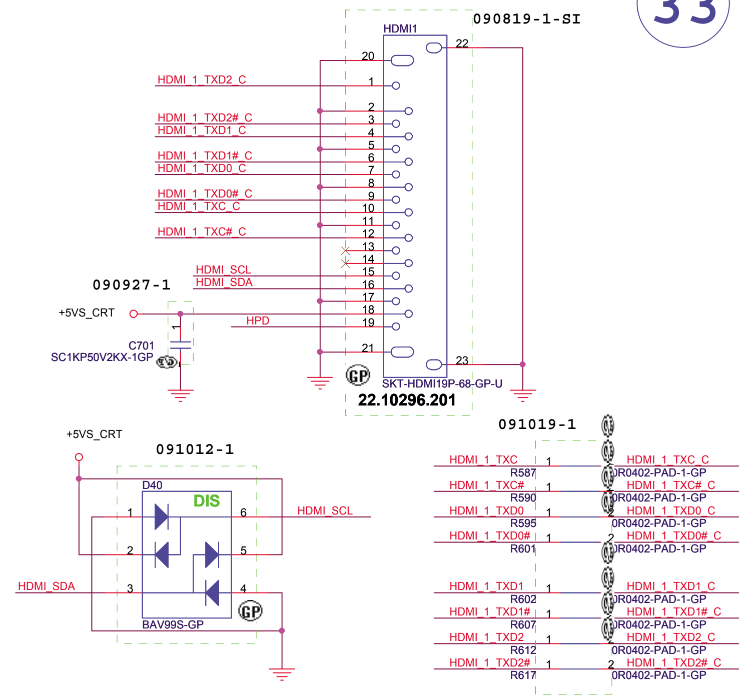


DIS HPD

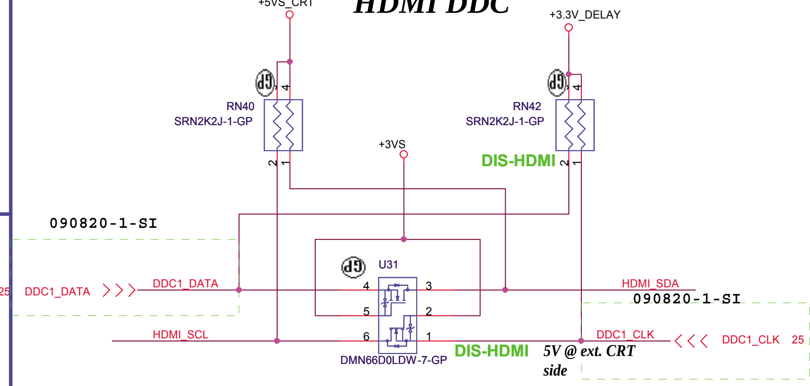


UMA HPD





HDMI DDC



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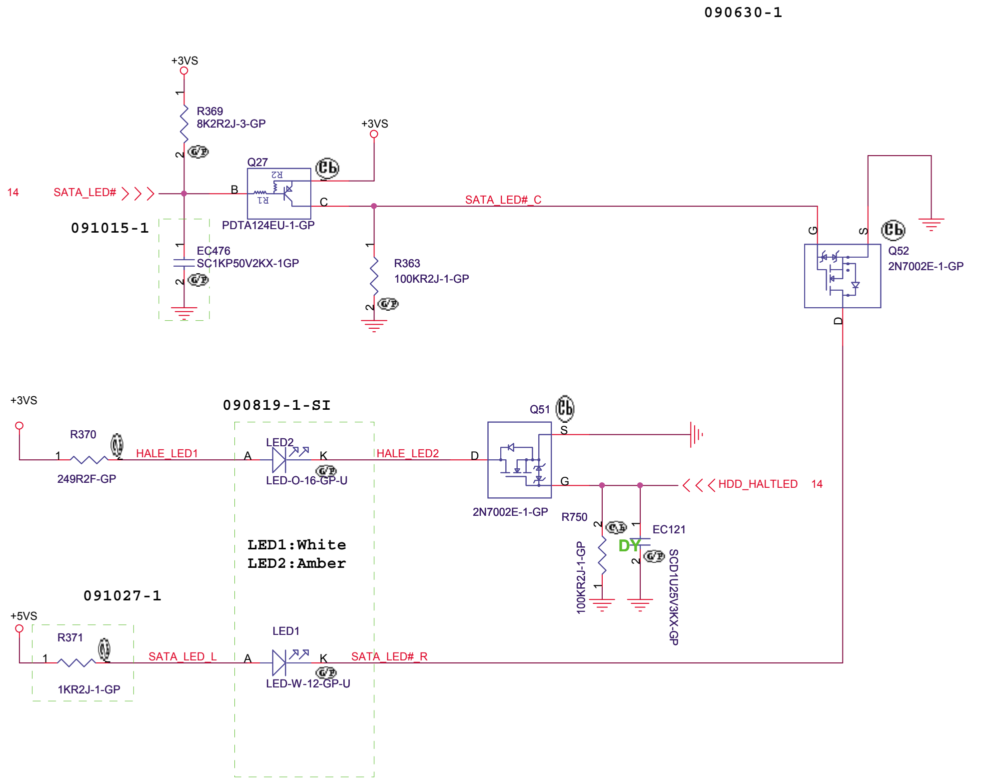
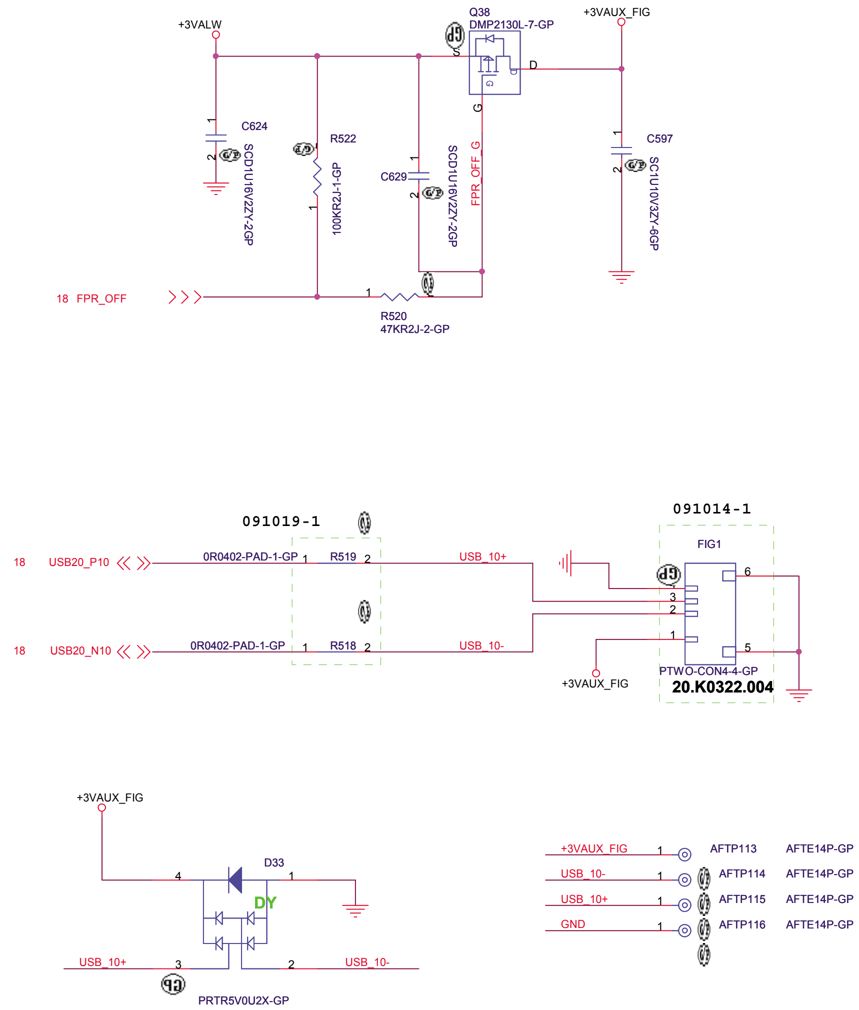
Title	HDMI CONN.		
Size A3	Document Number S-Class Intel		Rev SD
Date: Wednesday, October 28, 2009	Sheet 33 of 62		

SATA LED FOR HDD



Fingerprint



<Core Design>

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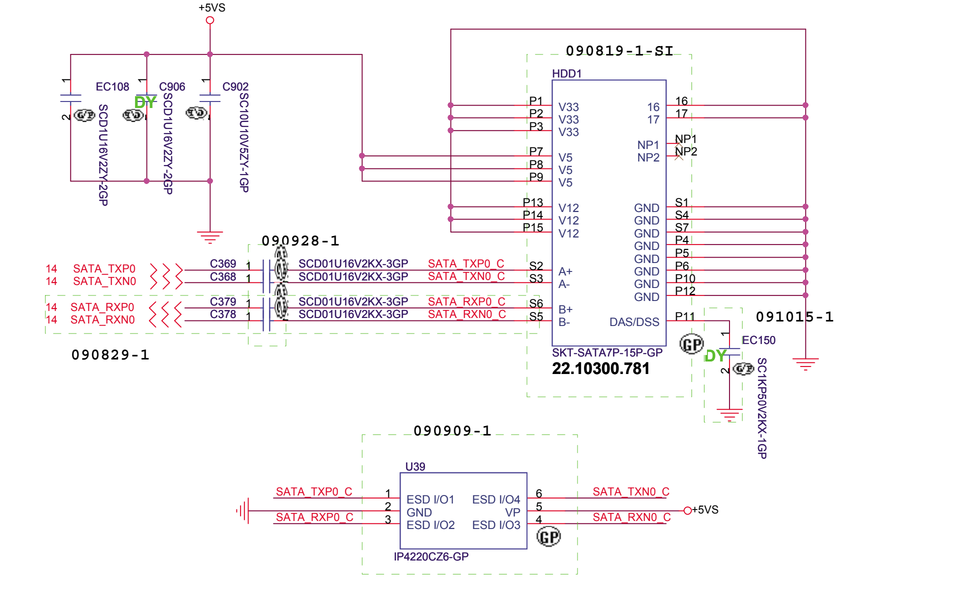
Title: **SATA&CAP LED&GOLDEN FINGER**

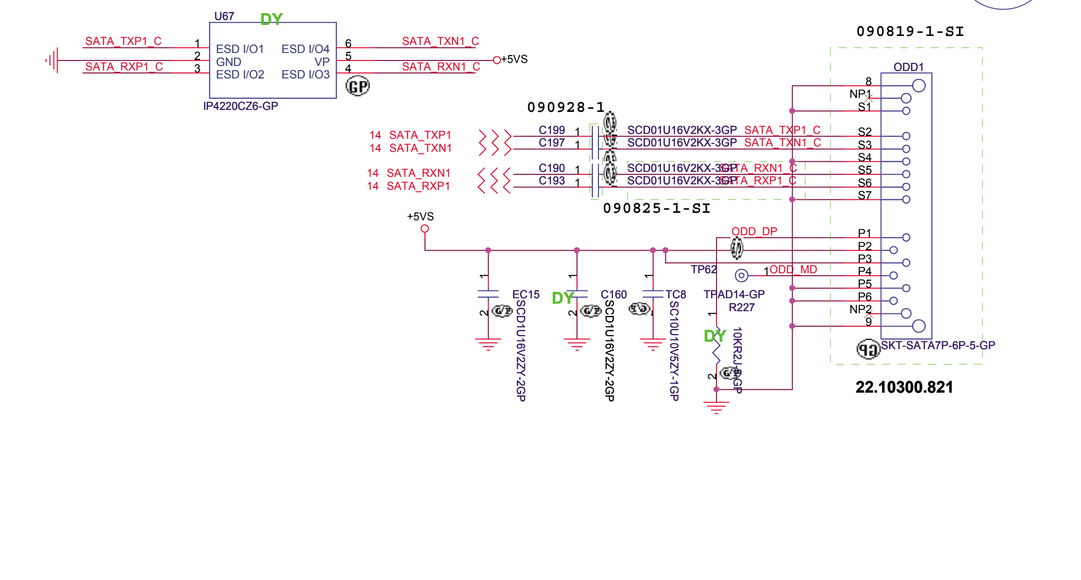
Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 | Sheet 34 of 62

SATA HD Connector

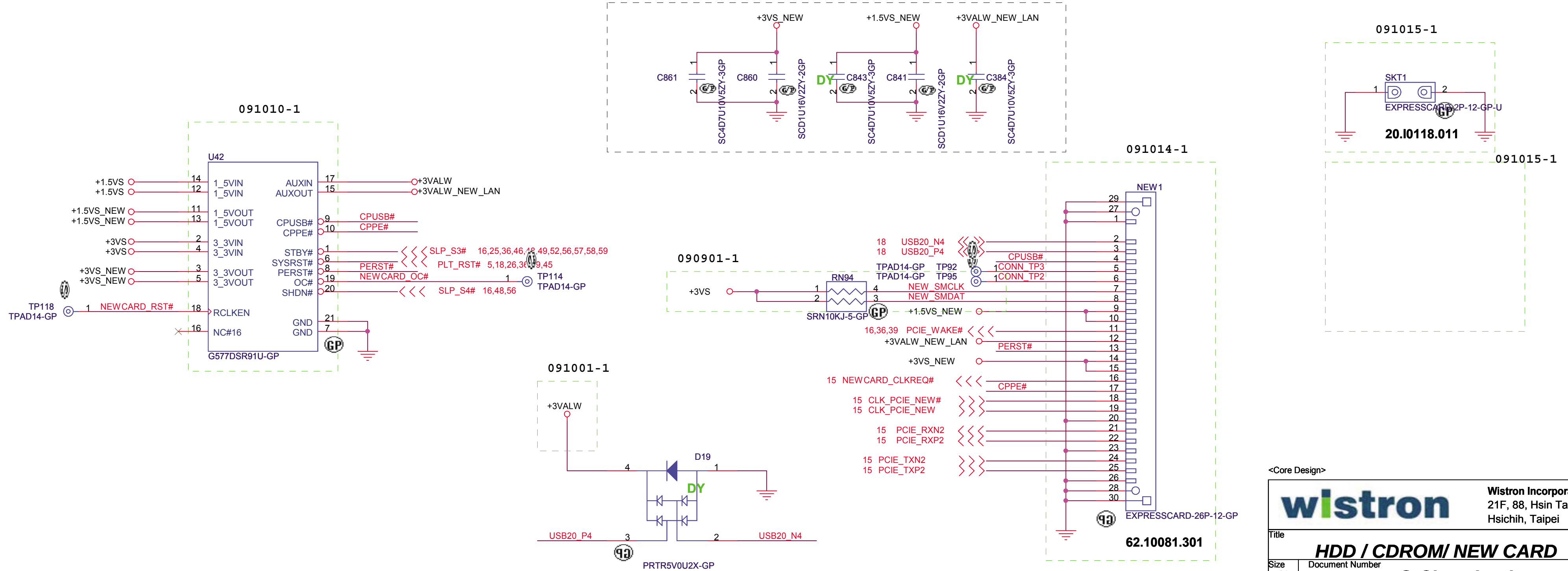


ODD Connector

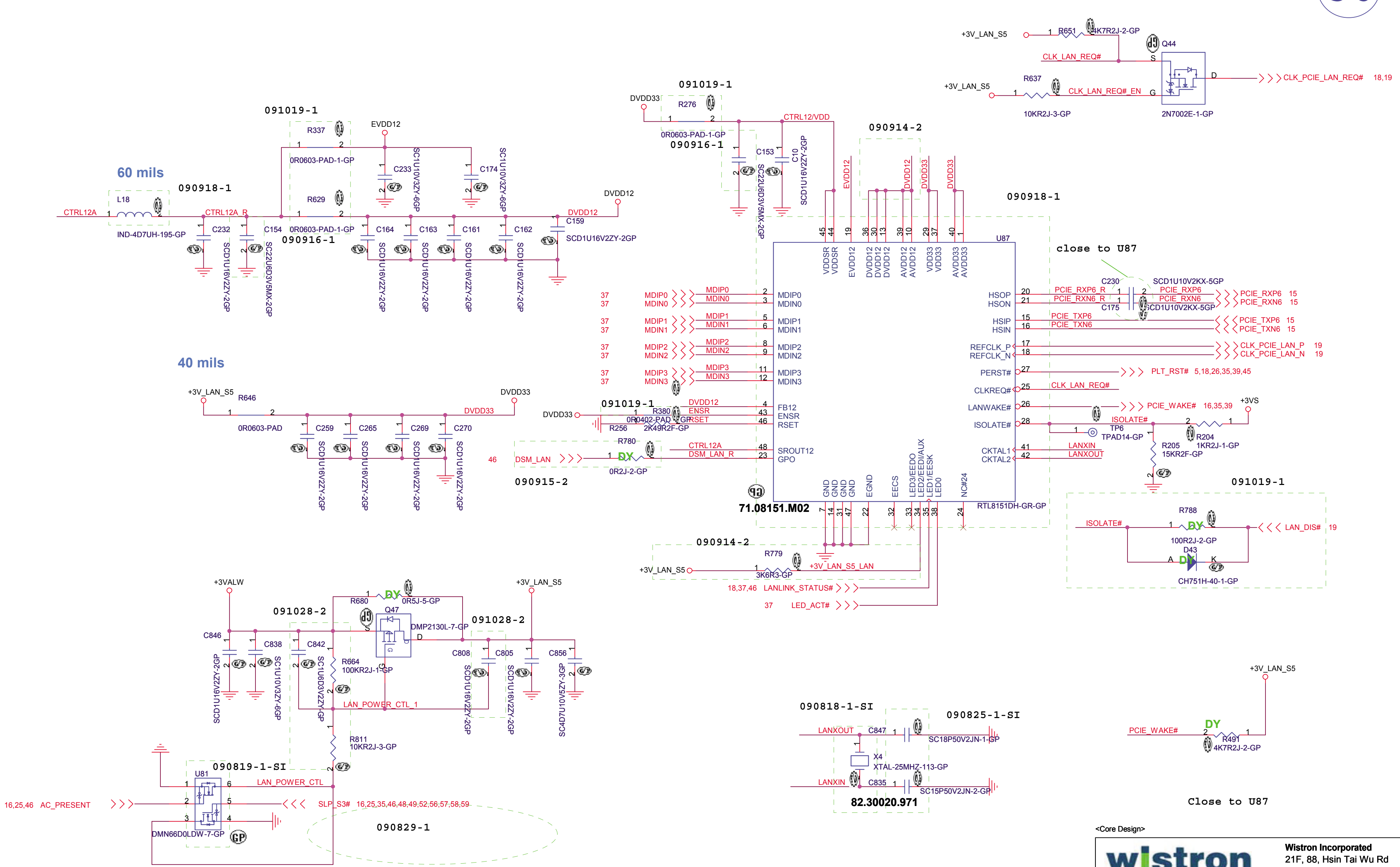


EXPRESS CARD Connector

Place them Near to Connector



LAN CHIP



<Core Design>

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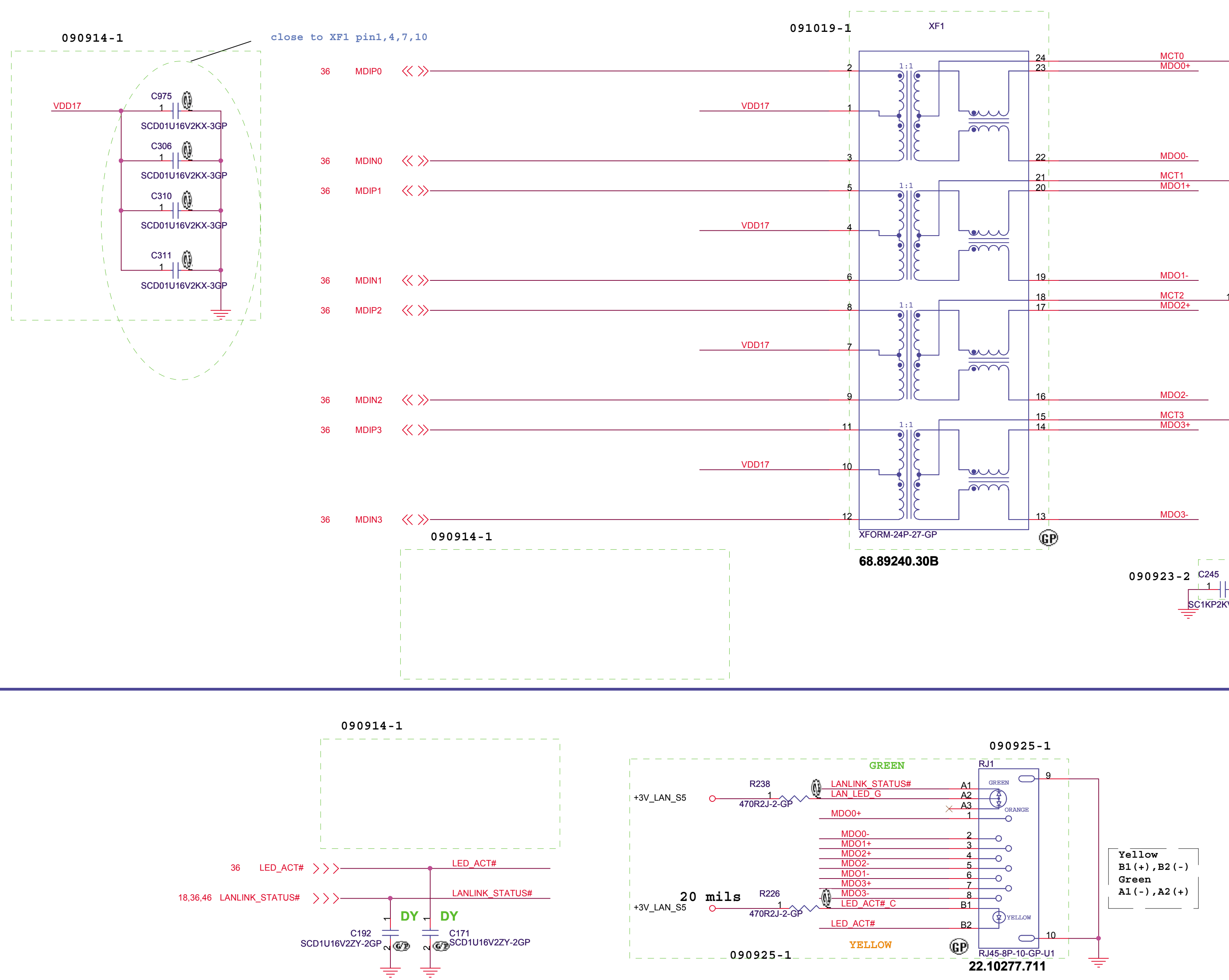
Title: LAN_REALTEK_RTL8151DH

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 36 of 62



IF NOT OVER CLOCKING, LED_ACT# WILL ACT HIGH

Check LAN chip for LED_ACT# function on RJ45 connector pin define.

<Core Design>

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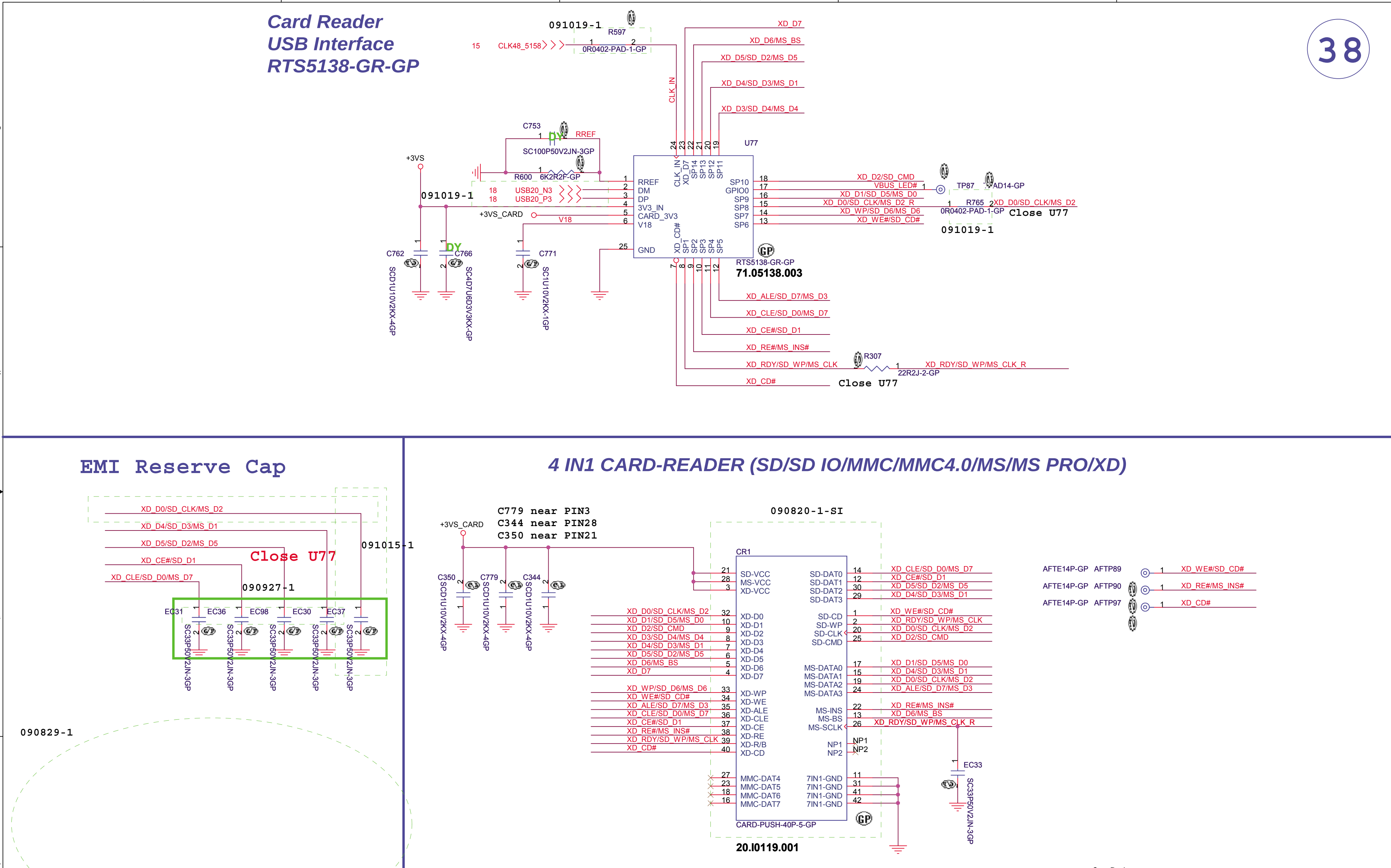
Title: **Magnetic & RJ45**

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 — Sheet 37 of 62



<Core Design>

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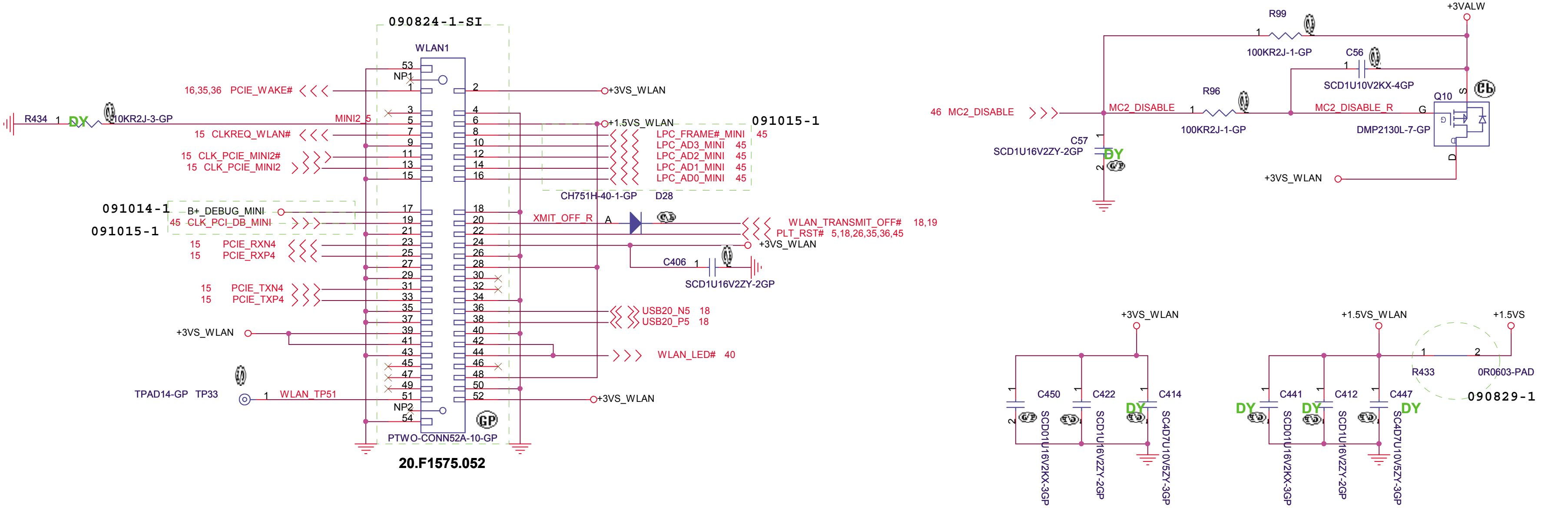
Title: CardReader RTS5138

Size: A3 | Document Number: S-Class Intel | Rev: SD

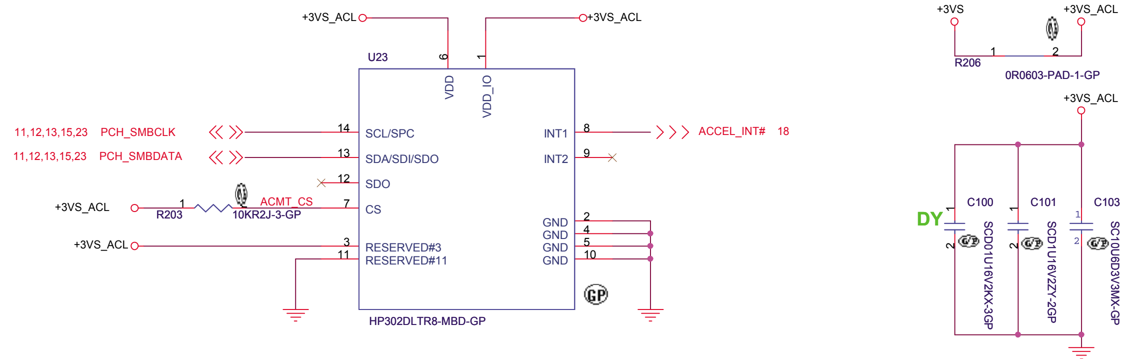
Date: Wednesday, October 28, 2009 | Sheet 38 of 62

Mini-Card--WLAN

Half minicard



ACCELEROMETER



<Core Design>

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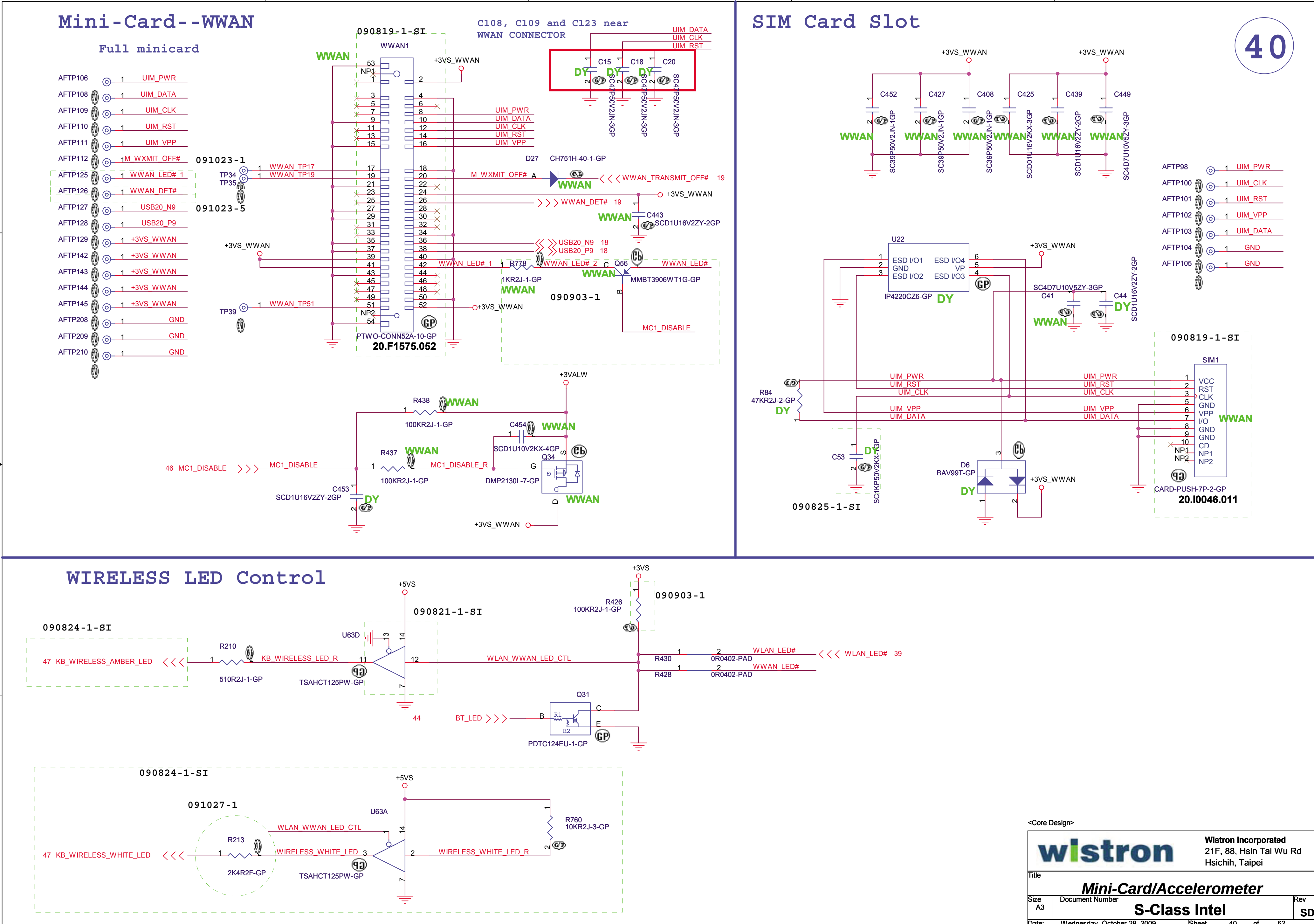
Title	Mini-Card/Accelerometer		
Size A3	Document Number	S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 39 of 62		



<Core Design>

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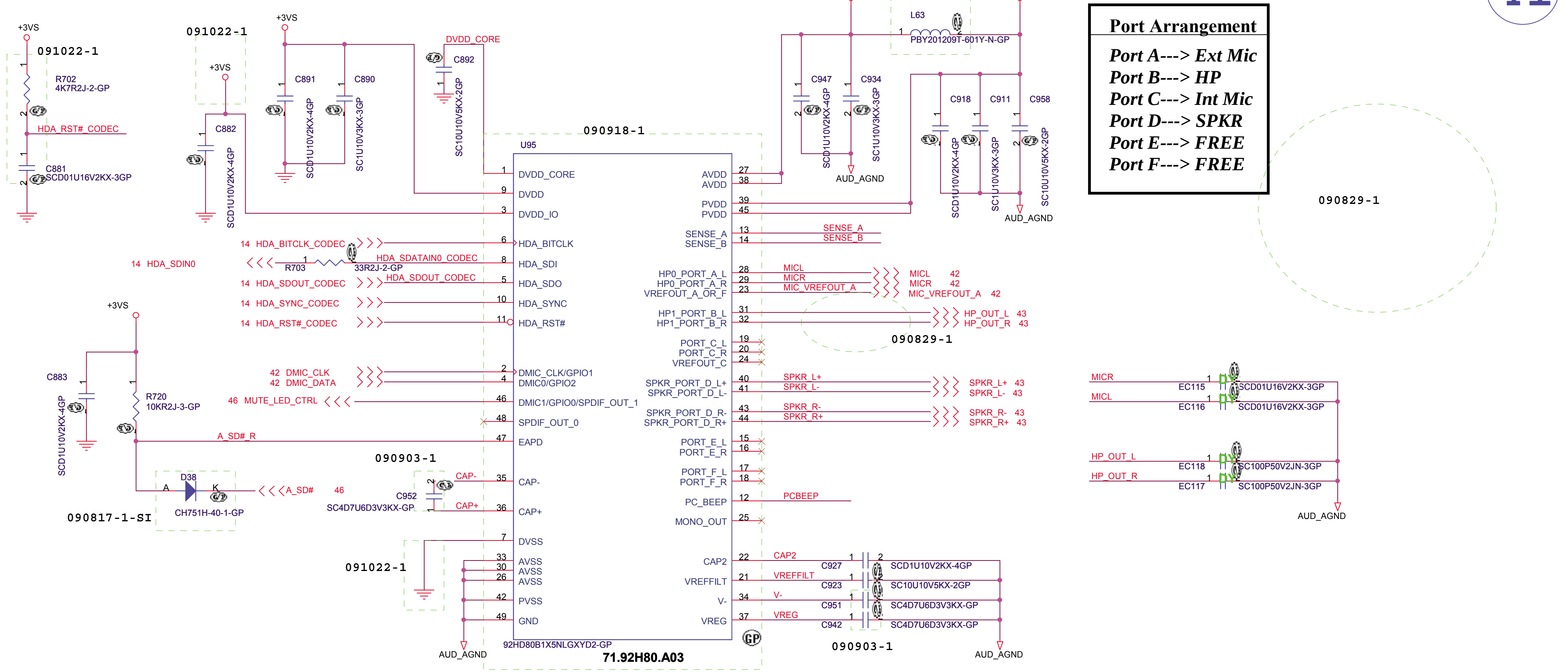
Title: Mini-Card/Accelerometer

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 | Sheet 40 of 62

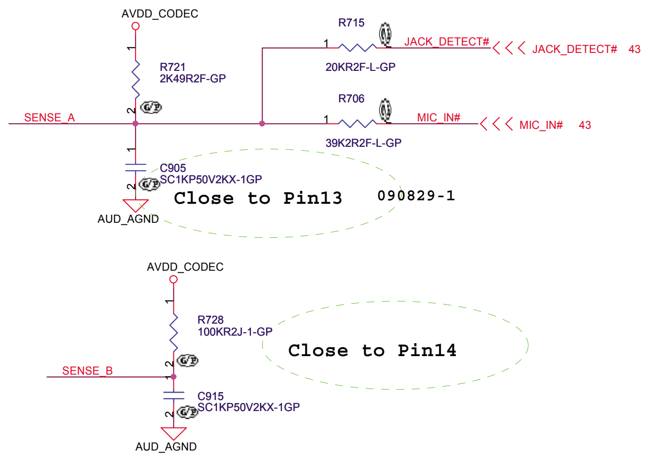
AUDIO CODEC(92HD80)



Port Arrangement

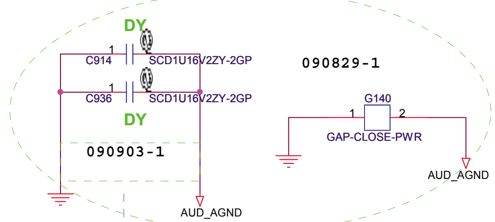
Port A---> Ext Mic
Port B---> HP
Port C---> Int Mic
Port D---> SPKR
Port E---> FREE
Port F---> FREE

SENSE Detect



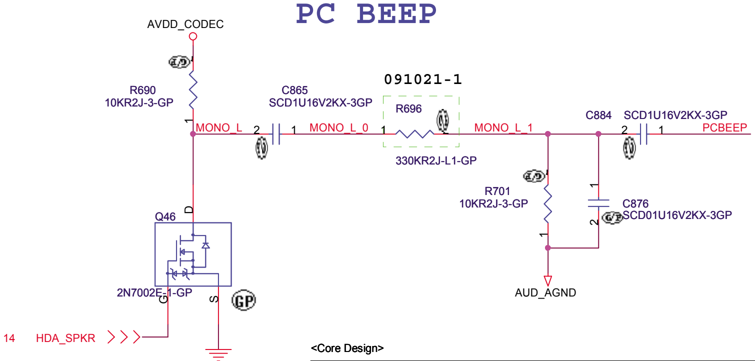
Digital GND & AUD_AGND

Place close to Codec chip



audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



<Core Design>

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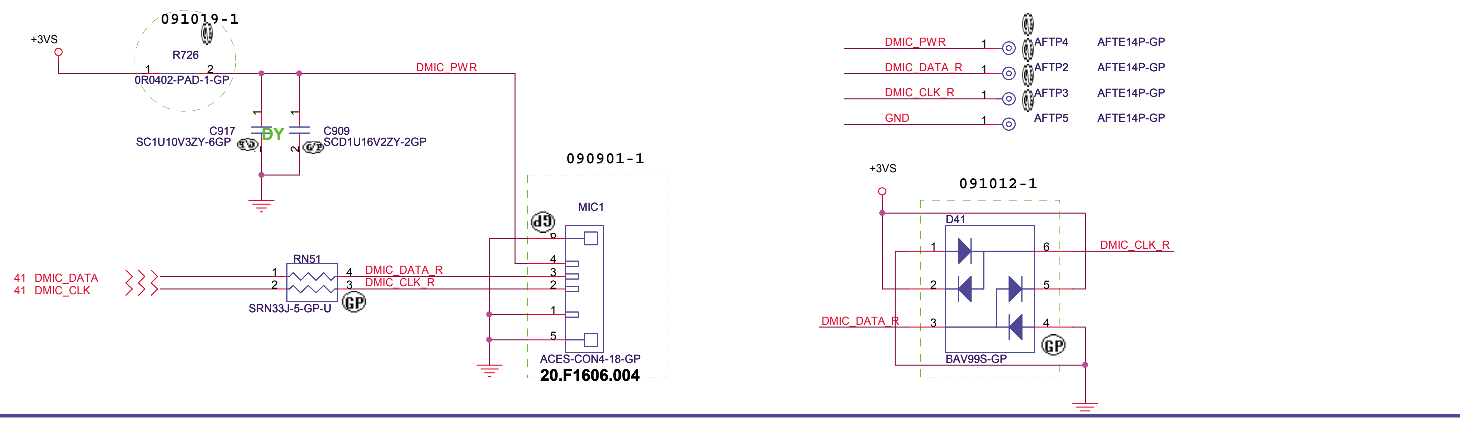
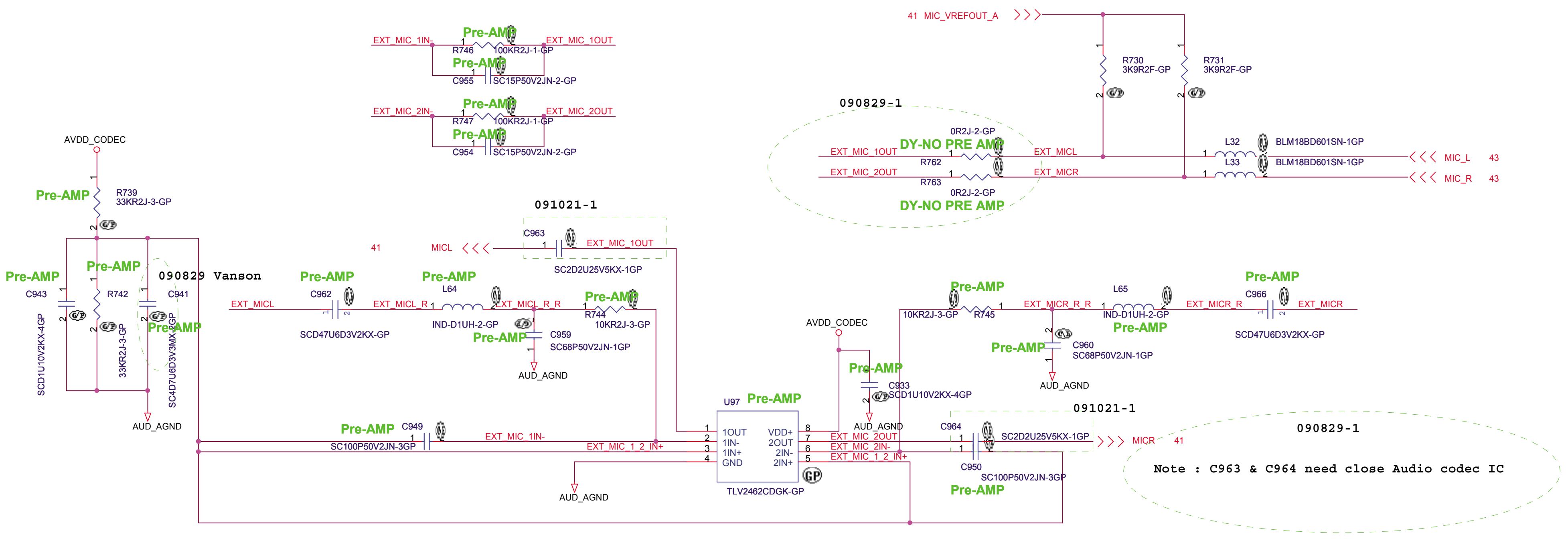
Title	AUDIO 92HD80 / OP AMP	
Size A3	Document Number: S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 41 of 62	

Internal Digital MIC



Ppre-AMP. for External MIC



<Core Design>

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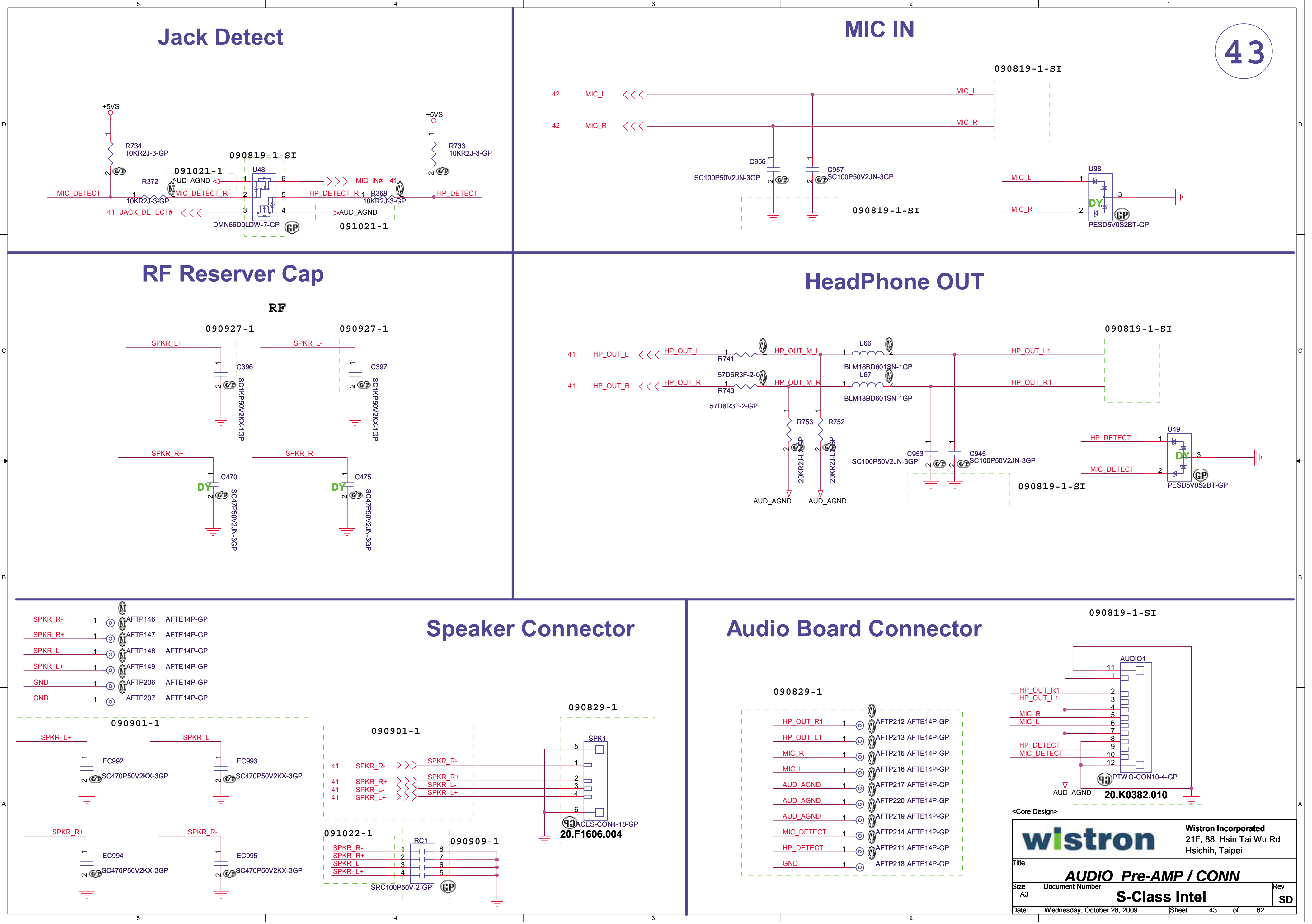
Title	AUDIO Pre-AMP / CONN
Size A3	Document Number: S-Class Intel — Rev SD
Date: Wednesday, October 28, 2009	Sheet 42 of 62



43
Jack Detect
MIC IN
RF Reserver Cap
HeadPhone OUT
Speaker Connector
Audio Board Connector
RF
+5VS
R734
10KR2J-3-GP
R733
10KR2J-3-GP
R372
10KR2J-3-GP
R368
10KR2J-3-GP
U48
DMN66D0LDW-7-GP
MIC_DETECT
MIC_DETECT_R
HP_DETECT_R
HP_DETECT
MIC_IN#
JACK_DETECT#
AUD_AGND
090819-1-SI
091021-1
MIC_L
MIC_R
C956
C957
SC100P50V2JN-3GP
U98
PESD5V0S2BT-GP
DY
SPKR_L+
SPKR_L-
SPKR_R+
SPKR_R-
090927-1
C396
C397
SC1KP50V2KX-1GP
C470
C475
SC47P50V2JN-3GP
HP_OUT_L
HP_OUT_R
HP_OUT_M_L
HP_OUT_M_R
HP_OUT_L1
HP_OUT_R1
R741
R743
57D6R3F-2-GP
L66
L67
BLM18BD601SN-1GP
R753
R752
20KR2J-L-GP
C953
C945
U49
AFTP146
AFTP147
AFTP148
AFTP149
AFTP206
AFTP207
AFTE14P-GP
GND
090901-1
EC992
EC993
EC994
EC995
SC470P50V2KX-3GP
090829-1
SPK1
ACES-CON4-18-GP
20.F1606.004
091022-1
RC1
SRC100P50V-2-GP
090909-1
AFTP212
AFTP213
AFTP215
AFTP216
AFTP217
AFTP220
AFTP219
AFTP214
AFTP211
AFTP218
AUDIO1
PTWO-CON10-4-GP
20.K0382.010
<Core Design>
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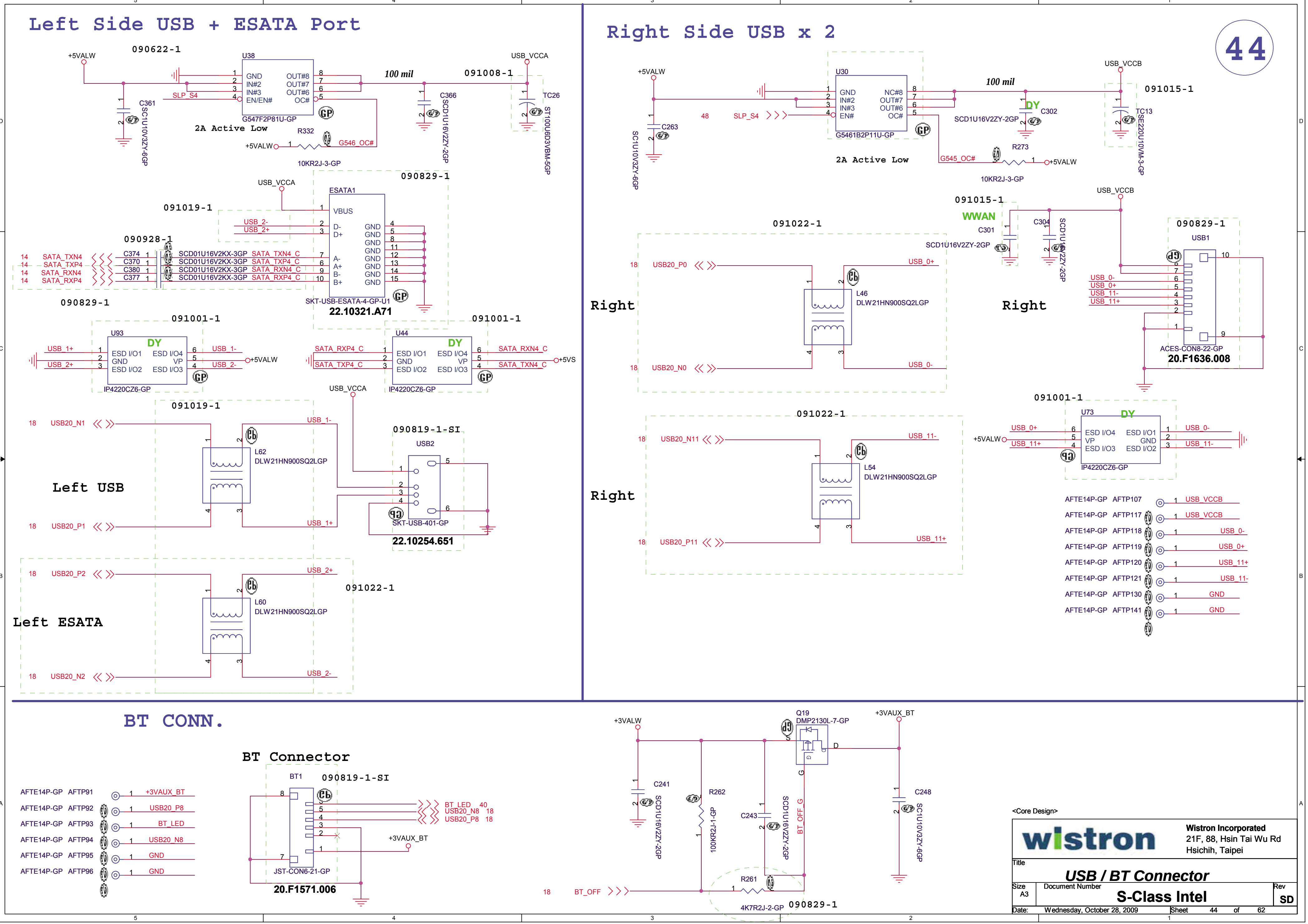
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
AUDIO Pre-AMP / CONN
Size A3
Document Number
S-Class Intel
Rev SD
Date: Wednesday, October 28, 2009
Sheet 43 of 62



Left Side USB + ESATA Port
090622-1
+5VALW
U38
GND
IN#2
IN#3
EN/EN#
OUT#8
OUT#7
OUT#6
OC#
G547F2P81U-GP
2A Active Low
SLP_S4
C361
SC1U10V3ZY-6GP
100 mil
091008-1
USB_VCCA
C366
SCD1U16V2ZY-2GP
TC26
ST100U6D3VBM-5GP
R332
10KR2J-3-GP
G546_OC#
090829-1
ESATA1
VBUS
D-
D+
A-
A+
B-
B+
GND
SKT-USB-ESATA-4-GP-U1
22.10321.A71
091019-1
USB_2-
USB_2+
090928-1
SATA_TXN4
SATA_TXP4
SATA_RXN4
SATA_RXP4
C374
C370
C380
C377
SCD01U16V2KX-3GP
SATA_TXN4_C
SATA_TXP4_C
SATA_RXN4_C
SATA_RXP4_C
091001-1
U93
DY
ESD I/O1
GND
ESD I/O2
ESD I/O4
VP
ESD I/O3
USB_1+
USB_1-
IP4220CZ6-GP
U44
+5VS
USB_VCCA
USB20_N1
USB20_P1
L62
DLW21HN900SQ2LGP
Left USB
USB_1-
USB_1+
090819-1-SI
USB2
SKT-USB-401-GP
22.10254.651
USB20_P2
USB20_N2
L60
Left ESATA
091022-1
USB_2+
USB_2-
Right Side USB x 2
44
U30
NC#8
OUT#7
OUT#6
G5461B2P11U-GP
C263
SC1U10V3ZY-6GP
C302
SCD1U16V2ZY-2GP
091015-1
TC13
SE220U10VM-3-GP
R273
G545_OC#
10KR2J-3-GP
USB_VCCB
WWAN
C301
C304
090829-1
USB1
USB_0-
USB_0+
USB_11-
USB_11+
ACES-CON8-22-GP
20.F1636.008
Right
091022-1
USB20_P0
USB20_N0
L46
USB20_N11
USB20_P11
L54
U73
AFTE14P-GP
AFTP107
AFTP117
AFTP118
AFTP119
AFTP120
AFTP121
AFTP130
AFTP141
BT CONN.
BT Connector
BT1
JST-CON6-21-GP
20.F1571.006
AFTP91
AFTP92
AFTP93
AFTP94
AFTP95
AFTP96
+3VAUX_BT
USB20_P8
BT_LED
USB20_N8
+3VALW
Q19
DMP2130L-7-GP
C241
R262
100KR2J-1-GP
C243
BT_OFF_G
C248
R261
4K7R2J-2-GP
BT_OFF
<Core Design>
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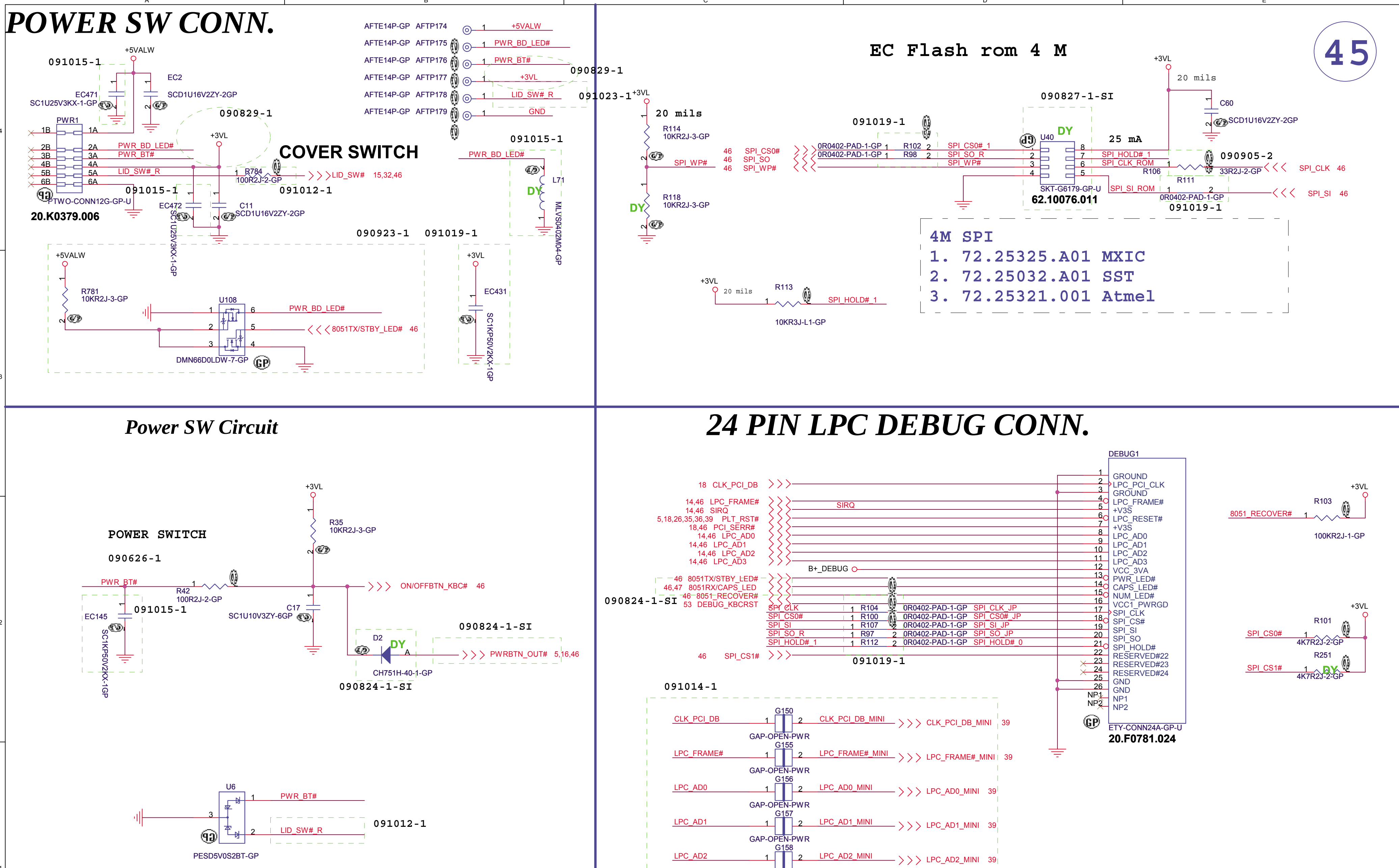
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
USB / BT Connector
Size A3
Document Number
S-Class Intel
Rev SD
Date: Wednesday, October 28, 2009
Sheet 44 of 62



<Core Design>

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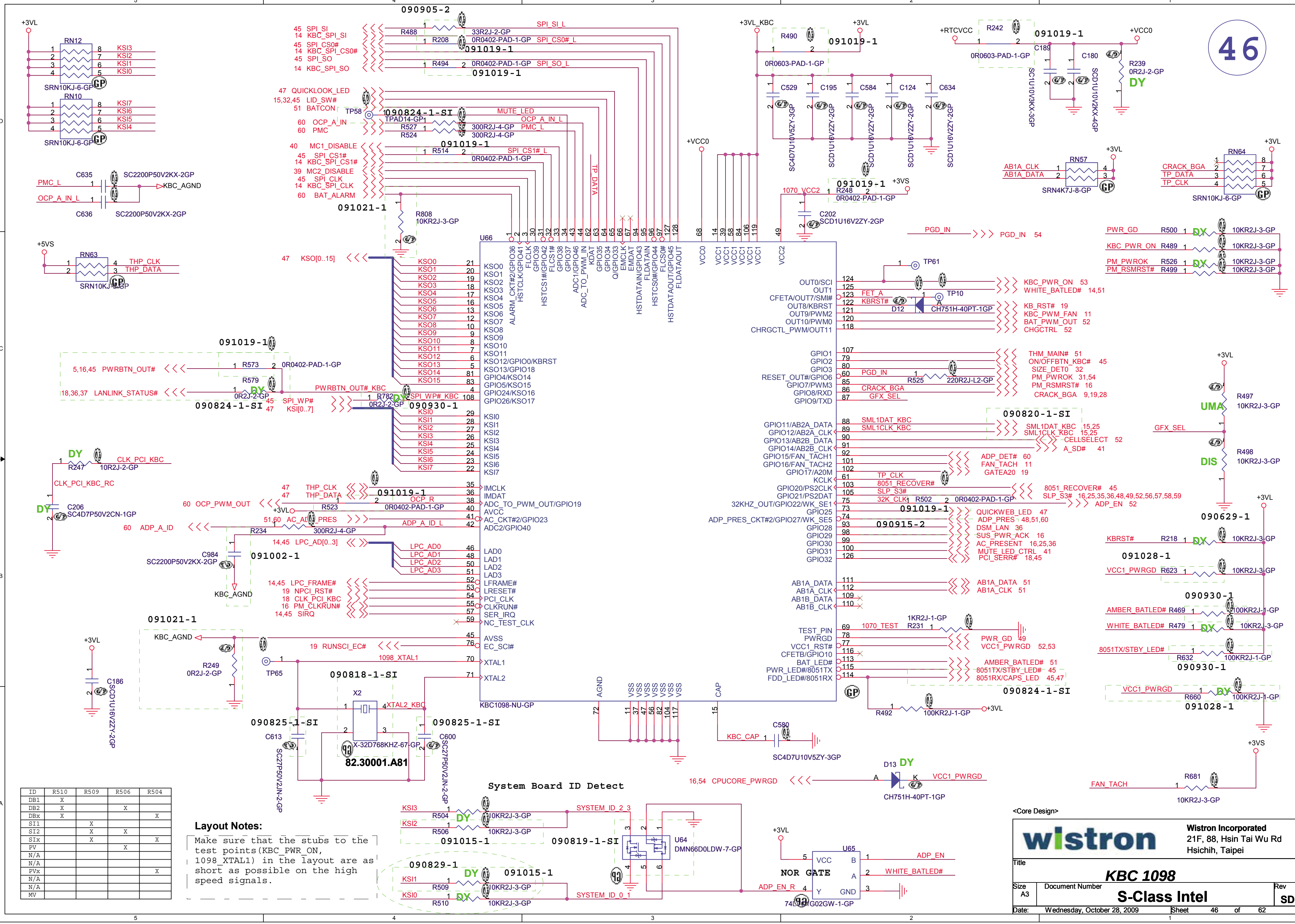
Hsichih, Taipei

Title: **FWH / BTN / DEBUG CONN.**

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 | Sheet 45 of 62



Layout Notes:

Make sure that the stubs to the test points(KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.

ID	R510	R509	R506	R504
DB1	X			
DB2	X		X	
DBx	X			X
SI1		X		
SI2		X	X	
SIx		X		X
PV			X	
N/A				
N/A				
PVx				X
N/A				
N/A				
MV				

<Core Design>

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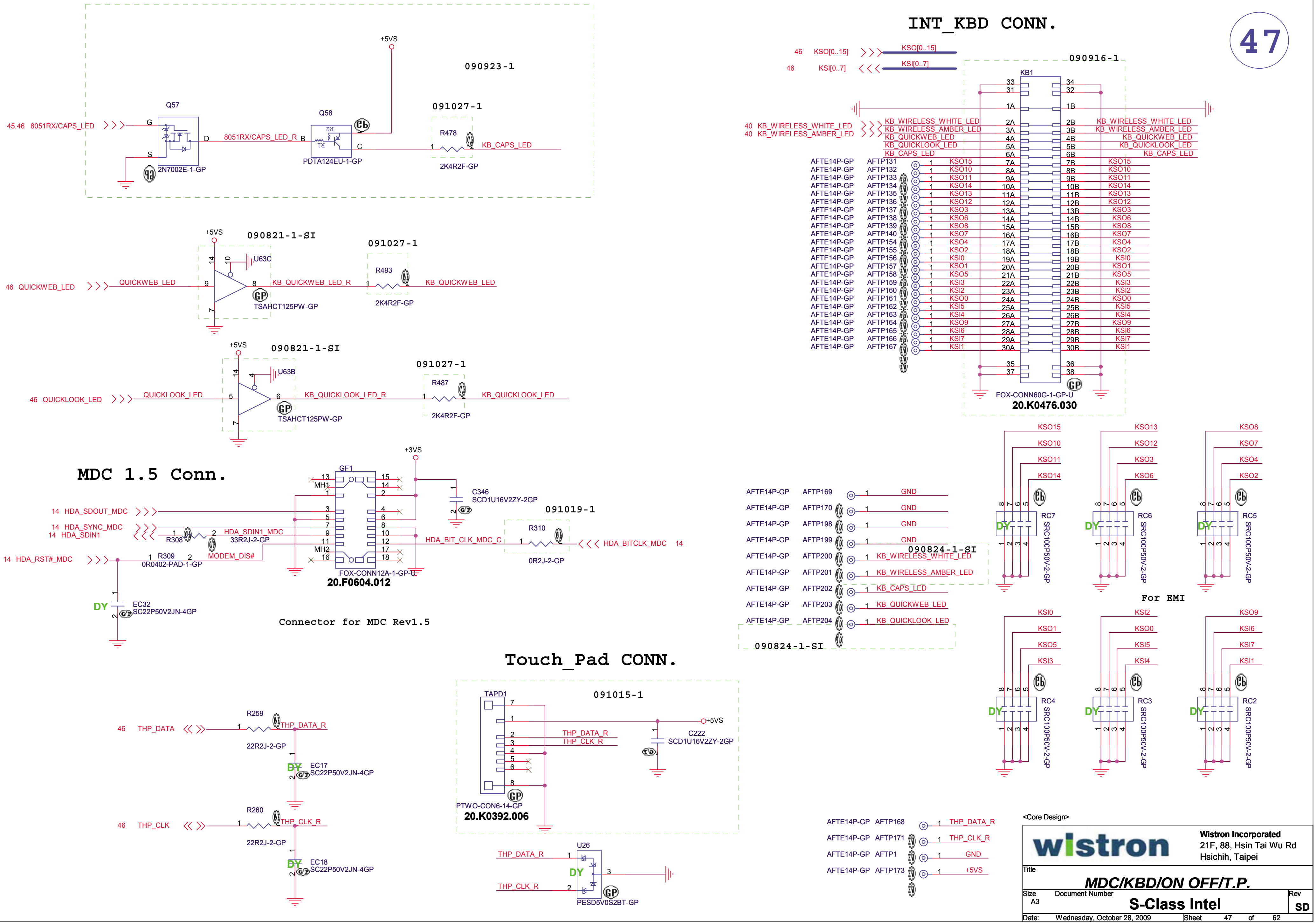
Title: KBC 1098

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 46 of 62



<Core Design>

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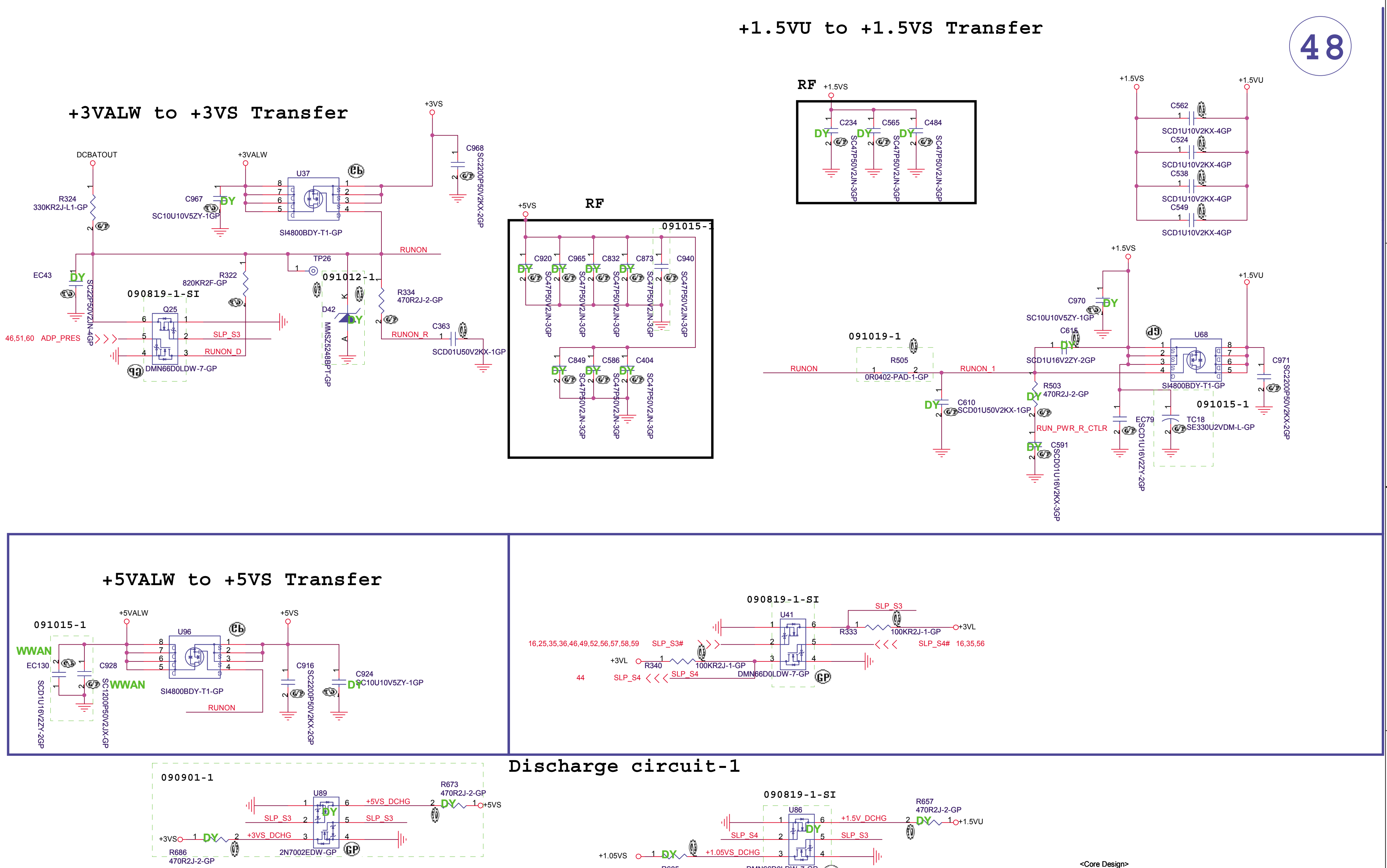
Hsichih, Taipei

Title: MDC/KBD/ON OFF/T.P.

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 47 of 62



<Core Design>

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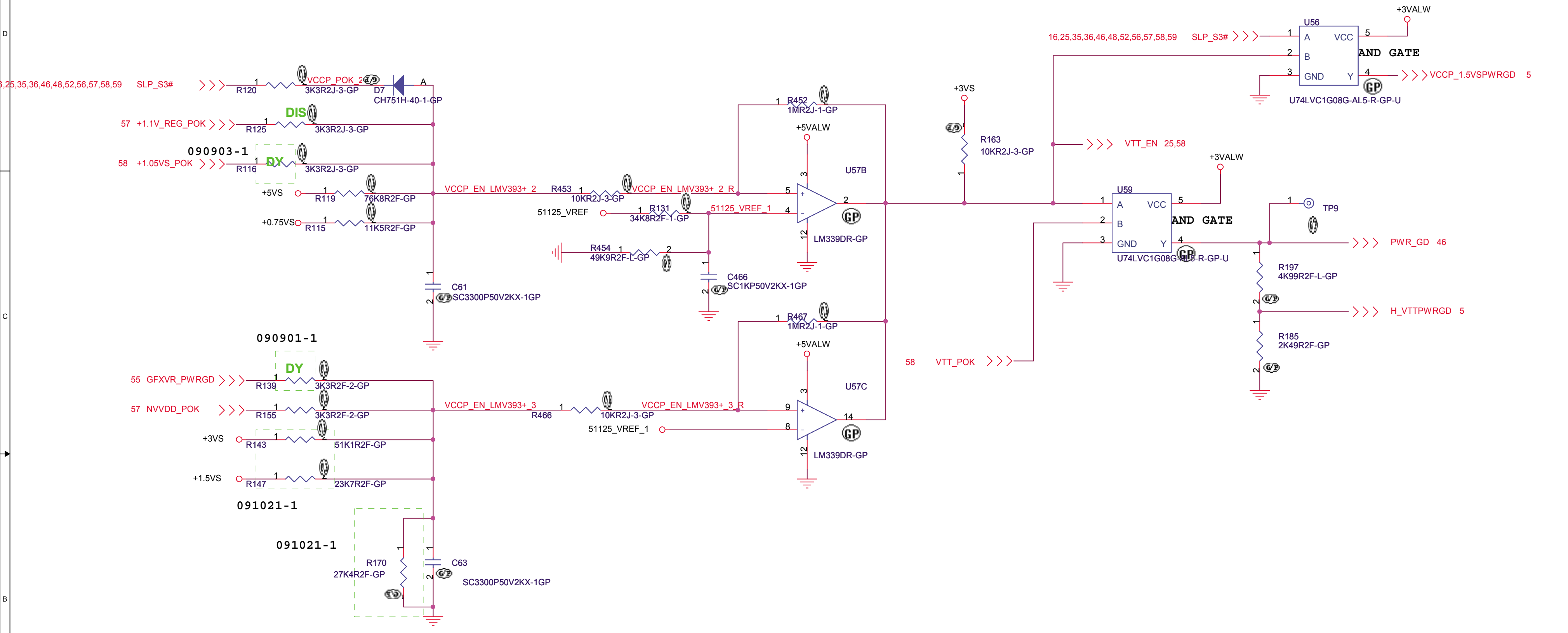
Title	DC/DC Circuit		
Size A3	Document Number	S-Class Intel	Rev SD
Date:	Wednesday, October 28, 2009	Sheet 48 of 62	



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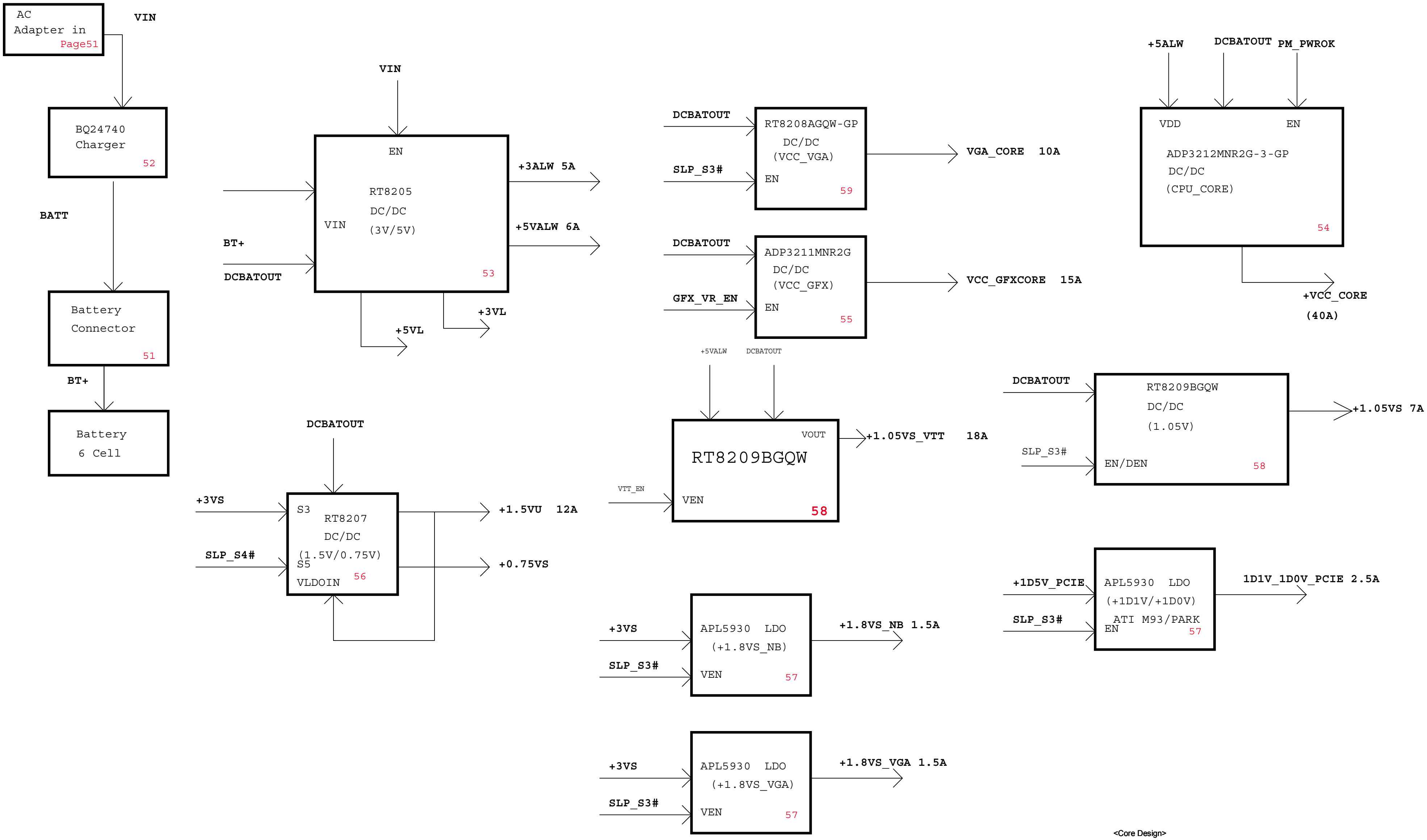
Title
POK CKT

Size	Document Number	Rev
A3	S-Class Intel	SD

Date: Wednesday, October 28, 2009 Sheet 49 of 62

Power Block Diagram



<Core Design>

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Title	Power Block Diagram	
Size A3	Document Number S-Class Intel	Rev SD
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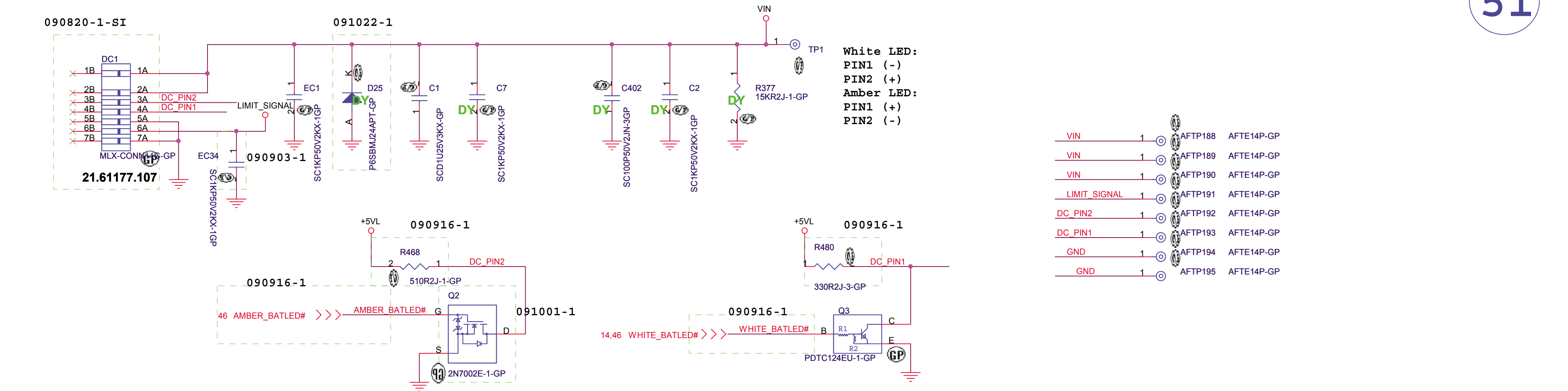
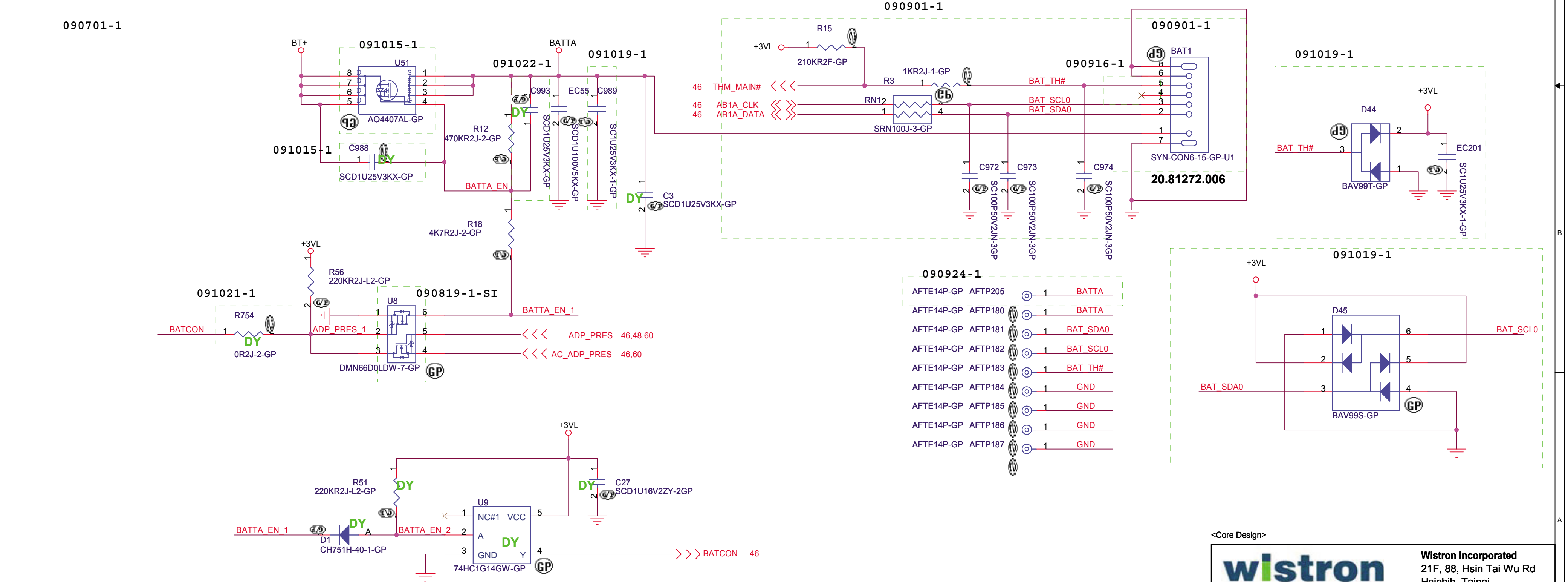
Adaptor in to generate DCBATOUT

51



BATTERY CONNECTOR



<Core Design>

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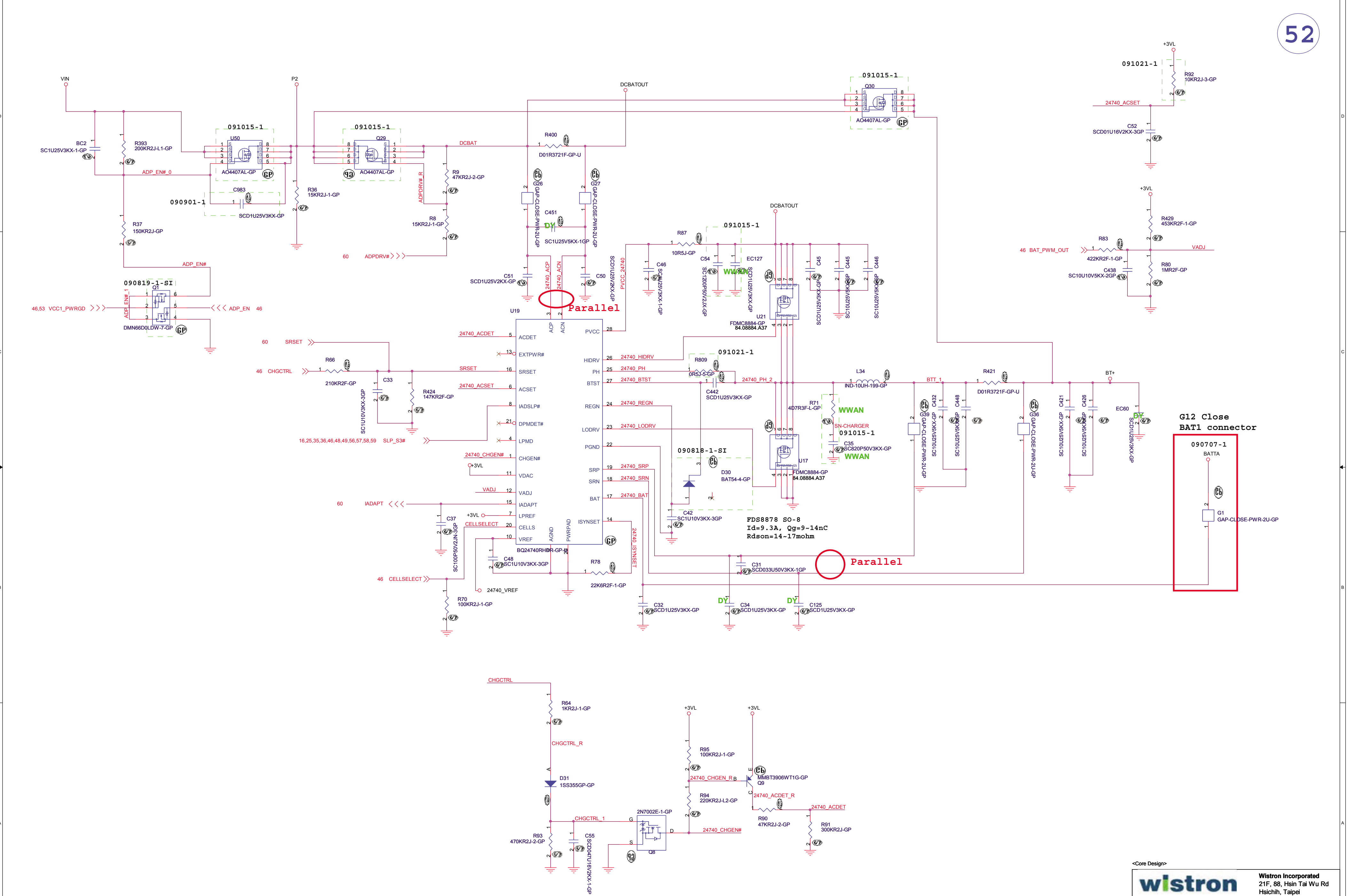
Title	DC & BATTERT CONN.	
Size: Custom	Document Number: S-Class Intel	Rev: SD
Date: Wednesday, October 28, 2009	Sheet 51 of 62	



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Title	CHARGER BQ24740
Size	A2
Document Number	S-Class Intel
Rev	SD
Date:	Wednesday, October 28, 2009
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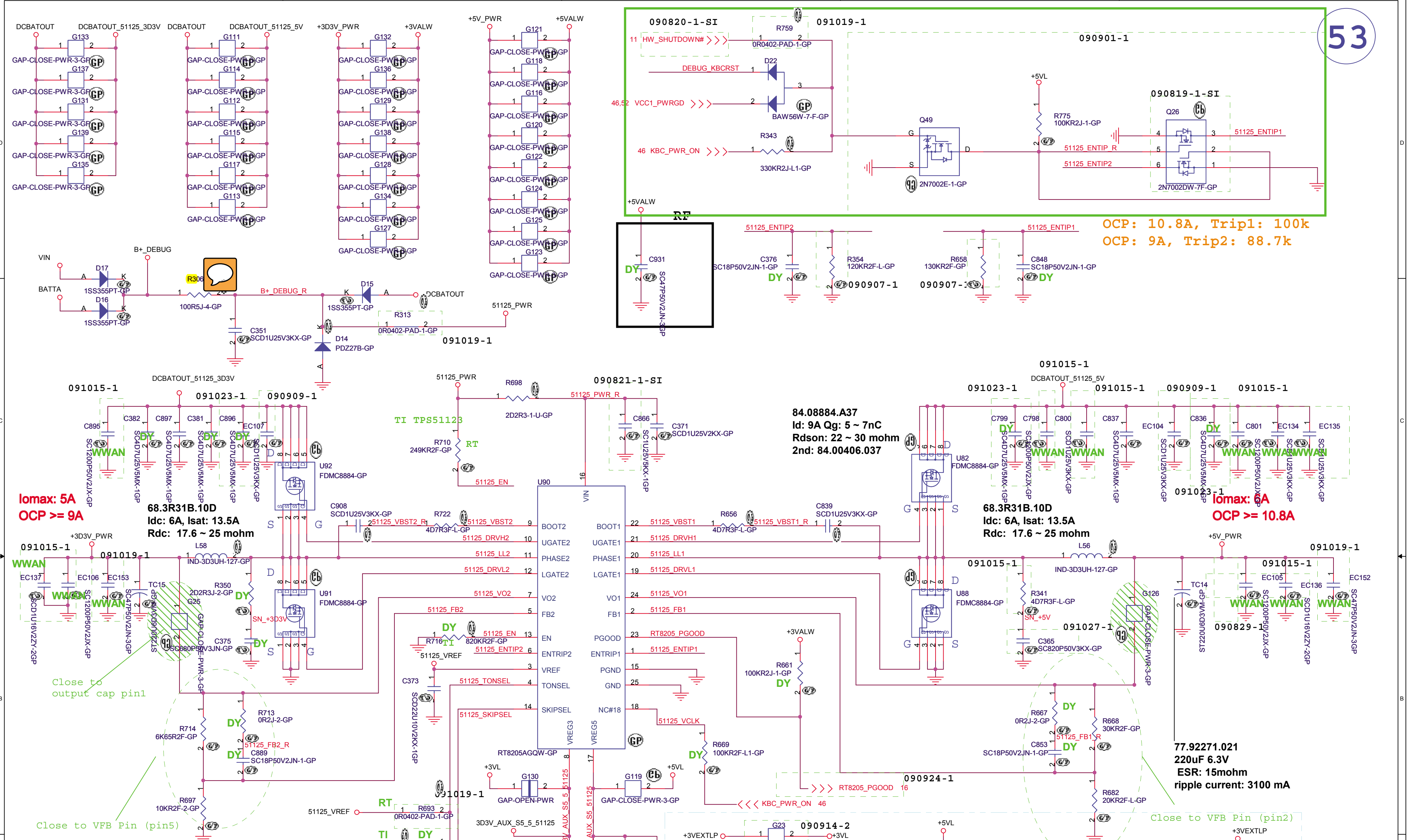

	TPS51125	TPS51123
Q49 Q26	Install	Non-Install
R694	Install	Install
R669	Non-Install	Install
R710	Non-Install	Install
R716	820K	100K
R693	Non-Install	Non-Install
R709	Install	Install
R687	Non-Install	Non-Install

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R694	Non-Install	Non-Install
R669	Non-Install	Install
R710	Install	Install
R716	Non-Install	Non-Install
R693	Install	Install
R709	Install	Install
R687	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz

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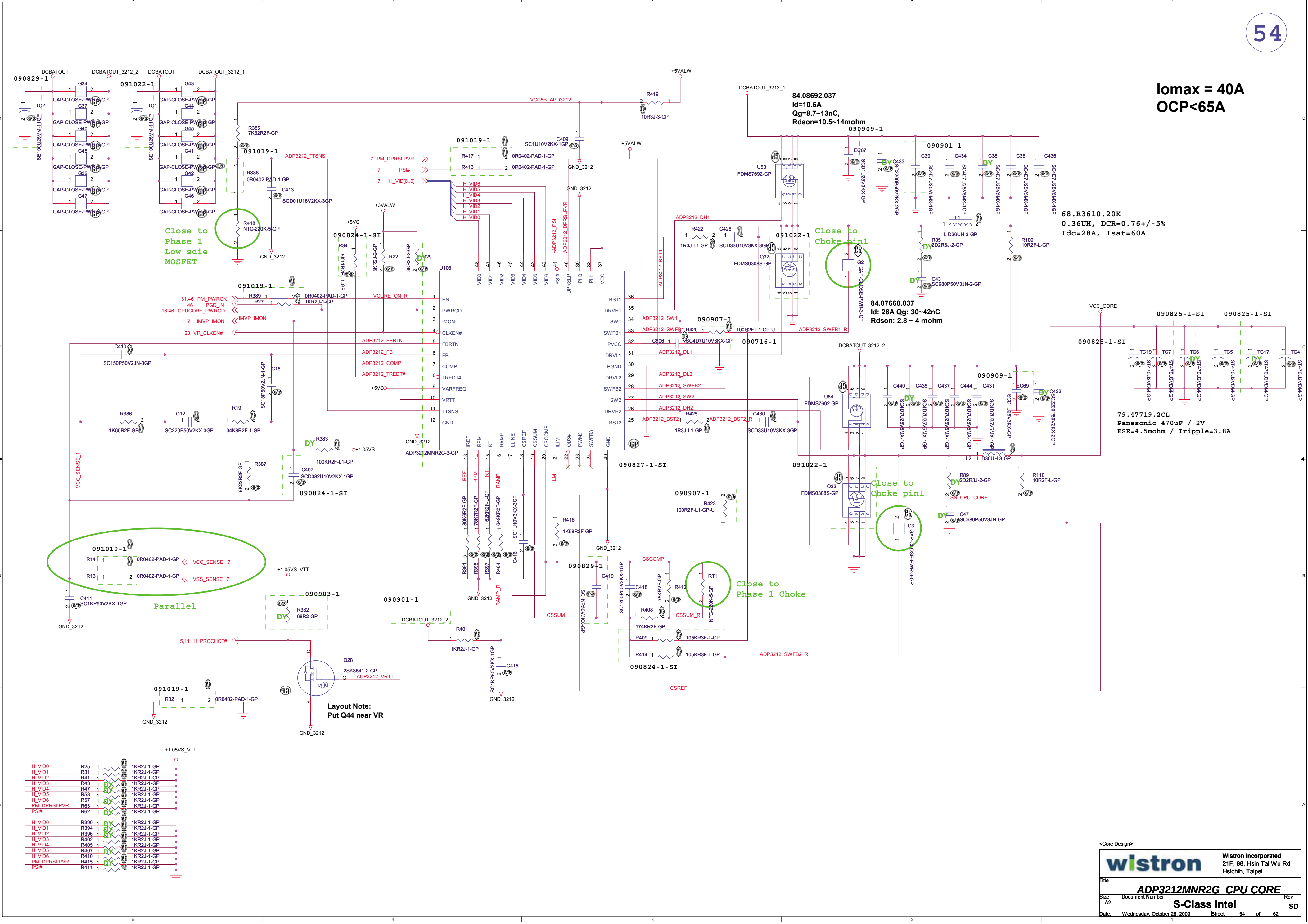
Title		
RT8205AGQW +5VALW/+3VALW		
Size: Custom	Document Number: S-Class Intel	Rev: SD
Date: Wednesday, October 28, 2009	Sheet 53 of 62	



54
Iomax = 40A
OCP<65A
84.08692.037
Id=10.5A
Qg=8.7~13nC,
Rdson=10.5~14mohm
84.07660.037
Id: 26A Qg: 30~42nC
Rdson: 2.8 ~ 4 mohm
68.R3610.20K
0.36UH, DCR=0.76+/-5%
Idc=28A, Isat=60A
79.47719.2CL
Panasonic 470uF / 2V
ESR=4.5mohm / Iripple=3.8A
Close to Phase 1 Low sdie MOSFET
Close to Choke pin1
Close to Phase 1 Choke
Parallel
Layout Note:
Put Q44 near VR
ADP3212MNR2G-3-GP
<Core Design>
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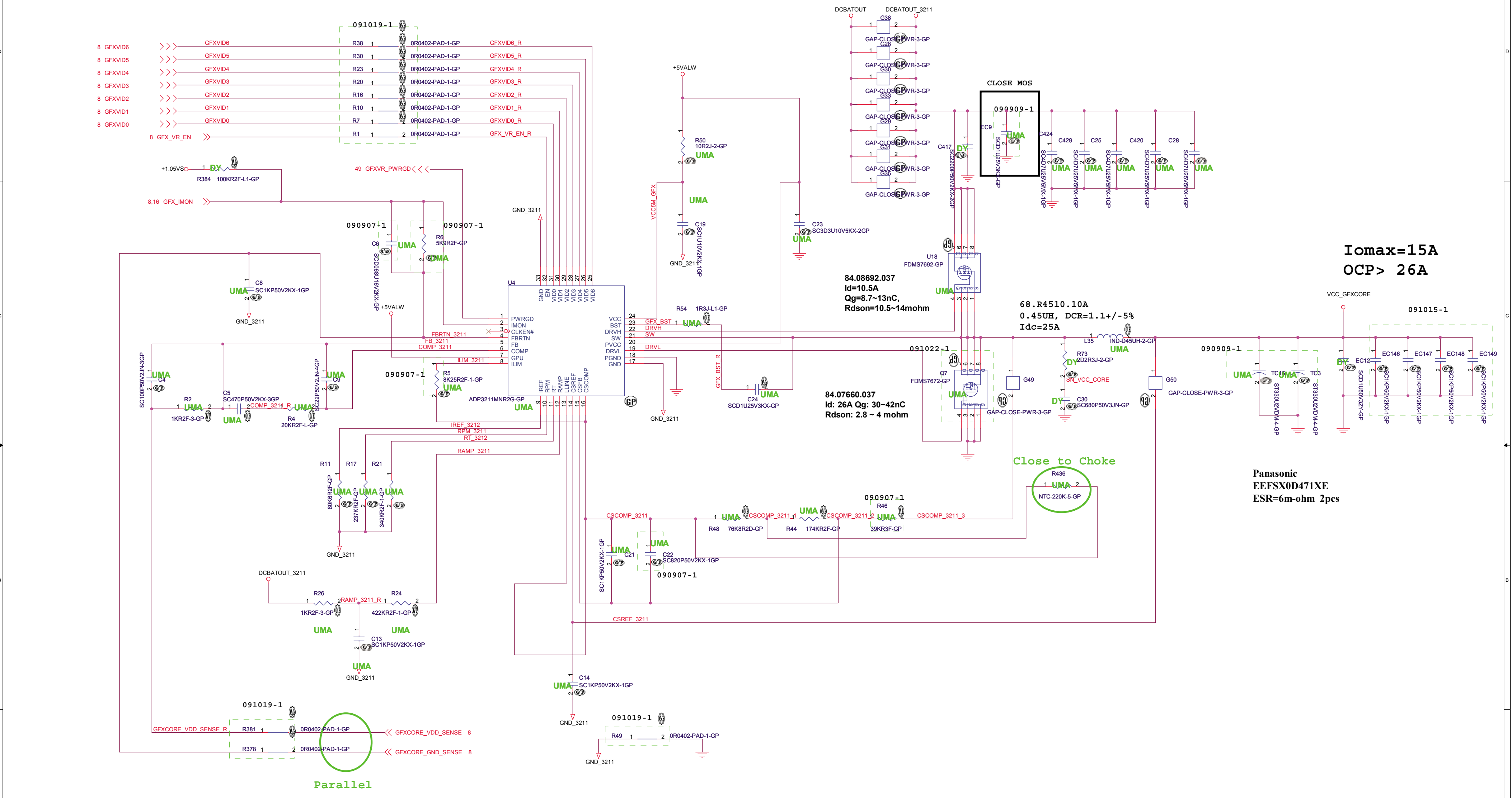
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
ADP3212MNR2G_CPU CORE
Size A2
Document Number
S-Class Intel
Rev SD
Date: Wednesday, October 28, 2009
Sheet 54 of 62



<Core Design>

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Title	ADP3211MNR2G_+VCC_GFX_CORE	
Size A2	Document Number S-Class Intel	Rev SD
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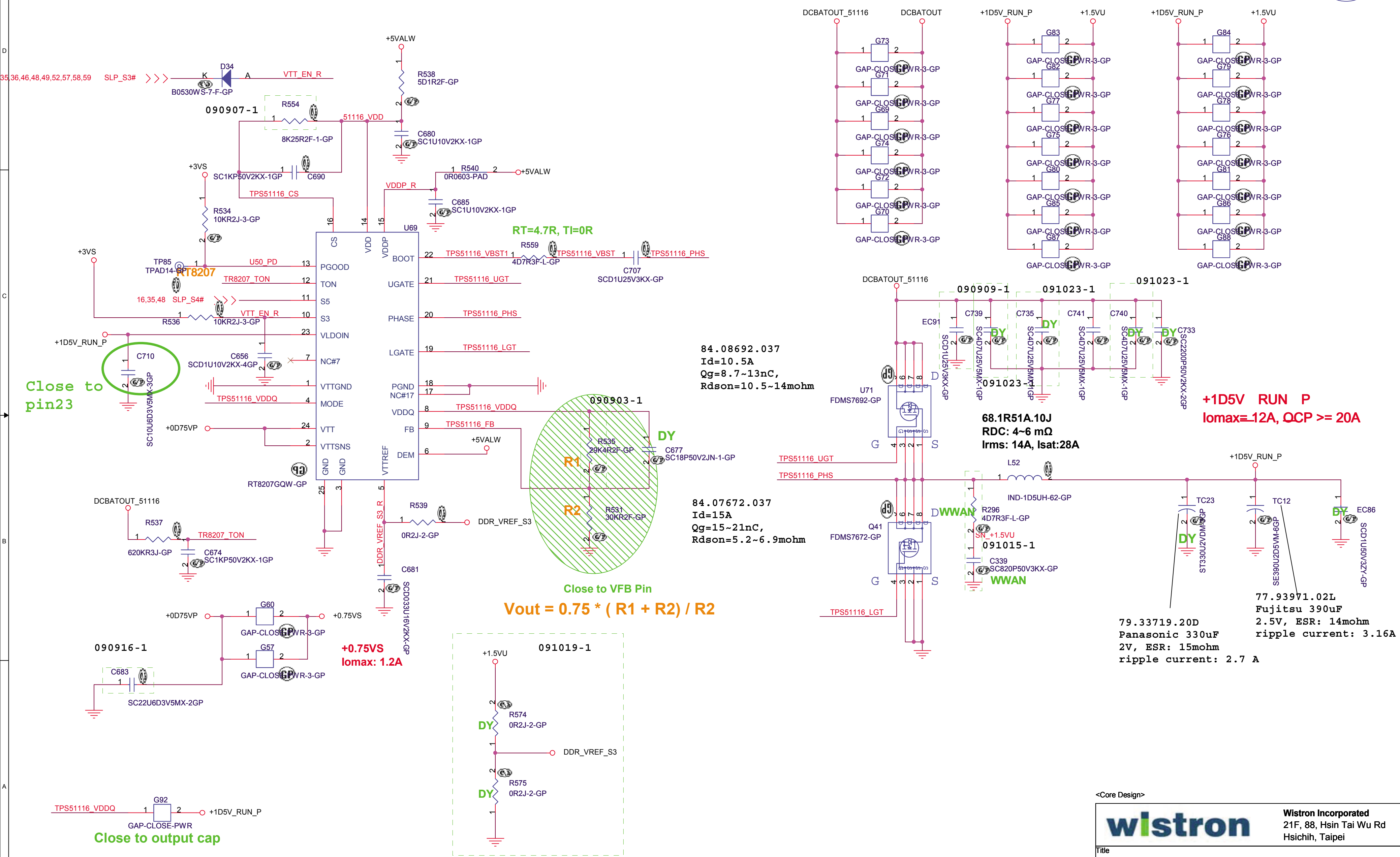
RT8207 for 1D5V and 0D75V



<Core Design>

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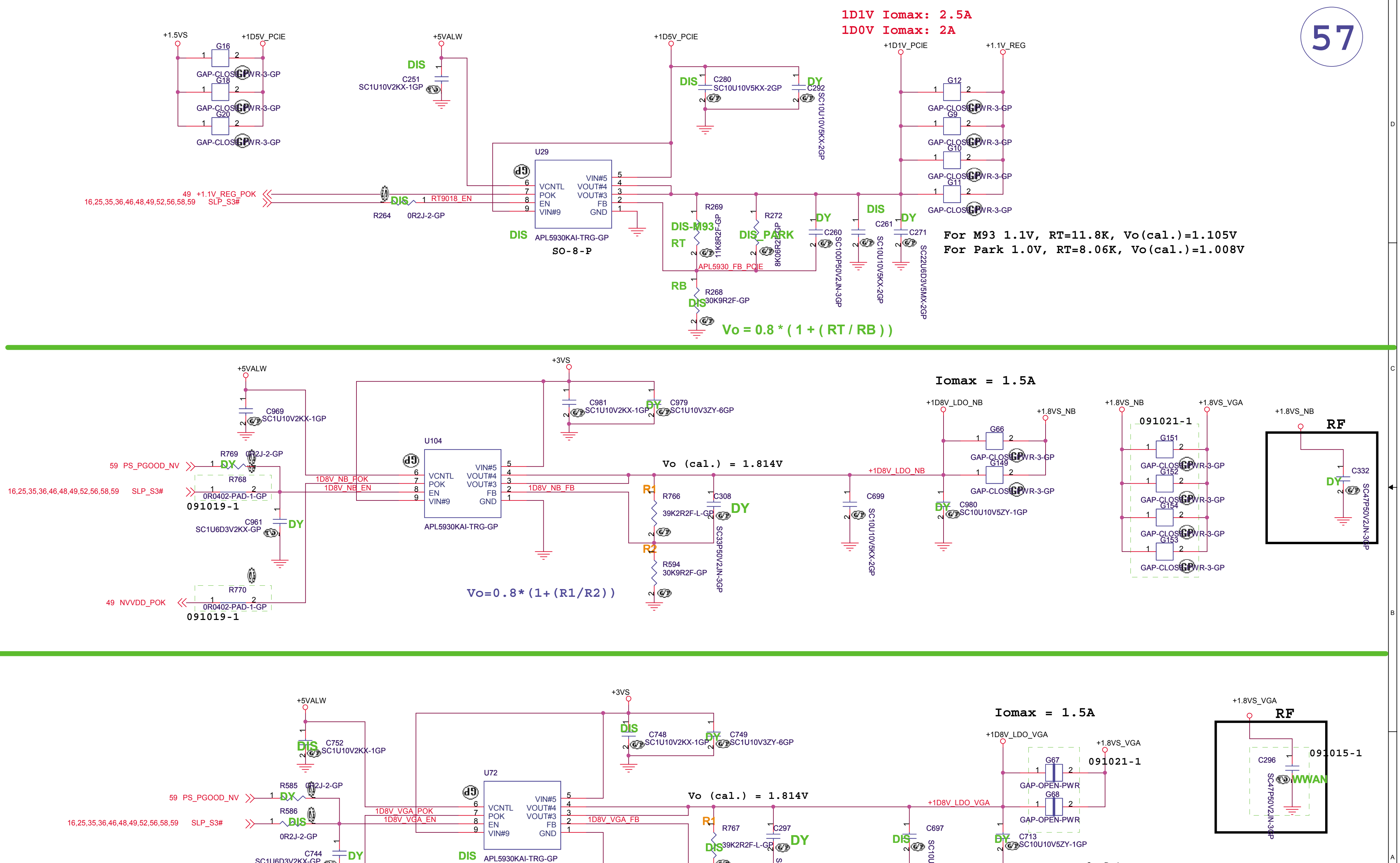
Title	RT8207GQW_+1.5VU / +0.75VS
Size	A3
Document Number	S-Class Intel
Rev	SD
Date:	Wednesday, October 28, 2009
Sheet	56 of 62



<Core Design>

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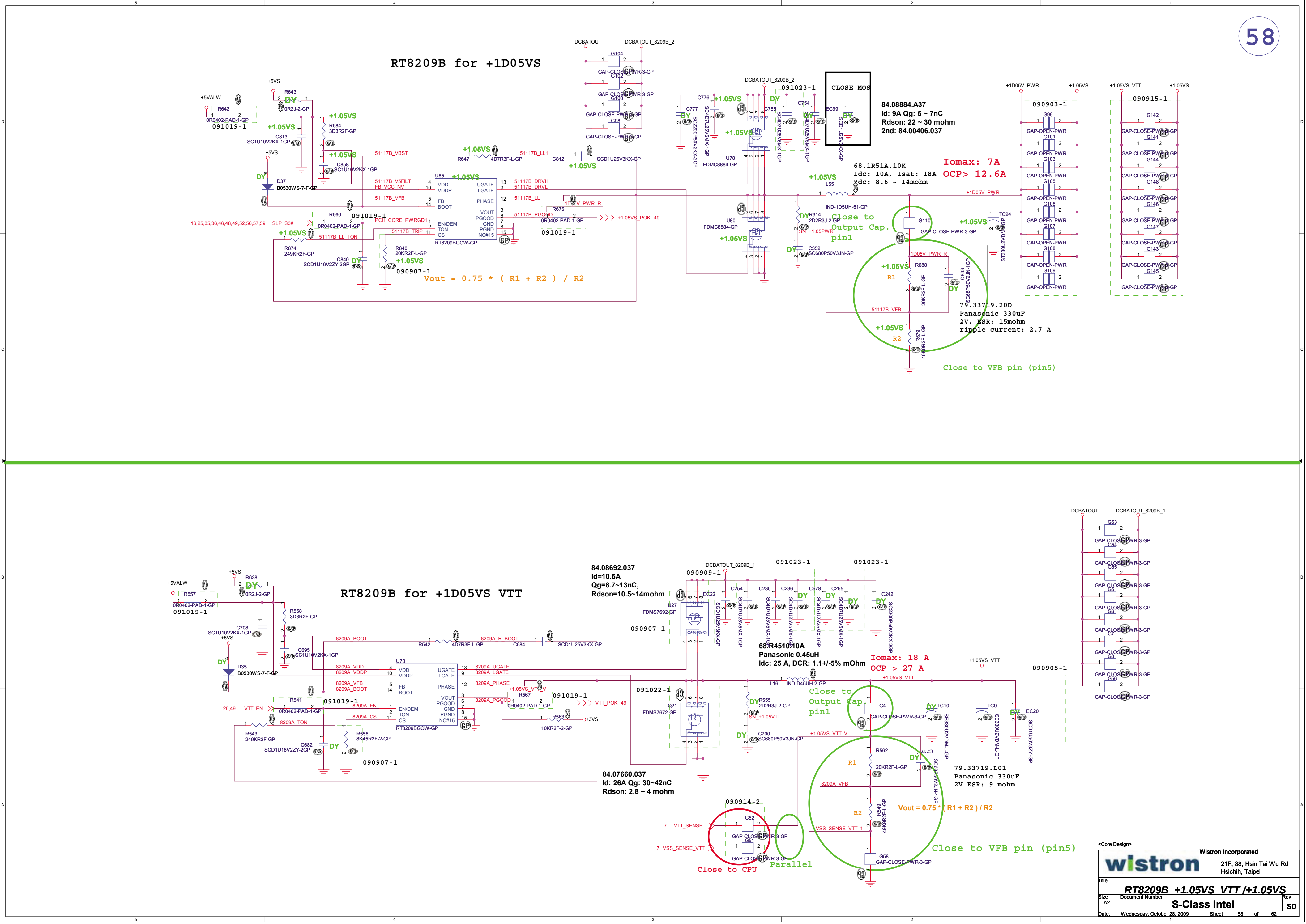
Title: APL5930_+1.8VS_VGA /+1.8VS_NB /+1D1V_REG

Size: A3 | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 57 of 62



RT8209B for +1D05VS
84.08884.A37
Id: 9A Qg: 5 ~ 7nC
Rdson: 22 ~ 30 mohm
2nd: 84.00406.037
CLOSE MOS
68.1R51A.10K
Idc: 10A, Isat: 18A
Rdc: 8.6 ~ 14mohm
Iomax: 7A
OCP> 12.6A
Close to Output Cap. pin1
79.33719.20D
Panasonic 330uF
2V, ESR: 15mohm
ripple current: 2.7 A
Close to VFB pin (pin5)
Vout = 0.75 * (R1 + R2) / R2
RT8209B for +1D05VS_VTT
84.08692.037
Id=10.5A
Qg=8.7~13nC,
Rdson=10.5~14mohm
68.R4510.10A
Panasonic 0.45uH
Idc: 25 A, DCR: 1.1+/-5% mOhm
Iomax: 18 A
OCP > 27 A
Close to Output Cap pin1
84.07660.037
Id: 26A Qg: 30~42nC
Rdson: 2.8 ~ 4 mohm
79.33719.L01
Panasonic 330uF
2V ESR: 9 mohm
Vout = 0.75 * (R1 + R2) / R2
Close to VFB pin (pin5)
Close to CPU
Parallel
<Core Design>
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Title
RT8209B +1.05VS_VTT /+1.05VS
Size A2
Document Number
S-Class Intel
Rev SD
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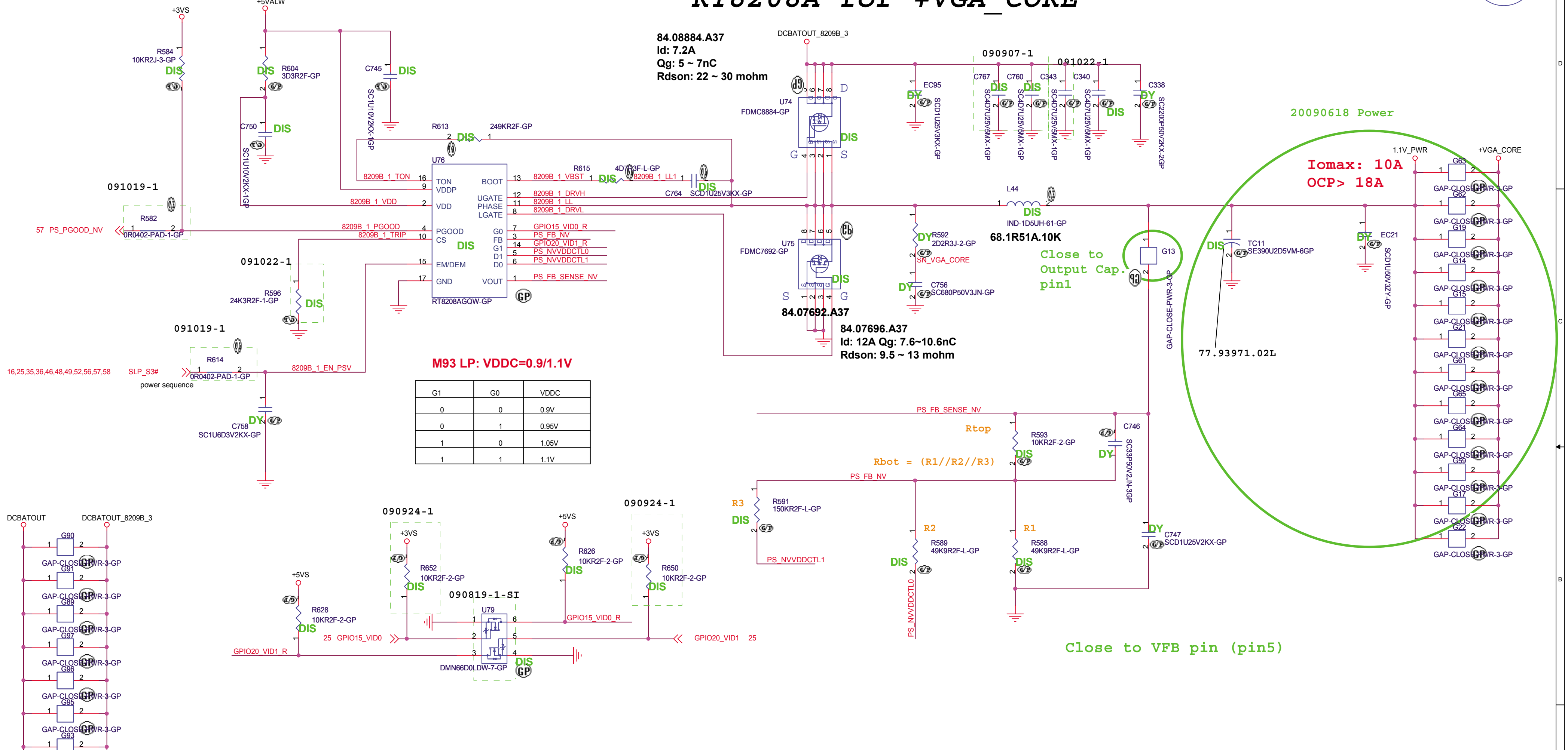
RT8208A for +VGA_CORE



G1	G0	VDDC
0	0	0.9V
0	1	0.95V
1	0	1.05V
1	1	1.1V

+VCC_GFX_CORE = (1 + Rt / Rb) X 0.75

+VCC_GFX_CORE	RTop	RBot	GPIO15_VID0_R	GPIO20_VID1_R	ideal voltage	actual voltage
0.9v	10k	R1 49.9k	LOW	LOW	0.9003	
0.95v	10k	R1 R2 49.9k // 49.9k	LOW	HIGH	0.9493	
1.05v	10k	R1 R3 49.9k // 150k	HIGH	LOW	1.0506	
1.1v	10k	R1 R2 R3 49.9k // 49.9k // 150k	HIGH	HIGH	1.0997	

<Core Design>

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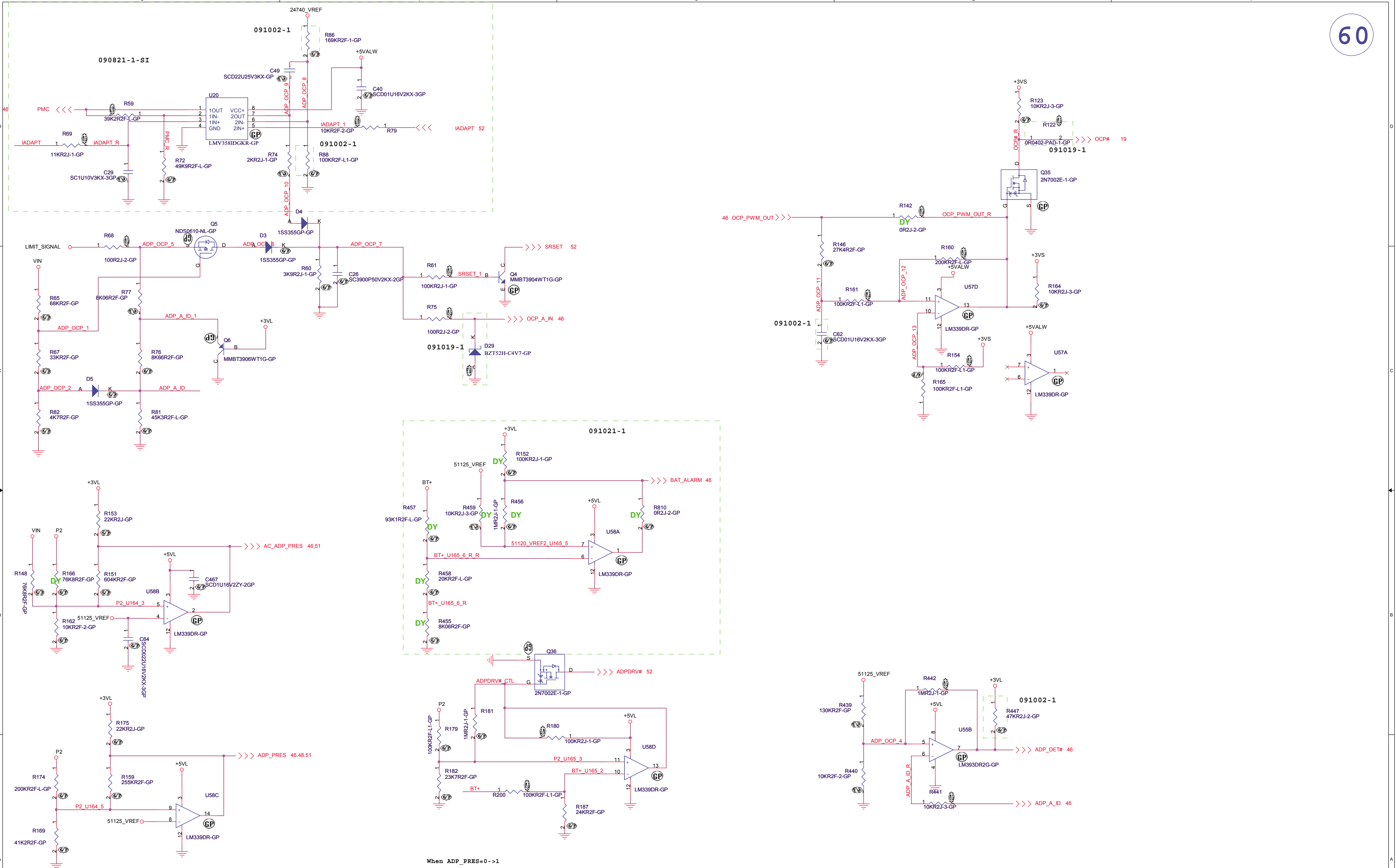
Title: RT8208AGQW +VGA_CORE

Size: Custom | Document Number: S-Class Intel | Rev: SD

Date: Wednesday, October 28, 2009 | Sheet 59 of 62



When AC_ADP_PRES=0 -->1
Vin*(R162//R151)/ [(R162//R151)+R148]=51125_VREF
Vin=17.6145V

When AC_ADP_PRES=1 --> 0
[(Vin-51125_VREF)/R148]+[(+3VL-51125_VREF)/(R151+R153)]=51125_VREF/R162

Vin=17.212554V

When ADP_PRES=0->1

P2*(R169//R159)/ [(R169//R159)+R174]=51125_VREF

P2=13.325V

When ADP_PRES=1->0

[(P2-51125_VREF)/R169]+[(+3VL-51125_VREF)/(R175+R159)]=51125_VREF/R169

P2=10.894V

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Title	ADP OCP	
Size A2	Document Number S-Class Intel	Rev SD
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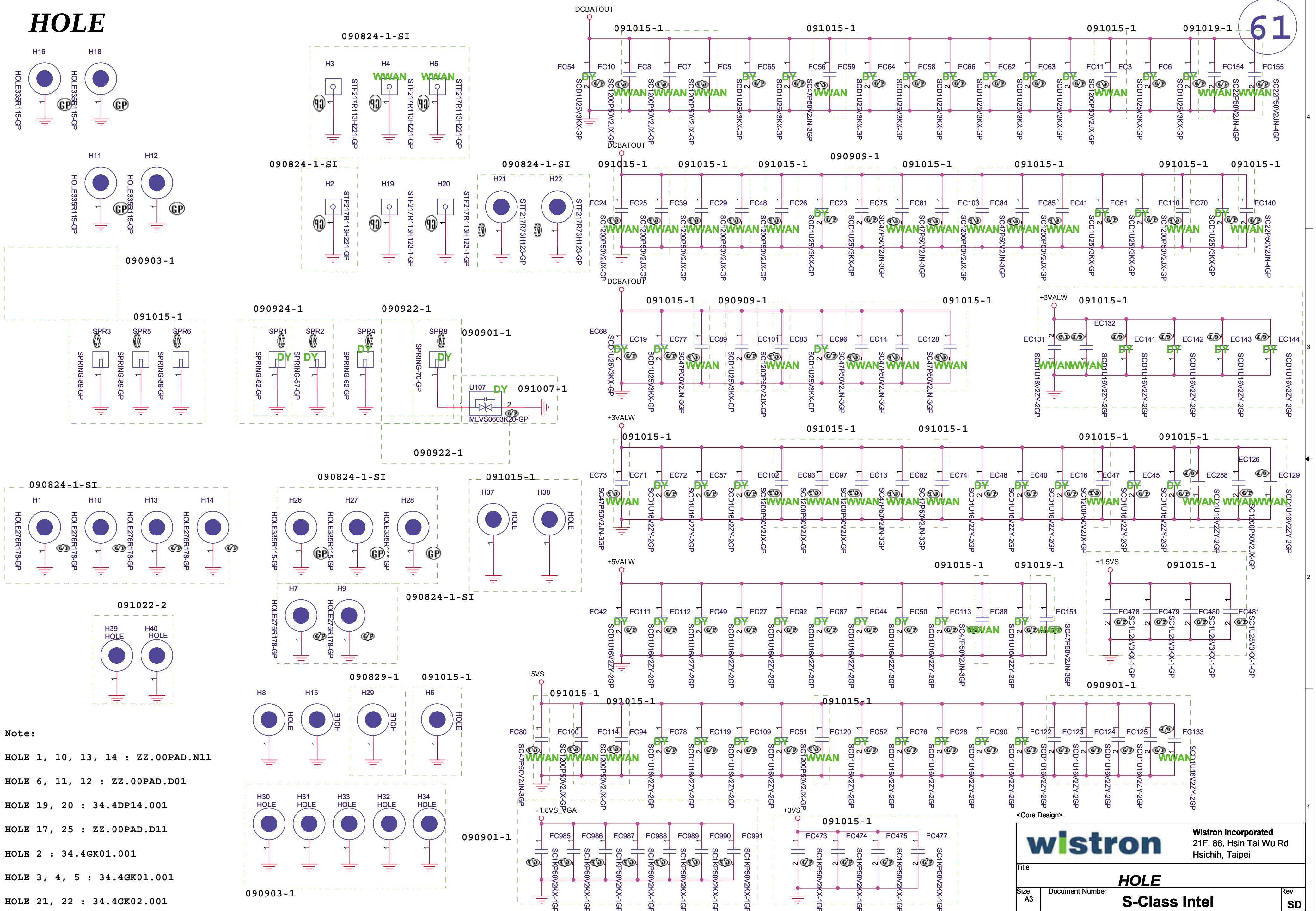
HOLE



Note:

HOLE 1, 10, 13, 14 : ZZ.00PAD.N11

HOLE 6, 11, 12 : ZZ.00PAD.D01

HOLE 19, 20 : 34.4DP14.001

HOLE 17, 25 : ZZ.00PAD.D11

HOLE 2 : 34.4GK01.001

HOLE 3, 4, 5 : 34.4GK01.001

HOLE 21, 22 : 34.4GK02.001

<Core Design>

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Title	HOLE	
Size A3	Document Number S-Class Intel	Rev SD
Date: Wednesday, October 28, 2009	Sheet 61 of 62	