2012 S-Series Richie 13.3"
UMA/DIS Muxless Schematic

Intel Chief River Platform
Ivy Bridge (rPGA989)
Panther Point PCH

REV:-1
2012-03-15

DY:No stuff
DIS_PX:Only DIS install

<Core Design>

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Title: ***Cover Page***		
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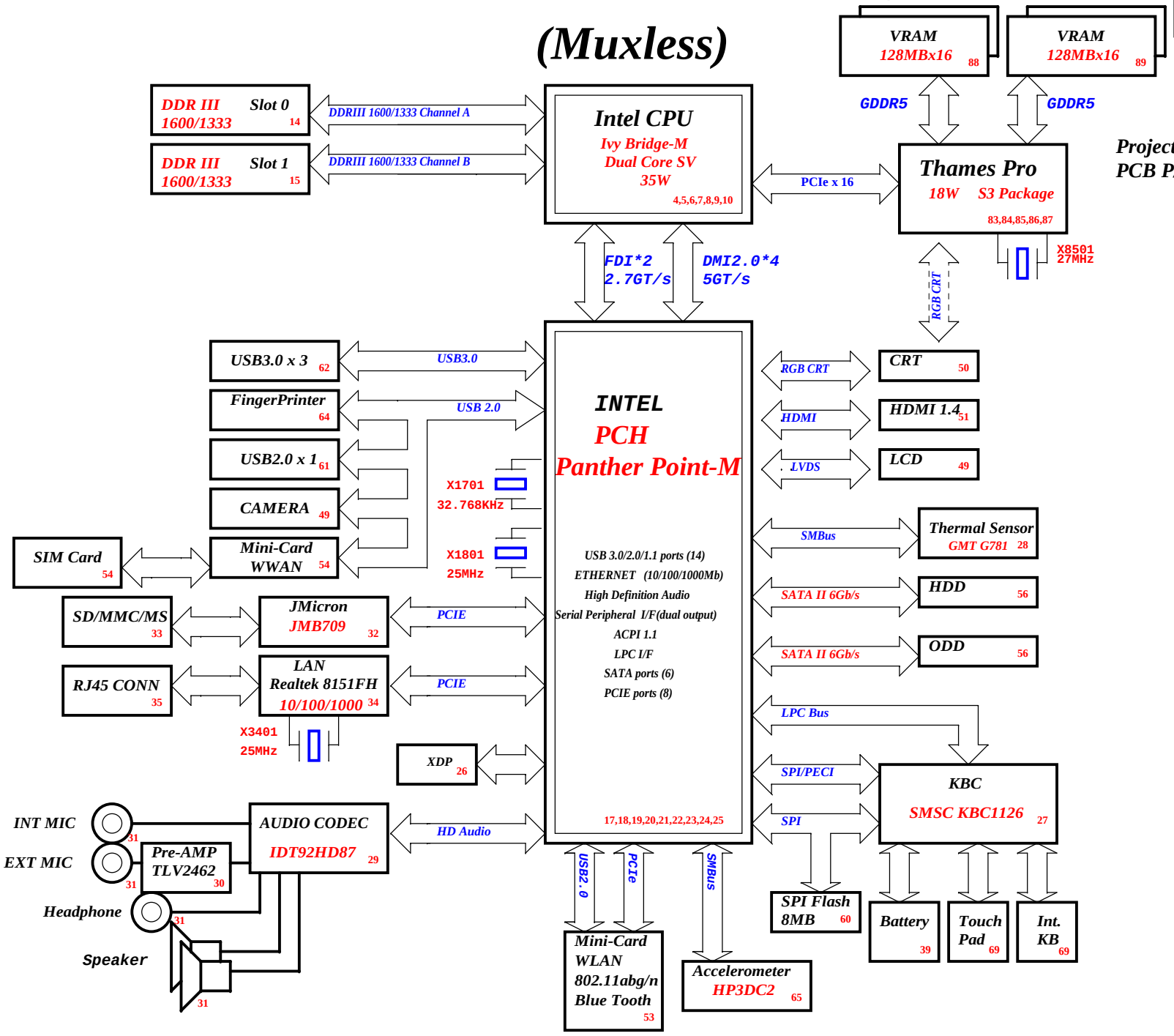
S-Series Richie Block Diagram (Muxless)



Project code:91.4RS01.001
PCB P/N:11241

SYSTEM DC/DC TPS51461RGER 48	
INPUTS	OUTPUTS
DCBATOUT	+VCCSA

CPU DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51211DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA UP1527QQDD 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736RGRR 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068AZQWID 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC FDMC7696 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

PCB LAYER

L1:Top	L5:Vcc
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

<Core Design>

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Title: Block Diagram

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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel? HD Audio dock signals to the corresponding Cougar Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. Note: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1K ohm resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2] CFG2 is for the 16x	**PCIe Static x16 Lane Numbering Reversal.**	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	**1**
CFG[4]	**Display Port Presence strap**	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull down to GND through a 1KΩ ± 5% resistor to enable port	**1**
CFG[6:5]	**PCIE Port Bifurcation Straps**	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	**11**
CFG[17:7]	**Reserved configuration lands. A test point may be placed on the board for these lands.**		

PCIe Routing

LANE1	X
LANE2	X
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	LAN
LANE7	X
LANE8	X

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE VGA_CORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
1D5V_S3 DDR_VREF_S3	5V 1.5V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-14.1V 9V-19.5V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

USB 2.0 Table

Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	N/A
3	N/A
4	N/A
5	N/A

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
DIMM1 DIMM2 Touch-Pad				PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA
N/A				PCH_SML0_CLK/PCH_SML0_DATA
KBC G781_Thermal IC GPU_Thames PRO G-Sensor		 1001100 0X41 0X52		PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA

<Core Design>

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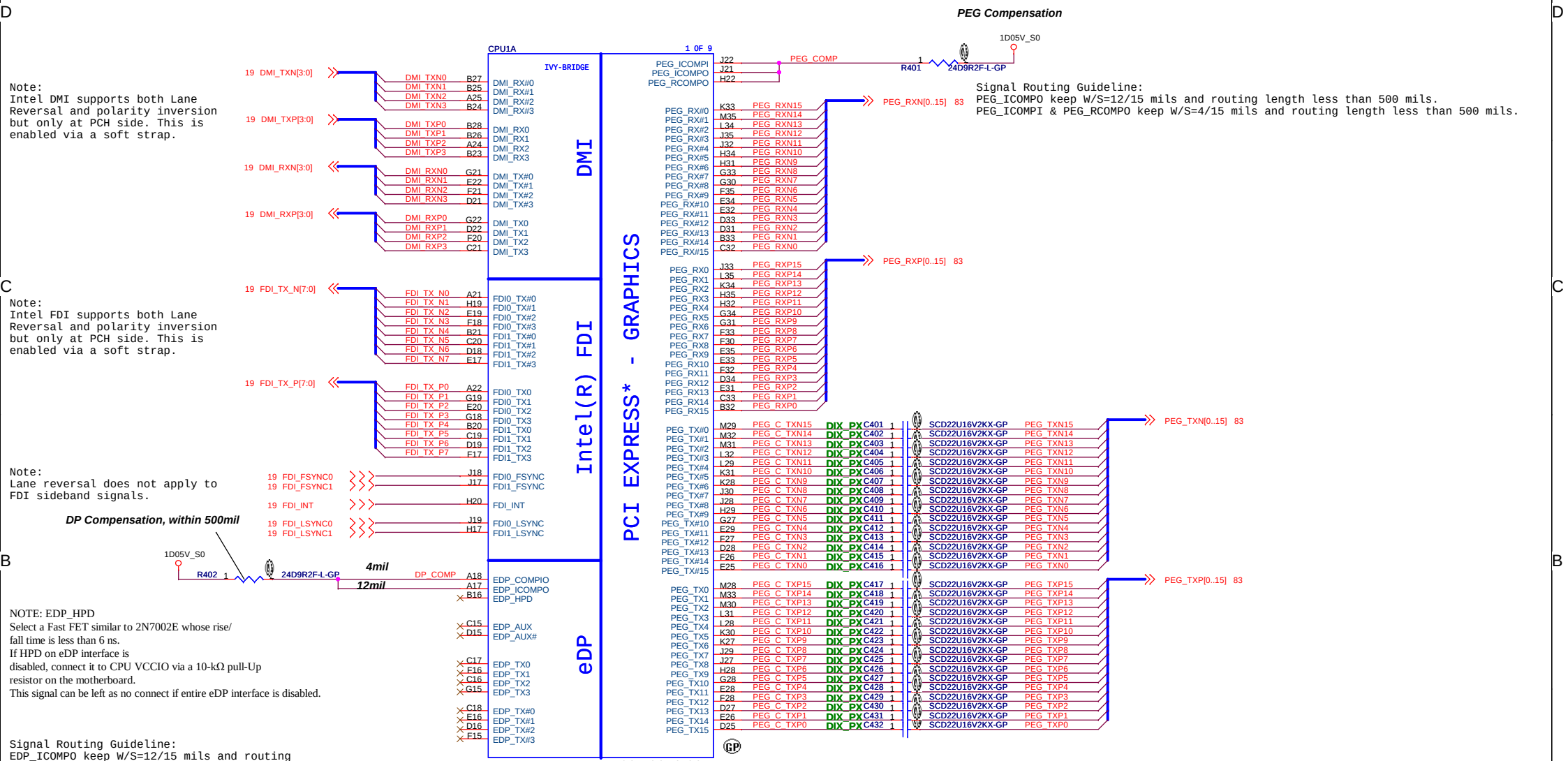
CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)



PEG Compensation

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

DP Compensation, within 500mil

4mil
12mil

NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

62.10040.821
1ST = 62.10055.551
2nd = 62.10055.321
3rd = 62.10055.731

BOM Note:1st/2nd/3rd Add in BOM

<Core Design>

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Title: CPU(1/7): DMI/PEG/FDI

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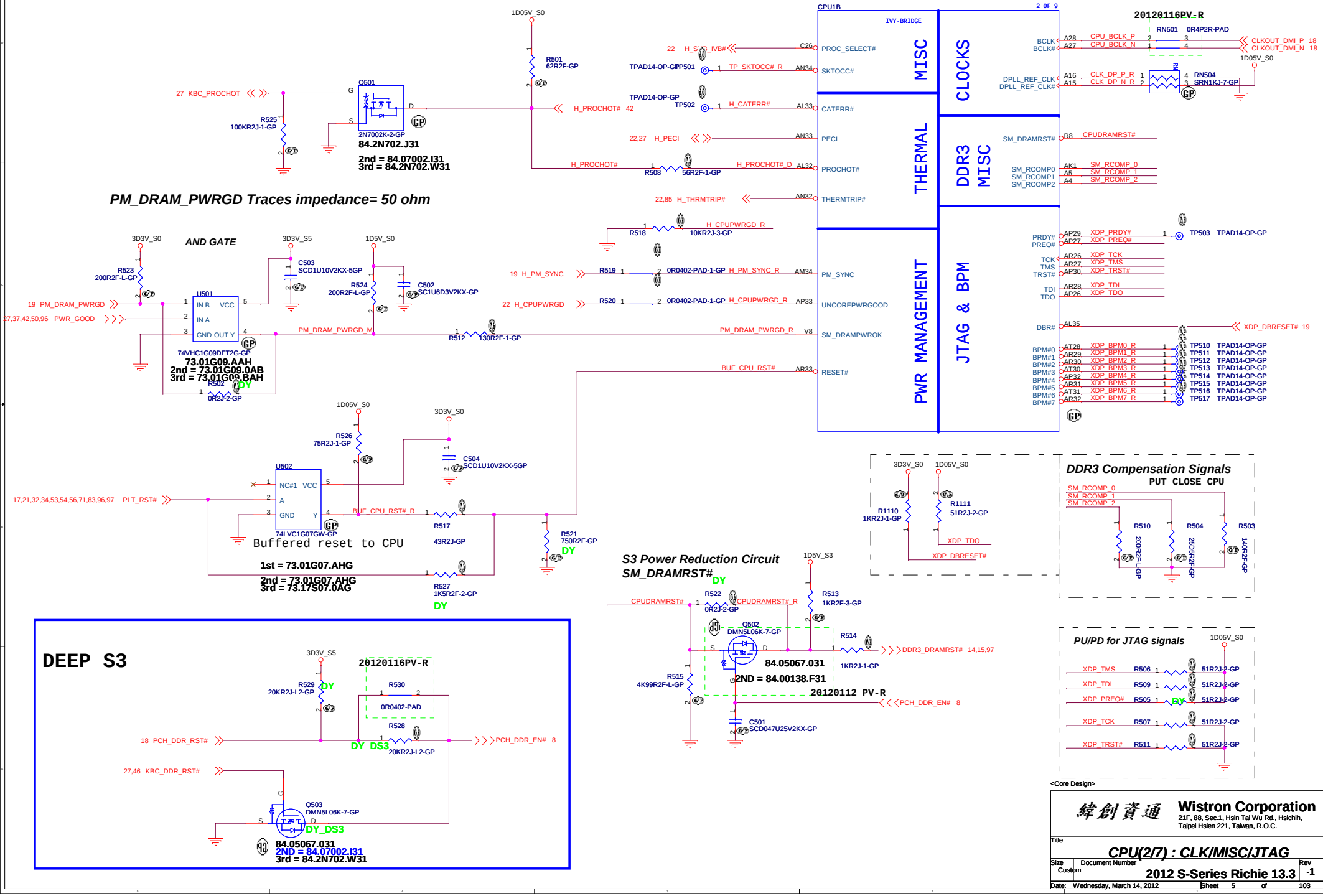
CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



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Title: CPU(2/7) : CLK/MISC/JTAG

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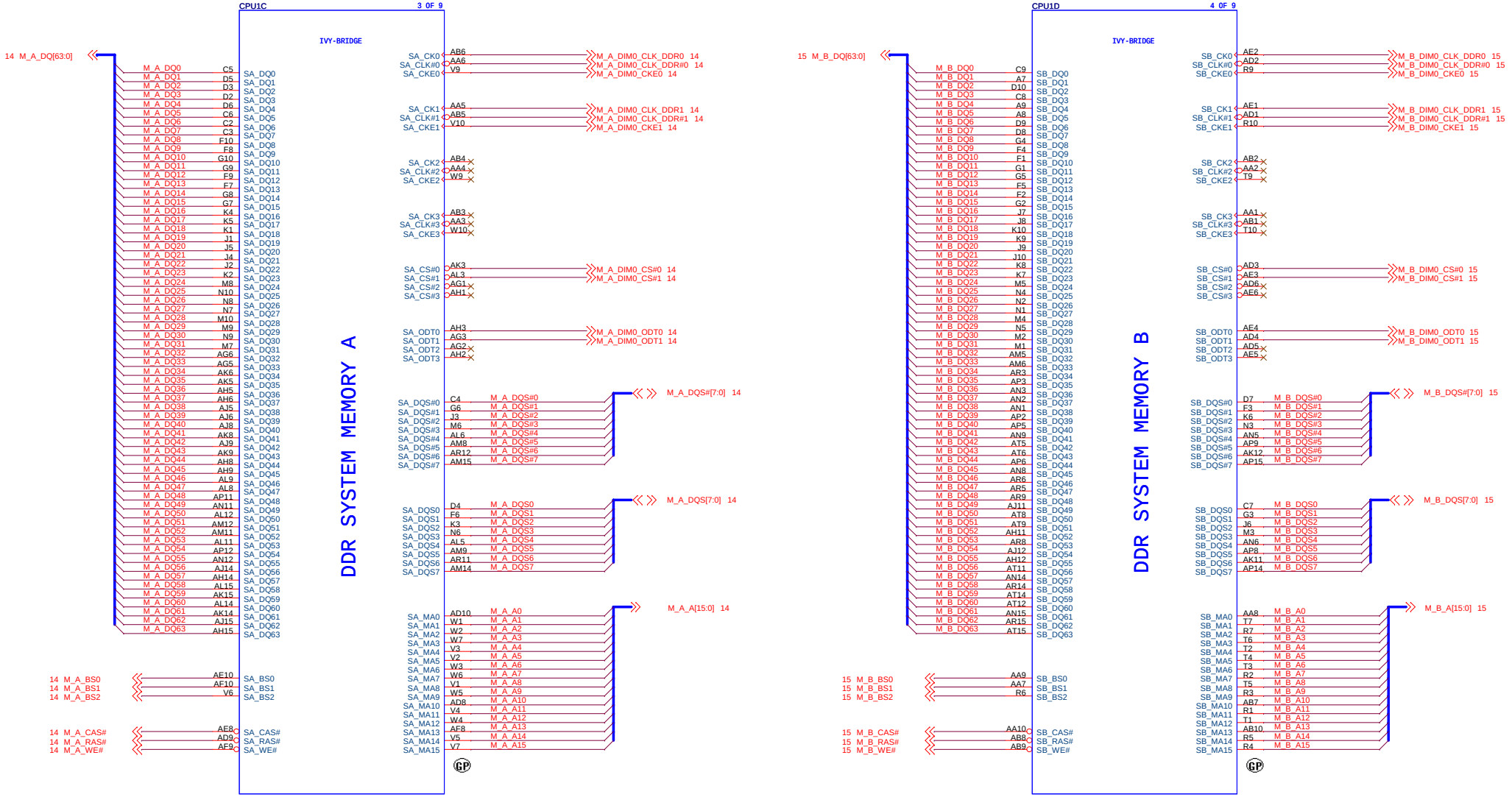
CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



<Core Design>

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Title: **CPU(3/7) : DDR3**

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CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

POWER

CPU1F — 6 OF 9 — IVY-BRIDGE

PROCESSOR CORE POWER

53A

VCC_CORE

Place Bottom

Place Top

C713 C722 C727 C736 C714 — SC22U6D3V5MX-2GP / SC10U6D3V3MX-GP

C735 C721 C726 C728 C723 — SC22U6D3V5MX-2GP / SC10U6D3V3MX-GP

C742 C701 C741 C703 C709 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-1GP / SC10U6D3V3MX-GP

C738 C702 C706 C707 C708 — SC10U6D3V5KX-1GP

C740 C739 C704 C712 C710 C711 — SC22U6D3V5MX-2GP

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

PROCESSOR UNCORE POWER

8.5A

1D05V_S0

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C729 C730 C731 C732 C715 C716 C717 C718 C733 C734 C719 C720 — SC10U6D3V3MX-GP / SC22U6D3V5MX-2GP

CORE SUPPLY

PEG AND DDR

SVID

VIDALERT# VIDSCLK VIDSOUT

H_CPU_SVIDALRT# H_CPU_SVIDCLK H_CPU_SVIDDAT

Route these three net together

R705 43R2J-GP — VR_SVID_ALERT# 42 / H_CPU_SVIDCLK 42 / H_CPU_SVIDDAT 42

R703 130R2F-1-GP — 1D05V_S0

SENSE LINES

reserve PAD for ESD

DY DY — 0R2J-2-GP — D701 D702

VCC_SENSE VSS_SENSE

VCCSENSE VSSSENSE — VCCSENSE 42 / VSSSENSE 42

PUT CLOSE CPU

R706 100R2F-L1-GP-U

R704 100R2F-L1-GP-U

VCCIO_SENSE VSS_SENSE_VCCIO

VTT_SENSE 45 / VSSP_SENSE 45

R707 R708 10R2F-L-GP — 1D05V_S0

PUT CLOSE CPU

Differential Sense feedback

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Title: CPU(4/7) : PWR

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CPU(5/7)

IVY BRIDGE PROCESSOR (GRAPHICS POWER)

33A

POWER

VCC_GFXCORE

Under Socket and Closed to CPU

C820 SC22U6D3V5MX-2GP, C821 SC22U6D3V5MX-2GP, C822 SC22U6D3V5MX-2GP, C823 SC10U6D3V5KX-1GP, C824 SC22U6D3V5MX-2GP, C825 SC22U6D3V5MX-2GP

VCC_GFXCORE

Closed to CPU Socket

C826 SC10U6D3V5KX-1GP, C827 SC22U6D3V5MX-2GP, C828 SC22U6D3V5MX-2GP, C829 SC22U6D3V5MX-2GP, C830 SC22U6D3V5MX-2GP, C831 SC22U6D3V5MX-2GP

CPU1G — IVY-BRIDGE — 7 OF 9

GRAPHICS: VAXG1–VAXG54 (AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17)

SENSE LINES: VAXG_SENSE (AK35), VSSAXG_SENSE (AK34)

R820 100R2F-L1-GP-U → VCC_GFXCORE

R819 100R2F-L1-GP-U

VCCGT_SENSE 42

VSSGT_SENSE 42

VCCGT_SENSE, VSSGT_SENSE

D801 0R2J-2-GP DY, D802 0R2J-2-GP DY

reserve PAD for ESD

M3 - Processor Generated SO-DIMM VREF_DQ

CAD Note: +V_SM_VREF should have 10 mil trace width

VREF: SM_VREF (AL1) +V_SM_VREF_CNT

B4:VREF_DQ CHA
D1:VREF_DQ CHB

SA_DIMM_VREFDQ (B4) DDR_VREF_S3_B4
SB_DIMM_VREFDQ (D1) DDR_VREF_S3_D1

R815 1KR2F-3-GP DY, R816 1KR2F-3-GP DY

C801 SC2D2U10V2ZY-2GP DY, C802 SC2D2U10V2ZY-1GP DY

14 M_VREF_DQ_DIMM0
15 M_VREF_DQ_DIMM1

DDR_VREF_S3_B4
DDR_VREF_S3_D1

Q802 AP2302GN-HF-GP, R810 0R2J-2-GP DY

Q803 AP2302GN-HF-GP, R814 0R2J-2-GP DY

5 PCH_DDR_EN#

PCH_DDR_EN#

1st = 84.05067.031
2nd = 84.00138.F31
3rd = 84.05067.031

20120112 PV-R

DDR3 -1.5V RAILS

VDDQ1 (AE7), VDDQ2 (AE4), VDDQ3 (AE1), VDDQ4 (AC7), VDDQ5 (AC4), VDDQ6 (AC1), VDDQ7 (Y7), VDDQ8 (Y4), VDDQ9 (Y1), VDDQ10 (U7), VDDQ11 (U4), VDDQ12 (U1), VDDQ13 (P7), VDDQ14 (P4), VDDQ15 (P1)

12~16A

1D5V_S0

C803 SC10U6D3V5MX-GP, C804 SC10U6D3V5KX-1GP, C805 SC10U6D3V5KX-1GP, C806 SC10U6D3V5KX-1GP, C807 SC10U6D3V5KX-1GP, C808 SC10U6D3V5KX-1GP

330U*1 10U*6

TC803 ST330U2D5VBM-1-GP

80.3371V.A2L

2nd = 77.22771.00L

20120131PVR

SA RAIL

VCCSA1 (M27), VCCSA2 (M26), VCCSA3 (L26), VCCSA4 (J26), VCCSA5 (J25), VCCSA6 (J24), VCCSA7 (H26), VCCSA8 (H25)

6A

VCCSA

C813 SC10U6D3V5KX-1GP, C814 SC10U6D3V5KX-1GP, C815 SC10U6D3V5KX-1GP

TC802 SF330U2D5VDM-1GP DY

1st = 77.23371.13L
2ND = 79.33719.L01

VCCSA

R0801 need be close to pin H23.

R801 100R2J-2-GP DY

VCCSA_SENSE (H23) VCCUSA_SENSE

VCCUSA_SENSE 48

1.5A

1D8V_S0

1.8V RAIL

VCCPLL1 (B6), VCCPLL2 (A6), VCCPLL3 (A2)

C819 SC10U6D3V5KX-1GP DY, C816 SC10U6D3V5KX-1GP, C817 SC1U10V2KX-1GP, C818 SC1U10V2KX-1GP

MISC

VCCSA_VID0 (C22), VCCSA_VID1 (C24)

H_FC_C22

VCCSA_SEL

H_FC_C22 48
VCCSA_SEL 48

R804 1KR2J-1-GP, R806 1KR2J-1-GP

VCCIO_SEL (A19) H_VCCP_SEL

SNB: No Connect
IVB: VSS

R817 0R2J-2-GP DY → H_SNB_IVB#_PWRCTRL 45

R818 0R2J-2-GP DY

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

S3 Power Reduction Circuit Processor VREF_DQ Implementation

1D5V_S3

R821 1KR2F-3-GP DY

R822 1KR2F-3-GP DY

DDR_VREF_S3 — 20120112 PV-R

R807 0R0402-PAD

R811 0R2J-2-GP DY

Q801 DMN5L06K-7-GP

+V_SM_VREF — 84.05067.031
1st = 84.2N702.J31
2ND = 84.07002.I31
3rd = 84.2N702.W31

+V_SM_VREF_CNT

R803 100KR2J-1-GP

R802 0R2J-2-GP DY

5 PCH_DDR_EN#

20120112 PV-R R823 0R0402-PAD

C832 SC470P50V2KX-3GP

19,27,29,34,35,36,37,45,46,47,48,92,93 PM_SLP_S3#

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

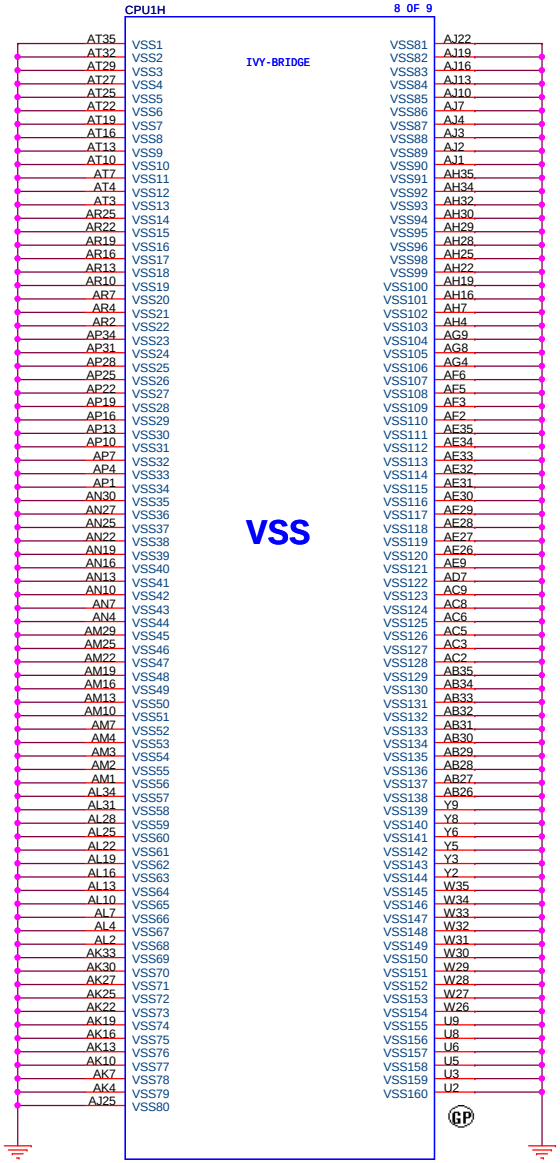
Title: CPU(5/7) : GFX/PWR

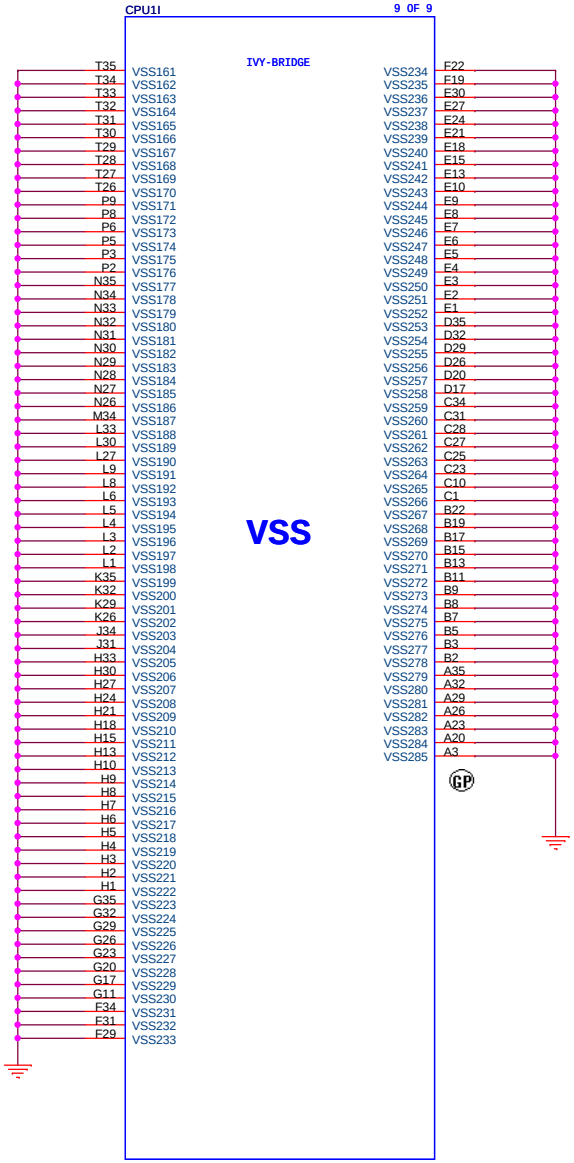
Size: Custom | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 8 of 103

CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(6/7) : GND

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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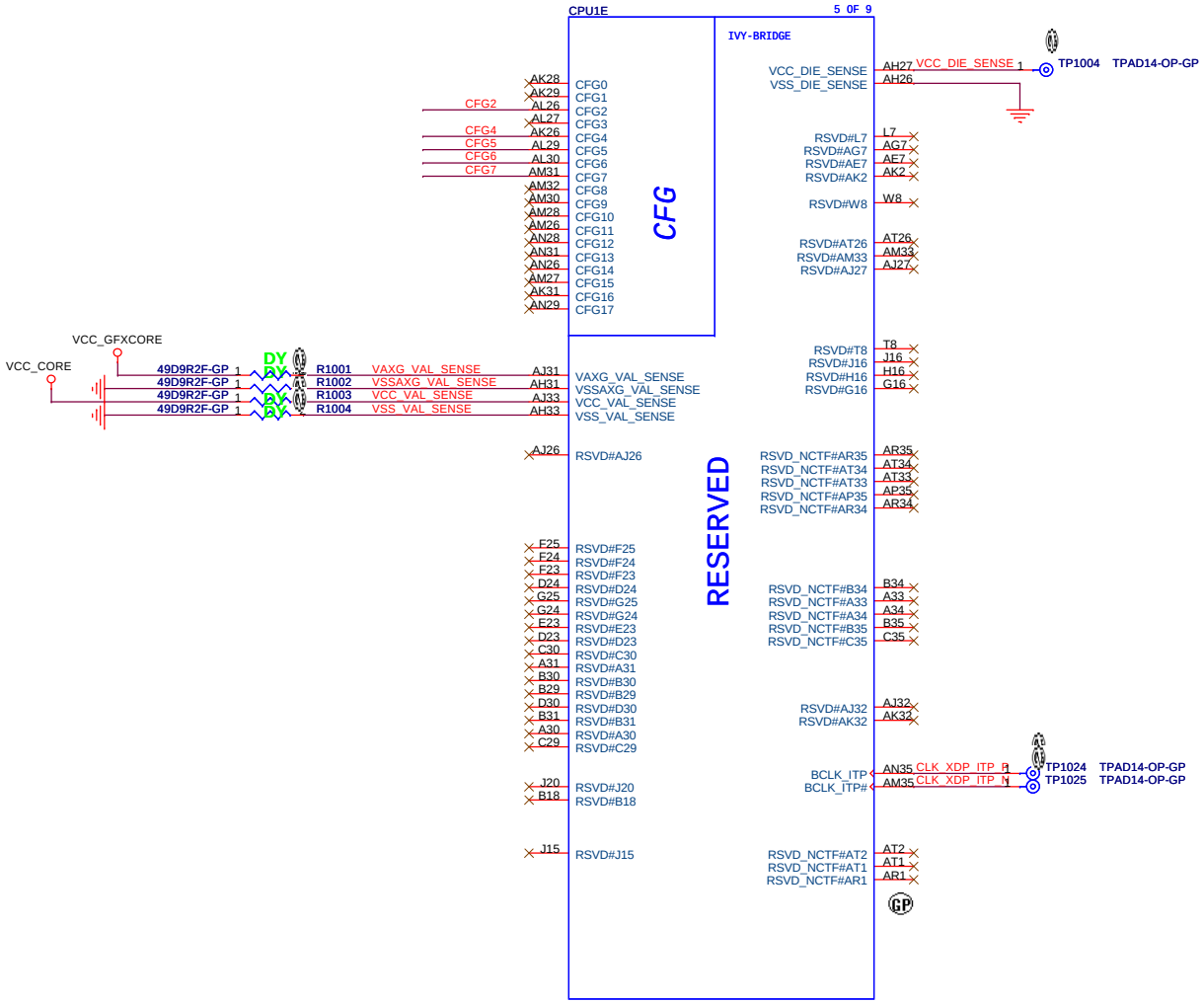
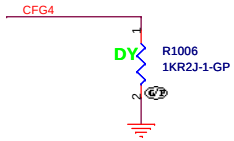
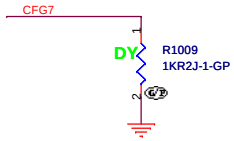
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

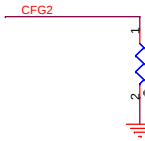




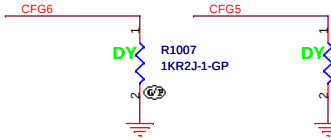
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

<Core Design>

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Title: CPU(7/7): CFG/RSVD/DDR3_VREF

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 10 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CPU XDP

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 11 of 103

(Blanking)

<Core Design>

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Title: ***RESERVED***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 12 of 103

(Blanking)

<Core Design>

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Title: ***RESERVED***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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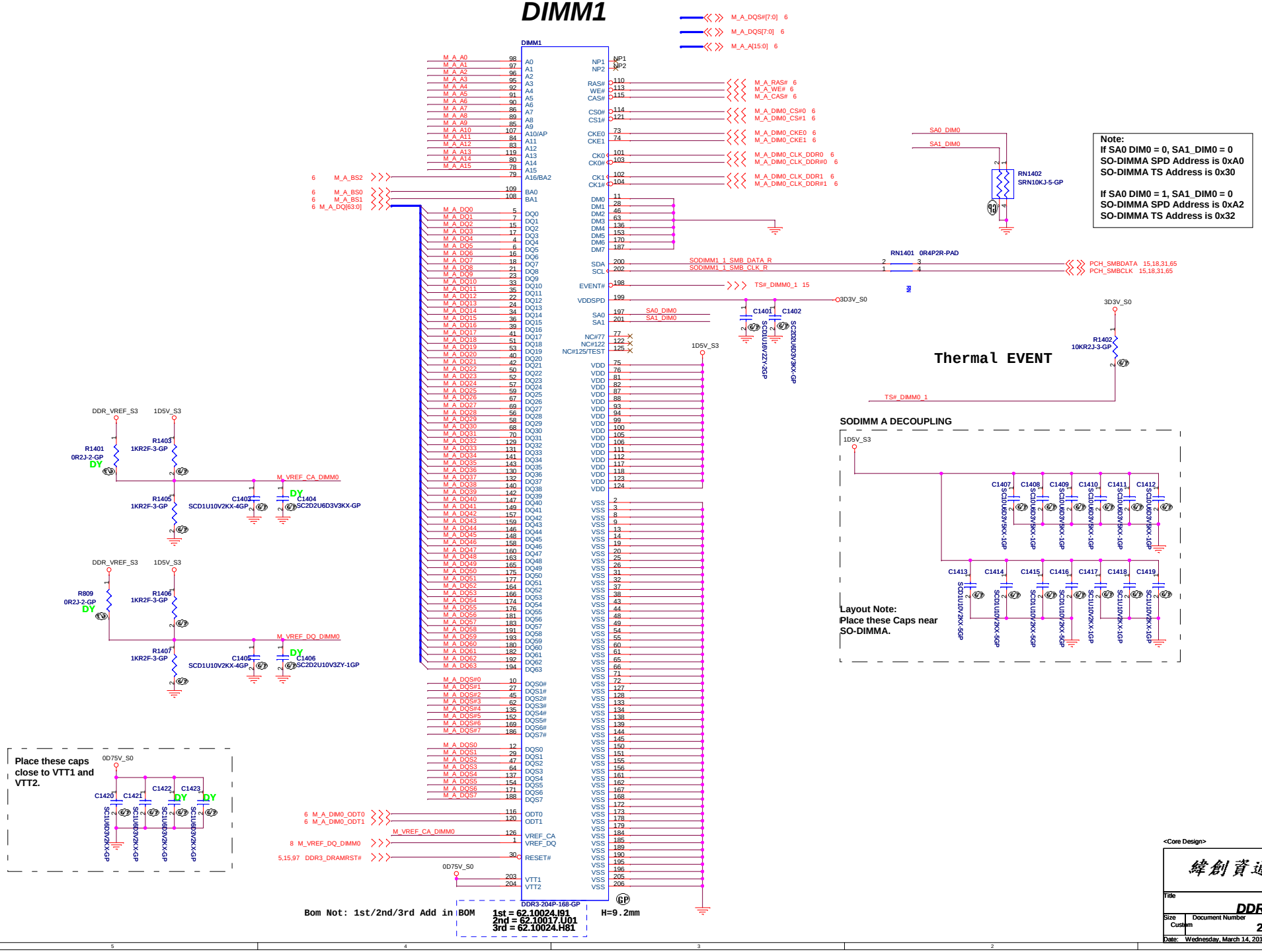
DIMM1



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM1

Size	Document Number	Rev
Custom	2012 S-Series Richie 13.3	-1

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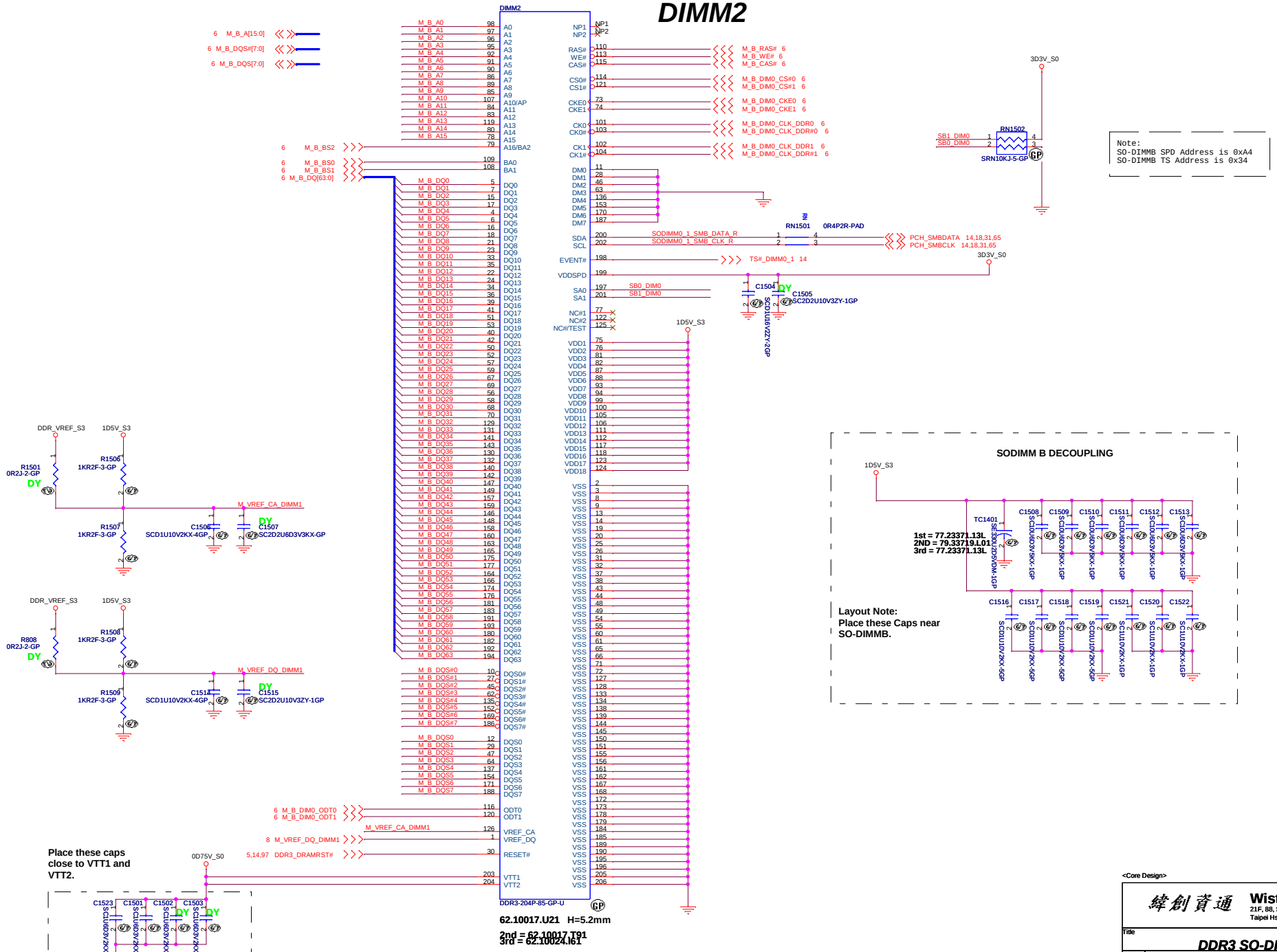
DIMM2



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SODIMM B DECOUPLING

1st = 77.23371.13L
2ND = 79.33719.L01
3rd = 77.23371.13L

Layout Note:
Place these Caps near SO-DIMMB.

62.10017.U21 H=5.2mm
2nd = 62.10017.T91
3rd = 62.10024.161

<Core Design>

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Title: DDR3 SO-DIMM2

Size: Custom | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 15 of 103

(Blanking)

<Core Design>

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Title: ***RESERVED***

Size	Document Number	Rev
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PCH(1/9)

INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — PANTHER-GP-NF

RTC: RTC_X1, RTC_X2, RTC_RST#, SRTC_RST#, INTRUDER#, INTVRMEN
LPC: LPC_AD[3:0] 27,71; FWH0/LAD0 C38 LPC_AD0; FWH1/LAD1 A38 LPC_AD1; FWH2/LAD2 B37 LPC_AD2; FWH3/LAD3 C37 LPC_AD3; FWH4/LFRAME# D36 LPC_FRAME# R 1 R1726 22R2J-2-GP LPC_FRAME# 27,71; LDRQ0# E36; LDRQ1#/GPIO23 K36 PCH_GPIO23 1 TP1701 TPAD14-OP-GP; SERIRQ V5 SIRQ 27,71
IHDA: HDA_BIT_CLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SYNC_C, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32
JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3
SATA 6G: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5; SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10; SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4; SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1; SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1; SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1
SATA: SATAICOMPO Y11, SATAICOMPI Y10 SATA_COMP R1713 1 2 37D4R2F-GP 1D05V_S0; SATA3RCOMPO AB12, SATA3COMPI AB13 SATA3_COMP R1714 1 2 49D9R2F-GP 1D05V_S0; SATA3RBIAS AH1 RBIAS_SATA3 1 R1715 750R2F-GP 3D3V_S0; NEED TO PLACE CLOSE TO PCH; SATALED# P3 SATA_LED# R1716 10KR2J-3-GP SATA_LED# 68; SATA0GP/GPIO21 V14 SATA0GP_GPIO21 22; SATA1GP/GPIO19 P1 SATA_ODD_DET# 56

HDD: SATA_RXN0 56, SATA_RXP0 56, SATA_TXN0 56, SATA_TXP0 56
ODD: SATA_RXN1 56, SATA_RXP1 56, SATA_TXN1 56, SATA_TXP1 56

X1701 X-32D768KHZ-34GPU; C1702 C1703 7pF20PPM SC68P50V2CN-1GP; 82.20312MV; 82.30001.661; 2ND = 82.30001.B21
R1706 10MR2J-L-GP; R1705 20KR2J-L2-GP; C1701 SC1U10V2KX-1GP; R1707 DY 330KR2J-L1-GP PCH_INTVRMEN
R1708 20KR2J-L2-GP; C1704 SC1U10V2KX-1GP; G1701 GAP-OPEN
R1709 1MR2J-1-GP; R1710 330KR2J-L1-GP PCH_INTVRMEN; RN1701 SRN33J-7-GP
R1711 0R0402-PAD; 20120112 PV-R
R1725 1KR2J-1-GP; R1712 1KR2J-1-GP HDD_HALTLED_R; 68 HDD_HALTLED
R1701 10KR2J-3-GP; 27,82 BAT_GRNLED#; BAT_GRNLED# G; Q1701 BSS84-7-F-GP; 84.00084.F31; 2nd = 84.BSS84.B31
R1702 10KR2J-3-GP; PLT_RST# G; Q1702 BSS84-7-F-GP; 84.00084.F31; 2nd = 84.BSS84.B31
R1724 1KR2J-1-GP HDA_SYNC; R1729 10KR2J-3-GP ISO_PREP#

For Flash Descriptor Security Override HW strap

RTC Battery

RTC1 BAT-060003HA02M213ZL-GP-U; 62.70014.001; 2nd = 62.70001.061
+RTC_VCC; R1720; RTC_PWR 1 1KR2J-1-GP
U1701 CH715FGP-GP-U; C1705 SC1U10V3ZY-6GP
83.R0304.D81; 2ND = 83.00040.E81; 20120210PV-R
20120314 MV; 20120315 MV

NO REBOOT STRAP

No Reboot Strap R710	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S0 R1722 10KR2J-3-GP HDA_SPKR DY; R1723 10KR2J-3-GP SIRQ

5V_S0 RN1702 SRN10KJ-5-GP; HDA_SDO_G; U1704 2N7002KDW-GP; HDA_SYNC_C; HDA_SYNC; HDA_SDO; HDA_SDO_R
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

PCHXDP R1717 210R2F-L-GP PCH_JTAG_TMS; R1718 210R2F-L-GP PCH_JTAG_TDO; R1719 210R2F-L-GP PCH_JTAG_TDI
RN1703 SRN100J-4-GP: PCH_JTAG_TDO, PCH_JTAG_TDI, PCH_JTAG_TMS
R1721 51R2J-2-GP PCH_JTAG_TCK_BUF; R1727 DY 1KR2J-1-GP HDD_HALTLED_R; R1728 20KR2J-L2-GP HDA_SDO

LAYOUT NOTE:
JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: PCH(1/9) : HDA/JTAG/SATA
Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
Date: Wednesday, March 14, 2012 | Sheet 17 of 103

PCH(2/9)

PCH1B

2 OF 10

PANTHER-GP-NF

PCI-E*

BG34	PERN1		
BJ34	PERP1		
AV32	PETN1		
AU32	PETP1		
BE34	PERN2		
BF34	PERP2		
BB32	PETN2		
AY32	PETP2		
BG36	PERN3		
BJ36	PERP3		
AV34	PETN3		
AU34	PETP3		
BF36	PERN4		
BE36	PERP4		
AY34	PETN4		
BB34	PETP4		
BG37	PERN5		
BH37	PERP5		
AY36	PETN5		
BB36	PETP5		
BJ38	PERN6		
BG38	PERP6		
AU36	PETN6		
AV36	PETP6		
BG40	PERN7		
BJ40	PERP7		
AY40	PETN7		
BB40	PETP7		
BE38	PERN8		
BC38	PERP8		
AW38	PETN8		
AY38	PETP8		

Media

32 PCIE_RXN3_MEDIA
32 PCIE_RXP3_MEDIA
32 PCIE_TXN3_MEDIA
32 PCIE_TXP3_MEDIA

C1805 1 — SCD1U10V2KX-5GP — PCIE_TXN3_C
C1806 1 — SCD1U10V2KX-5GP — PCIE_TXP3_C

WLAN

53 PCIE_RXN4_WLAN
53 PCIE_RXP4_WLAN
53 PCIE_TXN4_WLAN
53 PCIE_TXP4_WLAN

C1809 1 — SCD1U10V2KX-5GP — PCIE_TXN4_C
C1807 1 — SCD1U10V2KX-5GP — PCIE_TXP4_C

LAN

34 PCIE_RXN6_LAN
34 PCIE_RXP6_LAN
34 PCIE_TXN6_LAN
34 PCIE_TXP6_LAN

C1810 1 — SCD1U10V2KX-5GP — PCIE_TXN6_C
C1811 1 — SCD1U10V2KX-5GP — PCIE_TXP6_C

SMBUS

SMBALERT#/GPIO11	E12	FPR_OFF 64,97
SMBCLK	H14	PCH_SMB_CLK
SMBDATA	C9	PCH_SMB_DATA
SML0ALERT#/GPIO60	A12	PCH_DDR_RST# 5
SML0CLK	C8	PCH_SML0_CLK
SML0DATA	G12	PCH_SML0_DATA
SML1ALERT#/PCHHOT#/GPIO74	C13	PCH_GPIO74
SML1CLK/GPIO58	E14	PCH_SML1CLK
SML1DATA/GPIO75	M16	PCH_SML1DATA

R1806 10KR2J-3-GP — 3D3V_S5
R1807 1KR2J-1-GP — 3D3V_S5

RN1803 SRN2K2J-1-GP — 3D3V_S0

U1801 2N7002KDW-GP
14,15,31,65 PCH_SMBDATA — PCH_SMB_DATA
PCH_SMB_CLK — PCH_SMBCLK 14,15,31,65

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

Controller Link

CL_CLK1	M7	
CL_DATA1	T11	
CL_RST1#	P10	

R1801 10KR2J-3-GP — 3D3V_S5

84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
2N7002K-2-GP

DIS_PX
PE_PWRGD 22,86,92,93,96,97

Q1801

3D3V_AUX_S5 — 3D3V_S5

RN1802 SRN2K2J-4-GP

PCH_SML1DATA
PCH_SML1CLK

U1802 2N7002KDW-GP
PCH_KBC_DATA 27,28,85
PCH_KBC_CLK 27,28,85

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

CLOCKS

CLKOUT_PCIE0N	Y40	
CLKOUT_PCIE0P	Y39	
PCIECLKRQ0#/GPIO73	J2	GPIO73
CLKOUT_PCIE1N	AB49	
CLKOUT_PCIE1P	AB47	
PCIECLKRQ1#/GPIO18	M1	GPIO18
CLKOUT_PCIE2N	AA48	
CLKOUT_PCIE2P	AA47	
PCIECLKRQ2#/GPIO20	V10	GPIO20
CLKOUT_PCIE3N	Y37	
CLKOUT_PCIE3P	Y36	
PCIECLKRQ3#/GPIO25	A8	
CLKOUT_PCIE4N	Y43	
CLKOUT_PCIE4P	Y45	
PCIECLKRQ4#/GPIO26	L12	
CLKOUT_PCIE5N	V45	
CLKOUT_PCIE5P	V46	
PCIECLKRQ5#/GPIO44	L14	GPIO44
CLKOUT_PEG_B_N	AB42	
CLKOUT_PEG_B_P	AB40	
PEG_B_CLKRQ#/GPIO56	E6	GPIO56
CLKOUT_PCIE6N	V40	
CLKOUT_PCIE6P	V42	
PCIECLKRQ6#/GPIO45	T13	
CLKOUT_PCIE7N	V38	
CLKOUT_PCIE7P	V37	
PCIECLKRQ7#/GPIO46	K12	CLKRQ_WWAN#
CLKOUT_ITPXDP_N	AK14	
CLKOUT_ITPXDP_P	AK13	

20120212 MV
20120112 PV-R
R1804 0R2J-2-GP
54 WWAN_DET# — GPIO18

Media

32 CLK_PCIE_MEDIA#
32 CLK_PCIE_MEDIA
32 CLKREQ_MEDIA#

WLAN

53 CLK_PCIE_WLAN#
53 CLK_PCIE_WLAN
53 CLKRQ_WLAN#

LAN

34 CLK_PCIE_LAN#
34 CLK_PCIE_LAN
34 CLKREQ_LAN#

TPAD14-OP-GP P1805 — PCIE_CLK_XDP_N
TPAD14-OP-GP P1806 — PCIE_CLK_XDP_P

PEG_A_CLKRQ#/GPIO47	M10	CLKREQ_PEG_A#
CLKOUT_PEG_A_N	AB37	CLKOUT_PEG_A_N
CLKOUT_PEG_A_P	AB38	CLKOUT_PEG_A_P
CLKOUT_DMI_N	AV22	CLKOUT_DMI_N 5
CLKOUT_DMI_P	AU22	CLKOUT_DMI_P 5
CLKOUT_DP_N	AM12	
CLKOUT_DP_P	AM13	
CLKIN_DMI_N	BF18	CLK_BUF_EXP_N
CLKIN_DMI_P	BE18	CLK_BUF_EXP_P
CLKIN_GND1_N	BJ30	CLK_BUF_CPYCLK_N
CLKIN_GND1_P	BG30	CLK_BUF_CPYCLK_P
CLKIN_DOT_96N	G24	CLK_BUF_DOT96_N
CLKIN_DOT_96P	E24	CLK_BUF_DOT96_P
CLKIN_SATA_N	AK7	CLK_BUF_CKSSCD_N
CLKIN_SATA_P	AK5	CLK_BUF_CKSSCD_P
REFCLK14IN	K45	CLK_BUF_REF14
CLKIN_PCILOOPBACK	H45	
XTAL25_IN	V47	XTAL25_IN
XTAL25_OUT	V49	XTAL25_OUT
XCLK_RCOMP	Y47	XCLK_RCOMP

RN1810 0R4P2R-PAD — 20120116PV-R
CLK_PCIE_VGA# 83
CLK_PCIE_VGA 83

CLOCK TERMINATION FOR FCIM

RN1806 SRN10KJ-5-GP
RN1807 SRN10KJ-5-GP
RN1808 SRN10KJ-5-GP
RN1809 SRN10KJ-5-GP

R1802 10KR2J-3-GP

All resistors need very close to PCH

CLK_PCI_FB 21

R1803 90D9R2F-1-GP — 1D05V_S0

RN1801 SRN2K2J-4-GP — 3D3V_S5
PCH_SML0_DATA
PCH_SML0_CLK
PCH_SMB_CLK
PCH_SMB_DATA

FLEX CLOCKS

CLKOUTFLEX0/GPIO64	K43	CLK_48_USB30
CLKOUTFLEX1/GPIO65	F47	CLK_27_NSSC
CLKOUTFLEX2/GPIO66	H47	CLK_48_KBC_PCH_SIO
CLKOUTFLEX3/GPIO67	K49	CLK_14M_KBC_P

TP1801 TPAD14-OP-GP
TP1802 TPAD14-OP-GP
TP1803 TPAD14-OP-GP
TP1804 TPAD14-OP-GP
<Core Design>

RN1804 SRN10KJ-L3-GP
CLKREQ_LAN# — CLKRQ_WLAN#
PCH_GPIO74 — GPIO56
GPIO44 — CLKREQ_MEDIA#
CLKRQ_WWAN# — GPIO73
3D3V_S5

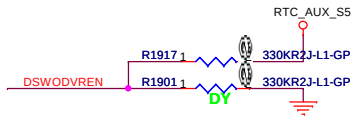
RN1805 SRN10KJ-5-GP
3D3V_S0
GPIO18
GPIO20

XTAL25_IN — XTAL25_OUT
R1805 1MR2J-1-GP
X1801 XTAL-25MHZ-155-GP
82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61
C1801 SC15P50V2JN-2-GP
C1802 SC18P50V2JN-1-GP

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH : PCI/USB/NVRAM/RSVD
Size A3	Document Number 2012 S-Series Richie 13.3
Rev -1	
Date: Wednesday, March 14, 2012	Sheet 18 of 103

PCH(3/9)

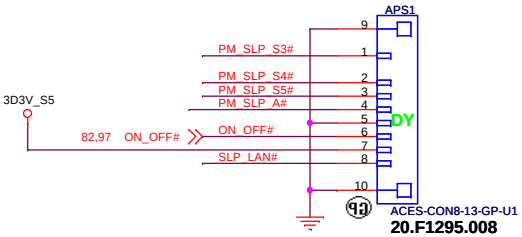
DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1901 STUFFED, R1917 UNSTUFFED	Disabled



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

AMT/ME COMPLIANCY TEST CONN.



<Core Design>

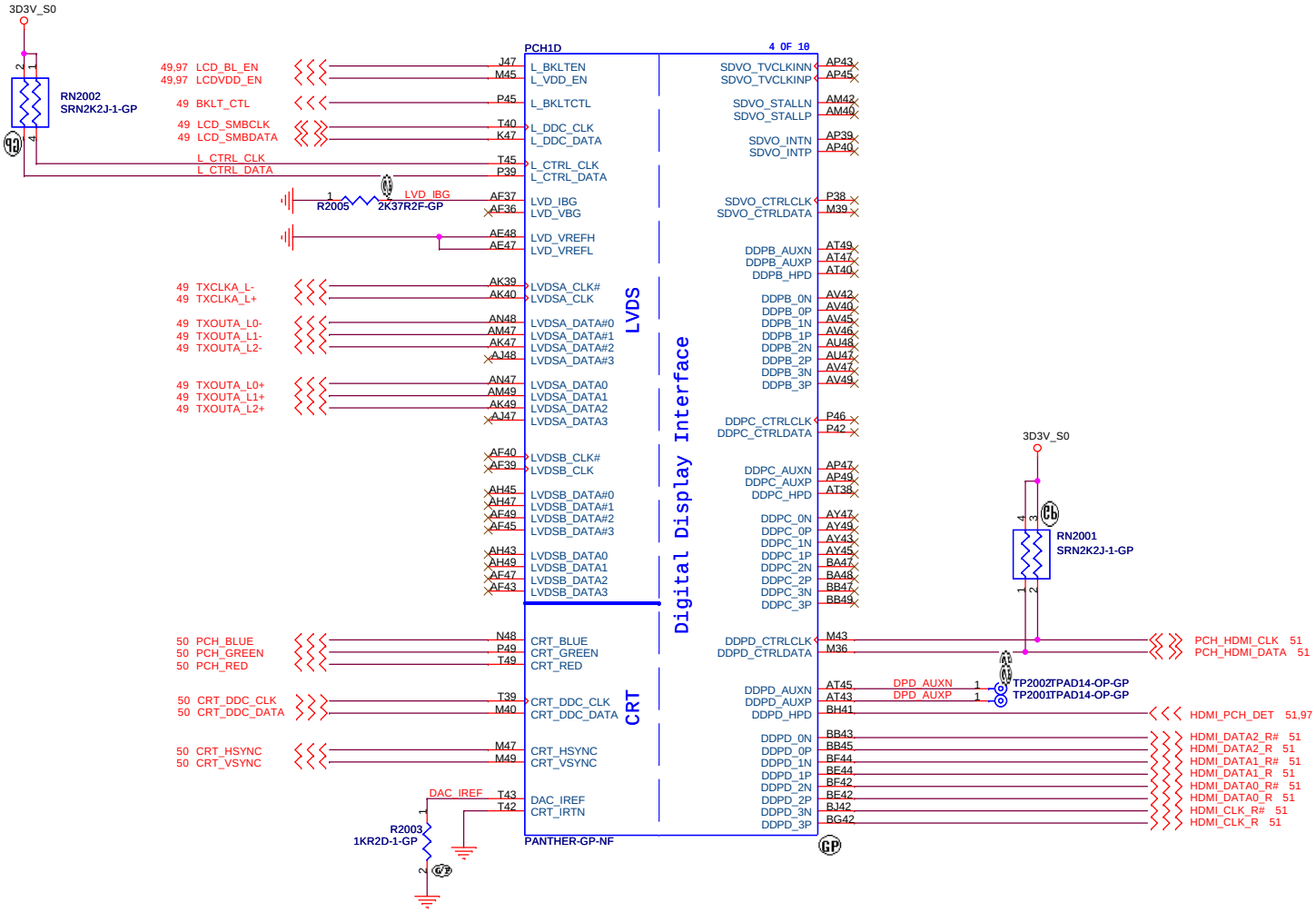
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(3/9) : DMI/FDI/PM

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 19 of 103

PCH(4/9)



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH(4/9) : LVDS/CRT/DDI**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 20 of 103

PCH(5/9)

GPIO Table

S 2012 Chief River	PCH GPIO 52
Richie U&D (13 inches)	1
Rocky U&D (14 inches)	1
Rocky U&D (15/17 inches)	0

Boot BIOS Strap

GNT1#/GPIO51	SATA1GP#/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

USB2.0 Table

USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

PCH1E 5 OF 10

RSVD: TP1–TP24

USB3RN1–USB3RN4, USB3RP1–USB3RP4, USB3TN1–USB3TN4, USB3TP1–USB3TP4

USBP0N–USBP13P

PCI: PIRQA#–PIRQD#, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#

CLKOUT_PCI0–CLKOUT_PCI4

OC0#/GPIO59–OC7#/GPIO14

PANTHER-GP-NF

USB 3.0 Conn. 1
USB 3.0 Conn. 2
USB 3.0 Conn. 3
BT WLAN combo
Fingerprint
USB 2.0 Conn. 1
Camera
WWAN

20120112 PV-R

AND GATE U2101 U74LVC1G08G-AL5-R-GP-U

73.01G08.EHG
2nd = 73.7SZ08.EAH
3rd = 73.01G08.L04

RN2104 SRN10KJ-6-GP

RN2103 SRN10KJ-6-GP

<Core Design>

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Title: PCH(5/9) : PCI/USB/NVM

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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PCH(6/9)

VRAM ID TABLE

PCH_GPIO39	PCH_GPIO38	VENDER
0	1	Samsung
1	0	Hynix
1	1	Elpida
0	0	UMA

GDDR5/DDR3 TABLE

20110822SI

2012 Chief River	PCH GPIO 12
Richie U&D (13 inches)	0 (13") GDDR5
Rocky U&D (14 inches)	1(14",15",17")DDR3
Rocky U&D (15/17 inches)	1(14",15",17")DDR3

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

PROC_SELECT	
DF_TVS	SNB: "1" IVB: "0"

DMI & FDI Termination Voltage

<Core Design>

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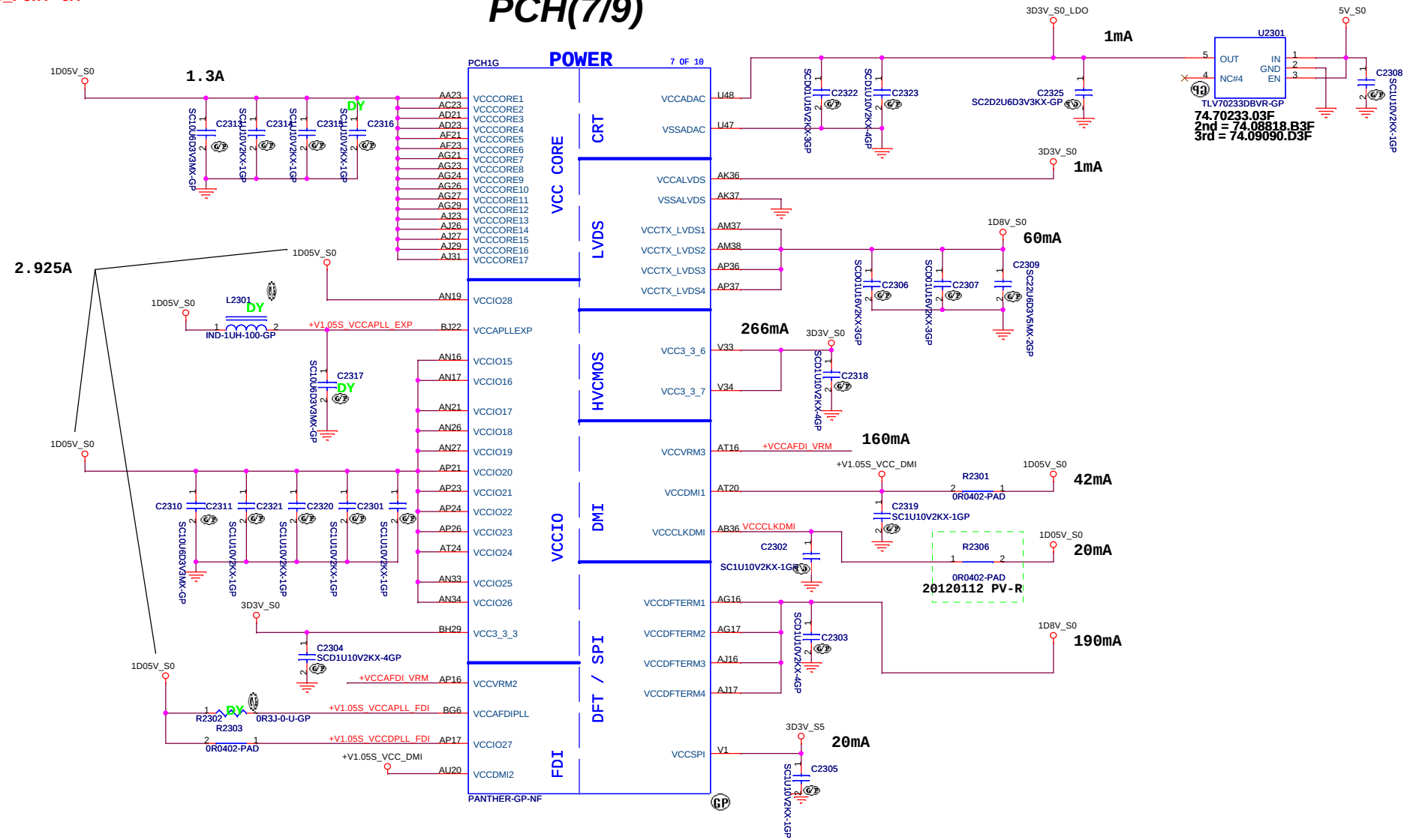
Title: PCH(6/9) : GPIO/NTCF/RSVD

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 22 of 103

VCC_PCH: 6A

PCH(7/9)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(7/9) : PWR1

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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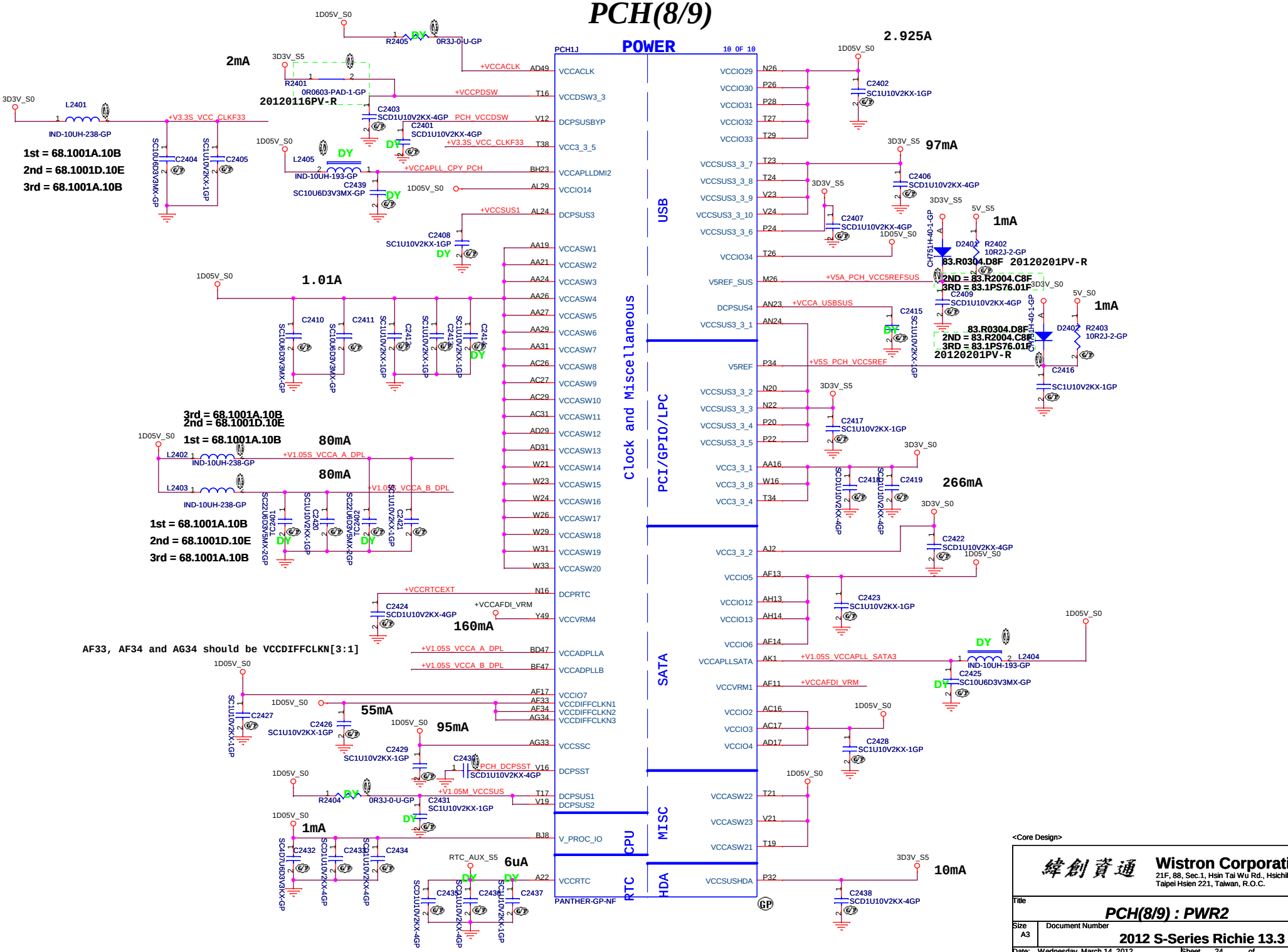
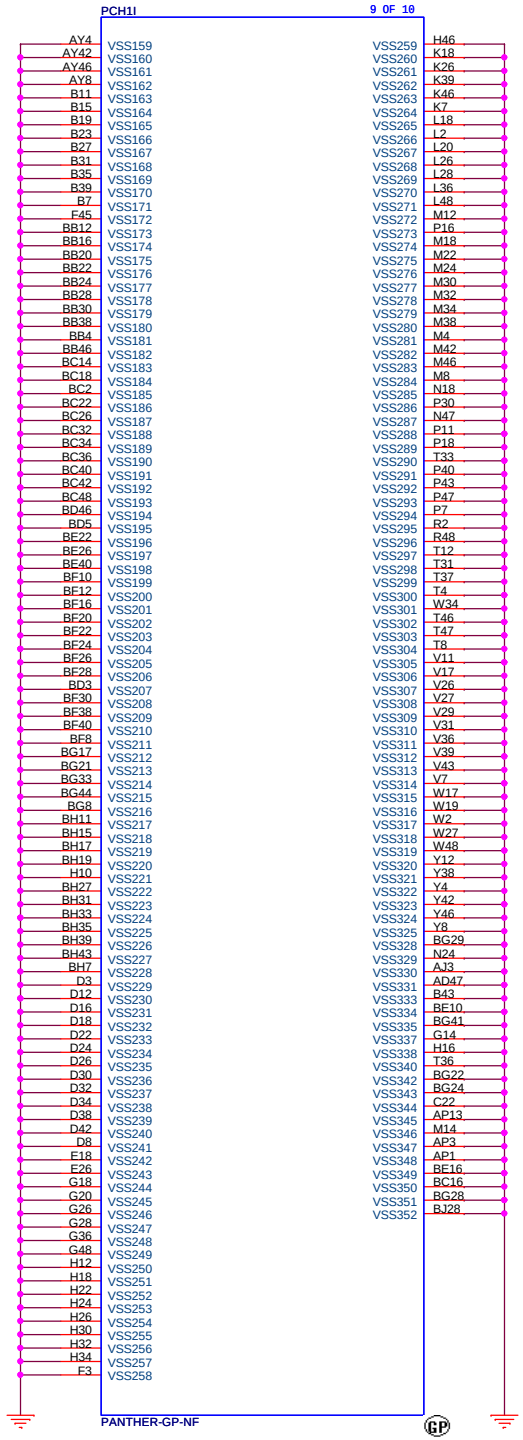
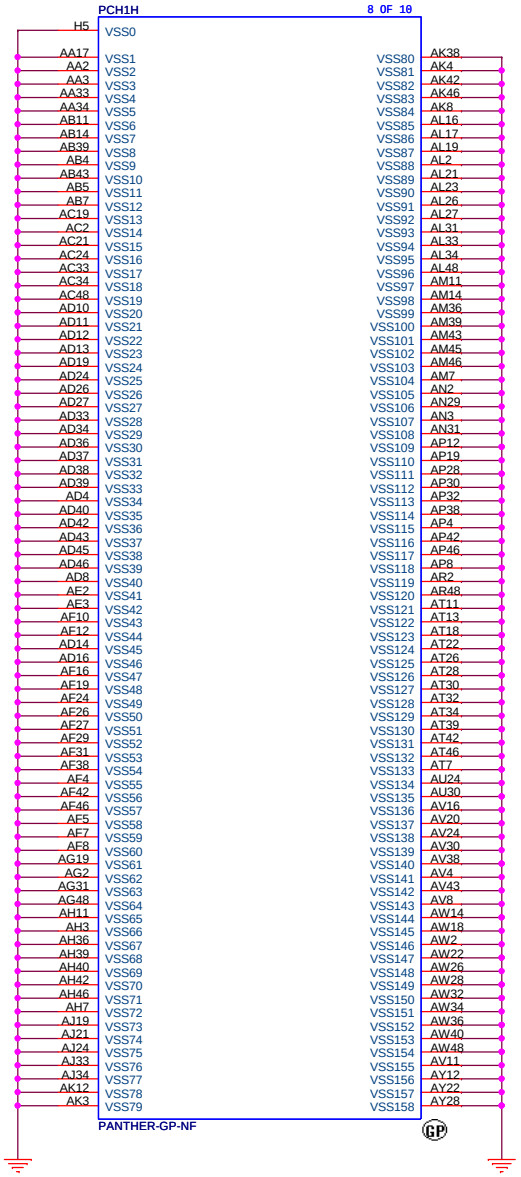
PCH(8/9)


POWER
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
PCH1J
PANTHER-GP-NF
10 OF 10
2mA
2.925A
97mA
1mA
1.01A
80mA
266mA
160mA
55mA
95mA
6uA
10mA
20120116PV-R
20120201PV-R
1st = 68.1001A.10B
2nd = 68.1001D.10E
3rd = 68.1001A.10B
AF33, AF34 and AG34 should be VCCDIFFCLKN[3:1]
+VCCACLK
+VCCPDSW
PCH_VCCDSW
+V3.3S_VCC_CLKF33
+VCCAPLL_CPY_PCH
+VCCSUS1
+V5A_PCH_VCC5REFSUS
+V5S_PCH_VCC5REF
+VCCA_USBSUS
+V1.05S_VCCA_A_DPL
+V1.05S_VCCA_B_DPL
+VCCRTCEXT
+VCCAFDI_VRM
+V1.05S_VCCAPLL_SATA3
PCH_DCPSST
+V1.05M_VCCSUS
RTC_AUX_S5
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH(8/9) : PWR2
Size A3
Document Number 2012 S-Series Richie 13.3
Rev -1
Date: Wednesday, March 14, 2012
Sheet 24 of 103

PCH(9/9)





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(9/9) : GND

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(Blanking)

<Core Design>

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Title: PCH XDP

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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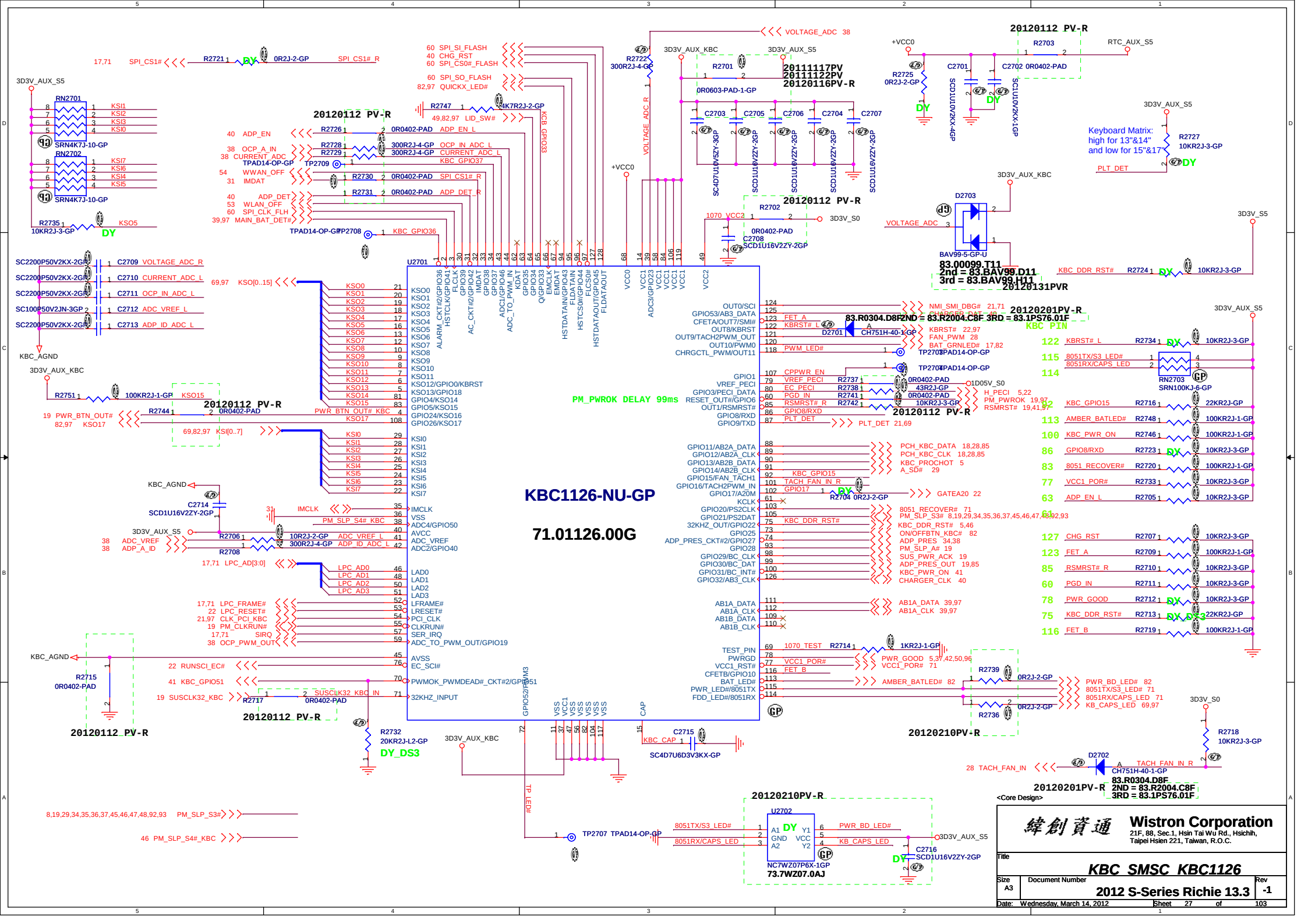
KBC1126-NU-GP
71.01126.00G
PM_PWROK DELAY 99ms
U2701
20120112 PV-R
20120131PVR
20120201PV-R
20120210PV-R
20111117PV
20111122PV
20120116PV-R
83.00099.T11
2nd = 83.BAV99.D11
3rd = 83.BAV99.H11
BAV99-5-GP-U
83.R0304.D8F
2ND = 83.R2004.C8F
3RD = 83.1PS76.01F
CH751H-40-1-GP
KBC PIN
Keyboard Matrix:
high for 13"&14"
and low for 15"&17"
NC7WZ07P6X-1GP
73.7WZ07.0AJ
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_SMSC_KBC1126
2012 S-Series Richie 13.3
Wednesday, March 14, 2012
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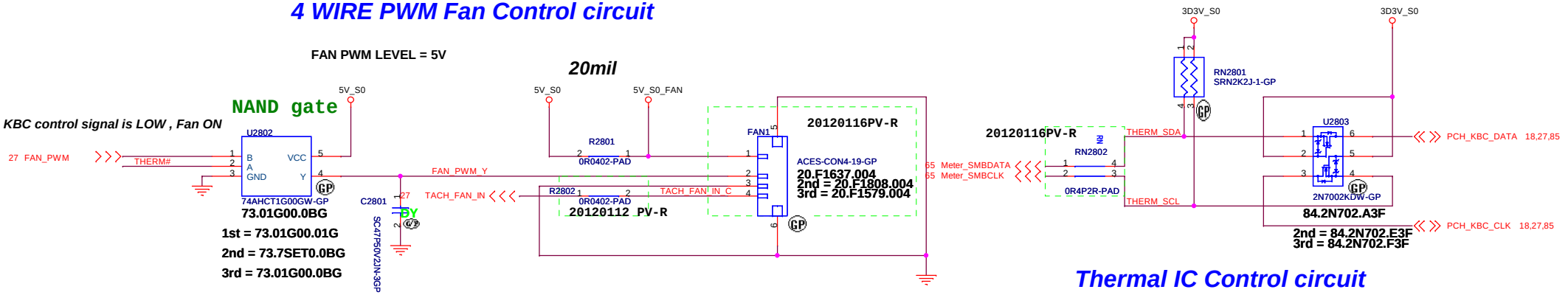
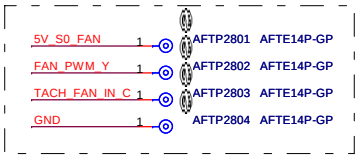
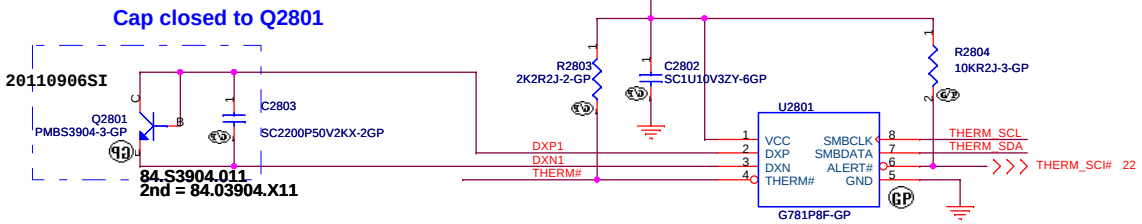
4 WIRE PWM Fan Control circuit



A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

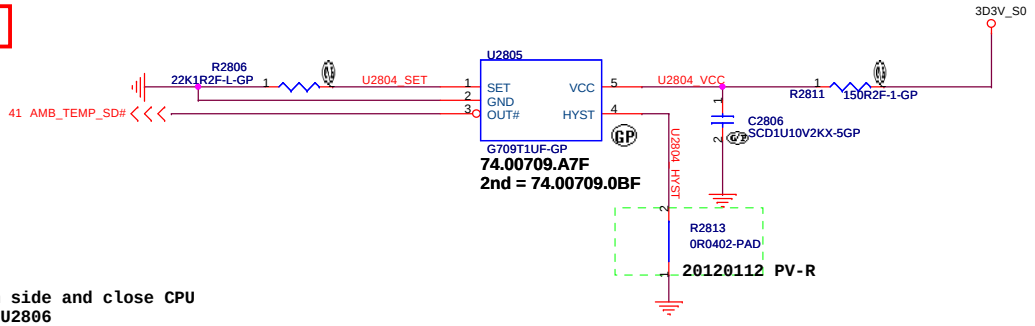


Thermal IC Control circuit



T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



Layout: PUT U2805 Bottom side and close CPU
PUT R2806 Close U2806

<Core Design>

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Title: Thermal G781 / FAN

Size	Document Number	Rev
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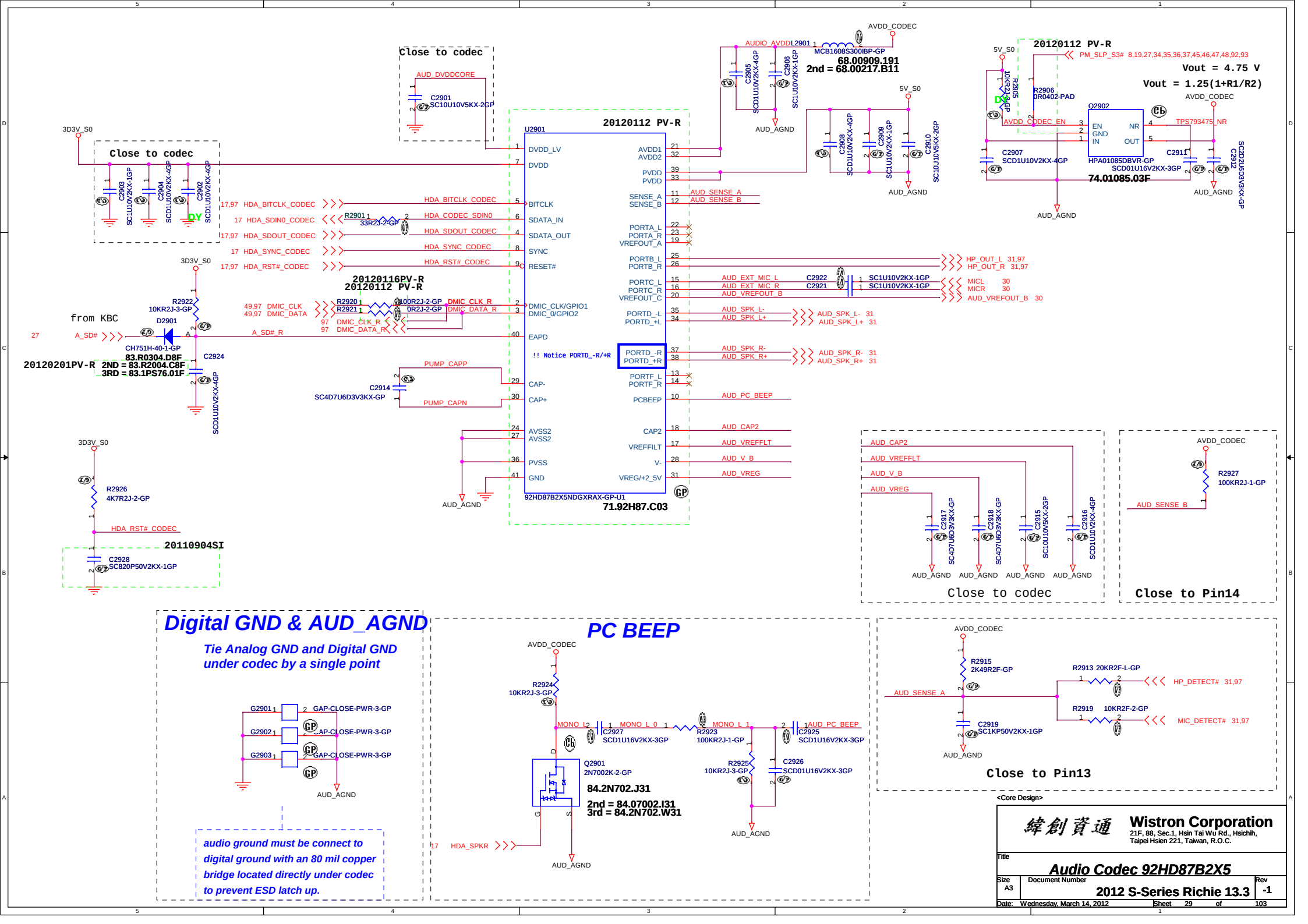
Close to codec
AUD_DVDDCORE
C2901
SC10U10V5KX-2GP
20120112 PV-R
U2901
DVDD_LV
DVDD
BITCLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
DMIC_CLK/GPIO1
DMIC_0/GPIO2
EAPD
!! Notice PORTD_-R/+R
CAP-
CAP+
AVSS2
AVSS2
PVSS
GND
AVDD1
AVDD2
PVDD
PVDD
SENSE_A
SENSE_B
PORTA_L
PORTA_R
VREFOUT_A
PORTB_L
PORTB_R
PORTC_L
PORTC_R
VREFOUT_C
PORTD_-L
PORTD_+L
PORTD_-R
PORTD_+R
PORTF_L
PORTF_R
PCBEEP
CAP2
VREFFILT
V-
VREG/+2_5V
92HD87B2X5NDGXRAX-GP-U1
71.92H87.C03
AVDD_CODEC
AUDIO_AVDD
L2901
MCB1608S300IBP-GP
68.00909.191
2nd = 68.00217.B11
AUD_AGND
5V_S0
3D3V_S0
HDA_BITCLK_CODEC
HDA_CODEC_SDIN0
HDA_SDOUT_CODEC
HDA_SYNC_CODEC
HDA_RST#_CODEC
R2901
33R2J-2-GP
20120116PV-R
20120112 PV-R
R2920
100R2J-2-GP
R2921
0R2J-2-GP
DMIC_CLK_R
DMIC_DATA_R
from KBC
A_SD#
A_SD#_R
D2901
CH751H-40-1-GP
83.R0304.D8F
20120201PV-R
2ND = 83.R2004.C8F
3RD = 83.1PS76.01F
R2922
10KR2J-3-GP
C2924
SCD1U10V2KX-4GP
PUMP_CAPP
PUMP_CAPN
C2914
SC4D7U6D3V3KX-GP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_B
C2922
C2921
SC1U10V2KX-1GP
HP_OUT_L 31,97
HP_OUT_R 31,97
MICL 30
MICR 30
AUD_VREFOUT_B 30
AUD_SPK_L-
AUD_SPK_L+
AUD_SPK_L- 31
AUD_SPK_L+ 31
AUD_SPK_R-
AUD_SPK_R+
AUD_SPK_R- 31
AUD_SPK_R+ 31
AUD_PC_BEEP
AUD_CAP2
AUD_VREFFLT
AUD_V_B
AUD_VREG
20120112 PV-R
PM_SLP_S3# 8,19,27,34,35,36,37,45,46,47,48,92,93
Vout = 4.75 V
Vout = 1.25(1+R1/R2)
R2906
0R0402-PAD
Q2902
AVDD_CODEC_EN
EN
GND
IN
NR
OUT
TPS793475_NR
HPA01085DBVR-GP
74.01085.03F
C2907
SCD1U10V2KX-4GP
C2911
SCD01U16V2KX-3GP
C2912
SC22U6D3V3KX-GP
R2927
100KR2J-1-GP
AUD_SENSE_B
Close to Pin14
C2917
C2918
C2915
C2916
SC4D7U6D3V3KX-GP
SC10U10V5KX-2GP
SCD1U10V2KX-4GP
Close to codec
20110904SI
R2926
4K7R2J-2-GP
C2928
SC820P50V2KX-1GP
Digital GND & AUD_AGND
Tie Analog GND and Digital GND
under codec by a single point
G2901
G2902
G2903
GAP-CLOSE-PWR-3-GP
audio ground must be connect to
digital ground with an 80 mil copper
bridge located directly under codec
to prevent ESD latch up.
PC BEEP
R2924
10KR2J-3-GP
MONO_L2
MONO_L_0
MONO_L_1
C2927
SCD1U16V2KX-3GP
R2923
100KR2J-1-GP
C2925
SCD1U16V2KX-3GP
Q2901
2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
R2925
10KR2J-3-GP
C2926
SCD01U16V2KX-3GP
HDA_SPKR
R2915
2K49R2F-GP
R2913 20KR2F-L-GP
HP_DETECT# 31,97
R2919 10KR2F-2-GP
MIC_DETECT# 31,97
C2919
SC1KP50V2KX-1GP
Close to Pin13
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Audio Codec 92HD87B2X5
Size A3
Document Number
2012 S-Series Richie 13.3
Rev -1
Date: Wednesday, March 14, 2012
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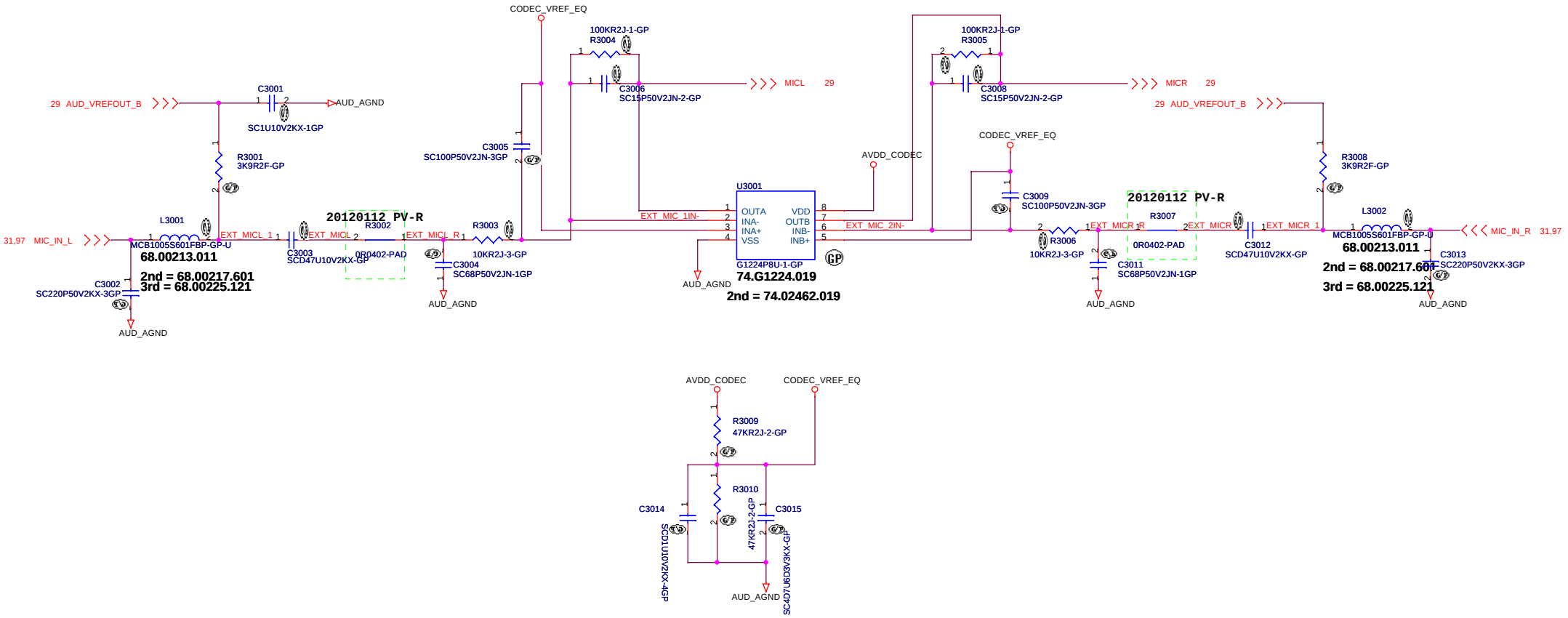
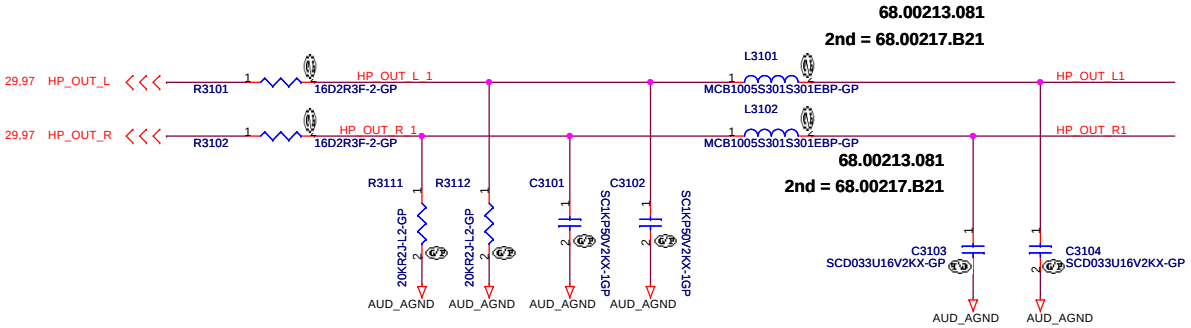
Pre-AMP. for External MIC



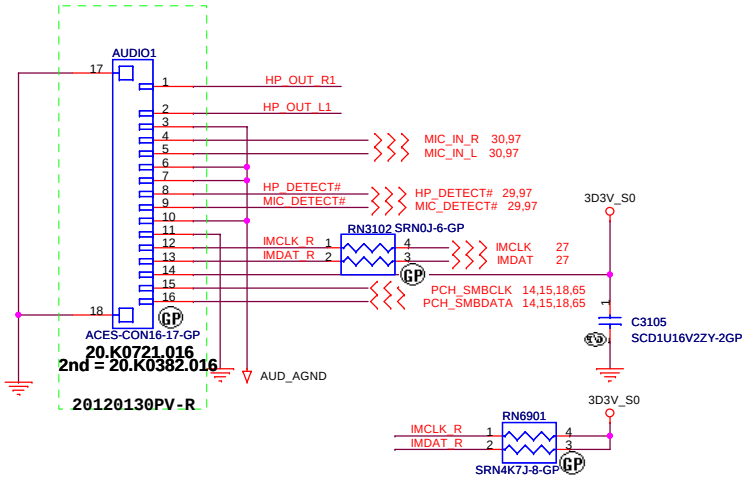
<Core Design>

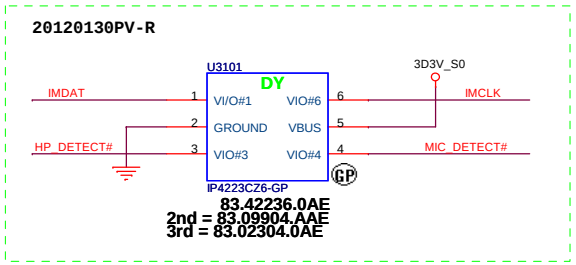
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *External MIC Pre-Amp*		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
Date: Wednesday, March 14, 2012	Sheet 30 of 103	

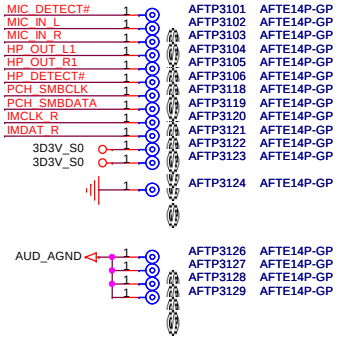
HeadPhone OUT



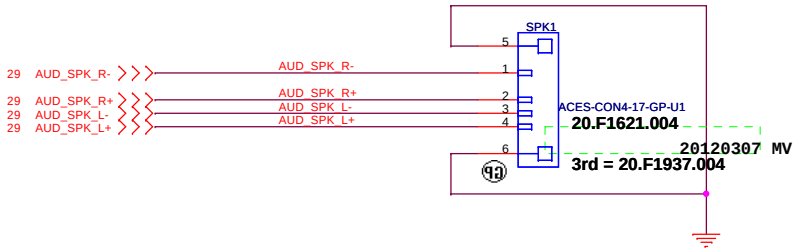
Audio Board +Touch Pad Connector

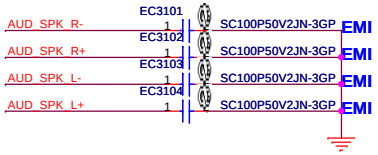


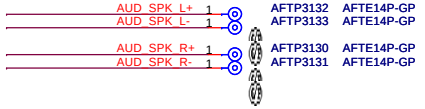




Speaker Connector







<Core Design>

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Title: AUDIO Connector

Size	Document Number	Rev
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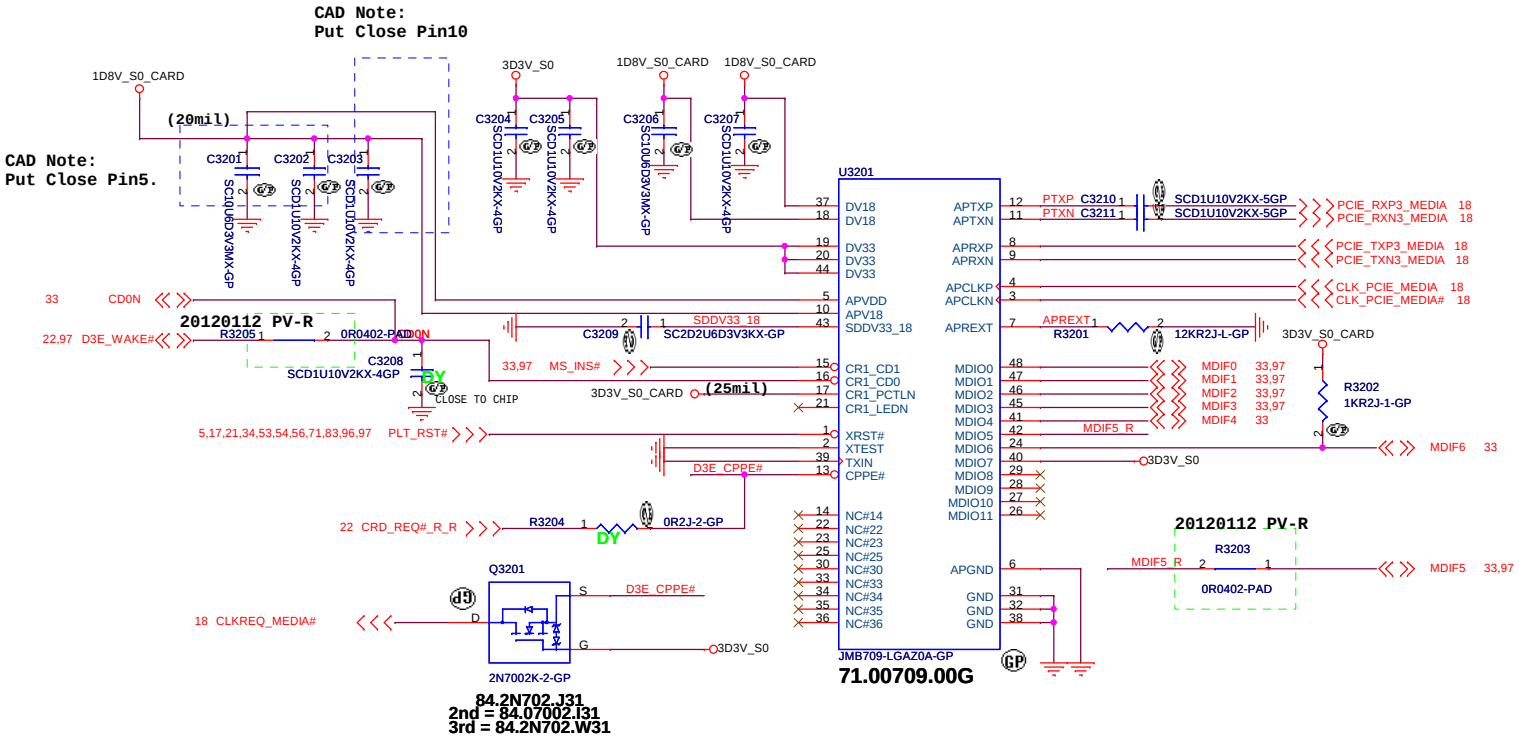
CardReader JMicron JMB709



84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

D3E Detection Table

D3E_CPPE#	Status
H	D3E mode
L	Normal mode

CR1_CDxN Detection Table

CR1_CDxN		Card Type
1	0	
H	H	(No Card)
H	L	SD Card/MMC
L	H	MemoryStick
L	L	XD Card

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-JMB 709

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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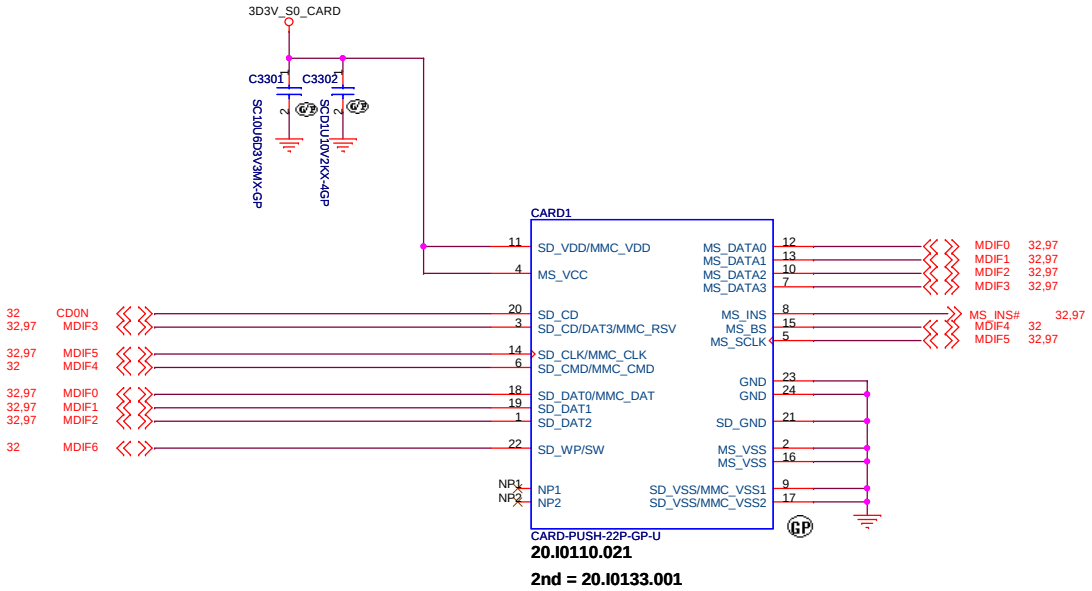

Pin Name	Default Mode	SD/MMC Card	MS Card
MDIO0	SD/MMC/MS	SD1_DAT0	MS1_DAT0
MDIO1		SD1_DAT1	MS1_DAT1
MDIO2		SD1_DAT2	MS1_DAT2
MDIO3		SD1_DAT3	MS1_DAT3
MDIO4		SD1_CMD	MS1_BS
MDIO5		SD1_CLK	MS1_CLK
MDIO6		SD1_WP	
MDIO7			
MDIO8		MMC_DAT4	MS1_DAT4
MDIO9		MMC_DAT5	MS1_DAT5
MDIO10		MMC_DAT6	MS1_DAT6
MDIO11		MMC_DAT7	MS1_DAT7
CR1_LEDN		SD1_LED#	MS1_LED#
CR1_PCTLN		SD1_PCTL#	MS1_PCTL#
CR1_CD0		SD1_CD#	
CR1_CD1			MS1_CD#

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SD/MS/MMC CONNECTOR***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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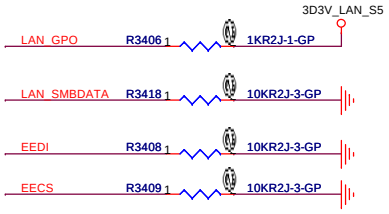
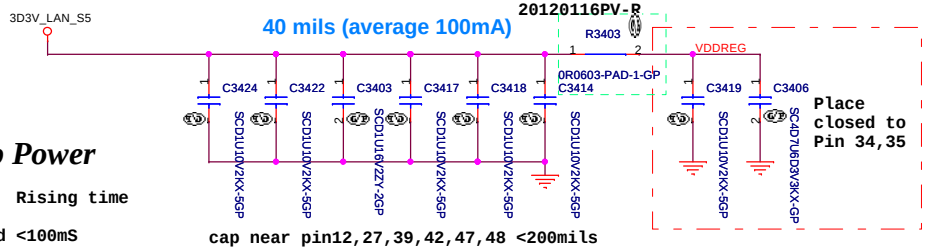
LAN CHIP-RTL8151FH

USE EFuse No ASF

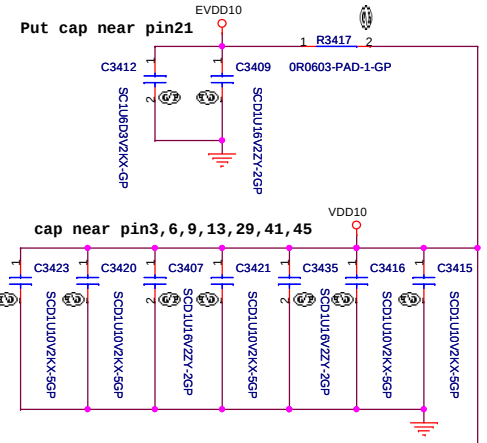


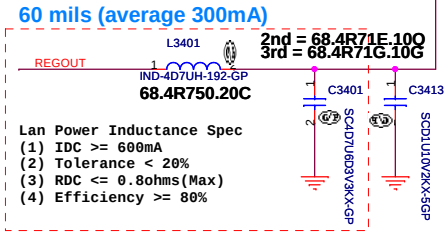
LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS



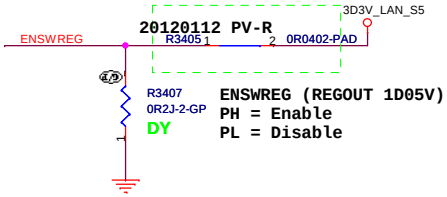
Regout power plane(1D05V)

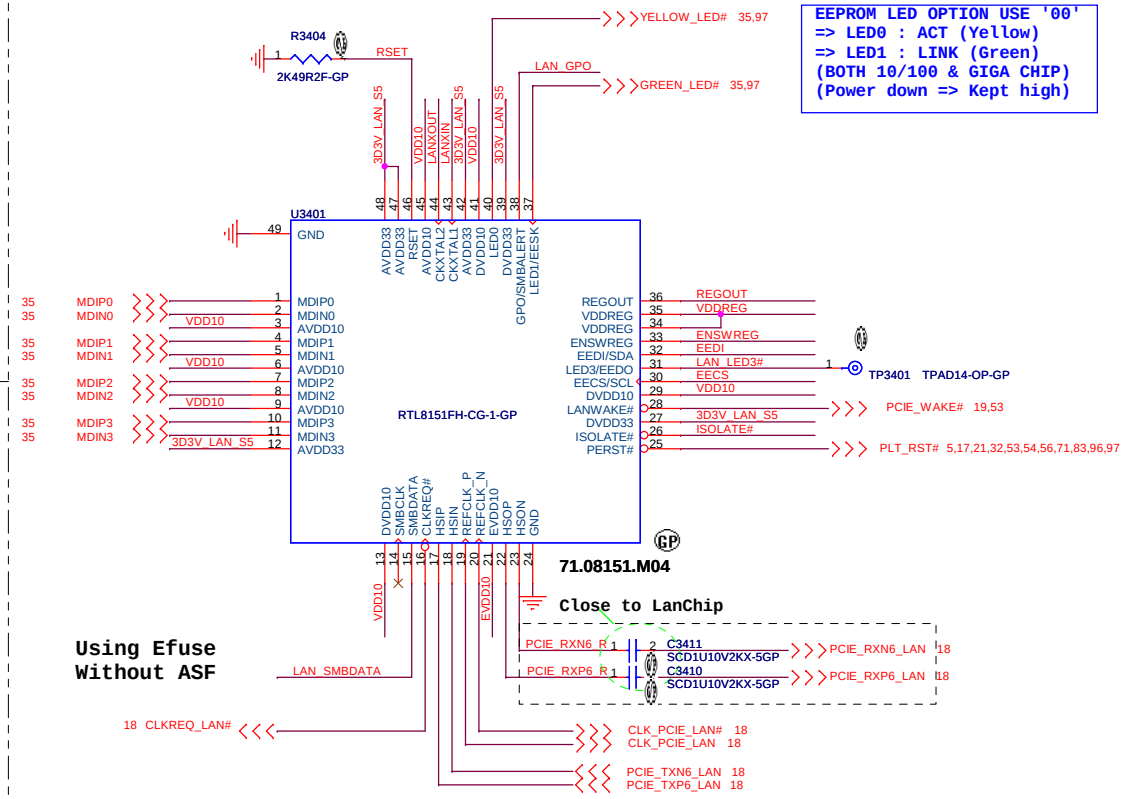


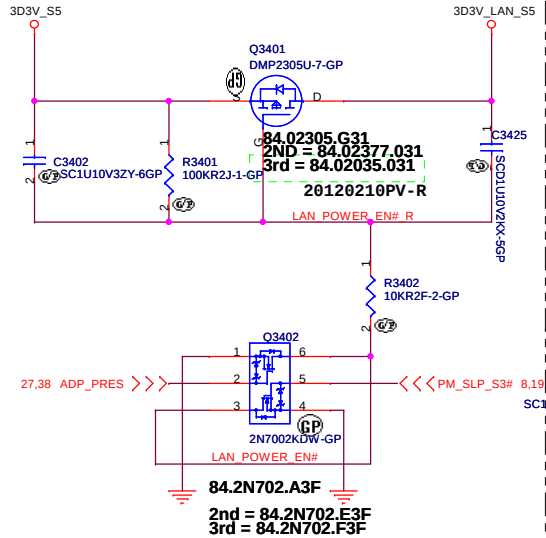


Put 4D7U L + 4D7U cap near pin36 <200mils
(2nd = 78.22610.81L)

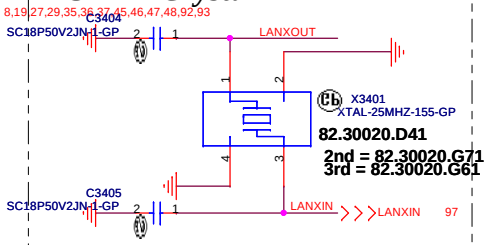
Regout Switch



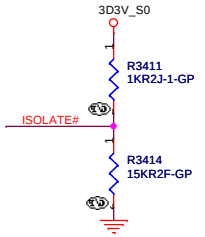




25MHz Crystal



Isolate Strap Pin



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Lan Realtek 8151FH

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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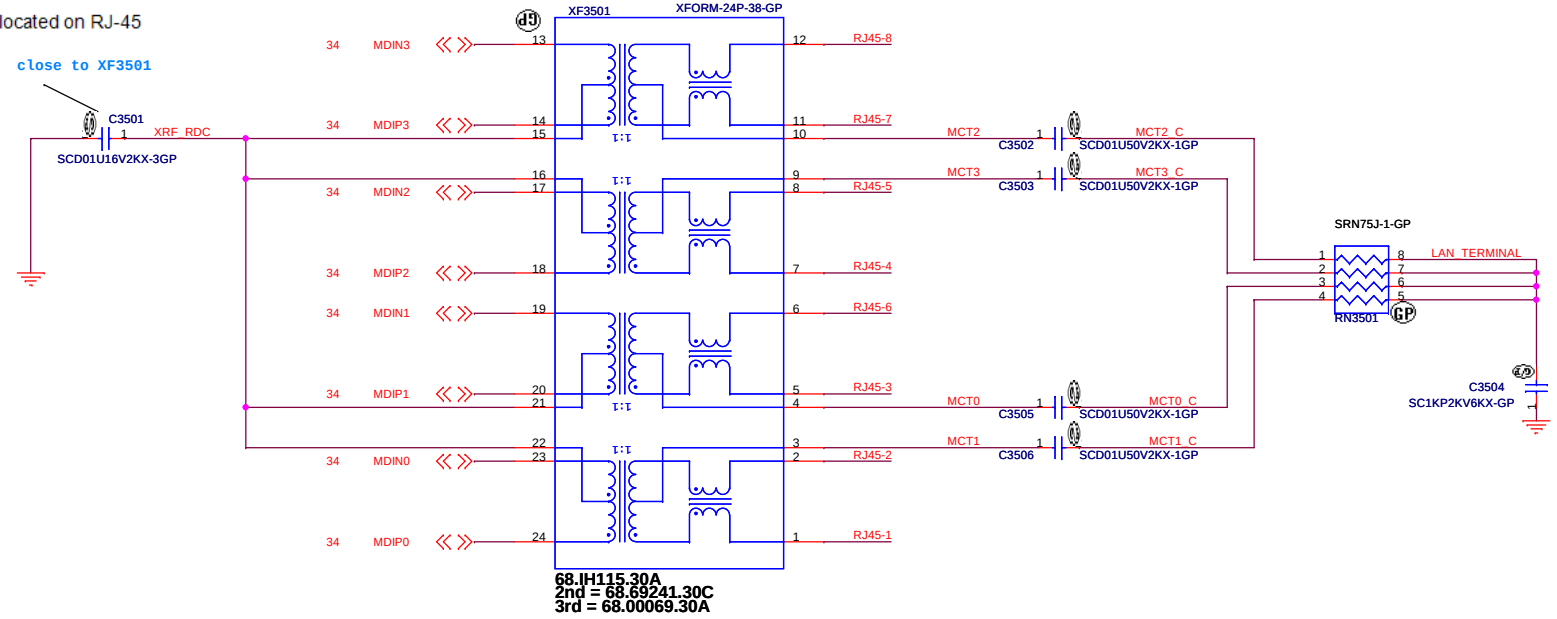
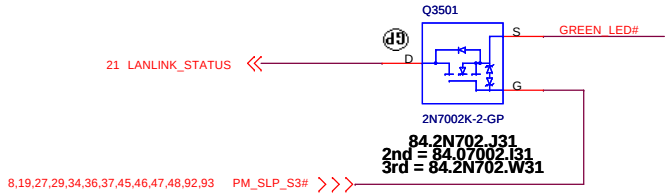
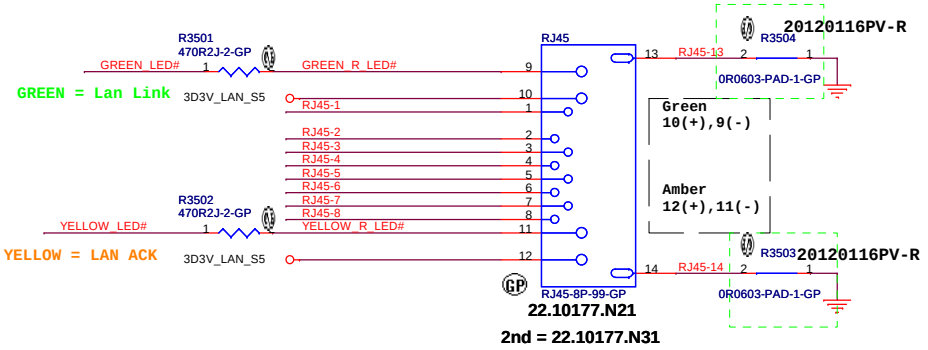
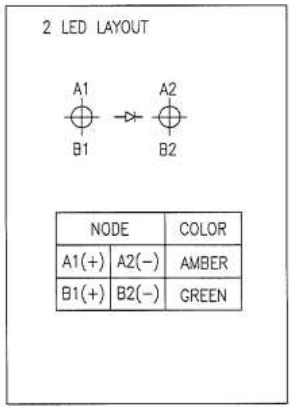
White LED for connectivity and Amber LED for activity located on RJ-45 connector

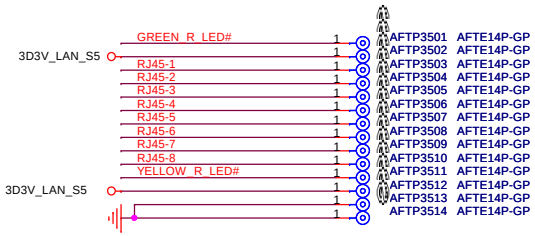


RJ45 Connector









(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RJ45

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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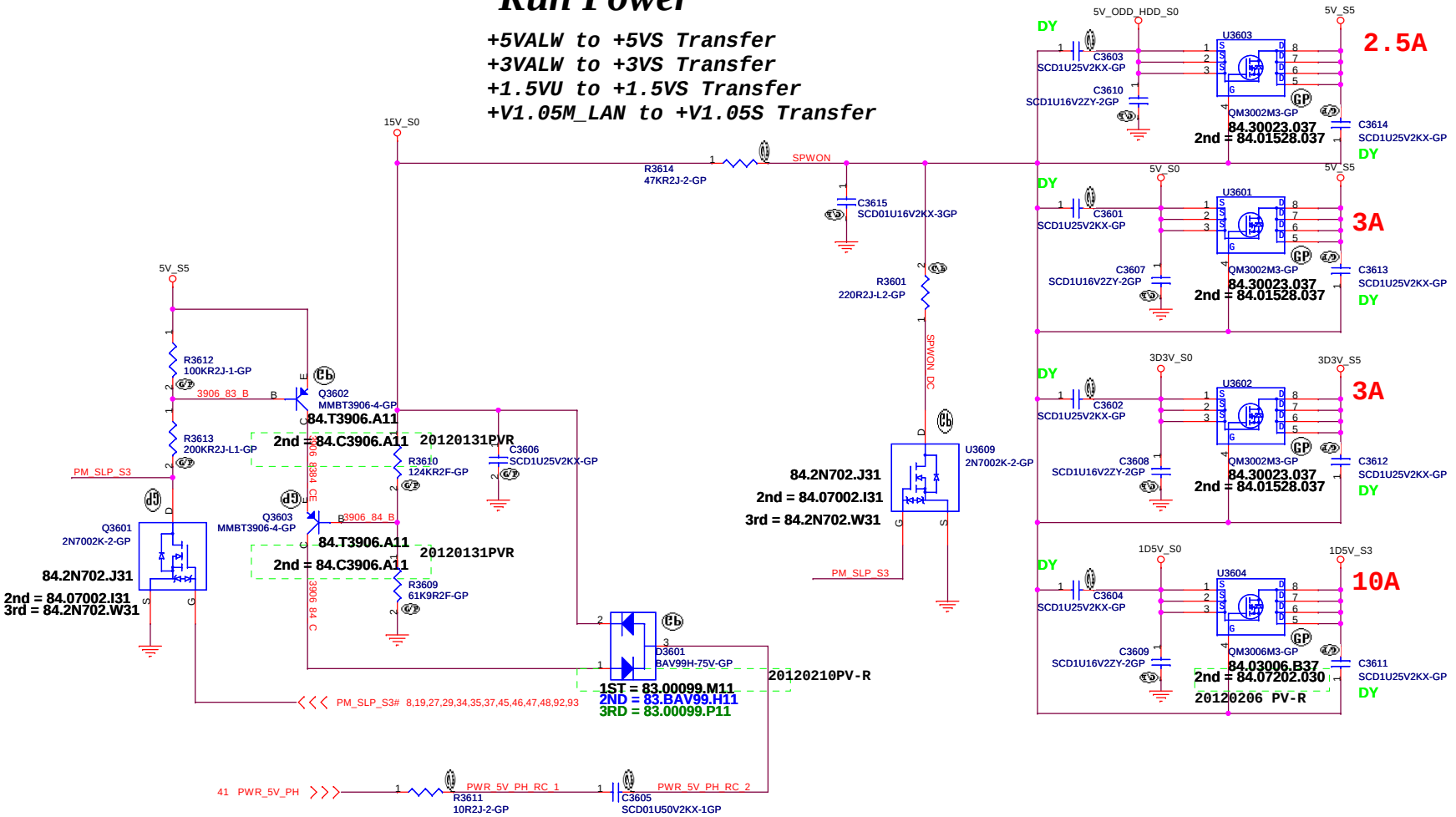
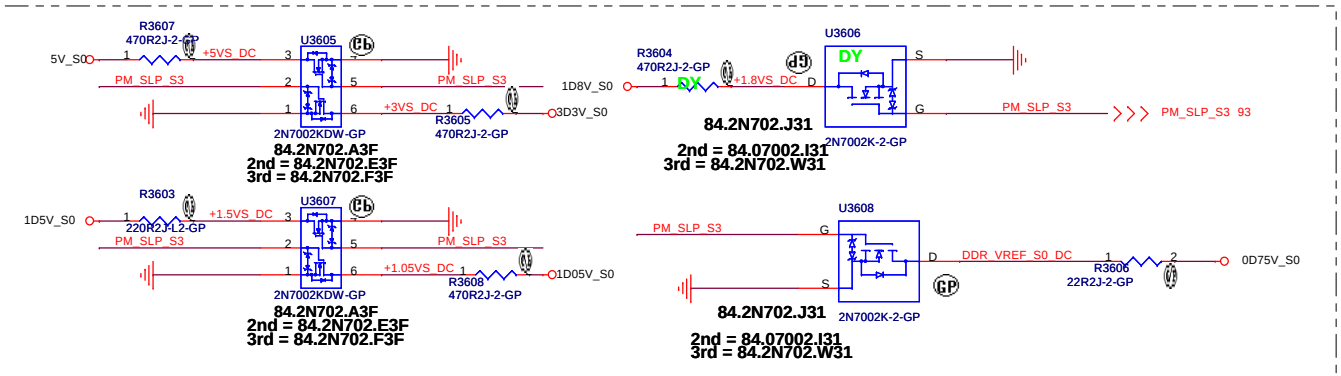
Run Power

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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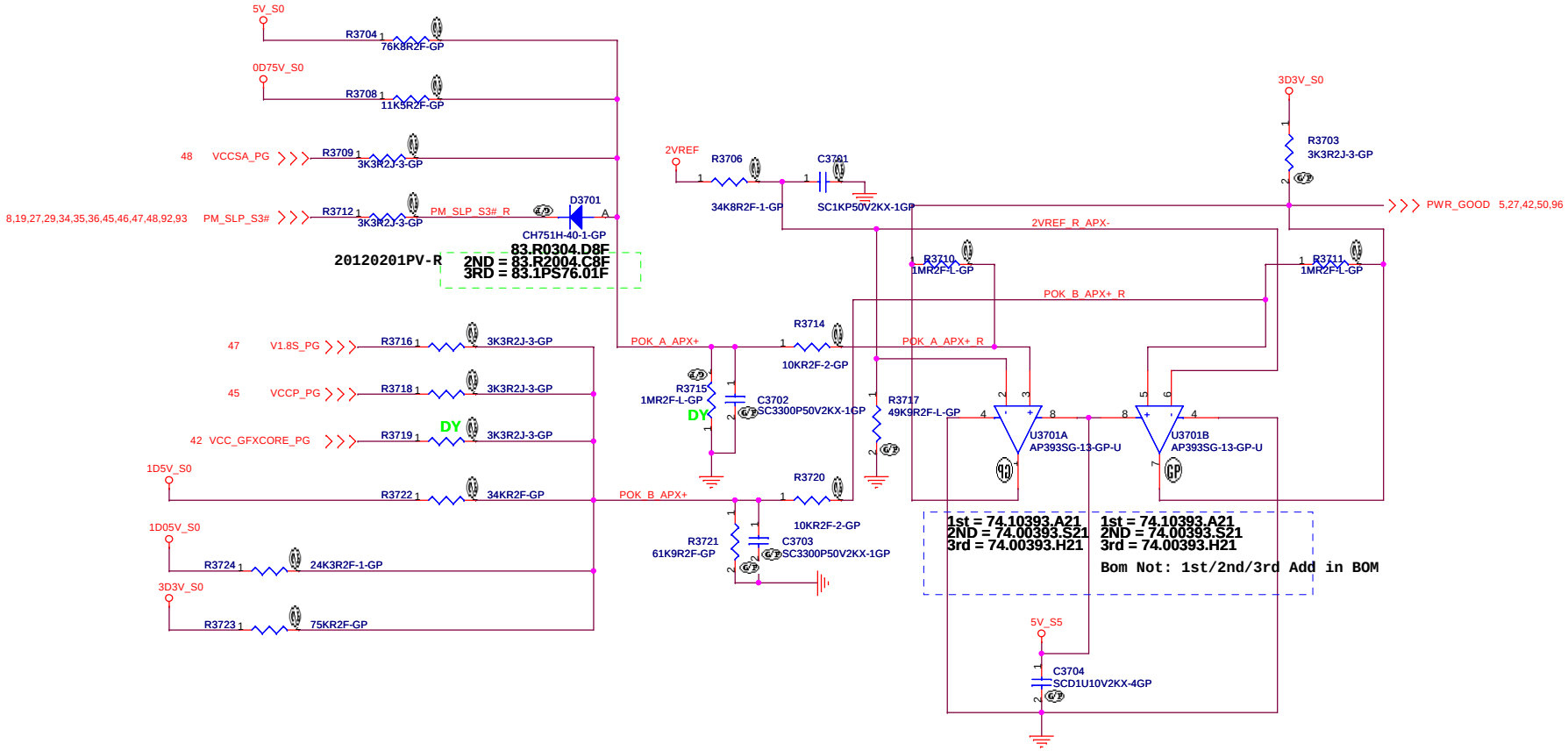
POK



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POK	
Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
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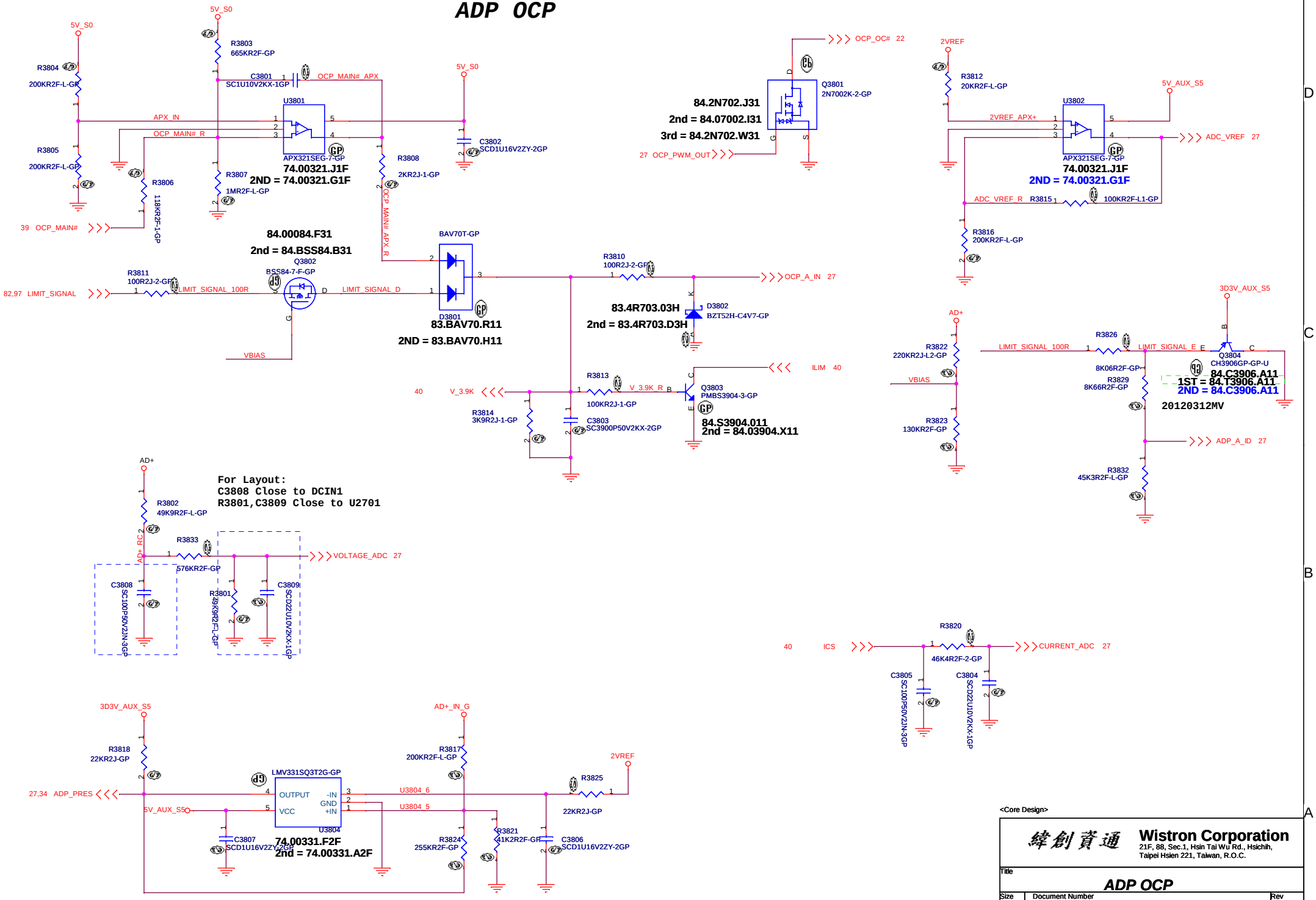
ADP OCP

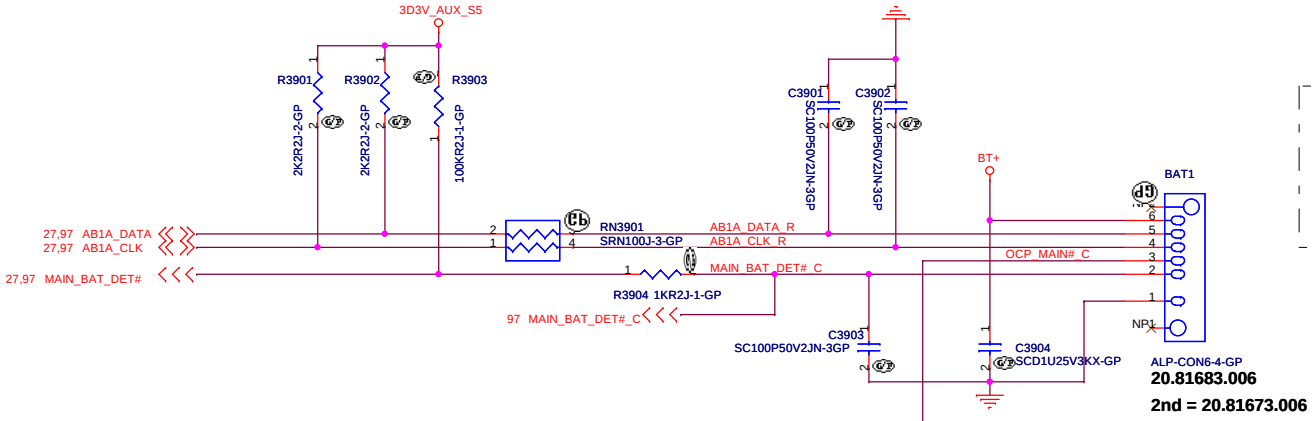


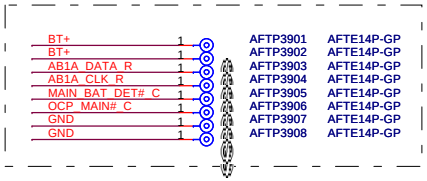
<Core Design>

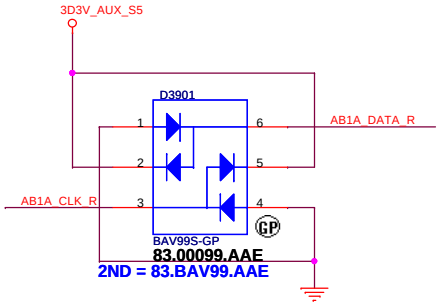
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

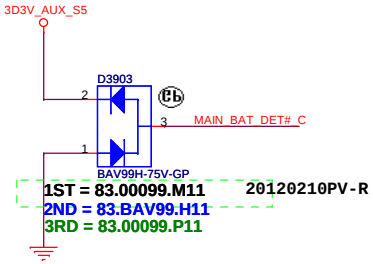
Title	ADP OCP	
Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012	Sheet 38 of 103	

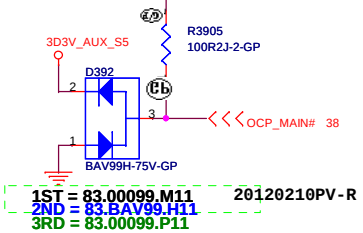
Battery Connector











<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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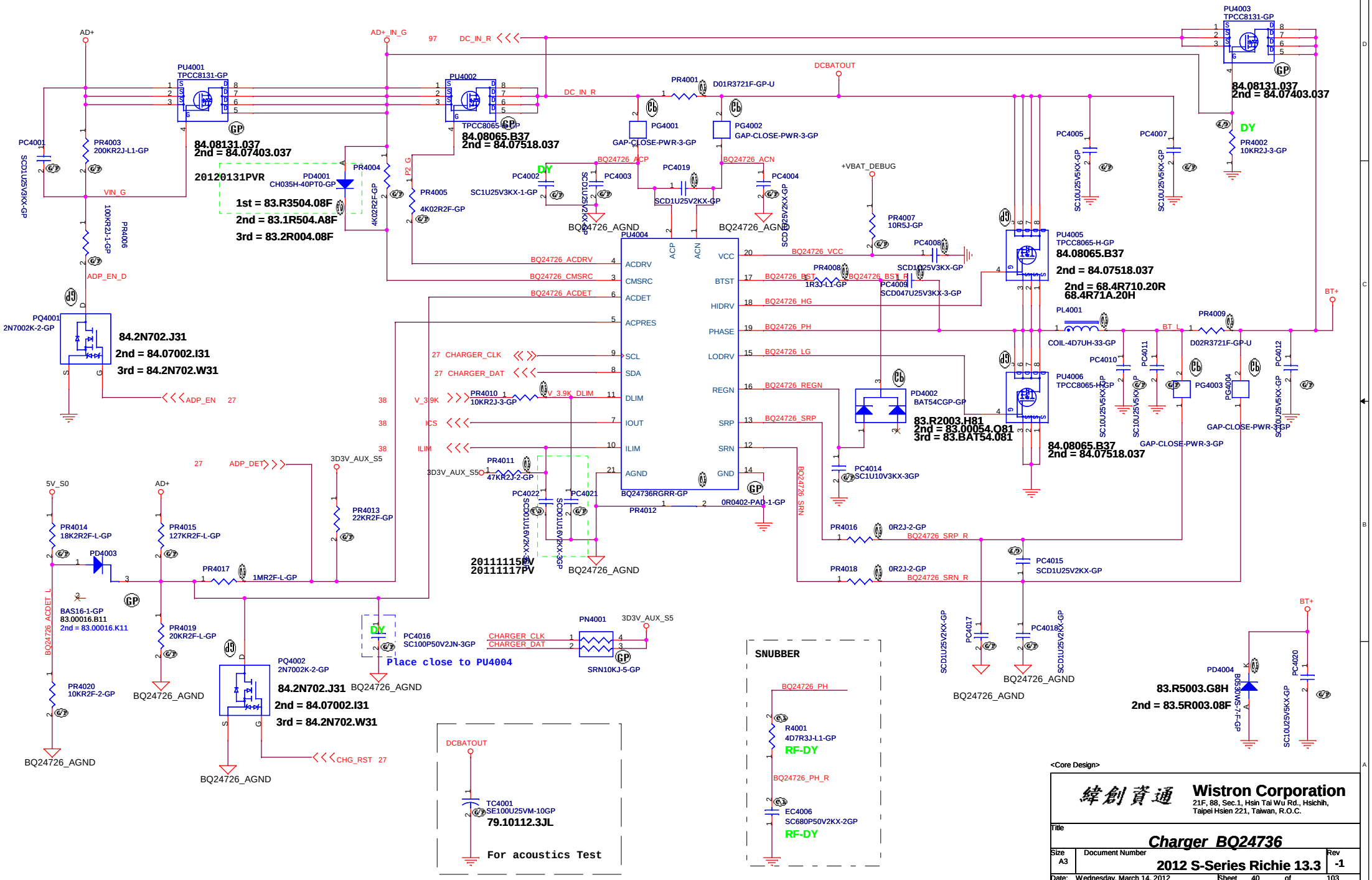
BQ24736 for CHARGER



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger BQ24736

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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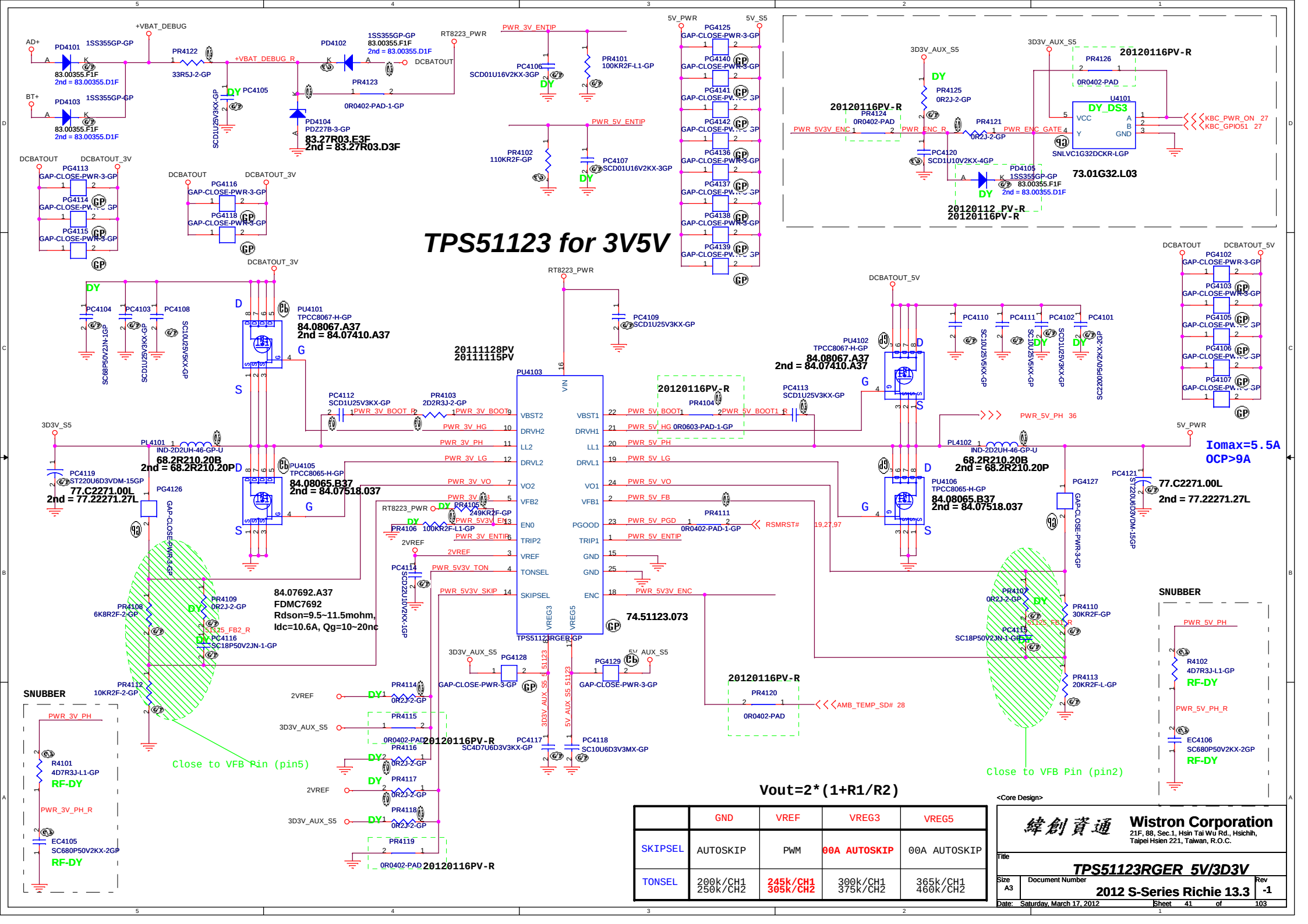


	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Core Design>

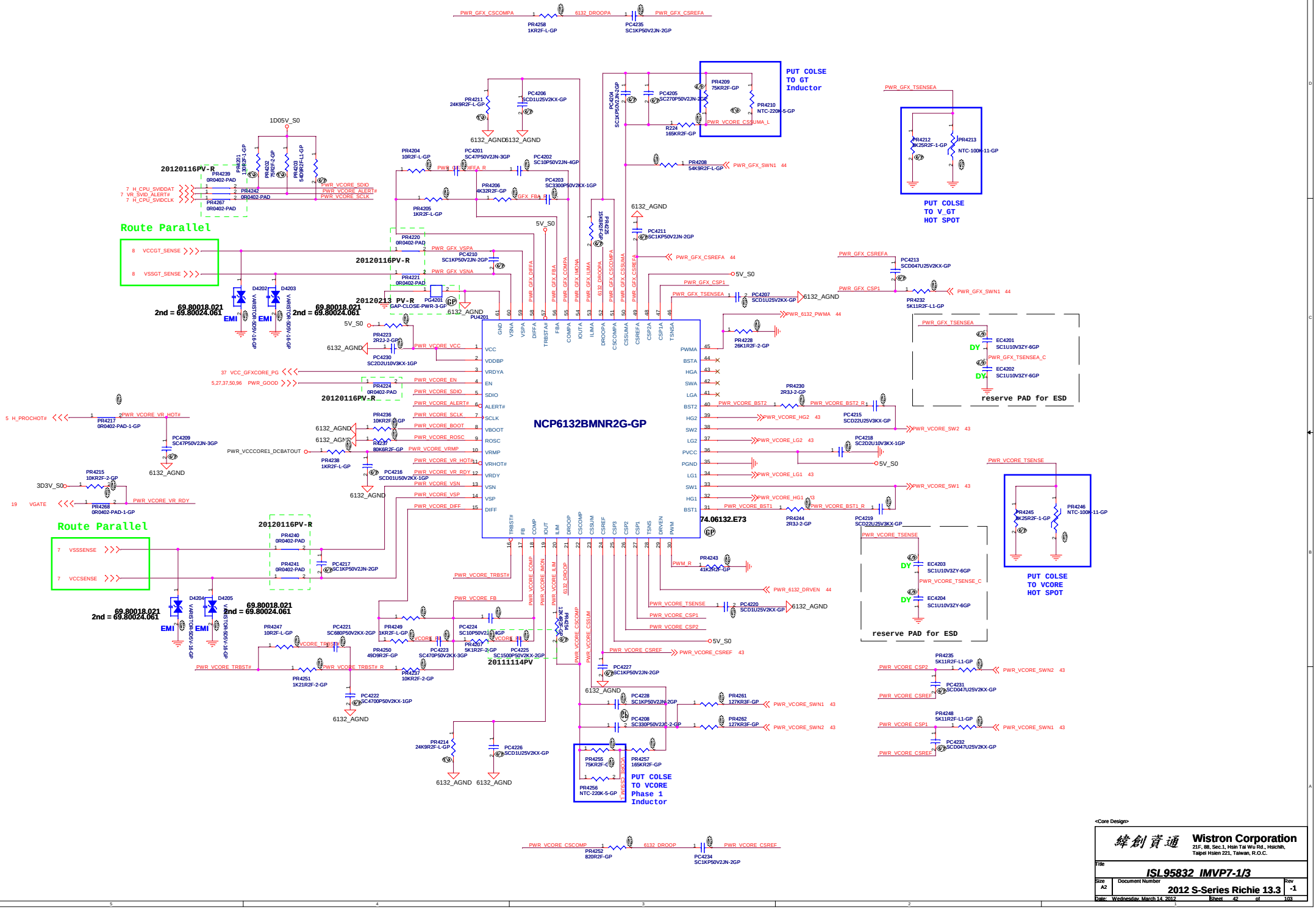
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123RGER 5V/3D3V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Saturday, March 17, 2012 | Sheet 41 of 103

SSID = CPU.Regulator



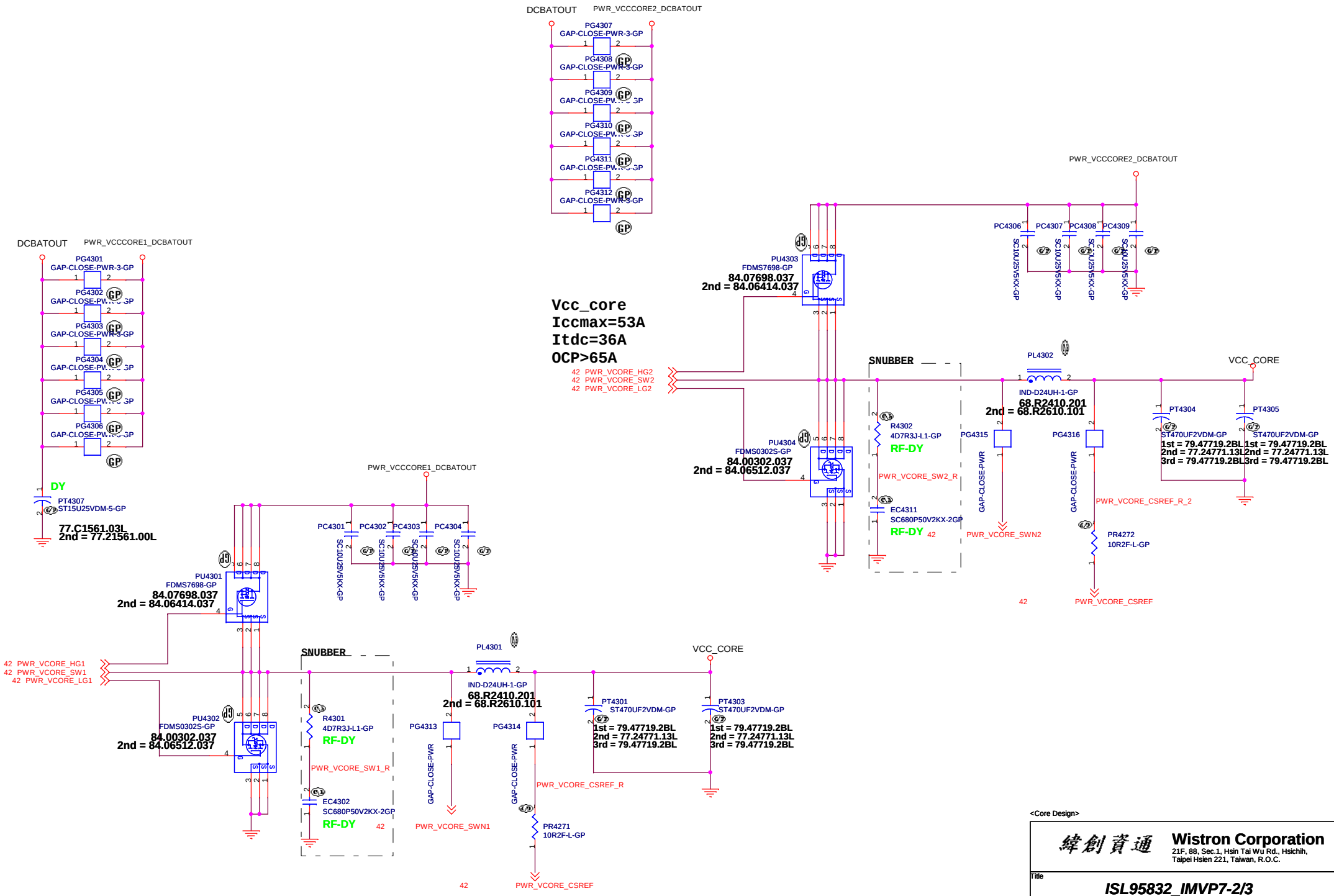
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832 IMVP7-1/3

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 42 of 103



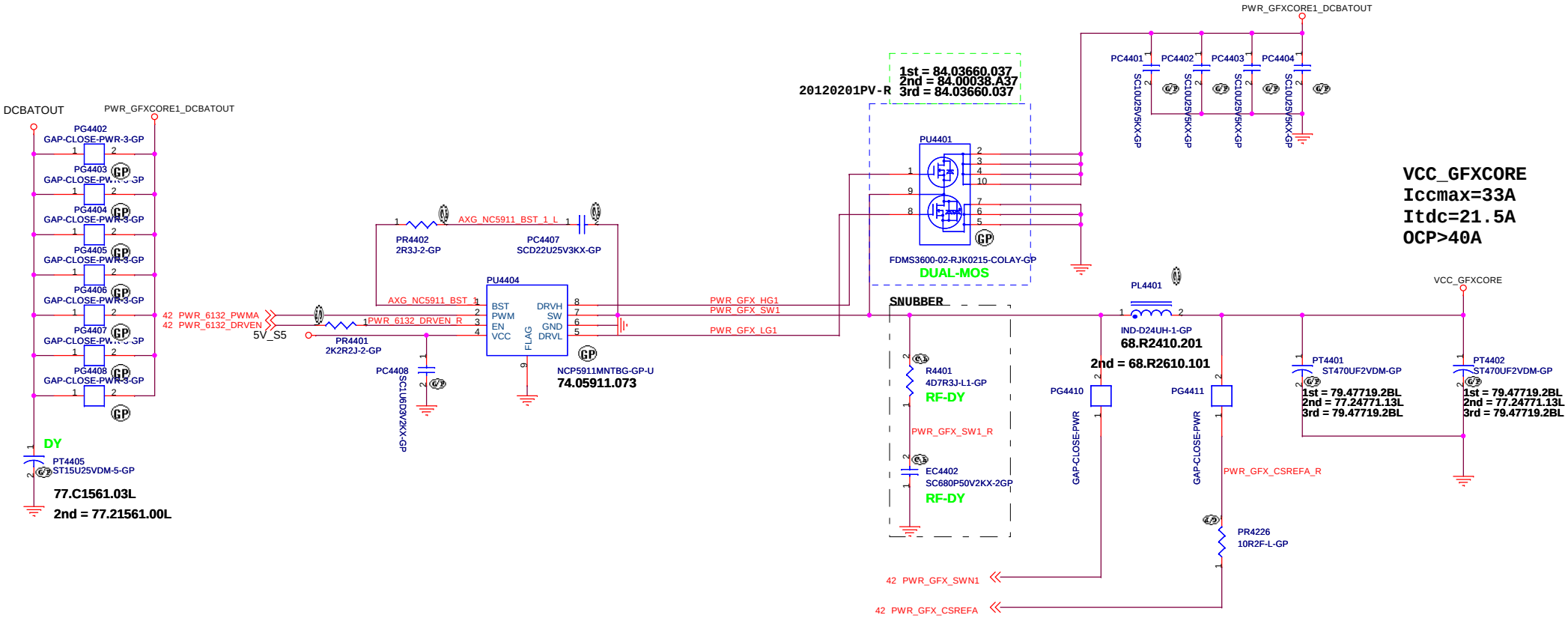
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832_IMVP7-2/3

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 43 of 103



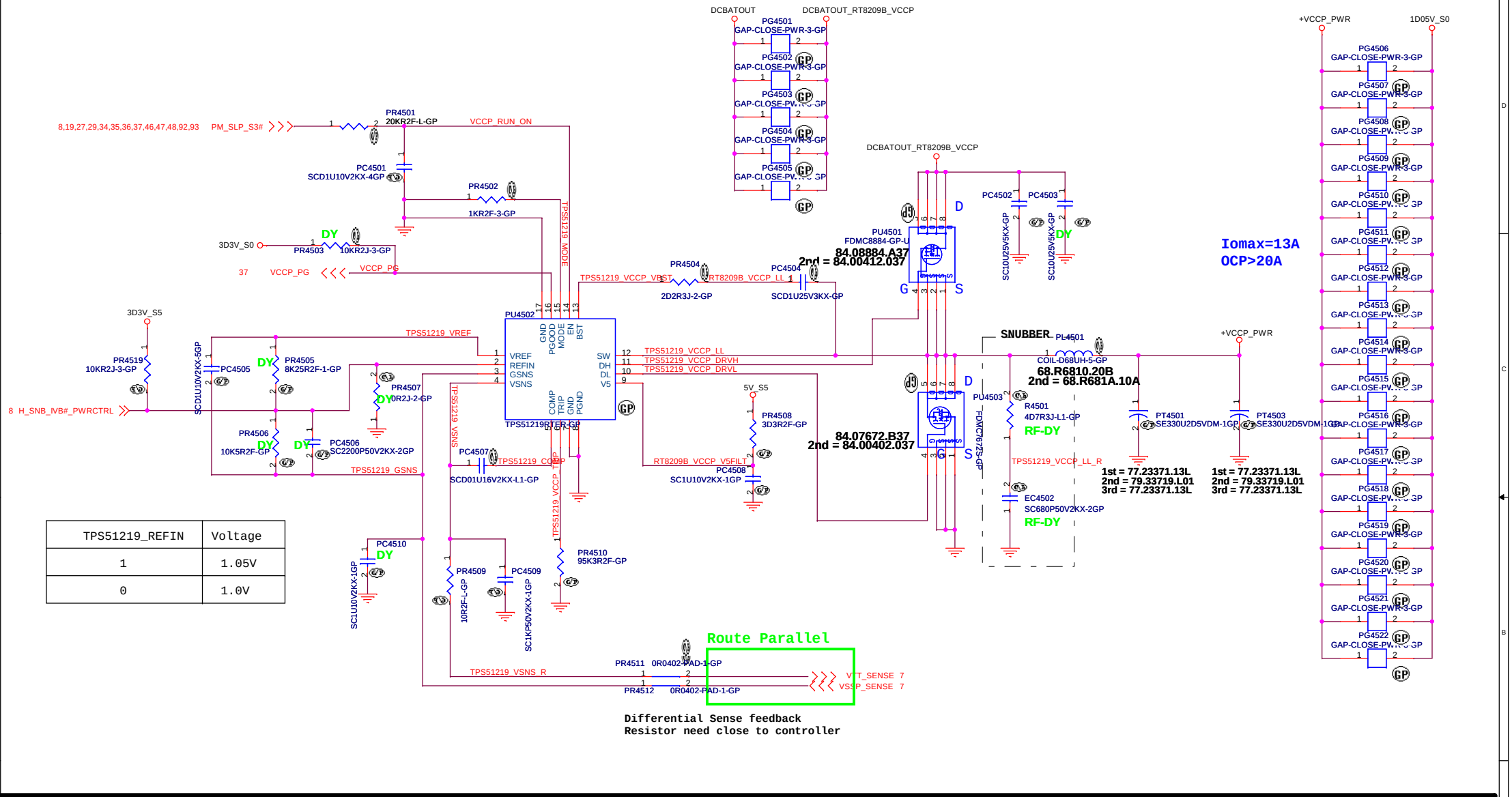
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832_IMVP7-3/3

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Monday, March 19, 2012 Sheet 44 of 103



TPS51219_REFIN	Voltage
1	1.05V
0	1.0V

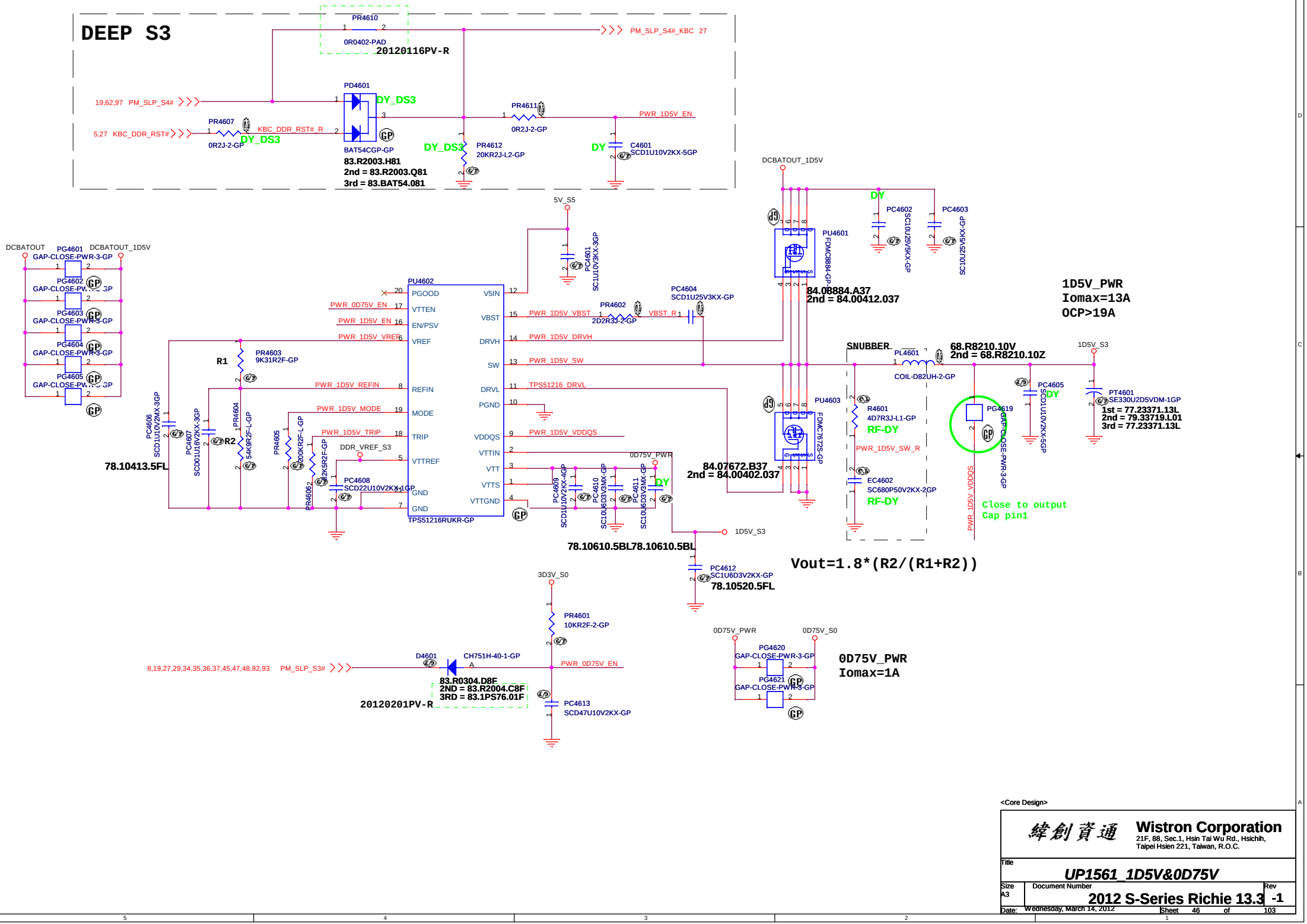
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_1D05V / 1D0V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 45 of 103



<Core Design>

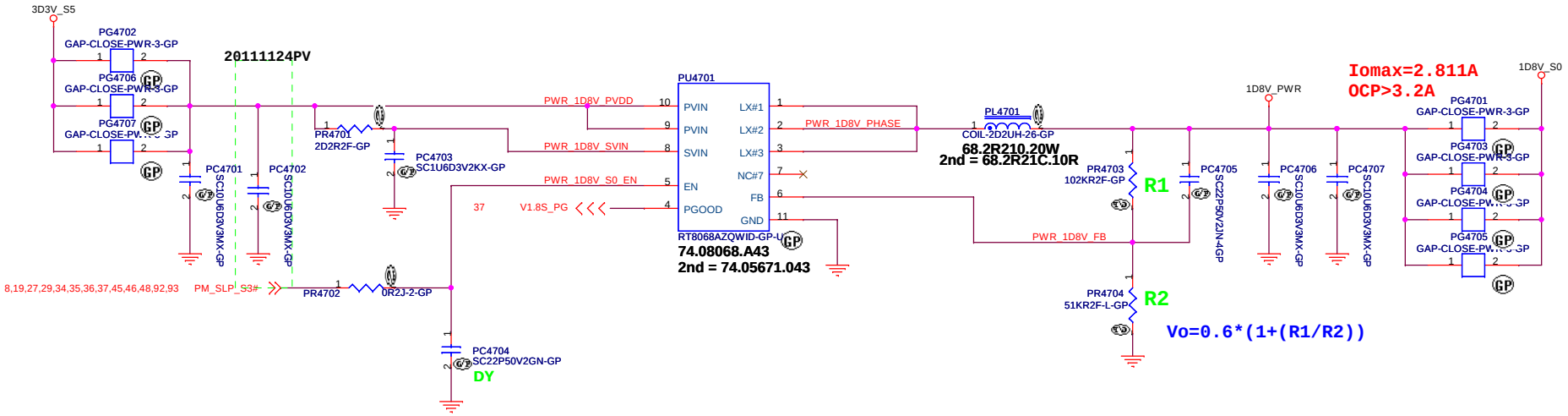
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UP1561_1D5V&0D75V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 46 of 103

RT8068A for 1D8V_S0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_S0

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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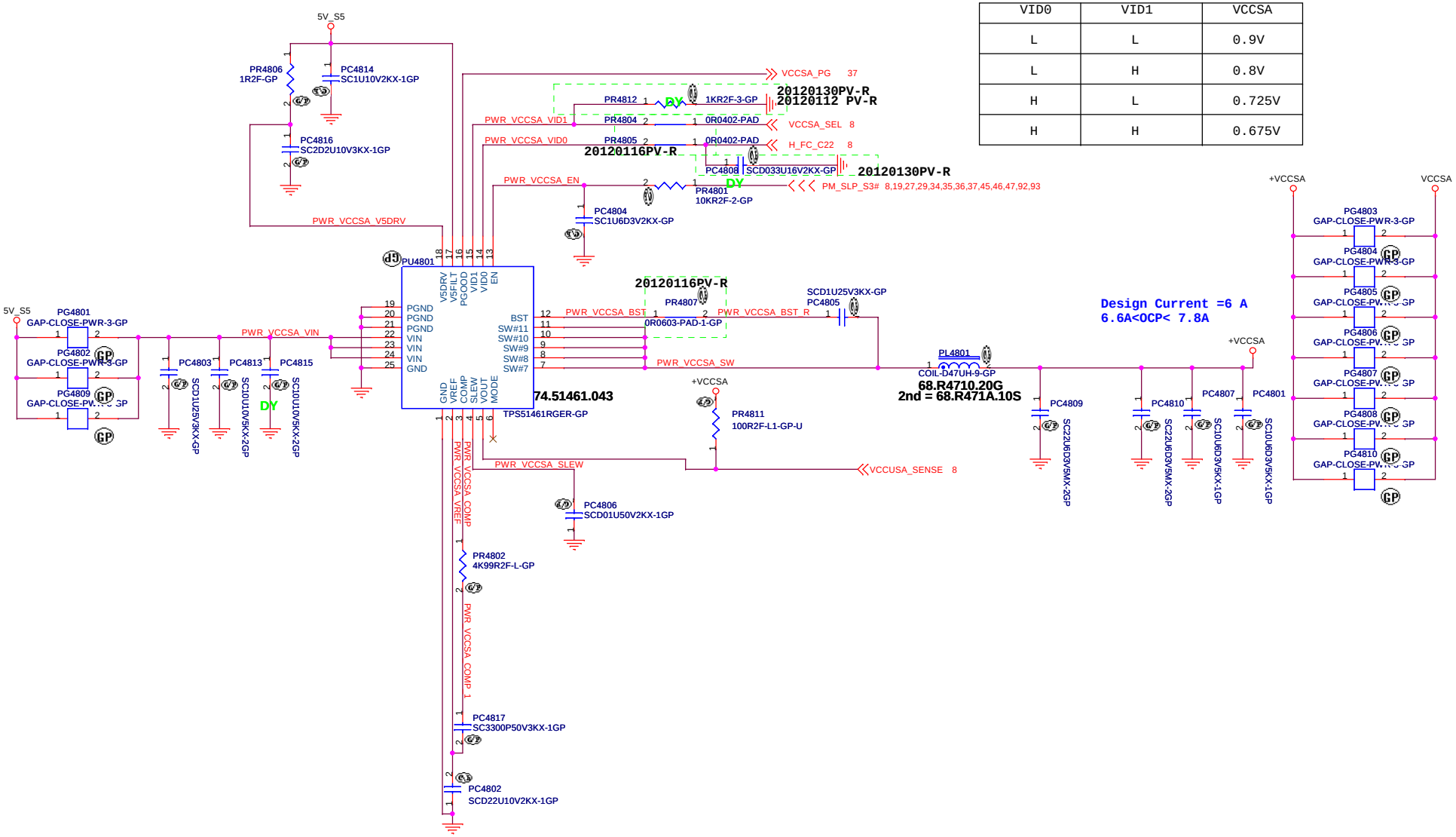
TPS51461 for VCCSA

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



<Core Design>

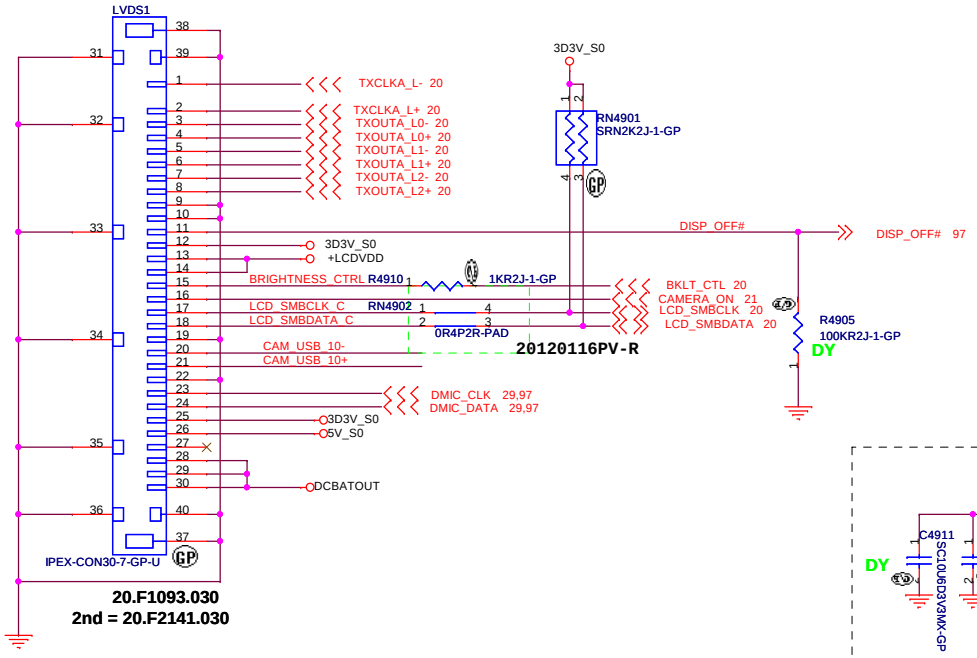
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95870A VCCSA

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

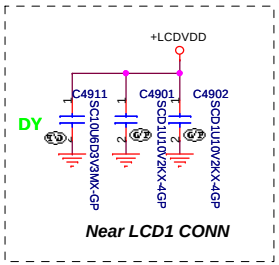
Date: Wednesday, March 14, 2012 | Sheet 48 of 103

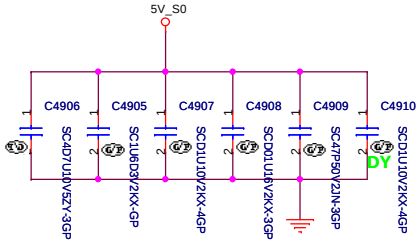
LCD Connector

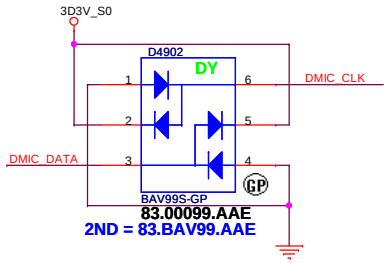


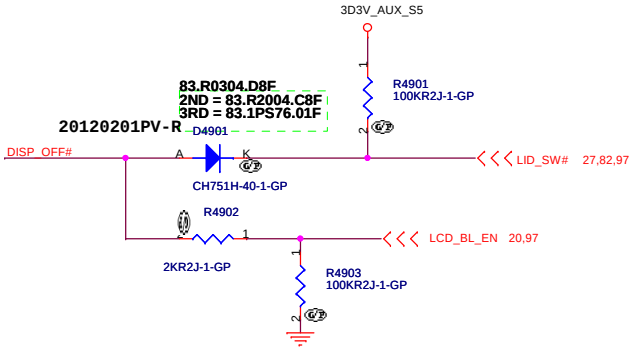
CARMER PINDEFINE

No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-

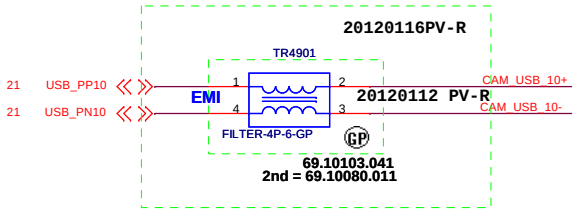




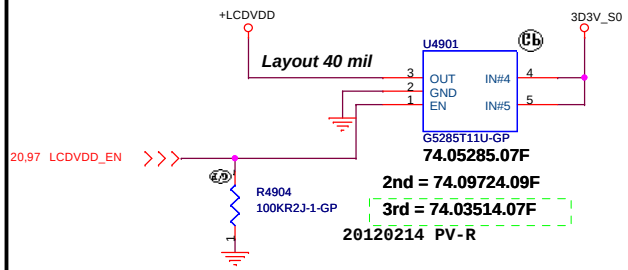




CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
Date: Wednesday, March 14, 2012	Sheet 49 of 103	

CRT Connector

CRT1
Transmission line characteristic impedance for RGB signals Zo = 37.5 Ohm

Transmission line characteristic impedance Zo= 50 Ohm

CRT RGB

68.00084.B61
2nd = 68.00245.051
3rd = 68.00226.141

L5001 BLM18BB470SN1D-GP
L5002 BLM18BB470SN1D-GP
L5003 BLM18BB470SN1D-GP

MUX_R MUX_G MUX_B
MUX_L_R MUX_L_G MUX_L_B
R5011 R5012 R5013 0R2J-2-GP
CRT_R CRT_G CRT_B

R1
R5001 R5002 R5003 75R2F-2-GP
C5001 C5002 C5003 SC22P50V2JN-4GP
C5004 C5005 C5006 SC22P50V2JN-4GP
C5007 C5008 C5009 SC22P50V2JN-4GP

DY DY DY 20120112 PV-R 20120116PV-R

Place these resistors as the closest components to connector CRT1

Transmission line characteristic impedance Zo = 50 Ohm

5V_S0 → F5001 FUSE-1D1A6V-4GP-U → +5VS_CRT_F2
1.1A/8V

84.02305.G31
2nd = 84.02377.031
3rd = 84.02035.031
20120210PV-R

Q5002 DMP2305U-7-GP
69.50007.691
2nd = 69.50007.771
3rd = 69.60040.011

CRTVDD_EN# 1
R5020 10KR2J-3-GP
R5019 10KR2J-3-GP
CRTVDD_EN#

C5020 SC4D7U10V5ZY-3GP DY
C5022 SCD1U16V2ZY-2GP

5V_S0_CRT
RN5001 SRN2K2J-1-GP

Q5001 2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

5,27,37,42,96 PWR_GOOD

C5019 SCD1U16V2ZY-2GP DY

CRT1
NC#4 NC#11
VCC_CRT
DDCDATA_ID1 DDCCLK_ID3
CRT_RED CRT_GREEN CRT_BLUE
VSYNC HSYNC
GND ×8
D-SUB-15-123-GP
DDC_DATA_CON
DDC_CLK_CON
CRT_R CRT_G CRT_B
CRT_VSYNC_CON_1
CRT_HSYNC_CON_1

20.20938.015
2nd = 20.20984.015

C5023 C5021 SC22P50V2JN-4GP DY
C5024 C5025 SC33P50V2JN-3GP DY

DDC&HSYNC&VSYNC

3D3V_S0
RN5007 SRN10KJ-5-GP
M_HSYNC
M_VSYNC

20120116PV-R
20120112 PV-R
20 PCH_RED → R5006 0R0402-PAD MUX_R
20 PCH_GREEN → R5007 0R0402-PAD MUX_G
20 PCH_BLUE → R5008 0R0402-PAD MUX_B

5V_S0_CRT
C5016 SCD1U16V2ZY-2GP

73.1G125.D0G
2nd = 73.07125.0AG
3rd = 73.1G125.0JH
U5001 U74AHCT1G125G-AL5-R-GP-U
U5002 U74AHCT1G125G-AL5-R-GP-U

20120116PV-R
RN5002 0R4P2R-PAD
20 CRT_HSYNC
20 CRT_VSYNC

M_HSYNC
M_VSYNC

5V @ ext. CRT side
RN5003 SRN33J-5-GP
HSYNC_5
VSYNC_5
CRT_HSYNC_CON_1
CRT_VSYNC_CON_1

C5018 C5017 SC10P50V2JN-4GP DY

3D3V_S0
RN5004 SRN2K2J-1-GP
Q5003 2N7002KDW-GP
CRT_DDC_DATA_R
CRT_DDC_CLK_R
DDC_DATA_CON
DDC_CLK_CON

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

20120116PV-R
2011102PV
20120116PV-R
RN5008 0R4P2R-PAD
20 CRT_DDC_DATA
20 CRT_DDC_CLK

DDC

5V_S0_CRT
D5004 BAV99S-GP DY
CRT_VSYNC_CON_1
CRT_HSYNC_CON_1
83.00099.AAE
2ND = 83.BAV99.AAE

D5005 BAV99S-GP DY
DDC_CLK_CON
DDC_DATA_CON
83.00099.AAE
2ND = 83.BAV99.AAE

D5006 BAV99S-GP DY
CRT_R
CRT_G
83.00099.AAE
2ND = 83.BAV99.AAE

AFTP5001 AFTP5002 AFTP5003 AFTP5004 AFTP5005 AFTP5006 AFTP5007 AFTP5009 AFTP5011 AFTP5008 AFTP5010 AFTP5012 AFTE14P-GP

D5003 BAV99-5-GP-U DY
CRT_B
83.00099.T11
2nd = 83.BAV99.D11
3rd = 83.BAV99.H11
20120131PVR

C5010 SCD1U10V2KX-4GP DY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: A3
Document Number: 2012 S-Series Richie 13.3
Rev: -1
Date: Wednesday, March 14, 2012
Sheet 50 of 103

HDMI Connector

HDMI CONN

20120130PV-R

TR5101
HDMI_CLK_R_C 1 2 HDMI_CLK_R_C_CON
HDMI_CLK_R_C# 4 3 HDMI_CLK_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5103
HDMI_DATA1_R_C 1 2 HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C# 4 3 HDMI_DATA1_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5102
HDMI_DATA0_R_C 1 2 HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C# 4 3 HDMI_DATA0_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5104
HDMI_DATA2_R_C 1 2 HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C# 4 3 HDMI_DATA2_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

HDMI_PLL_GND
DY R5123 0R2J-2-GP
Q5103 2N7002K-2-GP
3D3V_S0
DY R5113 100KR2J-1-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

HDMI1
SKT-HDMI23-54-GP
22.10296.721
2nd = 22.10296.761
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_S0_CRT
C5102 SCD1U10V2KX-5GP
HPD_HDMI_CON

Close to PCH

20 HDMI_CLK_R#
20 HDMI_CLK_R
C5103 SCD1U10V2KX-5GP
C5104 SCD1U10V2KX-5GP
HDMI_CLK_R_C#
HDMI_CLK_R_C

20 HDMI_DATA0_R#
20 HDMI_DATA0_R
C5105 SCD1U10V2KX-5GP
C5106 SCD1U10V2KX-5GP
HDMI_DATA0_R_C#
HDMI_DATA0_R_C

20 HDMI_DATA1_R#
20 HDMI_DATA1_R
C5110 SCD1U10V2KX-5GP
C5107 SCD1U10V2KX-5GP
HDMI_DATA1_R_C#
HDMI_DATA1_R_C

20 HDMI_DATA2_R#
20 HDMI_DATA2_R
C5108 SCD1U10V2KX-5GP
C5109 SCD1U10V2KX-5GP
HDMI_DATA2_R_C#
HDMI_DATA2_R_C

Close to HDMI Connector

RN5106 SRN680J-GP
RN5107 SRN680J-GP
HDMI_PLL_GND

3D3V_S0
DY R5110 200KR2J-L1-GP
HDMI_HPD_B1
R5111 150KR2J-L1-GP
Q5102 PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.X11
HDMI_HPD_R1
R5128 0R0402-PAD
HDMI_PCH_DET 20,97
R5112 20KR2F-L-GP
20120116PV-R

5V_S0_CRT
3D3V_S0
RN5101 SRN2K2J-1-GP
Q5104 2N7002KDW-GP
20 PCH_HDMI_CLK
DDC_CLK_HDMI
20 PCH_HDMI_DATA
DDC_DATA_HDMI
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.P3F

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Conn
Size: A3
Document Number: 2012 S-Series Richie 13.3
Rev: -1
Date: Wednesday, March 14, 2012
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

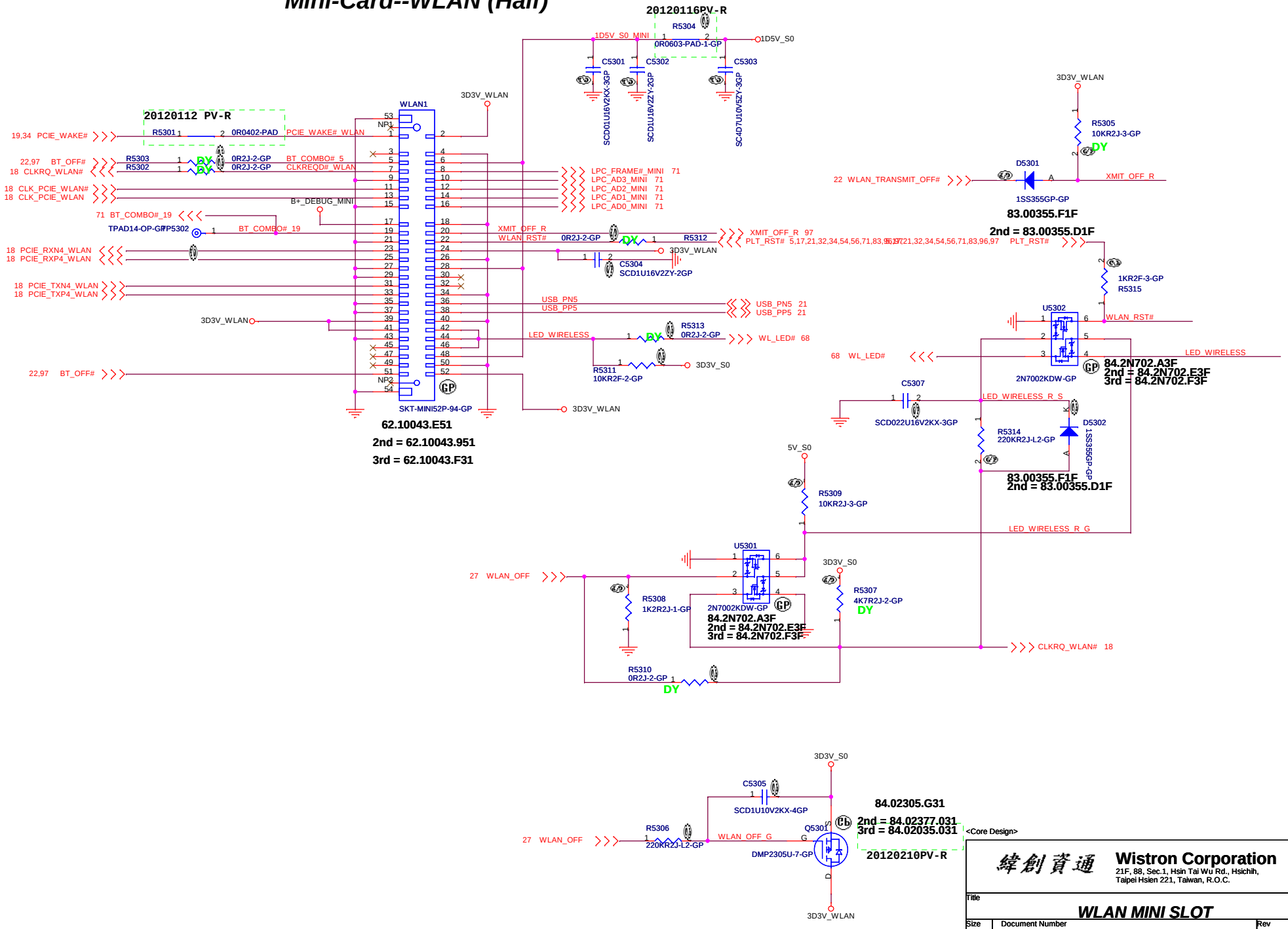
Title

(Reserved)

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

WLAN Connector

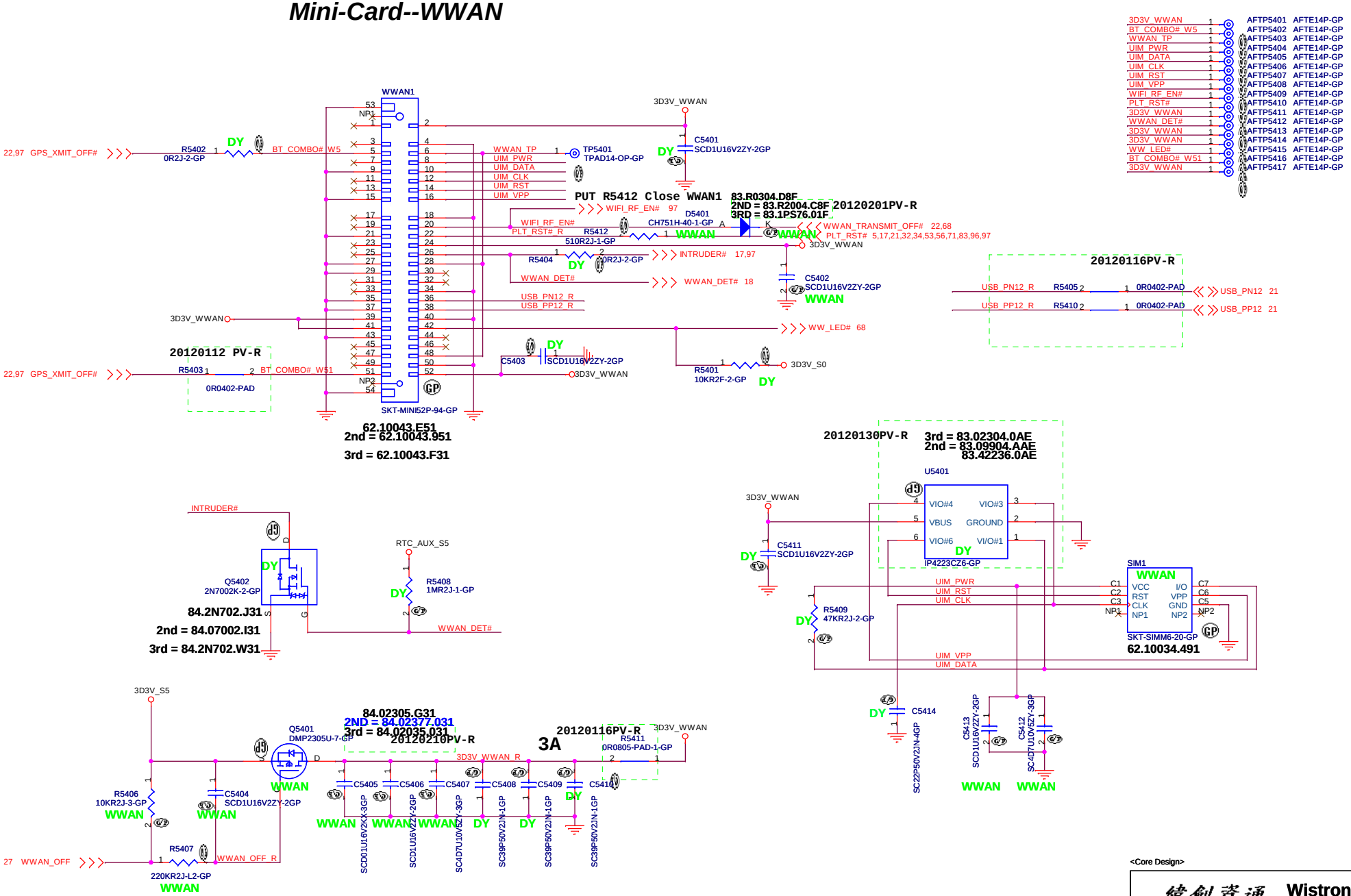
Mini-Card--WLAN (Half)



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***WLAN MINI SLOT***	
Size: A3	Document Number: **2012 S-Series Richie 13.3**	Rev: -1
Date: Wednesday, March 14, 2012	Sheet 53 of 103	

WWAN Connector

Mini-Card--WWAN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN MINI SLOT/SIM**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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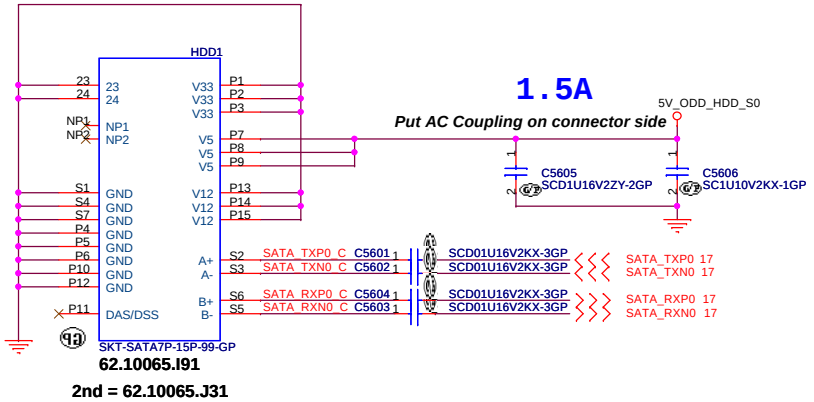
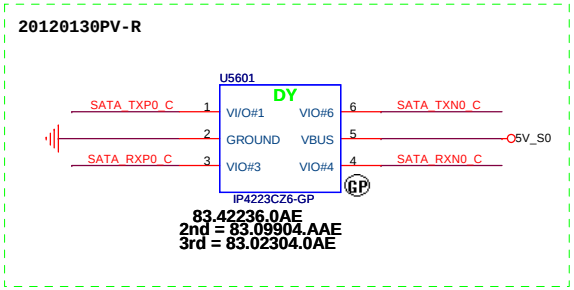
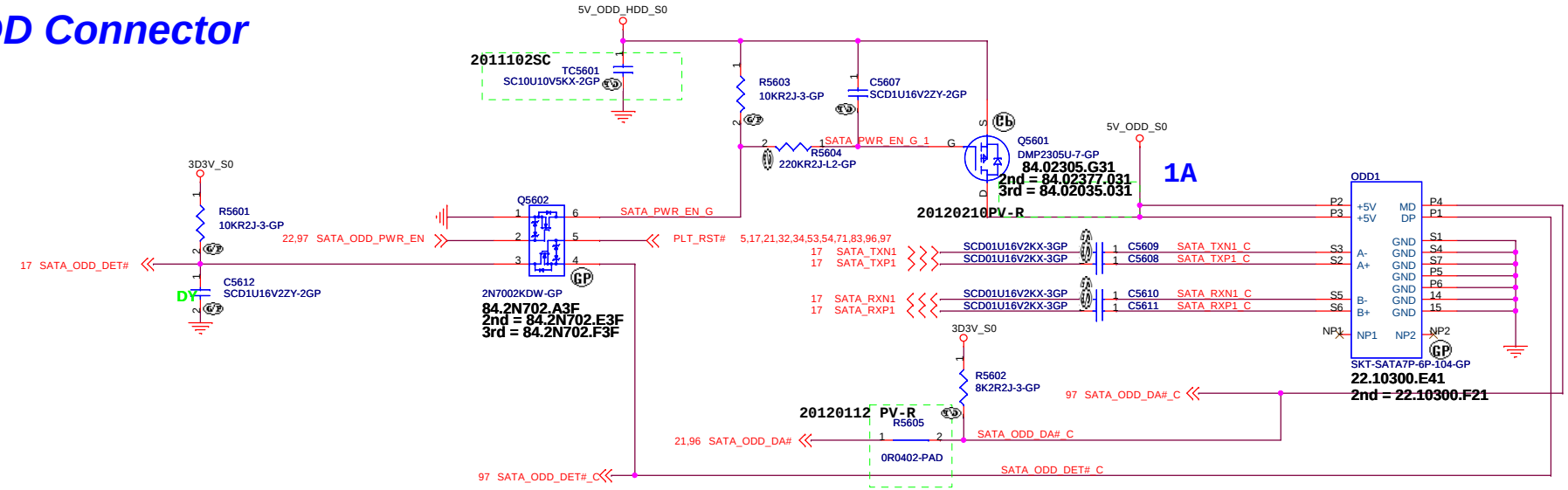
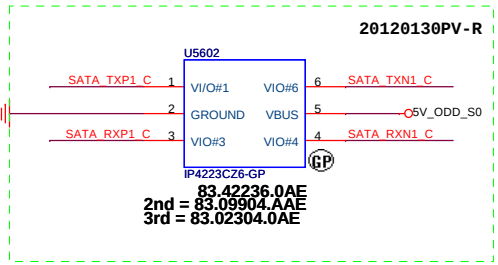
HDD Connector





ODD Connector





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 56 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***(Reserved)***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***(Reserved)***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 58 of 103

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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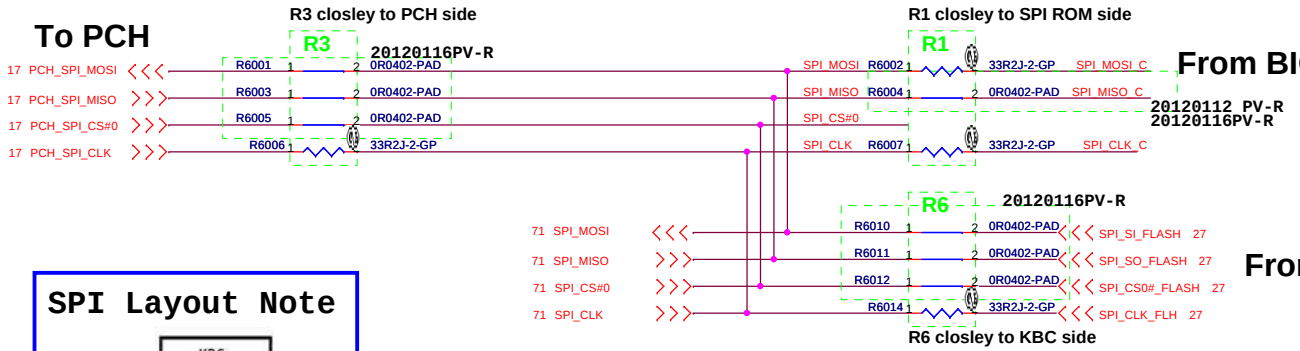
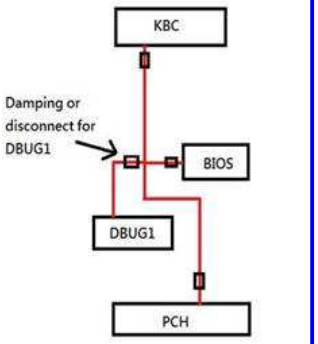
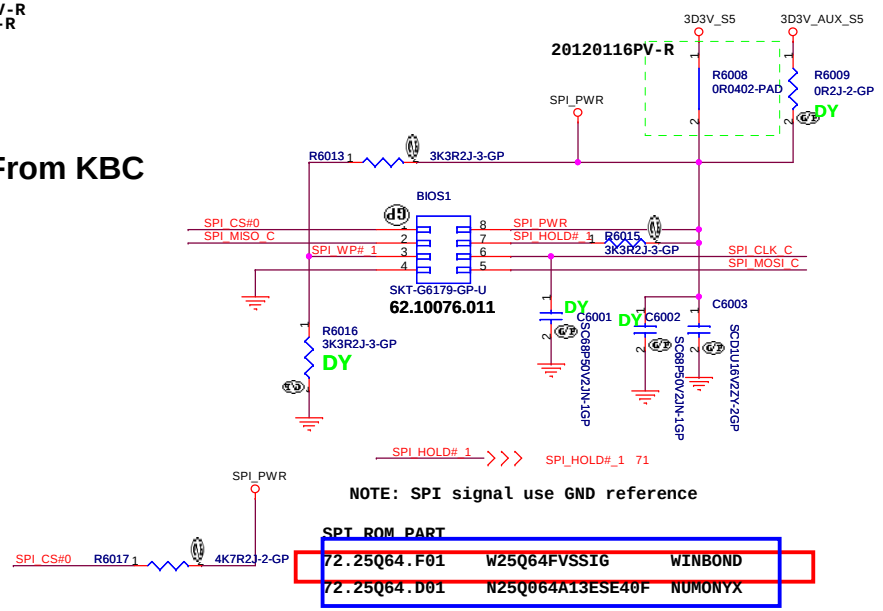
SSID = Flash.ROM



SPI Layout Note



SYSTEM SPI ROM Socket



NOTE: SPI signal use GND reference

SPI ROM PART

72.25Q64.F01	W25Q64FVSSIG	WINBOND
72.25Q64.D01	N25Q064A13ESE40F	NUMONYX

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Flash**

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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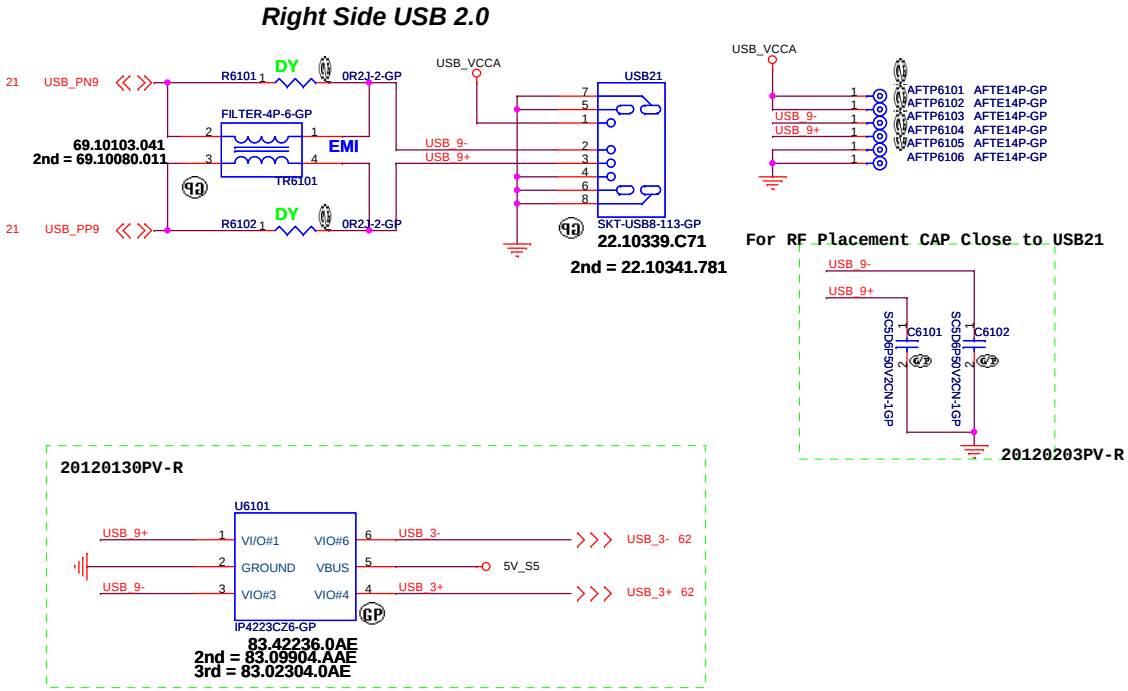
Right Side USB 2.0 Connector



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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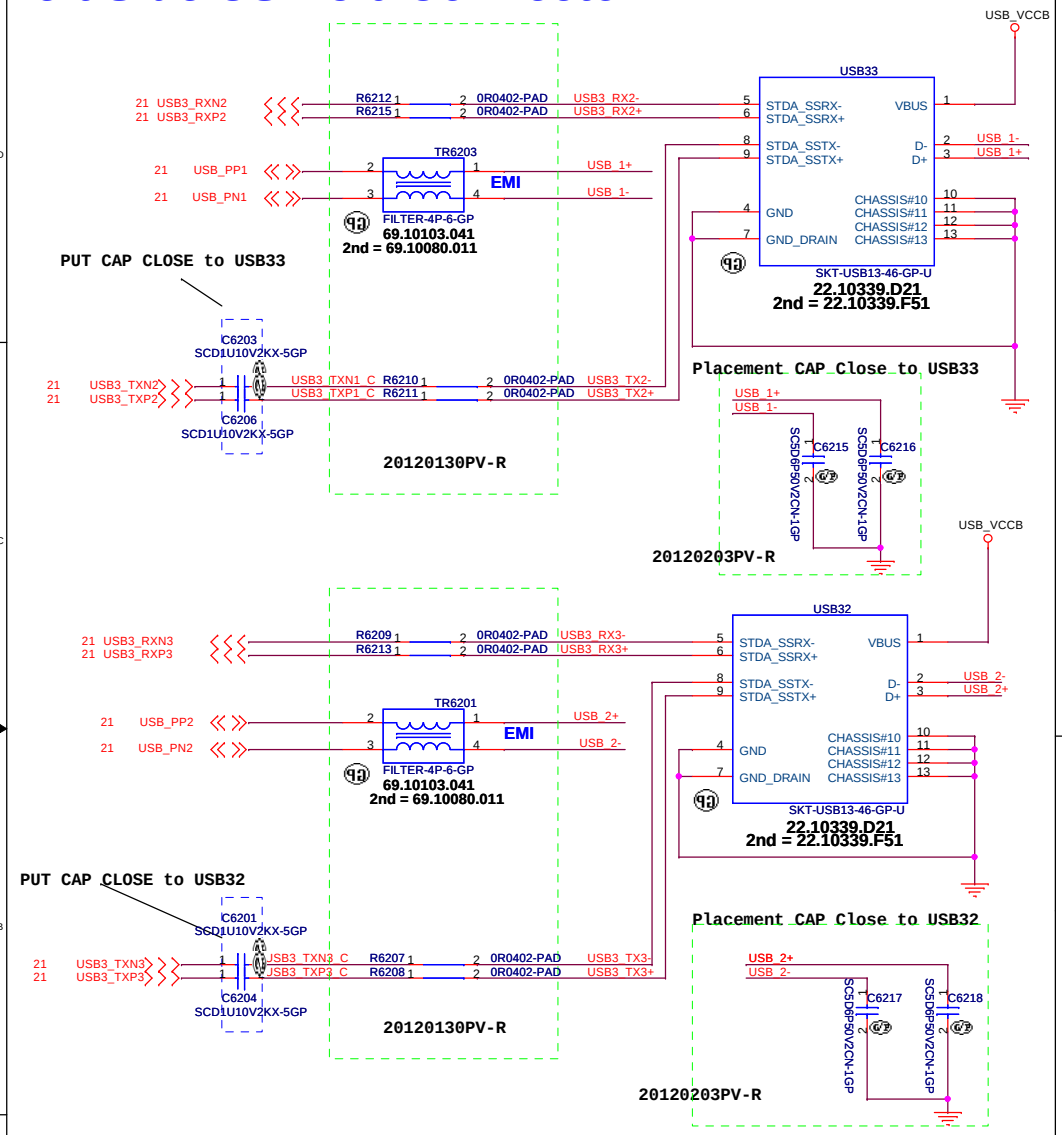
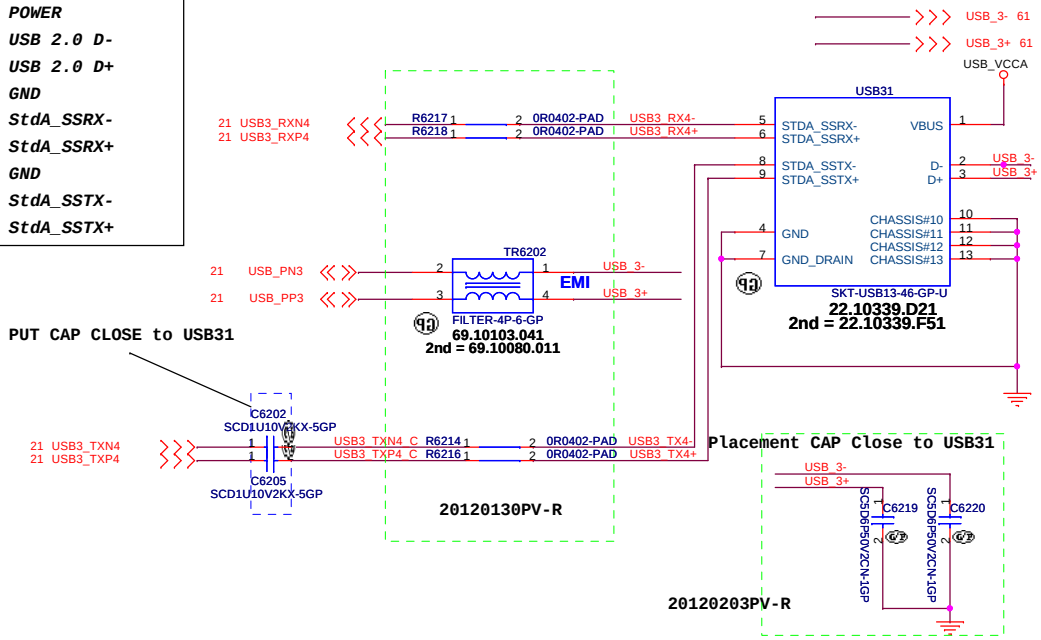
Left Side USB 3.0 Connector

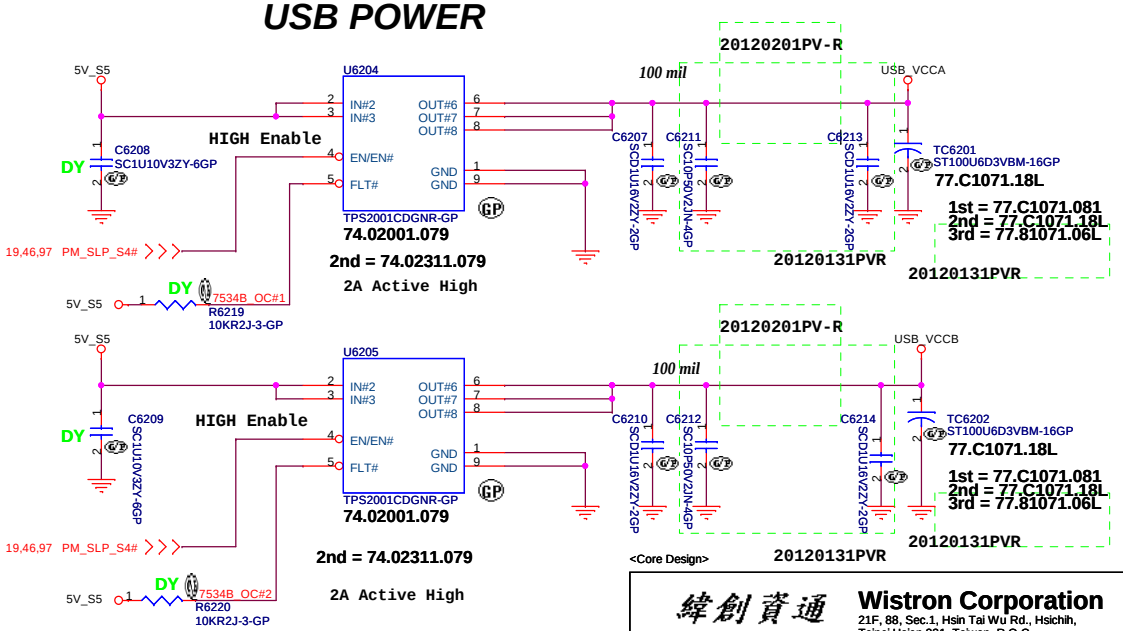


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

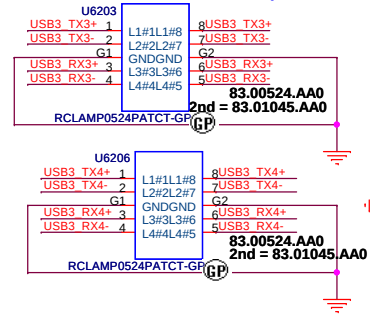
Right Side USB 3.0 Connector



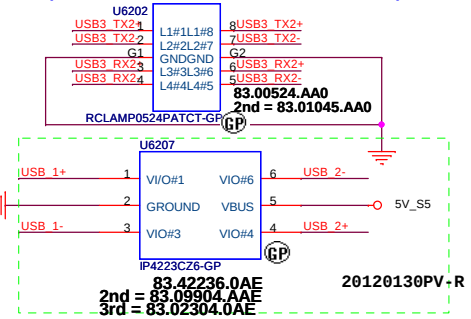
USB POWER



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB3.0**	
Size A3	Document Number **2012 S-Series Richie 13.3**	Rev -1
Date: Wednesday, March 14, 2012	Sheet 62 of 103	

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<Core Design>

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Title: ***(Reserved)***

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A3	2012 S-Series Richie 13.3	-1

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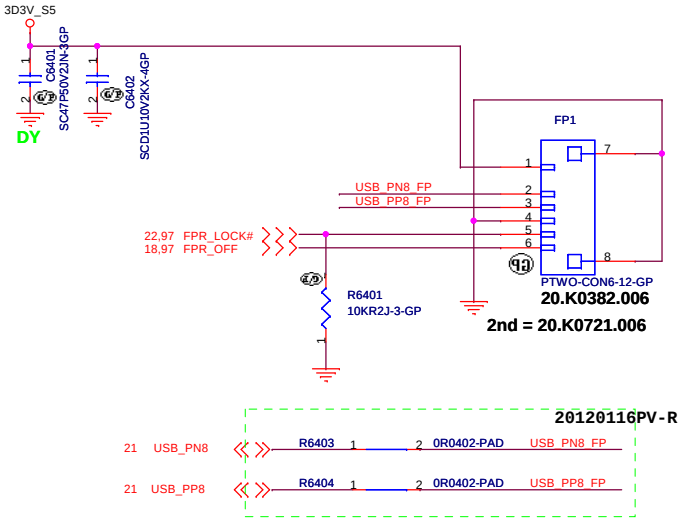
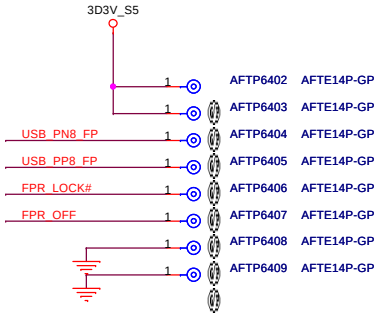
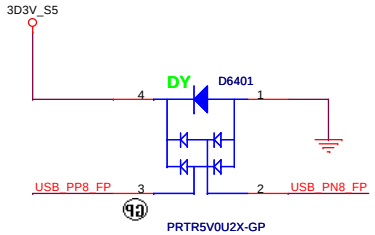
Finger Printer Connector







<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Finger Print Conn*		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
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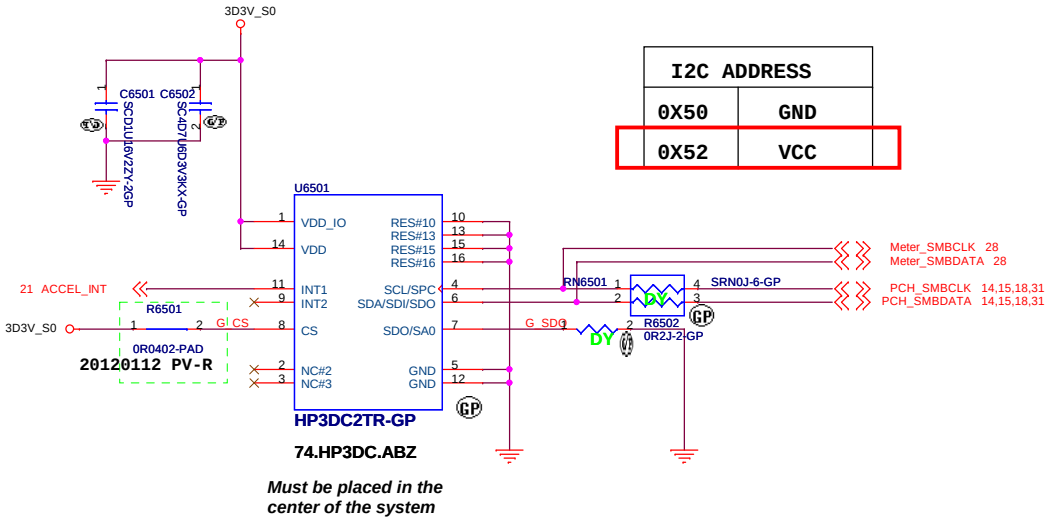
ACCELEROMETER



I2C ADDRESS	
0X50	GND
0X52	VCC

Must be placed in the center of the system

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ACCELEROMETER

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 65 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 66 of 103

(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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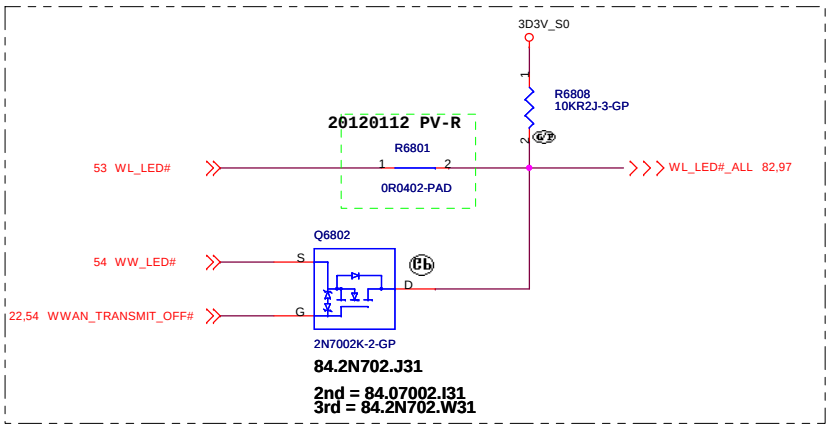
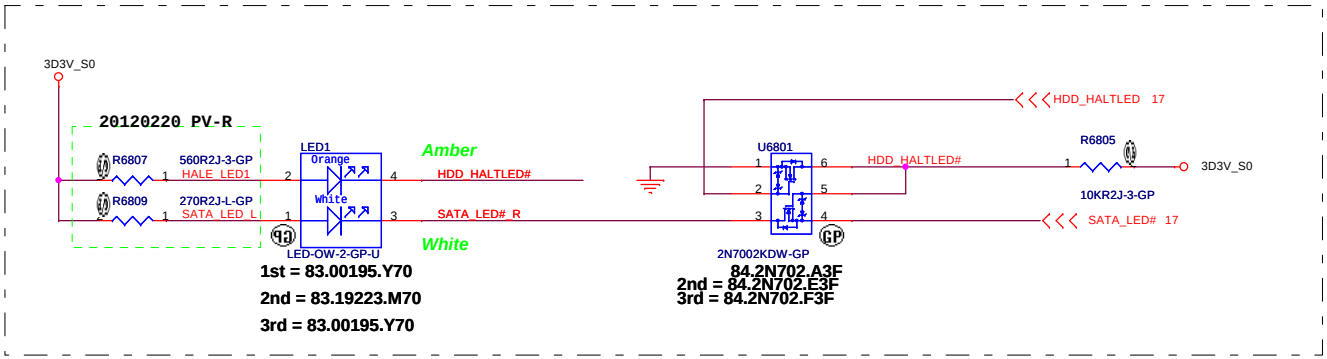
WLAN / WWAN POWER LED



HDD LED



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Control

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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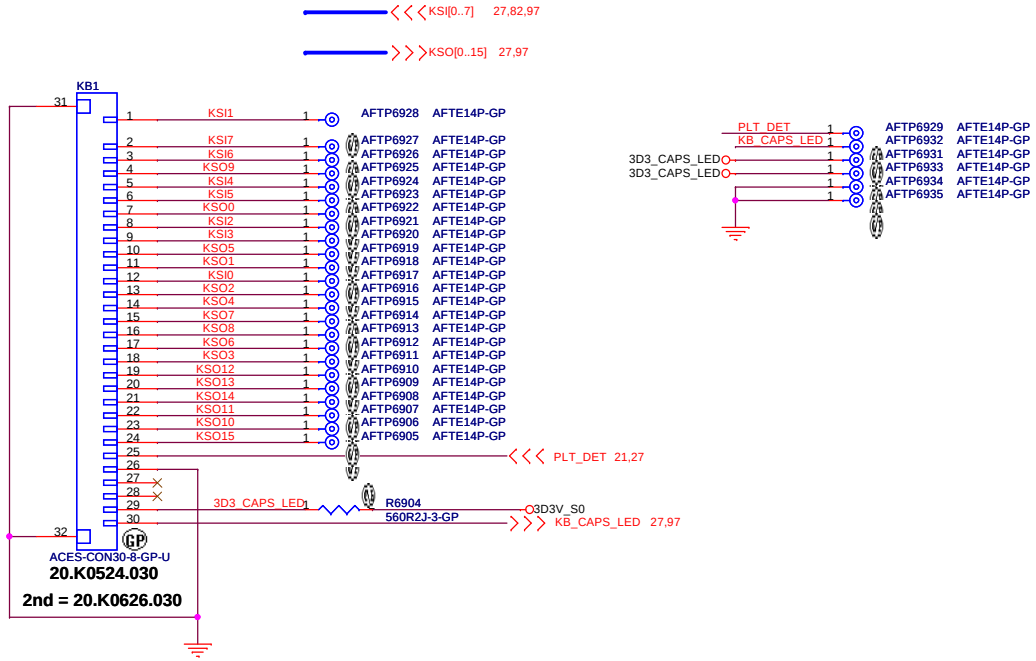
Keyboard Connector



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Key Board/Touch Pad***

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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(Blanking)

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***(Reserved)***

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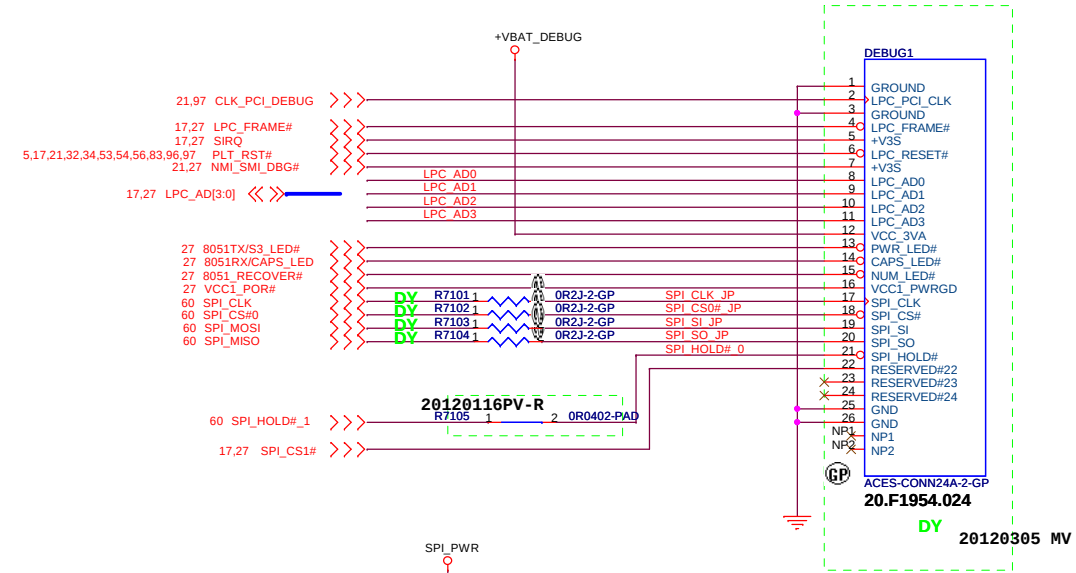
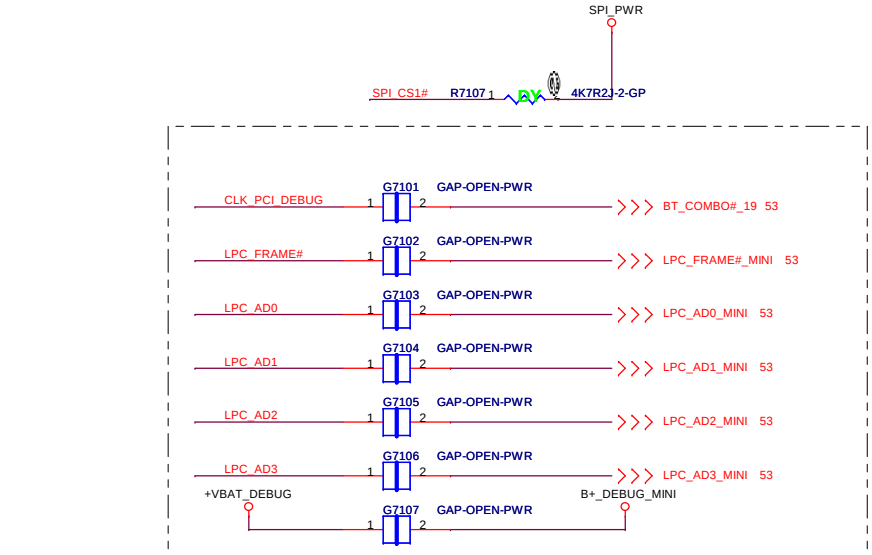
24 PIN LPC DEBUG CONN.





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Title: ***Dubug connector***

Size	Document Number	Rev
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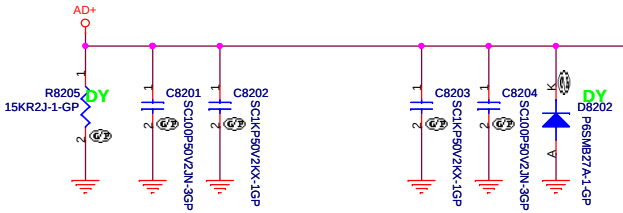
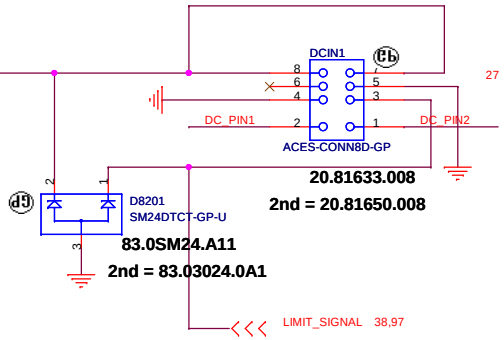
Adaptor in to generate DCBATOUT



83.P6SMB.KAG

2ND = 83.P6SBM.EAG



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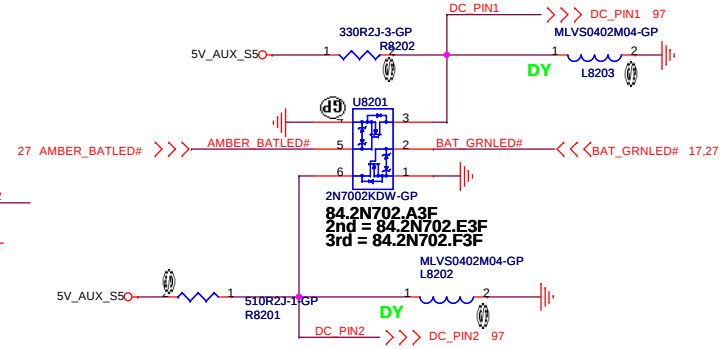
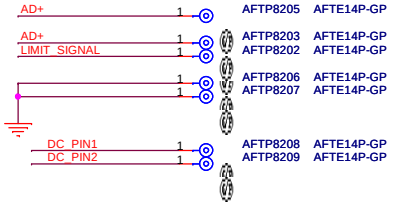
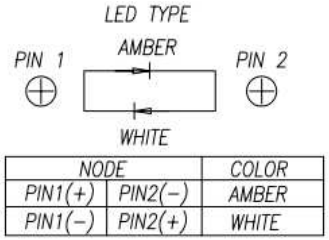
2nd = 20.81650.008

83.0SM24.A11

2nd = 83.03024.0A1



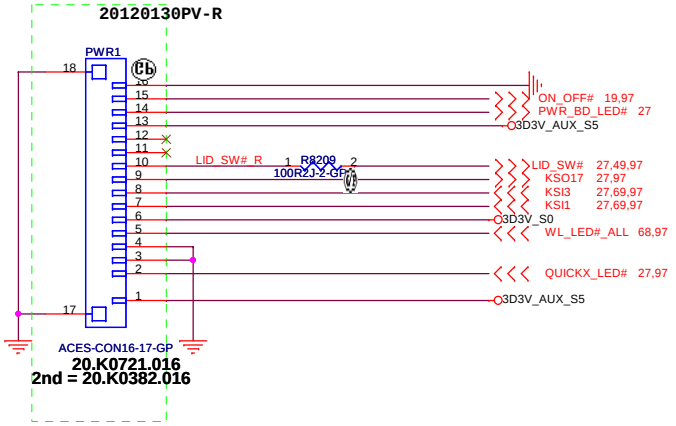




NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE

	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low

Power Button +Quick Lanch board



20.K0721.016

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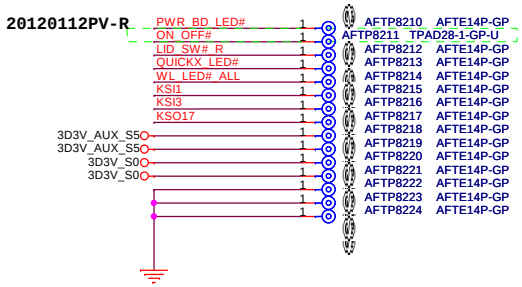

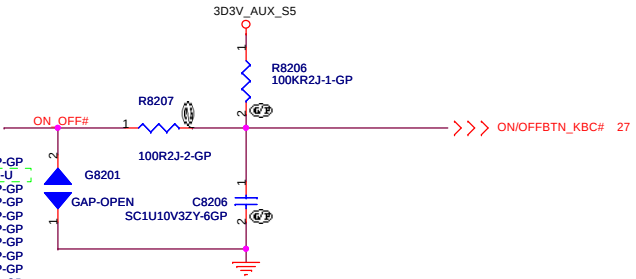

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Title: **POWER Button/ DCIN Connector**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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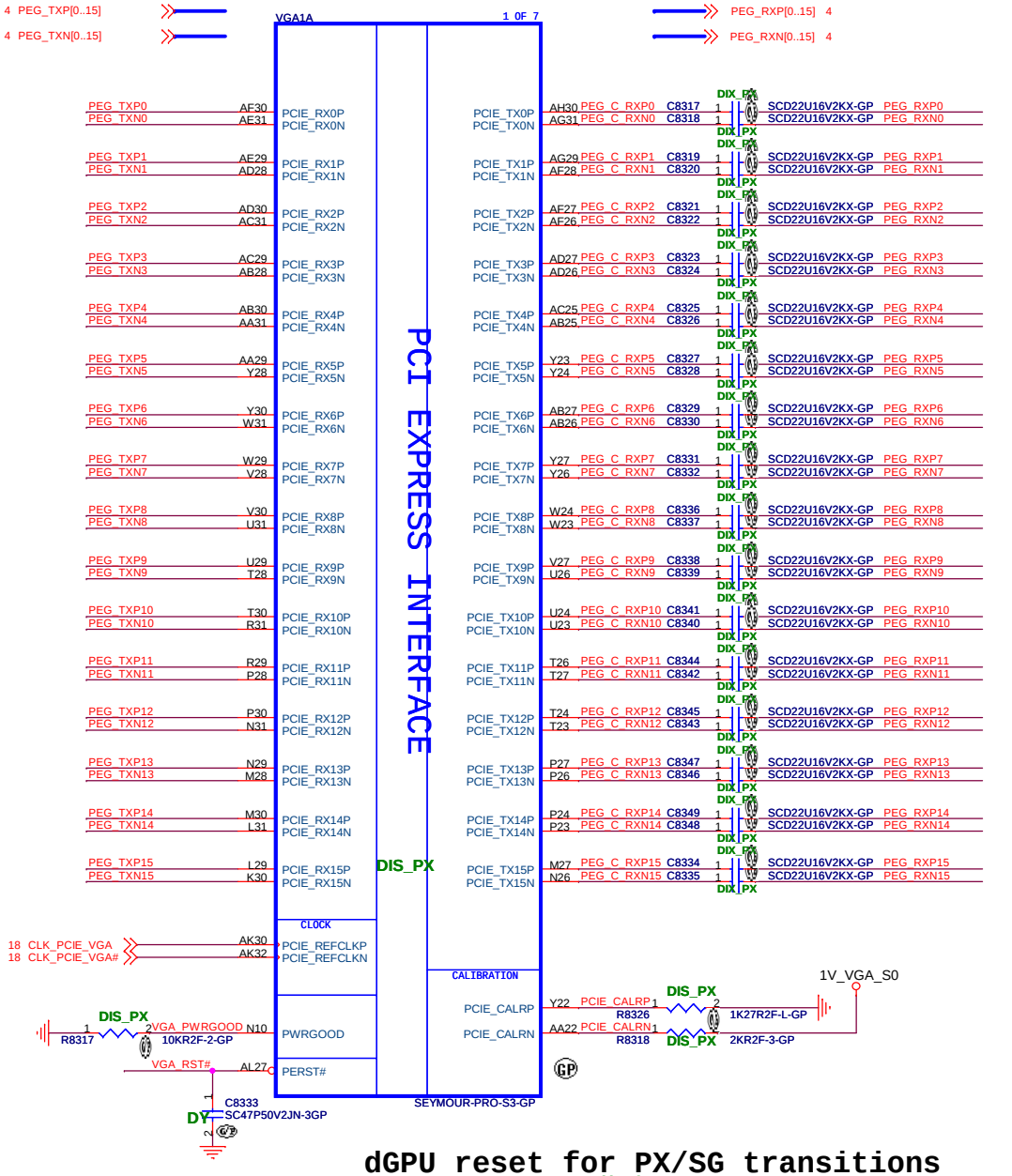
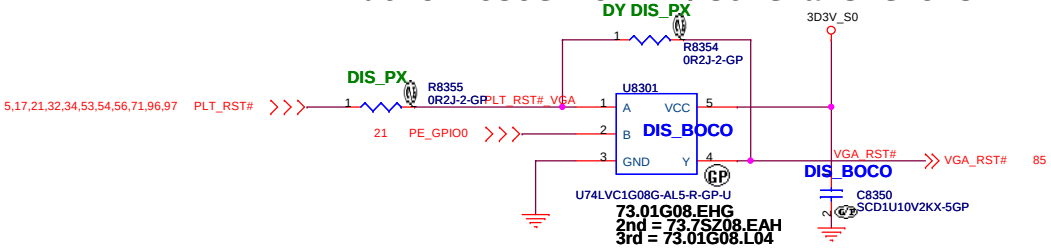


dGPU reset for PX/SG transitions

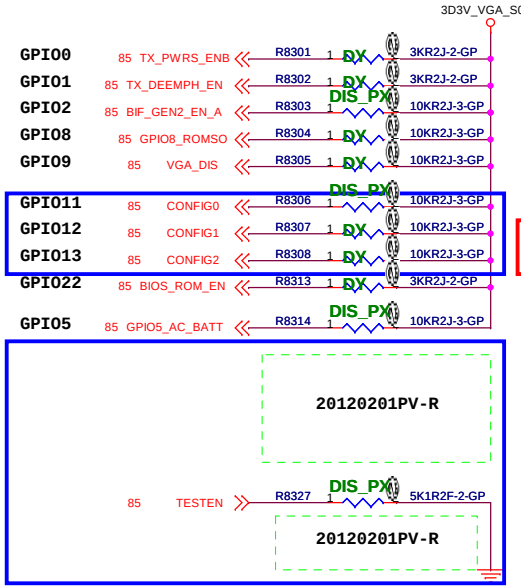


CONFIGURATION STRAPS

ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1



GPIO_13	GPIO_12	GPIO_11	Memory Aperture Size
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

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Title: **GPU PCIE/STRAPPING(1/5)**

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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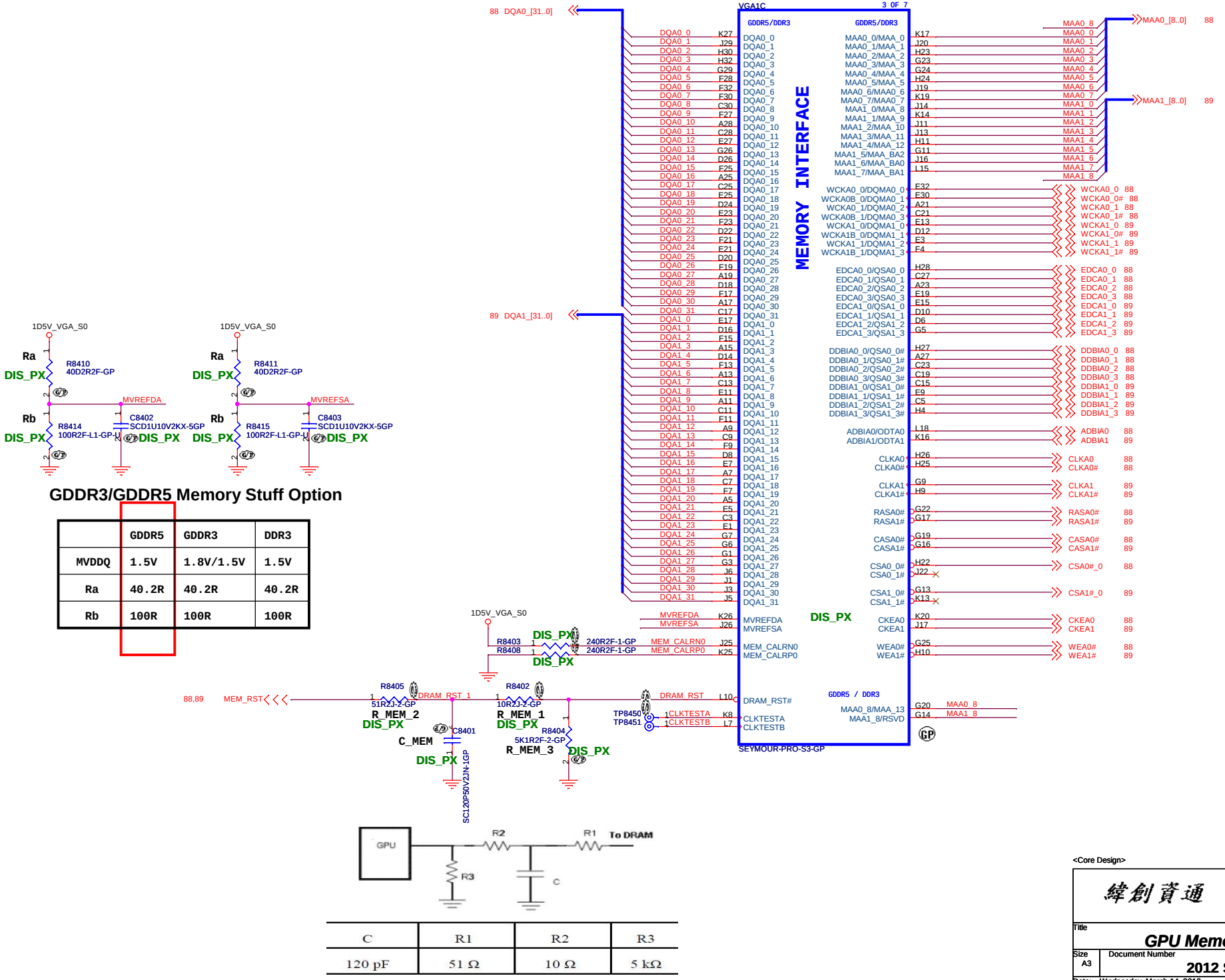

GDDR3/GDDR5 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

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Title: GPU Memory(2/5)

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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VRAM ID TABLE

MEM ID3	MEM ID2	MEM ID1	MEM ID0	MEM ID VALUE	Vendor & PN	DIE Ver
NC	NC	0	0	0	Samsung(128X16) K4G20325FC-HC04	C
NC	NC	1	0	2	Samsung(128X16) K4G20325FD-FC04	D
NC	NC	0	1	1	Hynix(128MX16) H5GQ2H24MFR-T2C	M
NC	NC	1	1	3	Hynix(128MX16) H5GQ2H24AFR-T2C	A
NC	NC	0	0	0	Elpida(128MX16) EDW2032BBBG-50-F	B
NC	NC	NC	NC	NC	UMA	

Reserve Pul-High Resistor for MEM_ID2/MEM_ID3

0= Old Die
1= New Die

VBIOS 1 : Samsung
VBIOS 2 : Hynix
VBIOS 3 : Elpida

GPU Power ID Table

GPU SIDE		UP1527QQDD
GPIO_15_PWRCNTL_0	GPIO_20_PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V

LVDS Interface

VGA1F 6 OF 7

LVDS CONTROL: VARY_BL, DIGON

LVTMDP: TXCLK_UP_DPF3P/N, TXOUT_U0P_DPF2P/N, TXOUT_U1P_DPF1P/N, TXOUT_U2P_DPF0P/N, TXOUT_U3P/N, TXCLK_LP_DPE3P/N, TXOUT_L0P_DPE2P/N, TXOUT_L1P_DPE1P/N, TXOUT_L2P_DPE0P/N, TXOUT_L3P/N

SEYMOUR-PRO-S3-GP

CTF setpoint is 118°C, and is programmed during ASIC initialization.

Intel is H_THERMTRIP#

SSEL1 (Pin 3)	SSEL0 (Pin 7)	Spread Percent (%) SSCLK (Pin 5)
Low (VSS)	Low (VSS)	Spread Off (No Spread)
Low (VSS)	Middle (Floating)	-0.50%
Low (VSS)	High (VDD)	-2.5%
Middle (Floating)	Low (VSS)	-0.25%
Middle (Floating)	Middle (Floating)	-0.75%
Middle (Floating)	High (VDD)	-1.0%
High (VDD)	Low (VSS)	-1.5%
High (VDD)	Middle (Floating)	-2.0%
High (VDD)	High (VDD)	-3.0%

Recommended Clock-Input Configurations

Memory Type	Description
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

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Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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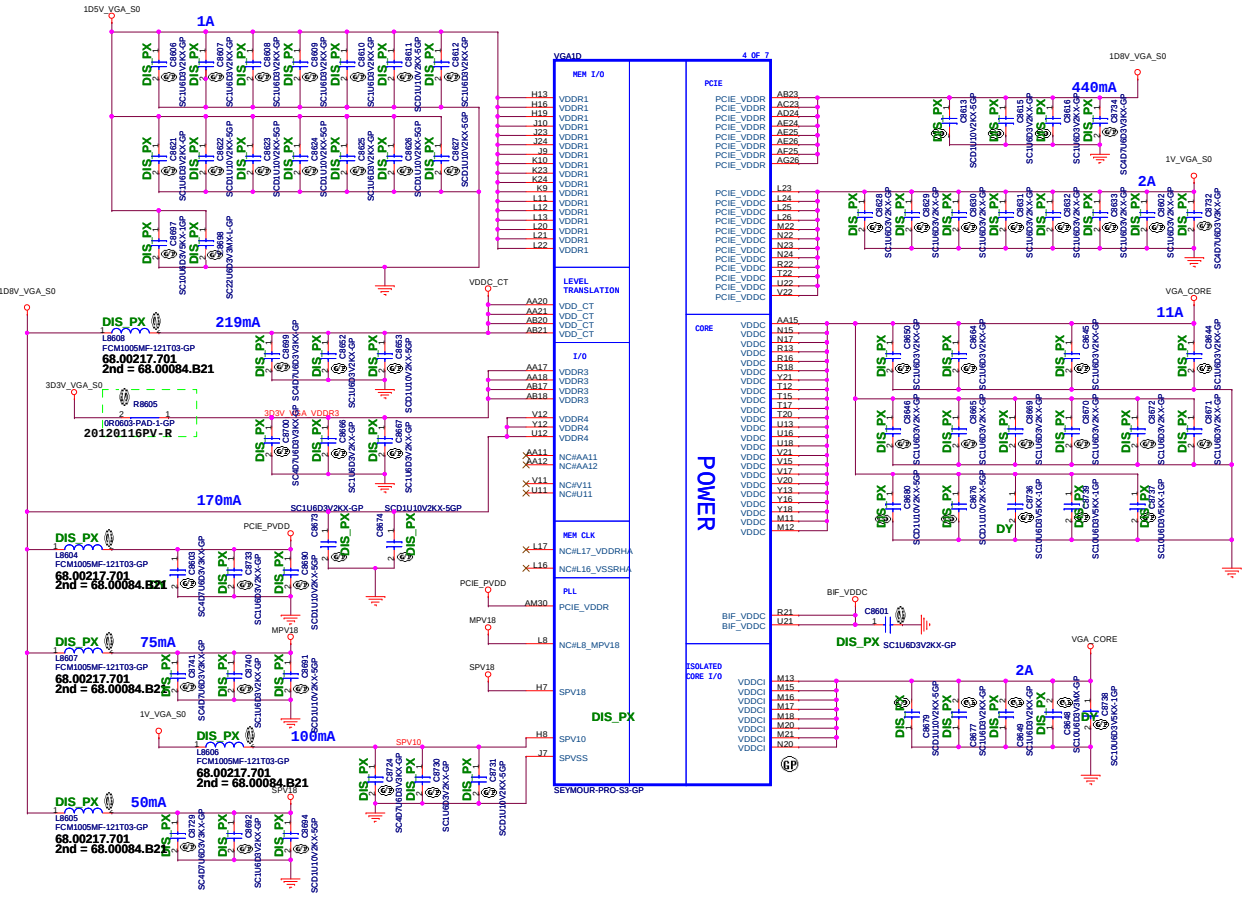
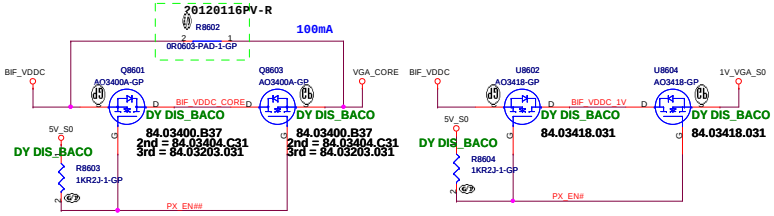
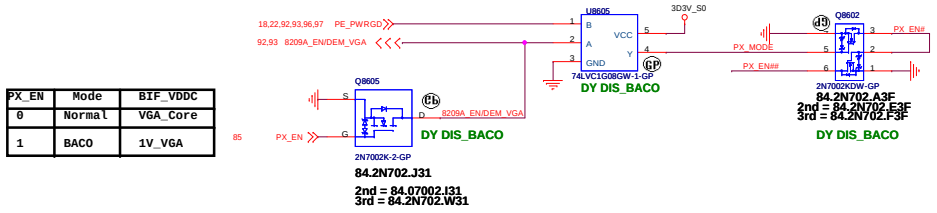




	PX_EN	8209A_EN/DEM_VGA	PX_MODE	PX_EN#	PX_EN##	BIF_VDDC
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE



PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

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Title: GPU_POWER(4/5)

Size	Document Number	Rev
A2	2012 S-Series Richie 13.3	-1

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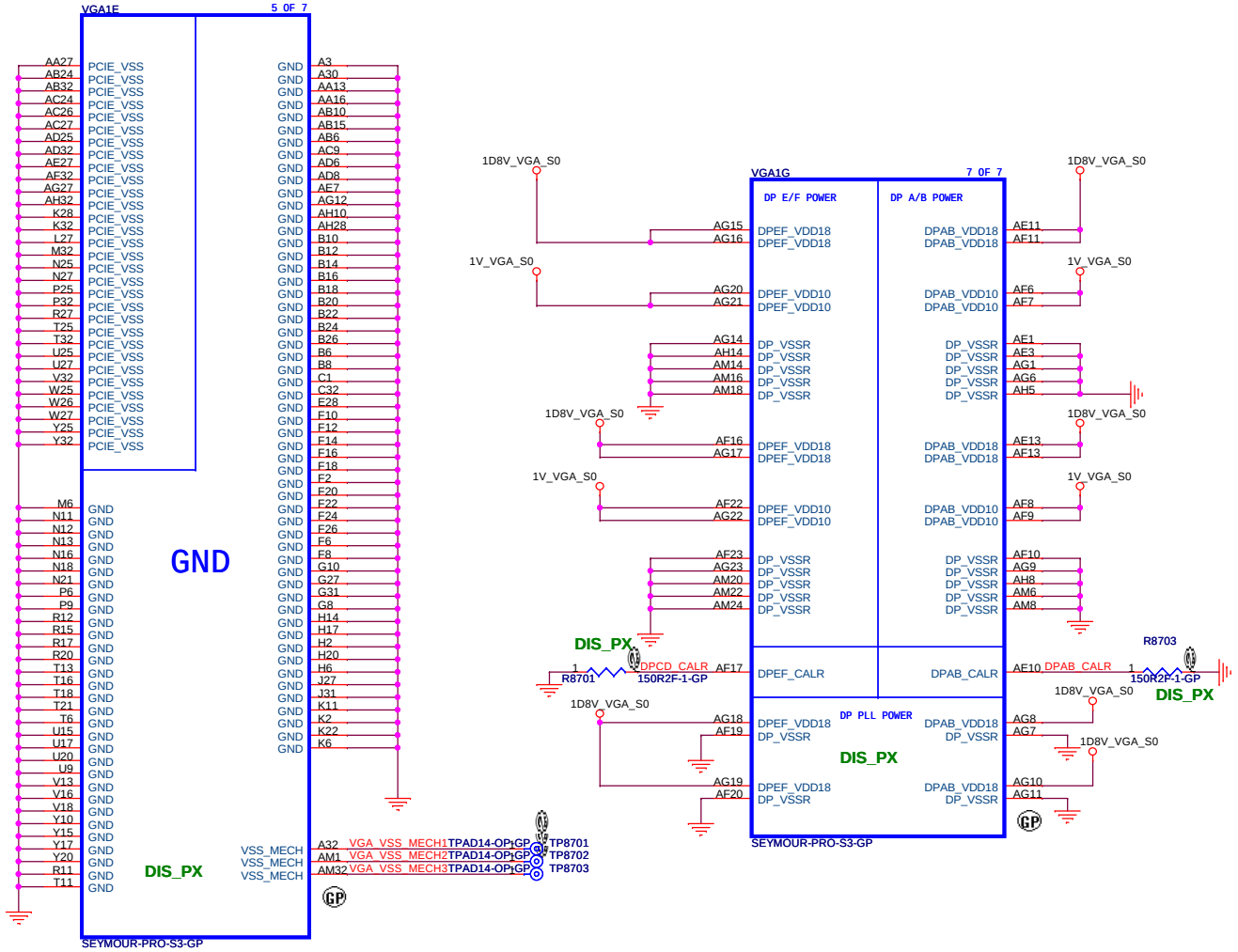

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Title: **GPU_DPPWR/GND(5/5)**

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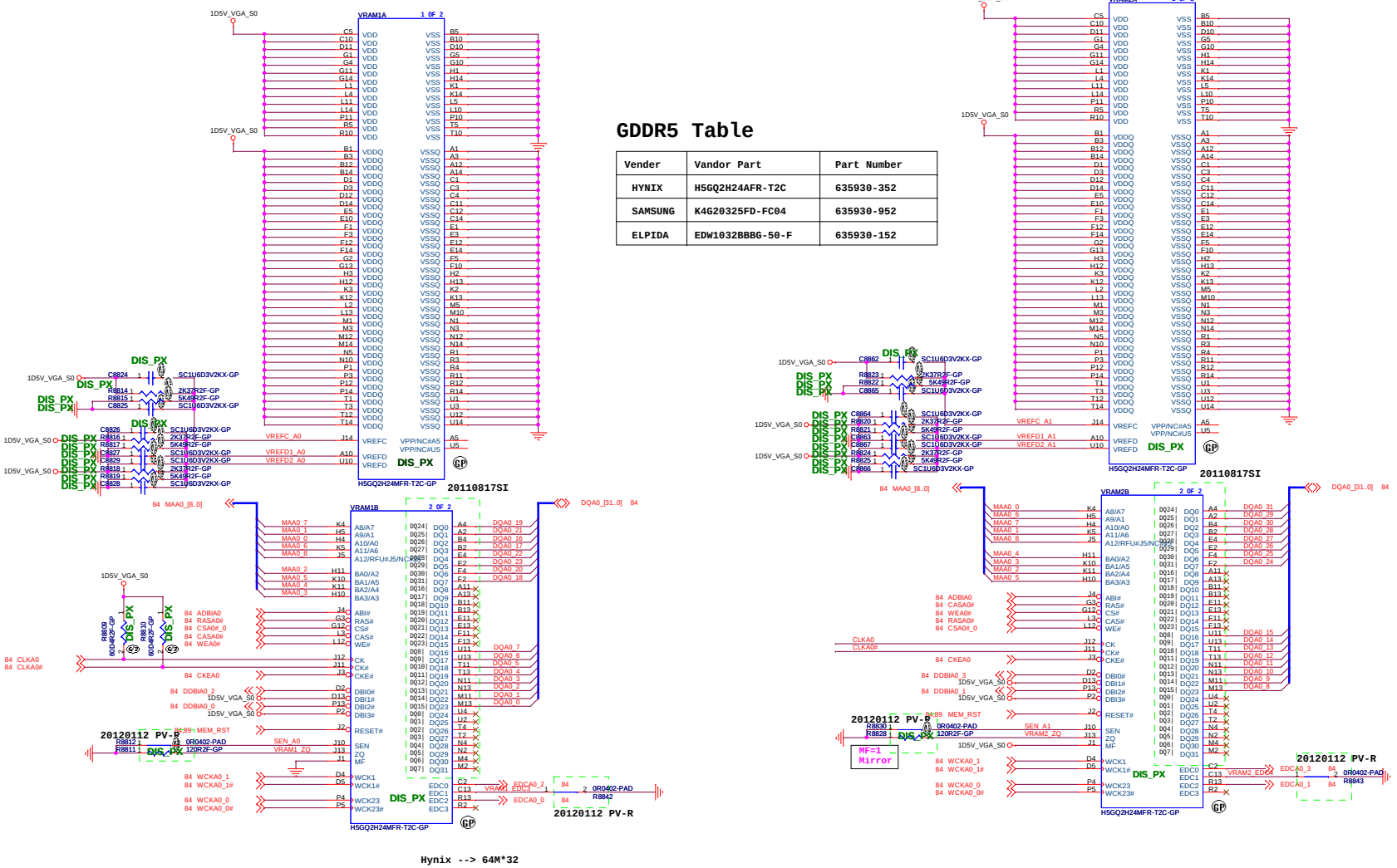
GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24AFR-T2C	635930-352
SAMSUNG	K4G20325FD-FC04	635930-952
ELPIDA	EDW1032BBBG-50-F	635930-152



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<Core Design>
Title: GPU-VRAM1,2 (1/4)
Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
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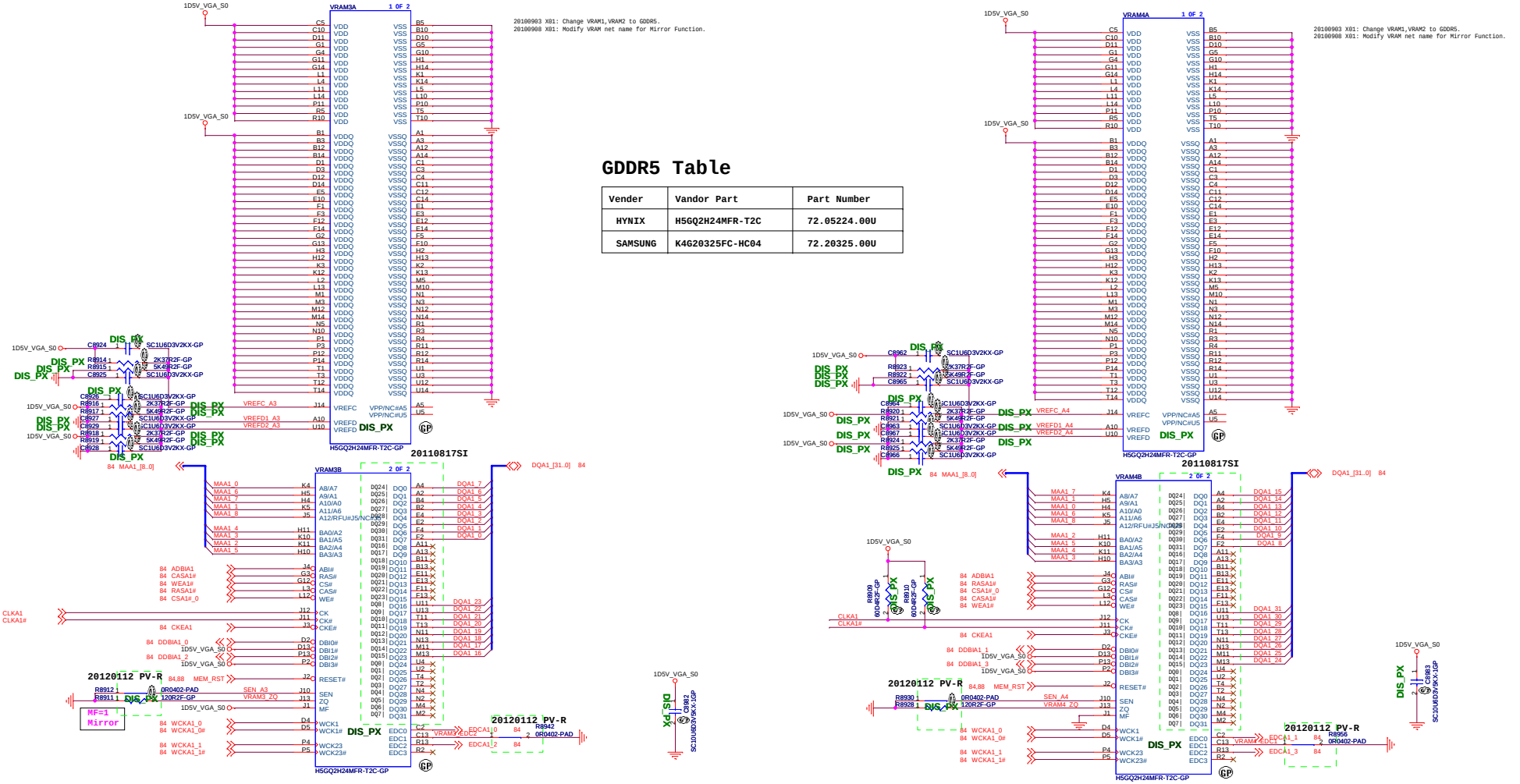

GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24MFR-T2C	72.05224.00U
SAMSUNG	K4G20325FC-HC04	72.20325.00U

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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
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Title: ***(Reserved) GPU-VRAM5,6 (3/4)***

Size	Document Number	Rev
A3	**2012 S-Series Richie 13.3**	-1

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Title: ***(Reserved) GPU-VRAM7,8 (4/4)***

Size	Document Number	Rev
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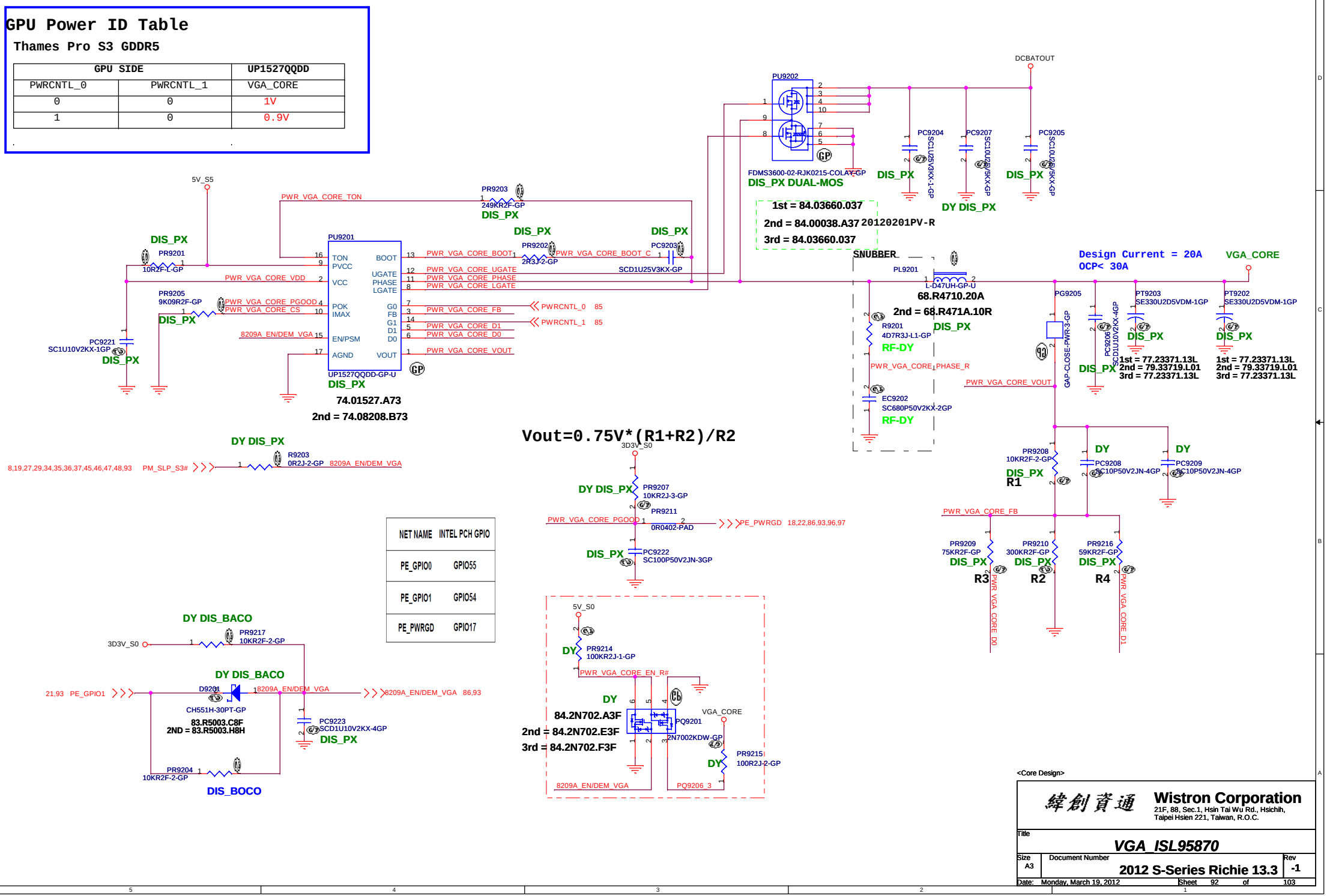
+VGA_CORE

GPU Power ID Table

Thames Pro S3 GDDR5

GPU SIDE		UP1527QQDD
PWRCNTL_0	PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V



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Title: VGA_ISL95870

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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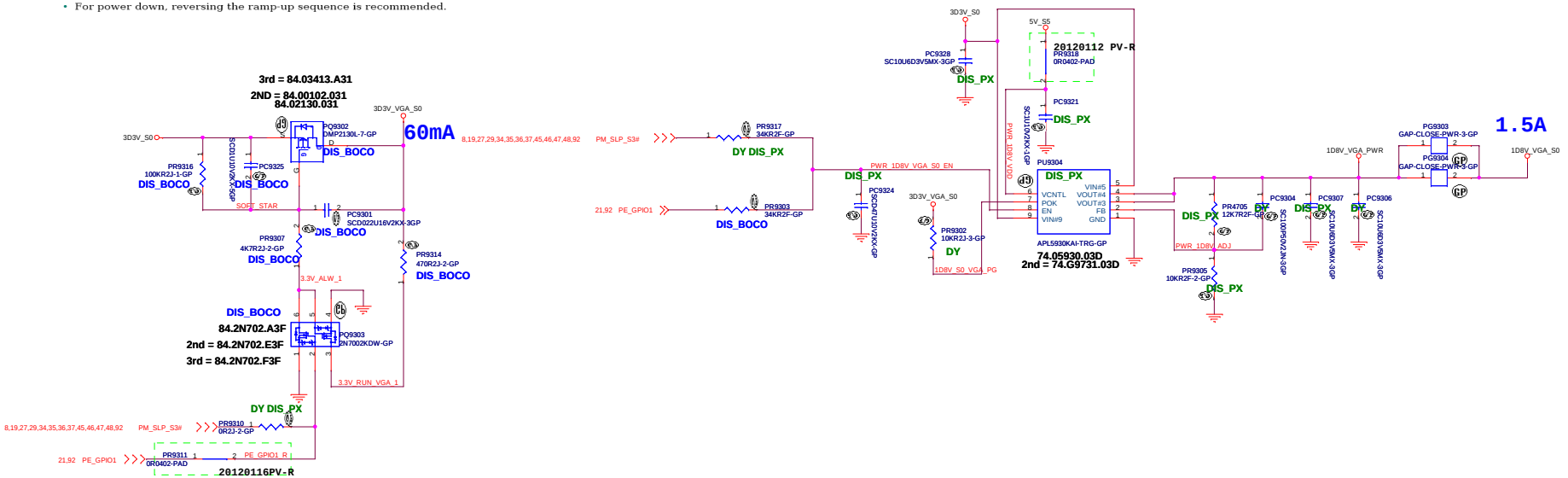
5.3 Power-Up/Down Sequence

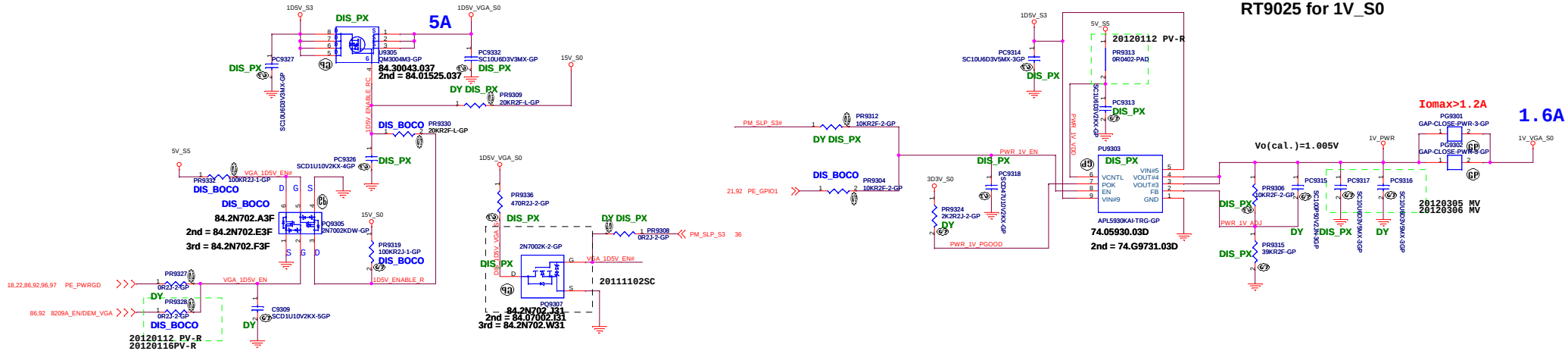
Seymour has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for **VDDR3**, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of **VDDR3** relative to other power rails.
- The external pull-up resistors on the **DDC/AUX** signals (if applicable) should ramp up before or after both **VDDC** and **VDD_CT** have ramped up.
- **VDDC** and **VDD_CT** should not ramp up simultaneously. For exmaple, **VDDC** should reach 90% before **VDD_CT** starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0



1D5V_VGA_S0



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Title: DISCRETE VGA POWER

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A2	2012 S-Series Richie 13.3	-1

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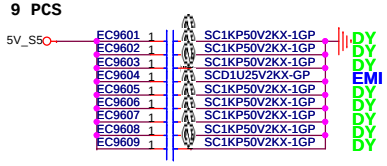
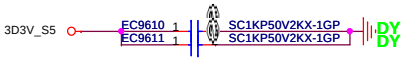
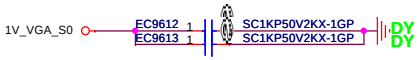
5V_S5 9 PCS



1D8V_PWR 2 PCS



1V_VGA_S0 2 PCS



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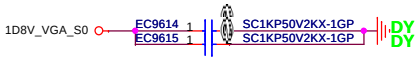
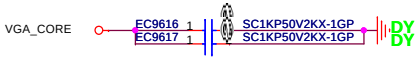
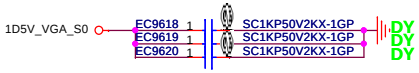


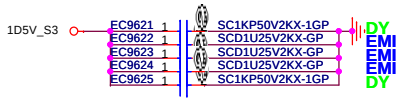
VGA_CORE 2 PCS



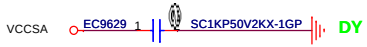
1D5V_VGA_S0 2 PCS



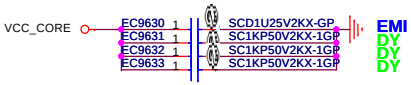
1D5V_S3 8 PCS



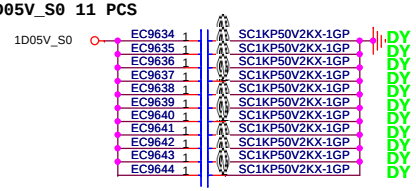
VCCSA 1 PCS



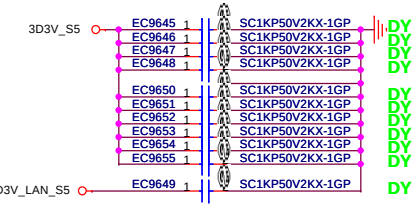
VCC_CORE 4 PCS



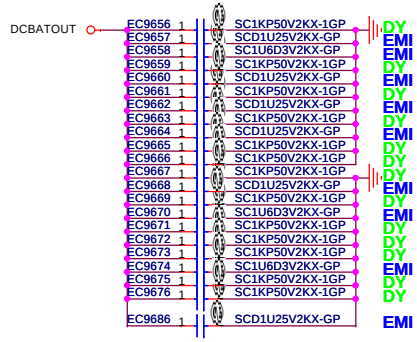
1D05V_S0 11 PCS

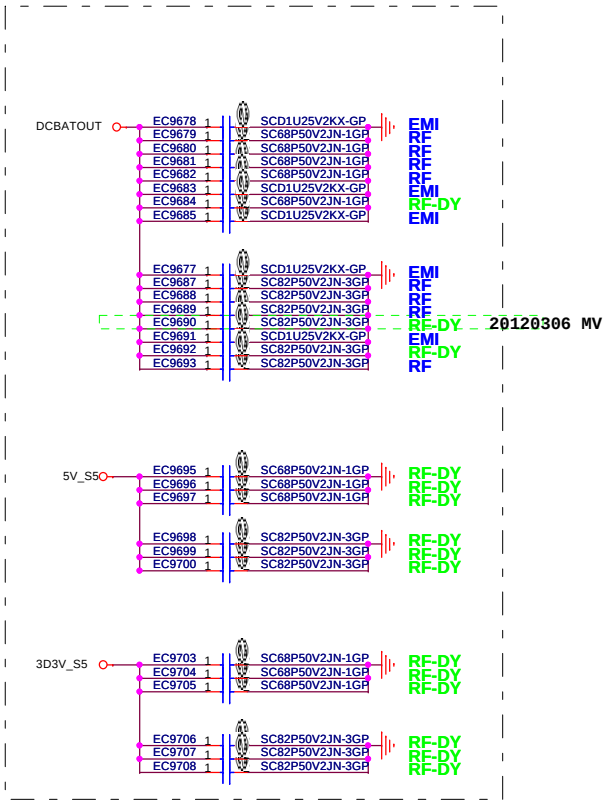


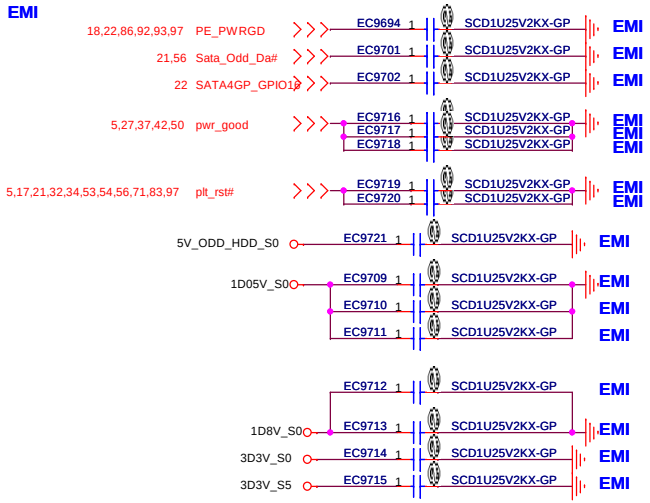
3D3V_S5 11 PCS



DCBATOUT 21 PCS







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PAGE 14_DIMM1 EMI CAP

5,14,15 DDR3_DRAMRST# — EC1428 — SC1KP50V2KX-1GP — DY

PAGE 15_DIMM1 EMI CAP

5,14,15 DDR3_DRAMRST# — EC1524 — SC1KP50V2KX-1GP — DY

PAGE 17_PCH(1/9)

17,29 HDA_BITCLK_CODEC — EC1701 — SC22P50V2JN-4GP — DY
17,29 HDA_SDOUT_CODEC — EC1702 — SC22P50V2JN-4GP — DY

PAGE 27_KBC

22,27 KBrst# — EC2701 — SC1KP50V2KX-1GP — DY
19,27 Pm_Pwrok — EC2702 — SC1KP50V2KX-1GP — DY
19,27,41 Rsmrst# — EC2703 — SC1KP50V2KX-1GP — DY

PAGE 29_AUDIO CODEC EMI CAP

17,29 HDA_RST#_CODEC — EC2901 — SC1KP50V2KX-1GP — DY

PAGE 31_AUDIO CONNECTOR EMI CAP

30,31 MIC_IN_R — EC3111 — SC100P50V2JN-1-GP — DY
30,31 MIC_IN_L — EC3112 — SC100P50V2JN-1-GP — DY
29,31 HP_OUT_L — EC3113 — SC100P50V2JN-1-GP — DY
29,31 HP_OUT_R — EC3114 — SC100P50V2JN-1-GP — DY — AUD_AGND

20120130PV-R

AVDD_CODEC — EC3115 — SC1U6D3V2KX-GP — AUD_AGND — DY
5V_S0 — EC3107 — SCD1U16V2ZY-2GP — DY

DY — EC3108 — SC1KP50V2KX-1GP — AUD_AGND
DY — EC3109 — SC1KP50V2KX-1GP
DY — EC3110 — SC1KP50V2KX-1GP

PAGE 32_Card Reader EMI CAP

32,33 MDIF5 — EC3201 — SC22P50V2JN-4GP — DY

CLOSE U3201 PIN1

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC3212 — SC100P50V2JN-L-GP — DY

PAGE 33_SD/MS/MMC CONNECTOR EMI CAP

CLOSE CARD1

22,32 D3E_WAKE — EC3307 — SC1KP50V2KX-1GP — DY
32,33 MS_INS# — EC3308 — SC1KP50V2KX-1GP — DY
32,33 MDIF2 — EC3306 — SC22P50V2JN-4GP — DY
32,33 MDIF1 — EC3305 — SC22P50V2JN-4GP — DY
32,33 MDIF0 — EC3304 — SC22P50V2JN-4GP — DY
32,33 MDIF3 — EC3303 — SC22P50V2JN-4GP — DY

PAGE 34_Lan RTL8111E EMI CAP

CLOSE U3401 Pin25

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC3401 — SCD1U25V2KX-GP — EMI

PAGE 35_LAN RJ45 EMI CAP

34,35 GREEN_LED# — EC3502 — SCD1U16V2ZY-2GP — DY
34,35 YELLOW_LED# — EC3501 — SCD1U16V2ZY-2GP — DY

PAGE 39_BATT CONN EMI CAP

27,39 AB1A_DATA — EC3901 — SC22P50V2JN-4GP — DY
27,39 AB1A_CLK — EC3902 — SC22P50V2JN-4GP — DY
27,39 MAIN_BAT_DET# — EC3903 — SC1KP50V2KX-1GP — DY
39 MAIN_BAT_DET#_C — EC3904 — SC1KP50V2KX-1GP — DY

PAGE 49_LVDS EMI CAP

20,49 LCDVDD_EN — EC4911 — SC1KP50V2KX-1GP — DY
49 DISP_OFF# — EC4912 — SC1KP50V2KX-1GP — DY
27,49,82 LID_SW# — EC4913 — SC1KP50V2KX-1GP — DY
20,49 LCD_BL_EN — EC4914 — SC1KP50V2KX-1GP — DY
29,49 DMIC_DATA — EC4904 — SC33P50V2JN-3GP — DY
29,49 DMIC_CLK — EC4905 — SC33P50V2JN-3GP — DY

PUT CLOSE R4911

DCBATOUT — EC4915 — SCD1U50V3KX-GP — DY
+LCDVDD — EC4916 — SCD1U16V2ZY-2GP — DY
3D3V_S0 — EC4903 — SC1U6D3V2KX-GP — DY
EC4902 — SC1U6D3V2KX-GP — DY
EC4901 — SC1U6D3V2KX-GP — DY

PAGE 50_CRT EMI CAP

5V_S0 — EC5011 — SCD1U50V3KX-GP — DY

PAGE 51_HDMI EMI CAP

20,51 HDMI_PCH_DET — EC5101 — SC1KP50V2KX-1GP — DY

PAGE 53_WLAN SLOT EMI CAP

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC5303 — SC100P50V2JN-L-GP — DY
53 XMIT_OFF_R — EC5301 — SC1KP50V2KX-1GP — DY
22,53 BT_OFF# — EC5302 — SC1KP50V2KX-1GP — DY

PAGE 54_WLAN SLOT EMI CAP

CLOSE WWAN1

22,54 GPS_XMIT_OFF# — EC5401 — SC1KP50V2KX-1GP — DY
17,54 INTRUDER# — EC5402 — SC1KP50V2KX-1GP — DY
54 WIFI_RF_EN# — EC5403 — SC1KP50V2KX-1GP — DY
5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC5404 — SC100P50V2JN-L-GP — DY

PAGE 56_HDD/ODD EMI CAP

5V_S0 — EC5601 — SC1U10V3ZY-6GP — DY
22,56 SATA_ODD_PWR_EN — EC5615 — SC1KP50V2KX-1GP — DY
56 SATA_ODD_DET#_C — EC5613 — SC1KP50V2KX-1GP — DY
56 SATA_ODD_DA#_C — EC5614 — SC1KP50V2KX-1GP — DY

PAGE 61_USB2.0 EMI CAP

CLOSE USB21

USB_VCCA — EC6102 — SCD1U16V2ZY-2GP — DY

PAGE 62_USB3.0 EMI CAP

USB_VCCA — EC6202 — SC1U10V3ZY-6GP — DY
USB_VCCB — EC6201 — SC1U10V3ZY-6GP — DY
EC6203 — SC1U10V3ZY-6GP — DY

PAGE 64_FINGER PRINT EMI CAP

22,64 FPR_LOCK# — EC6404 — SC1KP50V2KX-1GP — DY
18,64 FPR_OFF — EC6405 — SC1KP50V2KX-1GP — DY

PAGE 82_DCIN EMI CAP

38,82 LIMIT_SIGNAL — EC8206 — SC1KP50V2KX-1GP — EMI
82 DC_PIN1 — EC8209 — SC1U25V3KX-1-GP — EMI
82 DC_PIN2 — EC8210 — SC1U25V3KX-1-GP — EMI
27,82 QUICKX_LED# — EC8212 — SC1KP50V2KX-1GP — EMI
19,82 ON_OFF# — EC8213 — SC1KP50V2KX-1GP — EMI
27,49,82 LID_SW# — EC8214 — SC1KP50V2KX-1GP — EMI
68,82 WL_LED#_ALL — EC8215 — SCD1U16V2ZY-2GP — DY

AD+ — EC8202 — SC1U25V3KX-1-GP — DY — EMI
EC8201 — SC1U25V3KX-1-GP — DY — EMI

CLOSE PWR1

27,69,82 KSI1 — EC8216 — SC1KP50V2KX-1GP — EMI
27,69,82 KSI3 — EC8217 — SC1KP50V2KX-1GP — EMI
27,82 KSO17 — EC8218 — SC1KP50V2KX-1GP — EMI

3D3V_S0 — EC8207 — SC1KP50V2KX-1GP — EMI
EC8211 — SCD1U25V2KX-GP — EMI
3D3V_AUX_S5 — EC8205 — SC1KP50V2KX-1GP — EMI
EC8208 — SCD1U25V2KX-GP — EMI

PAGE 40-48,92_POWER EMI CAP

CLOSE TO PU4005 — DCBATOUT — EC4001 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4301 — DCBATOUT — EC4301 — SCD1U50V3KX-GP — DY
CLOSE TO PU4303 — DCBATOUT — EC4303 — SCD1U50V3KX-GP — DY
CLOSE TO PU4401 — DCBATOUT — EC4401 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4501 — DCBATOUT — EC4501 — SCD1U50V3KX-GP — DY
CLOSE TO PU4601 — DCBATOUT — EC4601 — SCD1U50V3KX-GP — DY
CLOSE TO PU4701 — DCBATOUT — EC4701 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4801 — DCBATOUT — EC4801 — SCD1U25V2KX-GP — EMI
CLOSE TO PU9202 — DCBATOUT — EC9201 — SCD1U50V3KX-GP — DY

PAGE 62_USB3.0 EMI CAP

CLOSE USB31 — USB_VCCA — EC6215 — SCD1U16V2ZY-2GP — DY
CLOSE USB32 — USB_VCCB — EC6214 — SCD1U16V2ZY-2GP — DY
CLOSE USB33 — USB_VCCB — EC6213 — SCD1U16V2ZY-2GP — DY

19,46,62 PM_SLP_S4# — EC6212 — SC1KP50V2KX-1GP — DY

CLOSE U6205

19,46,62 PM_SLP_S4# — EC6211 — SC1KP50V2KX-1GP — DY

PAGE 69_KEYBOARD/TOUCH PAD EMI CAP

20120112 PV-R

SRC1KP50VM-GP EC6904 — KSI3 KSO5 KSO1 KSI0 — EMI
SRC1KP50VM-GP EC6903 — KSO2 KSO4 KSO7 KSO8 — EMI
SRC1KP50VM-GP EC6906 — KSO6 KSO3 KSO12 KSO13 — EMI
SRC1KP50VM-GP EC6905 — KSO14 KSO11 KSO10 KSO15 — EMI
SRC1KP50VM-GP EC6901 — KSI1 KSI7 KSI6 KSO9 — EMI
SRC1KP50VM-GP EC6902 — KSI4 KSI5 KSO0 KSI2 — EMI

KSI[0..7] 27,69,82
KSO[0..15] 27,69

27,69 KB_CAPS_LED — EC6907 — SC100P50V2JN-1-GP — DY

Put Caps near DIMMA1

1D5V_S3 — EC1425 — SC68P50V2JN-1GP — RF-DY
EC1424 — SC68P50V2JN-1GP — RF-DY

Put Caps near DIMMA2

1D5V_S3 — EC1525 — SC68P50V2JN-1GP — RF-DY
EC1526 — SC68P50V2JN-1GP — RF-DY

3D3V_LAN_S5 — EC3403 — SCD1U10V2KX-5GP — RF-DY
EC3405 — SC82P50V2JN-3GP — RF-DY
EC3402 — SC56P50V2JN-2GP — RF-DY

34 LANXIN — EC3404 — SC56P50V2JN-2GP — RF-DY

DCBATOUT — EC4003 — SC68P50V2JN-1GP — RF-DY
EC4002 — SC82P50V2JN-3GP — RF-DY
EC4004 — SC2200P50V2KX-2GP — RF-DY
EC4005 — SCD1U50V3KX-GP — RF-DY

DCBATOUT_3V — EC4101 — SC68P50V2JN-1GP — RF-DY
EC4102 — SC82P50V2JN-3GP — RF-DY
EC4103 — SC2200P50V2KX-2GP — RF-DY
EC4104 — SCD1U25V2KX-GP — EMI

DCBATOUT_5V — EC4107 — SCD1U25V2KX-GP — EMI
EC4108 — SC82P50V2JN-3GP — RF-DY
EC4109 — SC2200P50V2KX-2GP — RF-DY
EC4110 — SCD1U50V3KX-GP — RF-DY

PWR_VCCCORE1_DCBATOUT — EC4304 — SC68P50V2JN-1GP — RF-DY
EC4305 — SCD1U25V2KX-GP — EMI
EC4306 — SC2200P50V2KX-2GP — RF-DY
EC4307 — SCD1U50V3KX-GP — RF-DY

PWR_VCCCORE2_DCBATOUT — EC4312 — SC68P50V2JN-1GP — RF-DY
EC4308 — SCD1U25V2KX-GP — EMI
EC4309 — SC2200P50V2KX-2GP — RF-DY
EC4310 — SCD1U50V3KX-GP — RF-DY

PWR_GFXCORE1_DCBATOUT — EC4403 — SC68P50V2JN-1GP — RF-DY
EC4404 — SCD1U25V2KX-GP — EMI
EC4405 — SC2200P50V2KX-2GP — RF-DY
EC4406 — SCD1U50V3KX-GP — RF-DY

DCBATOUT_RT8209B_VCCP — EC4503 — SC68P50V2JN-1GP — RF
EC4504 — SC82P50V2JN-3GP — RF
EC4505 — SC2200P50V2KX-2GP — RF
EC4506 — SCD1U25V2KX-GP — RF

DCBATOUT_1D5V — EC4603 — SC68P50V2JN-1GP — RF-DY
EC4604 — SC82P50V2JN-3GP — RF-DY
EC4605 — SCD1U25V2KX-GP — EMI
EC4606 — SCD1U25V2KX-GP — EMI

+LCDVDD — EC4909 — SC68P50V2JN-1GP — RF-DY
EC4908 — SC1KP50V2KX-1GP — RF-DY

3D3V_WLAN — EC5304 — SC68P50V2JN-1GP — RF-DY
EC5305 — SC82P50V2JN-3GP — RF-DY
EC5306 — SC2200P50V2KX-2GP — RF-DY
EC5307 — SCD1U50V3KX-GP — RF-DY

1D5V_S0 — EC5309 — SC68P50V2JN-1GP — RF-DY
EC5310 — SC82P50V2JN-3GP — RF-DY
EC5311 — SC2200P50V2KX-2GP — RF-DY
EC5308 — SCD1U50V3KX-GP — RF-DY

3D3V_WWAN — EC5405 — SC68P50V2JN-1GP — RF-DY
EC5406 — SC82P50V2JN-3GP — RF-DY
EC5407 — SC2200P50V2KX-2GP — RF-DY
EC5408 — SCD1U50V3KX-GP — RF-DY

DCBATOUT — EC9203 — SC68P50V2JN-1GP — RF-DY
EC9204 — SCD1U25V2KX-GP — EMI
EC9205 — SC2200P50V2KX-2GP — RF-DY
EC9206 — SCD1U50V3KX-GP — RF-DY

40 DC_IN_R — EC4007 — SC1U25V3KX-1-GP — EMI
AD+_IN_G — EC4008 — SC1U25V3KX-1-GP — EMI

EC2904/EC2903 CLOSE U2901

21,27 CLK_PCI_KBC — EC2101 — SC12P50V2JN-3GP — RF-DY
21,71 CLK_PCI_DEBUG — EC2102 — SC12P50V2JN-3GP — RF-DY

29 DMIC_CLK_R — EC2904 — SC220P50V2KX-3GP — EMI
29 DMIC_DATA_R — EC2903 — SC220P50V2KX-3GP — EMI

18,22,86,92,93,96 PE_PWRGD

EC9207 — SC4750V2JN-3GP — EMI
EC9208 — SC4750V2JN-3GP — EMI

WLAN & WWAN

H1 ~ H16 --> ZZ.00PAD.D11
H17 ~ H22 --> ZZ.00PAD.N11
H23 ~ H26 --> 34.4Y824.001
H27 ~ H28 --> 34.4Q602.101

WWAN WWAN PCH

H23 H24 H25 H26 H27 H28
STF256R168H05-GP — 34.4KD36.00134.4KD36.001 — 34.4KD36.001 — 34.4KD36.001
STF256R168H03-GP

H19 H20 — HOLE276R178-GP — ZZ.00PAD.N11 ZZ.00PAD.N11
H11 H12 — HOLE256R115-GP — ZZ.00PAD.D11 ZZ.00PAD.D11
H30 H31 — HOLE276R178-GP — ZZ.00PAD.N11 ZZ.00PAD.D11
H1 H2 H3 H4 — HOLE256R115-GP — ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11
H29 H17 H15 H16 — HOLE276R178-GP — ZZ.00PAD.D11 ZZ.00PAD.N11 ZZ.00PAD.N11 ZZ.00PAD.N11
H5 H8 — HOLE256R115-GP — ZZ.00PAD.D11 ZZ.00PAD.D11

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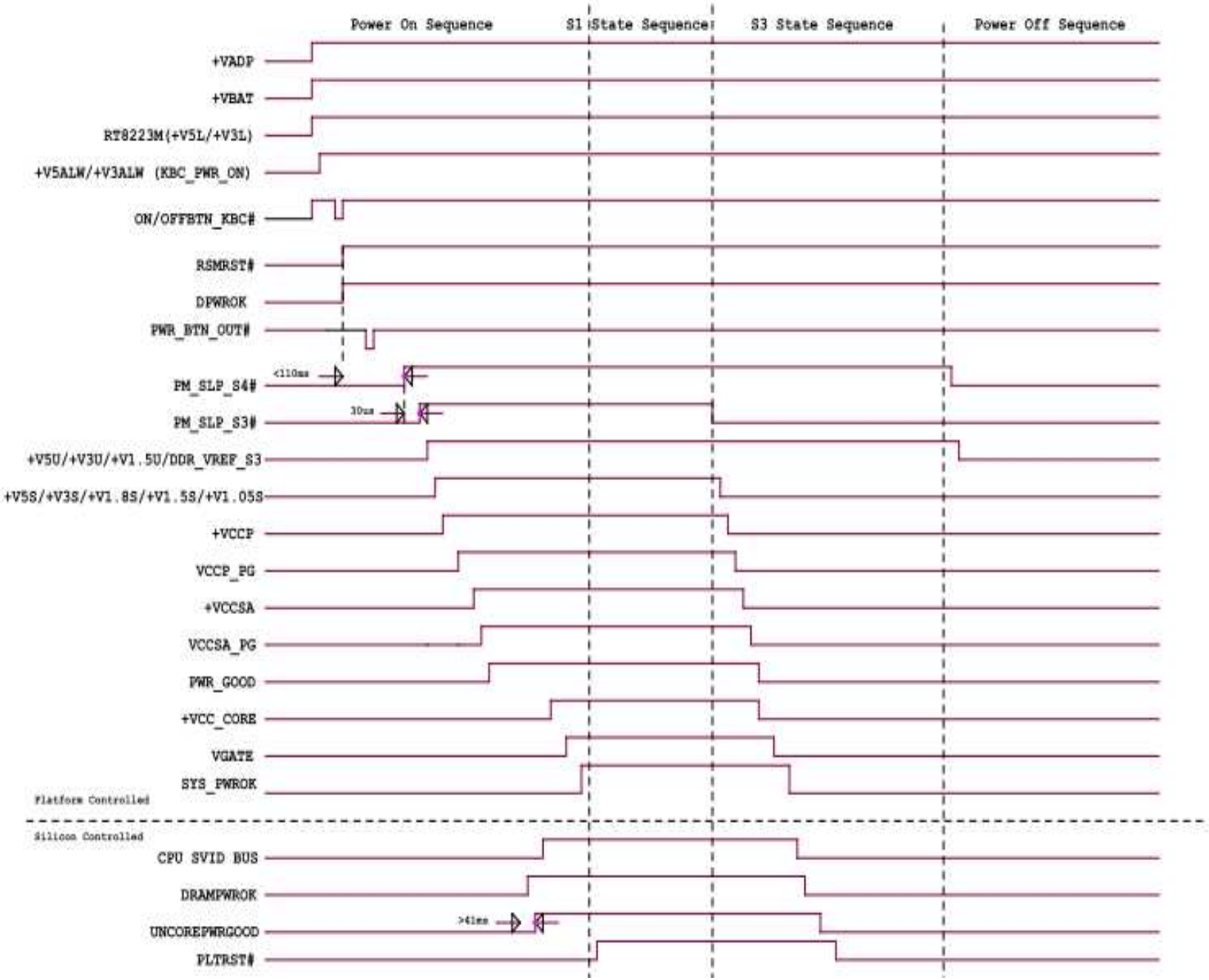
S-Series Power Sequence and Reset Signal Timing



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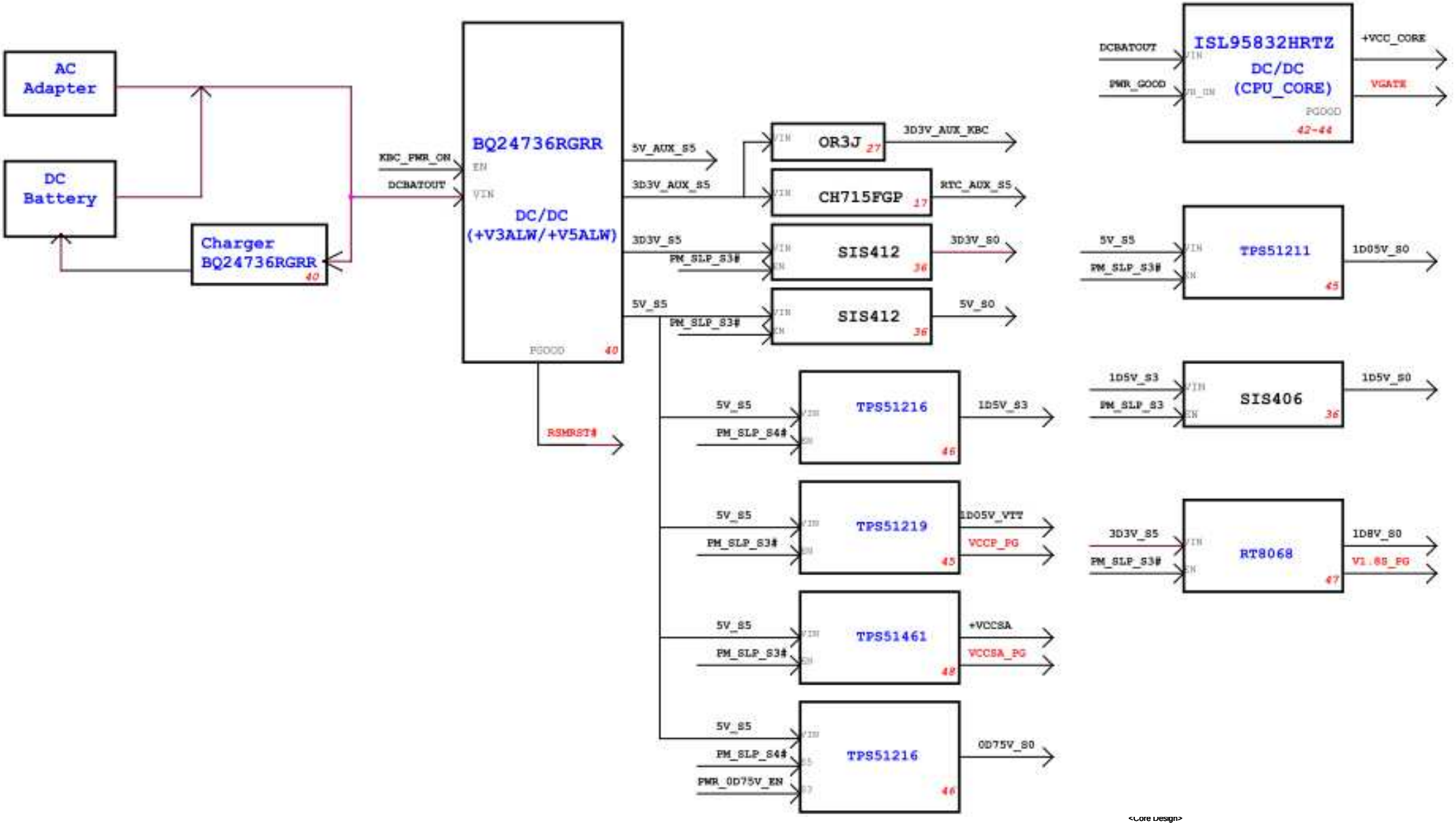
S-Series POWER BLOCK DIAGRAM



<Core Design>

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Title: *Power Block Diagram*		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
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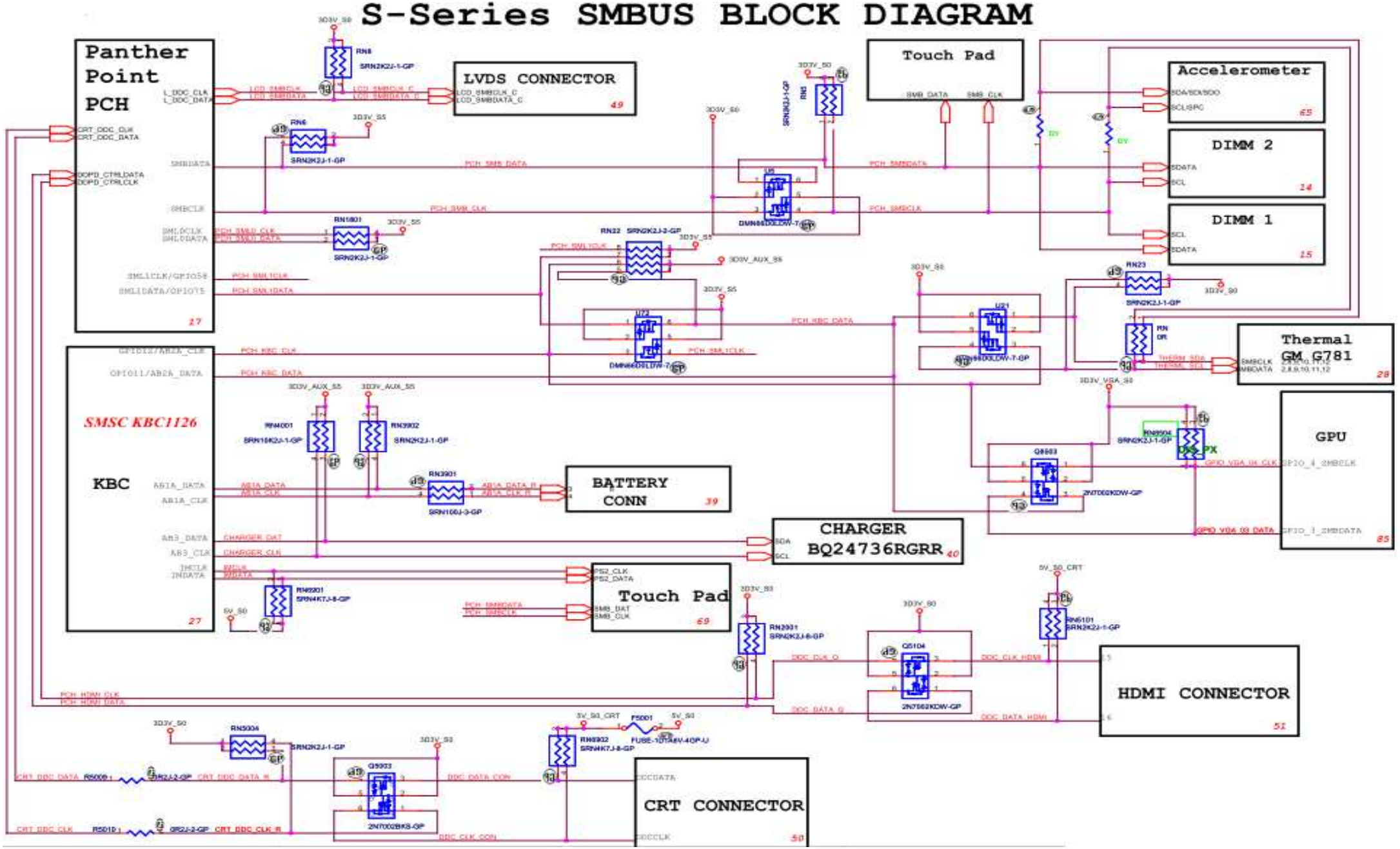
S-Series SMBUS BLOCK DIAGRAM



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Title	***SMBUS Block Diagram***	
Size: A3	Document Number: **2012 S-Series Richie 13.3**	Rev: -1
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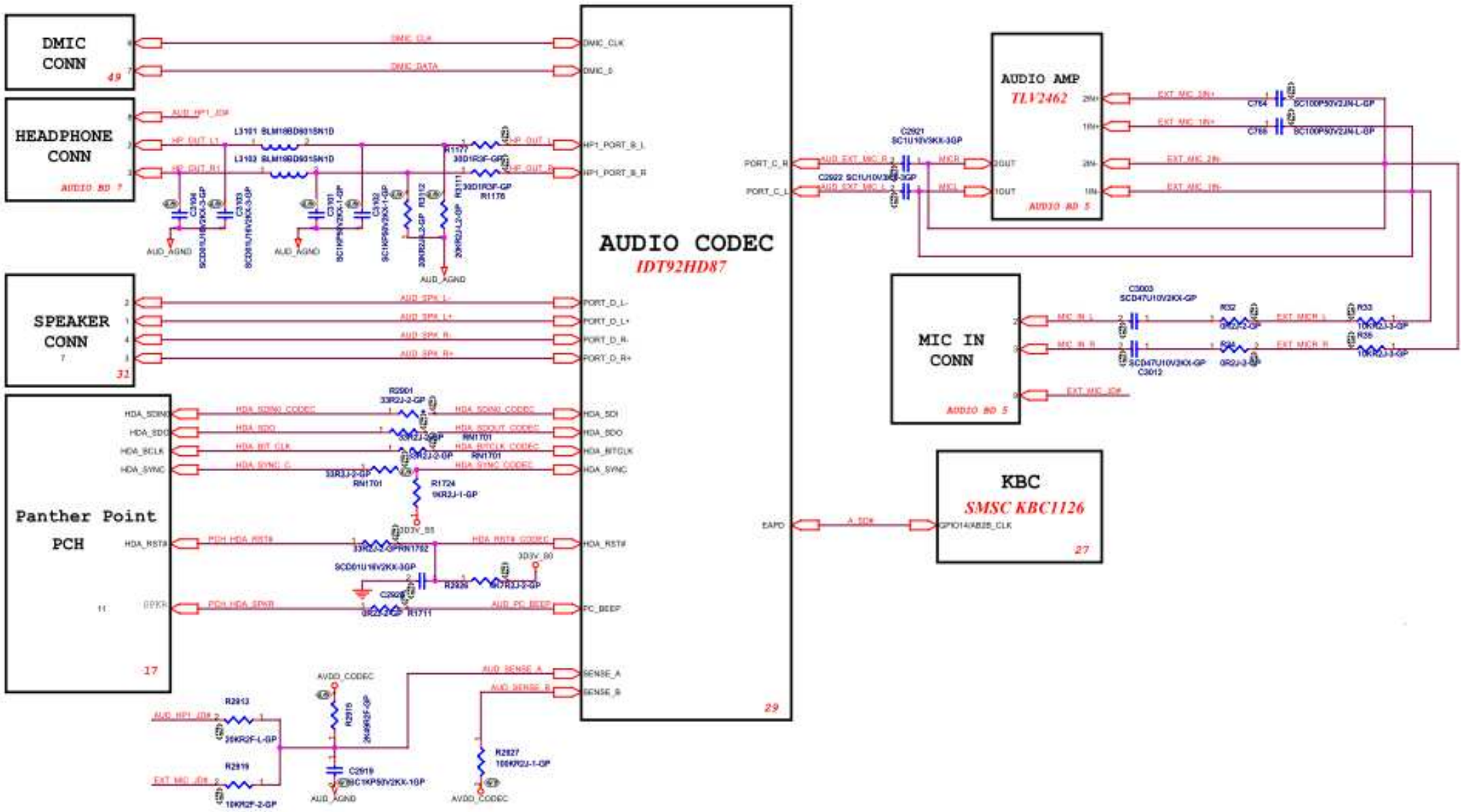
S-Series AUDIO BLOCK DIAGRAM



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Title	***Thermal/Audio Block Diagram***	
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Title: ***mSATA***

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