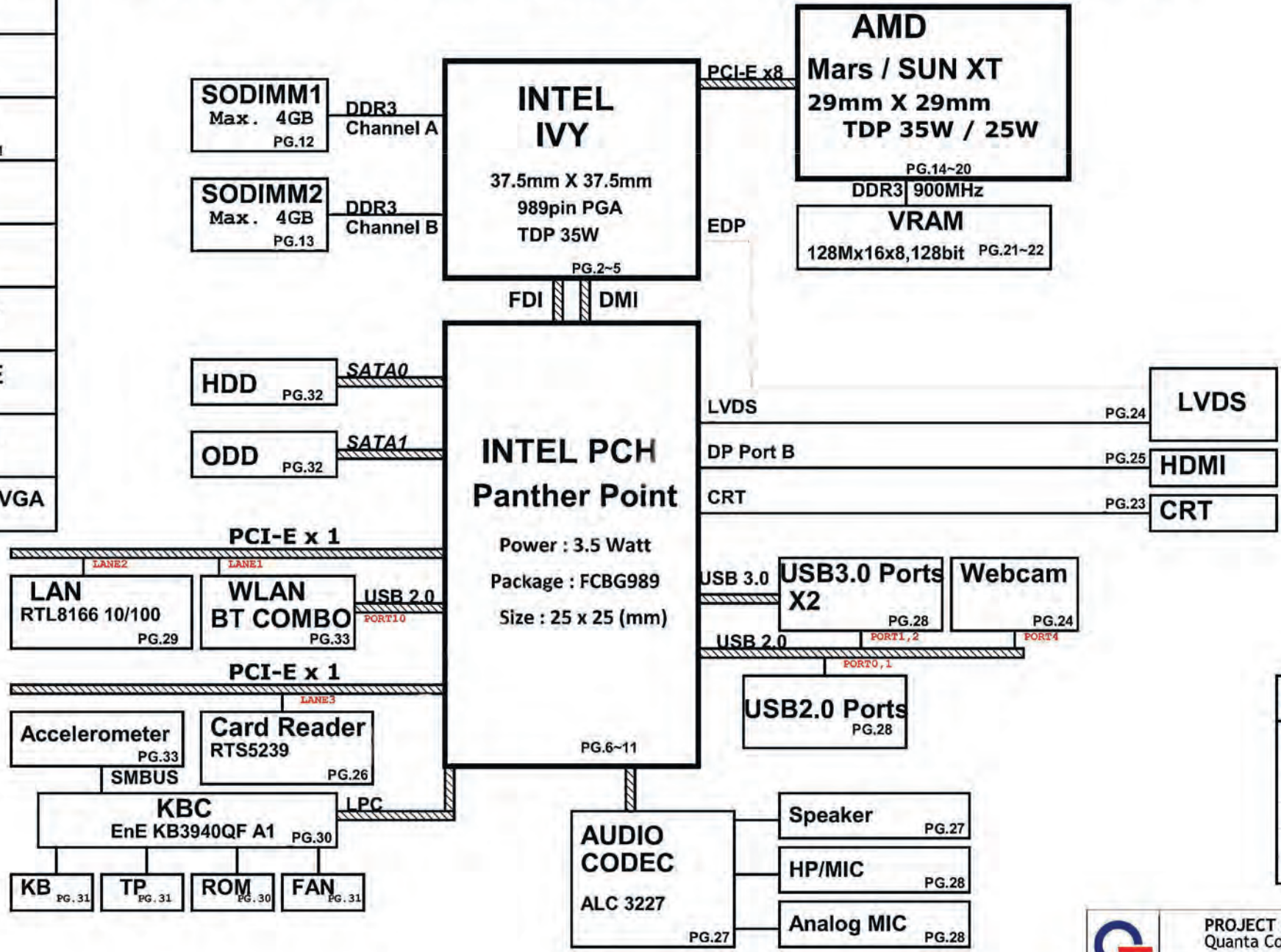
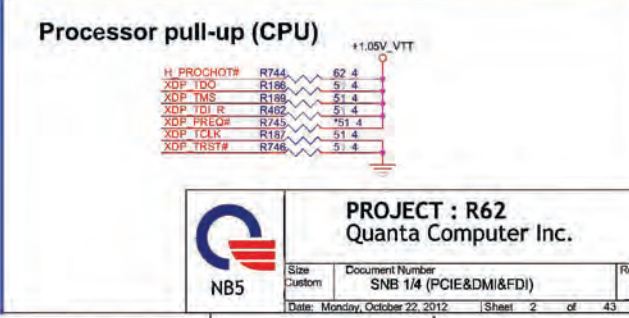
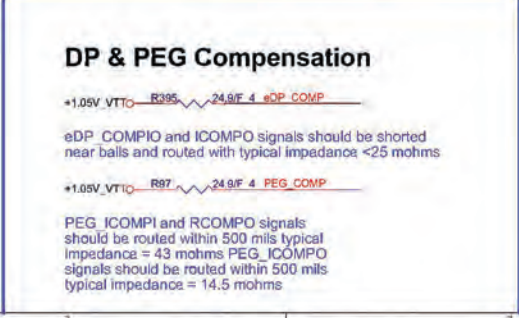
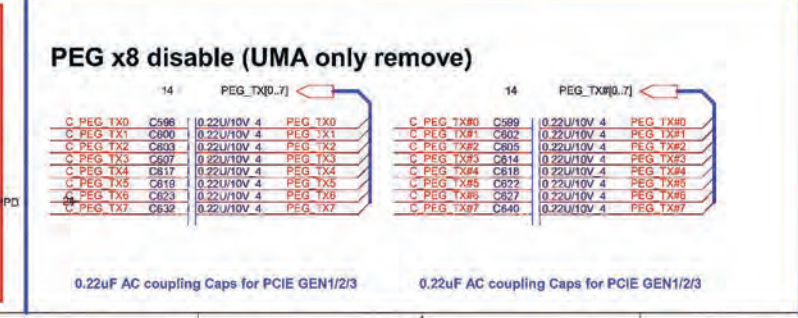
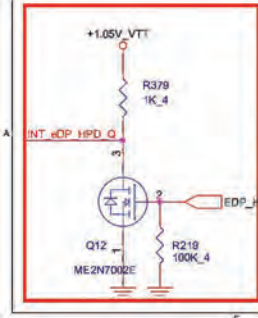
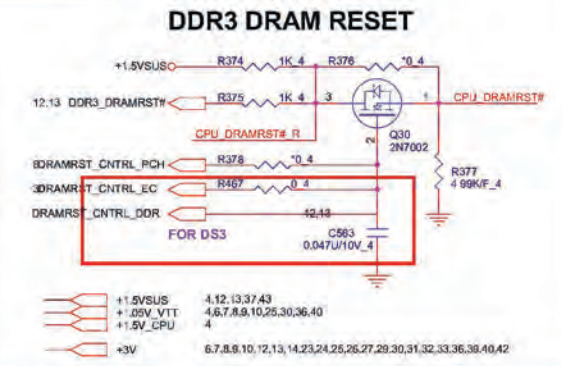
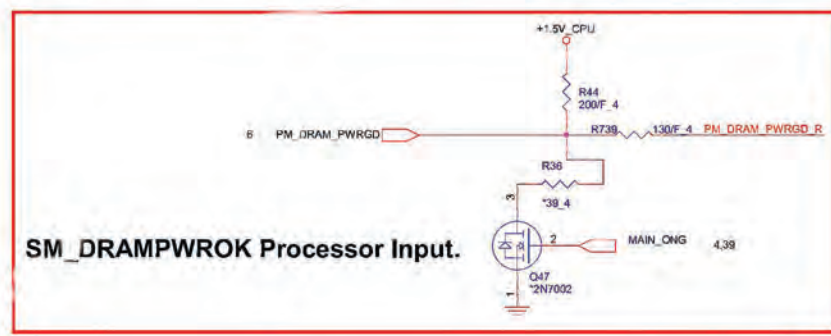
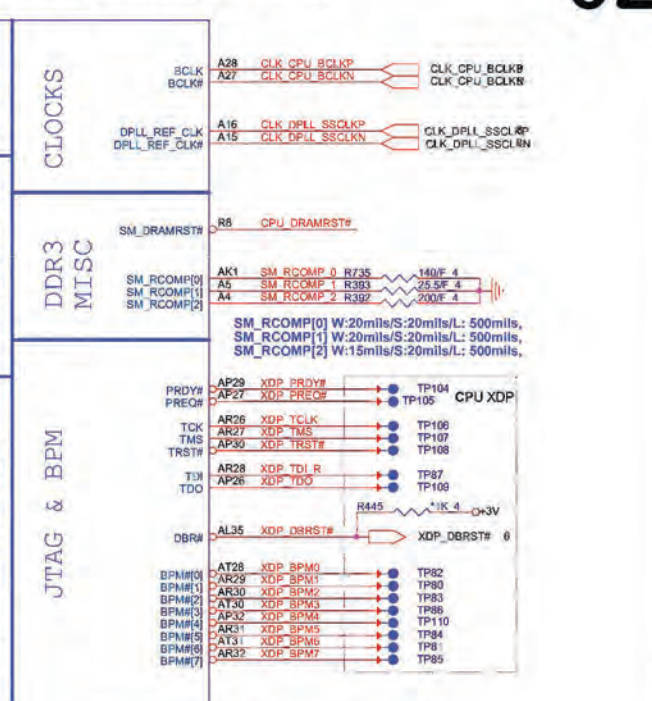
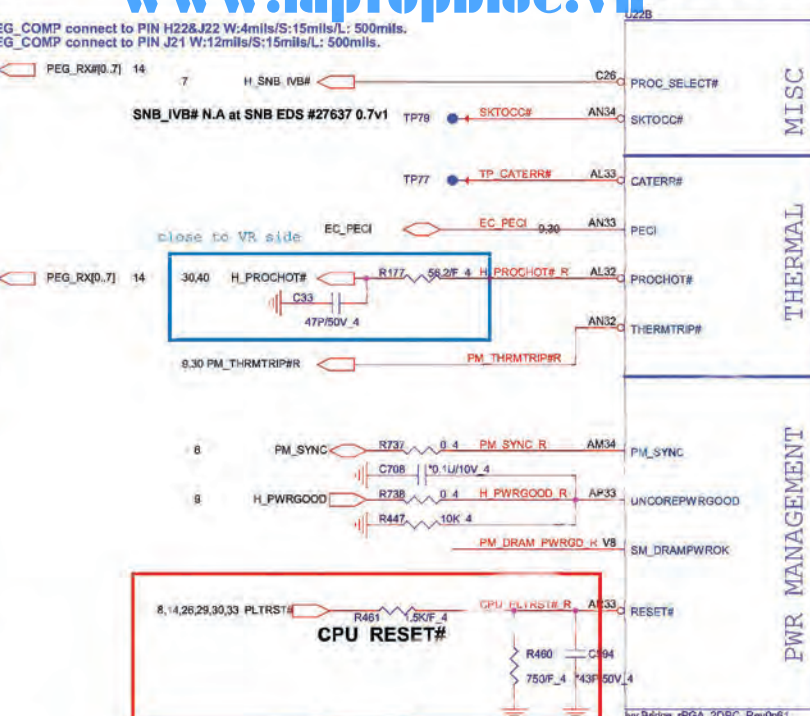
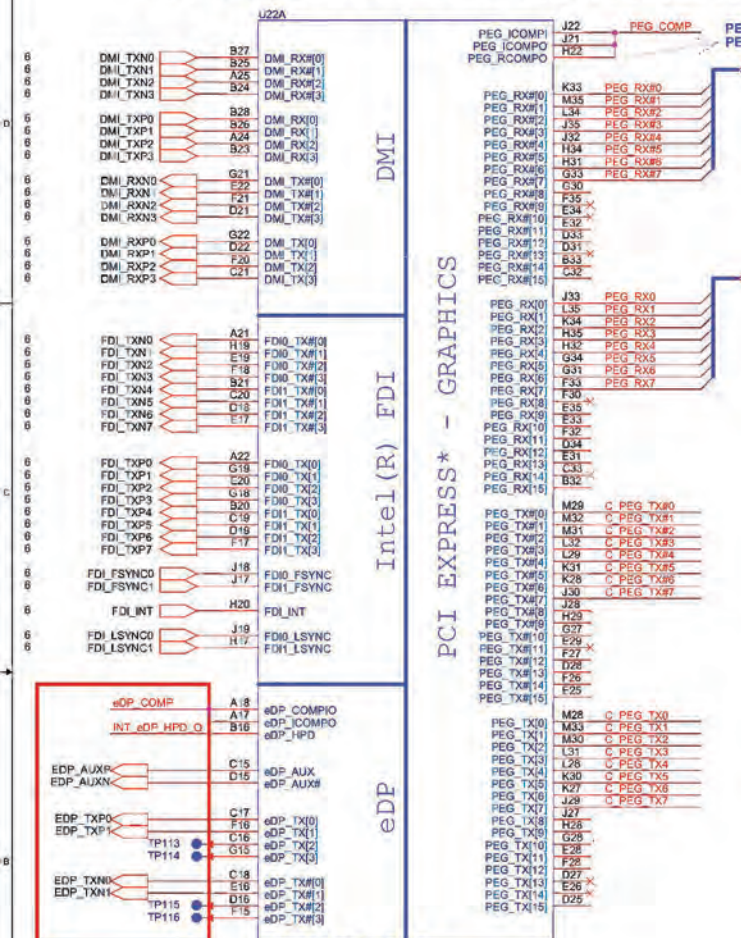


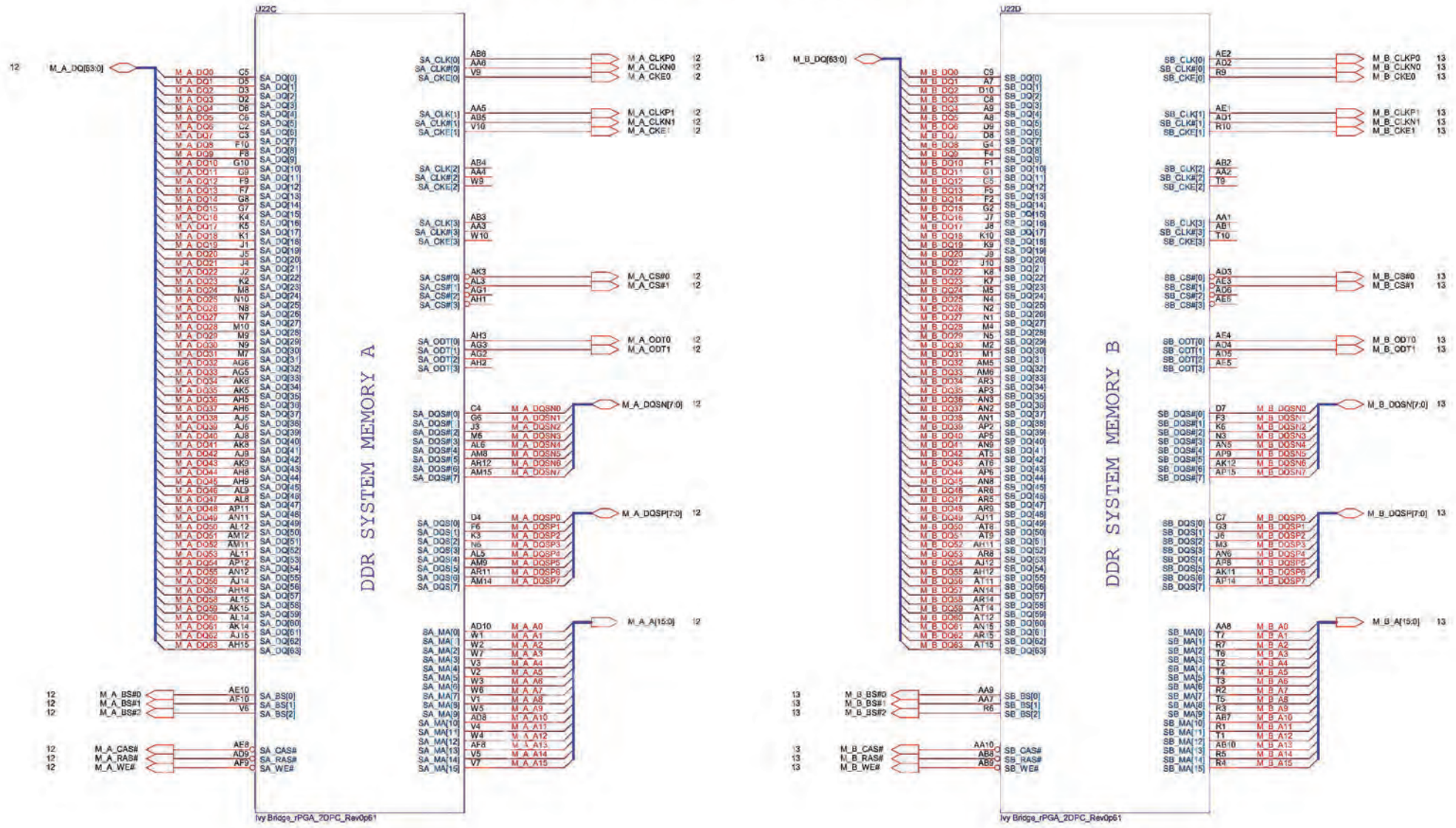
R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

+3V/+5V S5
PG.35
+1.05V
PG.36
CPU Core
PG.40~41
DDR3
PG.37
Charge
PG.34
Dis-Charge
PG.39
+VGACORE
PG.42
+VCCSA
PG.38
+1.0V/+1.8/ +3 VGA
PG.43



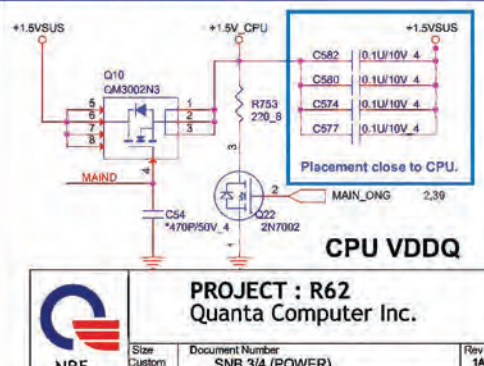
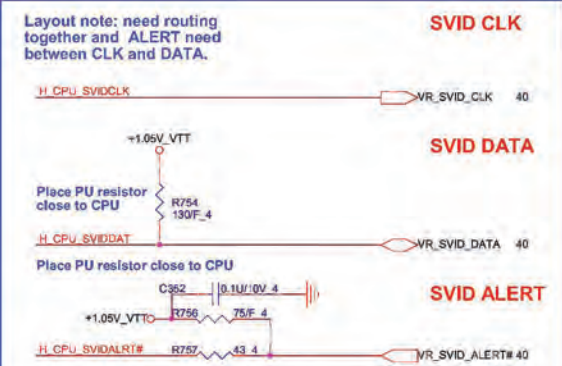
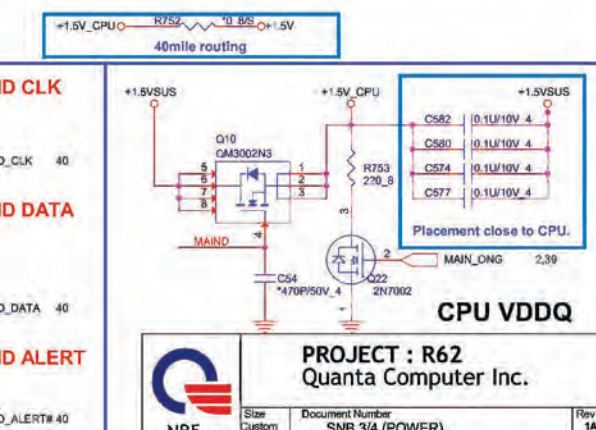
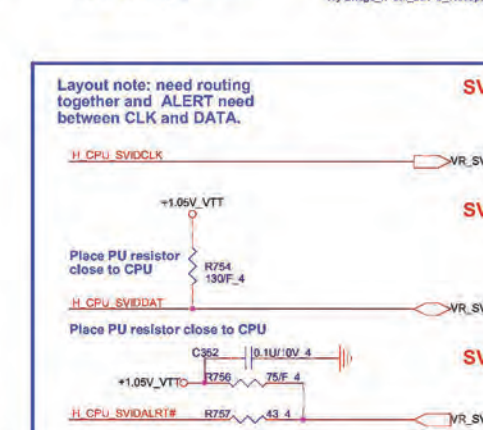
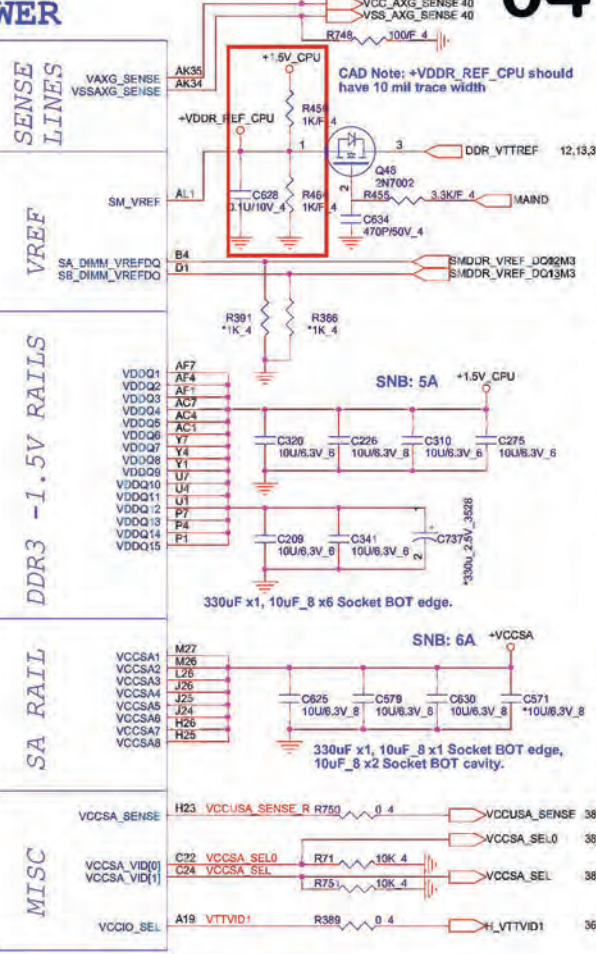
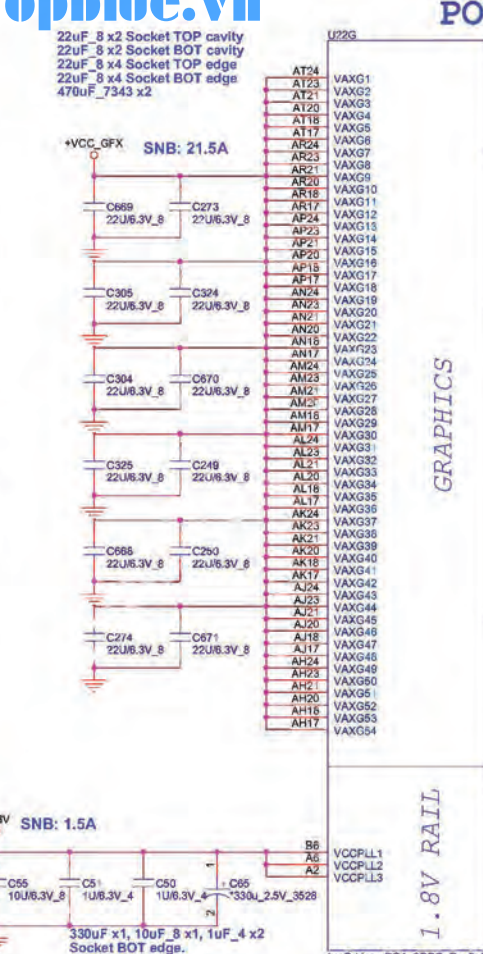
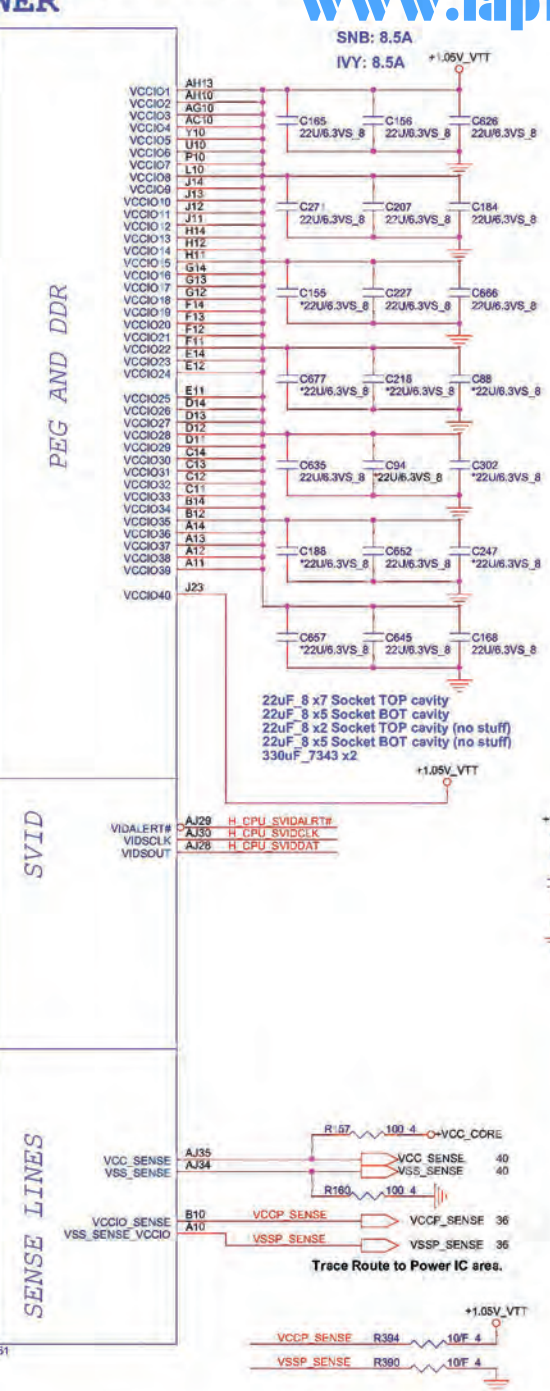
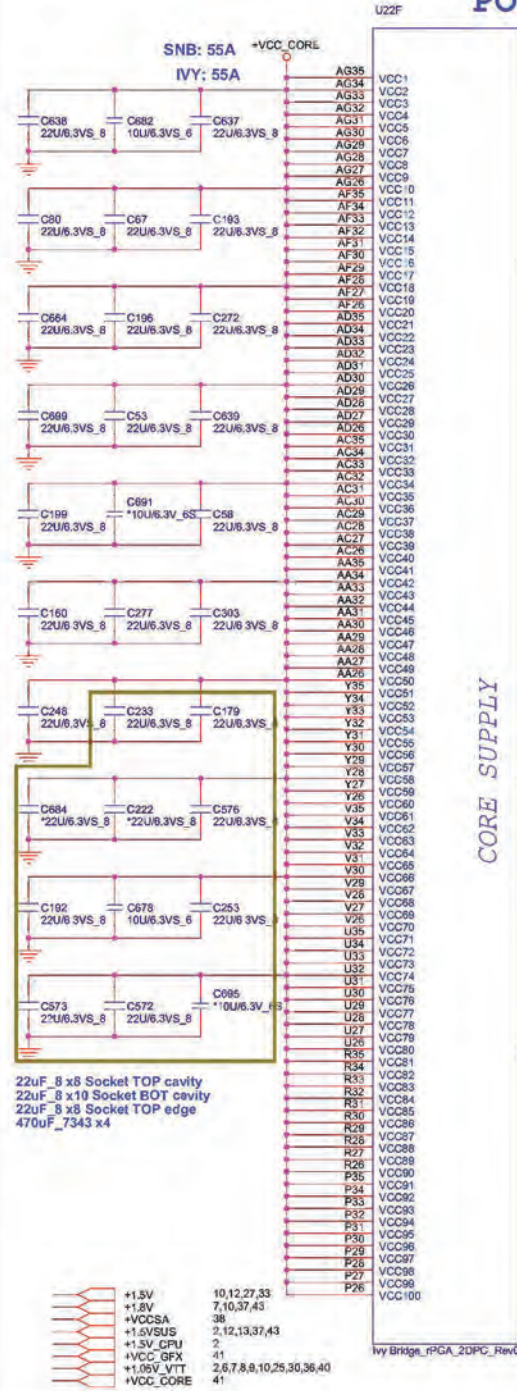
Stackup
TOP
GND
IN1
IN2
VCC
BOT

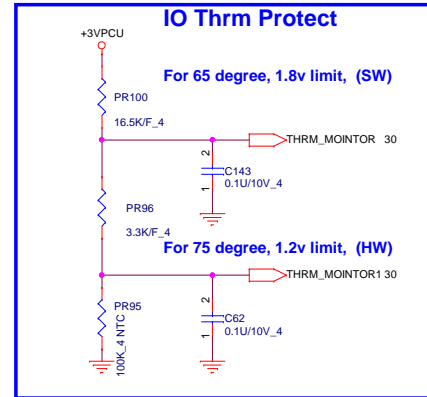
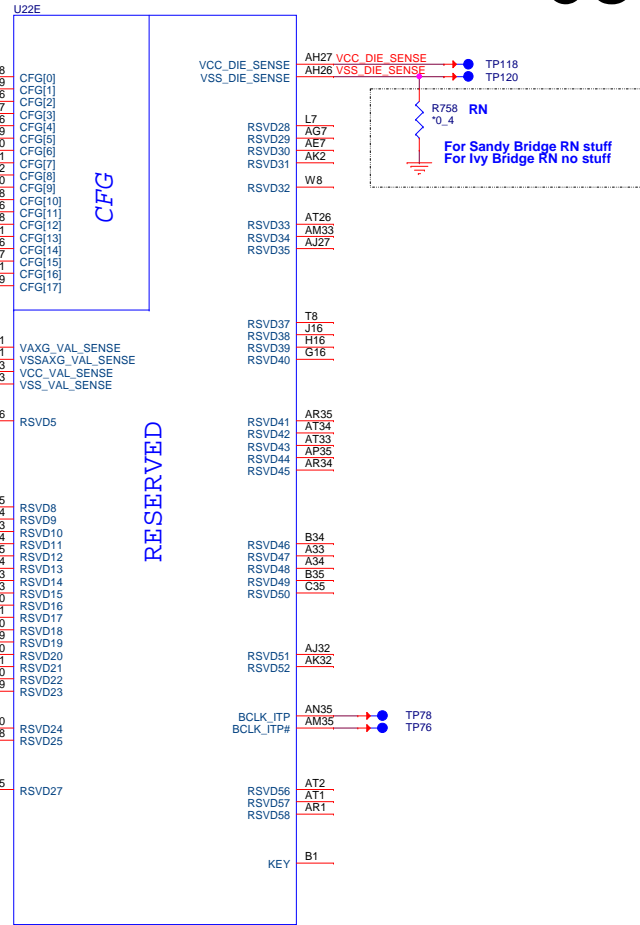
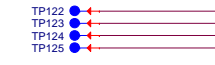
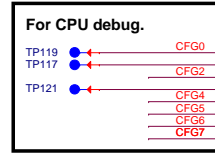
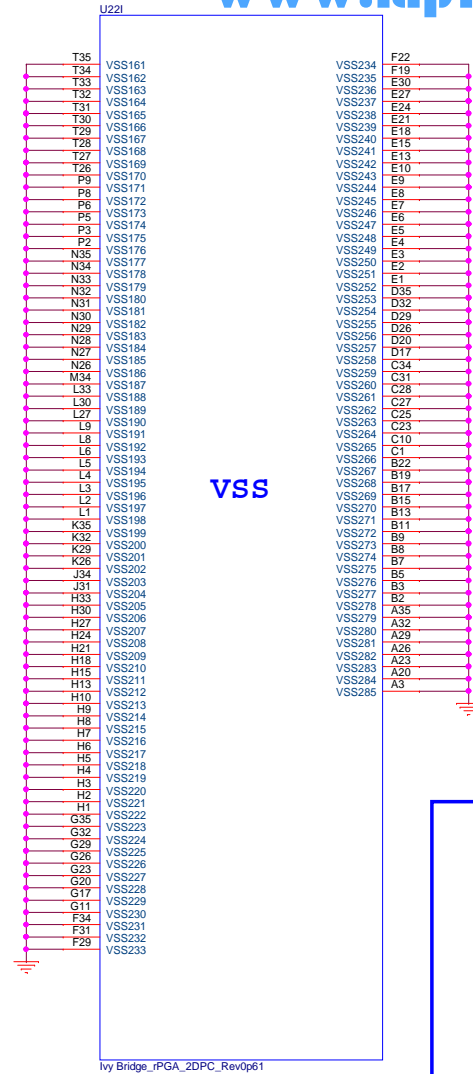
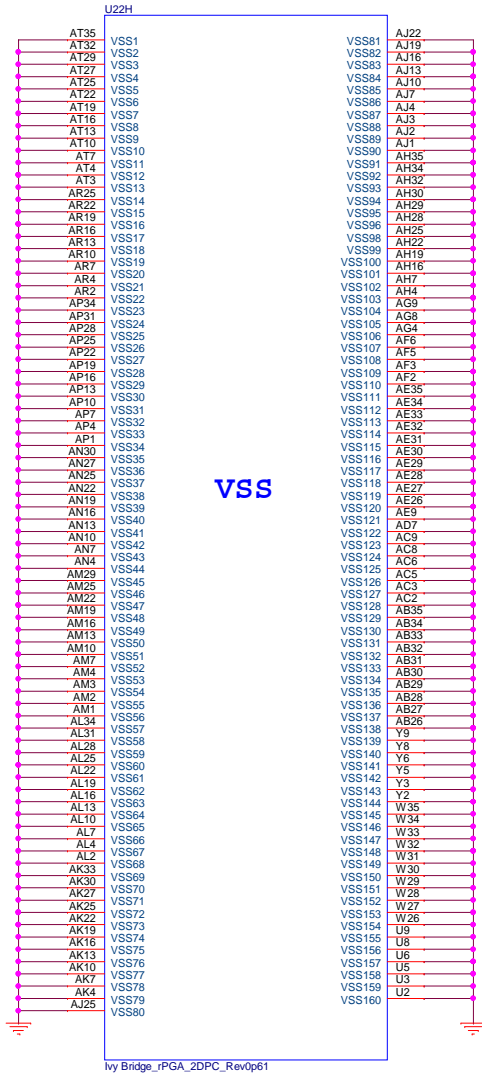




POWER

POWER

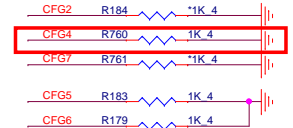




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversa)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

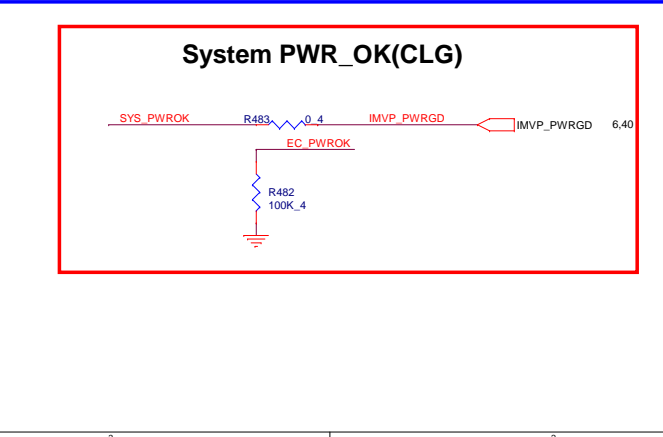
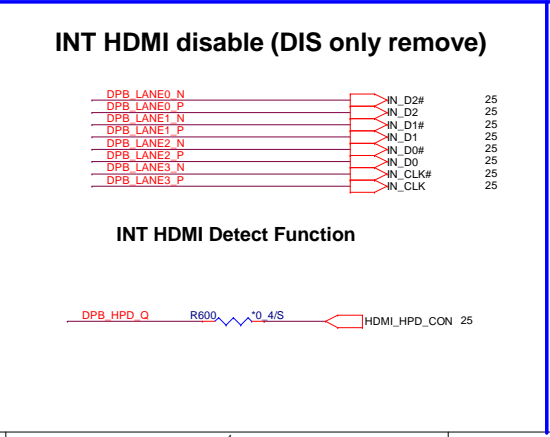
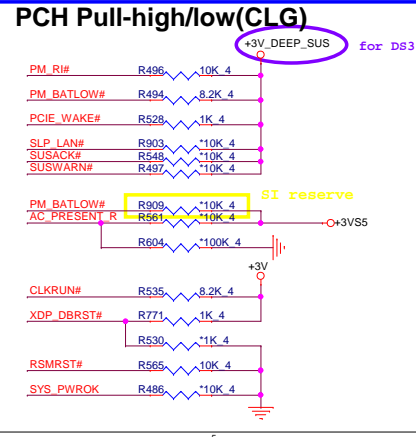
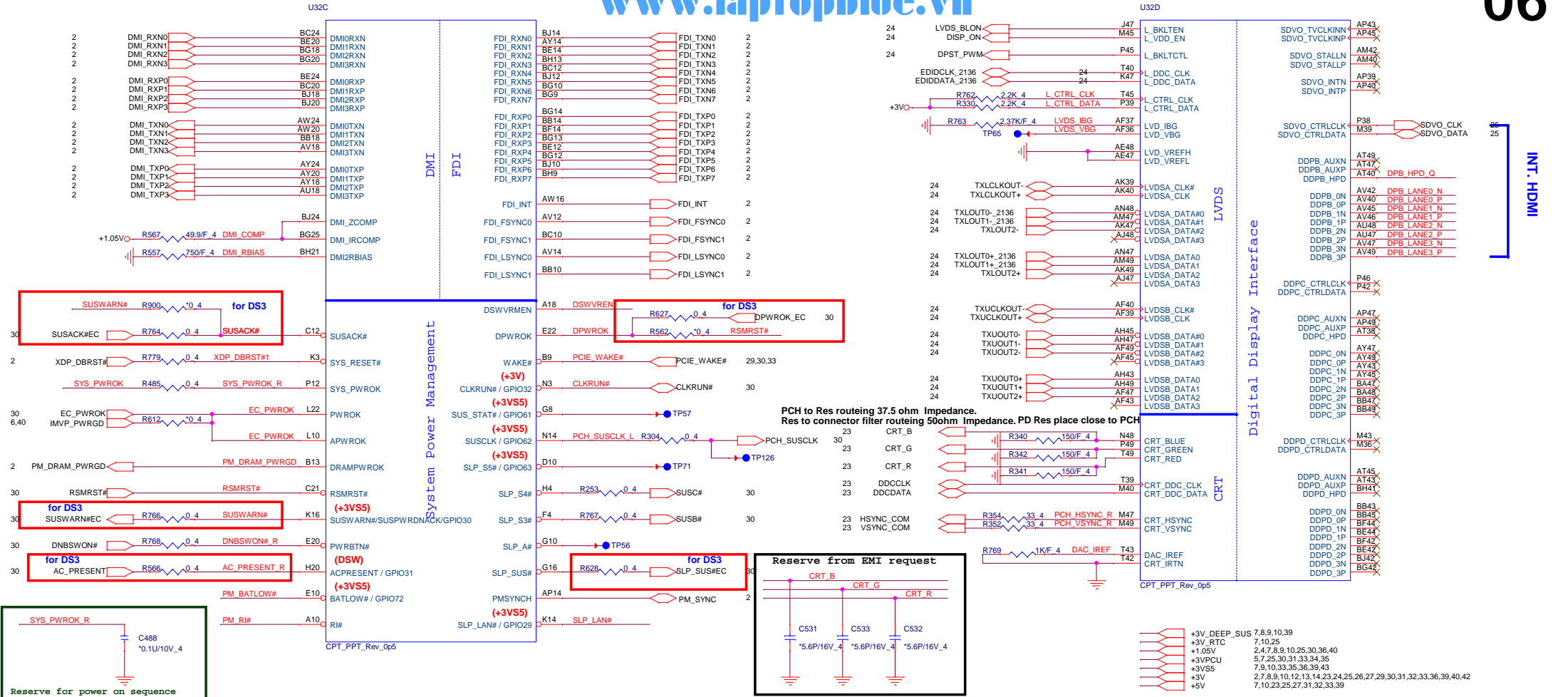


CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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NBS

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On Die DSW VR Enable

High = Enable (Default)
Low = Disable

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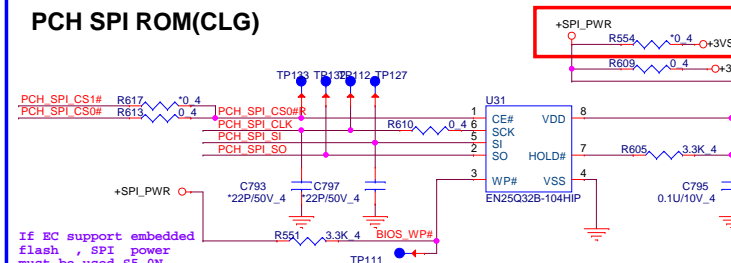
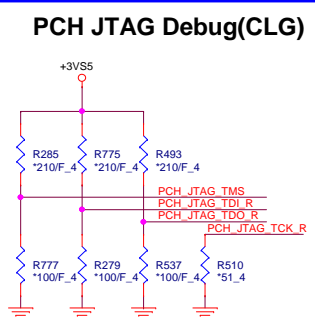
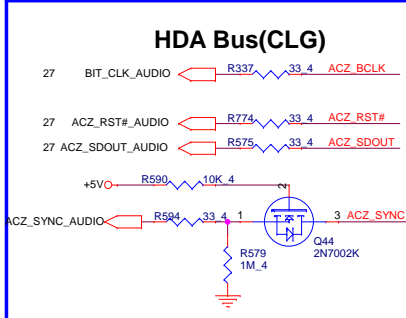
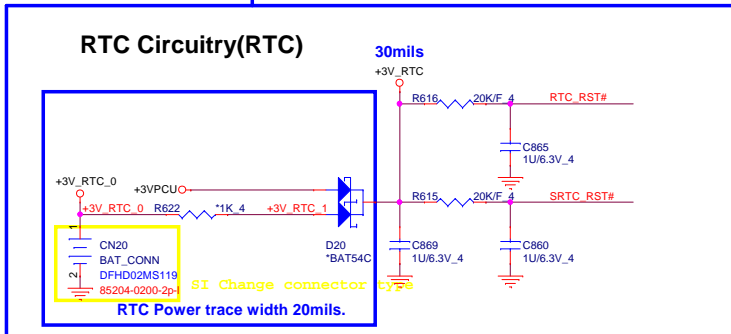
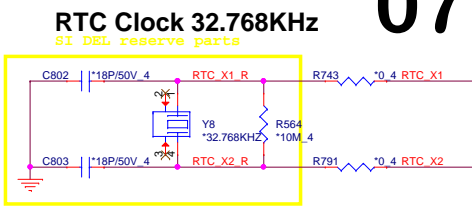
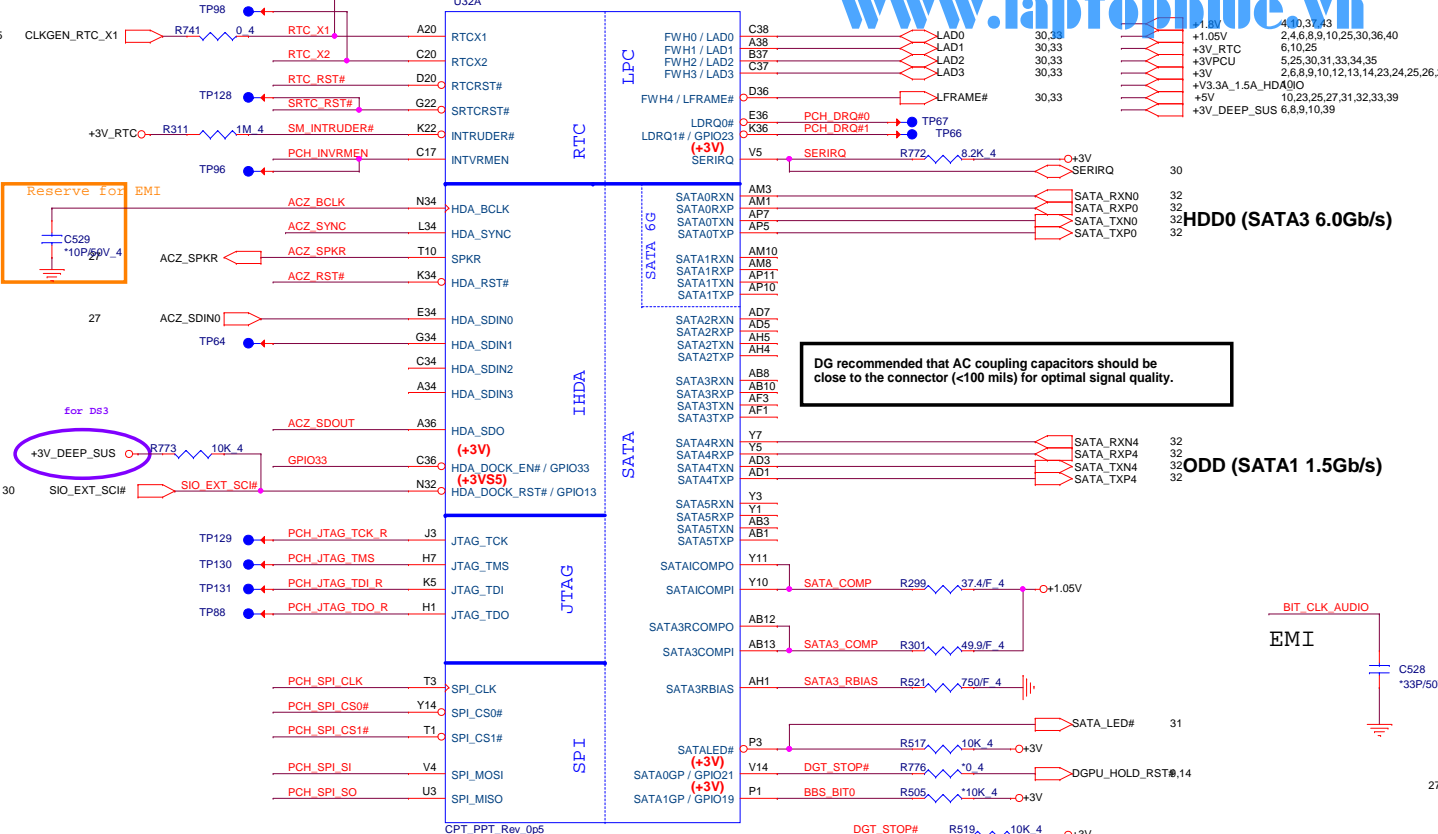
Size Custom Document Number PCH 1/6 (DMI/FDI/VIDEO) Rev 1A

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Cougar Point/Panther Point (HDA,JTAG,SATA)

www.laptopblue.vn

07



Vender	Size	P/N
EON	4MB	AKE392N0Q02 (EN25Q32B-104HIP)
PMC	4MB	AKE392N0500 (PM25LQ032C-BCE)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V0 R595 10K 4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R572 0.4 2 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWR0K		R782 1K 4 BBS_BIT0 R595 1K 4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWR0K	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWR0K	0 = Disable (Internal pull-down 20kohm)	+1.8V R783 1K 4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWR0K	weak pull-down 20kohm	+1.8V R526 2.2K 4 R546 1K 4 NV_CLE H_SNB_IVB# 9
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+V3.3A_1.5A_HDA_IO R784 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWR0K	0 = Default (weak pull-down 20K) 1 = Overriden	GPIO33_E ACZ_SDOUT R573 1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWR0K	0 = Default (weak pull-down 20K) 1 = Enable	

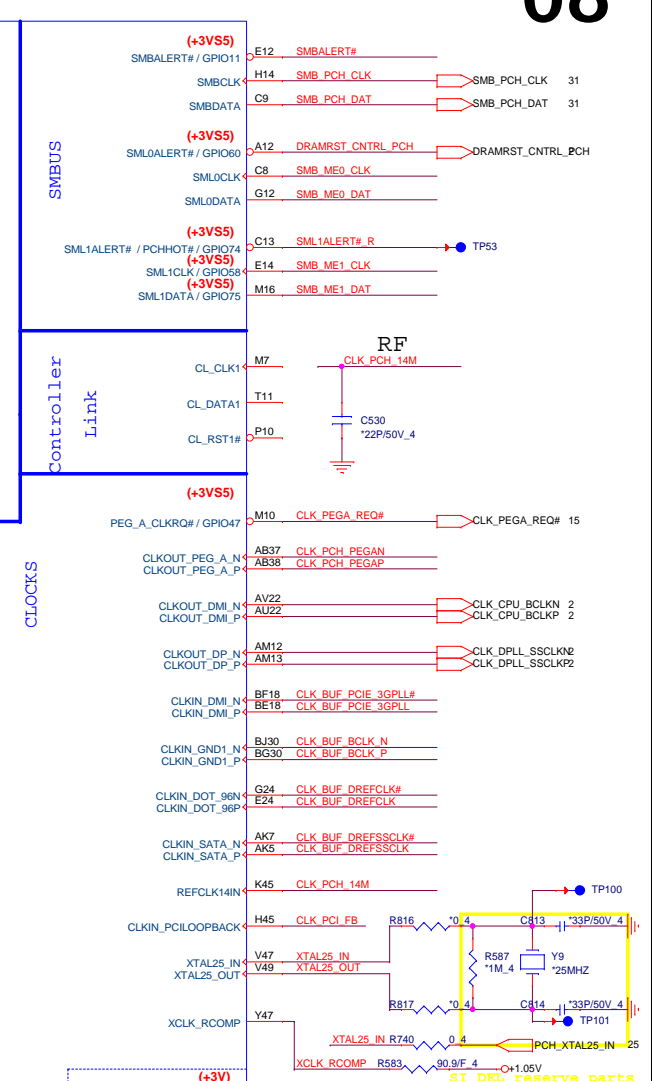
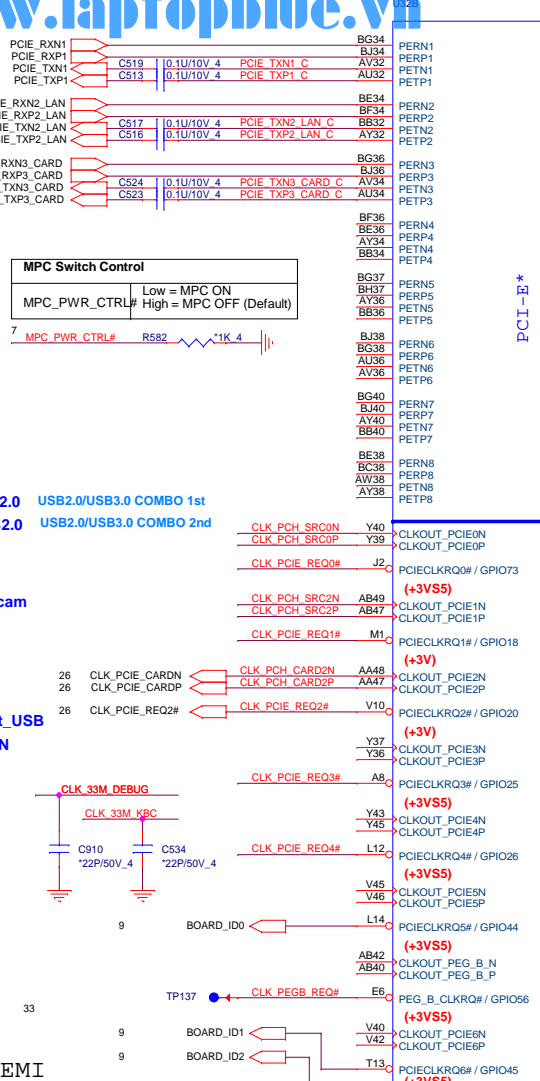
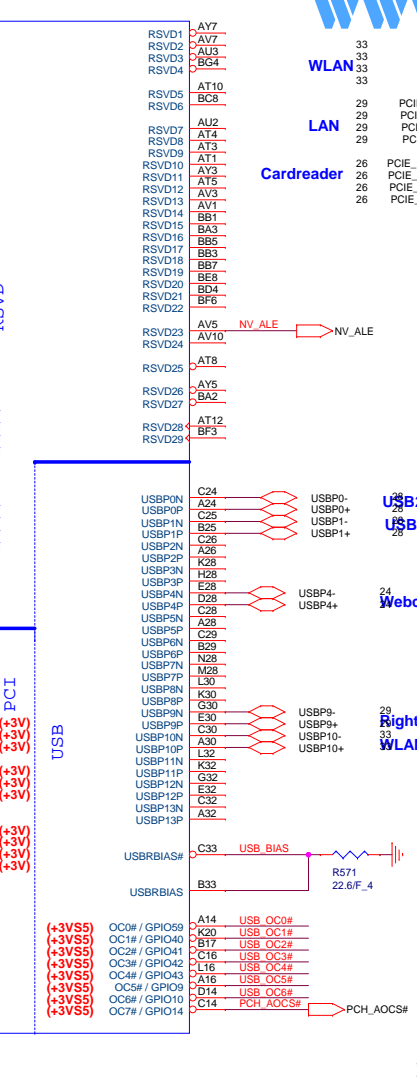
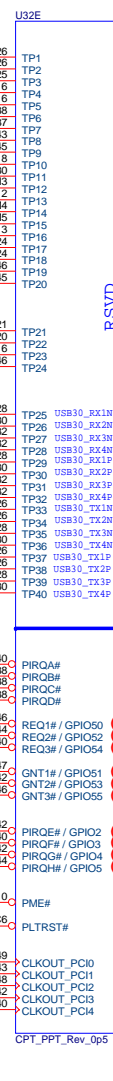
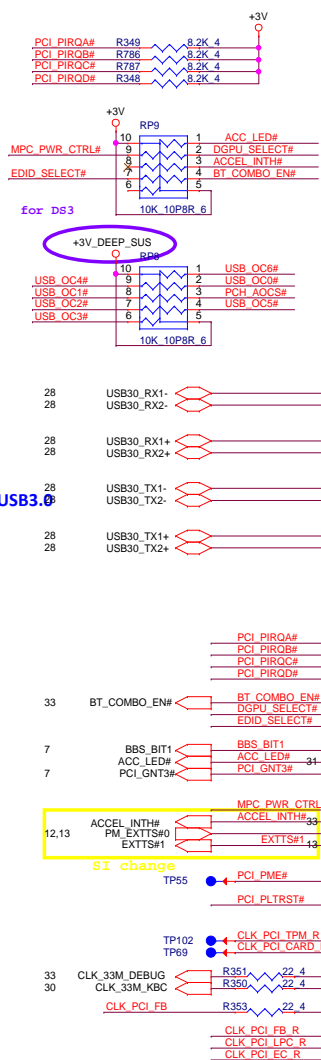
PROJECT : R62
Quanta Computer Inc.

NBS

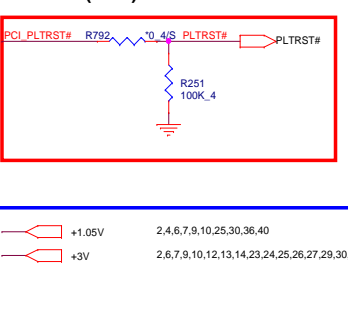
Size Custom Document Number PCH 2/6 (SATA/HDA/SPI) Rev 1A

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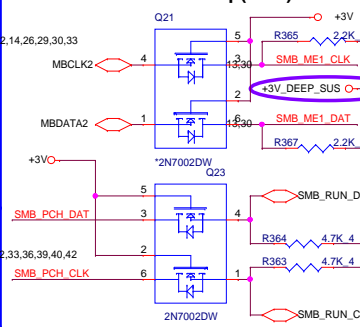
PCI/USBOC# Pull-up(CLG)



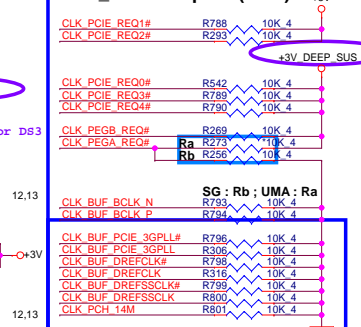
PLTRST#(CLG)



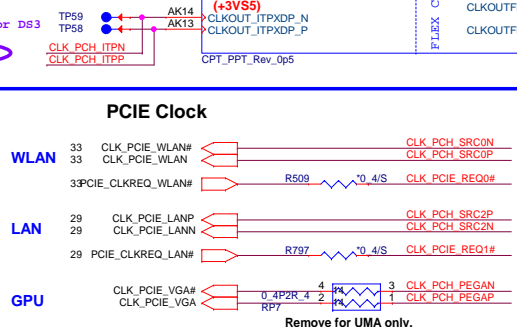
SMBus/Pull-up(CLG)



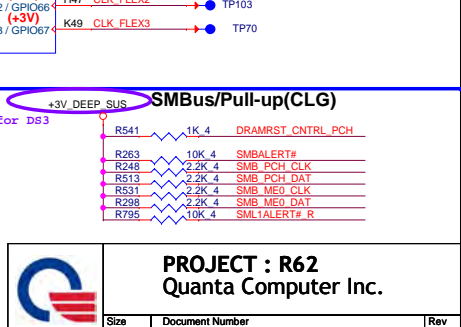
CLK_REQ/Strap Pin(CLG)



PCIE Clock

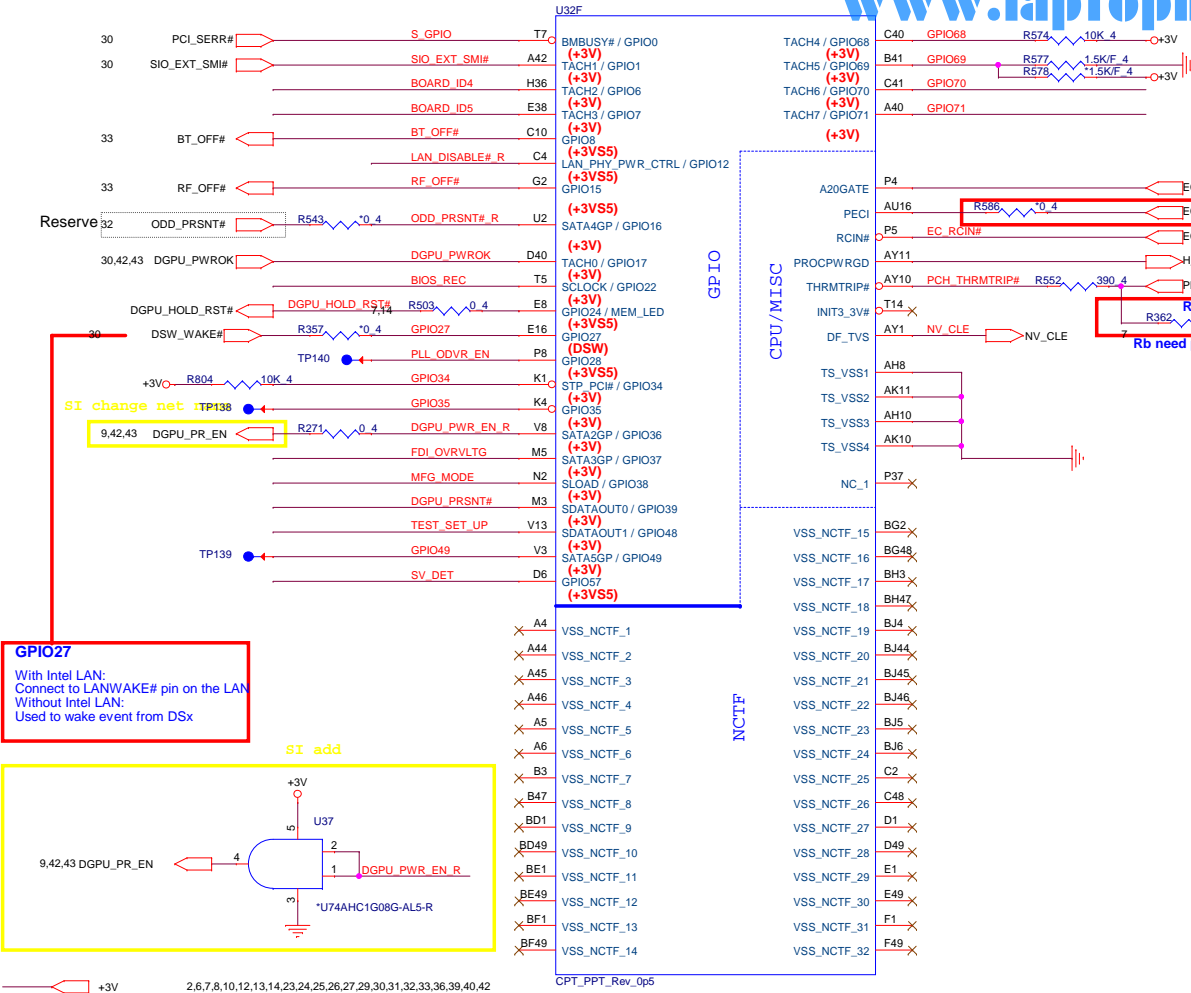


SMBus/Pull-up(CLG)

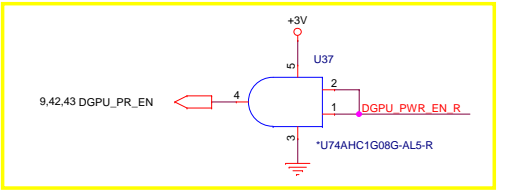


PROJECT : R62
Quanta Computer Inc.
NB5
Size Custom
Document Number PCH 3/6 (PCIe/USB/CLK)
Date: Monday, October 22, 2012
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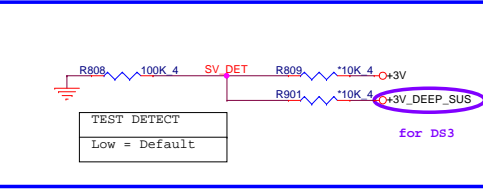
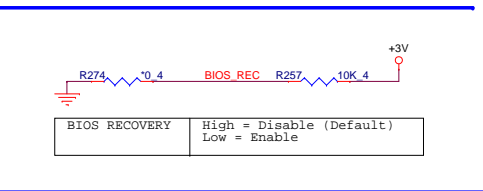
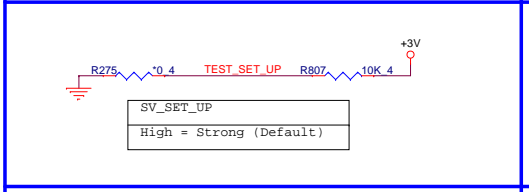
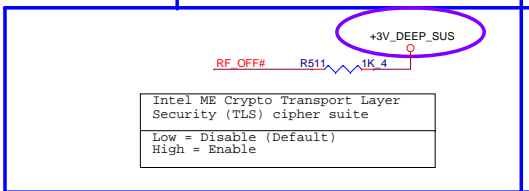
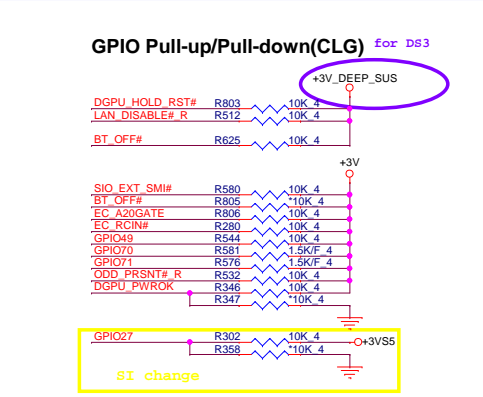
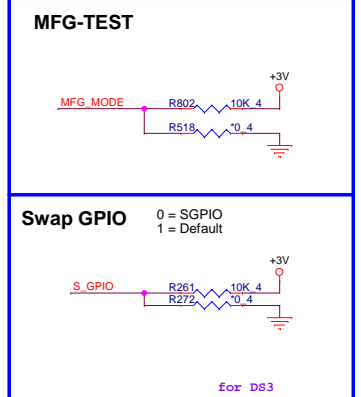
Cougar Point/Panther Point (GPIO,VSS,NCTF,RSVD)



GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

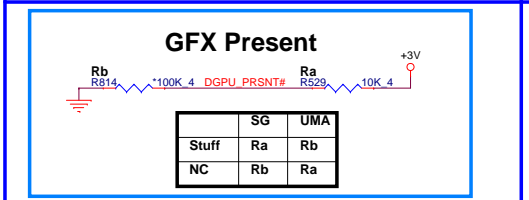
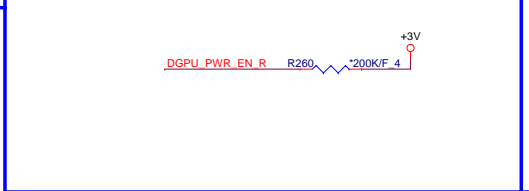
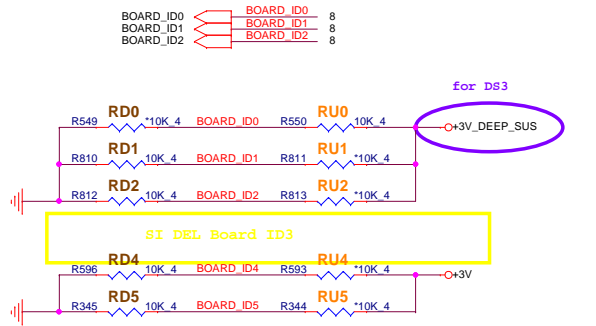


+3V 2.6,7,8,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42



BOARD ID SETTING

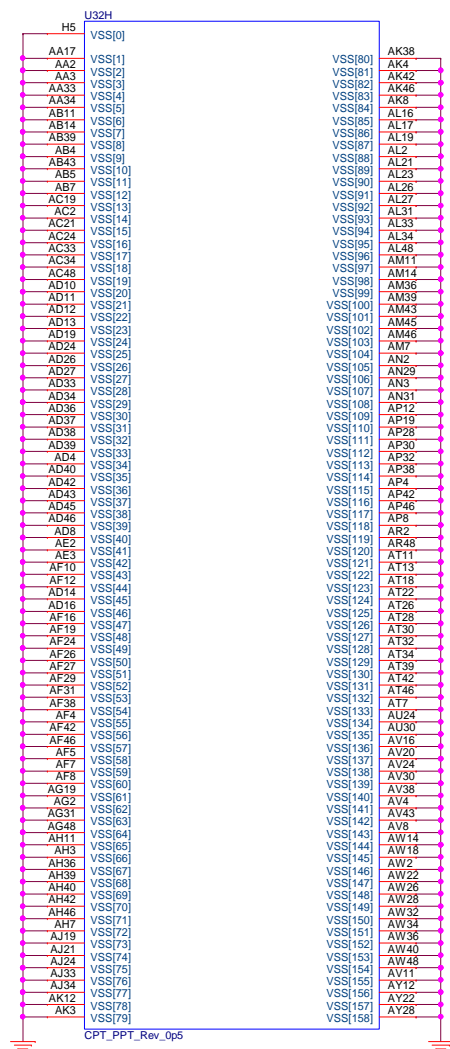
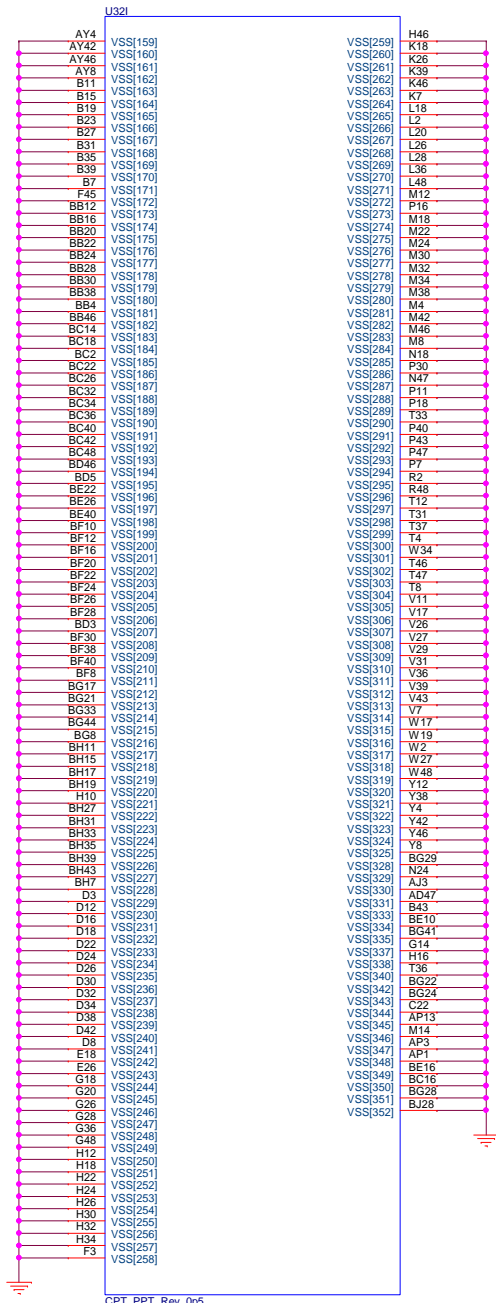
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DB R62 UMA			0	0	0	0
DB R62 DIS			0	0	1	1
			0	1	1	1
			0	0	0	0




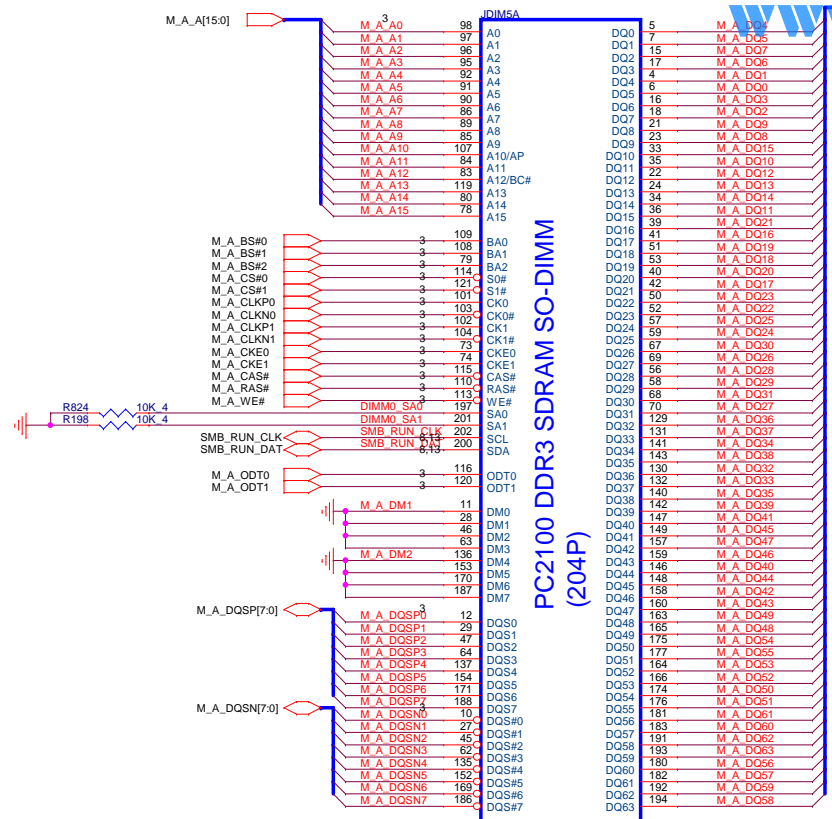
PROJECT : R62
Quanta Computer Inc.

NB5

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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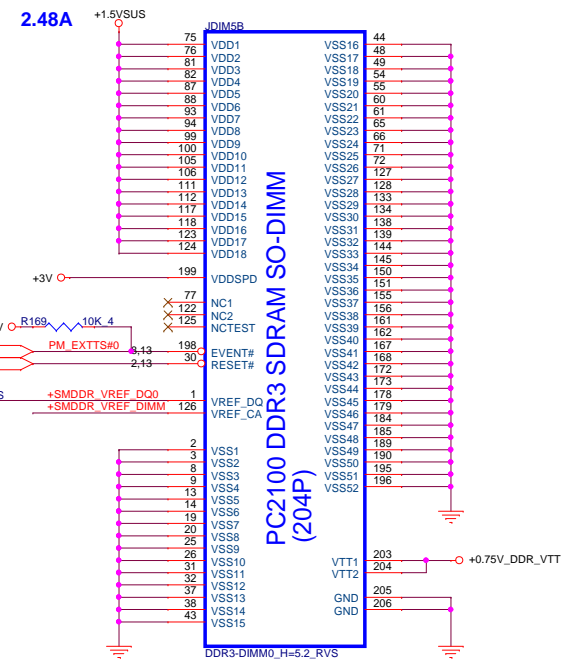
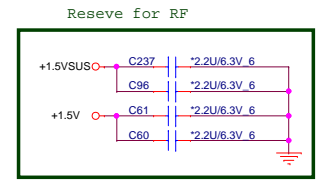


	PROJECT : R62		
	Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	Rev 1A
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PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=5.2_RVS
dtr-78279-001-rvs-204p
DGMK4000278
SOCKET DDR3 SODIMM(204P,H5.2,RV5)QBCON

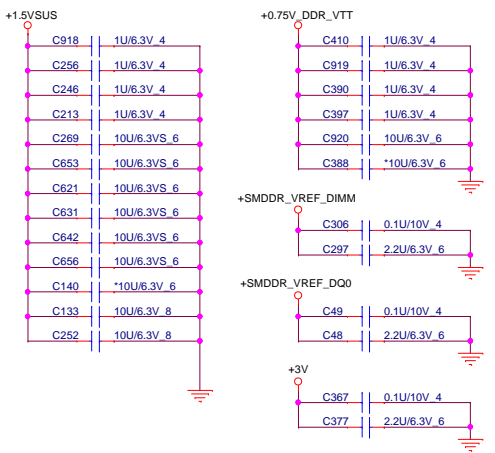


PC2100 DDR3 SDRAM SO-DIMM (204P)

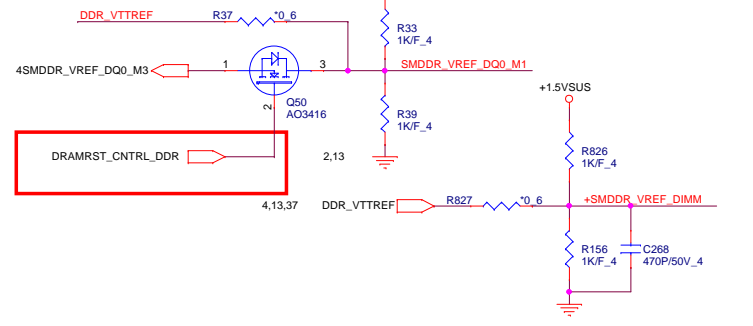
DDR3-DIMM0_H=5.2_RVS
dtr-78279-001-rvs-204p
DGMK4000278
SOCKET DDR3 SODIMM(204P,H5.2,RV5)QBCON

- +1.5V 4,10,27,33
- +0.75V_DDR_VTT 3,37,39
- +1.5VSUS 2,4,13,37,43
- +3VPCU 5,7,25,30,31,33,34,35
- +3V 2,6,7,8,9,10,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42

Place these Caps near So-Dimm0.

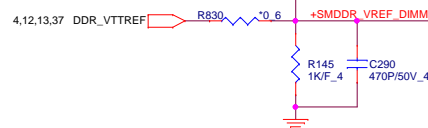
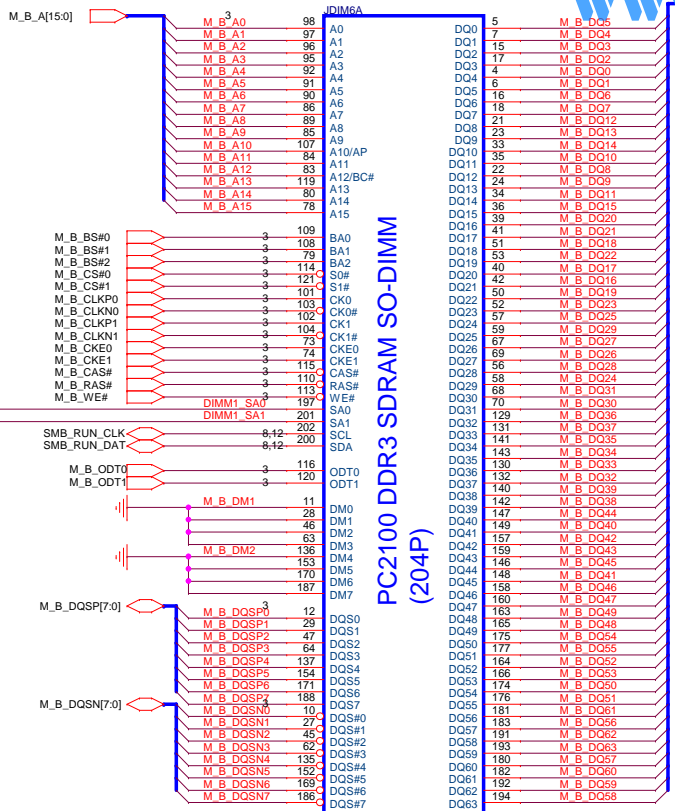


VREF DQ0 M1 Solution



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Quanta Computer Inc.

NB5	Size	Document Number	Rev
	Custom	DDR3 DIMM0-RVS (5.2H)	1A
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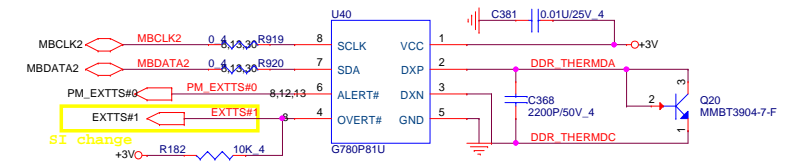


2.48A

PC2100 DDR3 SDRAM SO-DIMM (204P)

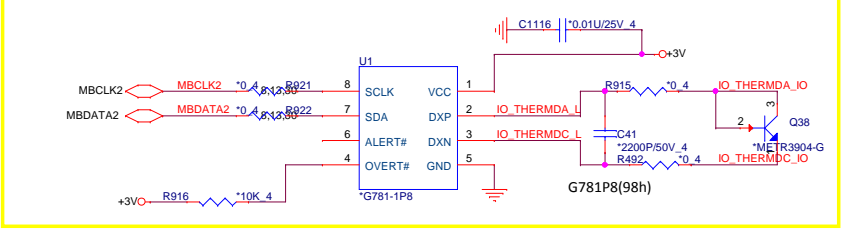
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 ddr-as0a26-uam-7f-204p-smt
 DGMK4000288
 SOCKET DDR3 SODIMM(204P,H9.2,RVS)QBCCN

DDR3 Thermal Sensor

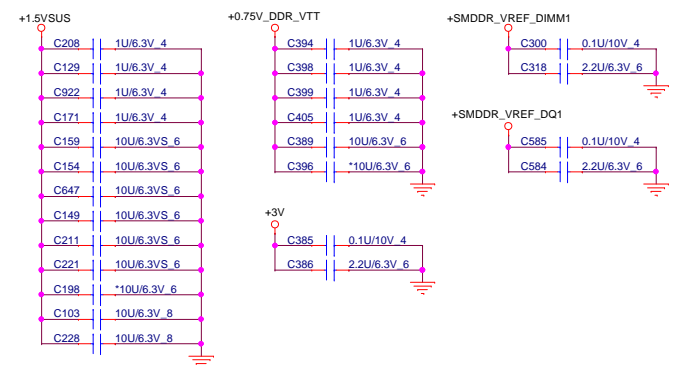


SI Add

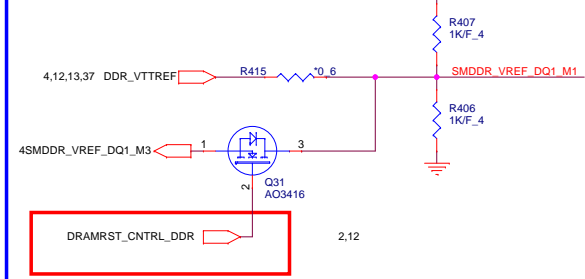
Local Thermal Sensor



Place these Caps near So-Dimm1.

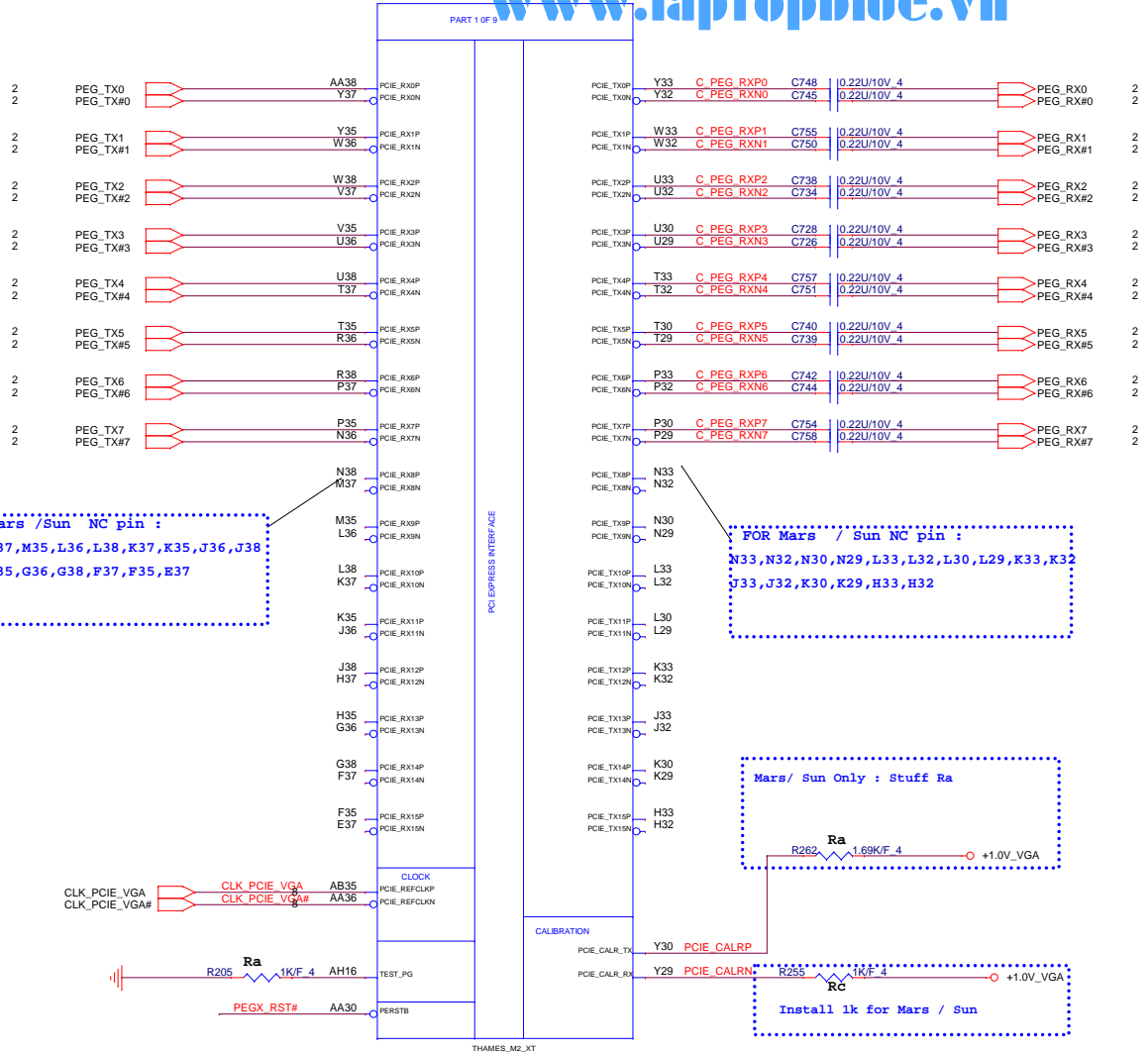


VREF DQ1 M1 Solution



PROJECT : R62
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	DDR3 DIMM1-RVS (9.2H)	
Date: Monday, October 22, 2012	Sheet 13	of 43

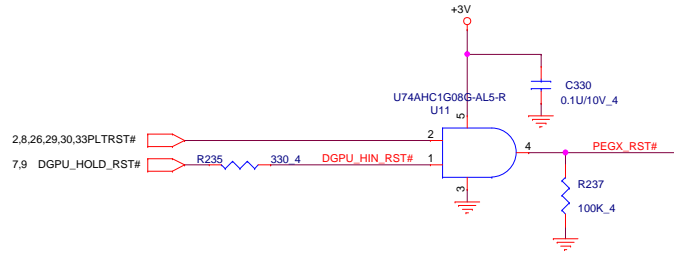


For Mars /Sun NC pin :
 N38, M37, M35, L36, L38, K37, K35, J36, J38,
 H37, H35, G36, G38, F37, F35, E37

FOR Mars / Sun NC pin :
 N33, N32, N30, N29, L33, L32, L30, L29, K33, K32,
 J33, J32, K30, K29, H33, H32

Mars/ Sun Only : Stuff Ra

Install 1k for Mars / Sun



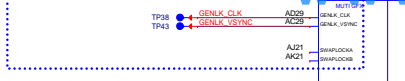
2,6,7,8,9,10,14,21,23,24,25,26,27,29,30,31,32,33,36,39-40,42,16,18,19,43 +1.0V_VGA

	PROJECT : R62 Quanta Computer Inc.		Rev 1A	
	Size Custom	Document Number THAMES_PCIE_Interface		
	Date: Monday, October 22, 2012			Sheet 14 of 43

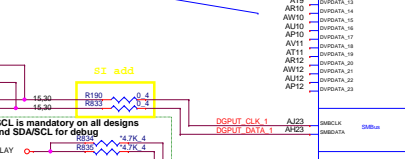
For Mars / Sun : AR1/AR6/AR3/AR8/AU8; NC pin

For Mars / Sun : DP A to D Port: all NC pin

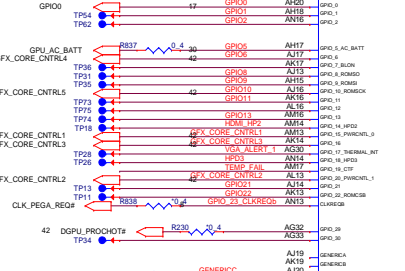
For Sun only : AP10 / AV11 / AT11 / AR12 / AM12 / AU12 / AP12 : NC pin



For Sun only : AP10 / AV11 / AT11 / AR12 / AM12 / AU12 / AP12 : NC pin



Access to SMBus and SDA/SCL is mandatory on all designs. Add test points on SMBus and SDA/SCL for debug.



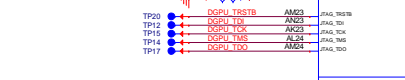
For Sun GPIO NC PIN : AJ19 / AK19 / AK24 / AM14 / AM14 / AJ24 / AR26 / AR24 / AJ20

Mars: aruffe +1.8V_VGA

For Sun No: R167, R141, C923



SI change to SUN setting



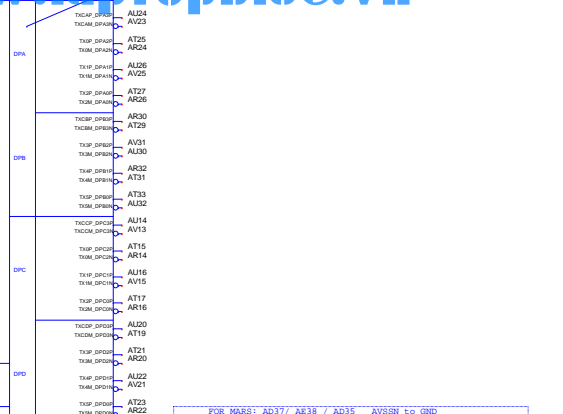
Main:AL000781039 G781-1P8(9Ah) 2nd:AL001412005 EMC1412-2-ACL-TR(9Ah)



For Mars: Stuff Ra, Rc=> VDDC 1.1V

For Mars / Sun:nc pin AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

For Sun Only :nc pin AL27, AM27, AM20, AN20, AM26, AM19, AM19, AJ30, AJ31



FOR MARS: AD37 / AR38 / AD35 AVSSEN to GND

FOR SUN: AD37 / AR38 / AD35 NC pin



SI DEL reverse R749,R755,R759



FOR SUN NC PIN : AD34 / AR34 / AC33 / AC34 / AD39 / AB36

AF37 / AC36 / AC38 / AB34 / 4

NC: TSVD50 AF33

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

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PS: AC31 PS_2 P27

PS: AD33 PS_3 P37

PS: AM34 PS_0 P88

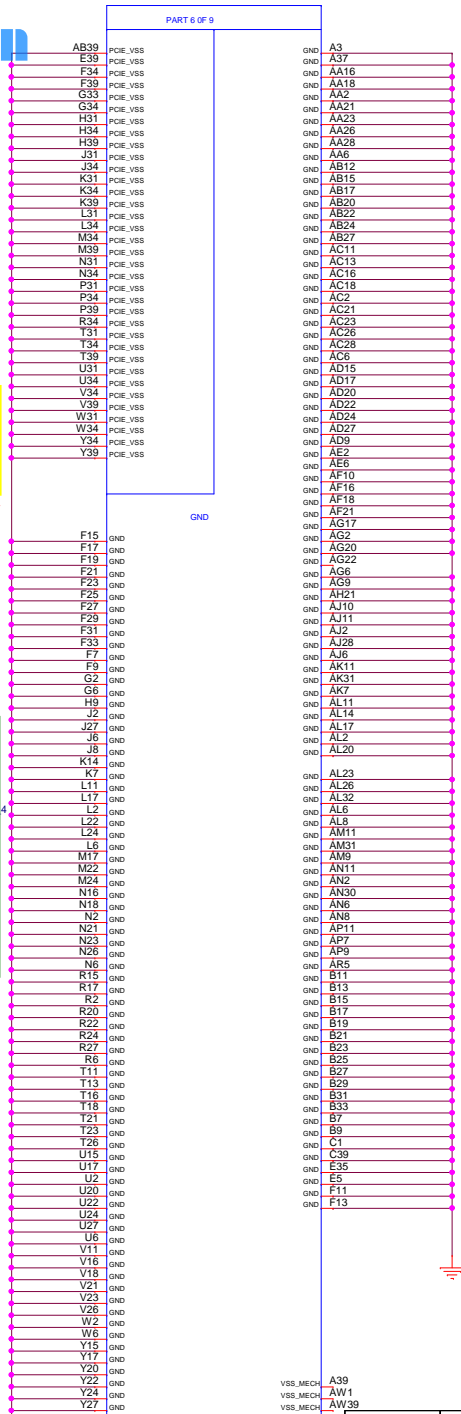
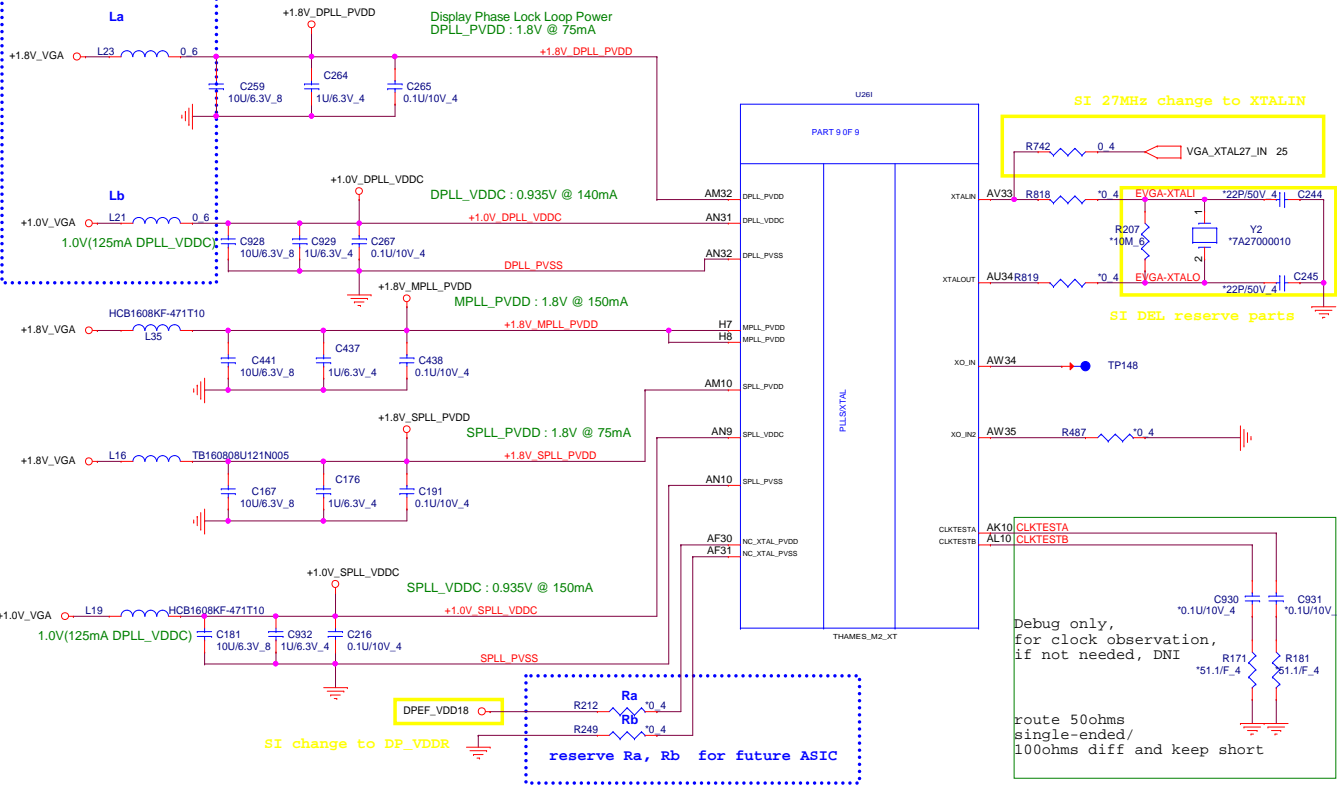
PS: AD31 PS_1 P40

PS: AC31 PS_2 P27

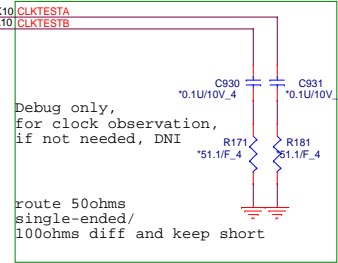
PS: AD33 PS_3 P37

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm



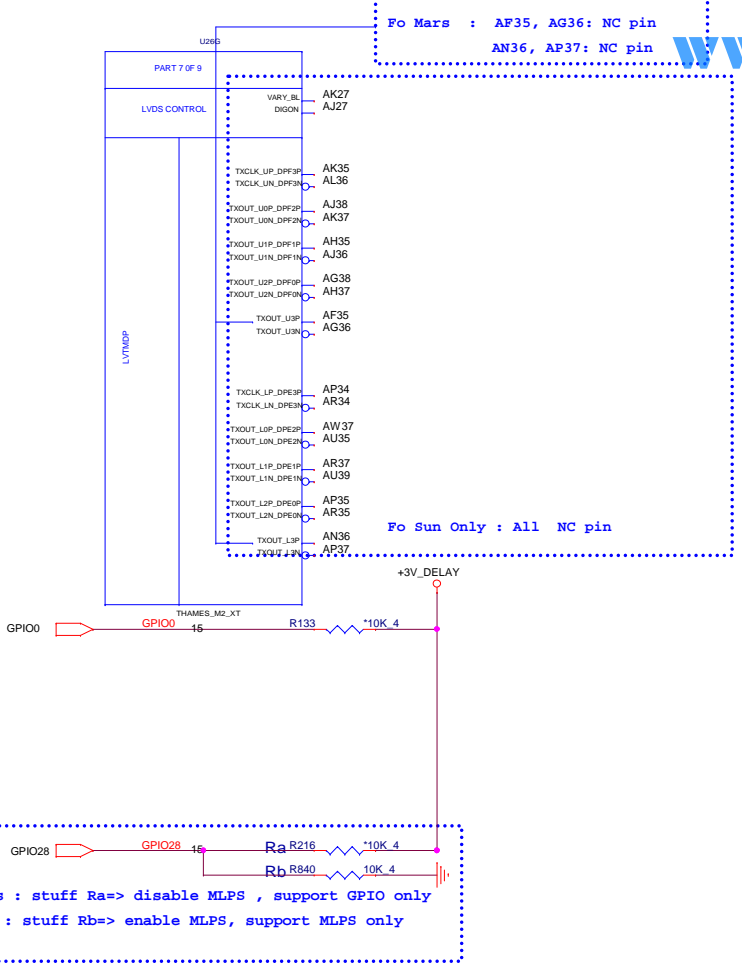
14,18,19,43 +1.0V_VGA → +1.0V_VGA
15,18,19,25,42 +1.8V_VGA → +1.8V_VGA



AG22 is nc pin



PROJECT : R62
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CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

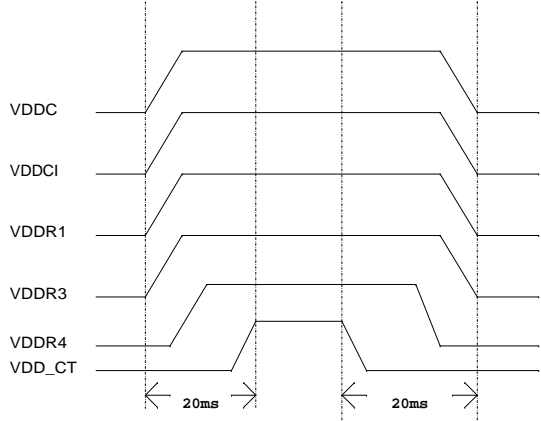
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P05A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9	BIOSROM	GPIO13	GPIO12	GPIO11
ROMIDCFG2	ROMIDCFG1	ROMIDCFG0		
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

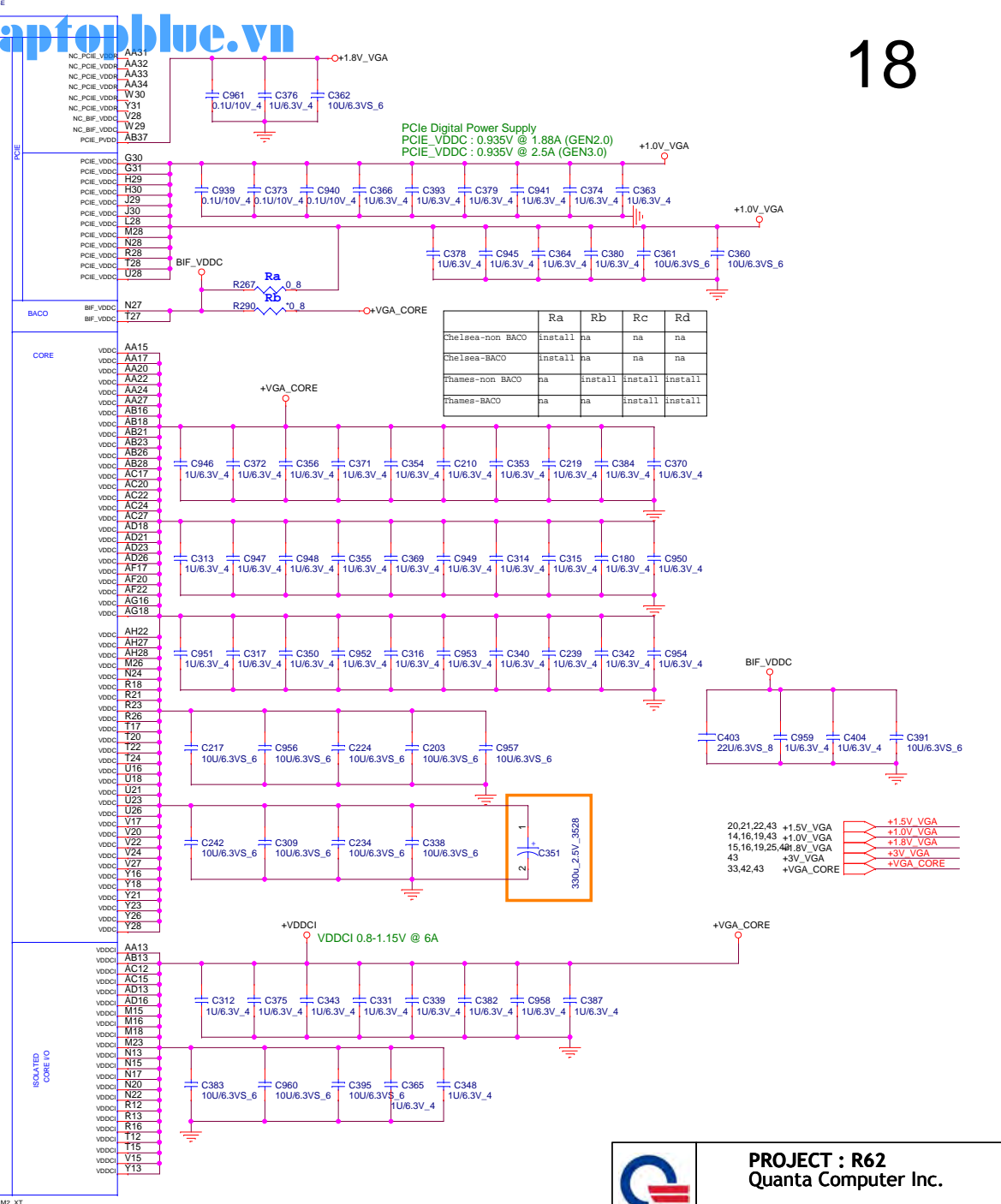
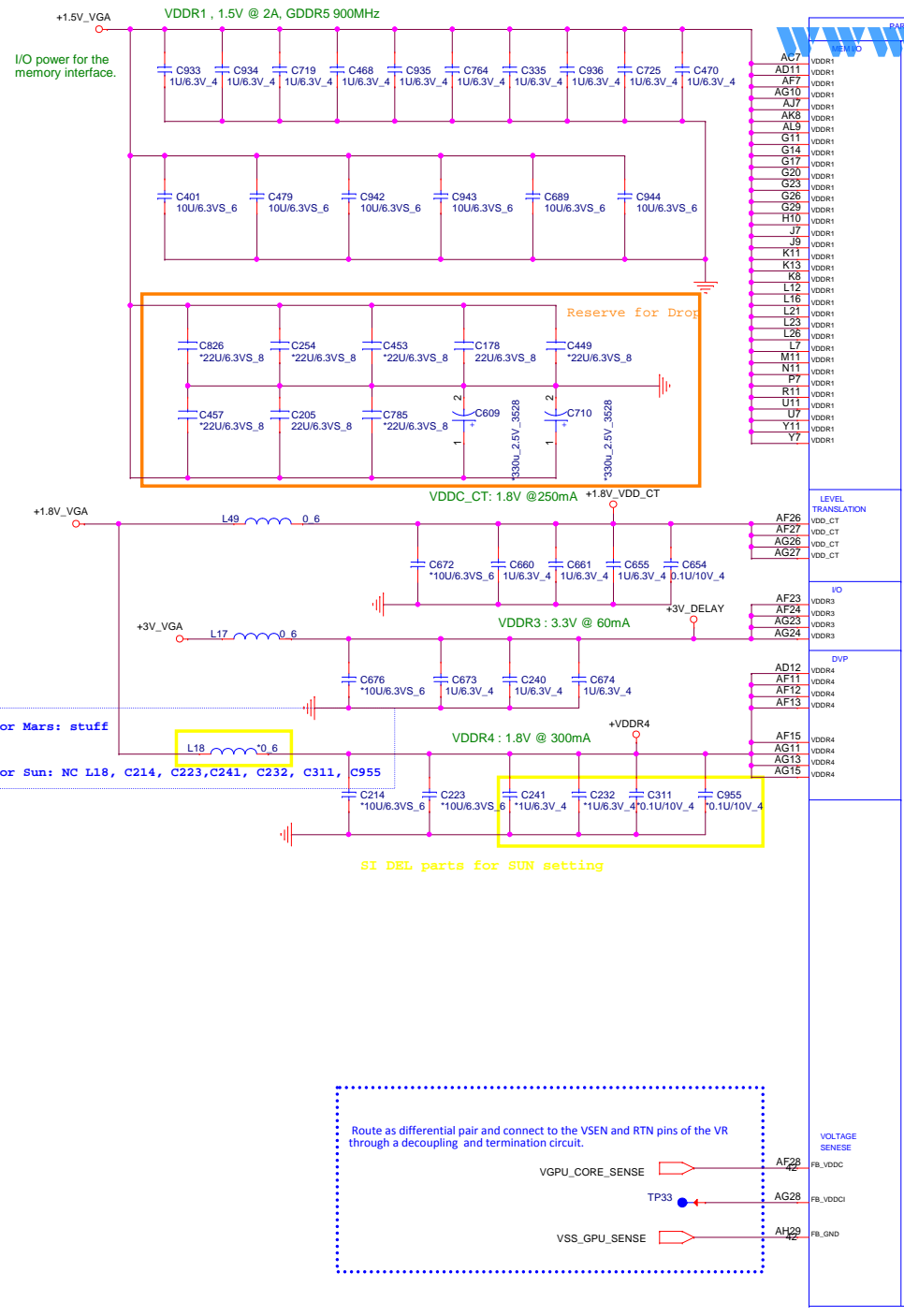
Power Up/Down Sequence



PROJECT : R62
Quanta Computer Inc.

NB5

Size Custom	Document Number THAMES_LVDS / STRAP	Rev 1A
Date: Monday, October 22, 2012		Sheet 17 of 43

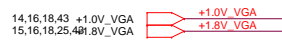
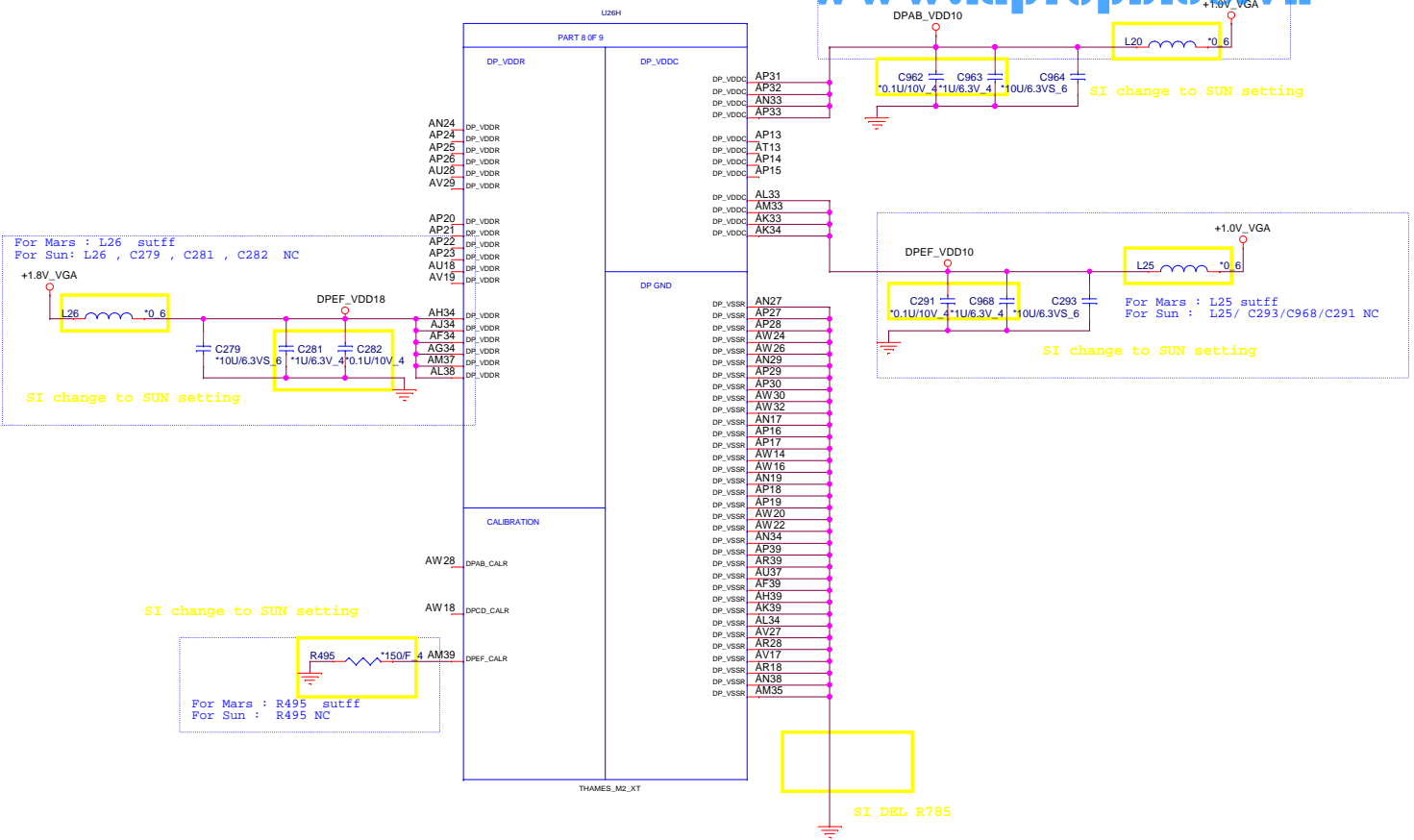


PROJECT : R62
Quanta Computer Inc.

NB5

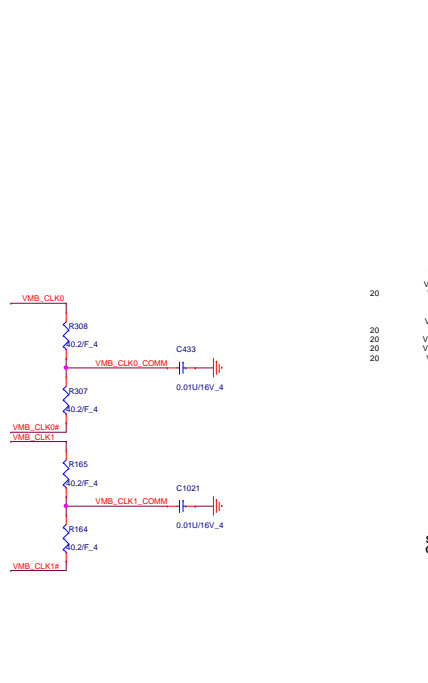
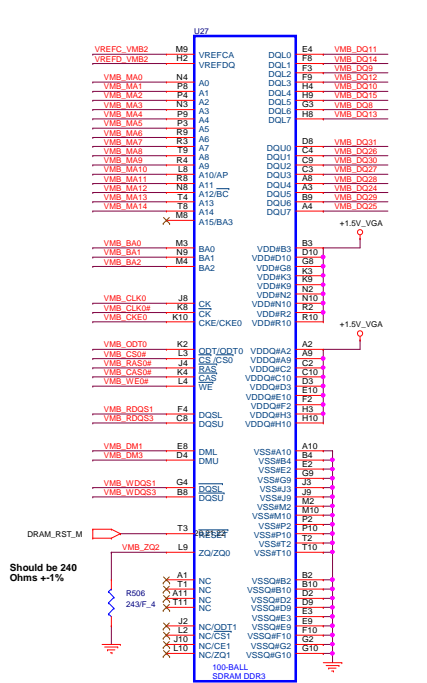
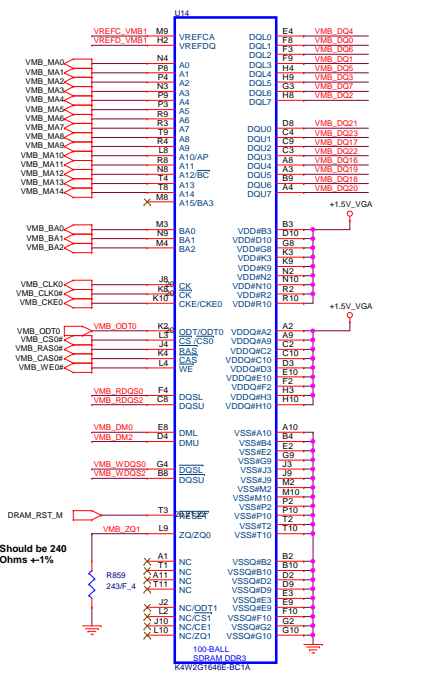
Size	Document Number	Rev
Custom	THAMES_Power & BACO	1A

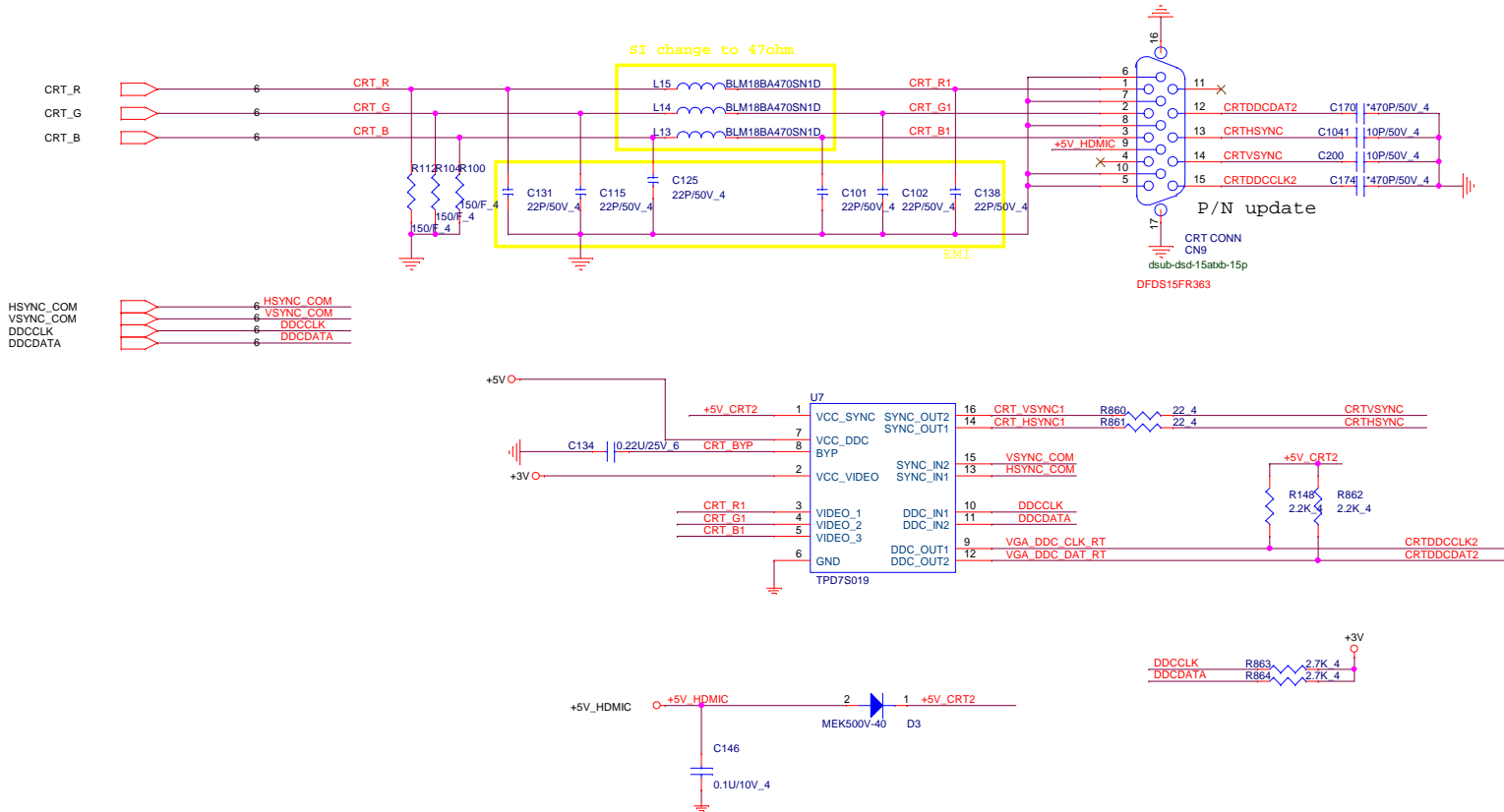
Date: Monday, October 22, 2012 | Sheet 18 of 43



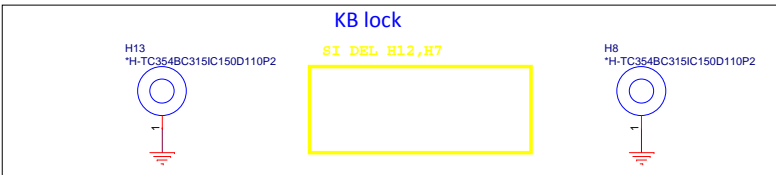
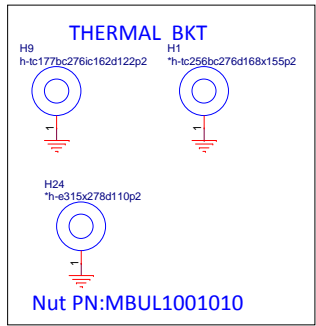
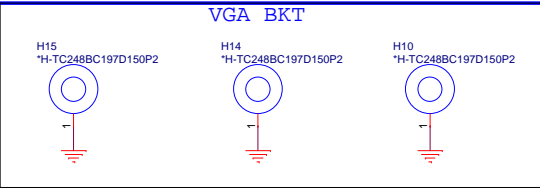
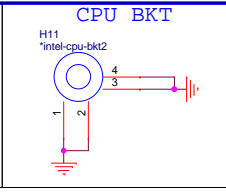
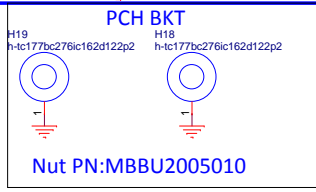
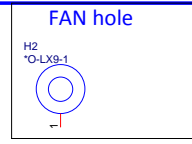
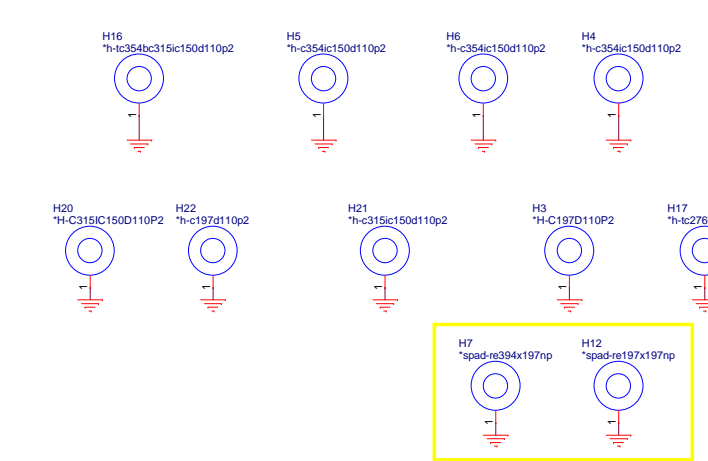
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number THAMES_DP Powers	
Date: Monday, October 22, 2012		Sheet 19 of 43	

CHANNEL B: 256MB/512MB DDR3

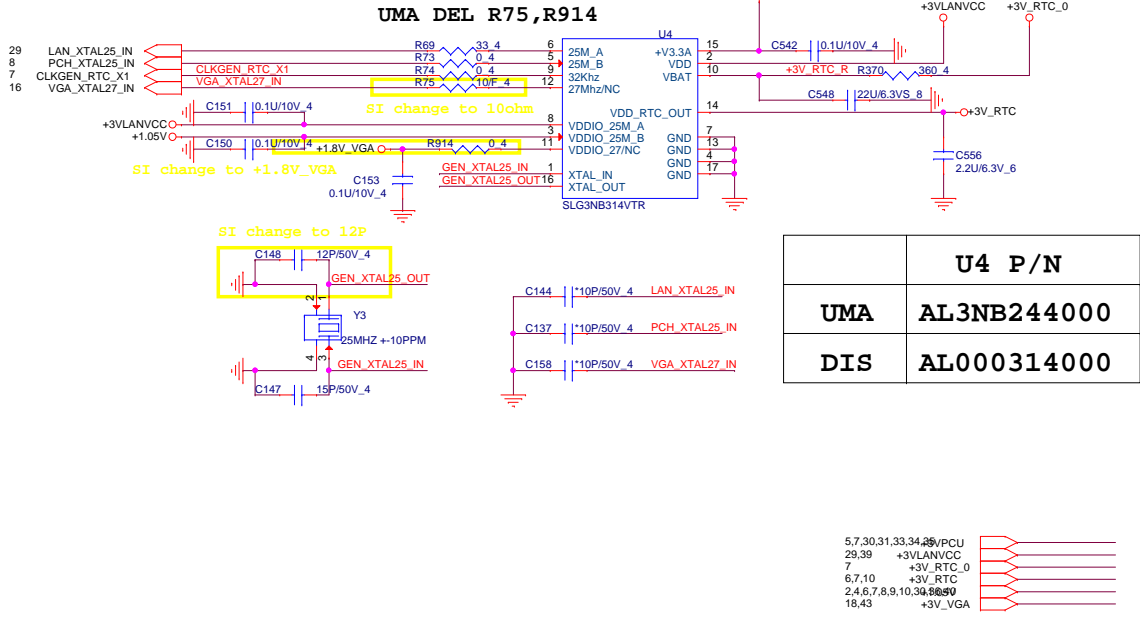




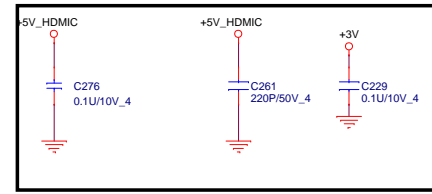
HOLE



	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number CRT,Hole	
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EMI request

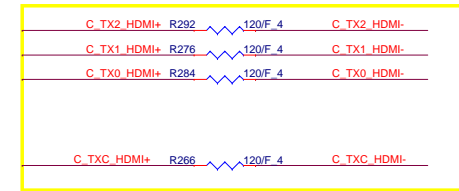


7,10,23,27,31,32,33,34,38,40,42

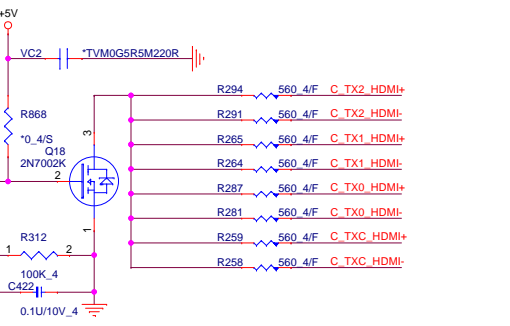
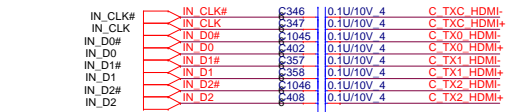
23 +5V_HDMIC

2,6,7,8,9,10,12,13,14,23,24,26,27,29,30,31,32,33,36,39,40,42

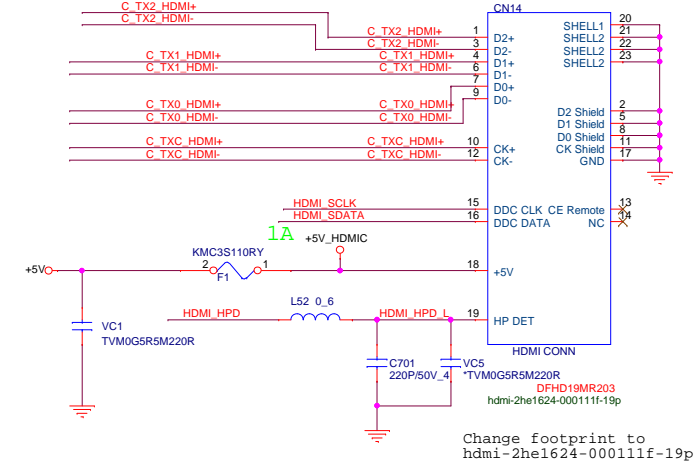
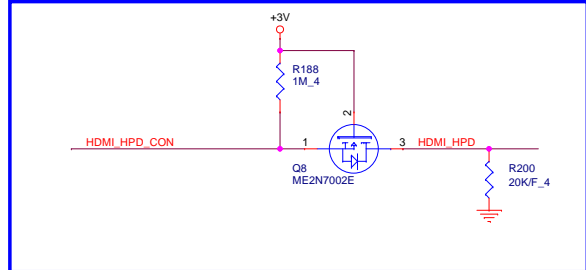
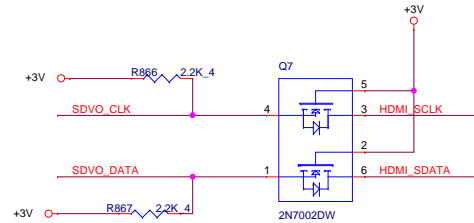
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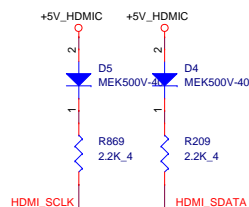
close to HDMI conn



Close to HDMI Connector



Change footprint to hdmi-2he1624-000111f-19p



PROJECT : R62
Quanta Computer Inc.

NB5

Size Custom	Document Number	Rev 1A
HDMI CONN		
Date: Monday, October 22, 2012	Sheet 25	of 43

8 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R446 0.4S CLK_PCIE_REQ2#_R

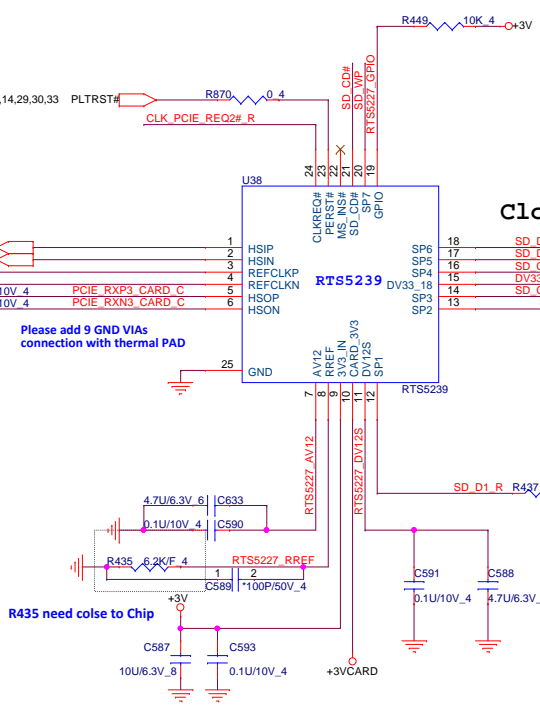
SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD_WP	MS_BS

Share Pin

Close to chip pin

- 8 CLK_PCIE_CARDP
- 8 CLK_PCIE_CARDN
- 8 PCIE_RXP3_CARD
- 8 PCIE_RXN3_CARD

- 1 HSIP
- 2 HSIN
- 3 REFCLKP
- 4 REFCLKN
- 5 HSOP
- 6 HSON



Please add 9 GND VIAs connection with thermal PAD

R435 need close to Chip

Close to chip pin

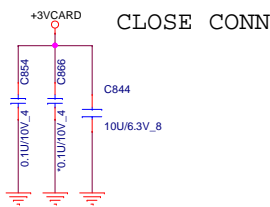
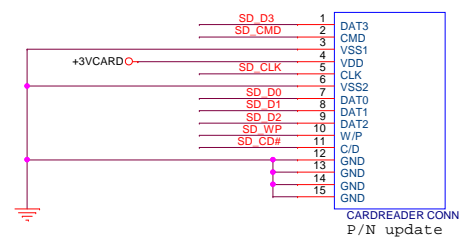
- 18 SD D2 R R871 0.4 SD D2
- 17 SD D3 R R443 0.4 SD D3
- 16 SD CMD R R444 0.4 SD CMD
- 15 DV33_1B DV33_1B
- 14 SD CLK R R441 22.4 SD CLK C1048 5.6P/16V_4
- 13 SD D0 R R442 0.4 SD D0

Reserve for EMI

SD D0	C1069	5.6P/16V_4
SD D1	C612	5.6P/16V_4
SD D2	C611	5.6P/16V_4
SD D3	C1068	5.6P/16V_4

Close to U38

SD / MMC CARD READER



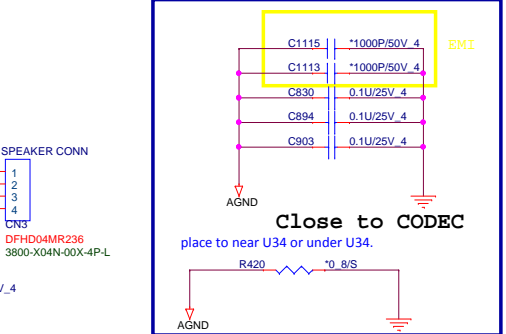
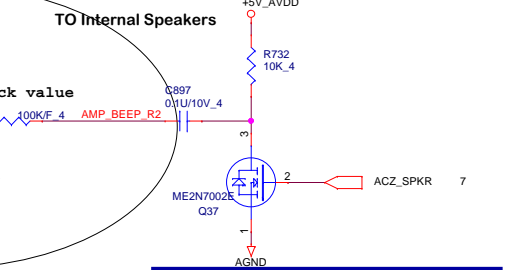
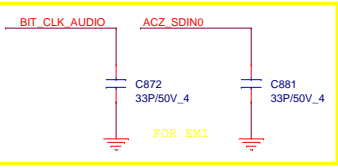
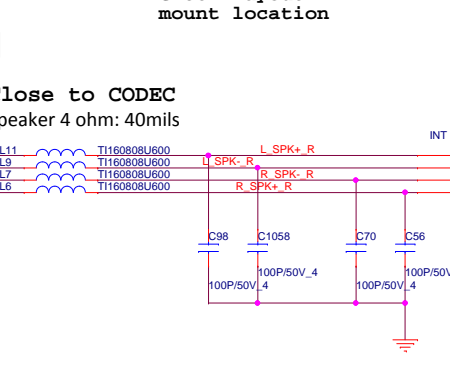
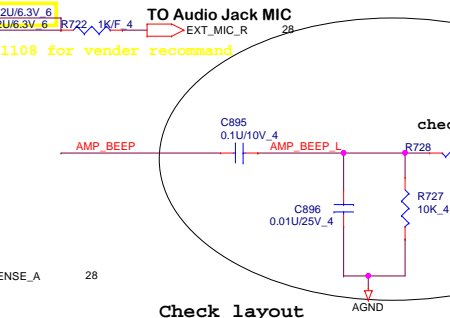
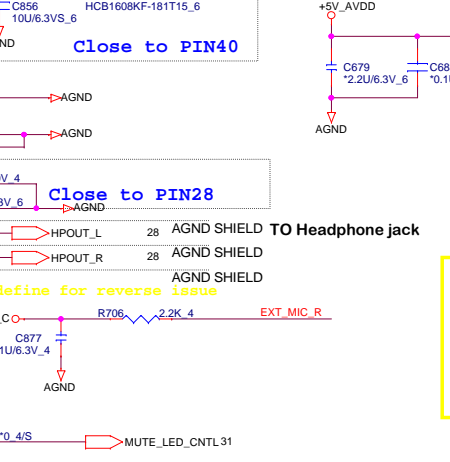
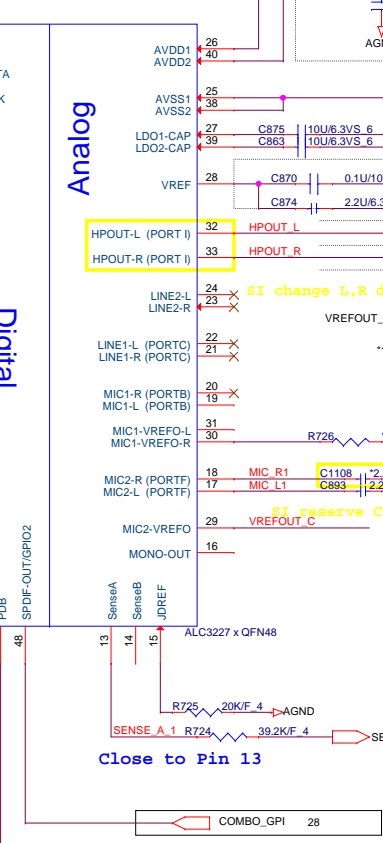
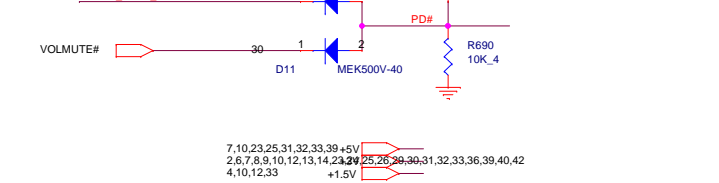
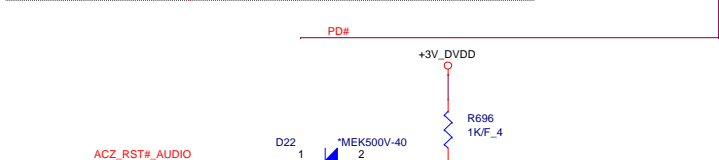
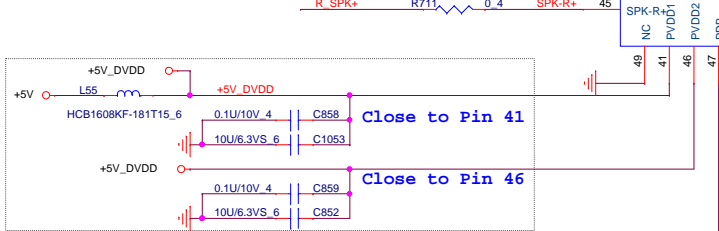
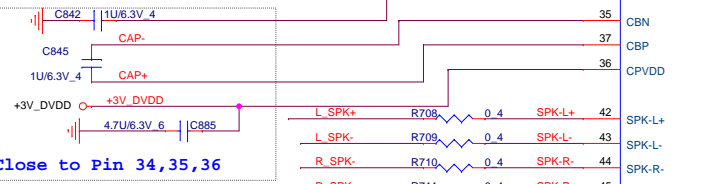
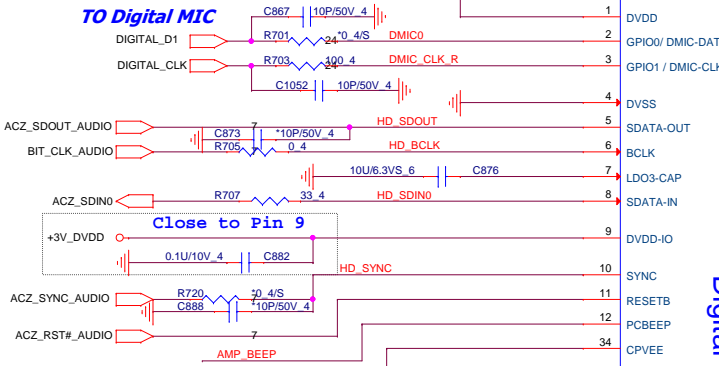
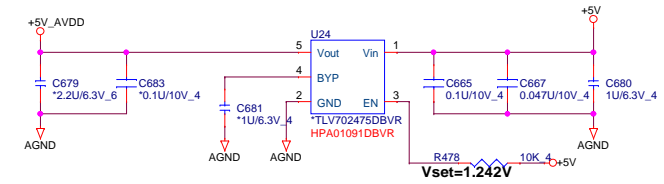
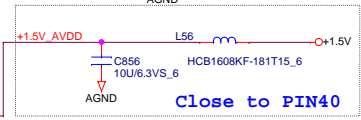
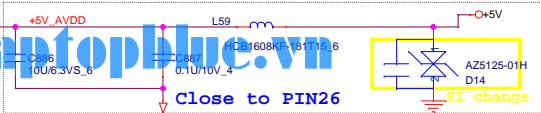
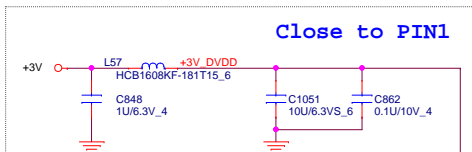
Reserve for EMI

SD D0	C1049	5.6P/16V_4
SD D1	C886	5.6P/16V_4
SD D2	C610	5.6P/16V_4
SD D3	C1050	5.6P/16V_4
SD CLK	C1100	5.6P/16V_4

Close to CN8

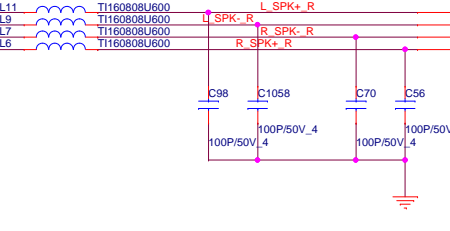
2,6,7,8,9,10,12,13,14,23,24,25,27,29,30,31,32,33,36,39,40,42

	<p>PROJECT : R62 Quanta Computer Inc.</p>		
	<p>Size Custom</p>	<p>Document Number RTS5229 & CR SOCKET</p>	<p>Rev 1A</p>
	<p>Date: Monday, October 22, 2012 Sheet 26 of 43</p>		

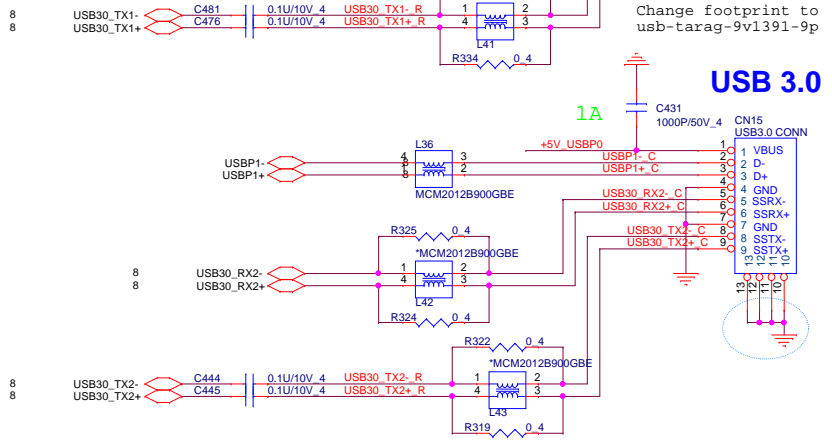
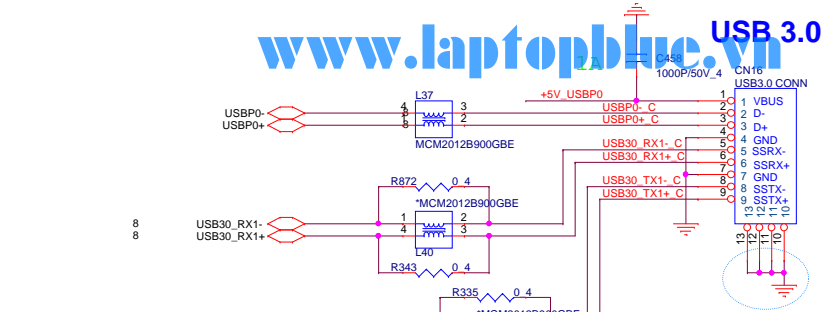
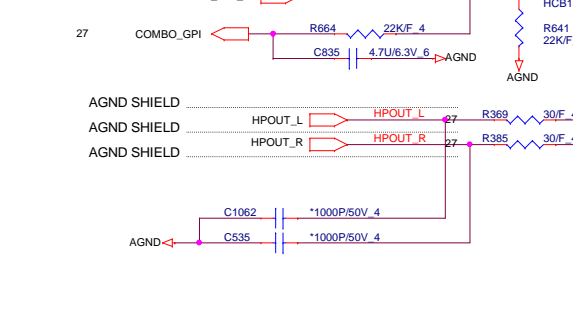
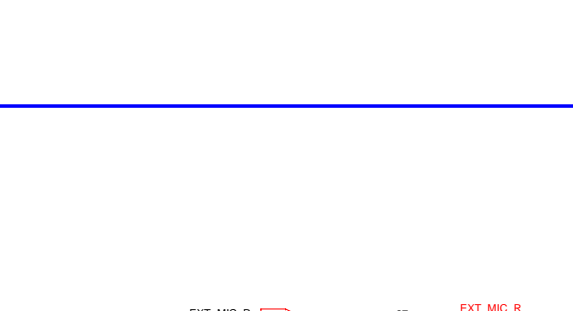
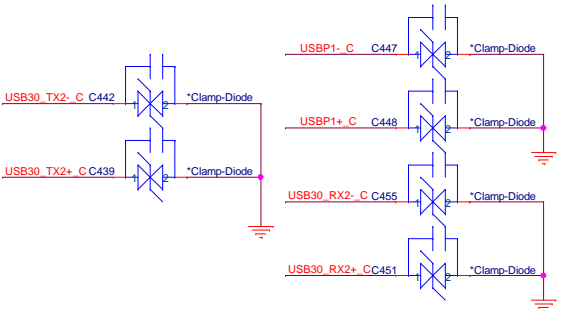
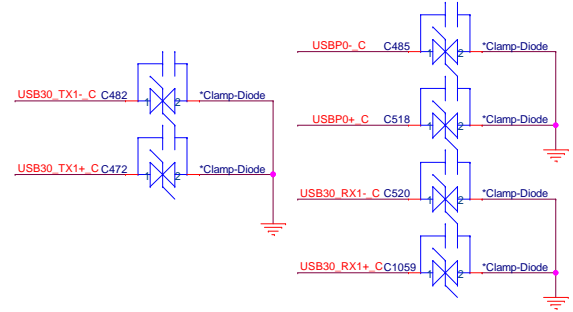


Keep L_SPK+/-, and R_SPK+/- trace width 30 mil least

Close to CODEC Speaker 4 ohm: 40mils

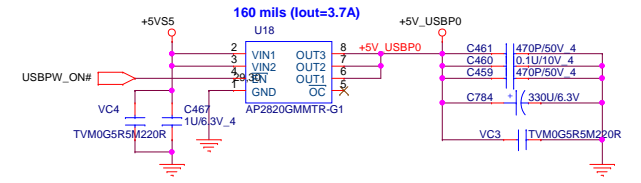


Close to CODEC place to near U34 or under U34.

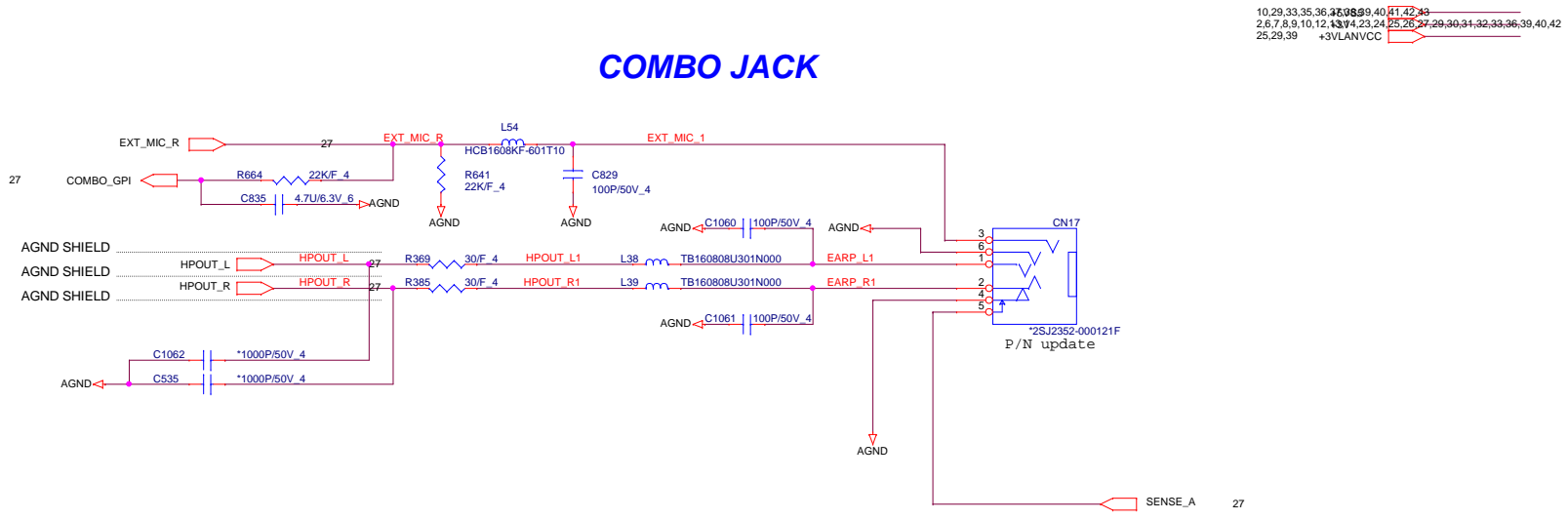


Change footprint to usb-tarag-9v1391-9p

USB3.0 X 2/USB2.0 COMBO

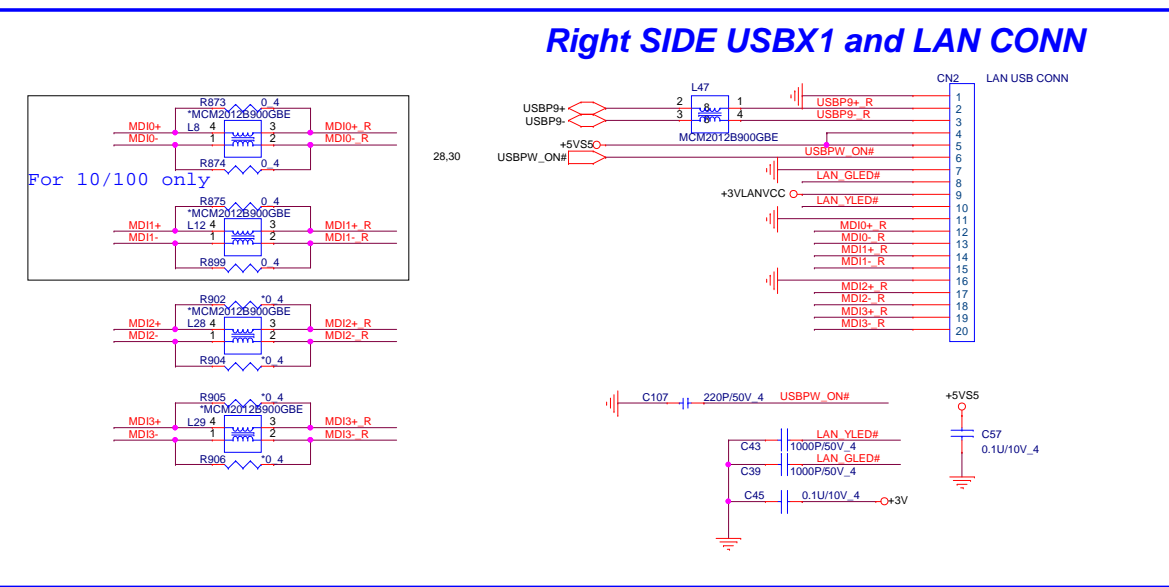
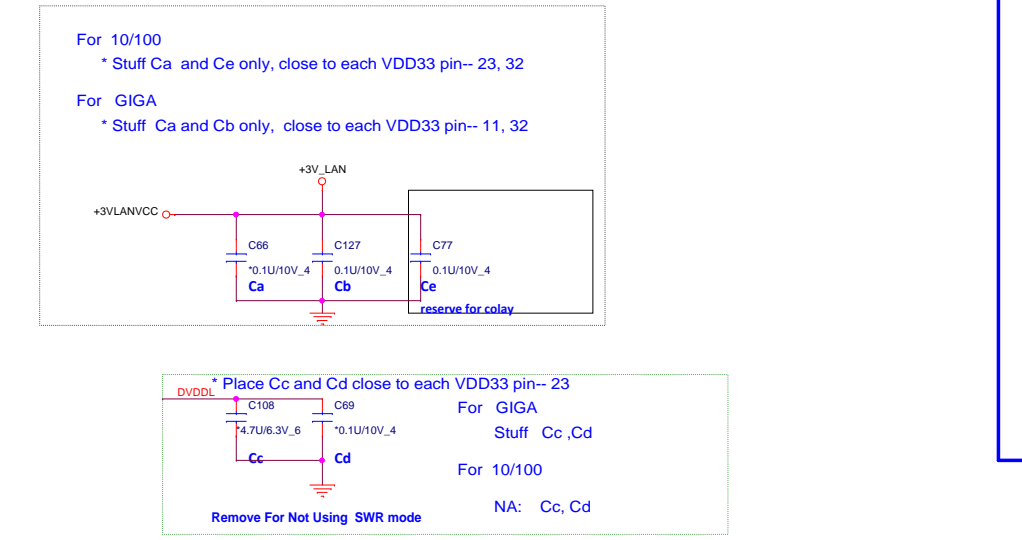
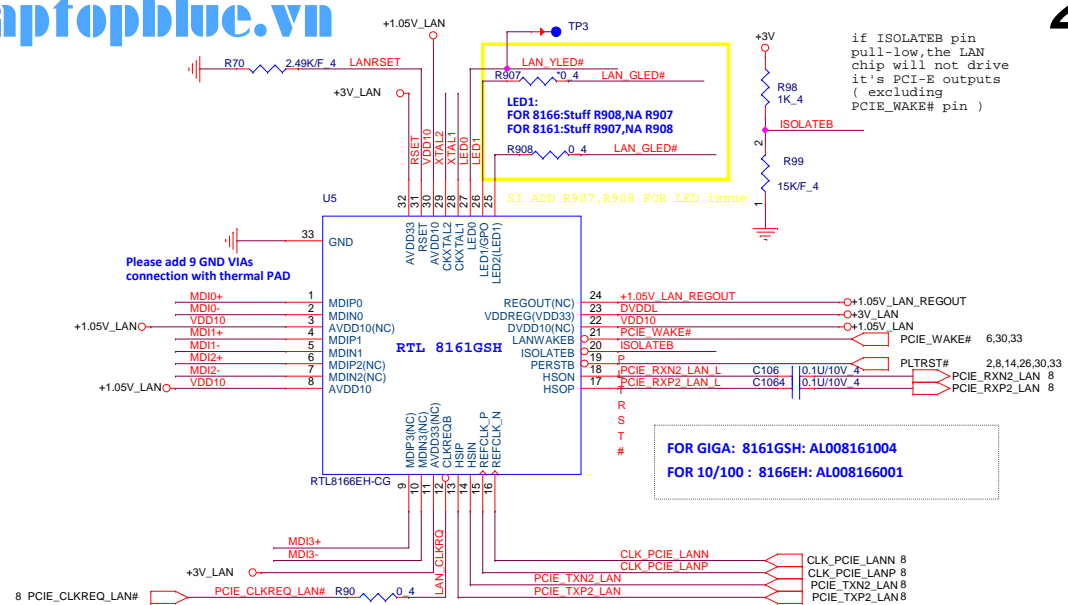
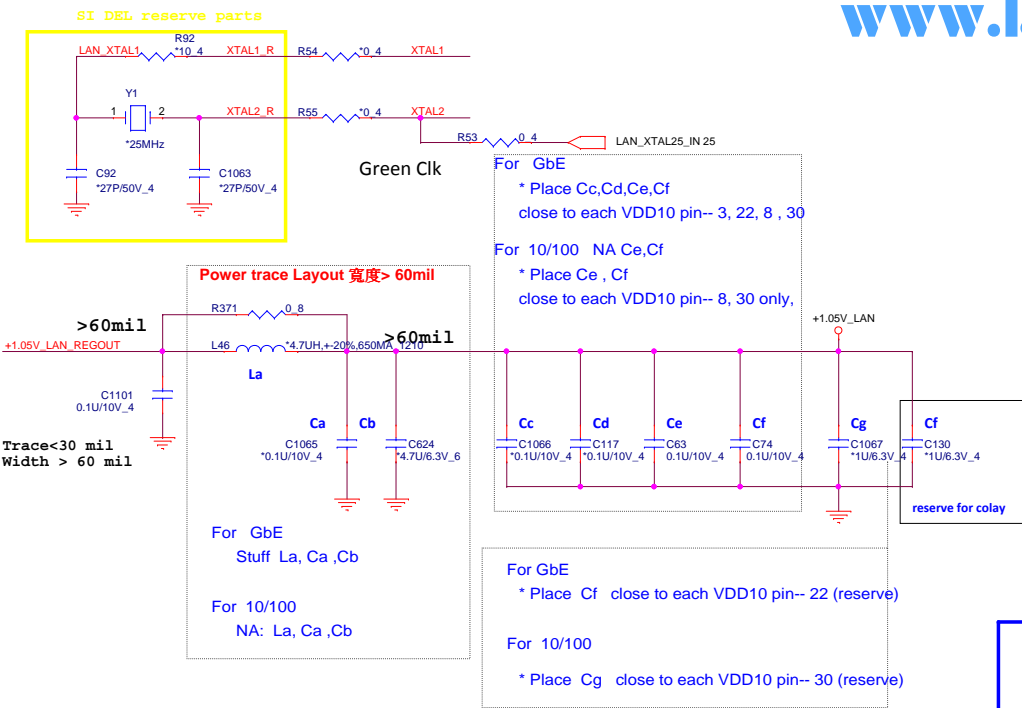


COMBO JACK

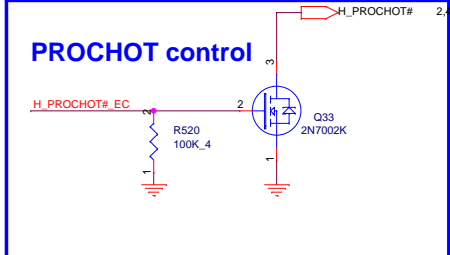
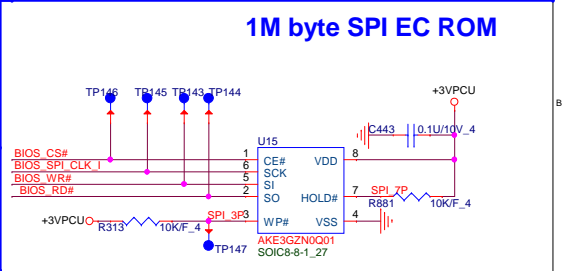
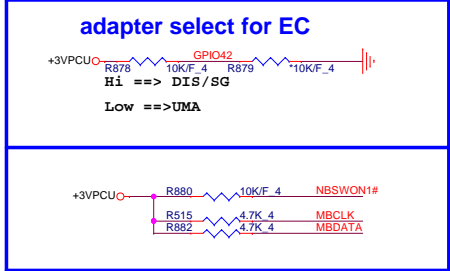
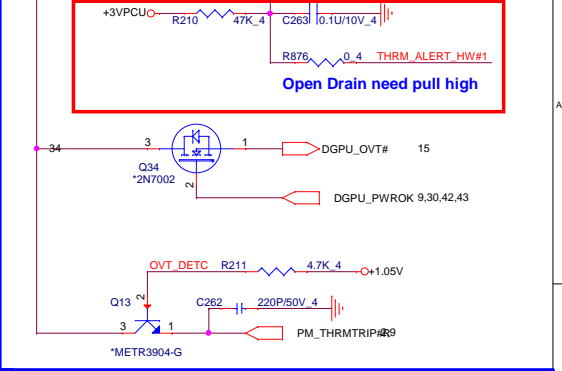
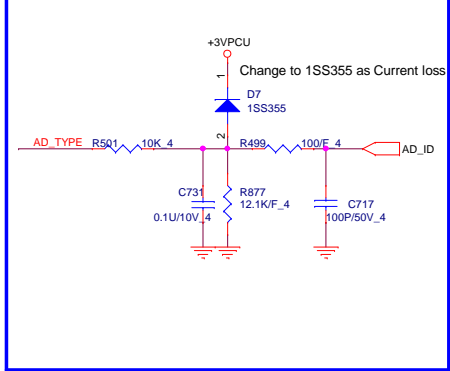
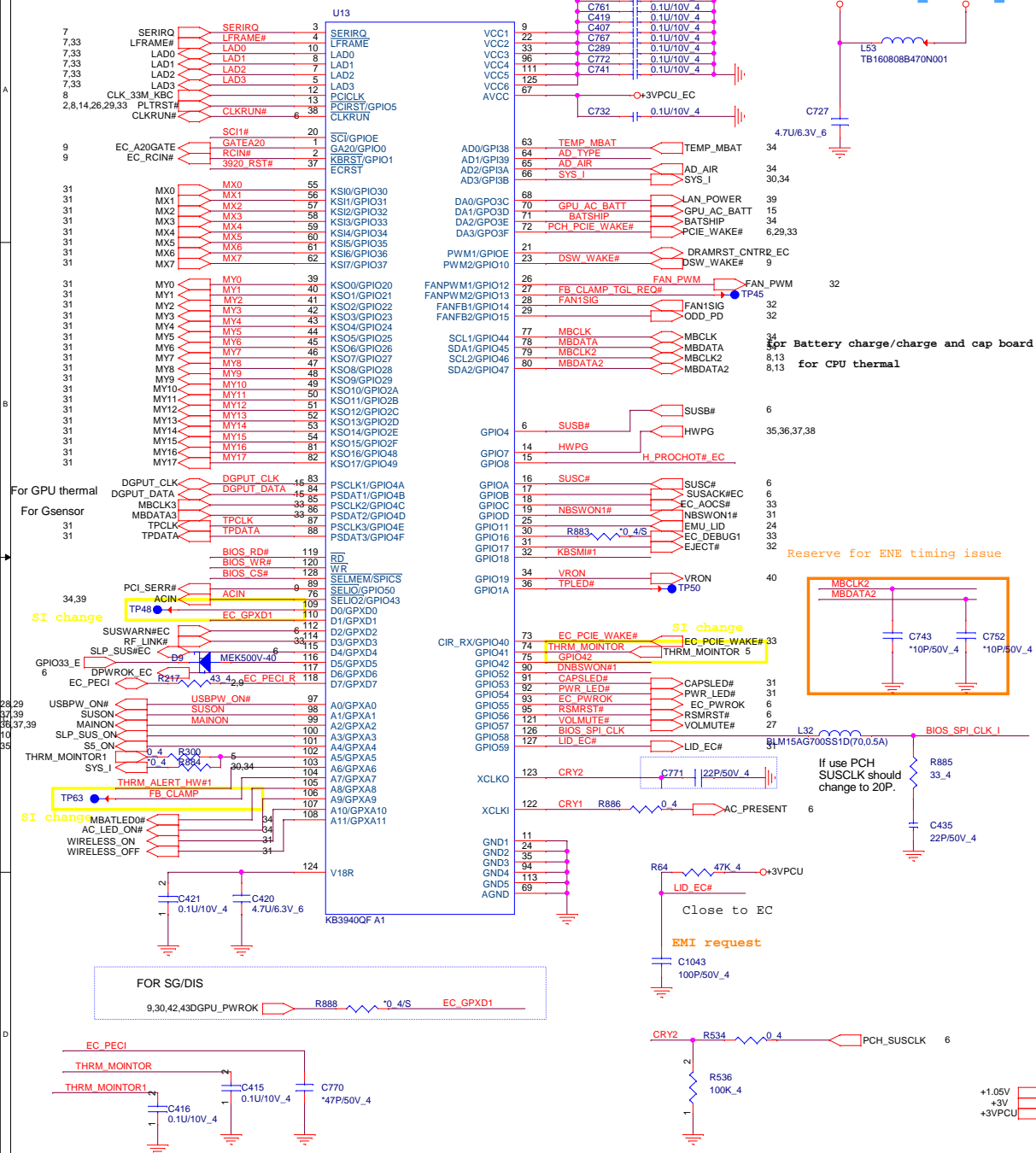


10,29,33,35,36,37,38,39,40,41,42,39
 2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
 25,29,39 +3VLANVCC

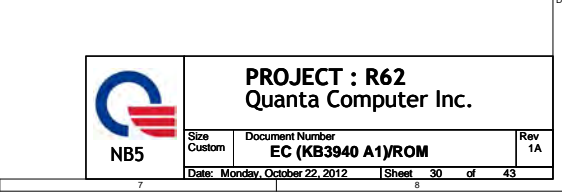
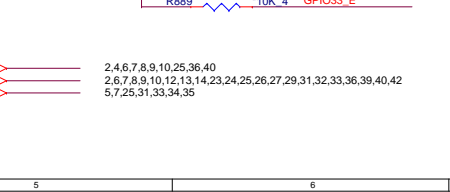
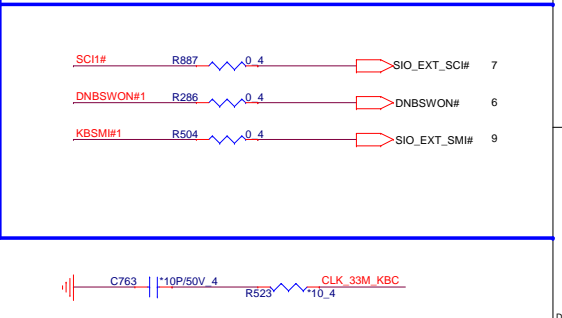
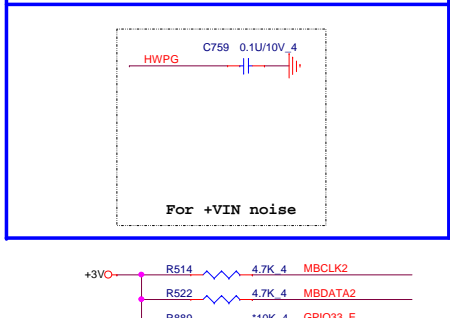
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number USB/BT/Audio Jack	Date: Monday, October 22, 2012 Sheet 28 of 43	



2,6,7,8,9,10,12,13,14,23,24,25,26,27,30,31,32,33,36,39,40,42,25,39 +3VLANVCC



Vender	Size	P/N
EON	1MB	AKE3GZNOQ01 (EN25Q80A-100HIP)
GigaDevice	1MB	AKE3GGN0Q00 (GD25Q80BSIGR)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

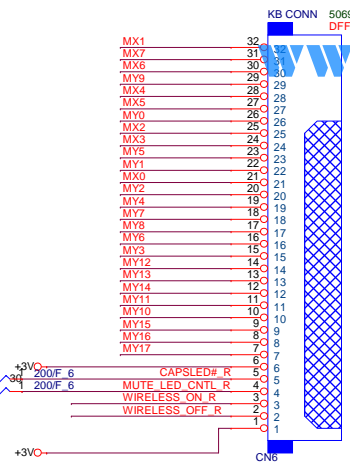
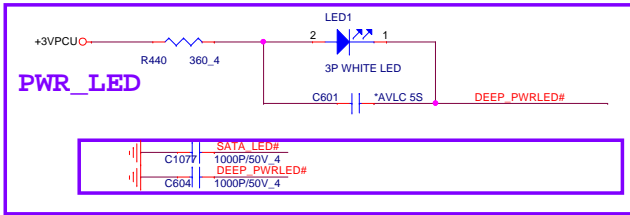
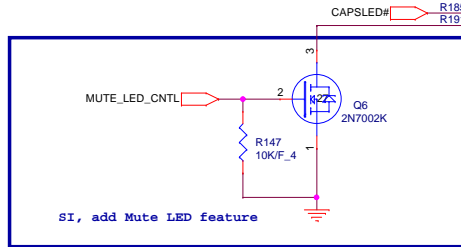
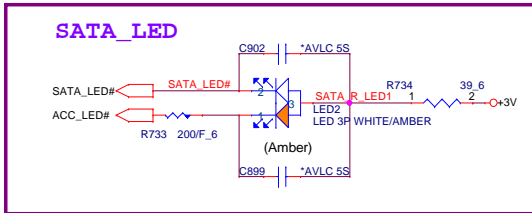
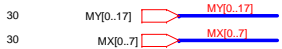


PROJECT : R62
Quanta Computer Inc.

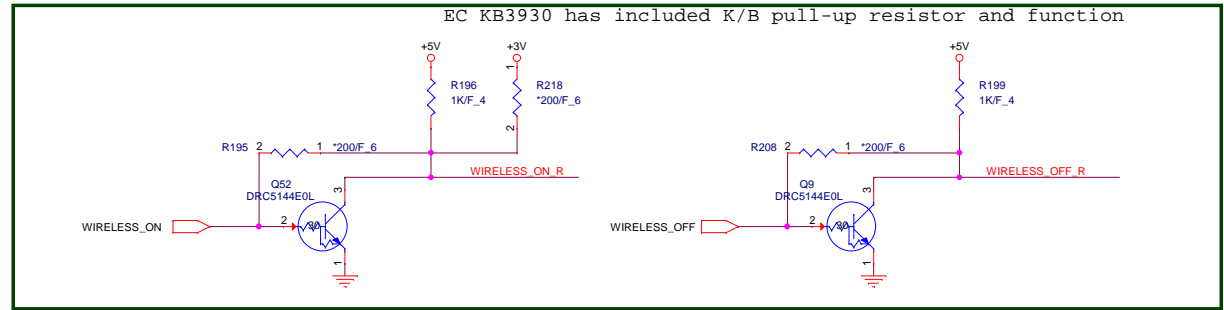
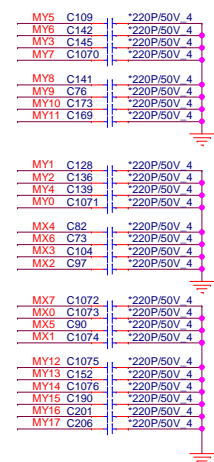
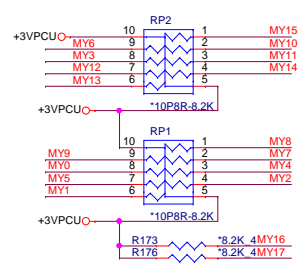
NB5

Size Custom	Document Number EC (KB3940 A1)/ROM	Rev 1A
Date: Monday, October 22, 2012	Sheet 30 of 43	

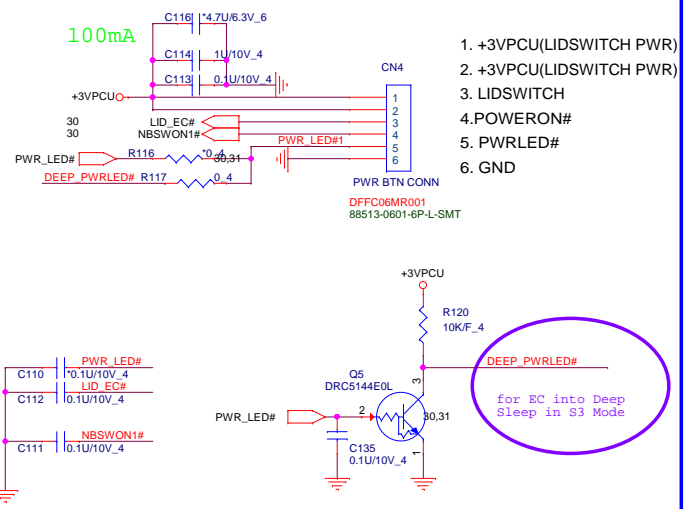
KEYBOARD Con.



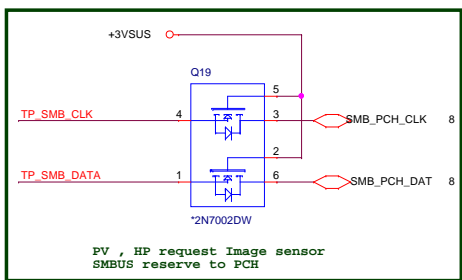
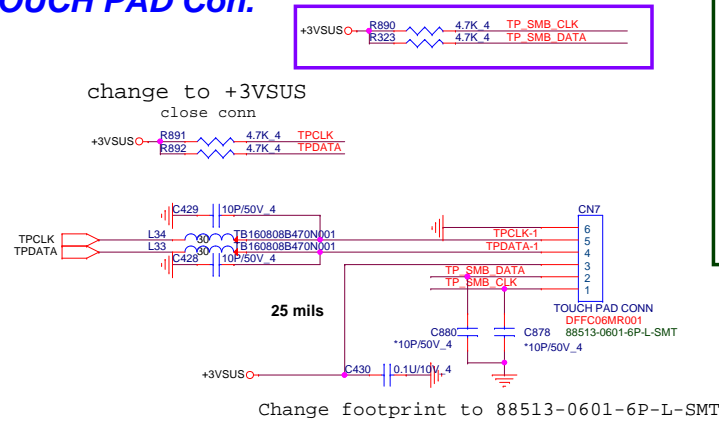
KEYBOARD PULL-UP



POWER BOTTON CONNECT



TOUCH PAD Con.

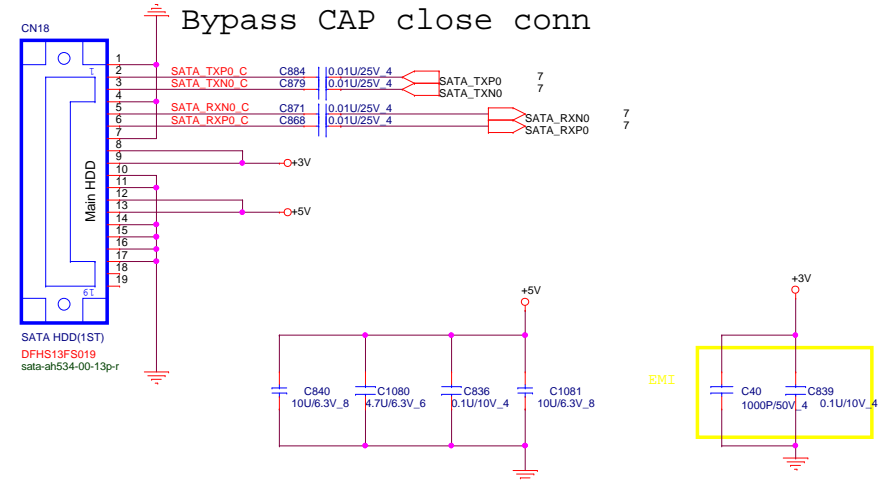
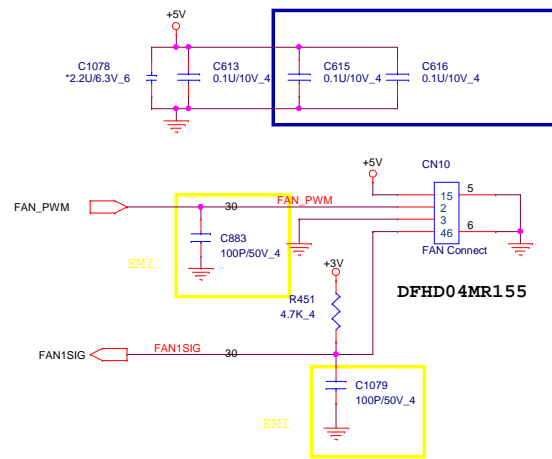


NB5	Size Custom	Document Number	Rev 1A
		LED/KB/SW/TP	

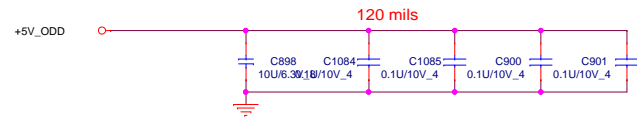
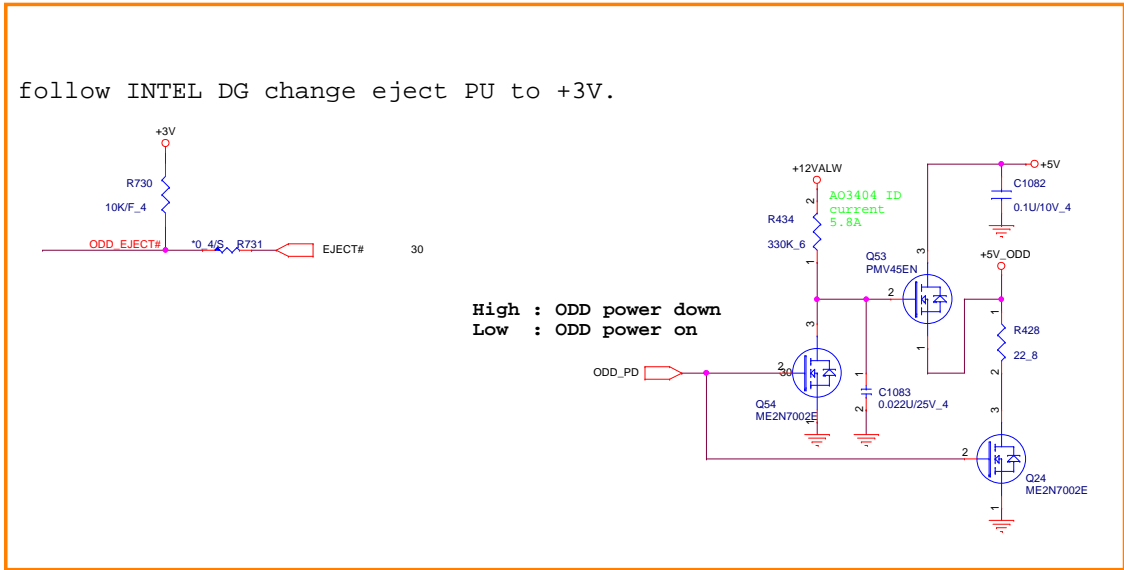
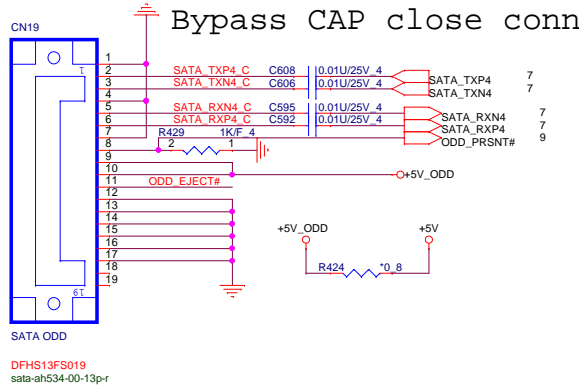
PROJECT : R62
Quanta Computer Inc.

Date: Monday, October 22, 2012 | Sheet 31 of 43

CPU FAN



SATA ODD CONNECTOR

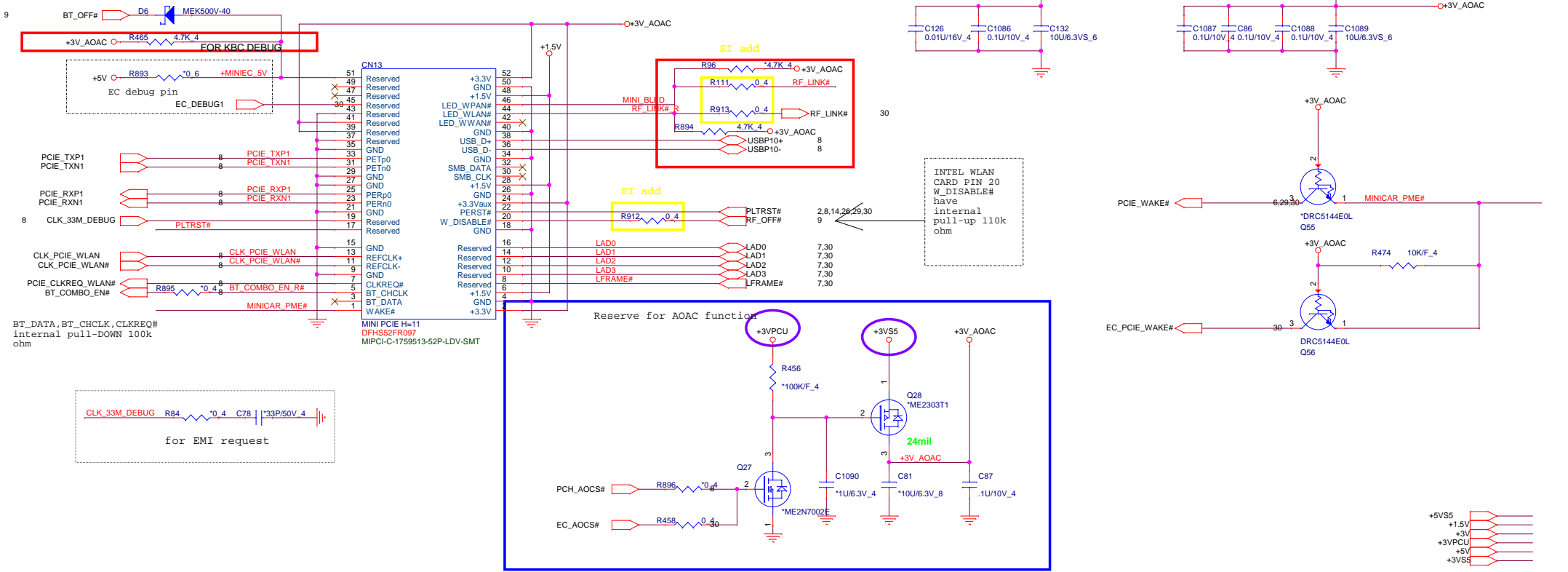


+3V	2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42
+3VPCU	5,7,25,30,31,33,34,35
+5V	7,10,23,25,27,31,33,39
+12VALW	34,39,43

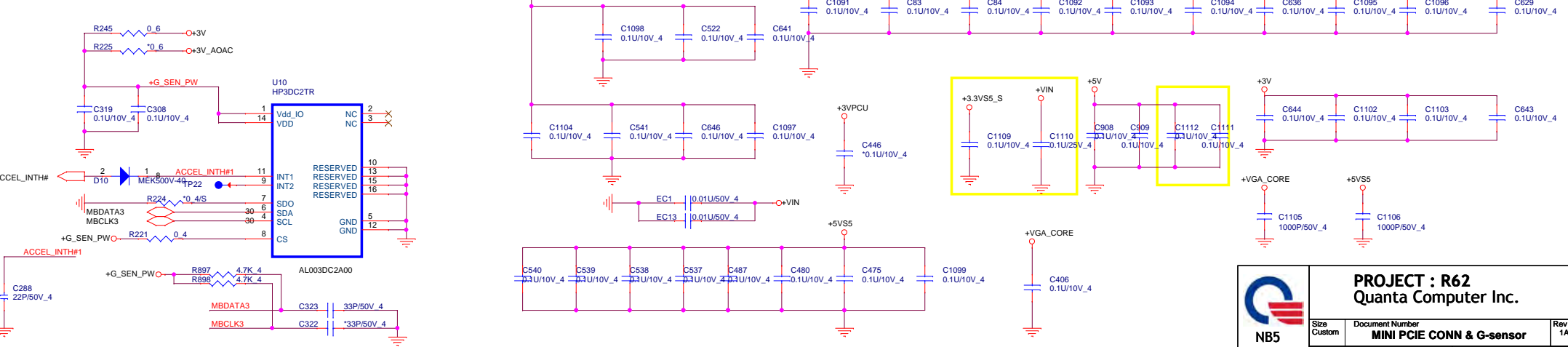
PROJECT : R62
Quanta Computer Inc.

Size Custom	Document Number HDD/ODD/FAN	Rev 1A
Date: Monday, October 22, 2012 Sheet 32 of 43		

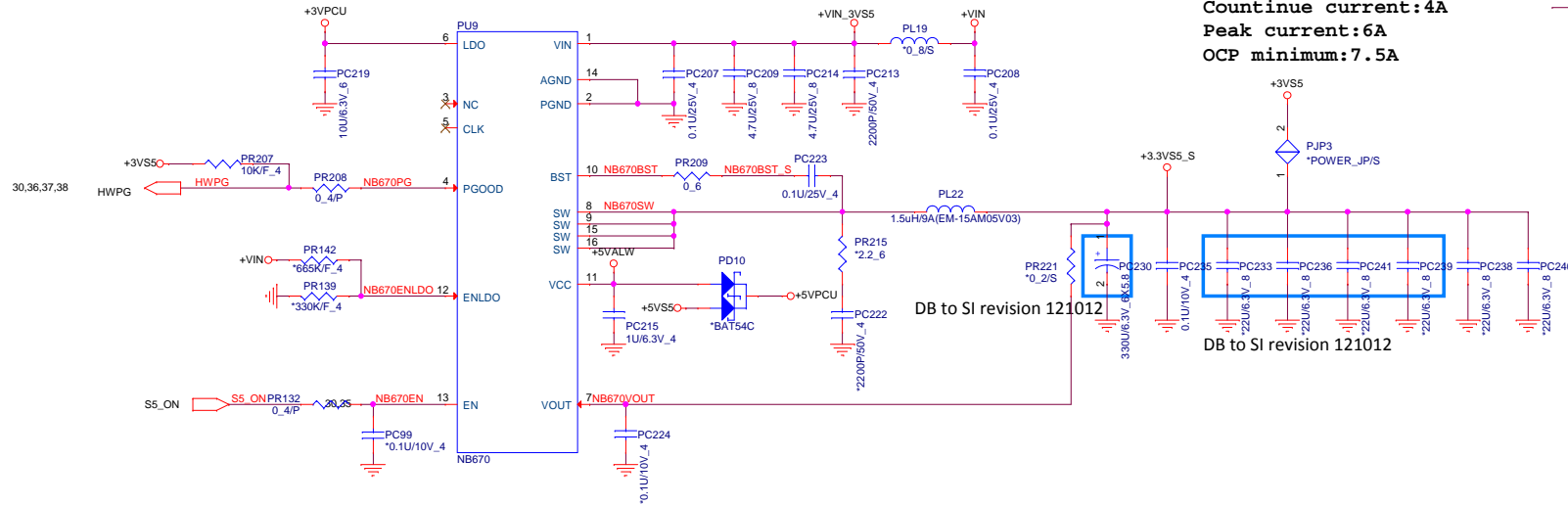
Mini PCI-E Card 1 WLAN



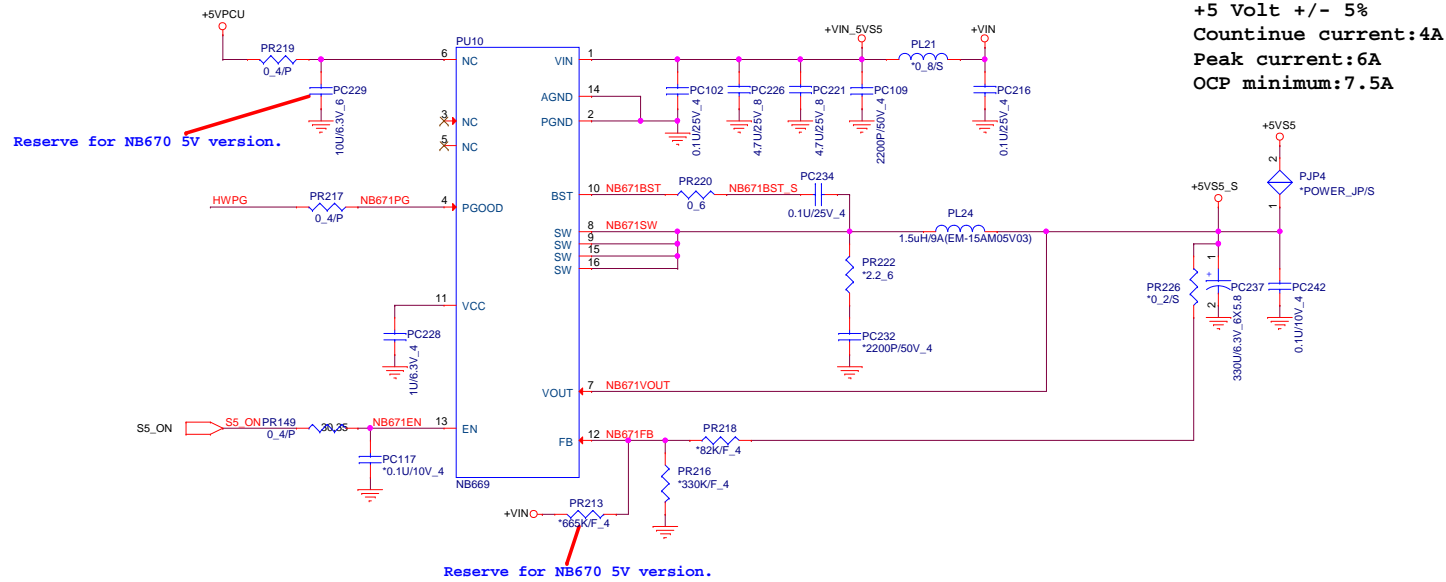
Accelerometer Sensor



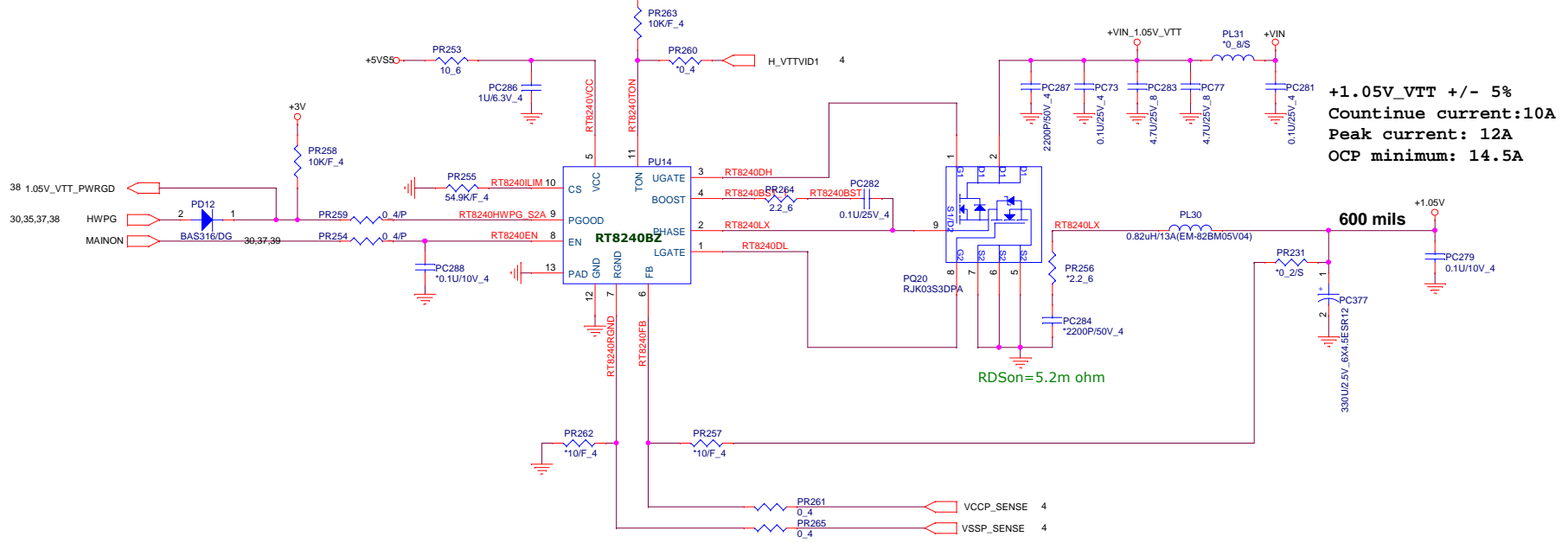
	PROJECT : R62	
	Quanta Computer Inc.	
	Size Custom	Document Number MINI PCIE CONN & G-sensor
Date: Monday, October 22, 2012 Sheet 33 of 43		




6,7,9,10,33,36,39,43
10,28,29,33,36,37,38,39,40,41,42,43

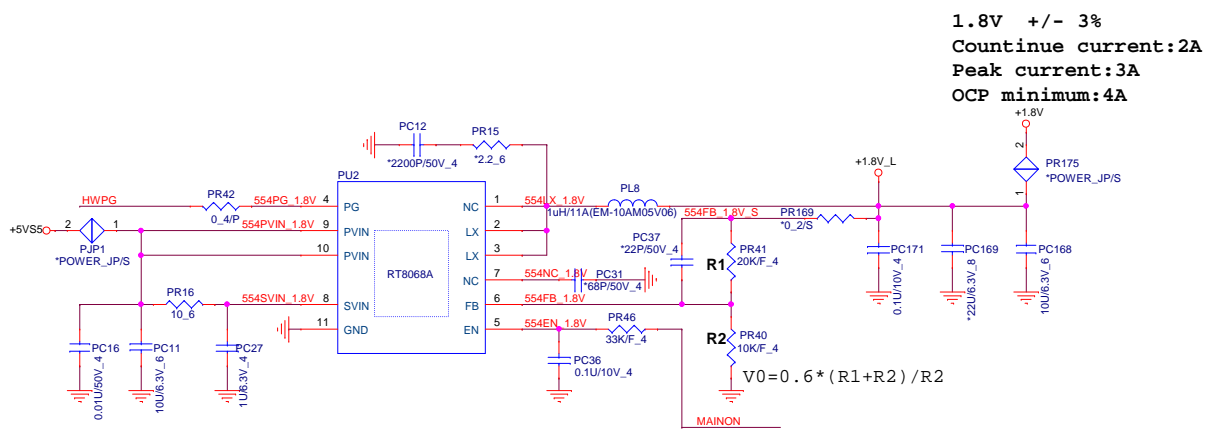
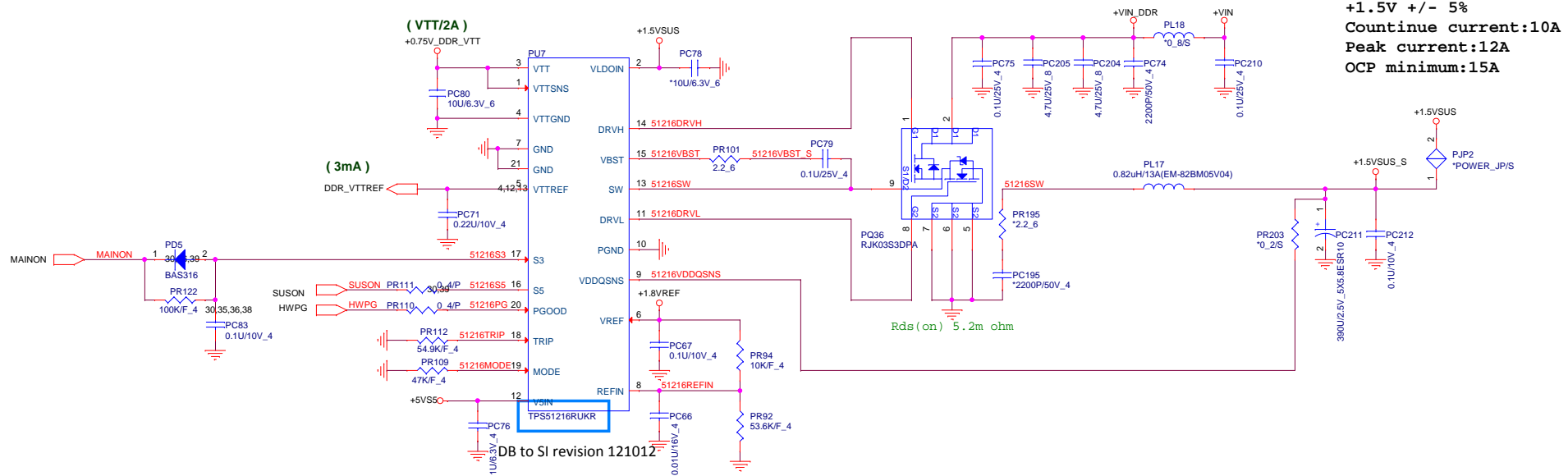


	PROJECT : R62			Rev 1A
	Quanta Computer Inc.			
	Size Custom	Document Number	3/5VPCU(RT8243A)	
Date: Monday, October 22, 2012		Sheet	35 of 43	



+1.05V 2,4,6,7,8,9,10,25,30,40

	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 1.05V(RT8228BZ)	
Sheet 36 of 43			

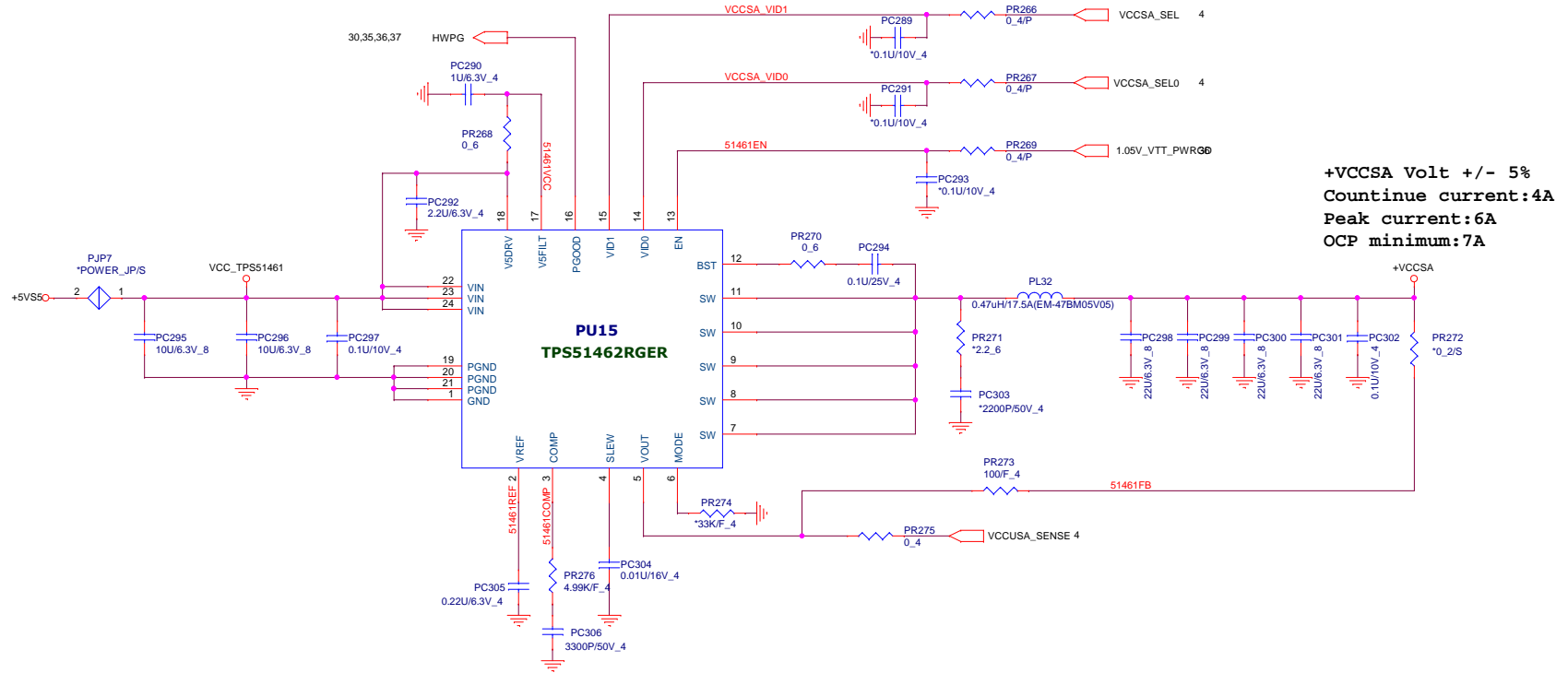


	PROJECT : R62 Quanta Computer Inc.		
	Size	Document Number	Rev
	Custom	DDR3L(APW8819)	1A
Date	Monday, October 22, 2012	Sheet	37 of 43

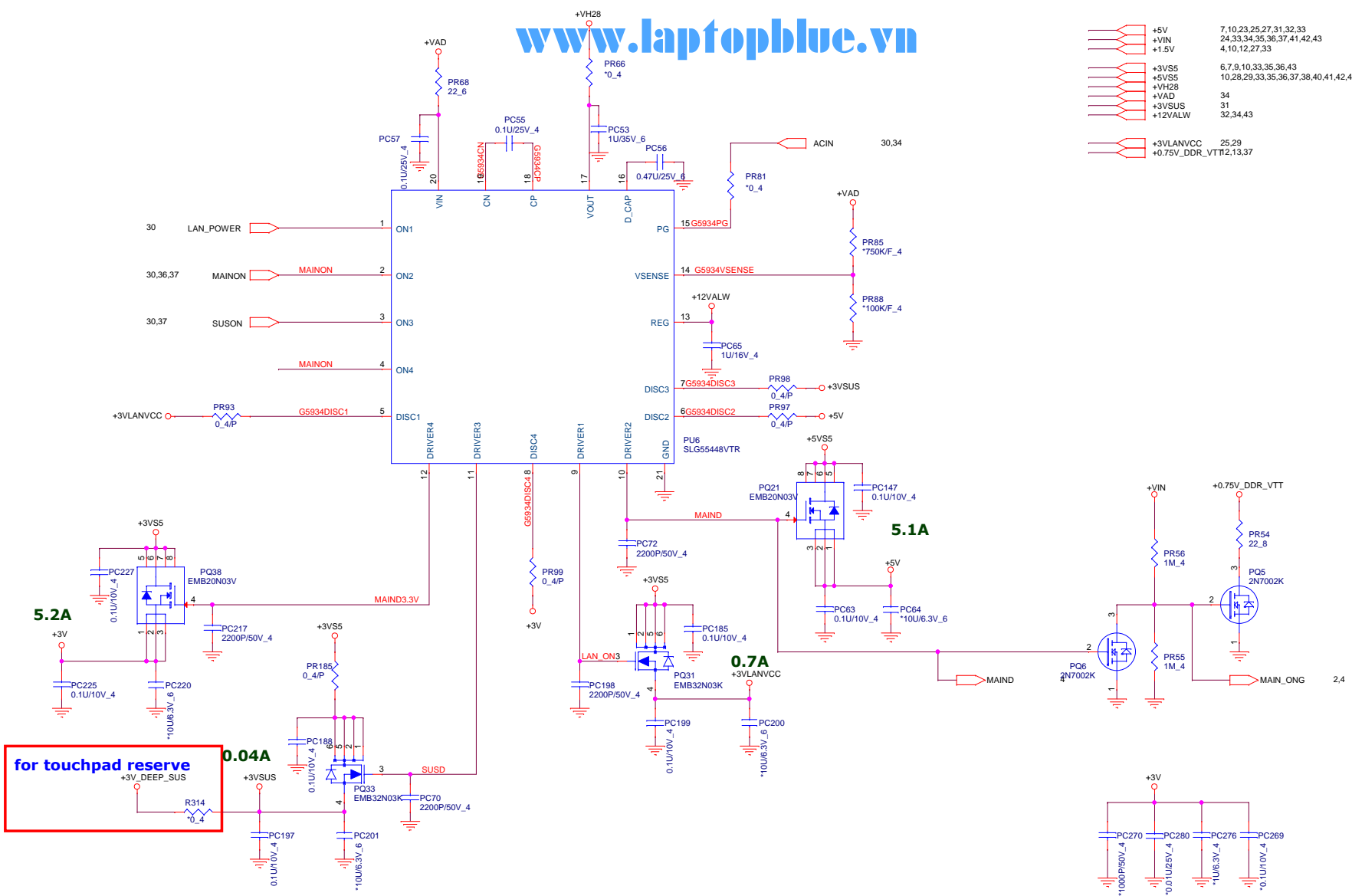
TPSS1462RGER/AL051462000


For CPU SV system agent
voltage slew rate of 0.5 -10 mV/μs

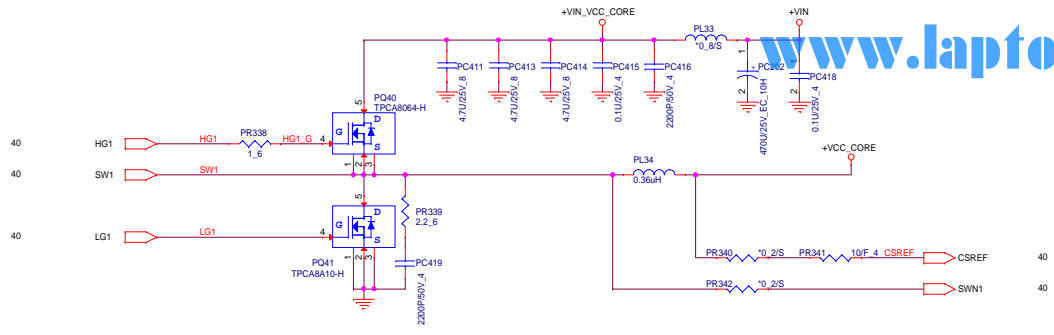
SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



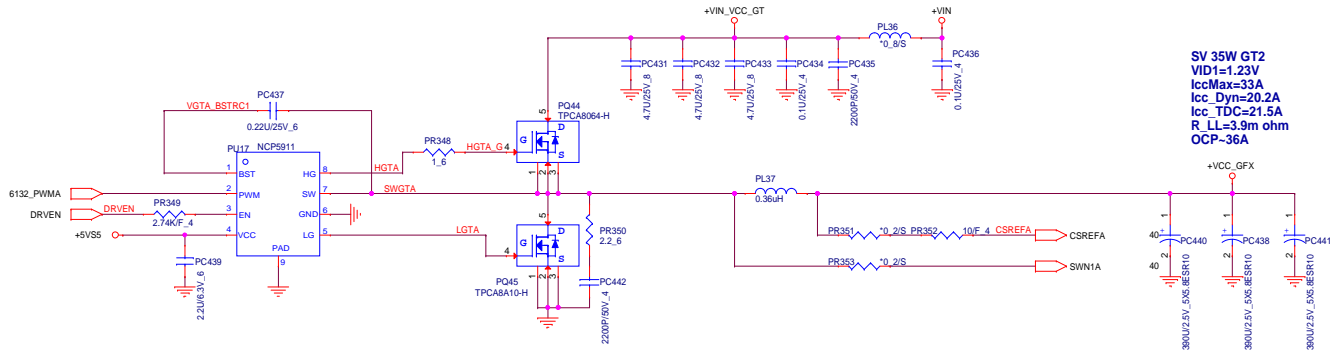
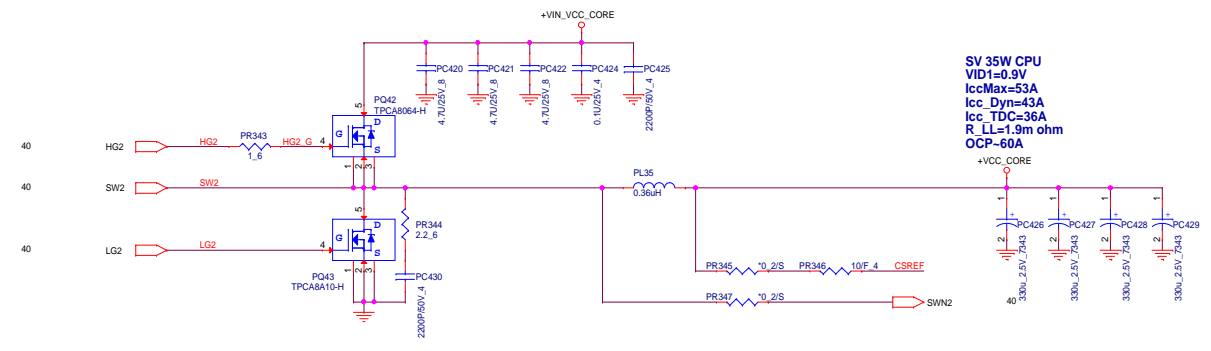
+5V	7,10,23,25,27,31,32,33
+VIN	24,33,34,35,36,37,41,42,43
+1.5V	4,10,12,27,33
+3VS5	6,7,9,10,33,35,36,43
+5VS5	10,28,29,33,35,36,37,38,40,41,42,43
+VH28	
+VAD	34
+3VSUS	31
+12VALW	32,34,43
+3VLAVCC	25,29
+0.75V_DDR_VTT2	13,37



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	Quanta Computer Inc.		
	Size Custom	Document Number Dis-charge IC (G5934)	
Date: Monday, October 22, 2012		Sheet 39 of 43	



SV 35W CPU
 VID1=0.9V
 IccMax=53A
 Icc_Dyn=43A
 Icc_TDC=36A
 R_LL=1.9m ohm
 OCP-60A



SV 35W GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm
 OCP-36A

VGA Core

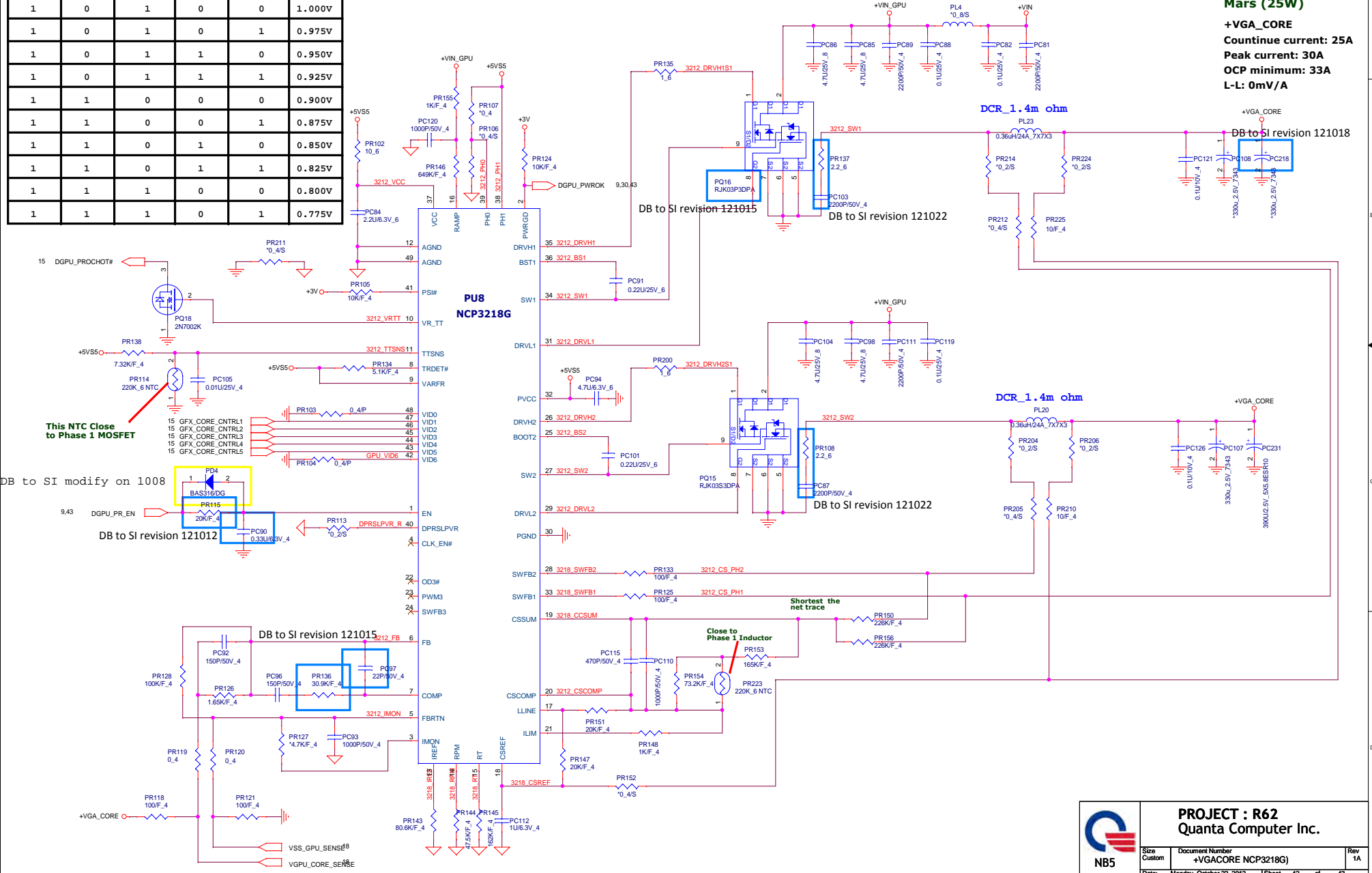
GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

Mars (25W)

+VGA_CORE
 Continune current: 25A
 Peak current: 30A
 OCP minimum: 33A
 L-L: 0mV/A



This NTC Close to Phase 1 MOSFET

DB to SI modify on 1008

DB to SI revision 121012

DB to SI revision 121015

Close to Phase 1 Inductor

Shortest the net trace

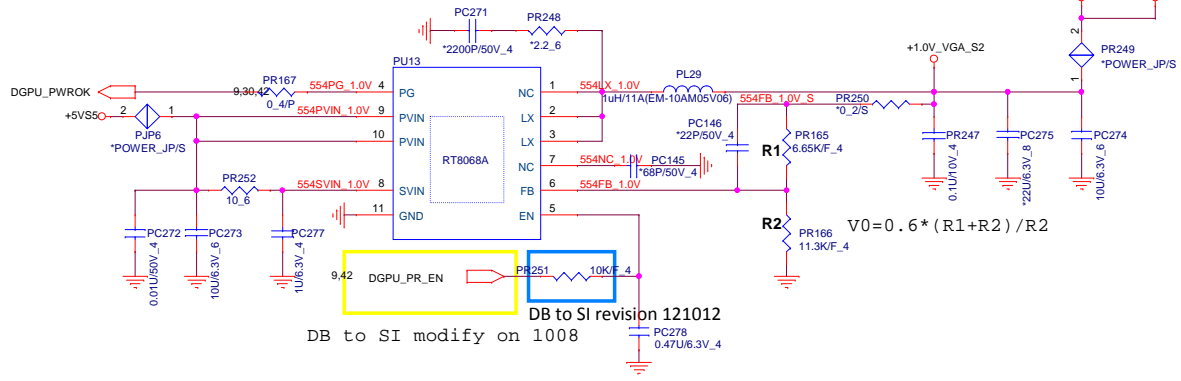


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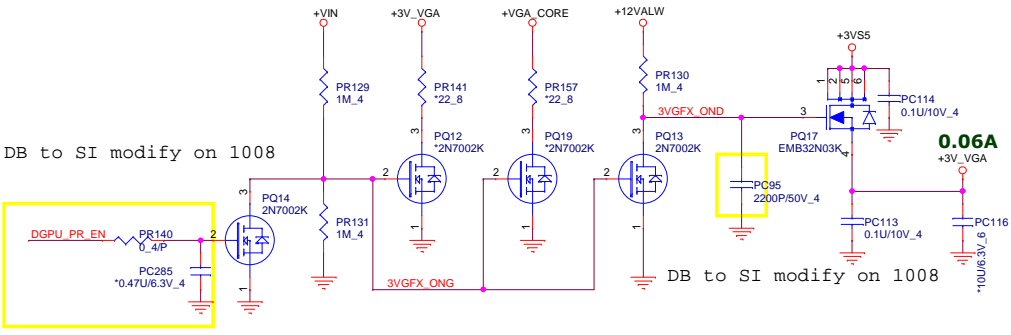
Size Custom	Document Number +VGA CORE NCP3218G)	Rev 1A
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R2 Value	P/N	1.0V_VGA
10K	CS31132FB07	1.0V
11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A

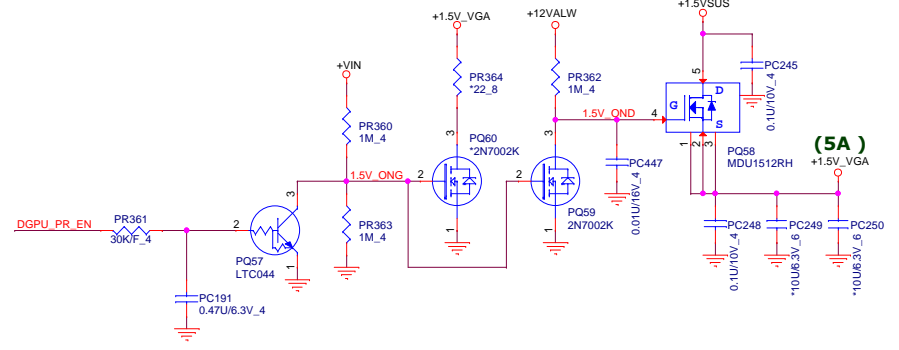


DB to SI modify on 1008

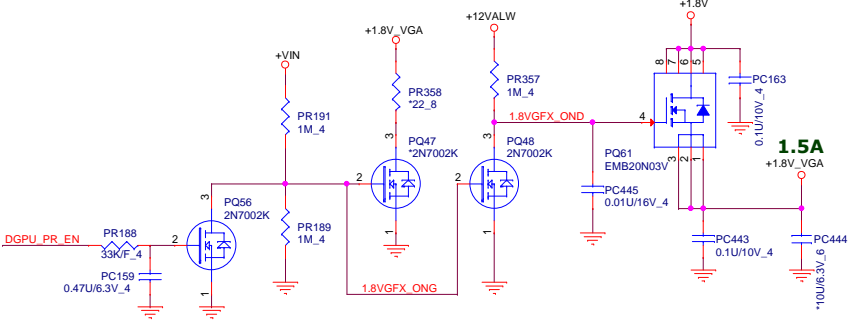


DB to SI modify on 1008

DB to SI modify on 1008



(5A)



- +1.8V_VGA 15,16,18,19,25
- +1.0V_VGA 14,16,18,19
- +3V_VGA 18

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