


Wistron Confidential

PV

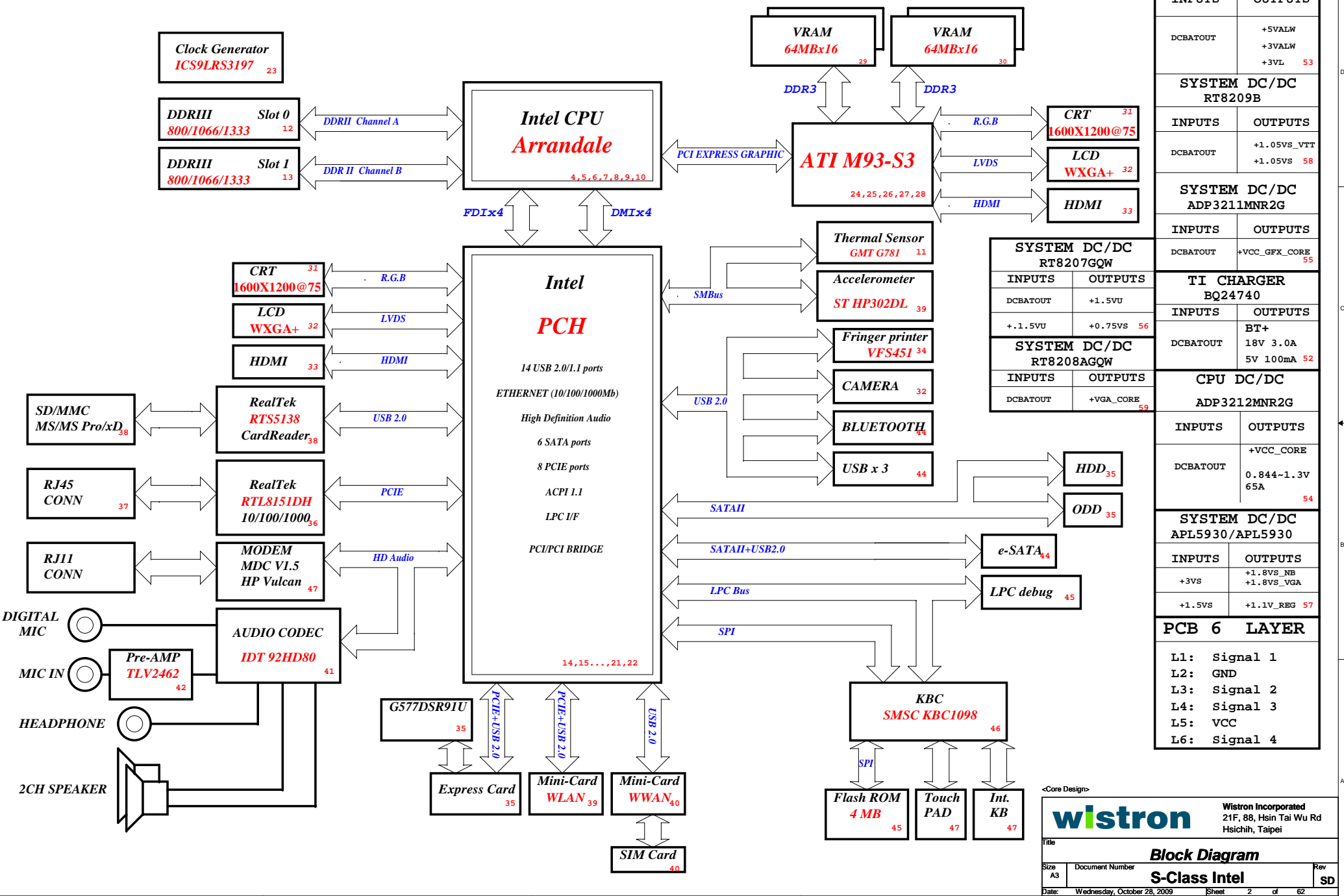
2009/10/19

REV :PV-01

<Variant Name>

		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title		S-Class Intel	
Size A3	Document Number	S-Class Intel	Rev SD
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Intel Calpella Arrandale Block Diagram



SYSTEM DC/DC RT8205A	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +3VALW +3VL 53
SYSTEM DC/DC RT8209B	
INPUTS	OUTPUTS
DCBATOUT	+1.05VS_VTT +1.05VS 58
SYSTEM DC/DC ADP3211MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_GFX_CORE 55
SYSTEM DC/DC RT8207GQW	
INPUTS	OUTPUTS
DCBATOUT	+1.5VU
+1.5VU	+0.75VS 56
SYSTEM DC/DC RT8208AGQW	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 59
TI CHARGER BQ24740	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA 52
CPU DC/DC ADP3212MNR2G	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 0.844~1.3V 65A 54
SYSTEM DC/DC APL5930/APL5930	
INPUTS	OUTPUTS
+3VS	+1.8VS_NB +1.8VS_VGA
+1.5VS	+1.1V_REG 57
PCB 6 LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

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Title	Block Diagram		Rev
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SD

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarkfield samples.	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

090901-1

SMBUS Control Table

	SOURCE	BATT	THERMAL SENSOR	CLK GEN	SODIMM	G-SENSOR	SMSC1098	M93
AB1A_DATA AB1A_CLK	SMSC1098	V	X	X	X	X	X	X
SML1CLK SML1DATA	Calpella	X	X	X	X	X	V	V
PCH_SMB_DATA PCH_SMB_CLK	Calpella	X	V	V	V	V	X	X

PCIE Routing page 15


LANE2	EXP
LANE4	WLAN
LANE6	LAN

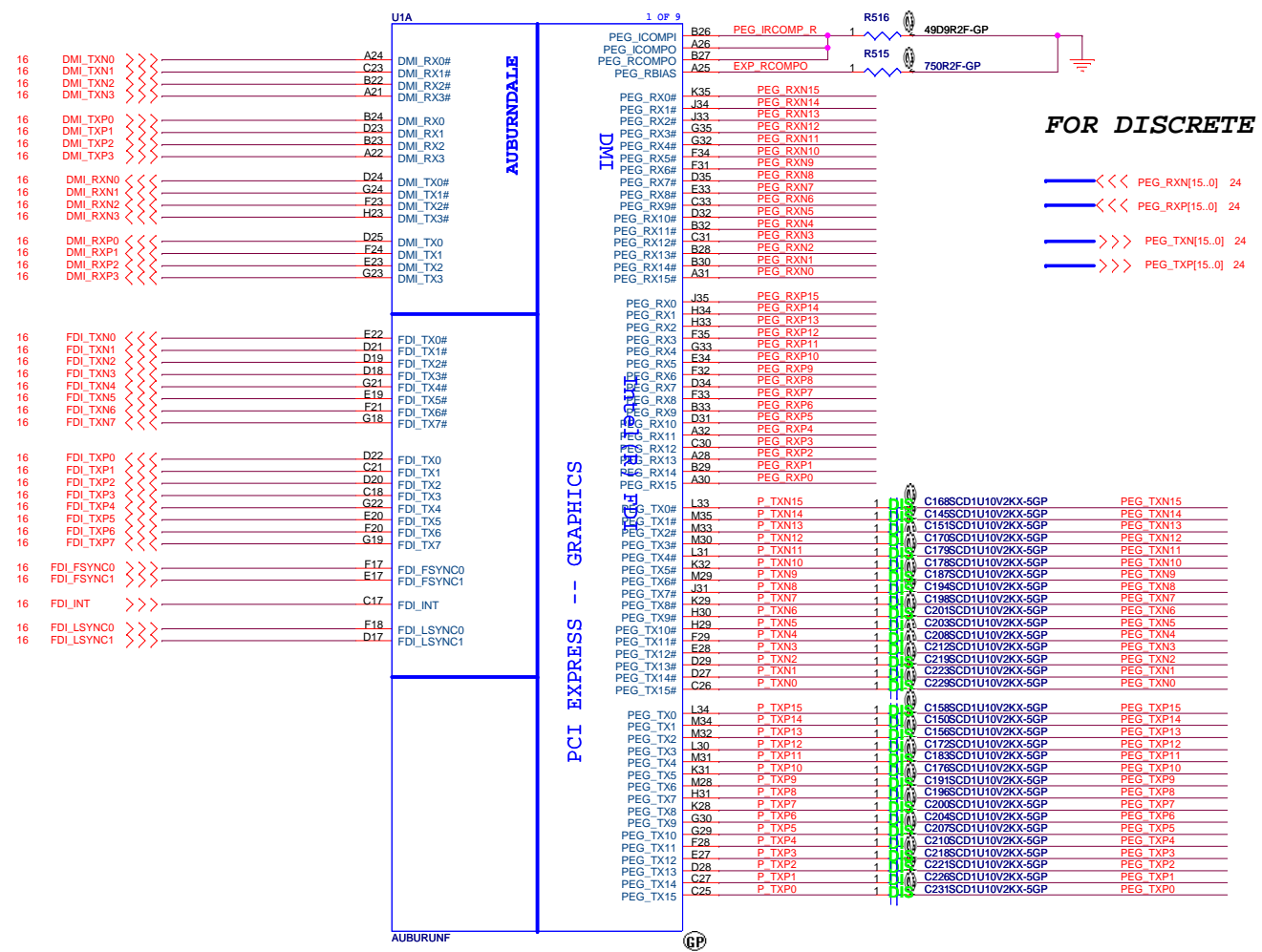
USB Table page 18

Pair	Device
0	External USB2
1	USB1 (Debug port)
2	ESATA USB4
3	Card Reader
4	NEW CARD
5	FREE
6	WLAN
7	FREE
8	BLUETOOTH
9	WWAN
10	Fingerprint
11	External USB3
12	CAMERA
13	FREE

0901019-1

<Core Design>

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Title		
Notes List		
Size	Document Number	Rev
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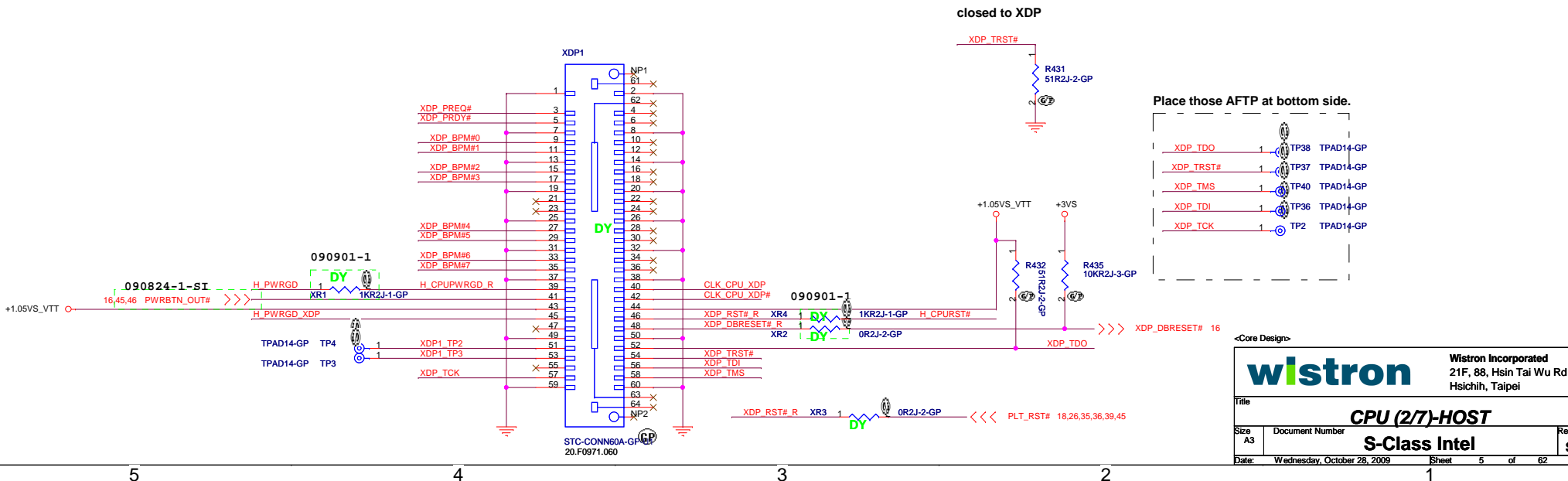
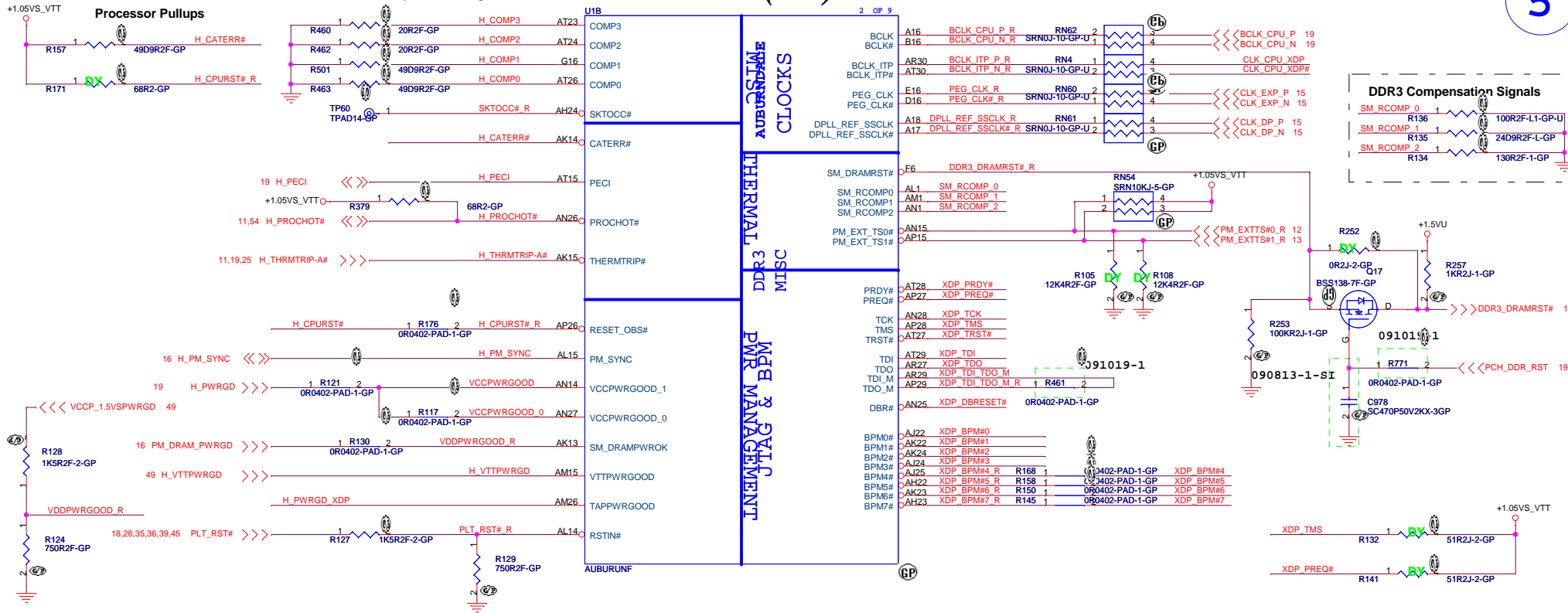
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Title: **CPU (1/7)-PEG / DMI / FDI**

Size: A3 Document Number: **S-Class Intel** Rev: **SD**

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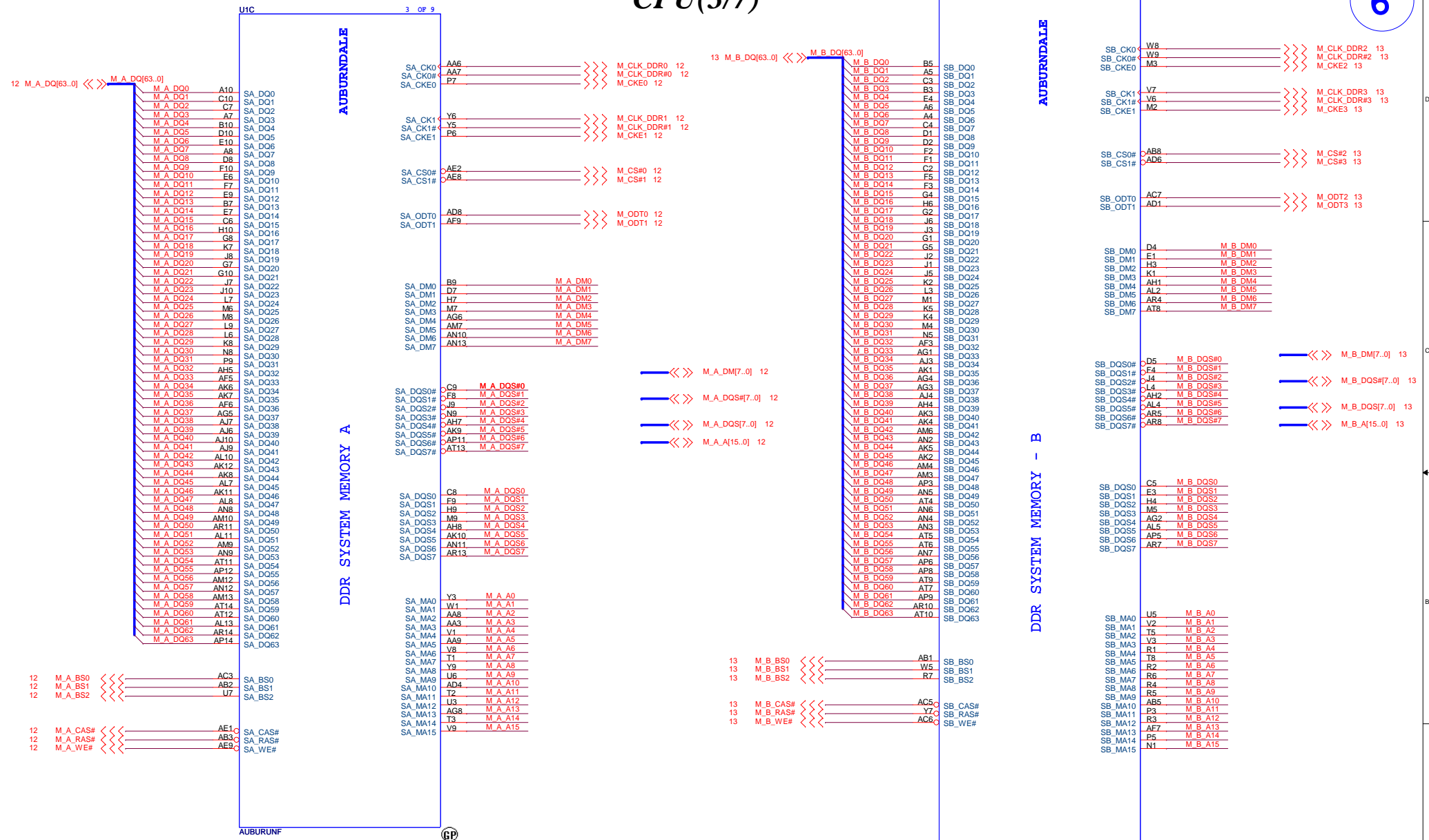


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Title: **CPU (2/7)-HOST**

Size A3 Document Number **S-Class Intel** Rev SD

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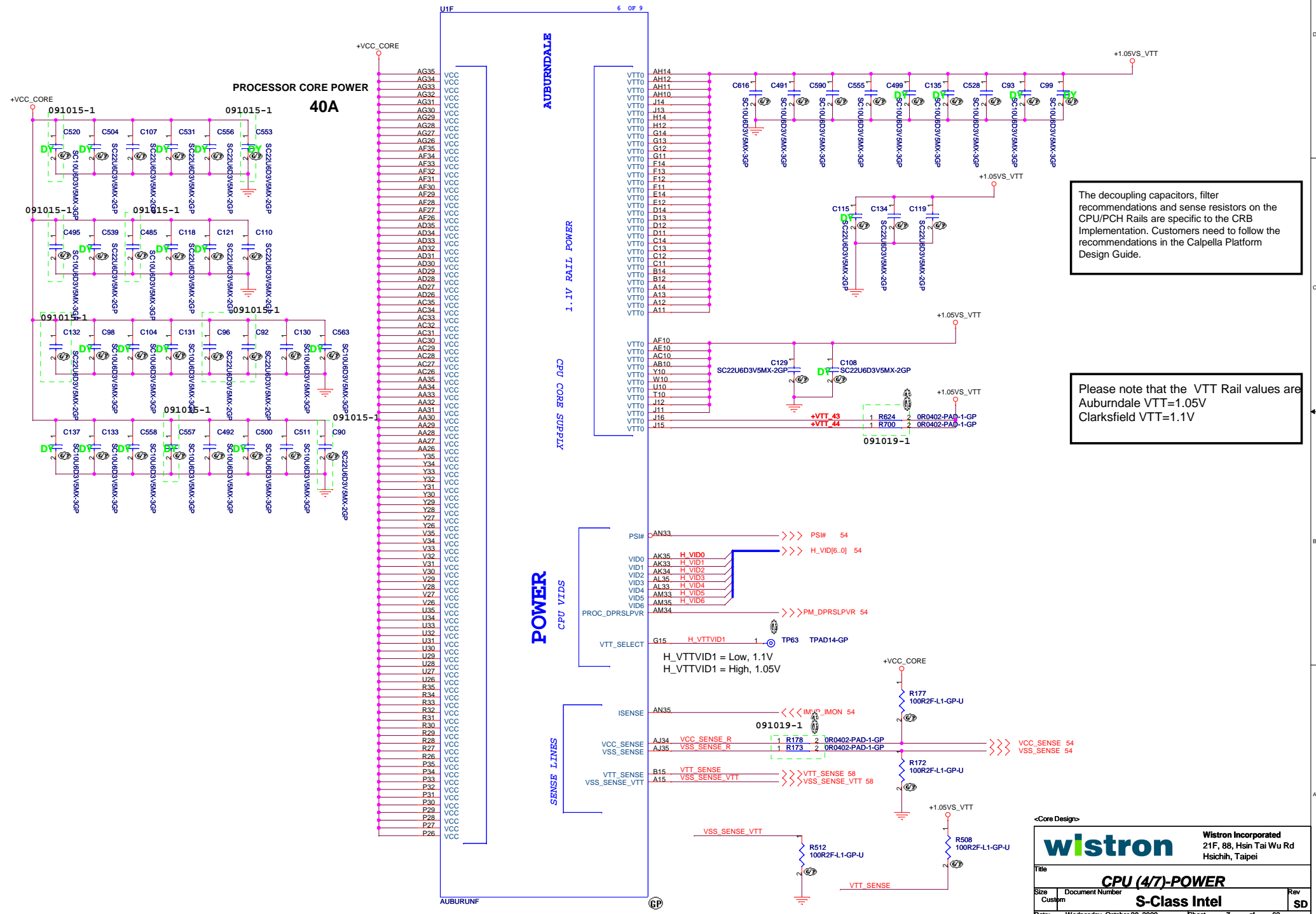


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Title: **CPU (3/7)-MEM INTERFACE**

Size: A3 Document Number: **S-Class Intel** Rev: SD

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The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail values are Auburndale VTT=1.05V Clarksfield VTT=1.1V

<Core Design>

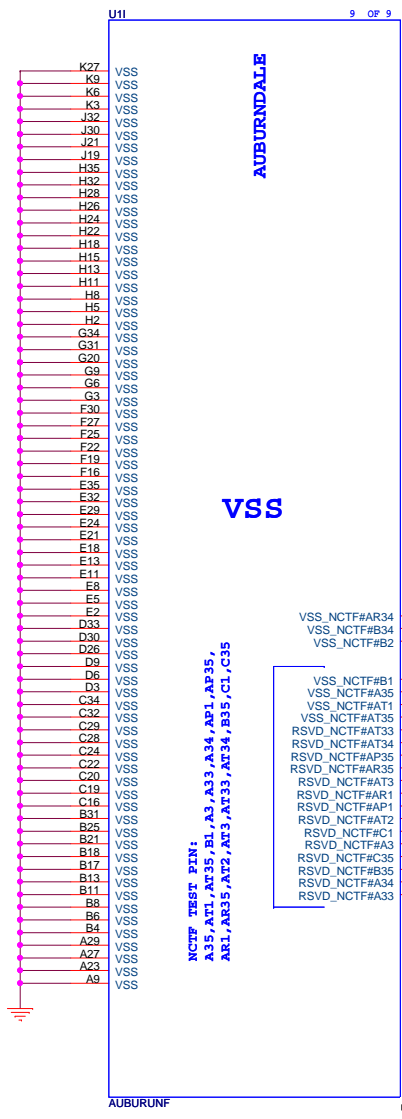
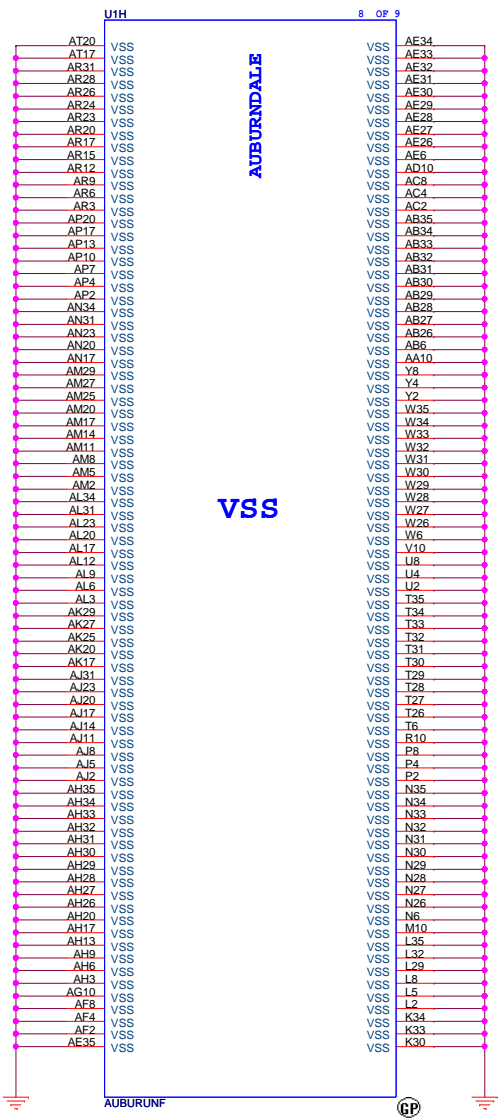
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Title: **CPU (4/7)-POWER**

Size: Custom	Document Number: S-Class Intel	Rev: SD
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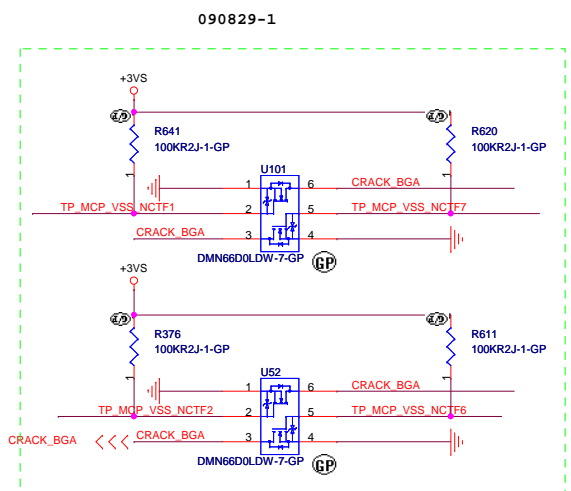
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CPU(6/7)



All NCTF pins should be Test Points and should be routed as trace.

- VSS_NCTF#AR34
- VSS_NCTF#B34
- VSS_NCTF#B2
- VSS_NCTF#B1
- VSS_NCTF#A35
- VSS_NCTF#A1
- VSS_NCTF#AT35
- RSVD_NCTF#AT33
- RSVD_NCTF#AT34
- RSVD_NCTF#AP35
- RSVD_NCTF#AR35
- RSVD_NCTF#AT3
- RSVD_NCTF#AR1
- RSVD_NCTF#AP1
- RSVD_NCTF#AT2
- RSVD_NCTF#C1
- RSVD_NCTF#A3
- RSVD_NCTF#C35
- RSVD_NCTF#B35
- RSVD_NCTF#A34
- RSVD_NCTF#A33



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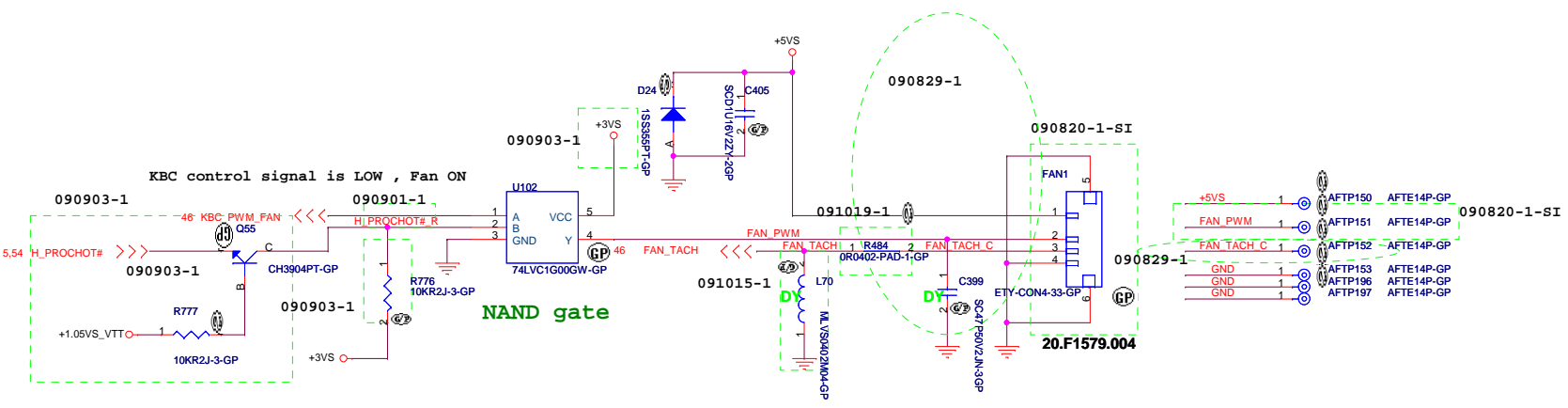
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Title **CPU (6/7)-VSS**

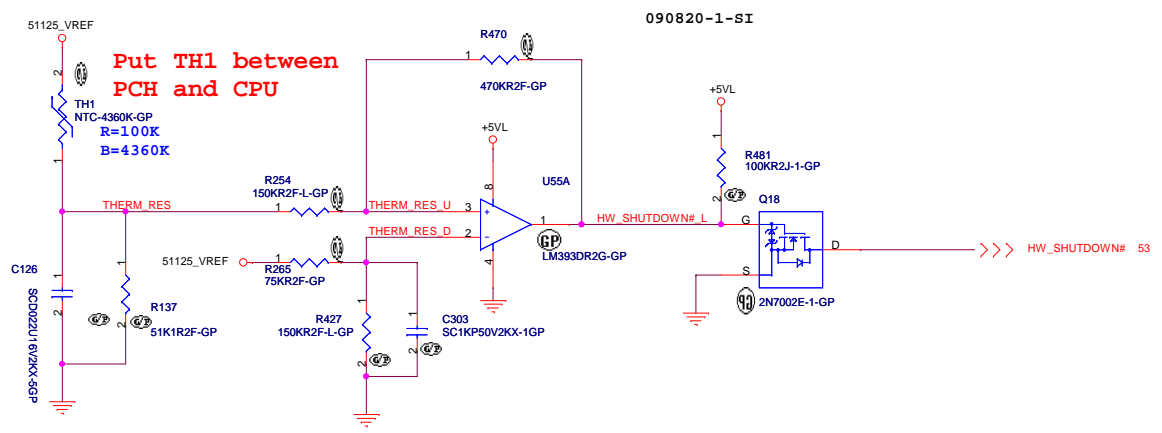
Size A3 Document Number **S-Class Intel** Rev SD

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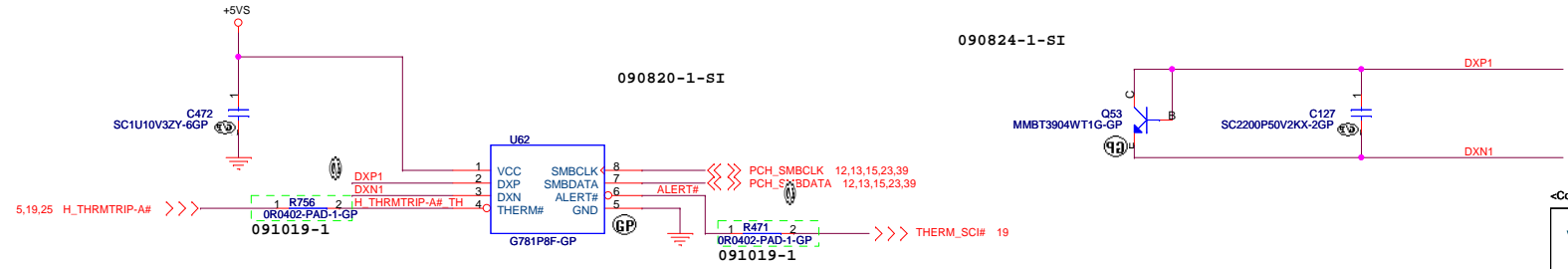
4 WIRE PWM Fan Control circuit



T8 H/W Shutdown Control circuit



Thermal IC Control circuit



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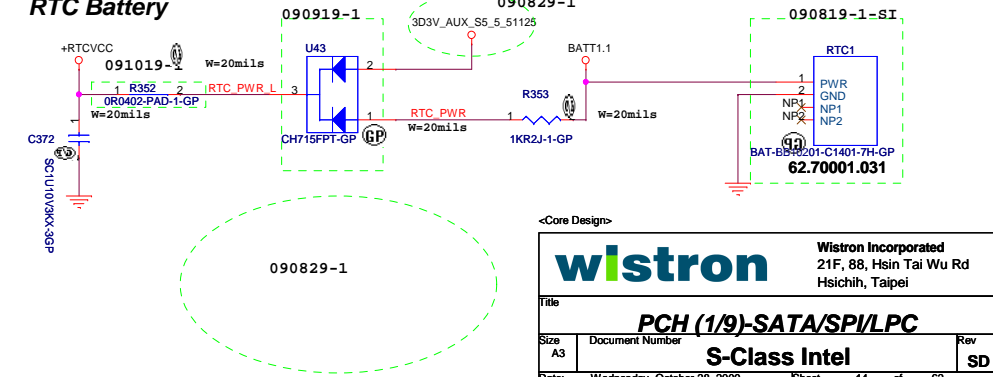
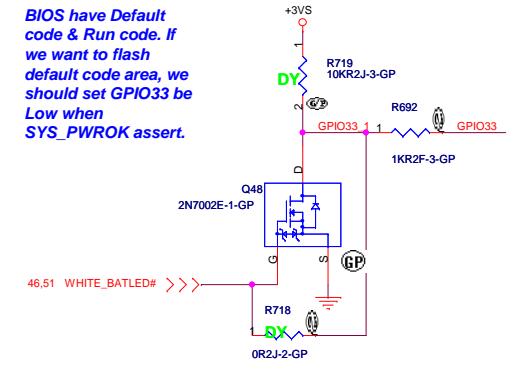
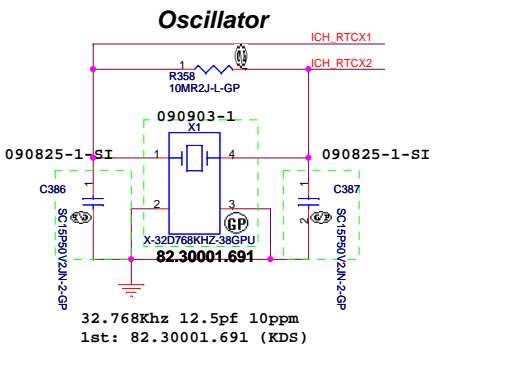
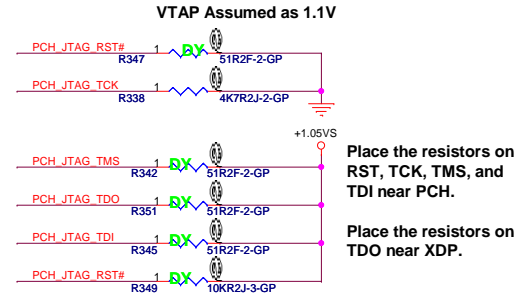
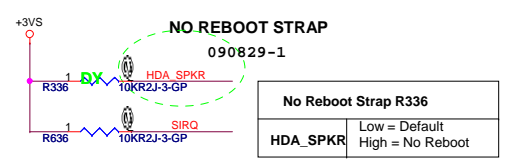
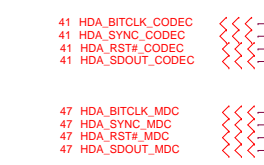
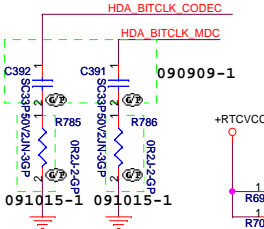
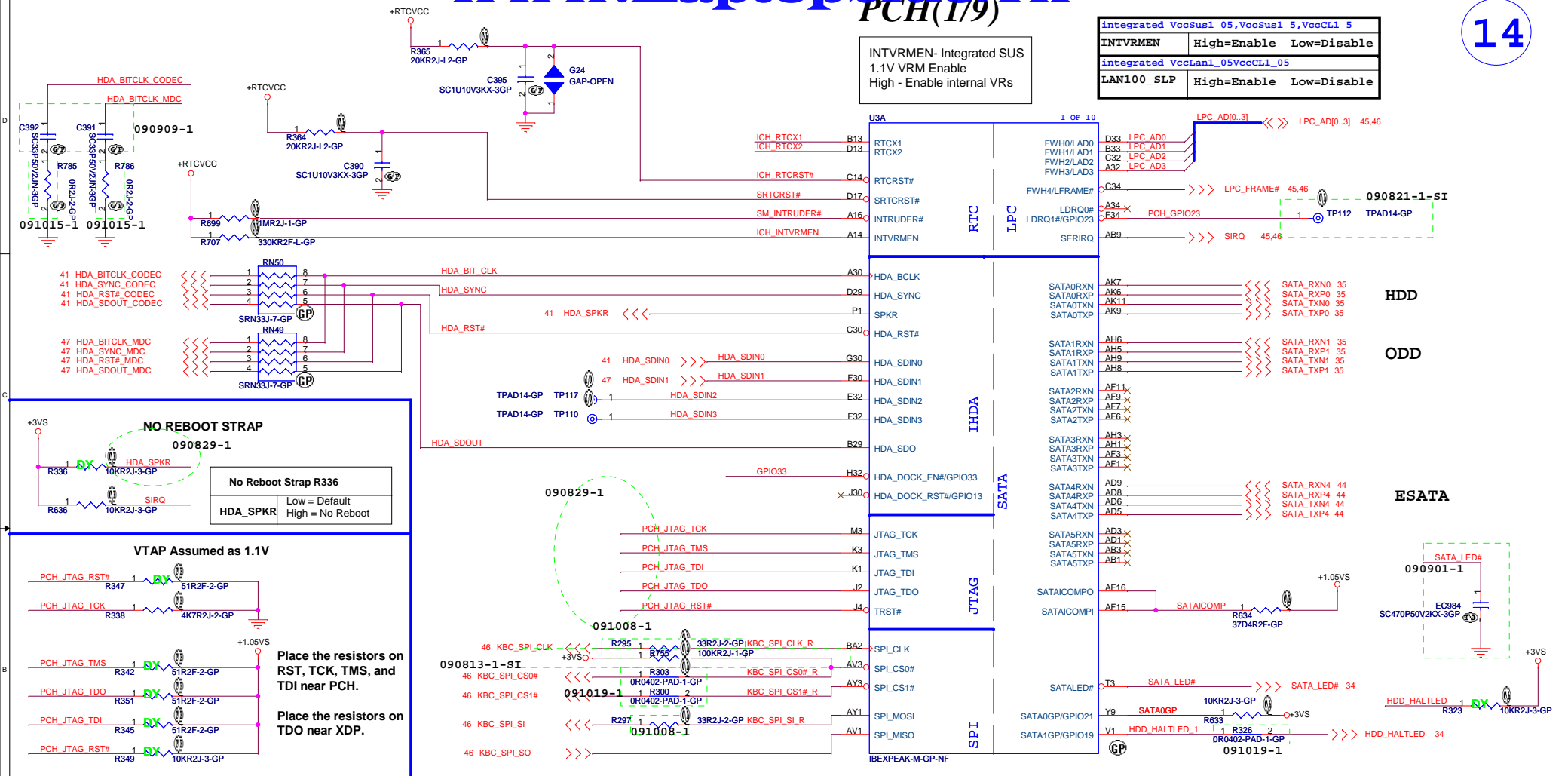
Title: **G787S11U-GP THERMAL**

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integrated VccSusi_05,VccSusi_5,VccCLL_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCLL_05		
LAN100_SLP	High=Enable	Low=Disable

INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable internal VRs

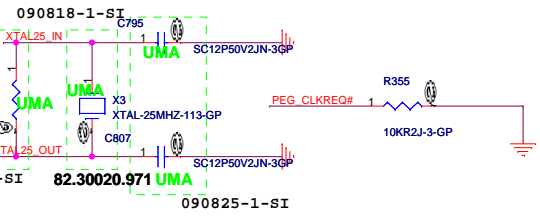
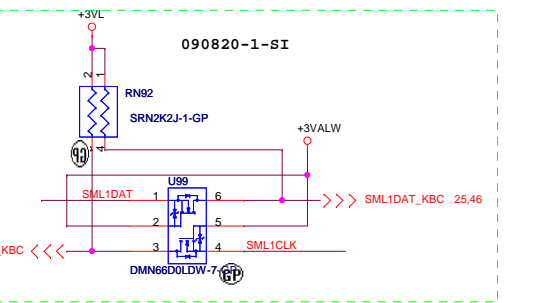
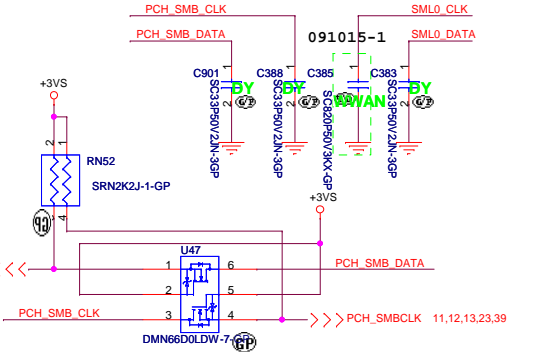
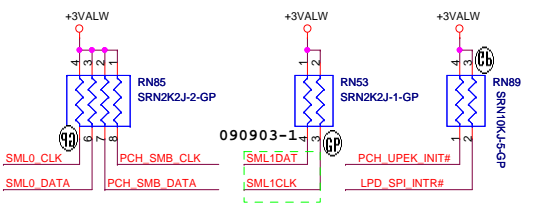
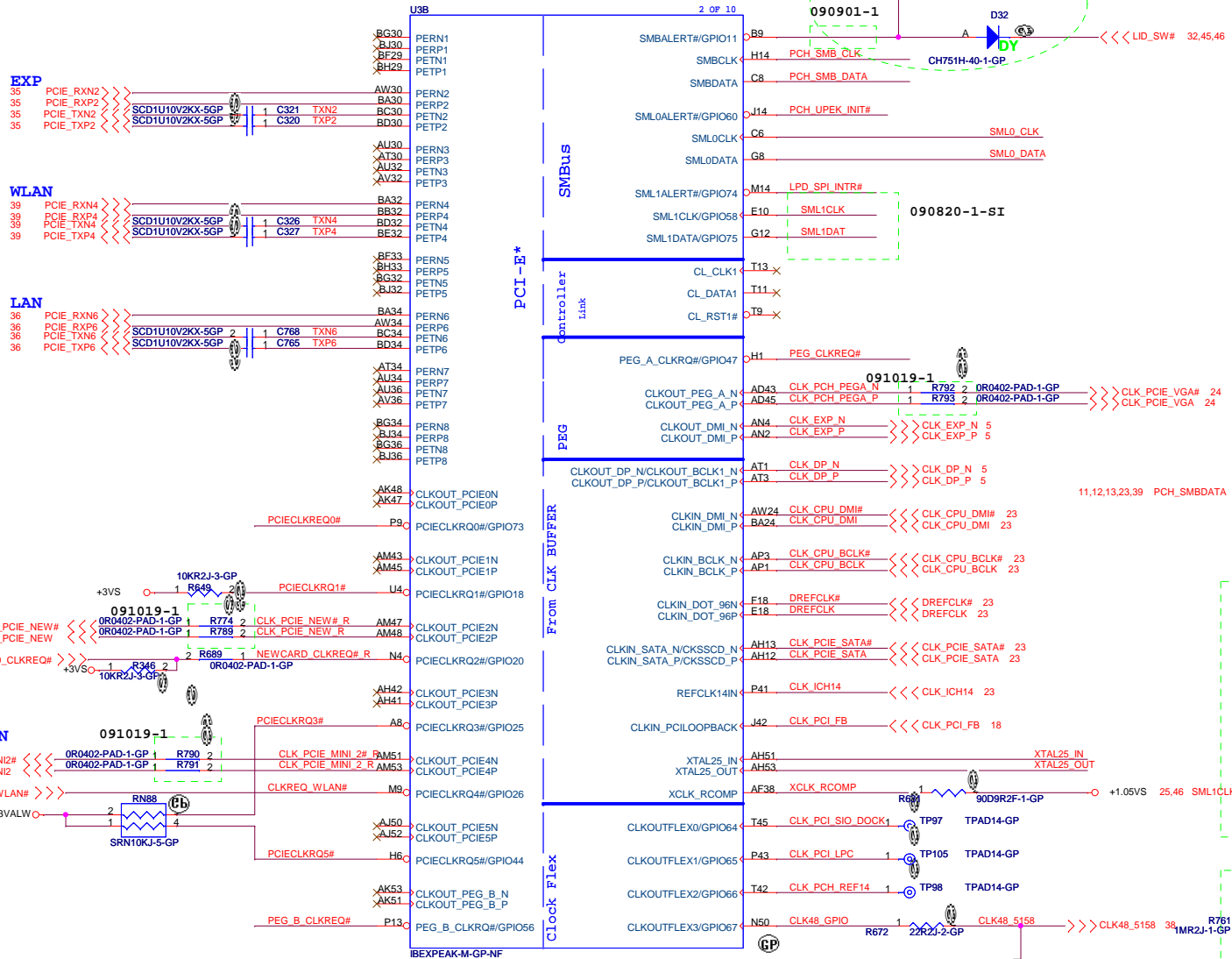


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Title: **PCH (1/9)-SATA/SPI/LPC**

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PCIECLKRQ(0,3,4,5,6,7)# should have a 10K pull-up to +3VALW.
PCIECLKRQ(1,2) should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

CLKOUTFLEX3/GPIO67:
Configurable as an programmable output clock 48MHz output to SIO.

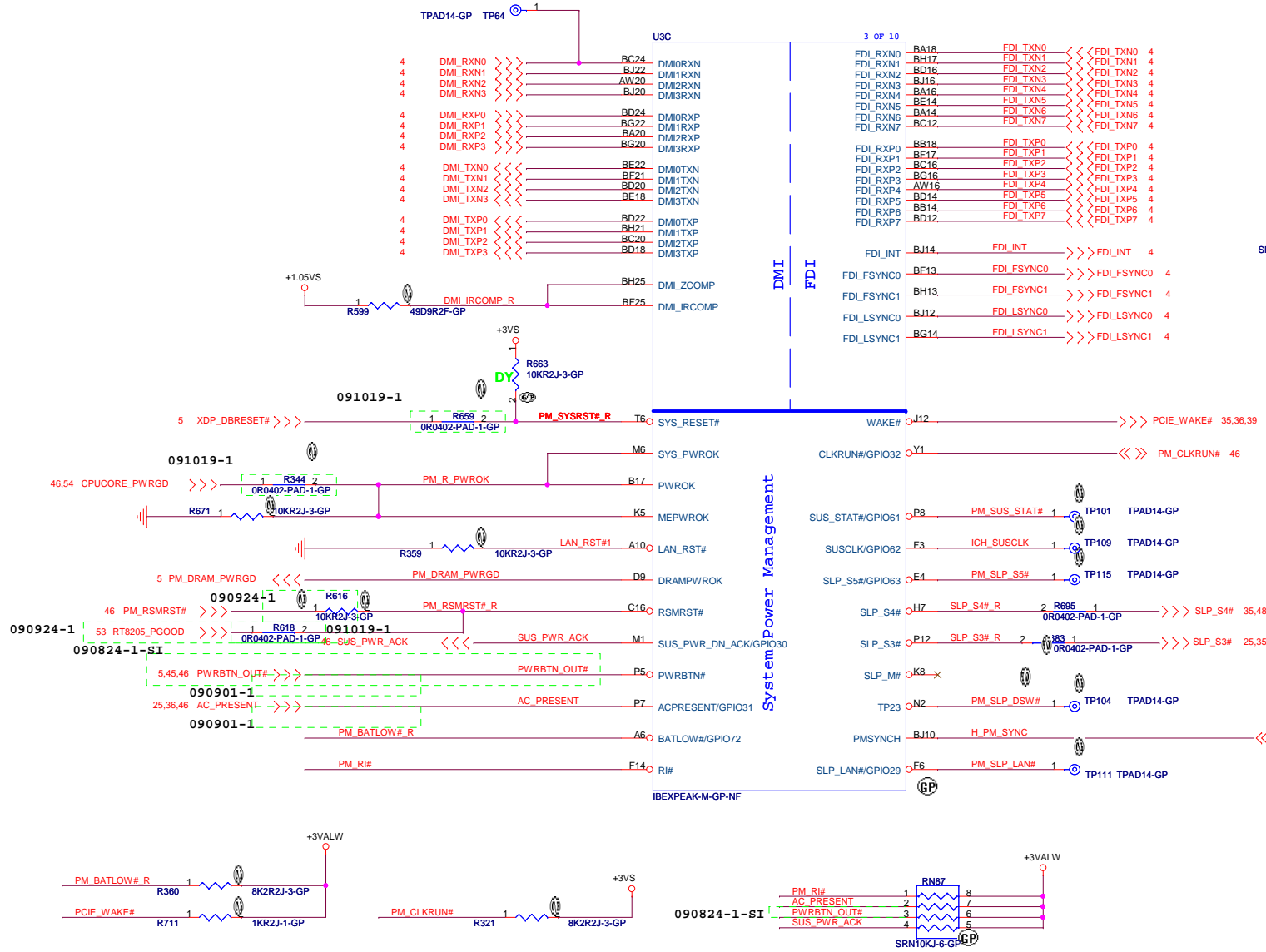
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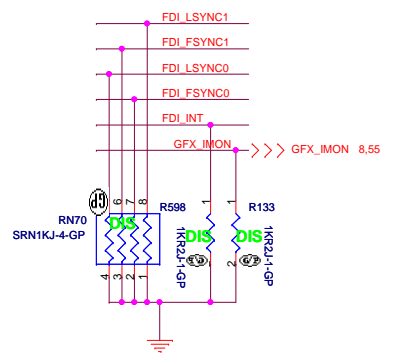
Title: **PCH (2/9)-PCIE/SMBUS**

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Layout Note:
Place these near PCH.

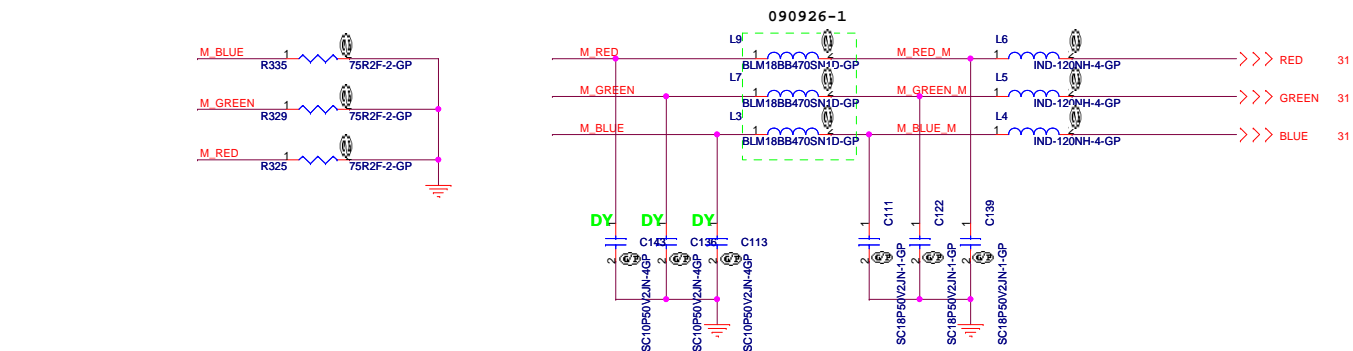
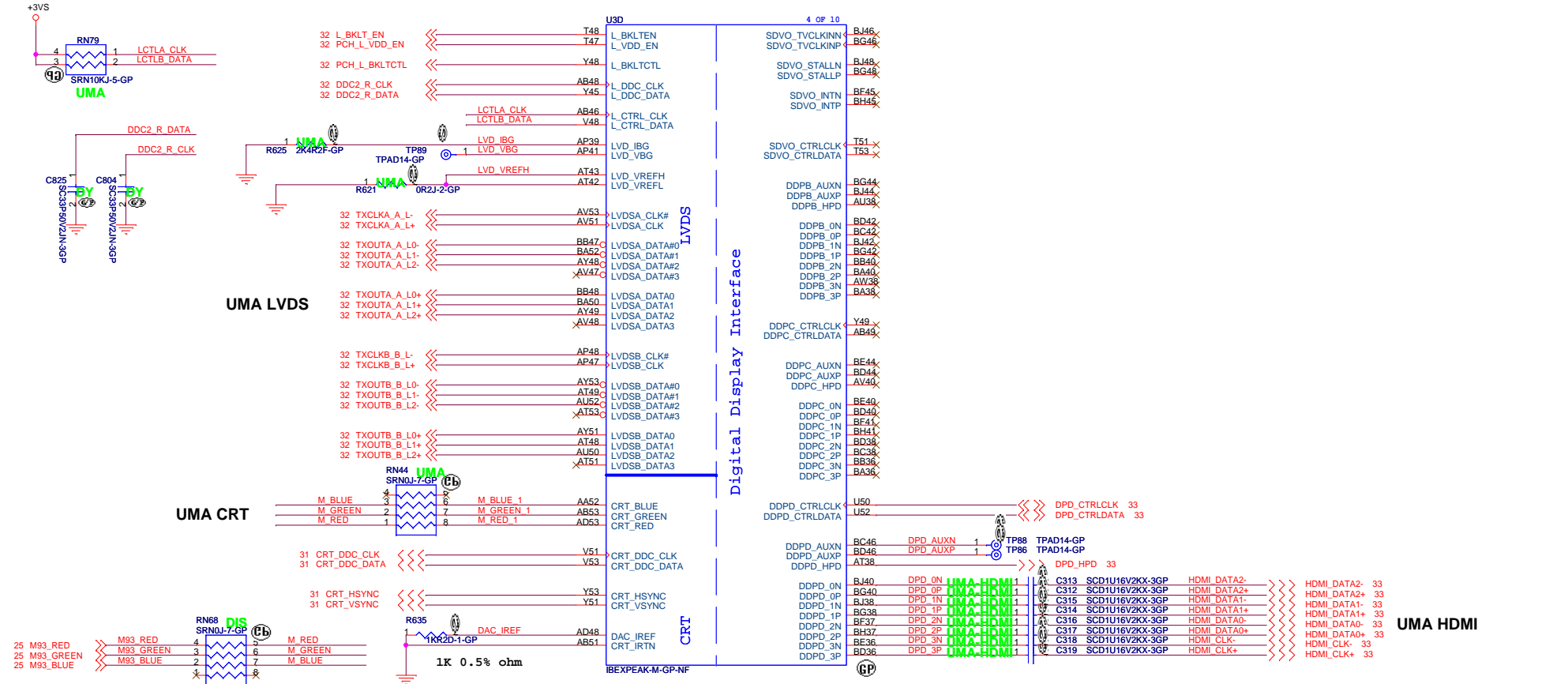


System Power Management

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Title PCH (3/9)-DMI/SYS PWR			
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PCH(4/9)



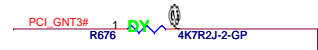
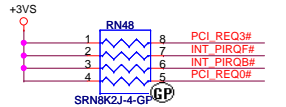
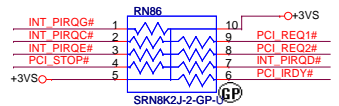
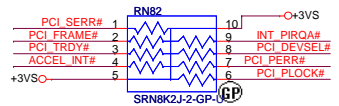
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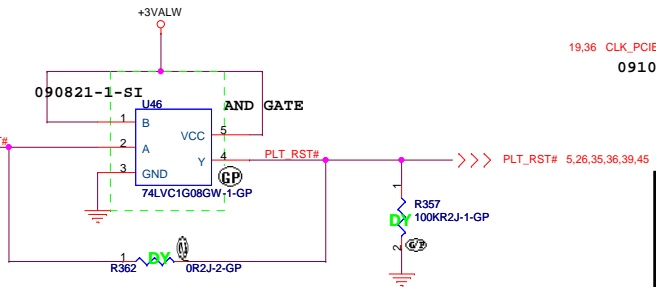
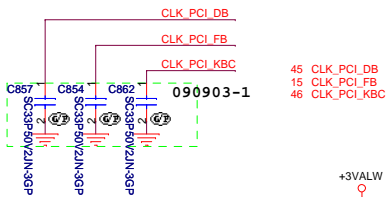
Title: **PCH (4/9)-LVDS/CRT**

Size: A3 Document Number: **S-Class Intel** Rev: SD

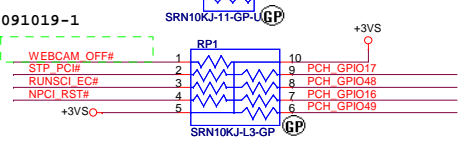
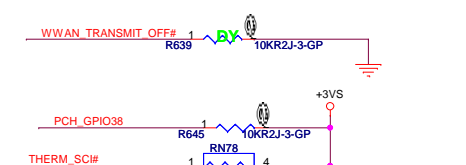
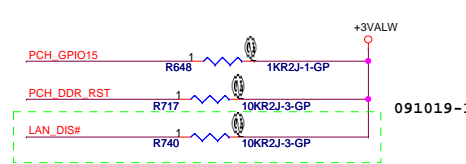
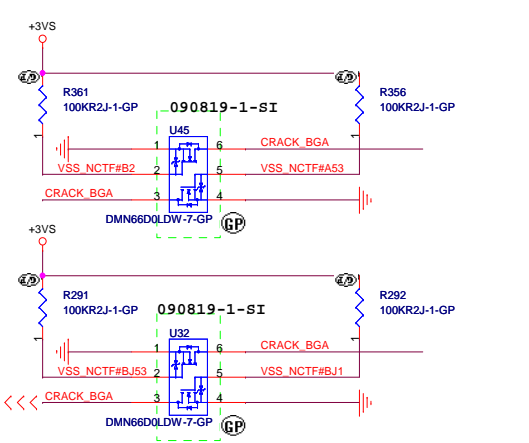
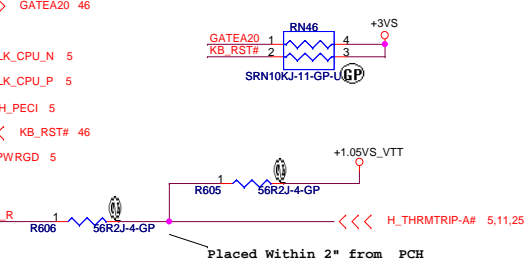
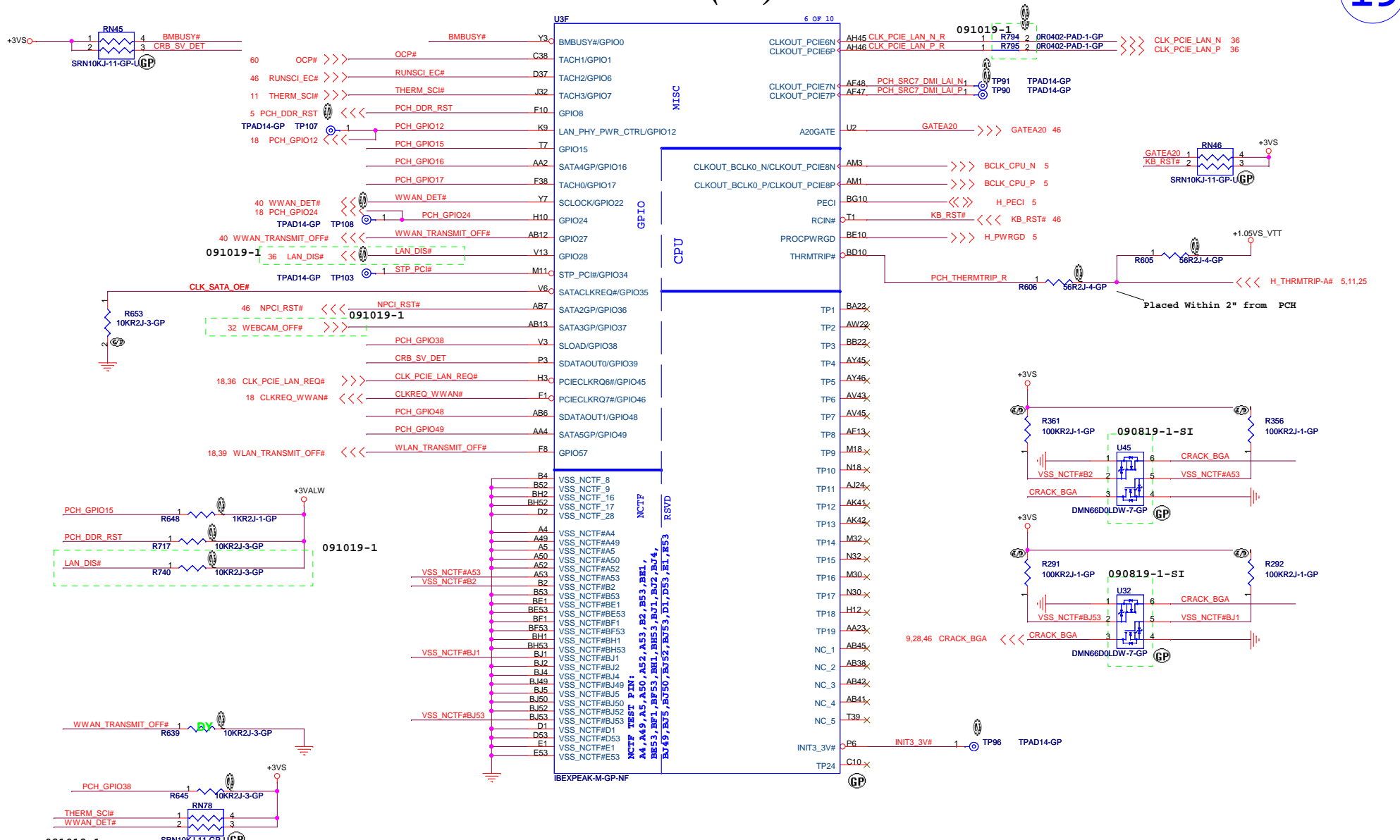
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BOOT BIOS Strap table with columns for PCI_GNT#0, PCI_GNT#1, and BOOT BIOS Location. Row 1 (1, 1) is highlighted in red and labeled SPI.



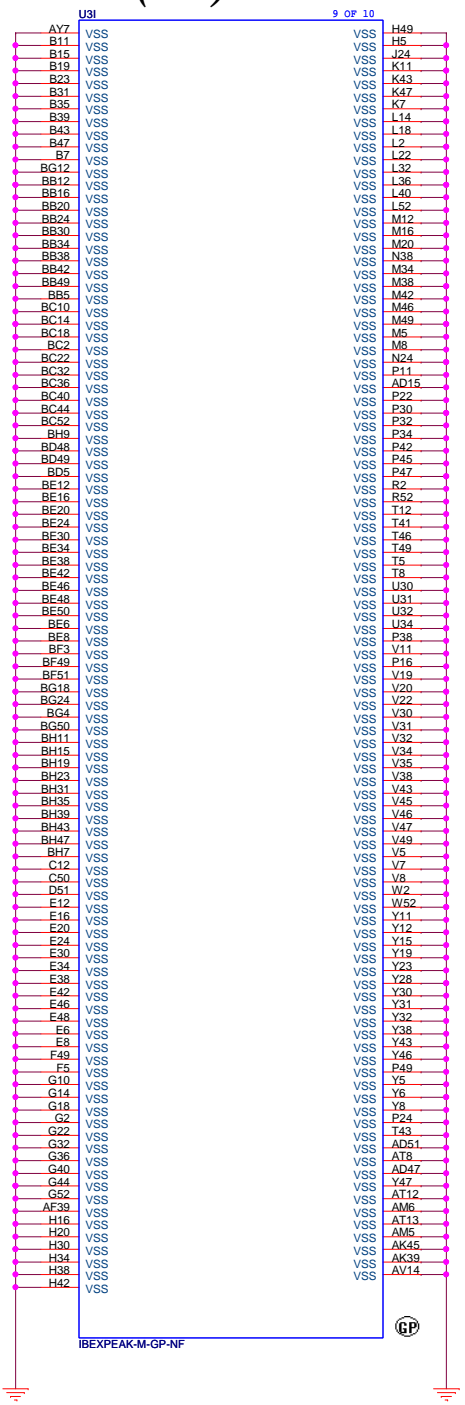
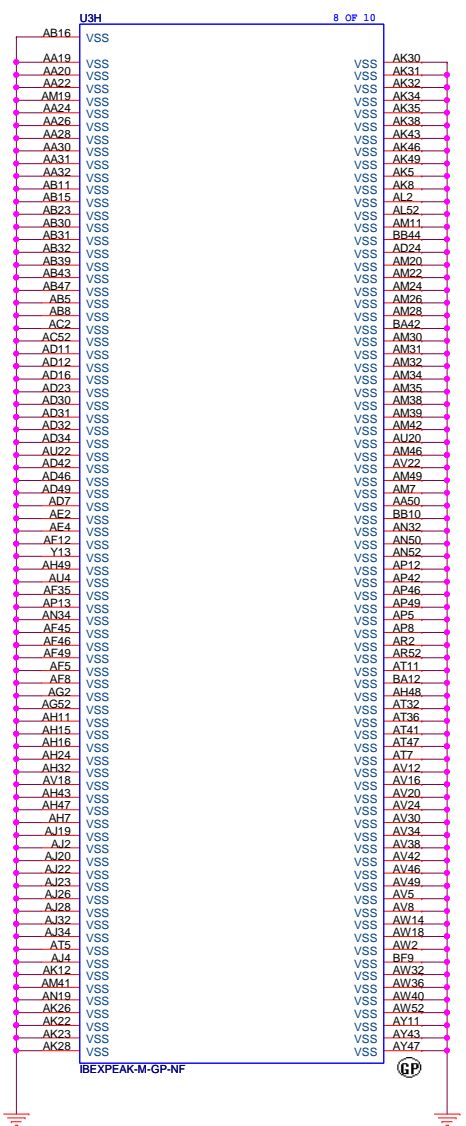
Pin header table listing connections for H40-H48, H49-H53, H54-H58, H59-H63, H64-H68, H69-H73, H74-H78, H79-H83, H84-H88, H89-H93, H94-H98, H99-H103, H104-H108, H109-H113, H114-H118, H119-H123, H124-H128, H129-H133, H134-H138, H139-H143, H144-H148, H149-H153, H154-H158, H159-H163, H164-H168, H169-H173, H174-H178, H179-H183, H184-H188, H189-H193, H194-H198, H199-H203, H204-H208, H209-H213, H214-H218, H219-H223, H224-H228, H229-H233, H234-H238, H239-H243, H244-H248, H249-H253, H254-H258, H259-H263, H264-H268, H269-H273, H274-H278, H279-H283, H284-H288, H289-H293, H294-H298, H299-H303, H304-H308, H309-H313, H314-H318, H319-H323, H324-H328, H329-H333, H334-H338, H339-H343, H344-H348, H349-H353, H354-H358, H359-H363, H364-H368, H369-H373, H374-H378, H379-H383, H384-H388, H389-H393, H394-H398, H399-H403, H404-H408, H409-H413, H414-H418, H419-H423, H424-H428, H429-H433, H434-H438, H439-H443, H444-H448, H449-H453, H454-H458, H459-H463, H464-H468, H469-H473, H474-H478, H479-H483, H484-H488, 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H5569-H5573, H5574-H5578



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Title	PCH (6/9)-GPIO		
Size	Document Number	S-Class Intel	
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Date:	Wednesday, October 28, 2009	Sheet	19 of 62



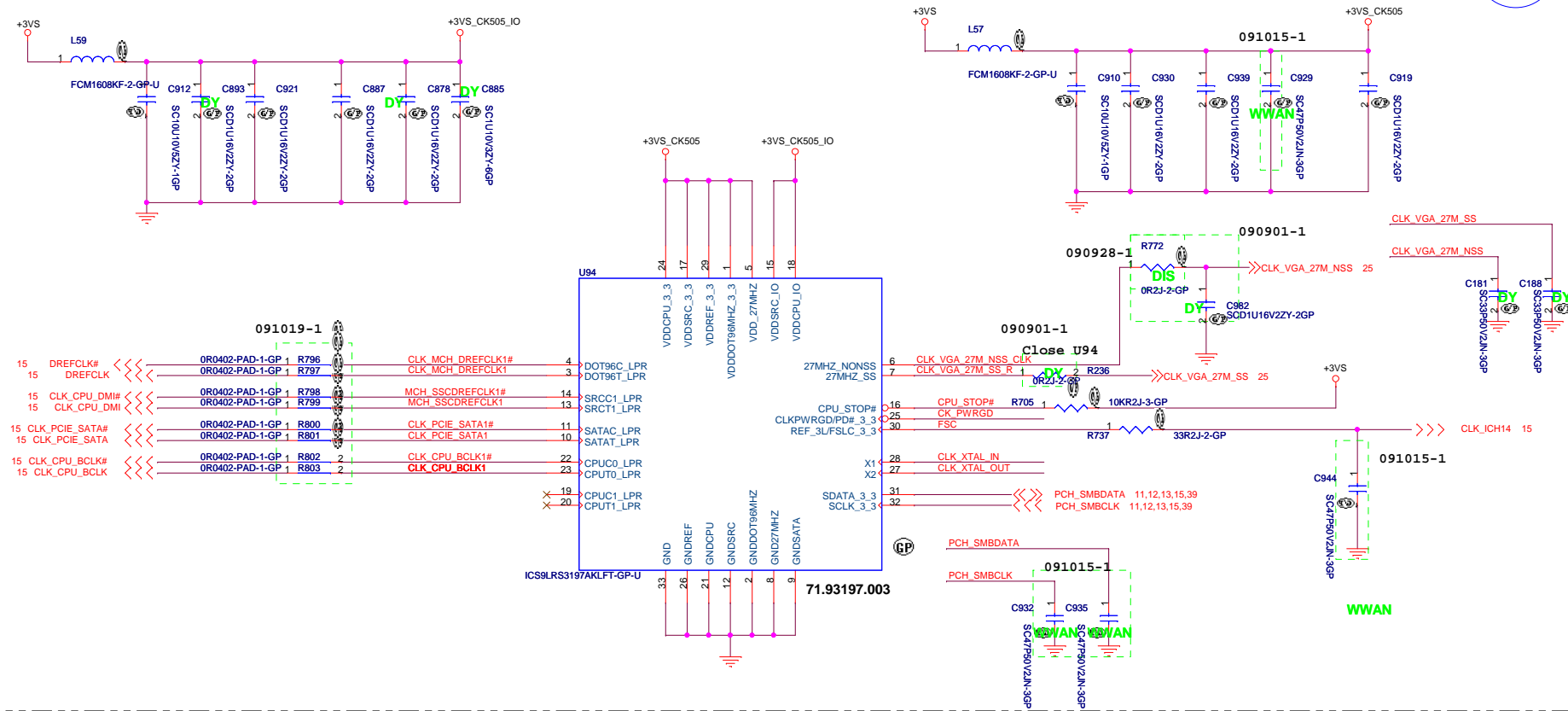
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Hsichih, Taipei

Title: **PCH (9/9)-VSS**

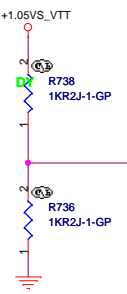
Size: A3 Document Number: **S-Class Intel** Rev: **SD**

Date: Wednesday, October 28, 2009 Sheet 22 of 62

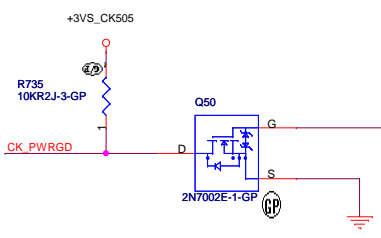


FSB Frequency Select

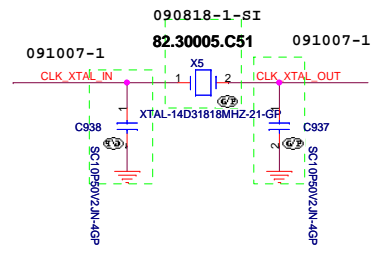
FSC	0	1
SPEED	133MHz (Default)	100MHz



Clock Gen. Eable



Clock Gen. Crystal



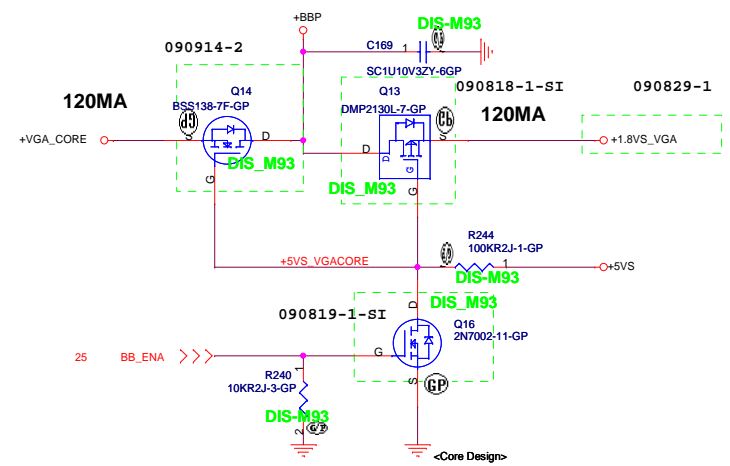
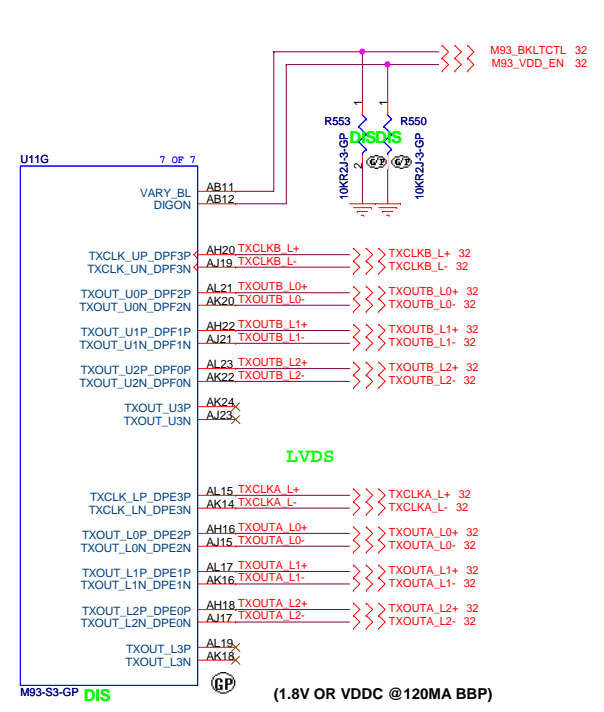
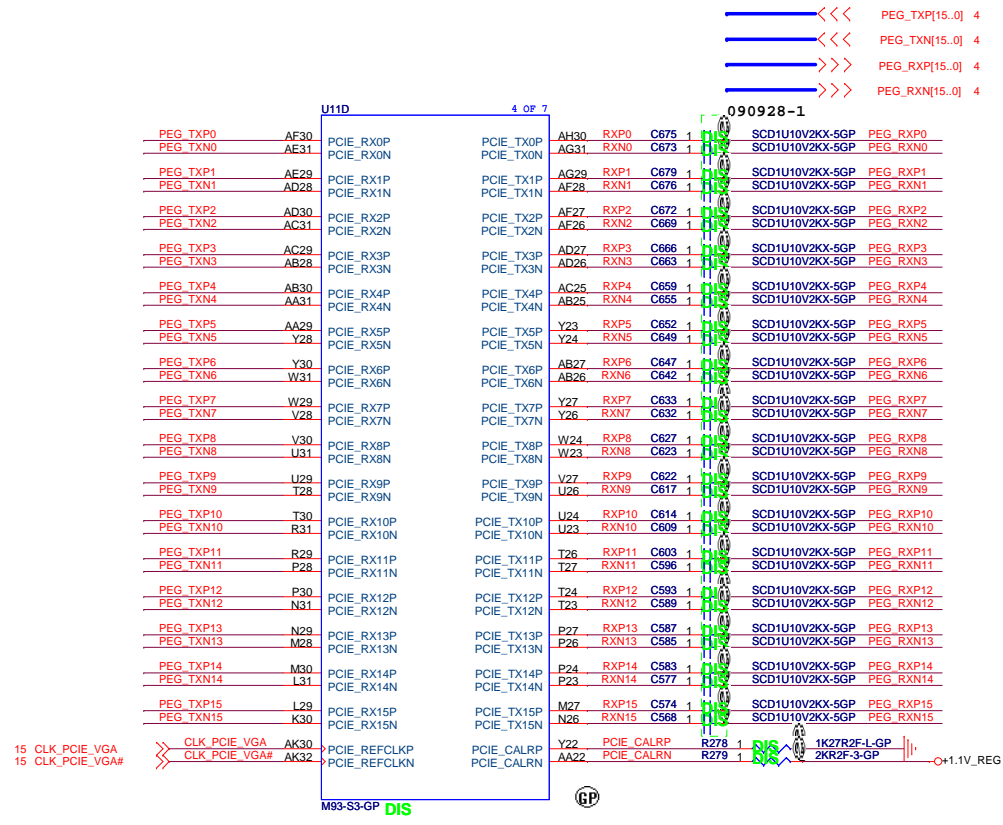
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Title: **Clock Generator ICS9LRS3197**

Size A3 Document Number: **S-Class Intel** Rev: **SD**

Date: Wednesday, October 28, 2009 Sheet 23 of 62



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Title: **VGA-PCIE/LVDS(1/5)**

Size: A3 Document Number: **S-Class Intel** Rev: SD

Date: Wednesday, October 28, 2009 Sheet: 24 of 62

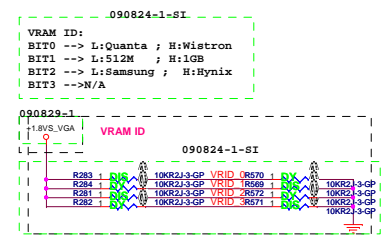
M93 GPU(2/5)

CONFIGURATION STRAPS
 0 = DON'T INSTALL RES
 1 = INSTALL 10K RES
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M93-S3
TX_PWRS_ENB	GPIO0	POE FULL TX OUTPUT SWING	X
TX_DEMPLH_EN	GPIO1	POE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	POE GEN2 ENABLED	X
RSVD	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO20		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROM_ID_CFG(2/0)	GPIO(13/1)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	XXX
RSVD	GENERICC	AUD[1] AUDIO[0]	0
AUD[1]	VSYSN	0 0 No audio function	0
AUD[0]	VSYSN	0 0 No audio function	0
		1 0 Audio for DisplayPort and HDMI if dangle is detected	XX
		1 0 Audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

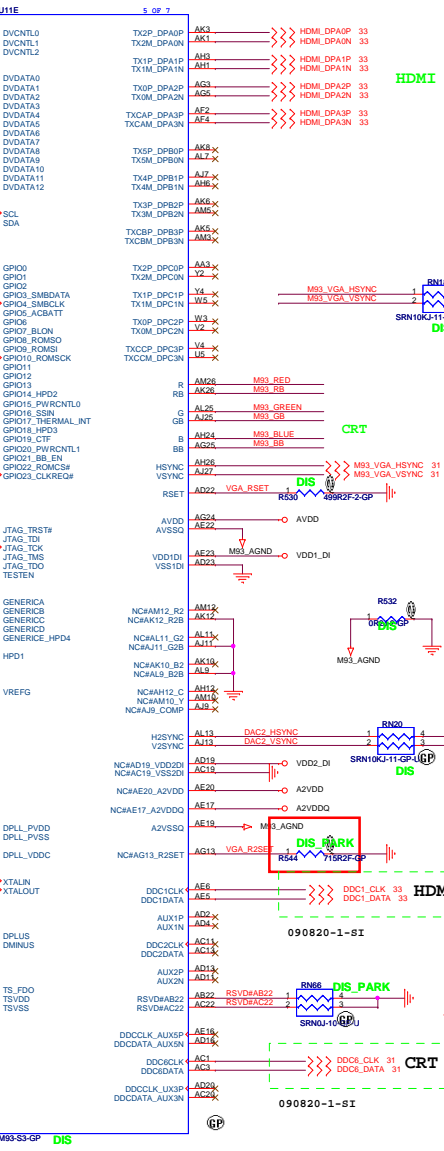
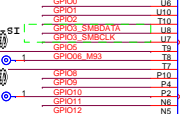
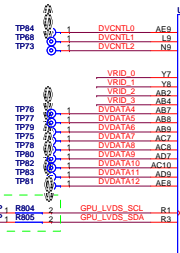
Aperture Config.	M93S3	Strapping Resistor	64MB VRAM	128MB VRAM	256MB VRAM
CONFIG0	GPIO_11	R243	0	0	1
CONFIG1	GPIO_12	R246	1	0	0
CONFIG2	GPIO_13	R250	0	0	0

VRID	3210	Vendor	Type	Vendor P/N
0000	Hynix Orion-die	64*16-800MHZ	H5TQ1G63BFR-12C	
0001	Samsung E-die	64*16-800MHZ	K4W1G1646E-HC12	



M93 LP: VDDC-0.9/1.1V

SPI020_VID1	SPI015_VID0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

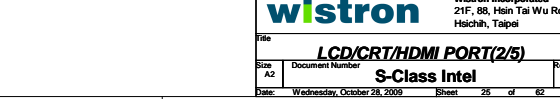
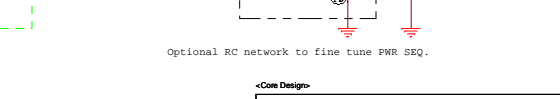
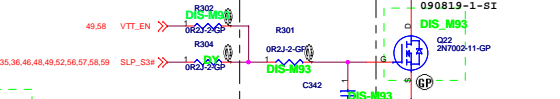
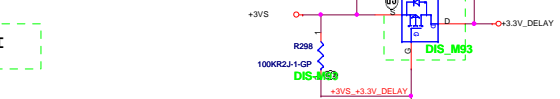
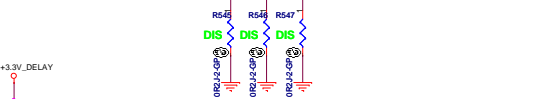
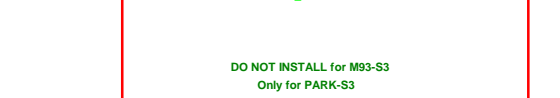
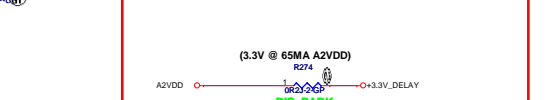
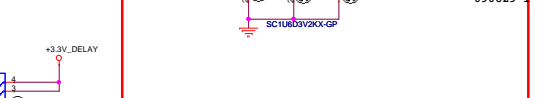
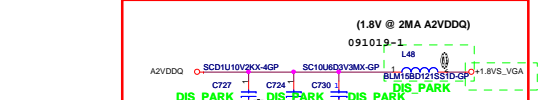
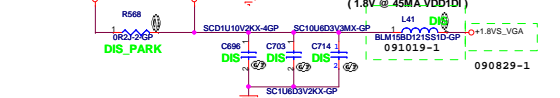
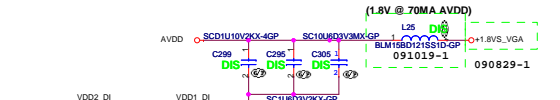
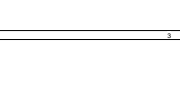
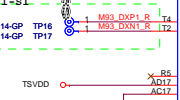
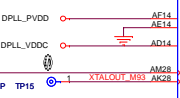
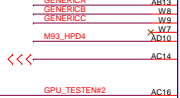
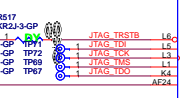
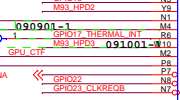
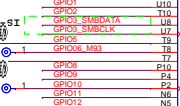
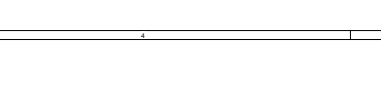
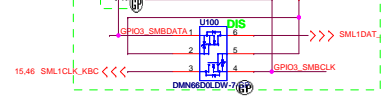
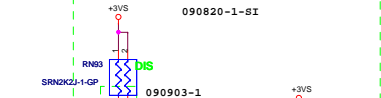
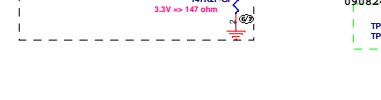
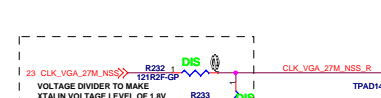
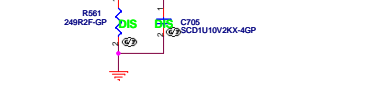
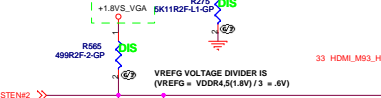
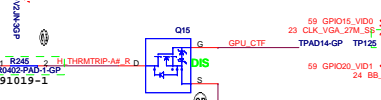
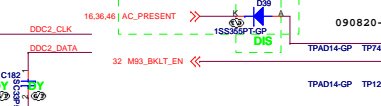
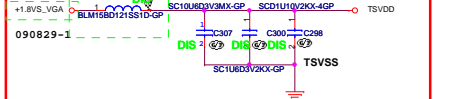
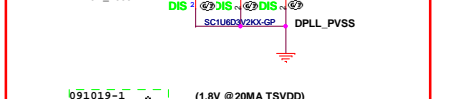
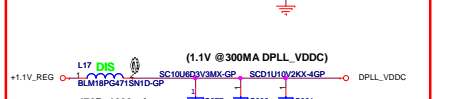
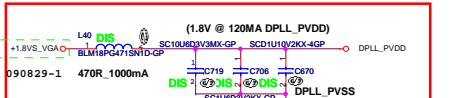
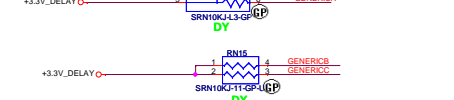
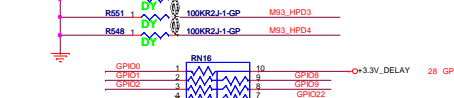
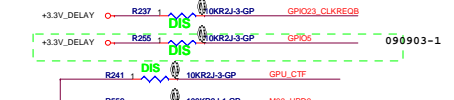
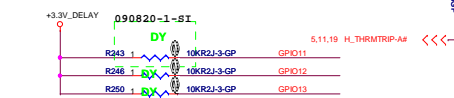


HDMI

CRT

HDMI

CRT



Optional RC network to fine tune PWR SEQ.

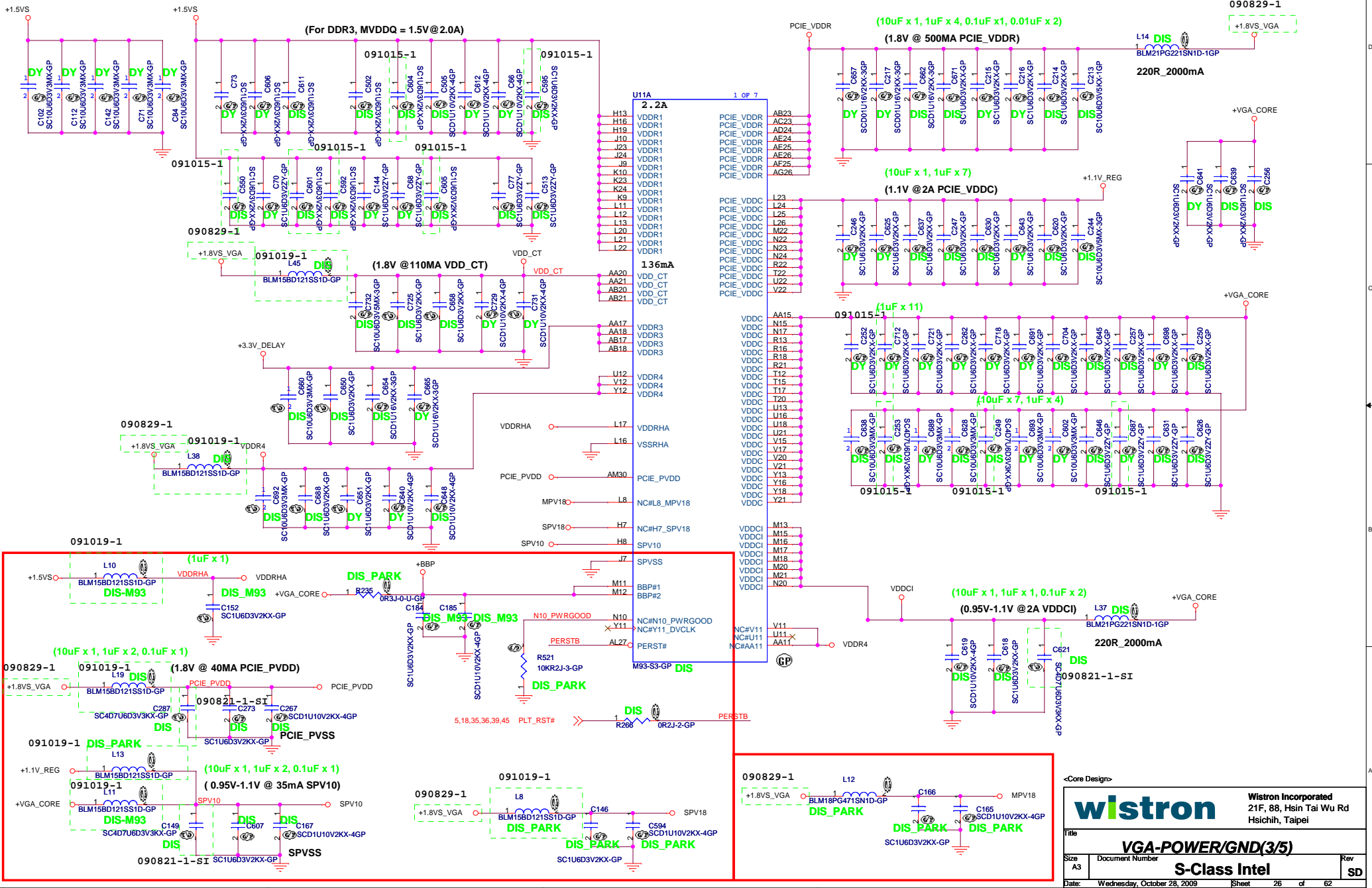
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File: **LCD/CRT/HDMI PORT(2/5)**

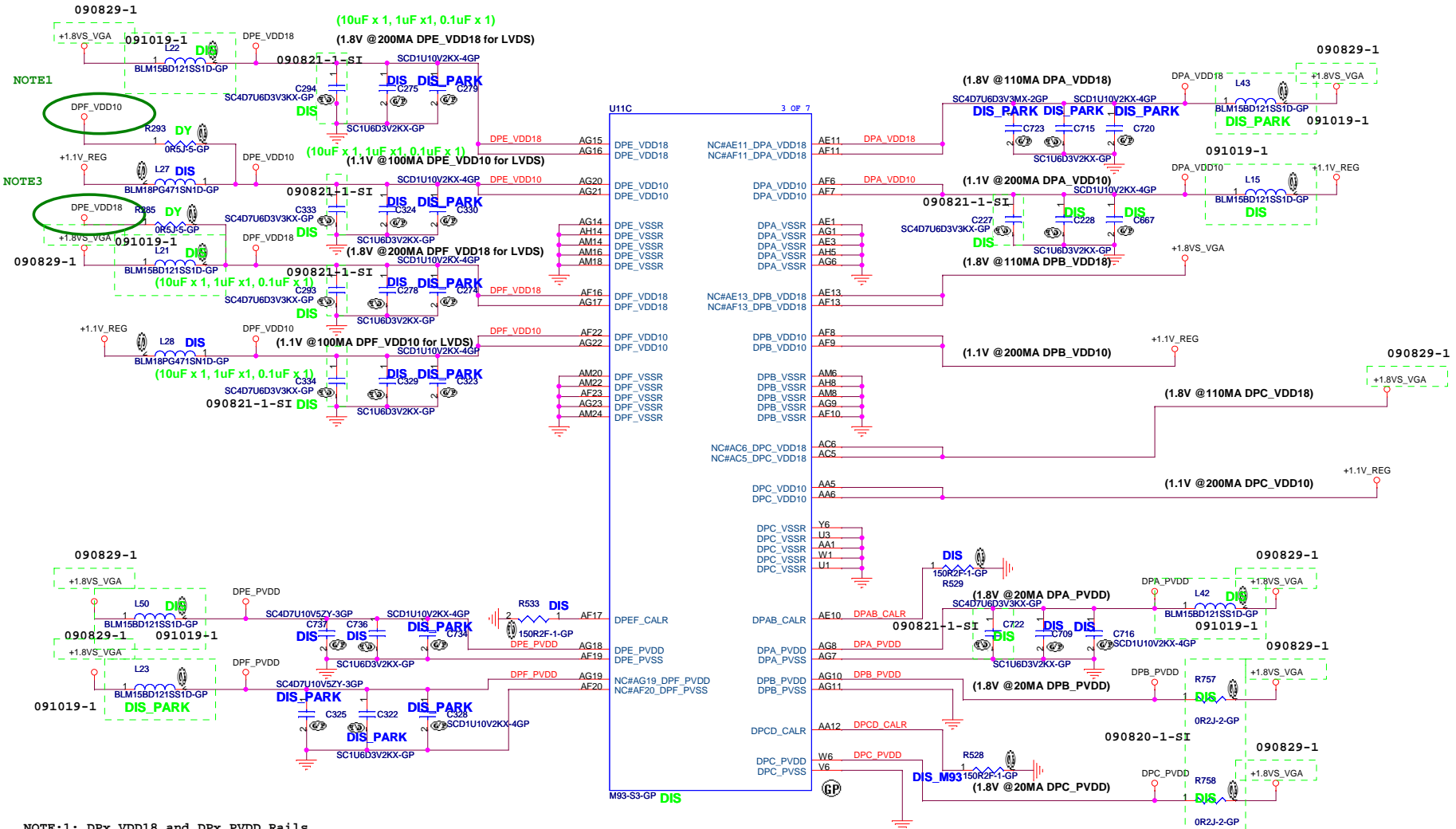
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Date: Wednesday, October 28, 2009 Sheet 25 of 62

M93 GPU(3/5)



M93 GPU(4/5)



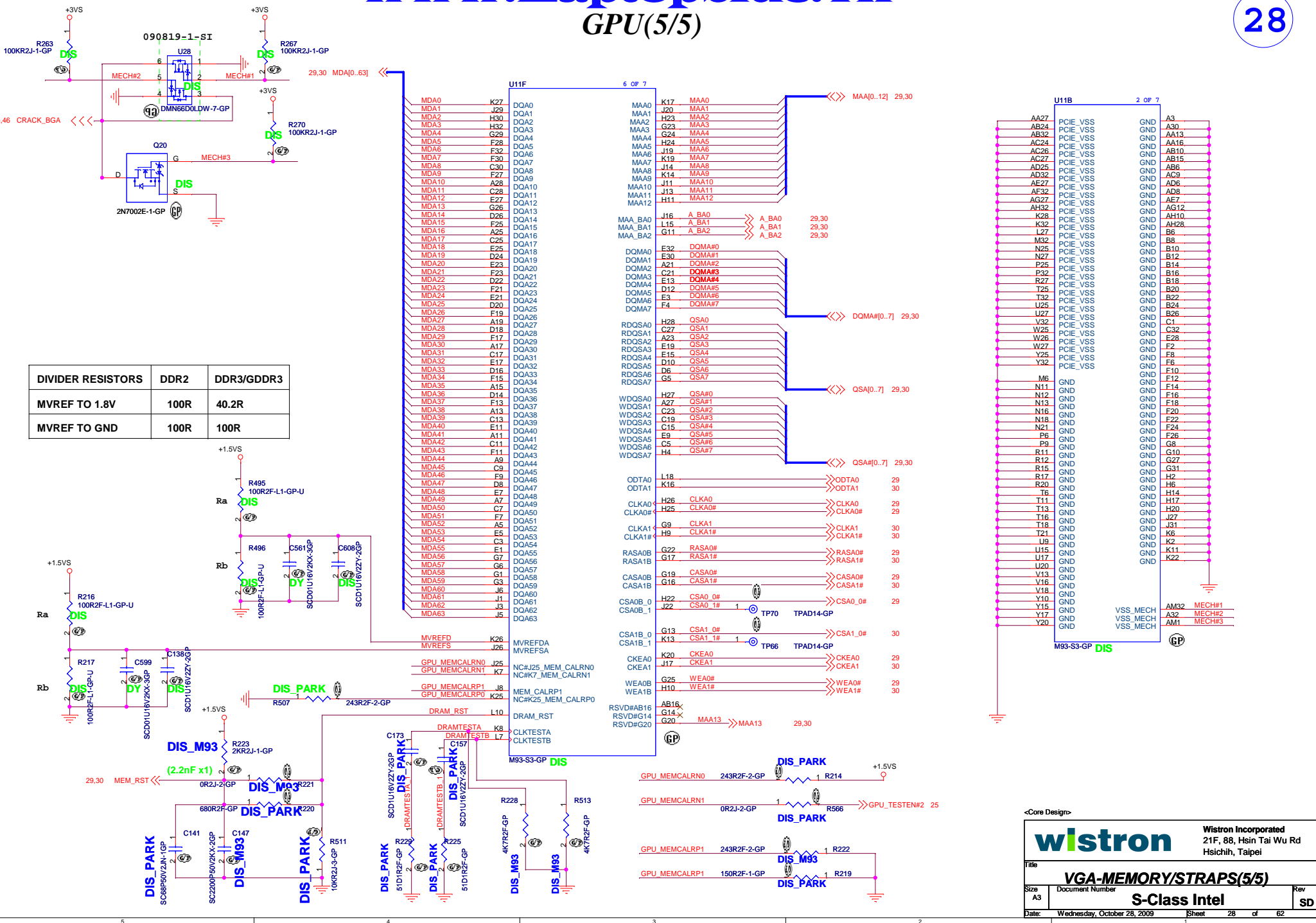
NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPE_VDD10 and DPF_VDD10 / DPE_VDD10 Rails can be join together and remove Decoupling Capacitors and BEAD for one rail of each pair if signal integrity for DP lanes are OK. We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove Decoupling Capacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need at least 500mA Bead to support join rails.

<Core Design>

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		Title: VGA-POWER/GND(4/5)	
Size: A3	Document Number:	S-Class Intel	
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DIVIDER RESISTORS	DDR2	DDR3/GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

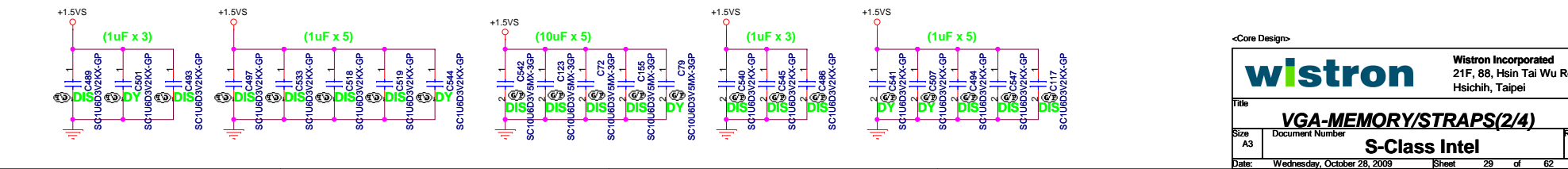
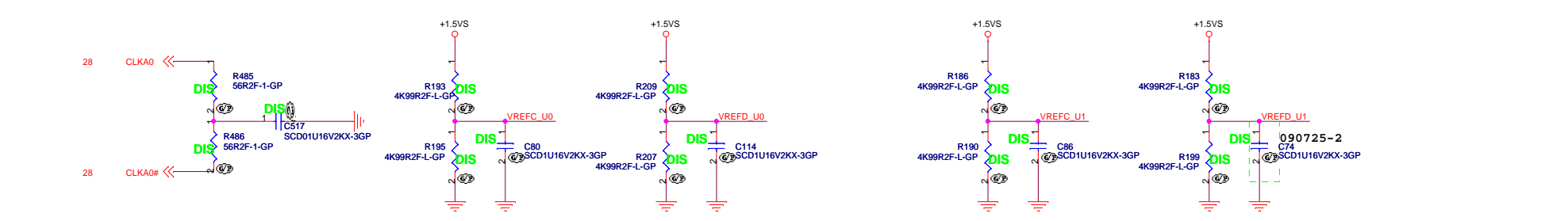
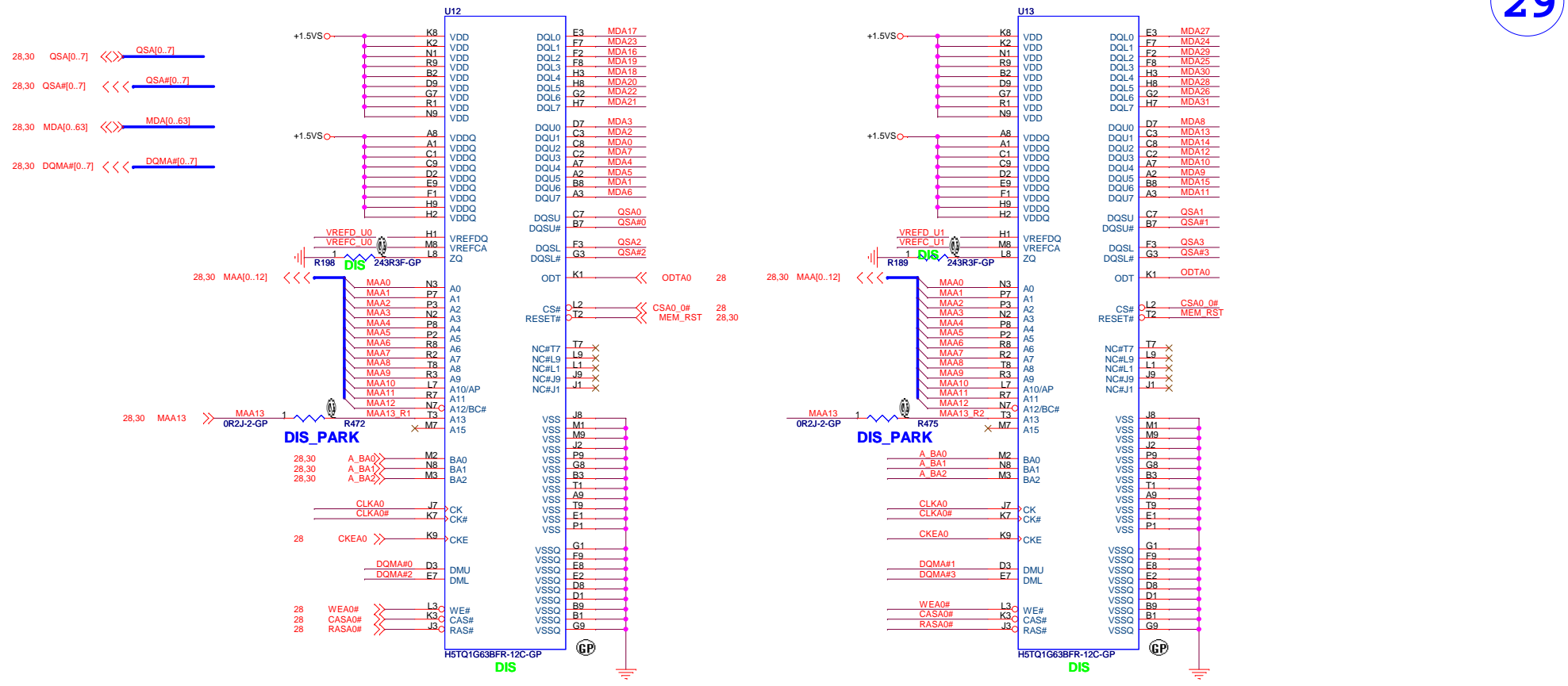
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Title: **VGA-MEMORY/STRAPS(5/5)**

Size: A3 Document Number: **S-Class Intel** Rev: SD

Date: Wednesday, October 28, 2009 Sheet 28 of 62



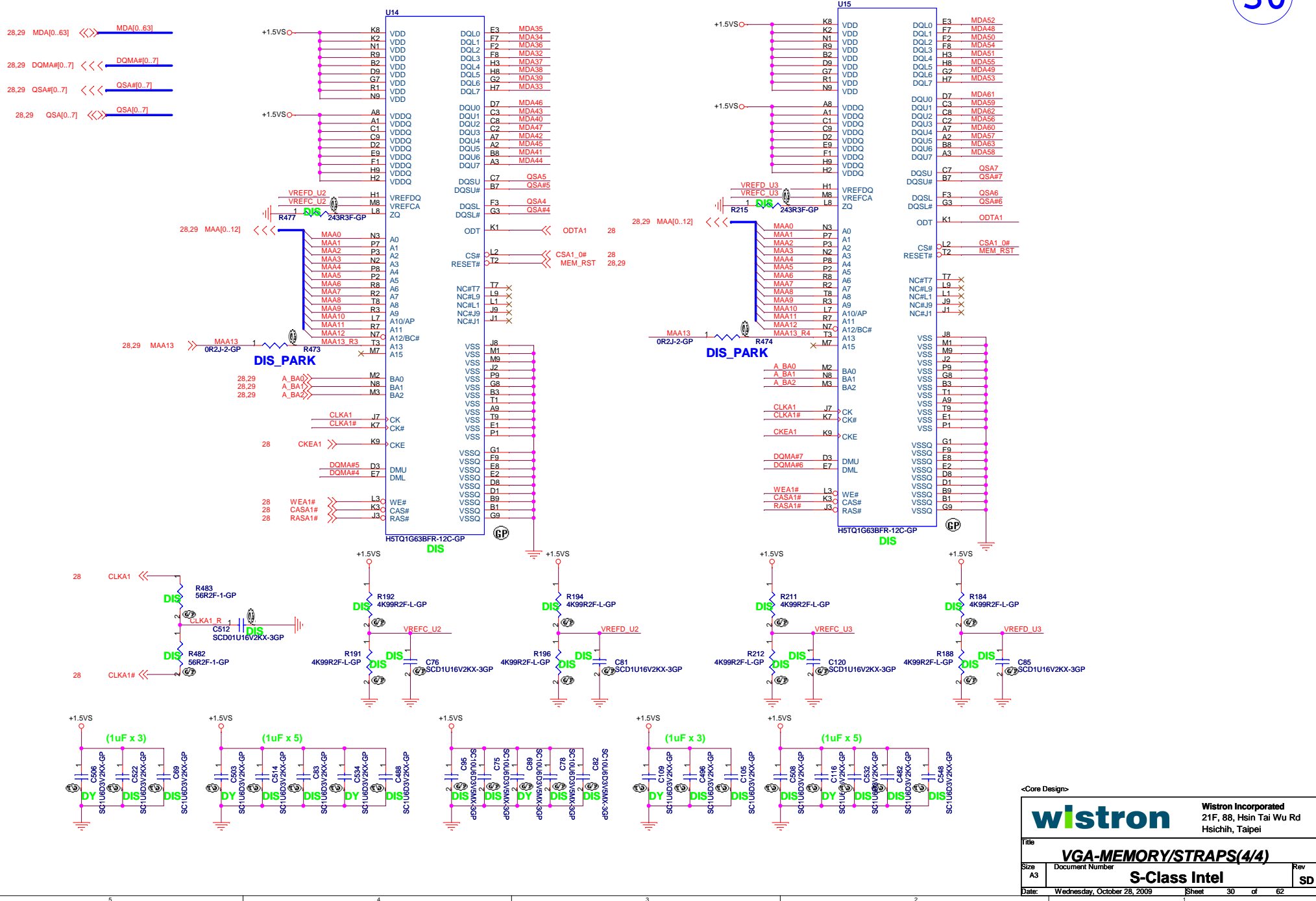
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Title: **VGA-MEMORY/STRAPS(2/4)**

Size: A3 Document Number: **S-Class Intel** Rev: SD

Date: Wednesday, October 28, 2009 Sheet 29 of 62



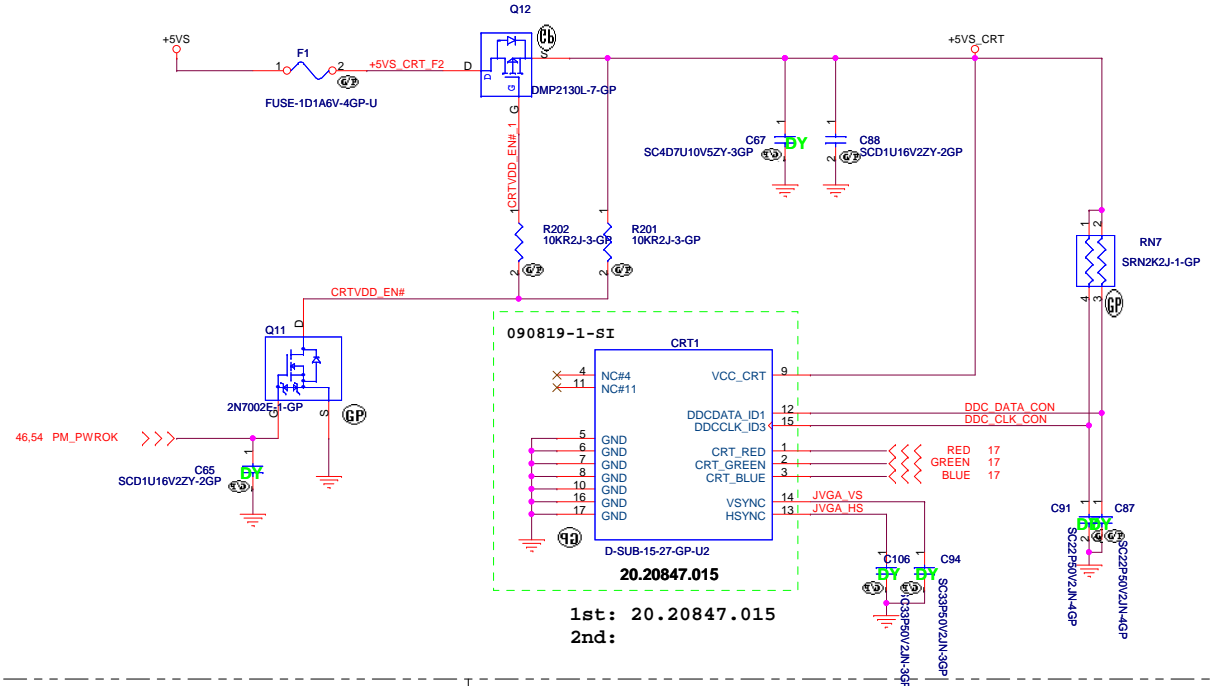
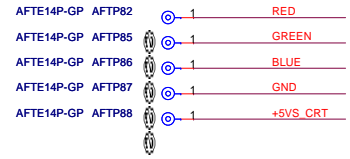
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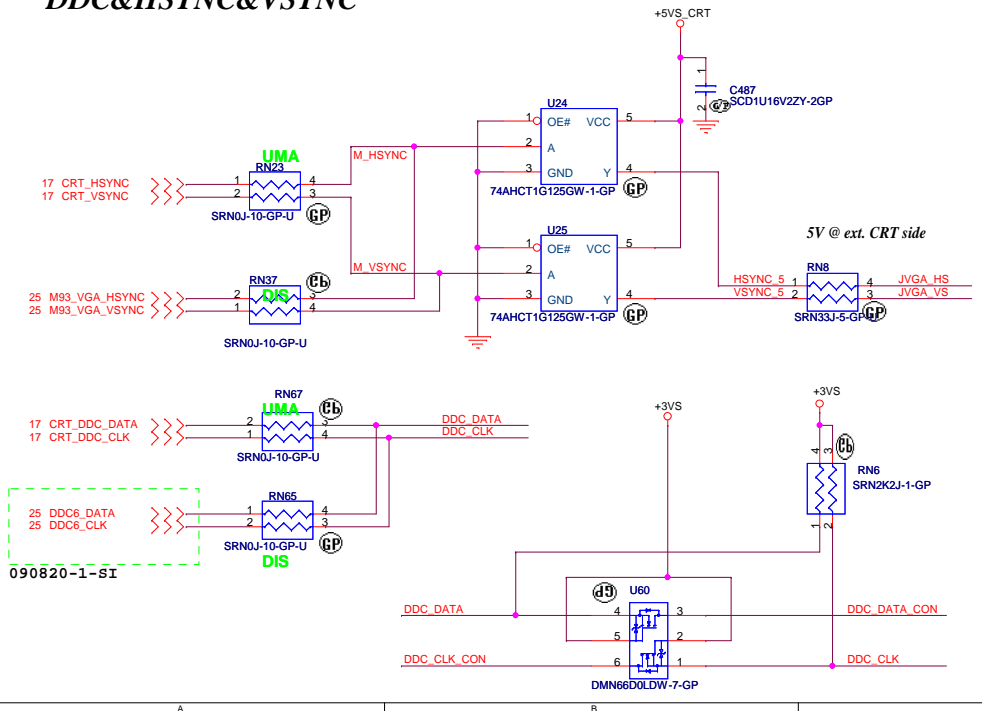
Title: **VGA-MEMORY/STRAPS(4/4)**

Size: A3 Document Number: **S-Class Intel** Rev: SD

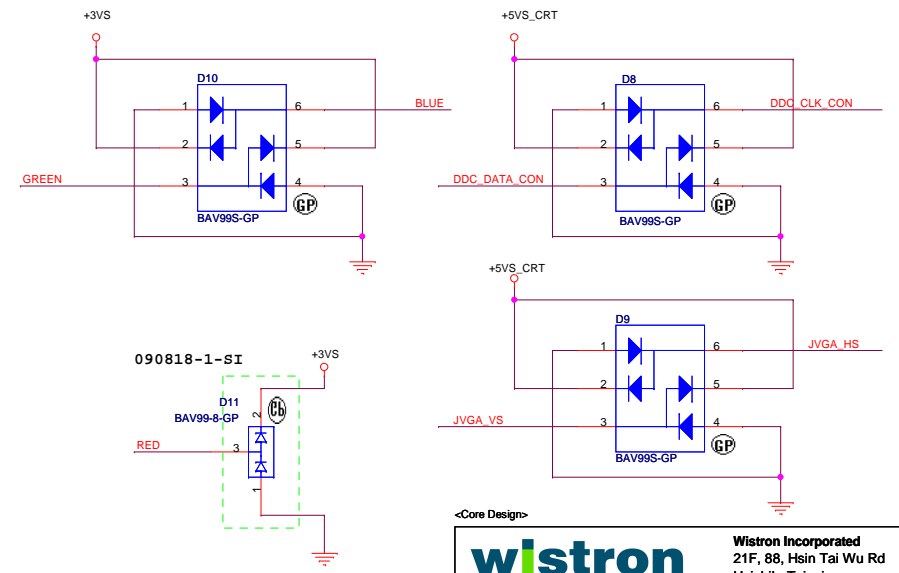
Date: Wednesday, October 28, 2009 Sheet 30 of 62



DDC&HSYNC&VSYNC



ESD



<Core Design>

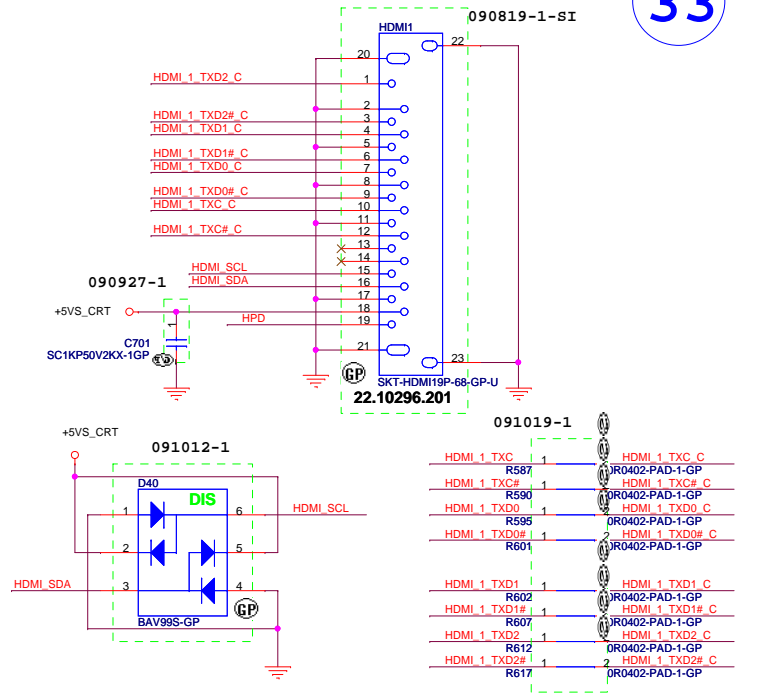
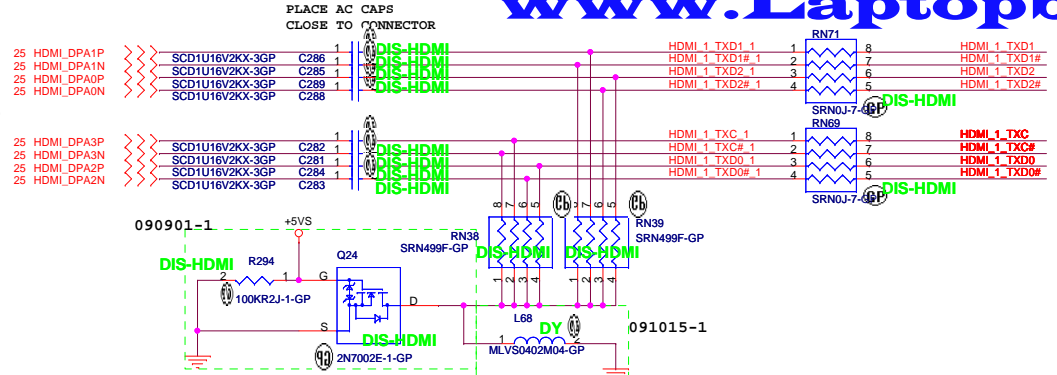
wistron Wistron Incorporated
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Hsichih, Taipei

Title: **CRT Connector**

Size A3 Document Number: **S-Class Intel** Rev: **SD**

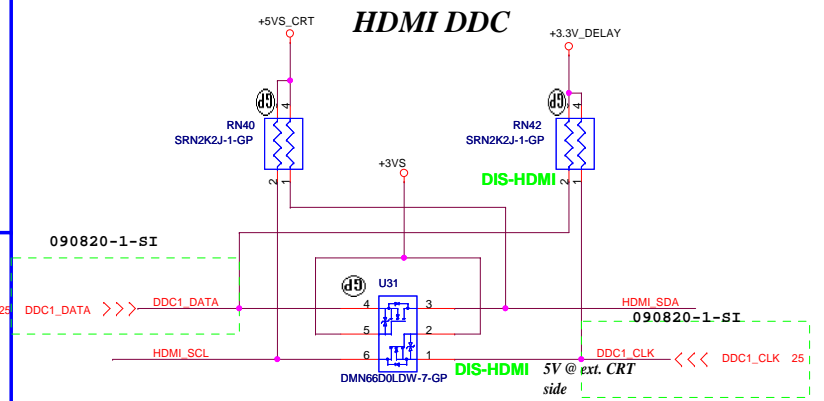
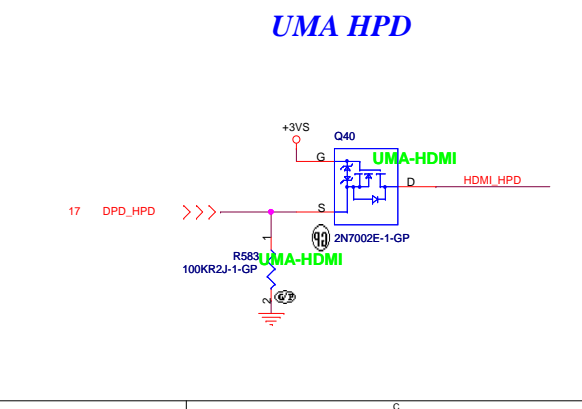
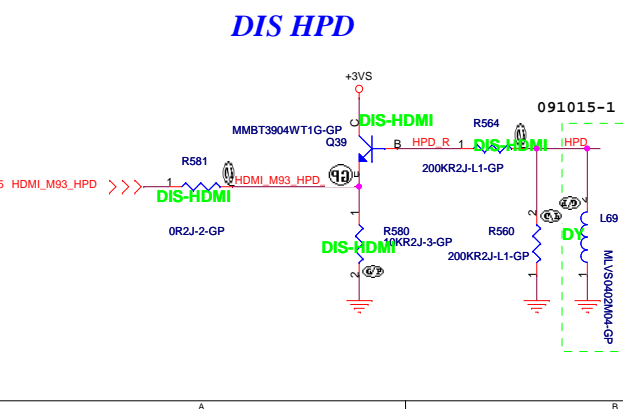
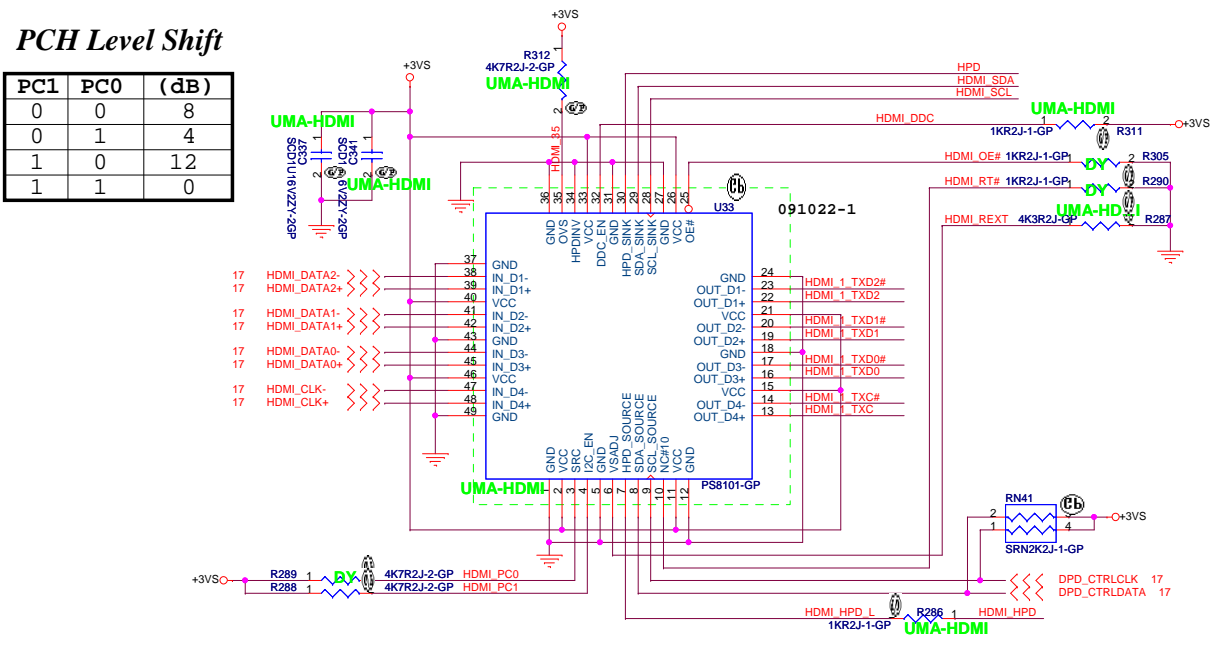
Date: Wednesday, October 28, 2009 Sheet 31 of 62

M93



PCH Level Shift

PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0



<Core Design>

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 Hsichih, Taipei

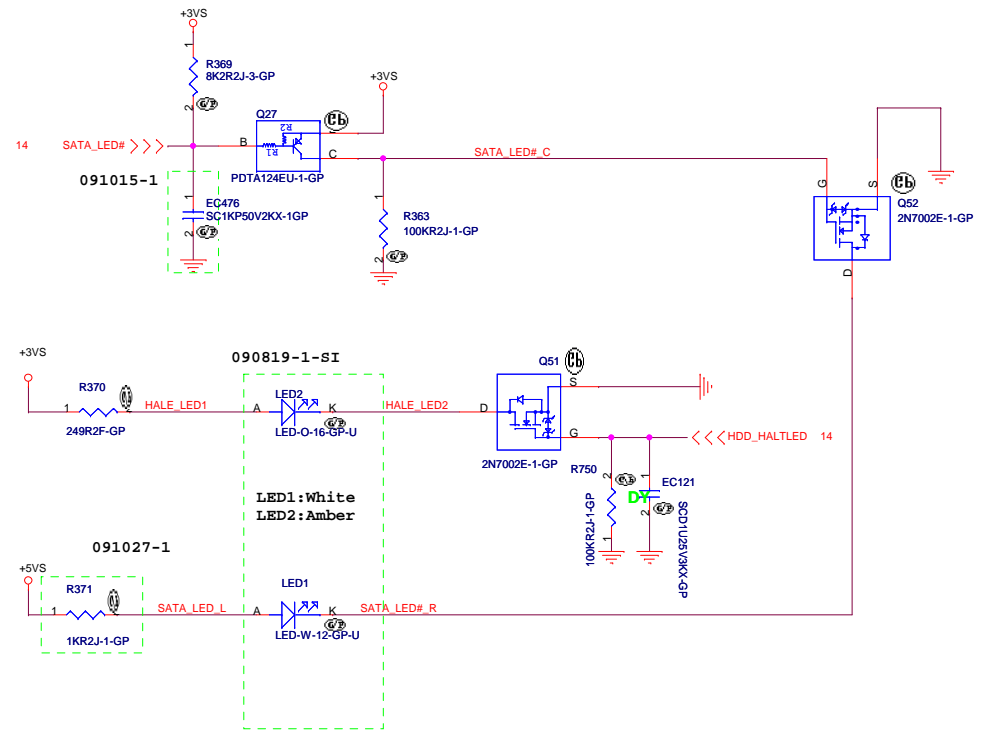
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Size: A3 Document Number: **S-Class Intel** Rev: **SD**

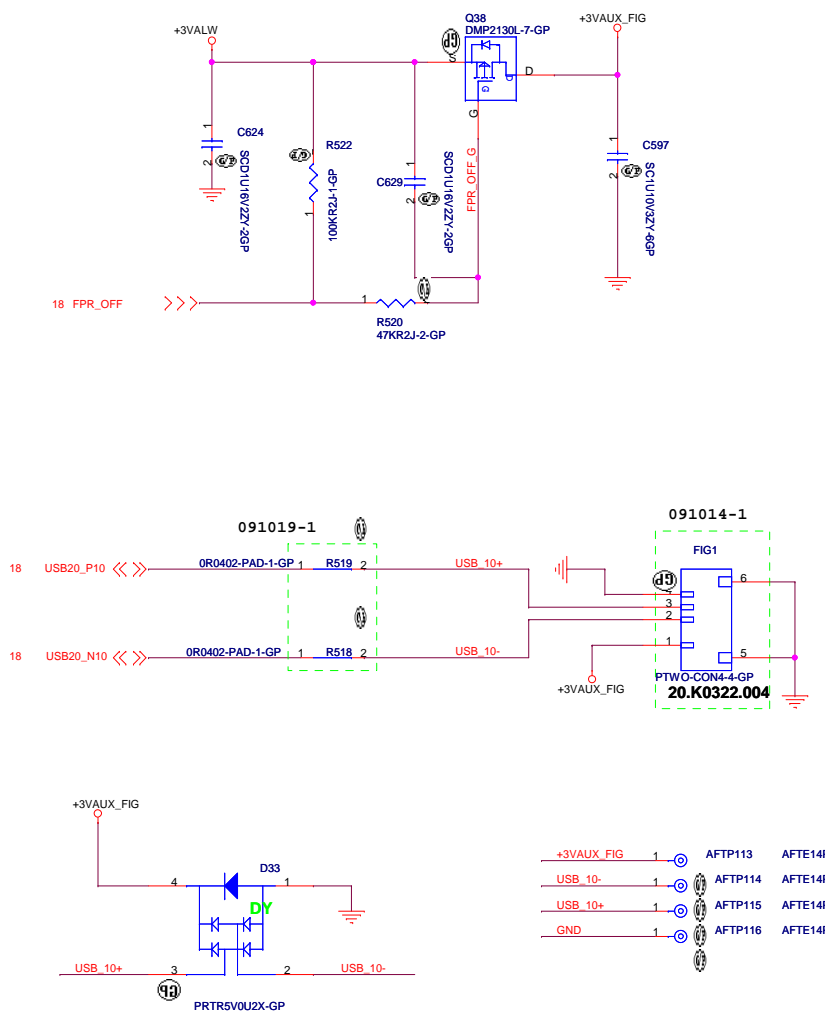
Date: Wednesday, October 28, 2009 Sheet: 33 of 62

SATA LED FOR HDD

090630-1



Fingerprint



+3VAUX_FIG	1	AFTP113	AFFE14P-GP
USB_10-	1	AFTP114	AFFE14P-GP
USB_10+	1	AFTP115	AFFE14P-GP
GND	1	AFTP116	AFFE14P-GP

<Core Design>

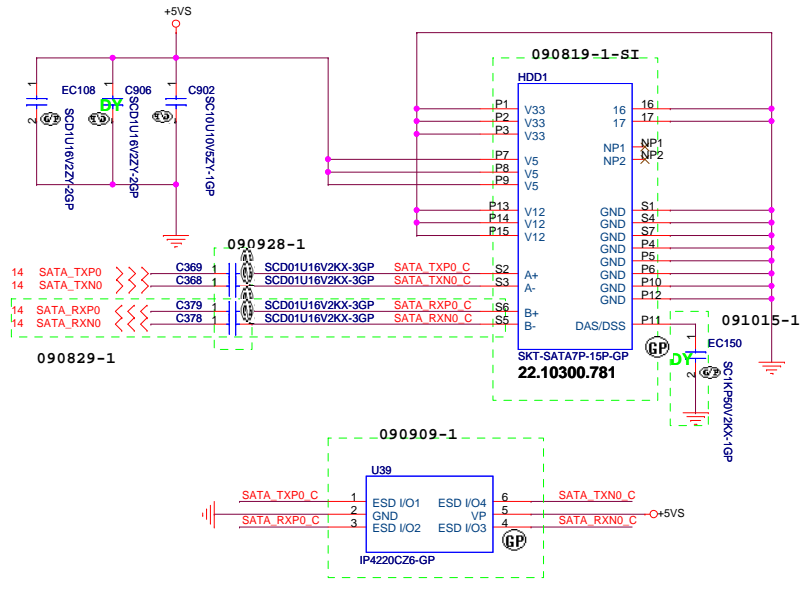
wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **SATA&CAP LED&GOLDEN FINGER**

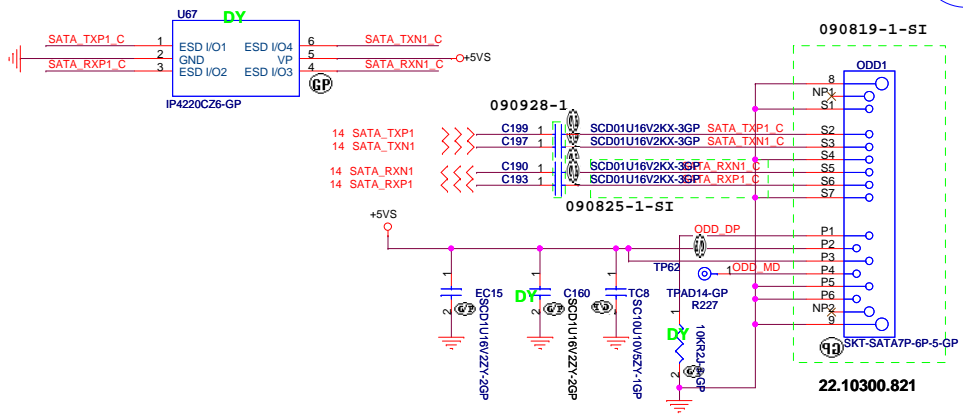
Size: A3 Document Number: **S-Class Intel** Rev: **SD**

Date: Wednesday, October 28, 2009 Sheet 34 of 62

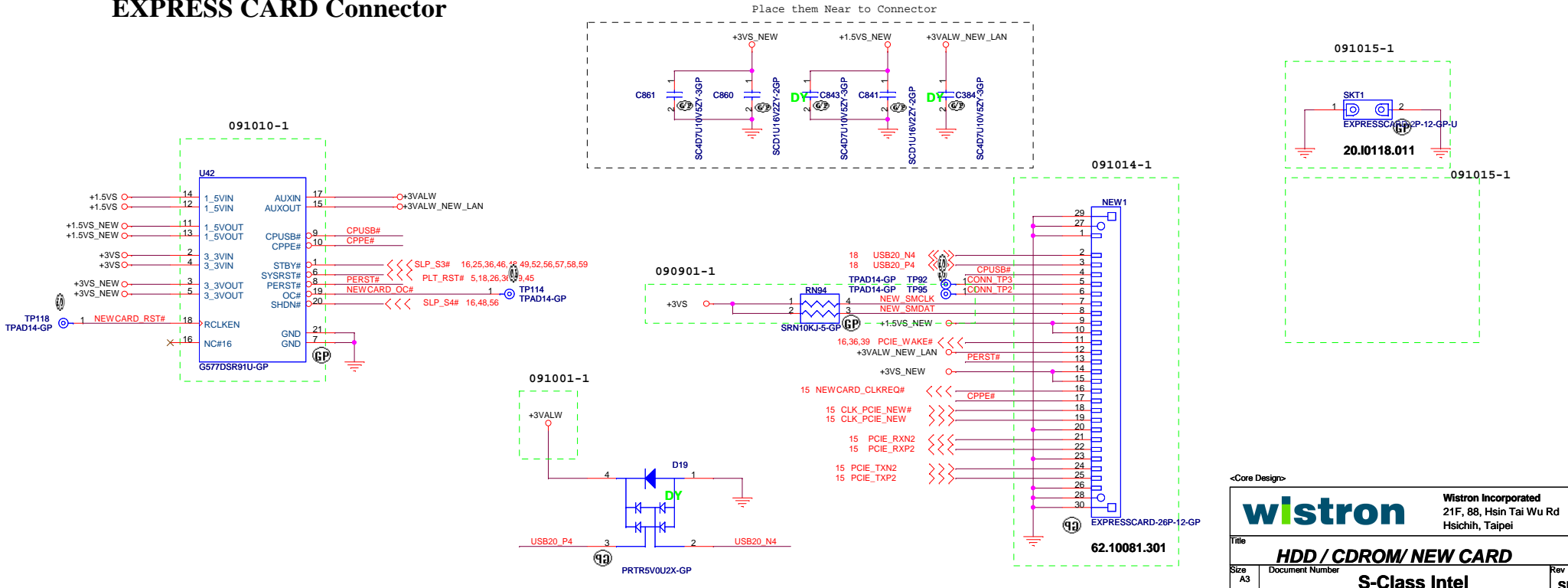
SATA HD Connector



ODD Connector



EXPRESS CARD Connector



<Core Design>

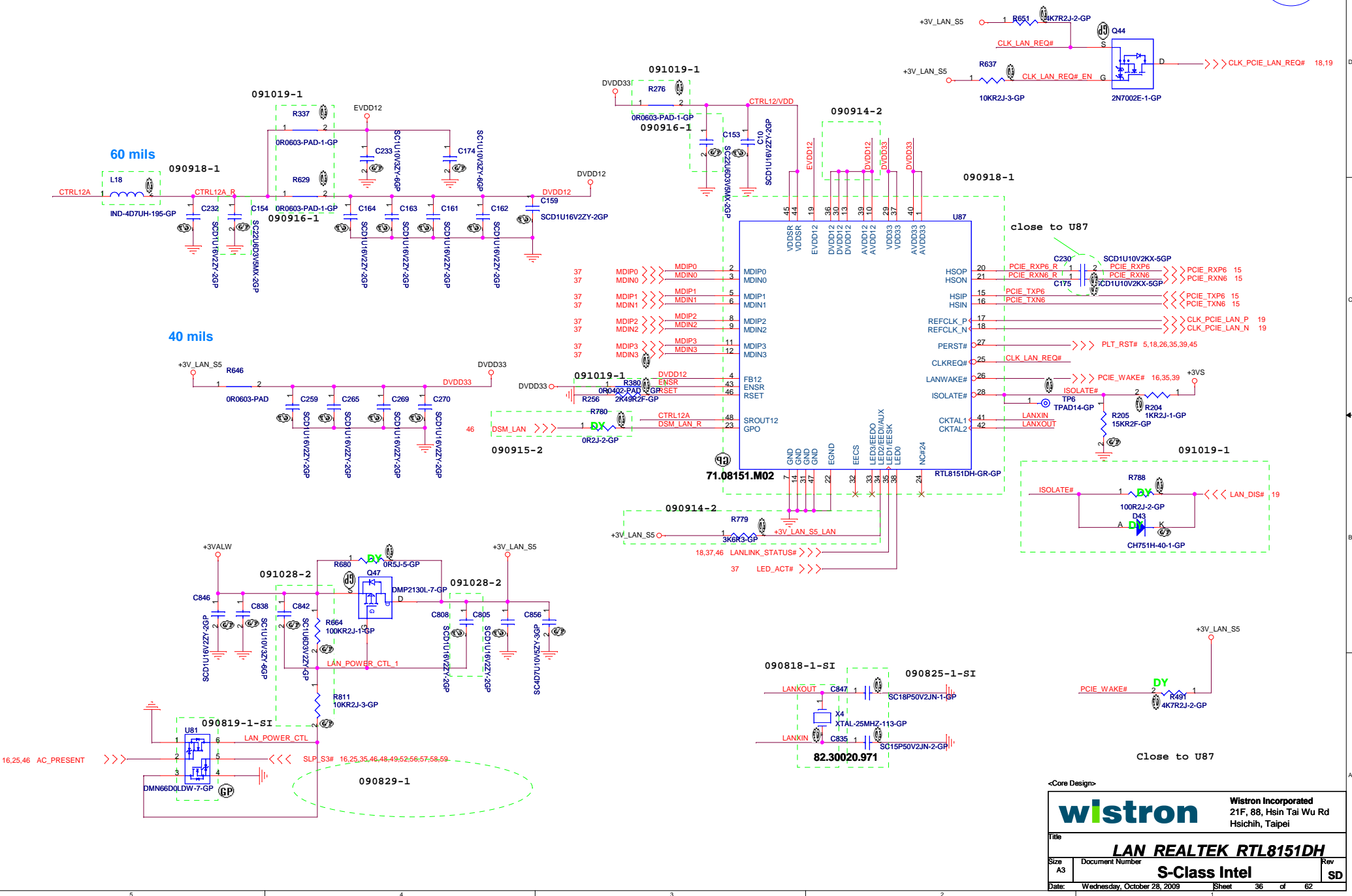
wistron

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **HDD / CDROM / NEW CARD**

Size A3: Document Number: **S-Class Intel** Rev: **SD**

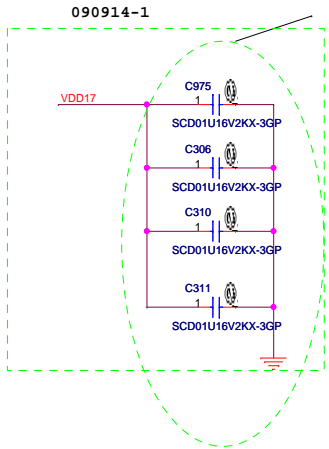
Date: Wednesday, October 28, 2009 Sheet 35 of 62



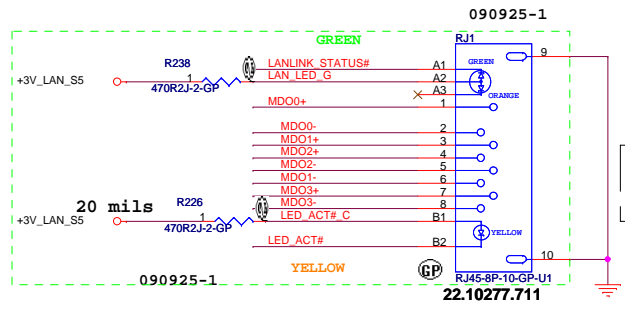
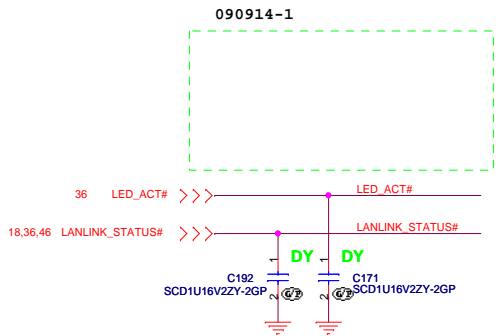
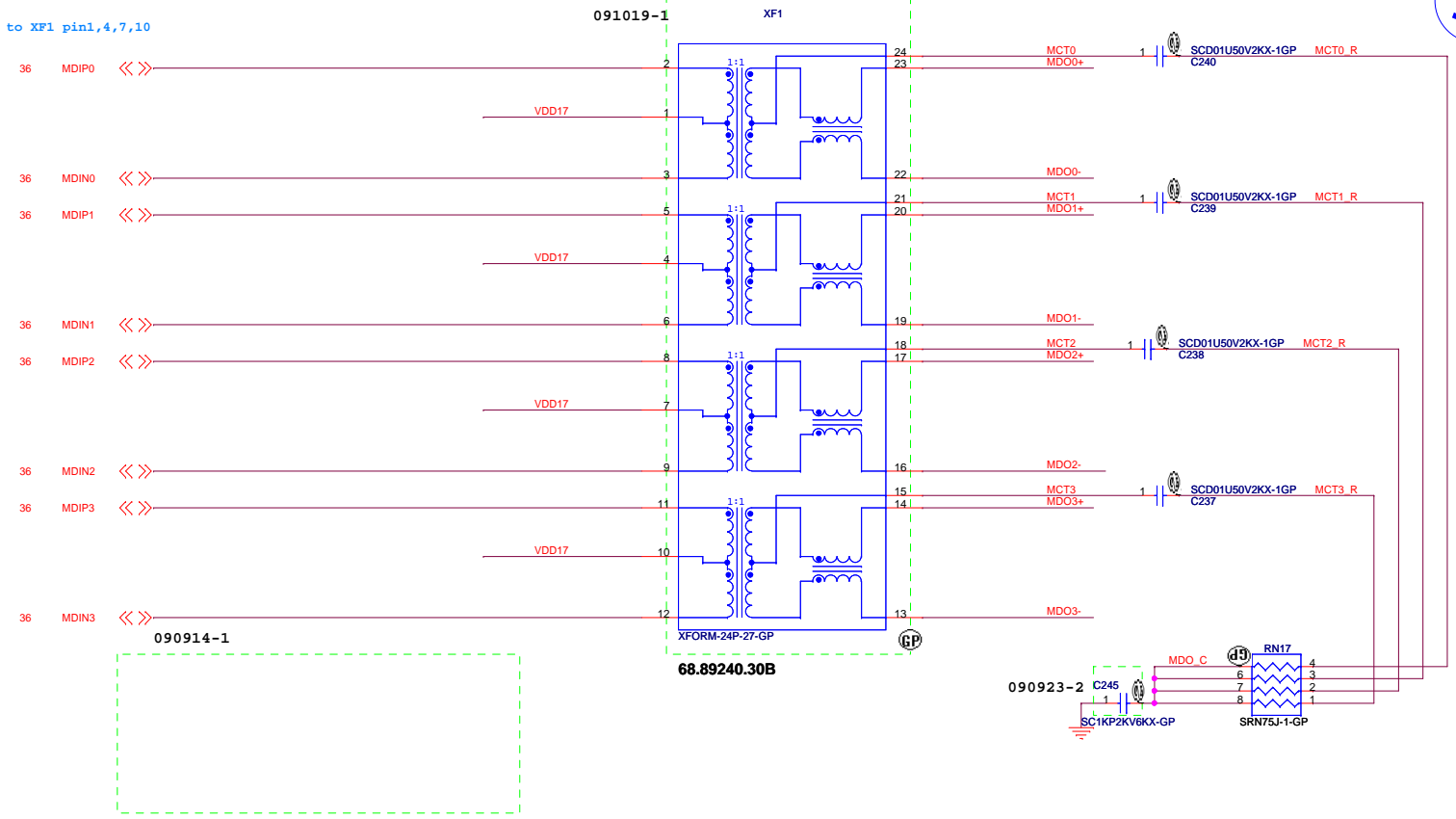
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Hsichih, Taipei

Title	LAN REALTEK RTL8151DH		
Size	Document Number	S-Class Intel	
A3		Rev	SD
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close to XF1 pin1,4,7,10



Yellow
B1(+), B2(-)
Green
A1(-), A2(+)

IF NOT OVER CLOCKING, LED_ACT# WILL ACT HIGH Check LAN chip for LED_ACT# function on RJ45 connector pin define.

<Core Design>

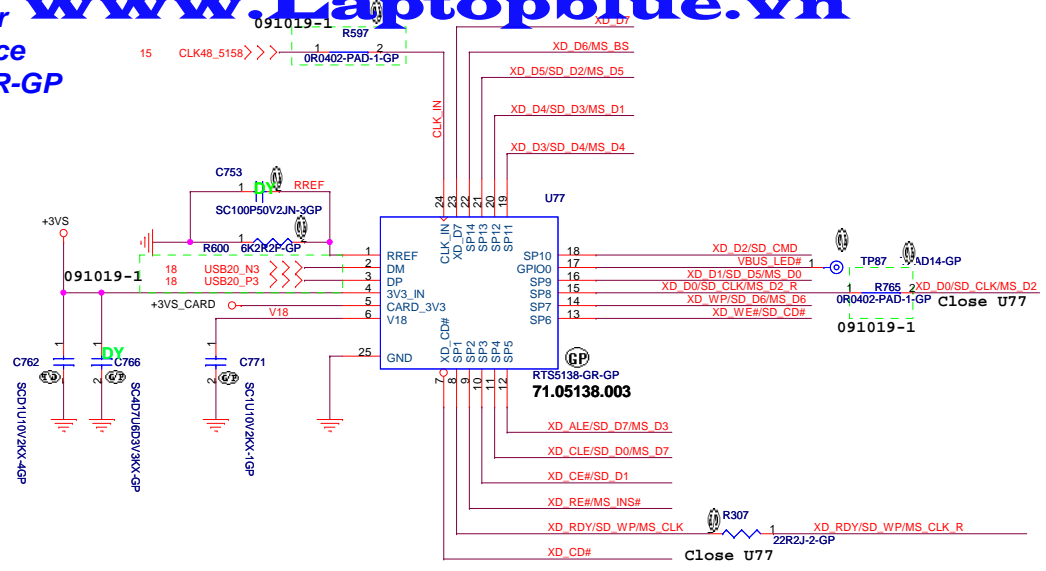
wistron Wistron Incorporated
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Hsichih, Taipei

Title: **Magnetic & RJ45**

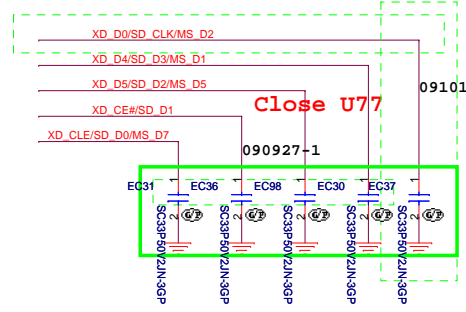
Size: A3 Document Number: **S-Class Intel** Rev: **SD**

Date: Wednesday, October 28, 2009 Sheet 37 of 62

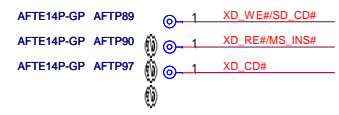
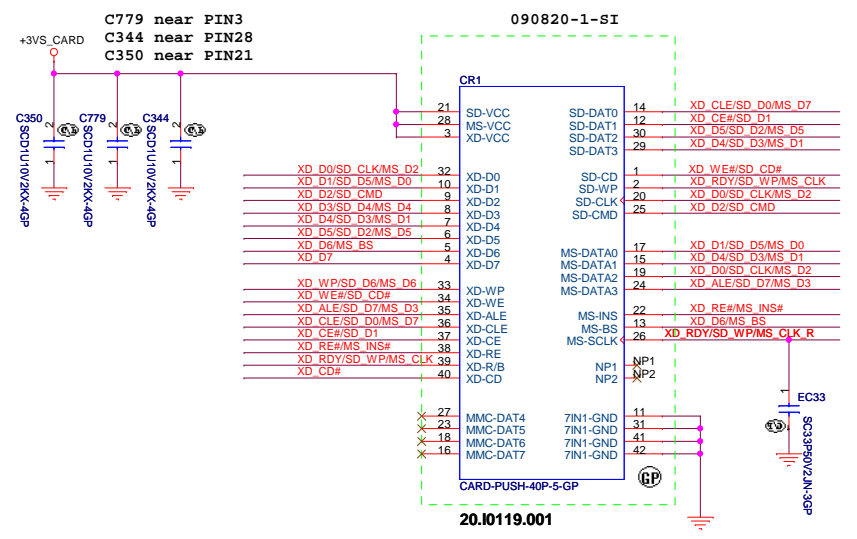
**Card Reader
USB Interface
RTS5138-GR-GP**



EMI Reserve Cap



4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)

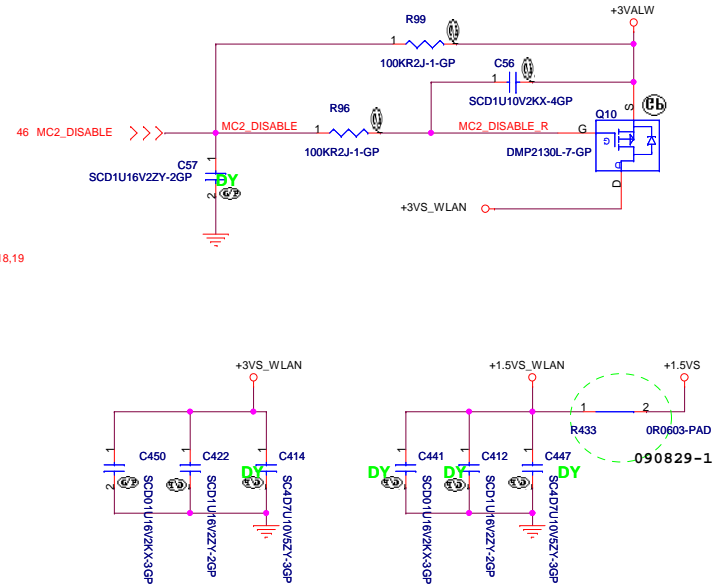
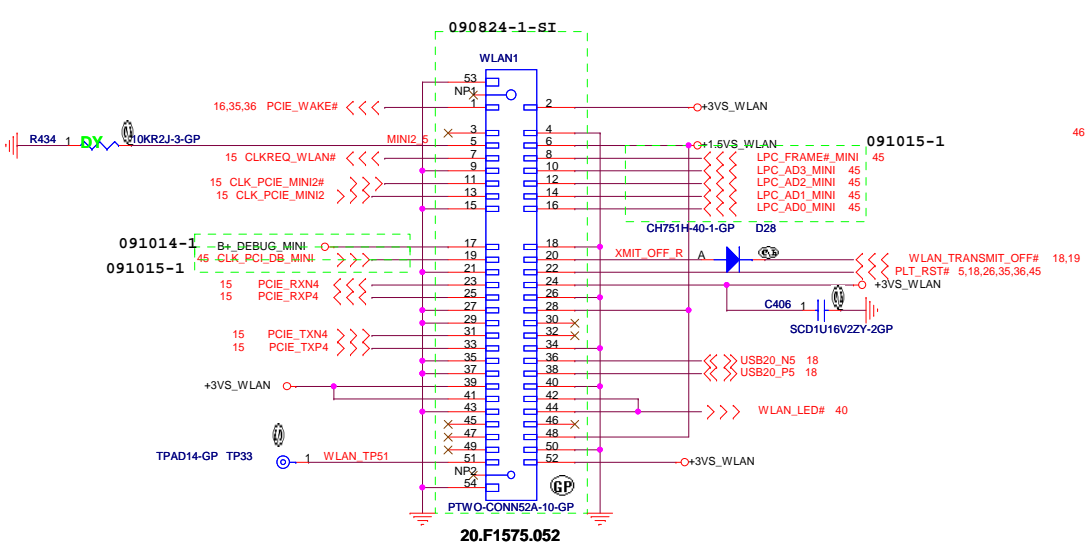


090829-1

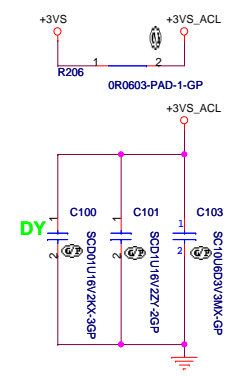
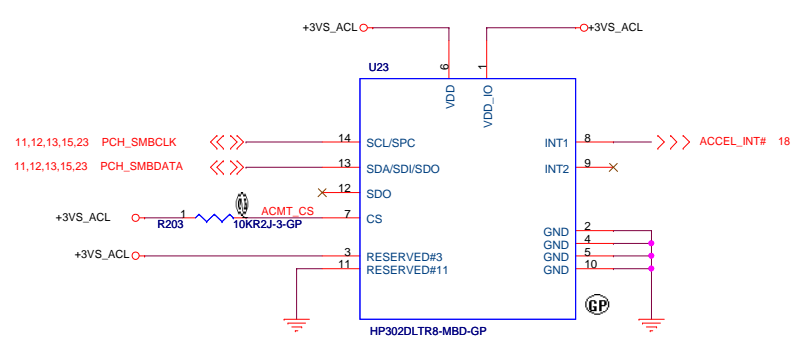
<Core Design>

wistron		Wistron Incorporated	
		21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title CardReader RTS5138			
Size A3	Document Number	S-Class Intel	Rev
Date: Wednesday, October 28, 2009	Sheet 38	of 62	SD

Mini-Card--WLAN
Half minicard



ACCELEROMETER



<Core Design>

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Hsichih, Taipei

Title: **Mini-Card/Accelerometer**

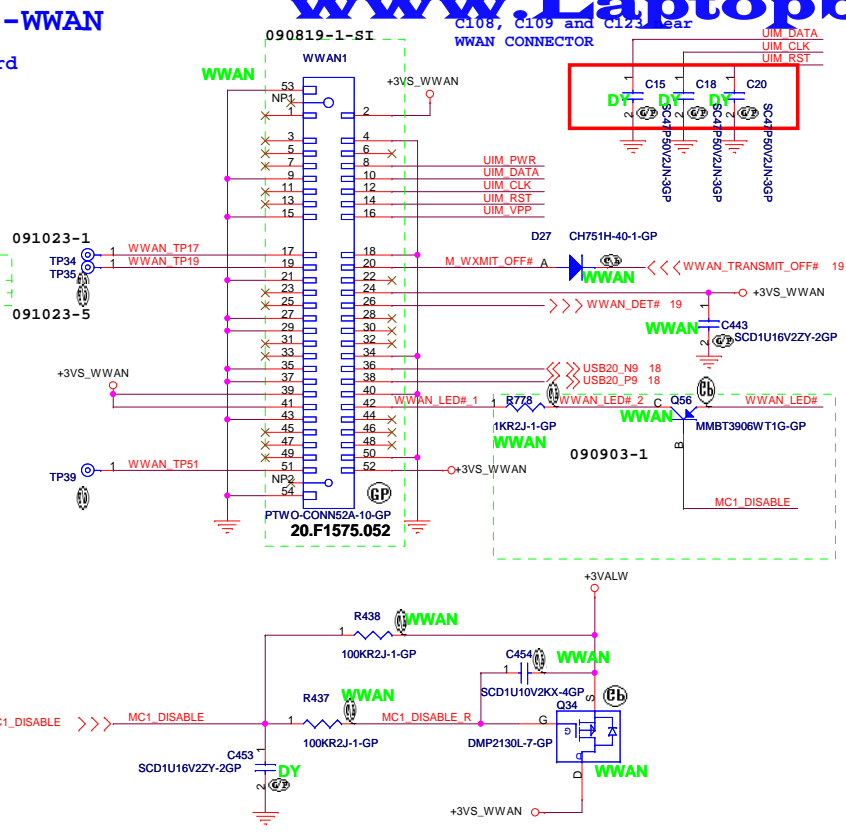
Size: A3 Document Number: **S-Class Intel** Rev: **SD**

Date: Wednesday, October 28, 2009 Sheet 39 of 62

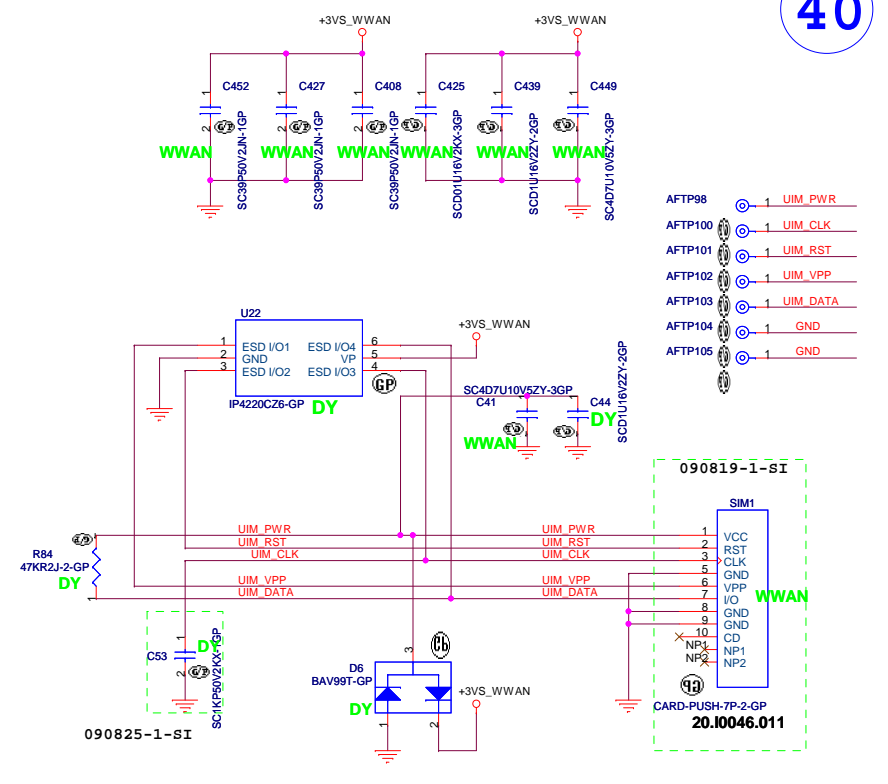
Mini-Card--WWAN

Full minicard

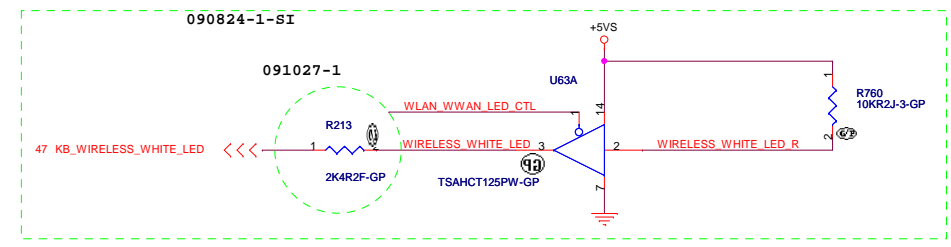
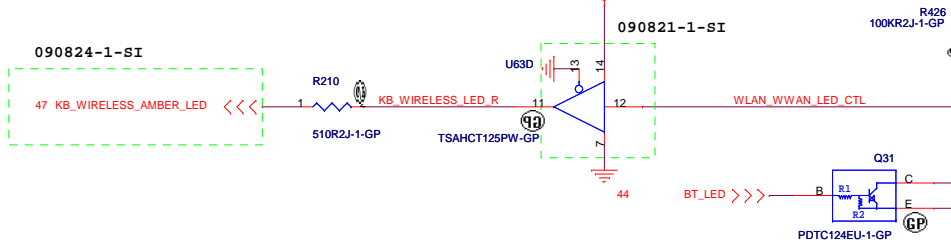
- AFTP106 ① 1 UIM_PWR
- AFTP106 ① 1 UIM_DATA
- AFTP109 ① 1 UIM_CLK
- AFTP110 ① 1 UIM_RST
- AFTP111 ① 1 UIM_VPP
- AFTP112 ① 1 M_WXMIT_OFF#
- AFTP125 ① 1 WWAN_LED# 1
- AFTP126 ① 1 WWAN_DET#
- AFTP127 ① 1 USB20_N9
- AFTP128 ① 1 USB20_P9
- AFTP129 ① 1 +3VS_WWAN
- AFTP142 ① 1 +3VS_WWAN
- AFTP143 ① 1 +3VS_WWAN
- AFTP144 ① 1 +3VS_WWAN
- AFTP145 ① 1 +3VS_WWAN
- AFTP208 ① 1 GND
- AFTP209 ① 1 GND
- AFTP210 ① 1 GND



www.Laptopblue.com SIM card slot



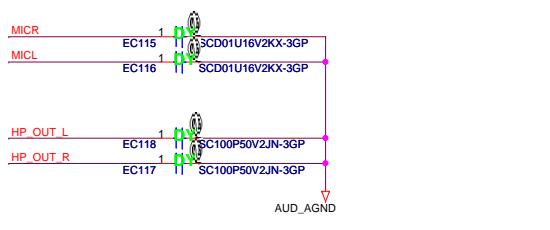
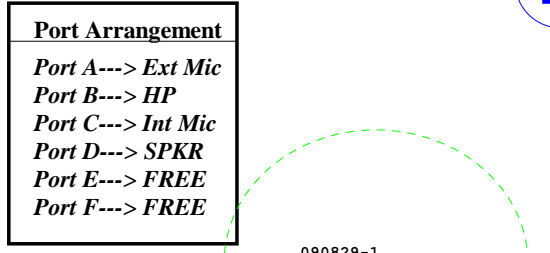
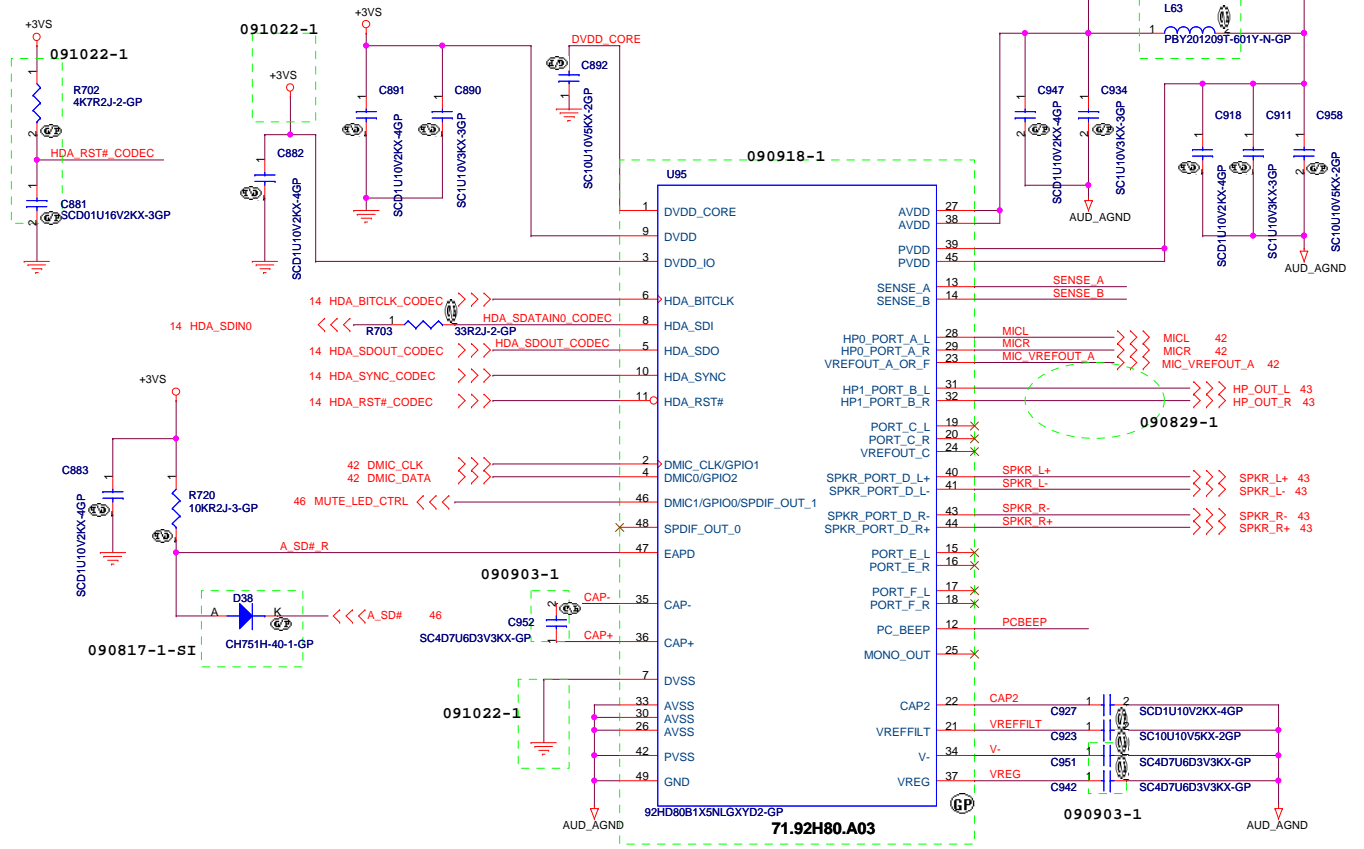
WIRELESS LED Control



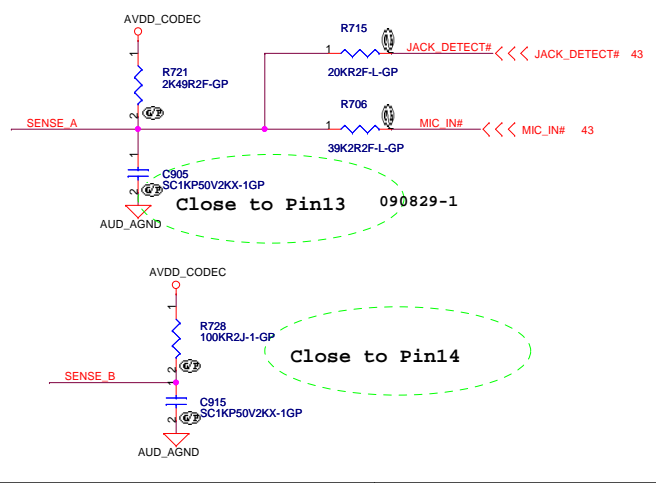
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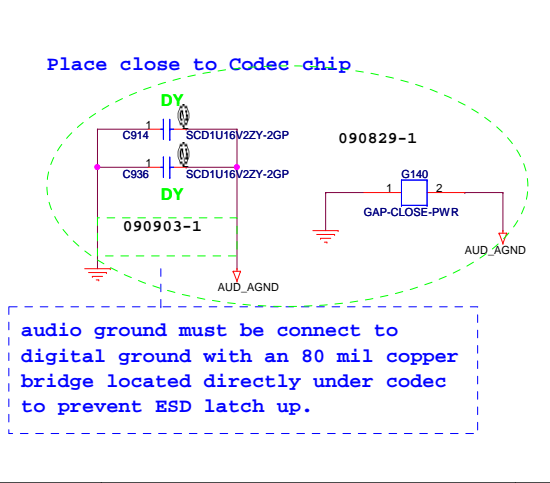
Title	Mini-Card/Accelerometer		
Size	Document Number	S-CLASS Intel	Rev
A3			SD
Date:	Wednesday, October 28, 2009	Sheet	40 of 62



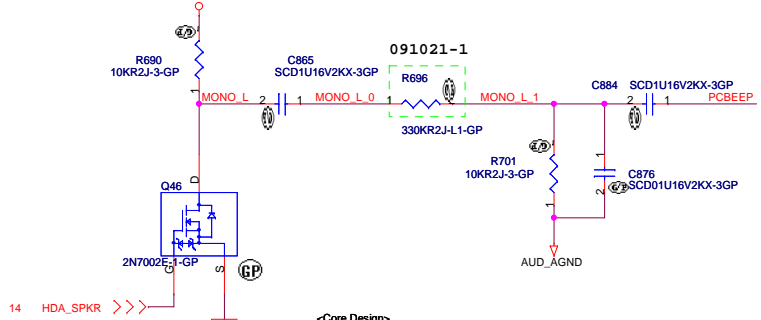
SENSE Detect



Digital GND & AUD_AGNND



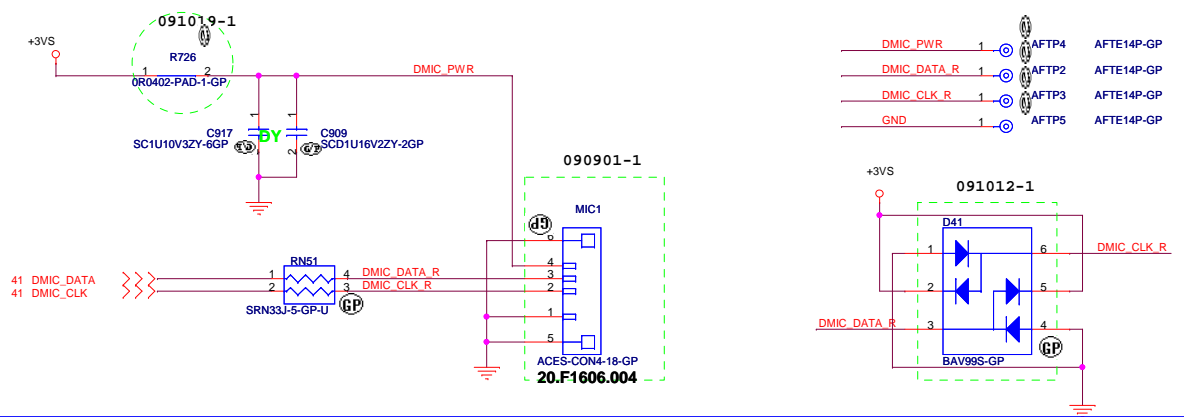
PC BEEP



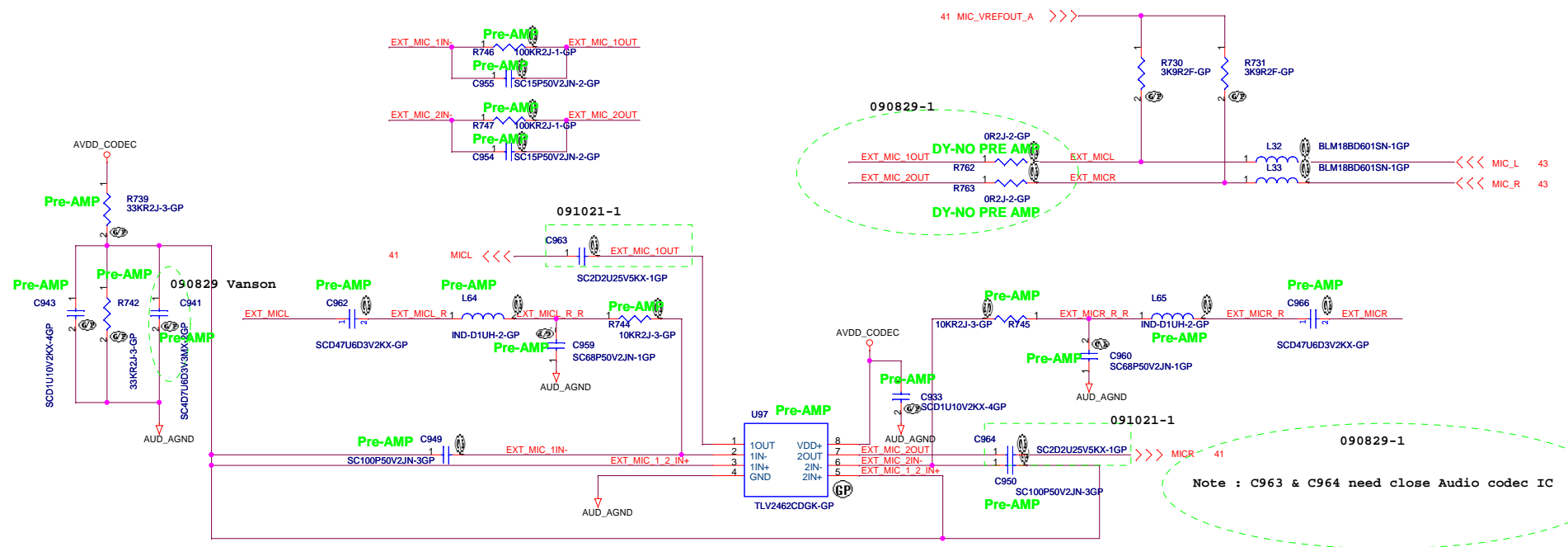
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Title			Rev
AUDIO 92HD80 / OP AMP			SD
Size	Document Number		
A3		S-Class Intel	
Date:	Wednesday, October 28, 2009	Sheet	41 of 62



Pre-AMP. for External MIC



<Core Design>

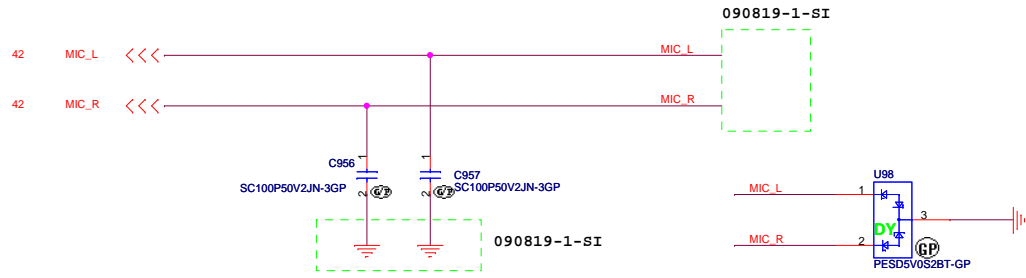
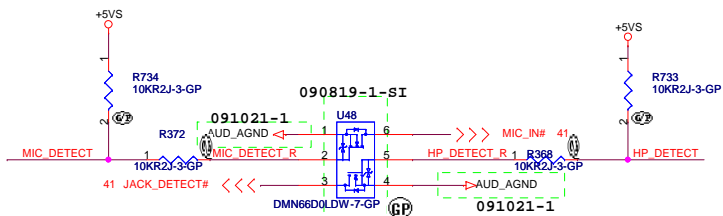
wistron Wistron Incorporated
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Title: **AUDIO Pre-AMP / CONN**

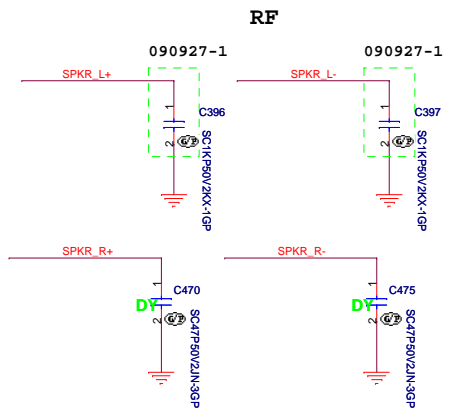
Size: A3 Document Number: **S-Class Intel** Rev: **SD**

Date: Wednesday, October 28, 2009 Sheet 42 of 62

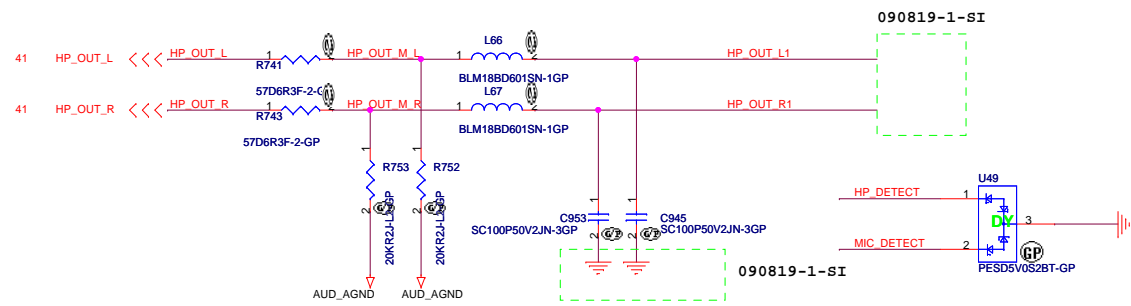
Jack Detect



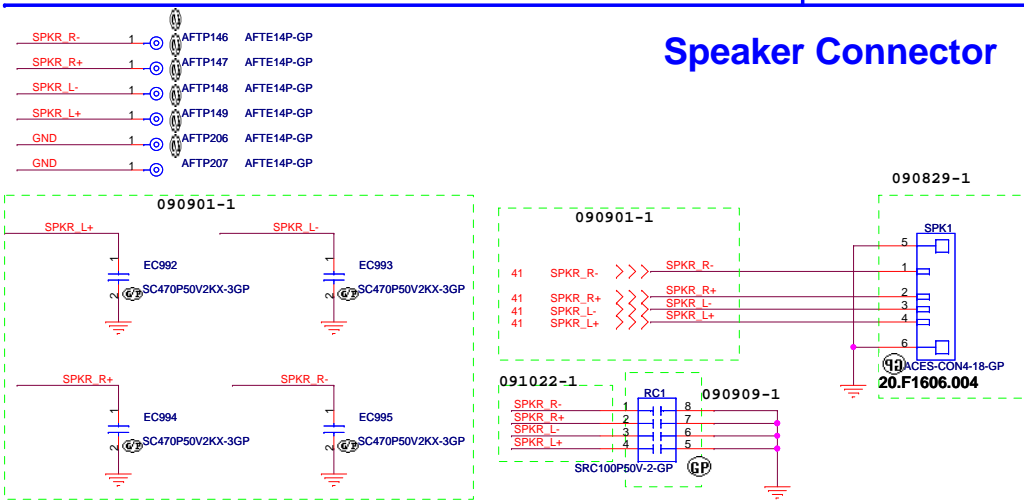
RF Reserver Cap



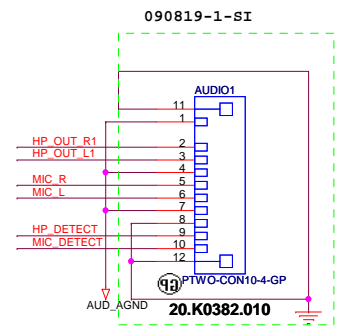
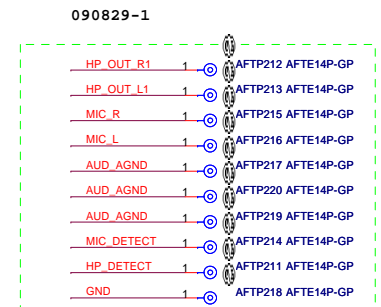
HeadPhone OUT



Speaker Connector



Audio Board Connector



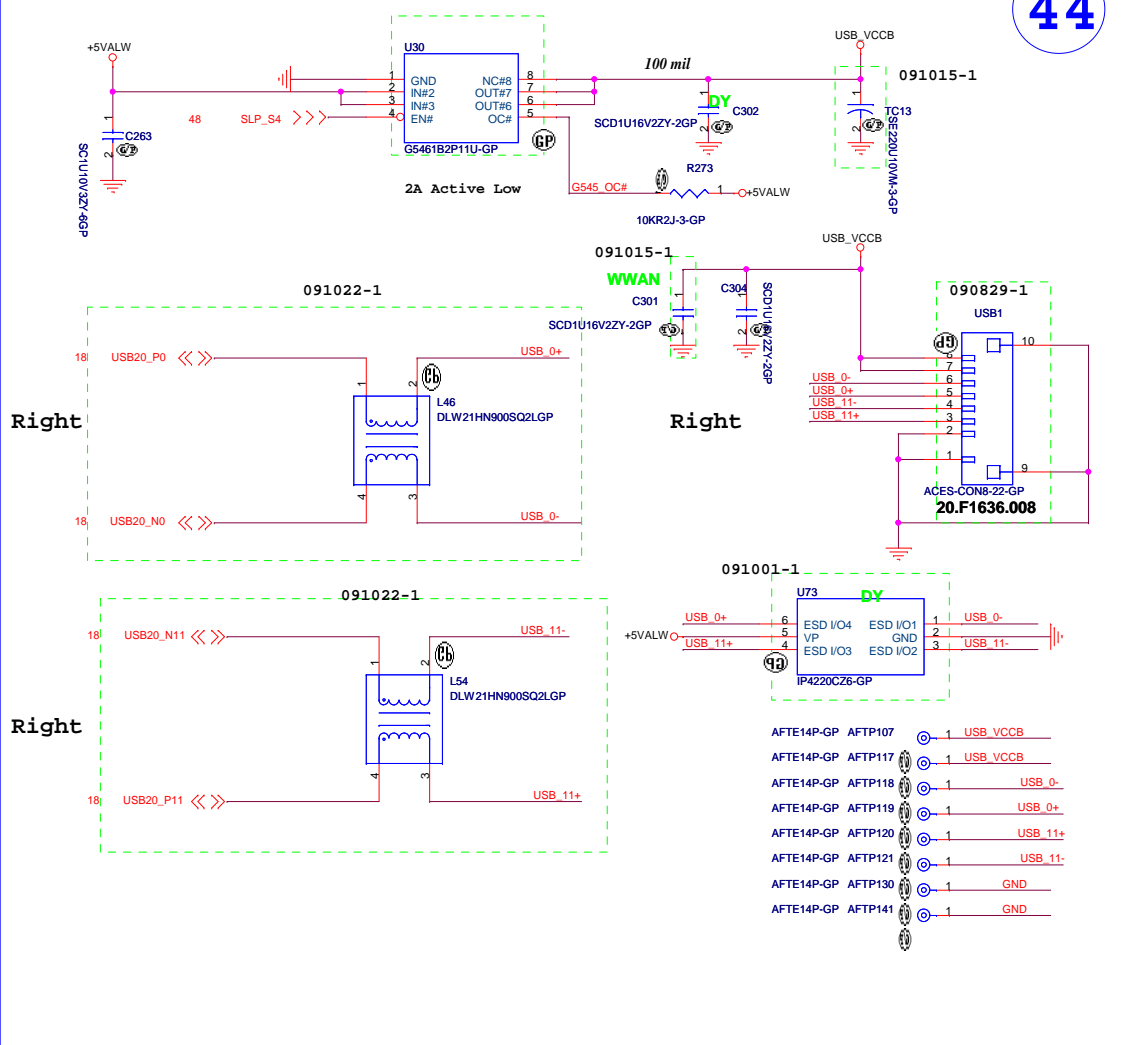
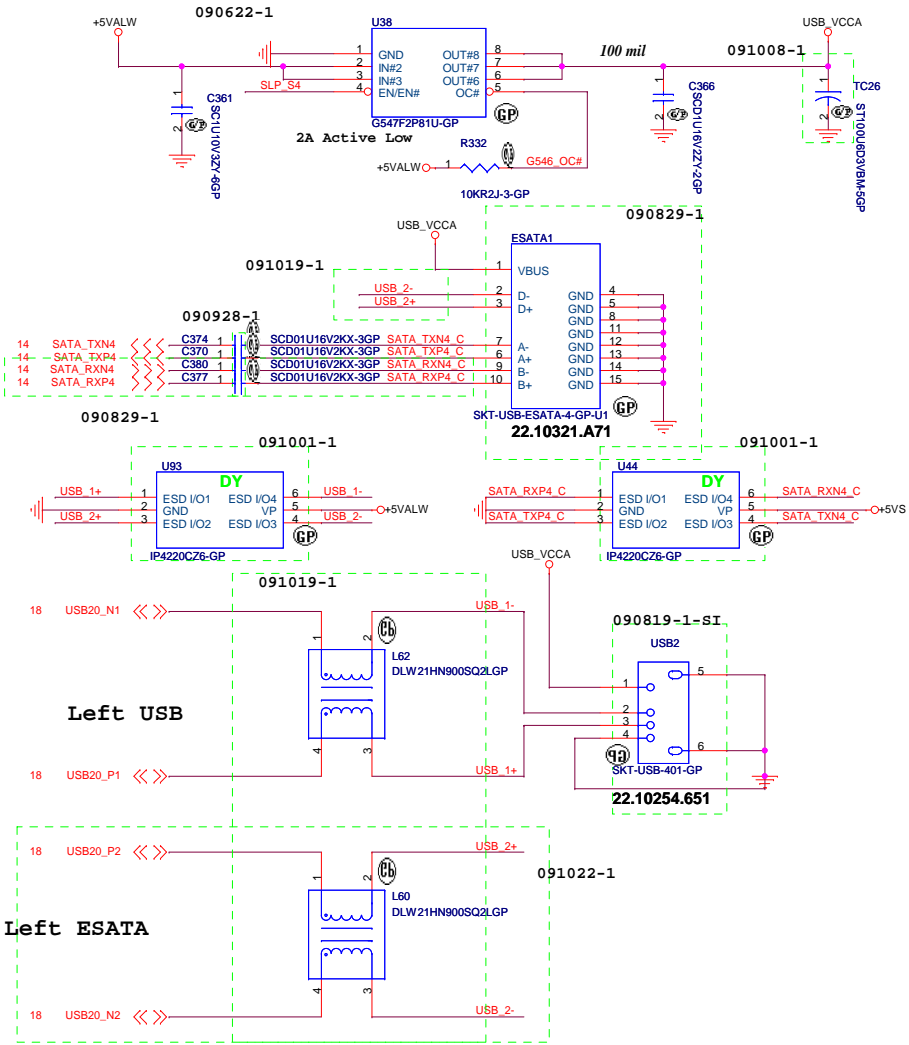
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Hsichih, Taipei

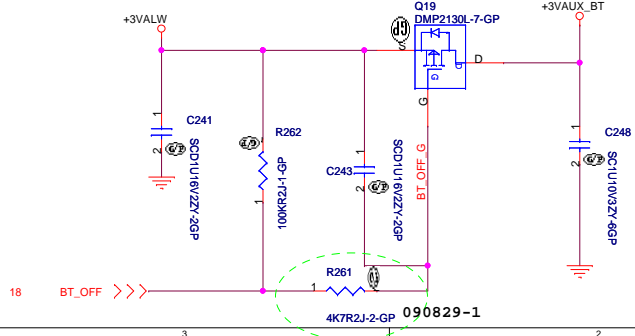
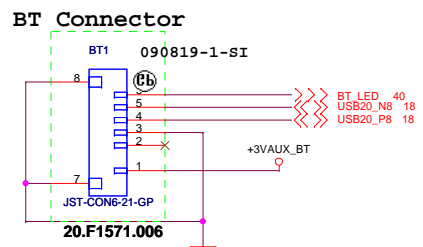
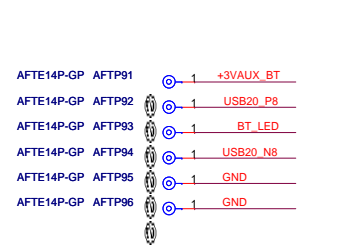
Title: **AUDIO Pre-AMP / CONN**

Size: A3 Document Number: **S-Class Intel** Rev: **SD**

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BT CONN.



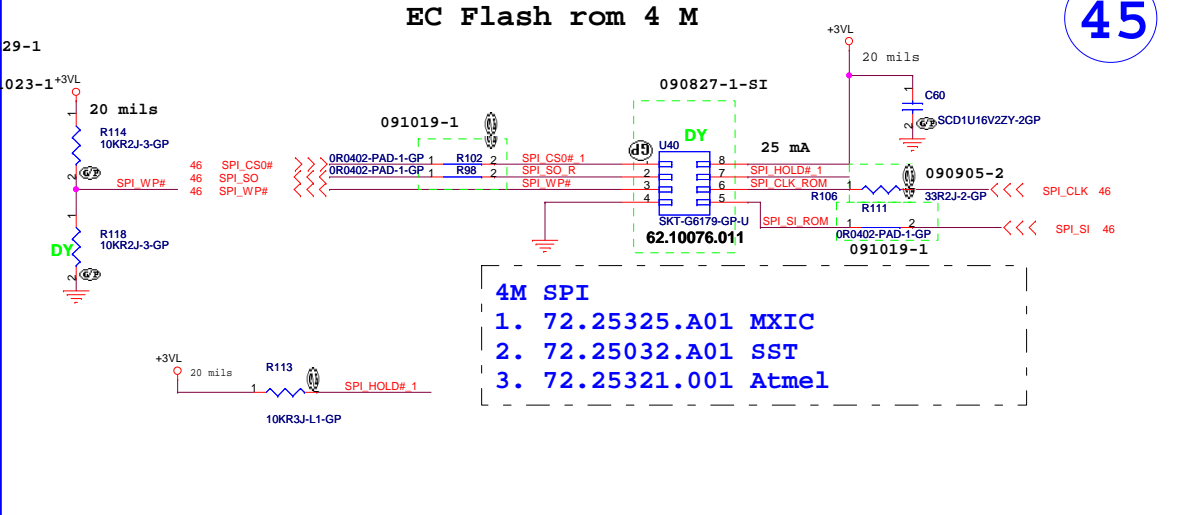
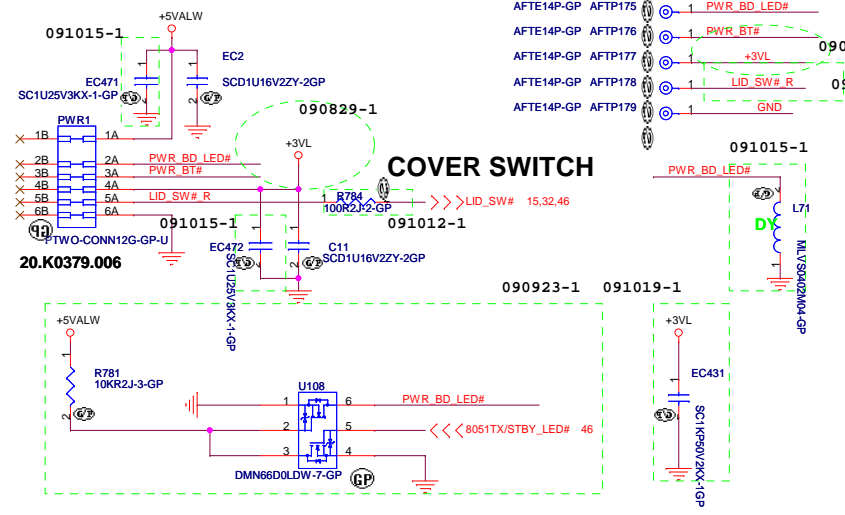
<Core Design>

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Hsichih, Taipei

Title: **USB / BT Connector**

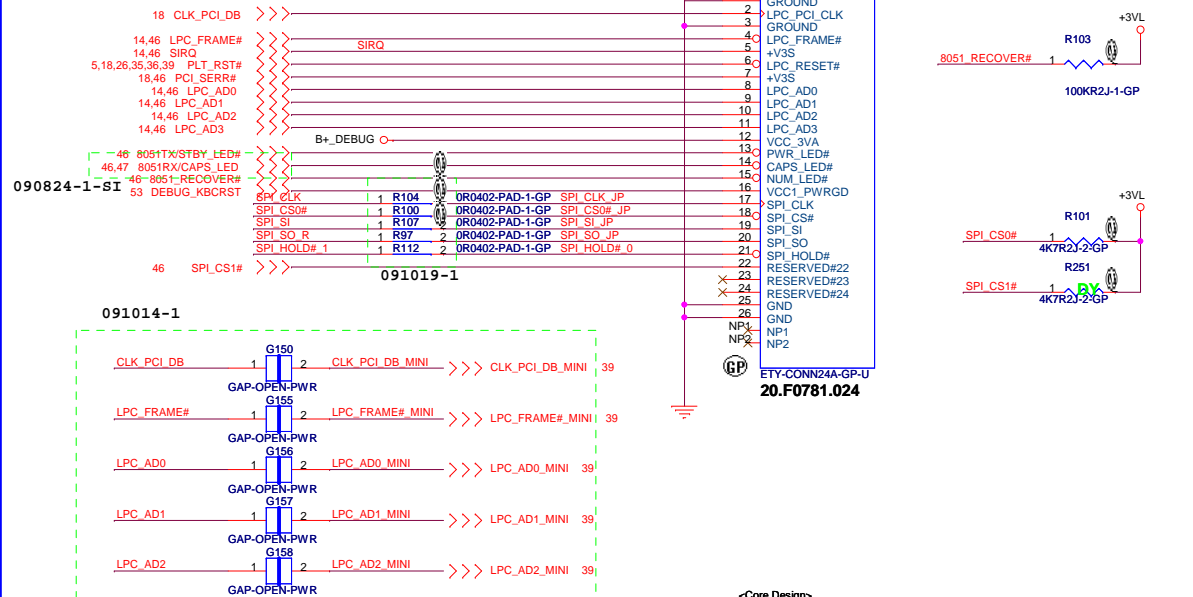
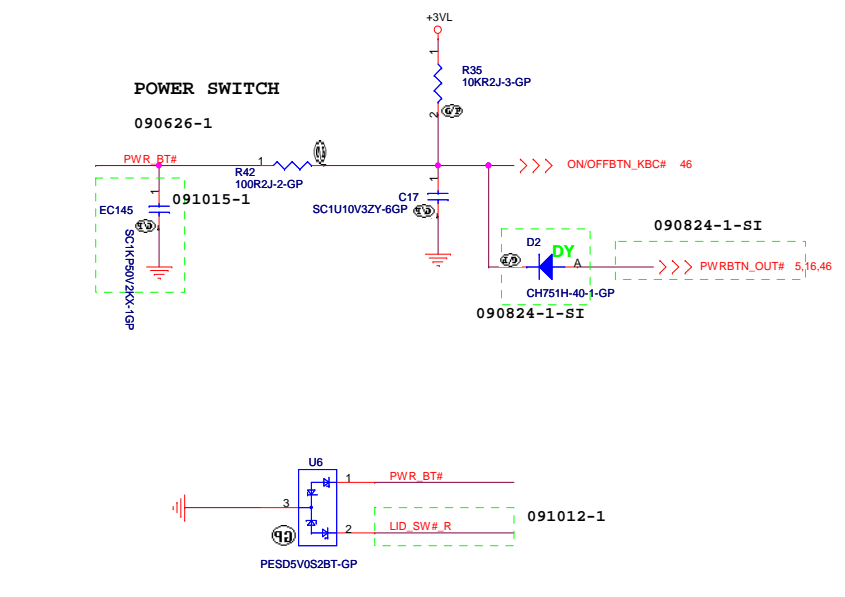
Size A3 Document Number: **S-Class Intel** Rev SD

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Power SW Circuit

24 PIN LPC DEBUG CONN.



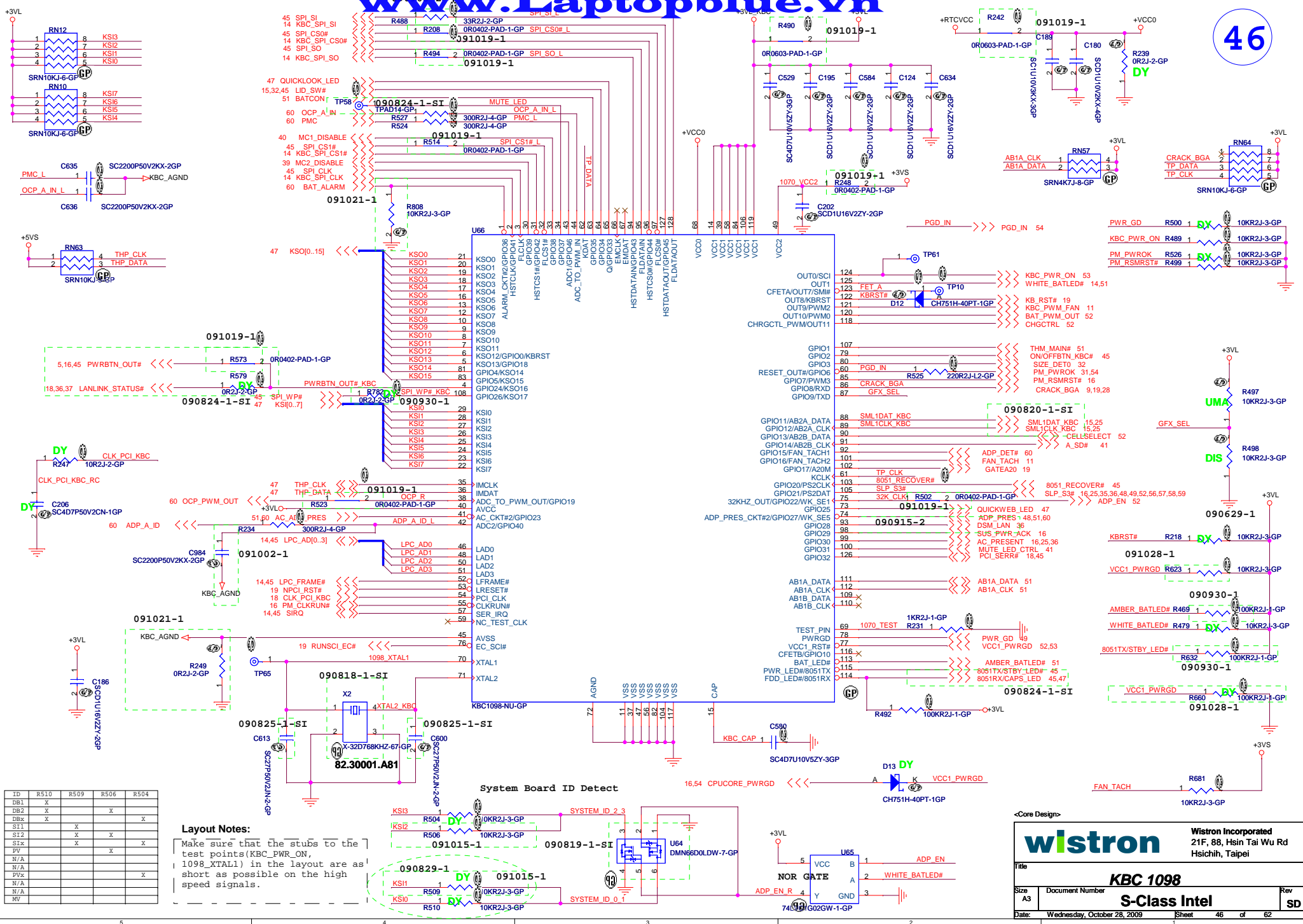
<Core Design>

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Hsichih, Taipei

Title: **FWH / BTN / DEBUG CONN.**

Size: A3 Document Number: **S-Class Intel** Rev: SD

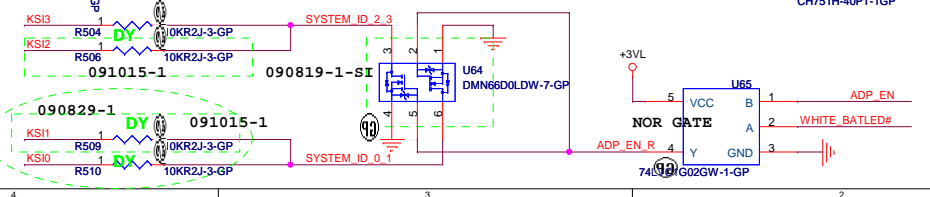
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ID	R510	R509	R506	R504
DB1	X		X	
DB2	X		X	
DBx	X		X	
SI1		X		X
SI2		X		X
SIx		X		X
PV			X	
N/A				X
PVx				X
N/A				X
N/A				X

Layout Notes:
 Make sure that the stubs to the test points (KBC_PWR_ON, 1098_XTAL1) in the layout are as short as possible on the high speed signals.

System Board ID Detect



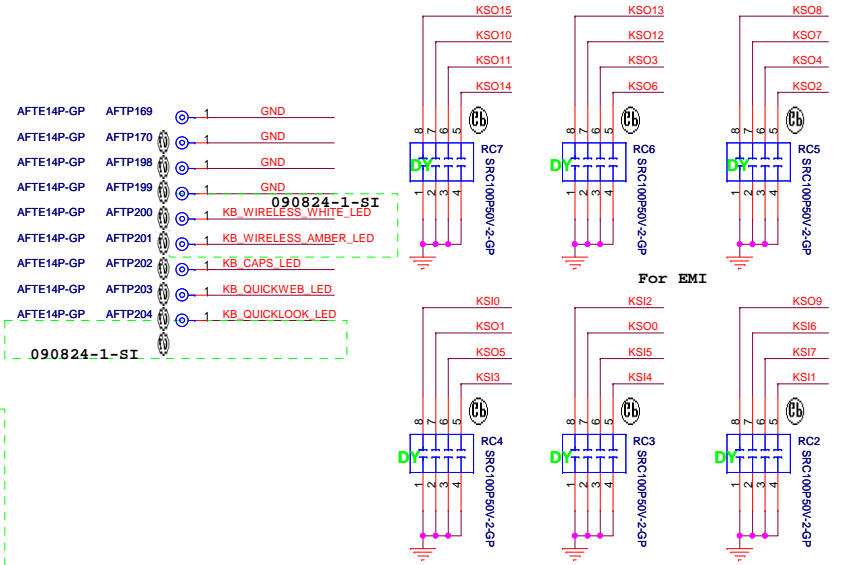
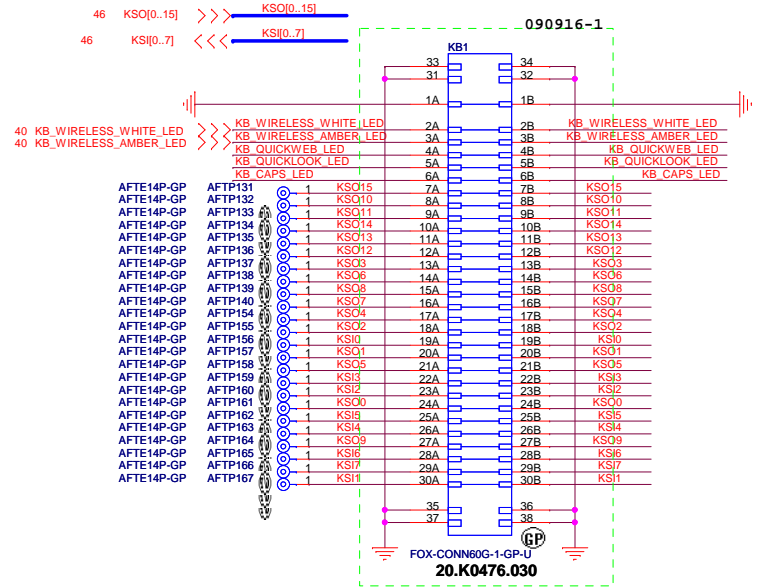
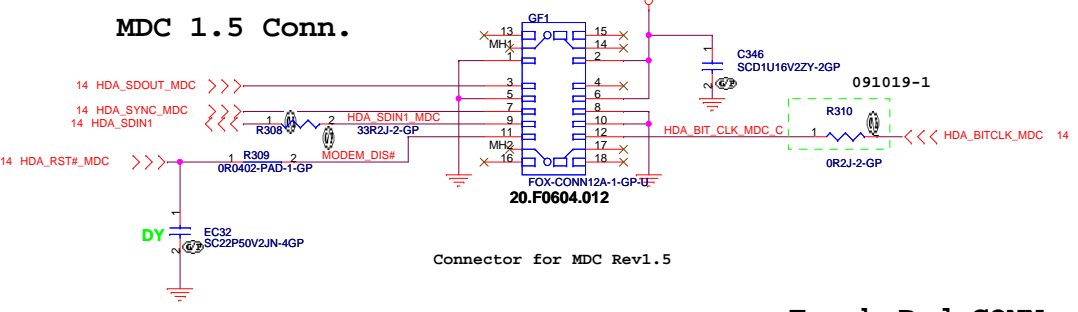
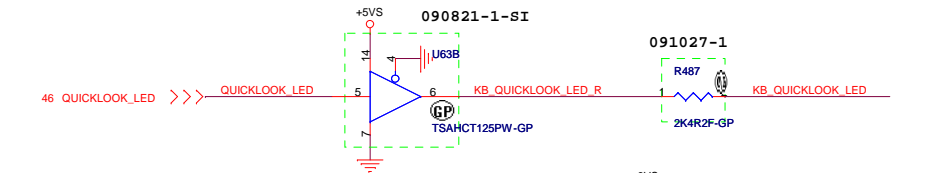
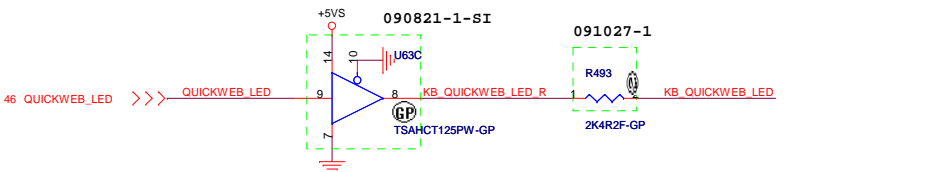
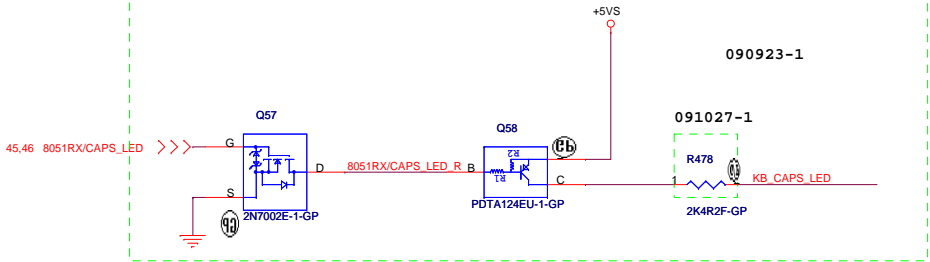
Core Design

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 Hsichih, Taipei

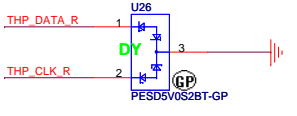
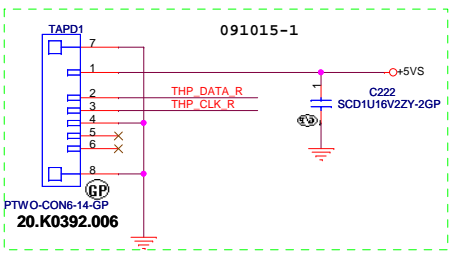
Title: **KBC 1098**

Size: A3 Document Number: **S-Class Intel** Rev: SD

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Touch_Pad CONN.



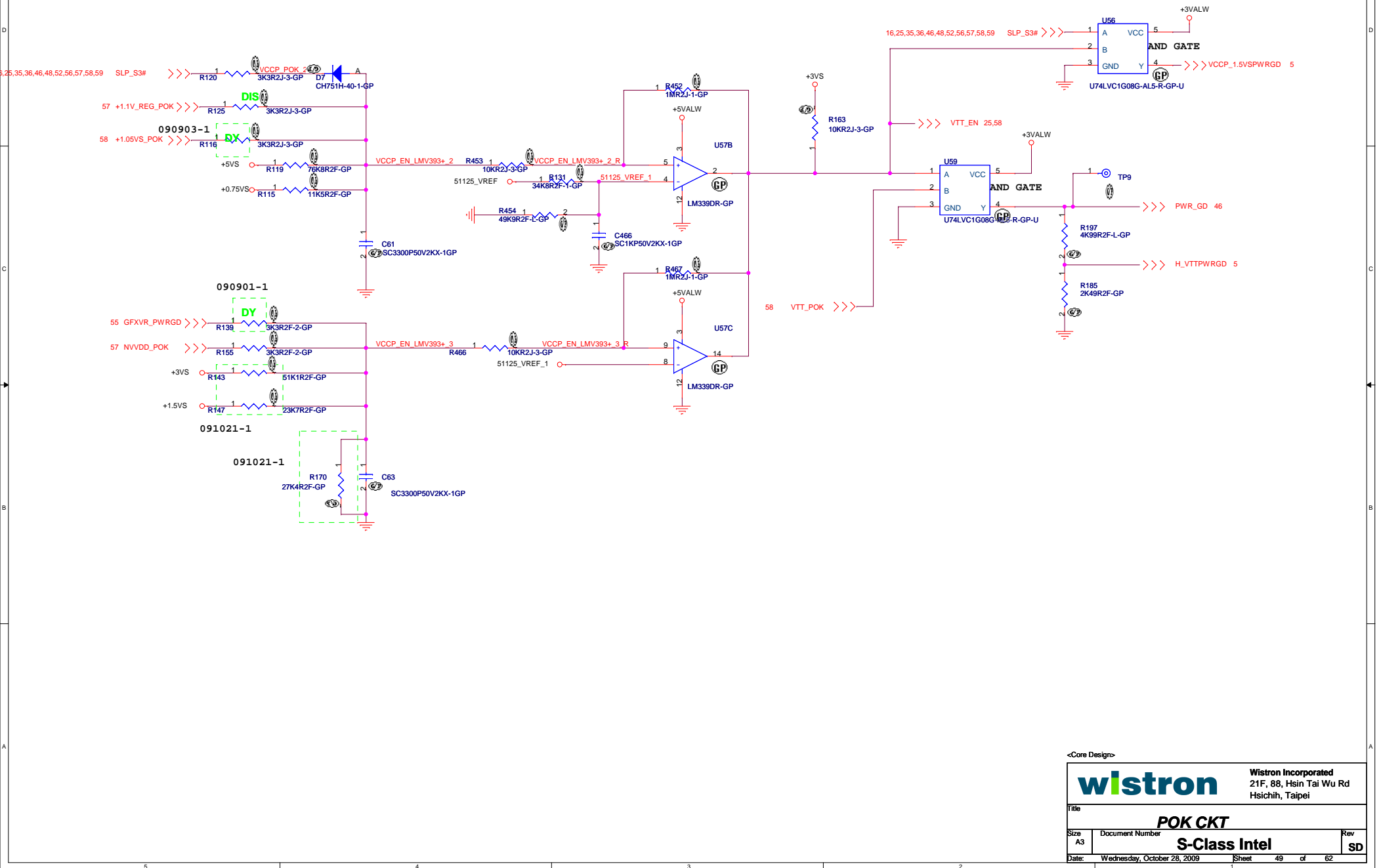
<Core Design>

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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: **MDC/KBD/ON OFF/T.P.**

Size: A3 Document Number: **S-Class Intel** Rev: **SD**

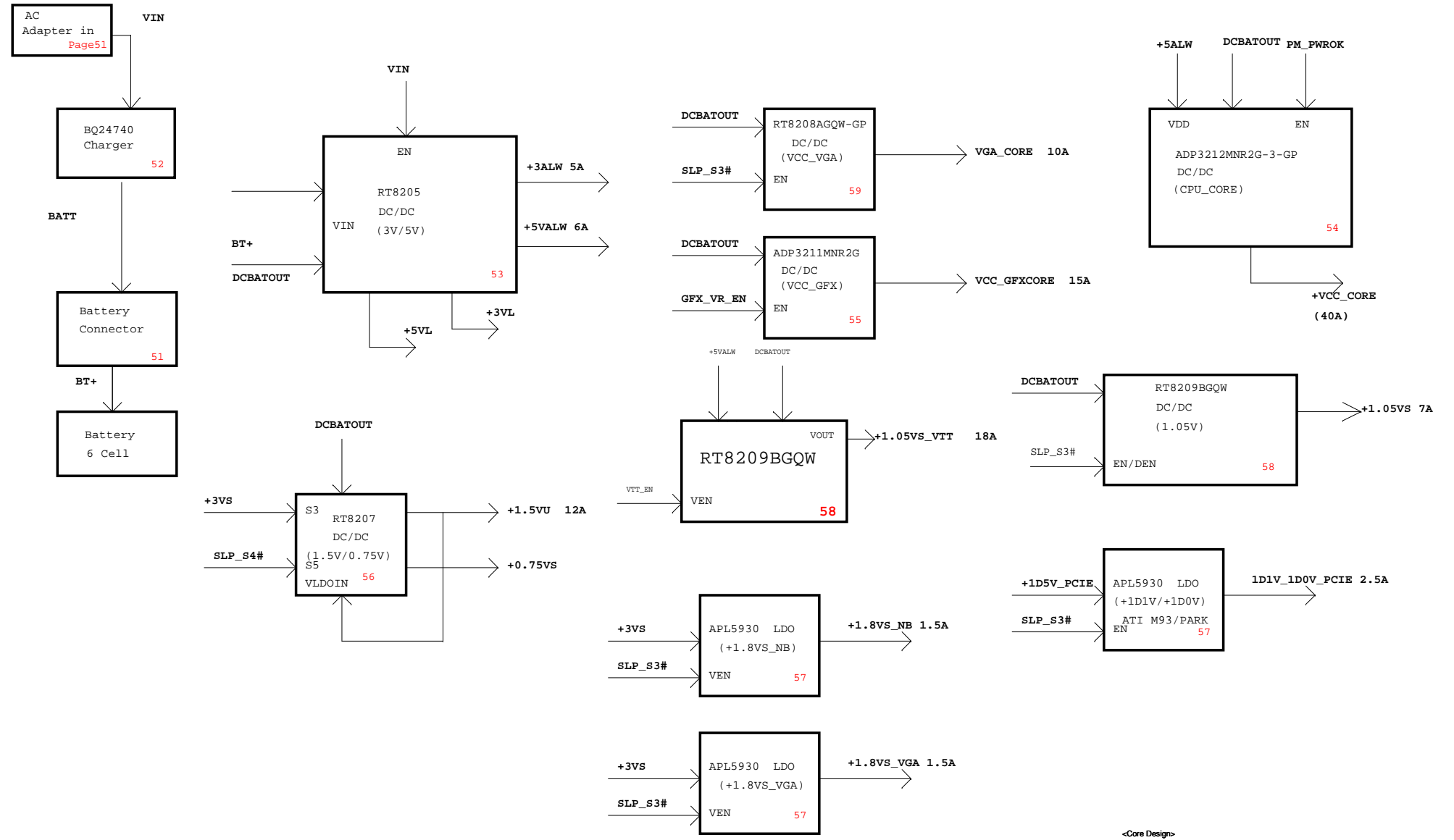
Date: Wednesday, October 28, 2009 Sheet: 47 of 62

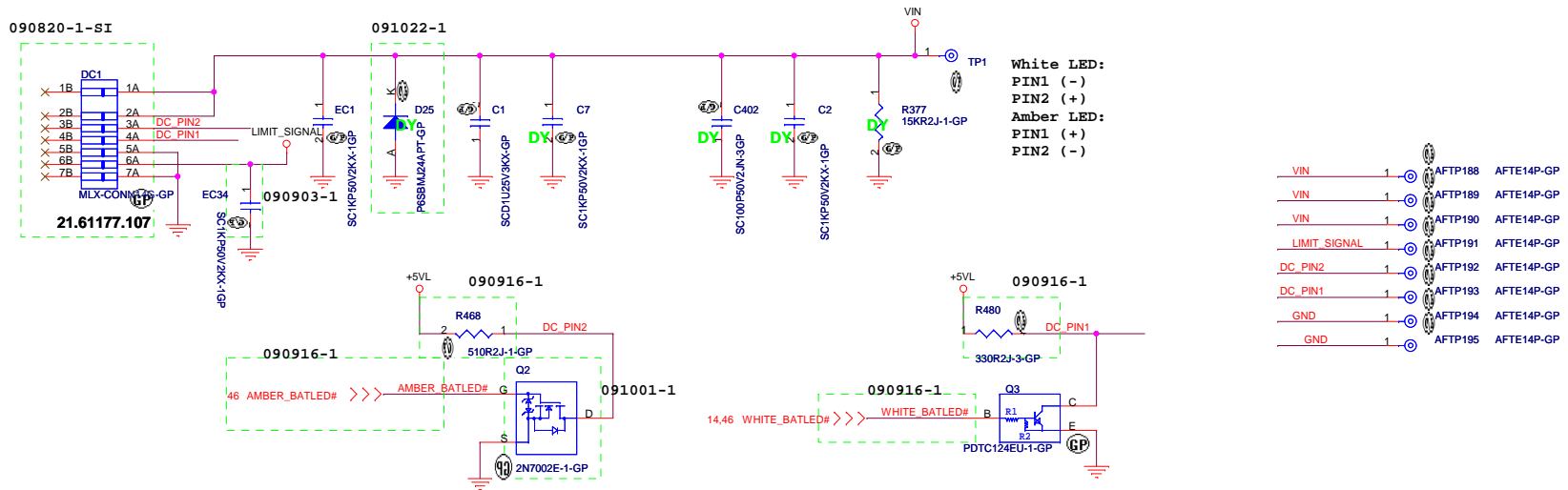


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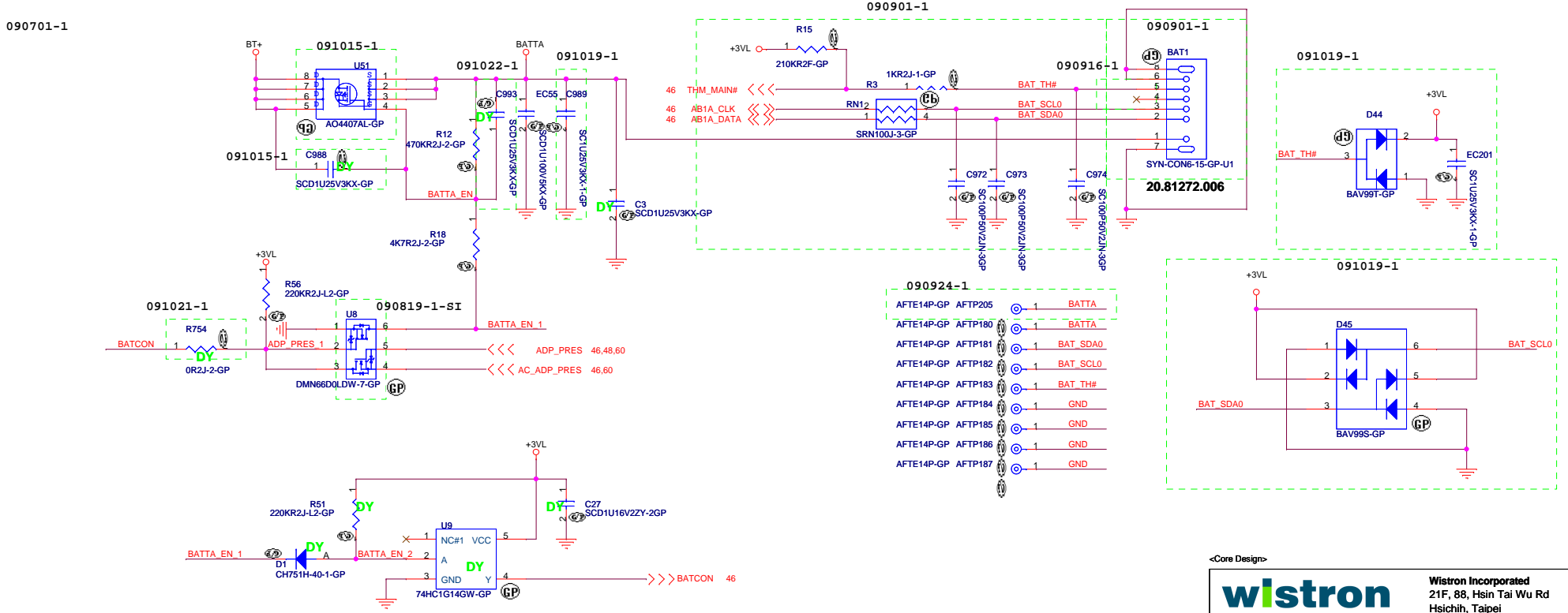
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Hsichih, Taipei

Title	POK CKT		Rev
Size	Document Number	S-Class Intel	SD
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BATTERY CONNECTOR



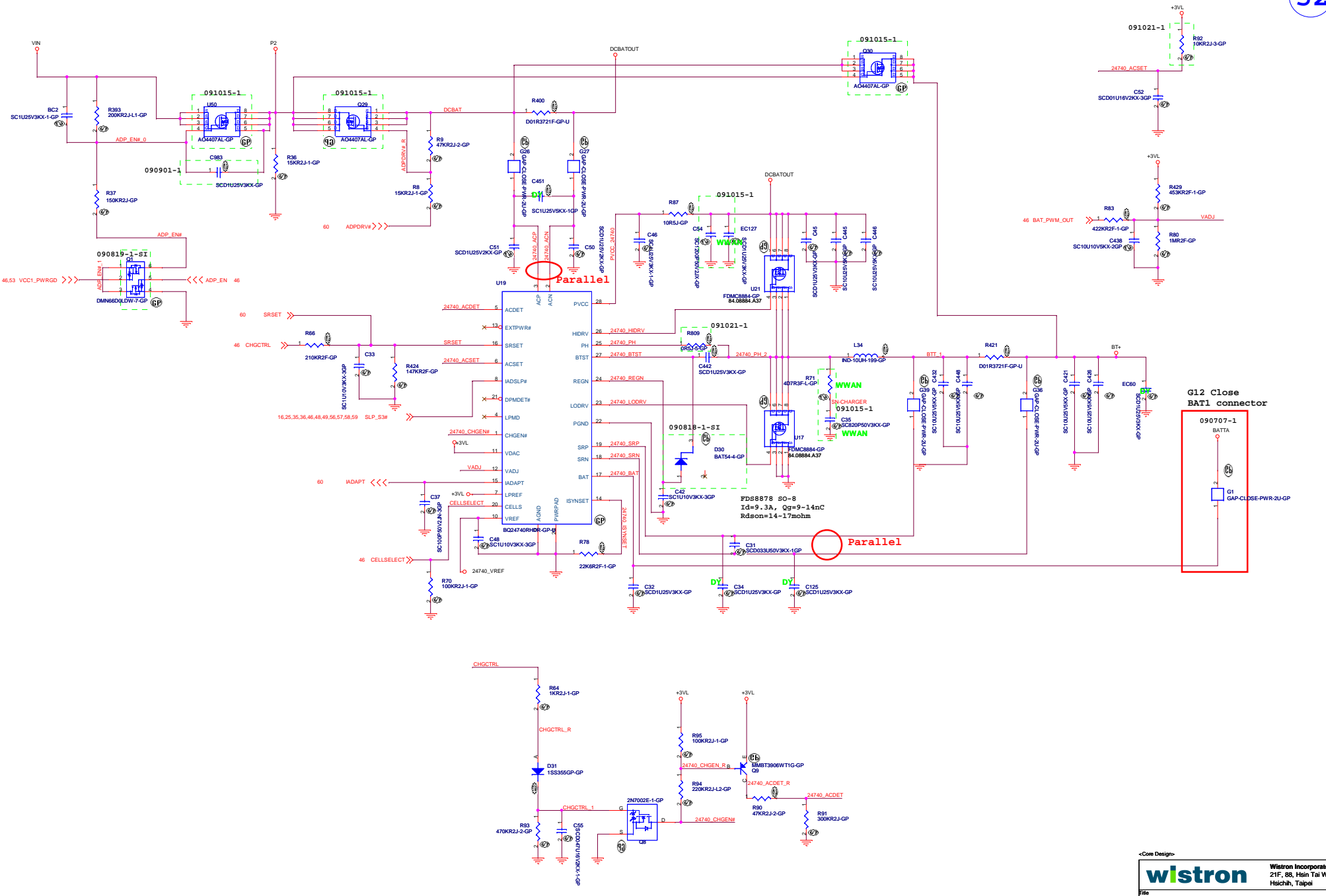
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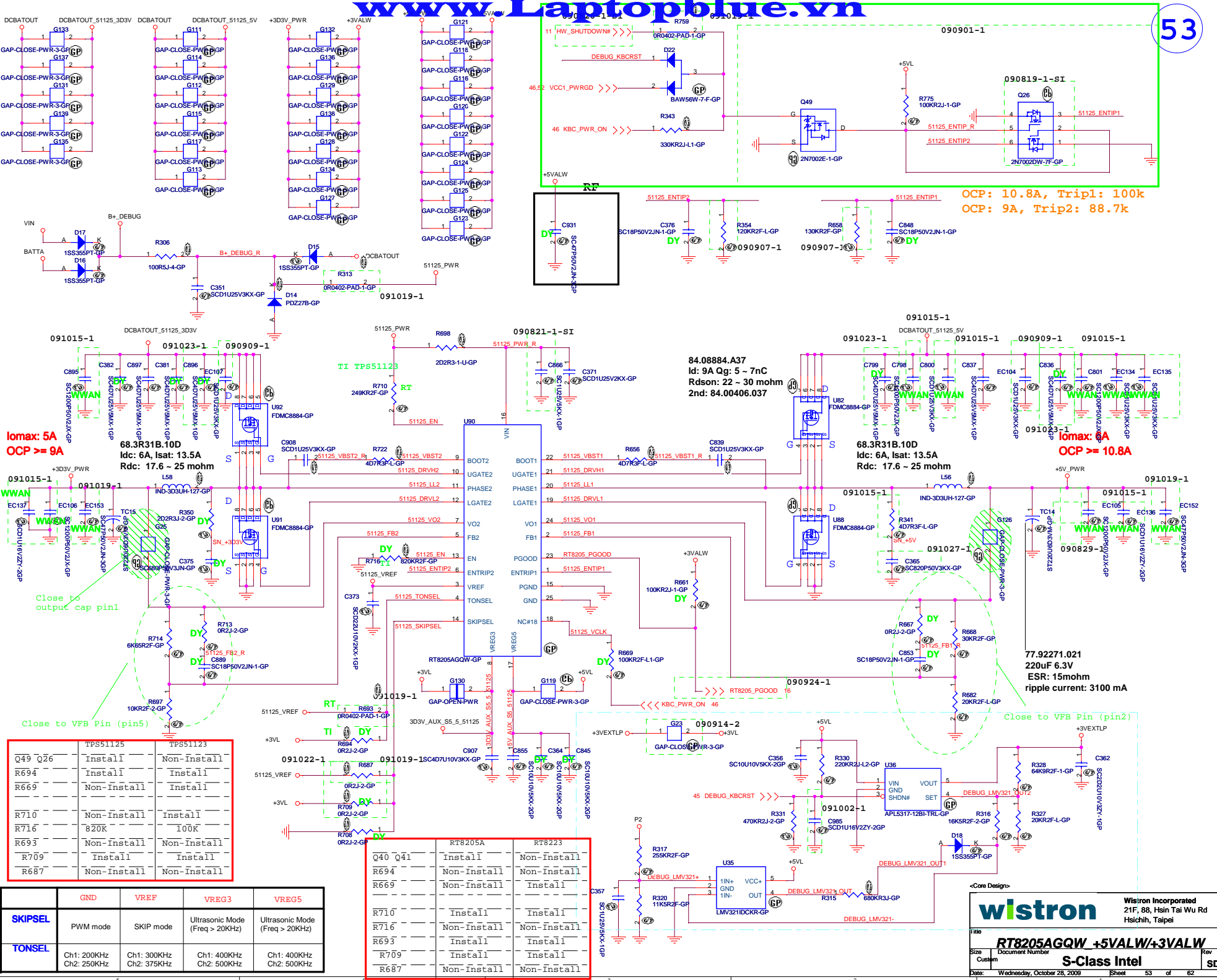
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Title: **DC & BATTERY CONN.**

Size: Document Number: **S-Class Intel** Rev: **SD**

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Iomax: 5A
OCP >= 9A

Close to output cap pin1

Close to VFB Pin (pin5)

	TPS51125	TPS51123
Q49 Q26	Install	Non-Install
R694	Install	Install
R669	Non-Install	Install
R710	Non-Install	Install
R716	820K	100K
R693	Non-Install	Non-Install
R709	Install	Install
R687	Non-Install	Non-Install

	GND	VREF	VREG3	VREG5
SKIPSEL	PWM mode	SKIP mode	Ultrasonic Mode (Freq > 20KHz)	Ultrasonic Mode (Freq > 20KHz)
TONSEL	Ch1: 200KHz Ch2: 250KHz	Ch1: 300KHz Ch2: 375KHz	Ch1: 400KHz Ch2: 500KHz	Ch1: 400KHz Ch2: 500KHz

	RT8205A	RT8223
Q40 Q41	Install	Non-Install
R694	Non-Install	Non-Install
R669	Non-Install	Install
R710	Install	Install
R716	Non-Install	Non-Install
R693	Install	Install
R709	Install	Install
R687	Non-Install	Non-Install

84.08884.A37
Id: 9A Qg: 5 ~ 7nC
Rds(on): 22 ~ 30 mOhm
2nd: 84.00406.037

68.3R31B.10D
Idc: 6A, Isat: 13.5A
Rdc: 17.6 ~ 25 mOhm

Iomax: 5A
OCP >= 10.8A

77.92271.021
220uF 6.3V
ESR: 15mohm
ripple current: 3100 mA

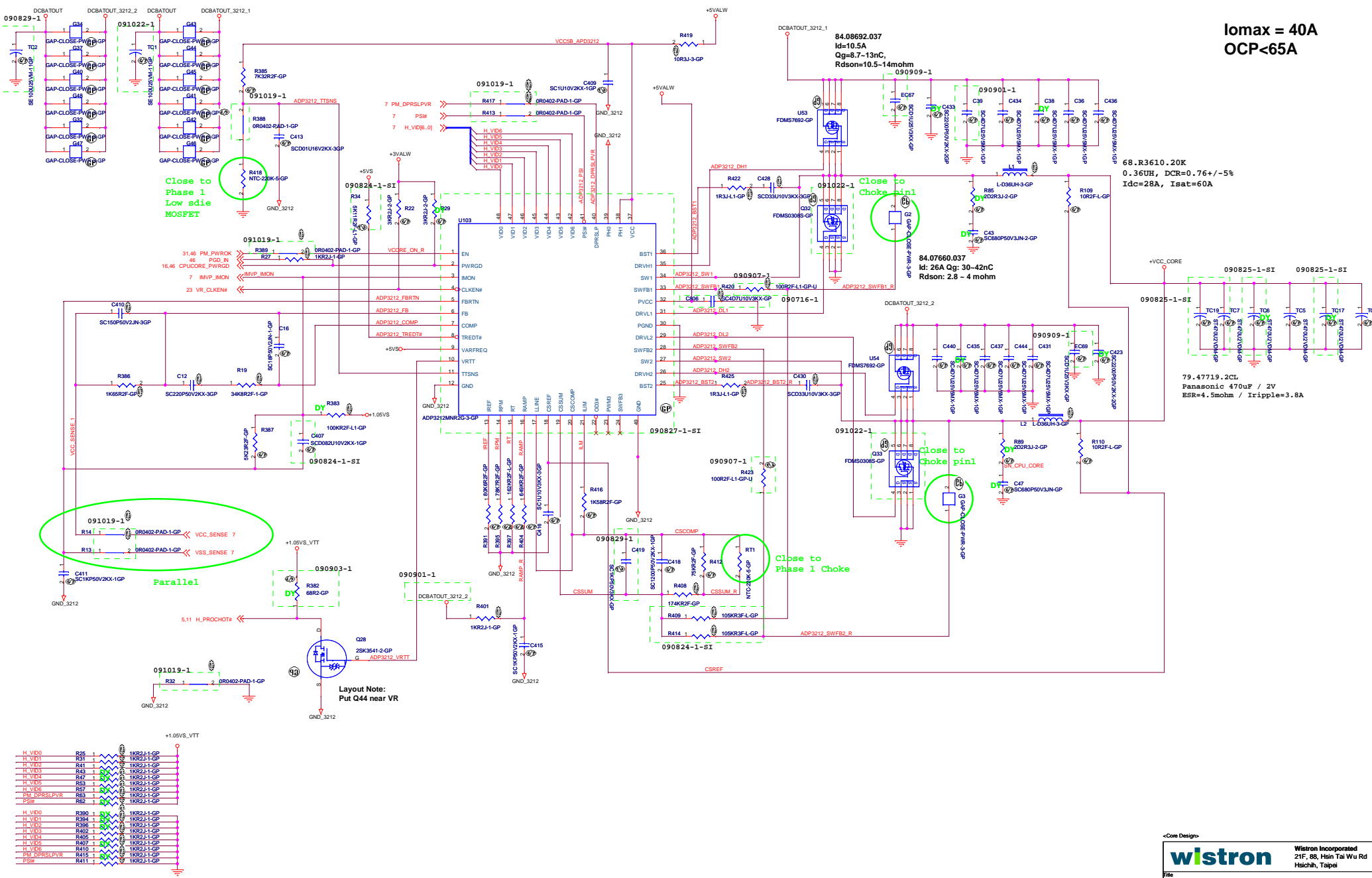
OCP: 10.8A, Trip1: 100k
OCP: 9A, Trip2: 88.7k

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Part: **RT8205AGQW +5VALW/+3VALW**
S-Class Intel

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Iomax = 40A
OCP<65A



Close to Phase 1 Low side MOSFET

Close to Choke pin1

Close to Phase 1 Choke

Parallel

Layout Note:
Put Q44 near VR

68.R3610.20K
0.36uH, DCR=0.76+/-5%
Idc=28A, Isat=60A

79.47719.2CL
Panasonic 470uF / 2V
ESR=4.5mohm / Ripple=3.8A

H_VDD9	R25	1KR21-L-GP
H_VDD1	R41	1KR21-L-GP
H_VDD3	R43	1KR21-L-GP
H_VDD4	R47	1KR21-L-GP
H_VDD5	R53	1KR21-L-GP
H_VDD6	R57	1KR21-L-GP
H_VDD8	R63	1KR21-L-GP
PM_DPRSPLVPR	R62	1KR21-L-GP
PSW	R62	1KR21-L-GP
H_VDD9	R380	1KR21-L-GP
H_VDD1	R384	1KR21-L-GP
H_VDD2	R386	1KR21-L-GP
H_VDD3	R402	1KR21-L-GP
H_VDD4	R405	1KR21-L-GP
H_VDD5	R407	1KR21-L-GP
H_VDD6	R410	1KR21-L-GP
H_VDD8	R415	1KR21-L-GP
PM_DPRSPLVPR	R411	1KR21-L-GP
PSW	R411	1KR21-L-GP

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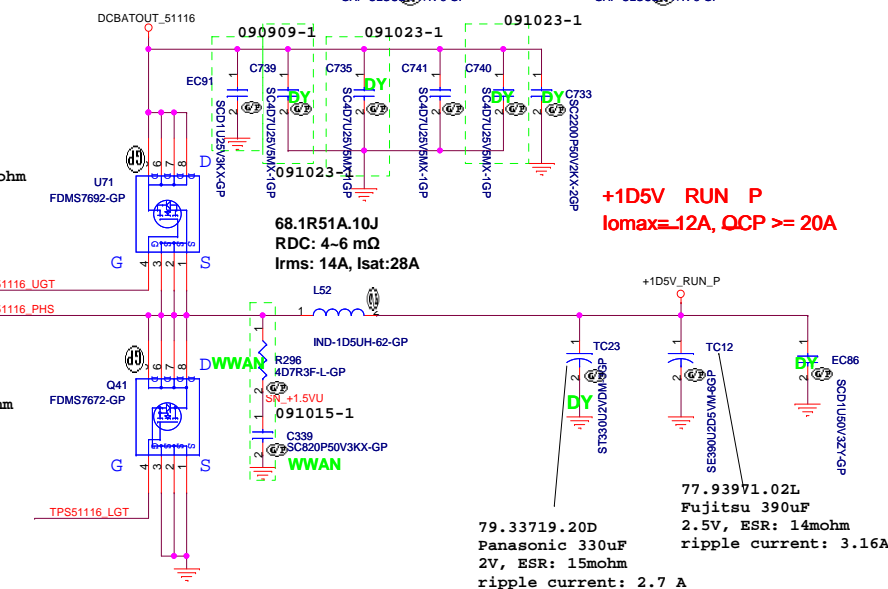
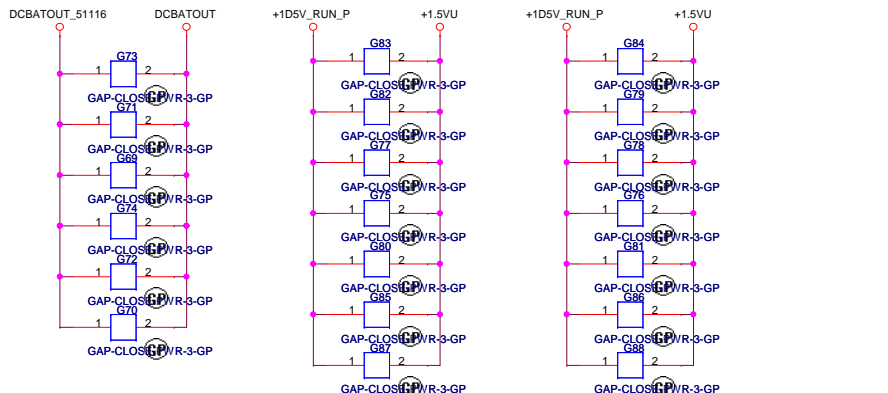
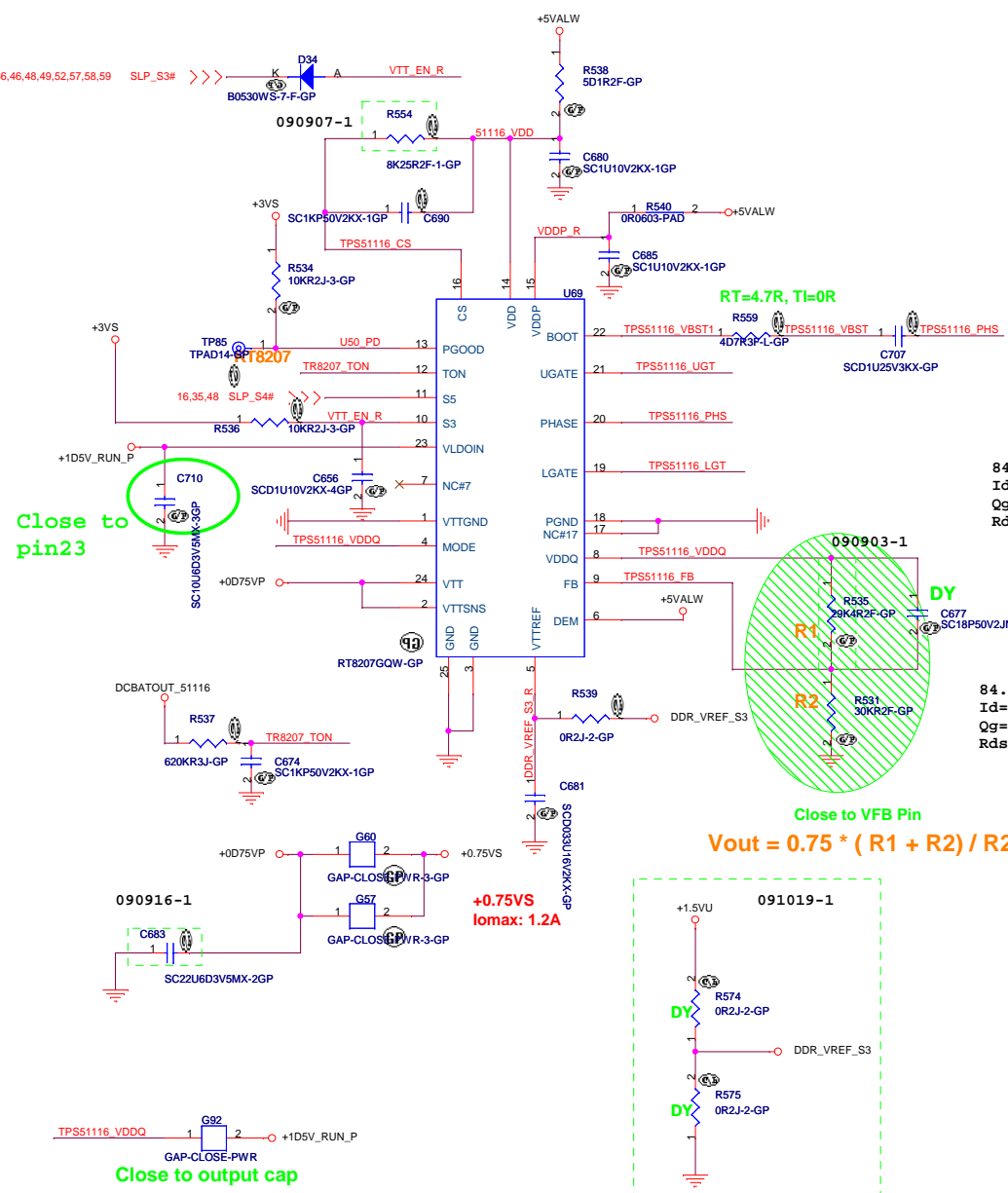
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File: **ADP3212MNR2G CPU CORE**

Size: A2 Document Number: **S-Class Intel** Rev: SD

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RT8207 for 1D5V and 0D75V



$V_{out} = 0.75 * (R1 + R2) / R2$

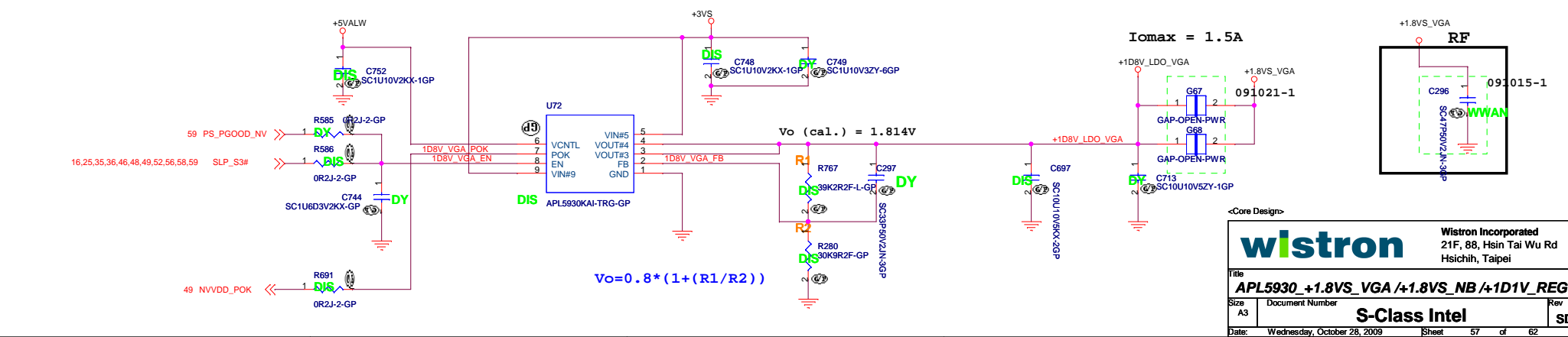
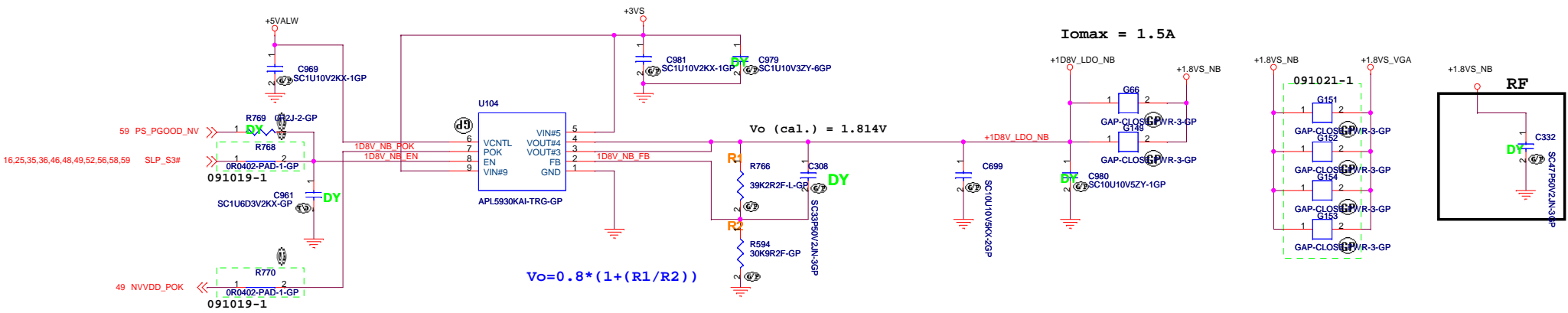
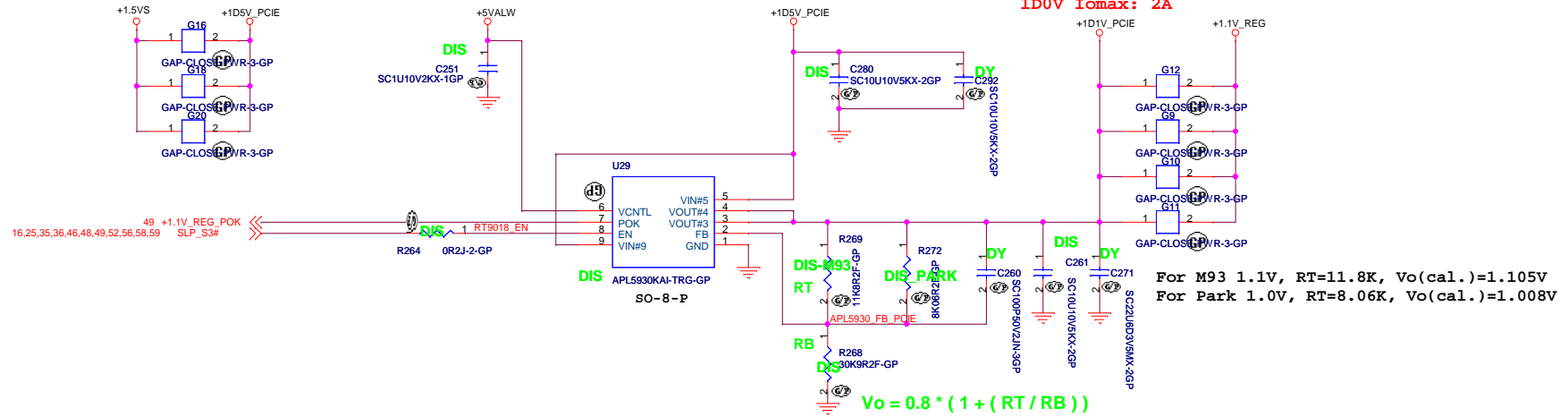
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Hsichih, Taipei

Title: **RT8207GQW +1.5VU / +0.75VS**

Size: A3 Document Number: **S-Class Intel** Rev: SD

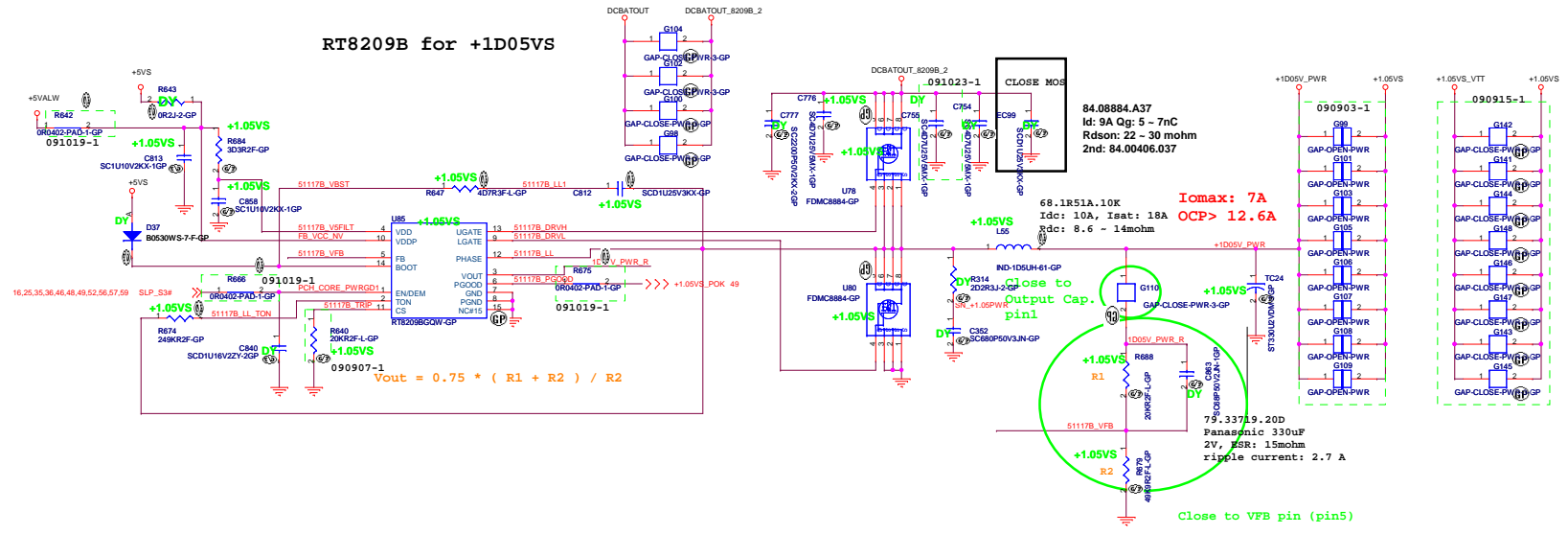
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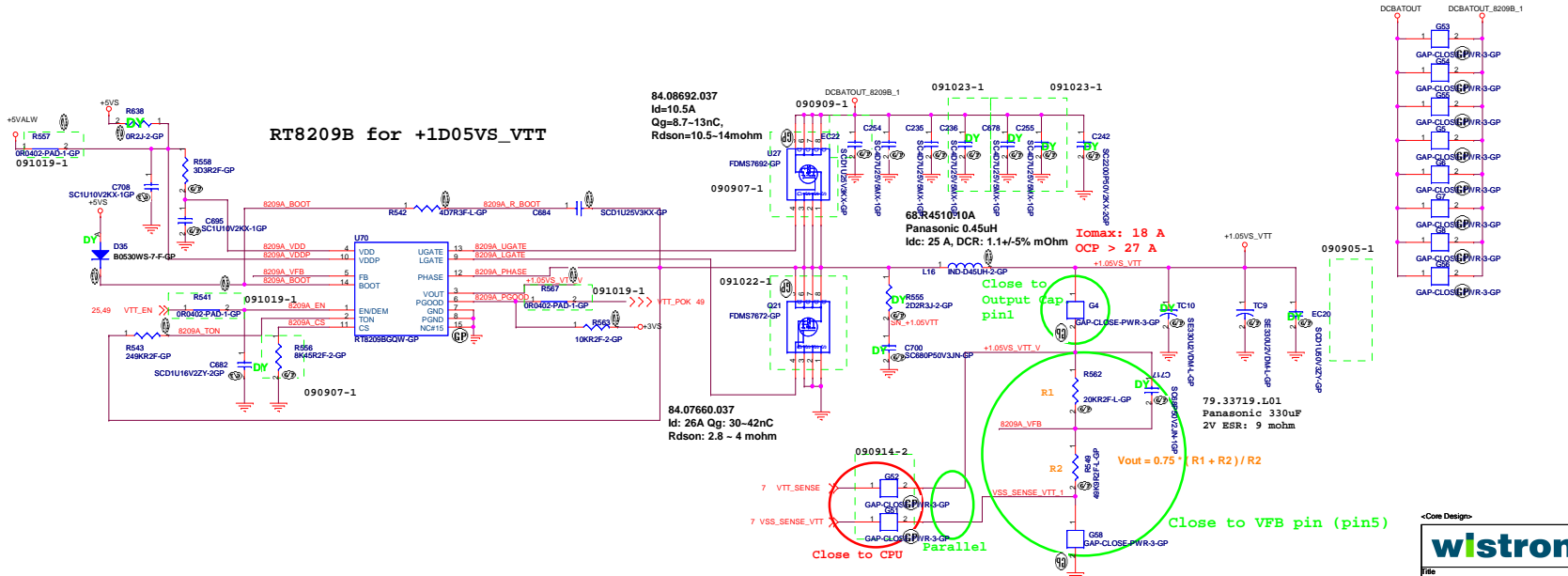
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 Hsichih, Taipei

Title: **APL5930 +1.8VS_VGA /+1.8VS_NB /+1D1V_REG**
 Size: A3 Document Number: **S-Class Intel** Rev: SD
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RT8209B for +1D05VS



RT8209B for +1D05VS_VTT



<Core Design>

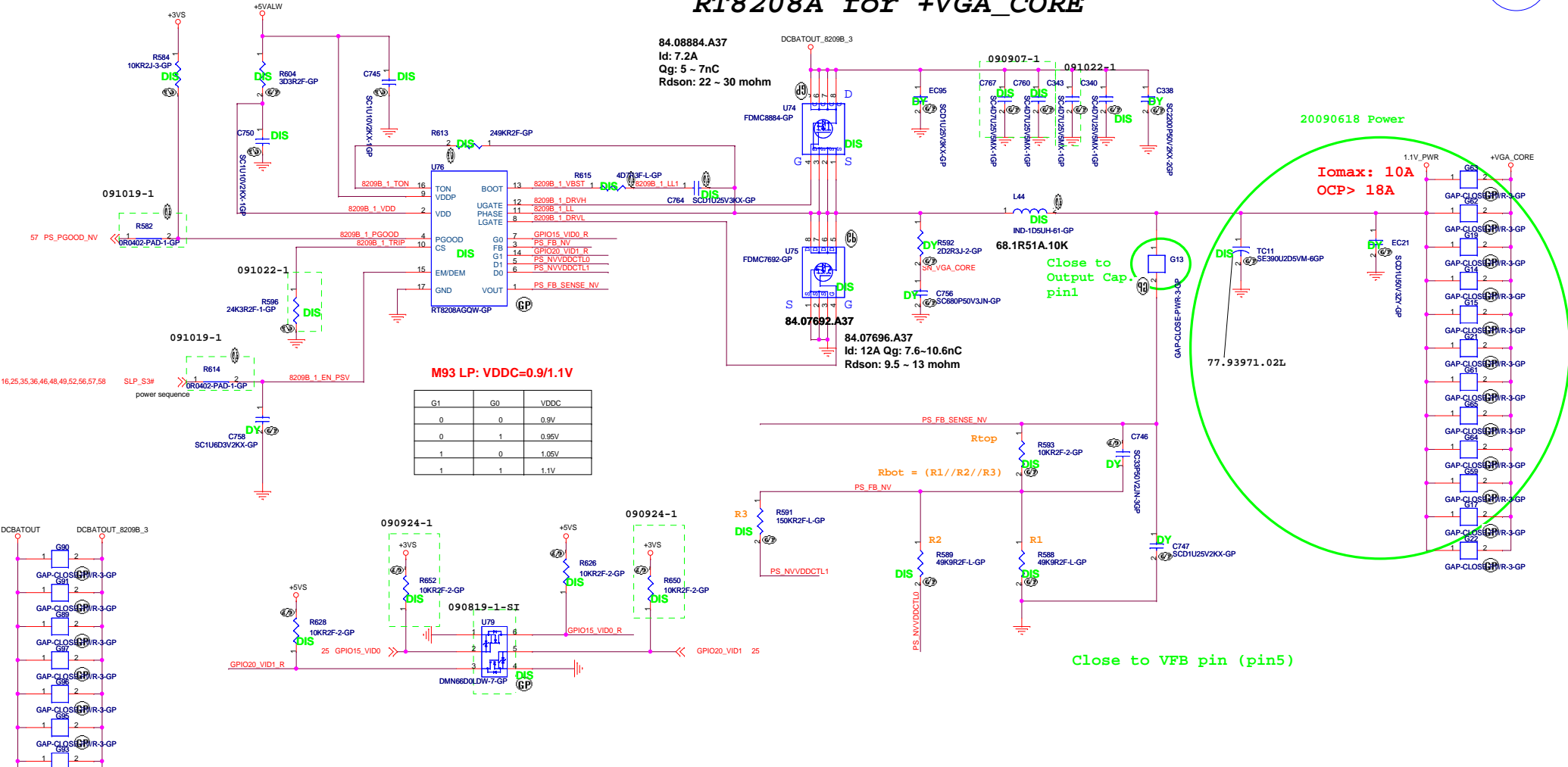
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File: RT8209B +1.05VS_VTT +1.05VS

Rev: SD

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RT8208A for +VGA_CORE

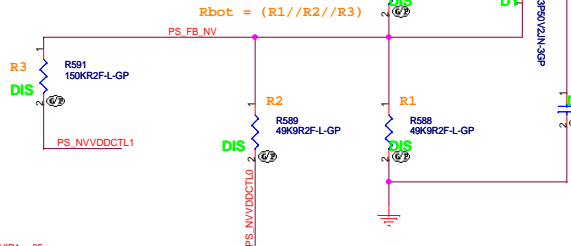


84.08884.A37
 Id: 7.2A
 Qg: 5 ~ 7nC
 Rds(on): 22 ~ 30 mOhm

84.07692.A37
 Id: 12A Qg: 7.6~10.6nC
 Rds(on): 9.5 ~ 13 mOhm

M93 LP: VDDC=0.9/1.1V

G1	G0	VDDC
0	0	0.9V
0	1	0.95V
1	0	1.05V
1	1	1.1V



$+VCC_GFX_CORE = (1 + R_t / R_b) \times 0.75$

+VCC_GFX_CORE	RTop	RBot	GPIO15_VID0_R	GPIO20_VID1_R	ideal voltage	actual voltage
0.9v	10k	R1 49.9k	LOW	LOW	0.9003	
0.95v	10k	R1 49.9k // R2 49.9k	LOW	HIGH	0.9493	
1.05v	10k	R1 49.9k // R3 150k	HIGH	LOW	1.0506	
1.1v	10k	R1 49.9k // R2 49.9k // R3 150k	HIGH	HIGH	1.0997	

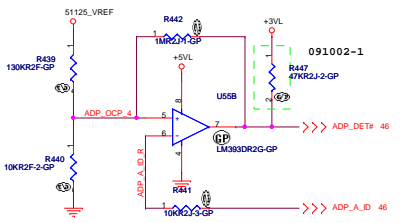
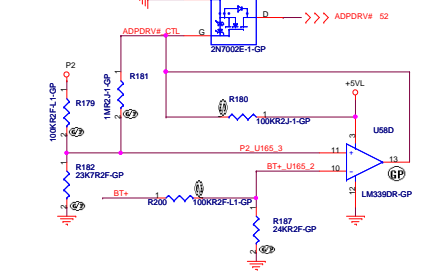
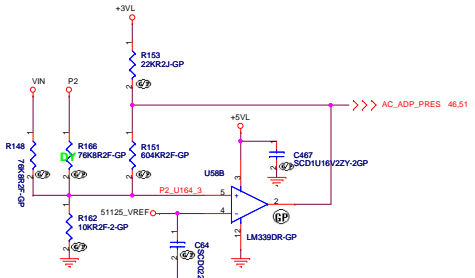
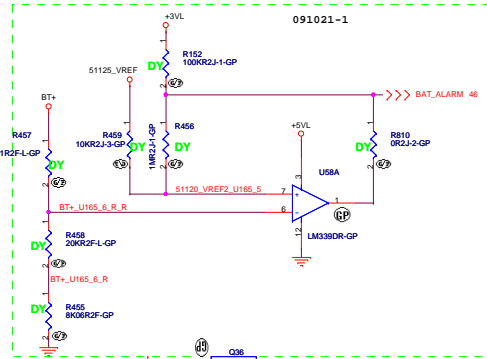
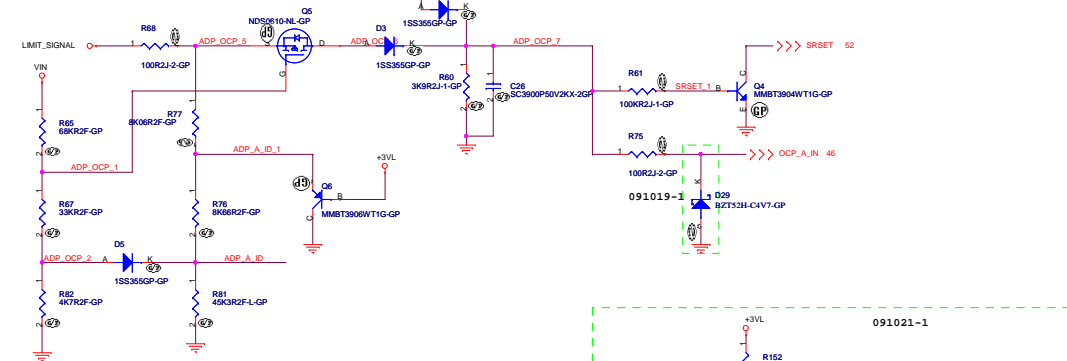
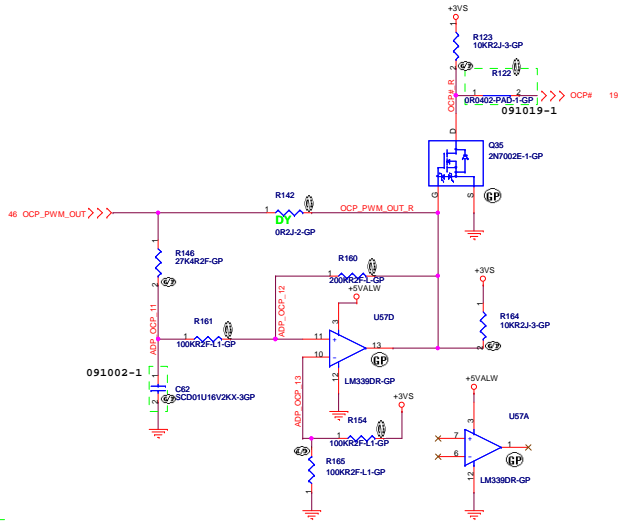
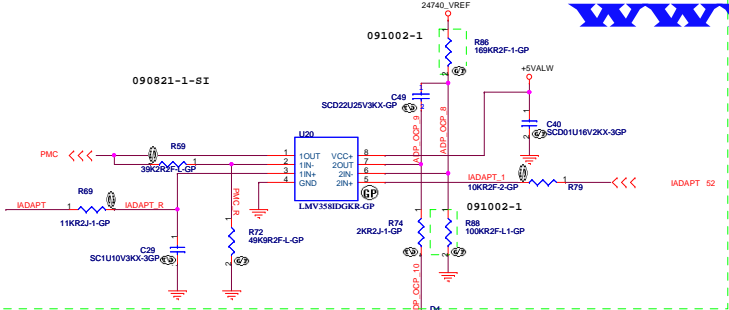
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Title: **RT8208AGQW +VGA_CORE**

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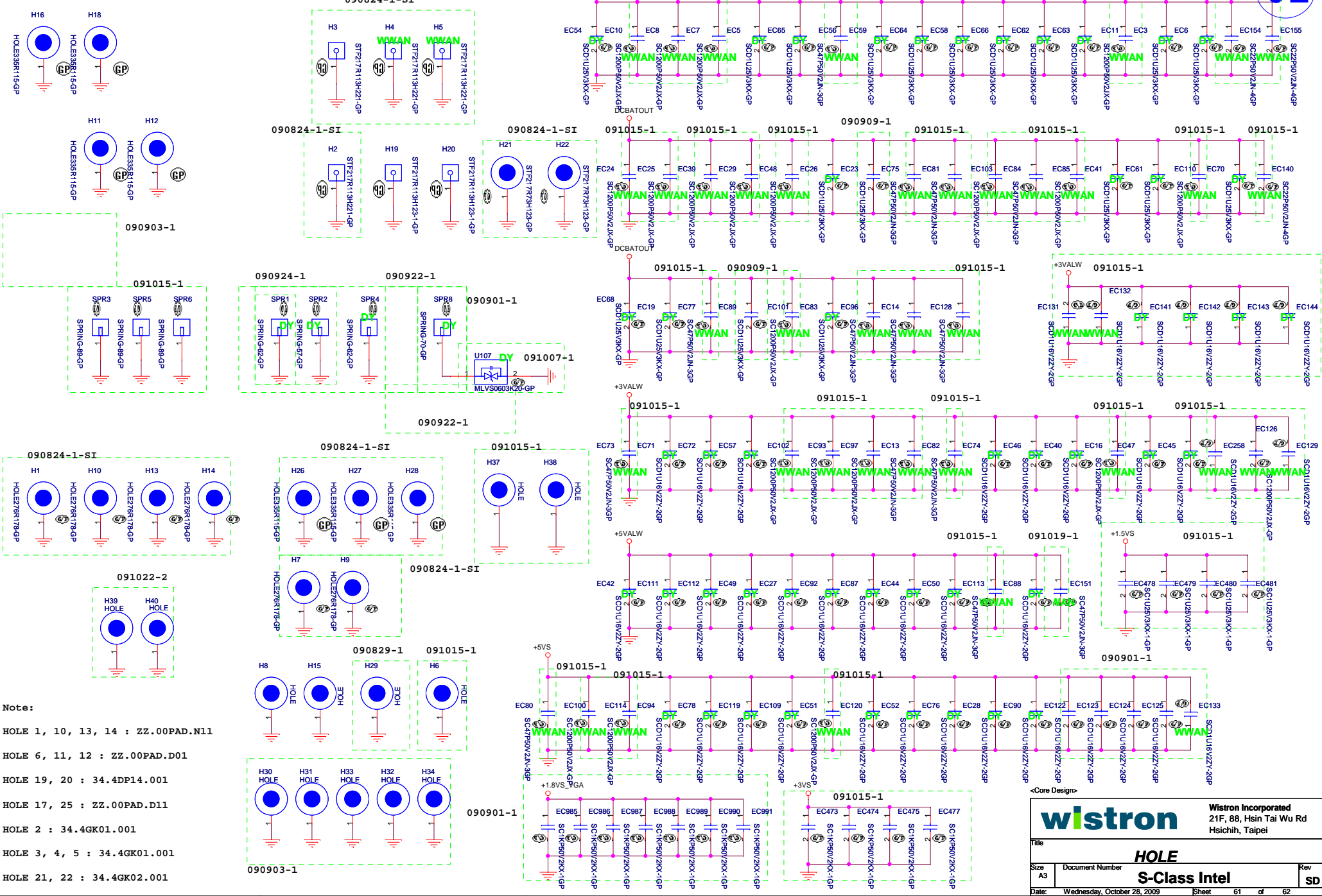
When AC_ADP_PRES=0 --> 1
 $V_{in} = (R_{162} // R_{151}) / [(R_{162} // R_{151}) + R_{148}] = 51125_VREF$
 $V_{in} = 1.7.6145V$

When AC_ADP_PRES=1 --> 0
 $[(V_{in} - 51125_VREF) / R_{148}] + [(+3VL - 51125_VREF) / (R_{151} + R_{153})] = 51125_VREF / R_{162}$
 $V_{in} = 1.7.212554V$

When ADP_PRES=0 -> 1
 $P2 = (R_{169} // R_{159}) / [(R_{169} // R_{159}) + R_{174}] = 51125_VREF$
 $P2 = 13.325V$

When ADP_PRES=1 -> 0
 $[(P2 - 51125_VREF) / R_{169}] + [(+3VL - 51125_VREF) / (R_{175} + R_{159})] = 51125_VREF / R_{162}$
 $P2 = 10.894V$


HOLE



- Note:**
- HOLE 1, 10, 13, 14 : ZZ.00PAD.N11
 - HOLE 6, 11, 12 : ZZ.00PAD.D01
 - HOLE 19, 20 : 34.4DP14.001
 - HOLE 17, 25 : ZZ.00PAD.D11
 - HOLE 2 : 34.4GK01.001
 - HOLE 3, 4, 5 : 34.4GK01.001
 - HOLE 21, 22 : 34.4GK02.001

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<Core Design>

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Title			
Change Notes List			
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