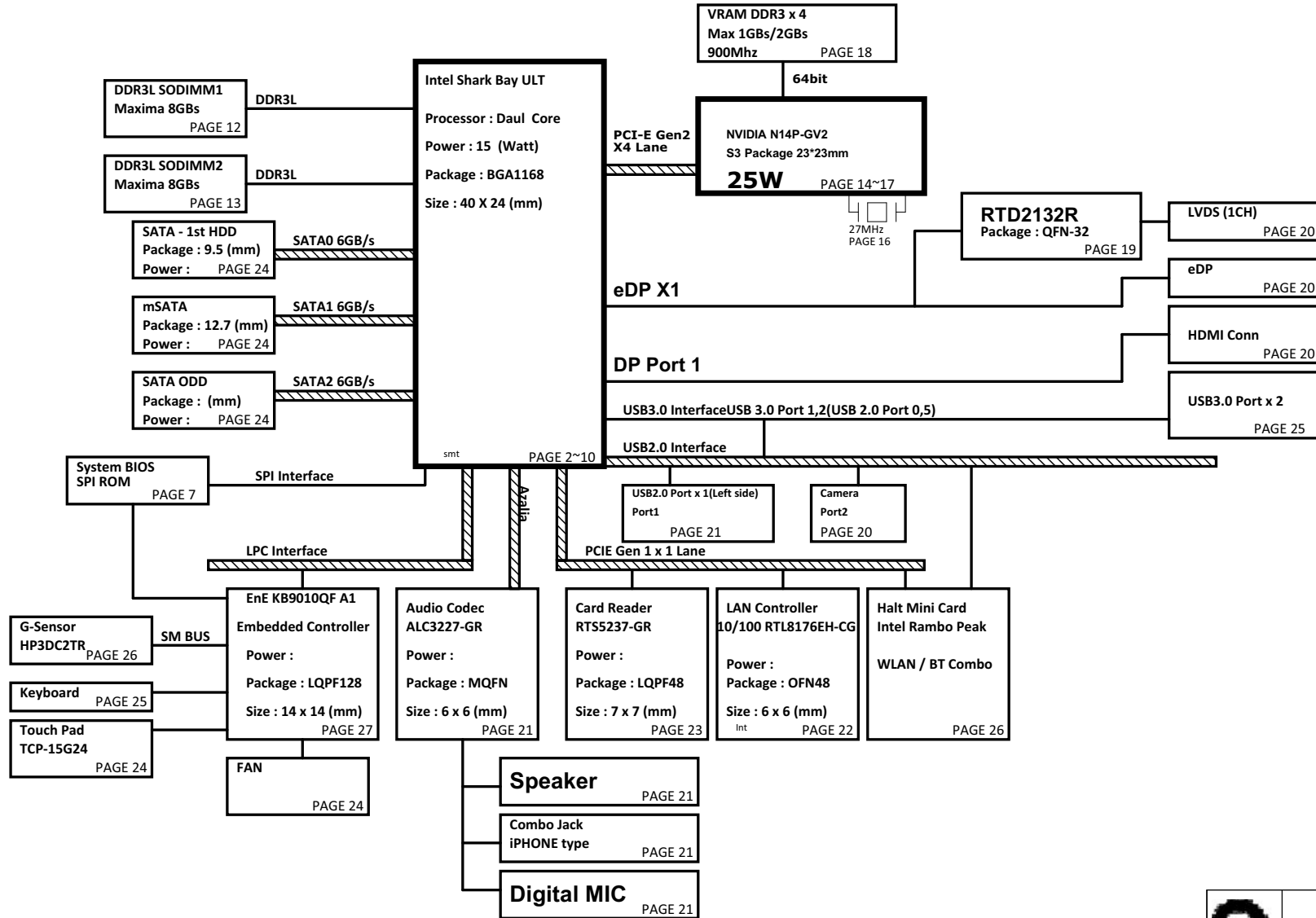
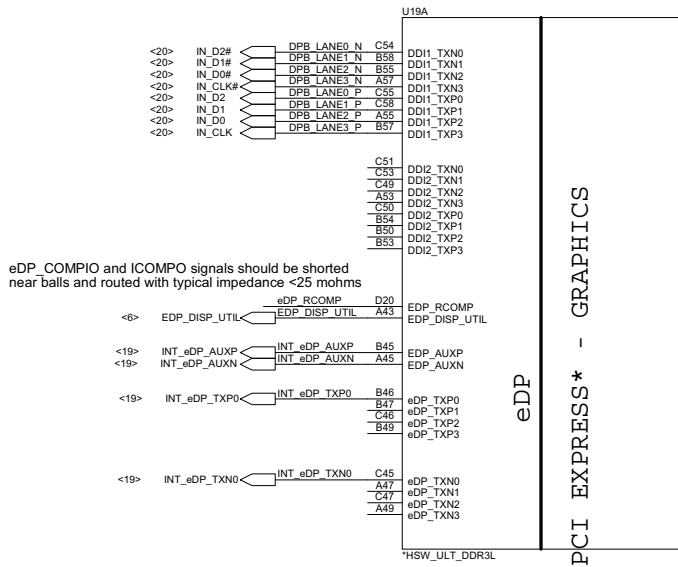


U82 DIS (14"/15.6") Ultra/Slim Intel Shark Bay ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

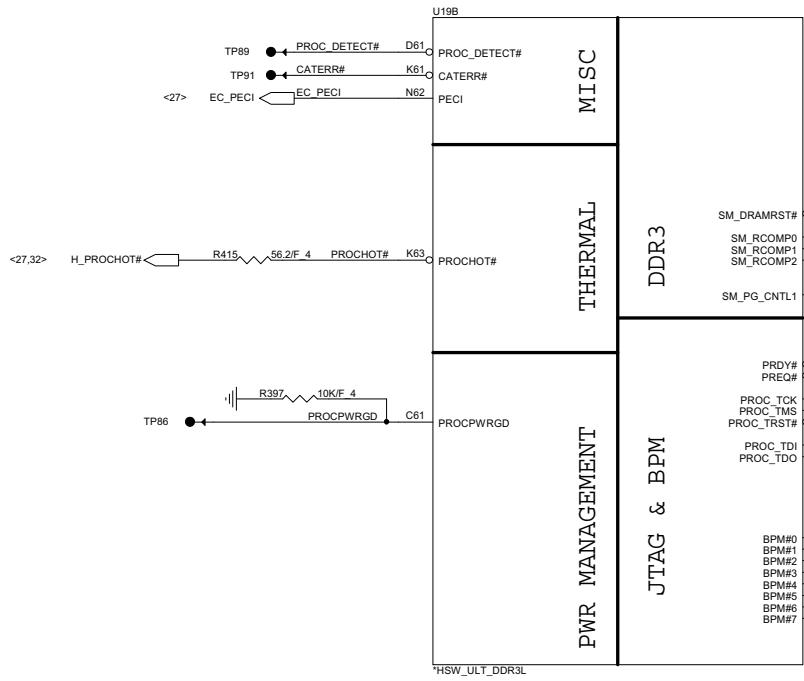




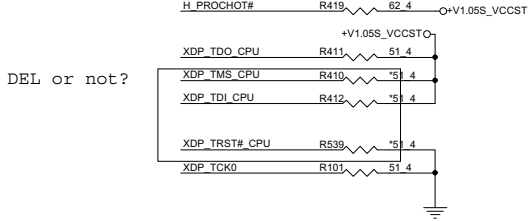
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+VCCIOA_OUT R109 24.9/F 4 eDP_RCOMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



Processor pull-up (CPU)



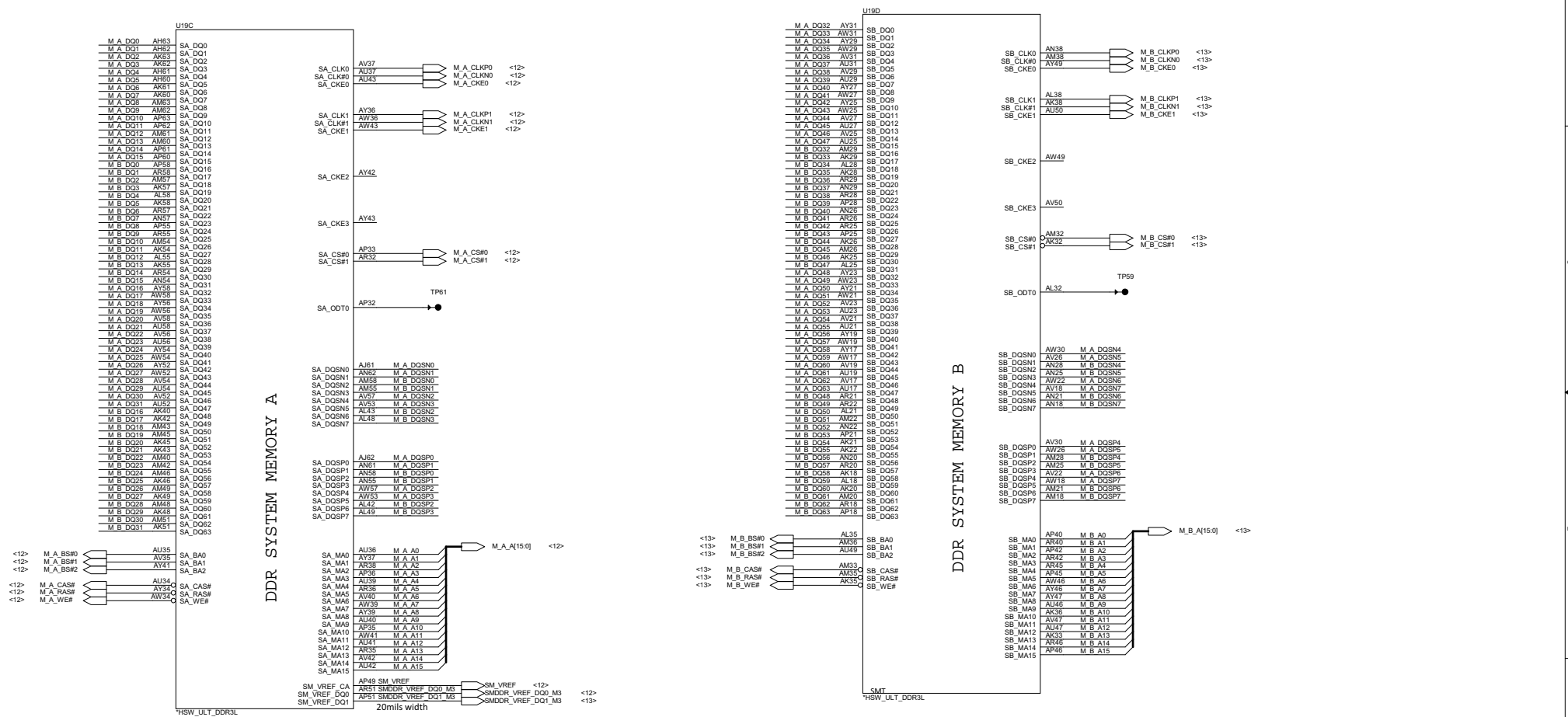
DEL or not?

PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number ULT 1/9(eDP/DDI)	Rev 1A
Date: Friday, April 26, 2013	Sheet 2 of 40	

Haswell ULT Processor (DDR3L)

- <12> M_A_DQ[8:0]
- <13> M_B_DQ[8:0]
- <12> M_A_DQS[7:0]
- <12> M_A_DQSP[7:0]
- <13> M_B_DQS[7:0]
- <13> M_B_DQSP[7:0]



DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

- <12> M_A_BS#0
- <12> M_A_BS#1
- <12> M_A_BS#2
- <12> M_A_CAS#
- <12> M_A_RAS#
- <12> M_A_WE#

- <13> M_B_BS#0
- <13> M_B_BS#1
- <13> M_B_BS#2
- <13> M_B_CAS#
- <13> M_B_RAS#
- <13> M_B_WE#

M_B_A[15:0] <13>

SM_VREF_CA <12> SM_VREF <12>
 SM_VREF_D00 <12> SM_VREF_D00_M3 <12>
 SM_VREF_D01 <13> SM_VREF_D01_M3 <13>

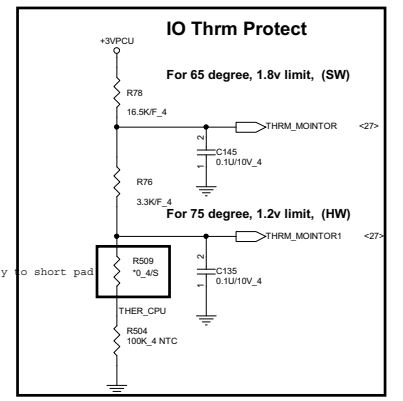
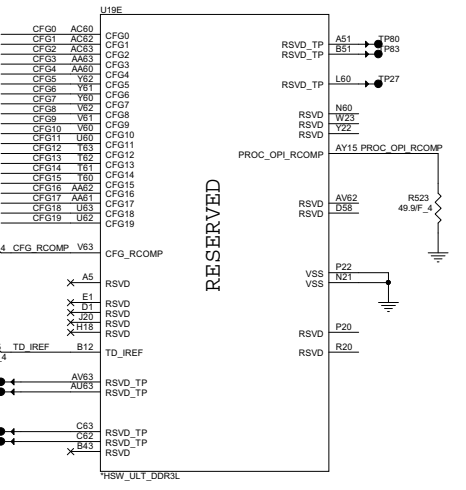
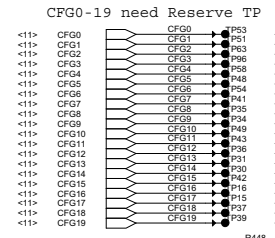
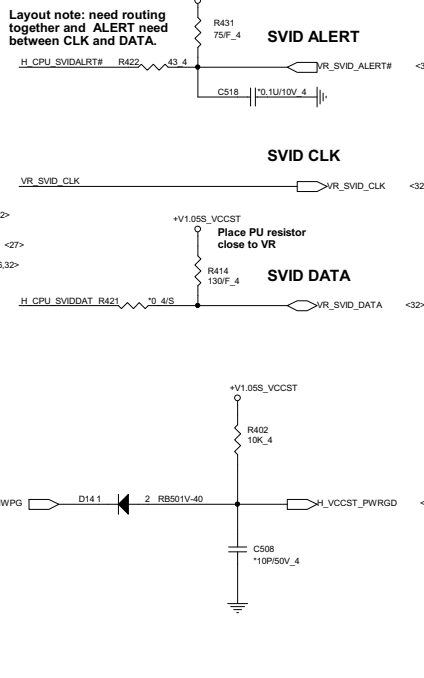
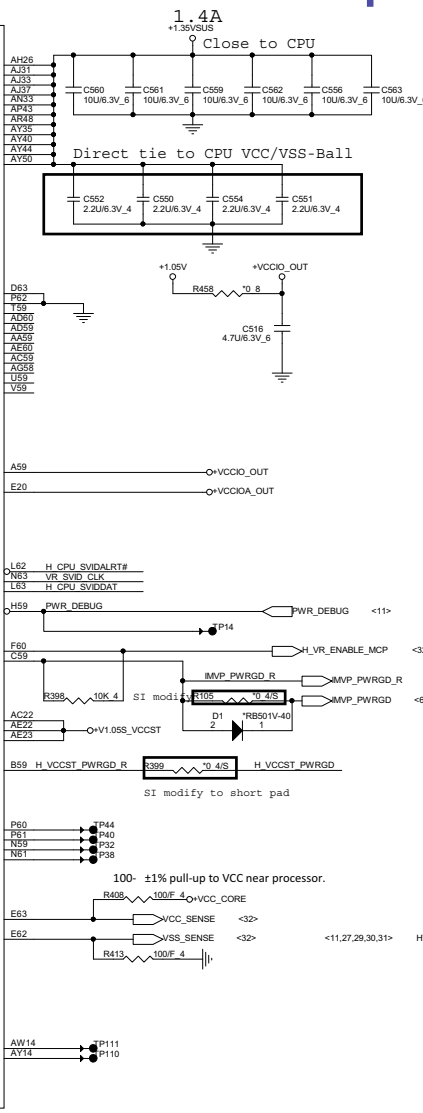
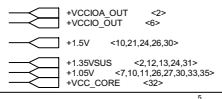
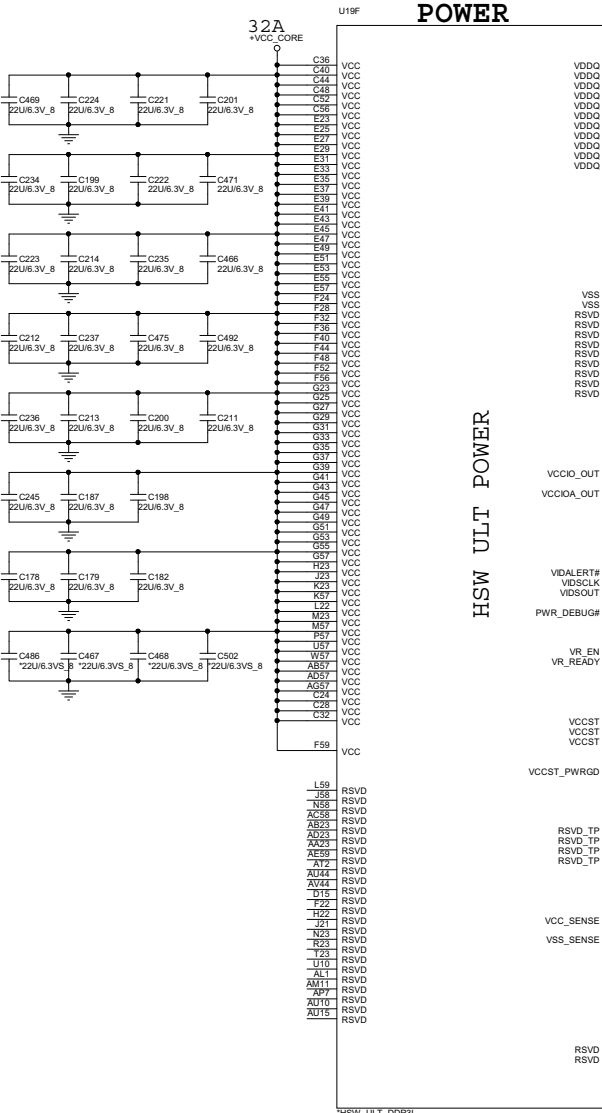
20mils width

SMT

*HSW_ULT_DDR3L

PROJECT :U82
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 2/9 (DDR3 I/F)	1A
Date:	Monday, May 06, 2013	Sheet 3 of 40

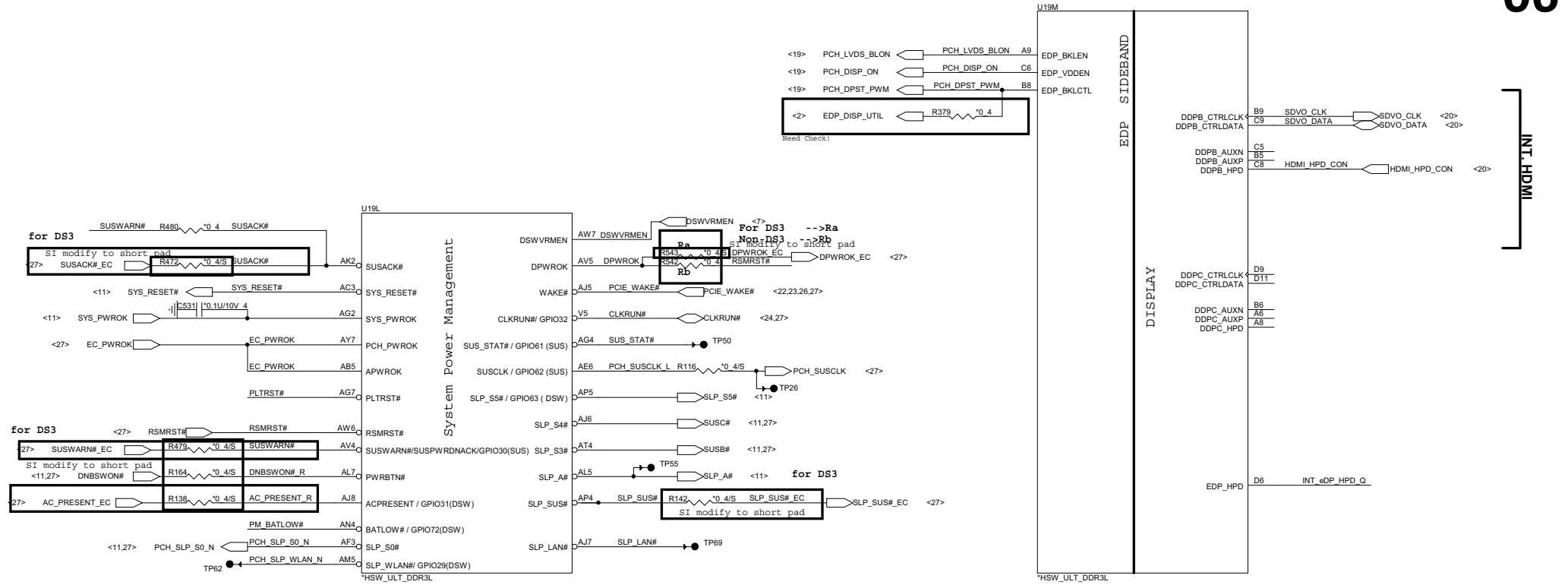


Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

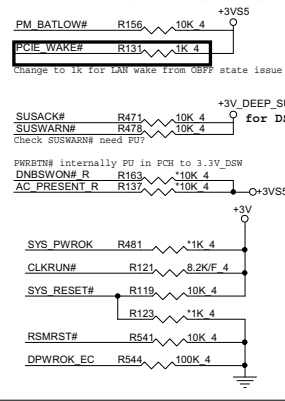
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R452 10K 4
CFG4 (DP Presence Strap)	Disable: No physical DP attached to eDP	Enable: An ext DP device is connected to eDP	CFG4 R143 1K 4

PROJECT :U82
Quanta Computer Inc.

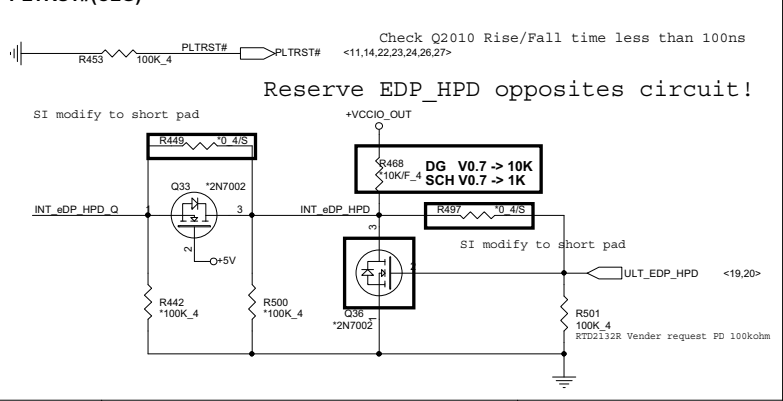
Size: Custom | Document Number: 04 - ULT 3/9 (POWER-1) | Rev: 1A
Date: Friday, April 26, 2013 | Sheet: 4 of 40



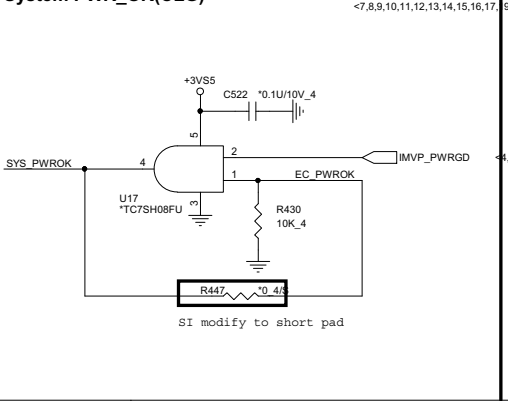
PCH Pull-high/low(CLG)



PLTRST#(CLG)



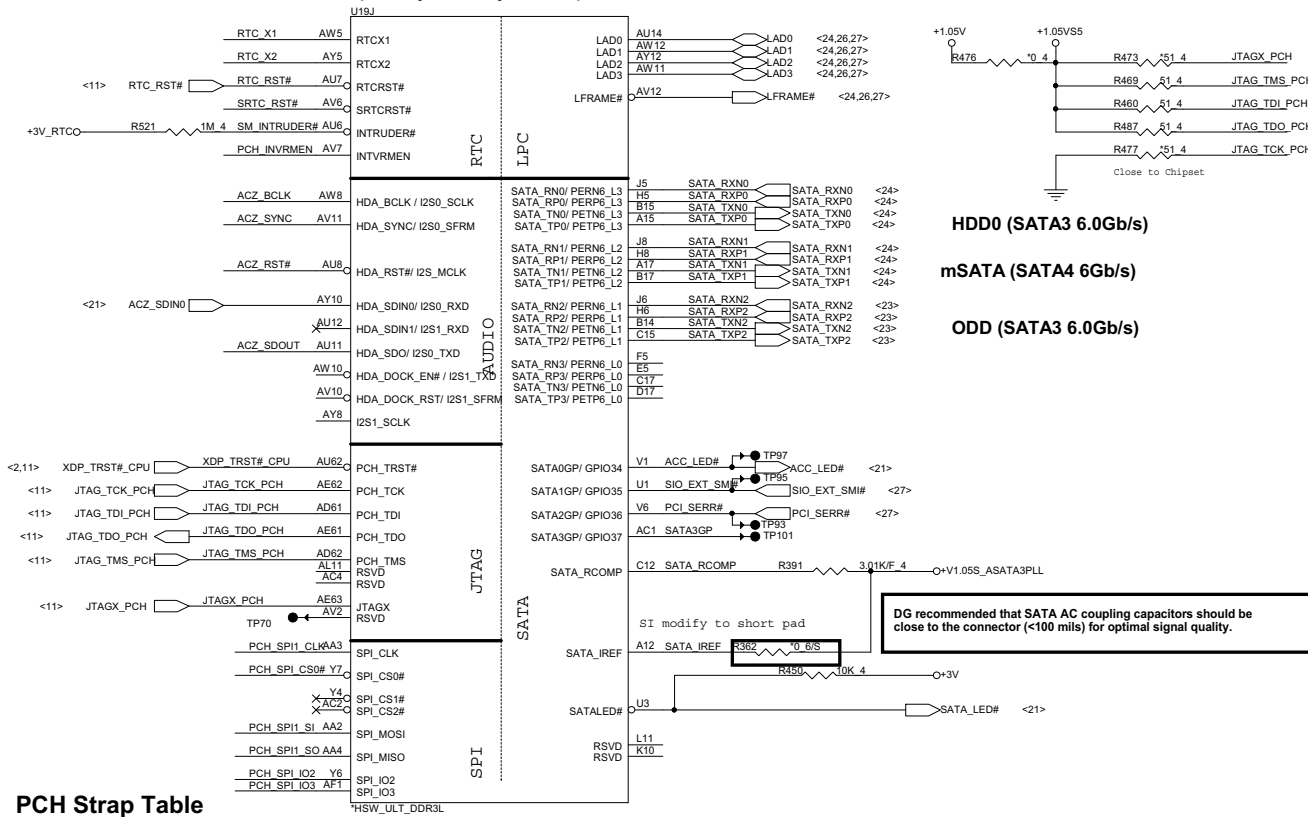
System PWR_OK(CLG)



PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number ULT 5/9(Power Manger)	Rev 1A
Date: Friday, April 26, 2013	Sheet 6 of	40

Lynx Point-LP Platform Controller Hub
(HDA, JTAG, SATA)

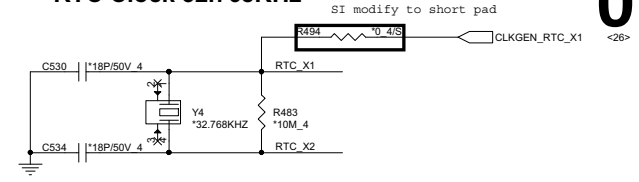


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V0 - R455 1K 4 - SPKR <9>												
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R376 1K 4 - GPIO66_ULT <9>												
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC0 - R519 330K 4 - PCH_INVRMEN												
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	<27> GPIO33_EC - R182 1K 4 - ACZ_SDOULT												
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"> <tr> <th>GNT0#</th> <th>Boot Location</th> </tr> <tr> <td>1</td> <td>LPC</td> </tr> <tr> <td>0</td> <td>SPI(Default)</td> </tr> </table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)							
GNT0#	Boot Location															
1	LPC															
0	SPI(Default)															
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	+3V_DEEP_SUS - R125 1K 4 - GPIO15_ULT <9>												
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC0 - R520 330K 4 - DSWVRMEN <6>												
				<table border="1"> <tr> <td><27></td> <td>PCH_SPI_CS0#_R</td> <td>PCH_SPI_CS0#_R</td> </tr> <tr> <td><27></td> <td>PCH_SPI_CLK_R</td> <td>PCH_SPI_CLK_R</td> </tr> <tr> <td><27></td> <td>PCH_SPI_SI_R</td> <td>PCH_SPI_SI_R</td> </tr> <tr> <td><27></td> <td>PCH_SPI_SO_R</td> <td>PCH_SPI_SO_R</td> </tr> </table>	<27>	PCH_SPI_CS0#_R	PCH_SPI_CS0#_R	<27>	PCH_SPI_CLK_R	PCH_SPI_CLK_R	<27>	PCH_SPI_SI_R	PCH_SPI_SI_R	<27>	PCH_SPI_SO_R	PCH_SPI_SO_R
<27>	PCH_SPI_CS0#_R	PCH_SPI_CS0#_R														
<27>	PCH_SPI_CLK_R	PCH_SPI_CLK_R														
<27>	PCH_SPI_SI_R	PCH_SPI_SI_R														
<27>	PCH_SPI_SO_R	PCH_SPI_SO_R														

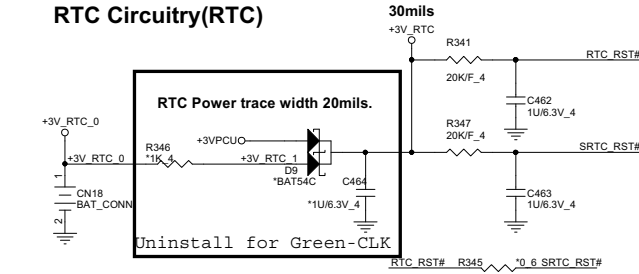
RTC Clock 32.768KHz

07

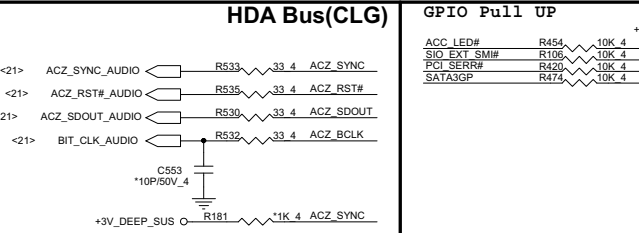


no stuff if use green Clock

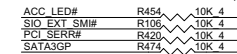
RTC Circuitry(RTC)



HDA Bus(CLG)



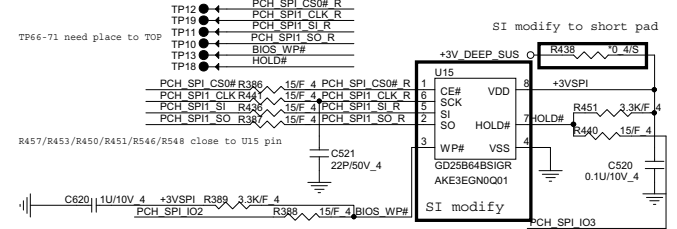
GPIO Pull UP



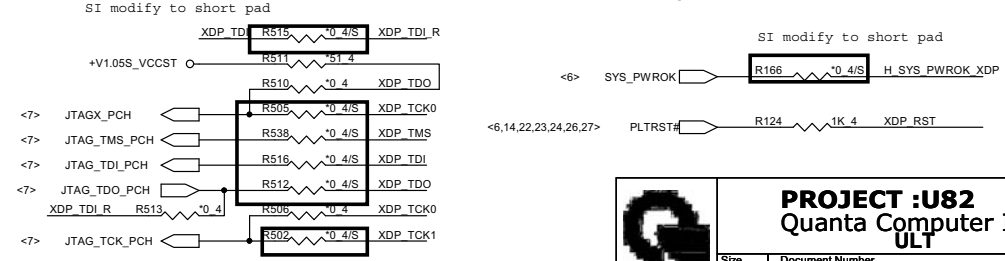
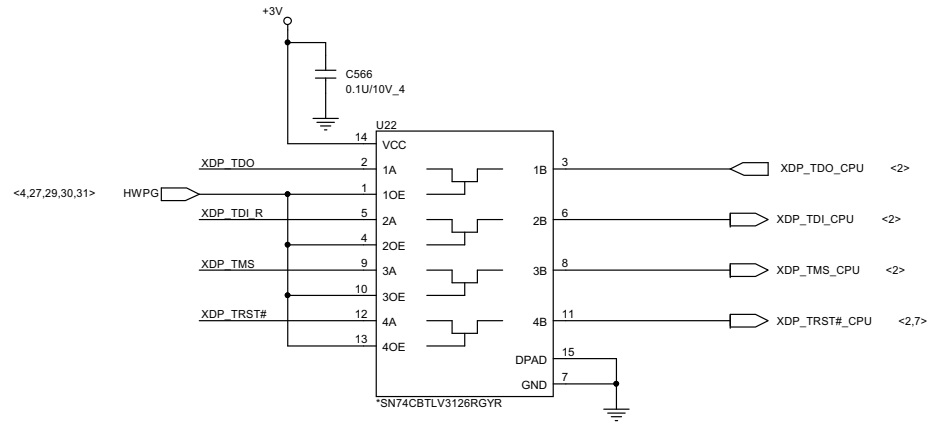
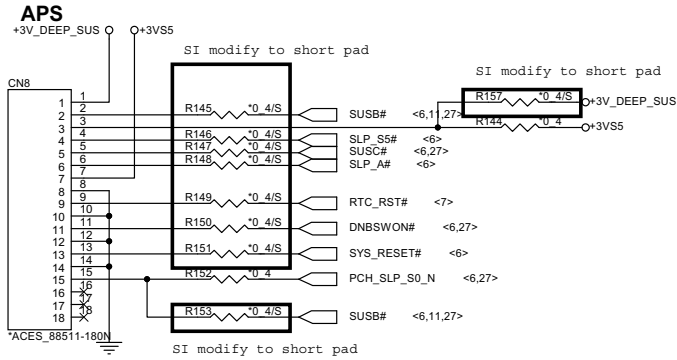
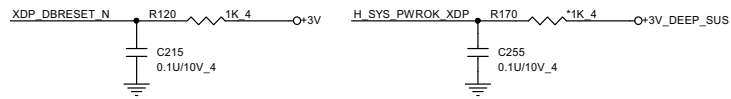
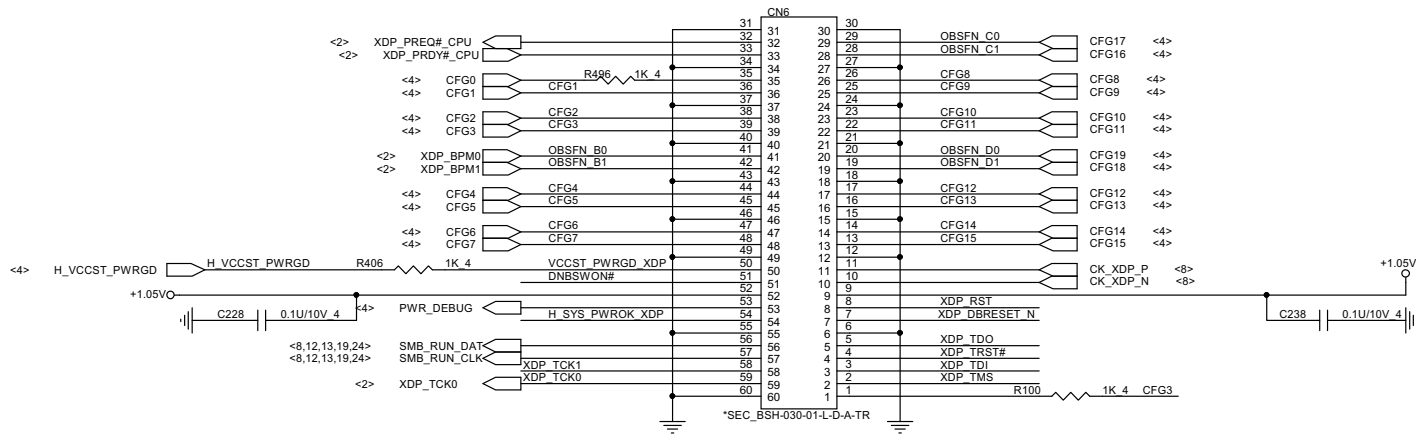
DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.


Vender	Size	P/N
MXIC	8MB	AKE3EZ00Z00 (MX25L6473EM2I-10G)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFH08FS023

PCH SPI ROM(CLG)



PROJECT :U82
Quanta Computer Inc.



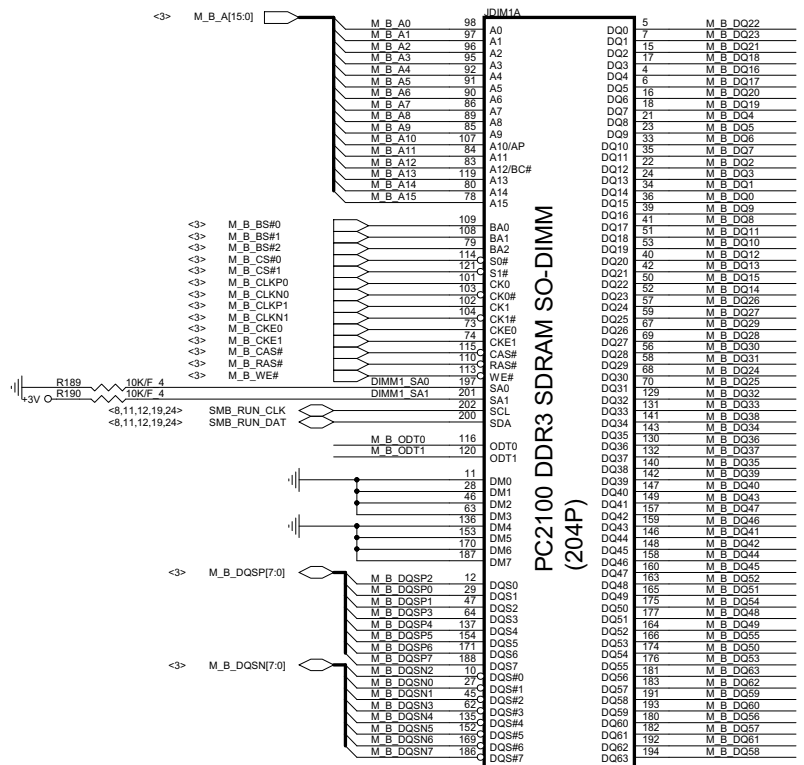


PROJECT :U82
Quanta Computer Inc.
ULT

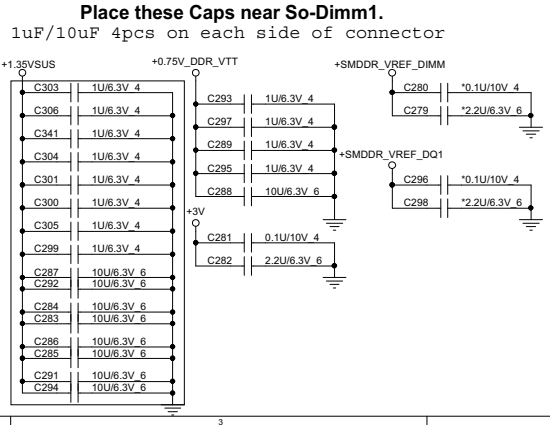
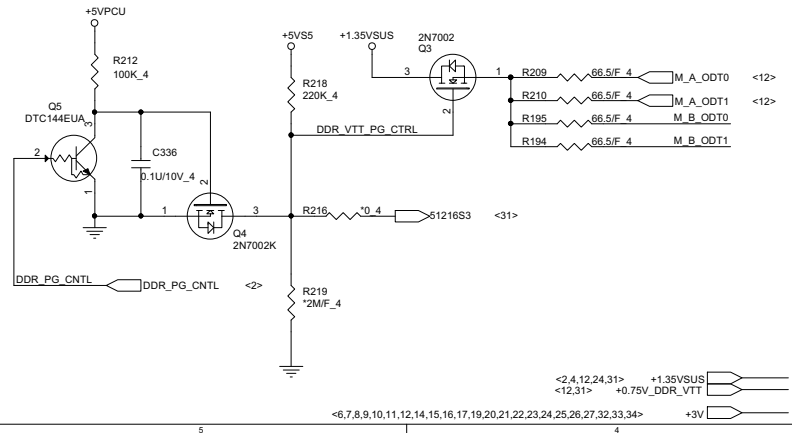
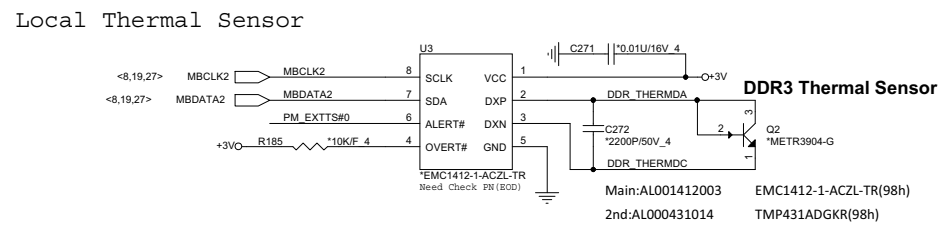
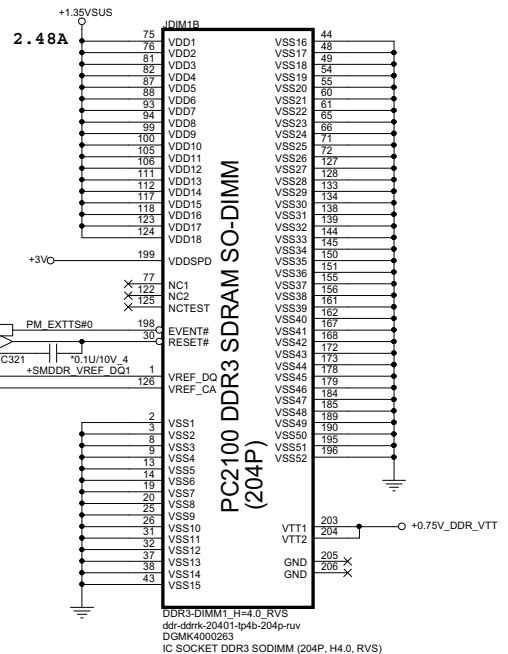
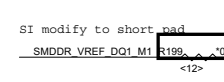
Size	Document Number	Rev
	HSW XDP & APS	1A

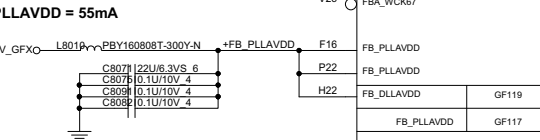
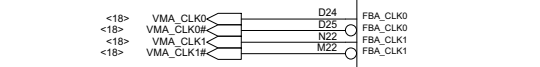
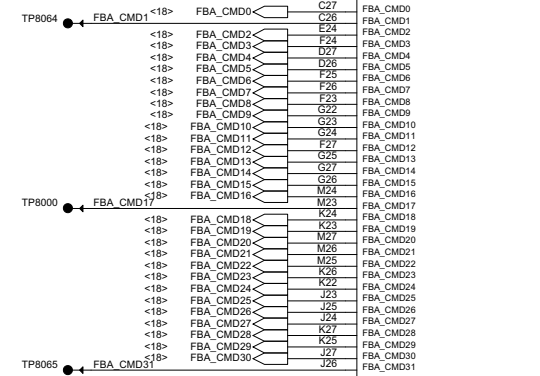
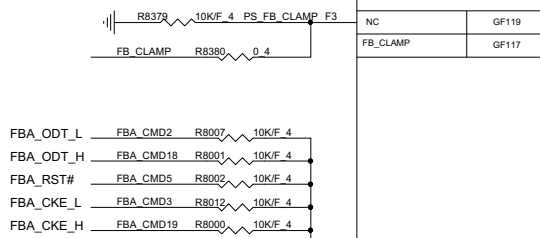
Friday, April 27, 2013 11:54:41 AM

M_B_DQ[63:0] <3>



DDR3-DIMM1_H=4.0_RVS
 ddr-ddrk-20401-1p4b-204p-ruv
 DGMK4000263
 IC SOCKET DDR3 SODIMM (204P, H4.0, RVS)



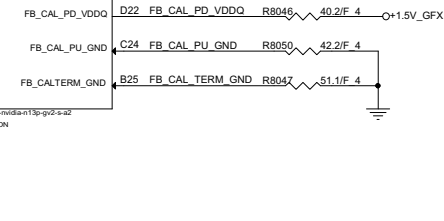
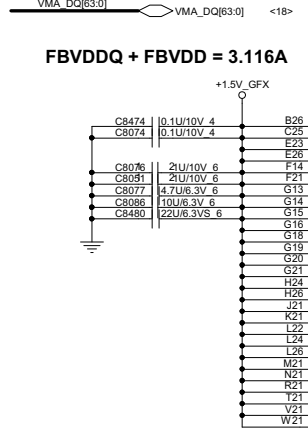


2/14 FBA	E18 VMA D00
FBA_D0	F18 VMA D01
FBA_D1	E16 VMA D02
FBA_D2	F17 VMA D03
FBA_D3	D20 VMA D04
FBA_D4	D21 VMA D05
FBA_D5	F20 VMA D06
FBA_D6	E21 VMA D07
FBA_D7	E15 VMA D08
FBA_D8	D15 VMA D09
FBA_D9	F15 VMA D010
FBA_D10	F13 VMA D011
FBA_D11	C13 VMA D012
FBA_D12	B13 VMA D013
FBA_D13	E13 VMA D014
FBA_D14	D13 VMA D015
FBA_D15	B15 VMA D016
FBA_D16	C16 VMA D017
FBA_D17	A13 VMA D018
FBA_D18	A15 VMA D019
FBA_D19	B18 VMA D020
FBA_D20	A18 VMA D021
FBA_D21	A19 VMA D022
FBA_D22	C19 VMA D023
FBA_D23	B24 VMA D024
FBA_D24	C23 VMA D025
FBA_D25	A25 VMA D026
FBA_D26	A24 VMA D027
FBA_D27	A21 VMA D028
FBA_D28	B21 VMA D029
FBA_D29	C20 VMA D030
FBA_D30	C21 VMA D031
FBA_D31	R22 VMA D032
FBA_D32	R24 VMA D033
FBA_D33	T22 VMA D034
FBA_D34	R23 VMA D035
FBA_D35	N25 VMA D036
FBA_D36	N26 VMA D037
FBA_D37	N23 VMA D038
FBA_D38	N24 VMA D039
FBA_D39	V23 VMA D040
FBA_D40	V22 VMA D041
FBA_D41	Y23 VMA D042
FBA_D42	Y22 VMA D043
FBA_D43	Y24 VMA D044
FBA_D44	AA24 VMA D045
FBA_D45	Y22 VMA D046
FBA_D46	AA23 VMA D047
FBA_D47	AD27 VMA D048
FBA_D48	AB25 VMA D049
FBA_D49	AD26 VMA D050
FBA_D50	AC25 VMA D051
FBA_D51	AC27 VMA D052
FBA_D52	AA26 VMA D053
FBA_D53	W26 VMA D054
FBA_D54	Y25 VMA D055
FBA_D55	T25 VMA D056
FBA_D56	T25 VMA D057
FBA_D57	N27 VMA D058
FBA_D58	R27 VMA D059
FBA_D59	Y26 VMA D060
FBA_D60	V27 VMA D061
FBA_D61	V27 VMA D062
FBA_D62	W25 VMA D063
FBA_D63	

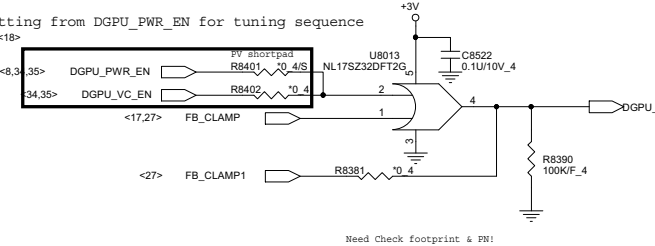
FBA_DM0	D19 VMA DM0
FBA_DM1	D14 VMA DM1
FBA_DM2	C17 VMA DM2
FBA_DM3	C22 VMA DM3
FBA_DM4	P24 VMA DM4
FBA_DM5	W24 VMA DM5
FBA_DM6	AA25 VMA DM6
FBA_DM7	U25 VMA DM7

FBA_DQS_WP0	E19 VMA DQSQ0
FBA_DQS_WP1	C15 VMA DQSQ1
FBA_DQS_WP2	B16 VMA DQSQ2
FBA_DQS_WP3	B22 VMA DQSQ3
FBA_DQS_WP4	R25 VMA DQSQ4
FBA_DQS_WP5	W23 VMA DQSQ5
FBA_DQS_WP6	AB26 VMA DQSQ6
FBA_DQS_WP7	T26 VMA DQSQ7

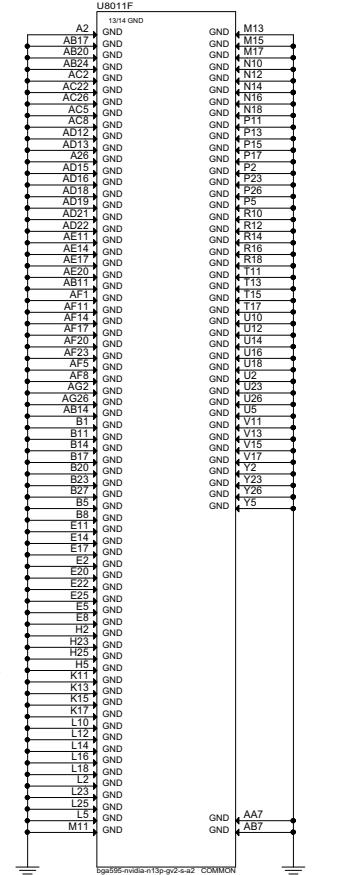
FBA_DQS_RN0	F19 VMA RDQS0
FBA_DQS_RN1	C14 VMA RDQS1
FBA_DQS_RN2	A16 VMA RDQS2
FBA_DQS_RN3	K27 VMA RDQS3
FBA_DQS_RN4	P25 VMA RDQS4
FBA_DQS_RN5	W22 VMA RDQS5
FBA_DQS_RN6	AB27 VMA RDQS6
FBA_DQS_RN7	T27 VMA RDQS7



For support GC6



Need Check footprint & FN1



FB_PLLAVDD = 55mA

FB_DLLAVDD = 15mA

FB_PLLAVDD	GF119
FB_DLLAVDD	GF117

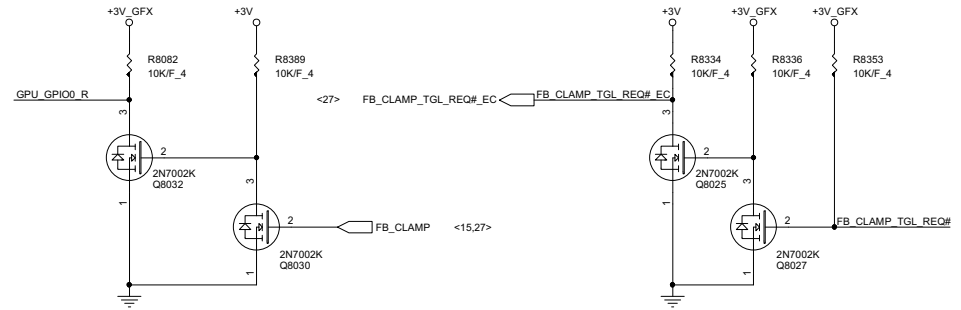
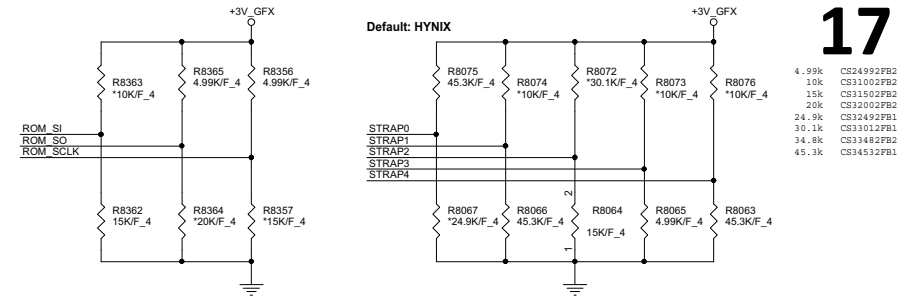
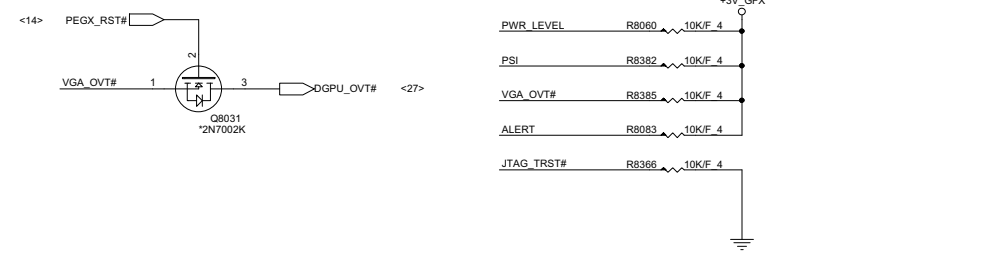
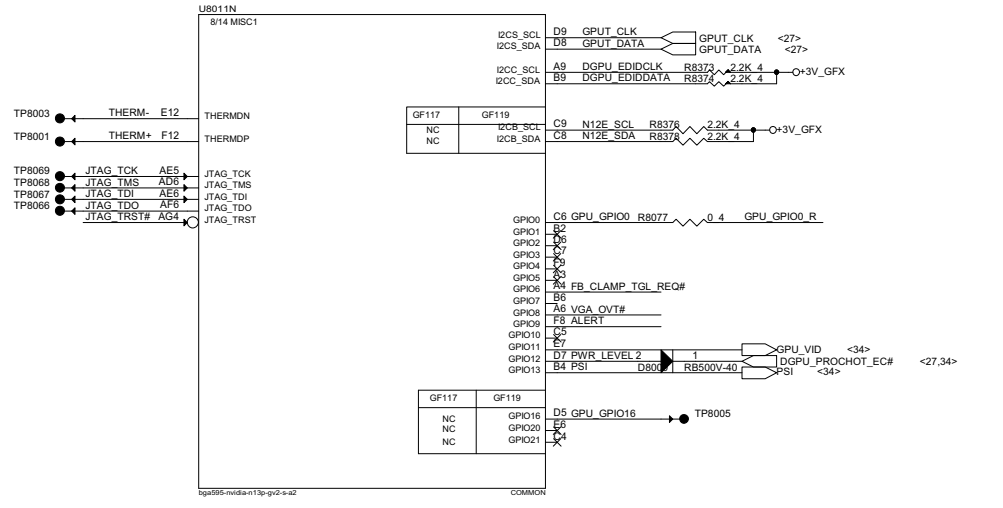
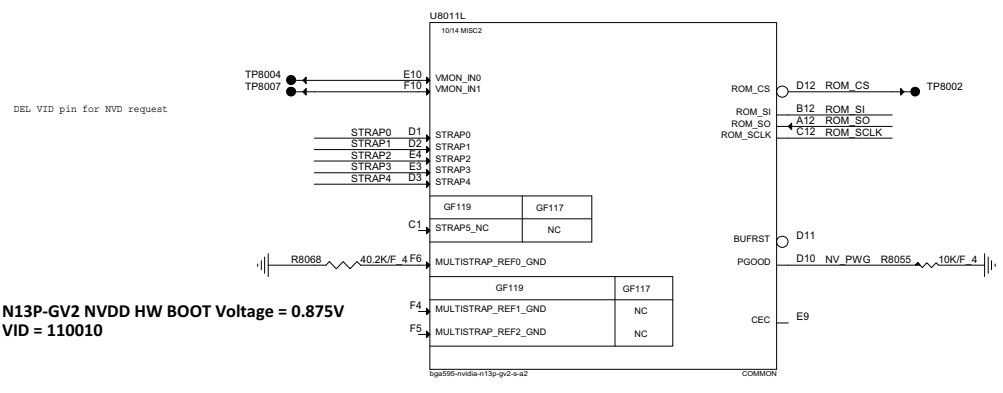
FB_VREF_PROBE	D23
---------------	-----

PROJECT :U82
Quanta Computer Inc.

Size Custom Document Number **N14M-GS (MEMORY/GND)** Rev 2A
Date: Monday, May 06, 2013 Sheet 15 of 40

DEL VID pin for NVD request

N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010



VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	QCI P/N
0000	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	Micron	MT41J128M16JT-107G:K	AKD5MGSTL06	AKD5MGSTL08
0000	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	HYNIX	H5TQ2G63DFR-11C	AKD5MGWTW16	AKD5MGWTW13
0111	DDR3 128Mx16x4, 64bit, 2Gb,900MHz	SAMSUNG	K4W2G1646E-BC11	AKD5MGGT520	AKD5MGGT522

GPIO ASSIGNMENTS

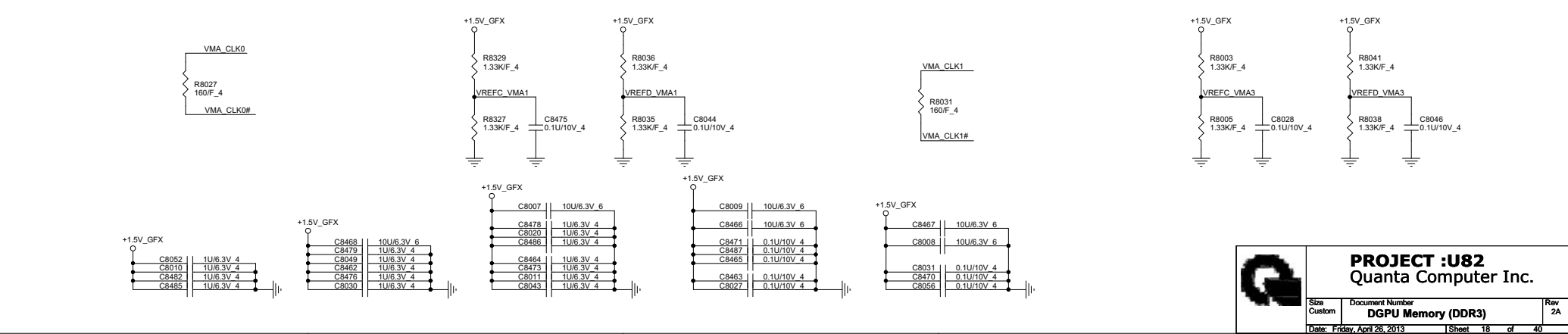
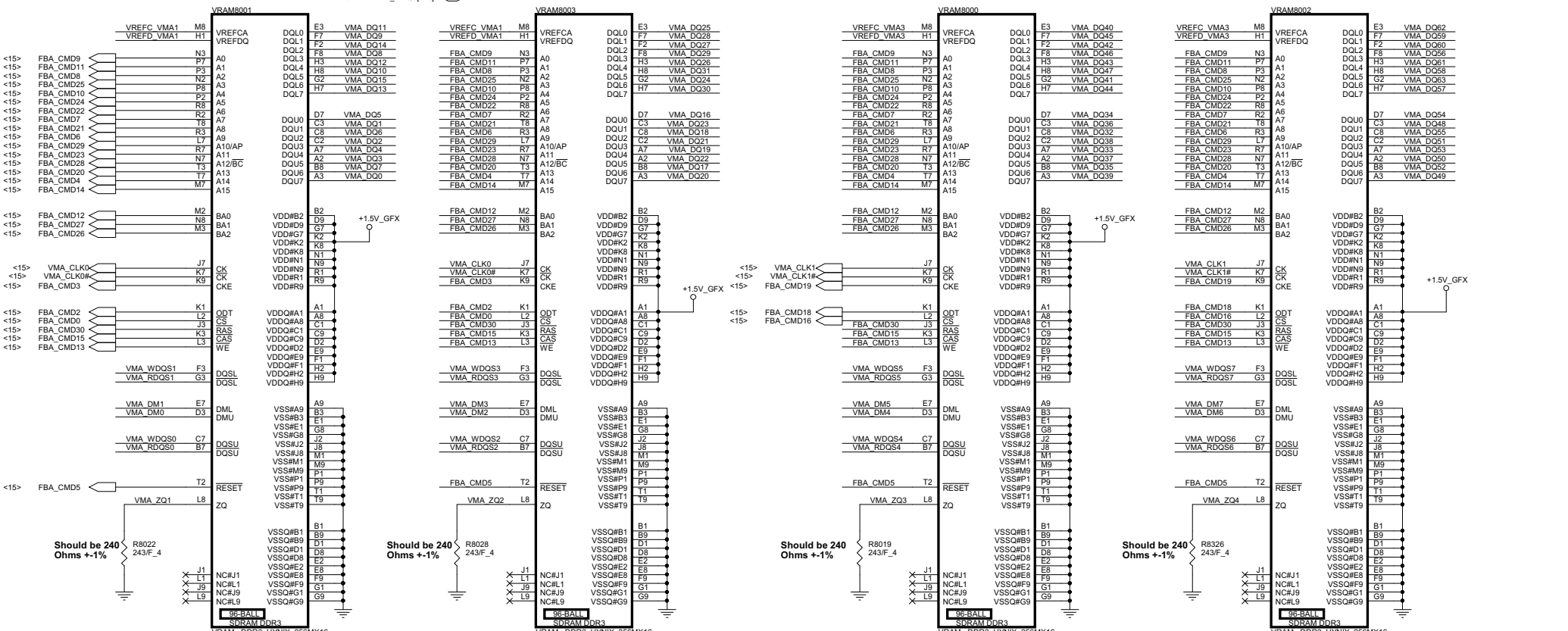
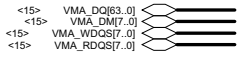
GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

PROJECT :U82
Quanta Computer Inc.

Size Custom Document Number N14M-GS (GPIO/STRAPS) Rev 2A
Date: Friday, April 26, 2013 Sheet 17 of 40

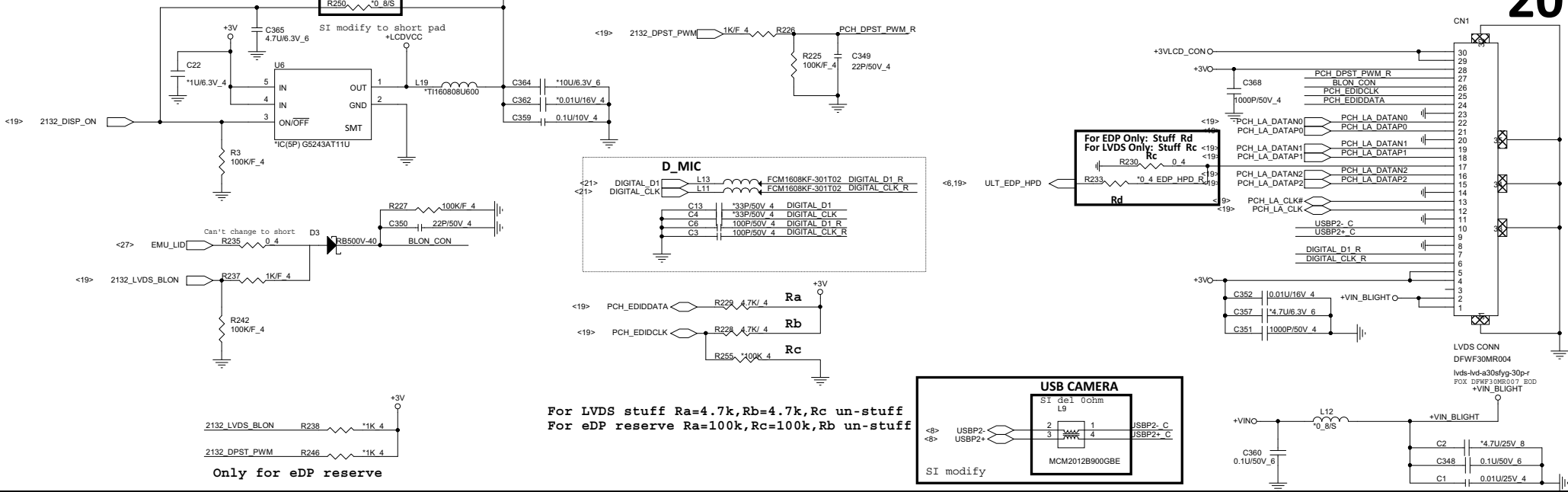
CHANNEL A: 256MB/512MB DDR3

HYU 256Mx16, PN : AKD5PGWTW08 --- AKD5PGWTW07
128Mx16, PN : AKD5MZDTW03 --- AKD5MZDTW02
SAM 256Mx16, PN : AKD5PZDT501 --- AKD5PZDT500
128Mx16, PN : AKD5MGT535 --- AKD5MGT534

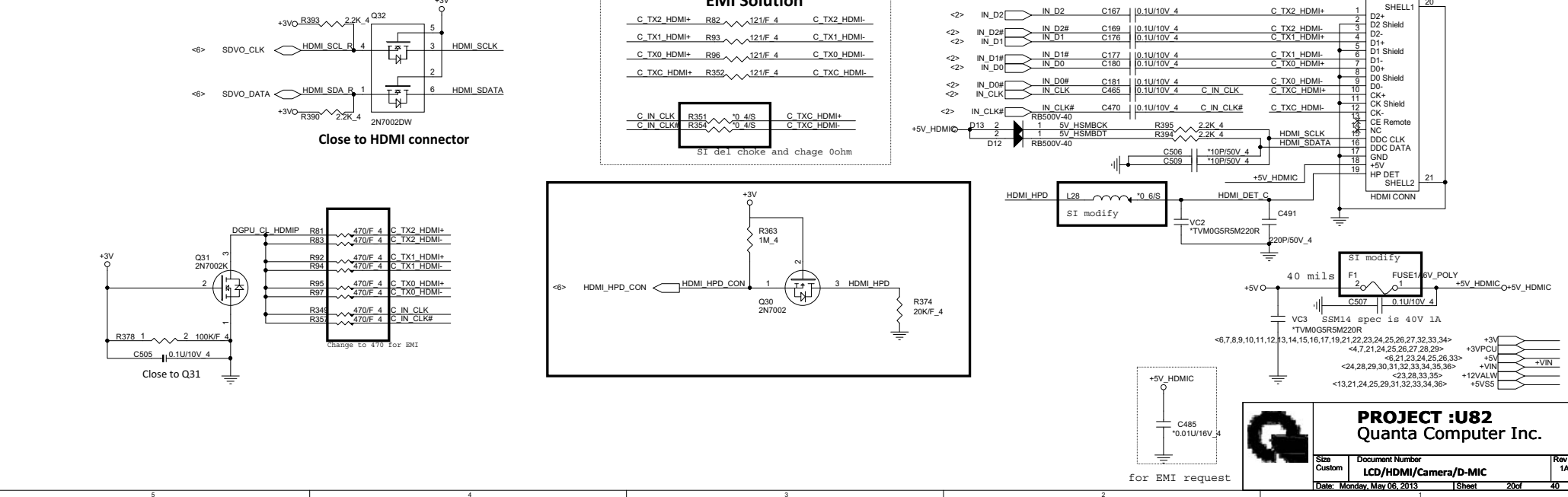


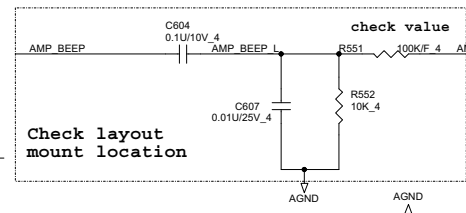
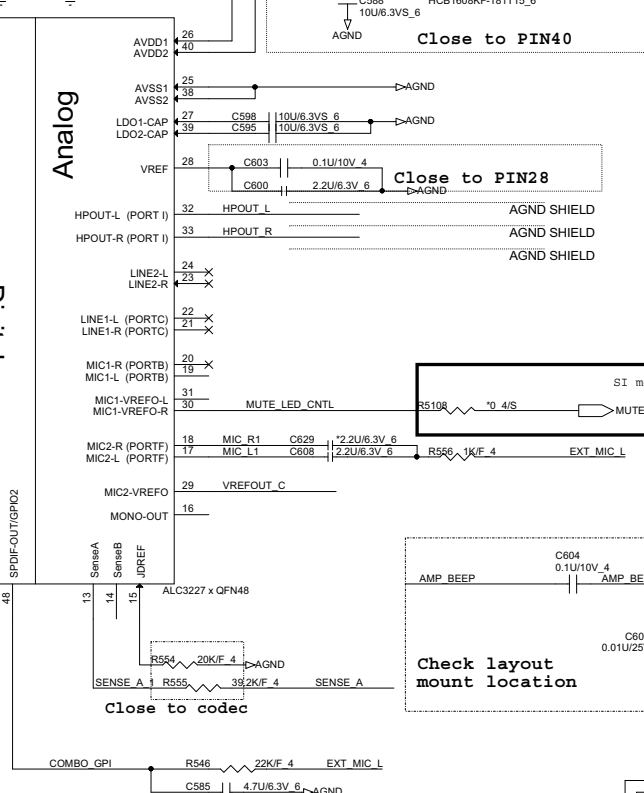
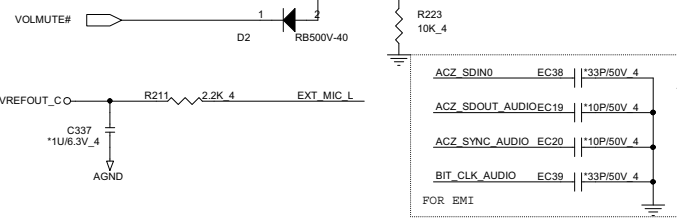
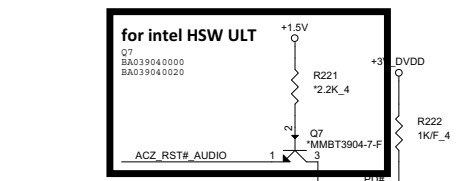
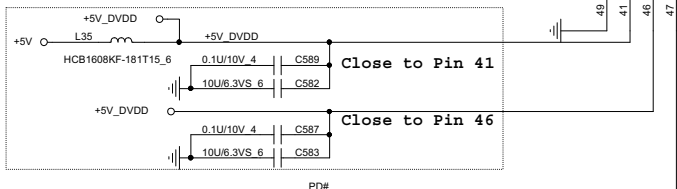
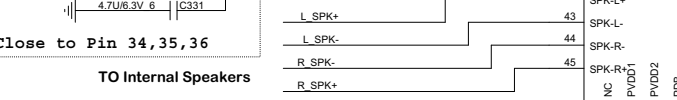
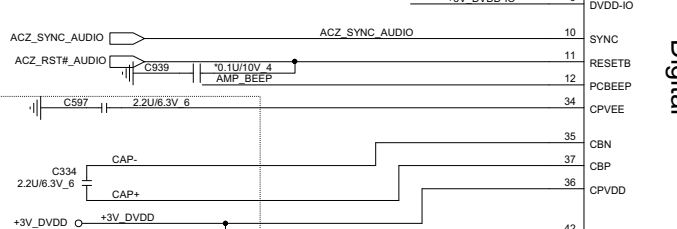
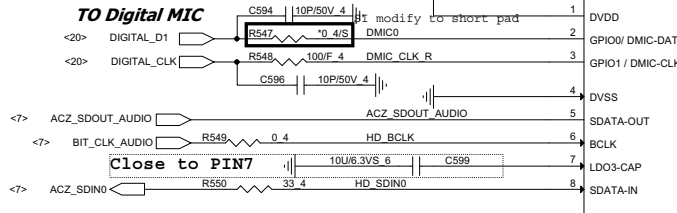
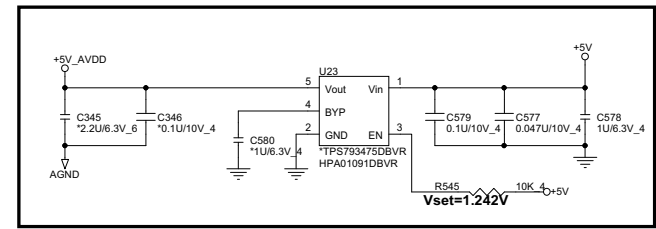
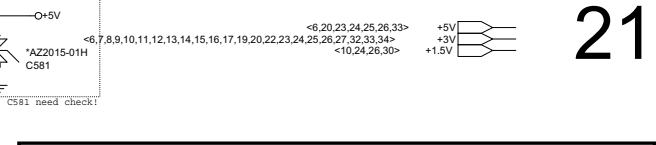
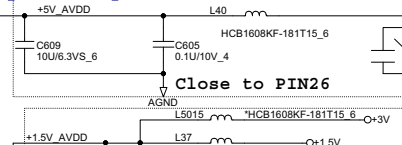
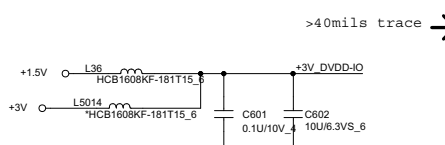
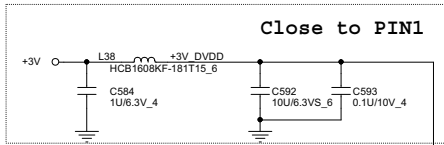
PROJECT :U82
Quanta Computer Inc.
Date: Friday, April 26, 2013
Sheet 18 of 40

LVDS Conn.

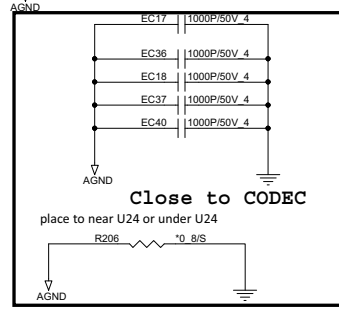
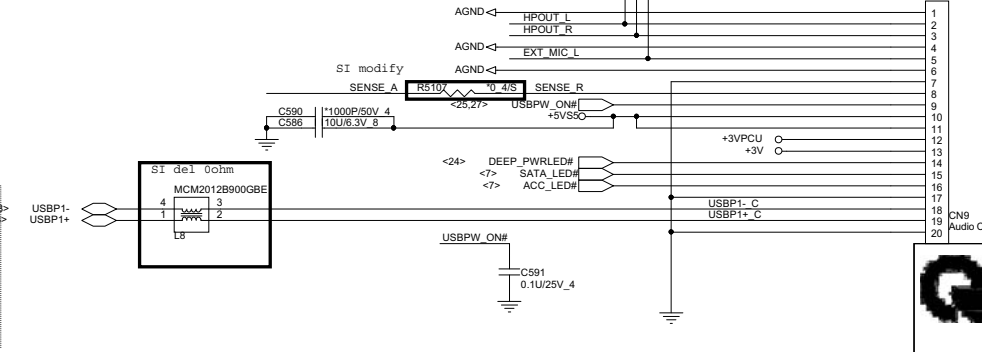


HDMI Conn.





USB 2.0 AND AUDIO COMBO JACK



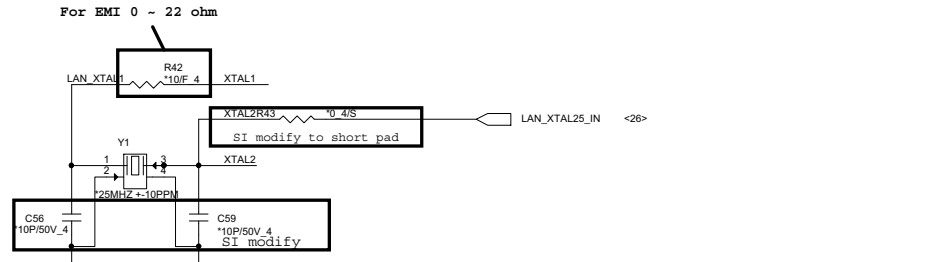
PROJECT :U82

Quanta Computer Inc.

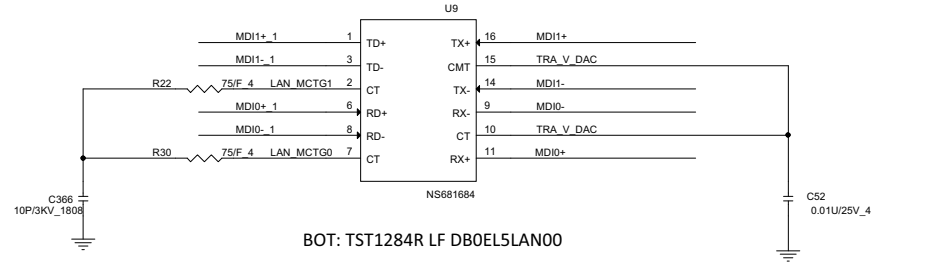
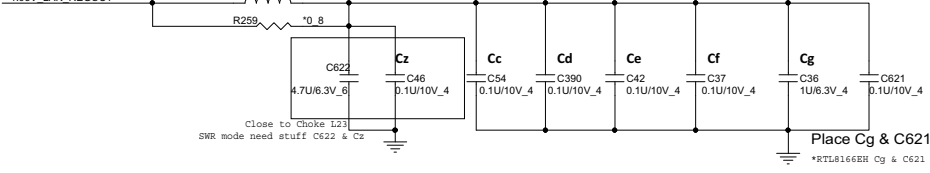
Document Number: Azalla ALC 3227

Date: Friday, April 26, 2013

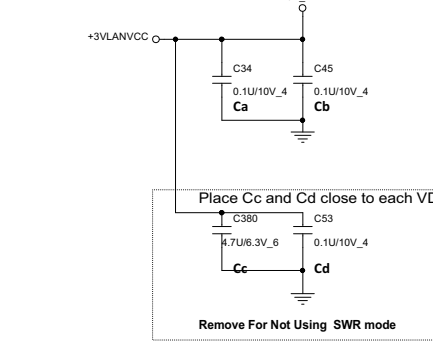
Sheet 21 of 40



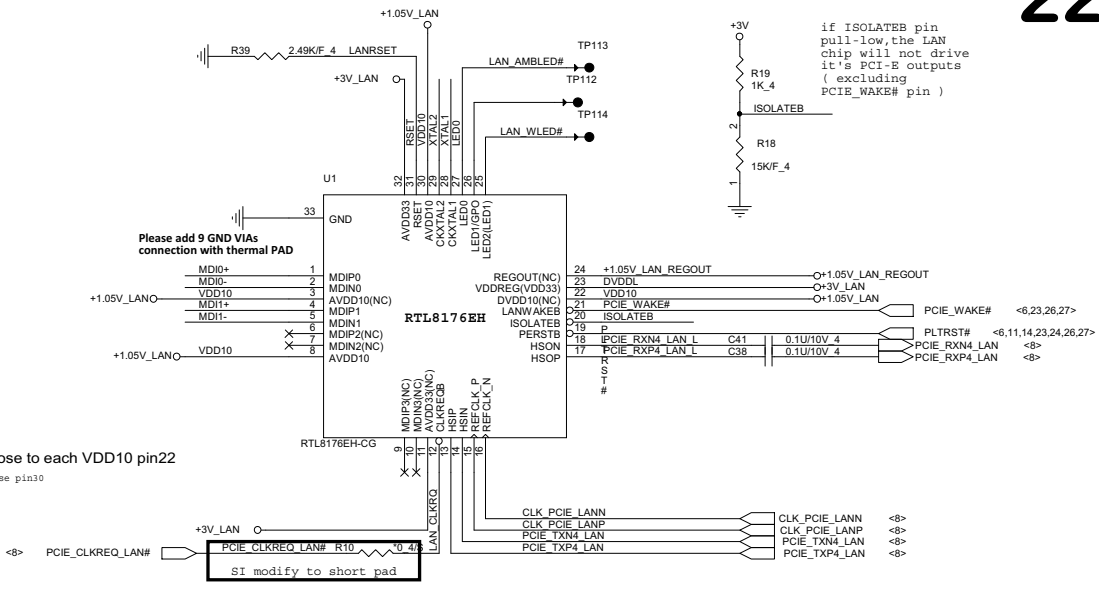
Trace < 30 mil
Width > 60 mil
Power trace Layout 宽度 > 60mil



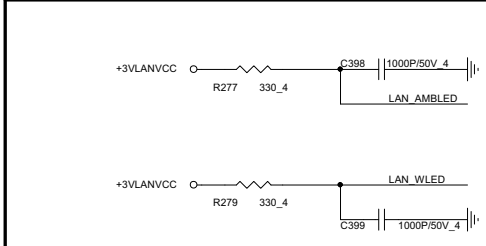
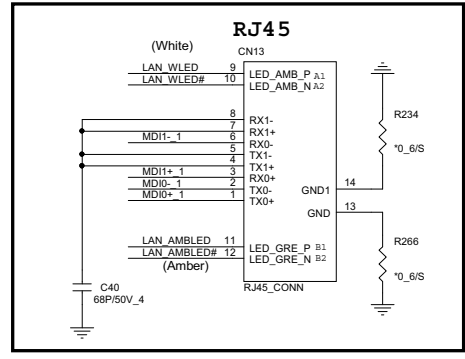
Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



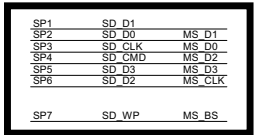
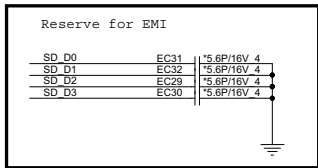
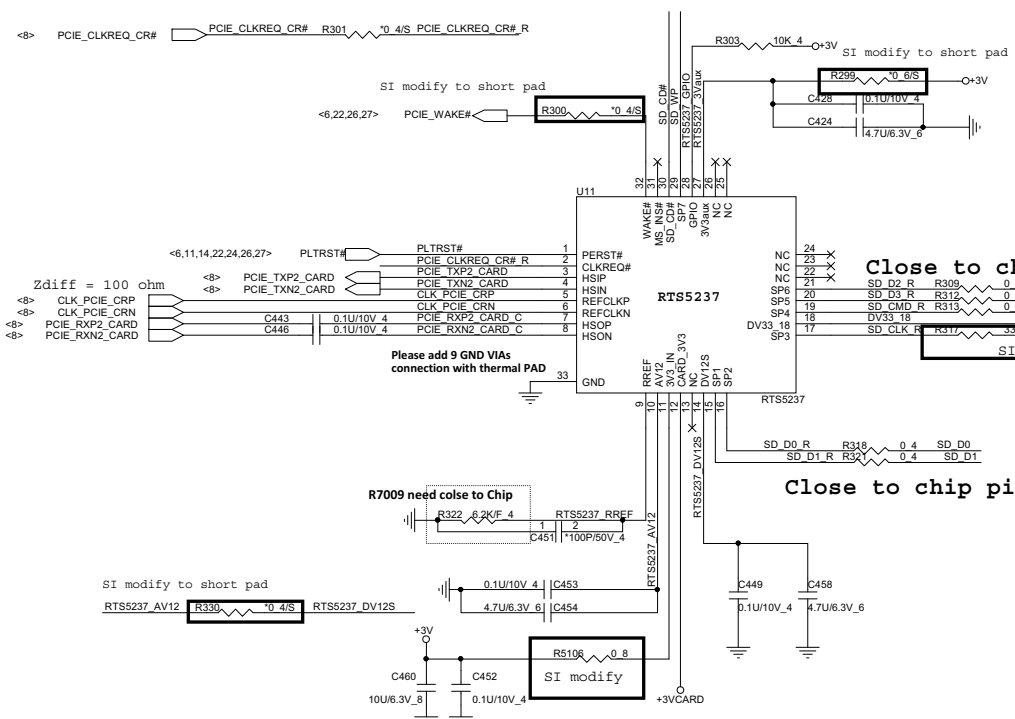
<6,7,8,9,10,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,32,33,34>
<26,33>



LAN conn
TWD Type



	PROJECT :U82	
	Quanta Computer Inc.	
	Size Custom Date: Friday, April 26, 2013	Document Number LAN RTL8176EH/RJ45
Date: Friday, April 26, 2013		Sheet 22 of 40



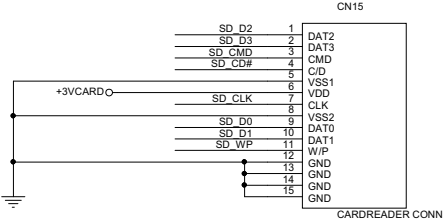
Share Pin
SD / MMC

Close to chip pin

Close to chip pin

CLOSE CONN

CARD READER

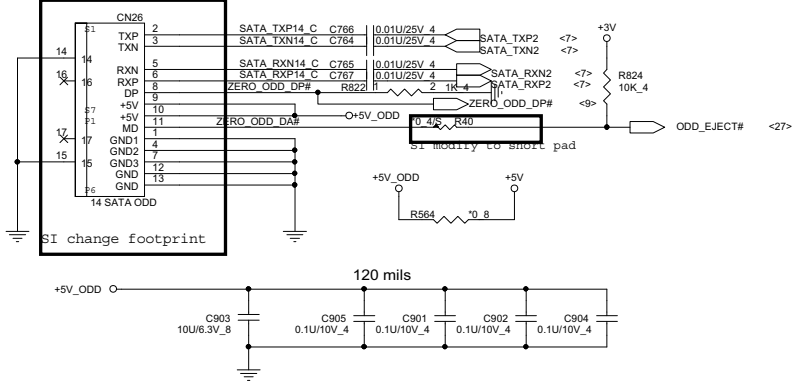


R3X Type

SATA ODD CONNECTOR

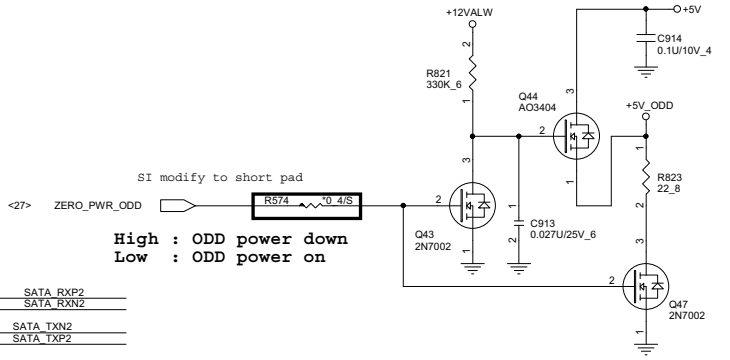
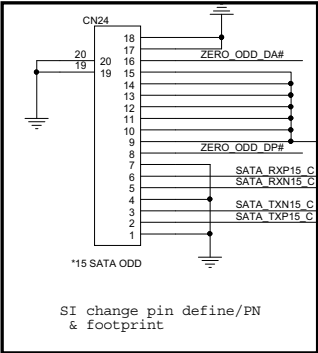
14" SATA ODD

Bypass CAP close conn



15" SATA ODD

New Type



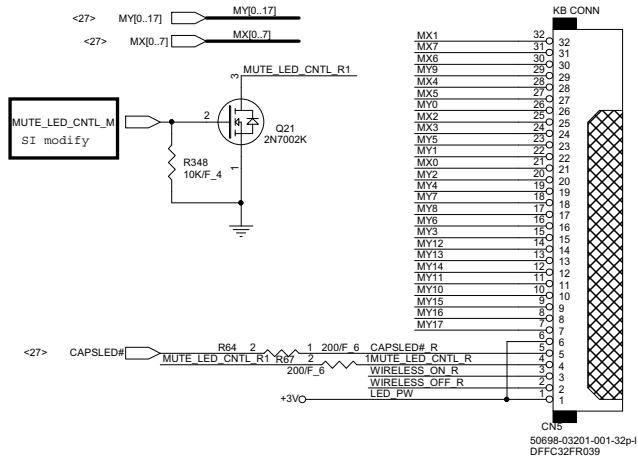
High : ODD power down
Low : ODD power on



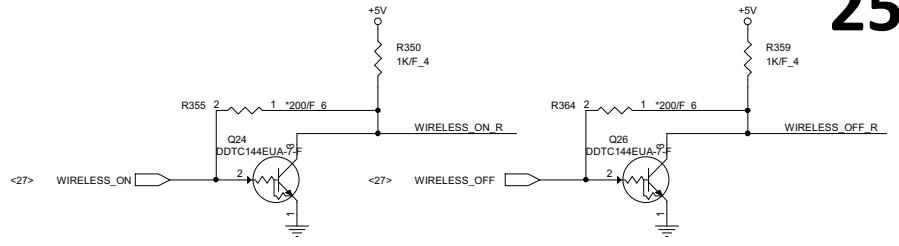
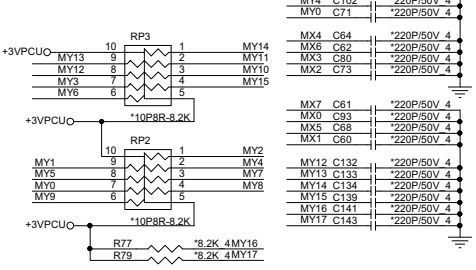
PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number CR RTS5237 & CR SOCKET	Rev 1A
Date: Friday, May 03, 2013	Sheet 23 of 40	

KEYBOARD Con.

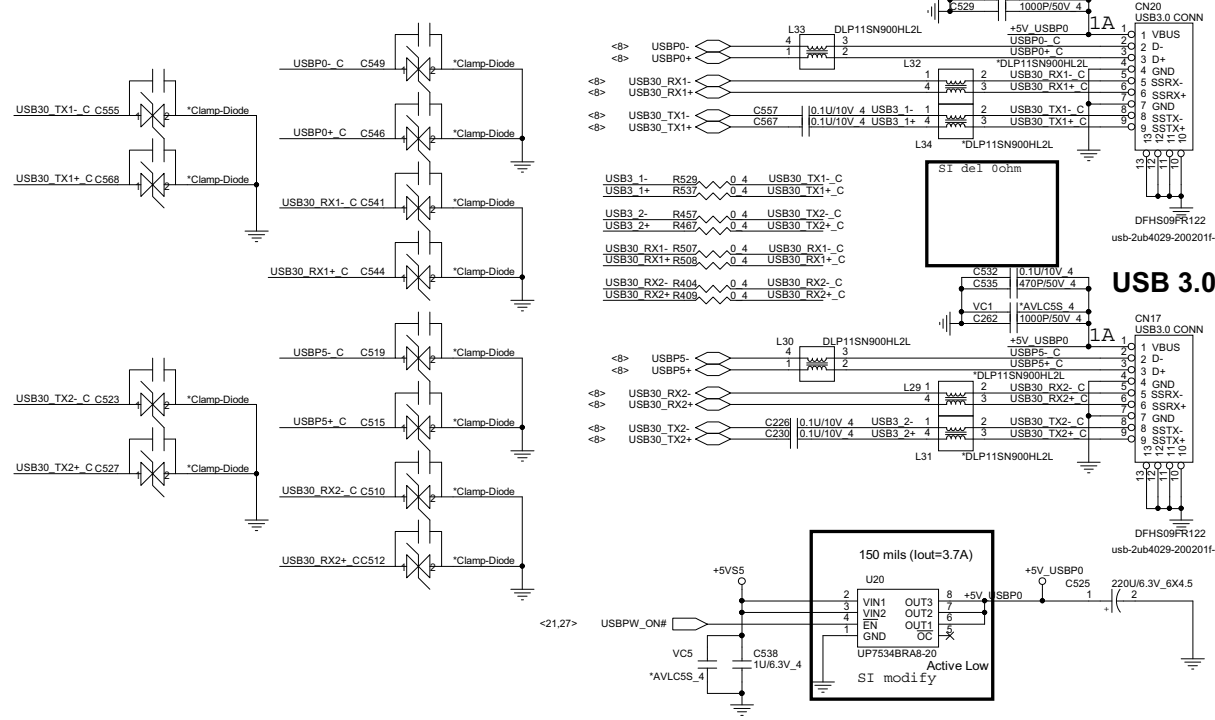


KEYBOARD PULL-UP

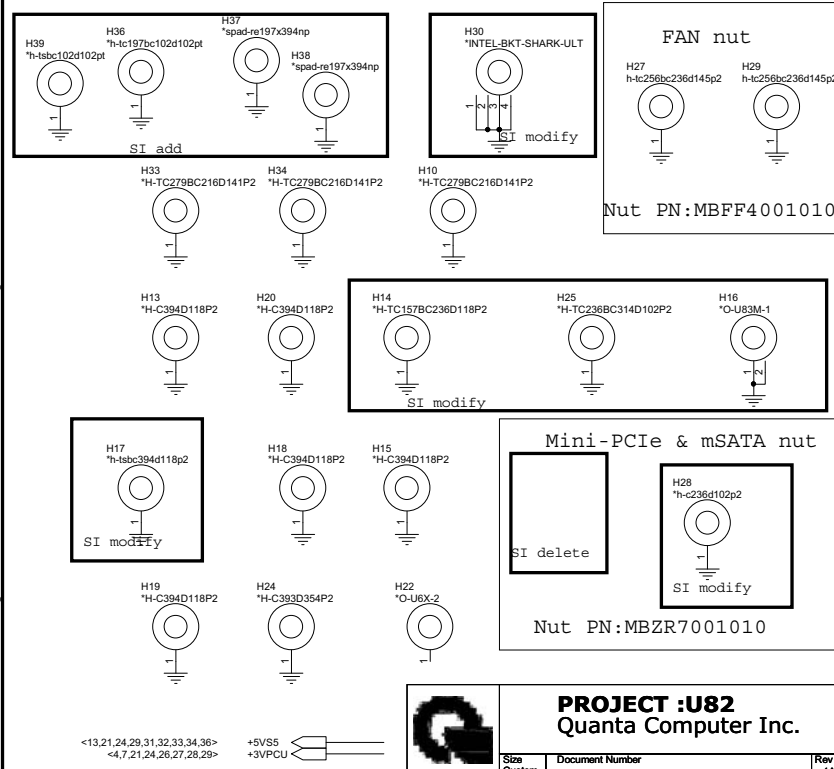


R6X Type

USB 2.0/3.0 Combo

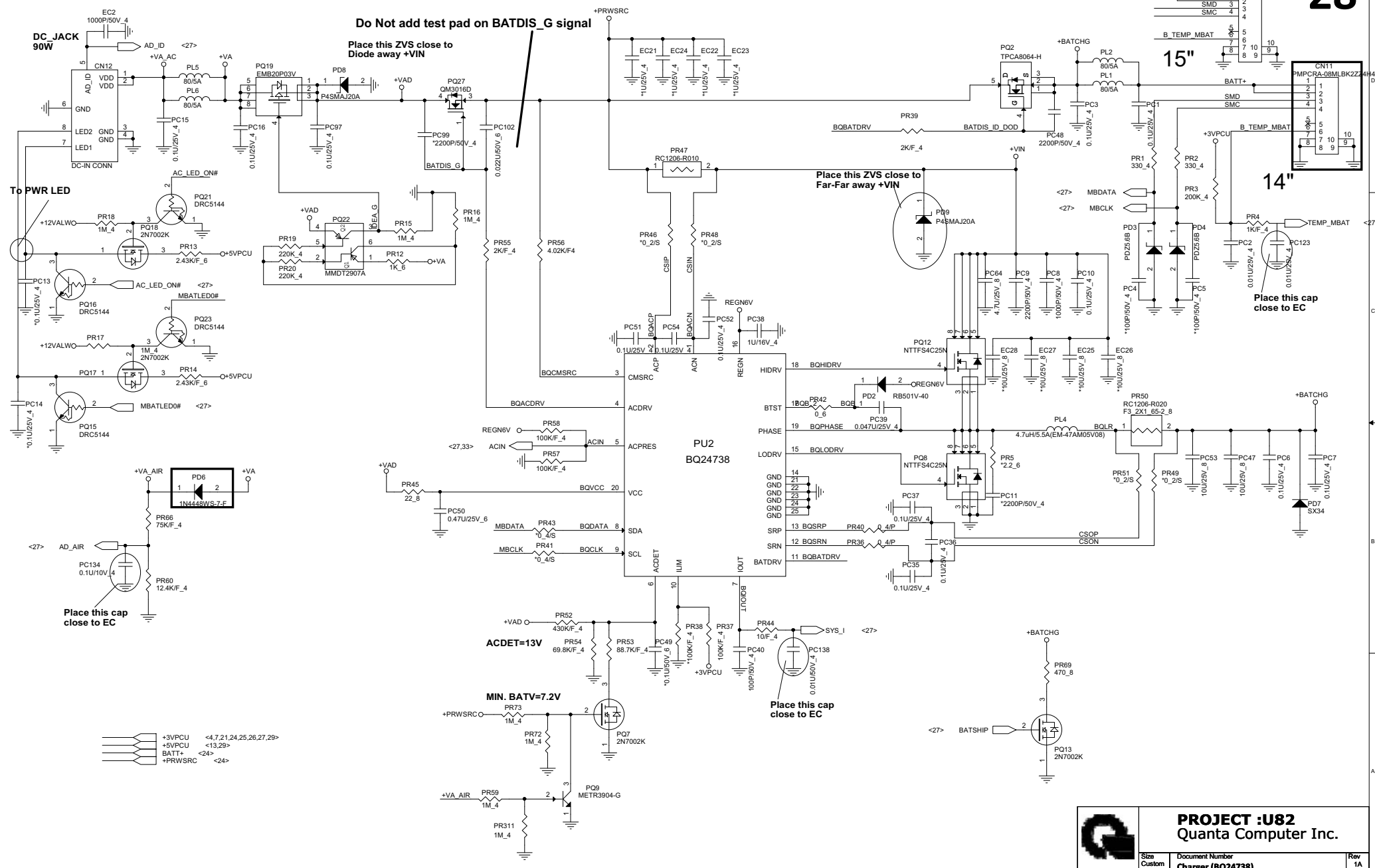


Hole



PROJECT :U82
 Quanta Computer Inc.

Size Custom	Document Number U8B3.0/KB	Rev 1A
Date: Monday, May 06, 2013	Sheet 25 of 40	



+3VPCU <4,7,21,24,25,26,27,29>
 +5VPCU <13,29>
 BATT+ <24>
 +PRWSRC <24>

ACDET=13V

MIN. BATV=7.2V

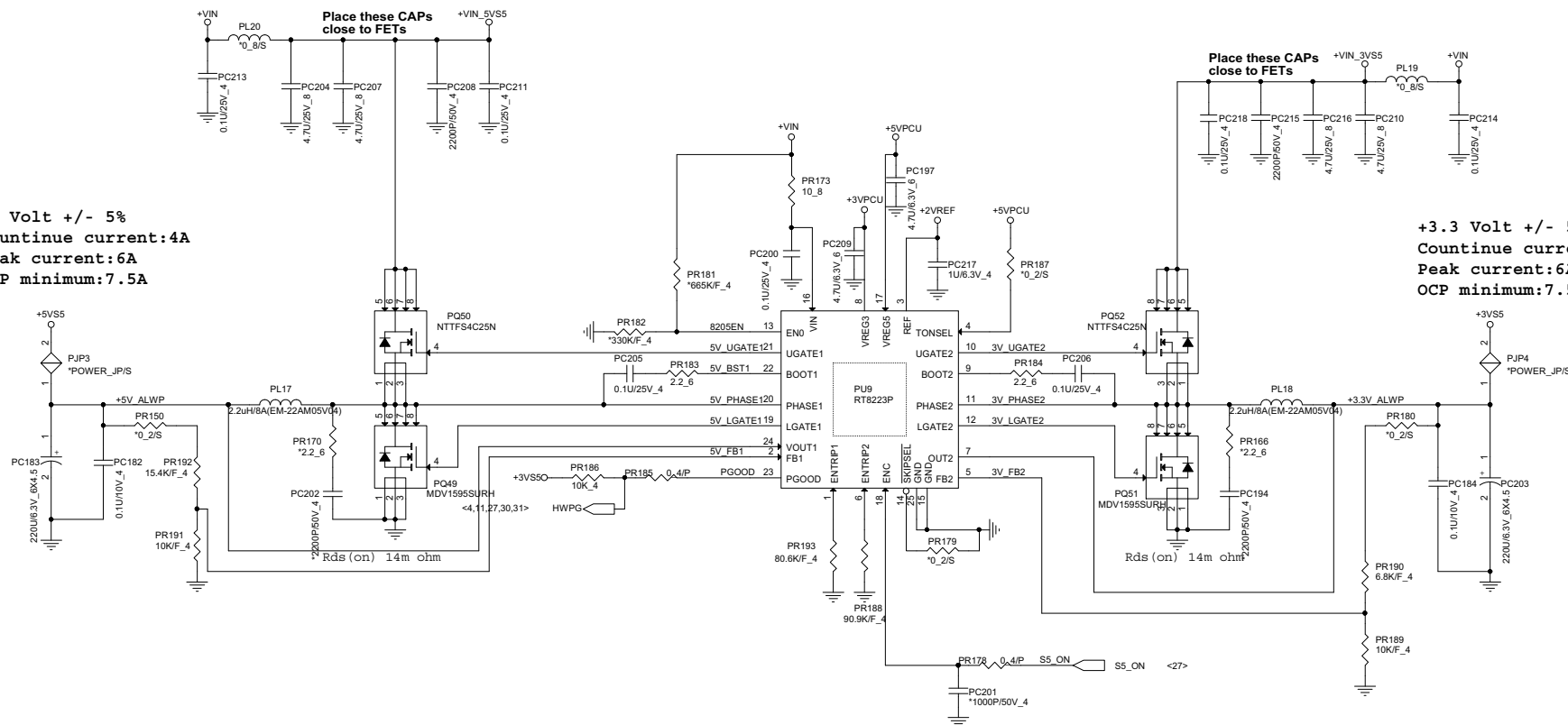
PROJECT :U82
Quanta Computer Inc.


Size Custom	Document Number Charger (BQ24738)	Rev 1A
Date: Friday, April 26, 2013		Sheet 28 of 40

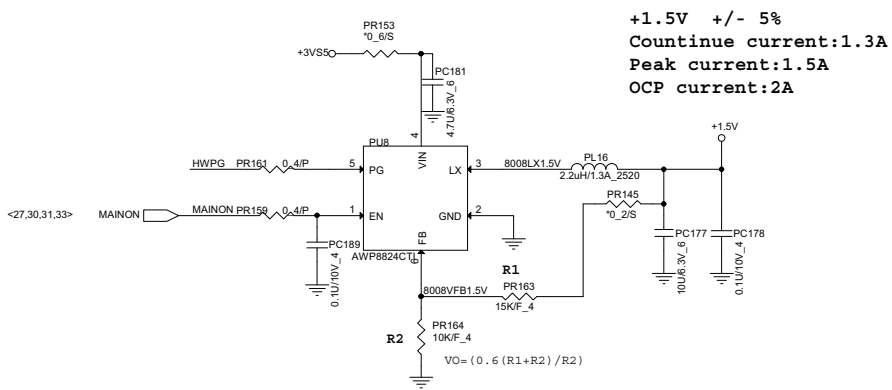
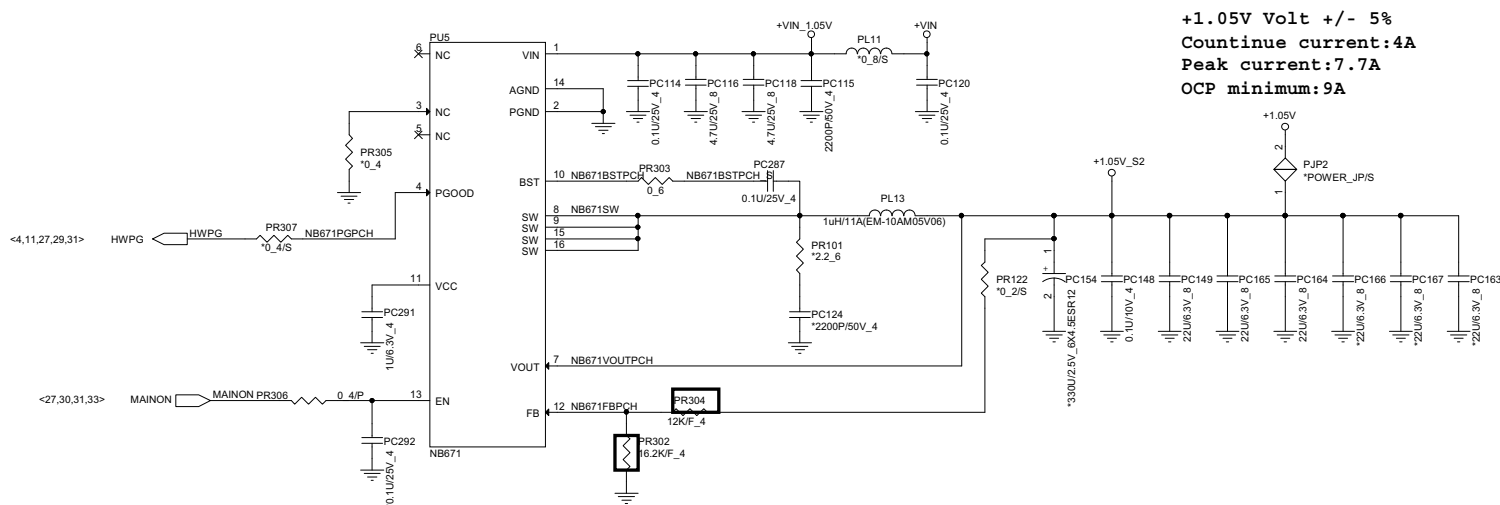
DC/DC +3VS5/+5VS5

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



	PROJECT :U82		Rev 1A
	Quanta Computer Inc.		
Size Custom	Document Number 3/5VPCU(RT8223P)		
Date: Friday, April 26, 2013	Sheet 29	of 40	

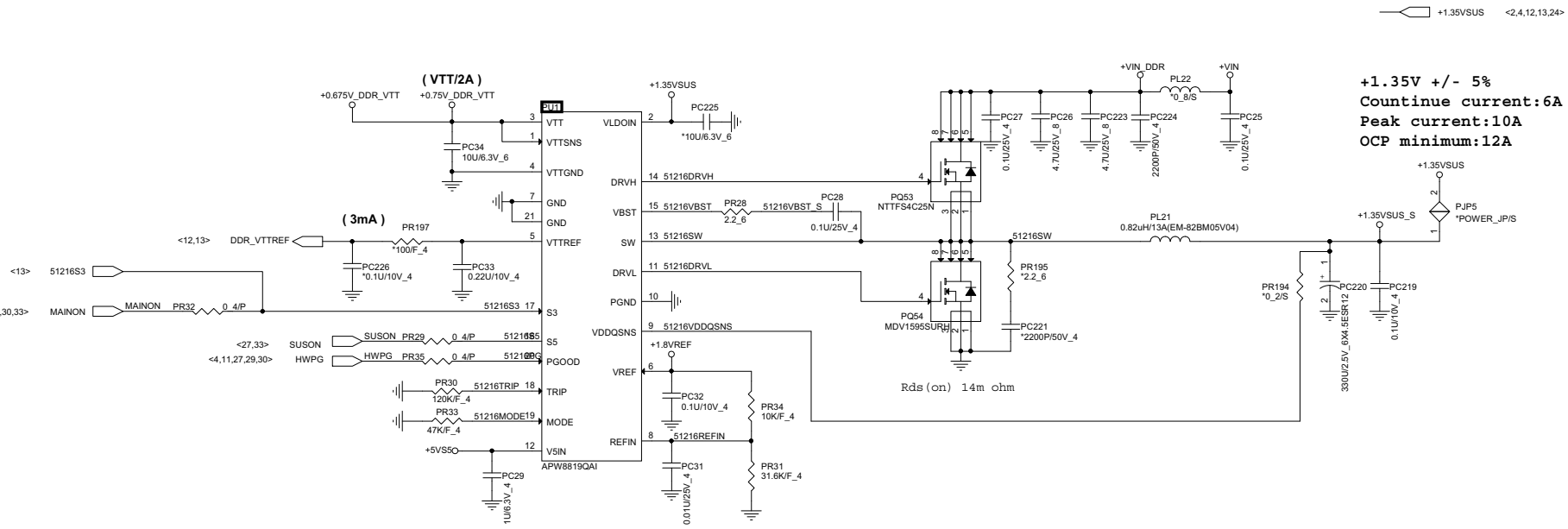



- +VIN <20,24,28,29,31,32,33,34,35,36>
- +3VS5 <6,9,10,11,24,26,29,33,35>
- +5VS5 <13,21,24,25,29,31,32,33,34,36>
- +5VPCU <13,28,29>

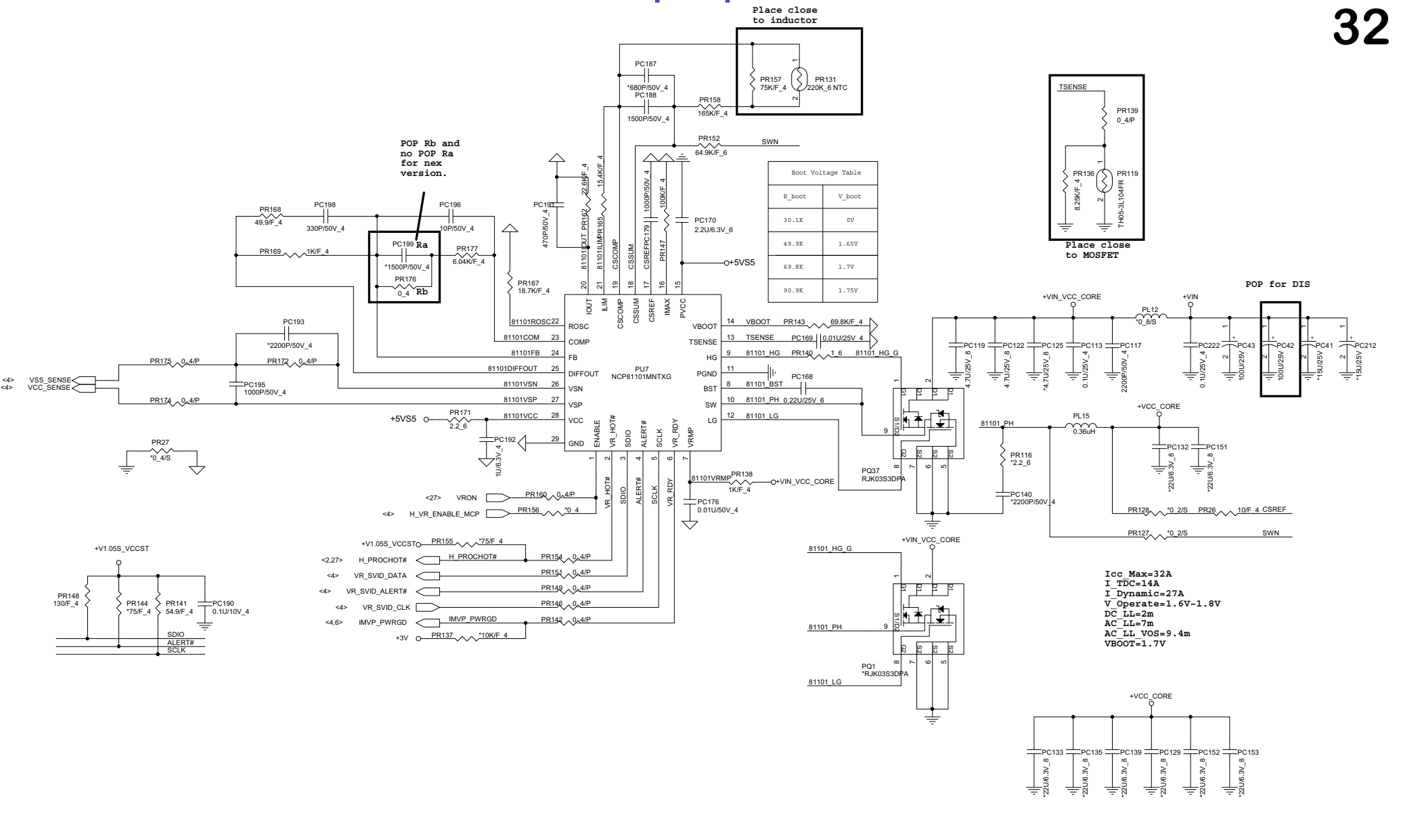


PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number +1.05V (NB671)/1.5V	Rev 1A
Date: Friday, April 26, 2013 Sheet 30 of 40		



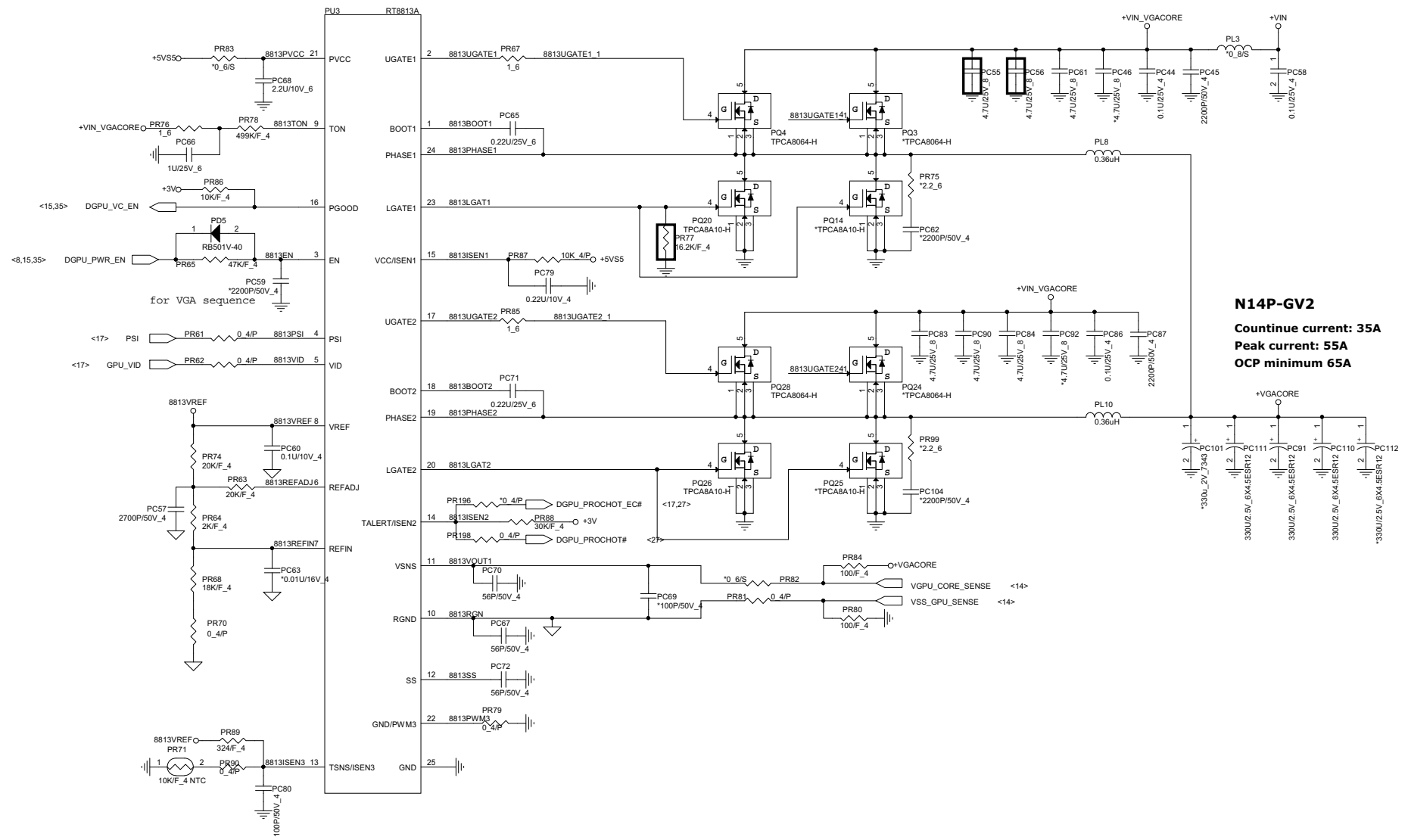
	PROJECT :U82 Quanta Computer Inc.	
	Size Custom Document Number DDR3 (APW8819)	Rev 1A
Date: Friday, April 26, 2013		Sheet 31 of 40



PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number CPU Core (NCP81101)JULT	Rev 1A
Date: Friday, April 26, 2013		Sheet 32 of 40

VGA Core

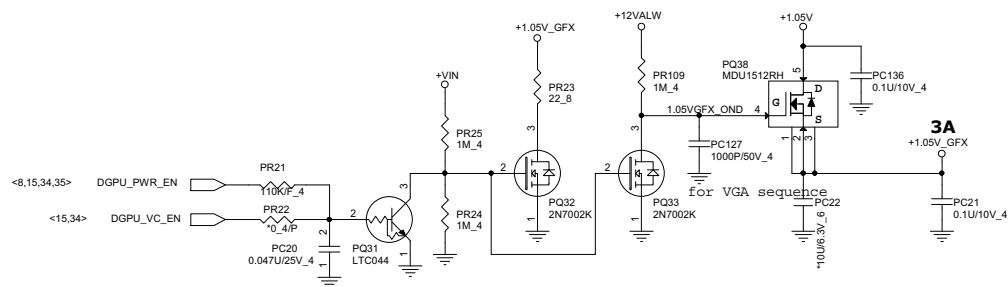
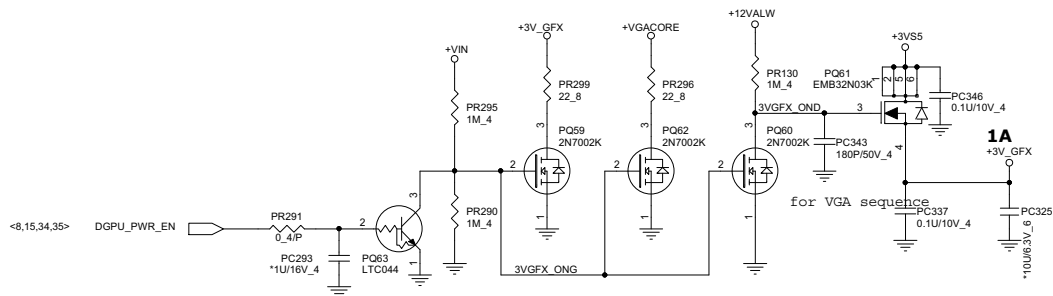


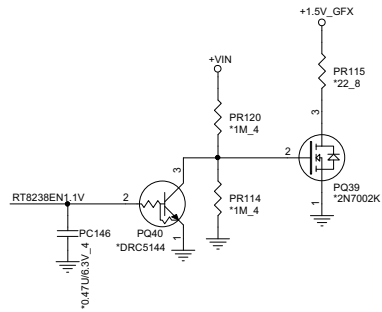
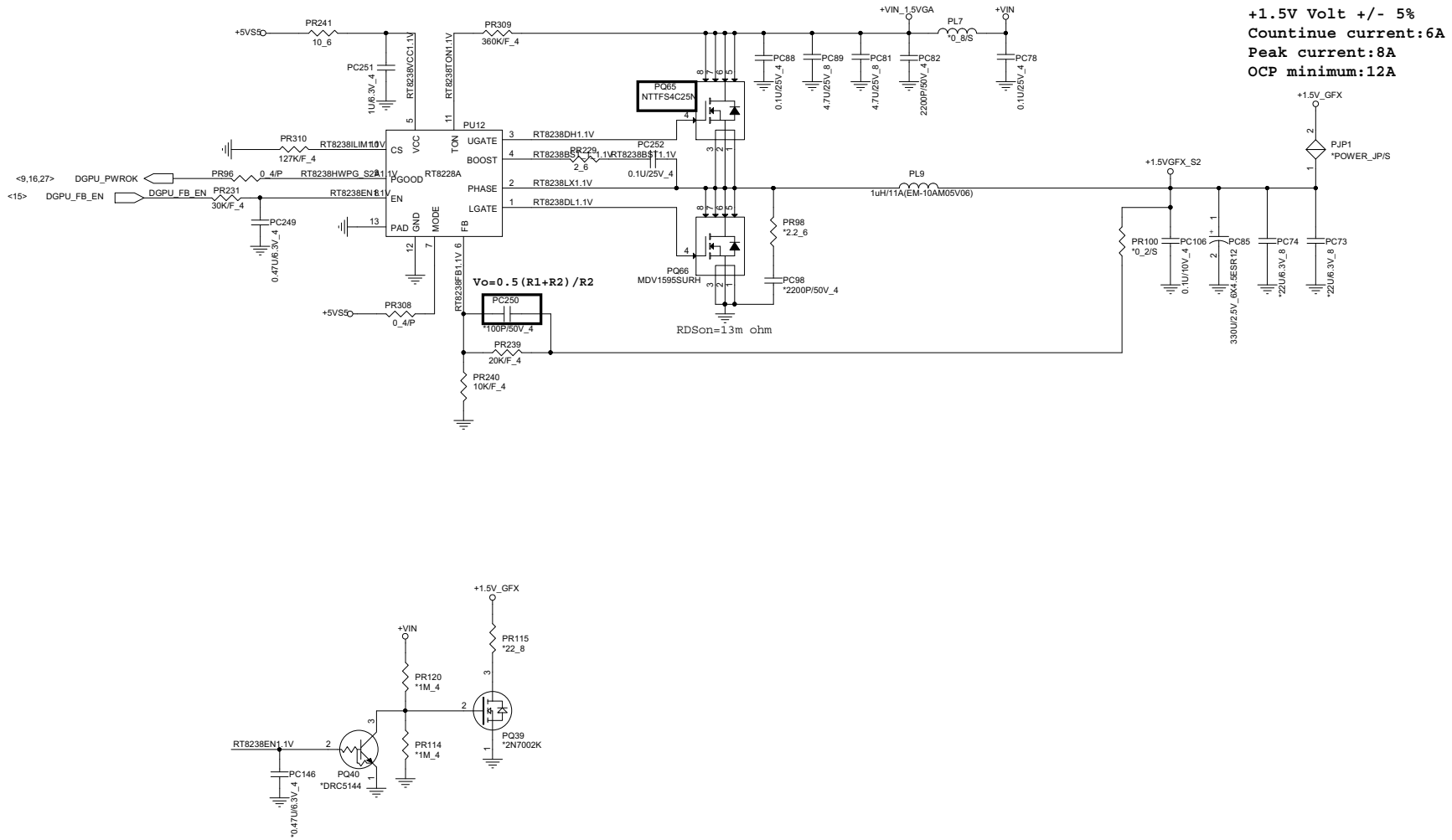
N14P-GV2
Continue current: 35A
Peak current: 55A
OCV minimum 65A




PROJECT :U82
Quanta Computer Inc.

Size Custom	Document Number +VGACORE (RT8813A)	Rev 1A
Date Friday, April 26, 2013	Sheet 34	of 40





	PROJECT :U82 Quanta Computer Inc.	
	Document Number +1.5V_VGA(RT8228)	Rev 1A
Date: Friday, April 26, 2013	Sheet 36 of 40	

USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON# (from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON# (from EC)
PORT3	NC	N/A
PORT4	NC	N/A

SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON# (from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON# (from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON# (from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON (from EC)

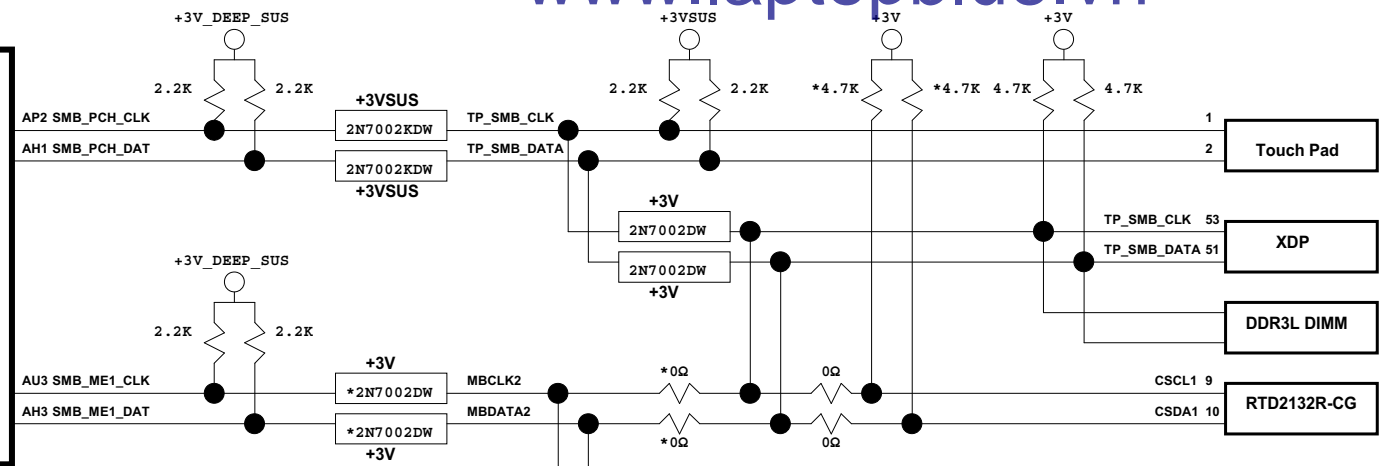
PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	



PROJECT :U82
Quanta Computer Inc.

Size	Document Number	Rev 1A
Date: Friday, April 26, 2013		Sheet 37 of 40

**Haswell
ULT**



**EC
KB9010QF**

