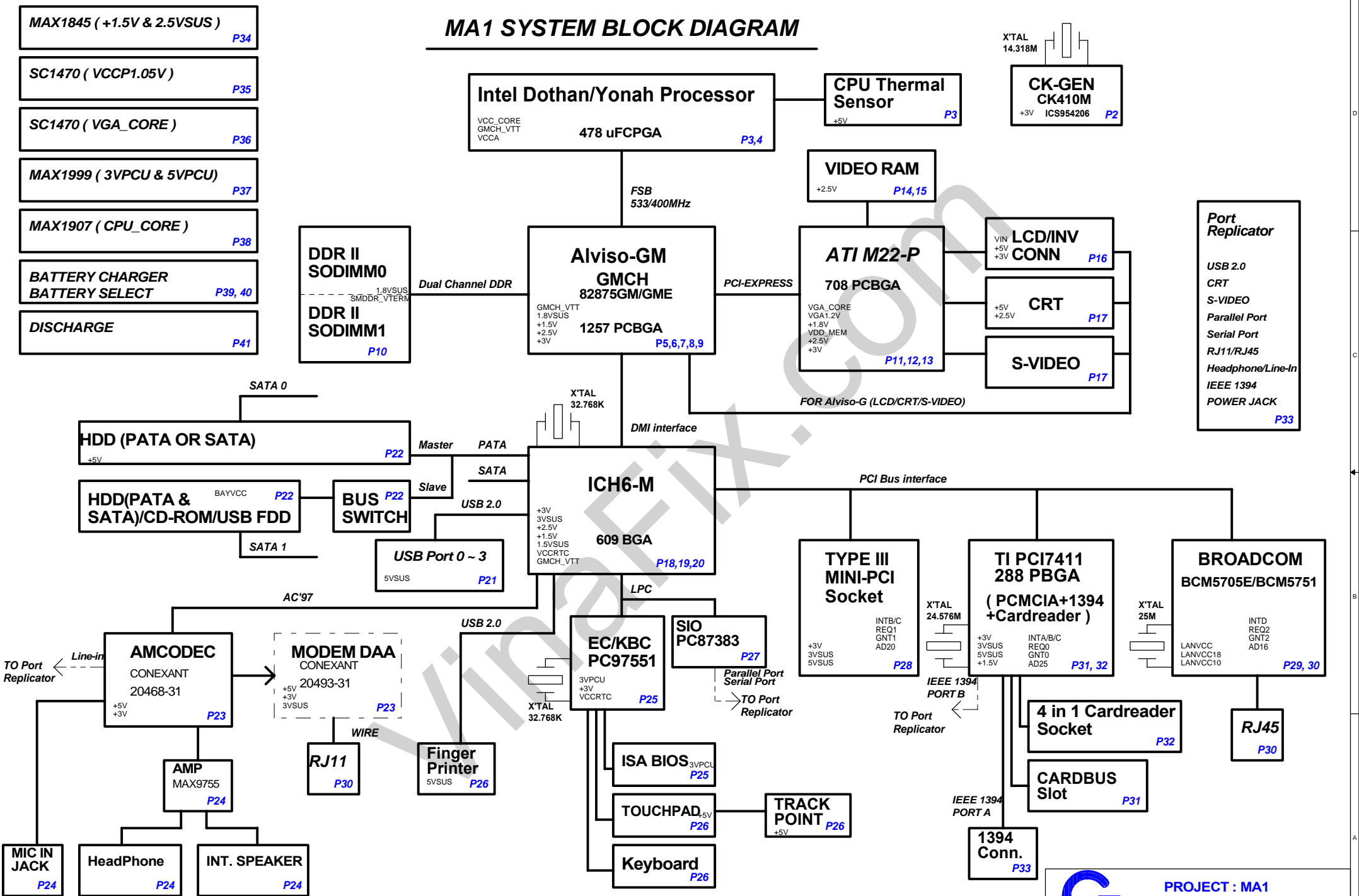
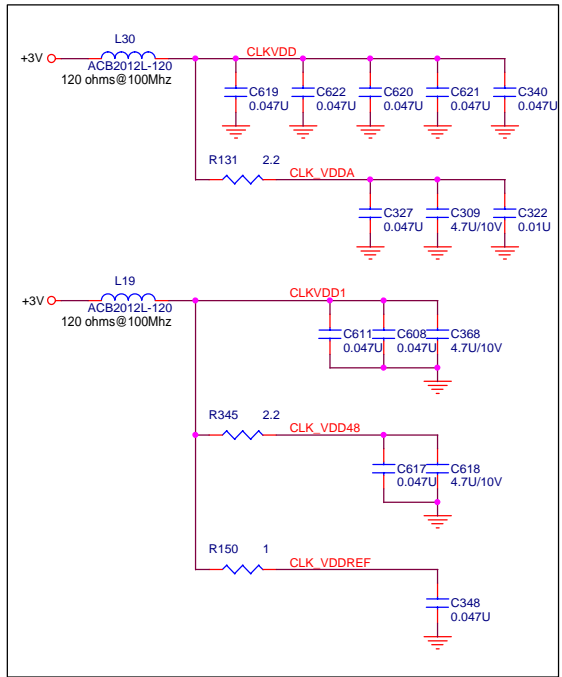
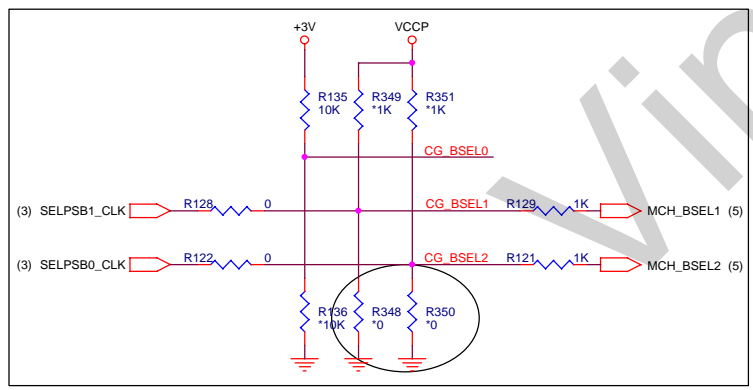


# MA1 SYSTEM BLOCK DIAGRAM

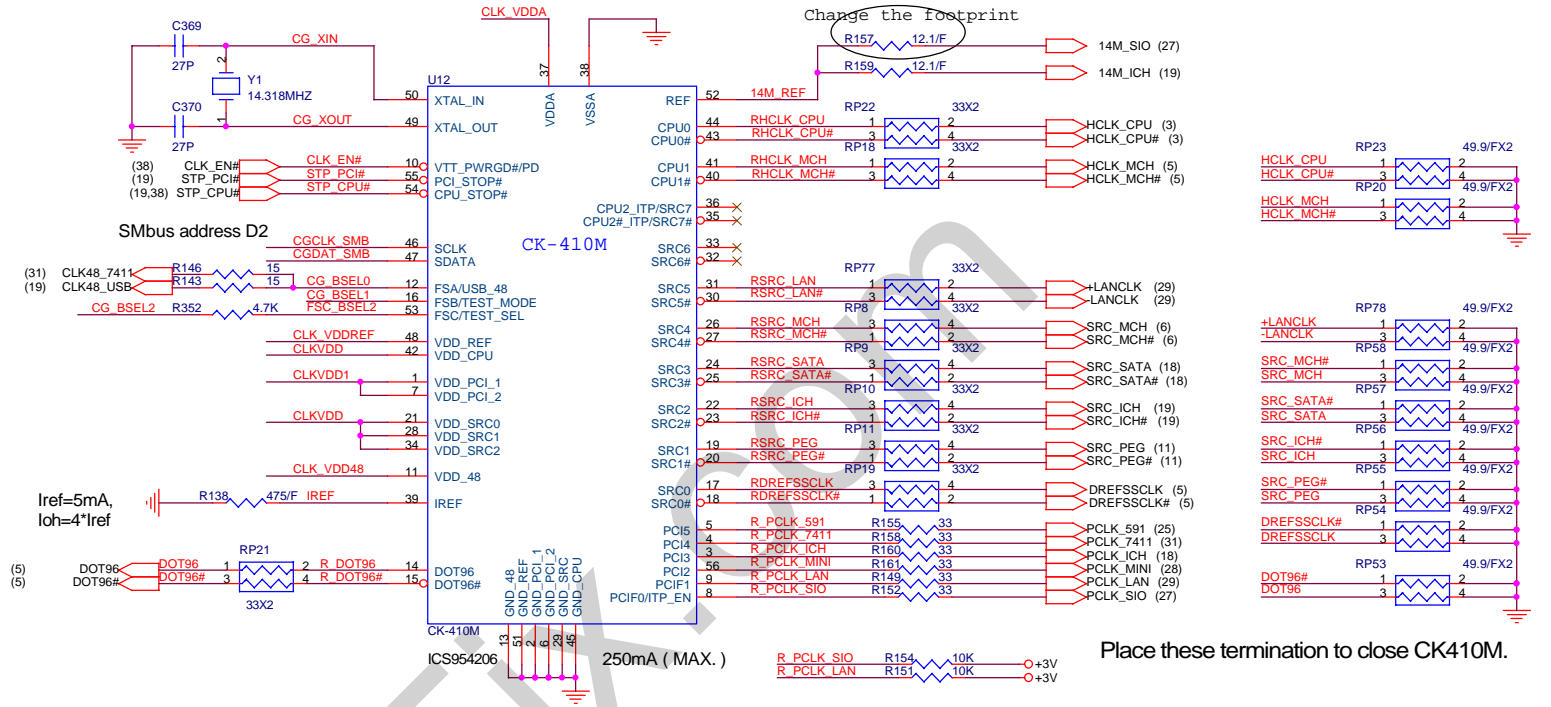




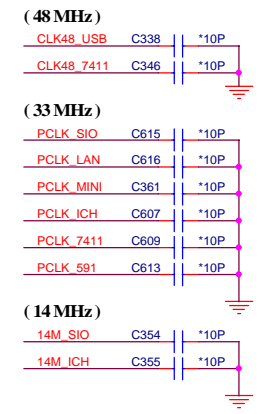
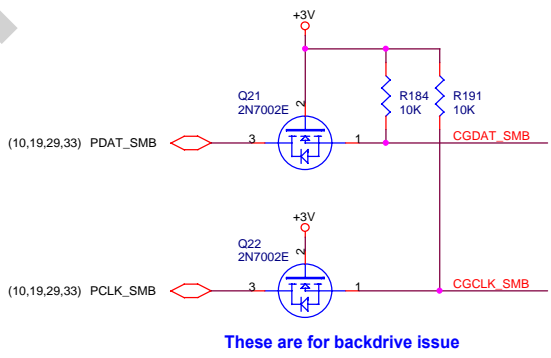
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	Default
0	0	1	133	100	33	
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			

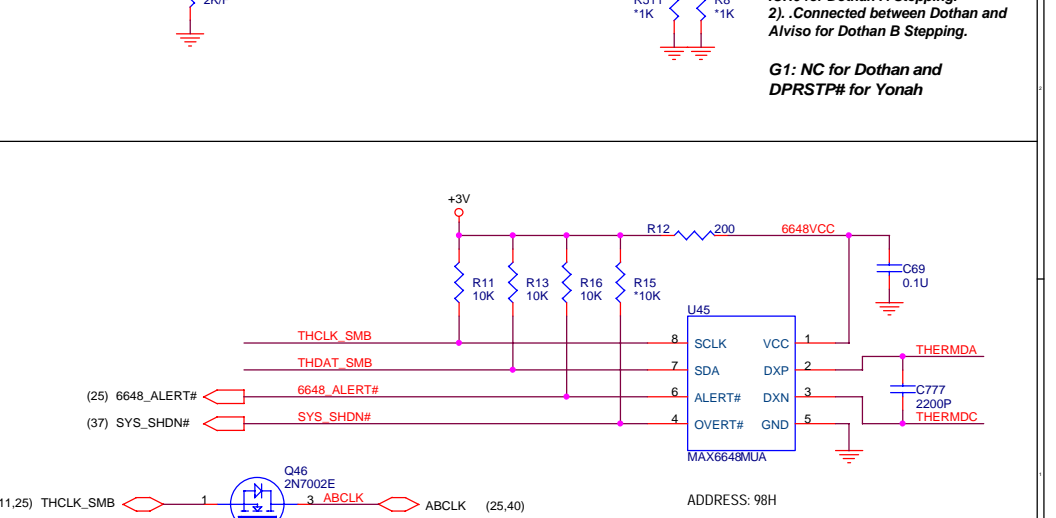
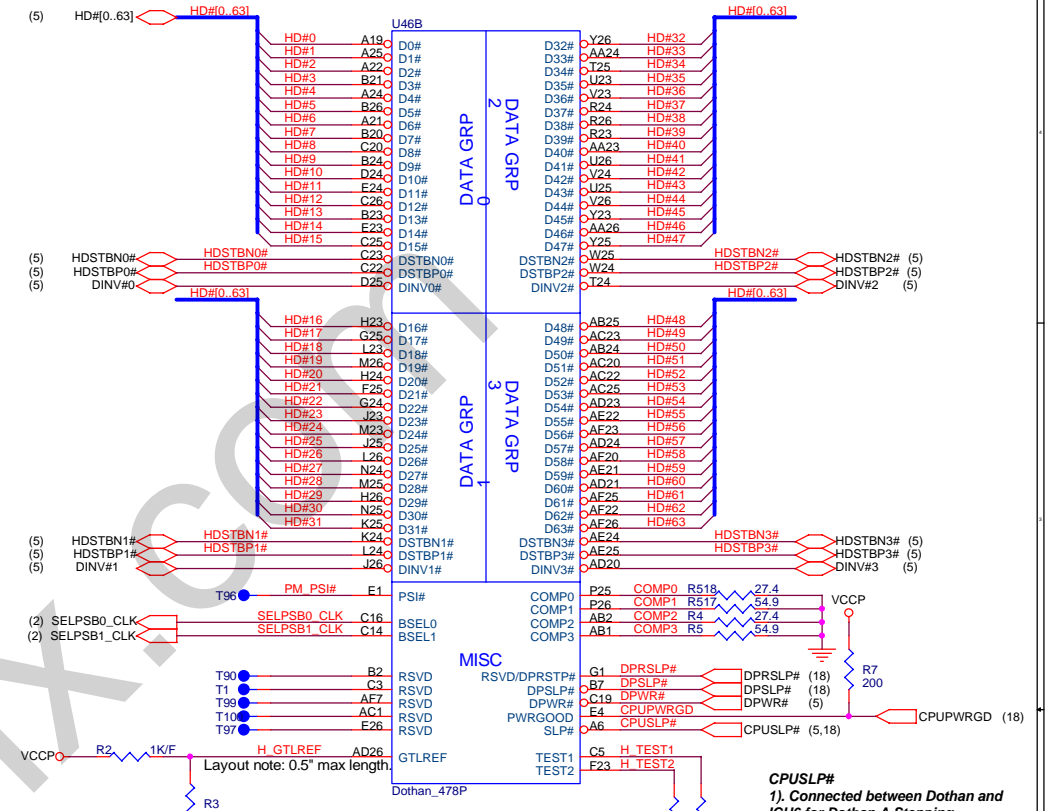
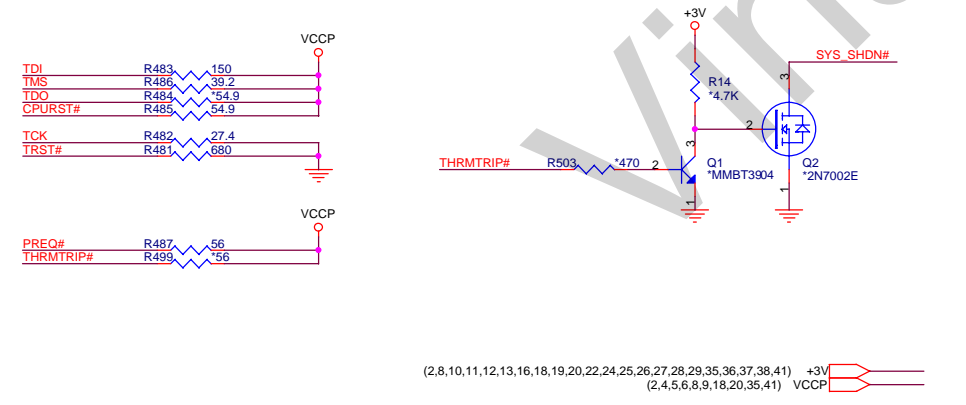
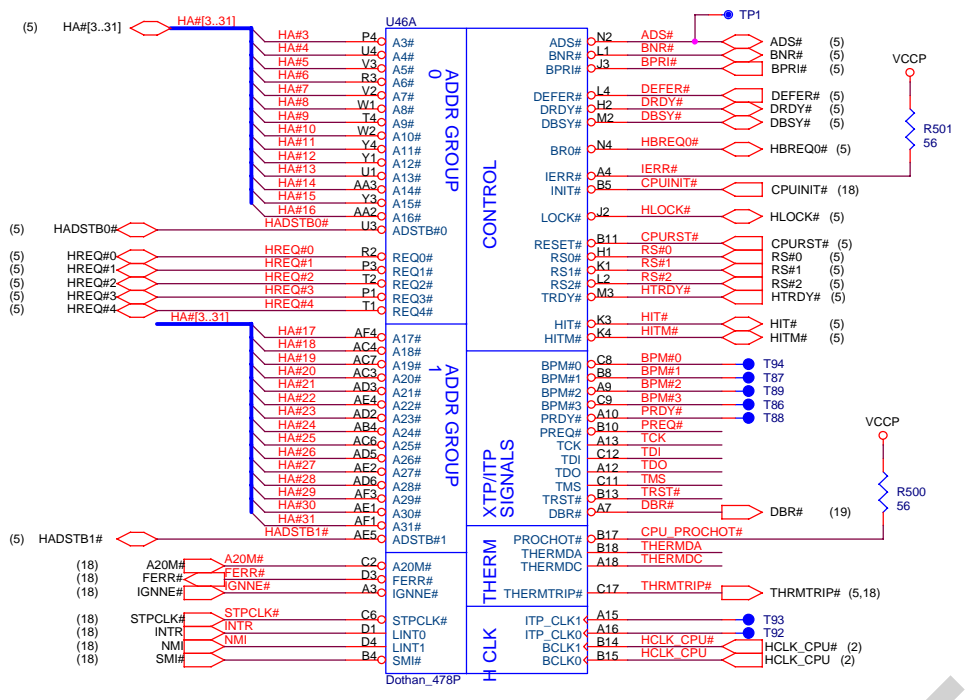


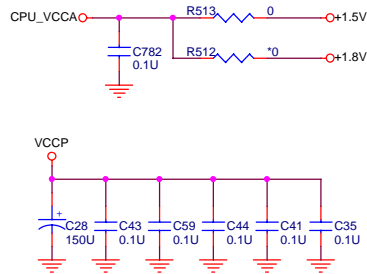
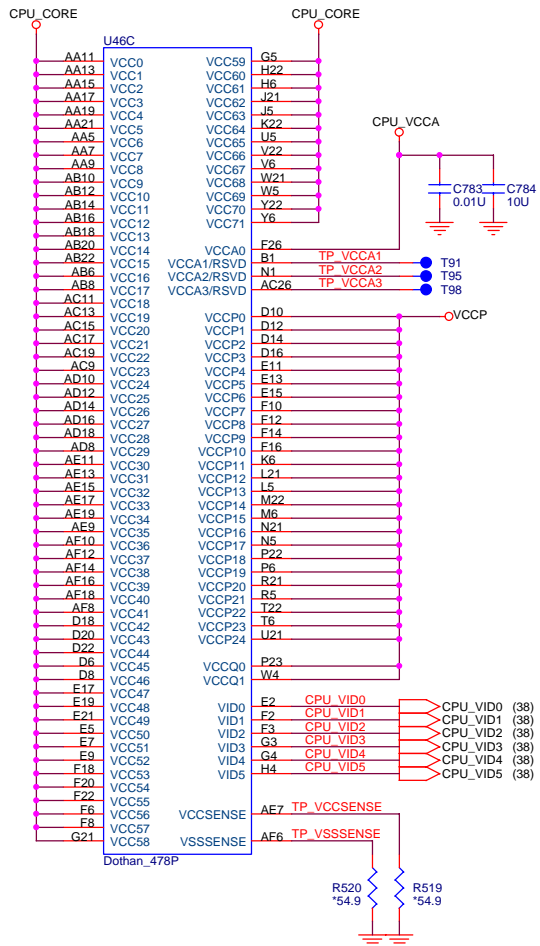
Place these termination to close CK410M.



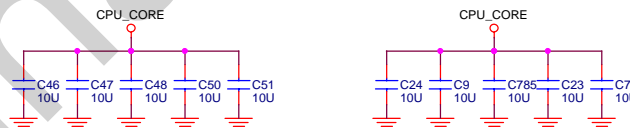
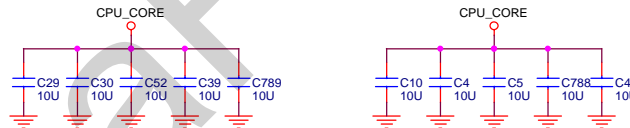
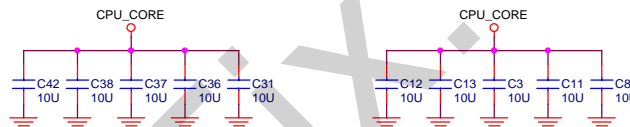
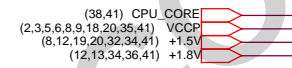
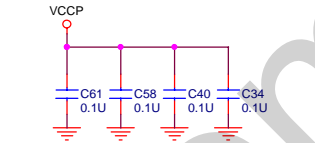
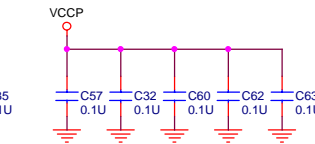
250mA ( MAX. )





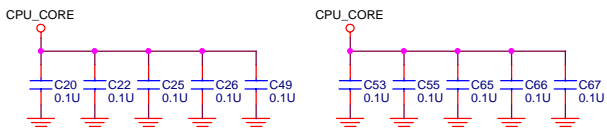
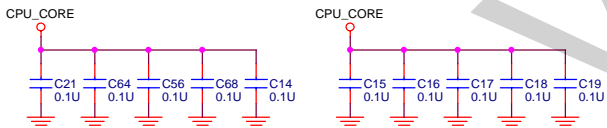


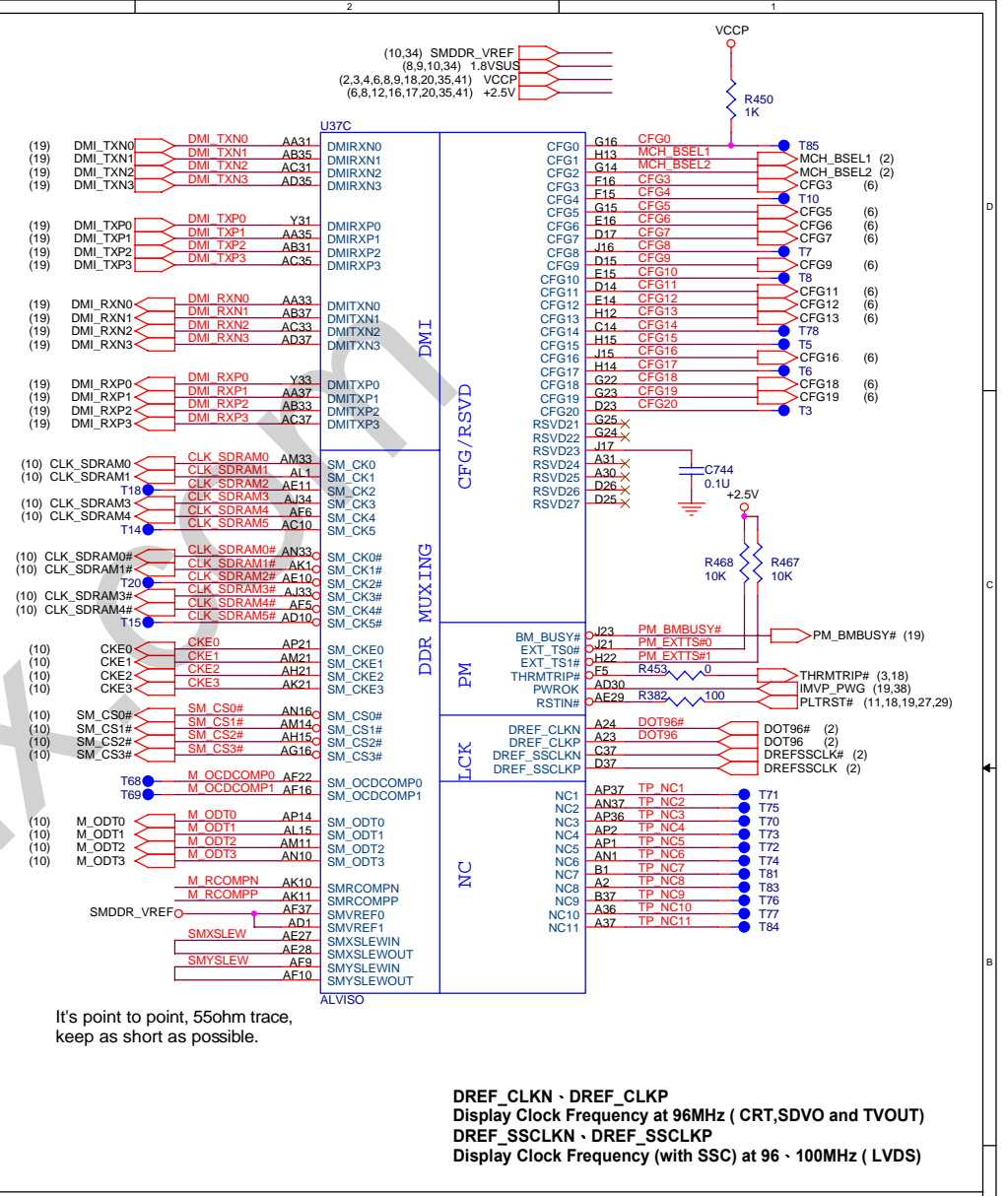
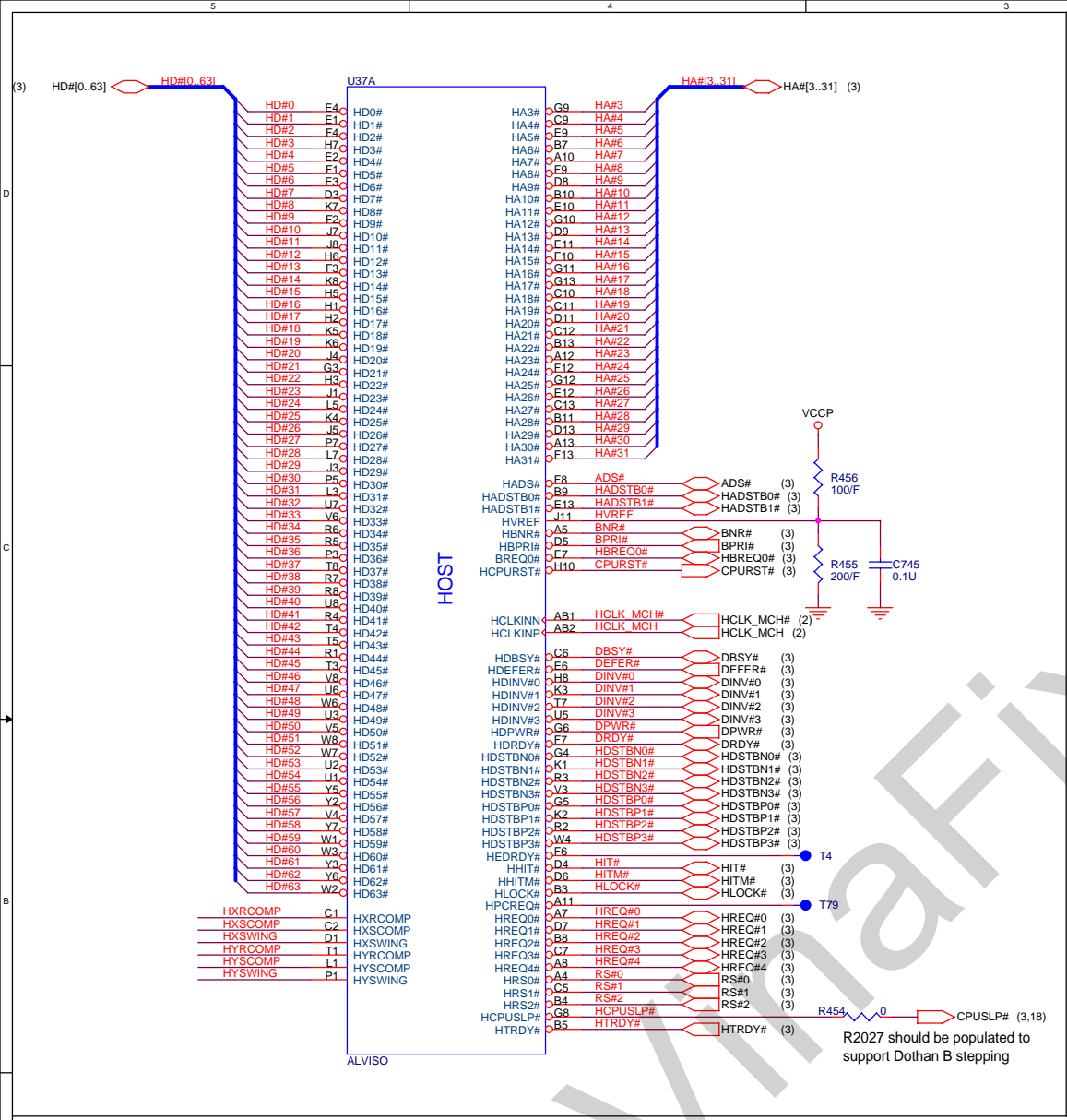
270U/2.0V(CC7343) 12 mQ \* 4  
04/13 Intel recommend



10U/6.3V/X5R(CC0805)  
5 mOhm\*35  
--> 10U/4V/X5R(CC0603)  
Murata

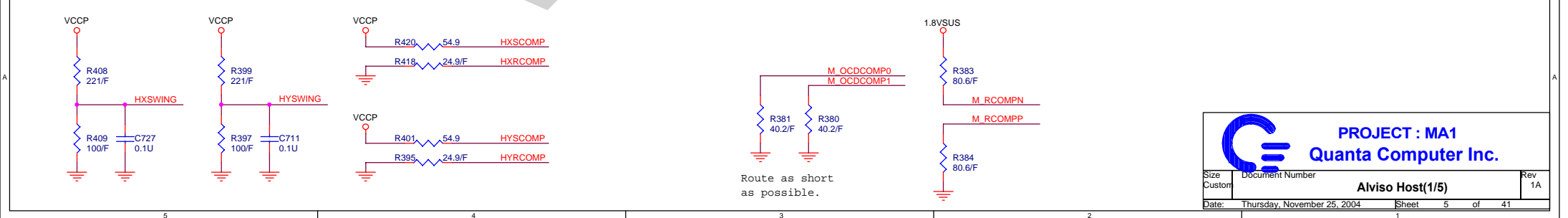
U46D			
A2	VSS0	VSS97	D13
A5	VSS1	VSS98	D15
A8	VSS2	VSS99	D17
A11	VSS3	VSS100	D19
A14	VSS4	VSS101	D21
A17	VSS5	VSS102	D23
A20	VSS6	VSS103	D26
A23	VSS7	VSS104	E3
A26	VSS8	VSS105	E6
AA1	VSS9	VSS106	E8
AA4	VSS10	VSS107	E10
AA6	VSS11	VSS108	E12
AA8	VSS12	VSS109	E14
AA10	VSS13	VSS110	E16
AA12	VSS14	VSS111	E18
AA14	VSS15	VSS112	E20
AA16	VSS16	VSS113	E22
AA18	VSS17	VSS114	E25
AA20	VSS18	VSS115	F4
AA22	VSS19	VSS116	F5
AA25	VSS20	VSS117	F7
AB3	VSS21	VSS118	F9
AB5	VSS22	VSS119	F11
AB7	VSS23	VSS120	F13
AB9	VSS24	VSS121	F15
AB11	VSS25	VSS122	F17
AB13	VSS26	VSS123	F19
AB15	VSS27	VSS124	F21
AB17	VSS28	VSS125	F24
AB19	VSS29	VSS126	G2
AB21	VSS30	VSS127	G6
AB23	VSS31	VSS128	G22
AB26	VSS32	VSS129	G23
AC2	VSS33	VSS130	G26
AC5	VSS34	VSS131	G26
AC8	VSS35	VSS132	H3
AC10	VSS36	VSS133	H5
AC12	VSS37	VSS134	H21
AC14	VSS38	VSS135	H25
AC16	VSS39	VSS136	J1
AC18	VSS40	VSS137	J4
AC21	VSS41	VSS138	J6
AC24	VSS42	VSS139	J22
AD1	VSS43	VSS140	J22
AD4	VSS44	VSS141	K2
AD7	VSS45	VSS142	K5
AD9	VSS46	VSS143	K21
AD11	VSS47	VSS144	K23
AD13	VSS48	VSS145	K26
AD15	VSS49	VSS146	L3
AD17	VSS50	VSS147	L6
AD19	VSS51	VSS148	L22
AD22	VSS52	VSS149	L25
AD25	VSS53	VSS150	M1
AE3	VSS54	VSS151	M4
AE6	VSS55	VSS152	M5
AE8	VSS56	VSS153	M21
AE10	VSS57	VSS154	M24
AE12	VSS58	VSS155	N3
AE14	VSS59	VSS156	N6
AE16	VSS60	VSS157	N22
AE18	VSS61	VSS158	N23
AE20	VSS62	VSS159	N26
AE23	VSS63	VSS160	P2
AE26	VSS64	VSS161	P5
AF2	VSS65	VSS162	P21
AF5	VSS66	VSS163	P24
AF9	VSS67	VSS164	R1
AF11	VSS68	VSS165	R4
AF13	VSS69	VSS166	R6
AF15	VSS70	VSS167	R22
AF17	VSS71	VSS168	R25
AF19	VSS72	VSS169	T3
AF21	VSS73	VSS170	T5
AF24	VSS74	VSS171	T21
B3	VSS75	VSS172	T23
B6	VSS76	VSS173	T26
B9	VSS77	VSS174	U2
B12	VSS78	VSS175	U6
B16	VSS79	VSS176	U22
B19	VSS80	VSS177	U24
B22	VSS81	VSS178	V1
B25	VSS82	VSS179	V4
C1	VSS83	VSS180	V5
C4	VSS84	VSS181	V21
C7	VSS85	VSS182	V25
C10	VSS86	VSS183	W3
C13	VSS87	VSS184	W6
C15	VSS88	VSS185	W22
C18	VSS89	VSS186	W23
C21	VSS90	VSS187	W26
C24	VSS91	VSS188	Y2
D2	VSS92	VSS189	Y5
D5	VSS93	VSS190	Y21
D7	VSS94	VSS191	Y24
D9	VSS95		
D11	VSS96		



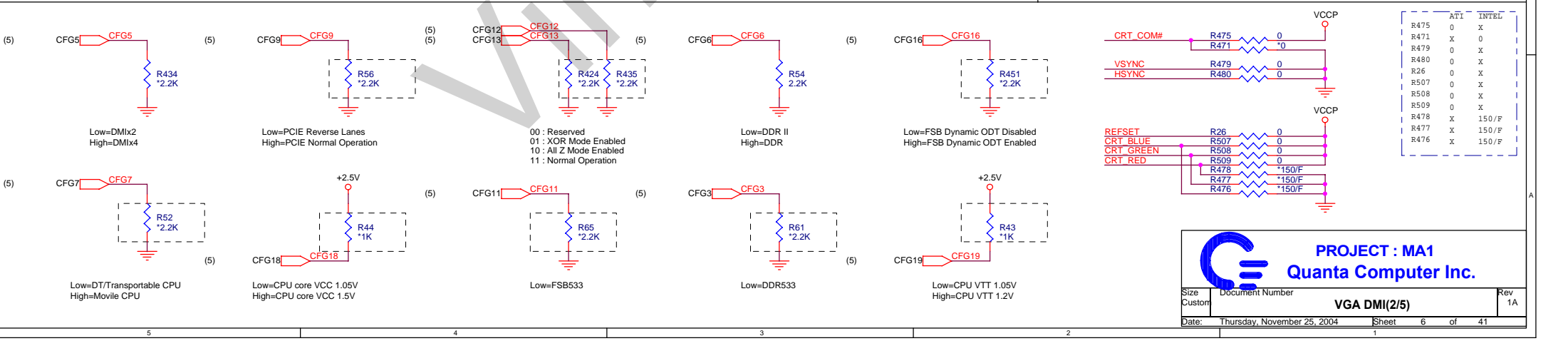
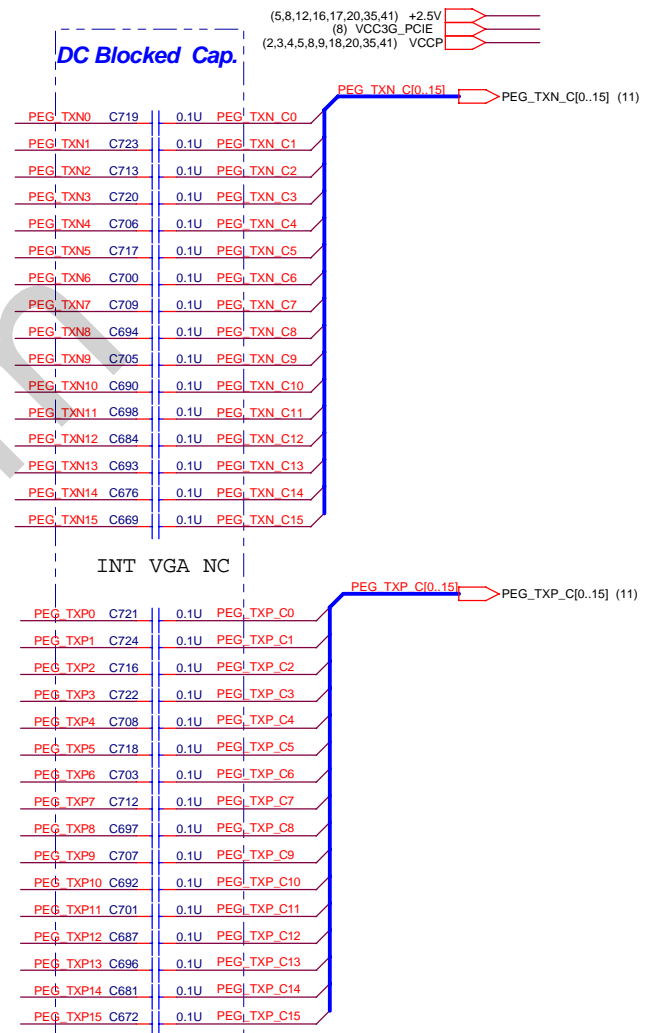
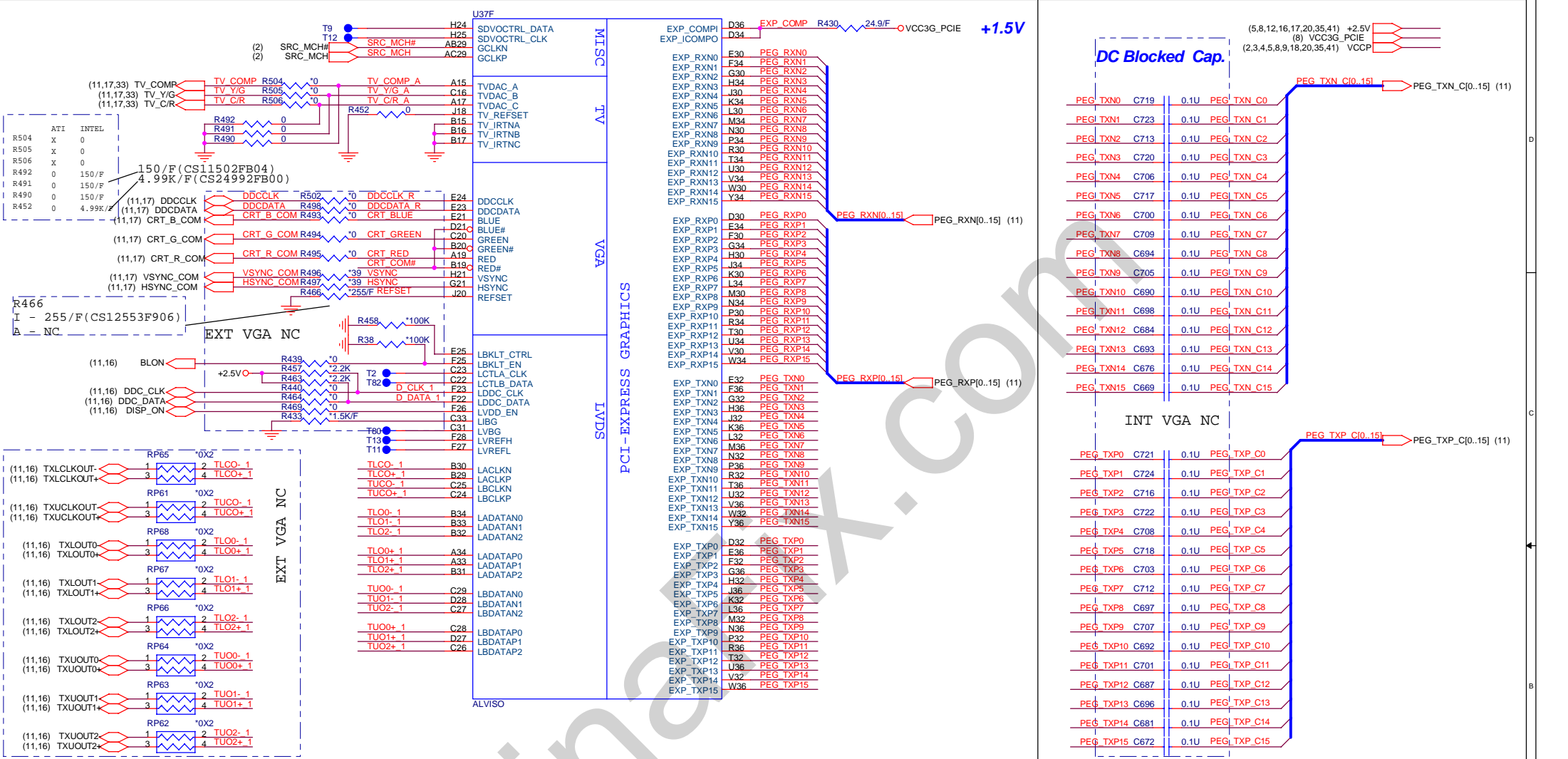


It's point to point, 55ohm trace,  
keep as short as possible.

**DREF\_CLKN · DREF\_CLKP**  
Display Clock Frequency at 96MHz ( CRT,SDVO and TVOUT)  
**DREF\_SSCLKN · DREF\_SSCLKP**  
Display Clock Frequency (with SSC) at 96 · 100MHz ( LVDS)



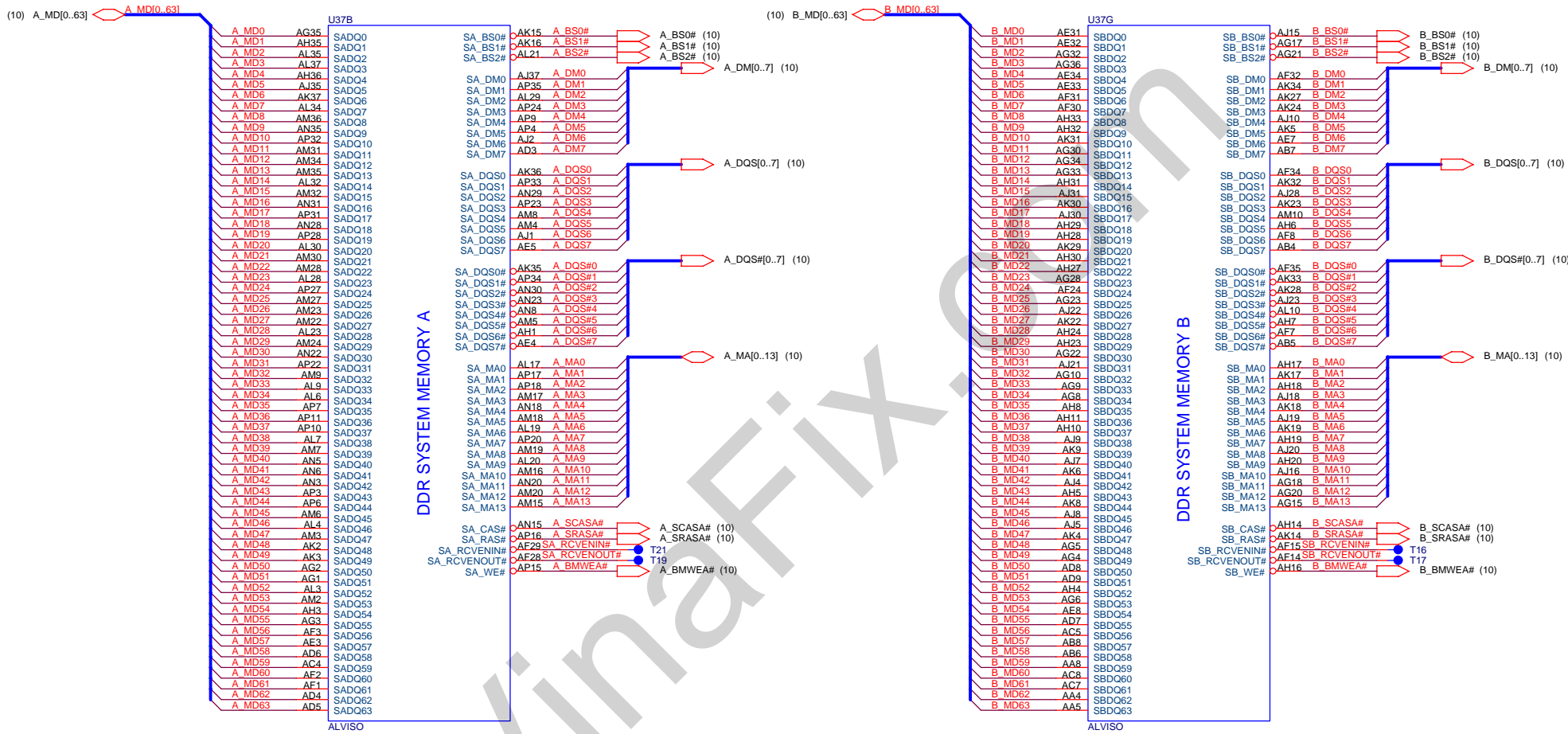
Size	Document Number	Rev
Custom	Alviso Host(1/5)	1A
Date:	Thursday, November 25, 2004	Sheet 5 of 41



**PROJECT : MA1**  
**Quanta Computer Inc.**

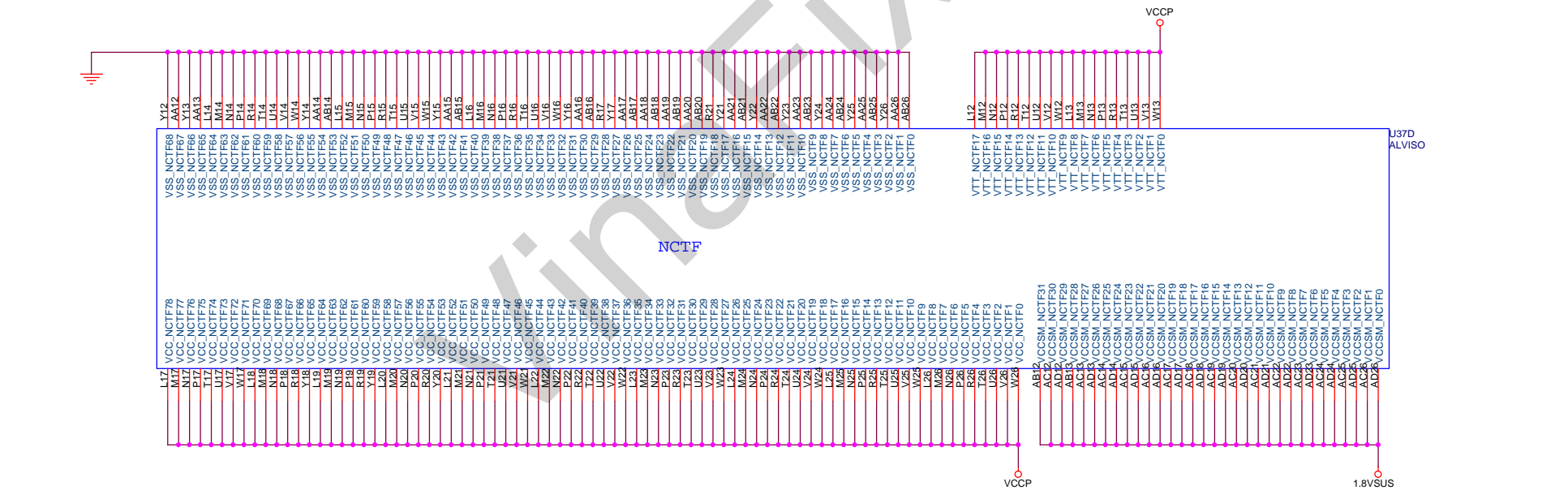
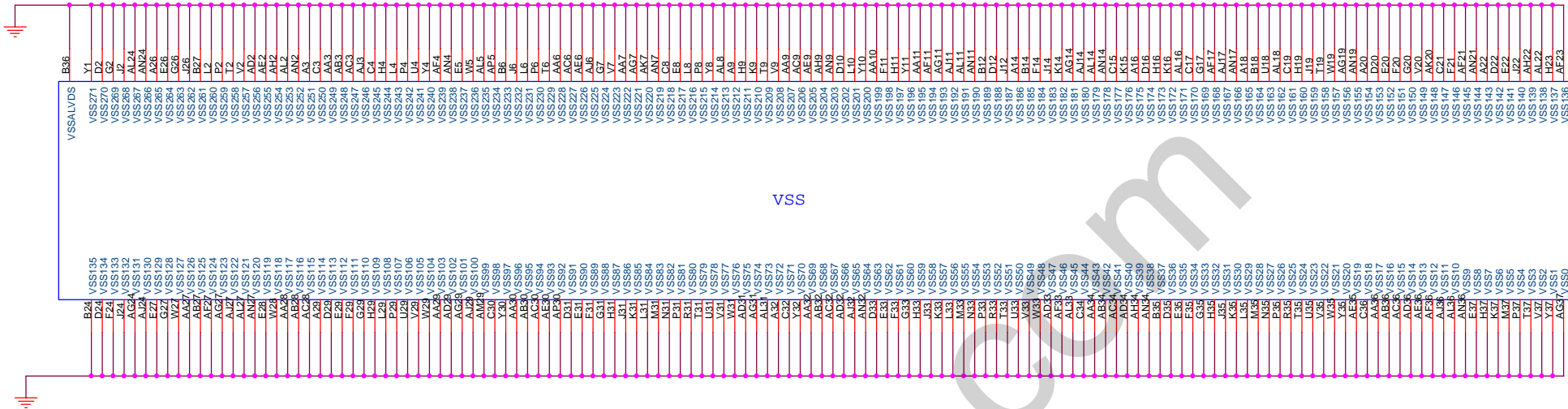
Size: Custom Document Number: **VGA DMI(2/5)** Rev: 1A

Date: Thursday, November 25, 2004 Sheet: 6 of 41







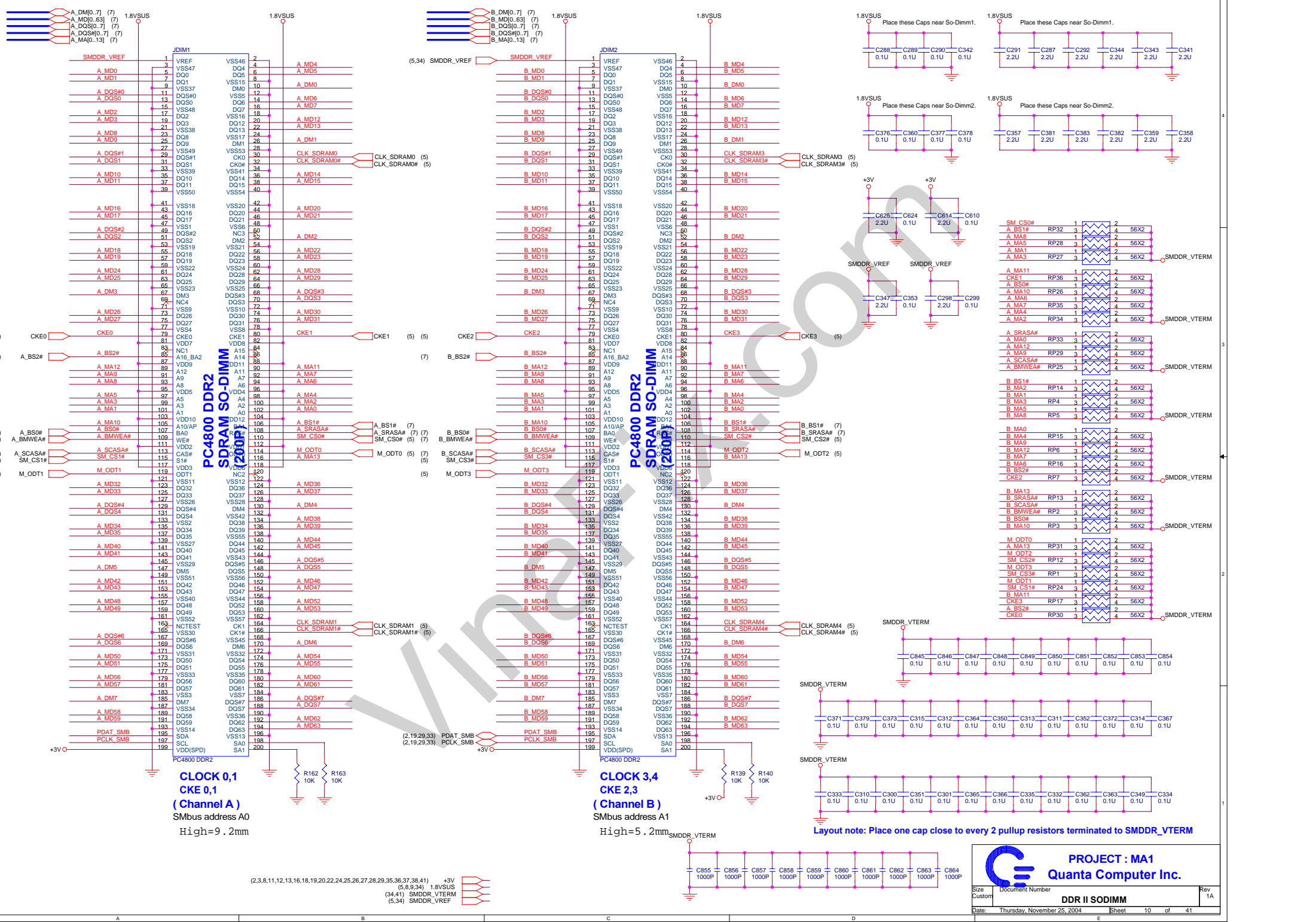


U37E  
ALVISO

U37D  
ALVISO

**PROJECT : MA1**  
**Quanta Computer Inc.**

Size Custom	Document Number	VSS/NCTF(5/5)	Rev 1A
Date: Thursday, November 25, 2004	Sheet	9	of 41



**CLOCK 0,1**  
**CKE 0,1**  
**(Channel A)**  
 Smbus address A0  
 High=9 . 2mm

**CLOCK 3,4**  
**CKE 2,3**  
**(Channel B)**  
 Smbus address A1  
 High=5 . 2mm

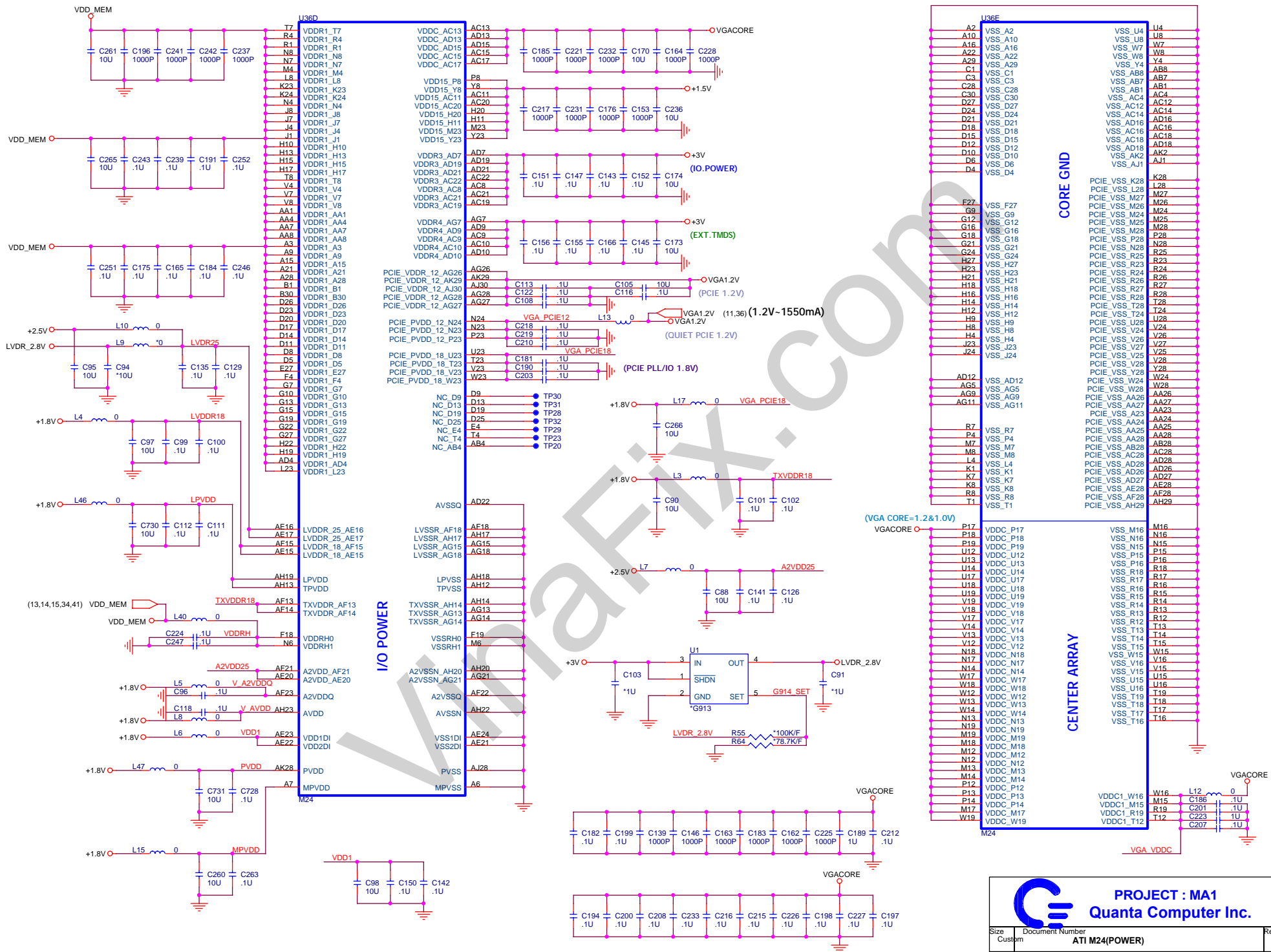
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR\_VTERM

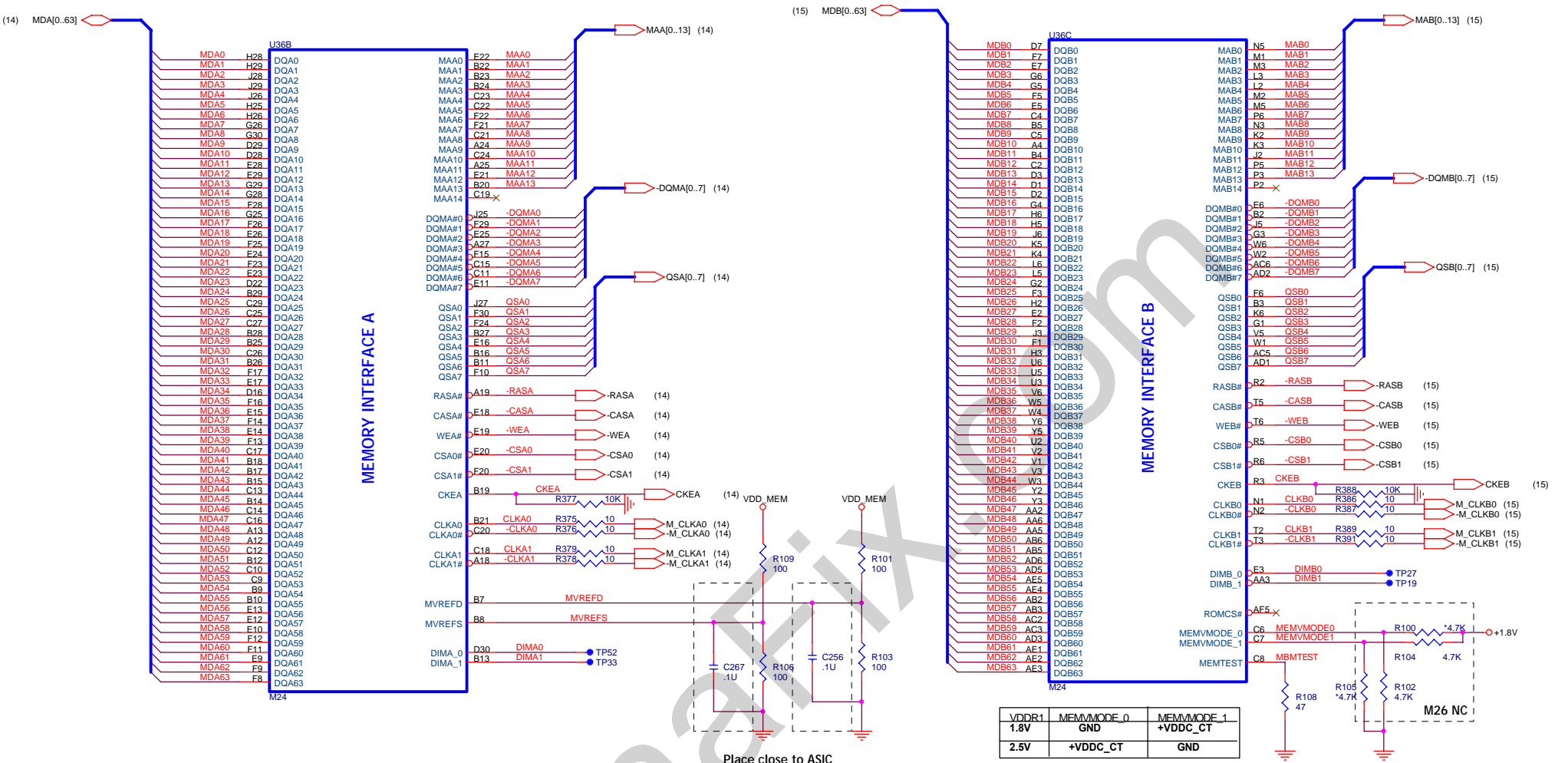
**PROJECT : MA1**  
**Quanta Computer Inc.**

Size Custom Document Number  
**DDR II SODIMM**  
 Date: Thursday, November 25, 2004 Sheet 10 of 41 Rev 1A

(2,3,8,11,12,13,16,18,19,20,22,24,25,26,27,28,29,35,36,37,38,41) +3V  
 (5,8,9,34) 1.8VSUS  
 (34,41) SMDDR\_VTERM  
 (5,34) SMDDR\_VREF







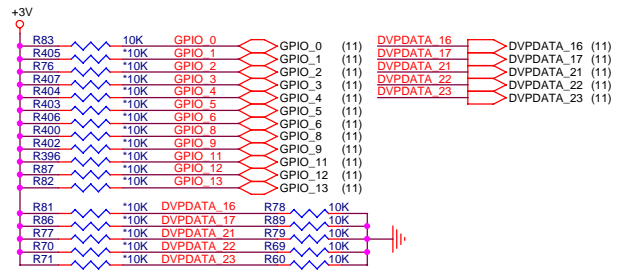
VDDR1	MEMMODE_0	MEMMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND

**STRAPS PIN**

GPIO_0	PCI-Express Current Calibration Bandgap Backup 0: use reference voltage from Bandgap 1: use reference voltage from resistor divider
GPIO_1	PCI-Express PLL Calibration force enable 0: Disable PLL force calibration 1: Enable PLL force calibration
GPIO_(3,2)	00: PCI Express 1.0 mode 01: RESERVED 10: PCI Express 1.0 mode 11: RESERVED
GPIO_4	Turn off PCI-Express impedance / strength calibration 0: enable 1: disable
GPIO_5	Bypass PCI-Express PLL
GPIO_6	PCI-Express transmitter current compensation 0: Normal 1: Inject extra current for output buffer switching

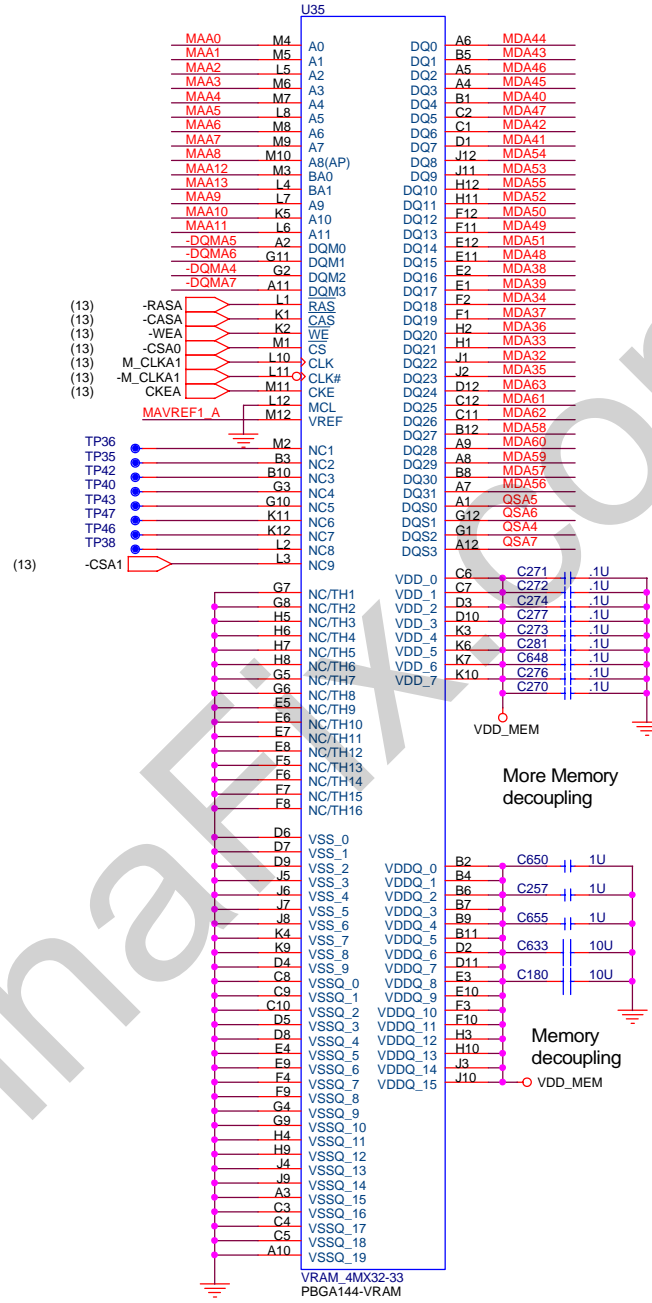
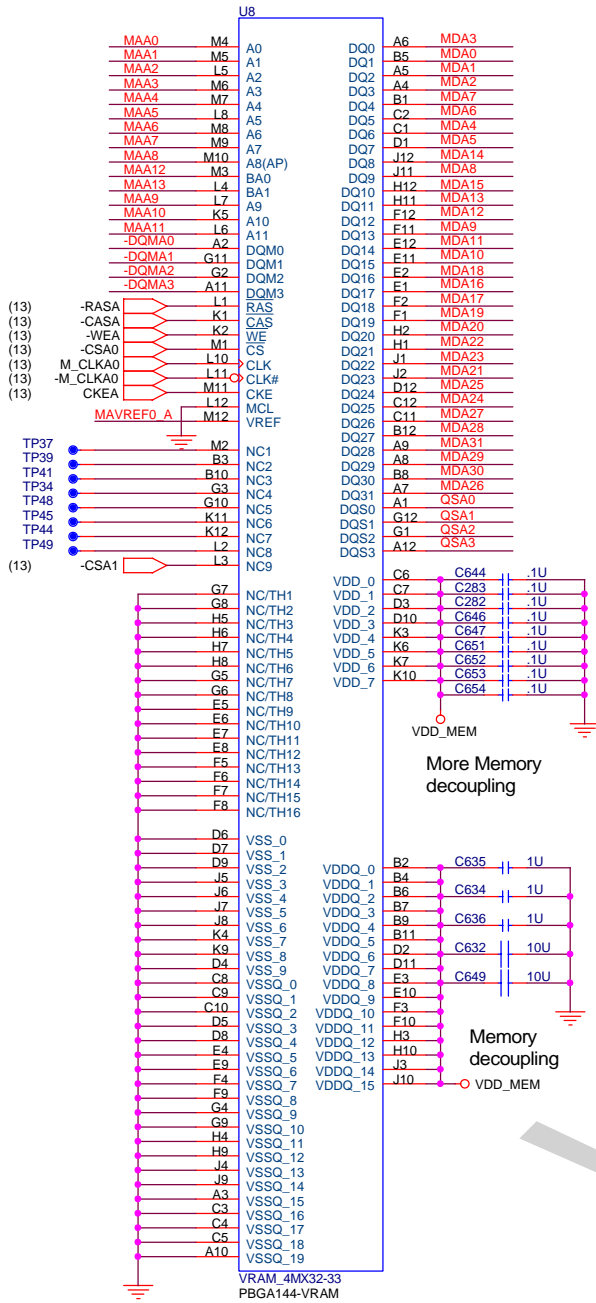
**STRAPS PIN**

GPIO_8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible
GPIO(9,13:11) INT P/D	ROMIDCFG 0x0x: No ROM, CHG_ID=0 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID's from ROM 1000: Parallel ROM, Chip ID's from ROM
DVPDATA_21-23	DVPDATA_23 DVPDATA_22 DVPDATA_21 DVPDATA_21
MEM TYPE	0 0 0 Samsung 8M x 32 (1.8V) - M24 0 0 1 Samsung 4M x 32 (1.8V) - M24 0 1 0 Hynix 8M x 32 (1.8V) - M24 0 1 1 Samsung 4M x 32 (1.8V) - M22 1 0 0 Hynix 4M x 32 (1.8V) - M24 1 1 0 1 1 1



**PROJECT : MA1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	ATI M24 MEM/STRAPS PIN	1A
Date:	Thursday, November 25, 2004	Sheet 13 of 41

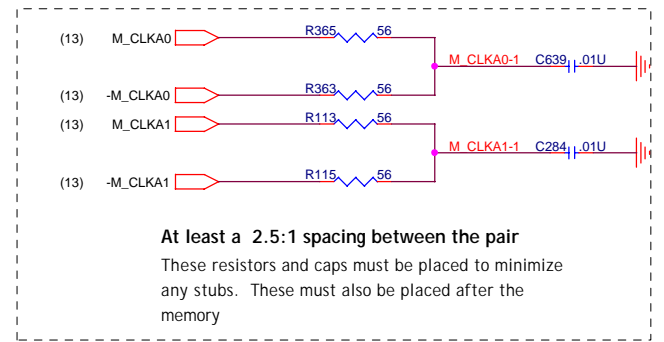
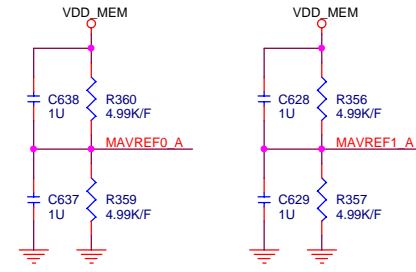


### VGA DDR MEMORY A

@64/128MBytes DDR 128Mbit 1MX32X4 uBGA

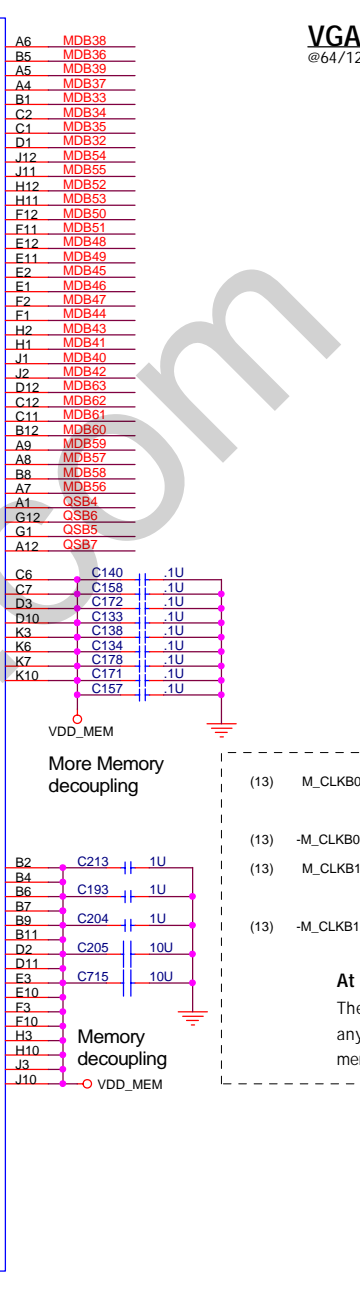
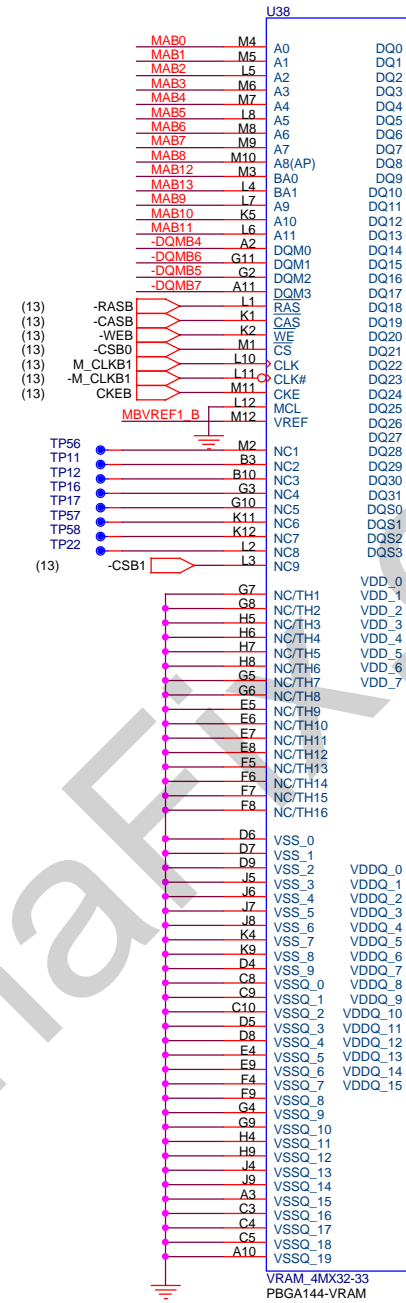
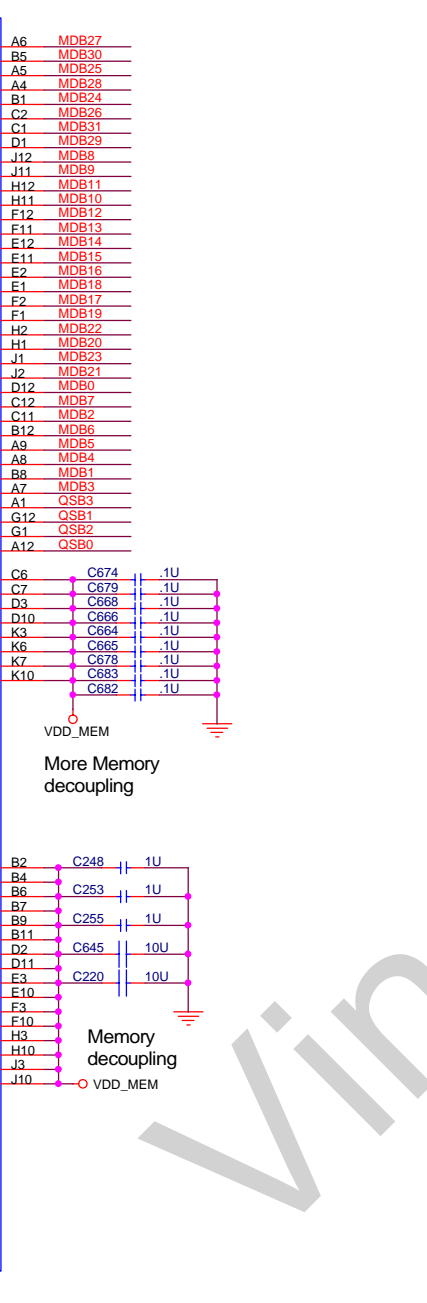
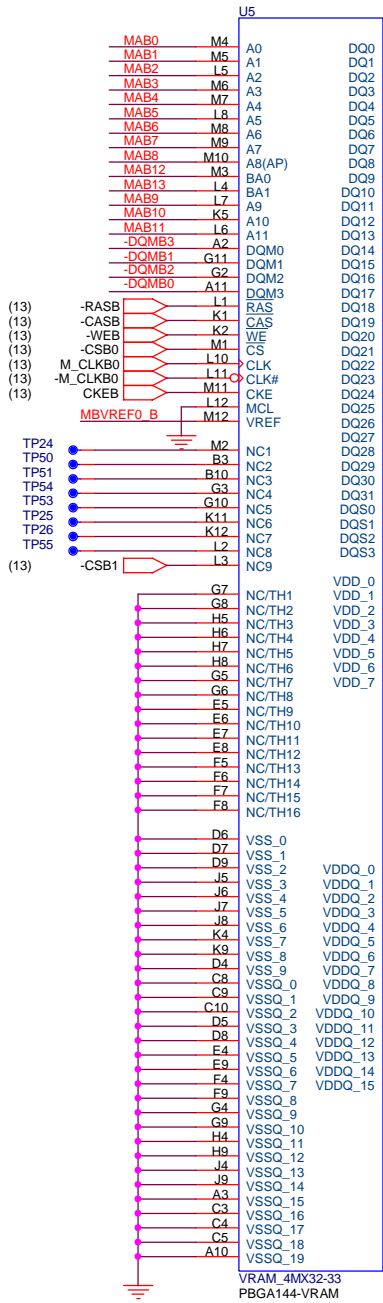


Place close to memory



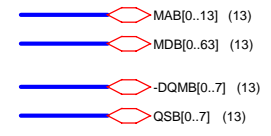
**PROJECT : MA1**  
**Quanta Computer Inc.**

Size B	Document Number <b>VGA DDR VRAM-A CANNEL</b>	Rev 1A
Date: Thursday, November 25, 2004	Sheet 14 of 41	

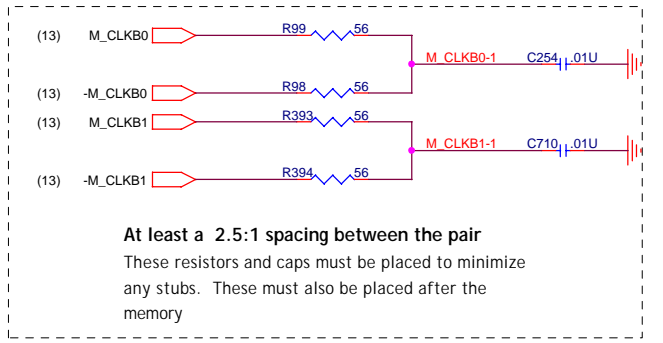
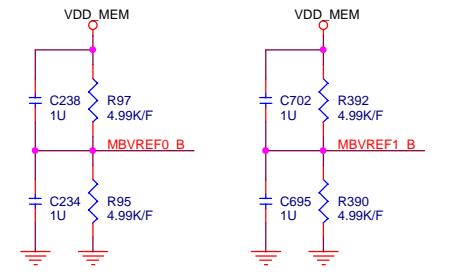


### VGA DDR MEMORY B

@64/128MBytes DDR 128Mbit 1MX32X4 uBGA



Place close to memory

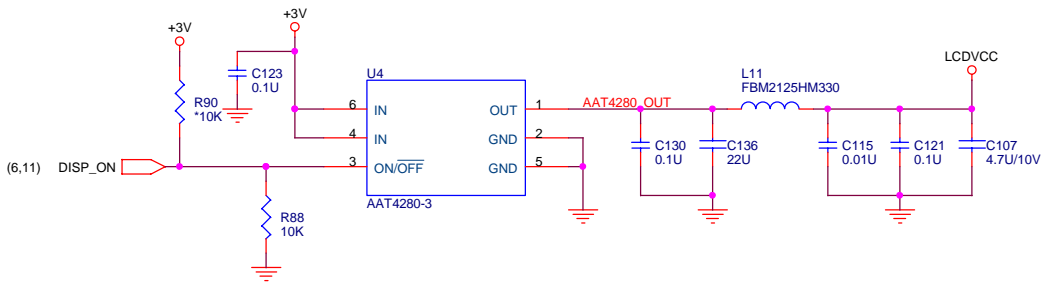


At least a 2.5:1 spacing between the pair  
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

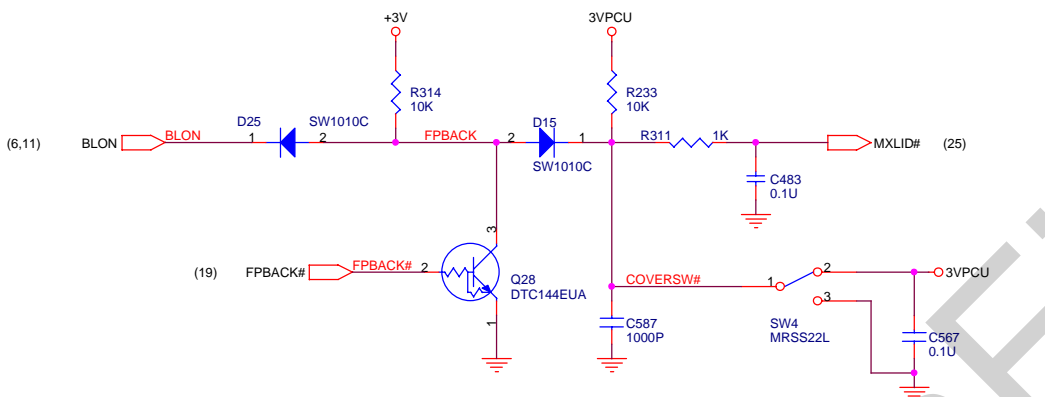
**PROJECT : MA1**  
**Quanta Computer Inc.**

Size B	Document Number <b>VGA DDR VRAM-B CANNEL</b>	Rev 1A
Date: Thursday, November 25, 2004		Sheet 15 of 41

### PANEL VCC CONTROL

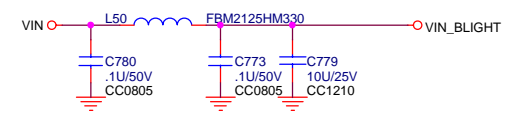
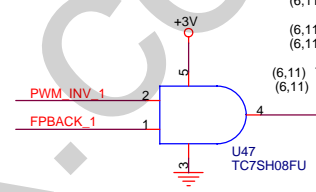
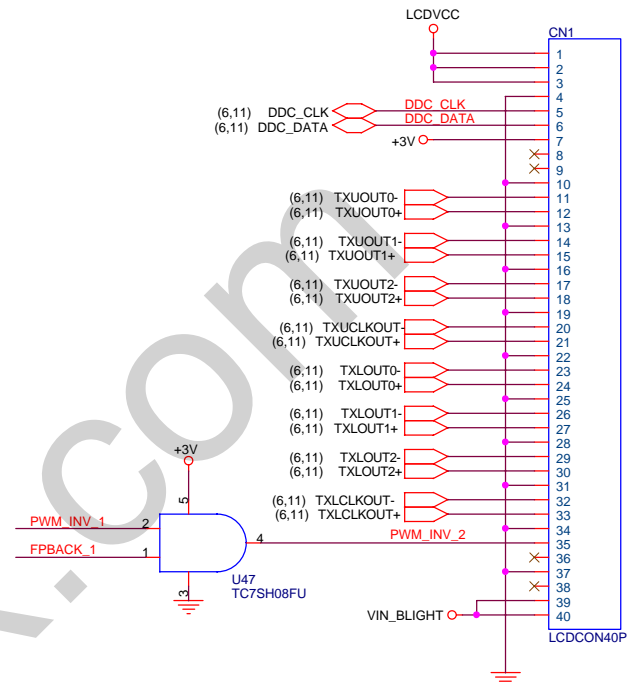



### BACKLIGHT CONTROL



Del Q5, Q9, R27, R51, Q159

### LCD CONNECTOR



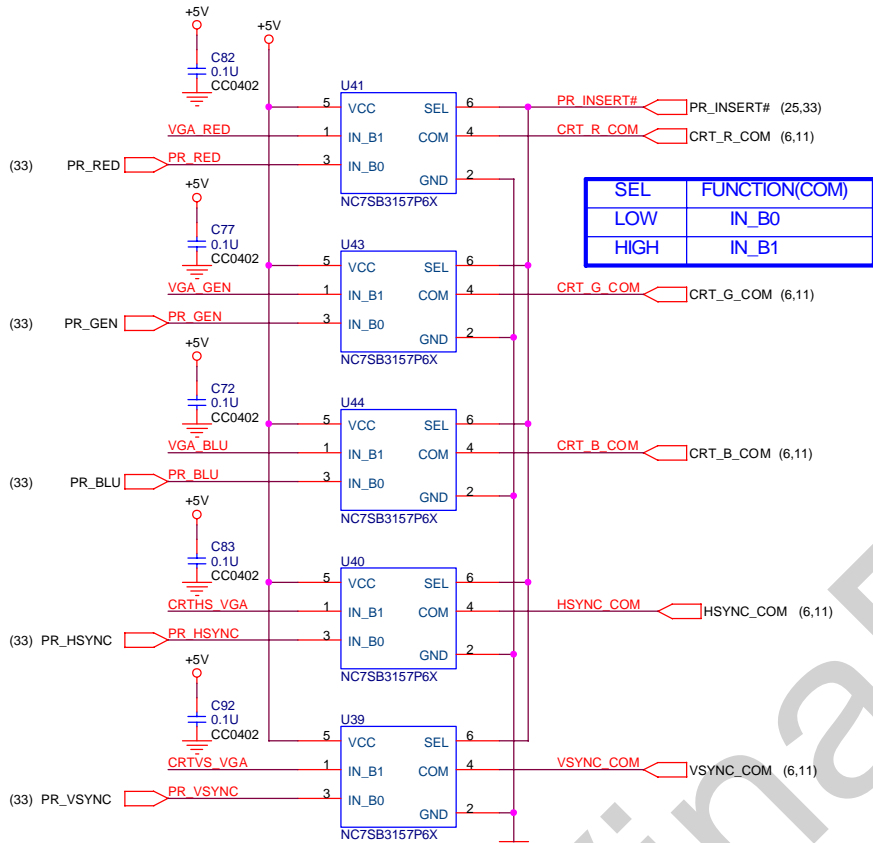


**PROJECT : MA1**  
**Quanta Computer Inc.**

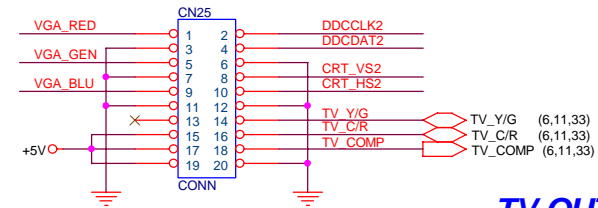
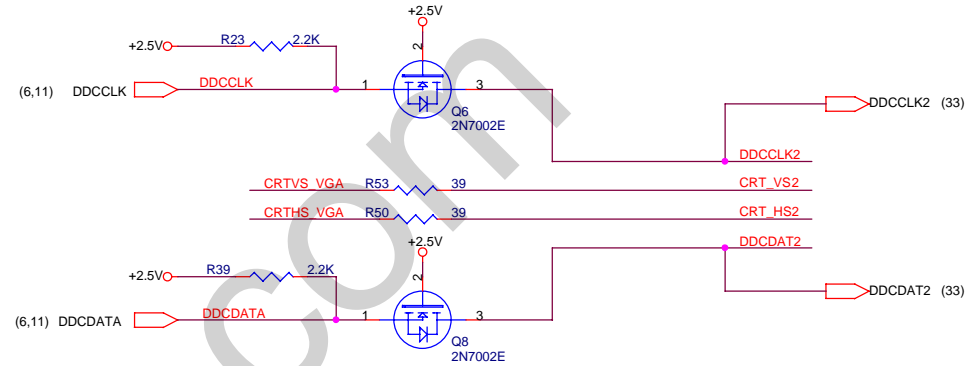
Size B	Document Number <b>LCD LVDS CON</b>	Rev 1A
Date: Thursday, November 25, 2004		
Sheet 16 of 41		



## CRT SWITCH



## CRT PORT

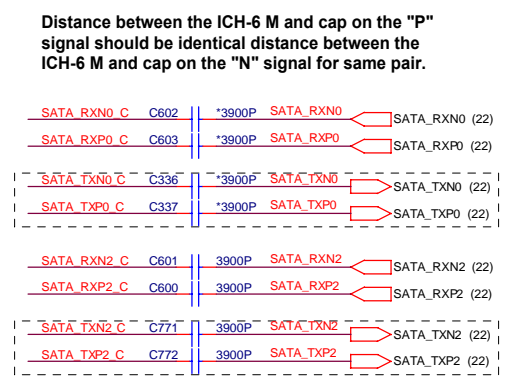
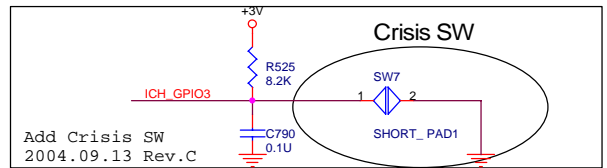
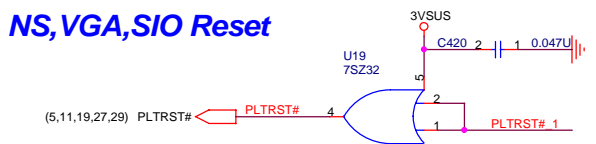
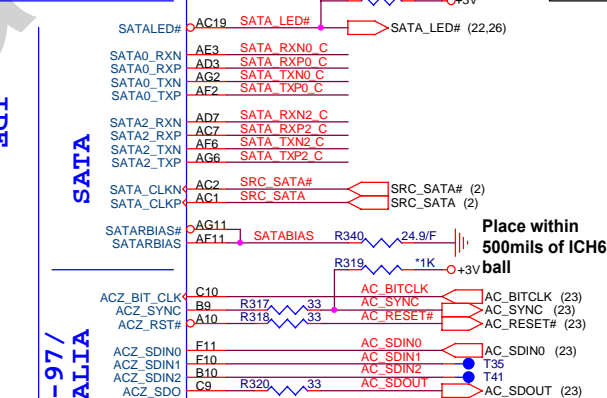
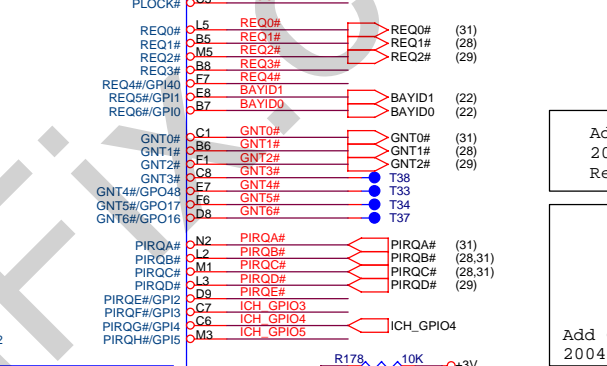
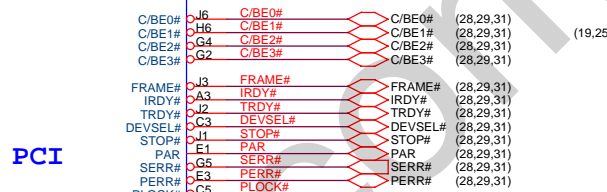
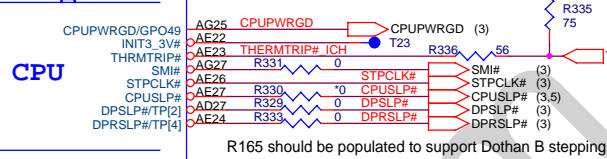
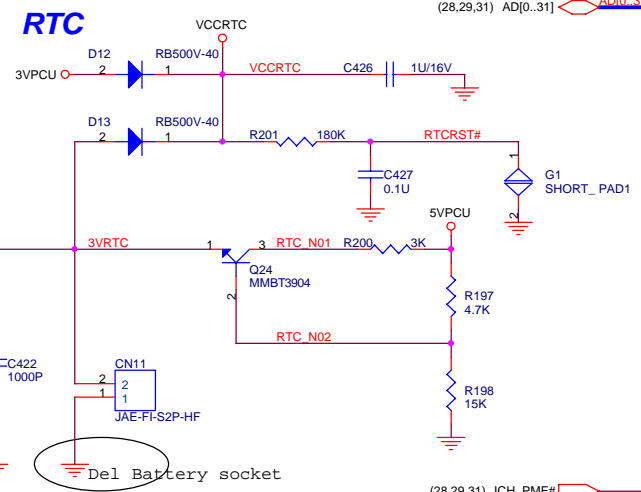
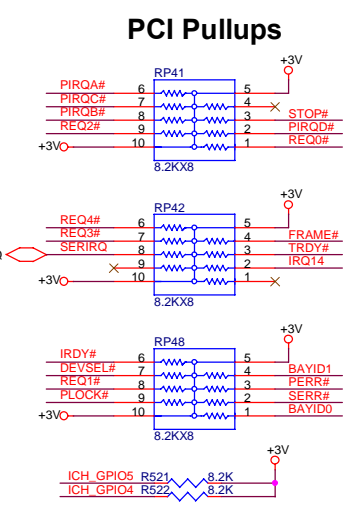
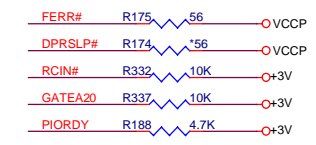
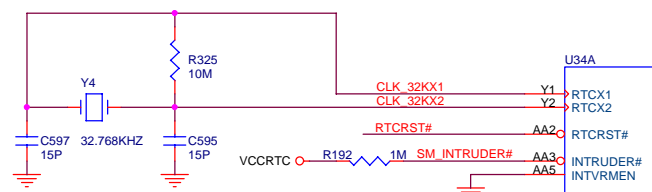


## TV-OUT



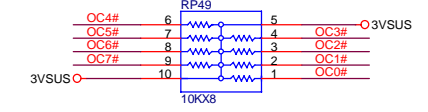
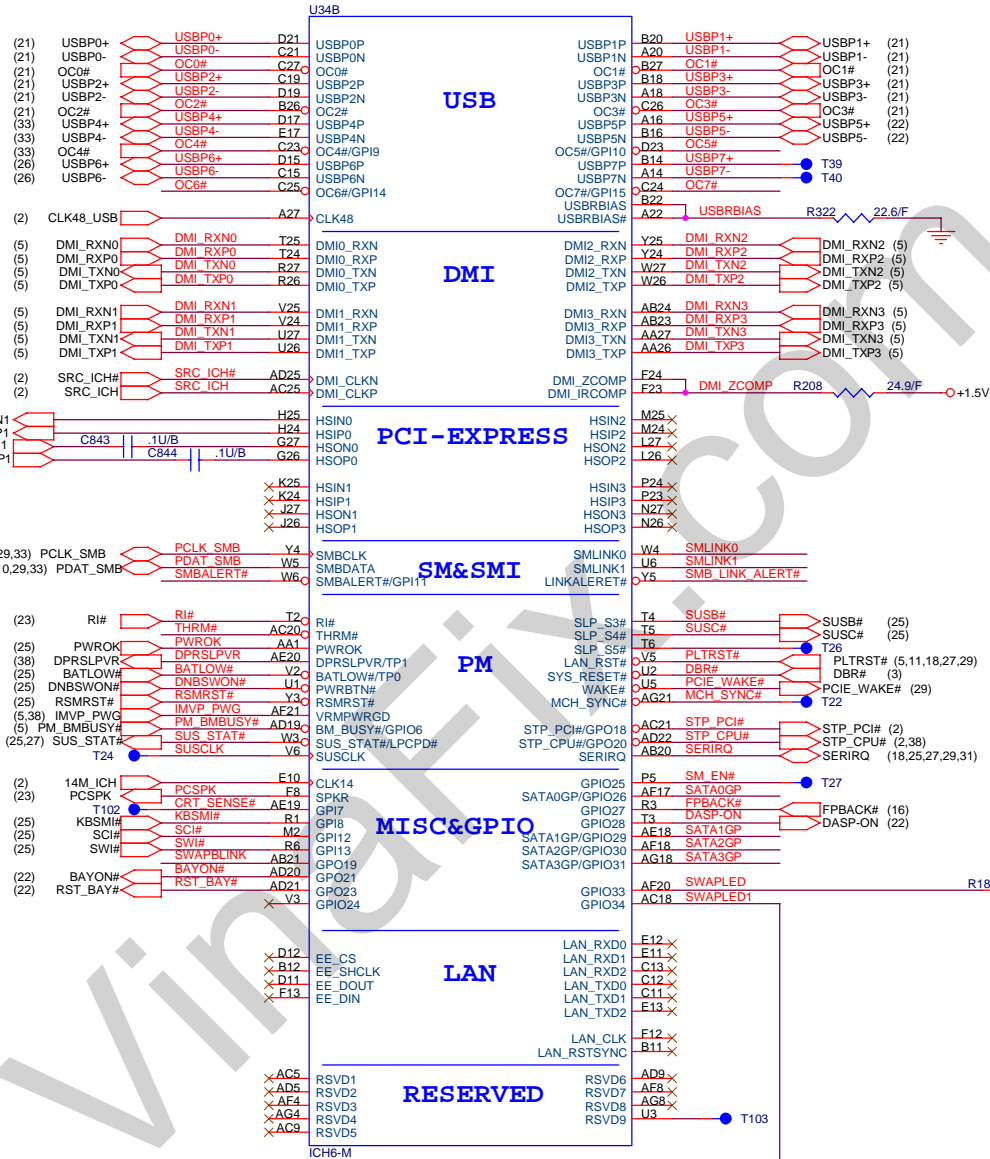
**PROJECT : MA1**  
**Quanta Computer Inc.**

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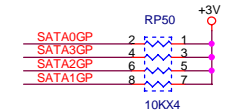
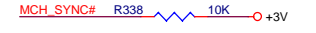
**PROJECT : MA1**  
**Quanta Computer Inc.**

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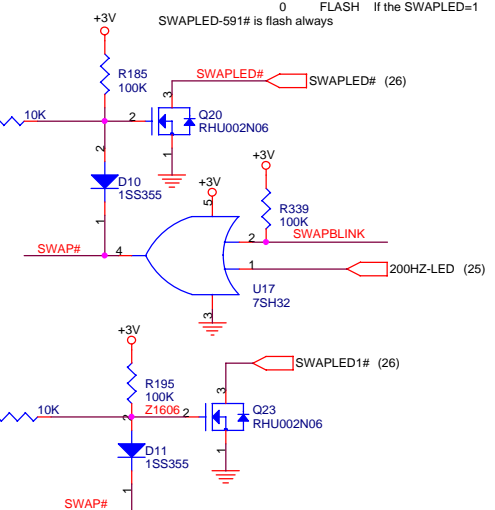
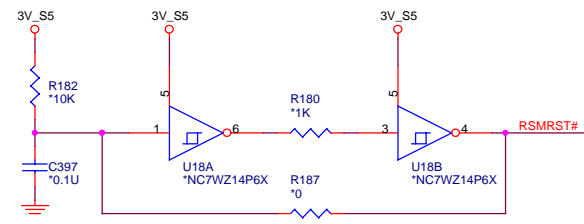
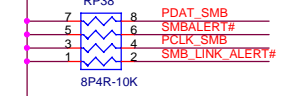
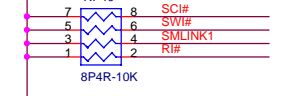
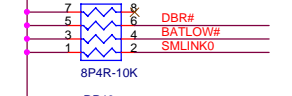
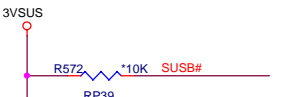
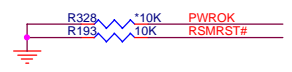
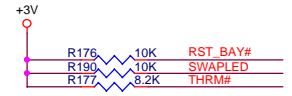
Place within 500mils of ICH-6

Place within 500mils of ICH-6



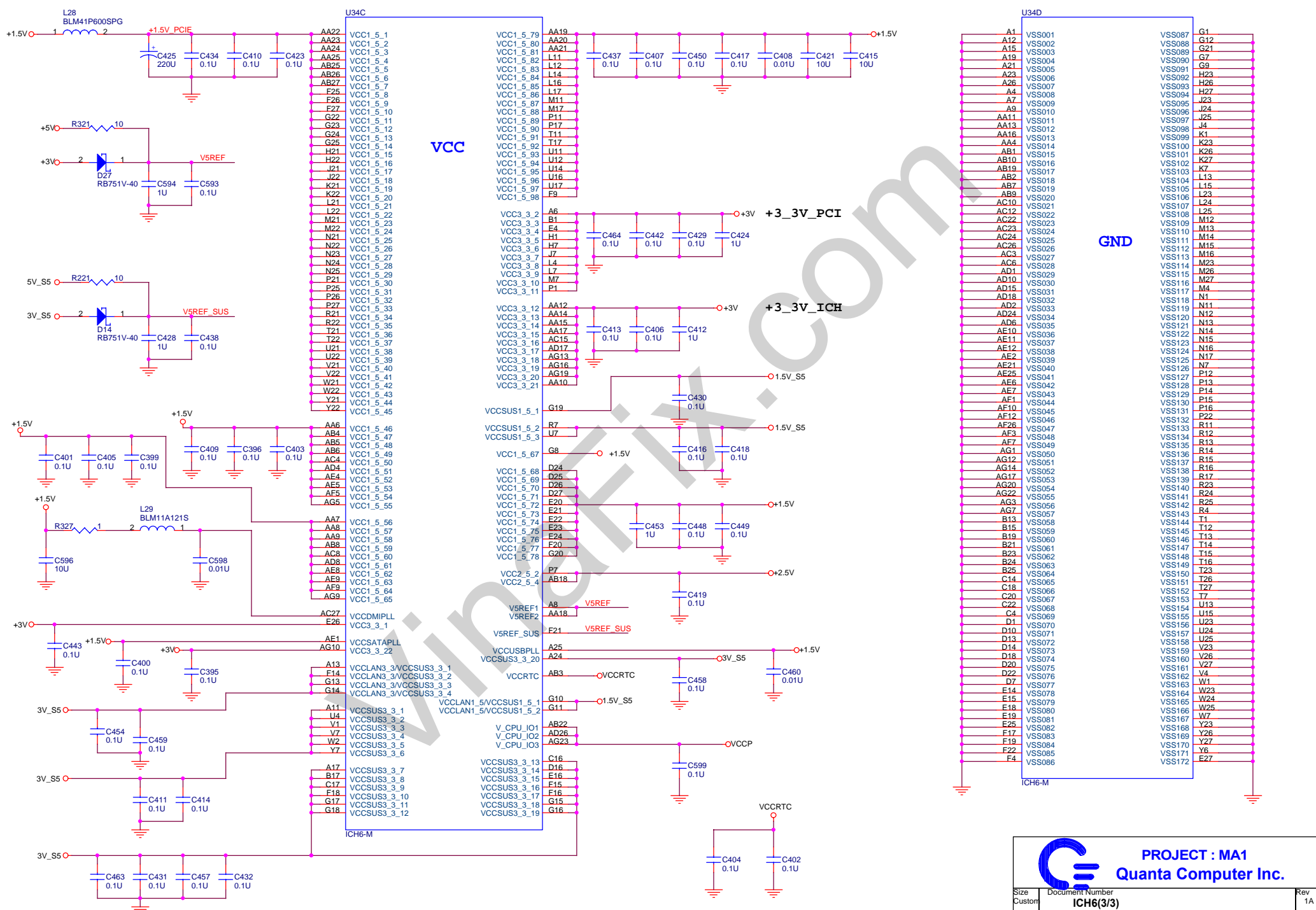
SWAPLED#	1	0	1
SWAPLED=0 (GLED light on)	1	0	1
SWAPBLANK	1	1	1
SWAPLED=591# is flash always	0	1	1
FLASH	1	1	1

If the SWAPLED=1



**PROJECT : MA1**  
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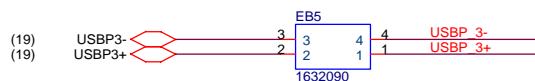
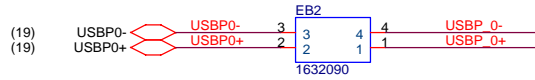
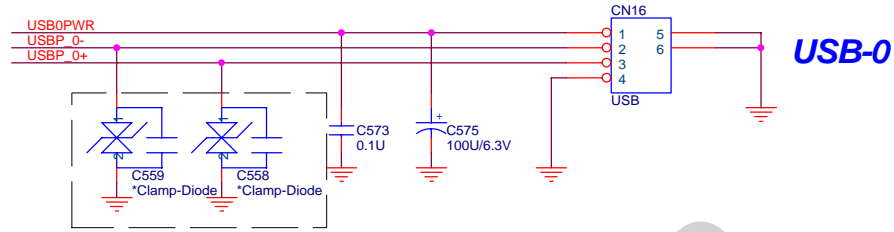
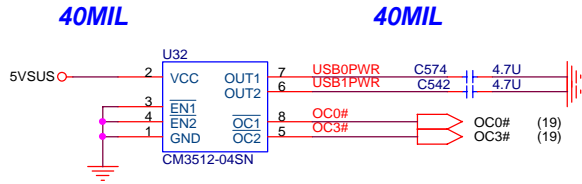
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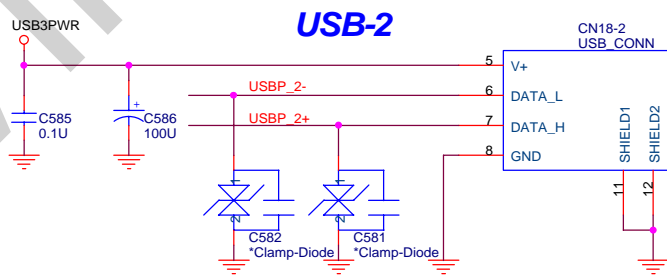
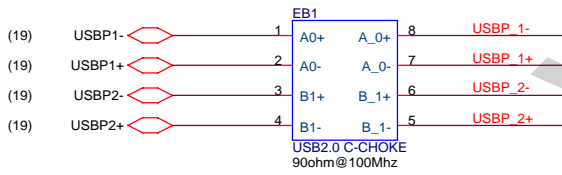
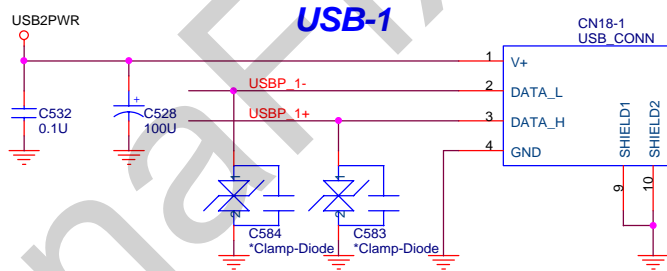
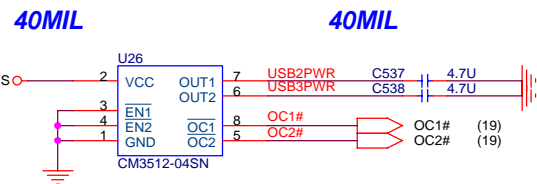
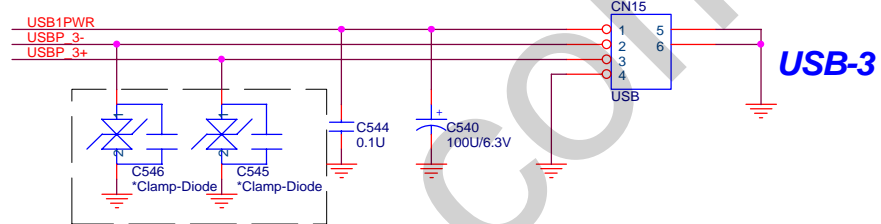
**PROJECT : MA1**  
Quanta Computer Inc.

Size	Document Number	Rev
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### LEFT SIDE



### LEFT SIDE

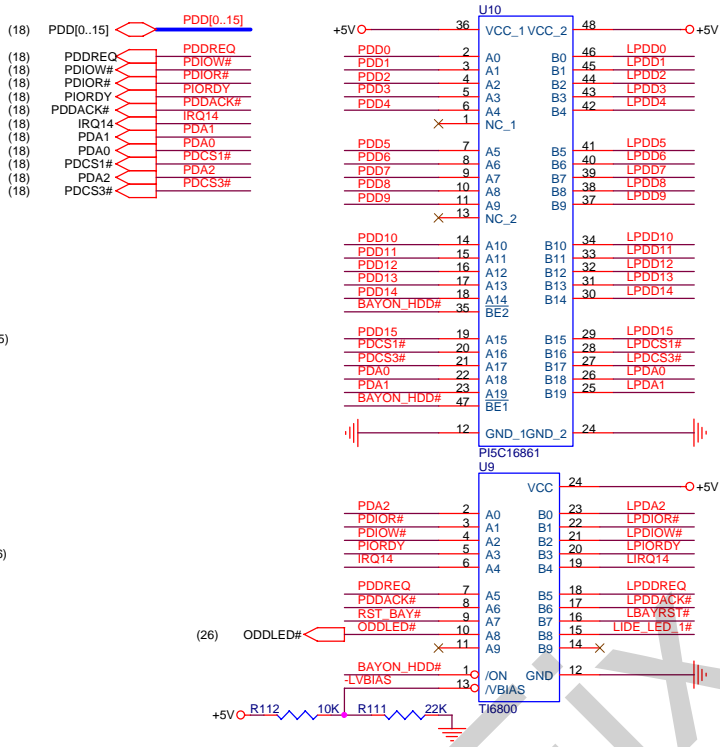
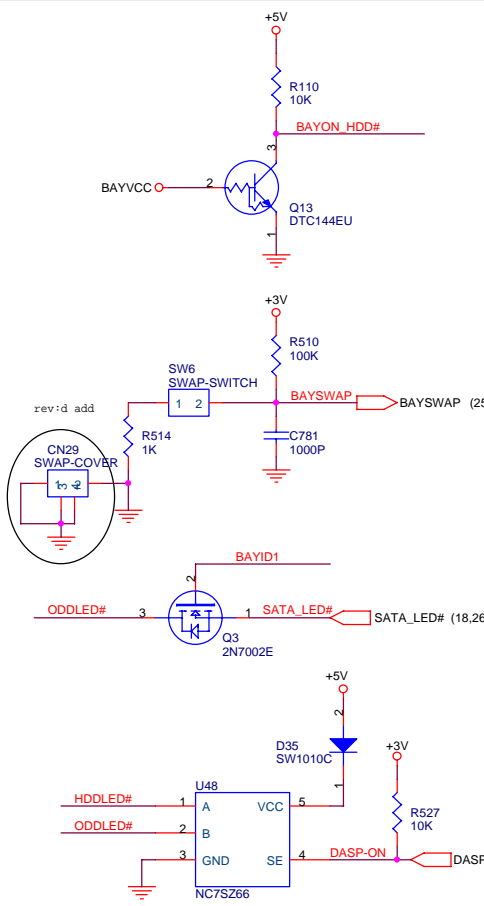


(26,28,31,33,35,37,38,41) 5VSUS

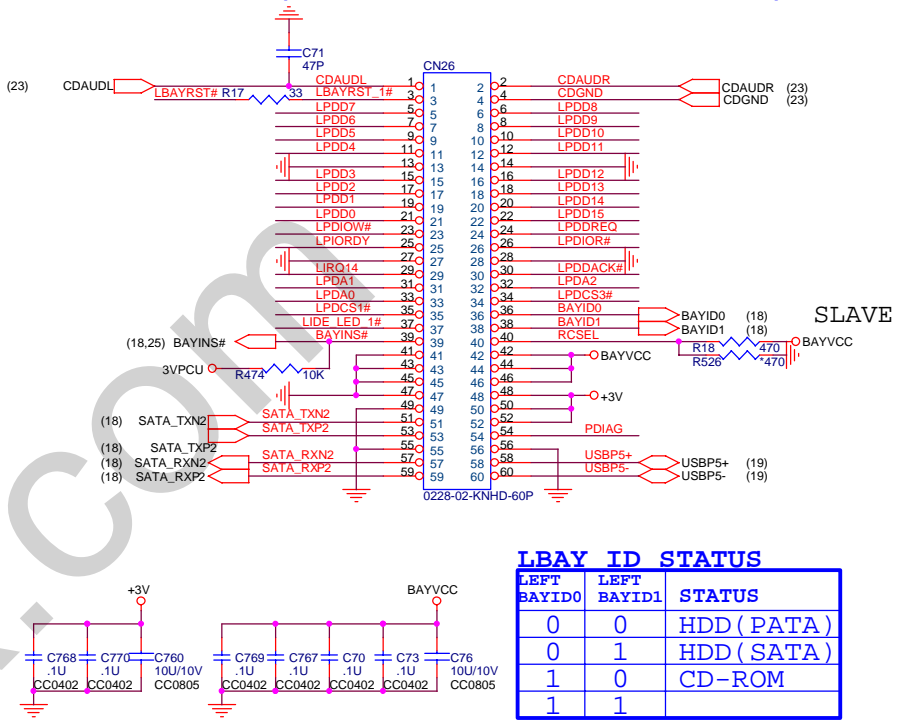


**PROJECT : MA1**  
**Quanta Computer Inc.**

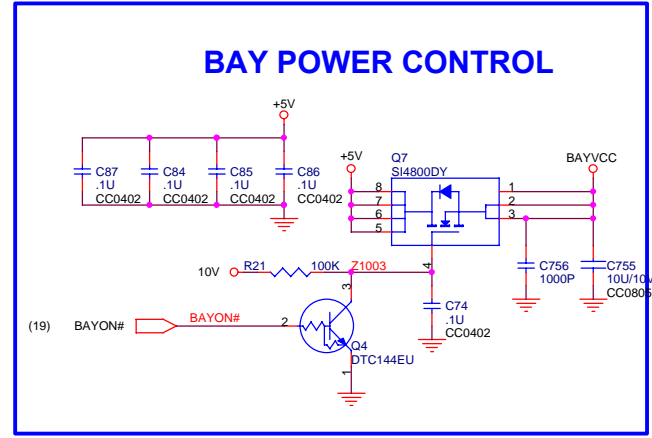
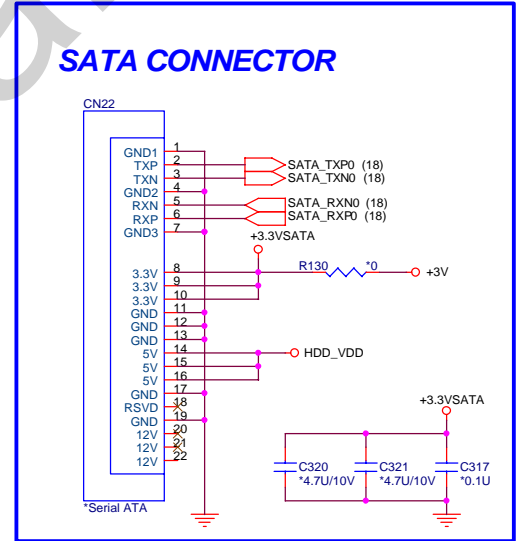
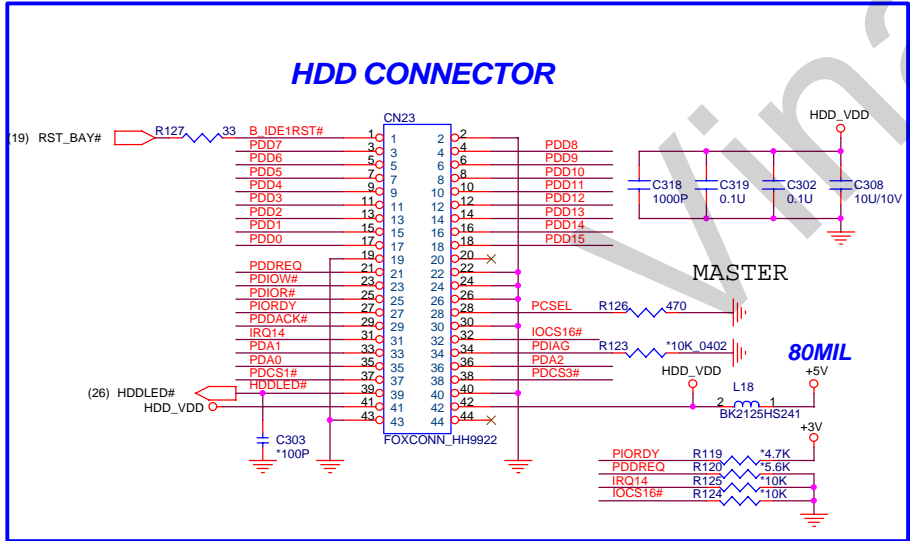
Size	Document Number	Rev
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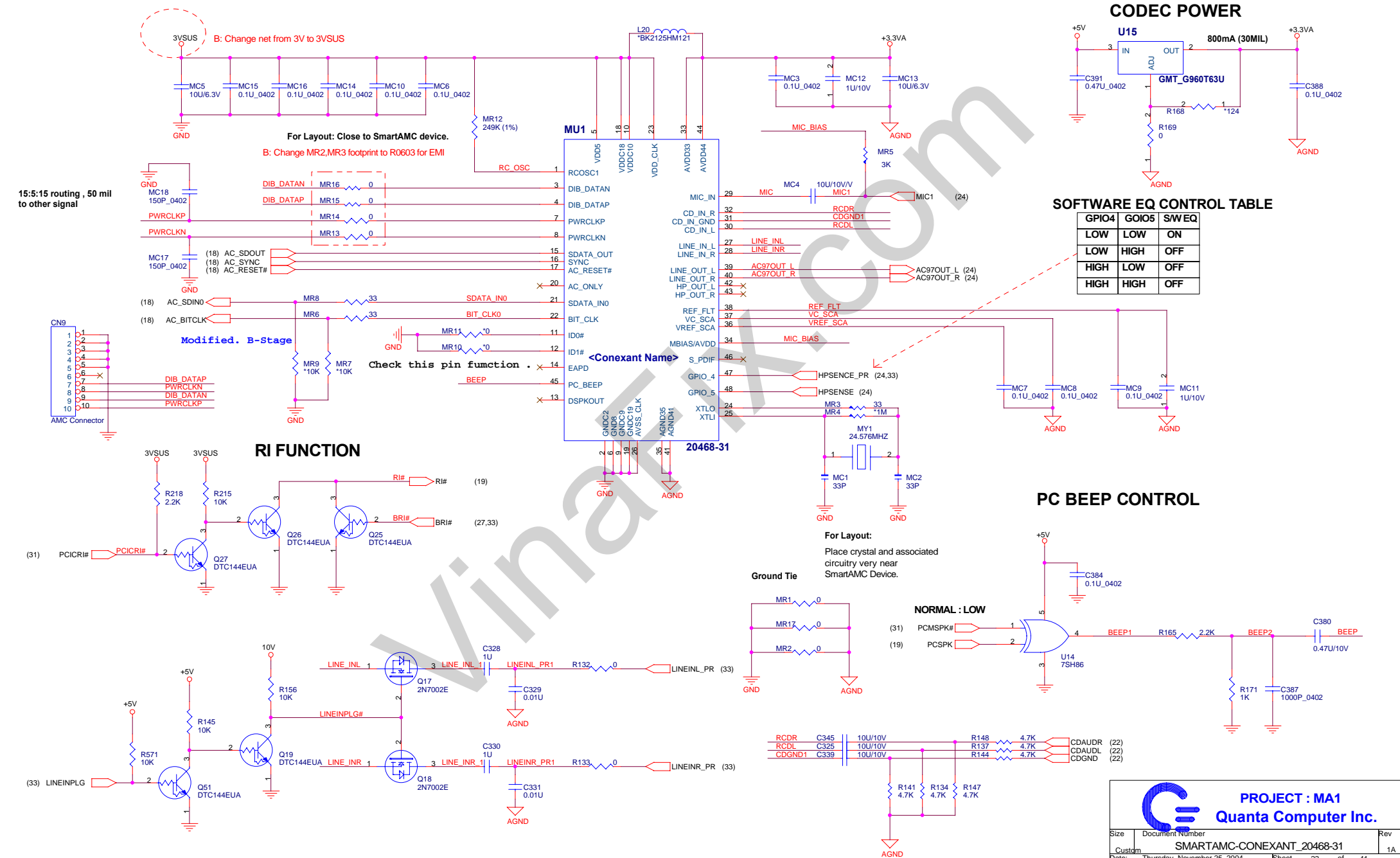
# LEFT BAY(CD-ROM, HDD-PATA/SATA, FDD,)



LBAY ID STATUS		
LEFT BAYID0	LEFT BAYID1	STATUS
0	0	HDD ( PATA )
0	1	HDD ( SATA )
1	0	CD-ROM
1	1	



**For Layout:**  
Place decoupling caps near the power pins of SmartAMC device.



15:5:15 routing, 50 mil to other signal

**B: Change net from 3V to 3VSUS**

**For Layout: Close to SmartAMC device.**  
**B: Change MR2,MR3 footprint to R0603 for EMI**

**Modified. B-Stage**

**Check this pin function.**

### RI FUNCTION

### CODEC POWER

### SOFTWARE EQ CONTROL TABLE

GPIO4	GOI05	S/W EQ
LOW	LOW	ON
LOW	HIGH	OFF
HIGH	LOW	OFF
HIGH	HIGH	OFF

### PC BEEP CONTROL

**For Layout:**  
Place crystal and associated circuitry very near SmartAMC Device.

### Ground Tie

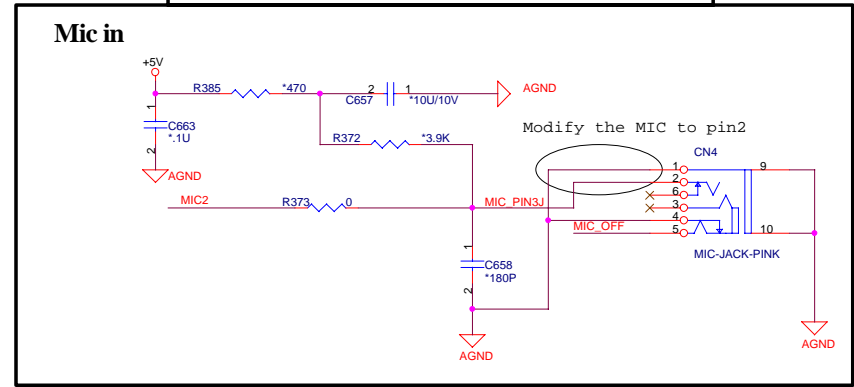
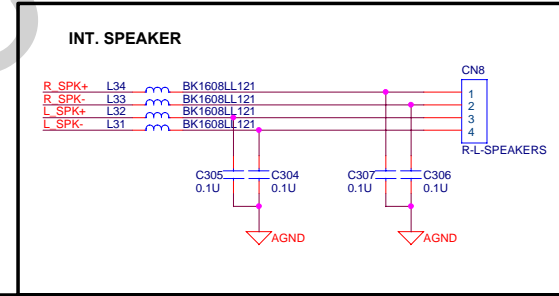
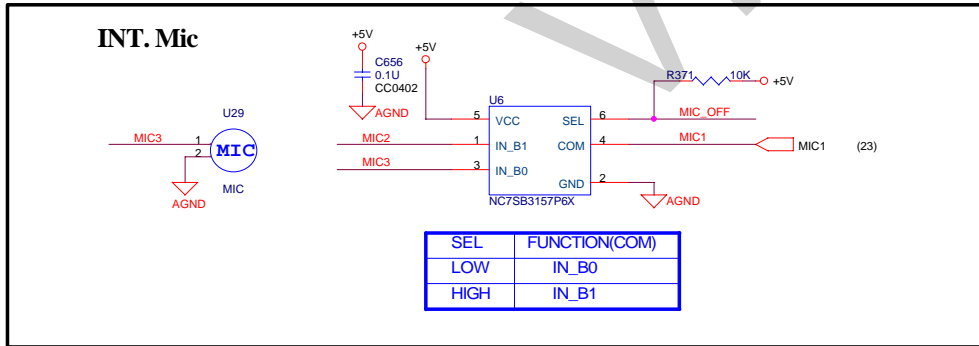
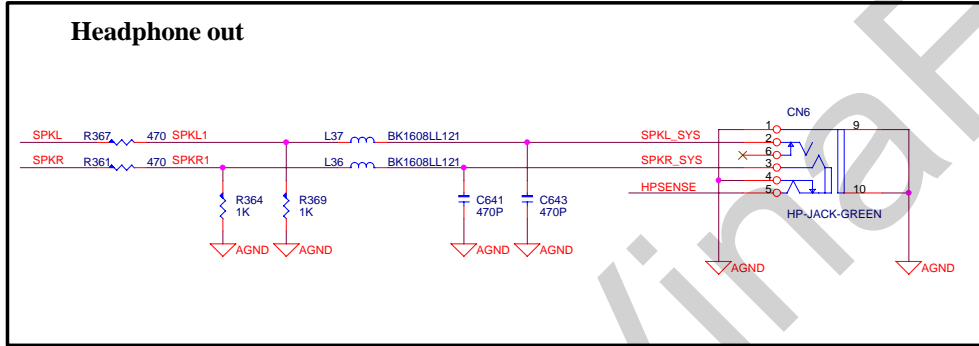
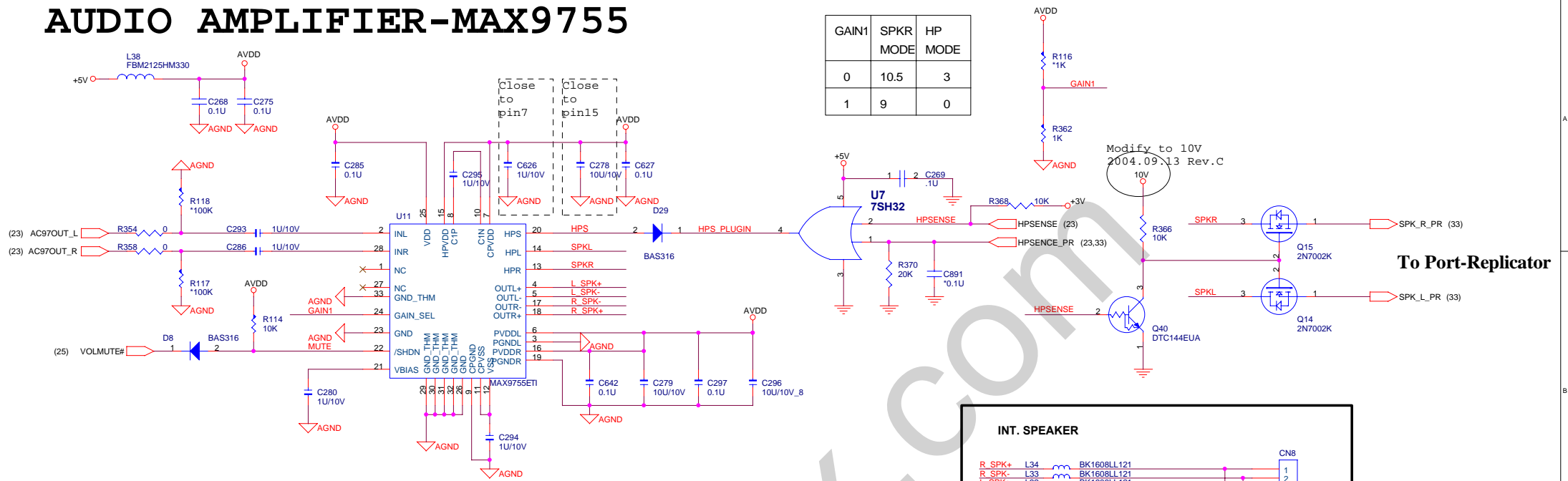
### NORMAL : LOW

**PROJECT : MA1**  
**Quanta Computer Inc.**

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Custom	SMARTAMC-CONEXANT_20468-31	1A
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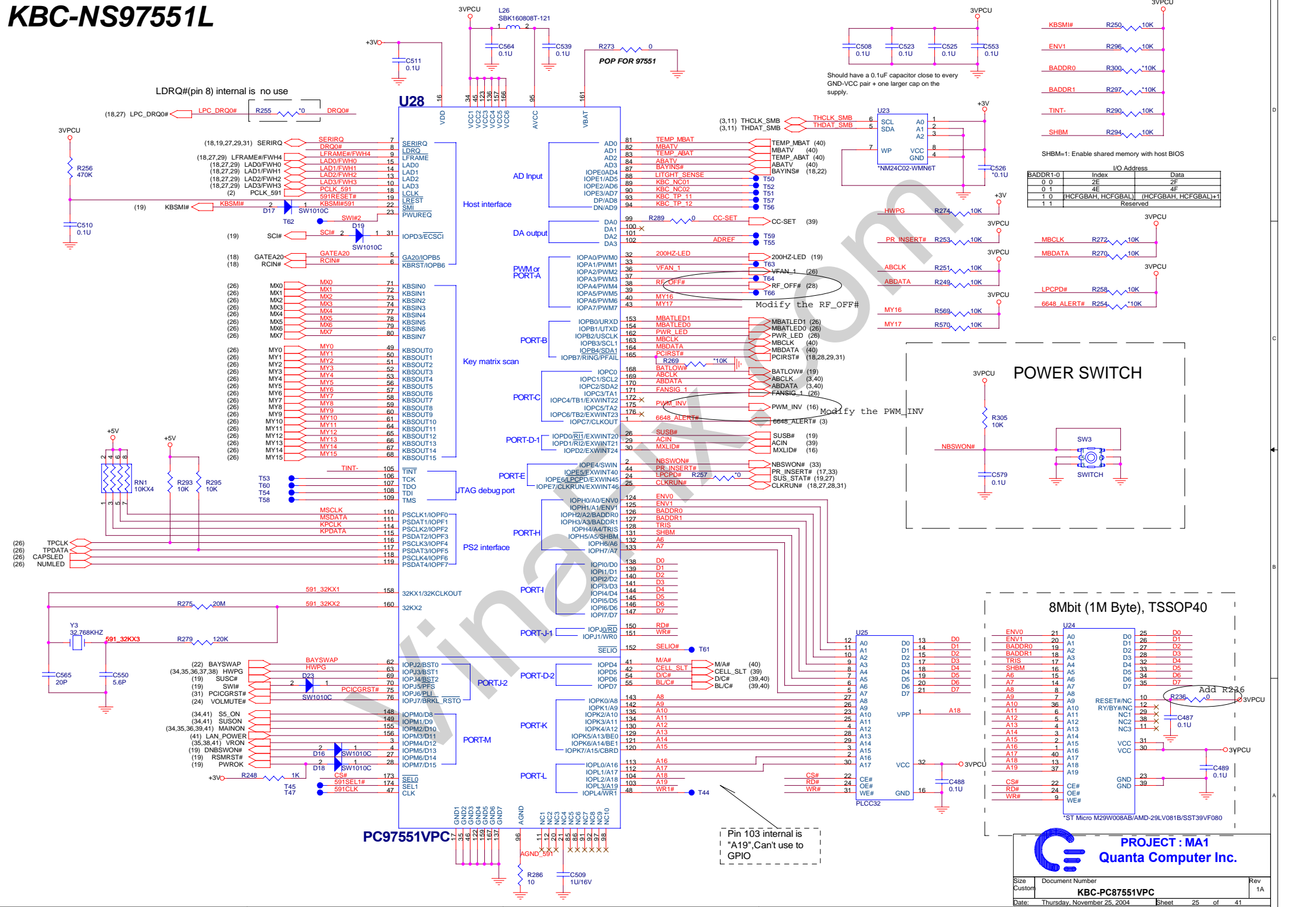
# AUDIO AMPLIFIER-MAX9755

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0





# KBC-NS97551L



LDRQ#(pin 8) internal is no use

(18,27) LPC\_DRQ0# ← LPC\_DRQ0# [R255] 10 DRQ0#

(18,19,27,29,31) SERIRQ → SERIRQ 7  
 (18,27,29) LFRAME#/FWH4 → LFRAME#/FWH4 9  
 (18,27,29) LAD0/FWH0 → LAD0/FWH0 15  
 (18,27,29) LAD1/FWH1 → LAD1/FWH1 14  
 (18,27,29) LAD2/FWH2 → LAD2/FWH2 13  
 (18,27,29) LAD3/FWH3 → LAD3/FWH3 10  
 (18,27,29) PCLK\_591 → PCLK\_591 18  
 (2) S91RESET# → S91RESET# 19  
 (19) KBSMI# → KBSMI# 2

(19) KBSMI# → KBSMI# 2  
 D17 → SW1010C  
 T62 → SW1010C  
 D19 → SW1010C  
 (19) SCI# → SCI# 2  
 (18) GATEA20 → GATEA20 5  
 (18) RCIN# → RCIN# 6

(26) MX0 → MX0 71  
 (26) MX1 → MX1 72  
 (26) MX2 → MX2 73  
 (26) MX3 → MX3 74  
 (26) MX4 → MX4 77  
 (26) MX5 → MX5 79  
 (26) MX6 → MX6 79  
 (26) MX7 → MX7 80

(26) MY0 → MY0 49  
 (26) MY1 → MY1 50  
 (26) MY2 → MY2 51  
 (26) MY3 → MY3 52  
 (26) MY4 → MY4 53  
 (26) MY5 → MY5 56  
 (26) MY6 → MY6 57  
 (26) MY7 → MY7 58  
 (26) MY8 → MY8 59  
 (26) MY9 → MY9 60  
 (26) MY10 → MY10 61  
 (26) MY11 → MY11 64  
 (26) MY12 → MY12 65  
 (26) MY13 → MY13 66  
 (26) MY14 → MY14 67  
 (26) MY15 → MY15 68

TINT- → TINT- 105  
 TCK → TCK 107  
 TDO → TDO 108  
 TDI → TDI 109  
 TMS → TMS 109

(26) TPCLK → TPCLK 110  
 (26) TPDATA → TPDATA 111  
 (26) CAPSLED → CAPSLED 114  
 (26) NUMLED → NUMLED 115  
 (26) PSCLK1/IOPF0 → PSCLK1/IOPF0 116  
 (26) PSCLK2/IOPF2 → PSCLK2/IOPF2 117  
 (26) PSCLK3/IOPF4 → PSCLK3/IOPF4 118  
 (26) PSCLK4/IOPF6 → PSCLK4/IOPF6 119

591\_32KX1 → 591\_32KX1 158  
 591\_32KX2 → 591\_32KX2 160  
 591\_32KX3 → 591\_32KX3 160

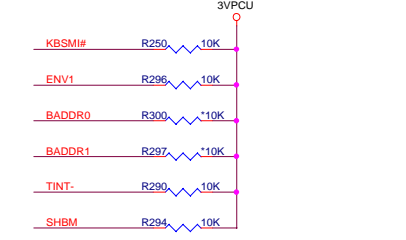
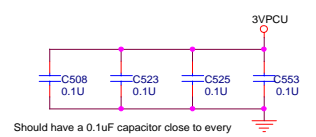
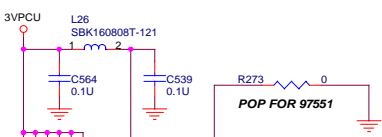
(22) BAYSWAP → BAYSWAP 62  
 (34,35,36,37,38) HWPG → HWPG 63  
 (19) SUSC# → SUSC# 69  
 (19) SWI# → SWI# 70  
 (31) PCICGRST# → PCICGRST# 76  
 (24) VOLMUTE# → VOLMUTE# 76

(34,41) S5\_ON → S5\_ON 148  
 (34,41) SUSON → SUSON 149  
 (34,35,36,39,41) MAINON → MAINON 156  
 (41) LAN\_POWER → LAN\_POWER 3  
 (35,38,41) VRON → VRON 4  
 (19) DNBSWON# → DNBSWON# 27  
 (19) RSMRST# → RSMRST# 28  
 (19) PWROK → PWROK 28

(19) DNBSWON# → DNBSWON# 27  
 (19) RSMRST# → RSMRST# 28  
 (19) PWROK → PWROK 28

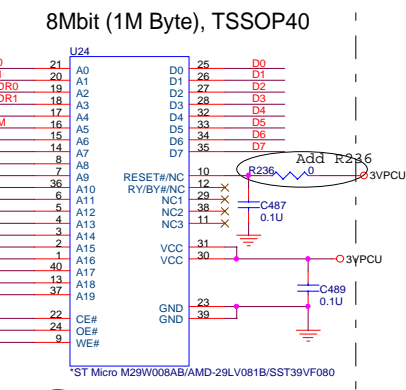
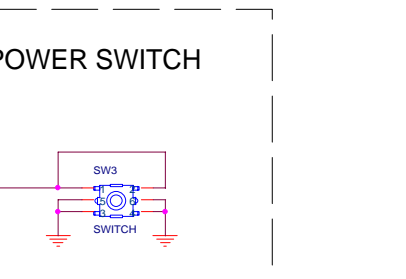
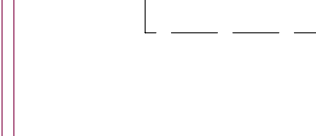
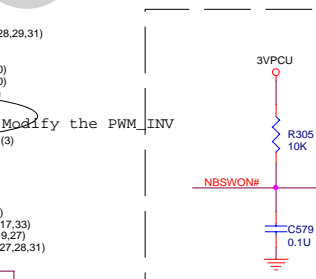
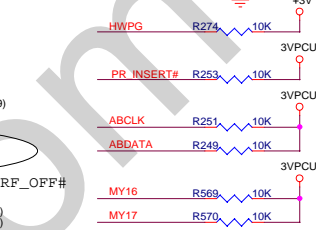
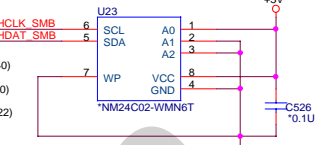
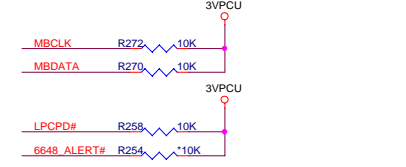
(19) DNBSWON# → DNBSWON# 27  
 (19) RSMRST# → RSMRST# 28  
 (19) PWROK → PWROK 28

(19) DNBSWON# → DNBSWON# 27  
 (19) RSMRST# → RSMRST# 28  
 (19) PWROK → PWROK 28



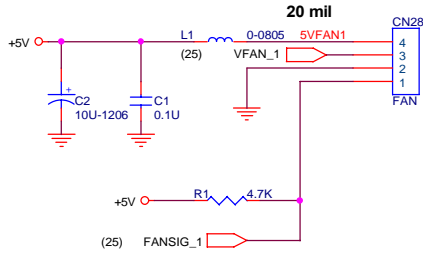
SHBM=1: Enable shared memory with host BIOS

BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	HCFGBAH, HCFGBAL	(HCFGBAH, HCFGBAL)+1
1 1		Reserved

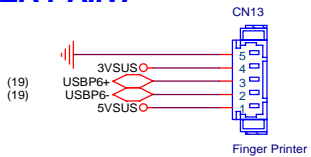


**PROJECT : MA1**  
**Quanta Computer Inc.**

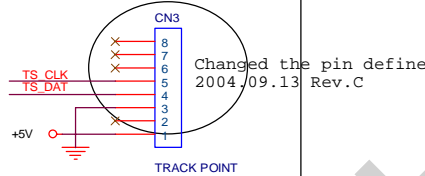
### FAN OUT PWM CONNECTOR



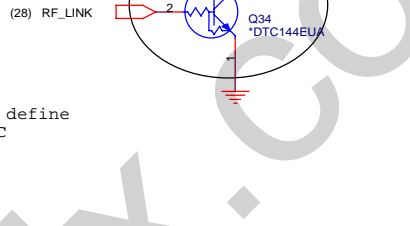
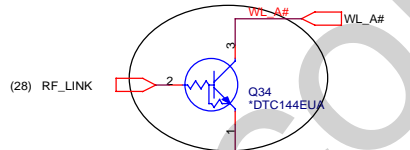
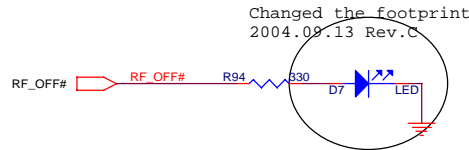
### FINGER PRINT



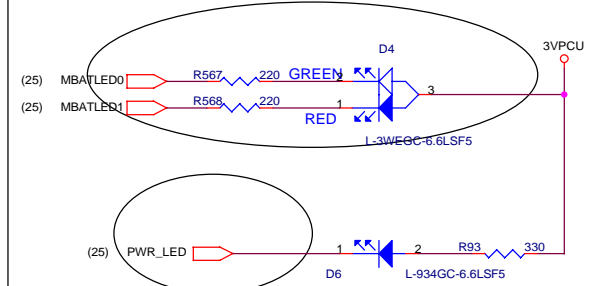
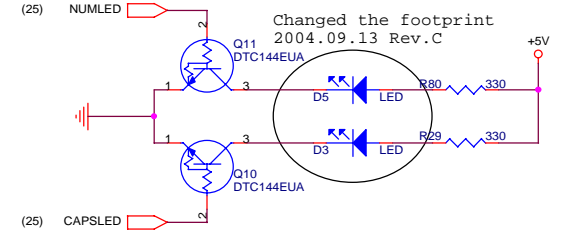
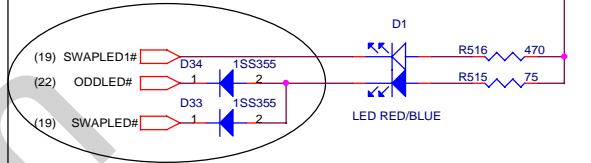
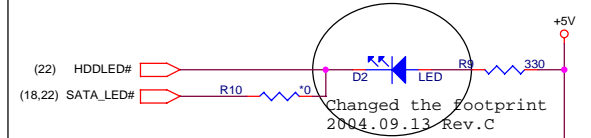
### TRACK POINT



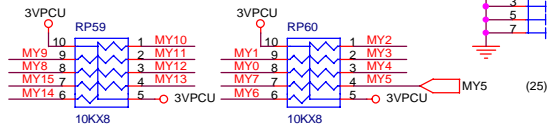
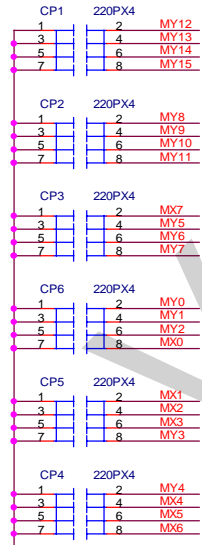
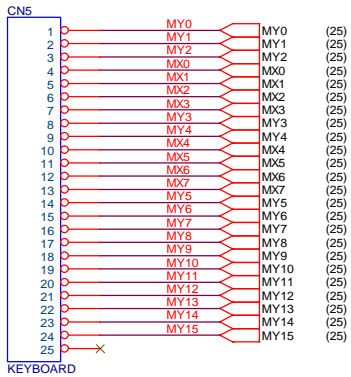
### WIRELESS LED



### LED INDIATOR

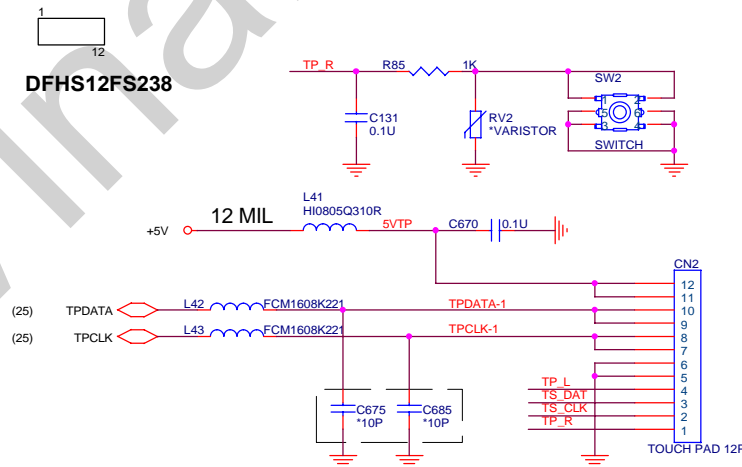


### KEYBOARD



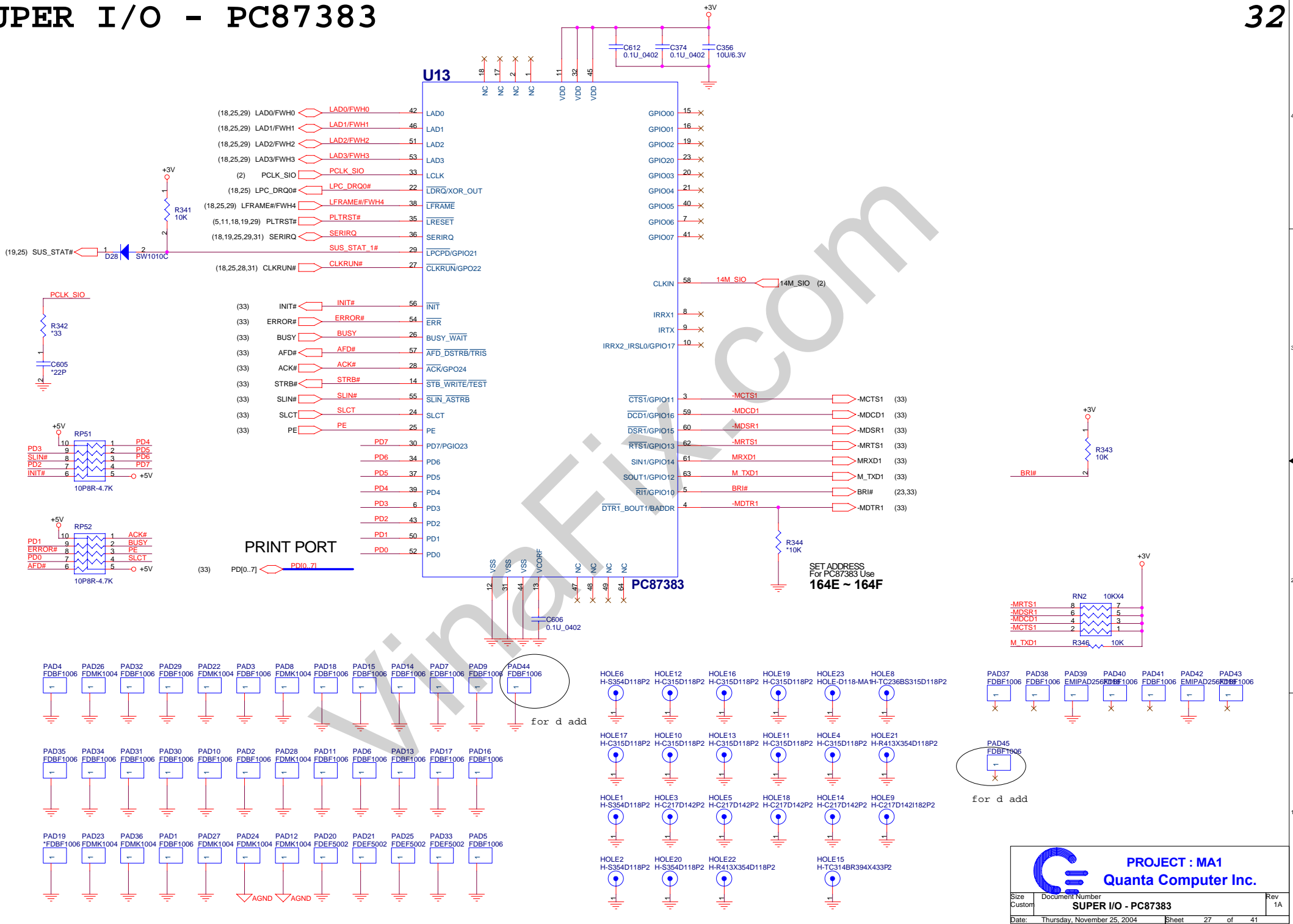
### TOUCHPAD

#### DFHS12FS238



E: Change the PN and footprint from DFHS12FS203 to DFHS12FS238.

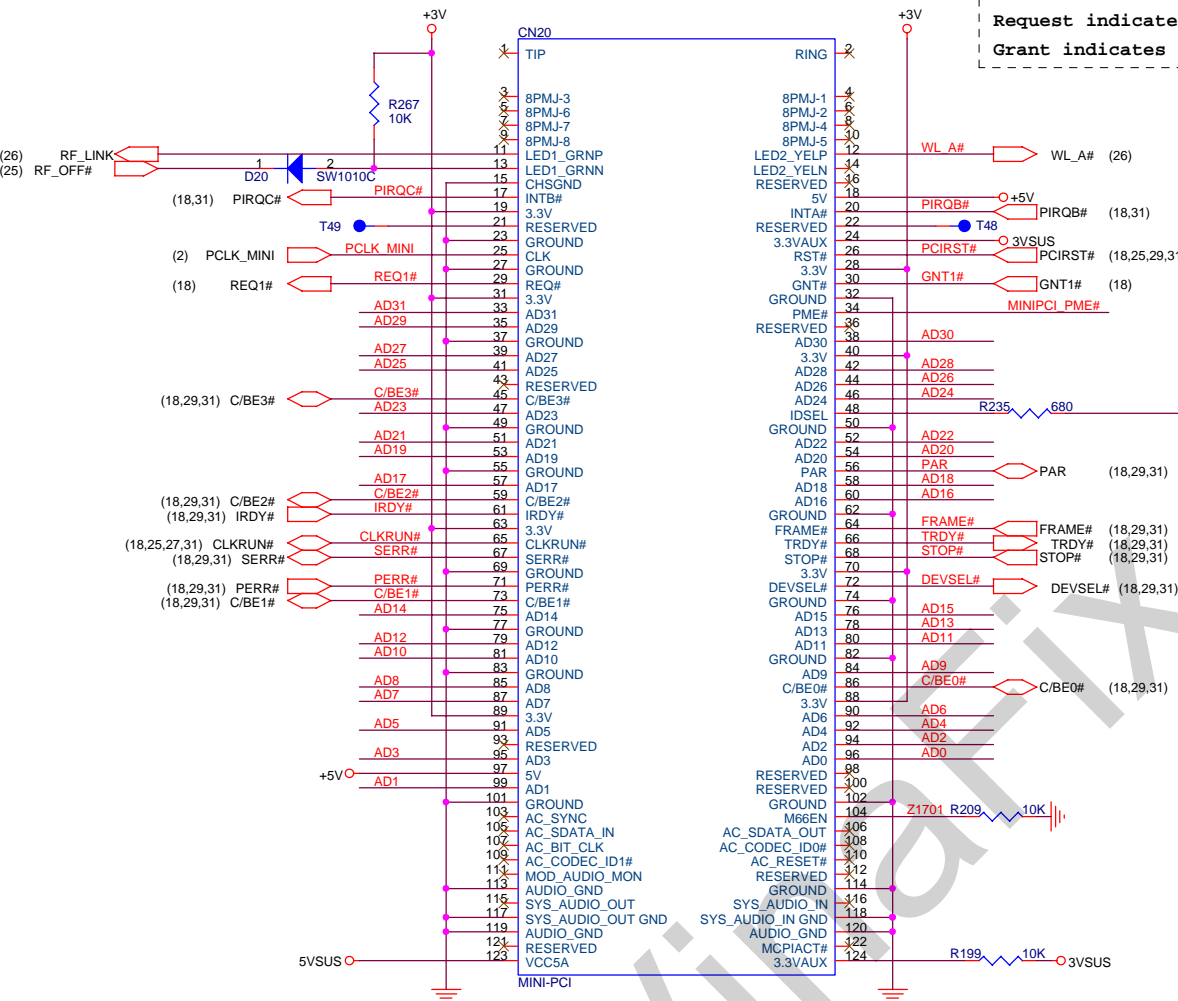
**PROJECT : MA1**  
**Quanta Computer Inc.**



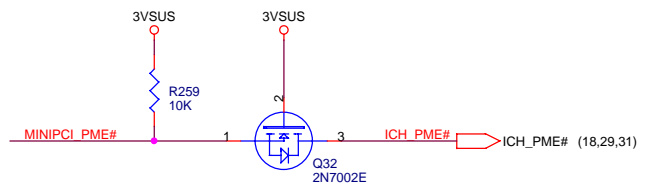
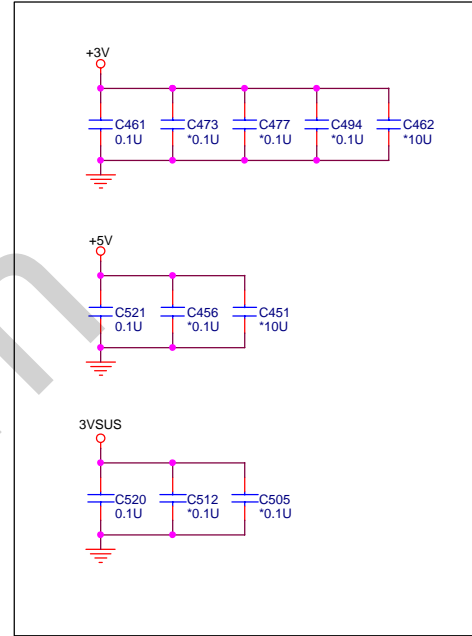
**PROJECT : MA1**  
**Quanta Computer Inc.**


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# TYPE III MINI PCI SOCKET



**ID Select** : AD20  
**Interrupt Pin** : PIRQB# , PIRQC#  
**Request indicates** : REQ1#  
**Grant indicates** : GNT1#




**PROJECT : MA1**  
**Quanta Computer Inc.**


Size B	Document Number	Rev 1A
<b>MINI PCI Socket &amp; MDC</b>		
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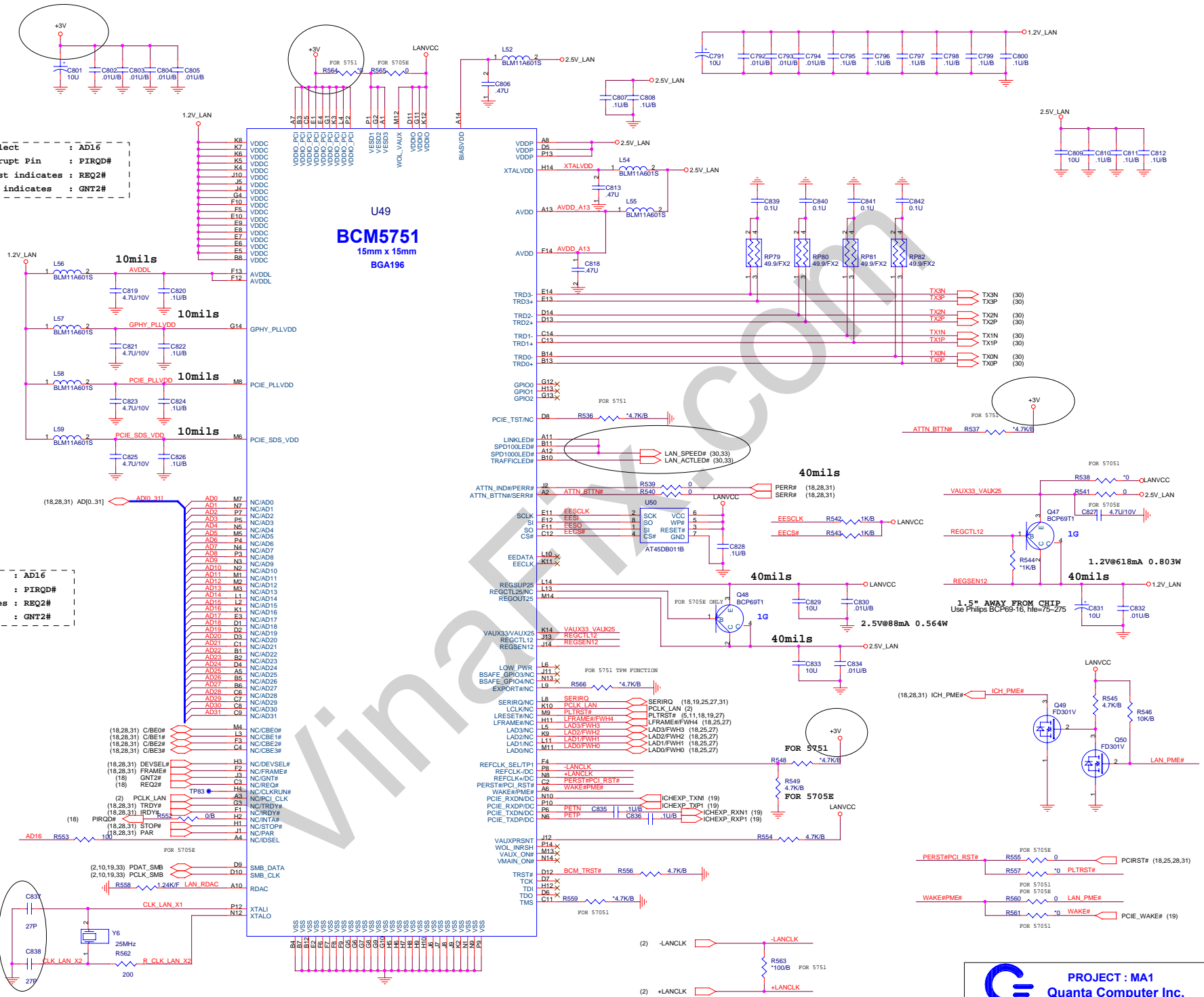
ID Select : AD16  
 Interrupt Pin : PIRQD#  
 Request indicates : REQ2#  
 Grant indicates : GNT2#

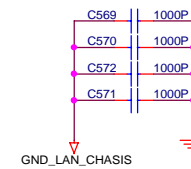
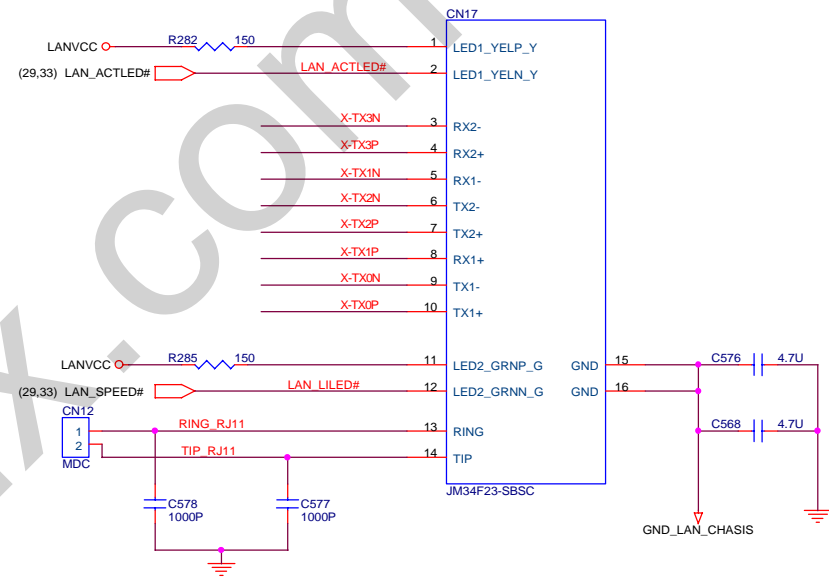
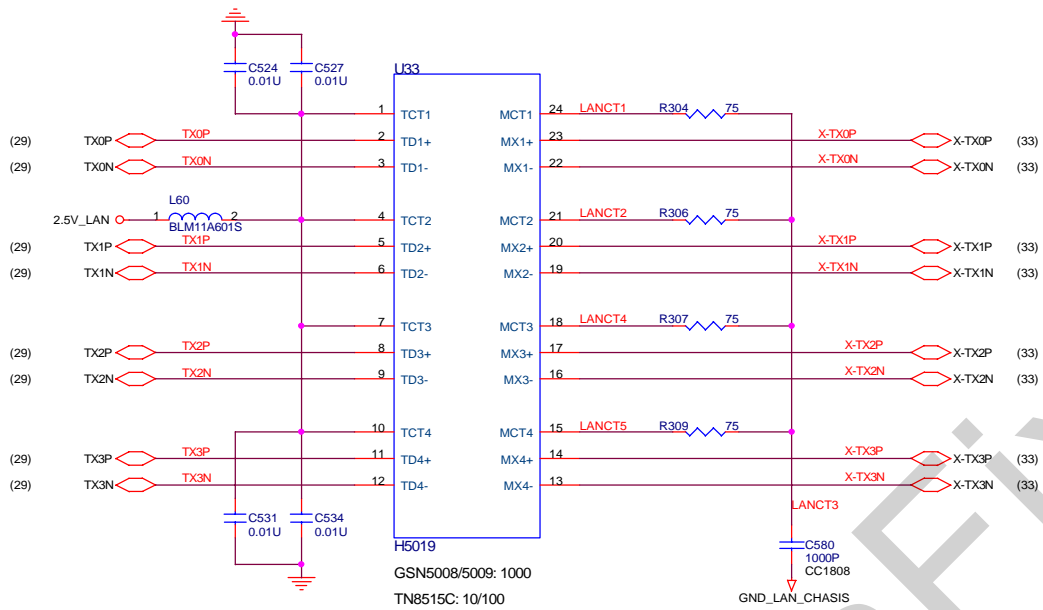
**U49**  
**BCM5751**  
 15mm x 15mm  
**BGA196**

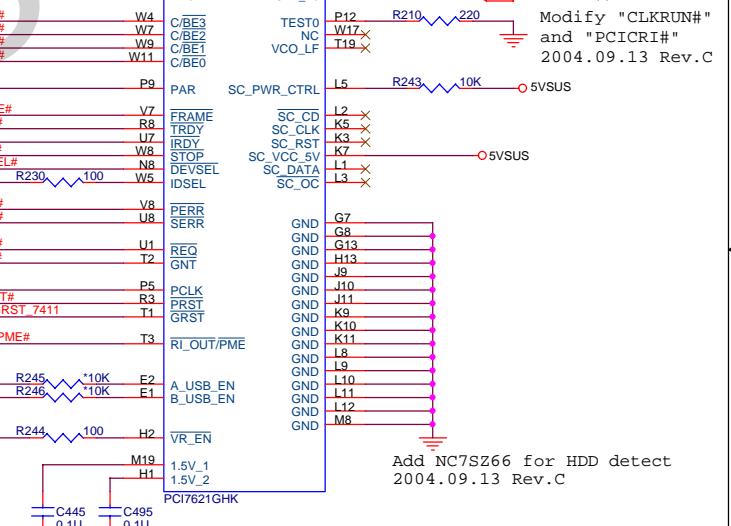
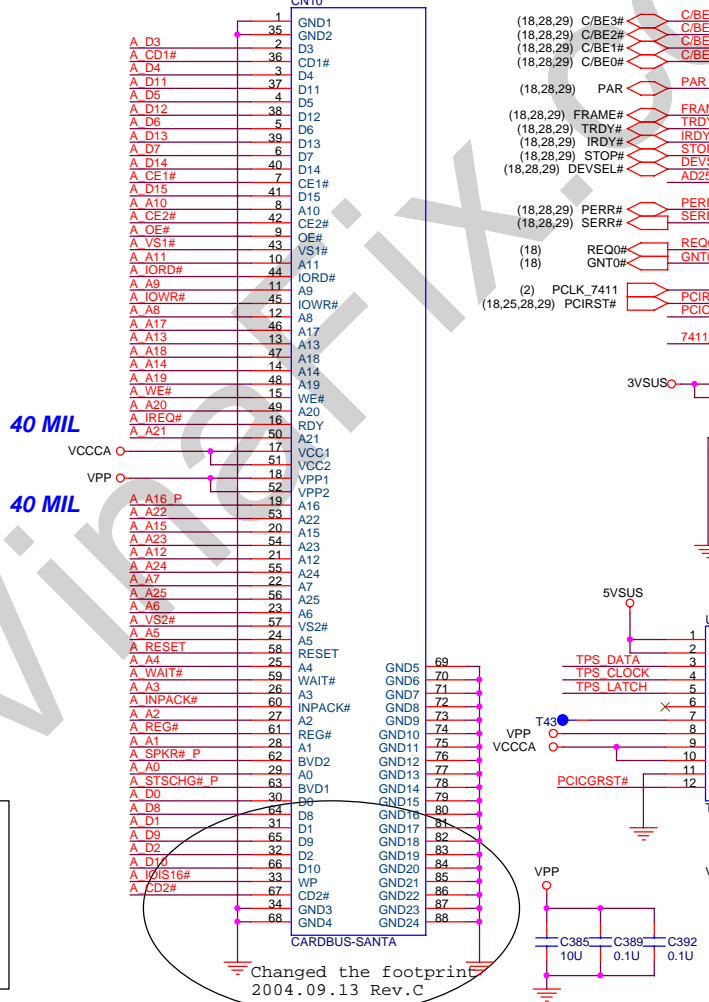
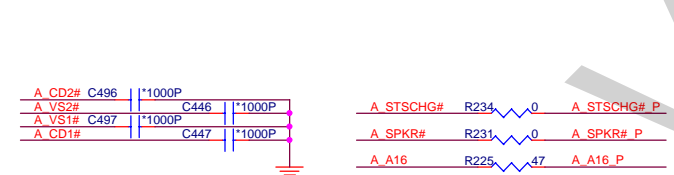
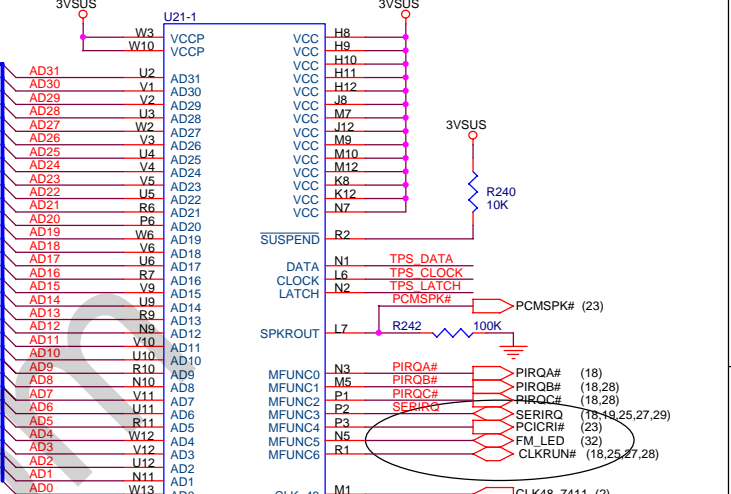
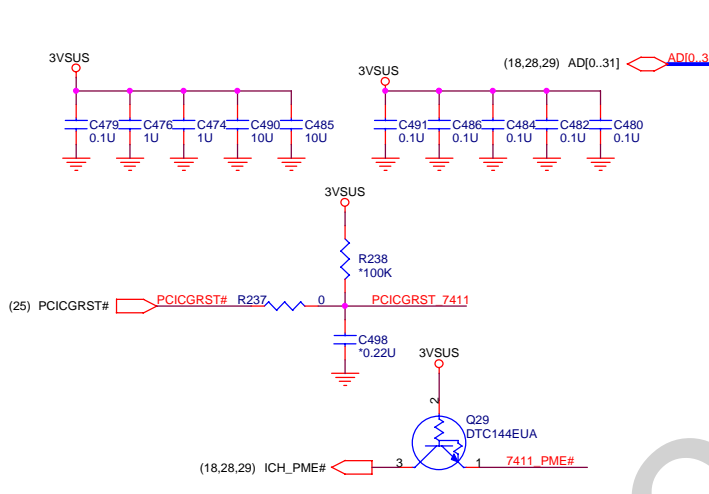
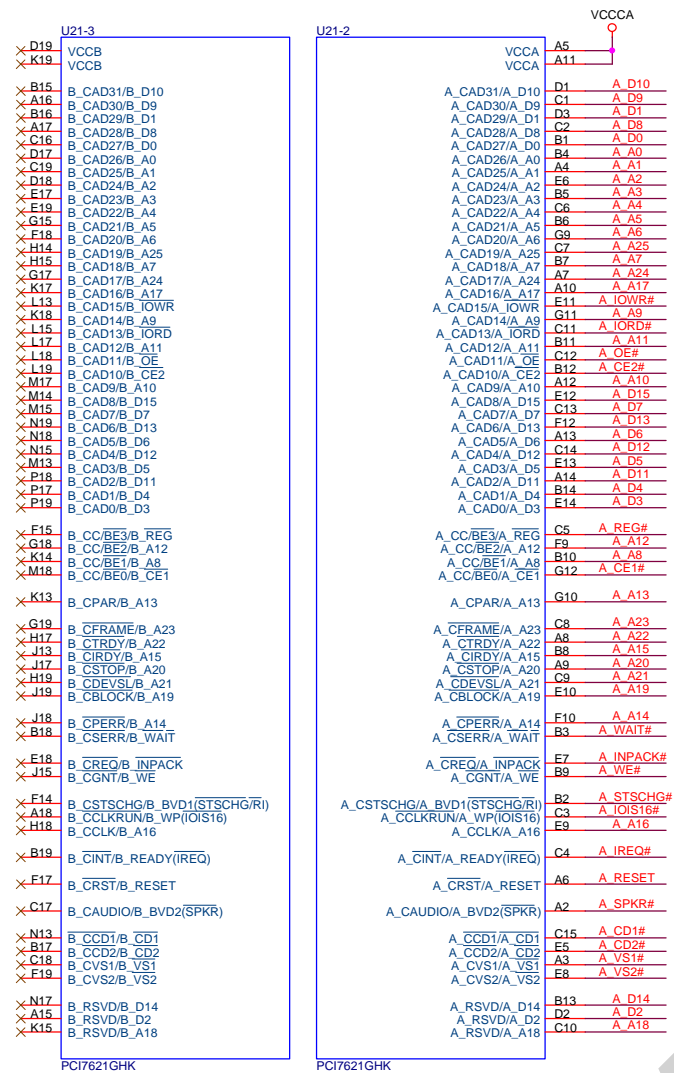
ID Select : AD16  
 Interrupt Pin : PIRQD#  
 Request indicates : REQ2#  
 Grant indicates : GNT2#

BCM4401 is for 10/100(1.8)  
 BCM5702 is for giga  
 BCM5705M is for giga cost-down(12)

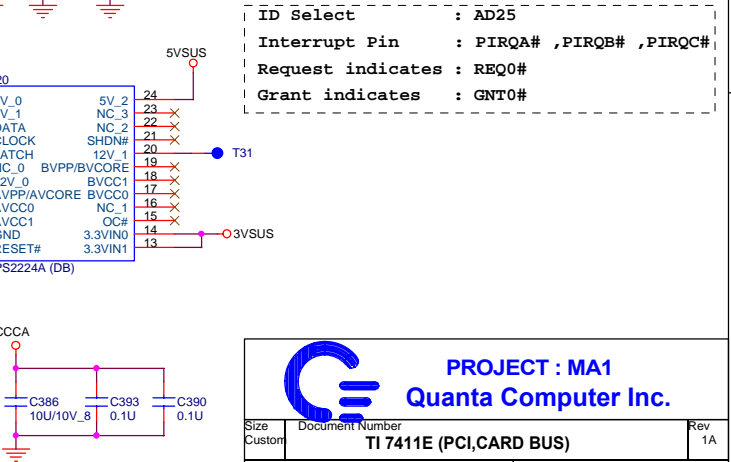
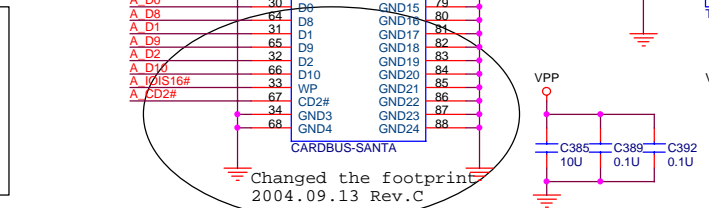
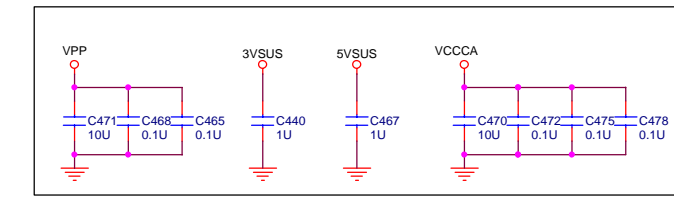

**PROJECT : MA1**  
**Quanta Computer Inc.**  
 Size C Document Number **BCM5705E/5751 LAN** Rev 1A  
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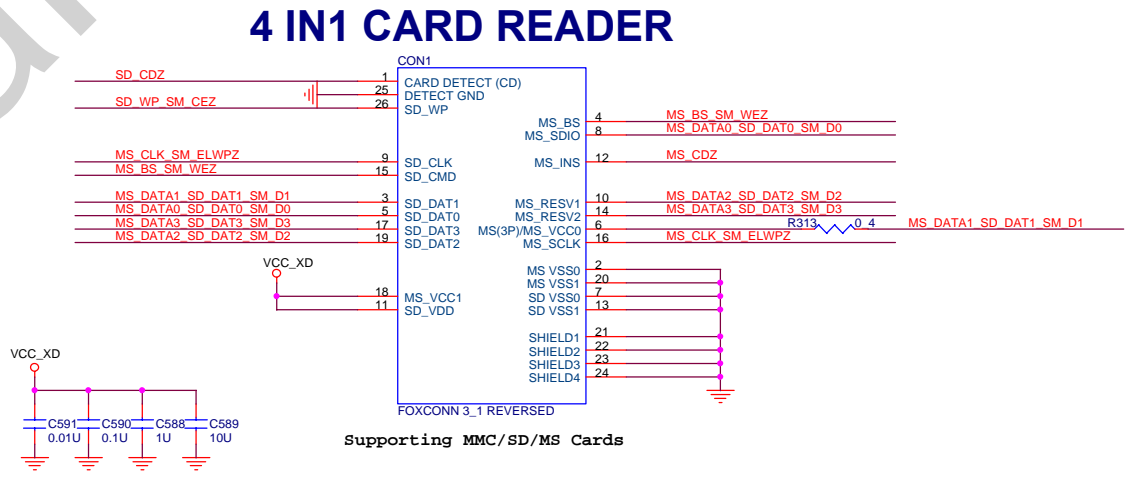
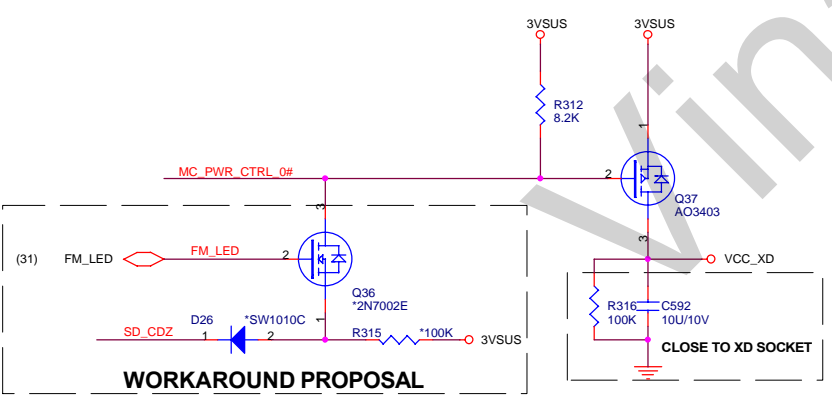
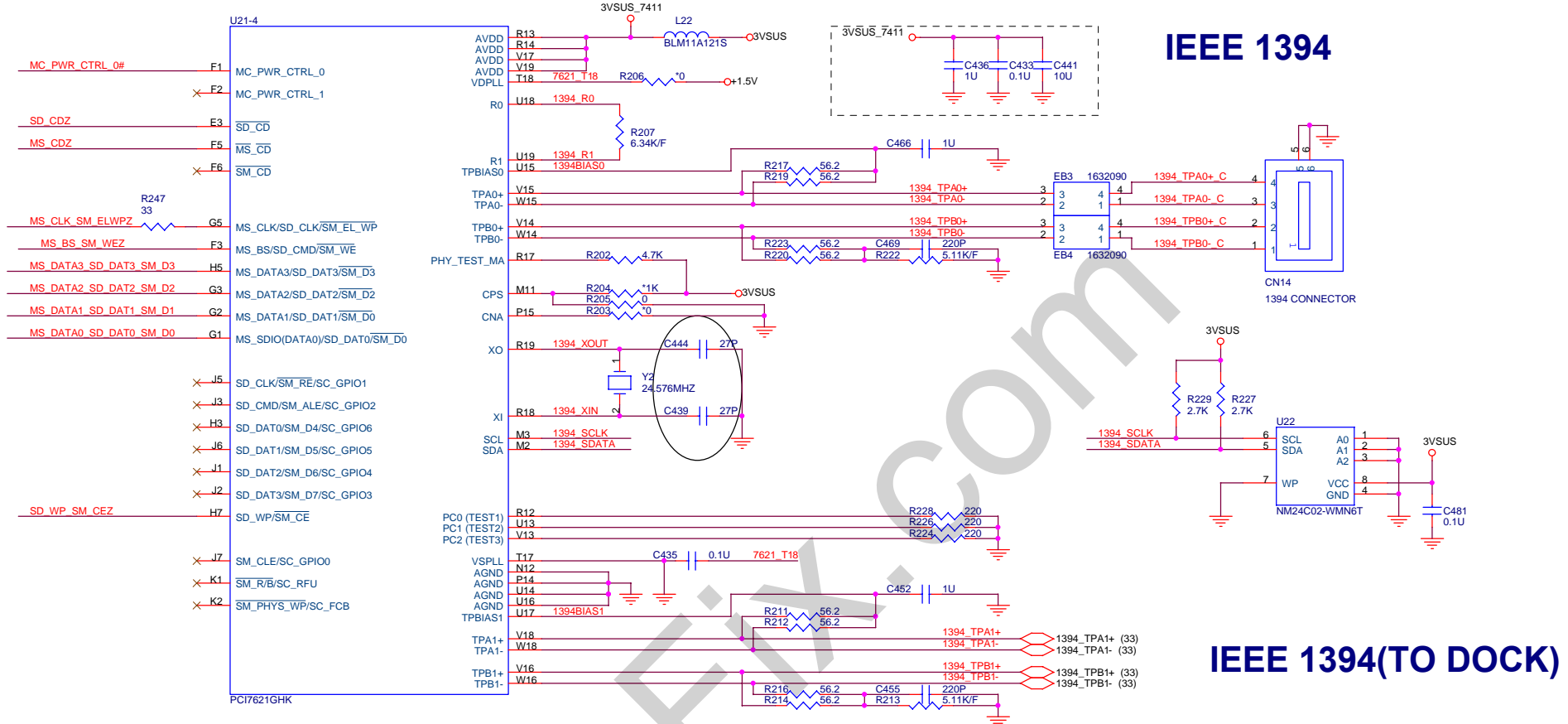
ID Select : AD25  
 Interrupt Pin : PIRQA# ,PIRQB# ,PIRQC#  
 Request indicates : REQ0#  
 Grant indicates : GNT0#



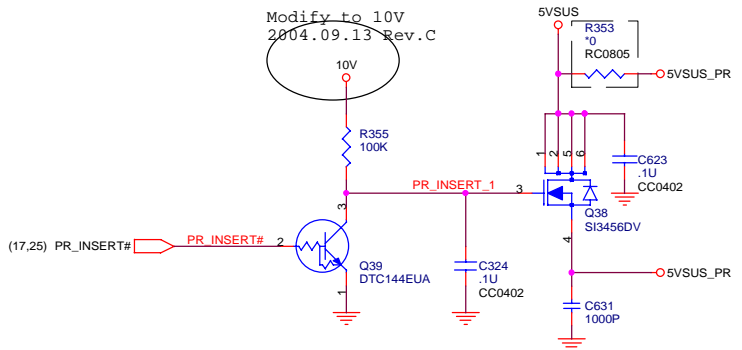
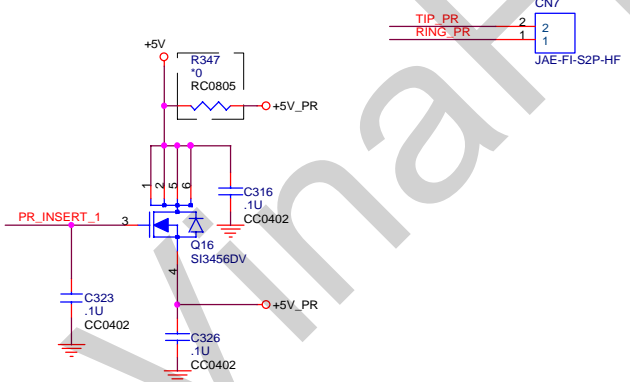
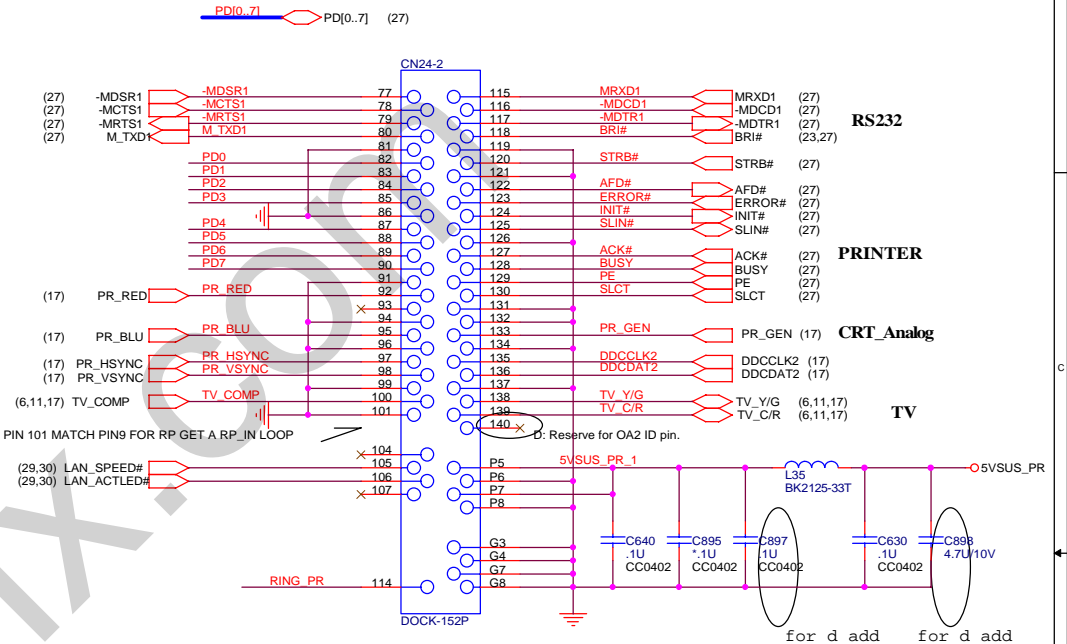
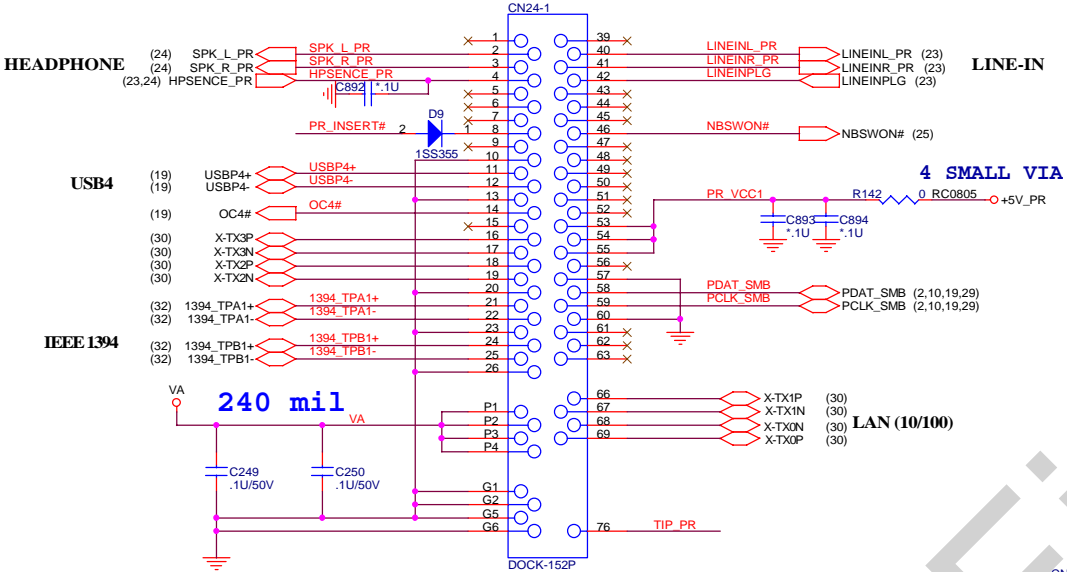
**PROJECT : MA1**  
**Quanta Computer Inc.**

Size Custom Document Number **TI 7411E (PCI,CARD BUS)** Rev 1A  
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Changed the footprint  
 2004.09.13 Rev.C

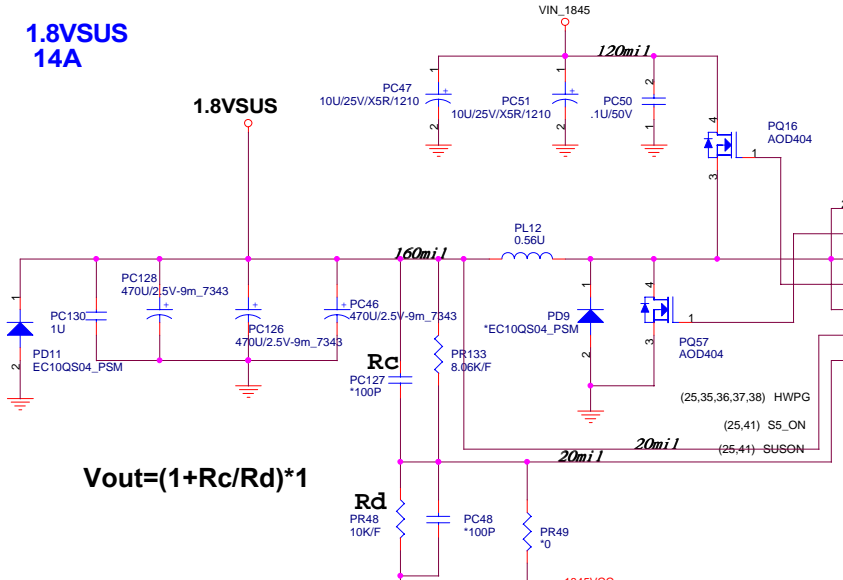




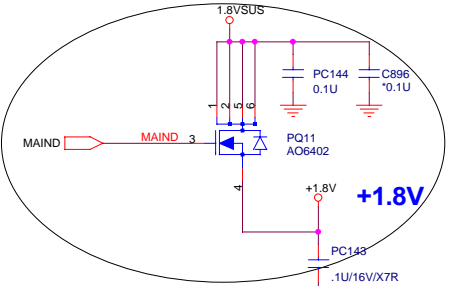
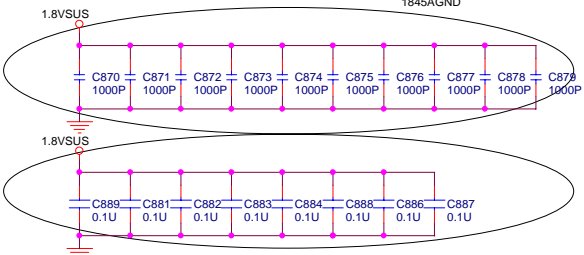


1.8VSUS  
14A

1.8VSUS



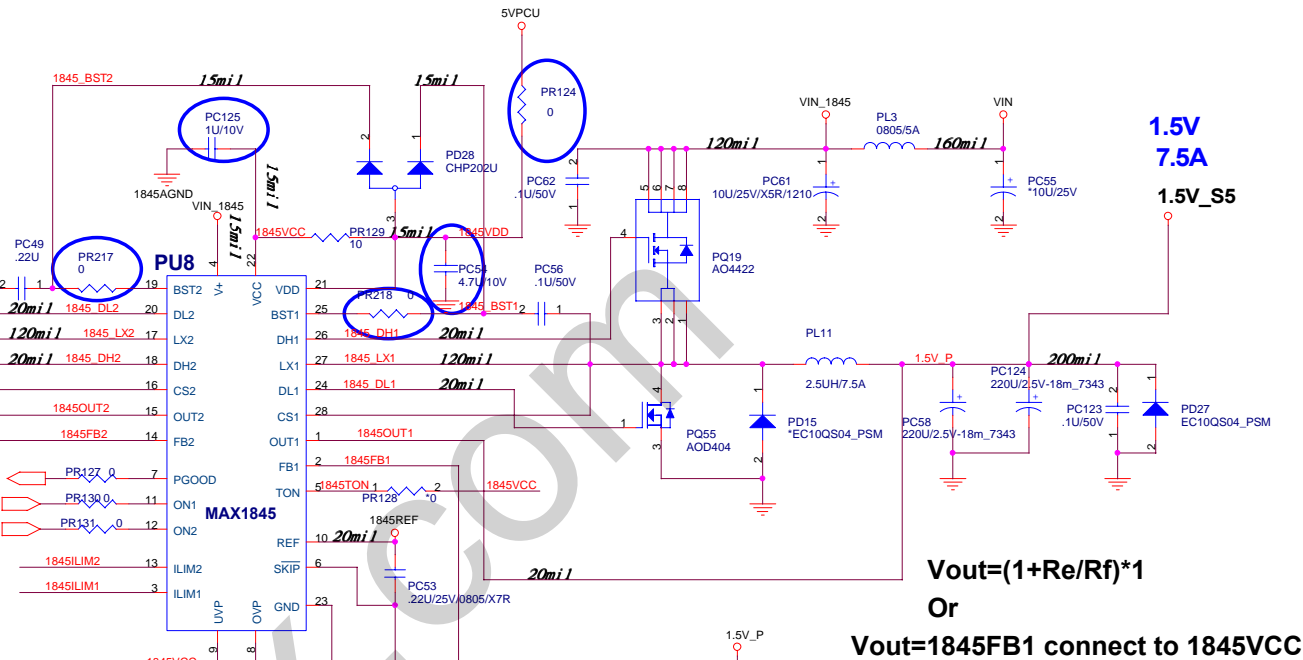
$V_{out} = (1 + R_c/R_d) * 1$



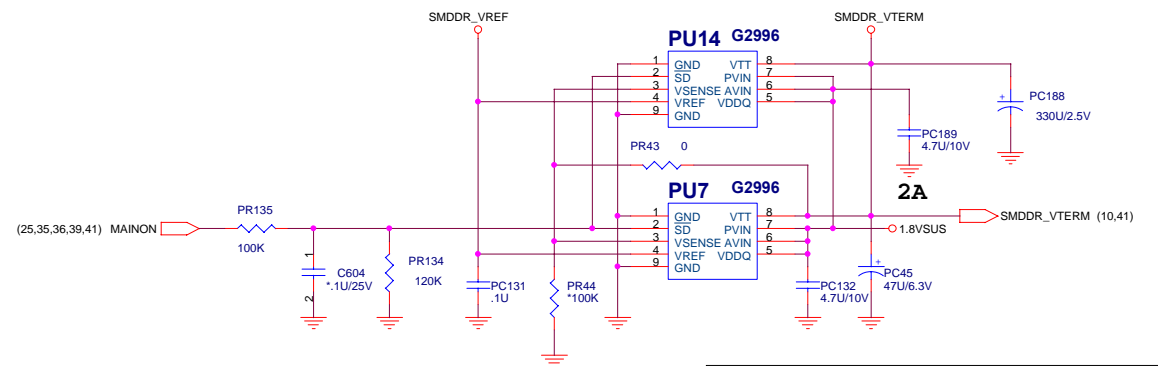
VDD\_MEM

1.5V  
7.5A

1.5V\_S5

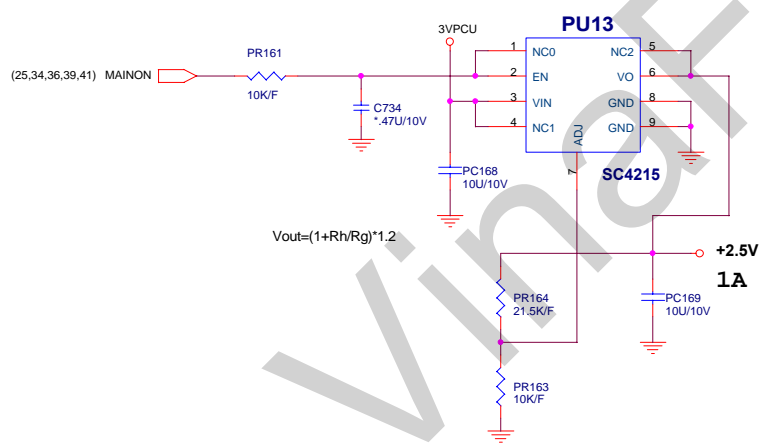
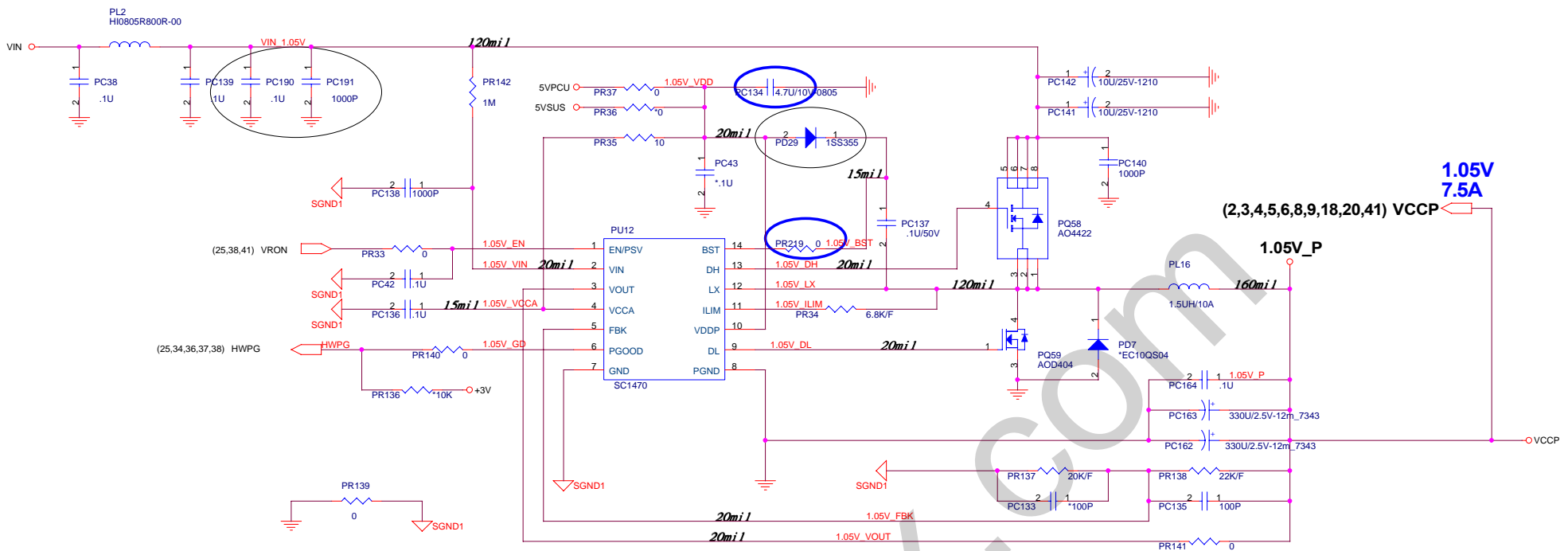


$V_{out} = (1 + R_e/R_f) * 1$   
Or  
 $V_{out} = 1845FB1$  connect to 1845VCC  
Fix  $V_{out} = 1.5V$

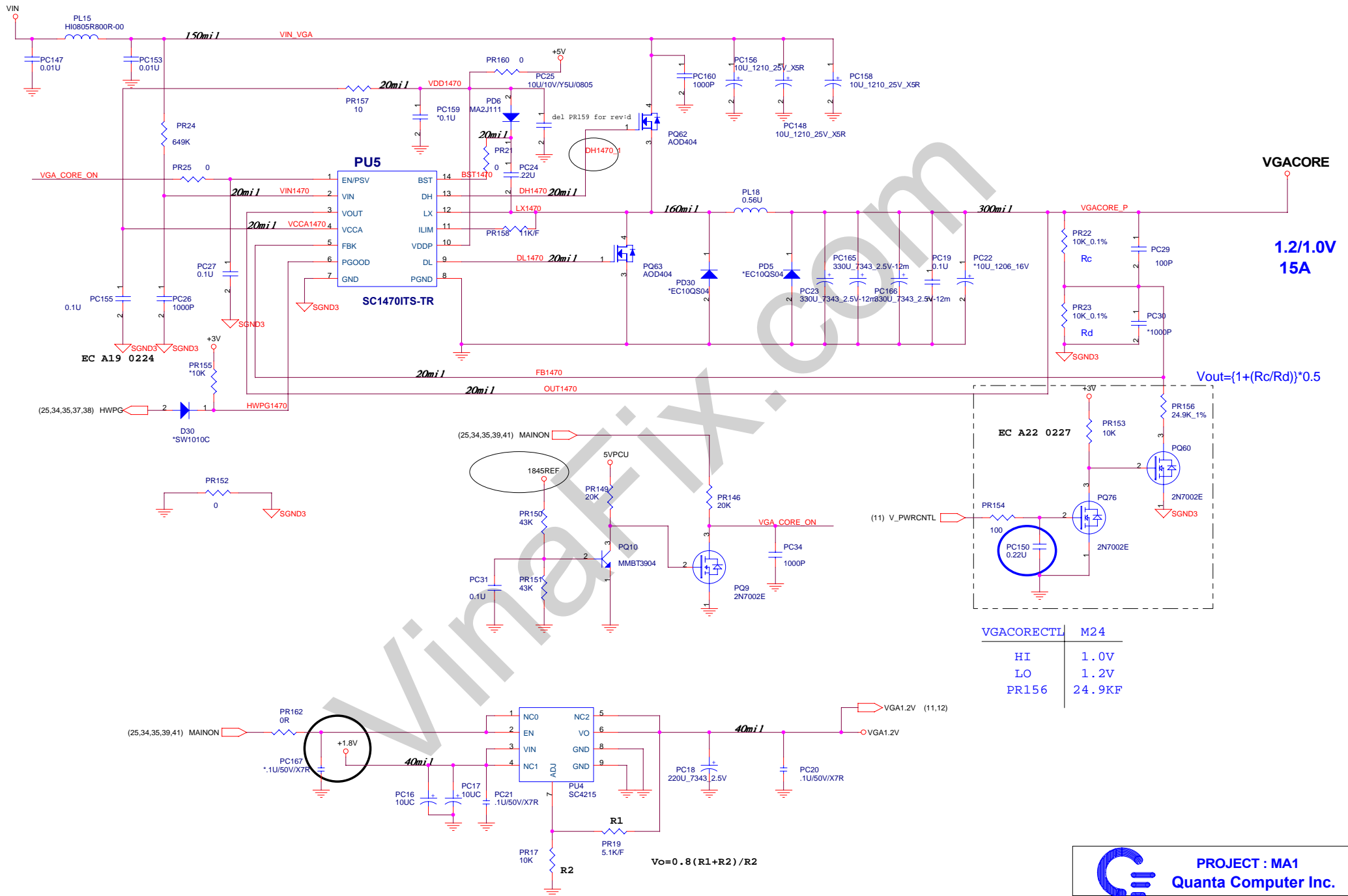


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**Quanta Computer Inc.**

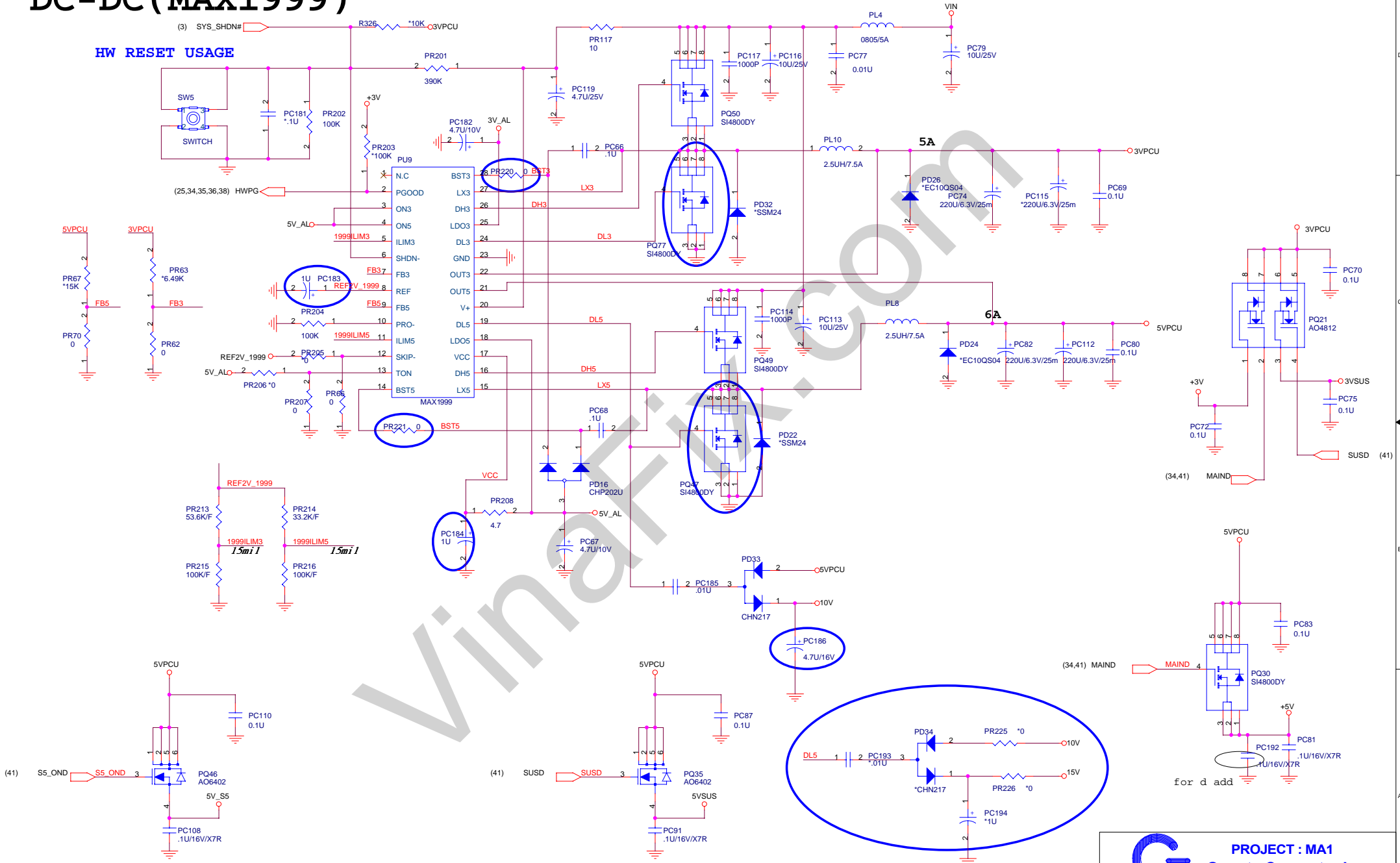
Size	Document Number	Rev
Custom	1.05V/1.5V	1A
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# VGA POWER

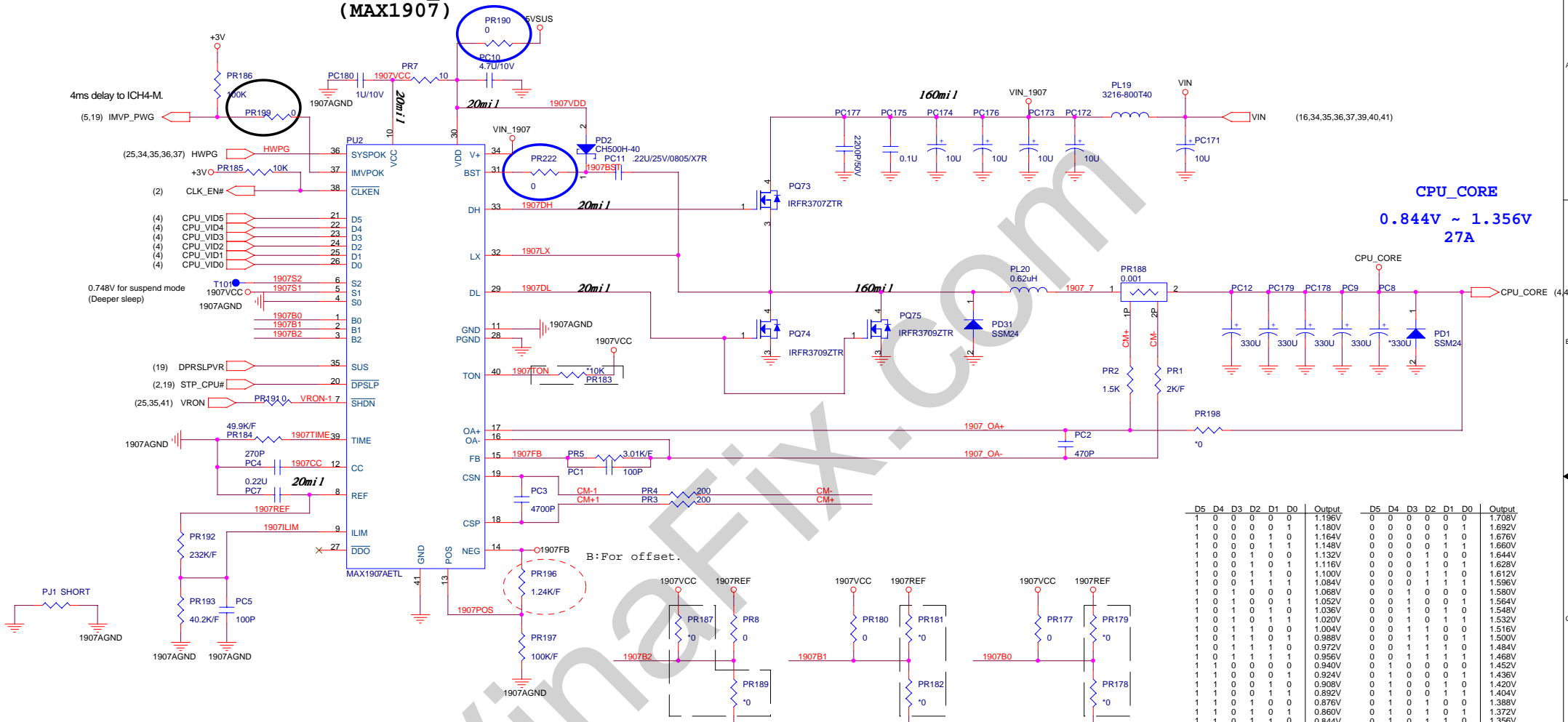


# DC-DC (MAX1999)



(21,26,28,31,33,35,37,41) 5VSUS  
 (16,18,22,25,26,33,37,39,40,41) 3VPCU  
 (2,3,8,10,11,12,13,16,18,19,20,22,24,25,26,27,28,29,35,36,37,41) +3V

### CPU VCC CORE (MAX1907)

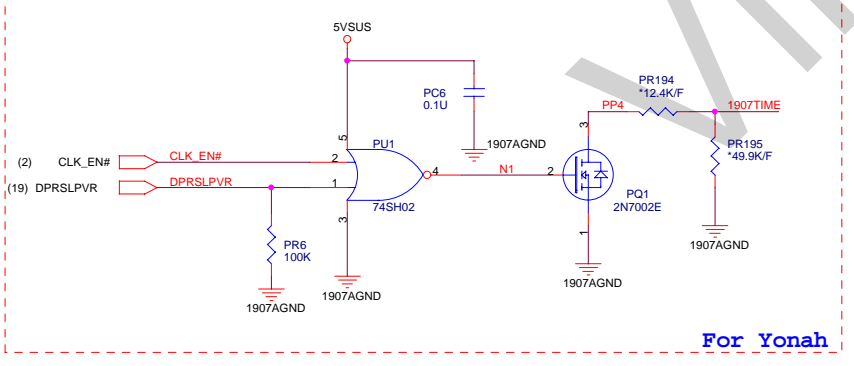


**CPU\_CORE**  
 0.844V ~ 1.356V  
 27A

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	1	0	0	0	1.084V	0	0	0	1	0	0	1.596V
1	0	1	0	0	1	1.068V	0	0	0	1	0	1	1.580V
1	0	1	0	1	0	1.052V	0	0	0	1	0	1	1.564V
1	0	1	0	1	1	1.036V	0	0	0	1	1	0	1.548V
1	0	1	1	0	0	1.020V	0	0	0	1	0	0	1.532V
1	0	1	1	0	1	1.004V	0	0	0	1	0	1	1.516V
1	0	1	1	1	0	0.988V	0	0	0	1	1	0	1.500V
1	0	1	1	1	1	0.972V	0	0	0	1	1	1	1.484V
1	1	0	0	0	0	0.956V	0	0	0	1	0	0	1.468V
1	1	0	0	0	1	0.940V	0	0	0	1	0	1	1.452V
1	1	0	0	1	0	0.924V	0	0	0	1	0	0	1.436V
1	1	0	0	1	1	0.908V	0	0	0	1	0	1	1.420V
1	1	0	1	0	0	0.892V	0	0	0	1	0	1	1.404V
1	1	0	1	0	1	0.876V	0	0	0	1	0	0	1.388V
1	1	0	1	1	0	0.860V	0	0	0	1	0	1	1.372V
1	1	1	0	0	0	0.844V	0	0	0	1	0	0	1.356V
1	1	1	0	0	1	0.828V	0	0	0	1	0	1	1.340V
1	1	1	0	1	0	0.812V	0	0	0	1	0	0	1.324V
1	1	1	0	1	1	0.796V	0	0	0	1	0	1	1.308V
1	1	1	1	0	0	0.780V	0	0	0	1	0	0	1.292V
1	1	1	1	0	1	0.764V	0	0	0	1	0	1	1.276V
1	1	1	1	1	0	0.748V	0	0	0	1	0	0	1.260V
1	1	1	1	1	1	0.732V	0	0	0	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	0	0	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	0	0	1	1	1	1.212V

SUSPEND MODE (SUS=HIGH)				Output
S2	S1	S0		
✓	OPEN	VCC	GND	0.748V

VCC_BOOT				Output
B2	B1	B0		
✓	GND	GND	GND	1.708V
	REF	REF	REF	1.372V
	OPEN	OPEN	OPEN	1.036V
	VCC	VCC	VCC	0.700V
	REF	VCC	VCC	1.212V



For Yonah

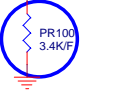
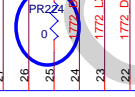
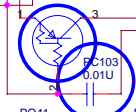
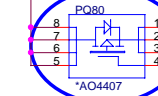
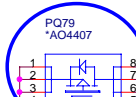
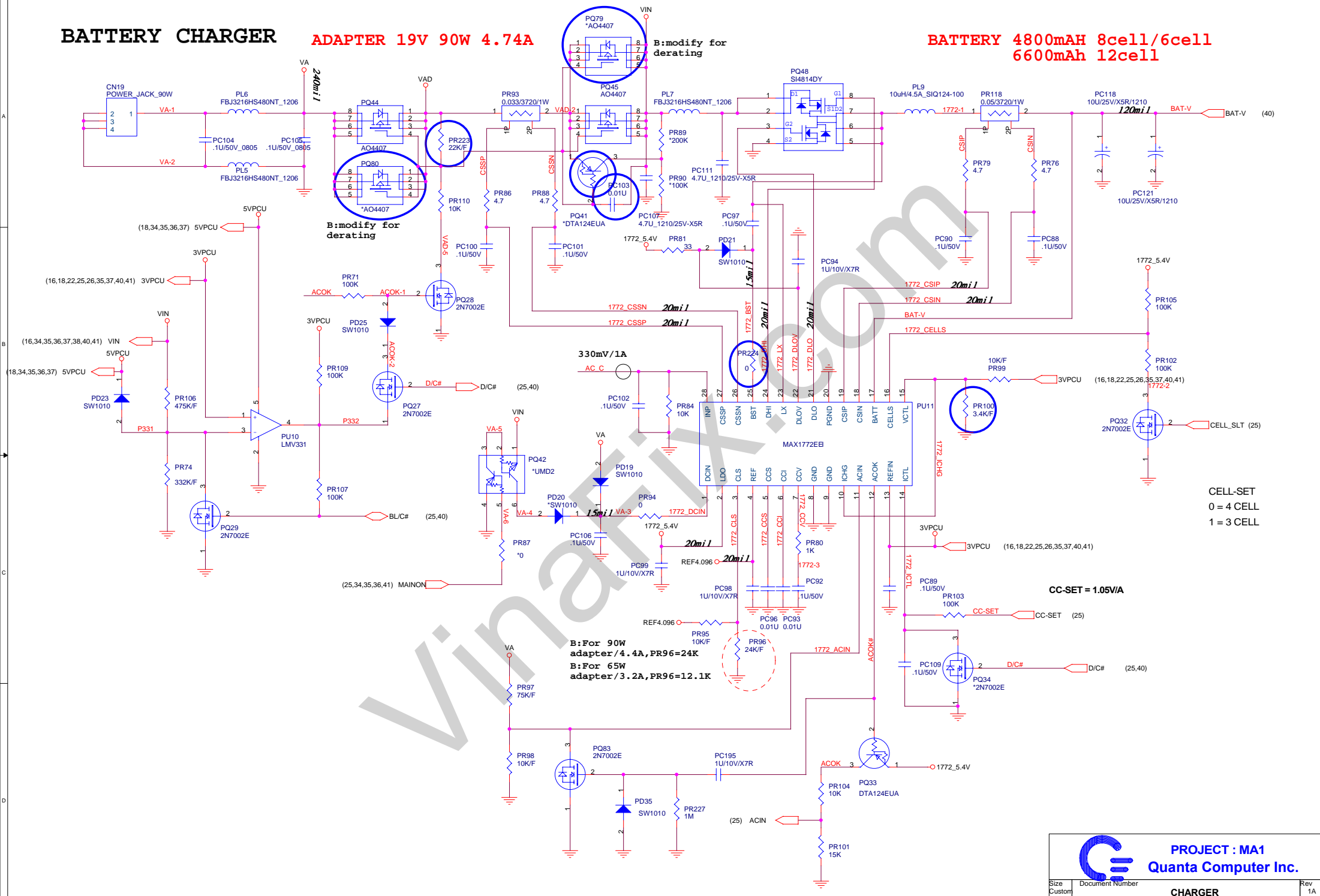
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**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>Block Diagram</b>	1A
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# BATTERY CHARGER

ADAPTER 19V 90W 4.74A


BATTERY 4800mAh 8cell/6cell  
6600mAh 12cell

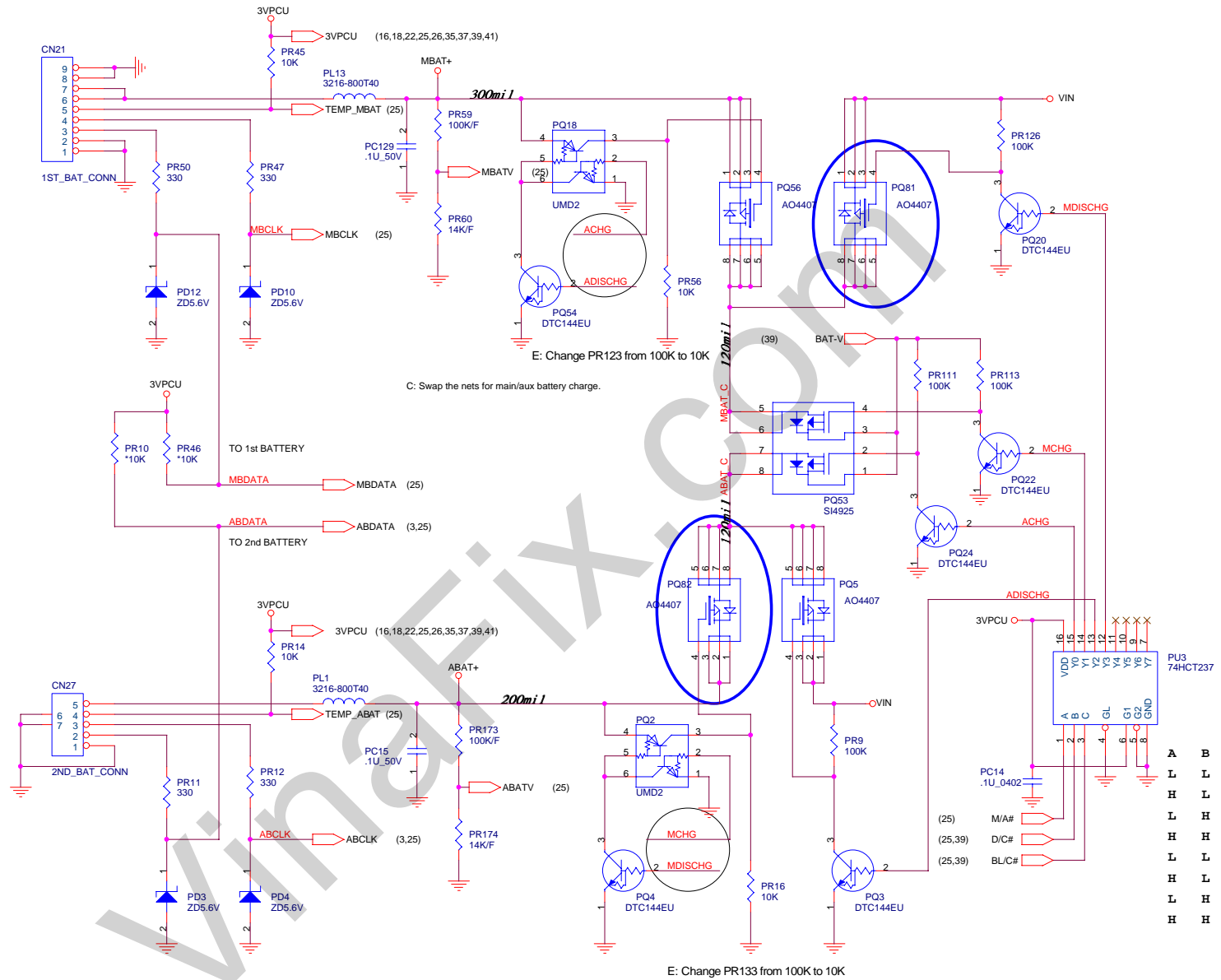


B:For 90W  
adapter/4.4A, PR96=24K  
B:For 65W  
adapter/3.2A, PR96=12.1K

CELL-SET  
0 = 4 CELL  
1 = 3 CELL

CC-SET = 1.05V/A


		
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Quanta Computer Inc.		
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CHARGER		
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E: Change PR123 from 100K to 10K  
 C: Swap the nets for main/aux battery charge.

E: Change PR133 from 100K to 10K

	A	B	C	Y0	Y1	Y2	Y3
1ST_BAT_CONN	L	L	L	H	L	L	L
2ND_BAT_CONN	H	L	L	L	H	L	L
TEMP_MBAT (25)	L	H	L	L	L	H	L
TEMP_ABAT (25)	L	L	H	L	L	L	L
MBAT+ (300mI)	H	L	H	L	L	L	L
ABAT+ (200mI)	L	H	H	L	L	L	L



**PROJECT : MA1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
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