

Compal Confidential

NIWE2

Schematics Document

Arrandale

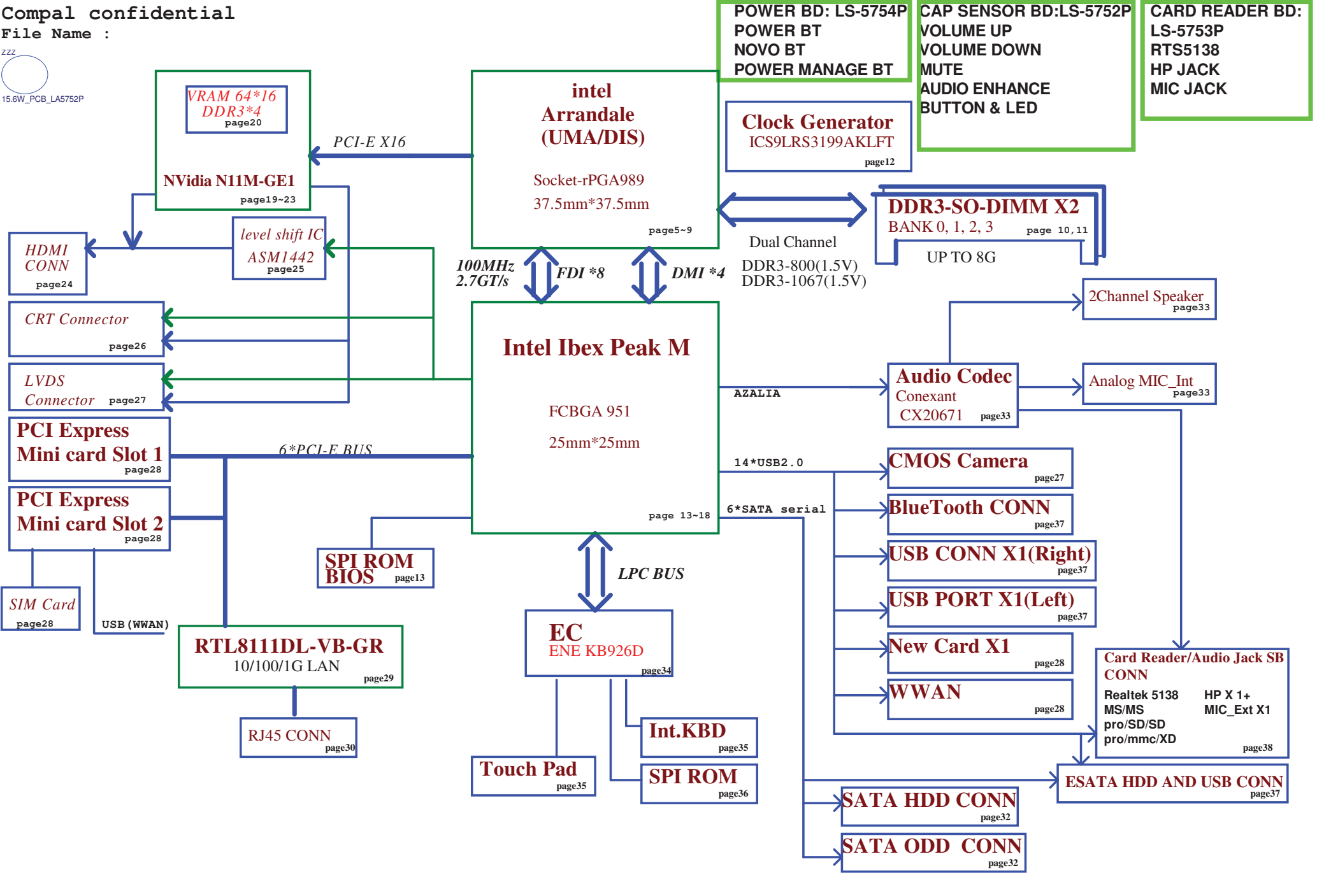
with Intel IBEX PEAK-M core logic

REV: 0.3

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet	
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15.6W_PCB_LA5752P



Security Classification		Compal Secret Data		Title	
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DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS
				+3VS
State				+1.5VS
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+1.8VS
				+0.75VS
				+1.05VS
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V +3VALW	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW											
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V +3VALW
SMB_EC_DA2	+3VALW											
SMBCLK	PCH	V +3VALW	X	X	V +3VS	V +3VS	X	X	X	X	V +3VS	X
SMBDATA	+3VALW											
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V +3VALW	X	X	X	V +3VS	X	V +3VS	X	X
SML1DATA	+3VALW											

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

	EVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA HDMI@	FOR UMA HDMI components	
HDMI@	FOR HDMI components	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
ESATA@	ESATA function	
CMOS@	Camera function	
BT@	Blue Tooth	
10M@	FOR 10M CHIP	
11M@	FOR 11M CHIP	
UMA@	UMA only (Arranddale)	
DIS@	DIS only (Arranddale)	
VGA@	FOR NVIDIA PART	
HYBRID@	FOR SWITCHABLE	
HU@	SWITCHABLE or UMA only	
HD@	SWITCHABLE or DIS only	

SKU

Arranddale (dGPU) DIS only	DIS@ / 100@ for EVT
Arranddale (iGPU) UMA only	UMA@ / 100@ for EVT
Arranddale (iGPU+dGPU) SWITCHABLE	VGA@+HD@+HU@+HYBRID@

PCIe PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID or Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6 GPIO5 N10M-GS N10P-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0, 10
1	1	1.0V (N10M-GS) 0.925V (N10P-GS)	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

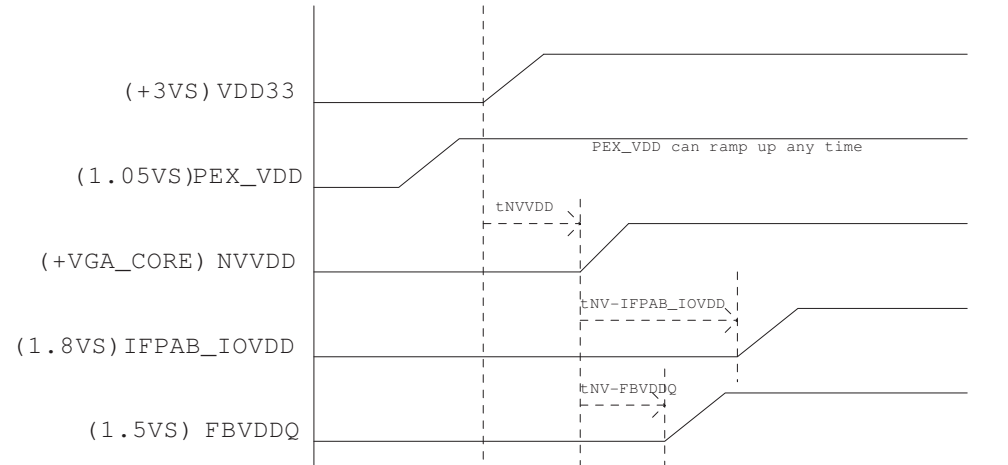
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (mA)		I/O and PLLVDD (1.8V) (mA)		I/O and PLLVDD (1.05V) (mA)		Other (3.3V) (mA)	
				(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (mA)		I/O and PLLVDD (1.8V) (mA)		I/O and PLLVDD (1.05V) (mA)		Other (3.3V) (mA)	
				(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

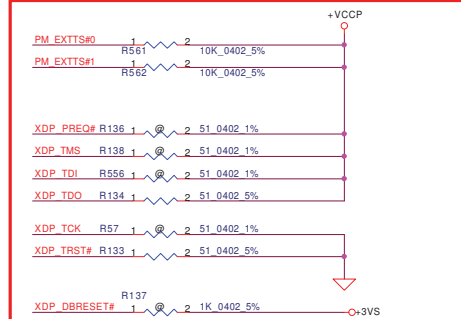
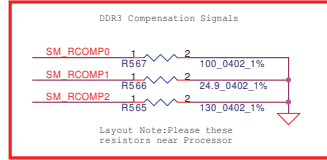
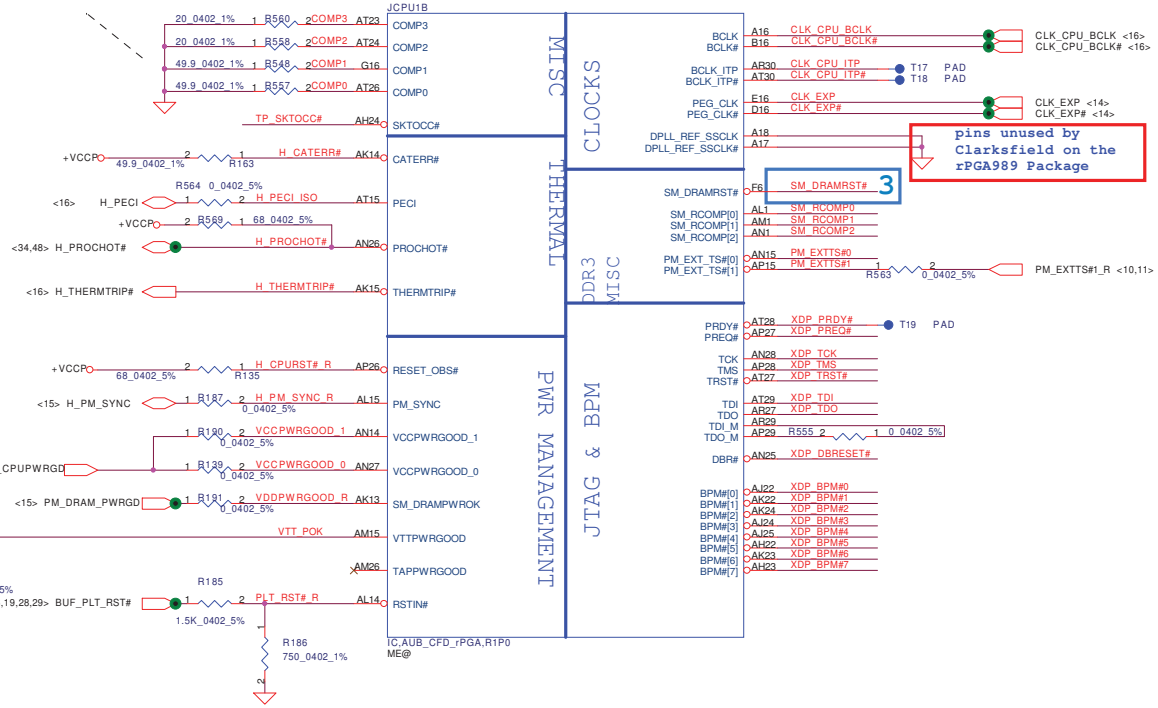
Power Sequence

The ramp time for any rail must be more than 40us

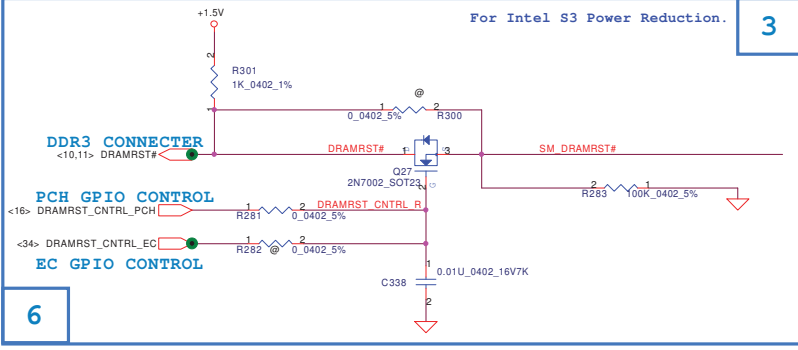
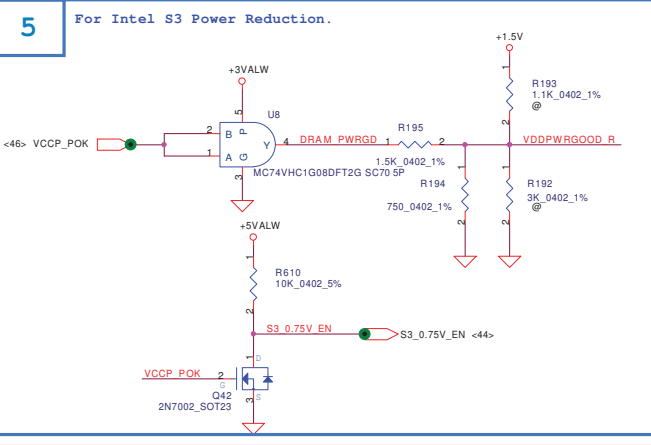
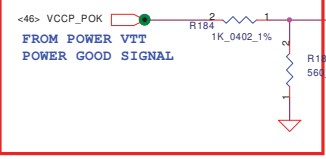


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				VGA Notes List		
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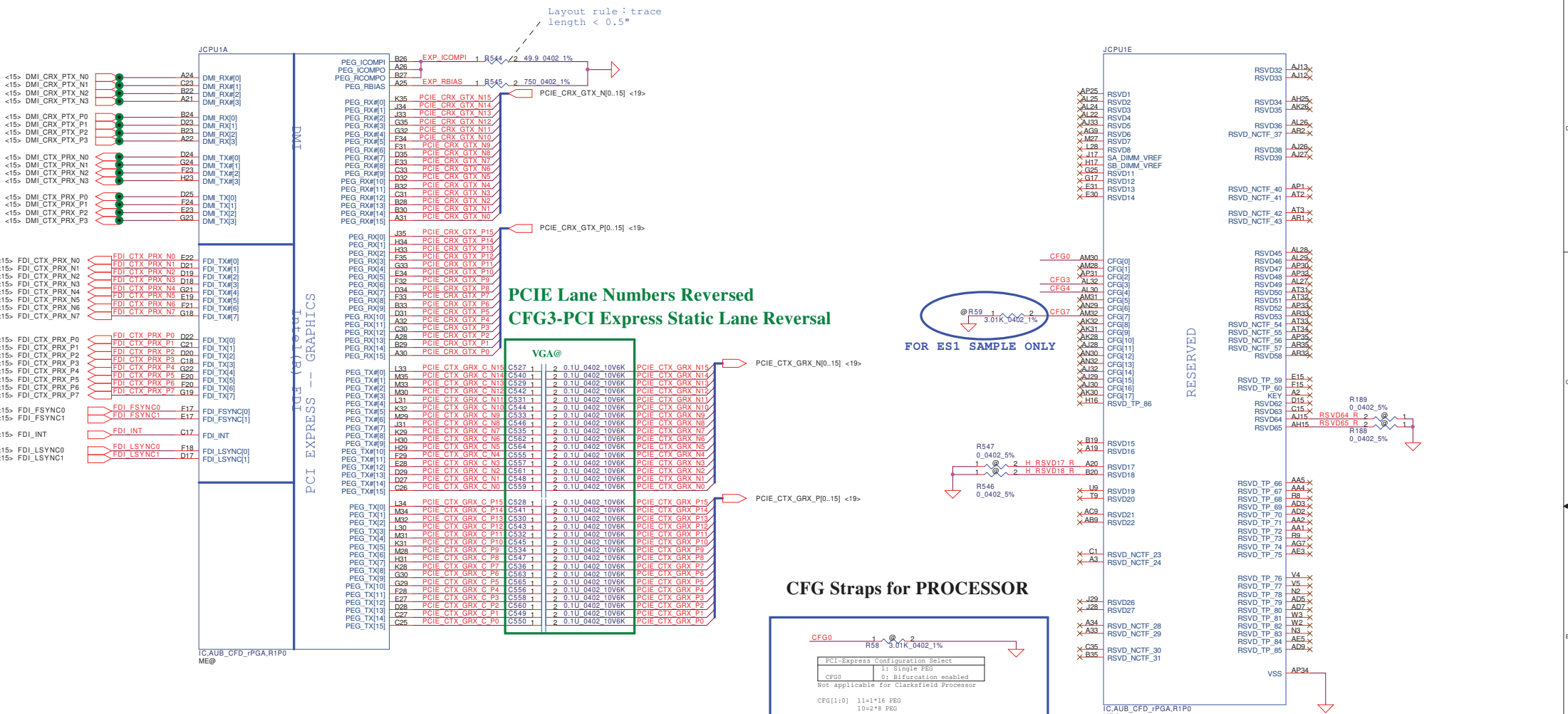
Layout rule: 10mil width trace
length < 0.5", spacing 20mil



**CHECK INTEL DOCUMENT #385422
Debug Port Design Guide Rev1.3**



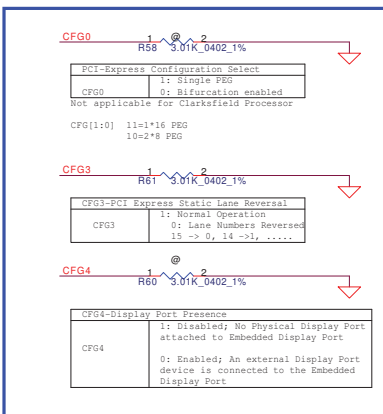
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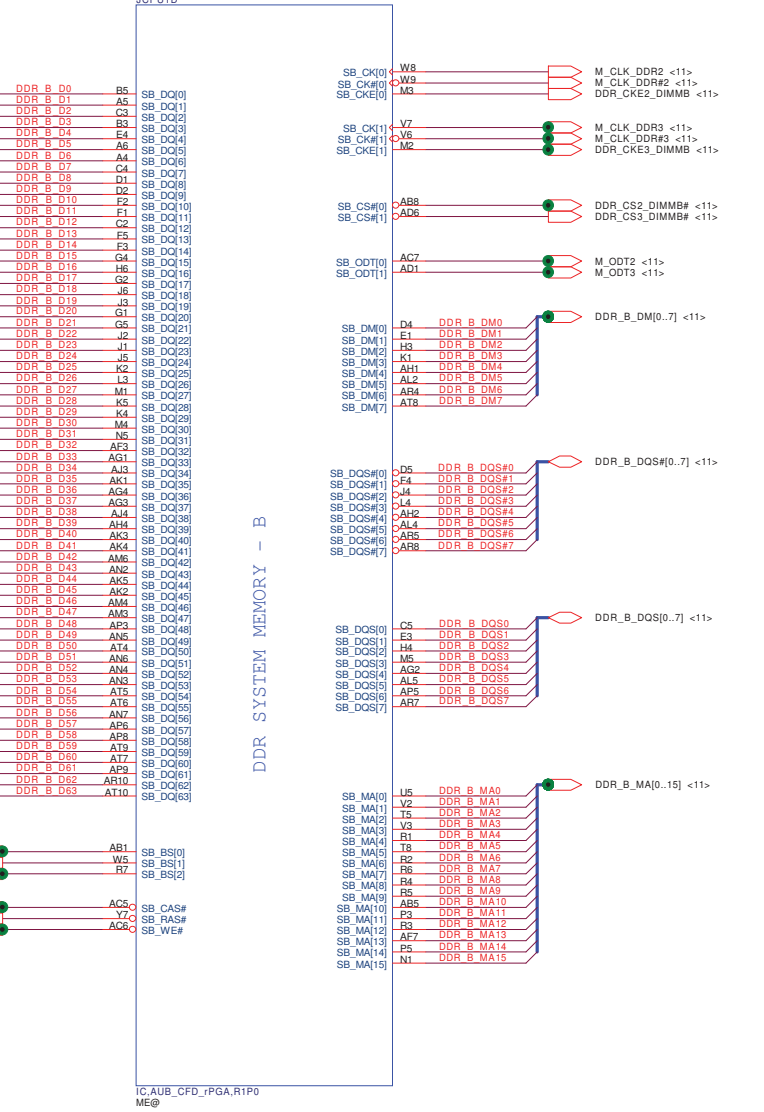
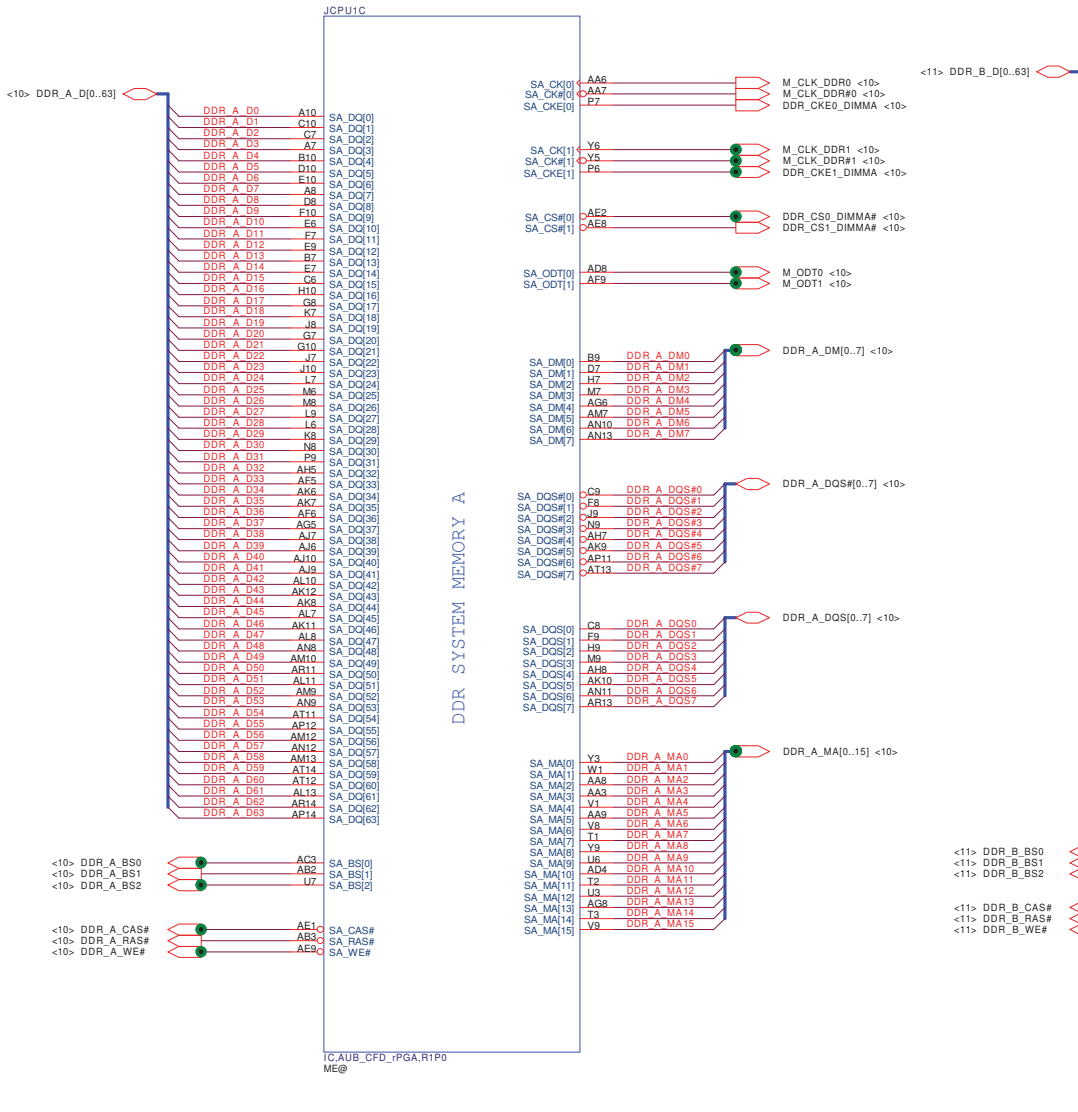
PCIE Lane Numbers Reversed CFG3-PCI Express Static Lane Reversal

PCIE CTX GRX N	PCIE CTX GRX P	PCIE CTX GRX C	PCIE CTX GRX N	PCIE CTX GRX P	PCIE CTX GRX C
133	134	135	136	137	138
139	140	141	142	143	144
145	146	147	148	149	150
153	154	155	156	157	158
159	160	161	162	163	164
165	166	167	168	169	170
173	174	175	176	177	178
183	184	185	186	187	188
193	194	195	196	197	198
203	204	205	206	207	208
213	214	215	216	217	218
223	224	225	226	227	228
233	234	235	236	237	238
243	244	245	246	247	248
253	254	255	256	257	258
263	264	265	266	267	268
273	274	275	276	277	278
283	284	285	286	287	288
293	294	295	296	297	298
303	304	305	306	307	308
313	314	315	316	317	318
323	324	325	326	327	328
333	334	335	336	337	338
343	344	345	346	347	348
353	354	355	356	357	358
363	364	365	366	367	368
373	374	375	376	377	378
383	384	385	386	387	388
393	394	395	396	397	398
403	404	405	406	407	408
413	414	415	416	417	418
423	424	425	426	427	428
433	434	435	436	437	438
443	444	445	446	447	448
453	454	455	456	457	458
463	464	465	466	467	468
473	474	475	476	477	478
483	484	485	486	487	488
493	494	495	496	497	498
503	504	505	506	507	508
513	514	515	516	517	518
523	524	525	526	527	528
533	534	535	536	537	538
543	544	545	546	547	548
553	554	555	556	557	558
563	564	565	566	567	568
573	574	575	576	577	578
583	584	585	586	587	588
593	594	595	596	597	598
603	604	605	606	607	608
613	614	615	616	617	618
623	624	625	626	627	628
633	634	635	636	637	638
643	644	645	646	647	648
653	654	655	656	657	658
663	664	665	666	667	668
673	674	675	676	677	678
683	684	685	686	687	688
693	694	695	696	697	698
703	704	705	706	707	708
713	714	715	716	717	718
723	724	725	726	727	728
733	734	735	736	737	738
743	744	745	746	747	748
753	754	755	756	757	758
763	764	765	766	767	768
773	774	775	776	777	778
783	784	785	786	787	788
793	794	795	796	797	798
803	804	805	806	807	808
813	814	815	816	817	818
823	824	825	826	827	828
833	834	835	836	837	838
843	844	845	846	847	848
853	854	855	856	857	858
863	864	865	866	867	868
873	874	875	876	877	878
883	884	885	886	887	888
893	894	895	896	897	898
903	904	905	906	907	908
913	914	915	916	917	918
923	924	925	926	927	928
933	934	935	936	937	938
943	944	945	946	947	948
953	954	955	956	957	958
963	964	965	966	967	968
973	974	975	976	977	978
983	984	985	986	987	988
993	994	995	996	997	998
1003	1004	1005	1006	1007	1008

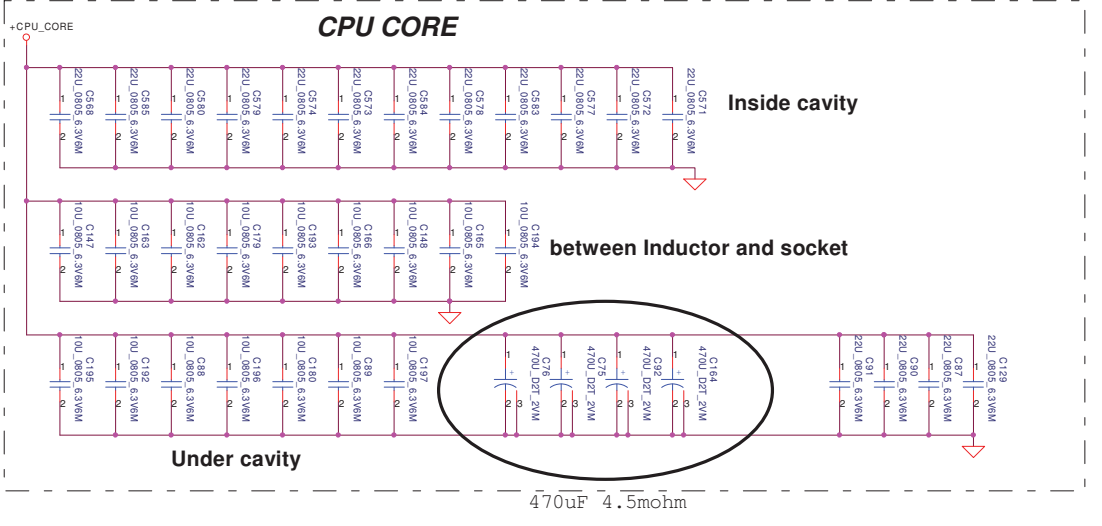
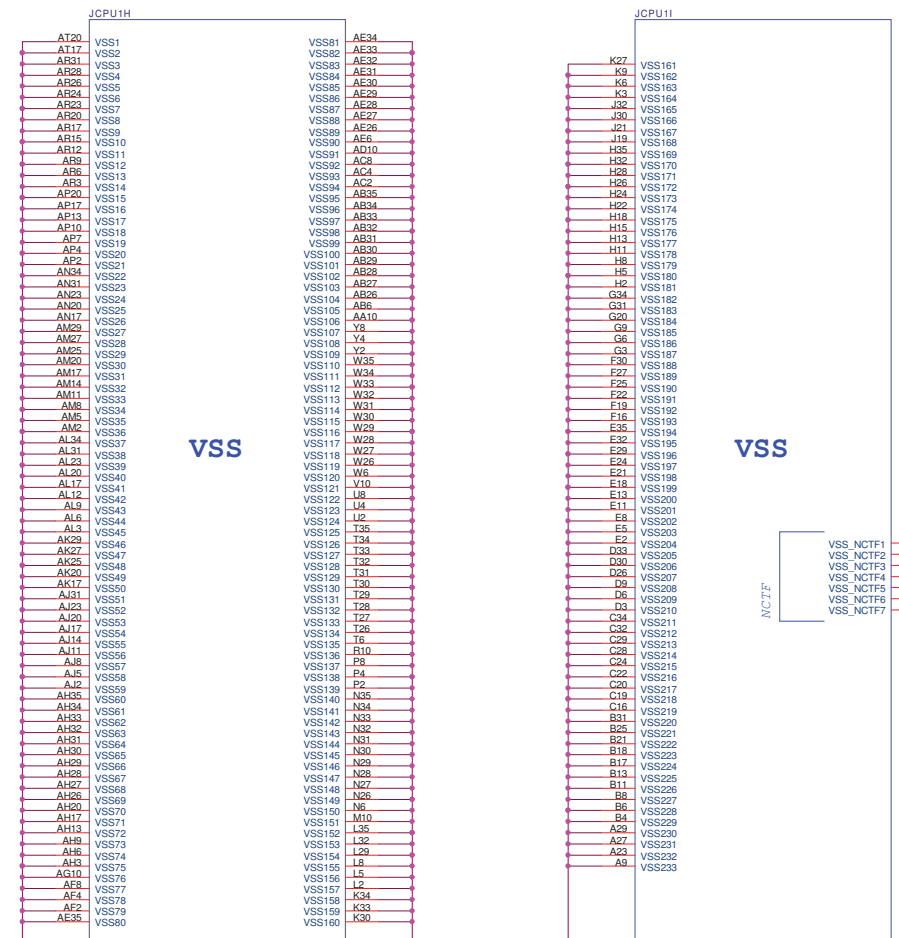
CFG Straps for PROCESSOR



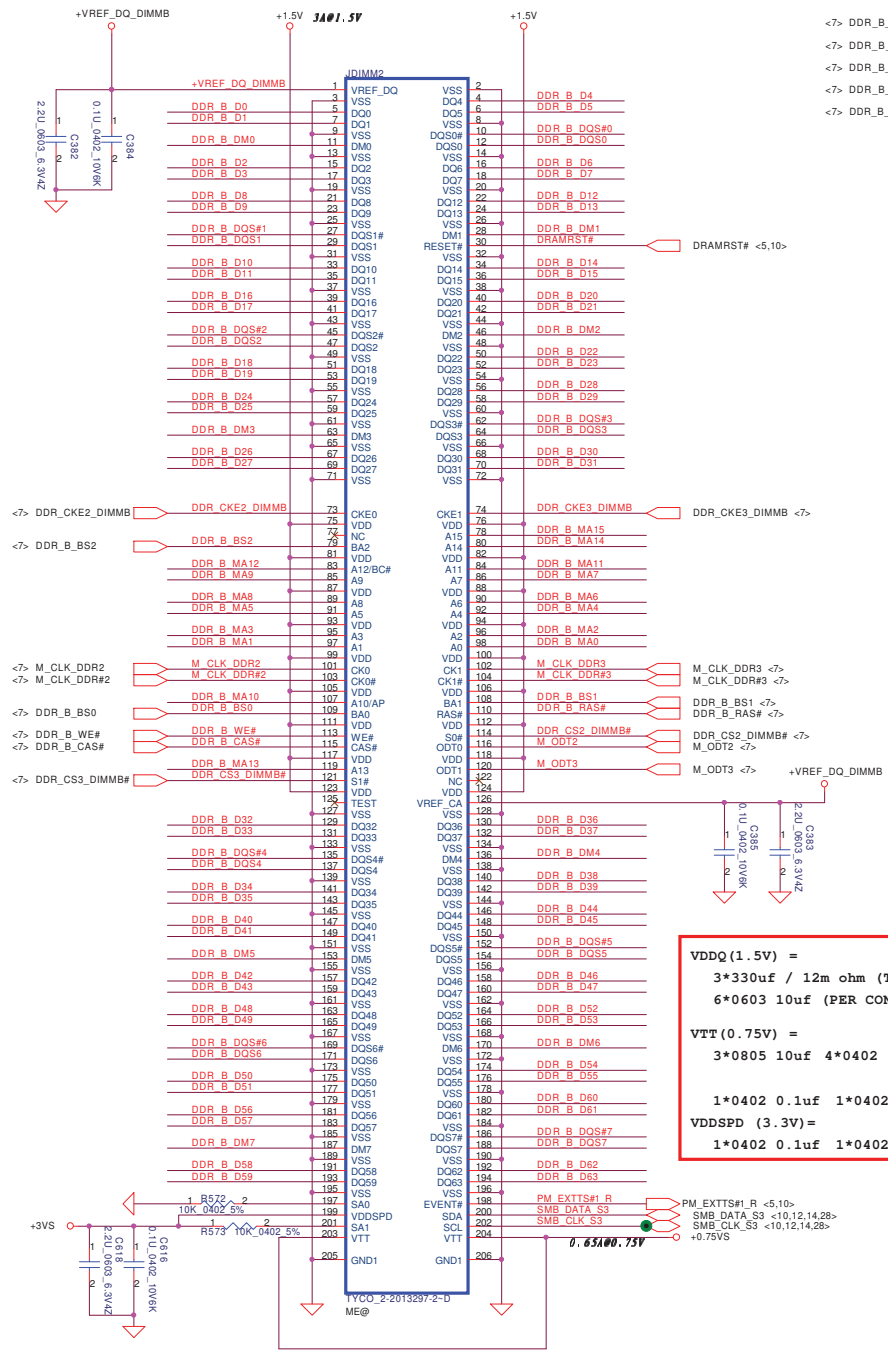
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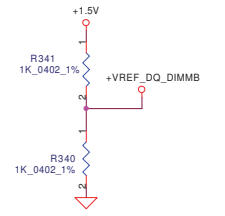
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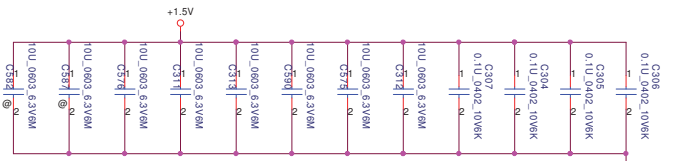


- <7> DDR_B_DQS#0[0..7]
- <7> DDR_B_D0[0..63]
- <7> DDR_B_DM[0..7]
- <7> DDR_B_DQS#0[0..7]
- <7> DDR_B_MA[0..15]



For Arranale only +VREF_DQ_DIMMB supply from an external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM

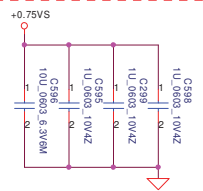


VDDQ (1.5V) =
 $3 \times 330\mu\text{f} / 12\text{m ohm}$ (TOTAL FOR 2 SO-DIMMs)
 6×603 10uF (PER CONNECTOR)

VTT (0.75V) =
 3×0805 10uF 4×0402 1uF

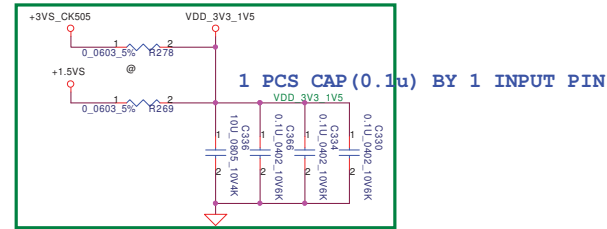
VDDSPD (3.3V) =
 1×0402 0.1uF 1×0402 2.2uF
 1×0402 0.1uF 1×0402 2.2uF

Layout Note:
Place near DIMM



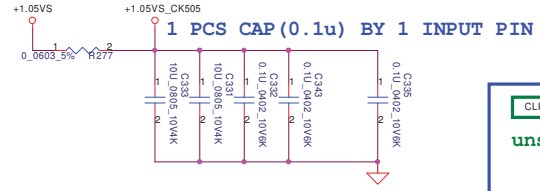
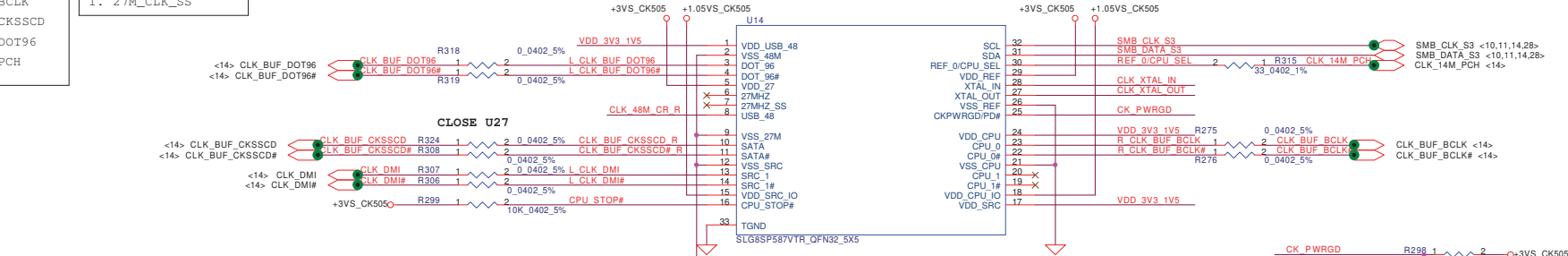
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Reserve for Low Power CLK GEN.
RTM890N-632
SLG8LV597VTR



- CLK GEN TO PCH**
1. CLK_DMI
 2. CLK_BUF_BCLK
 3. CLK_BUF_CKSSCD
 4. CLK_BUF_DOT96
 5. CLK_14M_PCH

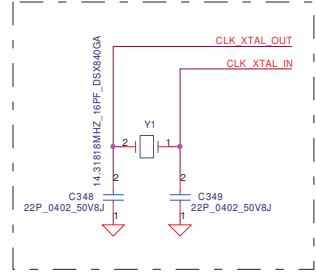
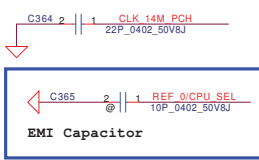
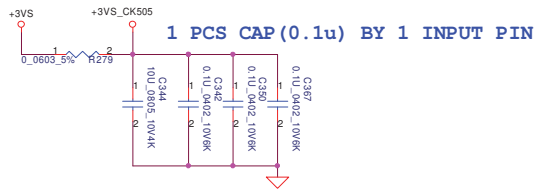
- CLK GEN TO VGA**
1. 27M_CLK
 1. 27M_CLK_SS



RTM890N-631-GRT QFN 32P CLK GEN (SA00003HQ00)
ICS9LV53199AKLFT MLF 32P CLK GEN (SA00003HR00)

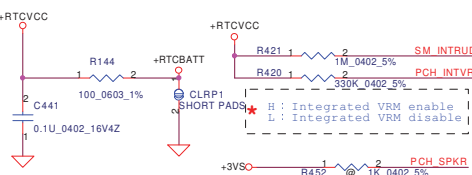
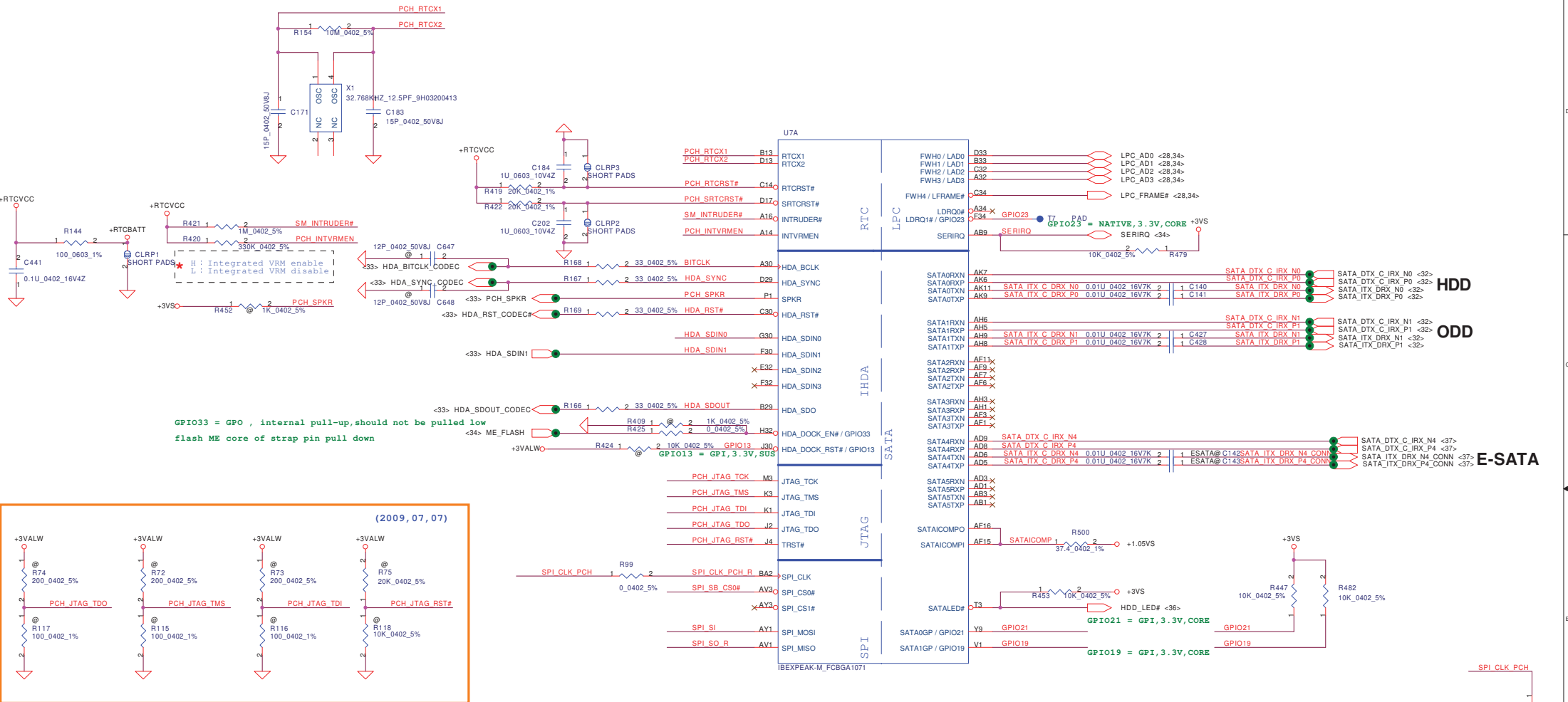
CLK_48M_CR R332 1 2 0.0402_5% R323 2 1 0.0402_5%

unstuff 09.09.08
PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199

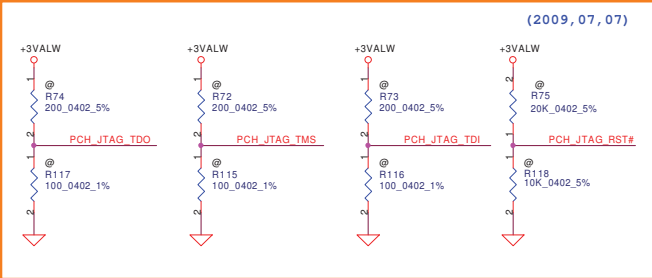


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	CLOCK GENERATOR
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				Document Number
				LA-5752P
				Rev
				0.3
Date: Thursday, October 29, 2009				Sheet 12 of 51

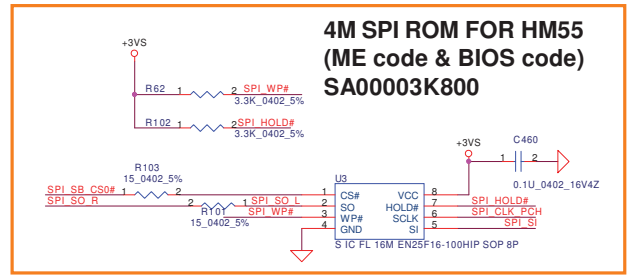


GPIO33 = GPO , internal pull-up, should not be pulled low
flash ME core of strap pin pull down



PCH_JTAG_TCK R114 1 2 51 0.402 5% (2009, 05, 04)
FOR INTEL DPDG REV1.6 (MAY 2009)

PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	★ MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
	R595	20Kohm	20Kohm	No Install
PCH_JTAG_RST#	R594	10Kohm	10Kohm	No Install

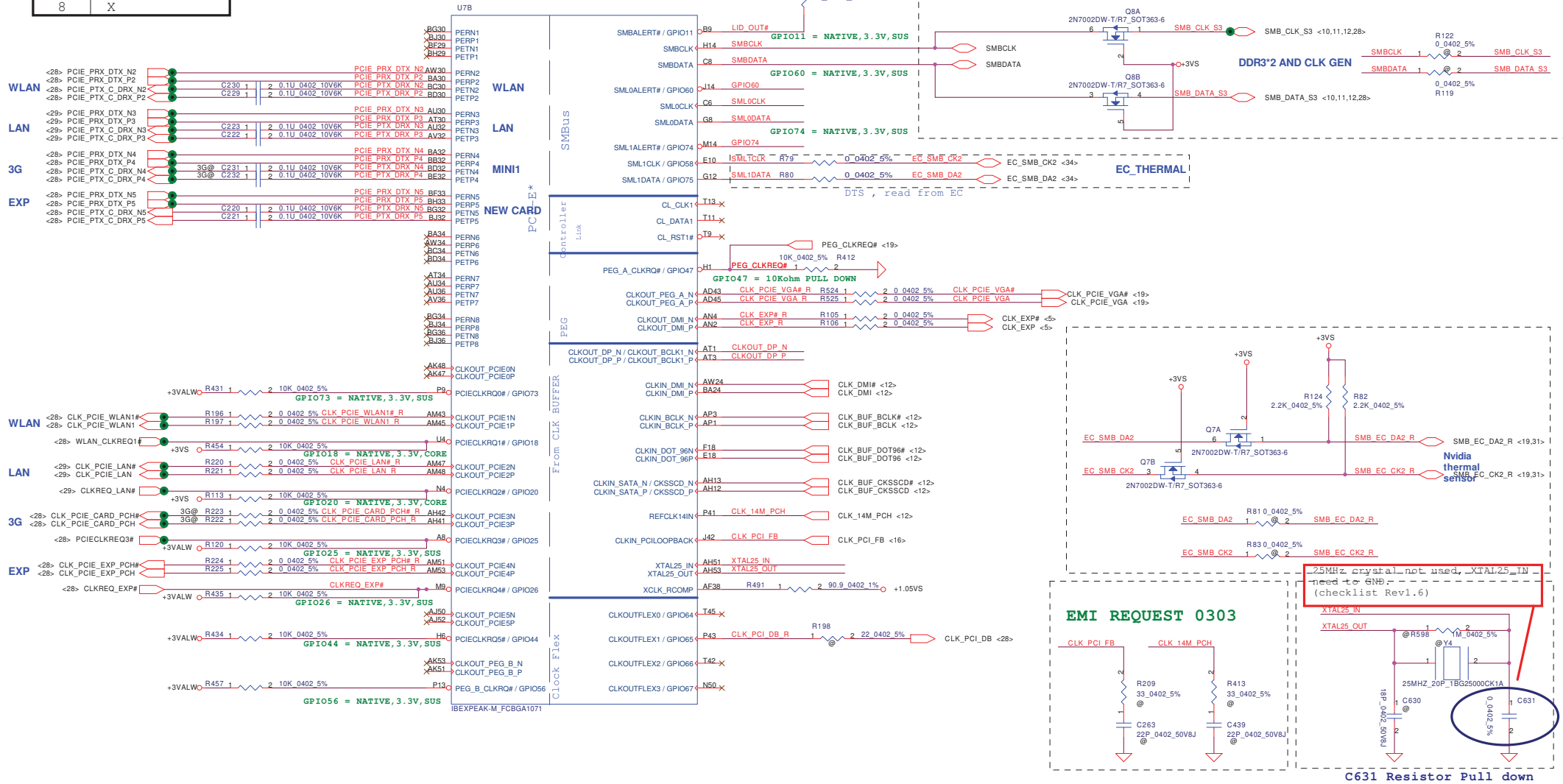


Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(1/6)-HDA/JTAG/SATA
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Date: Thursday, October 29, 2009				Sheet 13 of 51

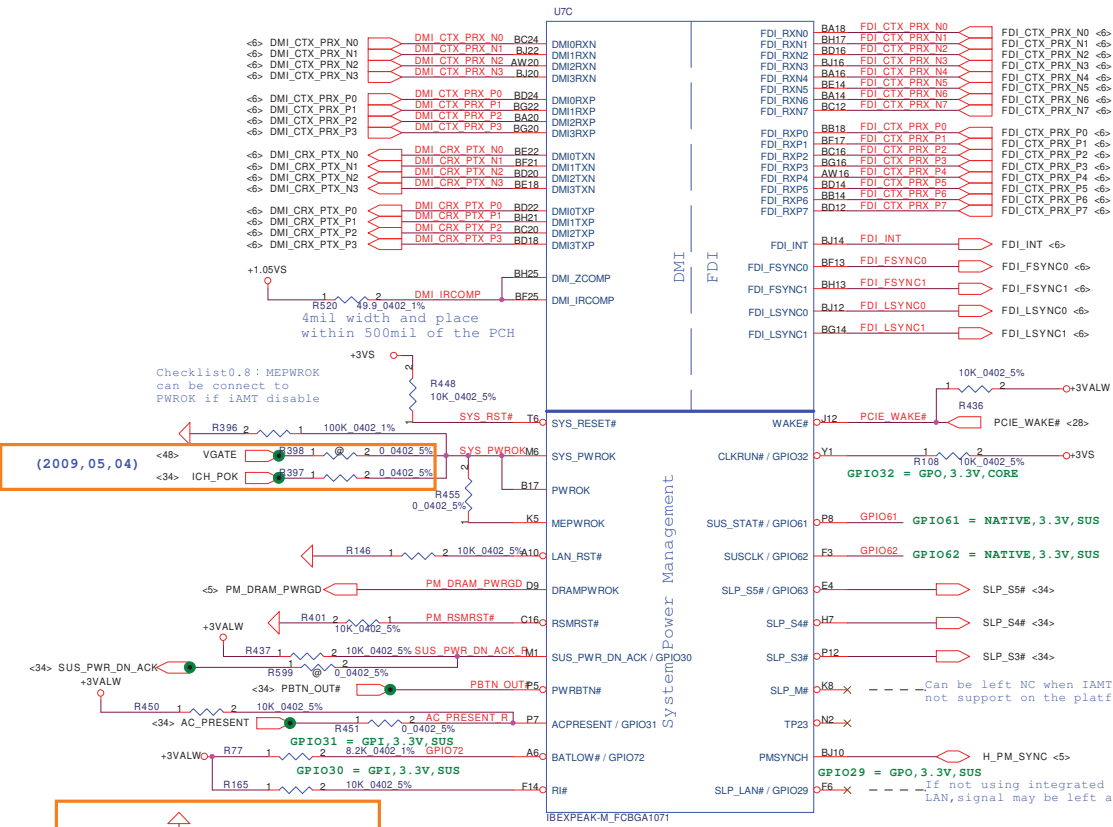
Compal Electronics, Inc.
IBEX-M(1/6)-HDA/JTAG/SATA
LA-5752P
Date: Thursday, October 29, 2009 Sheet 13 of 51

PCI-E PORT LIST

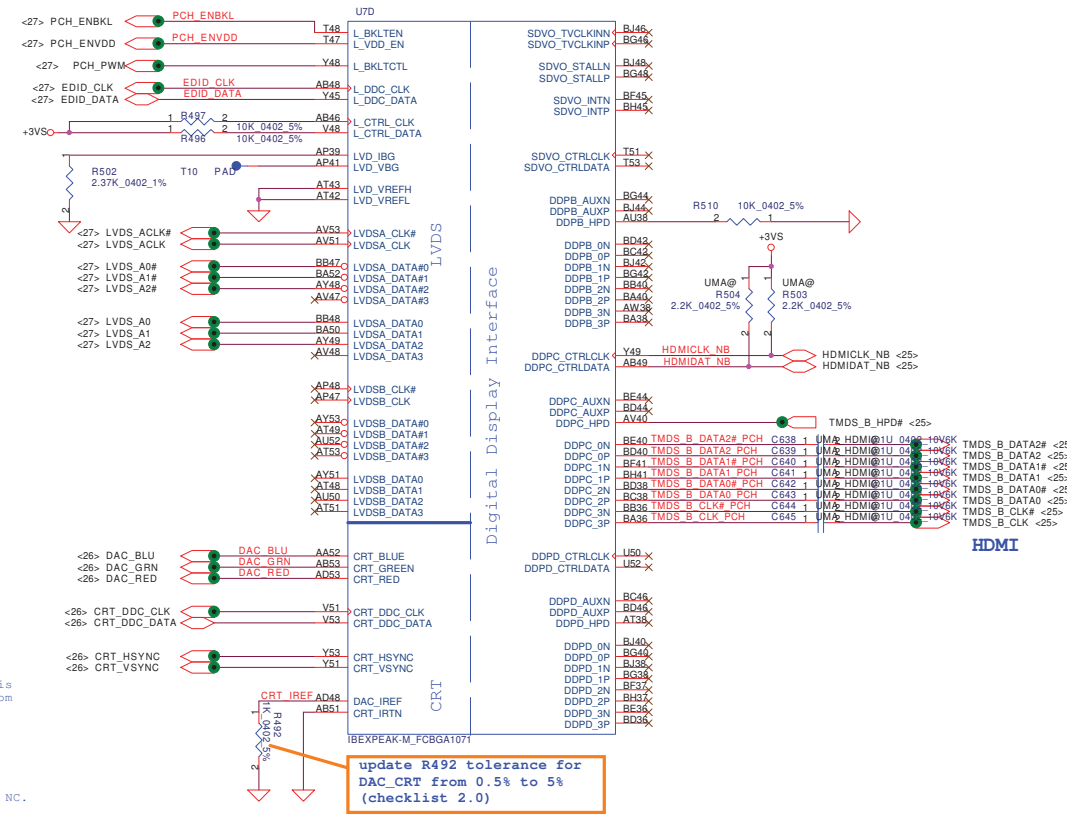
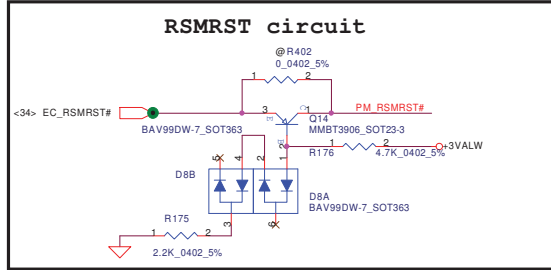
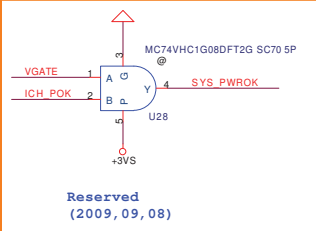
PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X



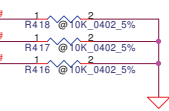
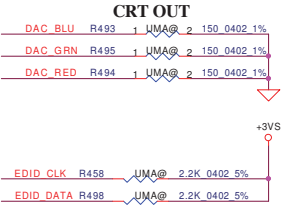
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(2/6)-PCI-E/SMBUS/CLK	
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Date	Thursday, October 29, 2009	Sheet	14	of 51	



(2009, 05, 04)



update R492 tolerance for DAC_CRT from 0.5% to 5% (checklist 2.0)



Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(3/6)-DMI/GPIO/LVDS		Rev
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U7I	
AY7	VSS[159]
B11	VSS[160]
B15	VSS[162]
B19	VSS[163]
B23	VSS[163]
B31	VSS[164]
B33	VSS[165]
B33	VSS[166]
B43	VSS[167]
B47	VSS[168]
B7	VSS[169]
BG12	VSS[170]
BB12	VSS[171]
BB20	VSS[173]
BB24	VSS[174]
BB30	VSS[175]
BB34	VSS[176]
BB38	VSS[177]
BB42	VSS[178]
BB49	VSS[179]
BB5	VSS[180]
BC10	VSS[181]
BC14	VSS[182]
BC18	VSS[183]
BC2	VSS[184]
BC22	VSS[185]
BC32	VSS[186]
BC36	VSS[187]
BC40	VSS[188]
BC44	VSS[189]
BC52	VSS[190]
BH8	VSS[191]
BD48	VSS[192]
BD49	VSS[193]
BD5	VSS[194]
BE12	VSS[195]
BE16	VSS[196]
BE20	VSS[197]
BE24	VSS[198]
BE30	VSS[199]
BE34	VSS[200]
BE38	VSS[201]
BE42	VSS[202]
BE46	VSS[203]
BE48	VSS[204]
BE50	VSS[205]
BE6	VSS[206]
BE8	VSS[207]
BE9	VSS[208]
BF3	VSS[209]
BF49	VSS[210]
BF51	VSS[211]
BG18	VSS[212]
BG24	VSS[213]
BG4	VSS[214]
BG50	VSS[215]
BH11	VSS[216]
BH15	VSS[217]
BH19	VSS[218]
BH23	VSS[219]
BH31	VSS[220]
BH35	VSS[221]
BH39	VSS[222]
BH43	VSS[223]
BH47	VSS[224]
BH7	VSS[225]
C12	VSS[226]
C50	VSS[227]
D51	VSS[228]
E12	VSS[229]
E16	VSS[230]
E20	VSS[231]
E24	VSS[232]
E30	VSS[233]
E34	VSS[234]
E38	VSS[235]
E42	VSS[236]
E46	VSS[237]
E48	VSS[238]
E6	VSS[239]
E8	VSS[240]
F6	VSS[241]
G10	VSS[242]
G14	VSS[243]
G18	VSS[244]
G2	VSS[245]
G22	VSS[246]
G32	VSS[247]
G36	VSS[248]
G40	VSS[249]
G44	VSS[250]
G62	VSS[251]
AF39	VSS[252]
H16	VSS[253]
H20	VSS[254]
H30	VSS[255]
H34	VSS[256]
H38	VSS[257]
H42	VSS[258]

IBEXPEAK-M_FCBGA1071

U7H	
AB16	VSS[0]
AA19	VSS[1]
AA20	VSS[2]
AA19	VSS[3]
AA24	VSS[4]
AA28	VSS[5]
AA30	VSS[6]
AA31	VSS[7]
AA32	VSS[8]
AA31	VSS[9]
AA32	VSS[10]
AB11	VSS[11]
AB15	VSS[12]
AB22	VSS[13]
AB30	VSS[14]
AB31	VSS[15]
AB32	VSS[16]
AB38	VSS[17]
AB43	VSS[18]
AB47	VSS[19]
AB5	VSS[20]
AB8	VSS[21]
AC2	VSS[22]
AC32	VSS[23]
AD11	VSS[24]
AD12	VSS[25]
AD16	VSS[26]
AD23	VSS[27]
AD30	VSS[28]
AD31	VSS[29]
AD32	VSS[30]
AD34	VSS[31]
AU22	VSS[111]
AD42	VSS[112]
AD43	VSS[113]
AD7	VSS[114]
AE2	VSS[36]
AE4	VSS[37]
AE5	VSS[38]
AF12	VSS[39]
AF18	VSS[40]
AF19	VSS[41]
AF4	VSS[42]
AF38	VSS[43]
AF39	VSS[44]
AF45	VSS[45]
AF46	VSS[46]
AF49	VSS[47]
AF5	VSS[48]
AF8	VSS[50]
AG2	VSS[51]
AG52	VSS[52]
AH11	VSS[53]
AH15	VSS[54]
AH16	VSS[55]
AH24	VSS[56]
AH32	VSS[57]
AV18	VSS[58]
AH43	VSS[59]
AH47	VSS[60]
AH7	VSS[61]
AJ19	VSS[62]
AJ2	VSS[63]
AJ20	VSS[64]
AJ22	VSS[65]
AJ23	VSS[66]
AJ26	VSS[67]
AJ28	VSS[68]
AJ32	VSS[69]
AJ34	VSS[70]
AT5	VSS[71]
AJ4	VSS[72]
AK12	VSS[73]
AM1	VSS[74]
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AK26	VSS[76]
AK22	VSS[77]
AK23	VSS[78]
AK28	VSS[79]

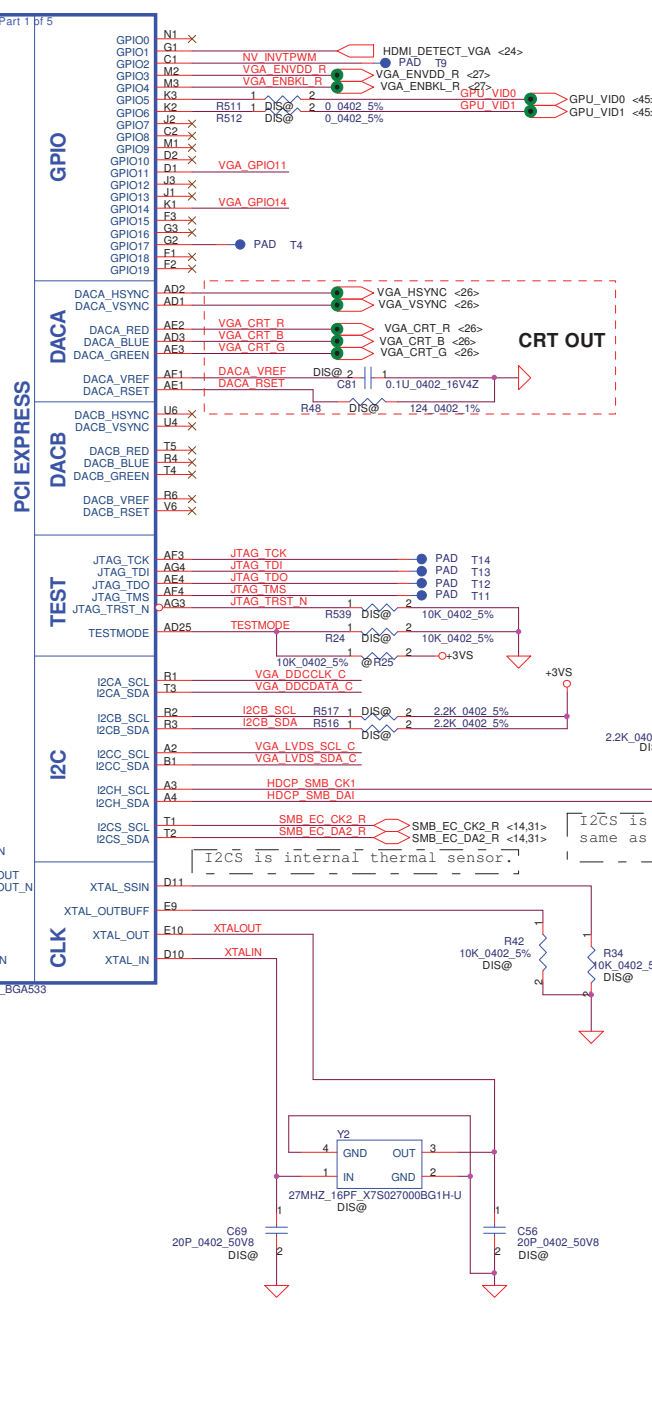
IBEXPEAK-M_FCBGA1071

VSS[80]	AK30
VSS[81]	AK31
VSS[82]	AK32
VSS[83]	AK34
VSS[84]	AK35
VSS[85]	AK38
VSS[86]	AK43
VSS[87]	AK46
VSS[88]	AK49
VSS[89]	AK5
VSS[90]	AK8
VSS[91]	AL2
VSS[92]	AL32
VSS[93]	AM11
VSS[94]	BB44
VSS[95]	AD24
VSS[96]	AM20
VSS[97]	AM22
VSS[98]	AM24
VSS[99]	AM25
VSS[100]	AM28
VSS[101]	BA42
VSS[102]	AM30
VSS[103]	AM31
VSS[104]	AM32
VSS[105]	AM34
VSS[106]	AM35
VSS[107]	AM38
VSS[108]	AM39
VSS[109]	AM42
VSS[110]	AM46
VSS[111]	AM66
VSS[112]	AV22
VSS[113]	AM49
VSS[114]	AM7
VSS[115]	AE50
VSS[116]	BE10
VSS[117]	AN32
VSS[118]	AN50
VSS[119]	AN52
VSS[120]	AP12
VSS[121]	AP42
VSS[122]	AP46
VSS[123]	AP49
VSS[124]	AP5
VSS[125]	AP8
VSS[126]	AR2
VSS[127]	AR52
VSS[128]	AT11
VSS[129]	BA12
VSS[130]	AH48
VSS[131]	AT32
VSS[132]	AT36
VSS[133]	AT41
VSS[134]	AT47
VSS[135]	AT7
VSS[136]	AV12
VSS[137]	AV16
VSS[138]	AV20
VSS[139]	AV24
VSS[140]	AV30
VSS[141]	AV34
VSS[142]	AV38
VSS[143]	AV42
VSS[144]	AV46
VSS[145]	AV49
VSS[146]	AV5
VSS[147]	AV8
VSS[148]	AW14
VSS[149]	AW18
VSS[150]	AW2
VSS[151]	BF9
VSS[152]	AW32
VSS[153]	AW36
VSS[154]	AW40
VSS[155]	AW52
VSS[156]	AT11
VSS[157]	AV43
VSS[158]	AY47

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Customer	Rev 0.3			

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<6> PCIE_CRX_GTX_N0..15]	PCIE_CRX_GTX_N0..15]	PCIE_CTX_GRX_N1	AE12	PEX_RX1
<6> PCIE_CRX_GTX_P0..15]	PCIE_CRX_GTX_P0..15]	PCIE_CTX_GRX_P2	AE12	PEX_RX1_N
		PCIE_CTX_GRX_N2	AE13	PEX_RX2
		PCIE_CTX_GRX_P3	AE13	PEX_RX2_N
		PCIE_CTX_GRX_N3	AE13	PEX_RX3
		PCIE_CTX_GRX_P4	AG15	PEX_RX3_N
		PCIE_CTX_GRX_N4	AG16	PEX_RX4
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		PCIE_CTX_GRX_N8	AE19	PEX_RX8_N
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		PCIE_CTX_GRX_N9	AE21	PEX_RX9_N
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		PCIE_CTX_GRX_P14	AE25	PEX_RX14
		PCIE_CTX_GRX_N14	AG26	PEX_RX14_N
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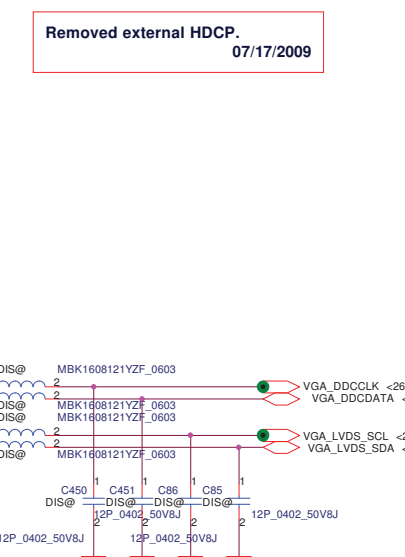
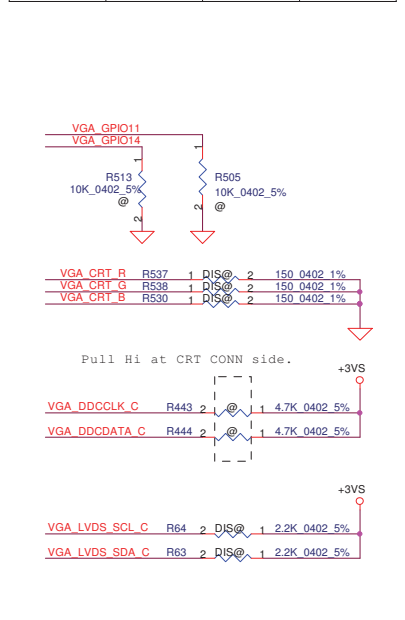
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PCIE_CRX_GTX_N0	C119	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N0	AD11	PEX_TX0_N
PCIE_CRX_GTX_P1	C118	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P1	AD12	PEX_TX1
PCIE_CRX_GTX_N1	C117	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N1	AC12	PEX_TX1_N
PCIE_CRX_GTX_P2	C80	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P2	AB11	PEX_TX2
PCIE_CRX_GTX_N2	C79	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N2	AB12	PEX_TX2_N
PCIE_CRX_GTX_P3	C78	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P3	AD13	PEX_TX3
PCIE_CRX_GTX_N3	C77	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N3	AD14	PEX_TX3_N
PCIE_CRX_GTX_P4	C116	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P4	AD15	PEX_TX4
PCIE_CRX_GTX_N4	C115	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N4	AC15	PEX_TX4_N
PCIE_CRX_GTX_P5	C114	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P5	AB14	PEX_TX5
PCIE_CRX_GTX_N5	C113	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N5	AB15	PEX_TX5_N
PCIE_CRX_GTX_P6	C112	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P6	AC16	PEX_TX6
PCIE_CRX_GTX_N6	C111	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N6	AD16	PEX_TX6_N
PCIE_CRX_GTX_P7	C109	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P7	AD17	PEX_TX7
PCIE_CRX_GTX_N7	C110	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N7	AD18	PEX_TX7_N
PCIE_CRX_GTX_P8	C108	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P8	AD18	PEX_TX7
PCIE_CRX_GTX_N8	C107	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N8	AB18	PEX_TX8
PCIE_CRX_GTX_P9	C105	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P9	AB19	PEX_TX9
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PCIE_CRX_GTX_N10	C103	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N10	AD20	PEX_TX10_N
PCIE_CRX_GTX_P11	C102	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P11	AD21	PEX_TX11
PCIE_CRX_GTX_N11	C101	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N11	AC21	PEX_TX11_N
PCIE_CRX_GTX_P12	C100	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P12	AB21	PEX_TX12
PCIE_CRX_GTX_N12	C99	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N12	AB22	PEX_TX12_N
PCIE_CRX_GTX_P13	C98	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P13	AC22	PEX_TX13
PCIE_CRX_GTX_N13	C97	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N13	AD22	PEX_TX13_N
PCIE_CRX_GTX_P14	C96	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P14	AD23	PEX_TX14
PCIE_CRX_GTX_N14	C95	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N14	AD24	PEX_TX14_N
PCIE_CRX_GTX_P15	C94	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_P15	AE25	PEX_TX15
PCIE_CRX_GTX_N15	C93	DIS@	1	2	0.1U	0.402	16V7K	PCIE_CRX_C_GTX_N15	AE26	PEX_TX15_N









Device ID	0x0A74
Device ID	0x0A7D

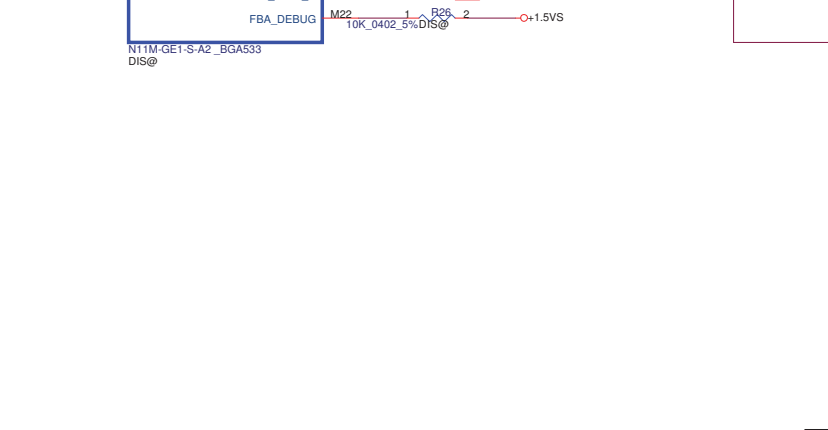
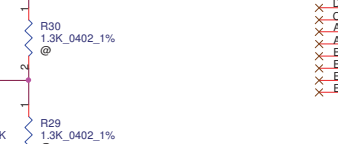
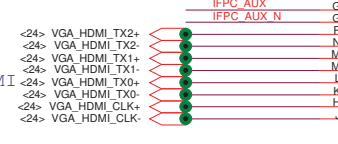
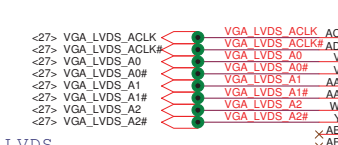
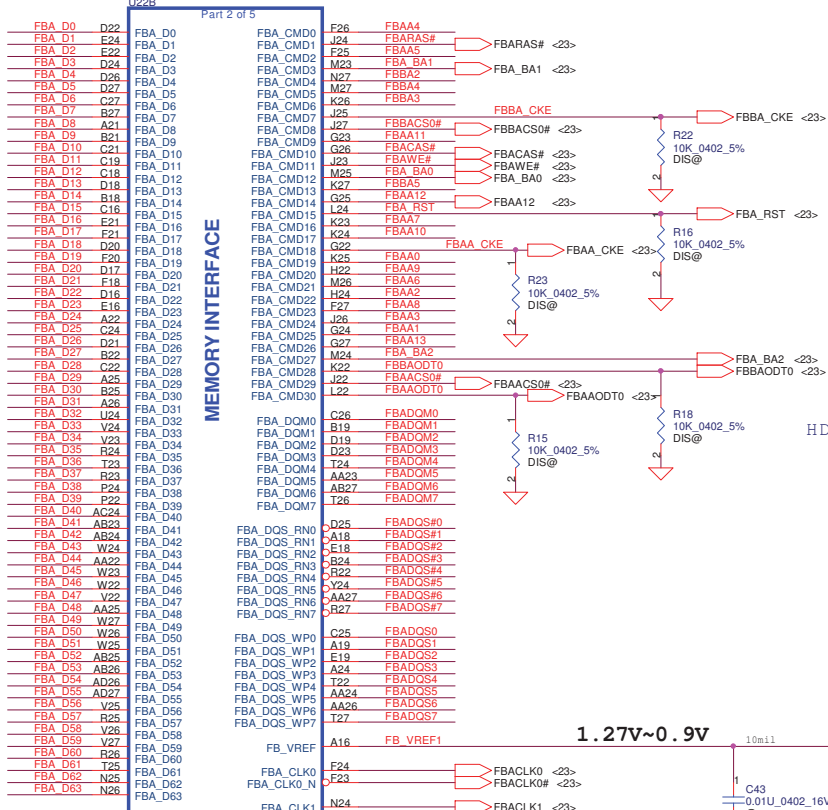
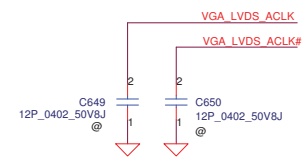
GPIO5 GPU_VID0	GPIO6 GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	1.0V	P0

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.9V	P0



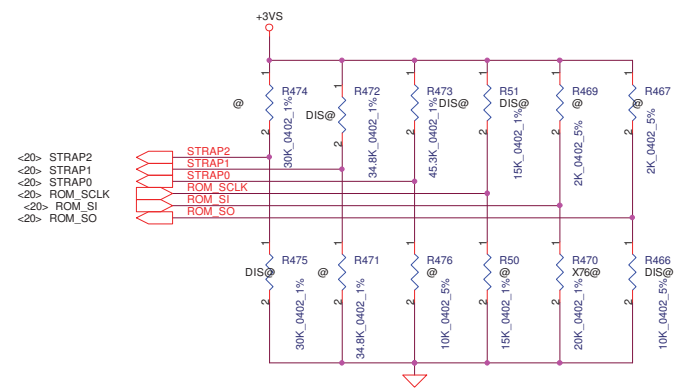
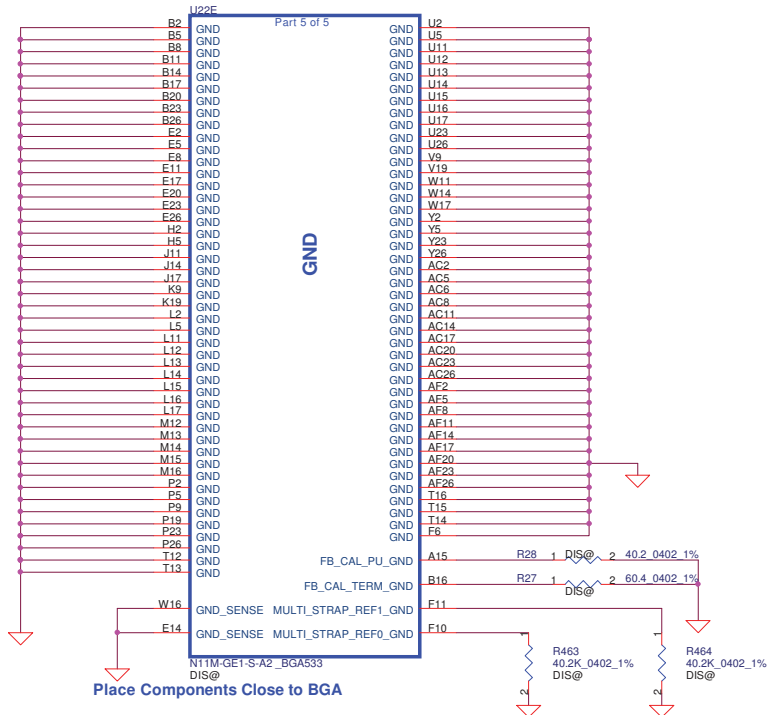
Removed external HDCP. 07/17/2009

- <23> FBAA[0..13]  FBAA[0..13]
- <23> FBBA[2..5]  FBBA[2..5]
- <23> FBADQM[0..7]  FBADQM[0..7]
- <23> FBADQS[0..7]  FBADQS[0..7]
- <23> FBADQS#[0..7]  FBADQS#[0..7]
- <23> FBAD[0..63]  FBA_D10..63]



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Size	Document Number	Rev		
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A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



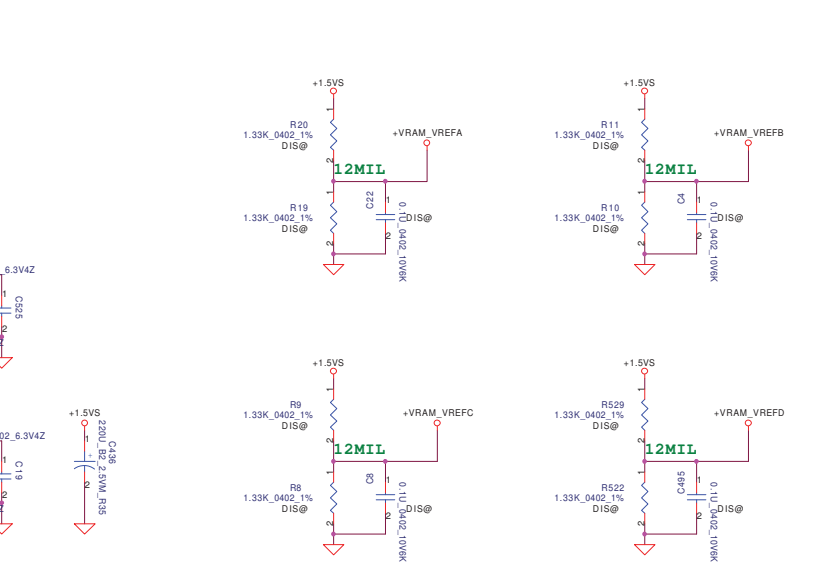
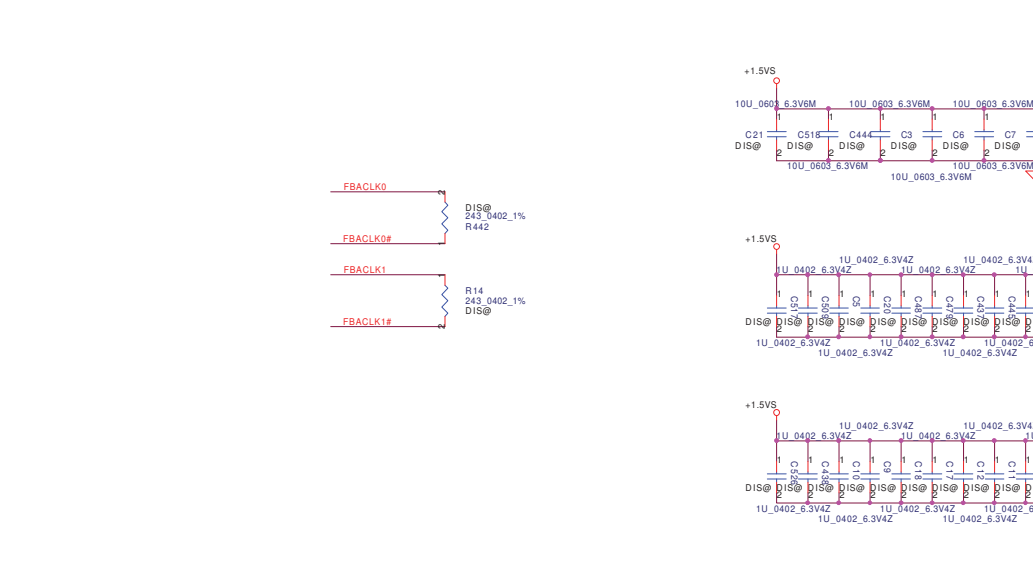
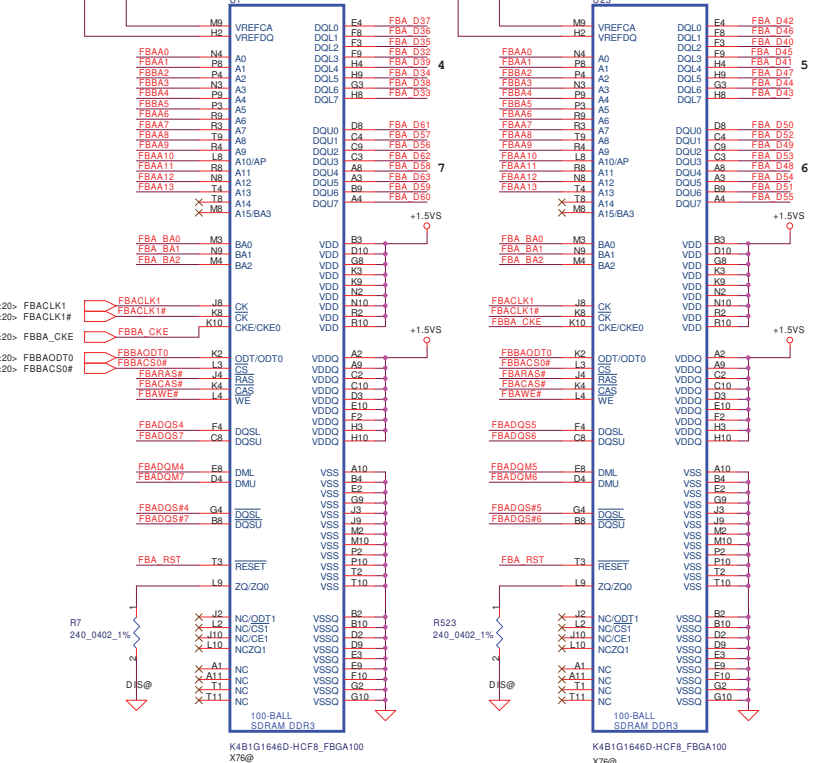
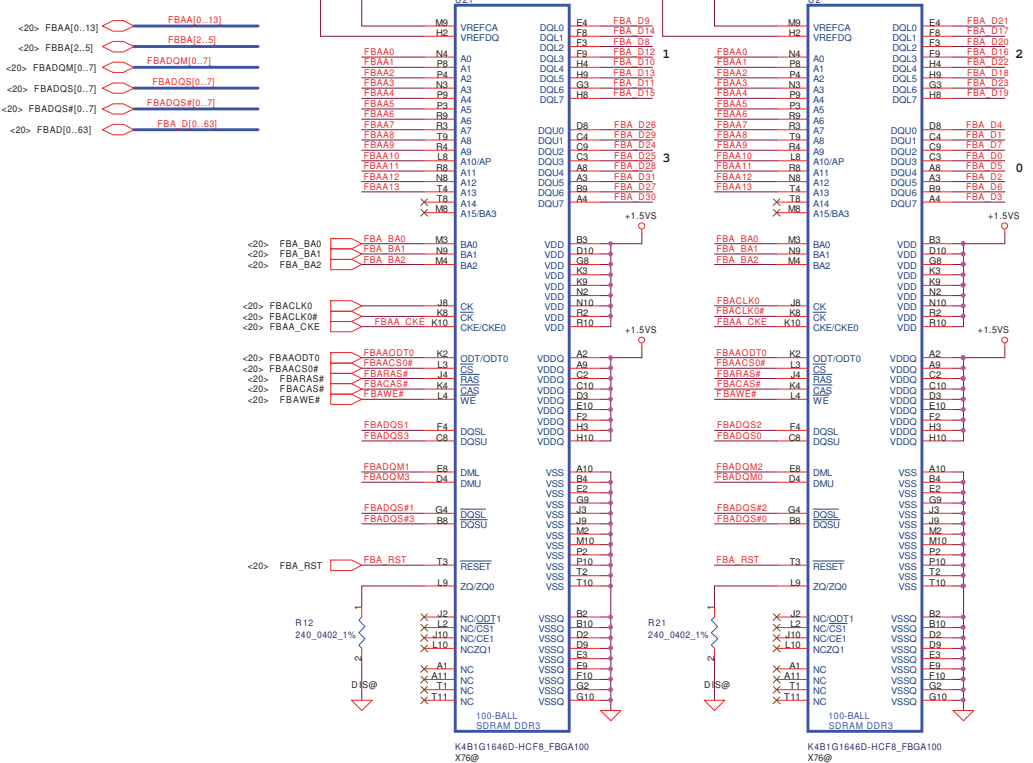
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
 (PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12					
	64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
Hynix 800MHz	H5TQ1G63BFR-12C						
	64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
				X76			

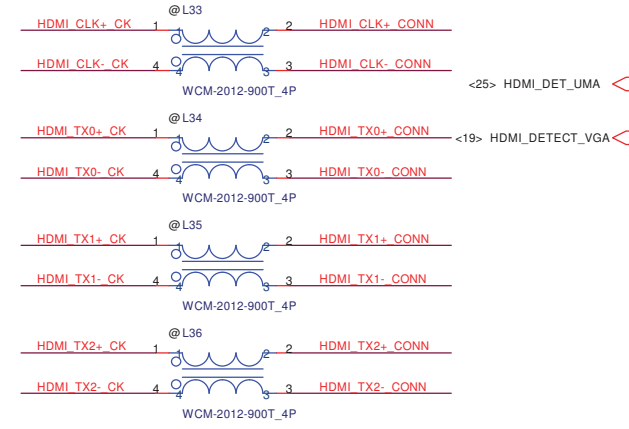
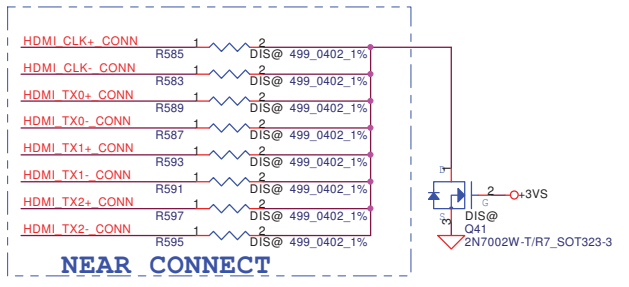
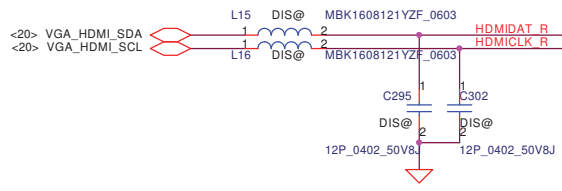
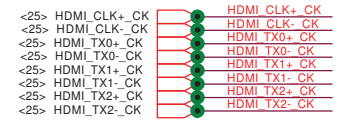
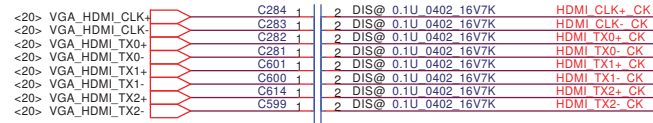
N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resistor for driver calibration DG-04642-001-V01(May 22, 2009)

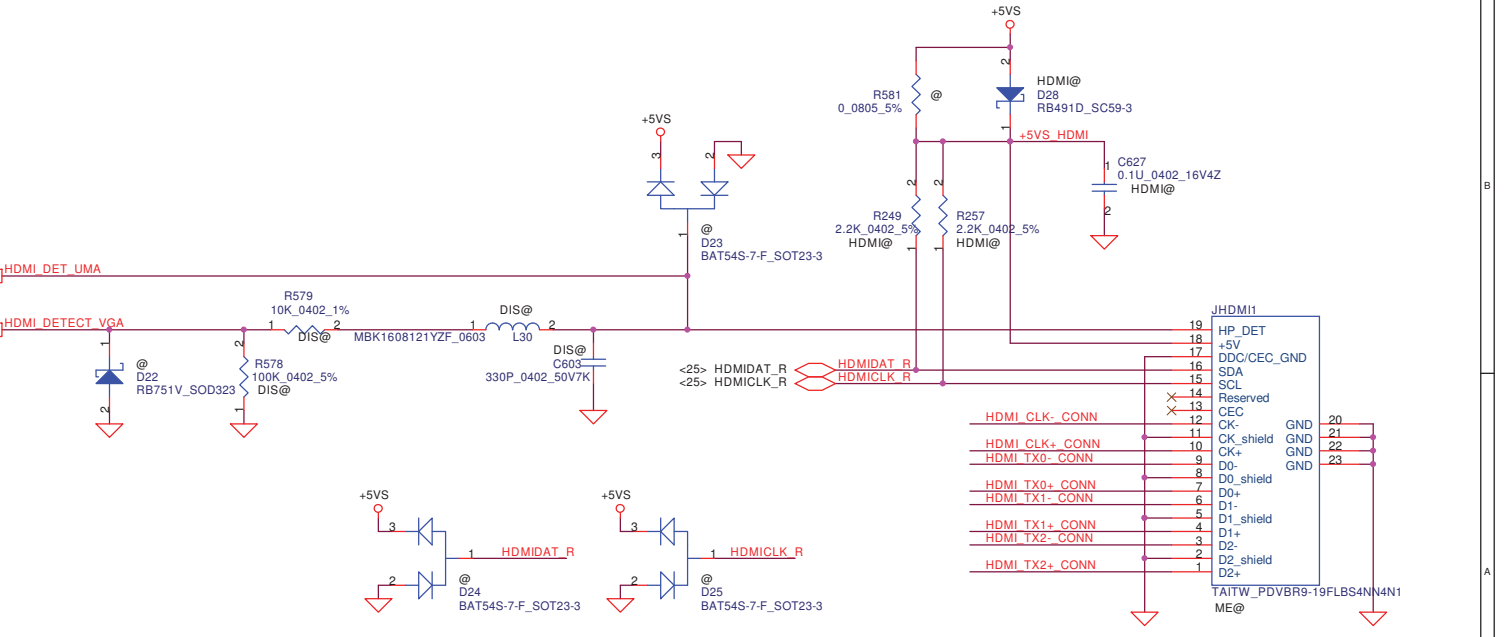
N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001



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HDMI_CLK+_CK	R584	HDMI@	2	0.0402	5%	HDMI_CLK+_CONN
HDMI_CLK-_CK	R582	HDMI@	2	0.0402	5%	HDMI_CLK-_CONN
HDMI_TX0+_CK	R588	HDMI@	2	0.0402	5%	HDMI_TX0+_CONN
HDMI_TX0-_CK	R586	HDMI@	2	0.0402	5%	HDMI_TX0-_CONN
HDMI_TX1+_CK	R592	HDMI@	2	0.0402	5%	HDMI_TX1+_CONN
HDMI_TX1-_CK	R590	HDMI@	2	0.0402	5%	HDMI_TX1-_CONN
HDMI_TX2+_CK	R596	HDMI@	2	0.0402	5%	HDMI_TX2+_CONN
HDMI_TX2-_CK	R594	HDMI@	2	0.0402	5%	HDMI_TX2-_CONN



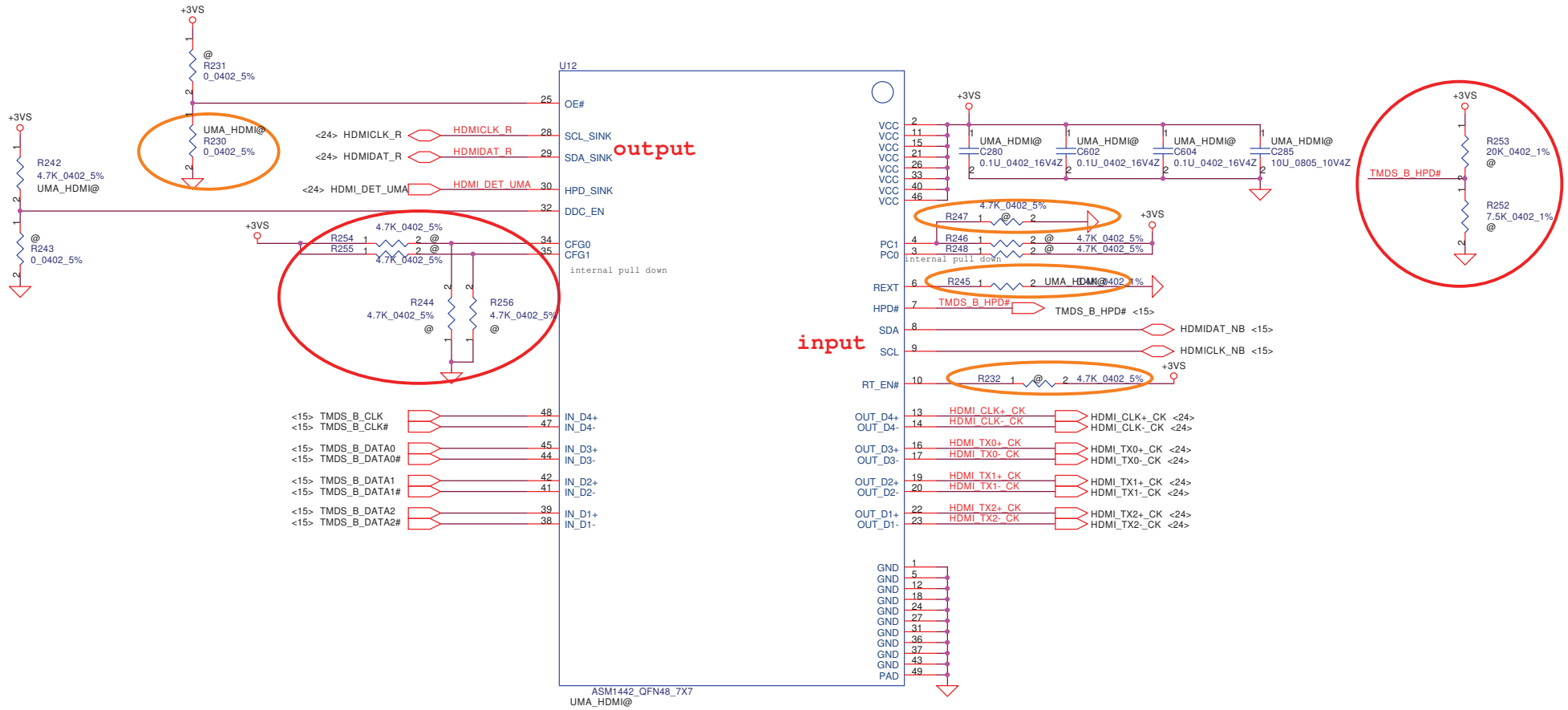
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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	
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Size	Document Number	Date: Thursday, October 29, 2009		Sheet	24 of 51
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P/N:SA00003GT00 (ASM1442)

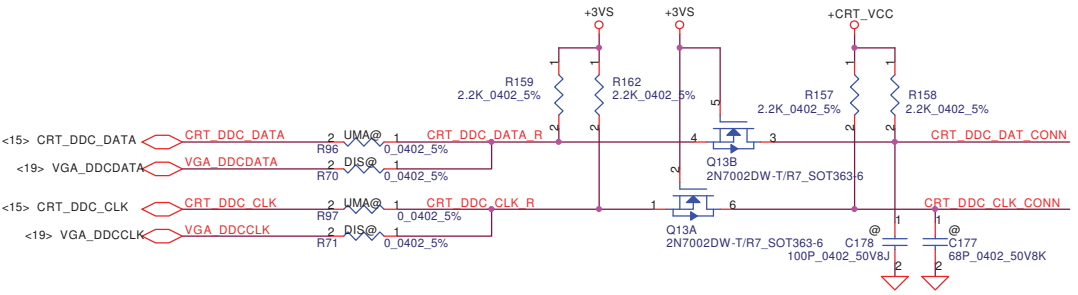
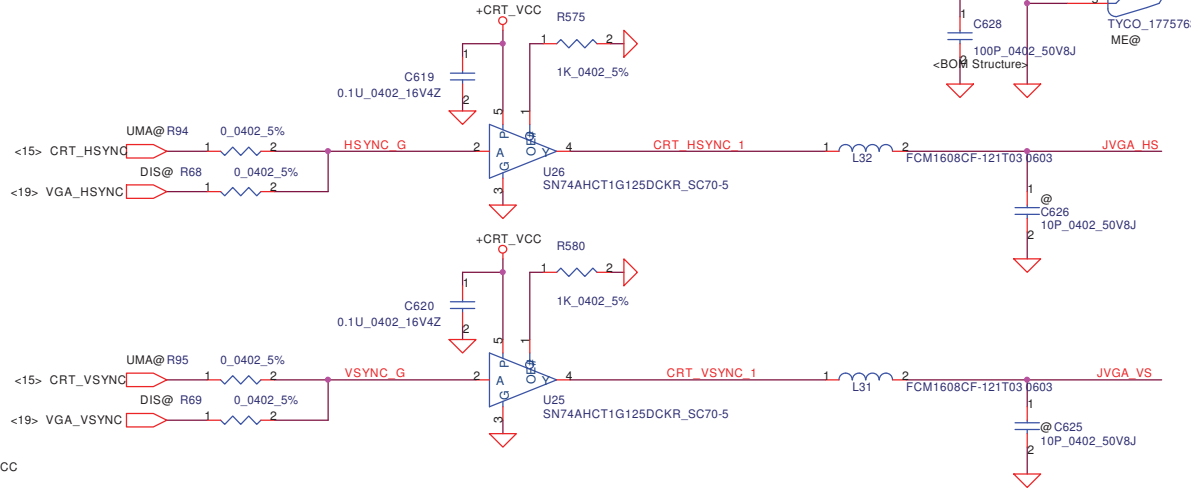
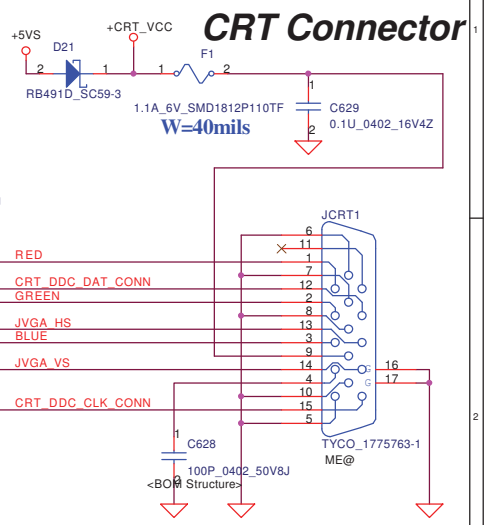
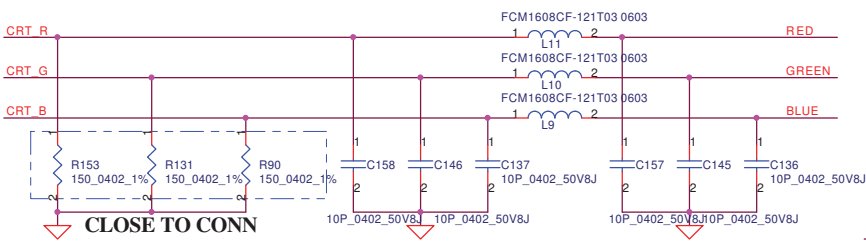
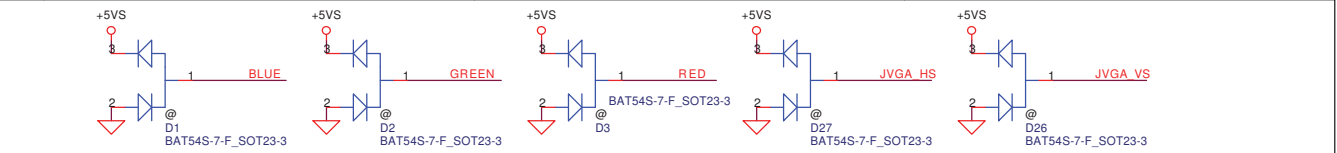
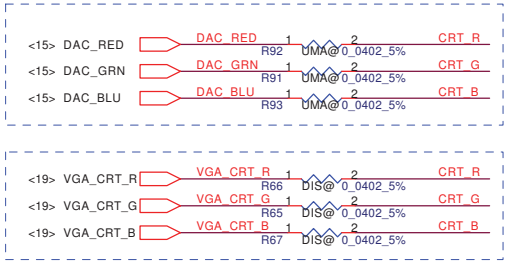
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P/N:SA00001U900 (CH7318A)

FOR asmedia R428 STUFF
RESERVE THE R668 PULL UP TO 3VS
RESERVE THE R670 PULL DOWN TO GND
CHANGE R483 FROM 499 TO 3.4K OHM

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm

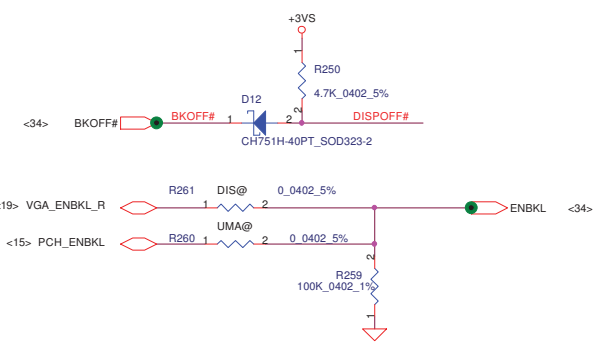
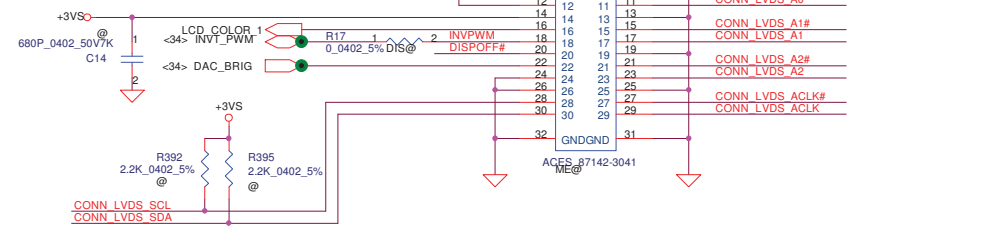
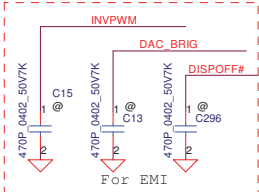
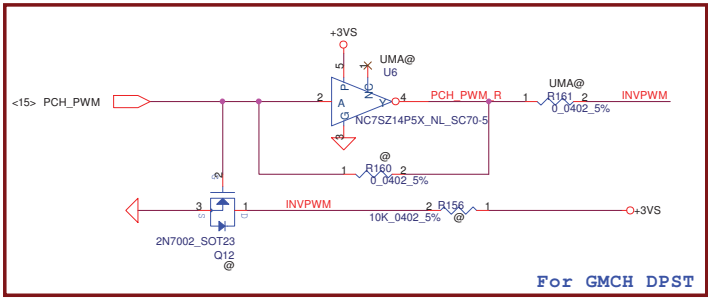
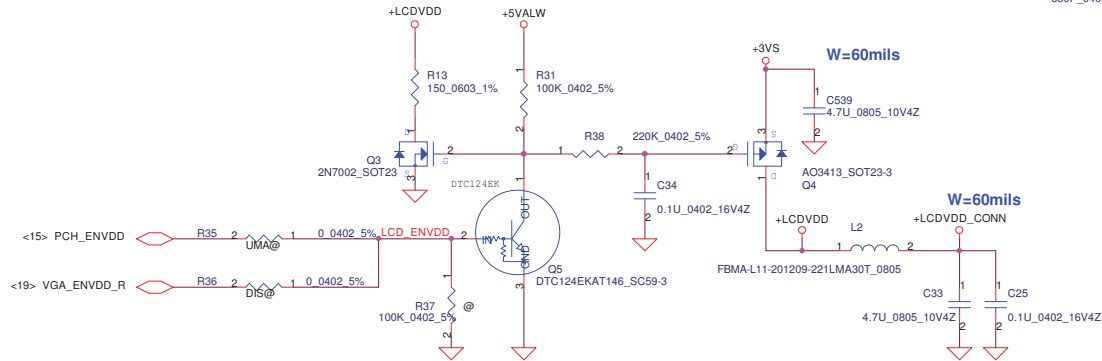


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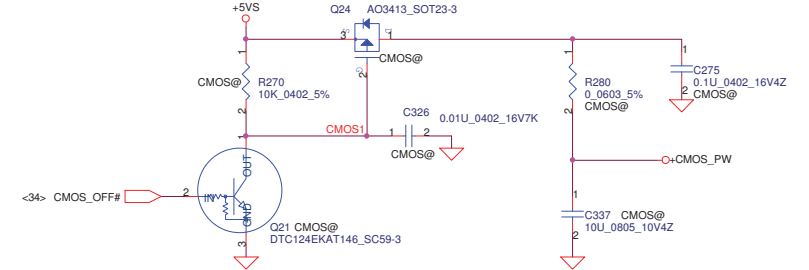
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Size	Document Number	Rev		0.3	
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		Sheet		26 of 51	

LCD POWER CIRCUIT



- <19> VGA_LVDS_SCL UMA@ 0.0402 5% 2 DIS@ 1 R390 CONN LVDS_SCL
- <19> VGA_LVDS_SDA DIS@ 0.0402 5% 2 DIS@ 1 R391 CONN LVDS_SDA
- <20> VGA_LVDS_A0# UMA@ 0.0402 5% 2 DIS@ 1 R86 CONN LVDS_A0#
- <20> VGA_LVDS_A0# DIS@ 0.0402 5% 2 DIS@ 1 R85 CONN LVDS_A0#
- <20> VGA_LVDS_A1# UMA@ 0.0402 5% 2 DIS@ 1 R150 CONN LVDS_A1#
- <20> VGA_LVDS_A1# DIS@ 0.0402 5% 2 DIS@ 1 R128 CONN LVDS_A1#
- <20> VGA_LVDS_A2# UMA@ 0.0402 5% 2 DIS@ 1 R126 CONN LVDS_A2#
- <20> VGA_LVDS_A2# DIS@ 0.0402 5% 2 DIS@ 1 R127 CONN LVDS_A2#
- <20> VGA_LVDS_ACLK# UMA@ 0.0402 5% 2 DIS@ 1 R84 CONN LVDS_ACLK#
- <20> VGA_LVDS_ACLK# DIS@ 0.0402 5% 2 DIS@ 1 R125 CONN LVDS_ACLK#
- <15> EDID_CLK UMA@ 0.0402 5% 2 UMA@ 1 R393 CONN LVDS_SCL
- <15> EDID_DATA UMA@ 0.0402 5% 2 UMA@ 1 R394 CONN LVDS_SDA
- <15> LVDS_A0 UMA@ 0.0402 5% 2 UMA@ 1 R383 CONN LVDS_A0
- <15> LVDS_A0# UMA@ 0.0402 5% 2 UMA@ 1 R382 CONN LVDS_A0#
- <15> LVDS_A1 UMA@ 0.0402 5% 2 UMA@ 1 R389 CONN LVDS_A1
- <15> LVDS_A1# UMA@ 0.0402 5% 2 UMA@ 1 R388 CONN LVDS_A1#
- <15> LVDS_A2 UMA@ 0.0402 5% 2 UMA@ 1 R386 CONN LVDS_A2
- <15> LVDS_A2# UMA@ 0.0402 5% 2 UMA@ 1 R387 CONN LVDS_A2#
- <15> LVDS_ACLK UMA@ 0.0402 5% 2 UMA@ 1 R384 CONN LVDS_ACLK
- <15> LVDS_ACLK# UMA@ 0.0402 5% 2 UMA@ 1 R385 CONN LVDS_ACLK#

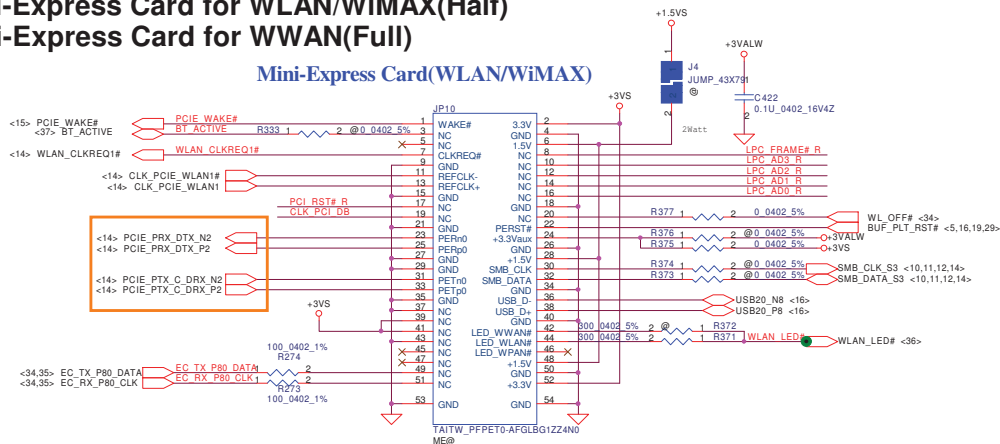
CMOS Camera



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Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for WWAN(Full)

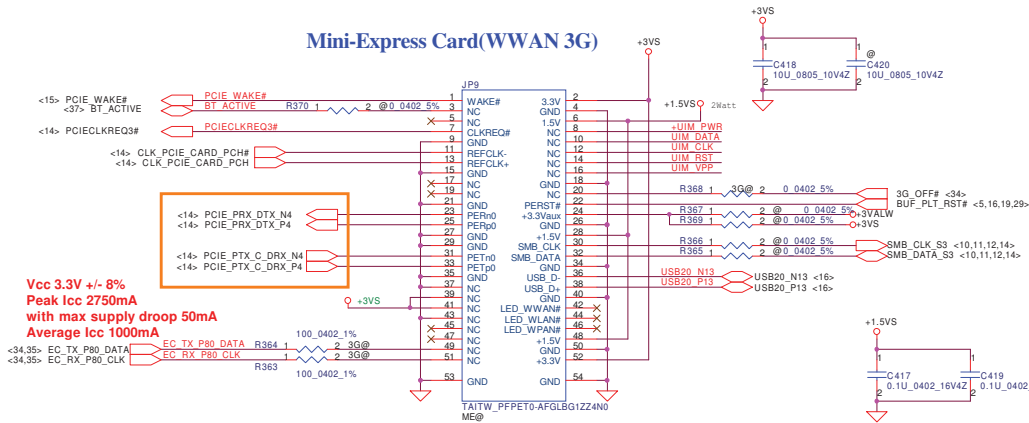
Mini-Express Card(WLAN/WiMAX)



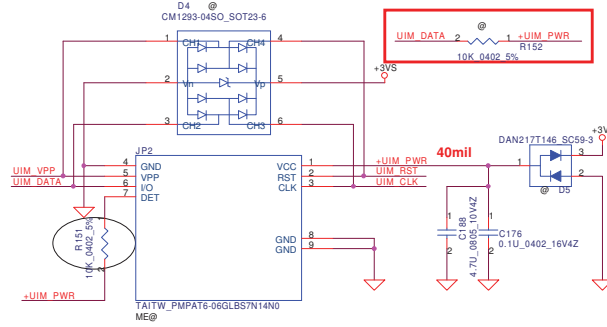
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R284	1	2	0.0402 5%	LPC_FRAME#	<13,34>
LPC_AD3# R	R285	1	2	0.0402 5%	LPC_AD3	<13,34>
LPC_AD2# R	R286	1	2	0.0402 5%	LPC_AD2	<13,34>
LPC_AD1# R	R287	1	2	0.0402 5%	LPC_AD1	<13,34>
LPC_ADD# R	R288	1	2	0.0402 5%	LPC_ADD	<13,34>
PCI_RST# R	R290	1	2	0.0402 5%	PCI_RST#	<13,34>
CLK_PCI_DB	R290	1	2	0.0402 5%	CLK_PCI_DB	<14>

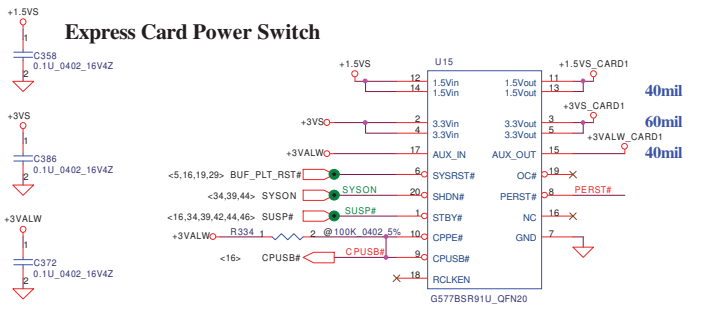
Mini-Express Card(WWAN 3G)



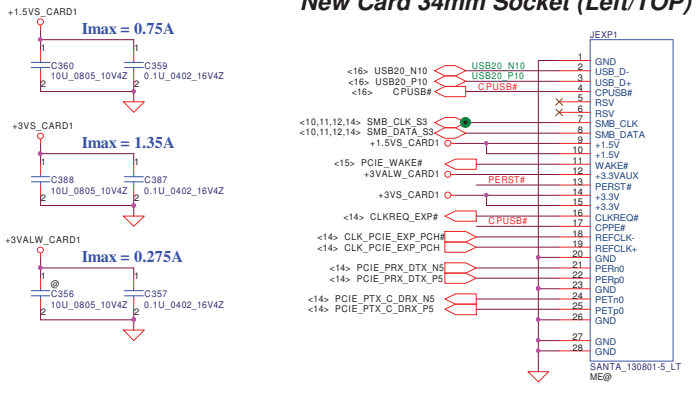
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mV
Average Icc 1000mA



Express Card Power Switch

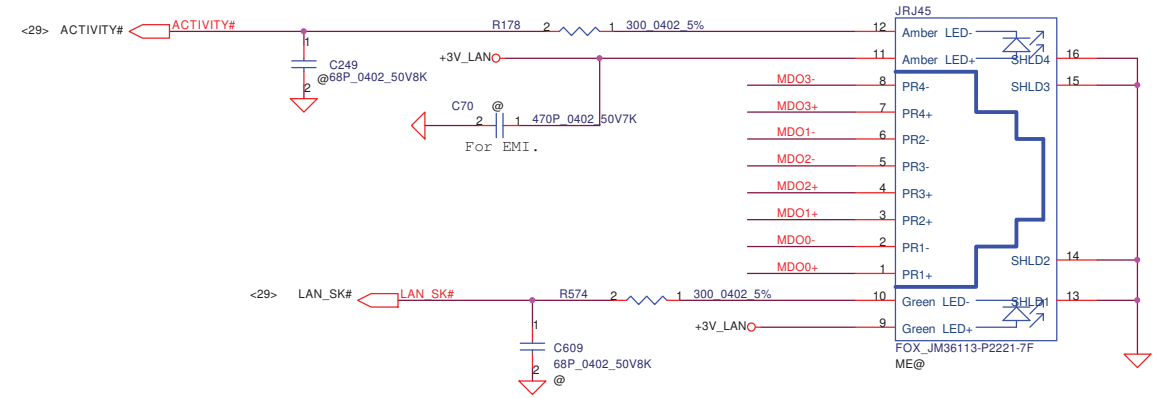
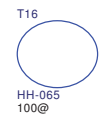
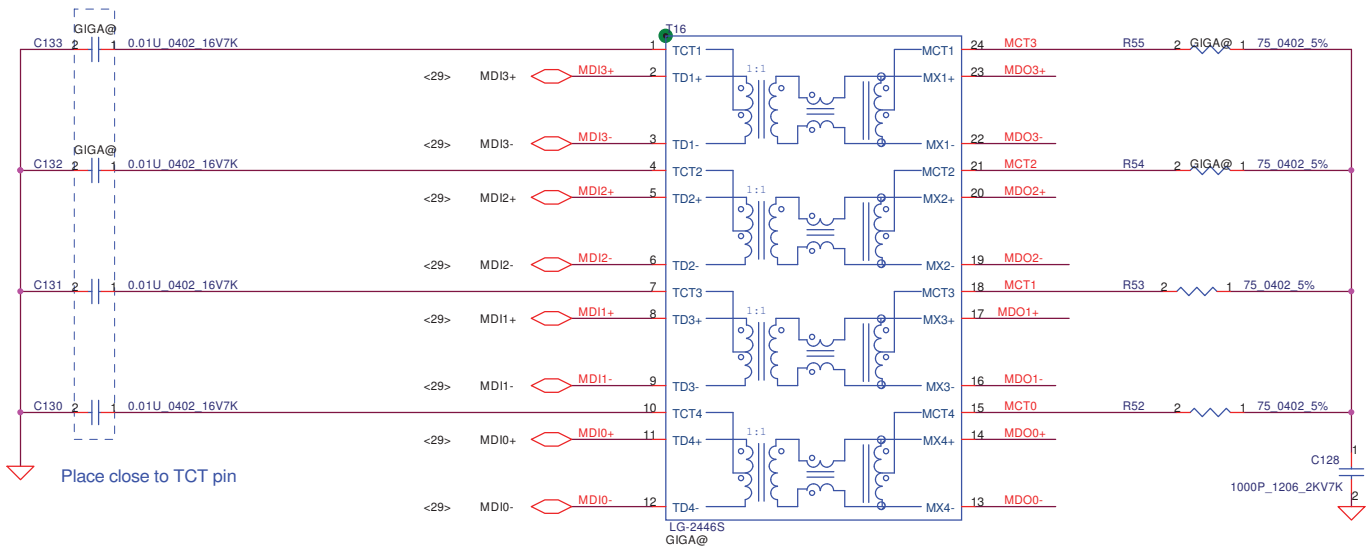


New Card 34mm Socket (Left/TOP)



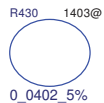
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Close to T14

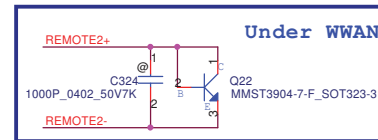
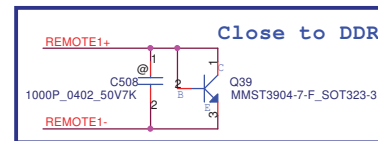
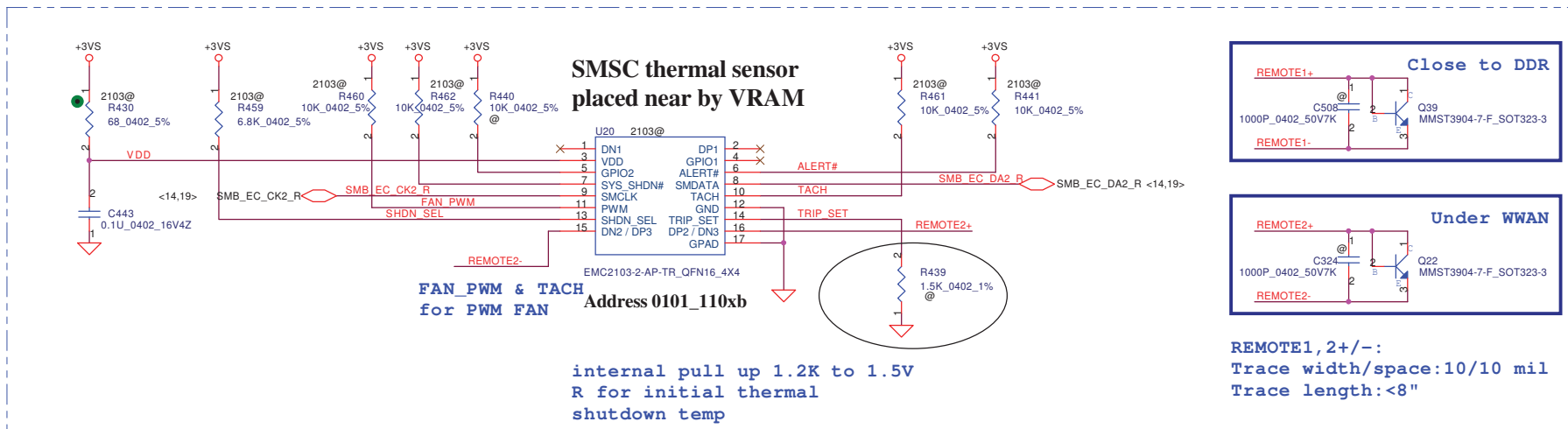


RJ45 Conn.

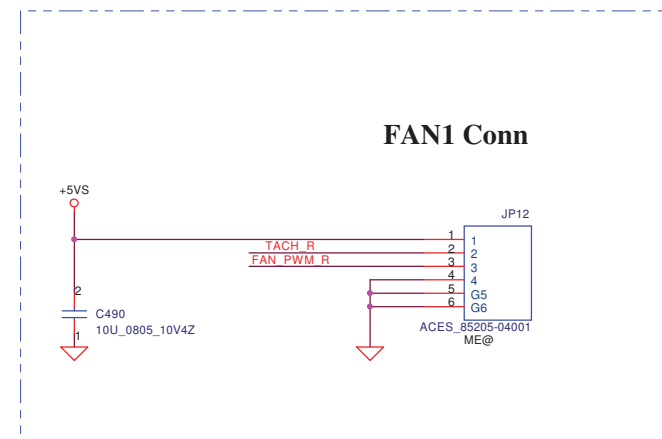
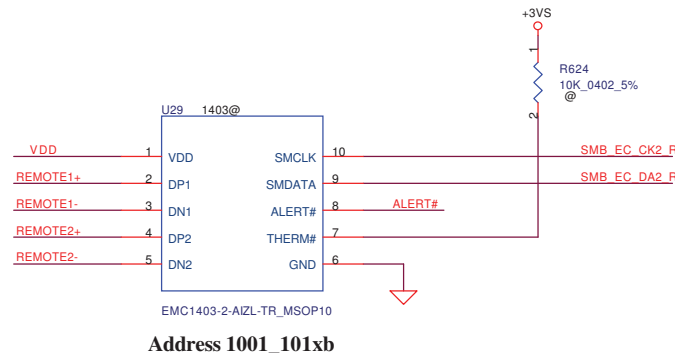
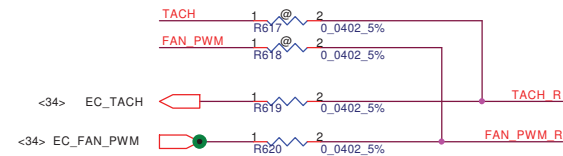
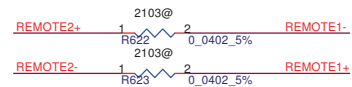
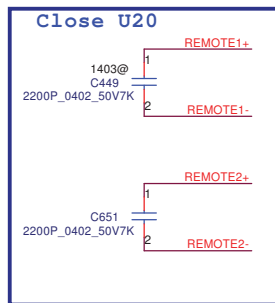
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Issued Date	2009/03/20	Deciphered Date	2010/03/20	Title	
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Custom	Document Number			LA-5752P	0.3
Date:	Thursday, October 29, 2009	Sheet	30 of 51		



1403:
@C508/@C324=100p



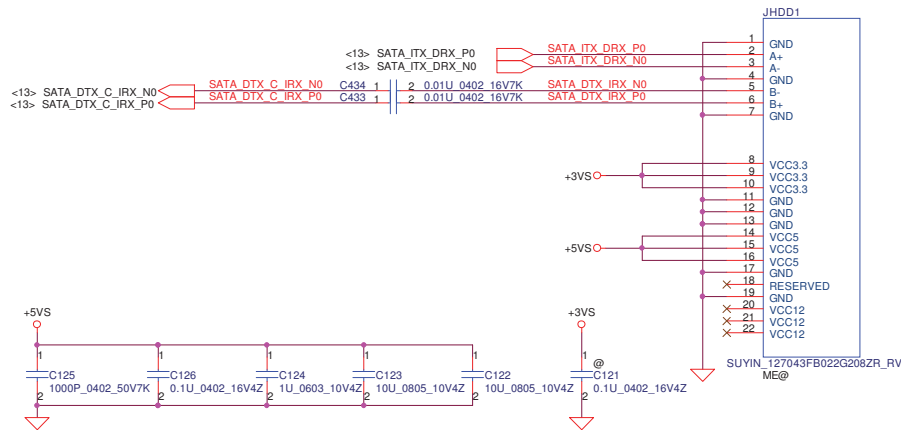
REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"



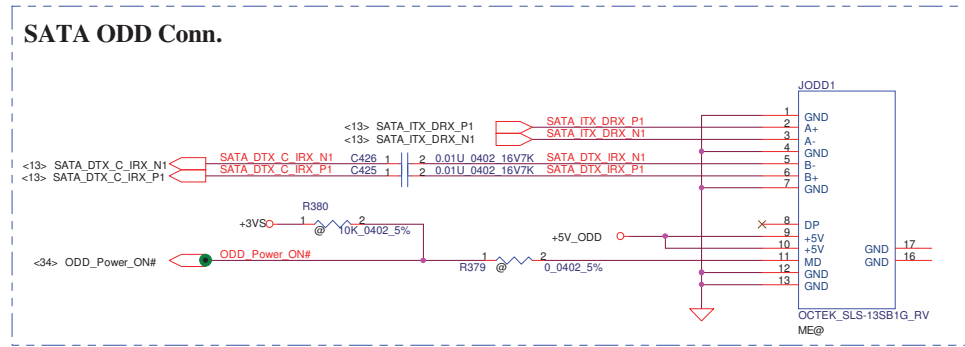
Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	EMC2103/1403_Thermal sensor/FAN
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Date:	Thursday, October 29, 2009	Sheet	31 of 51	Rev	0.3

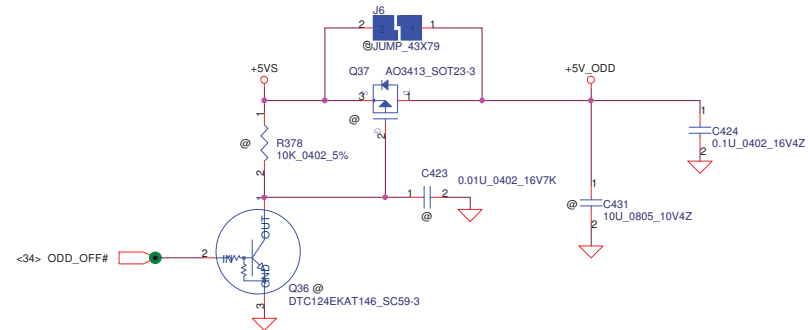
SATA HDD Conn.



SATA ODD Conn.

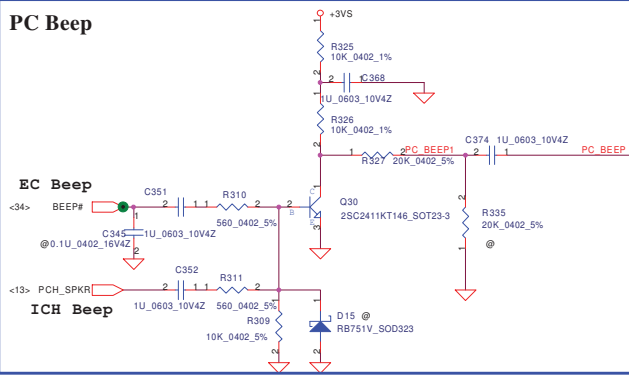
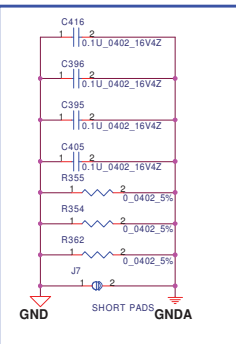
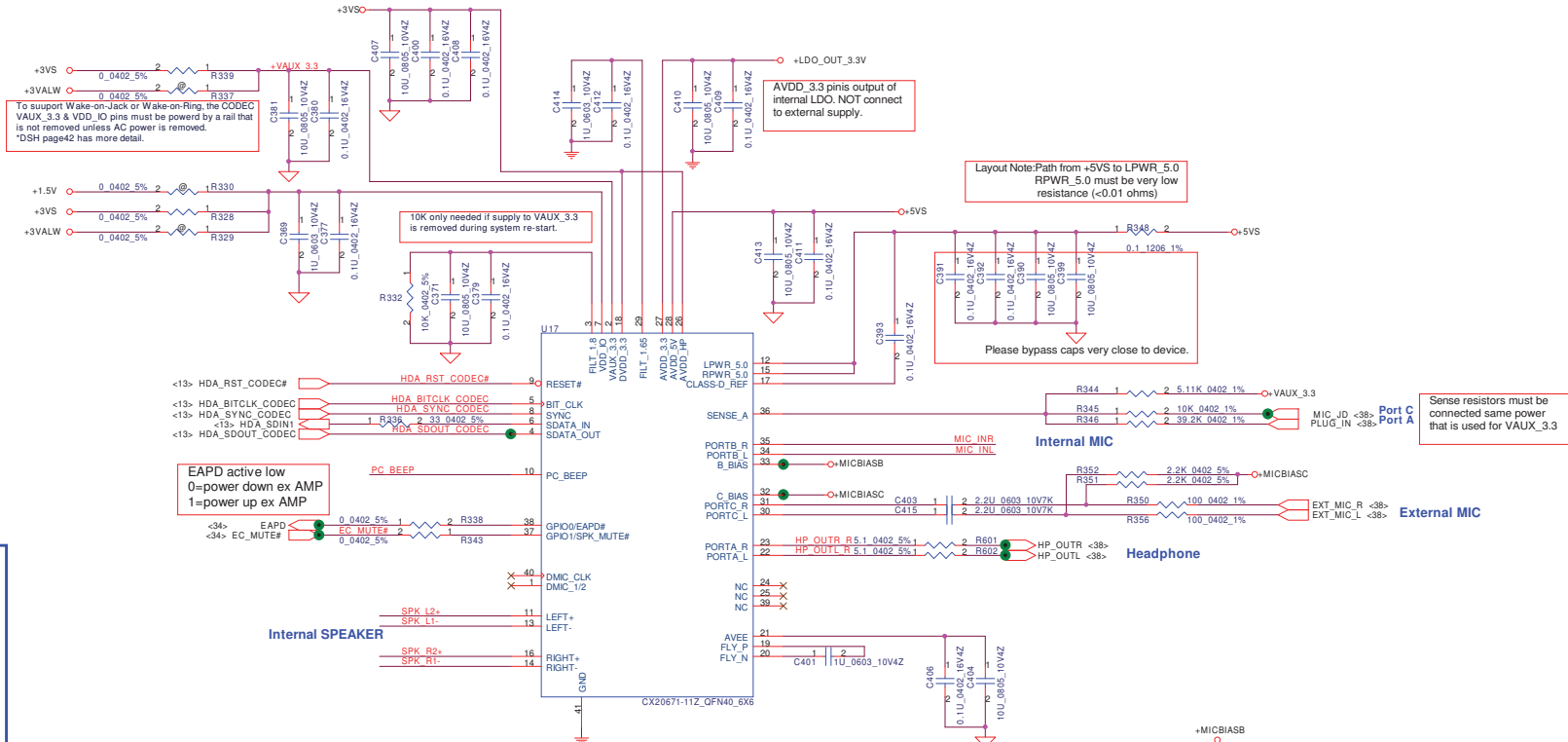
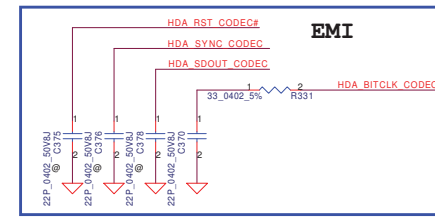


ODD Power Control

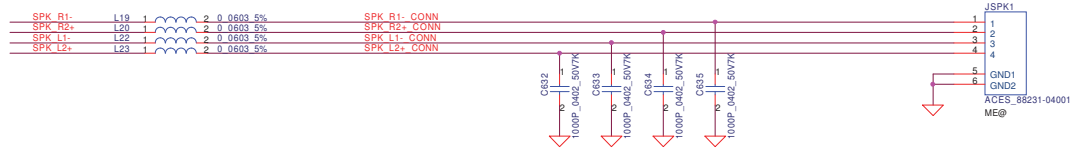


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				Size B	Document Number	Rev
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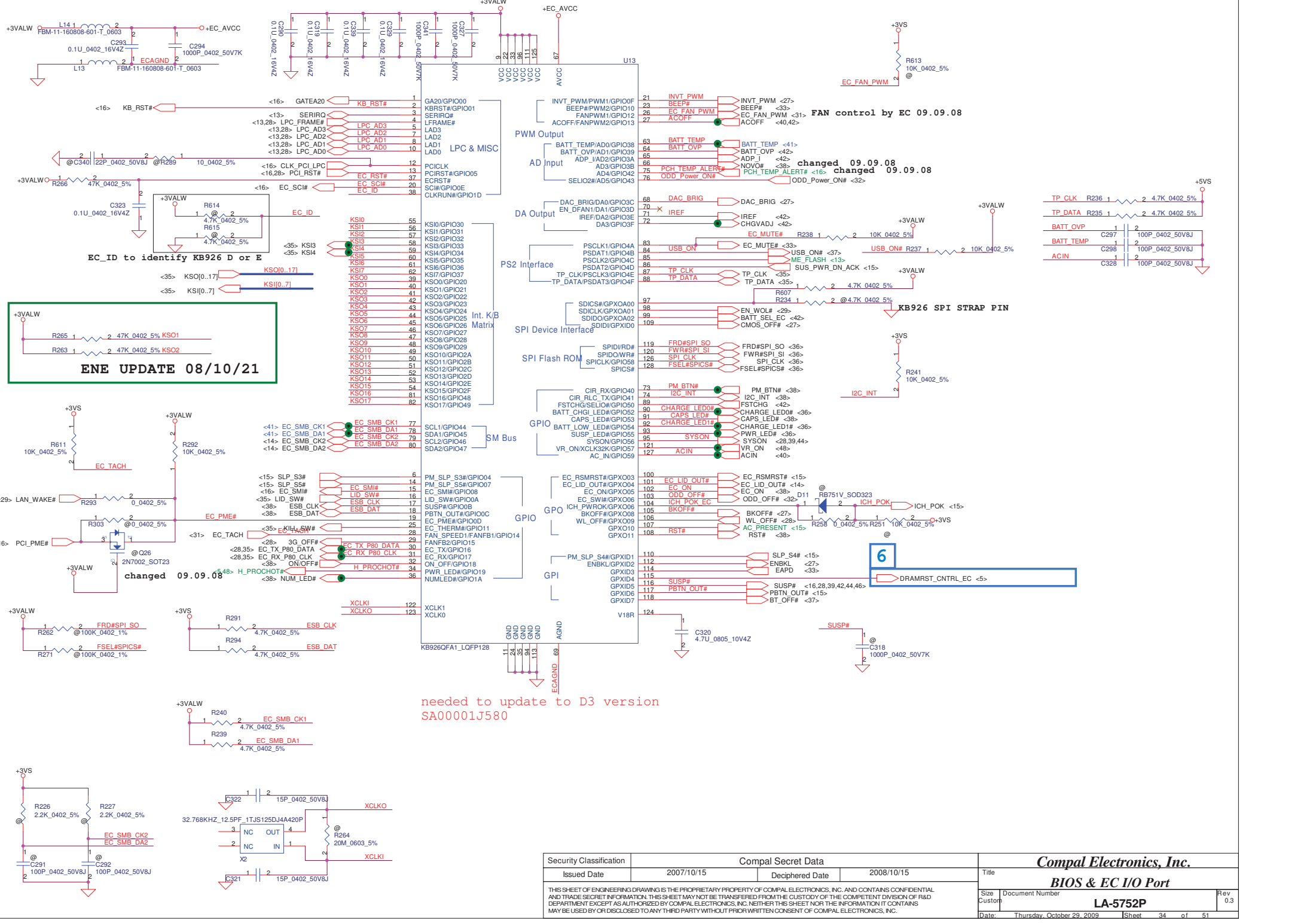
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



wide 20MIL



Security Classification	Compal Secret Data		Title	
Issued Date	2008/03/25	Deciphered Date	2008/04/	CX20671 Codec
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Date: Thursday, October 29, 2009	Sheet	33	of	51



EC_ID to identify KB926 D or E

ENE UPDATE 08/10/21

needed to update to D3 version
SA00001J580

Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	BIOS & EC I/O Port
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Size	Document Number	Rev		0.3
Custor	LA-5752P	Date		Thursday, October 29, 2009
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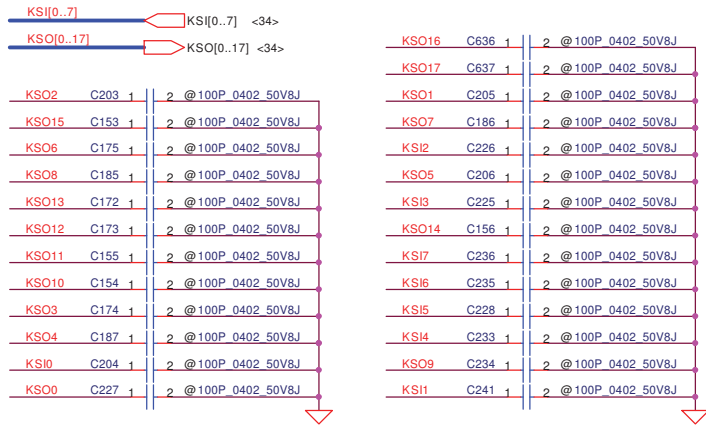
Compal Electronics, Inc.

BIOS & EC I/O Port

LA-5752P

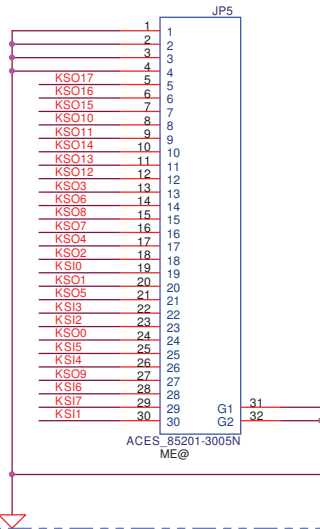
Thursday, October 29, 2009 Sheet 34 of 51

INT_KBD Conn.

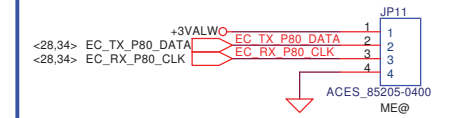


CONN PIN define need double check

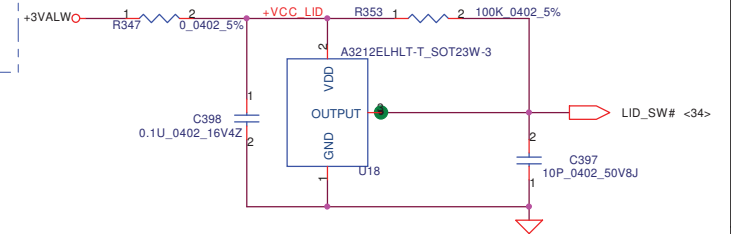
reversal of NIWE1



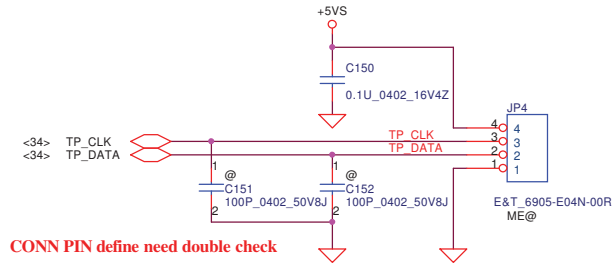
EC DEBUG PORT



Lid Switch

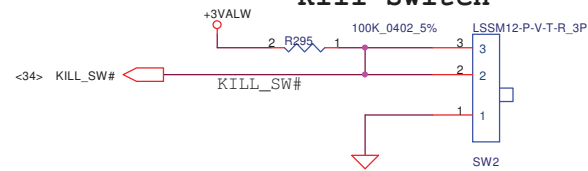


To TP/B Conn.



CONN PIN define need double check

Kill Switch

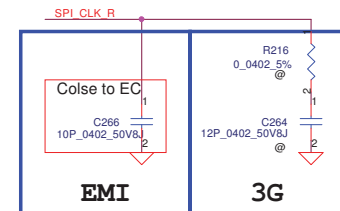
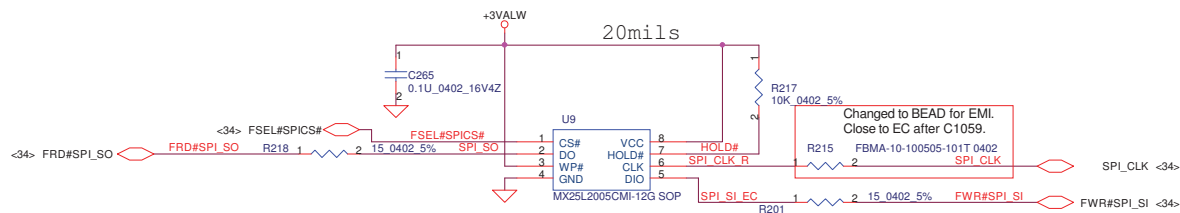


Kill

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Size	Document Number	Date:	Thursday, October 29, 2009	Sheet 35 of 51

**FOR EC 256KB SPI ROM
(150mil PACKAGE)
P/N : SA00003GK00**

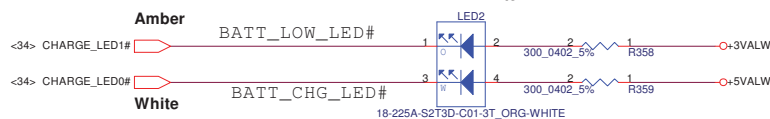


LED

SC500005B00



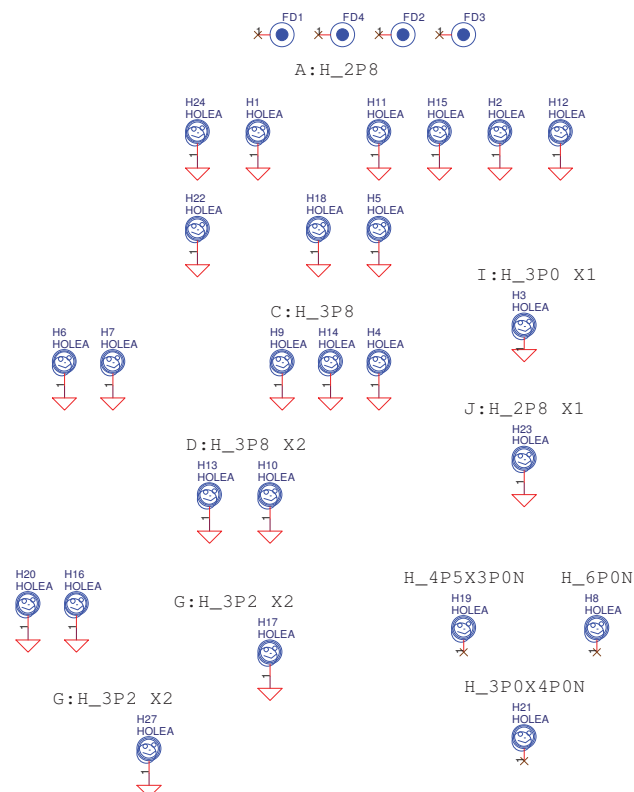
SC500006M00



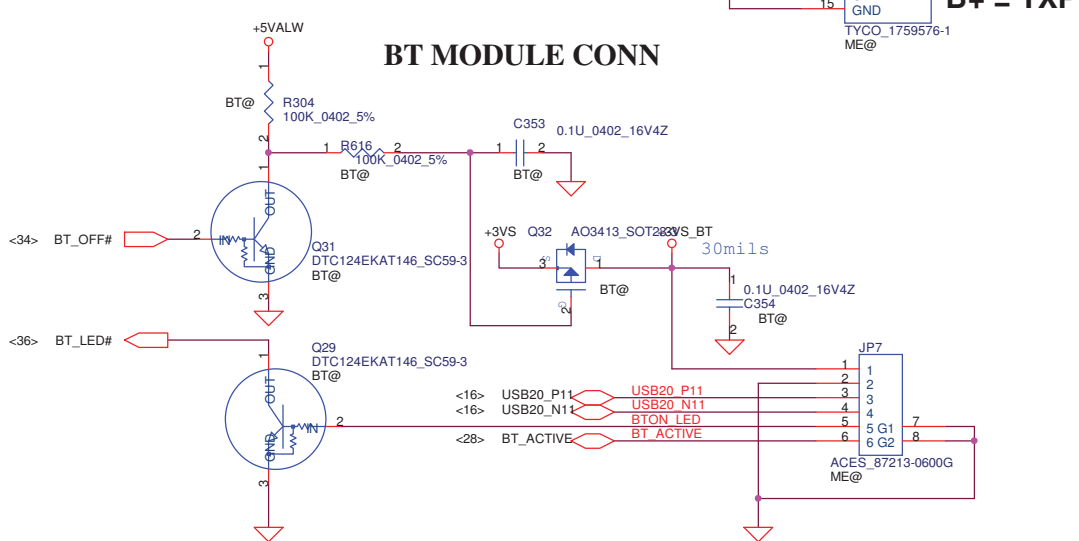
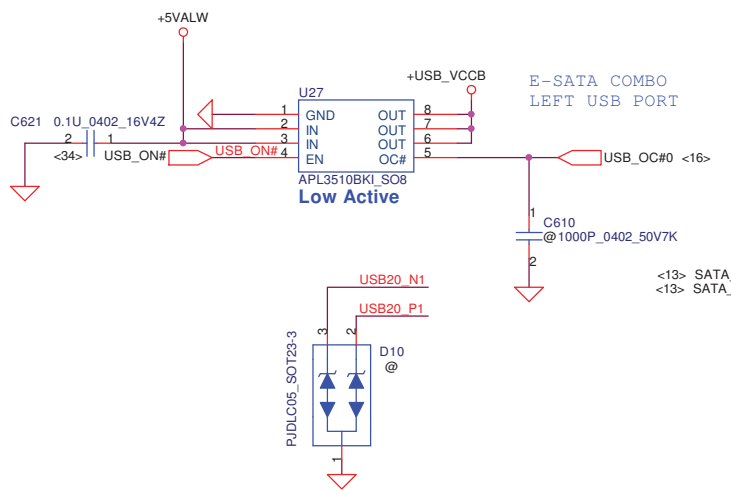
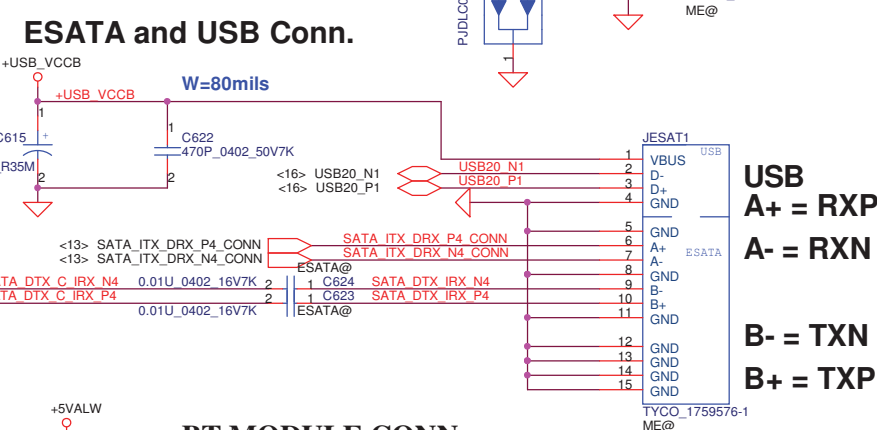
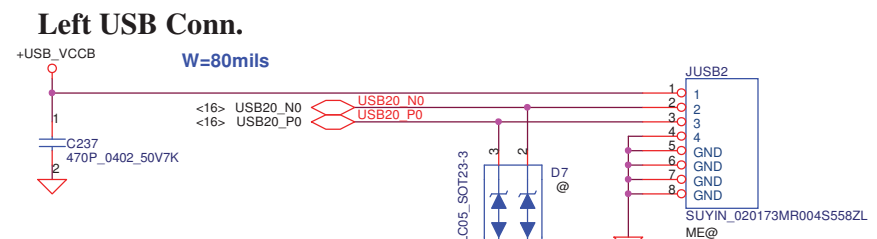
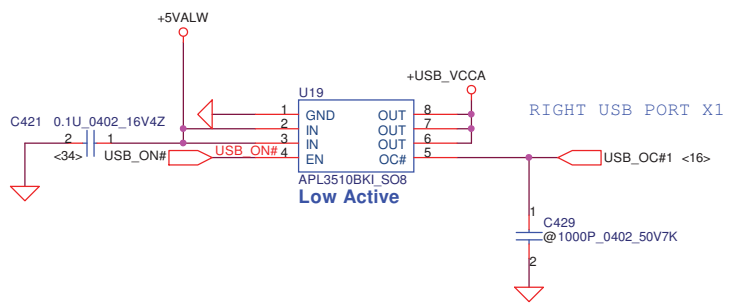
SC500005B00



SC500005B00

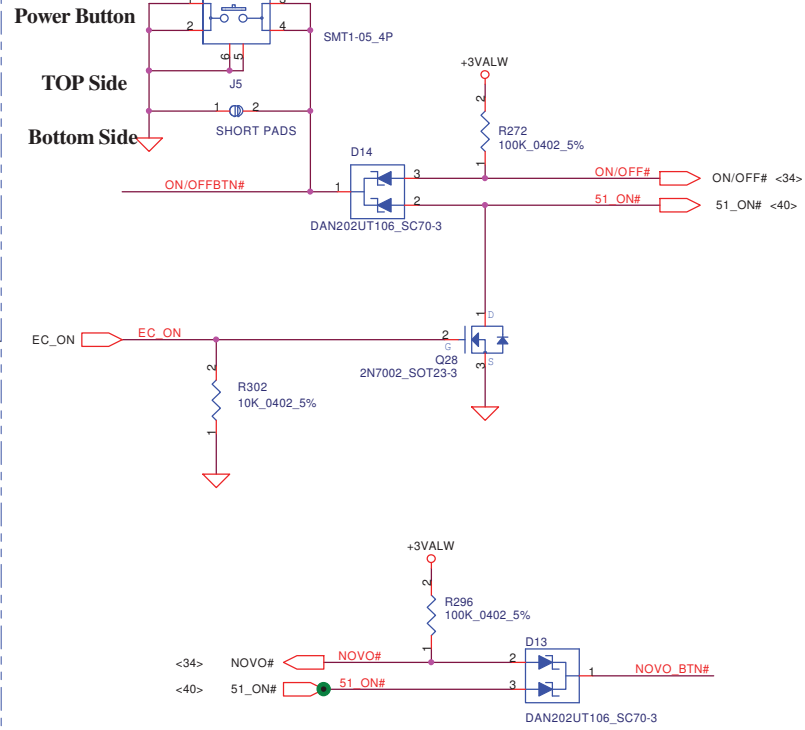


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Size B	Document Number	LA-5752P		Rev 0.3
Date:	Thursday, October 29, 2009	Sheet	36	of 51

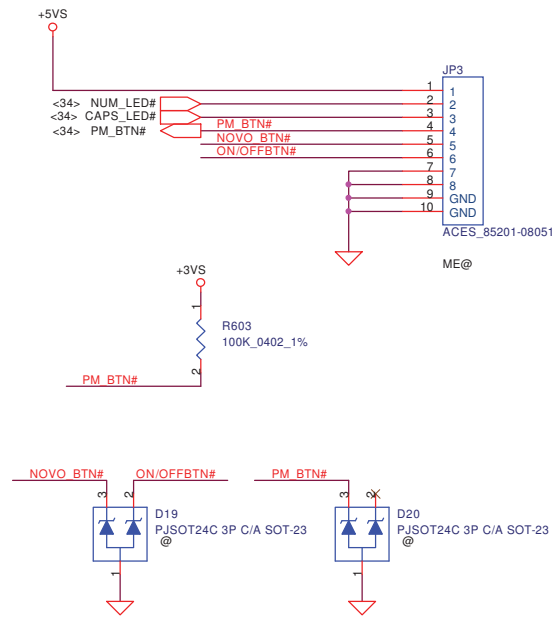


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Size	Custom	Document Number	LA-5752P	Rev	0.3
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ON/OFF switch

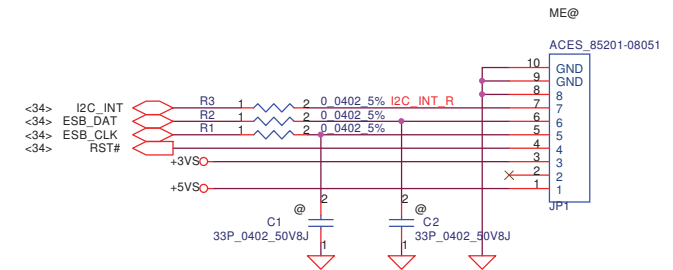


Power Bottom Board Conn. 8pin

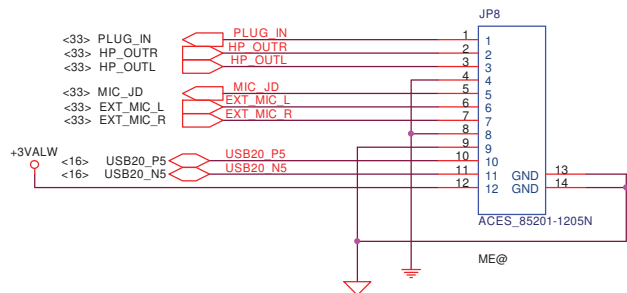


EMI REQUEST 1ST = SCA00000E00
 2ST = SCA00000R00

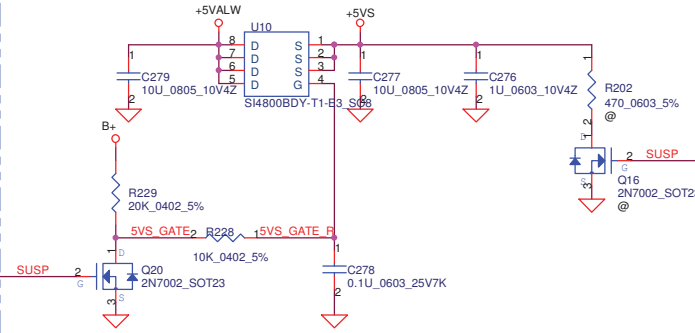
Cap Sensor Board Conn. 6pin ENE SB3534



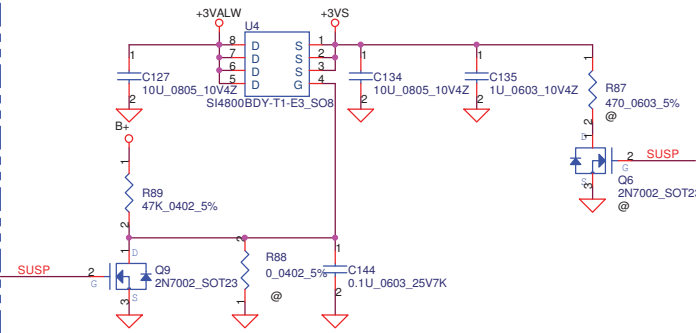
Card Reader/Audio Jack SB CONN



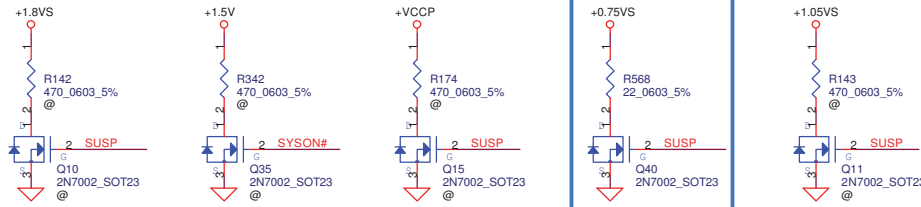
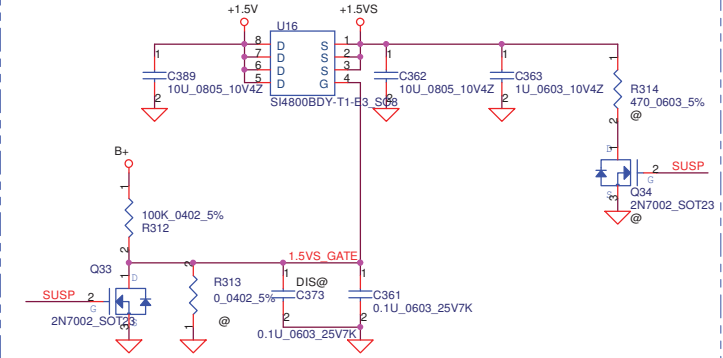
+5VALW TO +5VS



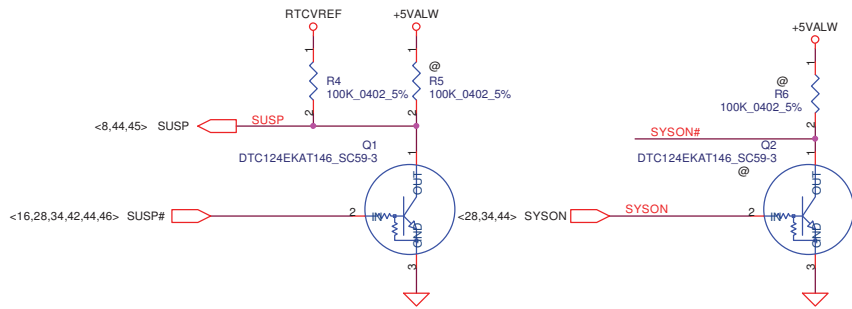
+3VALW TO +3VS



+1.5V to +1.5VS

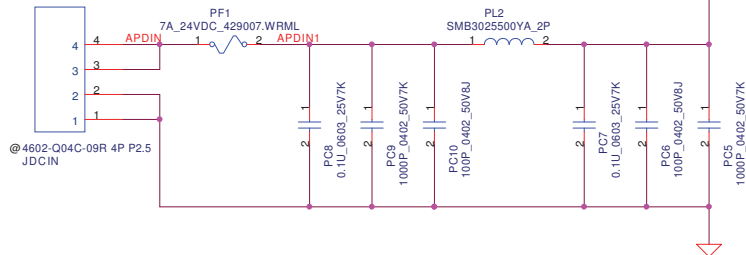


For Intel S3 Power Reduction.

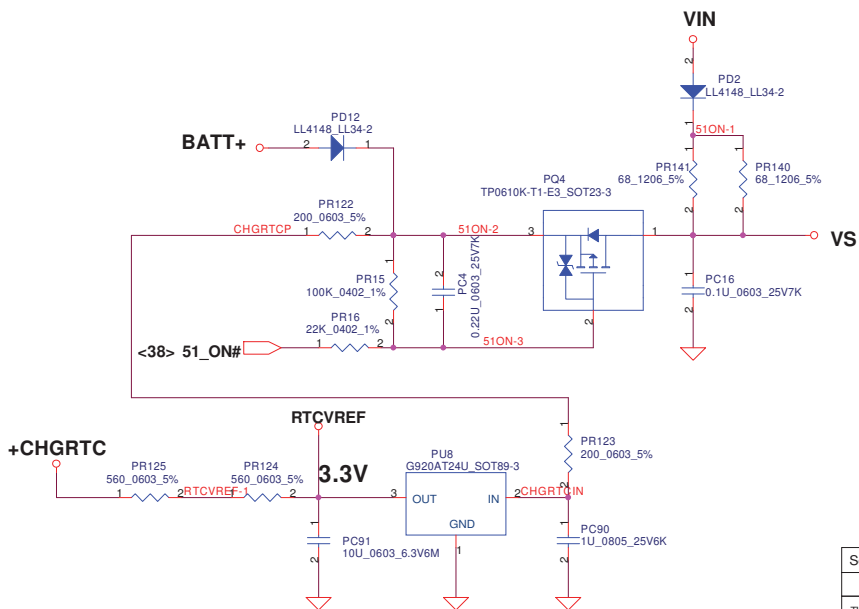
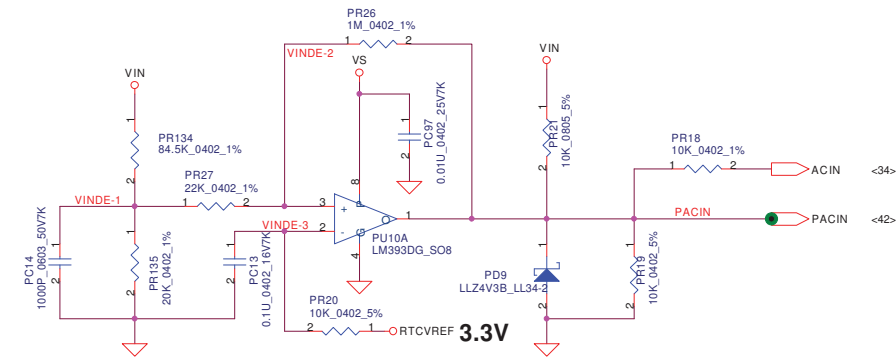


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2006/08/18		2007/8/18		Compal Electronics, Inc.	
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Size	Document Number	Rev		Date	
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				Sheet	39 of 51

DC030006J00

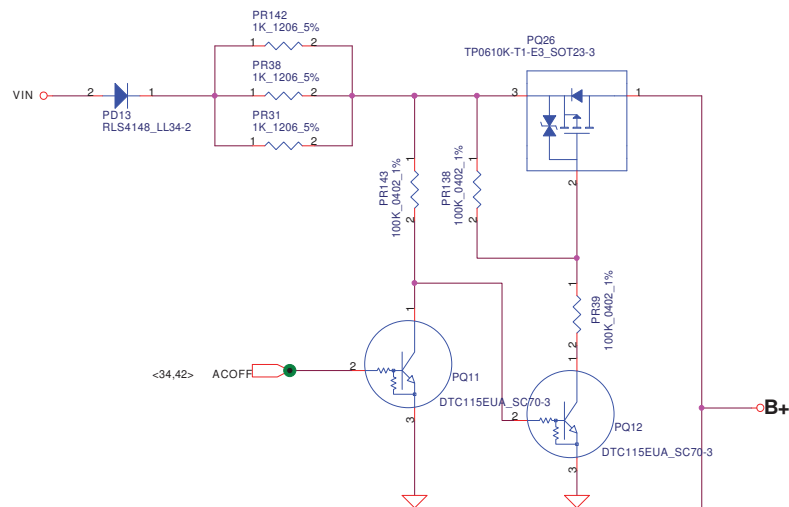


Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



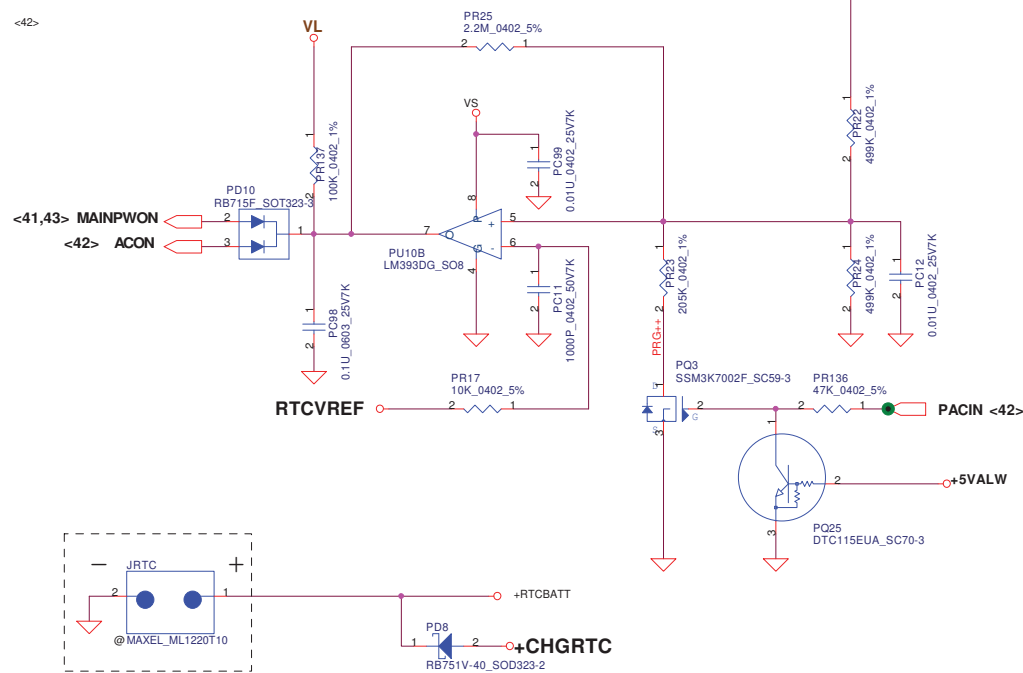
ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

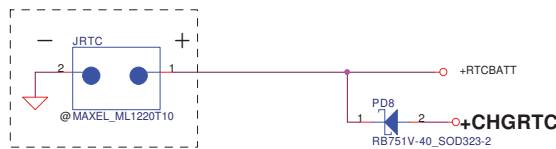


BATT ONLY

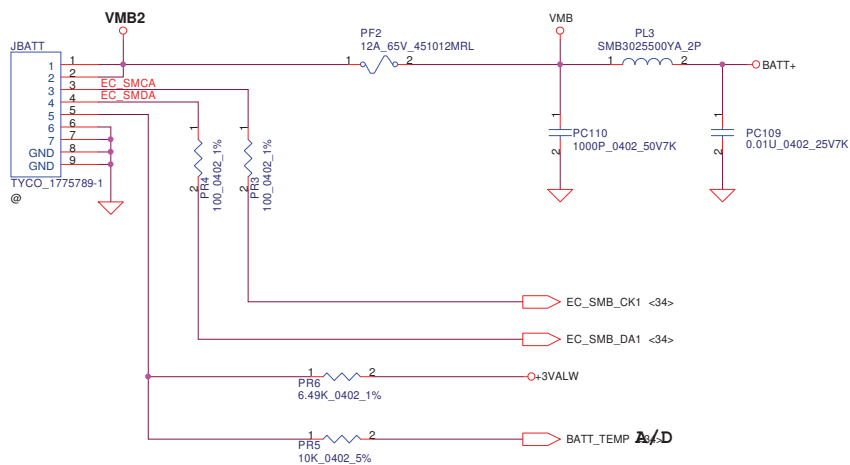
Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



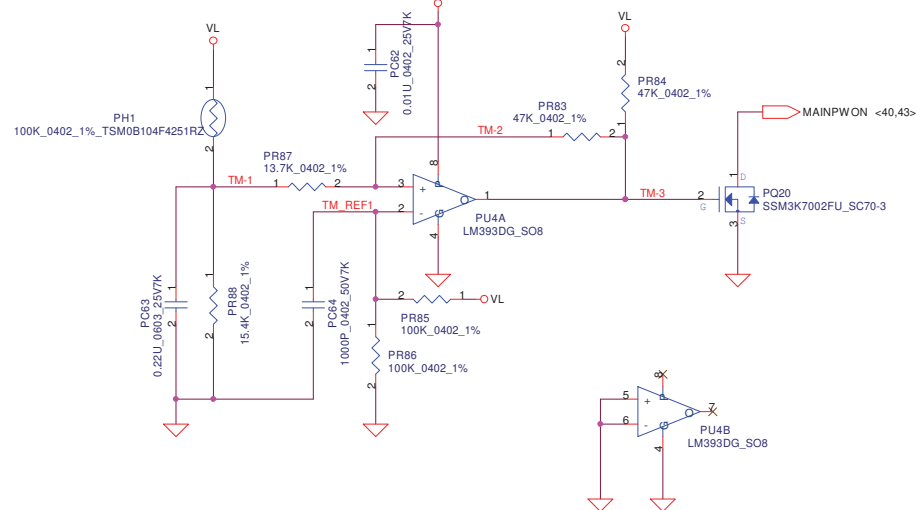
RTC Battery



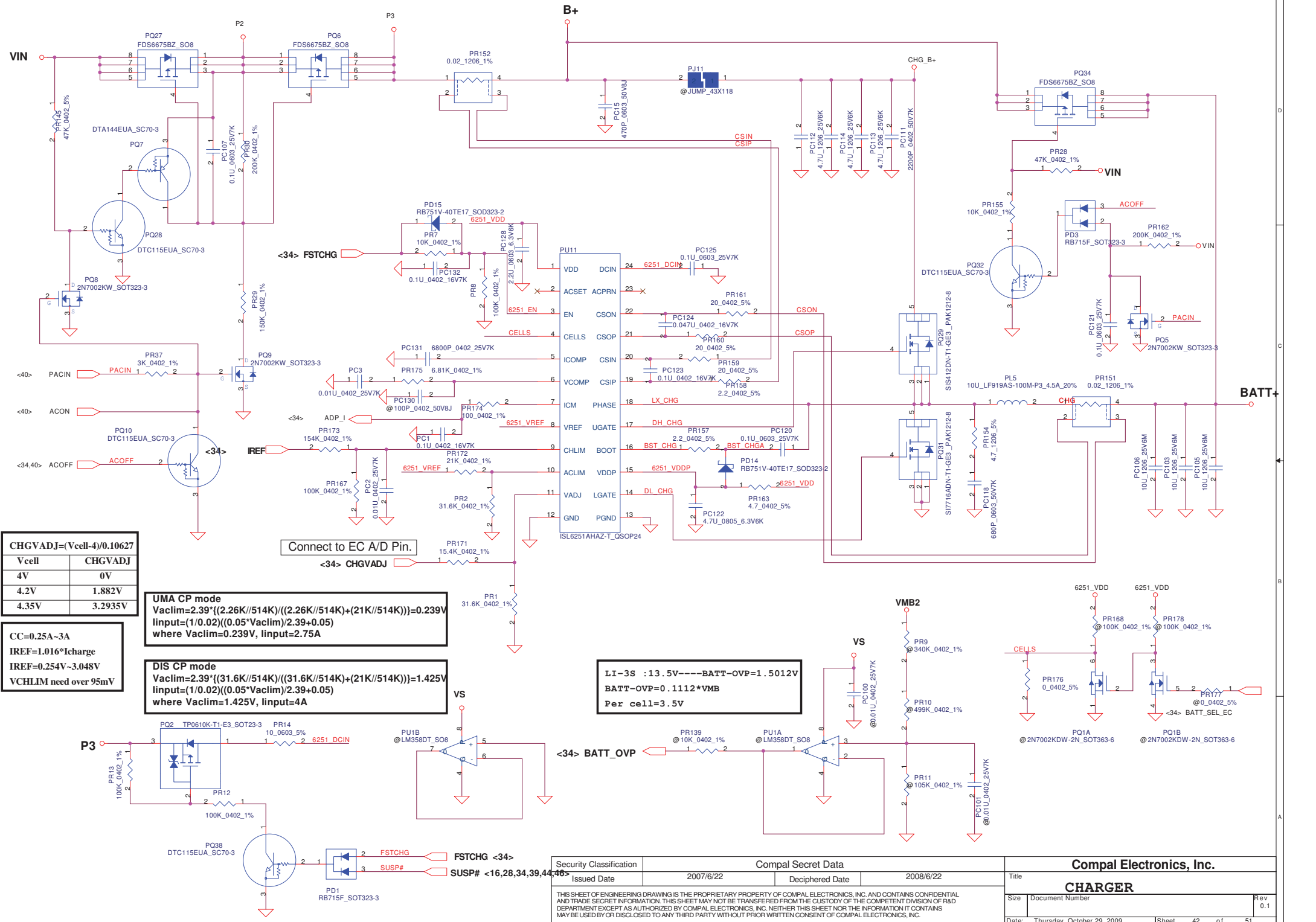
Security Classification				Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title				
				DCIN & DETECTOR				
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Custom								0.1
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title	BATTERY CONN / OTP
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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

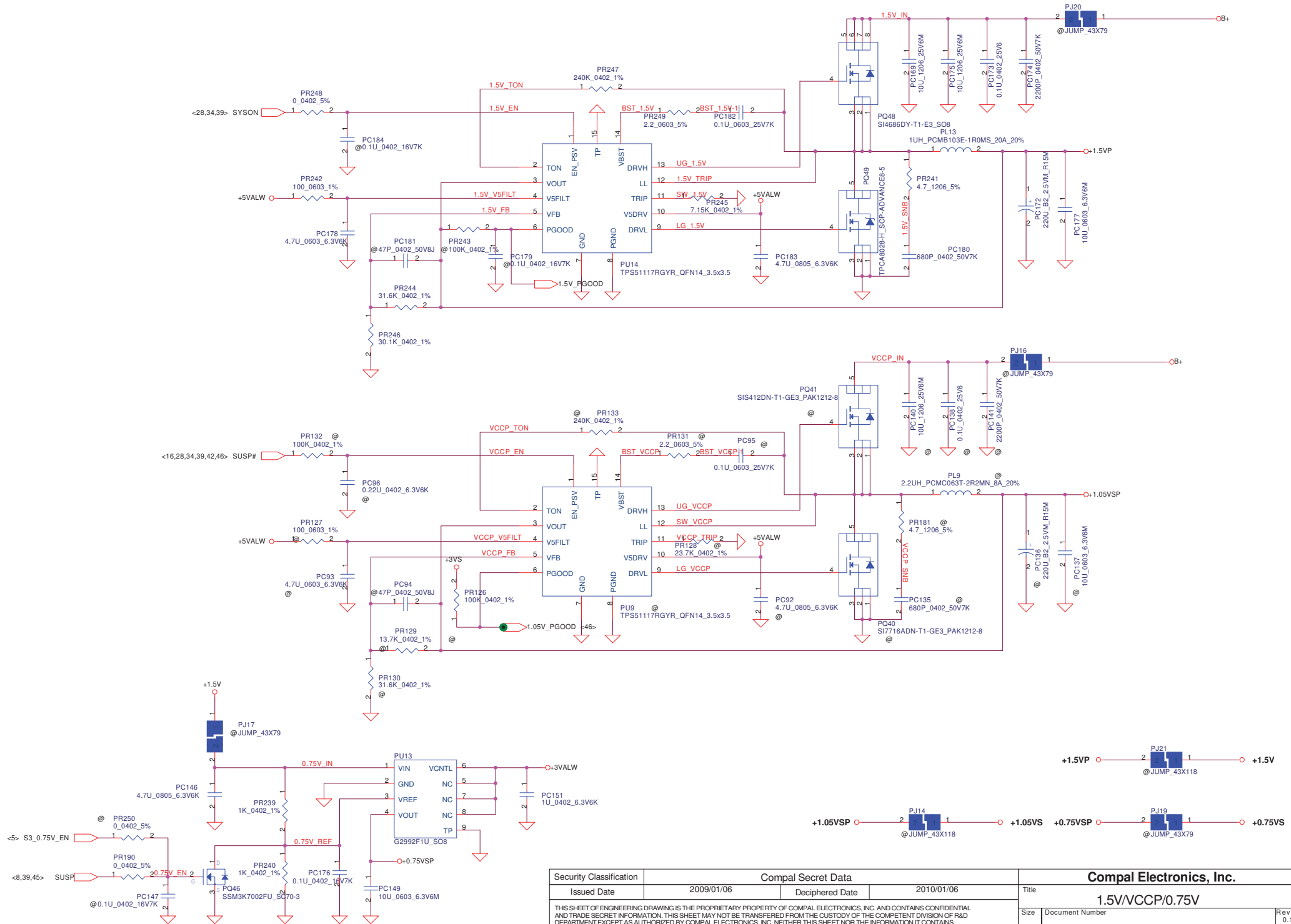
UMA CP mode
 $V_{acli} = 2.39 * ((2.26K/514K) / ((2.26K/514K) + (21K/514K))) = 0.239V$
 $I_{in} = (1/0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
 where $V_{acli} = 0.239V$, $I_{in} = 2.75A$

DIS CP mode
 $V_{acli} = 2.39 * ((31.6K/514K) / ((31.6K/514K) + (21K/514K))) = 1.425V$
 $I_{in} = (1/0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
 where $V_{acli} = 1.425V$, $I_{in} = 4A$

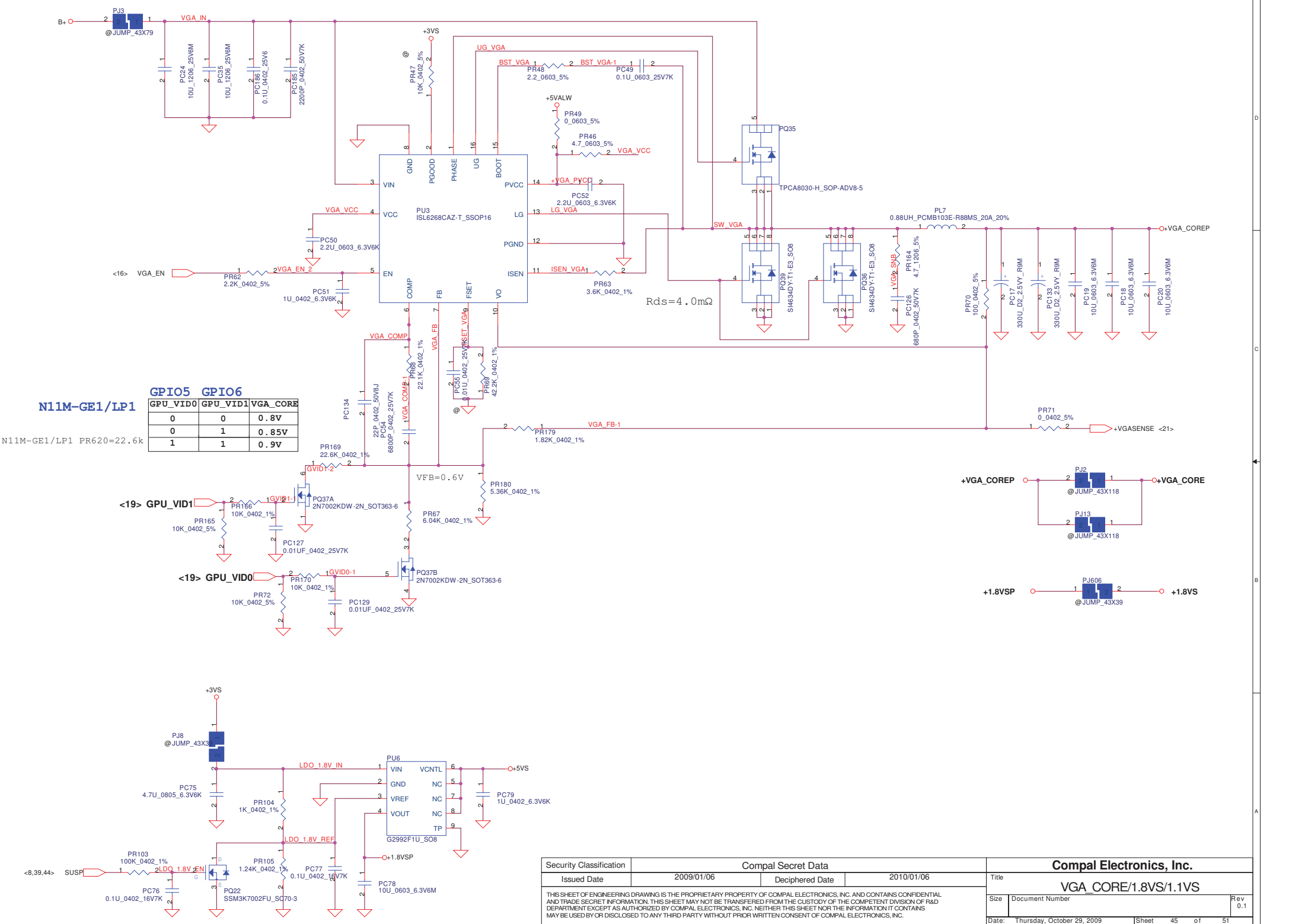
LI-3S : 13.5V --- BATT-OVP=1.5012V
 BATT-OVP=0.1112 * VMB
 Per cell=3.5V

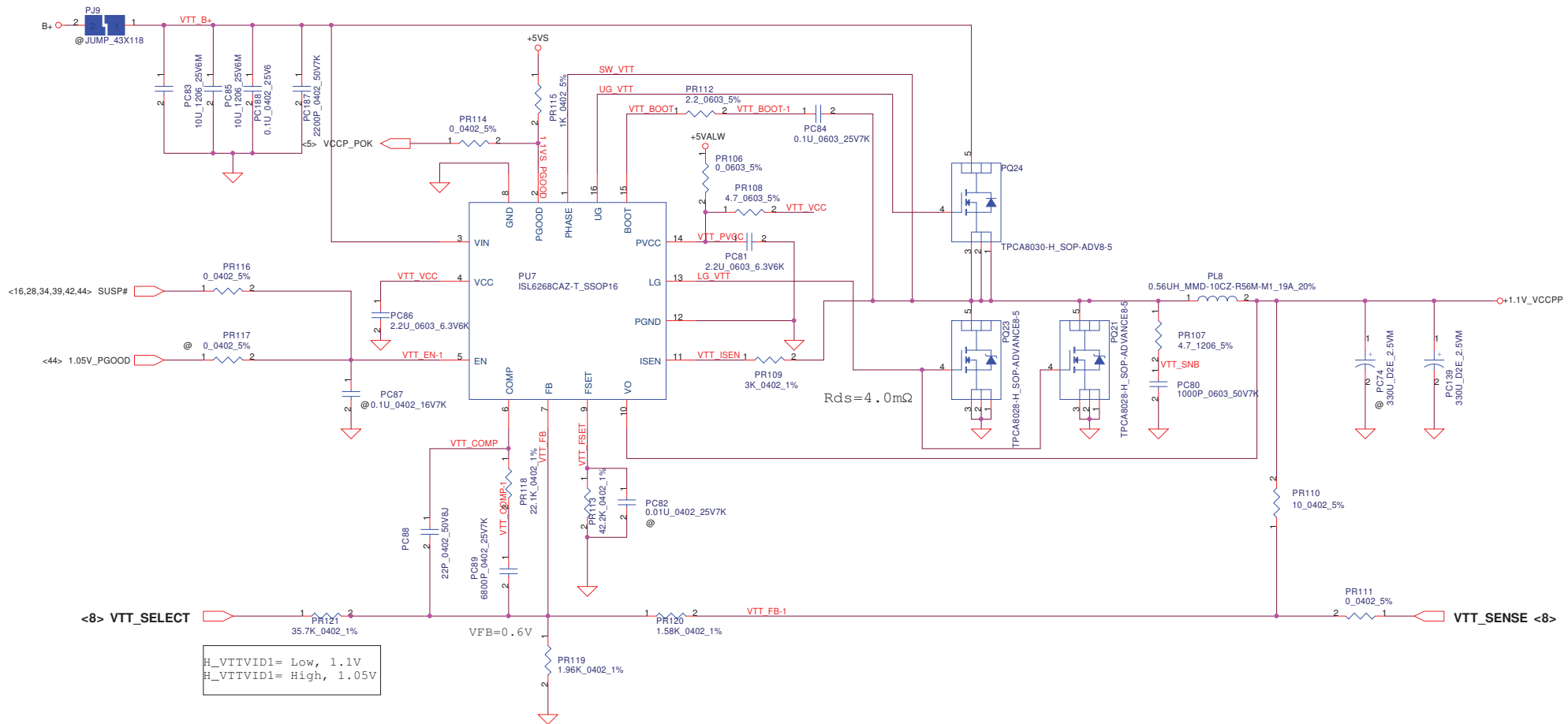
Connect to EC A/D Pin.
 <34> CHGVADJ

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	CHARGER	
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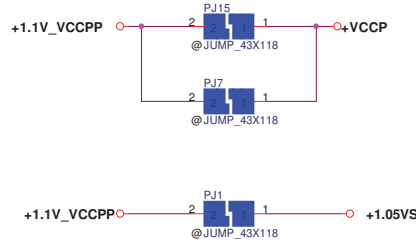


Security Classification	Compal Secret Data		Title	
Issued Date	2009/01/06	Deciphered Date	2010/01/06	1.5V/VCCP/0.75V
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Date:	Thursday, October 29, 2009	Sheet	44 of 51	Rev 0.1

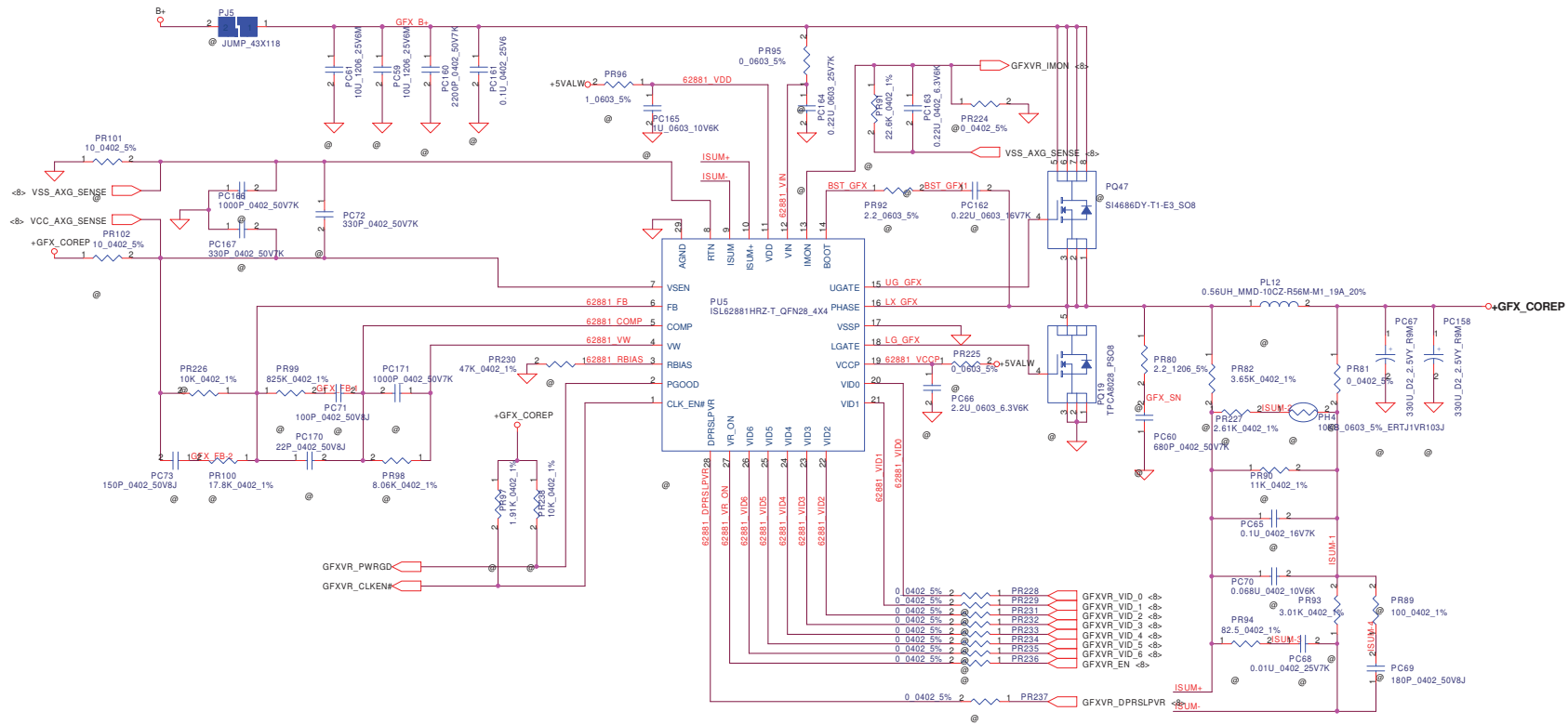




H_VTTVID1= Low, 1.1V
H_VTTVID1= High, 1.05V



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