Compal Confidential

NIWE2

Schematics Document

Arrandale

with Intel IBEX PEAK-M core logic

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **Cover Sheet**

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 1 of 51

Compal confidential
File Name :

zzz

15.6W_PCB_LA5752P

POWER BD: LS-5754P
POWER BT
NOVO BT
POWER MANAGE BT

CAP SENSOR BD:LS-5752P
VOLUME UP
VOLUME DOWN
MUTE
AUDIO ENHANCE
BUTTON & LED

CARD READER BD:
LS-5753P
RTS5138
HP JACK
MIC JACK

VRAM 64*16 DDR3*4 page20

NVidia N11M-GE1 page19~23

PCI-E X16

intel Arrandale (UMA/DIS)
Socket-rPGA989
37.5mm*37.5mm
page5~9

Clock Generator
ICS9LRS3199AKLFT page12

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3 page 10,11
UP TO 8G

Dual Channel
DDR3-800(1.5V)
DDR3-1067(1.5V)

HDMI CONN page24

level shift IC ASM1442 page25

100MHz 2.7GT/s

FDI *8

DMI *4

CRT Connector page26

LVDS Connector page27

Intel Ibex Peak M
FCBGA 951
25mm*25mm
page 13~18

2Channel Speaker page33

AZALIA

Audio Codec
Conexant
CX20671 page33

Analog MIC_Int page33

PCI Express Mini card Slot 1 page28

6*PCI-E BUS

14*USB2.0

CMOS Camera page27

PCI Express Mini card Slot 2 page28

6*SATA serial

BlueTooth CONN page37

USB CONN X1(Right) page37

USB PORT X1(Left) page37

New Card X1 page28

WWAN page28

Card Reader/Audio Jack SB CONN
Realtek 5138
MS/MS
pro/SD/SD
pro/mmc/XD
HP X 1+
MIC_Ext X1
page38

SPI ROM BIOS page13

LPC BUS

SIM Card page28

USB(WWAN)

RTL8111DL-VB-GR
10/100/1G LAN page29

EC
ENE KB926D page34

ESATA HDD AND USB CONN page37

RJ45 CONN page30

Int.KBD page35

Touch Pad page35

SPI ROM page36

SATA HDD CONN page32

SATA ODD CONN page32

Security Classification	Compal Secret Data		
Issued Date	2008/03/24	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: MB Block Diagram

Size: Custom | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 2 of 51

DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1 SMB_EC_DA1	KB926 +3VALW	X	V +3VALW	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926 +3VALW	X	X	X	X	X	X	X	X	X	X	V +3VALW
SMBCLK SMBDATA	PCH +3VALW	V +3VALW	X	X	V +3VS	V +3VS	X	X	X	X	V +3VS	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	V +3VALW	X	X	X	V +3VS	X	V +3VS	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

	EVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA_HDMI@	FOR UMA HDMI components	
HDMI@	FOR HDMI components	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
ESATA@	ESATA function	
CMOS@	Camera function	
BT@	Blue Tooth	
~~10M@~~	~~FOR 10M CHIP~~	
~~11M@~~	~~FOR 11M CHIP~~	
UMA@	UMA only (Arranddale)	
DIS@	DIS only (Arranddale)	
~~VGA@~~	~~FOR NVIDIA PART~~	
~~HYBRID@~~	~~FOR SWITCHABLE~~	
~~HU@~~	~~SWITCHABLE or UMA only~~	
~~HD@~~	~~SWITCHABLE or DIS only~~	

SKU

Arrandale(dGPU) DIS only	DIS@ / 100@ for EVT
Arrandale(iGPU) UMA only	UMA@ / 100@ for EVT
~~Arrandale(iGPU+dGPU)~~ ~~SWITCHABLE~~	~~VGA@+HD@+HU@+HYBRID@~~

PCIE PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID orPower supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6 GPIO5 N10M-GS N10P-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0,10
1	1	1.0V (N10M-GS) 0.925V (N10P-GS)	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

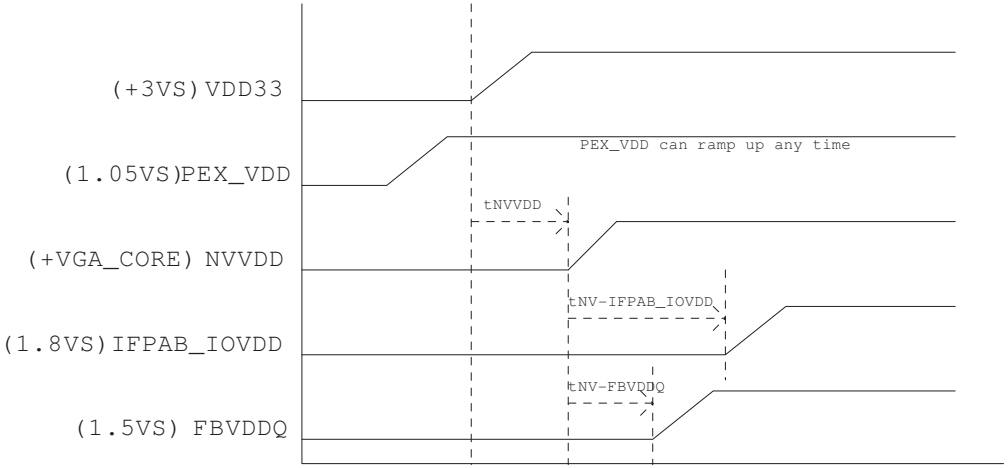
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.5V) (A)	FBVDD (1.5V) (W)	FBVDDQ (GPU+Mem) (1.5V) (A)	FBVDDQ (GPU+Mem) (1.5V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

Power Sequence

The ramp time for any rail must be more than 40us

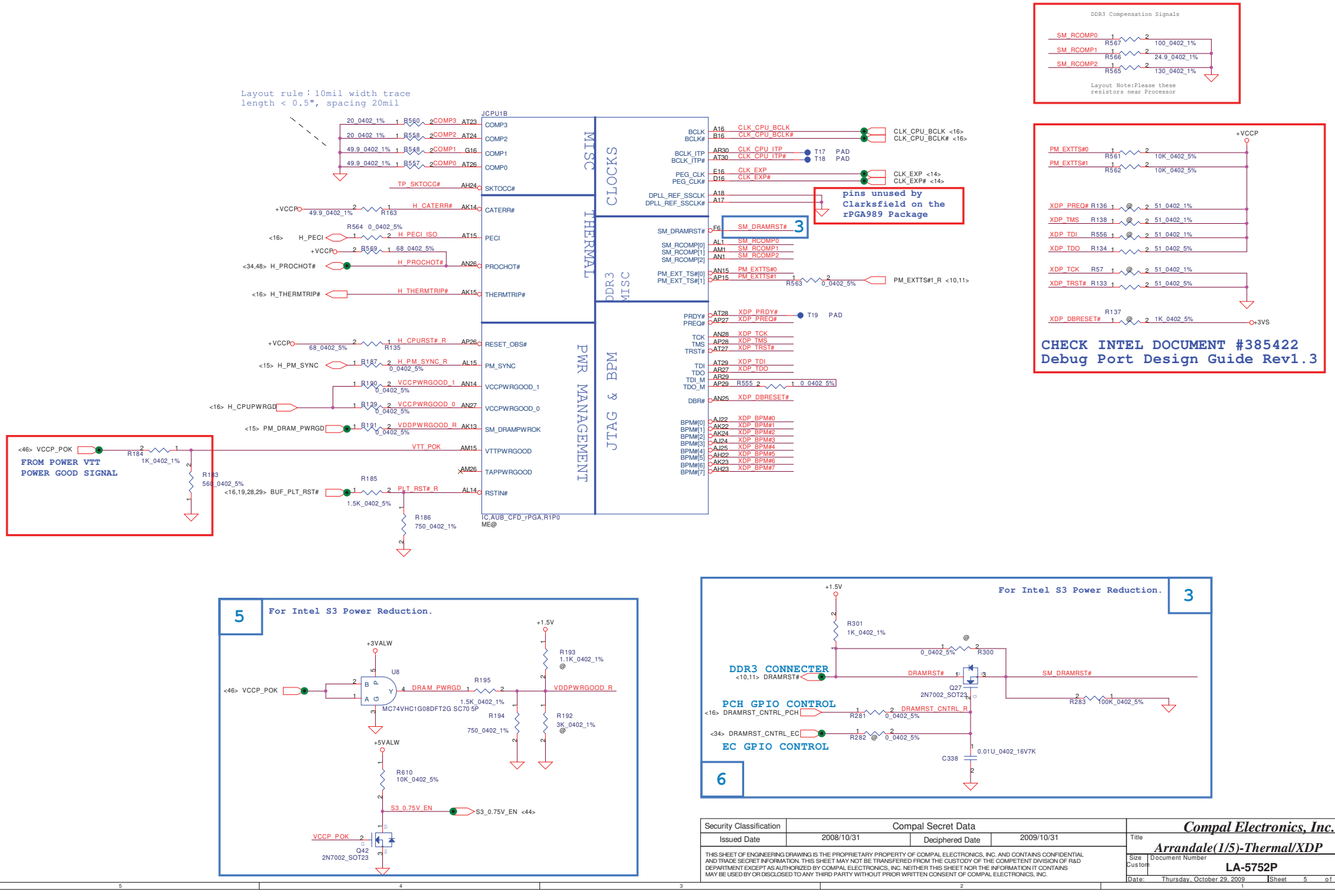


Compal Electronics, Inc.

Title: VGA Notes List

Size: B | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 4 of 51



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.			
Title	Arrandale(1/5)-Thermal/XDP		
Size: Custom	Document Number: LA-5752P		Rev: 0.3
Date: Thursday, October 29, 2009	Sheet 5 of 51		

Layout rule：trace length < 0.5"

JCPU1A

DMI

PCI EXPRESS -- GRAPHICS

FDI

IC,AUB_CFD_rPGA,R1P0
ME@

PCIE Lane Numbers Reversed
CFG3-PCI Express Static Lane Reversal

VGA@

JCPU1E

RESERVED

FOR ES1 SAMPLE ONLY

CFG Straps for PROCESSOR

CFG0	PCI-Express Configuration Select
	1: Single PEG
	0: Bifurcation enabled

Not applicable for Clarksfield Processor

CFG[1:0] 11=1*16 PEG
10=2*8 PEG

CFG3	CFG3-PCI Express Static Lane Reversal
	1: Normal Operation
	0: Lane Numbers Reversed 15 -> 0, 14 ->1, ...

CFG4	CFG4-Display Port Presence
	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

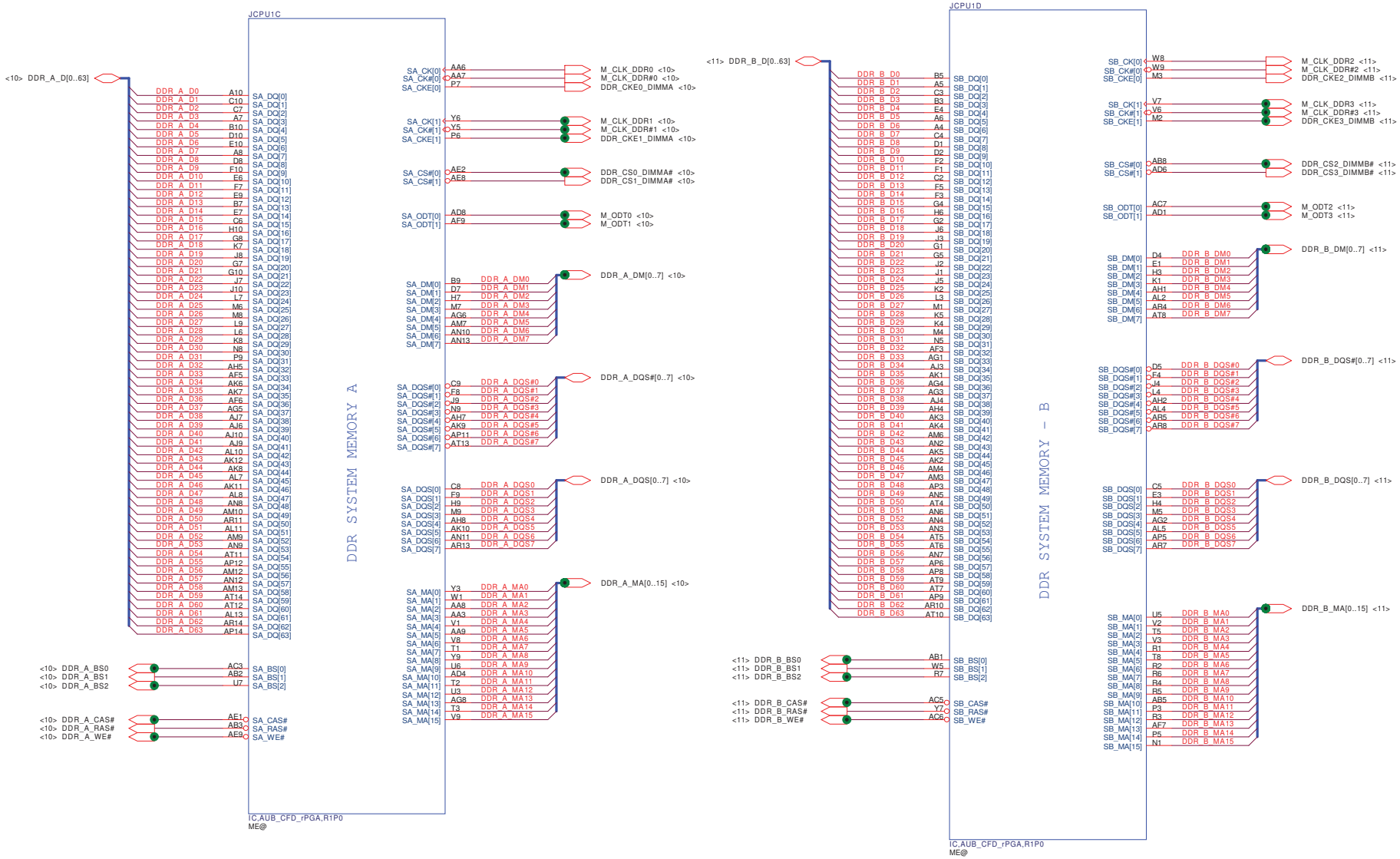
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: Arrandale(2/5)-DMI/PEG/FDI

Size: Custom | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 6 of 51



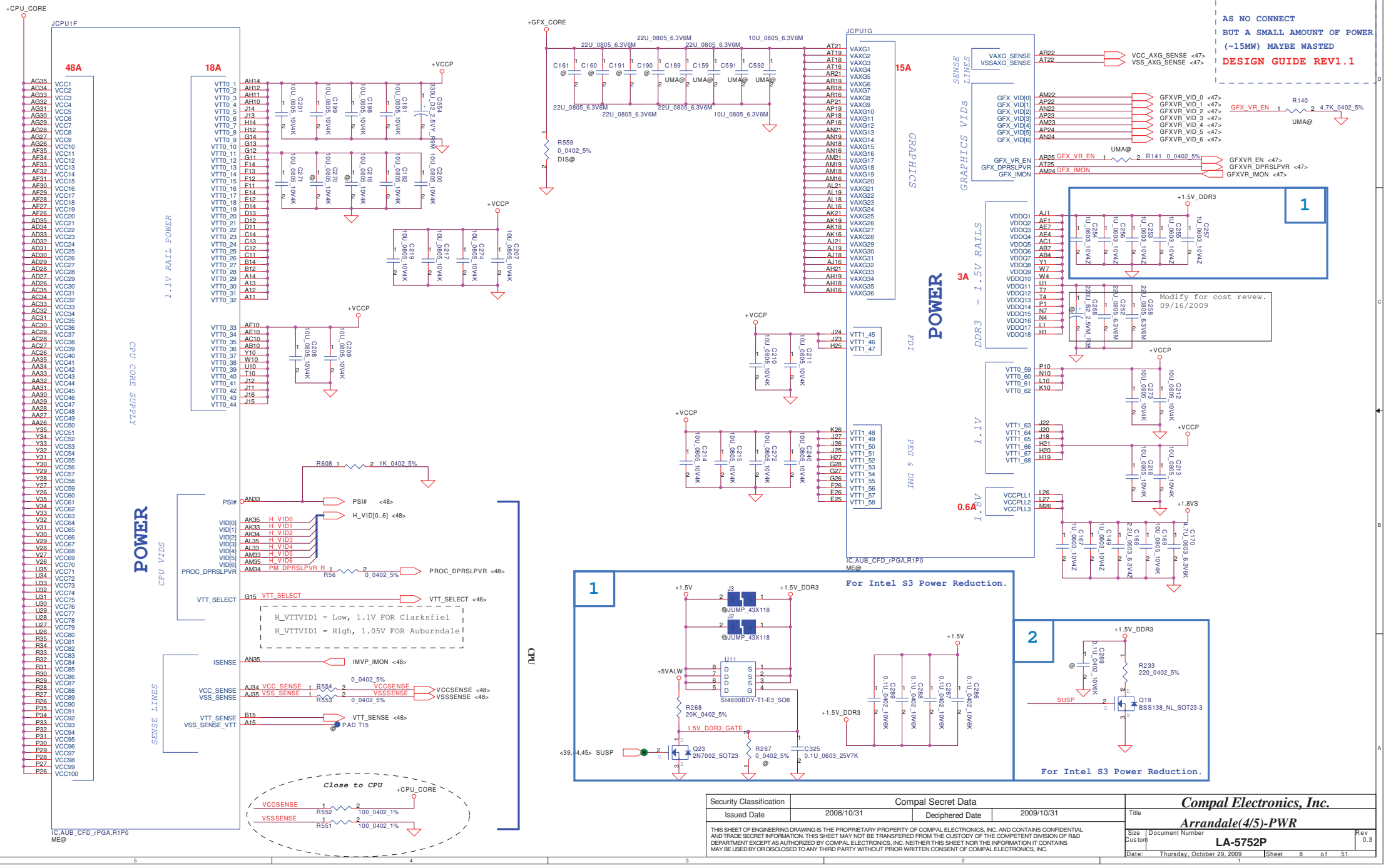
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: *Arrandale(3/5)-DDR III*

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 7 of 51



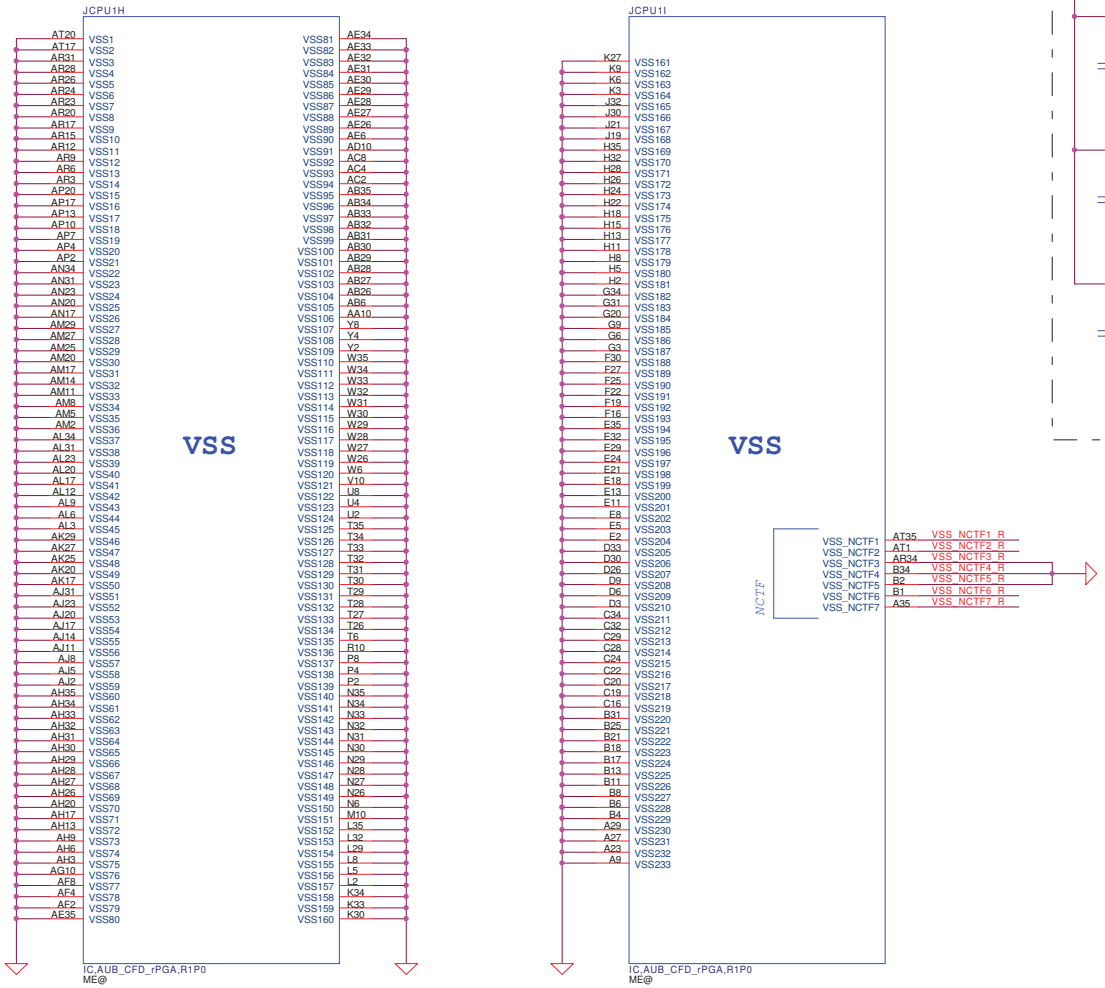
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

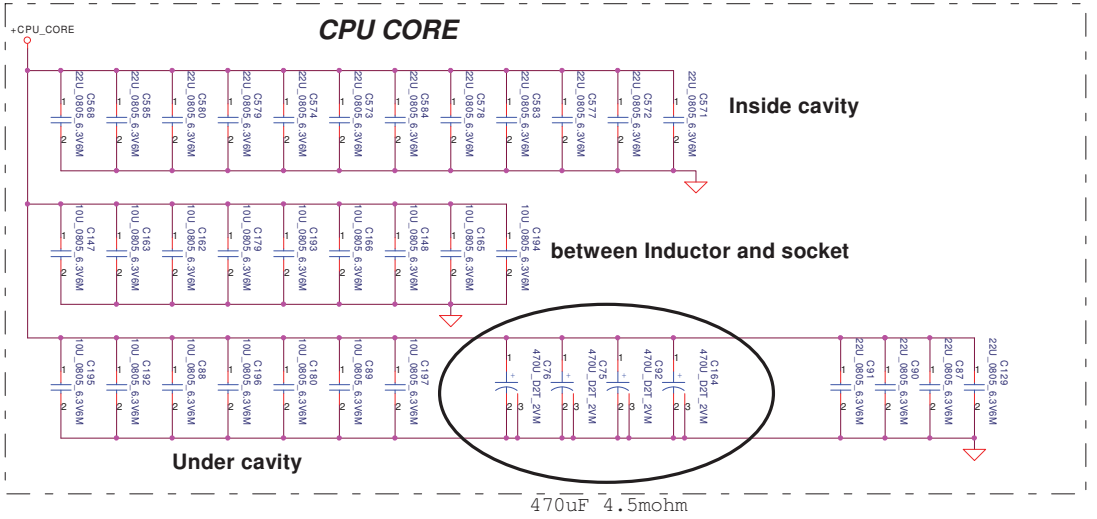
Compal Electronics, Inc.

Title: Arrandale(4/5)-PWR

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 8 of 51





Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: *Arrandale(5/5)-GND/Bypass*

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 9 of 51

DDR3 SO-DIMM A

3A@1.5V

JDIMM1

FOX_AS0A626-U4SN-7F

ME@

<7> DDR_A_D[0..63]
<7> DDR_A_DM[0..7]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

DRAMRST# <5,11>

DDR_CKE1_DIMMA <7>

M_CLK_DDR1 <7>
M_CLK_DDR#1 <7>

DDR_A_BS1 <7>
DDR_A_RAS# <7>

DDR_CS0_DIMMA# <7>
M_ODT0 <7>

M_ODT1 <7>

PM_EXTTS#1_R <5,11>
SMB_DATA_S3 <11,12,14,28>
SMB_CLK_S3 <11,12,14,28>

0.65A@0.75V

R297 1K_0402_1%
R305 1K_0402_1%

For Arranale only +VREF_DQ_DIMMA supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note: Place near DIMM

```
VDDQ(1.5V) =
   3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
   6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
   3*0805 10uf  4*0402 1uf
VREF =
   1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
   1*0402 0.1uf  1*0402 2.2uf
```

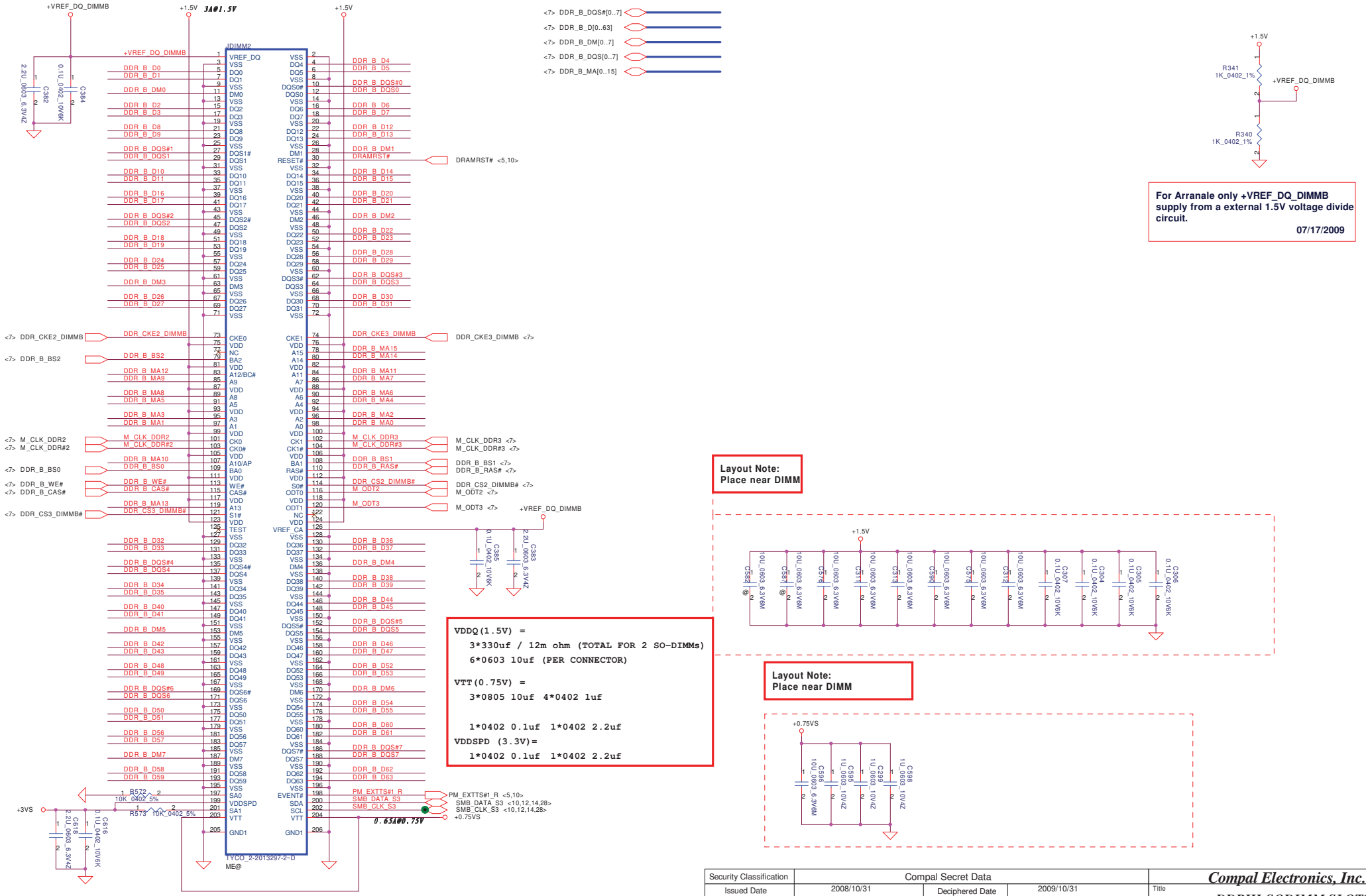
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **LA-5752P** | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 10 of 51



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size	Document Number	Rev
	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 11 of 51

Reserve for Low Power CLK GEN.
RTM890N-632
SLG8LV597VTR

1 PCS CAP(0.1u) BY 1 INPUT PIN

CLK GEN TO PCH
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA
1. 27M_CLK
1. 27M_CLK_SS

CLOSE U27

U14
SLG8SP587VTR_QFN32_5X5

1 PCS CAP(0.1u) BY 1 INPUT PIN

RTM890N-631-GRT QFN 32P CLK GEN (SA00003HQ00)
ICS9LVS3199AKLFT MLF 32P CLK GEN (SA00003HR00)

unstuff 09.09.08

PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199

1 PCS CAP(0.1u) BY 1 INPUT PIN

EMI Capacitor

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

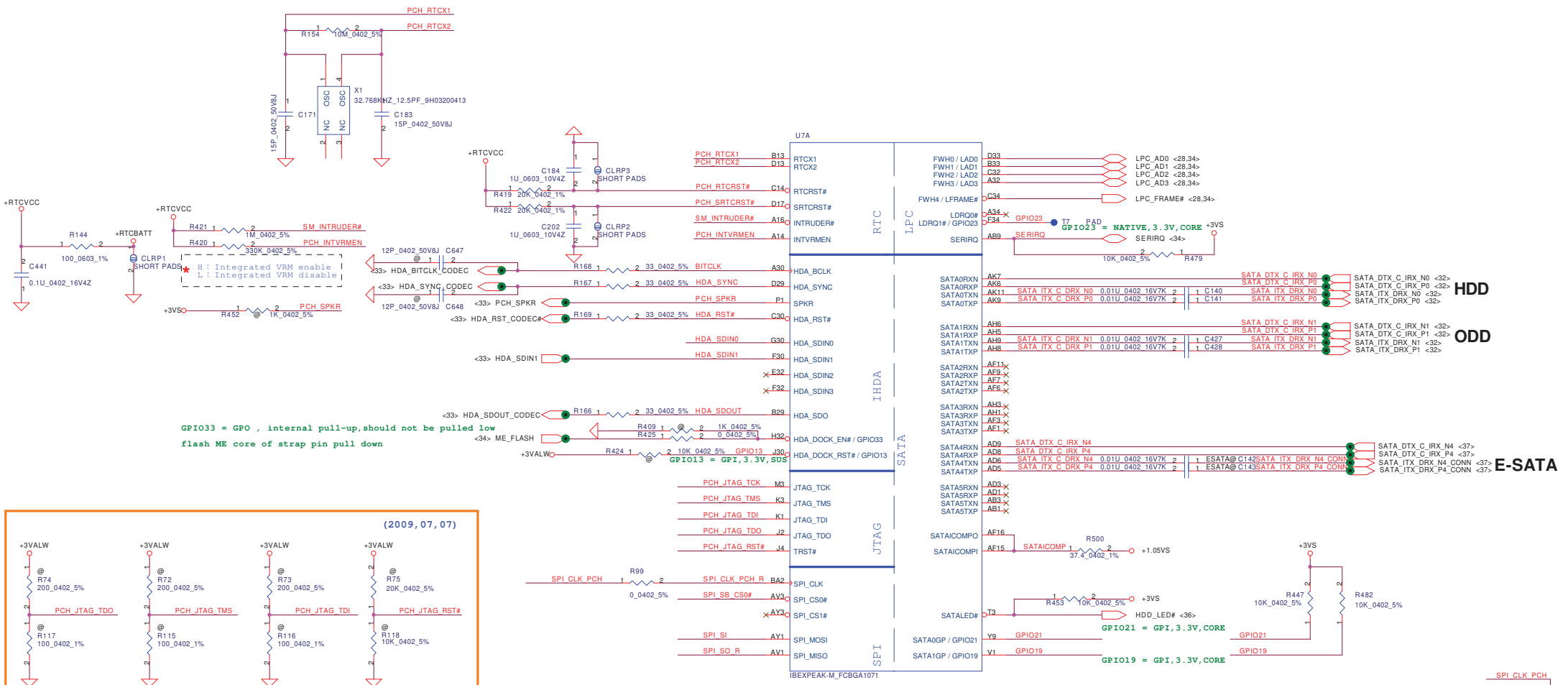
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: CLOCK GENERATOR

Size | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 12 of 51



PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R595	20Kohm	20Kohm	No Install
	R594	10Kohm	10Kohm	No Install

Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

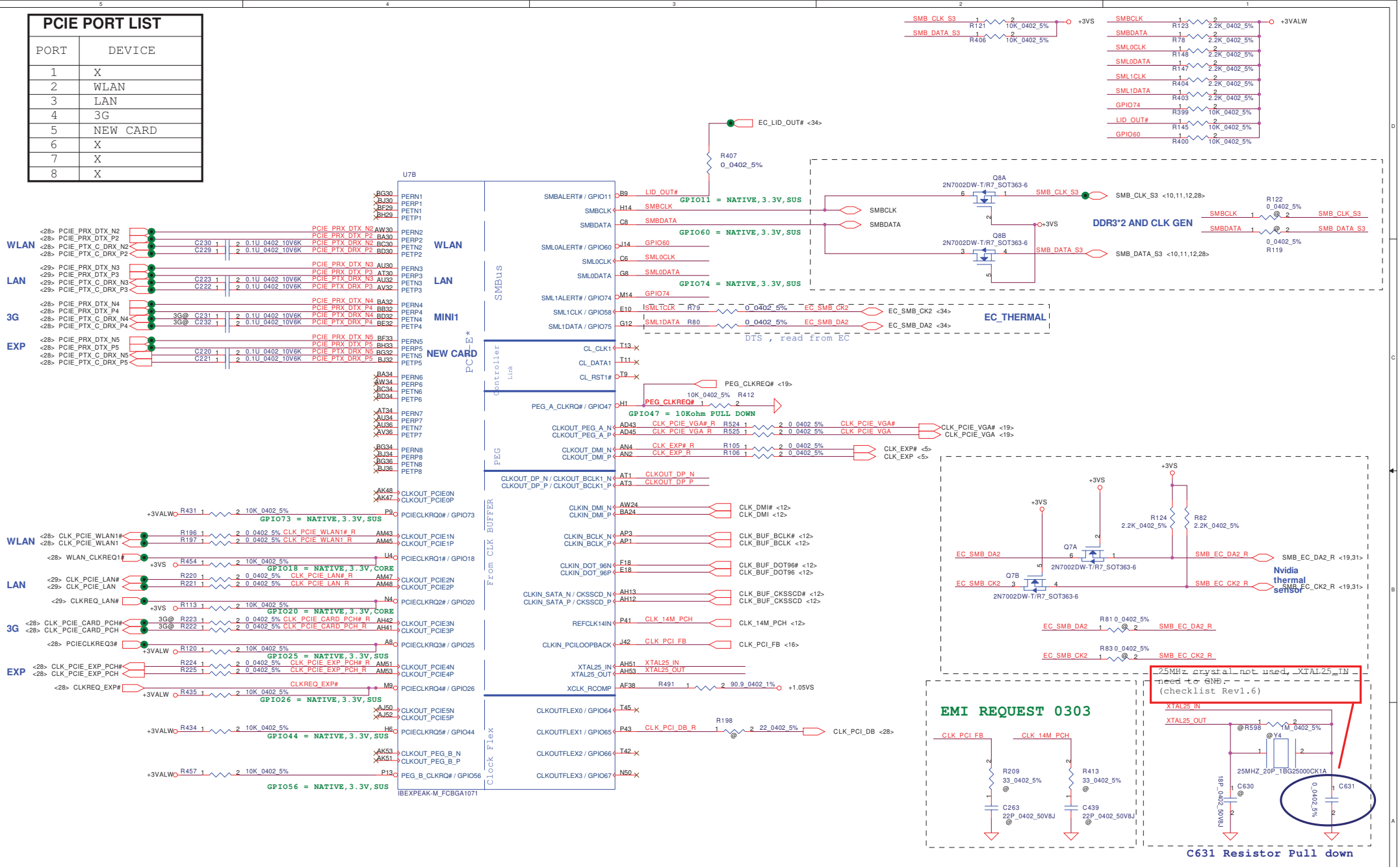
Title: IBEX-M(1/6)-HDA/JTAG/SATA

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 13 of 51

PCIE PORT LIST

PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X



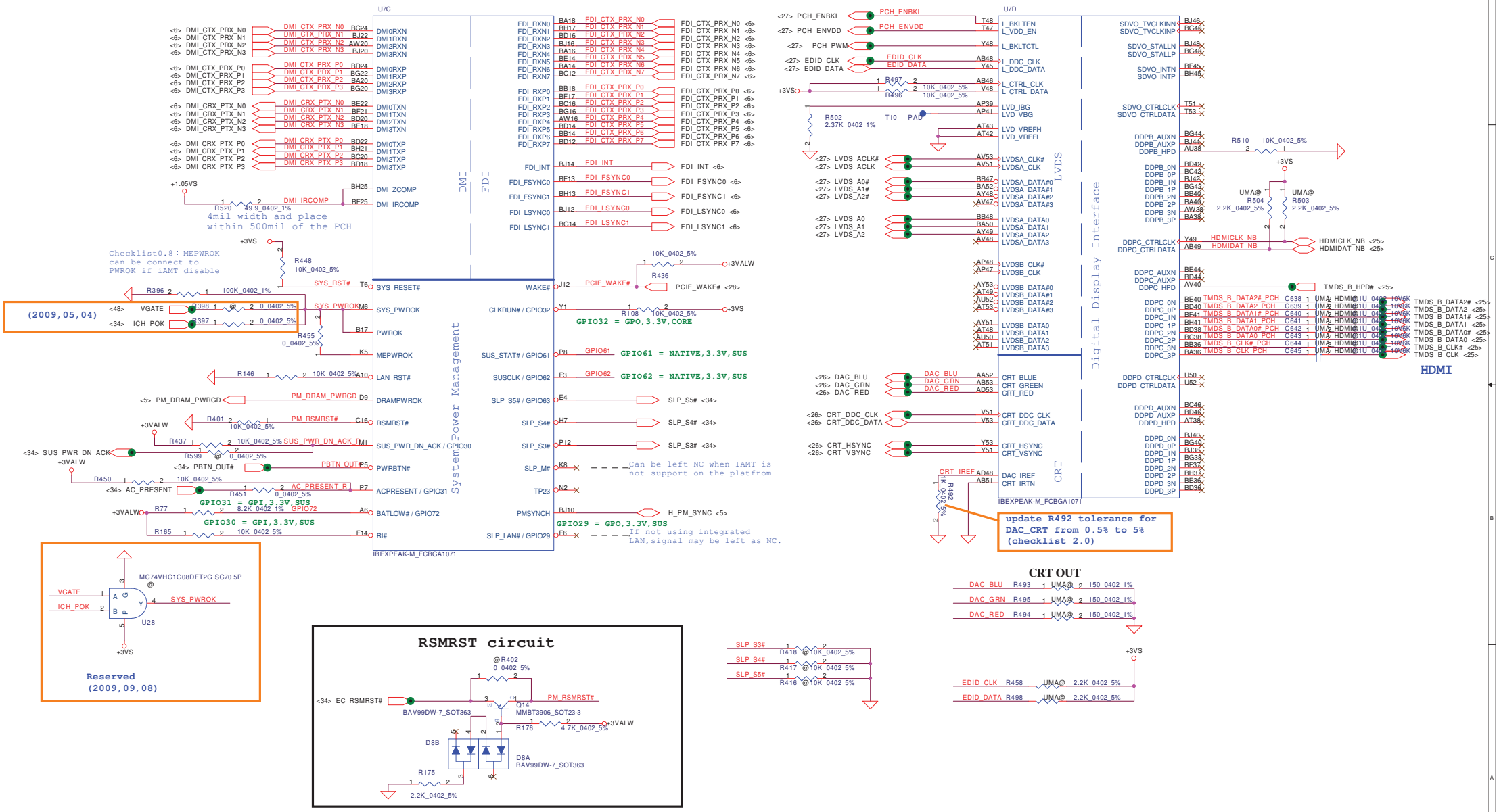
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: IBEX-M(2/6)-PCI-E/SMBUS/CLK

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 14 of 51



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: IBEX-M(3/6)-DMI/GPIO/LVDS

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 15 of 51

U7E

U7F

GPIO8
Weak internal PU, don't PD

Check list Rev0.8 section1.23.2
If not implemented, the
Braidwood
interface signals can be
left as No Connect (NC).

GPIO15
H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality
H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality
it have weak internal PU 20K

GPIO27
Default : Do not connect(floating)
High : Enables the internal VccVRM to have a clean supply for analog rails. no need to use on board filter circuit.

GPIO0 = GPI,3.3V,CORE
GPIO1 = GPI,3.3V,CORE
GPIO6 = GPI,3.3V,CORE
GPIO7 = GPI,3.3V,CORE
GPIO8 = GPO,3.3V,SUS
GPIO12 = GPI,3.3V,SUS

GPIO18 = NATIVE,5V,CORE
GPIO52 = NATIVE,5V,CORE
GPIO54 = NATIVE,5V,CORE

GPIO2 = GPI,5V,CORE
GPIO3 = GPI,5V,CORE
GPIO4 = GPI,5V,CORE
GPIO5 = GPI,5V,CORE

GNT2
Default-Internal pull up
Low=Configures DMI for ESI compatible operation(for servers only.Not for mobile/desktops)

LEFT USB
LEFT USB (COMBO)
USB Camera
RIGHT USB
CARD READER
WLAN
EXPRESS
Bluetooth
3G CARD

checklist 2.0 update 2009.09.16

within 500mil

Within 500 mils minimum spacing to other signal is 15mil

Boot BIOS Strap		
PCI_GNT0#	PCI_GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	PCI
1	1	SPI

Intel Anti-Theft Techonlogy
NV_ALE: High=Enabled; Low=Disable(floating)

DMI Termination Voltage
NV_CLE: Set to Vcc when HIGH; Set to Vss when LOW
Weak internal PU,Do not pull low

NV_ALE
Enable Intel Anti-Theft Technology : 8.2K PU to +3VS
Disable Intel Anti-Theft Technology : floating(internal PD)
NV_CLE
DMI termination voltage. weak internal PU, don't PD

A16 swap overide Strap/Top-Block Swap Override jumper

PCI_GNT3#	
	Low=A16 swap override/Top-Block Swap Override enabled
	High=Default

MC74VHC1G08DFT2G SC70_5P

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

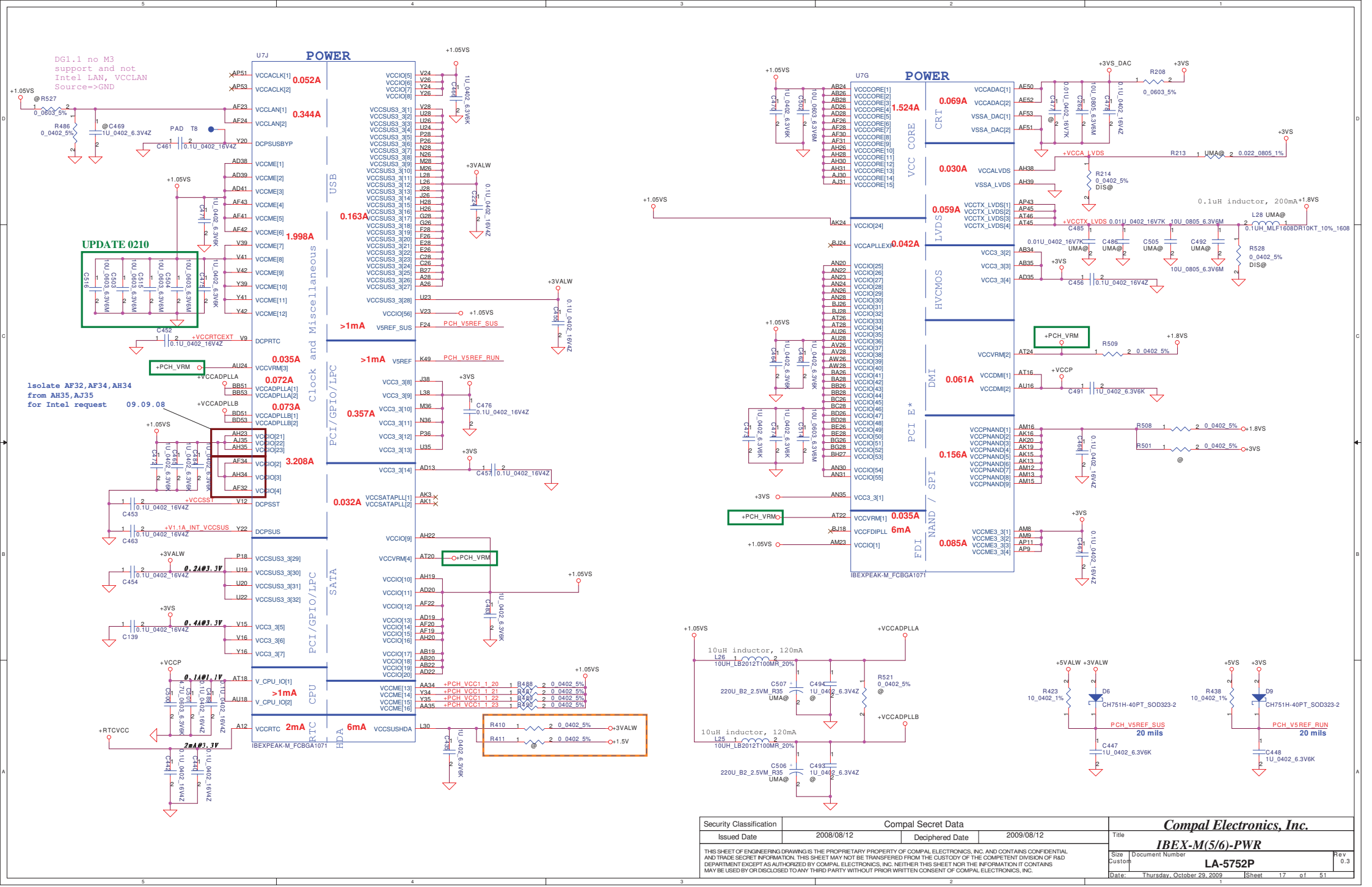
Security Classification	Compal Secret Data		
Issued Date	2008/08/12	Deciphered Date	2009/08/12

Compal Electronics, Inc.

Title: IBEX-M(4/6)-PCI/USB/RSVD

Size: Custom | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 16 of 51



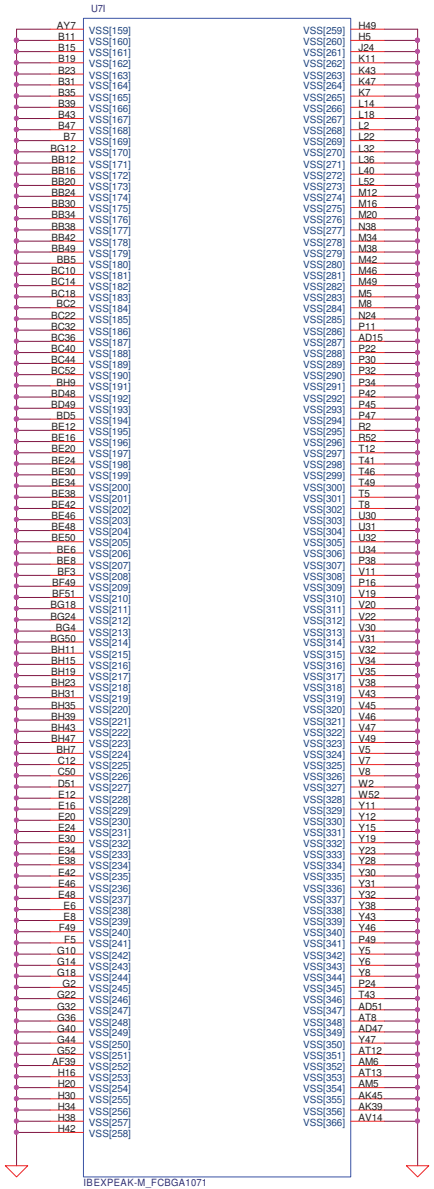
Security Classification	Compal Secret Data		
Issued Date	2008/08/12	Deciphered Date	2009/08/12

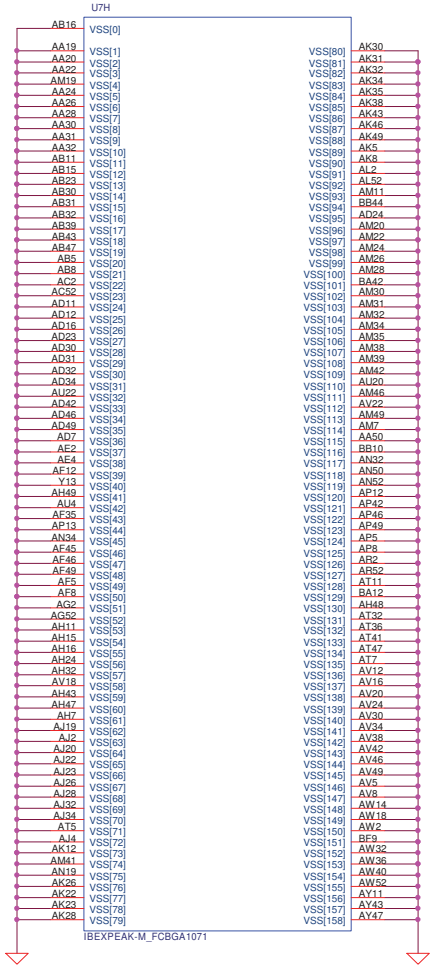
Compal Electronics, Inc.

Title: **IBEX-M(5/6)-PWR**

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 17 of 51





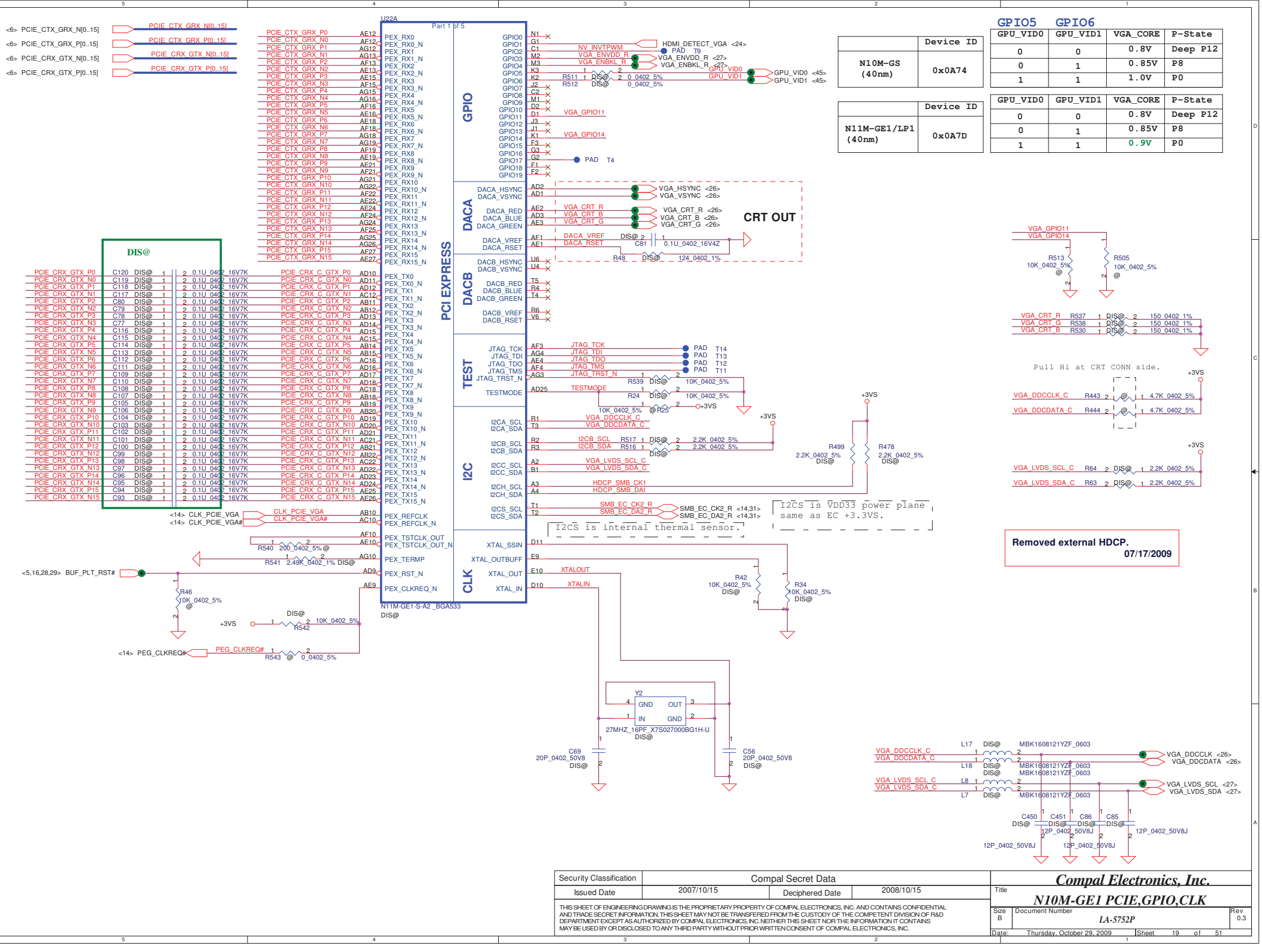
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **IBEX-M(6/6)-GND**

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 18 of 51



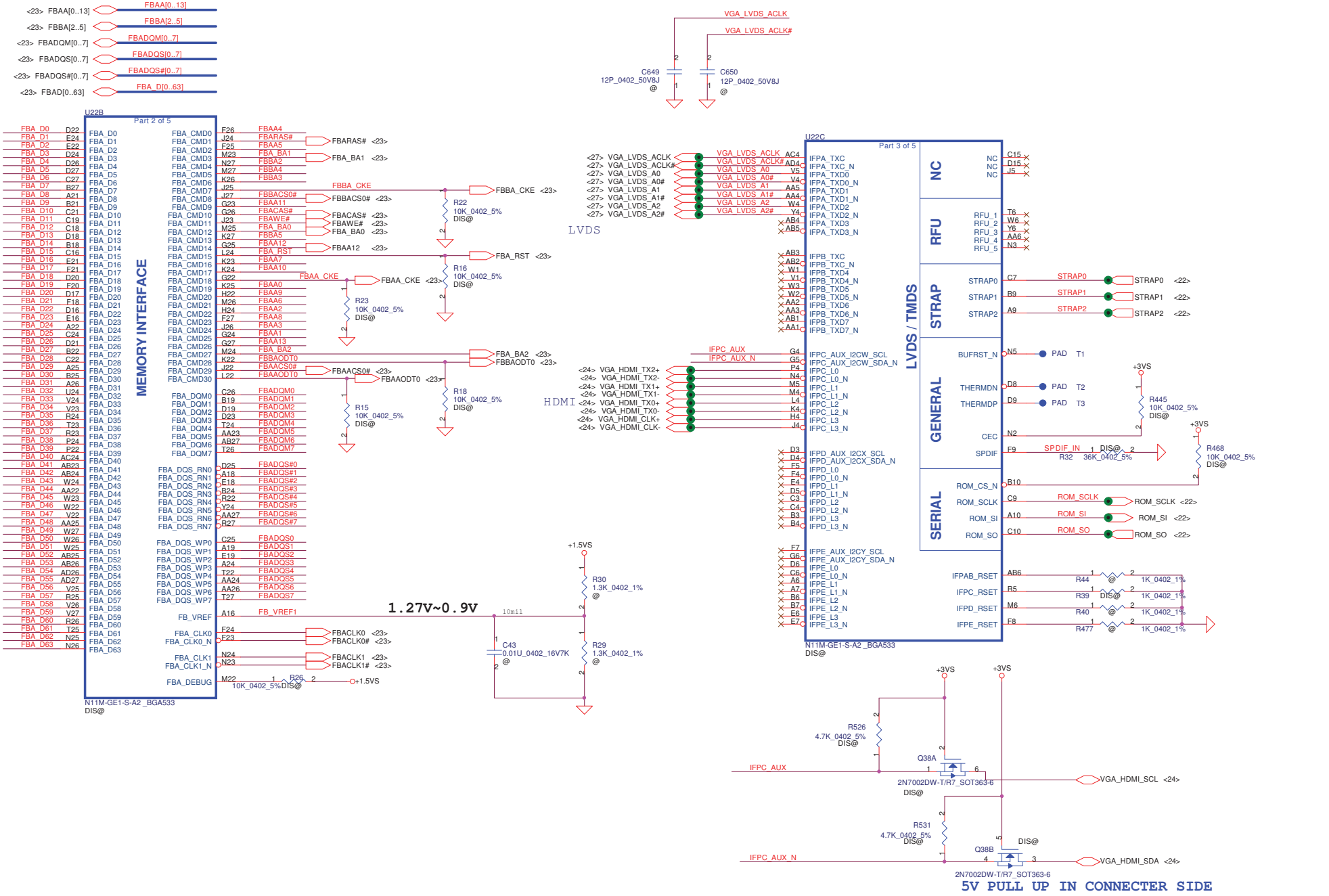
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: N10M-GE1 PCIE,GPIO,CLK

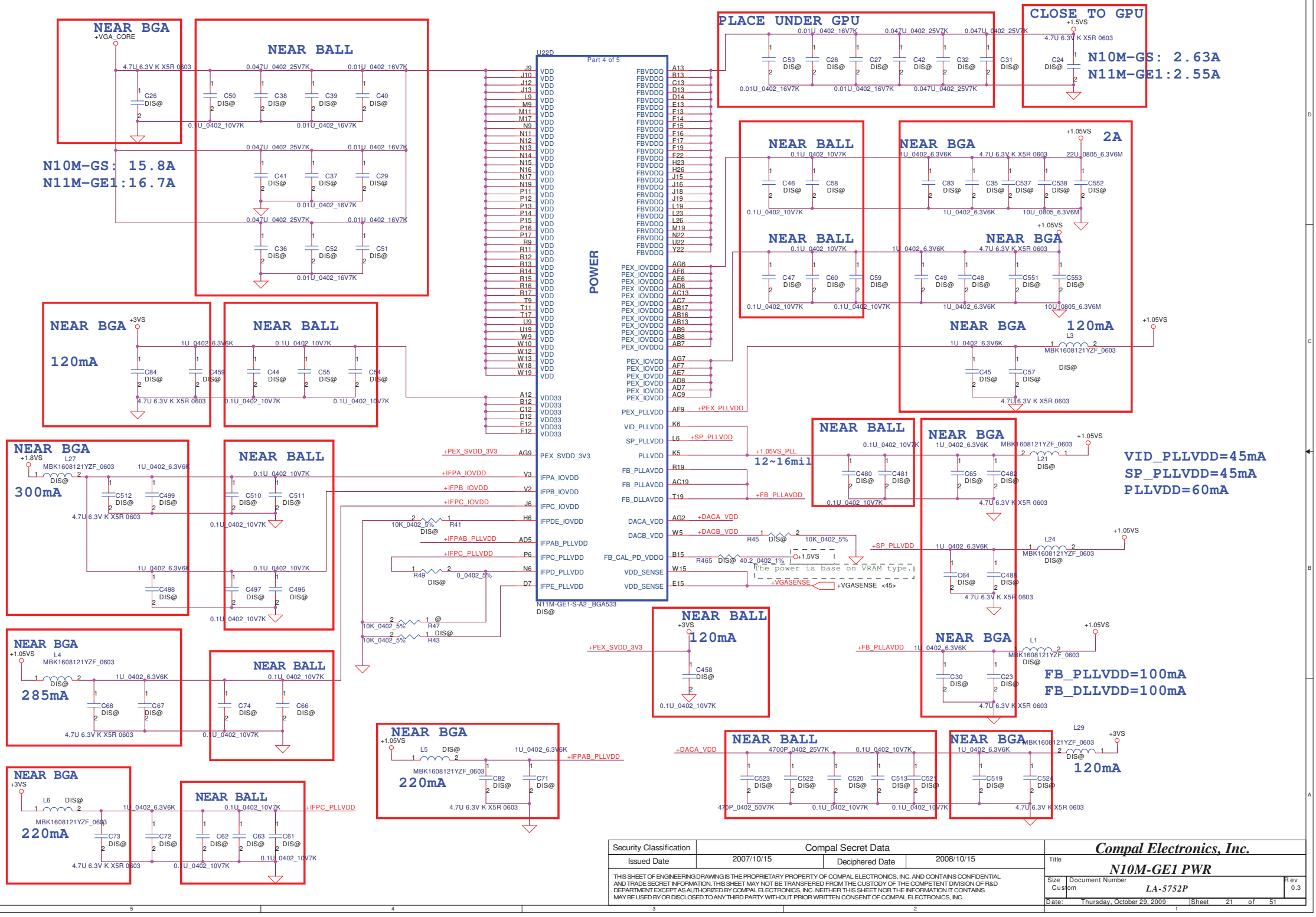
Size	Document Number	Rev
B	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 19 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: N10M-GE1 LVDS,Memory Bus			
Size: B	Document Number: LA-5752P		Rev: 0.3
Date: Thursday, October 29, 2009	Sheet 20 of 51		



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

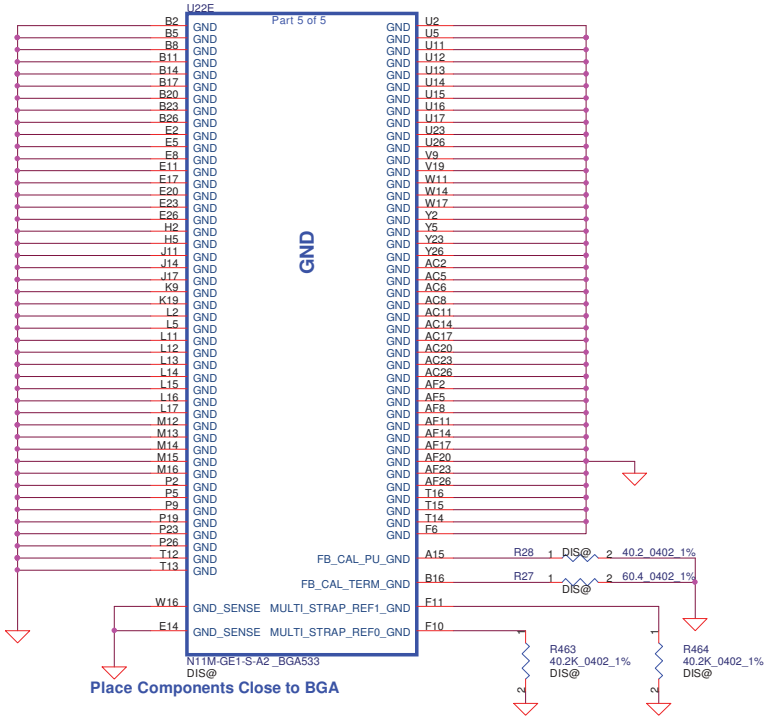
Compal Electronics, Inc.

Title: **N10M-GE1 PWR**

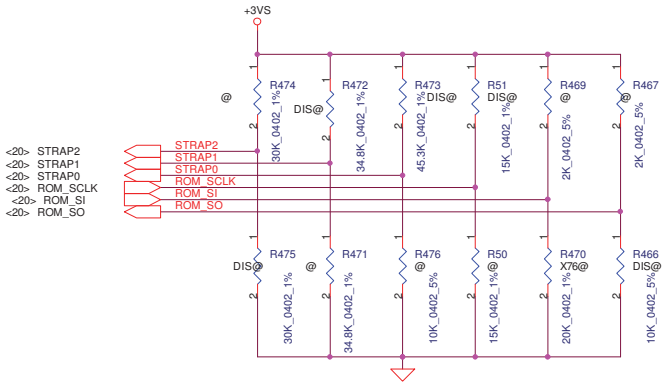
Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 21 of 51

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available



Place Components Close to BGA



STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (defaul)	K4W1G1646E-HC12						
		64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C						
		64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
					X76			

N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resister for driver calibration

DG-04642-001-V01(May 22, 2009)

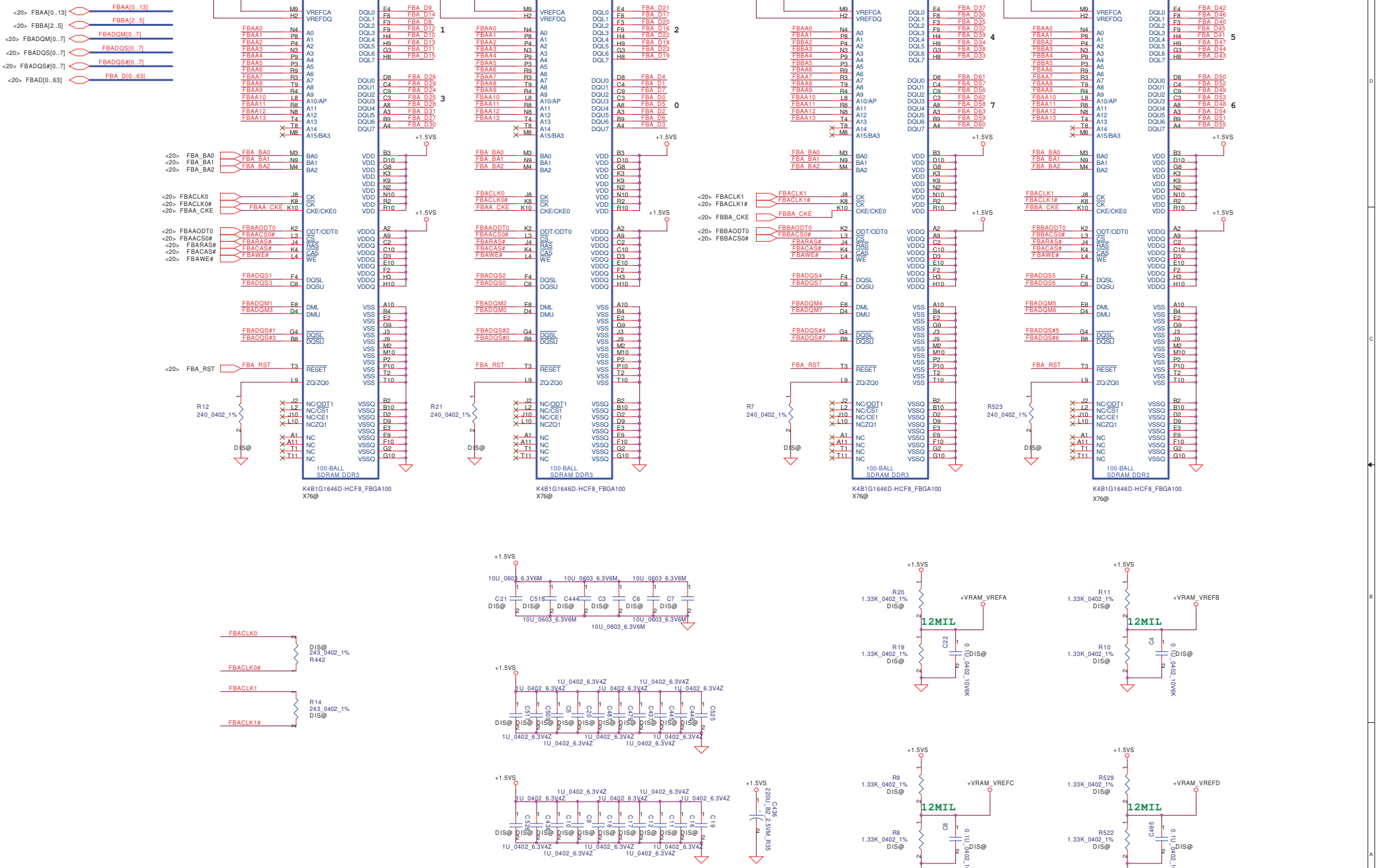
Compal Electronics, Inc.

Title: N10M-GE1 GND & STRAP

Size: B | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 22 of 51

N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



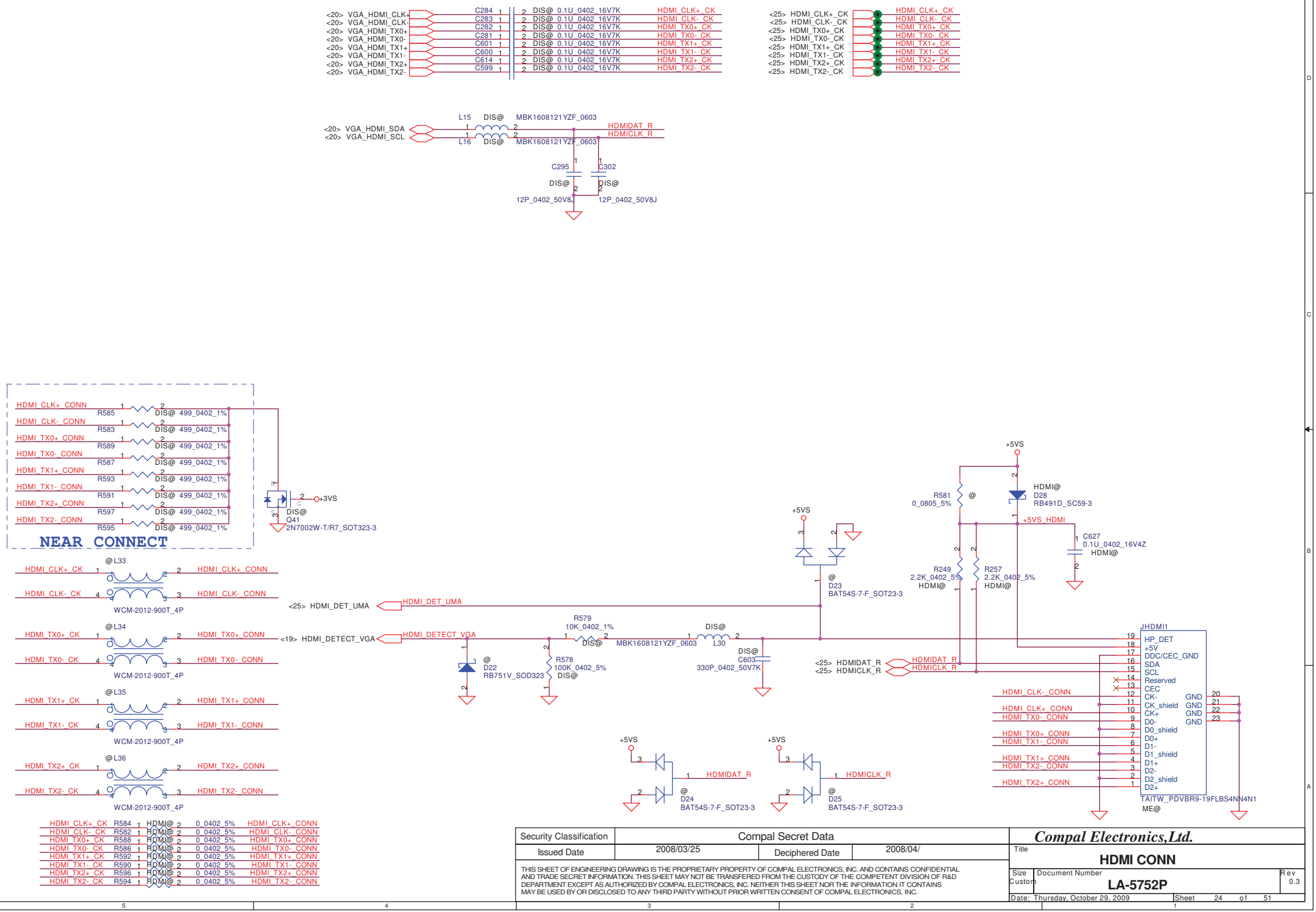
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **VRAM DDR3**

Size	Document Number	Rev
C	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 23 of 51



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
Custom	LA-5752P	0.3

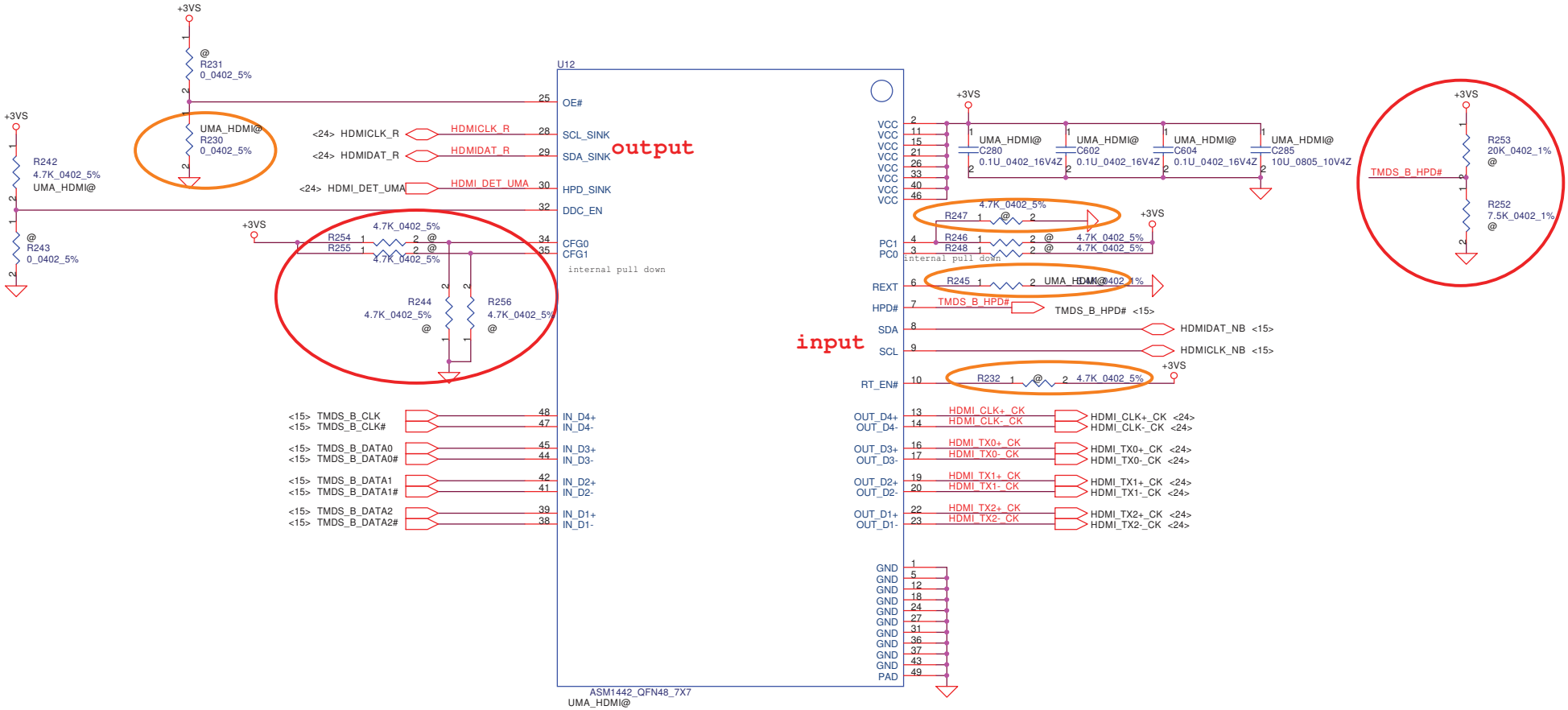
Date: Thursday, October 29, 2009 | Sheet 24 of 51

P/N:SA00003GT00 (ASM1442)

FOR asmedia R428 STUFF
RESERVE THE R668 PULL UP TO 3VS
RESERVE THE R670 PULL DOWN TO GND
CHANGE R483 FROM 499 TO 3.4K OHM

P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

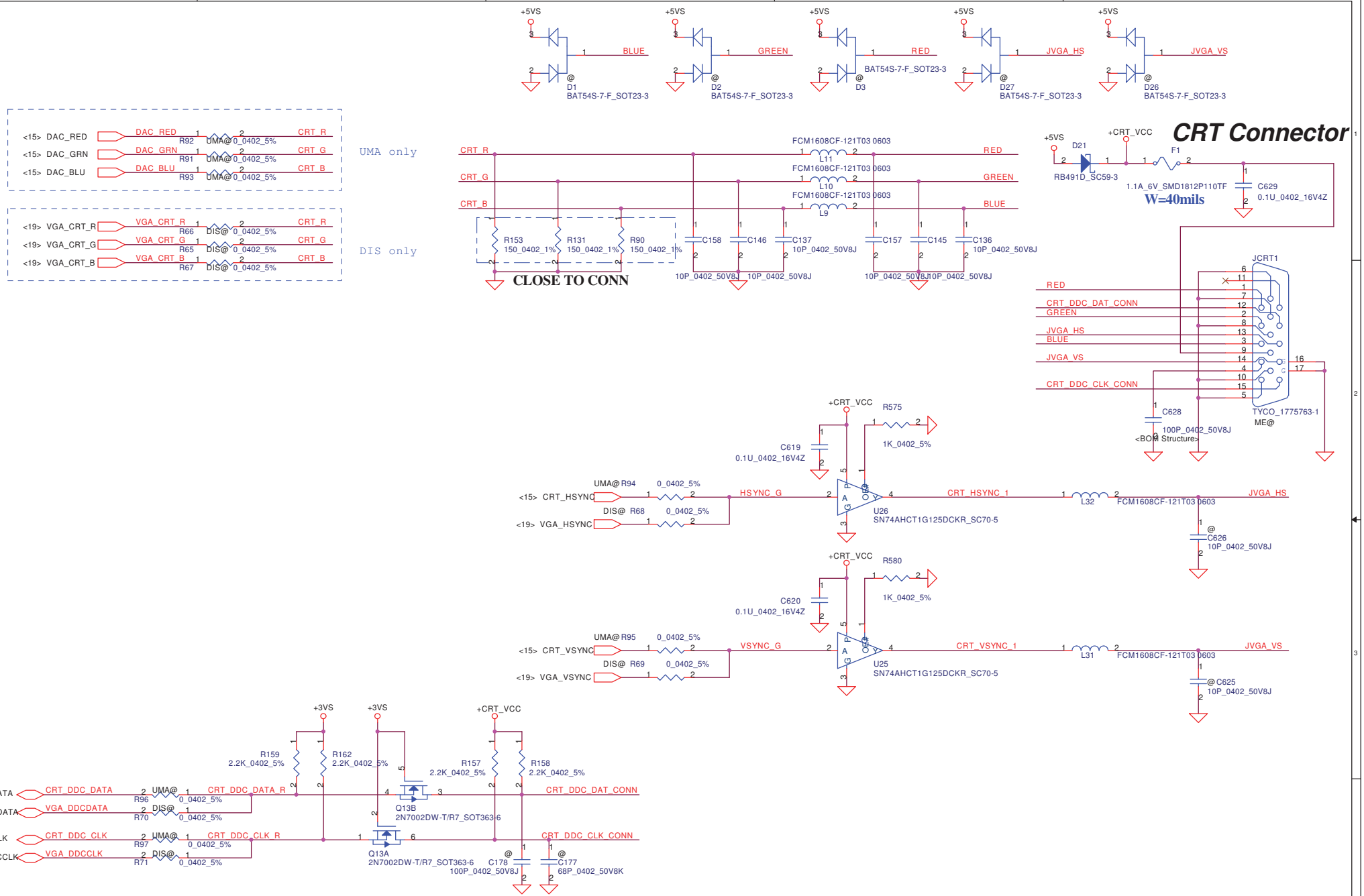
Compal Electronics,Ltd.

Title: Level Shiftter_ASM1442

Size: Custom | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 25 of 51

CRT Connector



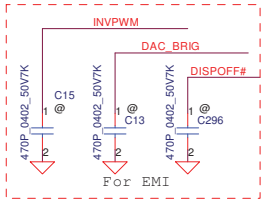
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

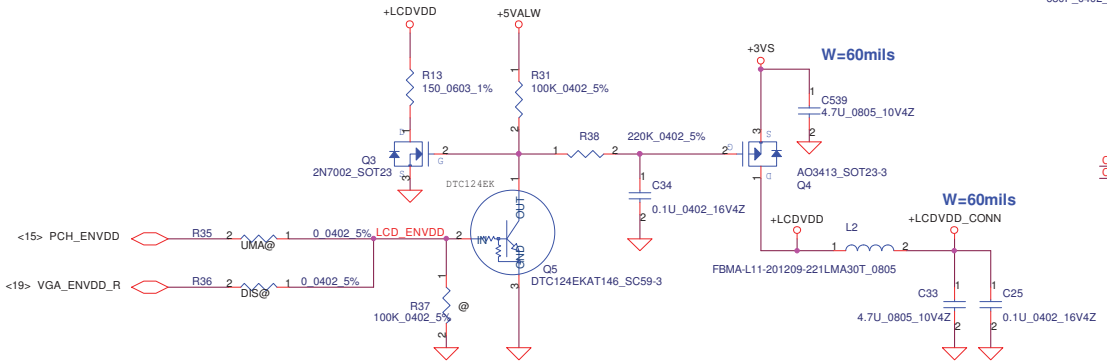
Title: **CRT Connector**

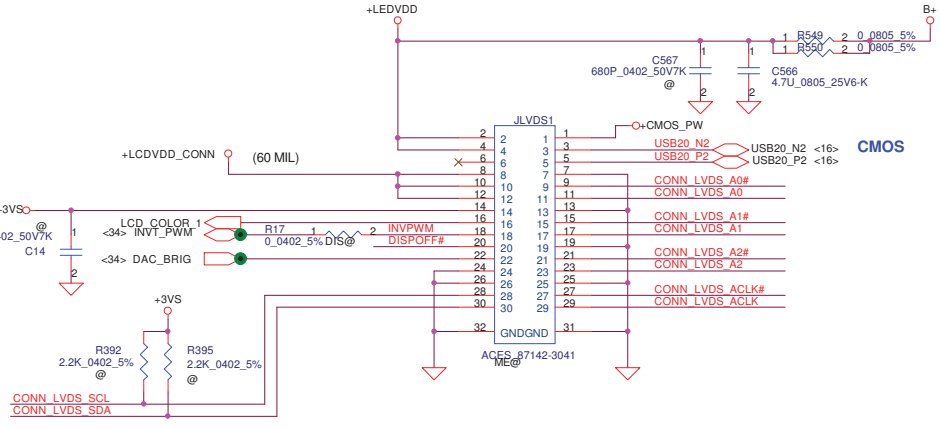
Size	Document Number	Rev
Custom	LA-5752P	0.3

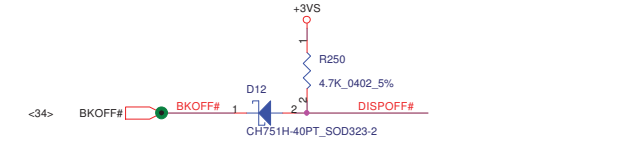
Date: Thursday, October 29, 2009 | Sheet 26 of 51

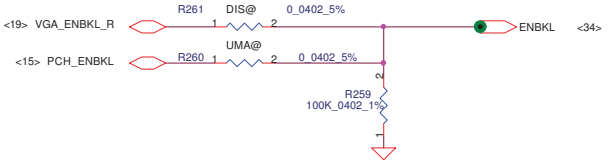


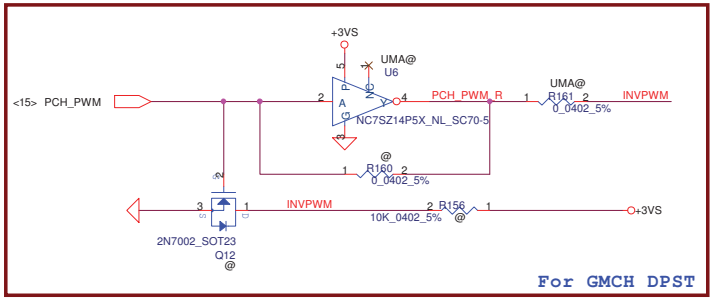
LCD POWER CIRCUIT

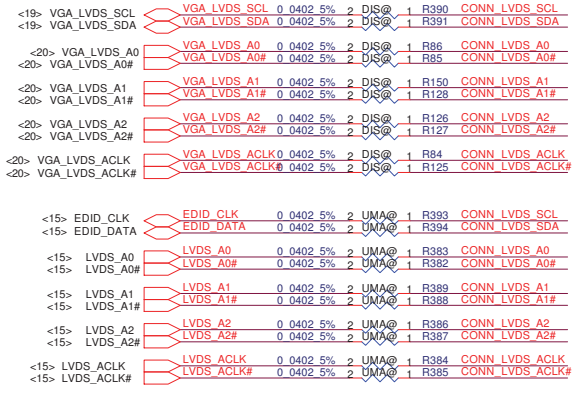




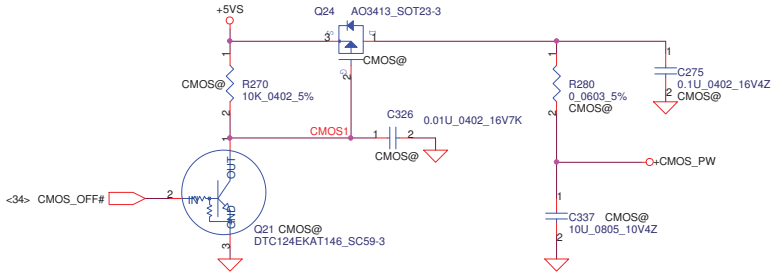








CMOS Camera

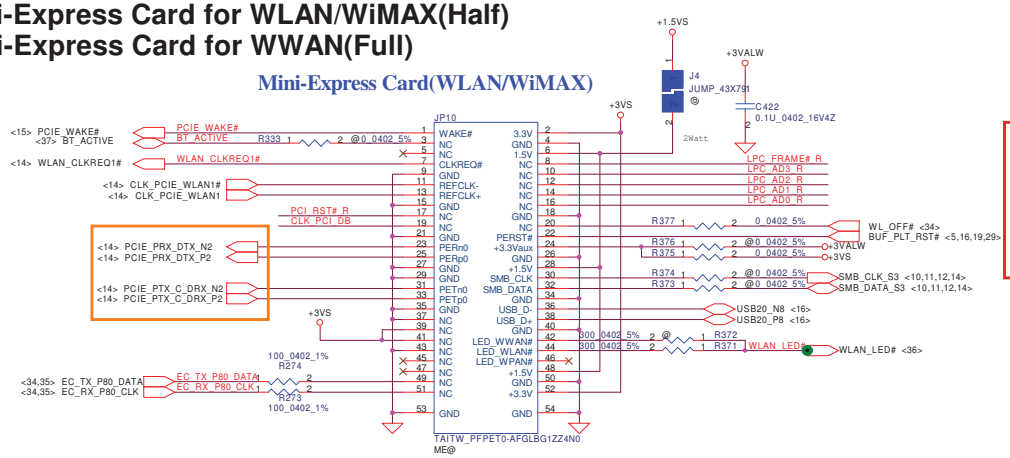


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

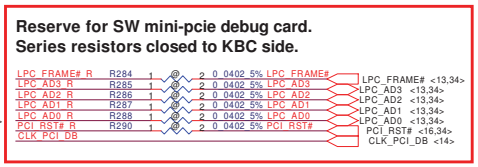
Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: B	Document Number: LA-5752P		Rev: 0.3
Date: Thursday, October 29, 2009		Sheet 27 of 51	

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for WWAN(Full)

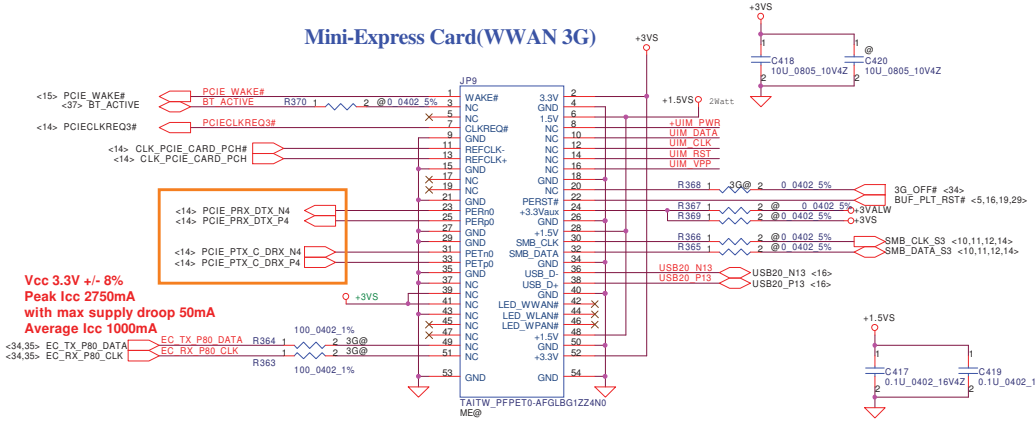
Mini-Express Card(WLAN/WiMAX)



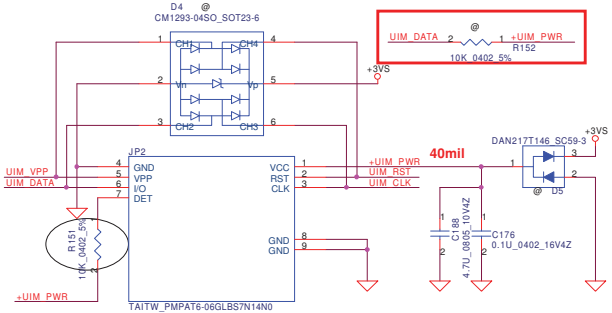
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



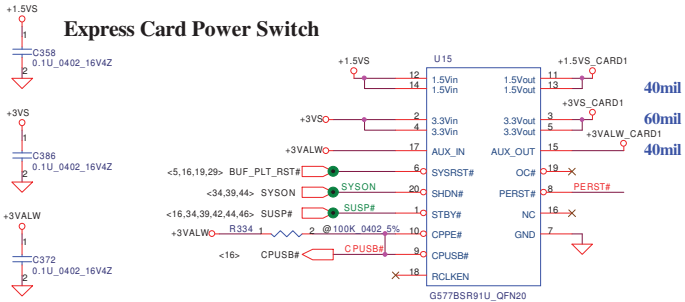
Mini-Express Card(WWAN 3G)

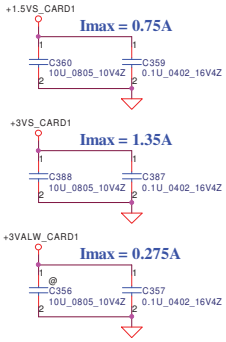


Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

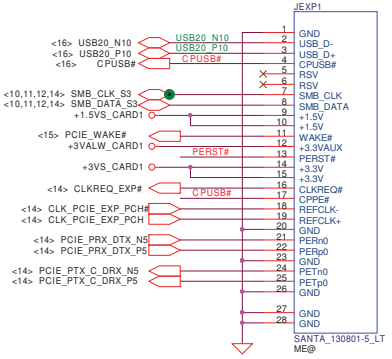


Express Card Power Switch





New Card 34mm Socket (Left/TOP)



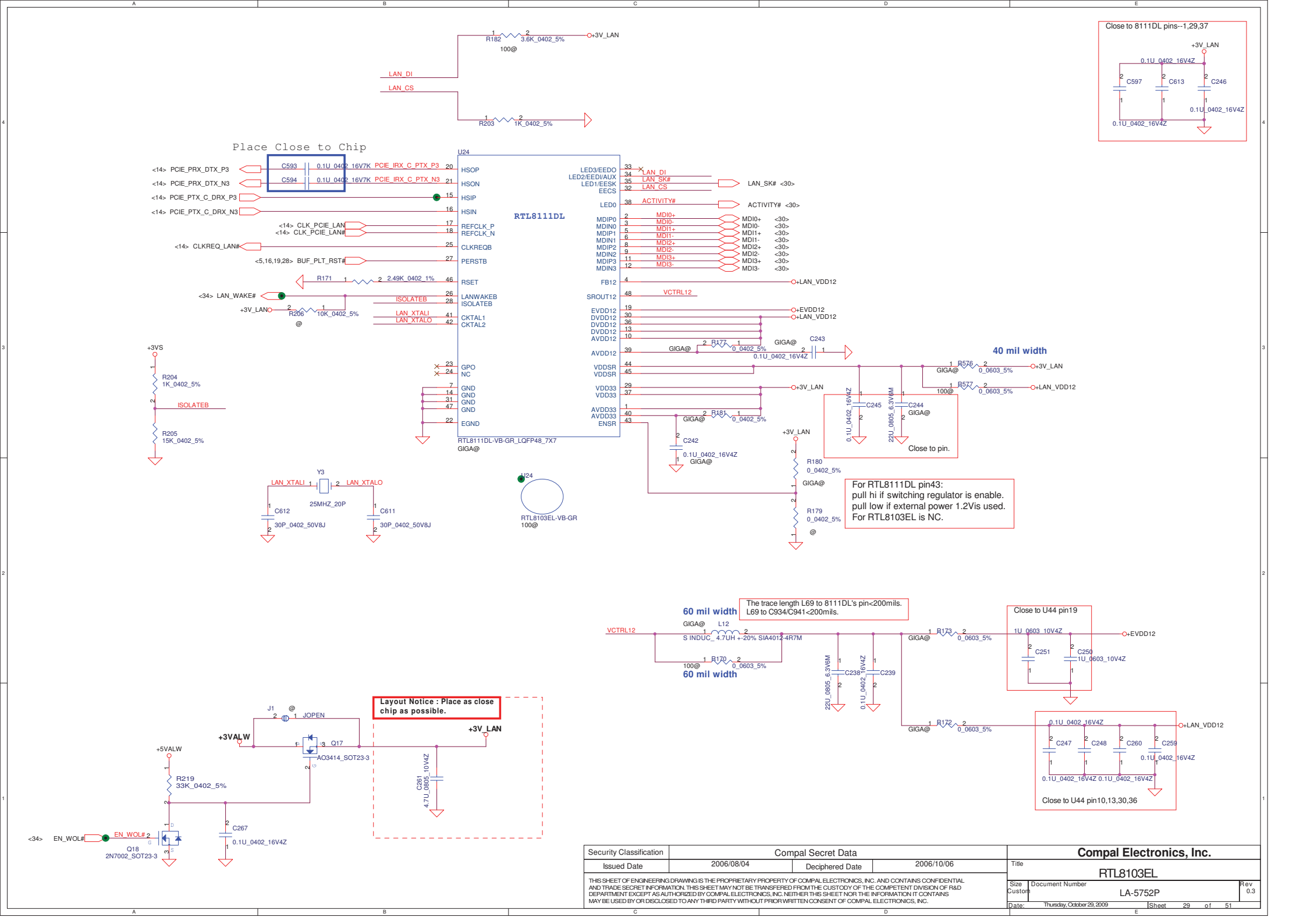
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: *Mini-Card/Nwe Card/SIM*

Size	Document Number	Rev
	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 28 of 51



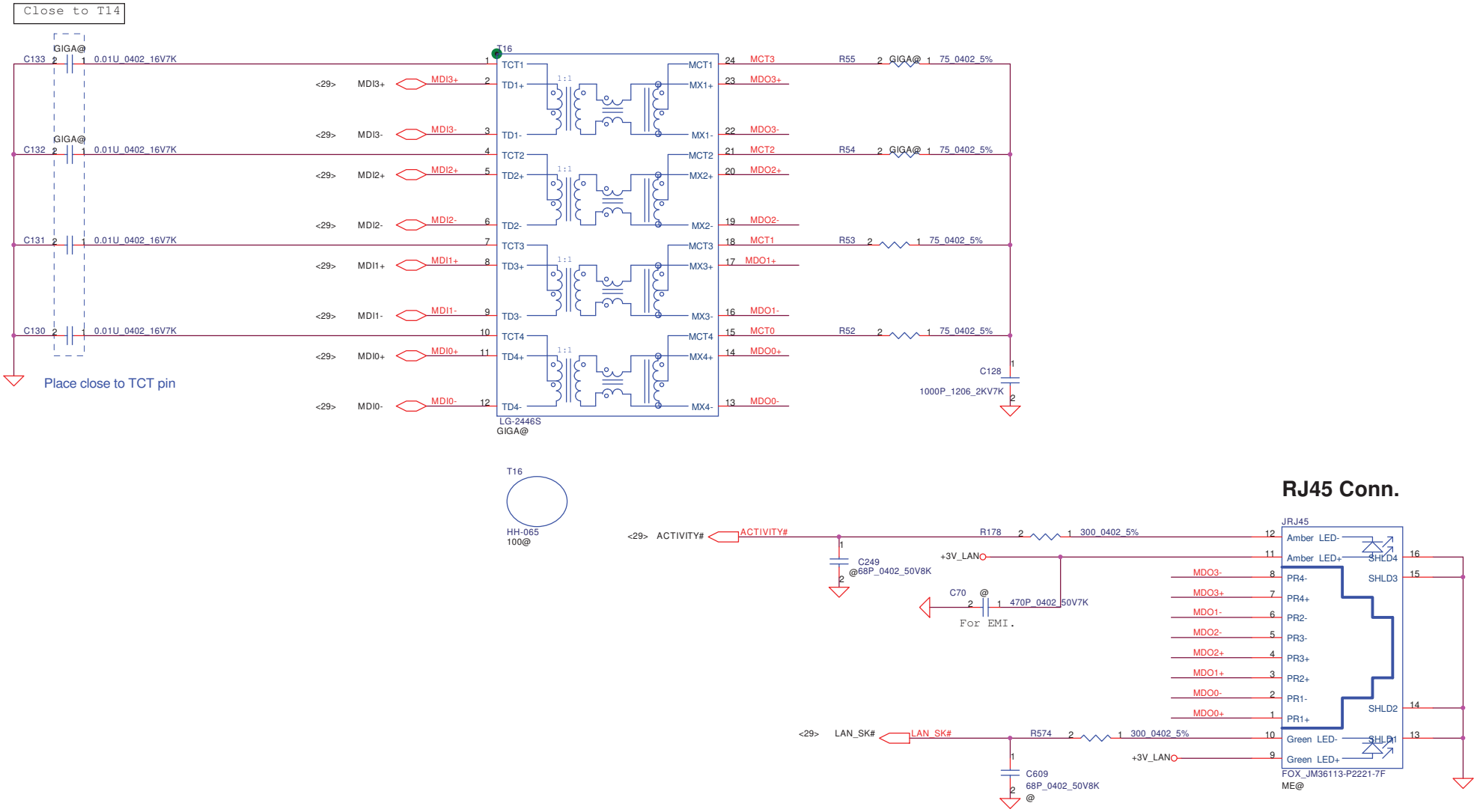
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: RTL8103EL

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 29 of 51

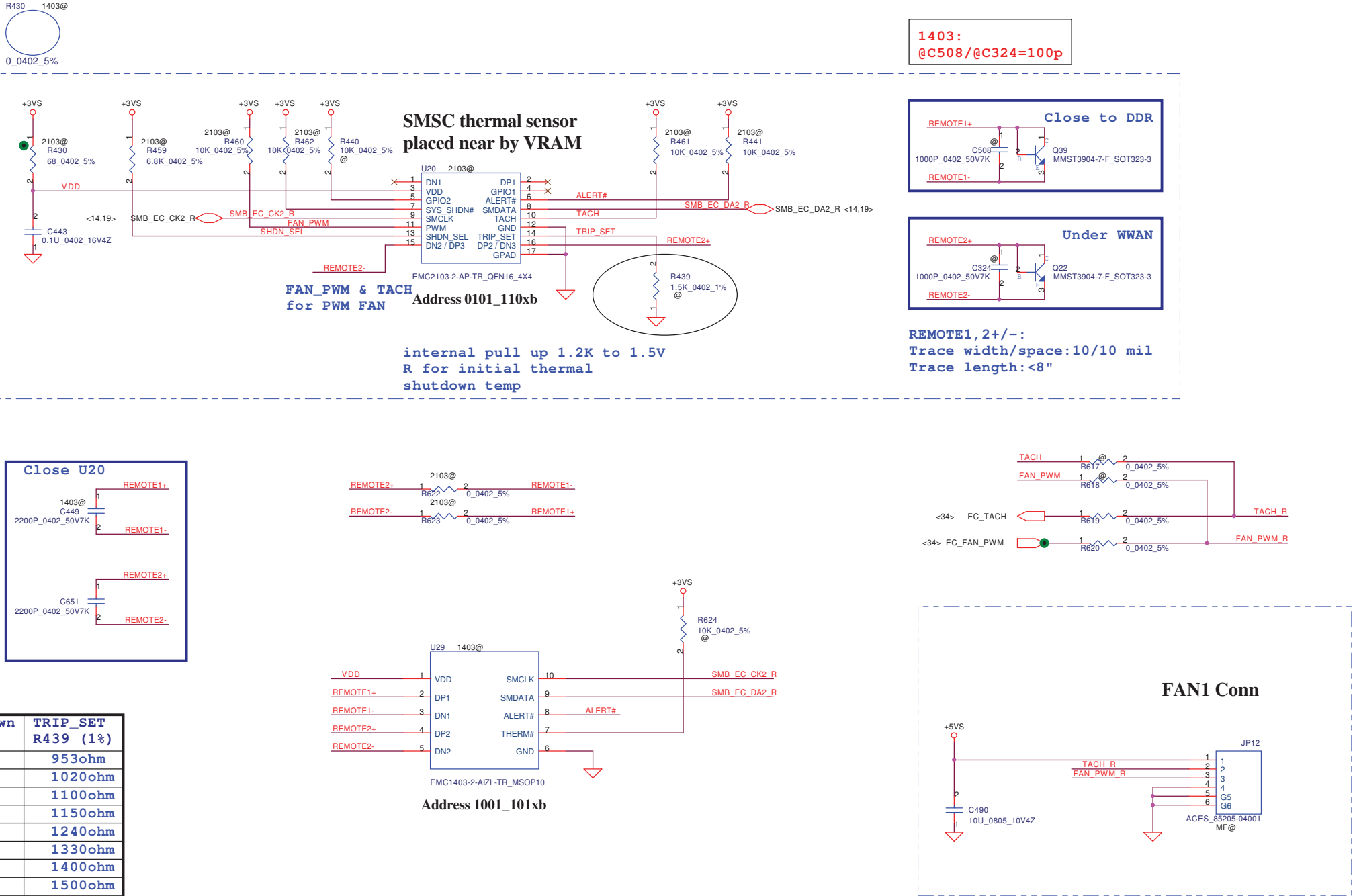


Compal Electronics, Inc.

Title: **LAN_Transformer**

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 30 of 51



Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

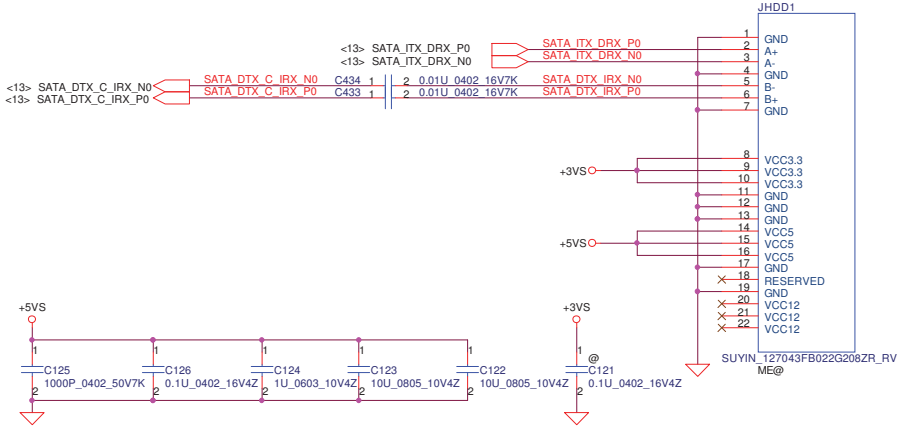
Compal Electronics,Ltd.

Title: EMC2103/1403_Thermal sensor/FAN

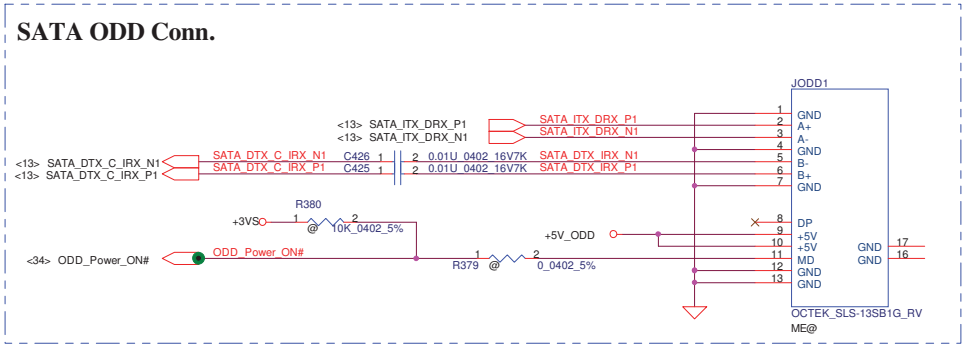
Size: Custom | Document Number: LA-5752P | Rev: 0.3

Date: Thursday, October 29, 2009 | Sheet 31 of 51

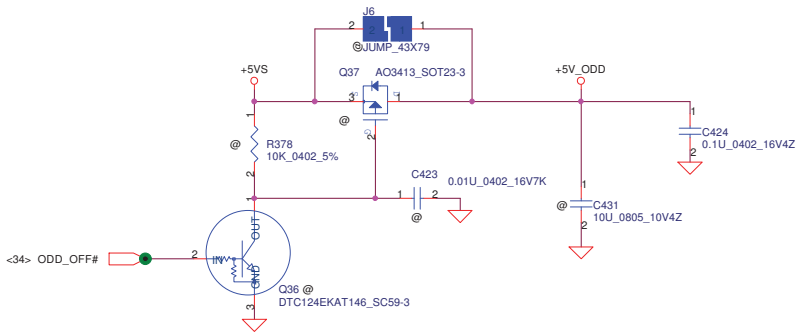
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

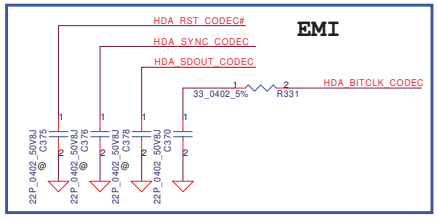
Compal Electronics, Inc.

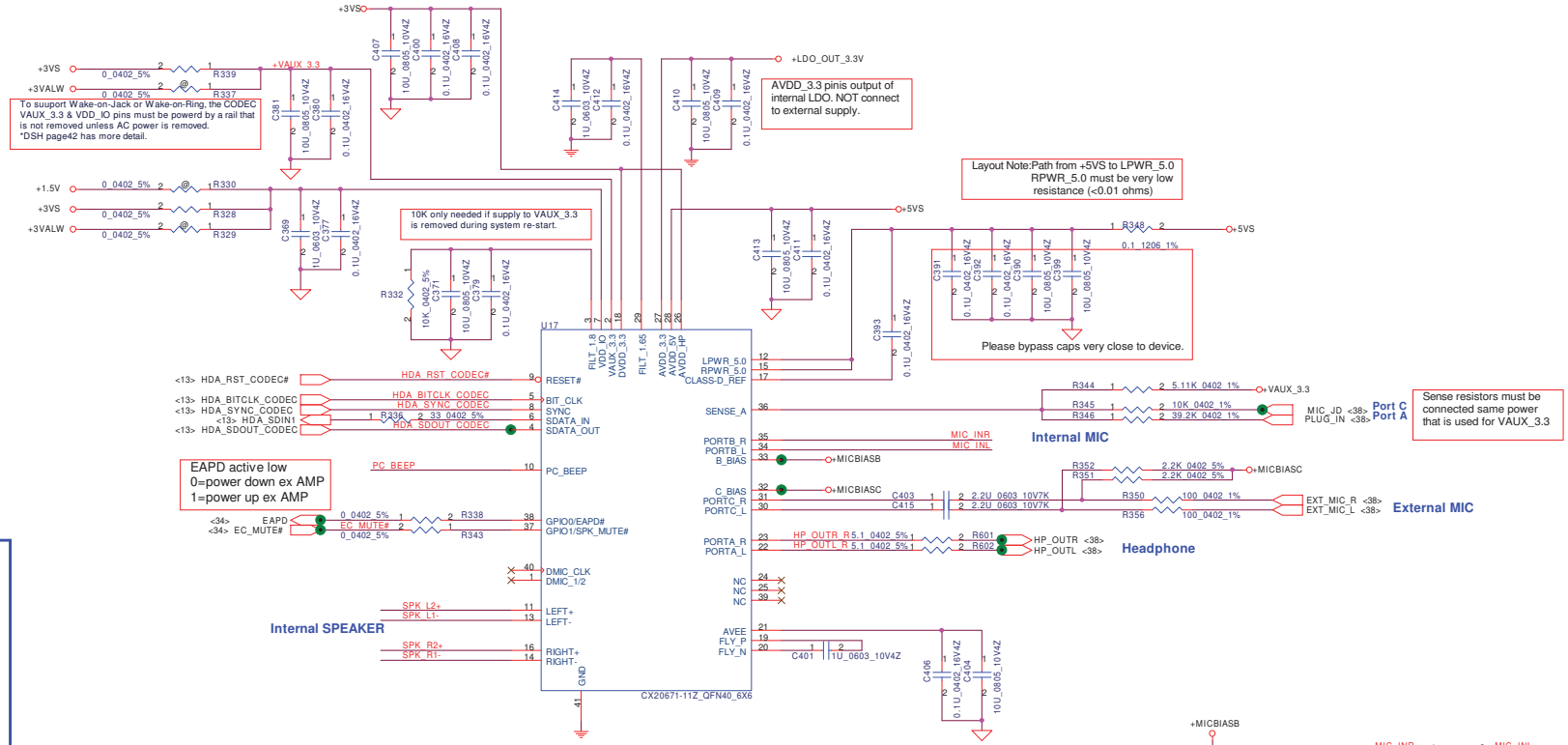
Title: *HDD/ODD Connector*

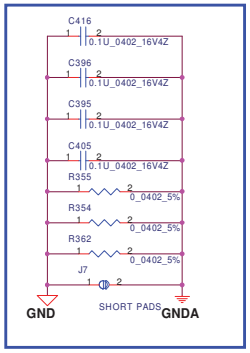
Size	Document Number	Rev
B	LA-5752P	0.3

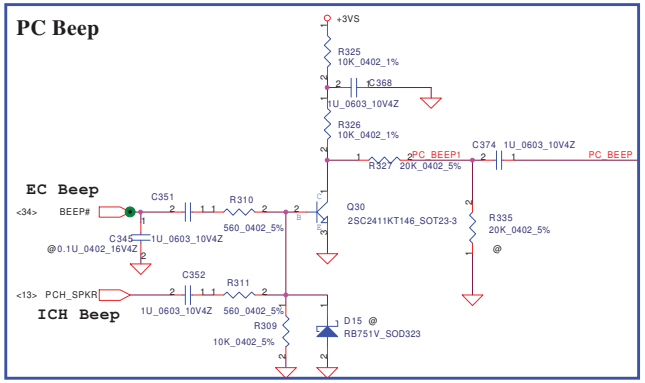
Date: Thursday, October 29, 2009 | Sheet 32 of 51

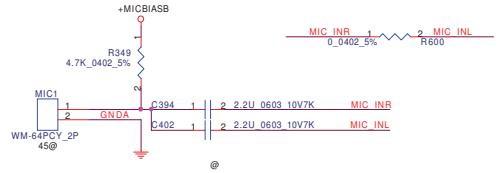
CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



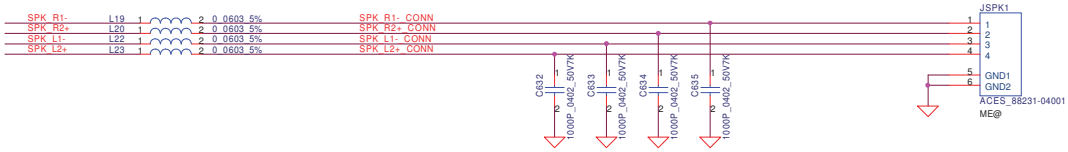








wide 20MIL



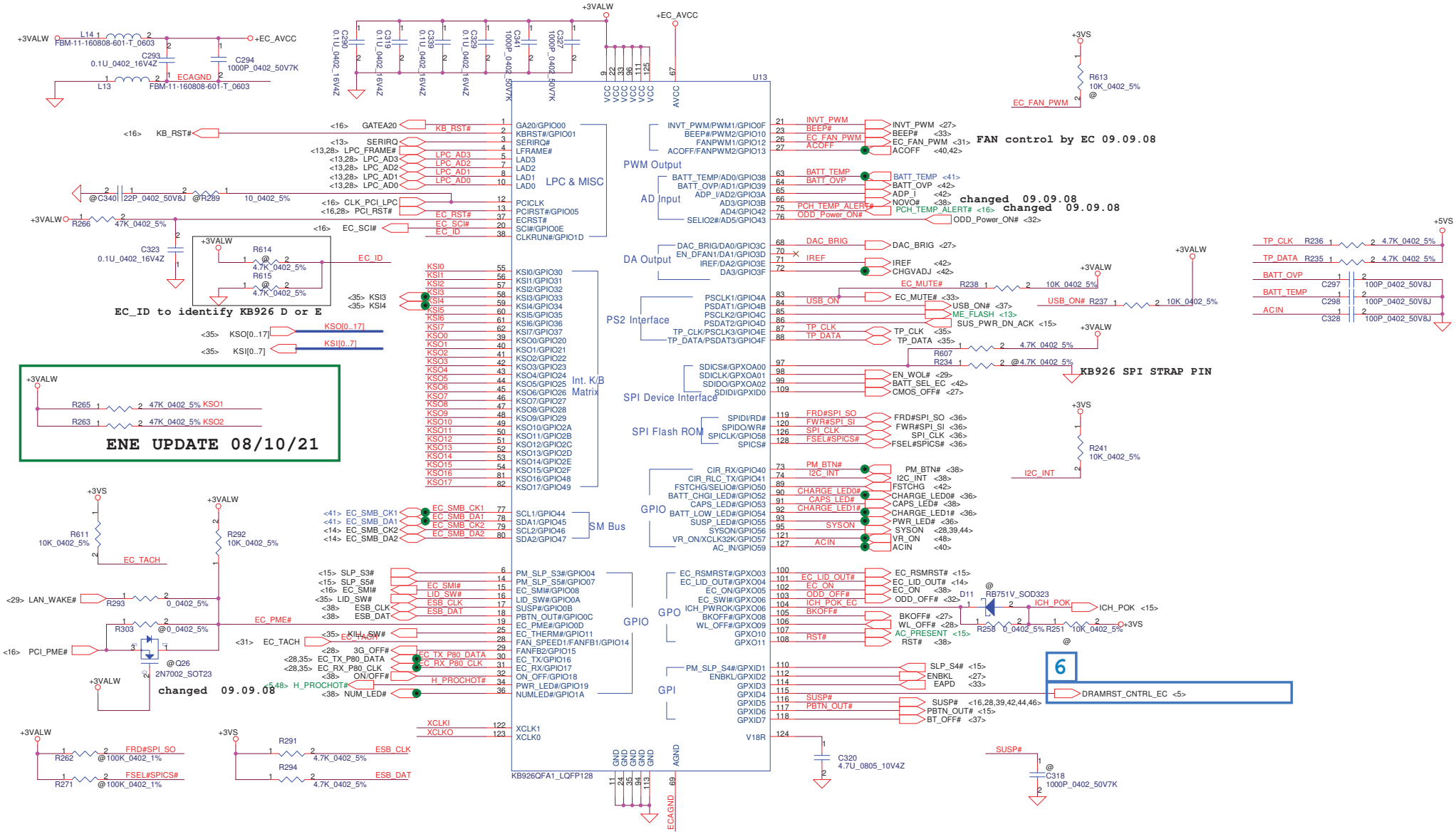
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: CX20671 Codec

Size	Document Number	Rev
C	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 33 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 34 of 51

INT_KBD Conn.

KSI[0..7] KSI[0..7] <34>

KSO[0..17] KSO[0..17] <34>

KSO2	C203	1	2	@100P_0402_50V8J	KSO16	C636	1	2	@100P_0402_50V8J
KSO15	C153	1	2	@100P_0402_50V8J	KSO17	C637	1	2	@100P_0402_50V8J
KSO6	C175	1	2	@100P_0402_50V8J	KSO1	C205	1	2	@100P_0402_50V8J
KSO8	C185	1	2	@100P_0402_50V8J	KSO7	C186	1	2	@100P_0402_50V8J
KSO13	C172	1	2	@100P_0402_50V8J	KSI2	C226	1	2	@100P_0402_50V8J
KSO12	C173	1	2	@100P_0402_50V8J	KSO5	C206	1	2	@100P_0402_50V8J
KSO11	C155	1	2	@100P_0402_50V8J	KSI3	C225	1	2	@100P_0402_50V8J
KSO10	C154	1	2	@100P_0402_50V8J	KSO14	C156	1	2	@100P_0402_50V8J
KSO3	C174	1	2	@100P_0402_50V8J	KSI7	C236	1	2	@100P_0402_50V8J
KSO4	C187	1	2	@100P_0402_50V8J	KSI6	C235	1	2	@100P_0402_50V8J
KSI0	C204	1	2	@100P_0402_50V8J	KSI5	C228	1	2	@100P_0402_50V8J
KSO0	C227	1	2	@100P_0402_50V8J	KSI4	C233	1	2	@100P_0402_50V8J
					KSO9	C234	1	2	@100P_0402_50V8J
					KSI1	C241	1	2	@100P_0402_50V8J

CONN PIN define need double check

reversal of NIWE1

JP5

1	1		
2	2		
3	3		
4	4		
KSO17	5	5	
KSO16	6	6	
KSO15	7	7	
KSO10	8	8	
KSO11	9	9	
KSO14	10	10	
KSO13	11	11	
KSO12	12	12	
KSO3	13	13	
KSO6	14	14	
KSO8	15	15	
KSO7	16	16	
KSO4	17	17	
KSO2	18	18	
KSI0	19	19	
KSO1	20	20	
KSO5	21	21	
KSI3	22	22	
KSI2	23	23	
KSO0	24	24	
KSI5	25	25	
KSI4	26	26	
KSO9	27	27	
KSI6	28	28	
KSI7	29	G1	31
KSI1	30	G2	32

ACES_85201-3005N
ME@

EC DEBUG PORT

JP11

+3VALW
<28,34> EC_TX_P80_DATA — EC_TX_P80_DATA
<28,34> EC_RX_P80_CLK — EC_RX_P80_CLK

ACES_85205-0400
ME@

Lid Switch

+3VALW — 1 R347 2 0_0402_5% — +VCC_LID — R353 1 2 100K_0402_5%

A3212ELHLT-T_SOT23W-3
VDD
OUTPUT
GND
U18

C398 0.1U_0402_16V4Z

LID_SW# <34>

C397 10P_0402_50V8J

To TP/B Conn.

+5VS

C150 0.1U_0402_16V4Z

<34> TP_CLK
<34> TP_DATA

TP_CLK
TP_DATA

JP4

@C151 100P_0402_50V8J
@C152 100P_0402_50V8J

E&T_6905-E04N-00R
ME@

CONN PIN define need double check

Kill Switch

+3VALW

2 R295 1 100K_0402_5%

LSSM12-P-V-T-R_3P

<34> KILL_SW#

KILL_SW#

SW2

Kill

STATUS	
1,2(LOW)	OFF
2,3(HI)	ON

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

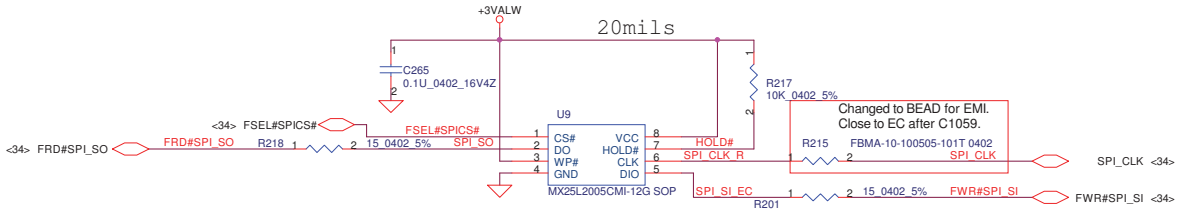
Compal Electronics, Inc.

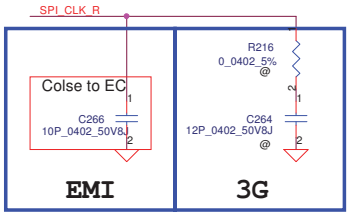
Title: KB /SW /LPC Debug Conn.

Size: B | Document Number: LA-5752P | Rev: 0.3

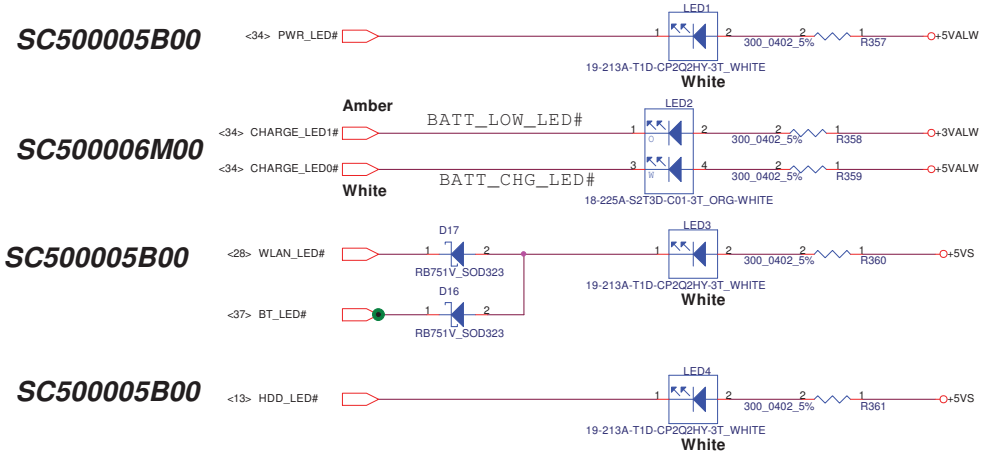
Date: Thursday, October 29, 2009 | Sheet 35 of 51

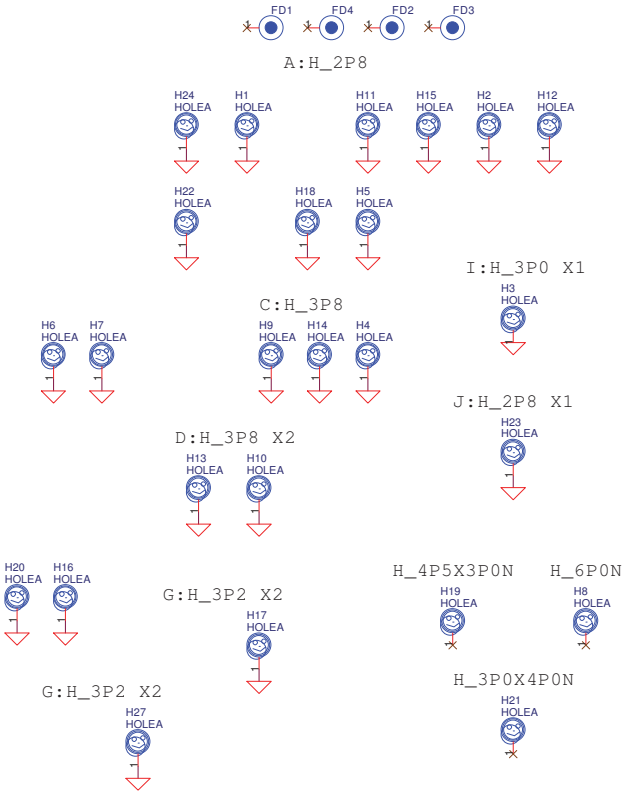
FOR EC 256KB SPI ROM
(150mil PACKAGE)
P/N : SA00003GK00





LED





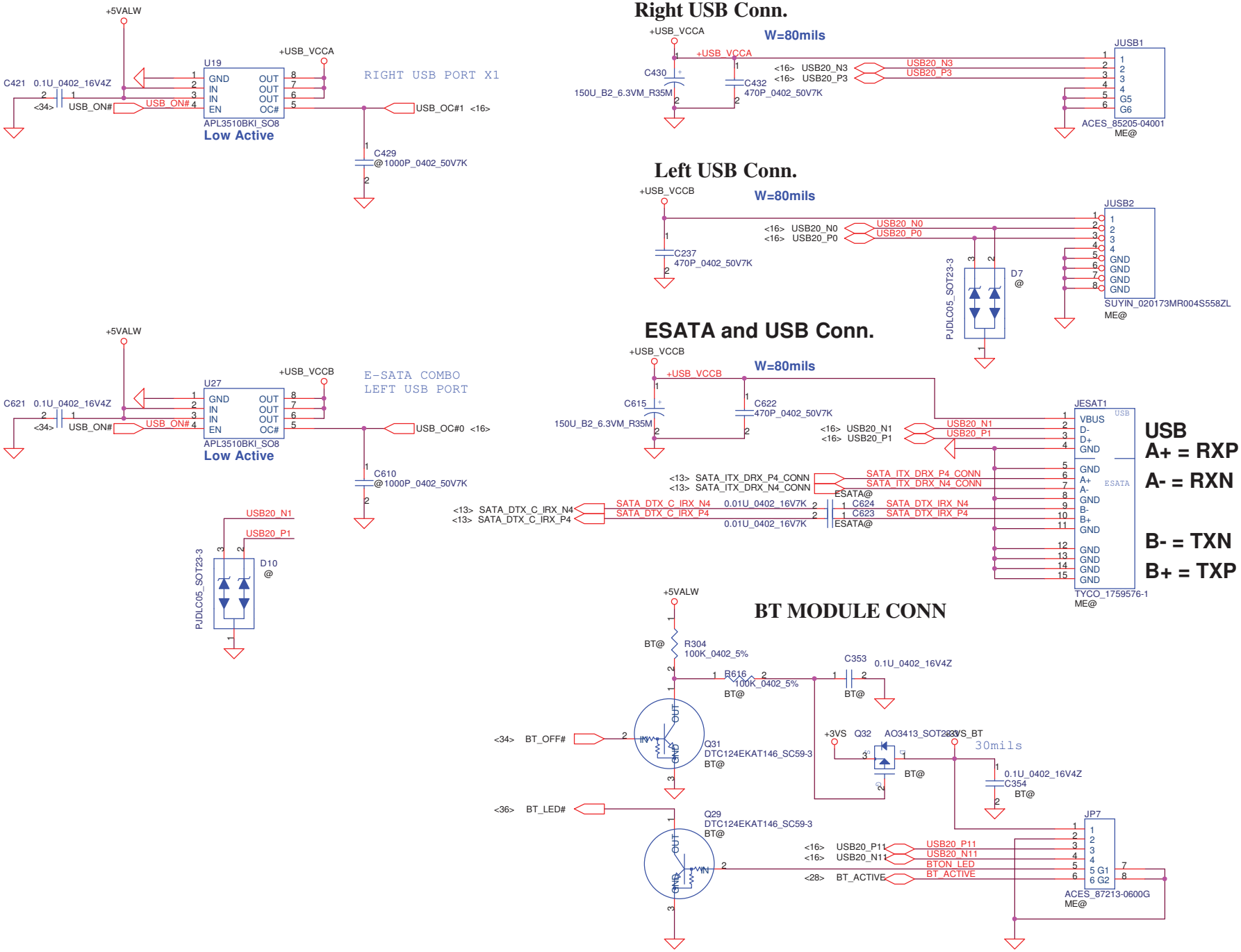
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **LED/EC SPI ROM**

Size	Document Number	Rev
B	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 36 of 51



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

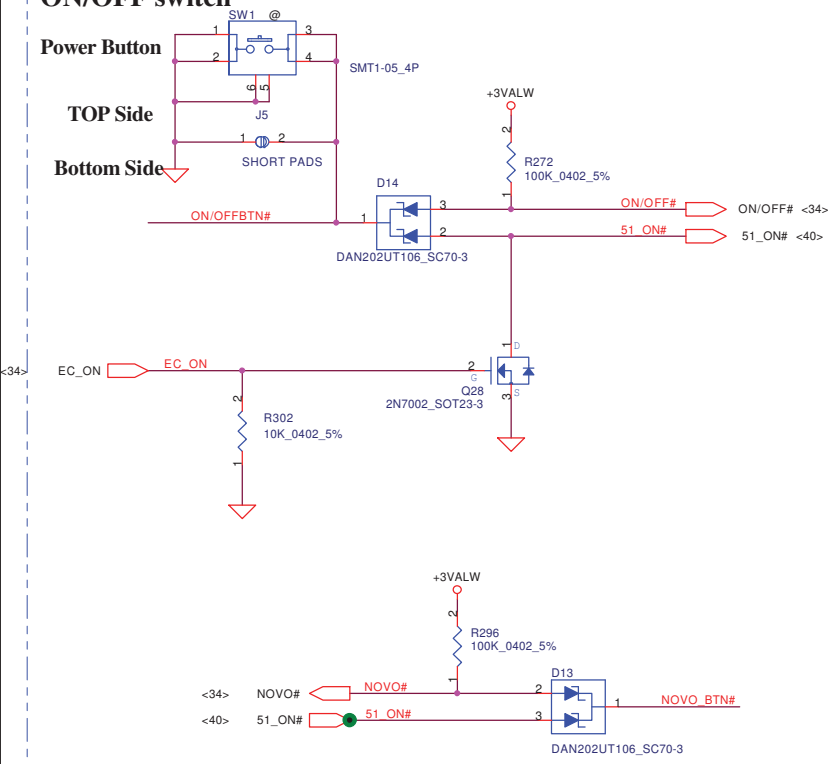
Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

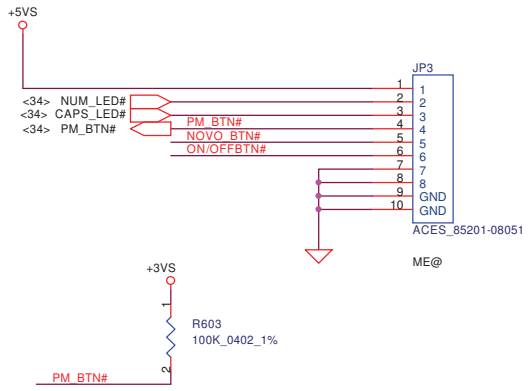
Size	Document Number	Rev
Custom	LA-5752P	0.3

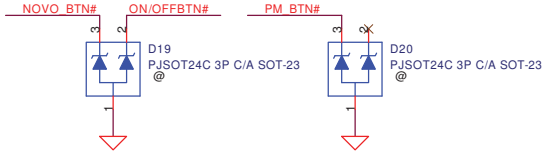
Date: Thursday, October 29, 2009 Sheet 37 of 51

ON/OFF switch



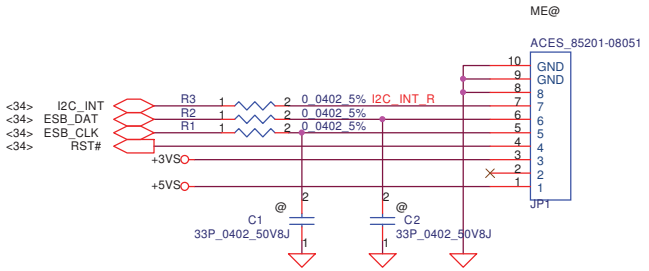
Power Bottom Board Conn. 8pin



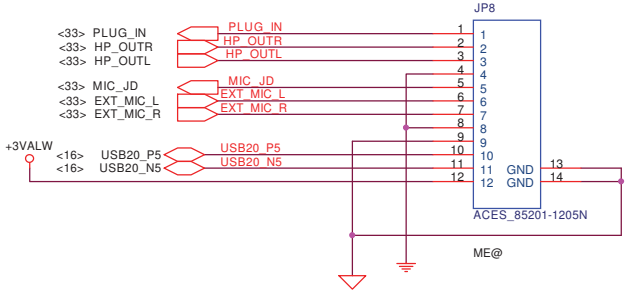


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Cap Sensor Board Conn. 6pin
ENE SB3534



Card Reader/Audio Jack SB CONN



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

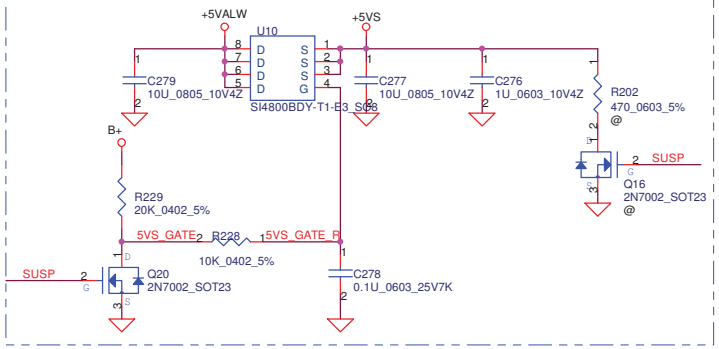
Compal Electronics,Ltd.

Title: **Audio Jack & SW connector**

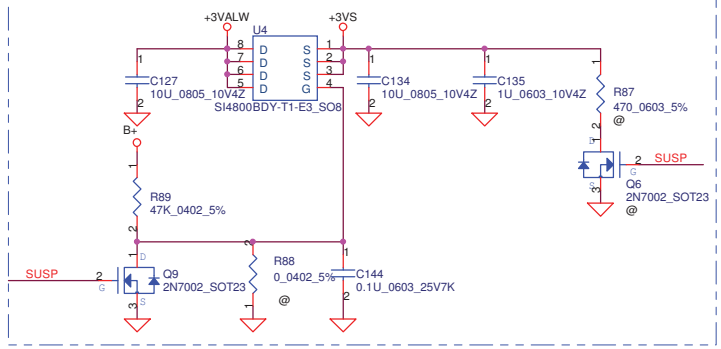
Size	Document Number	Rev
Custom	LA-5752P	0.3

Date: Thursday, October 29, 2009 | Sheet 38 of 51

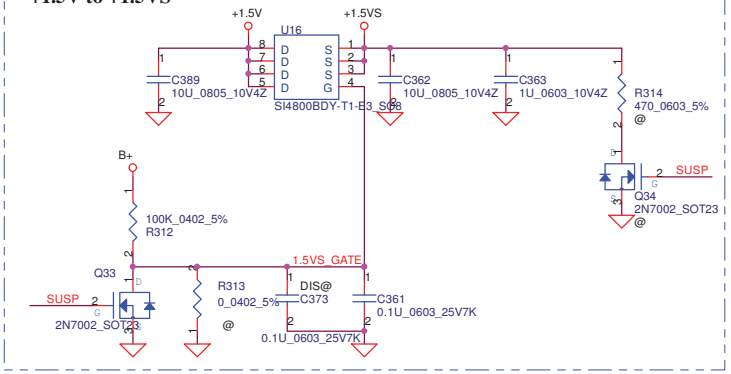
+5VALW TO +5VS

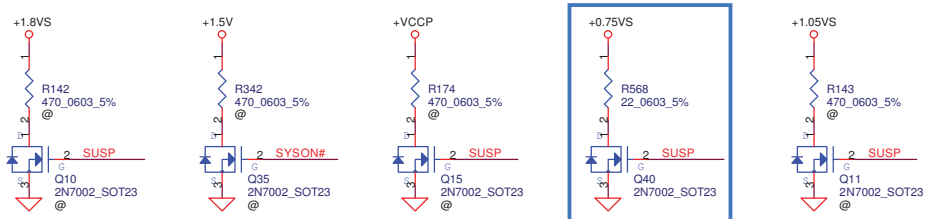


+3VALW TO +3VS

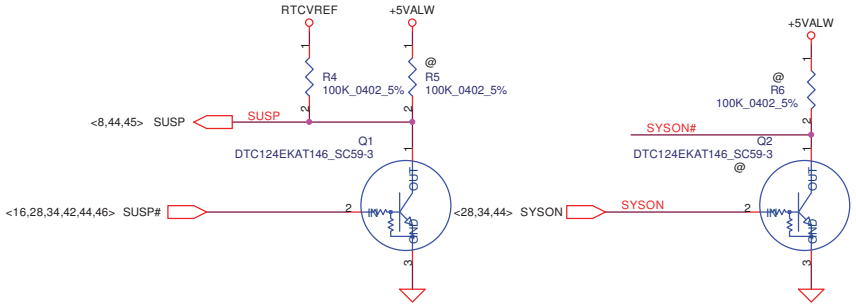


+1.5V to +1.5VS





For Intel S3 Power Reduction.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

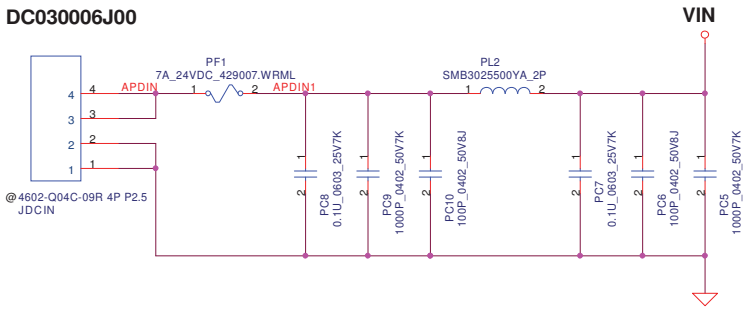
Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-5752P	0.3

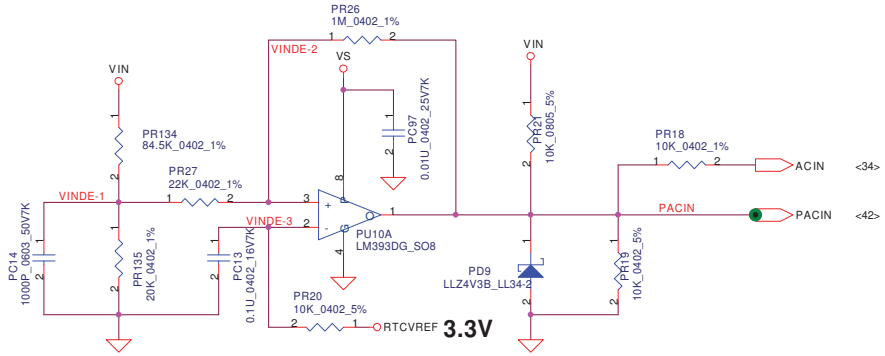
Date: Thursday, October 29, 2009 | Sheet 39 of 51

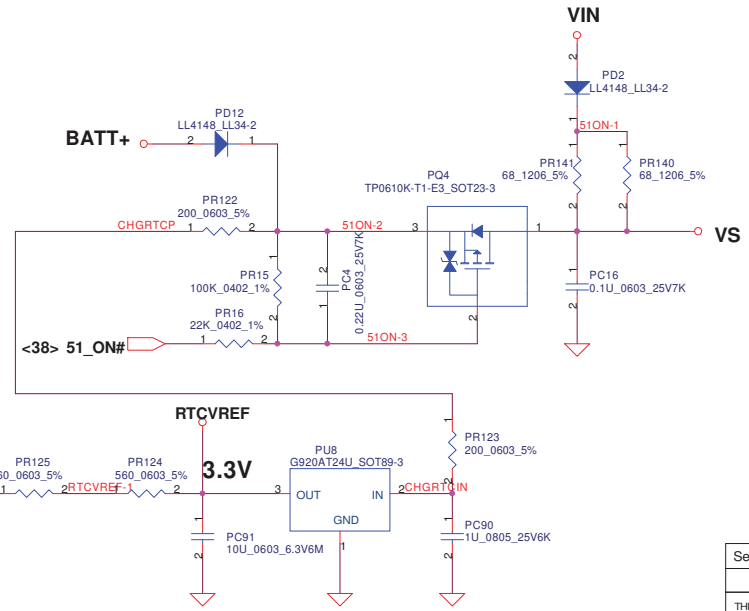
DC030006J00



Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



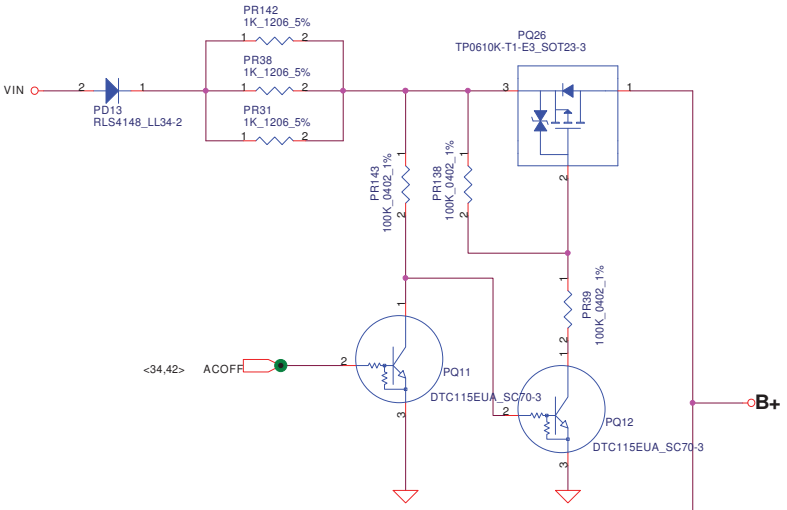


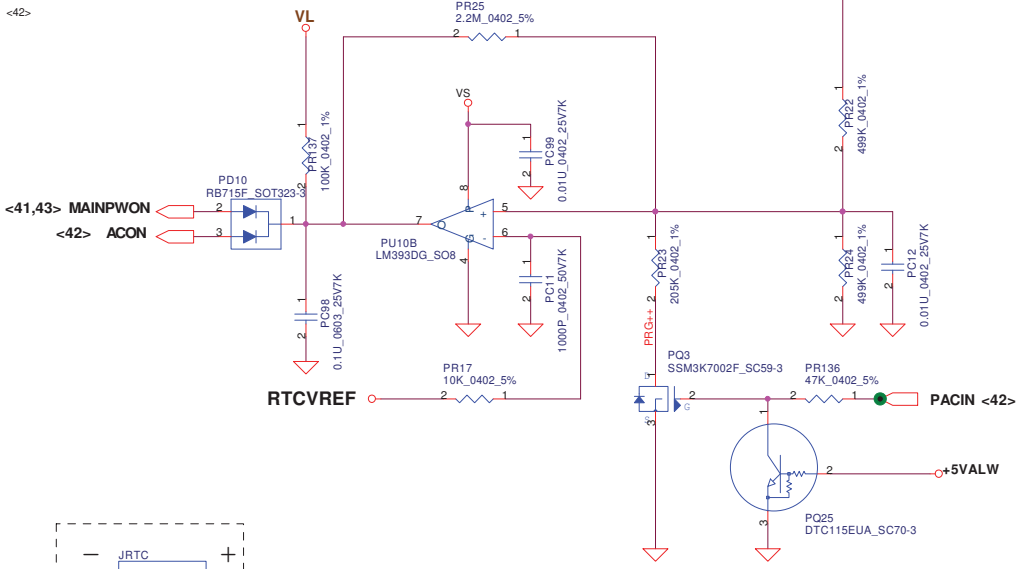
ACIN

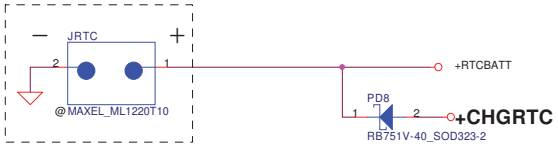
Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V







RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

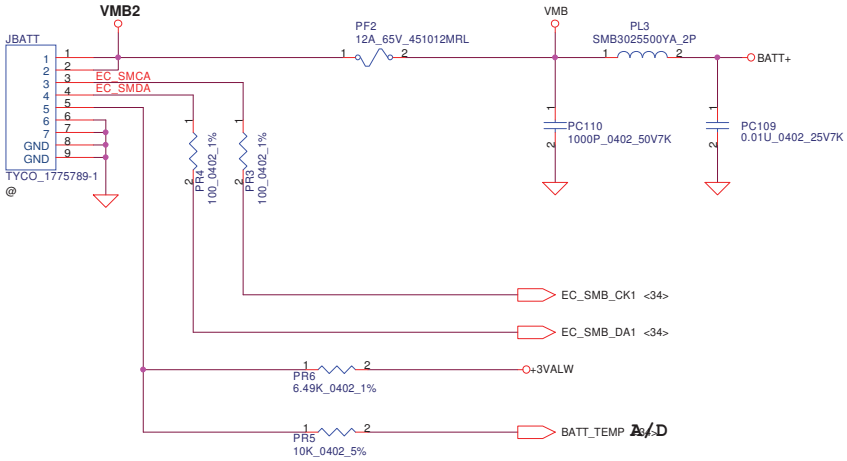
Compal Electronics, Inc.

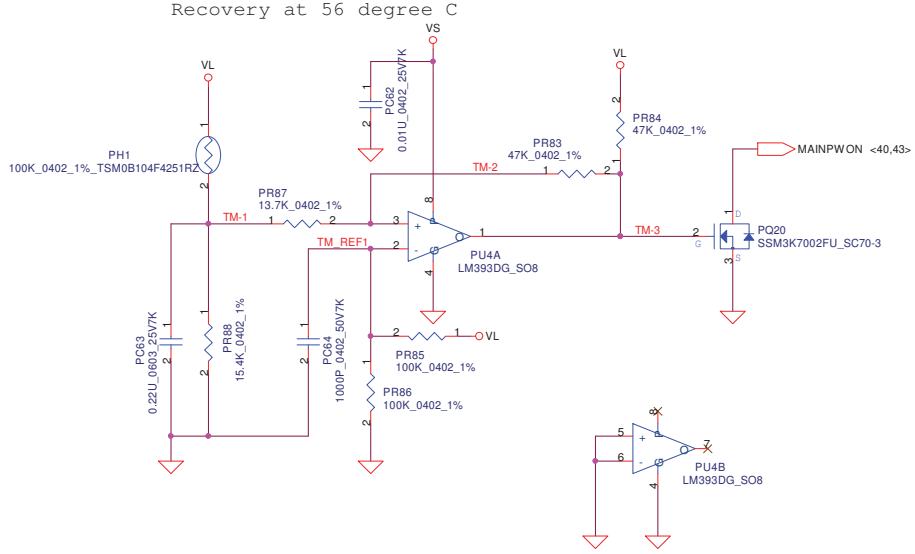
Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.1

Date: Thursday, October 29, 2009 | Sheet 40 of 51

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





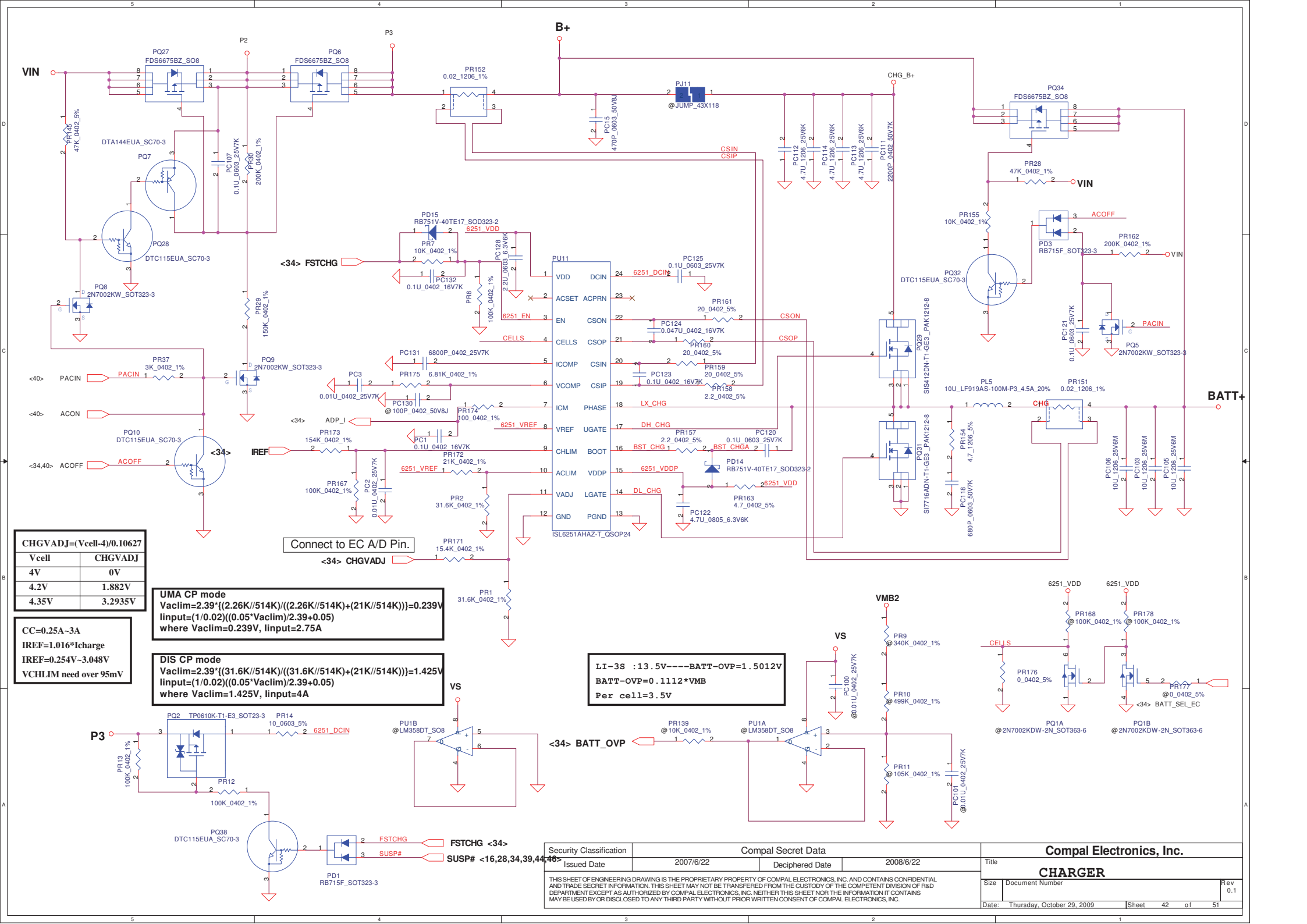
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 | Sheet 41 of 51



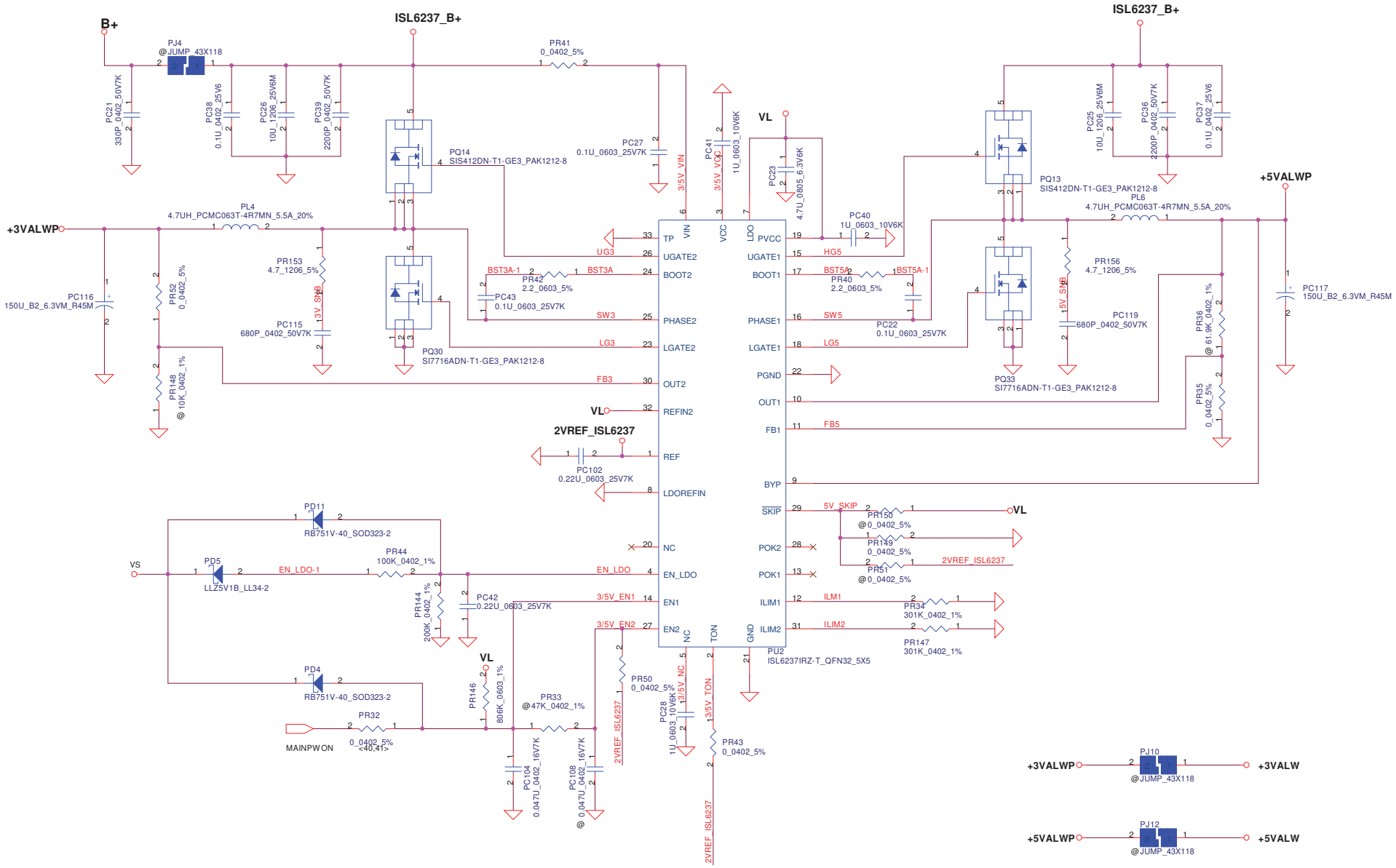
Security Classification	Compal Secret Data		
Issued Date	2007/6/22	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number | Rev 0.1

Date: Thursday, October 29, 2009 | Sheet 42 of 51



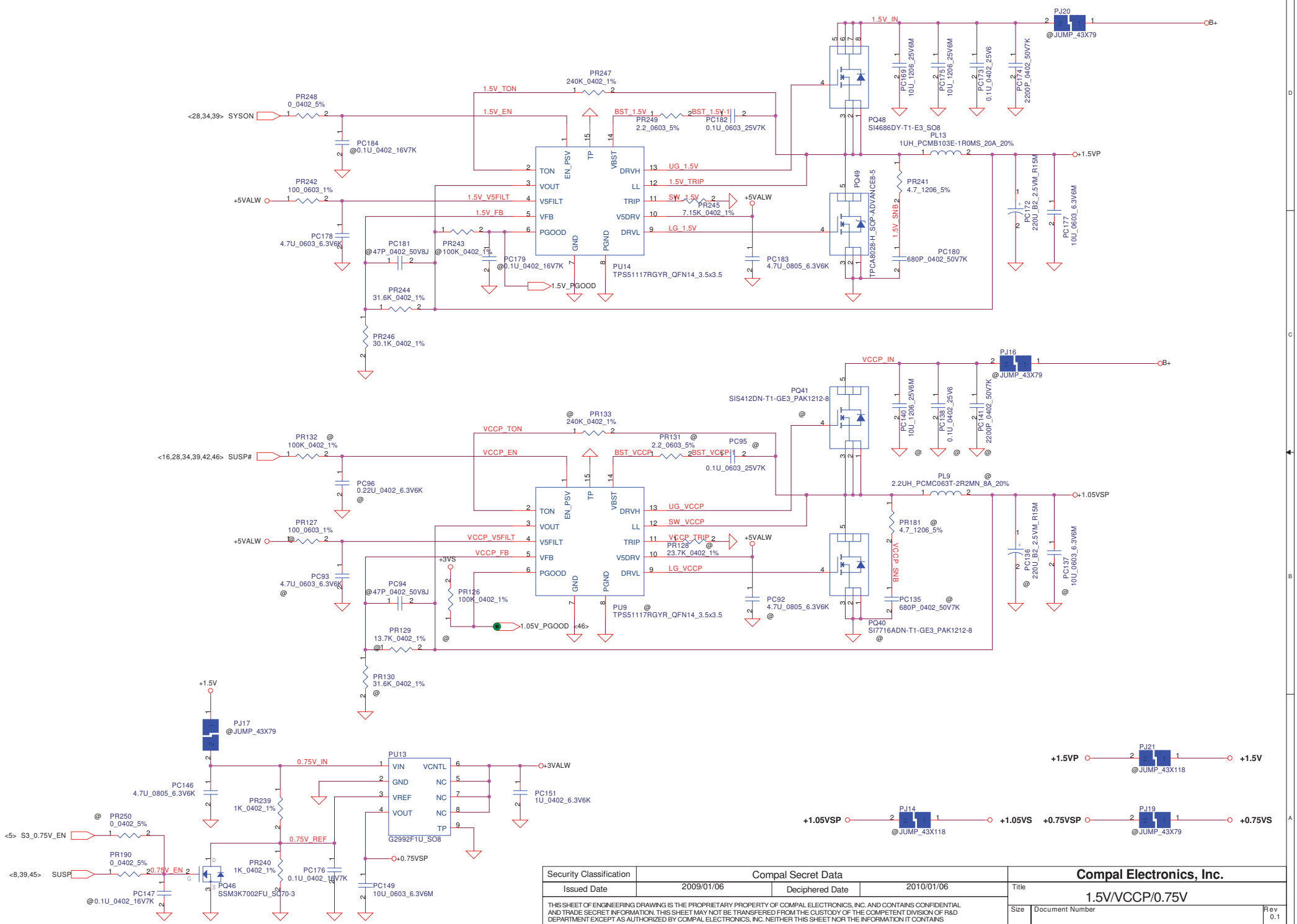
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: **3VALW/5VALW**

Size	Document Number	Rev
Custom		0.1

Date: Thursday, October 29, 2009 | Sheet 43 of 51



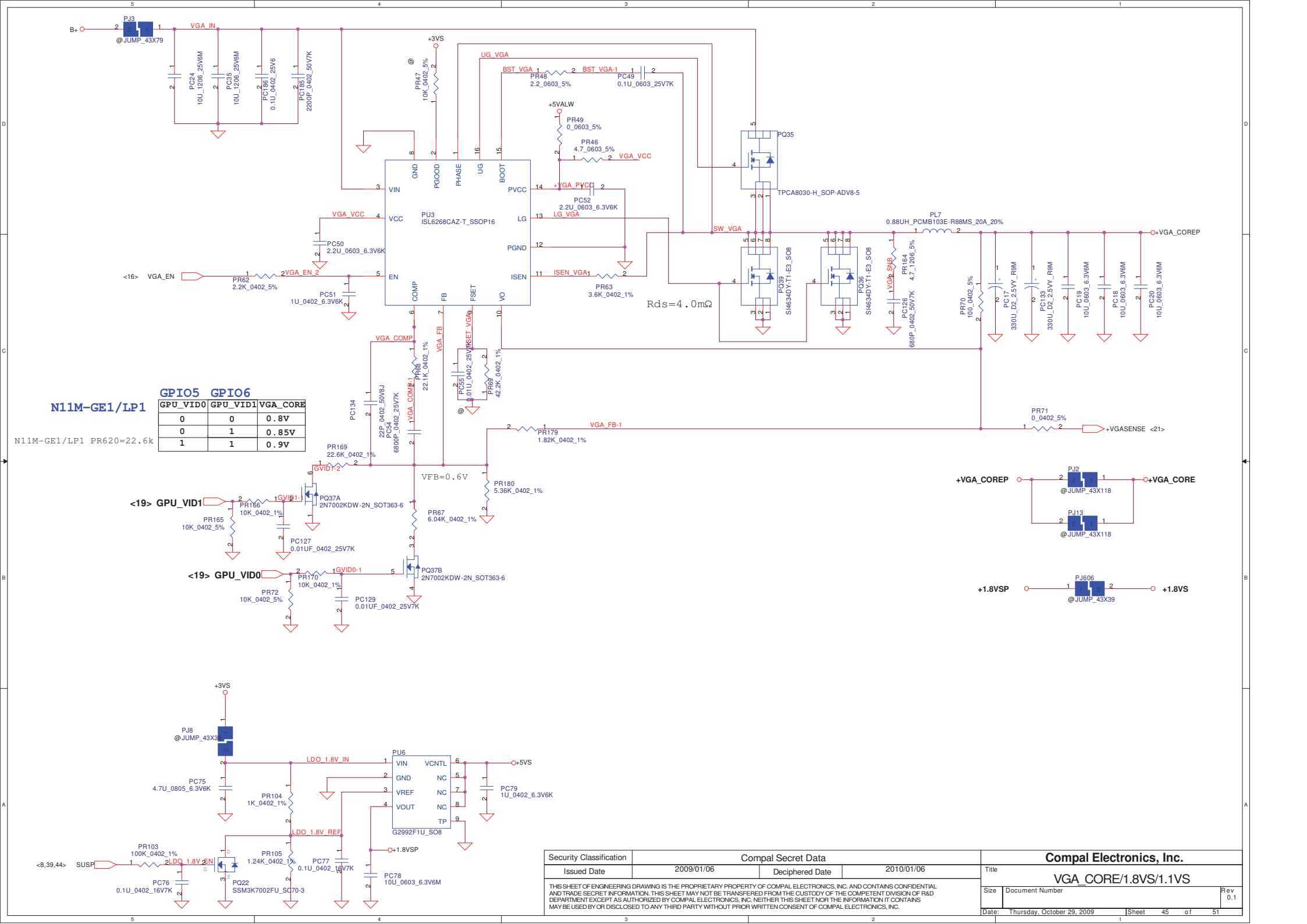
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.5V/VCCP/0.75V

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 | Sheet 44 of 51



N11M-GE1/LP1

N11M-GE1/LP1 PR620=22.6k

GPIO5 GPIO6		
GPU_VID0	GPU_VID1	VGA_CORE
0	0	0.8V
0	1	0.85V
1	1	0.9V

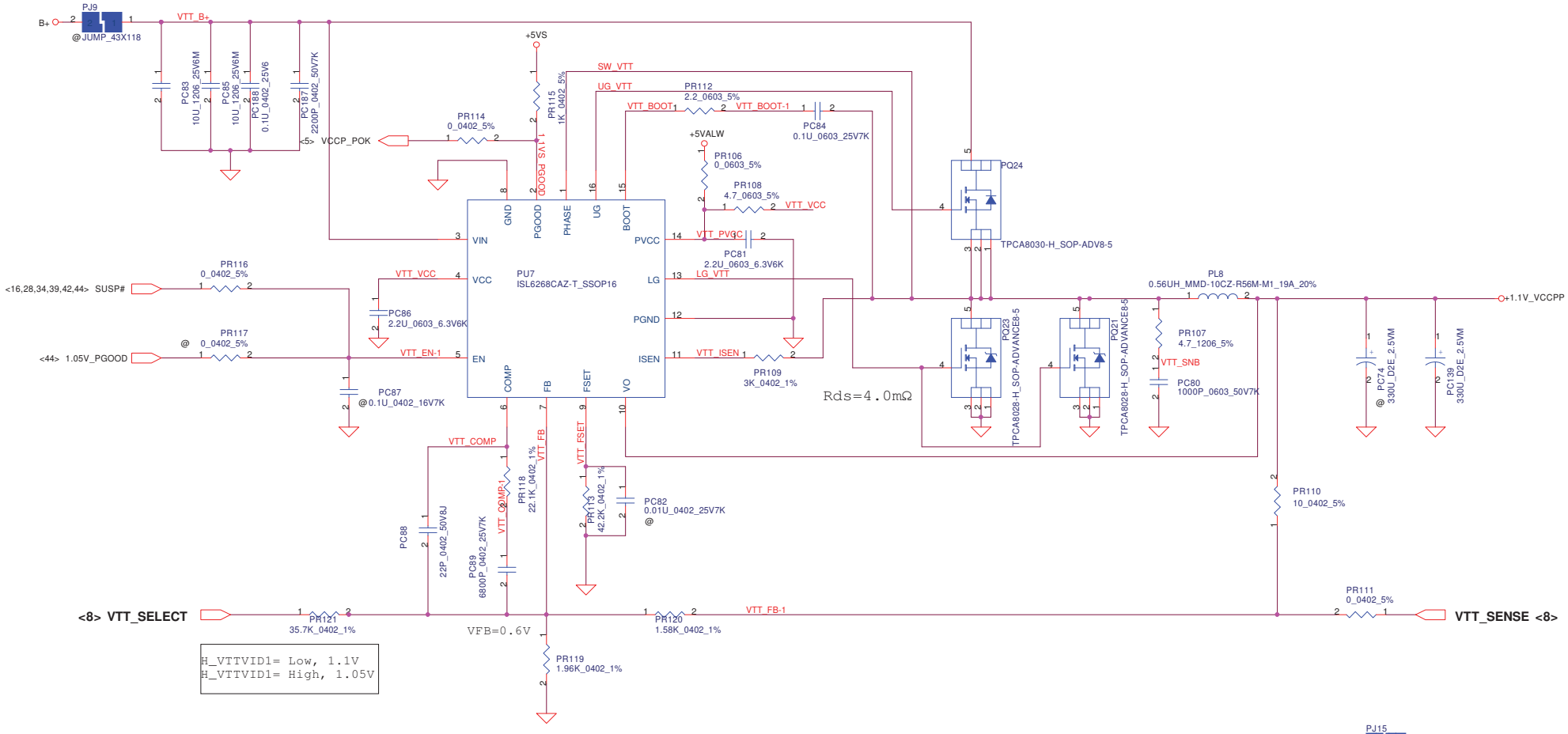
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: VGA_CORE/1.8VS/1.1VS

Size | Document Number | Rev 0.1

Date: Thursday, October 29, 2009 | Sheet 45 of 51



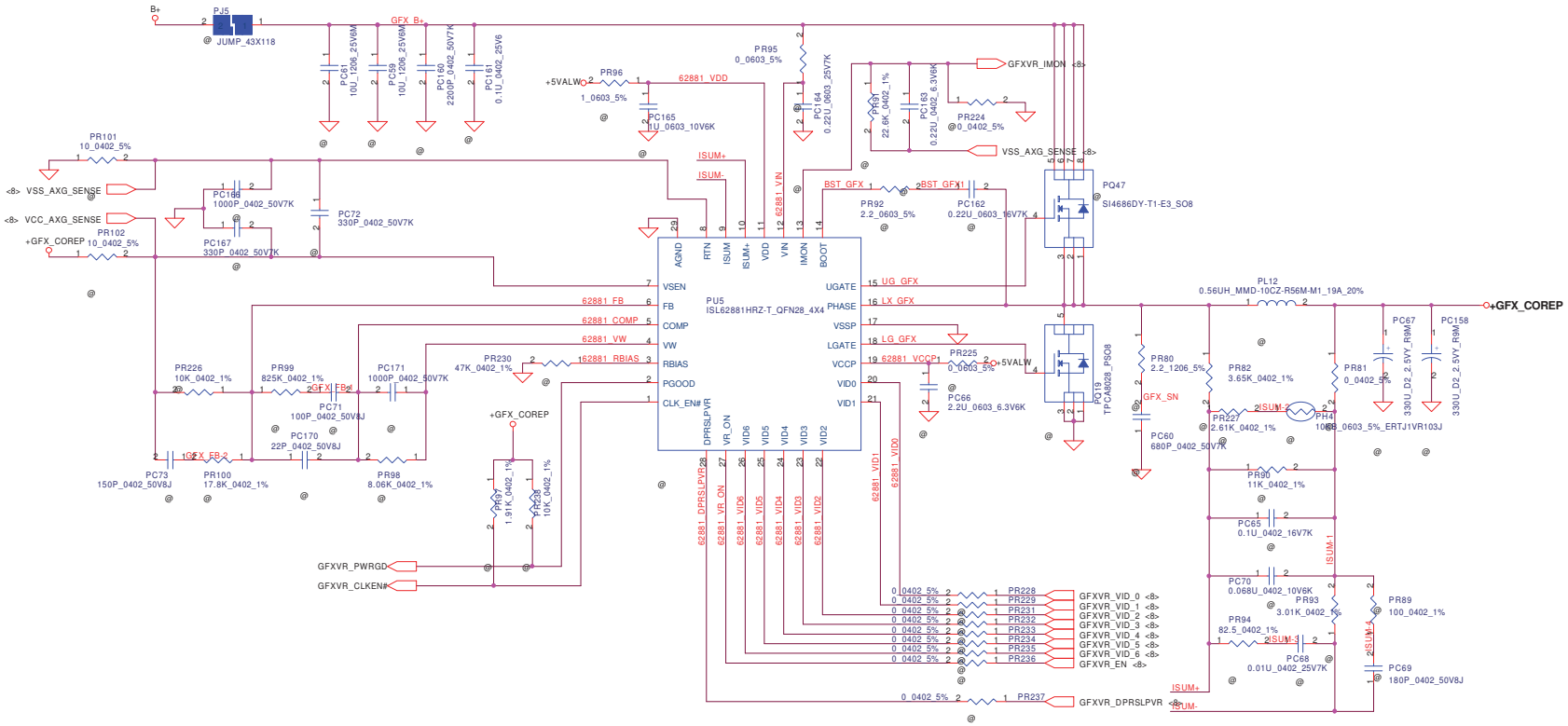
Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: +1.1VS_VTT

Size: Custom | Document Number | Rev: 0.1

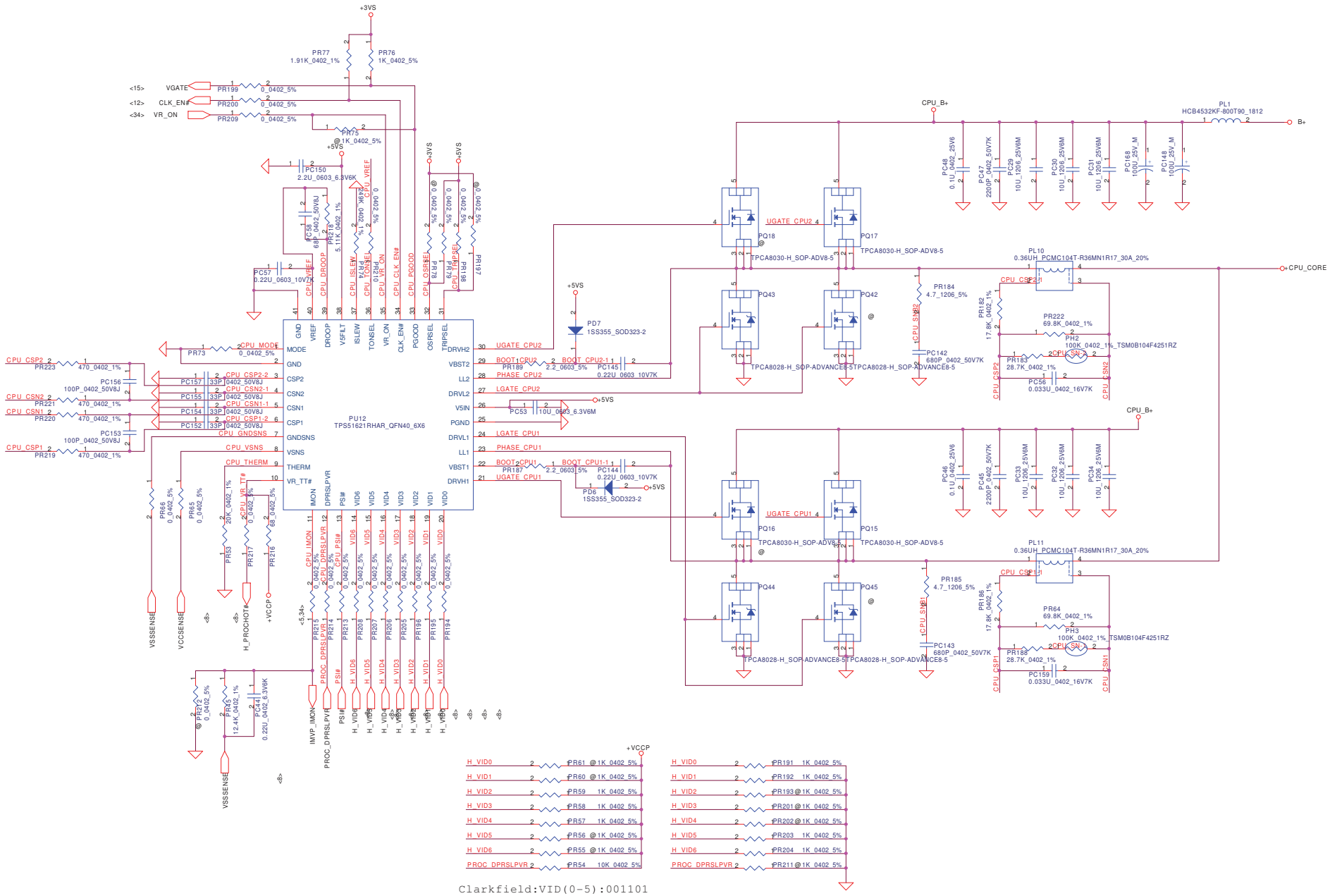
Date: Thursday, October 29, 2009 | Sheet 46 of 51



(15A,600mils ,Via NO.= 30)

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.			
Title	GFX_CORE		
Size	Document Number		Rev 0.1
Date: Thursday, October 29, 2009		Sheet 47 of 51	



Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: **CPU_CORE**

Size	Document Number	Rev
		0.1

Date: Thursday, October 29, 2009 Sheet 48 of 51

Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: <Doc> | Rev: 0.1

Date: Thursday, October 29, 2009 | Sheet 49 of 51

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT

Compal Electronics, Inc.

Title: **HW PIR**

Size	Document Number	Rev
B	LA-5752P	0.3

Date: Thursday, October 29, 2009 Sheet 50 of 51

Compal Electronics, Inc.	
Title	HW PIR
Size: B	Document Number: LA-5751
Rev: 0.3	
Date: Thursday, October 29, 2009	Sheet 51 of 51