

# Compal Confidential

## G400/G500 UMA M/B Schematics Document Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

2013-02-27

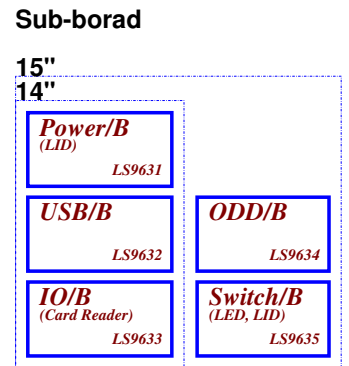
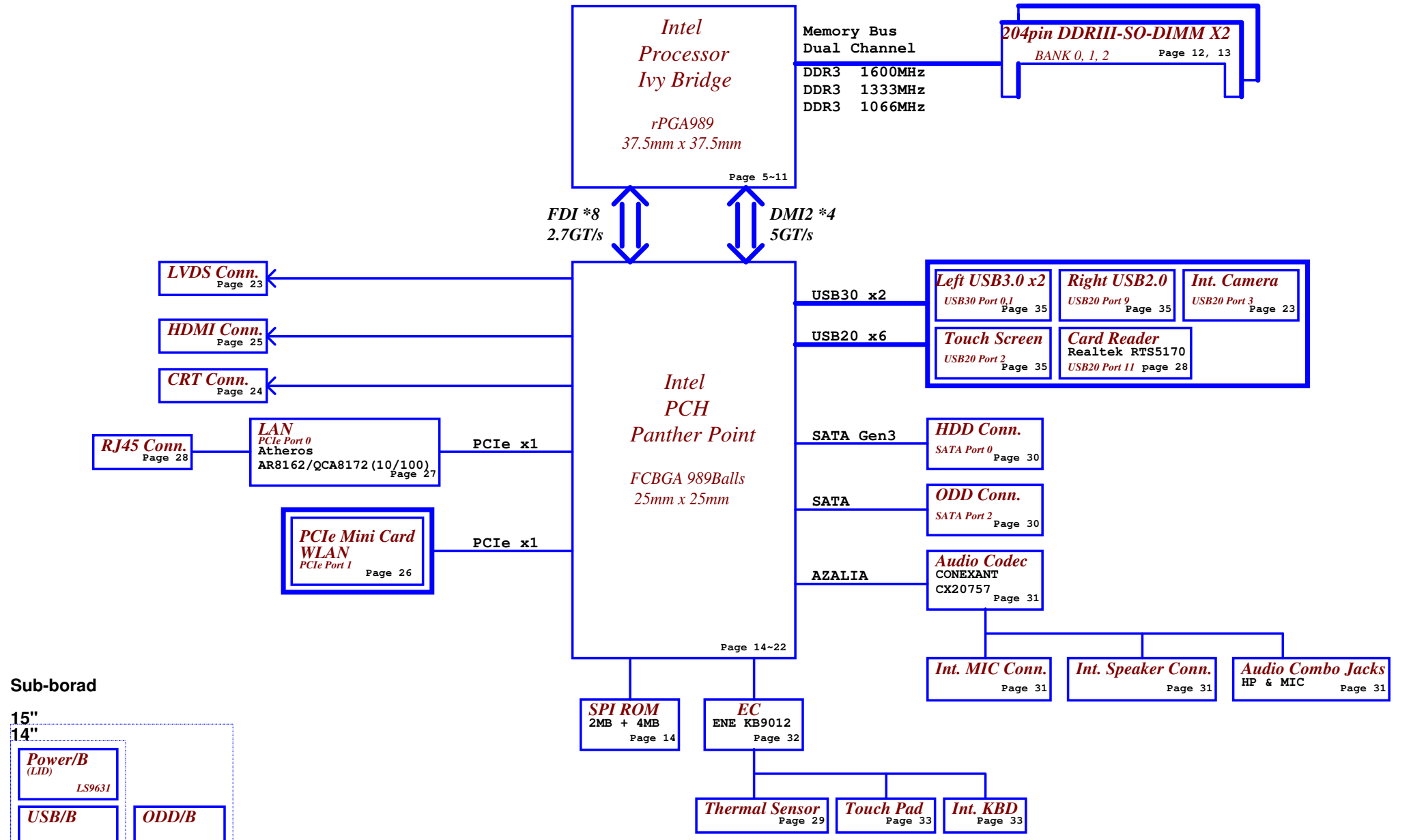
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REV: 1.0

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# Chief River



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### Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
		+3VALW		+3VS
State				+1.5VS
				+V1.05S_VCCP
				+VCC_CORE
				+VGA_CORE
				+VCC_GFXCORE_AXG
				+1.8VS
				+0.75VS
				+1.05VS
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V	Board ID / SKU ID Table for AD channel						
R694	100K +/- 1%	Board ID	R695	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC AD	
0	0	0	0 V	0 V	0 V	0 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT		
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	DVT		
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	EVT		

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address
Smart Battery	0001 011x

Device	Address
Thermal Sensor	0100 1100

### PCH SM Bus address

### AMD-GPU SM Bus address

Device	Address
DDR_JDIMM1	1010 000x A0h
DDR_JDIMM2	1010 010x A4h

Device	Address
Internal thermal sensor	0100 0001 41h

### USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) <sub>USB3.0</sub>
		1	USB Port (Left Side) <sub>USB3.0</sub>
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
7			
EHCI2	UHCI4	8	USB Port (Right Side USB-BD)
		9	Mini Card(WLAN)
	UHCI5	10	Card Reader
		11	
	UHCI6	12	
		13	

### BOM Structure Table

Item	BOM Structure
VIWGP (14")	14@
VIWGR (15")	15@
HDMI Logo	45@
LAN 10/100	8162@
LAN 10/100	8172@
LAN Switch mode	SWR@
LAN LDO Mode	LDO@
LAN Gas tube	GAS@
Camera	CMOS@
HDMI	HDMI@
PCH is HM76	HM76@
PCH is HM70	HM70@
PCH is NM70	NM70@
VGA is Mars XT	Mars@
VGA is Sun Pro	Sun@
For VGA	PX@
For VRAM and Strap	X76@
For UMA Strap	UMA@
Microphone	MIC@
Touch Screen	TS@
Connector	ME@
Board ID for EVT	EVT@
Board ID for DVT	DVT@
Board ID for PVT	PVT@
For USB2.0 (All PCH)	USB2@
For USB3.0 (HM76, HM70)	USB3@
For share ROM	SROM@
For non-share ROM	NOSROM@

### SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	V	X	X	X	X	V	V
SMB_EC_DA2	+3VS	+3VGS					+3VS	+3VALW
PCH_SMBCLK	PCH	X	X	X	V	V	X	X
PCH_SMBDATA	+3VALW				+3VS	+3VS		
PCH_SMLCLK	PCH	X	X	X	X	X	X	X
PCH_SMLDATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VGS		+3VS			+3VS	

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5

4

3

2

1

D

D

C

C

B

B

A

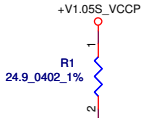
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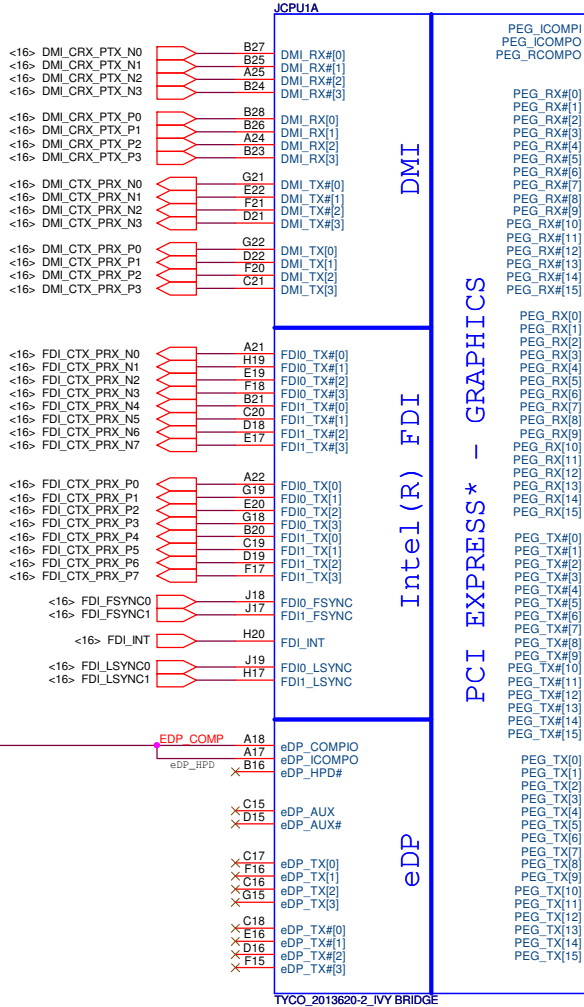
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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

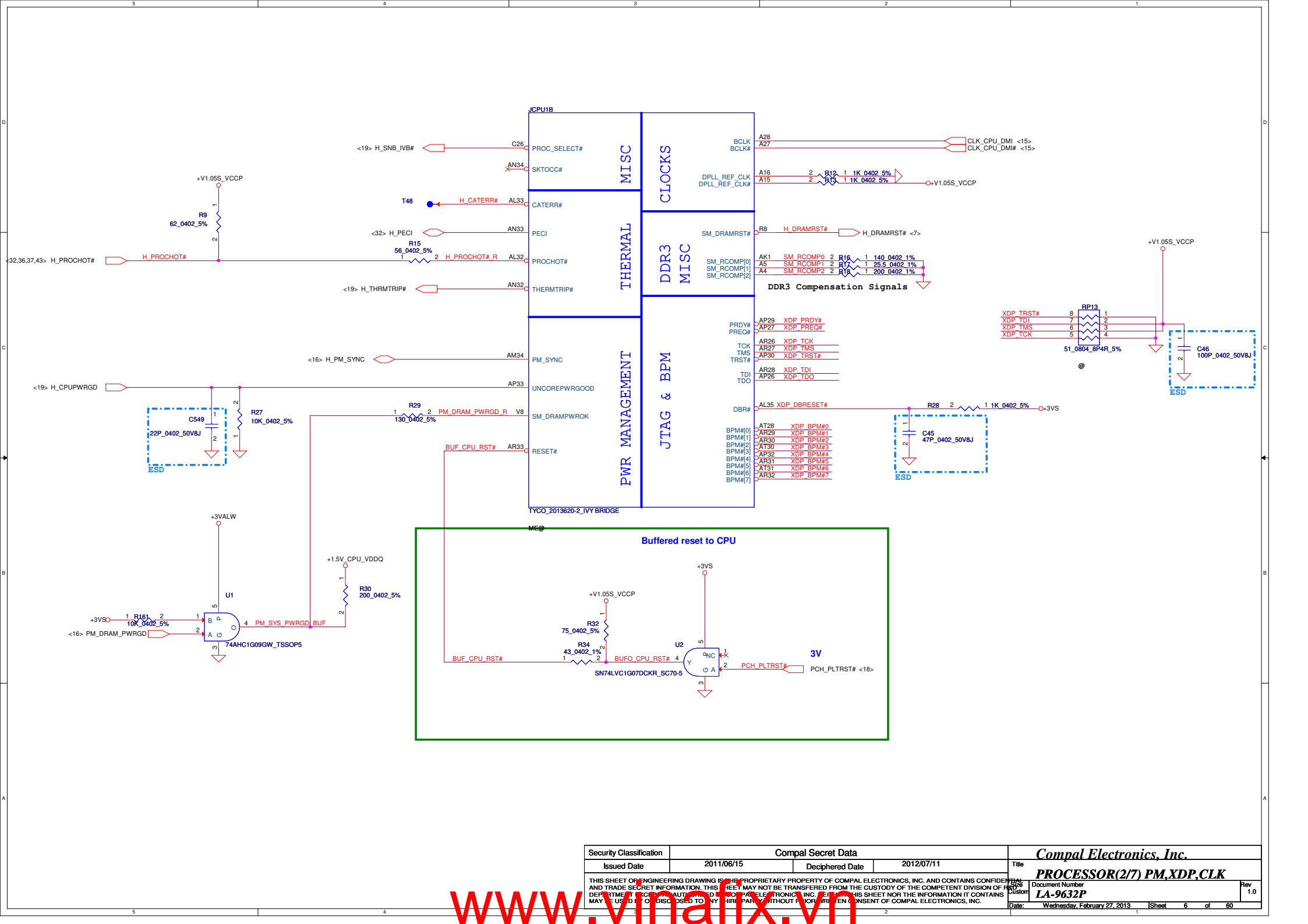


- PEG\_ICOMPI
- PEG\_ICOMPO
- PEG\_RCOMPO
- PEG\_RX#(0) K33
- PEG\_RX#(1) M35
- PEG\_RX#(2) L34
- PEG\_RX#(3) J35
- PEG\_RX#(4) J32
- PEG\_RX#(5) H34
- PEG\_RX#(6) H31
- PEG\_RX#(7) G30
- PEG\_RX#(8) F35
- PEG\_RX#(9) E34
- PEG\_RX#(10) E32
- PEG\_RX#(11) D33
- PEG\_RX#(12) D31
- PEG\_RX#(13) B33
- PEG\_RX#(14) C32
- PEG\_RX#(15) J33
- PEG\_RX(0) L35
- PEG\_RX(1) K34
- PEG\_RX(2) H35
- PEG\_RX(3) H32
- PEG\_RX(4) G34
- PEG\_RX(5) G31
- PEG\_RX(6) F33
- PEG\_RX(7) F30
- PEG\_RX(8) E35
- PEG\_RX(9) E33
- PEG\_RX(10) F32
- PEG\_RX(11) D34
- PEG\_RX(12) E31
- PEG\_RX(13) C33
- PEG\_RX(14) B32
- PEG\_RX(15) M28
- PEG\_TX#(0) M32
- PEG\_TX#(1) M31
- PEG\_TX#(2) L32
- PEG\_TX#(3) L29
- PEG\_TX#(4) K31
- PEG\_TX#(5) K28
- PEG\_TX#(6) J30
- PEG\_TX#(7) J28
- PEG\_TX#(8) H29
- PEG\_TX#(9) G27
- PEG\_TX#(10) E29
- PEG\_TX#(11) F27
- PEG\_TX#(12) D28
- PEG\_TX#(13) F26
- PEG\_TX#(14) E25
- PEG\_TX#(15) M28
- PEG\_TX(0) M33
- PEG\_TX(1) M30
- PEG\_TX(2) L31
- PEG\_TX(3) L28
- PEG\_TX(4) K30
- PEG\_TX(5) K27
- PEG\_TX(6) J29
- PEG\_TX(7) J27
- PEG\_TX(8) H28
- PEG\_TX(9) G28
- PEG\_TX(10) E28
- PEG\_TX(11) F28
- PEG\_TX(12) D27
- PEG\_TX(13) E26
- PEG\_TX(14) D25
- PEG\_TX(15) M28

eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

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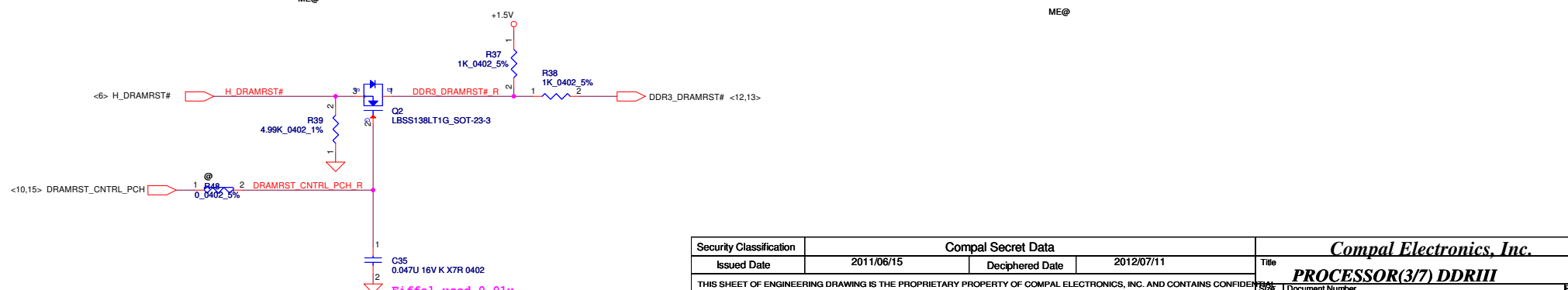
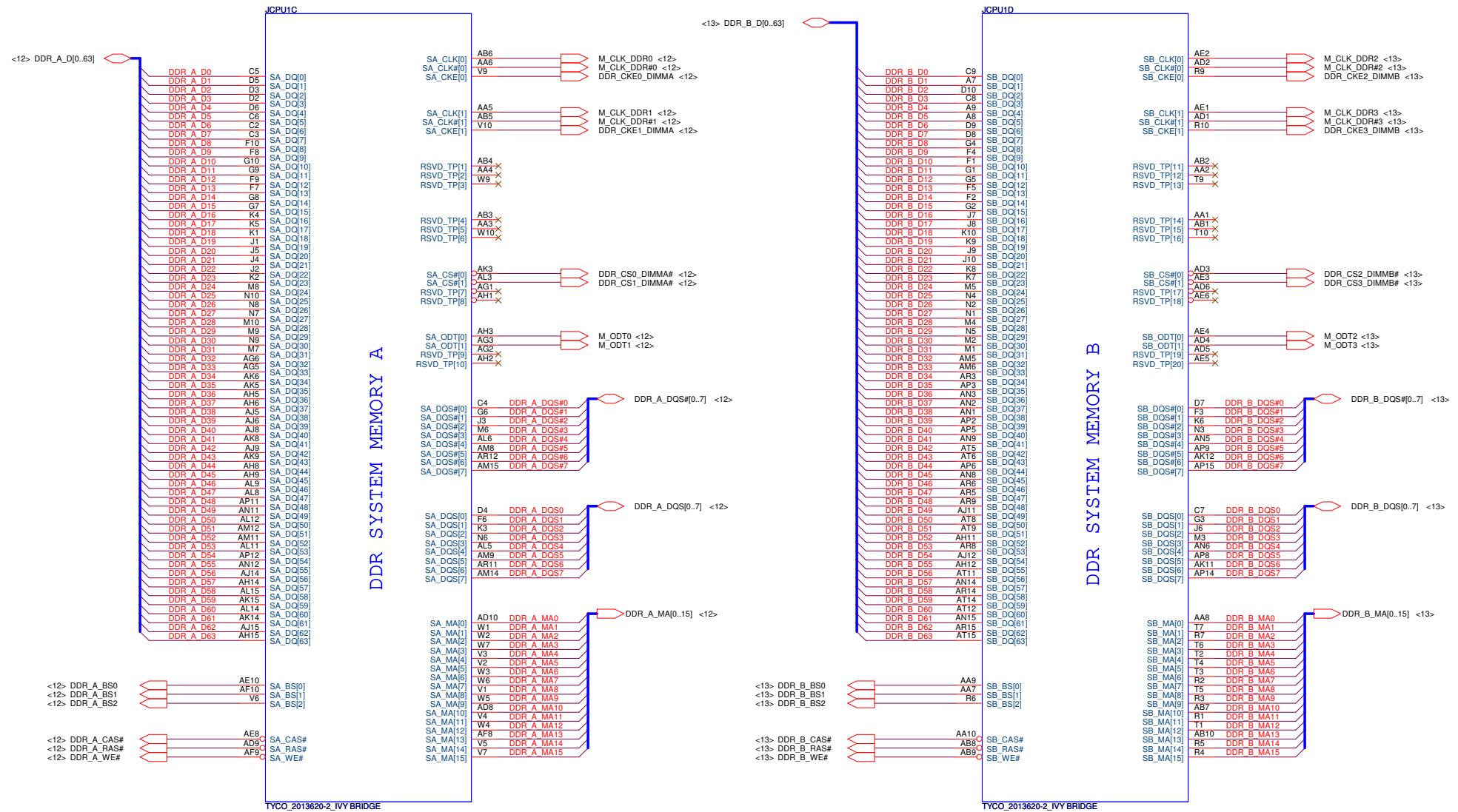
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<b>Compal Electronics, Inc.</b> <b>PROCESSOR(2/7) PM,XDP,CLK</b>	
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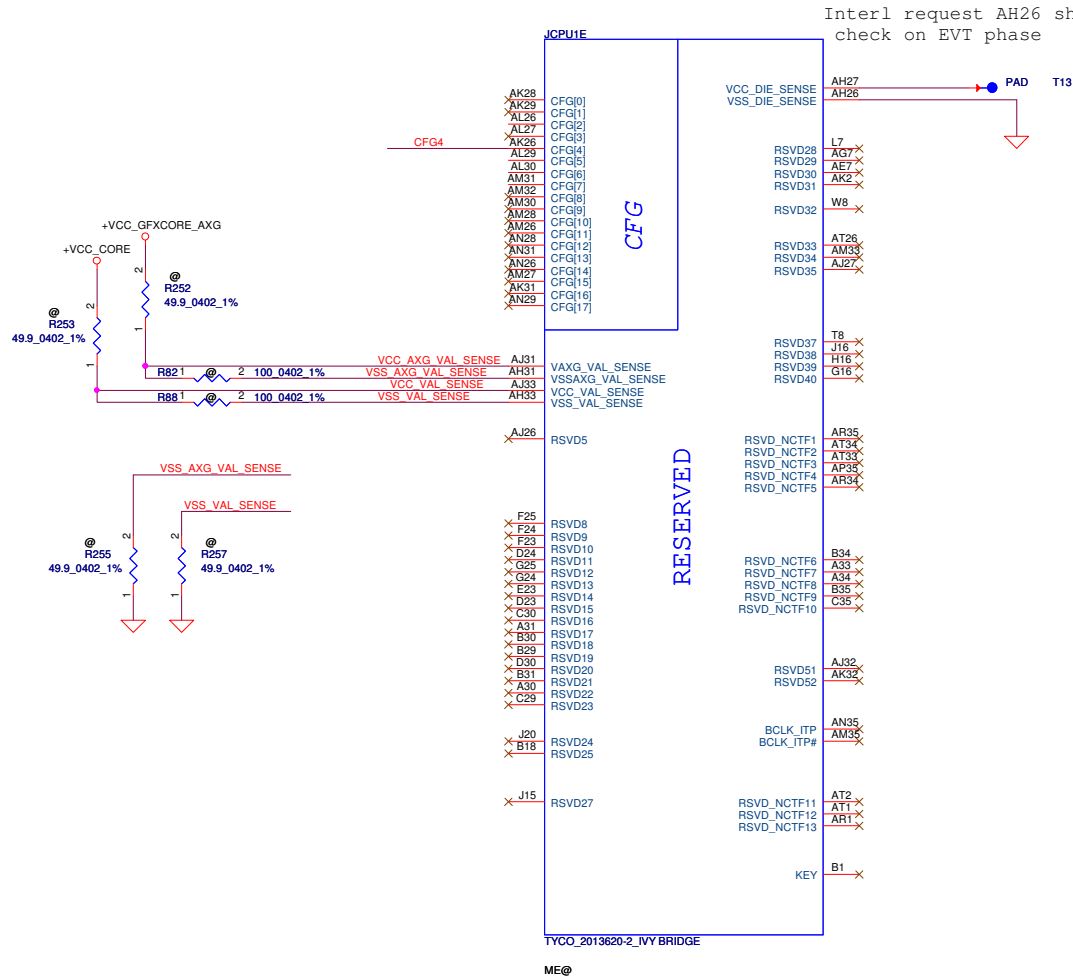
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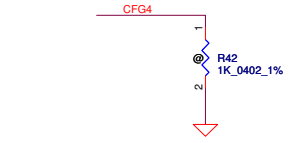
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# CFG Straps for Processor



Interl request AH26 short GND  
check on EVT phase

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled * 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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# POWER

+VCC\_CORE  
**QC=94A**  
**DC=53A**

JCPU1F

+V1.05S\_VCCP  
**8.5A**

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- U35 VCC70
- U34 VCC71
- U33 VCC72
- U32 VCC73
- U31 VCC74
- U30 VCC75
- U29 VCC76
- U28 VCC77
- U27 VCC78
- U26 VCC79
- R35 VCC80
- R34 VCC81
- R33 VCC82
- R32 VCC83
- R31 VCC84
- R30 VCC85
- R29 VCC86
- R28 VCC87
- R27 VCC88
- R26 VCC89
- P35 VCC90
- P34 VCC91
- P33 VCC92
- P32 VCC93
- P31 VCC94
- P30 VCC95
- P29 VCC96
- P28 VCC97
- P27 VCC98
- P26 VCC99
- VCC100

- VCCI01 AH13
- VCCI02 AH10
- VCCI03 AG10
- VCCI04 AC10
- VCCI05 Y10
- VCCI06 U10
- VCCI07 P10
- VCCI08 L10
- VCCI09 J14
- VCCI10 J13
- VCCI11 J12
- VCCI12 VCCI011
- VCCI13 VCCI012
- VCCI14 VCCI013
- VCCI15 VCCI014
- VCCI16 VCCI015
- VCCI17 VCCI016
- VCCI18 VCCI017
- VCCI19 VCCI018
- VCCI20 VCCI019
- VCCI21 VCCI020
- VCCI22 VCCI021
- VCCI23 VCCI022
- VCCI24 VCCI023
- VCCI25 VCCI024
- VCCI26 E11
- VCCI27 D14
- VCCI28 D13
- VCCI29 D12
- VCCI30 VCCI029
- VCCI31 C14
- VCCI32 C13
- VCCI33 VCCI031
- VCCI34 VCCI032
- VCCI35 VCCI033
- VCCI36 VCCI034
- VCCI37 VCCI035
- VCCI38 VCCI036
- VCCI39 VCCI037
- VCCI40 VCCI038
- VCCI41 A12
- VCCI42 A11
- VCCI43 J23

## PEG AND DDR

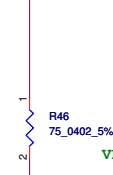
## CORE SUPPLY

## SVID

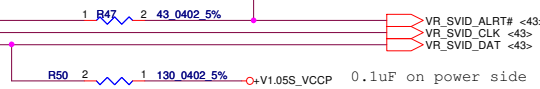
## SENSE LINES

- VIDALERT# AJ29
- VIDCLK AJ30
- VIDSOUT AJ28
- VCC\_SENSE VSS\_SENSE AJ35
- VCCIO\_SENSE VSS\_SENSE\_VCCIO AJ34

+V1.05S\_VCCP

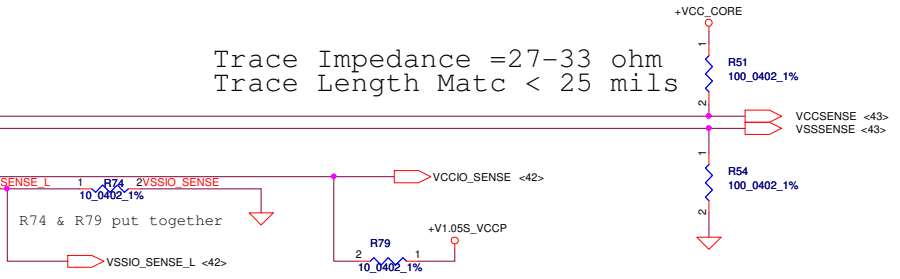


VR\_SVID\_CLK series-resistors close to VR



VCC\_SENSE 100ohm +-1% pull-up to VCC near processor

Trace Impedance = 27-33 ohm  
 Trace Length Matc < 25 mils



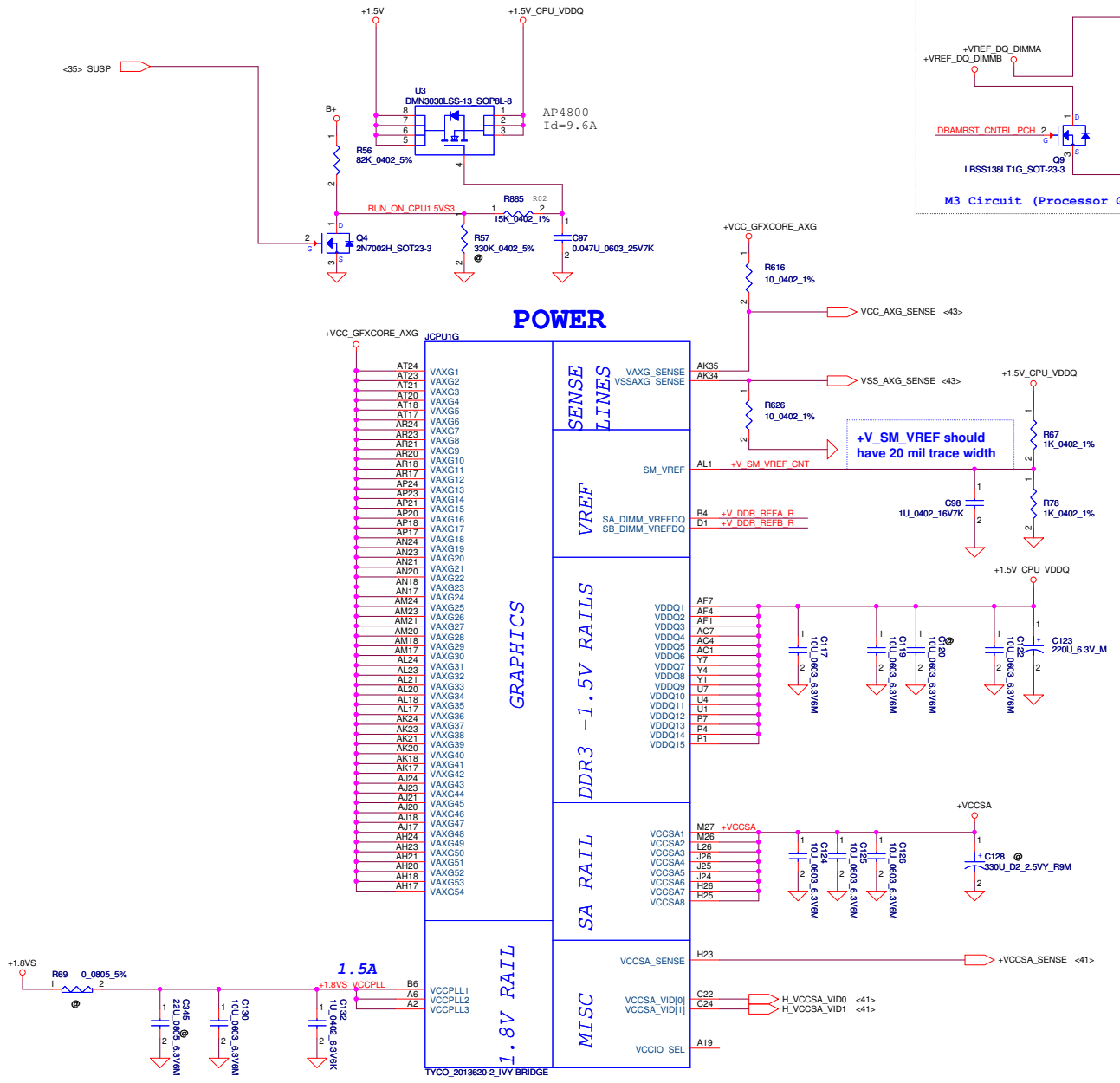
VSS\_SENSE 100ohm +-1% pull-down to GND near processor

TYCO\_2013620-2\_IVY BRIDGE

ME@

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**POWER**

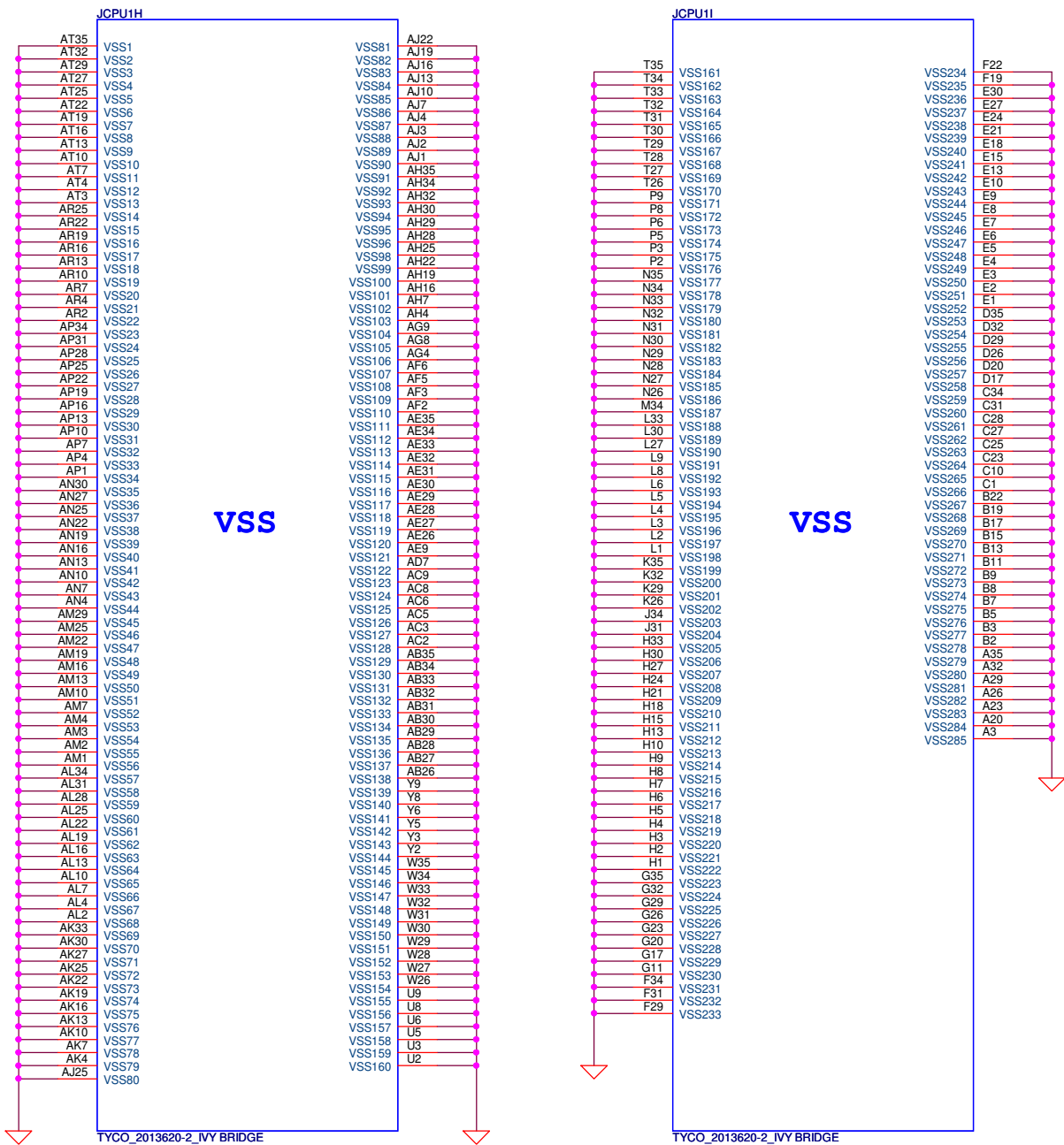
**GRAPHICS**

**1.8V RAIL**

IVY Bridge drives VCCIO\_SEL low  
 VCCP\_PWRCTRL:0  
 Sandy Bridge is NC for A19  
 VCCP\_PWRCTRL:1

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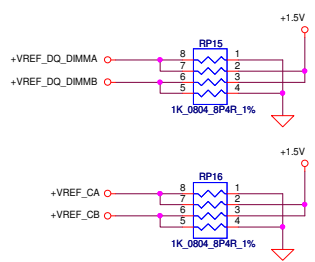
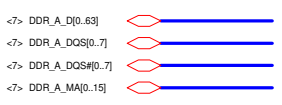
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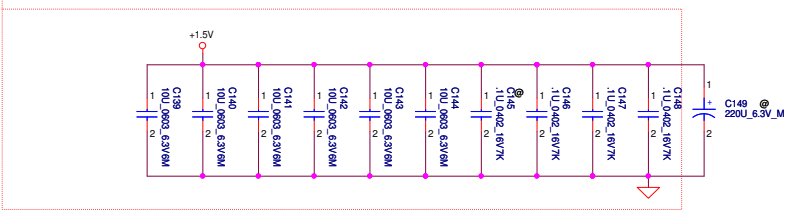
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Layout Note:  
Place near DIMM

OSCAN (220uF\_6.3V\_4.2L\_ESR17m)\*1=(SF000002Y00)  
(10uF\_0603\_6.3V)\*8  
(0.1uF\_402\_10V)\*4

Layout Note:  
Place near DIMM



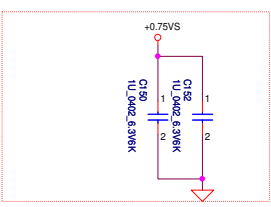
Layout Note:  
Place near DIMM

VDDQ (1.5V) =  
3\*330uF / 12m ohm (TOTAL FOR 2 SO-DIMM#)  
6\*0603 10uF (PER CONNECTOR)

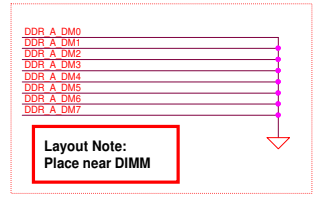
VTT (0.75V) =  
3\*0805 10uF 4\*0402 1uF

VREF =  
1\*0402 0.1uF 1\*0402 2.2uF

VDDSPD (3.3V) =  
1\*0402 0.1uF 1\*0402 2.2uF

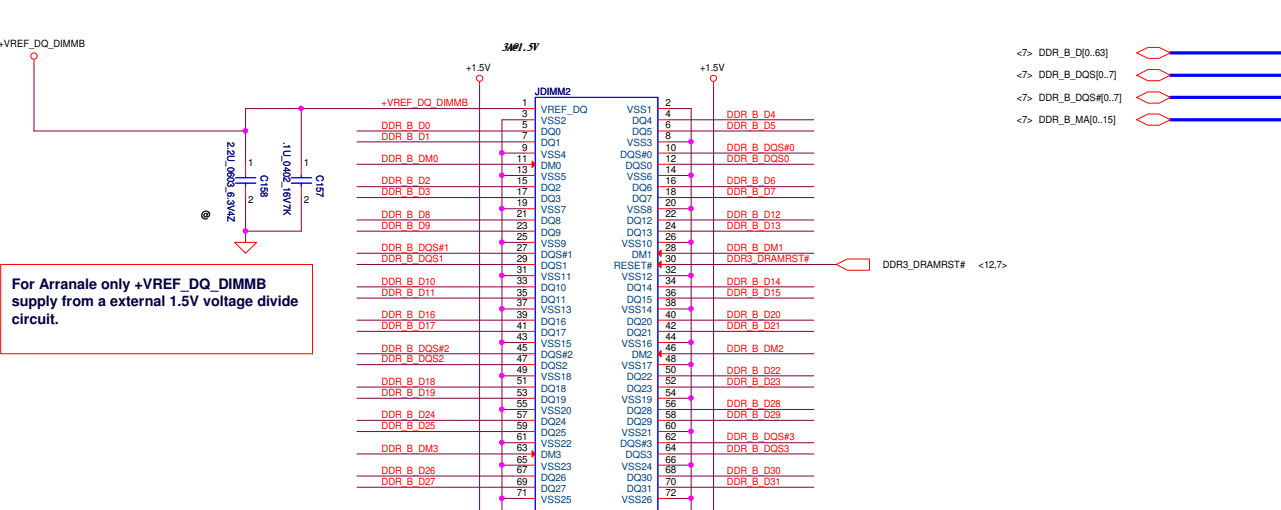


7/28 Update connect GND directly



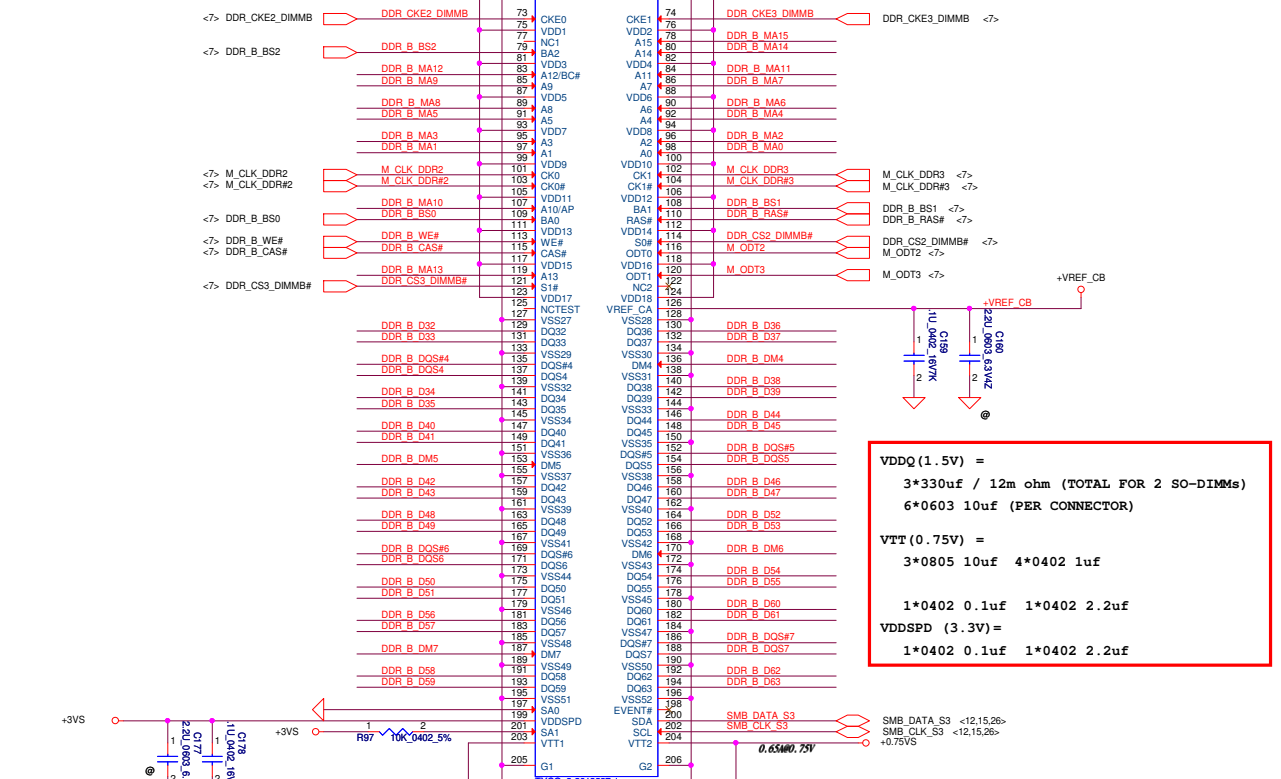
Layout Note:  
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			LA-9632P		0
			Date:	Wednesday, February 27, 2013	ISheet 12 of 60



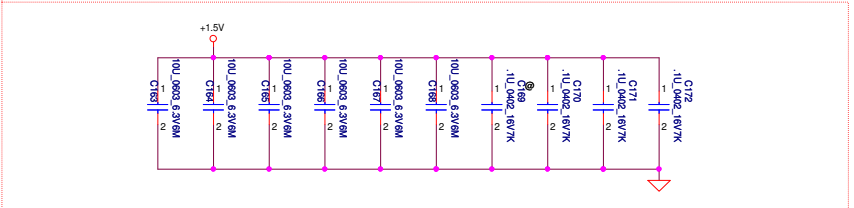
For Arranale only +VREF\_DQ\_DIMMB supply from a external 1.5V voltage divide circuit.

- <-7> DDR\_B\_D[0..63]
- <-7> DDR\_B\_DQS[0..7]
- <-7> DDR\_B\_DQS# [0..7]
- <-7> DDR\_B\_MA[0..15]

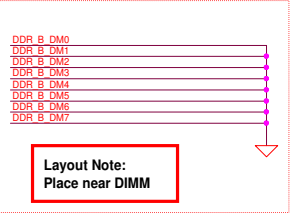
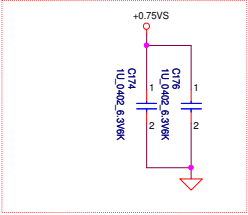


Layout Note:  
Place near DIMM

(10uF\_0603\_6.3V) \*8  
(0.1uF\_402\_10V) \*4

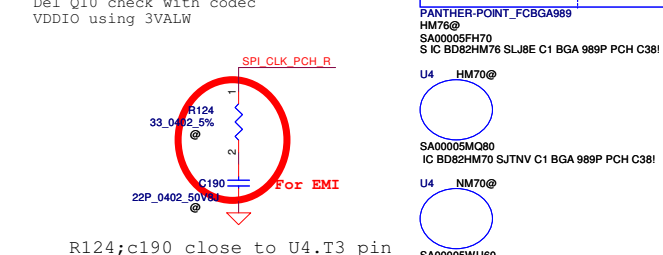
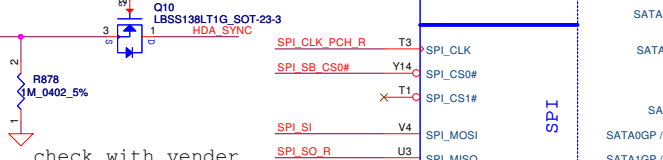
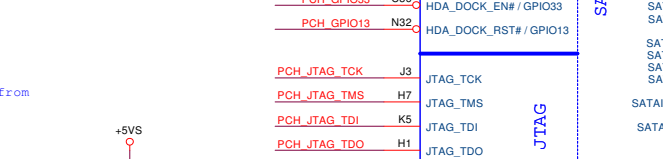
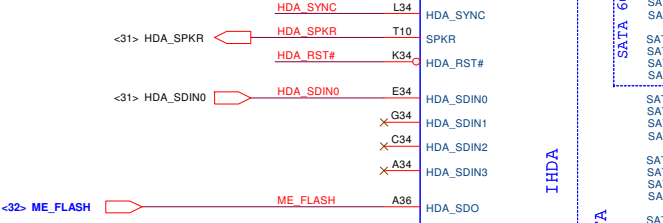
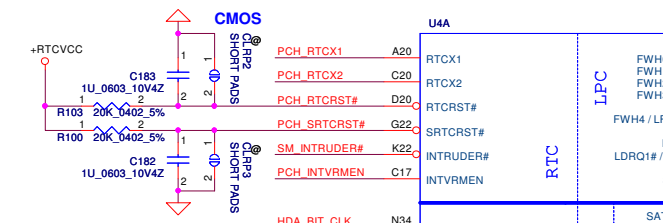
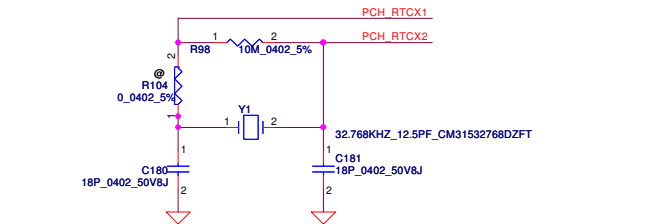
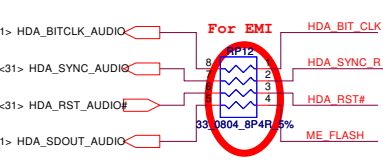
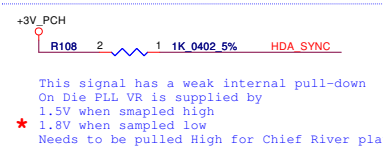
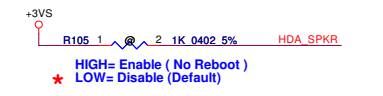
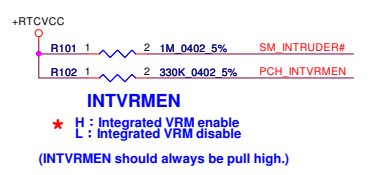
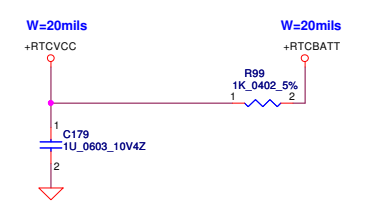


Layout Note:  
Place near DIMM



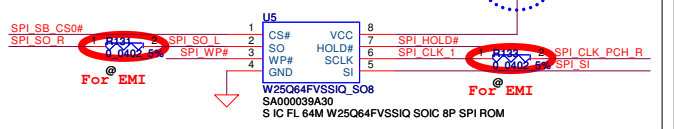
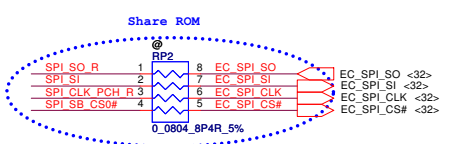
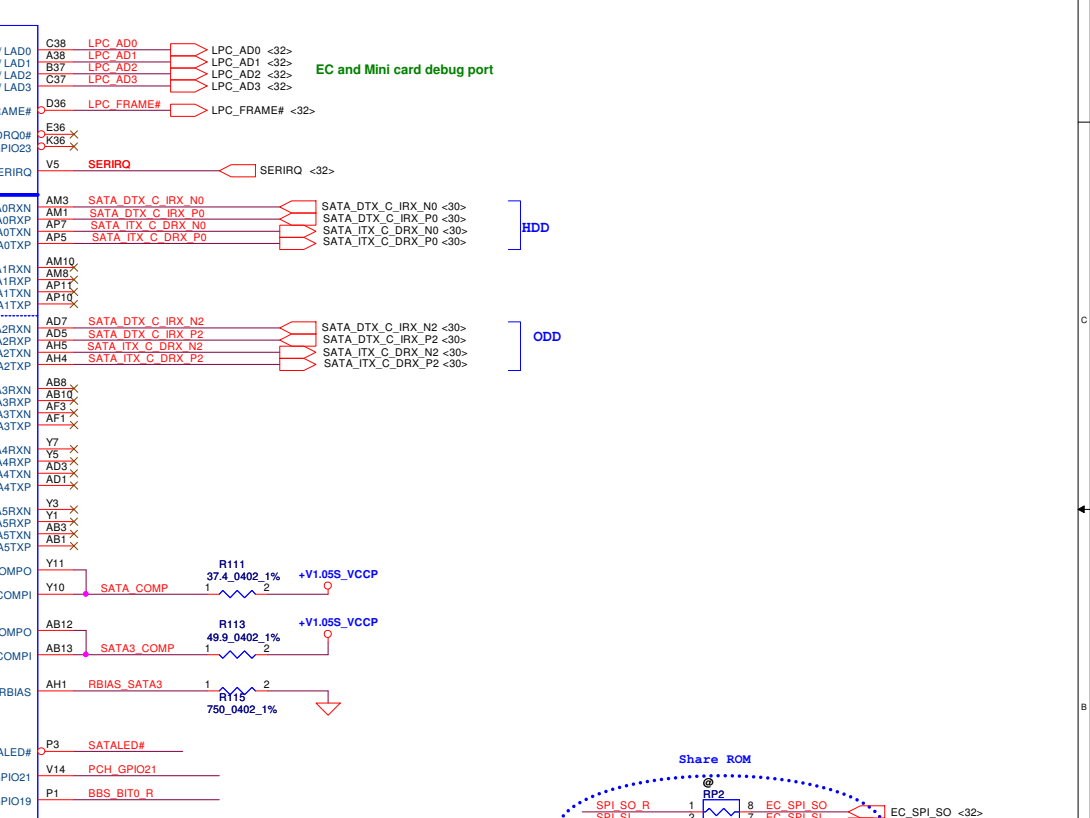
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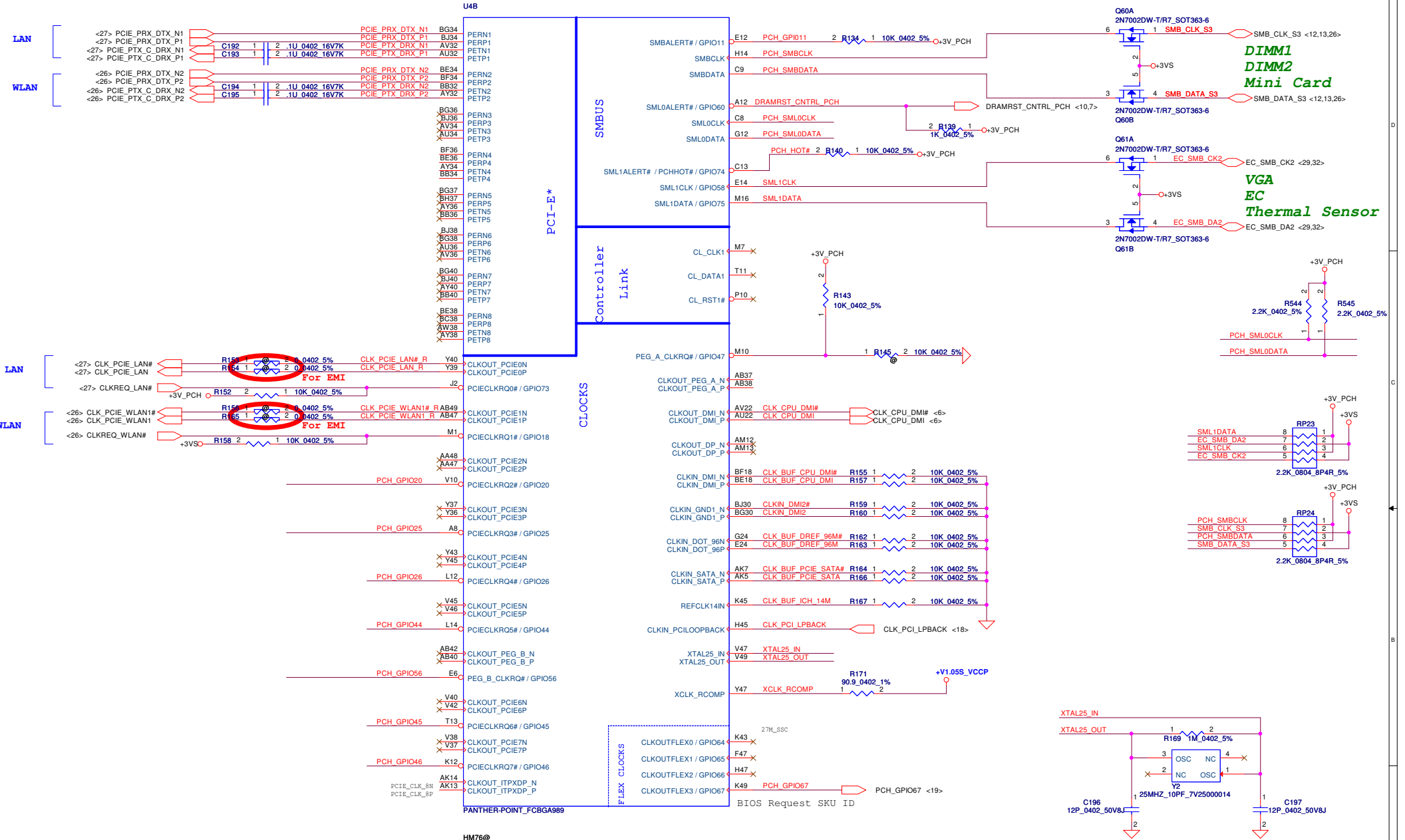


CLR2	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

CLR3	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



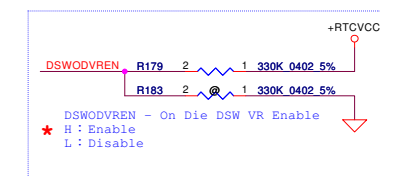
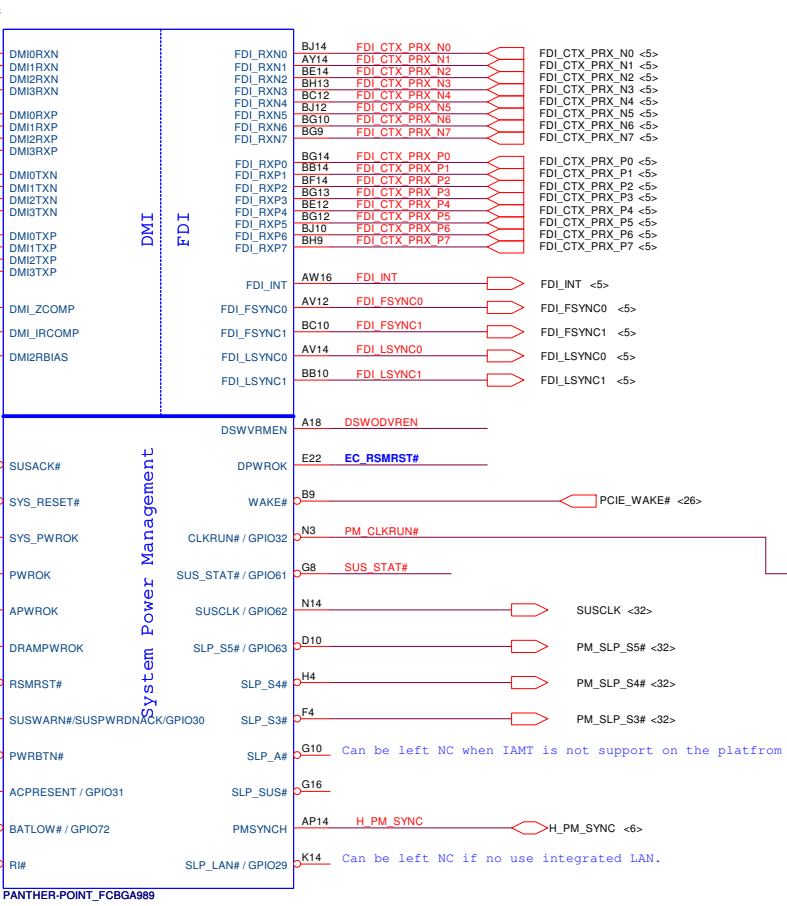
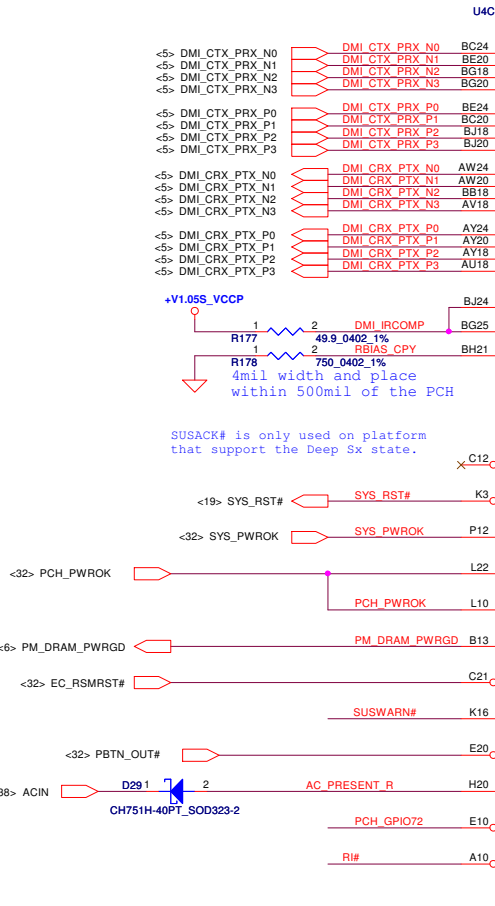
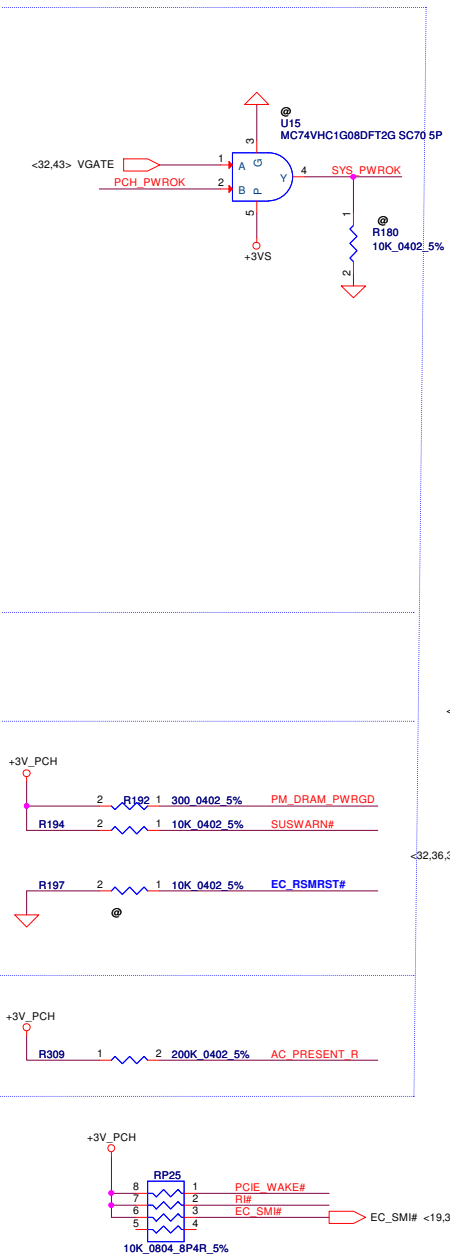
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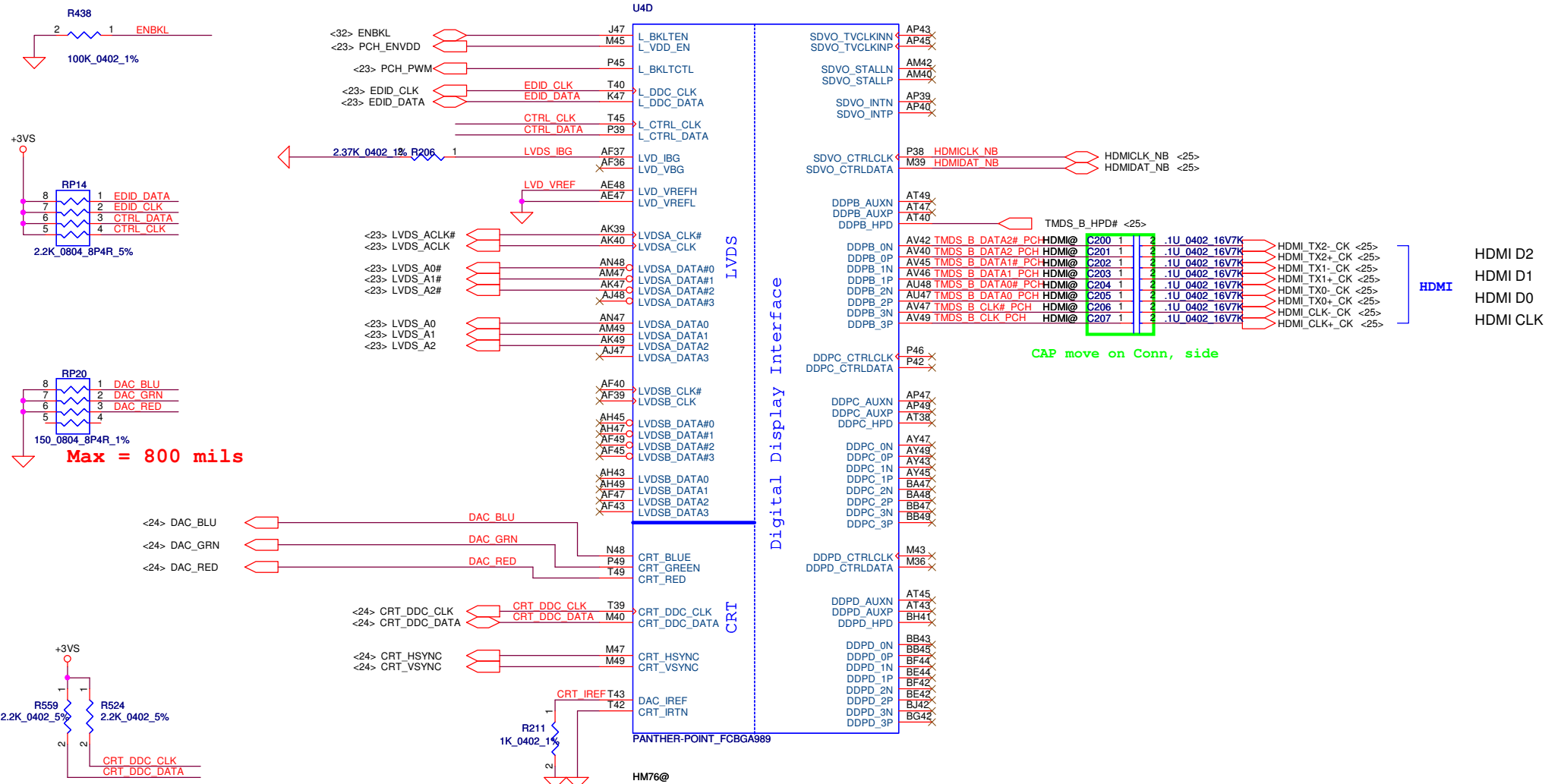
Security Classification	Compal Secret Data	
Issued Date	2011/06/15	Deciphered Date
		2012/07/11

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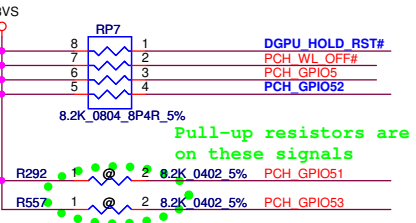
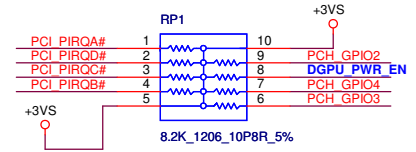
<b>Compal Electronics, Inc.</b>	
<b>PCH (3/9) DMI,FDI,PM,</b>	
Document Number	Rev
<b>LA-9632P</b>	1.0
Date: Wednesday, February 27, 2013	Sheet 16 of 60

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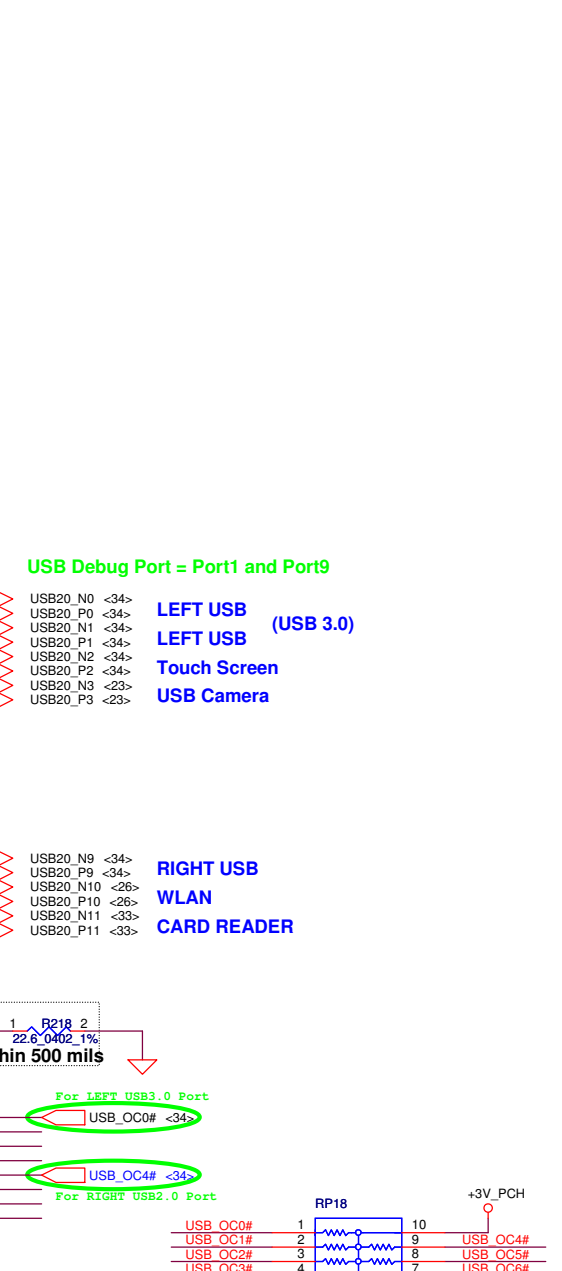
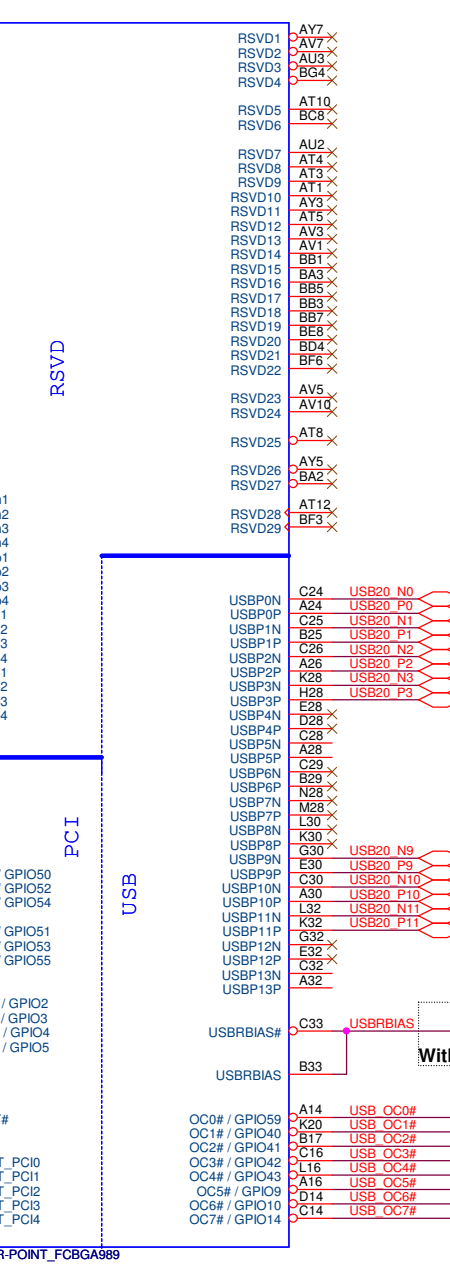
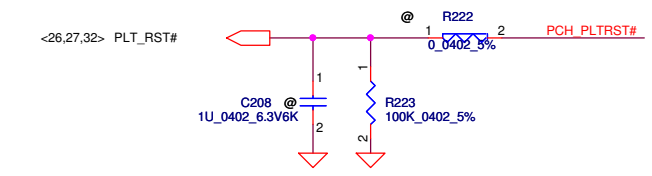
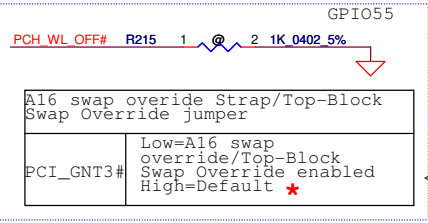
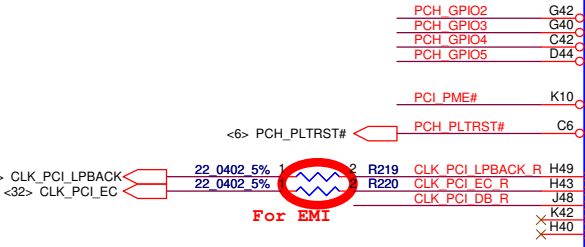
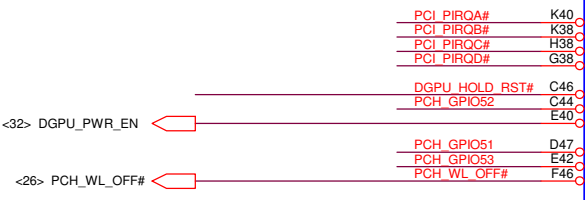
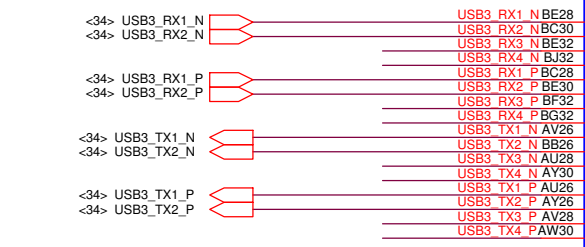


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Pull-up resistors are not required on these signals

Boot BIOS Strap bit1 BBS1		
Bit11	Bit10	Boot BIOS Destination
0	1	Reserved
1	0	Reserved
1	1	★ SPI (Default)
0	0	LPC



USB Debug Port = Port1 and Port9

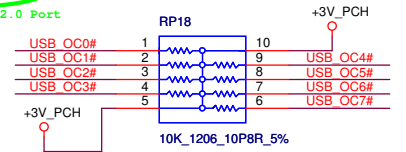
LEFT USB (USB 3.0)  
Touch Screen  
USB Camera

RIGHT USB  
WLAN  
CARD READER

Within 500 mils

For LEFT USB3.0 Port  
USB\_OC0# <34>

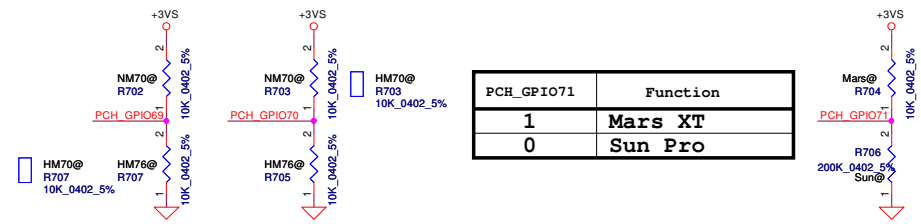
For RIGHT USB2.0 Port  
USB\_OC4# <34>



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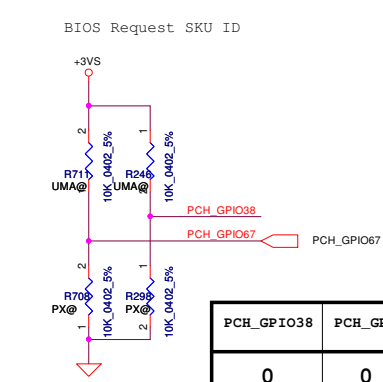
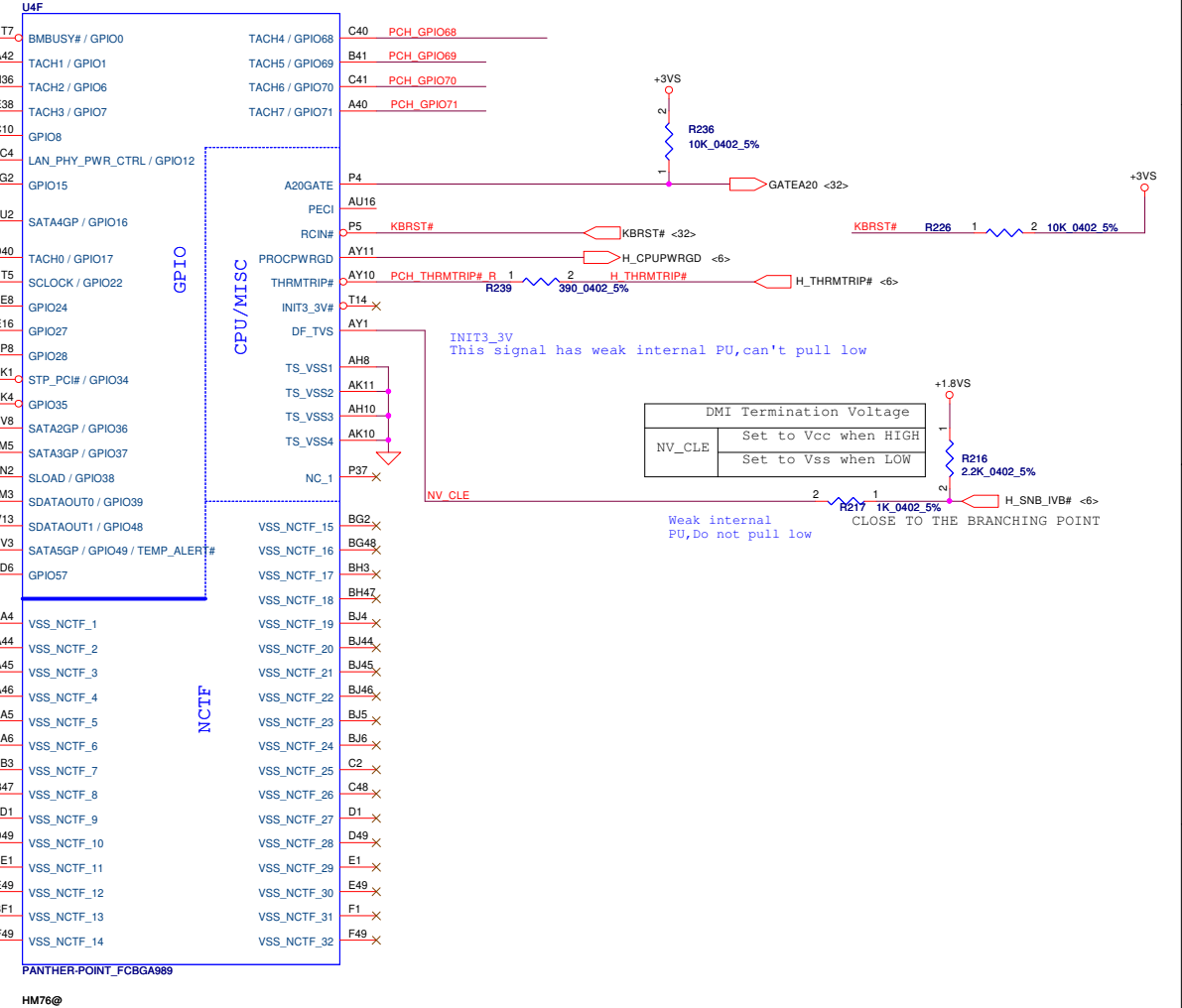
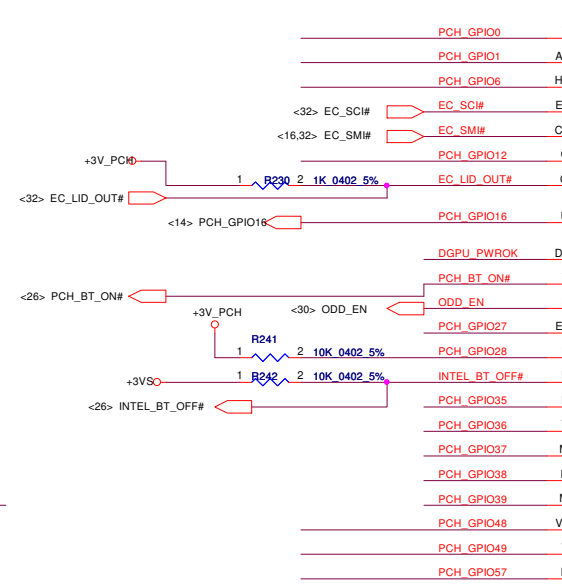
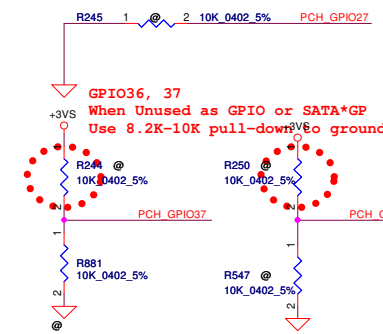
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PCH_GPIO69	PCH_GPIO70	Function
1	1	NM70
1	0	Reserved
0	1	HM70
0	0	HM76



PCH_GPIO71	Function
1	Mars XT
0	Sun Pro

**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
\* H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable

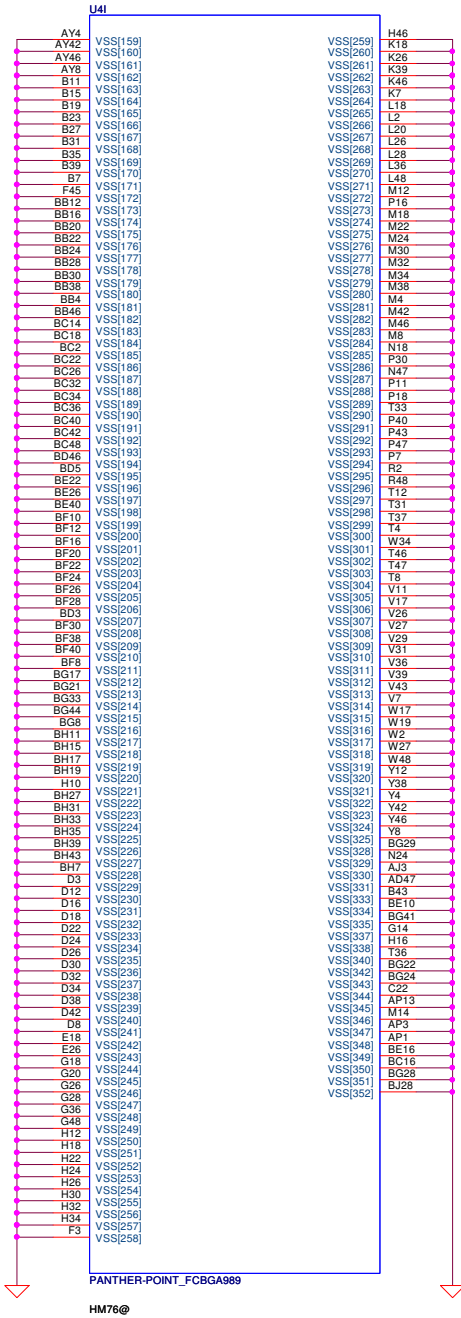
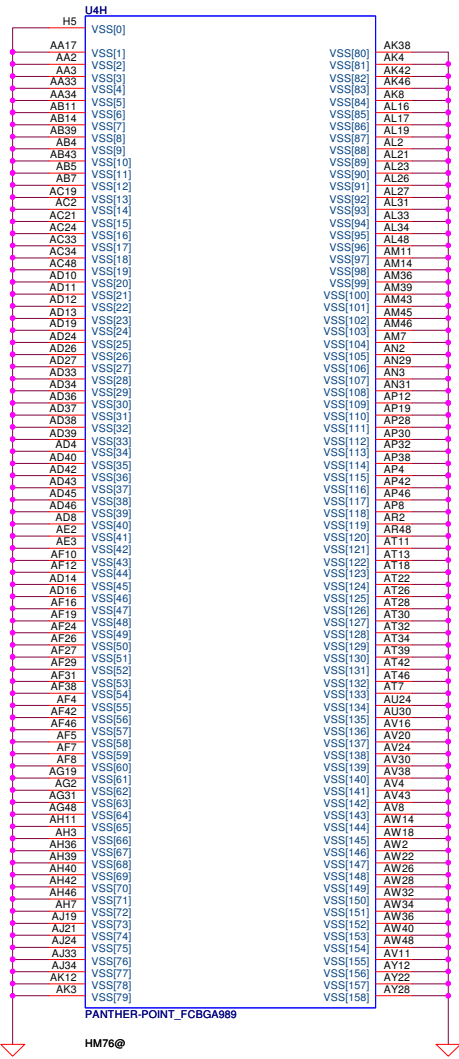


PCH_GPIO38	PCH_GPIO67	Function
0	0	SG (Optimus / PX)
0	1	Reserved
1	0	DIS
1	1	UMA

Security Classification		Compal Secret Data		Title	
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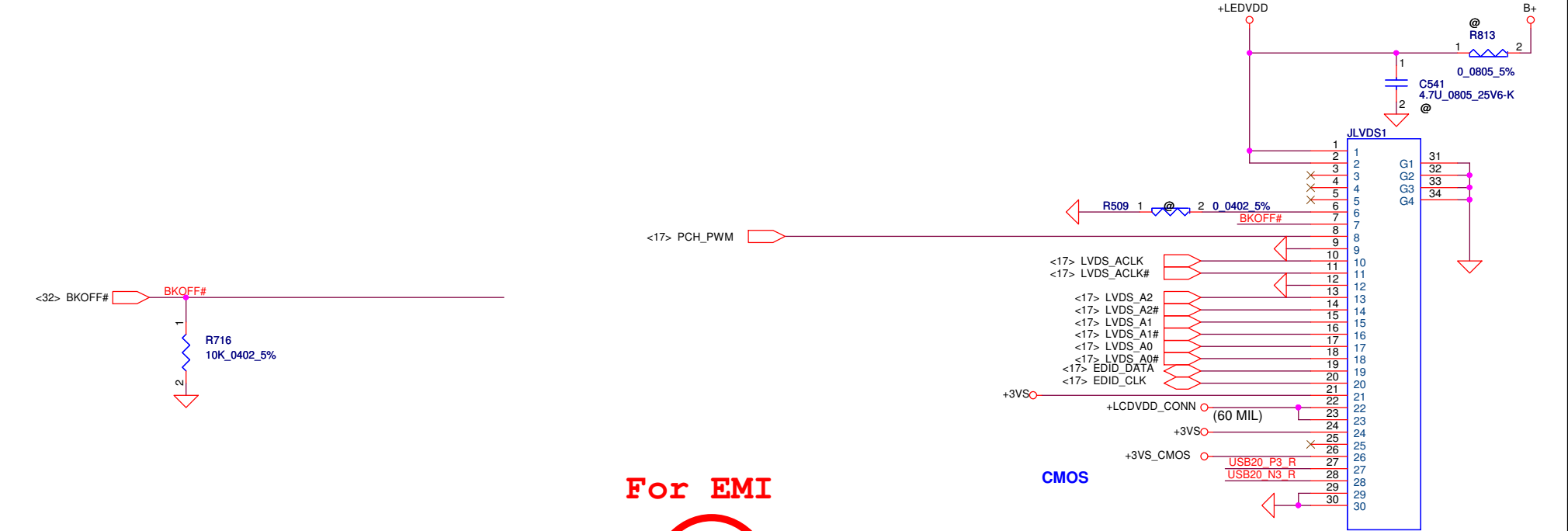
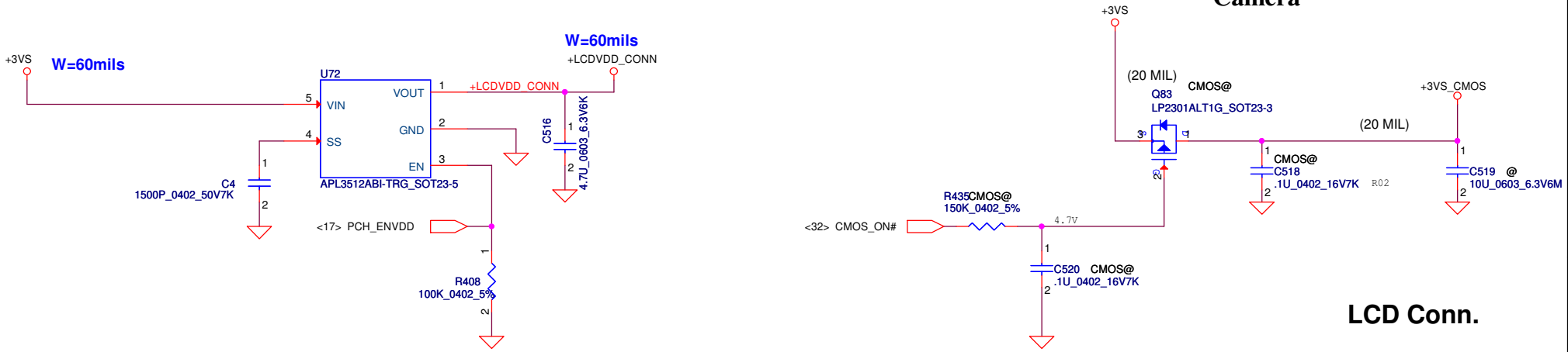




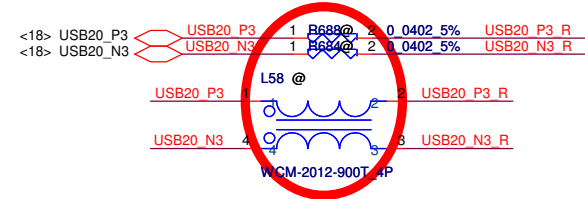
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# LCD POWER CIRCUIT

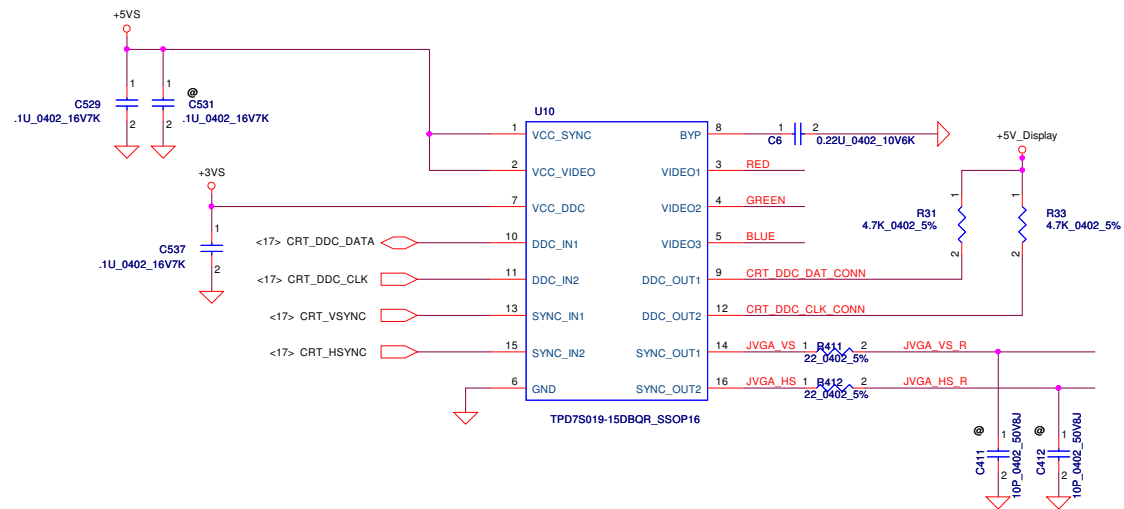
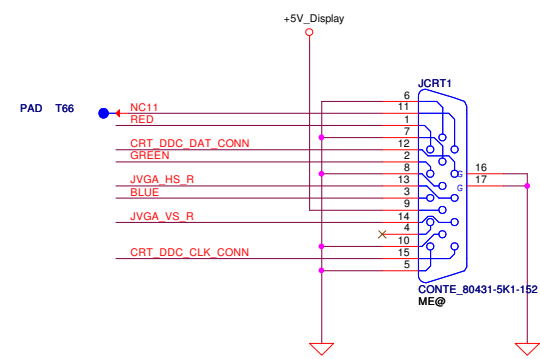
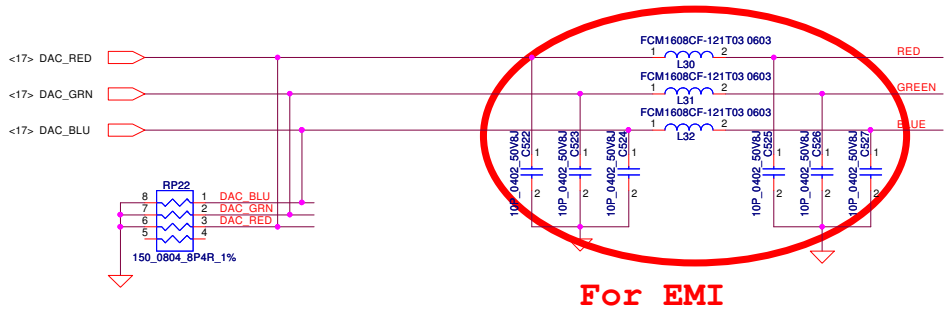


**For EMI**



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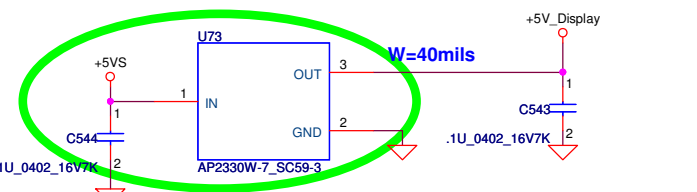
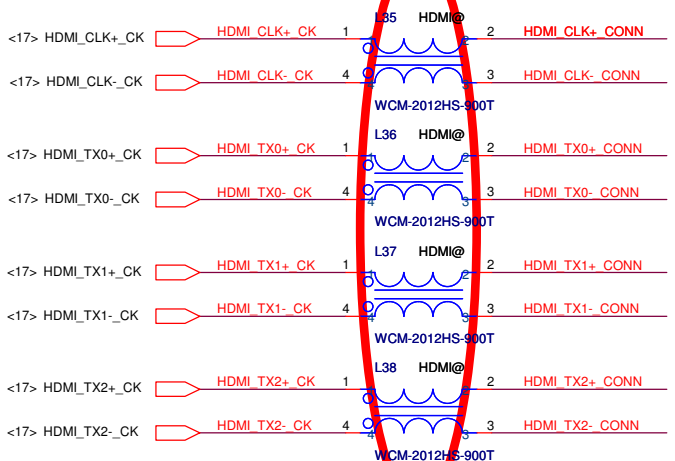


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Date: Wednesday, February 27, 2013				Rev 1.0
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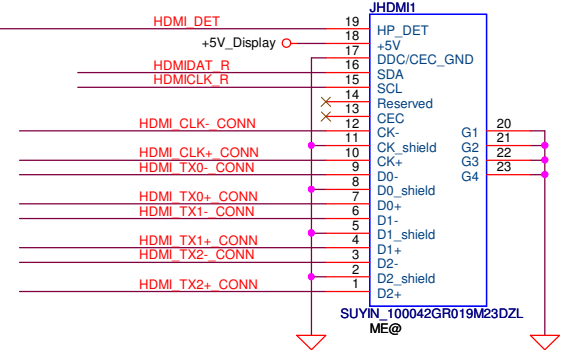
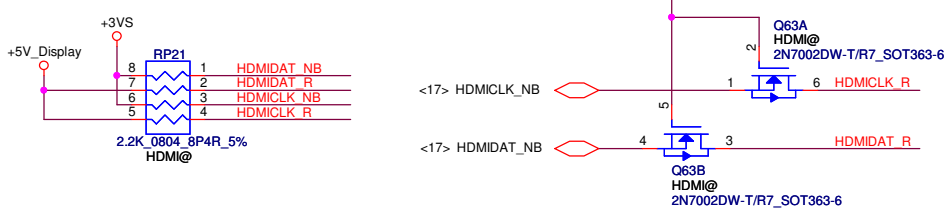
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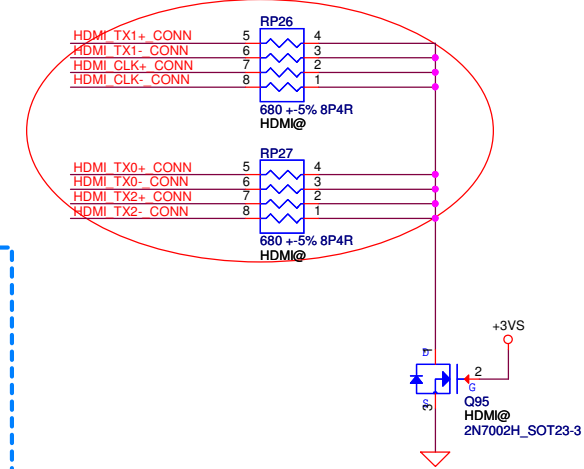
**For CRT and HDMI**



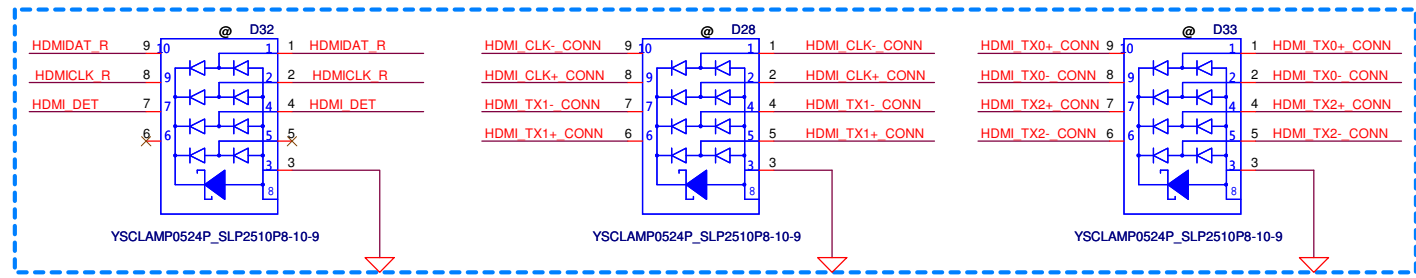
**Pull up R for PCH OR VGA SIDE**



**DVT**

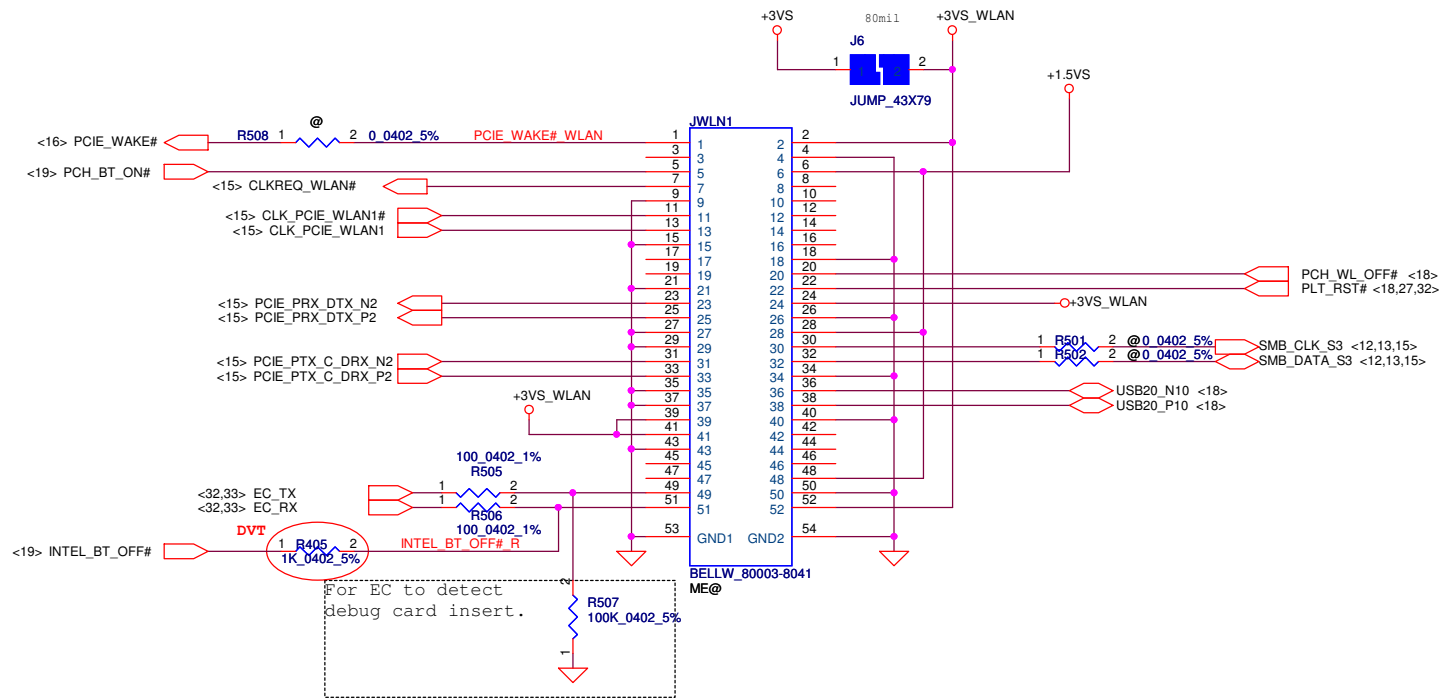


**ESD**



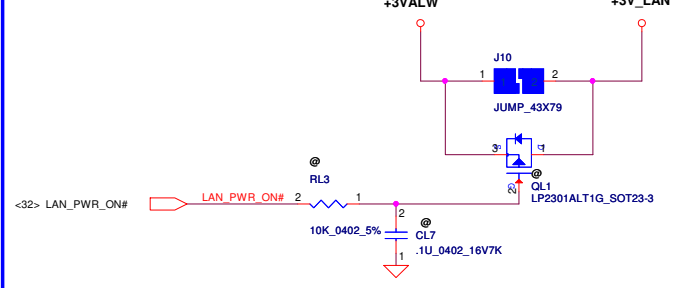
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				Date: Wednesday, February 27, 2013	Sheet 25 of 60

# Mini Card for WLAN/WiMAX(Half)

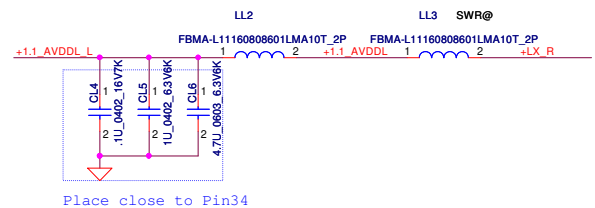
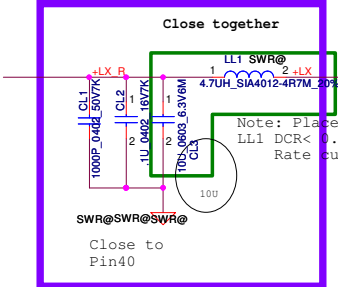
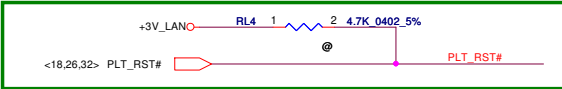


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title <b>Mini-Card/NEW Card/SIM</b>	
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				Date	Wednesday, February 27, 2013
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				Rev	1.0

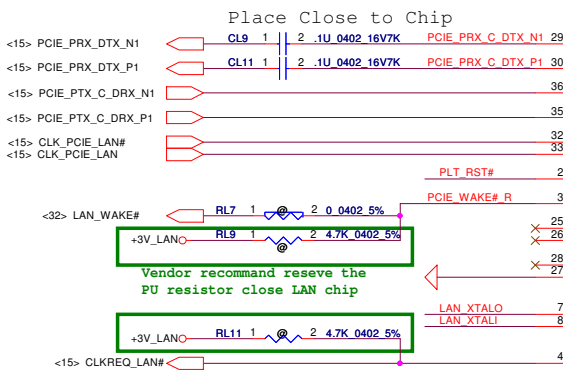
**For LAN & Green CLK**



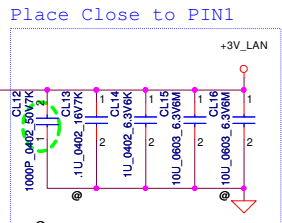
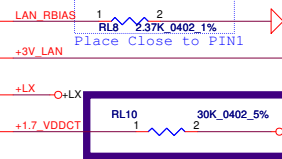
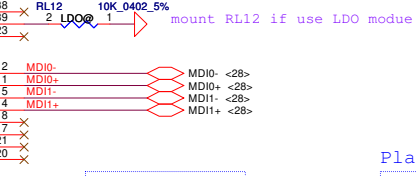
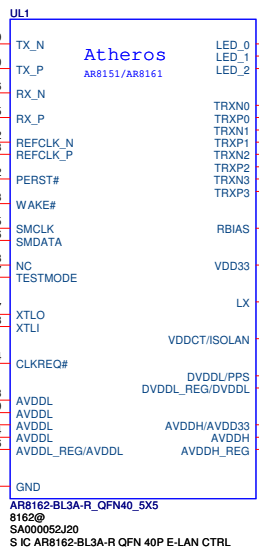
Vendor recommend reseve the PU resistor close LAN chip



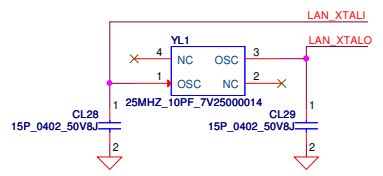
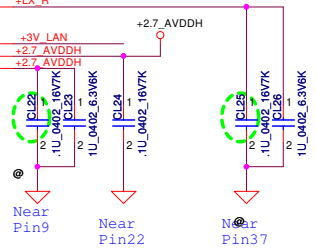
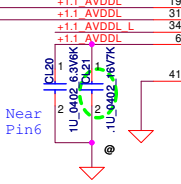
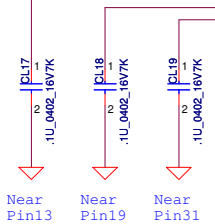
UL1 8172@  
QCA8172-BL3A-R  
SA00005410  
S IC QCA8172-BL3A-R QFN 40P E-LAN CTRL



Vendor recommend reseve the PU resistor close LAN chip



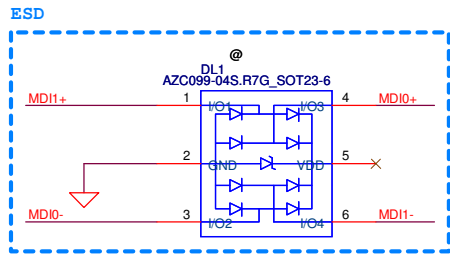
don't @ (could be B C cost done)



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				LAN-AR8162/8172	
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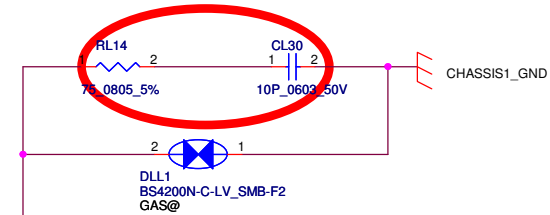
DL1  
1'S PN:SC300001G00  
2'S PN:SC300002E00

Place Close to TL1



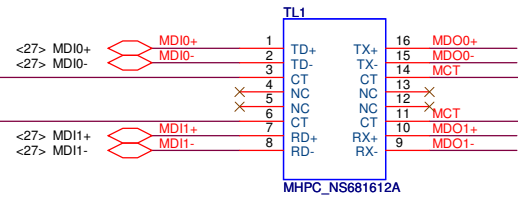
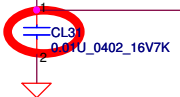
Reserve gas tube for EMI go rural solution

For EMI

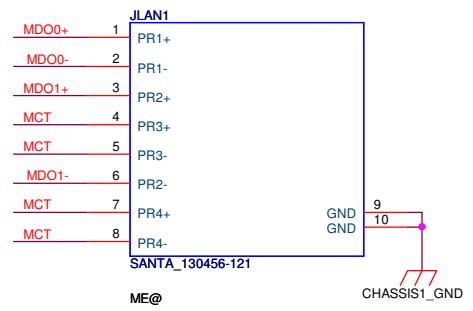
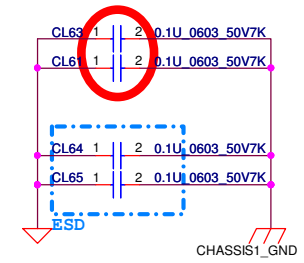


Place Close to TL1

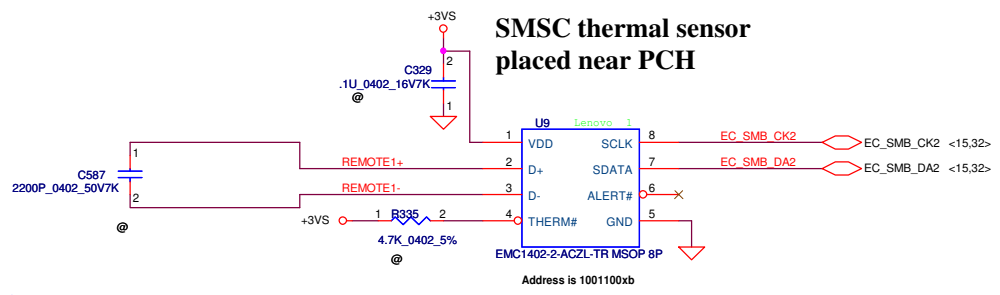
For EMI



For EMI

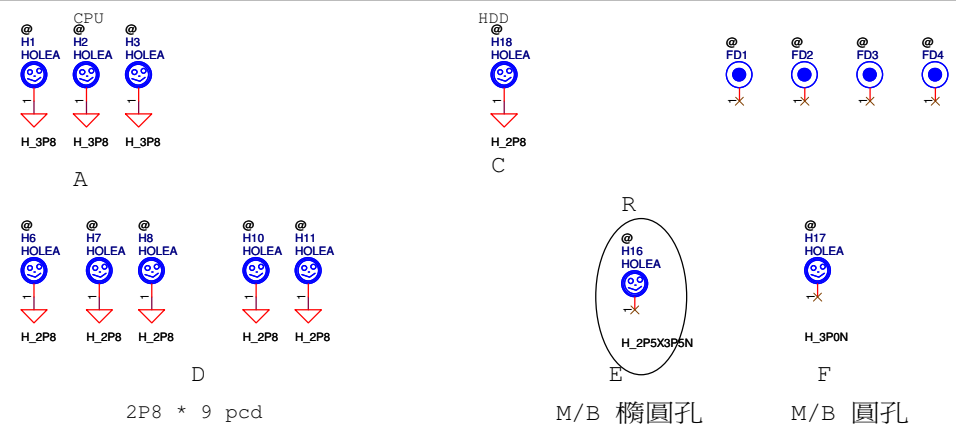
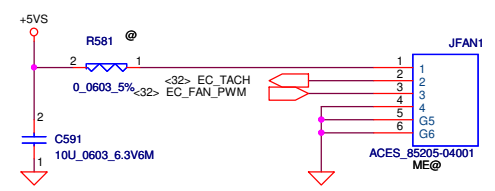


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					LA-9632P
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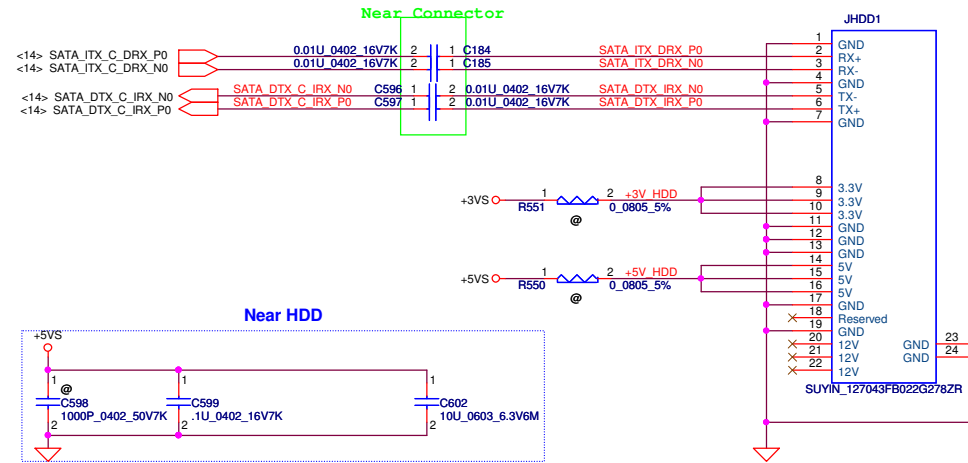
REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

FAN1 Conn

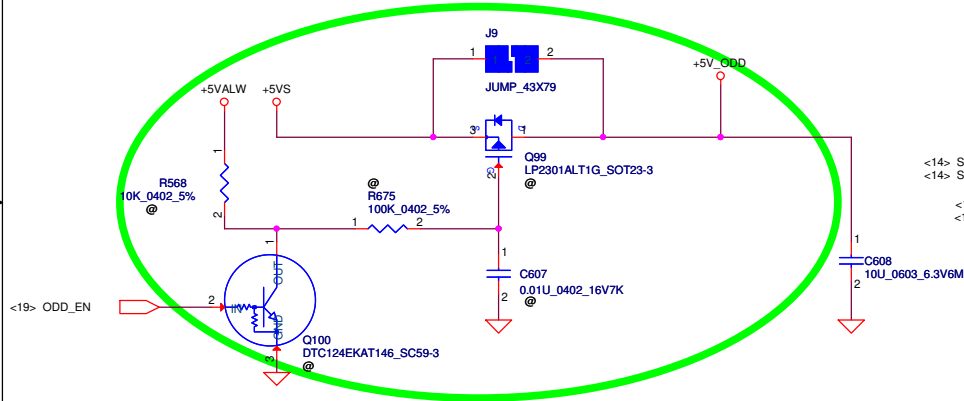


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				LA-9632P
				Revision
				1.0
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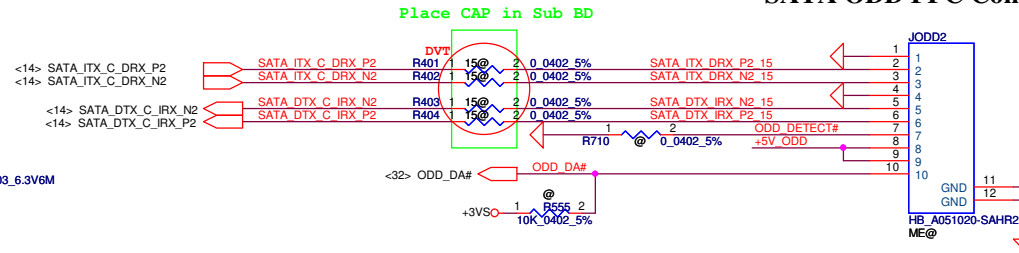
### SATA HDD Conn.



### ODD Power Control

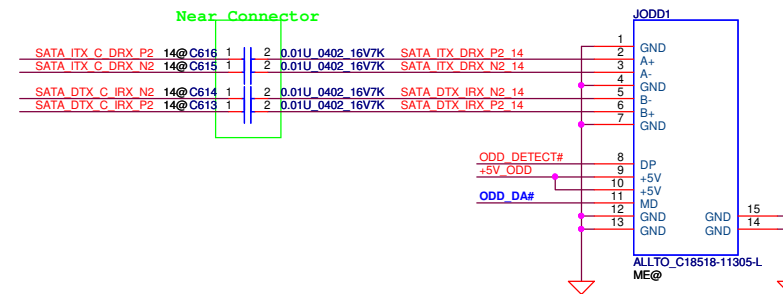


### FOR 15" SATA ODD FFC Conn.



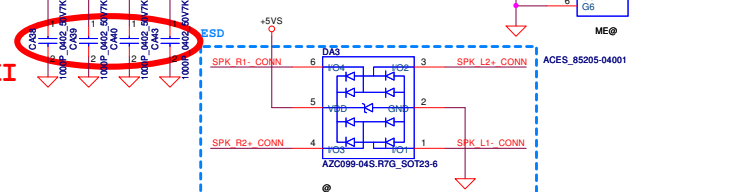
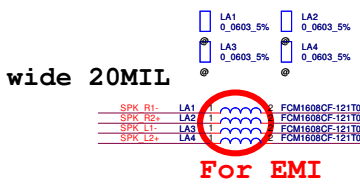
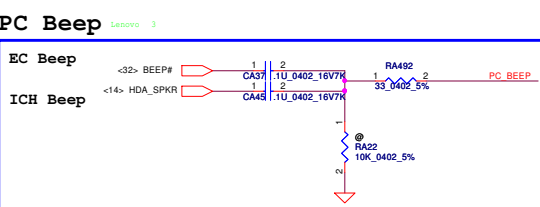
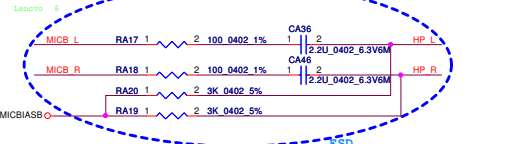
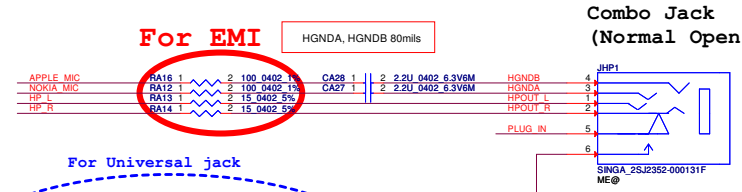
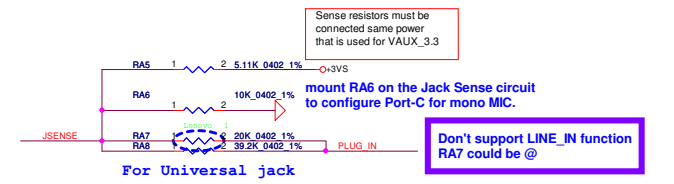
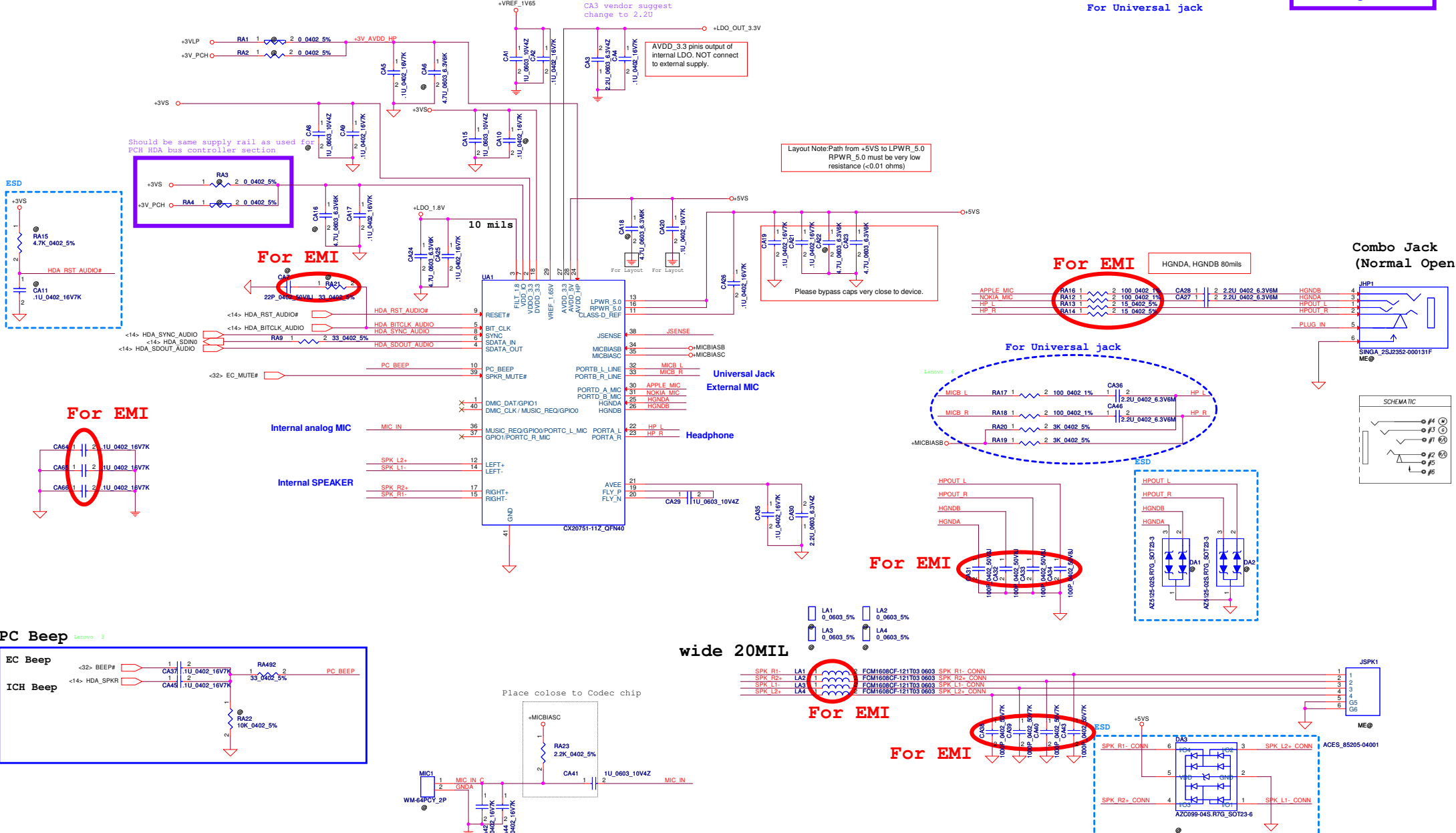
Co-lay

### FOR 14" SATA ODD Conn.

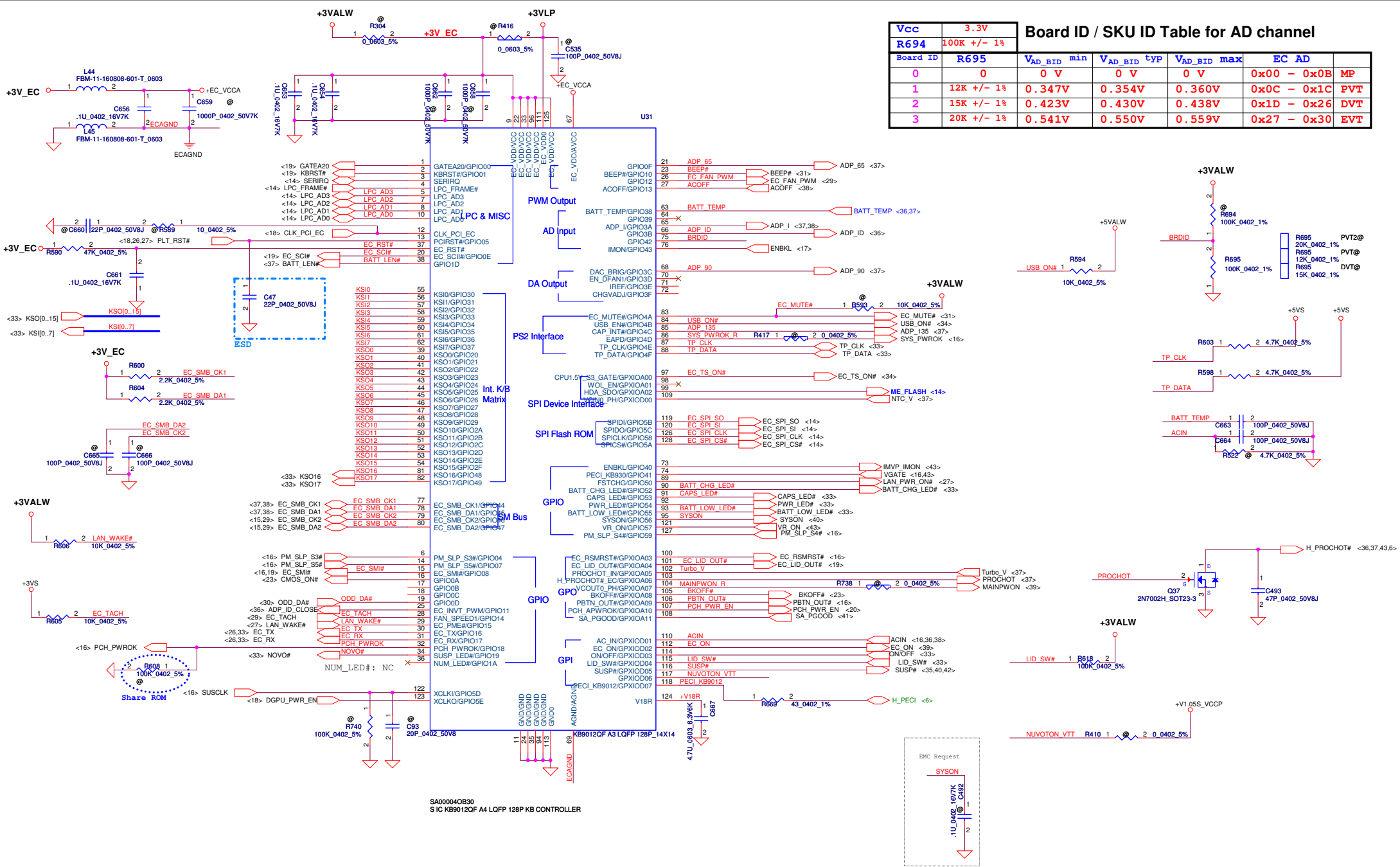


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www.vinalix.vn			Compal Electronics, Inc. <b>HDD/ODD/BT Connector</b>	
Size	Document Number	Rev	1.0	
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**CX20751**  
**High Definition Audio Codec SoC**  
**With Integrated Class-D Stereo**  
**Amplifier.**  
**An integrated 5 V to 3.3 V Low-dropout**  
**voltage regulator (LDO).**  
**An integrated 3.3 V to 1.8V Low-dropout**  
**voltage regulator (LDO).**



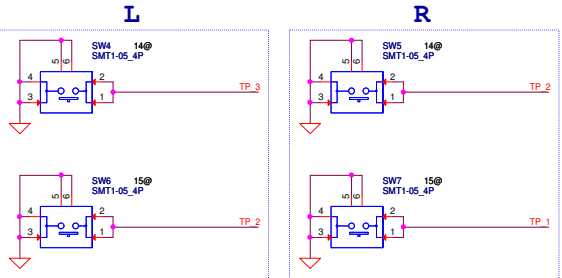
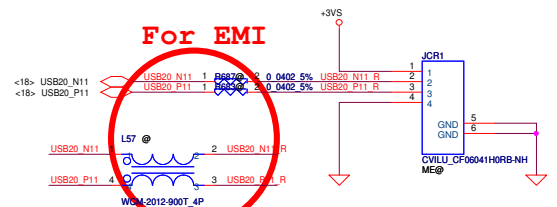
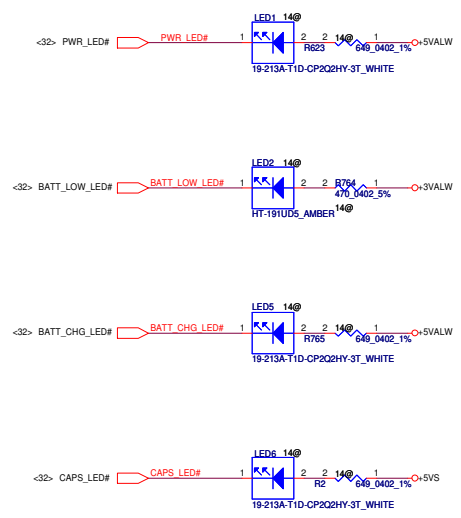
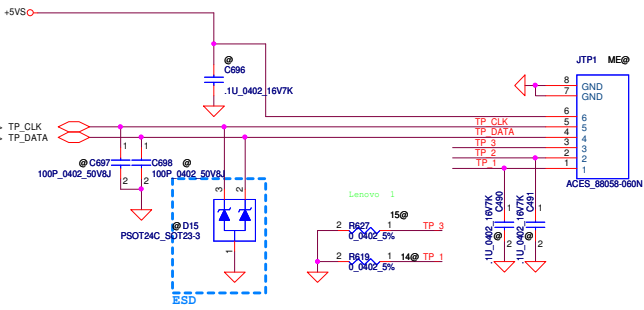
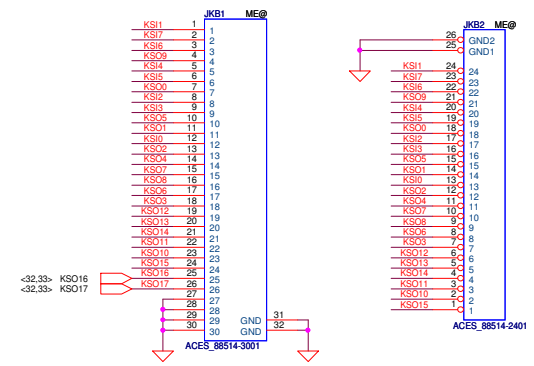
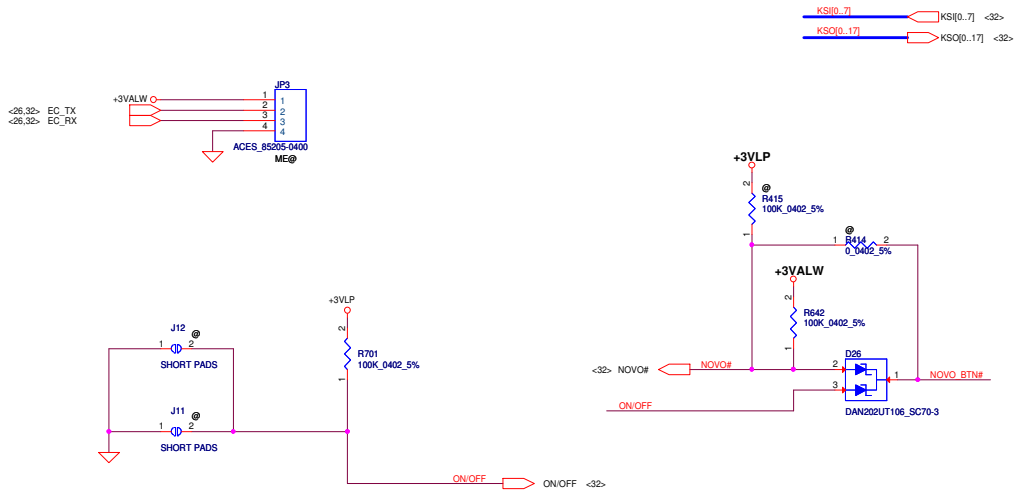
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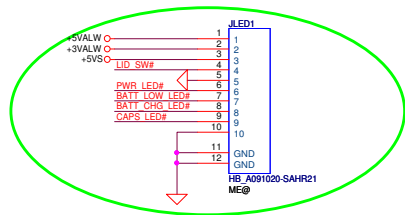
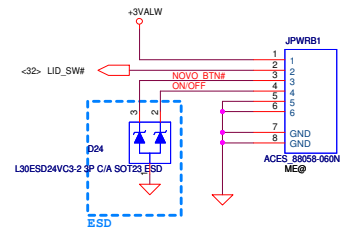
Vcc		3.3V			Board ID / SKU ID Table for AD channel		
R694	R695	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC AD		
0	0	0 V	0 V	0 V	0x00 - 0x0B	MP	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	PVT	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	DVT	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	EVT	

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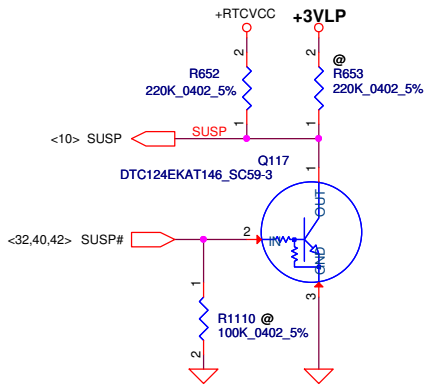
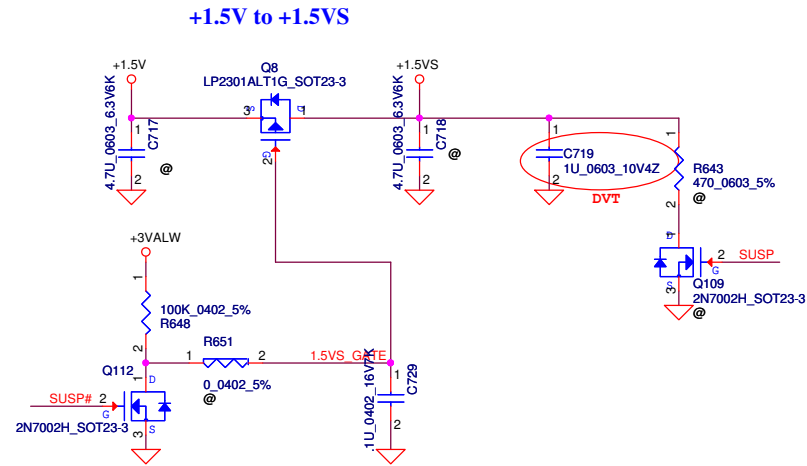
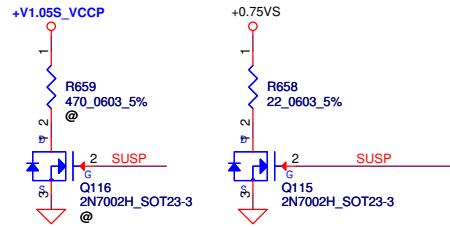
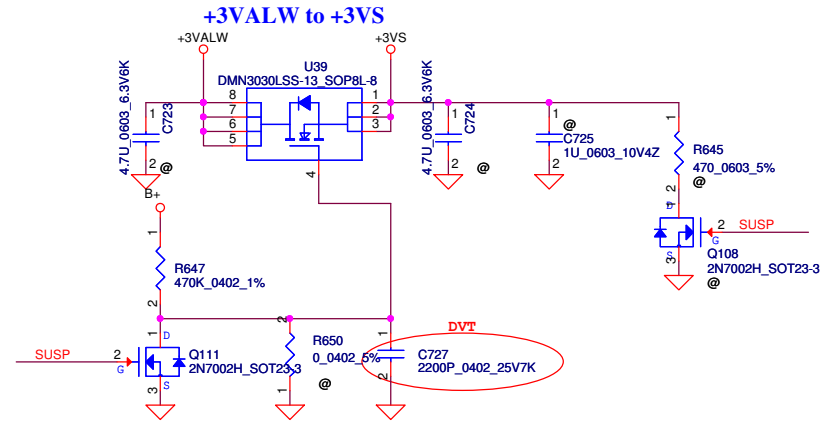
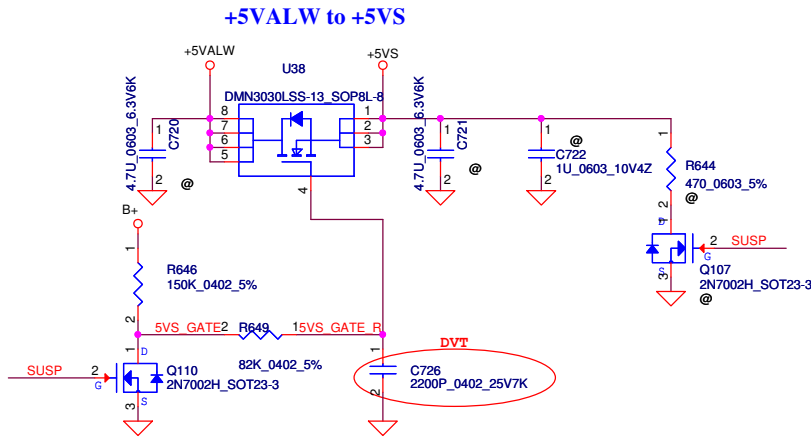


15/17"		14"	
1	VCC	1	VCC
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	L
5	L	5	R
6	R	6	GND

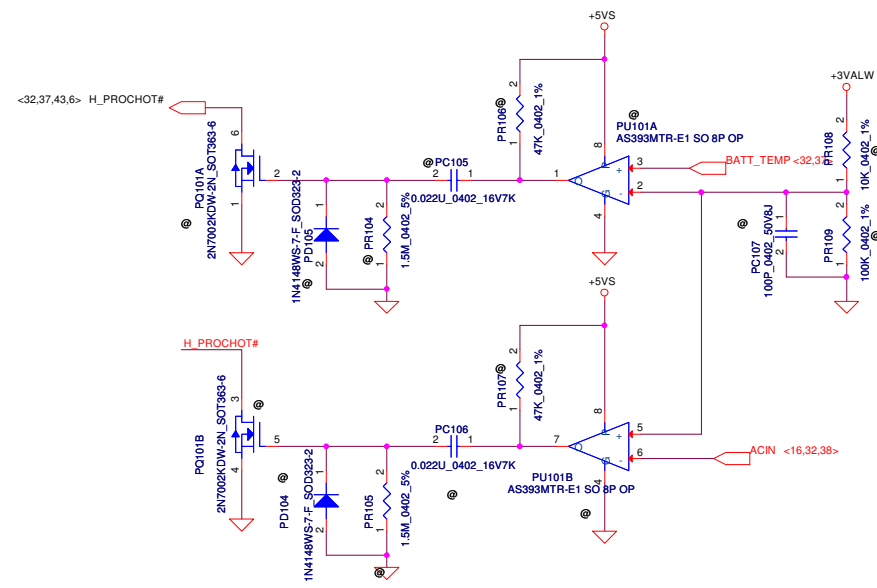
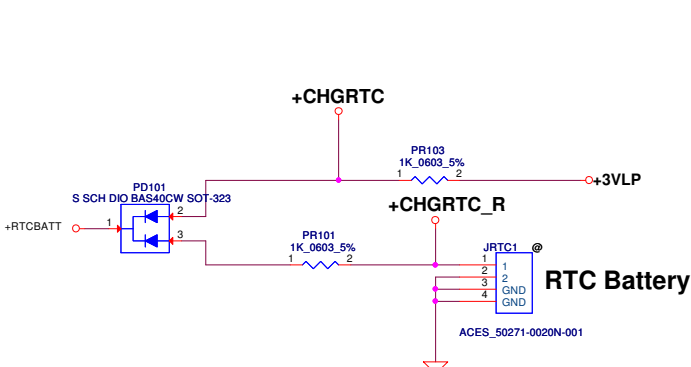
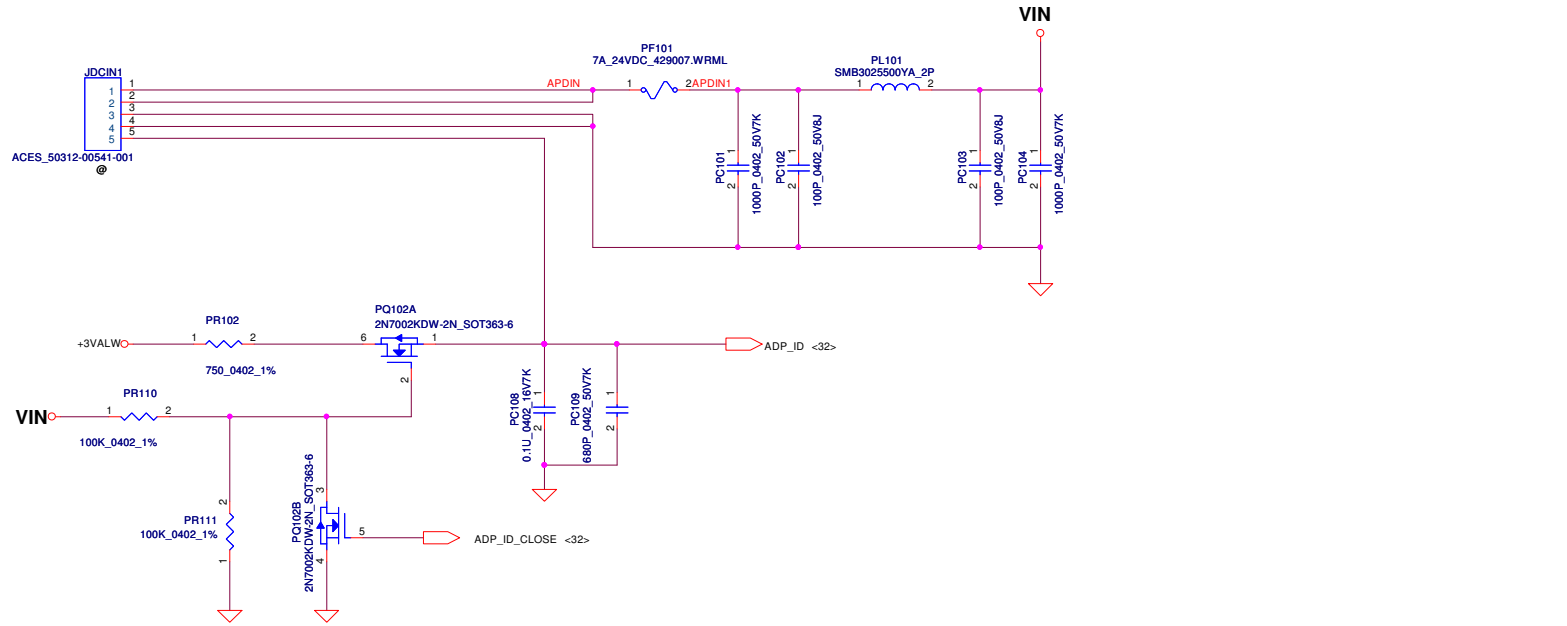


For 15"



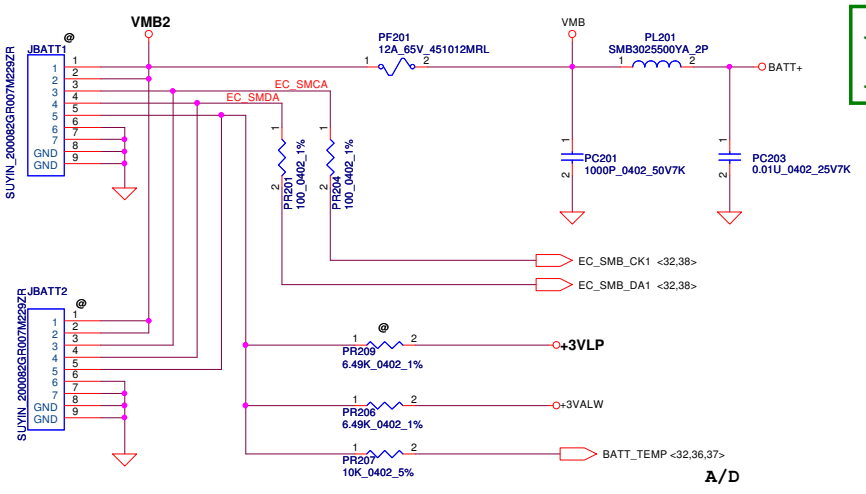


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				Gx00	1.0
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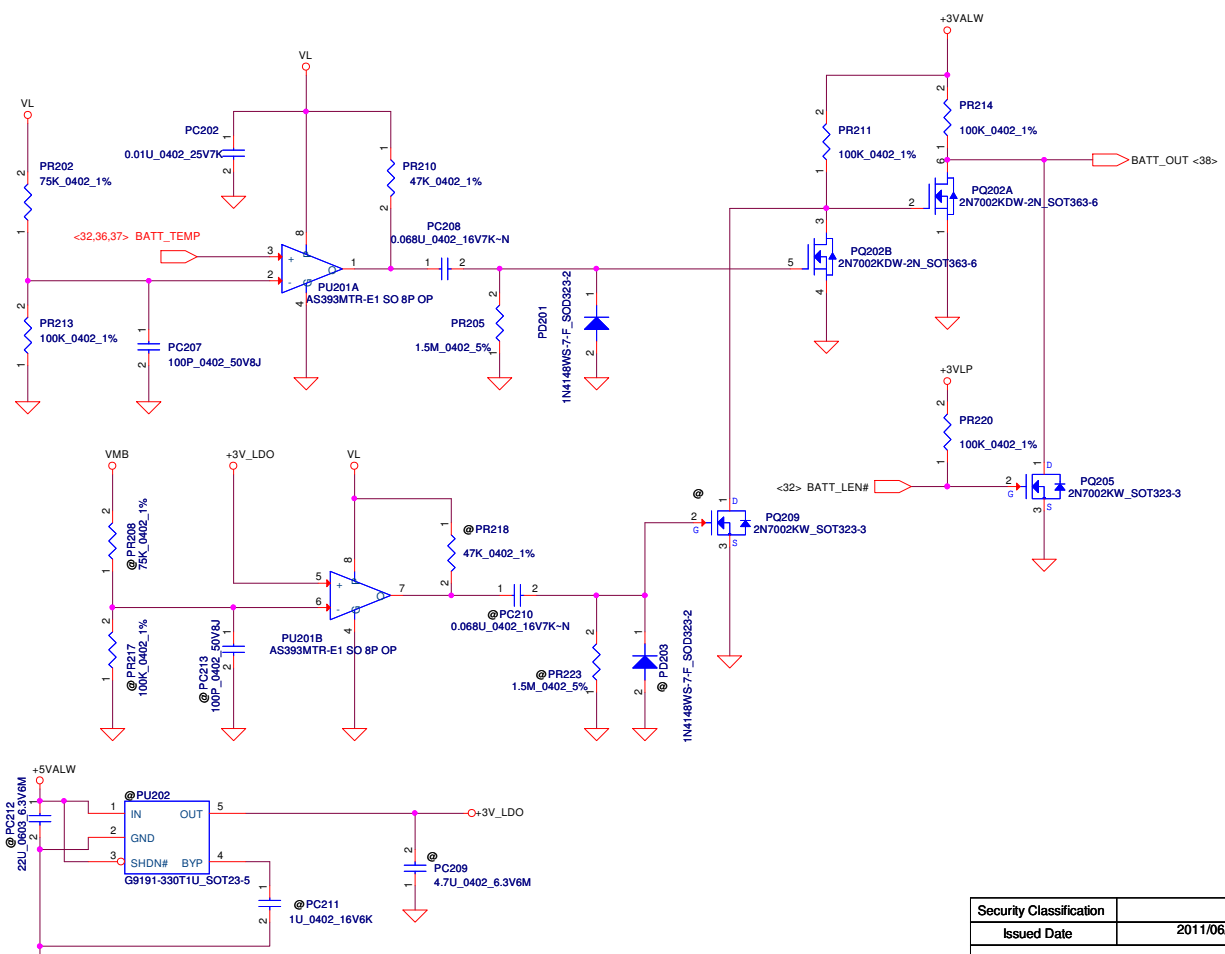
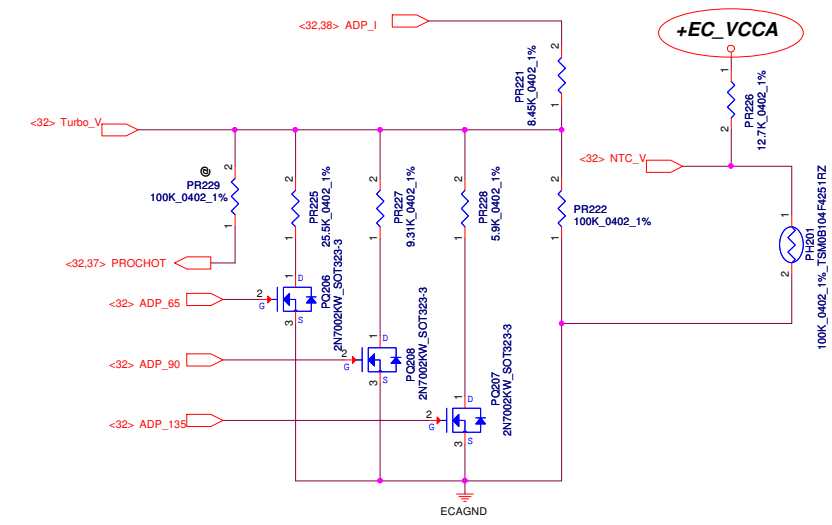
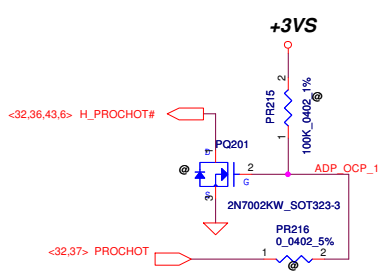
www.vitalix.vn



JBATT1 ---> 15"  
JBATT2 ---> 14"

PH201 under CPU bottom side :  
CPU thermal protection at 93 +/-3 degree C  
Recovery at 56 +/-3 degree C

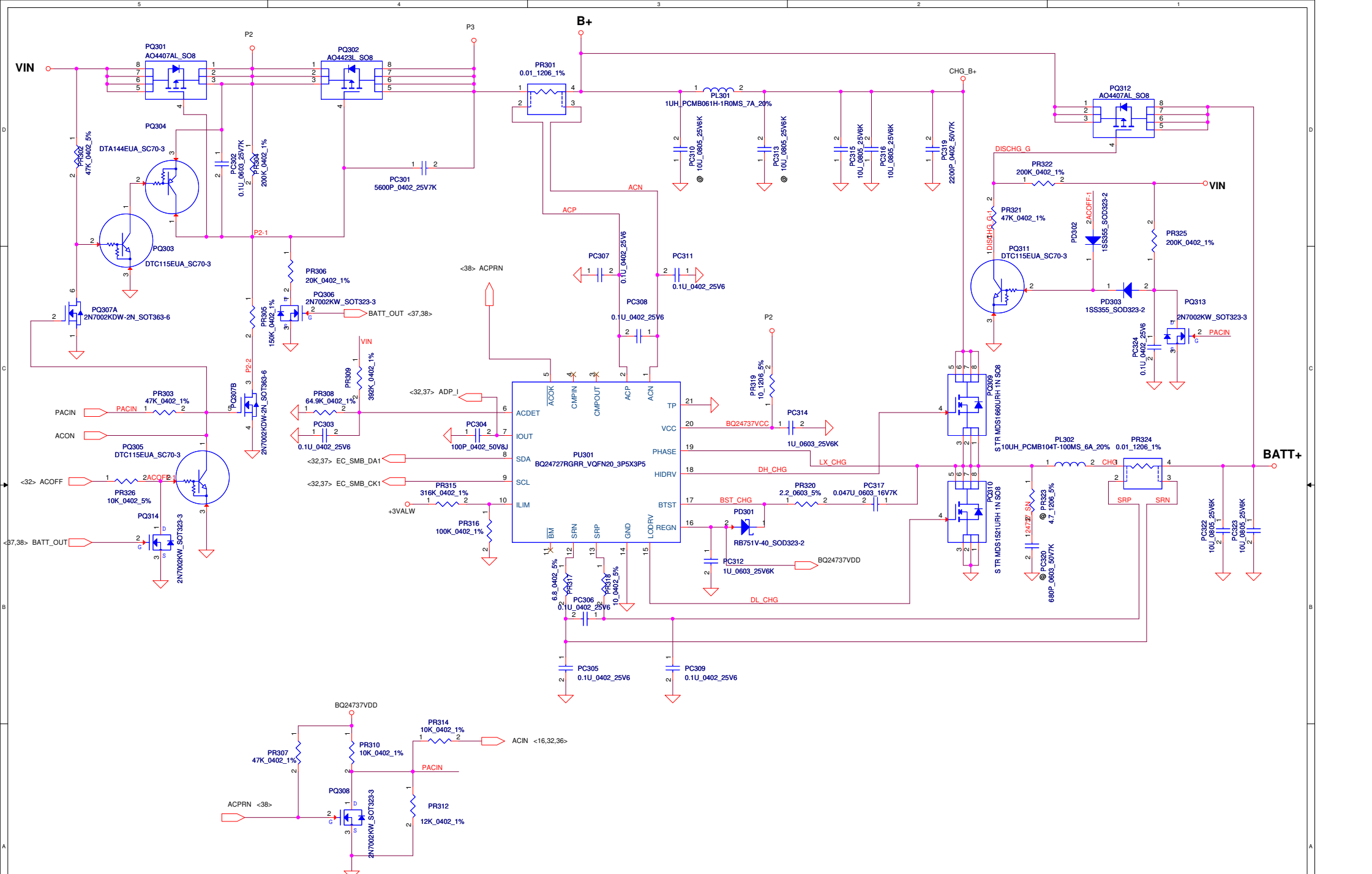
90W(DIS) : 6.65K 100W active 90W recovery  
65W(UMA) : 1.65K 70W active 65W recovery  
20120314  
Change to +EC\_VCCA from +3VLP



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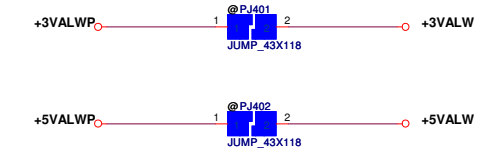
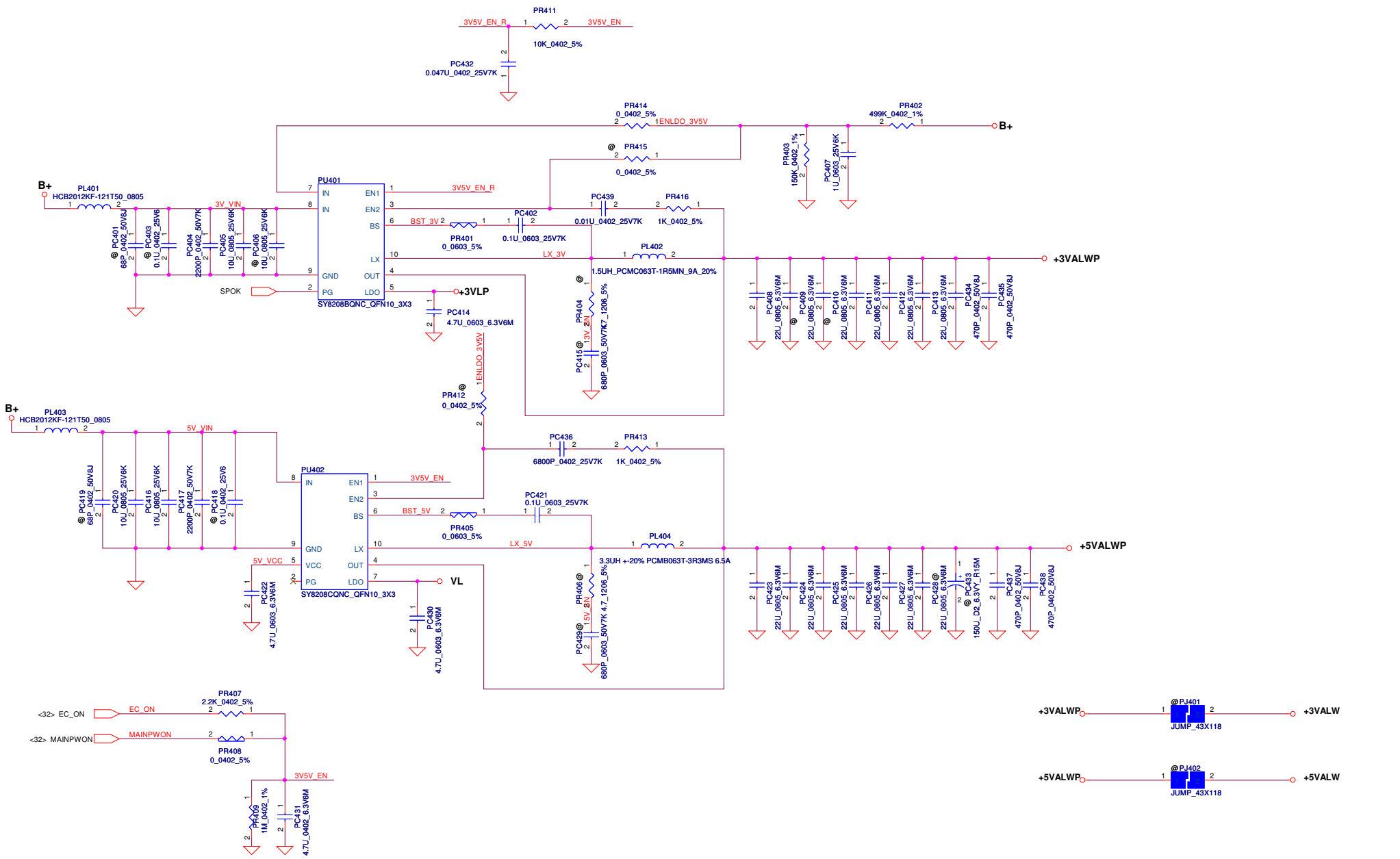
Compal Electronics, Inc.	
PWR-BATTERY CONN/OTP	
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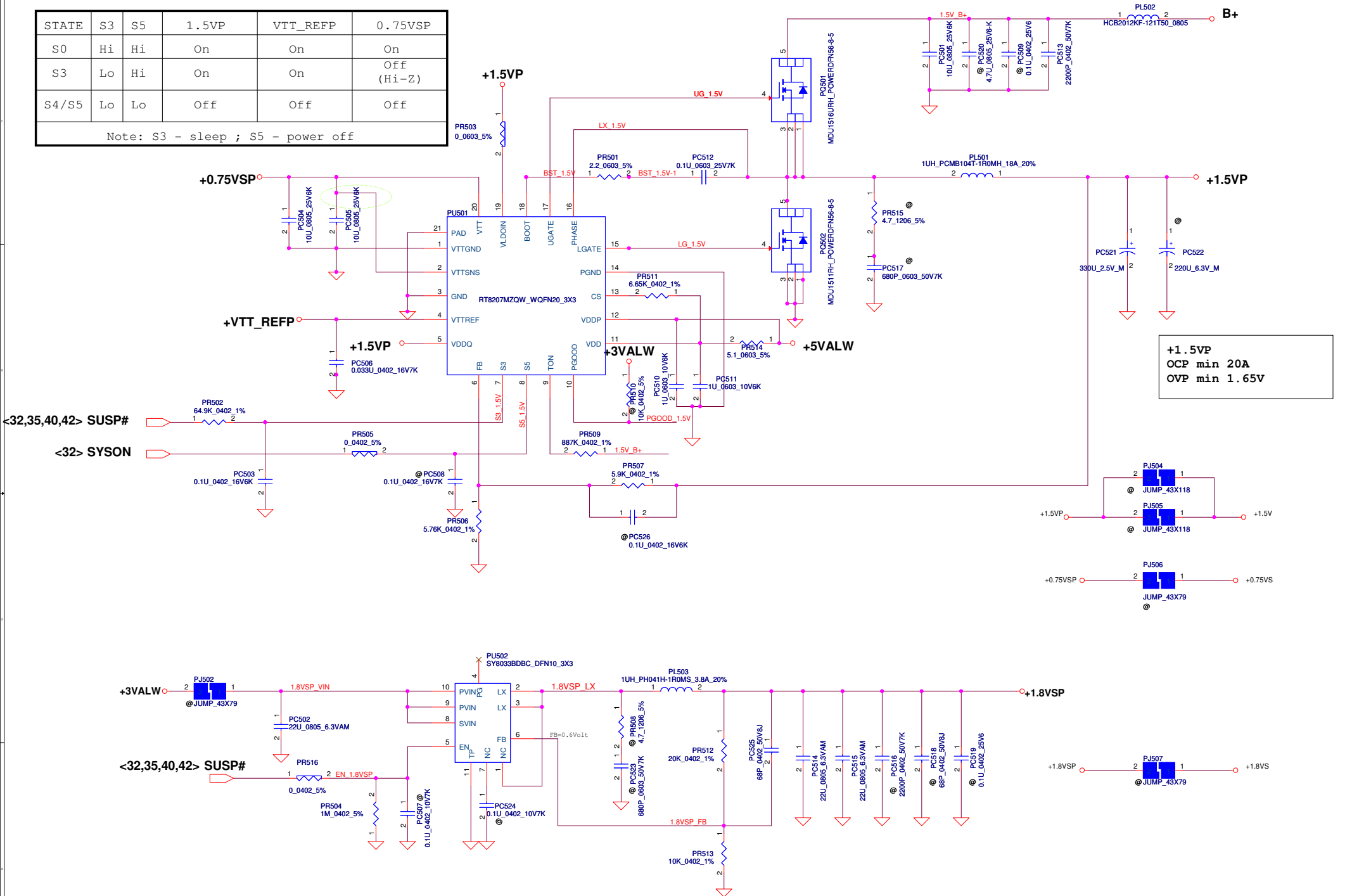


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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



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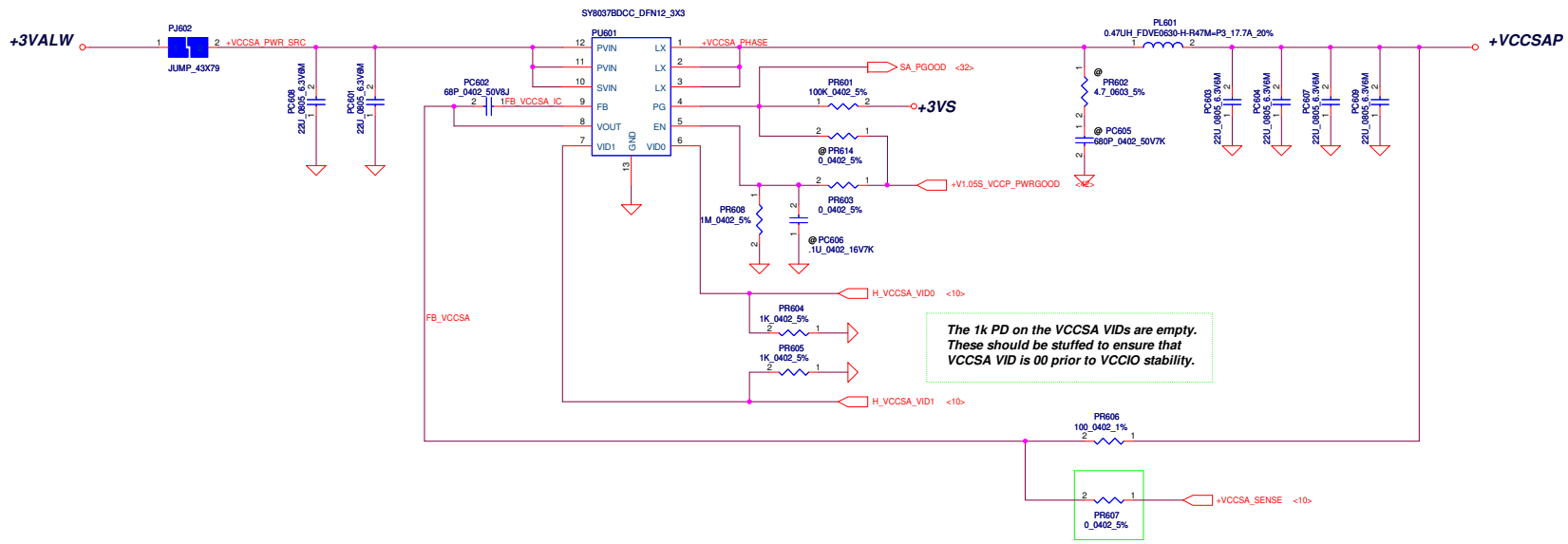
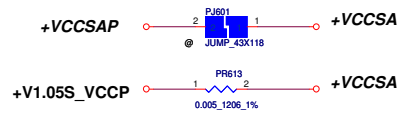
Date:	Wednesday, February 27, 2013	Sheet	40	of	60
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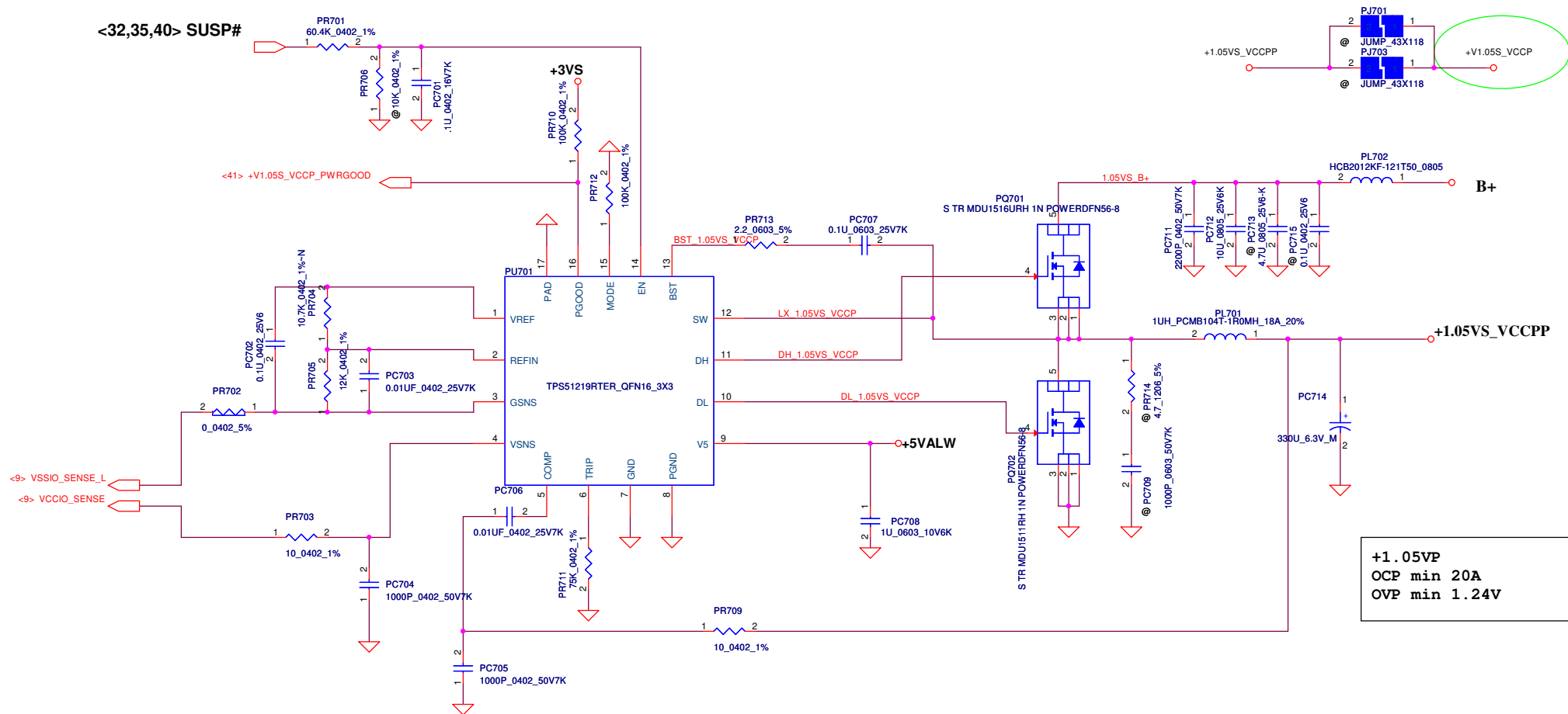
VID [0]	VID [1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



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Size	Rev 1.0			

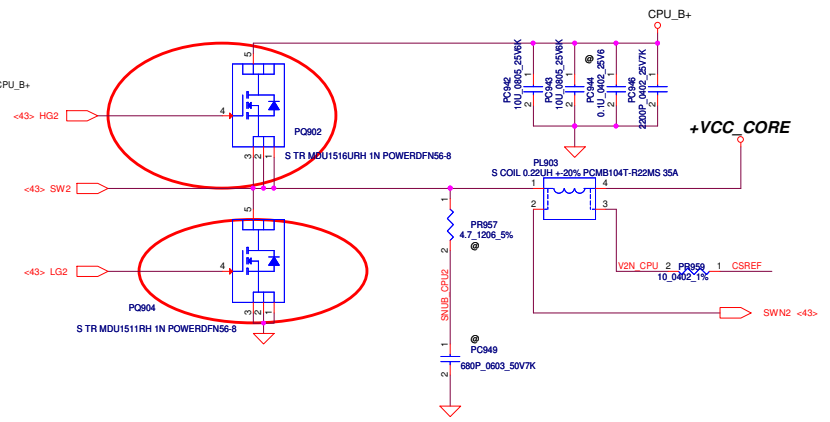
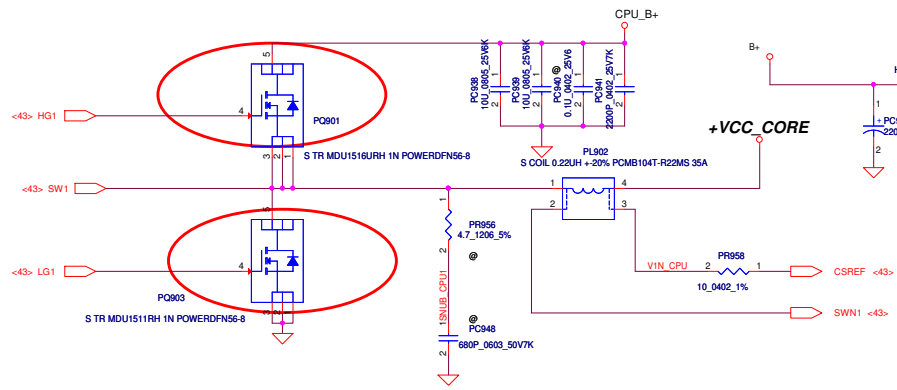
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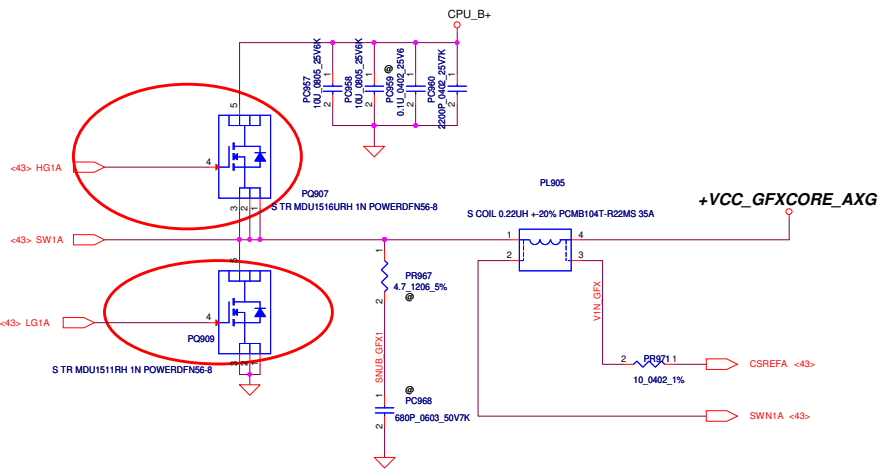
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QC 45W CPU  
 VID1=0.9V  
 IccMax=94A  
 Icc\_Dyn=66A  
 Icc\_TDC=52A  
 R\_LL=1.9m ohm  
 OCP-110A

DC 35W CPU  
 VID1=1.05V  
 IccMax=53A  
 Icc\_Dyn=43A  
 Icc\_TDC=36A  
 R\_LL=1.9m ohm  
 OCP-65A

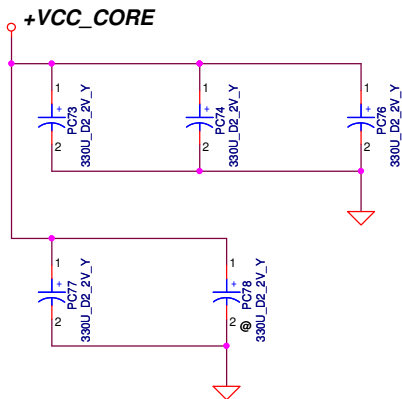
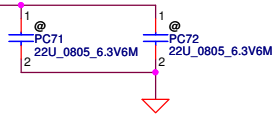
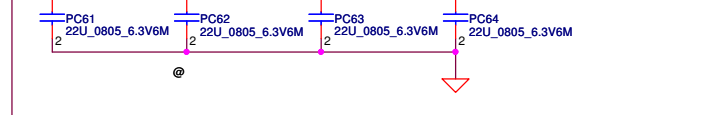
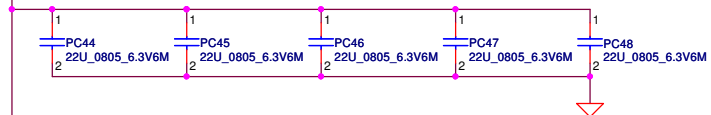
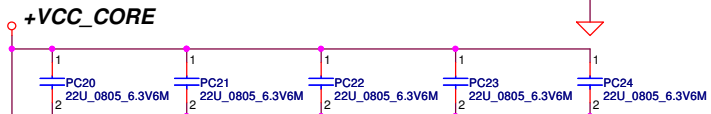
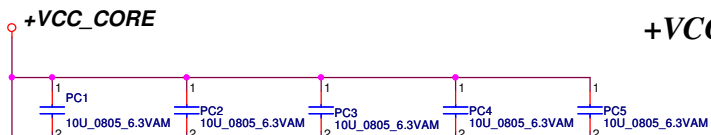


QC 45W GT2  
 VID1=1.23V  
 IccMax=46A  
 Icc\_Dyn=37A  
 Icc\_TDC=38A  
 R\_LL=3.9m ohm  
 OCP-55A

DC 35W GT2  
 VID1=1.23V  
 IccMax=33A  
 Icc\_Dyn=20.2A  
 Icc\_TDC=21.5A  
 R\_LL=3.9m ohm  
 OCP-40A

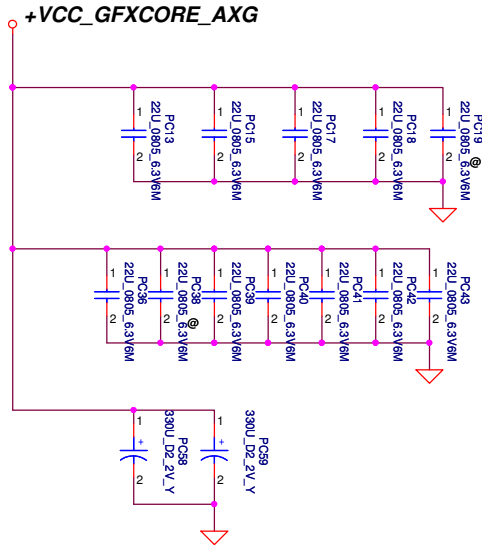
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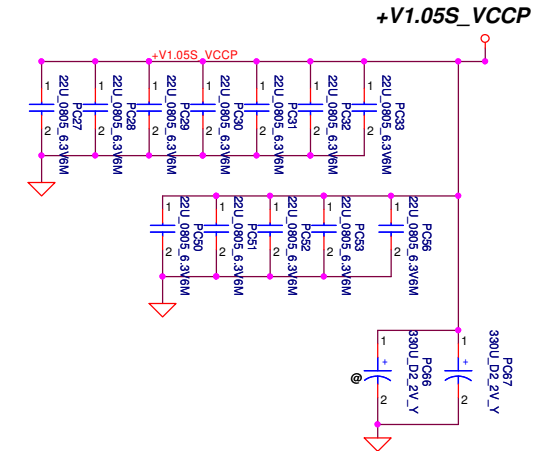
**+VCC\_CORE**

**+VCC\_GFXCORE\_AXG**



Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



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Size	Document Number	Date		Sheet	Rev
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# VIWGP/R HW PIR List

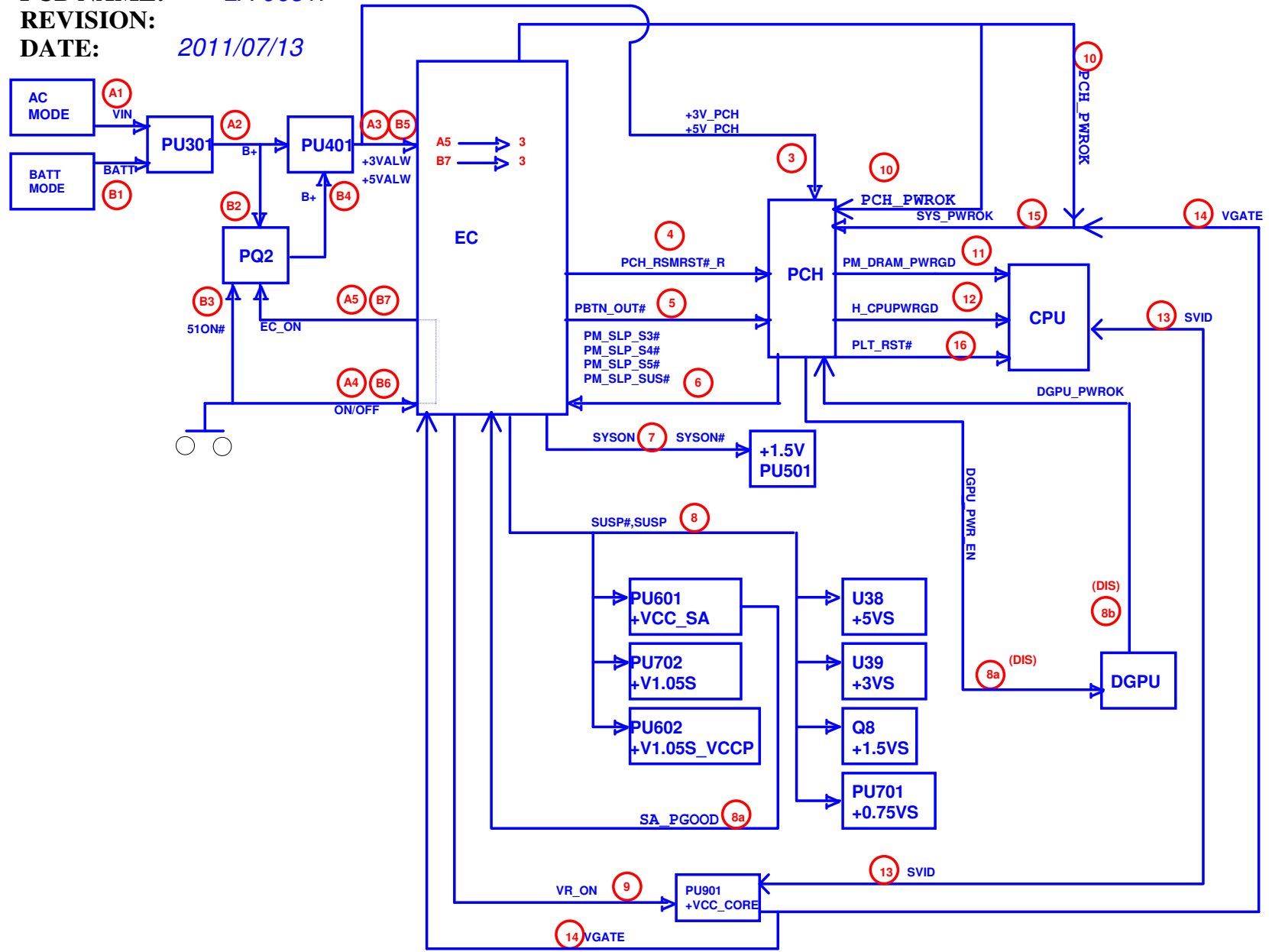
Item	Page	MODIFICATION LIST	PURPOSE	EVT TO DVT
1	P. 46	Add PR102, PC108, PC109	For ADP_ID pin detect	
2	P. 47	Add PR225, PR227, PR228, PQ206, PQ207, PQ208	For protect adapter function	
3	P. 49	Add PR410, PC433	For 3VALWP/5VALWP sequence	
4	P. 49	Add PC434, PC435, PC436, PC437	For EMI solution	
5	P. 49	Add PC432 and change PL404 from 1.5uH to 3.3uH	For improve output voltage ripple	
6	P. 50	Change PR502 from 49.9k to 64.9k	For +0.75VSP sequence	
7	P. 51	Add PC637	For +0.95VGSP sequence	
8	P. 54	Change PC907, PR912, PR927, PC928	For CPU Transient Compensation	
9				
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Size	Document Number	C38-G series Chief River Schematic		Rev 1.0
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# COMPAL CONFIDENTIAL

**MODEL NAME:** *Power Sequence Block Diagram*  
**PCB NAME:** *LA-9631P*  
**REVISION:**  
**DATE:** *2011/07/13*



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# VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 36	Change C726, C727 to 2.2nF	For Sequence
2	P. 26	Add R405	For Intel Combo Card
3	P. 25	Delete RP19. Add RP26, RP27	Because ME modify MIC location
4	P. 14	Add R406, R407, R408, R409	Reserve for improvement factory processes
5	P. 32	Add EC_SPI_S0, EC_SPI_S1, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
6	P. 32	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
7	P. 32	Reserve R410	Reserve Pull-high for GPIO
8	P. 5-22	Change footprint of JCPU1, U4	For Lenovo rule
9	P. 21	Add Q21, R40, C237, R225, C243	Reserve for power consumption
10	P. 24	Add R411, R412, C411, C412	Reserve for EMI
11	P. 32	Add ADP_65 to EC Pin.21	For adapter protection
12	P. 32	Add ADP_90 to EC Pin.68	For adapter protection
13	P. 32	Add ADP_135 to EC Pin.85	For adapter protection
14	P. 32	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
15	P. 32	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
16	P. 32	Add ADP_ID to EC Pin.66	For adapter
17	P. 32	Change PCH_ENBKL from EC Pin.73 to EC Pin.76	For common design
18	P. 32	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
19	P. 32	Add VGATE to EC Pin.74	Reserve for sequence
20	P. 32	Add SYS_PWROK to EC Pin.86	Reserve for sequence
21	P. 32	Change EC_TS_ON# from EC Pin.85 to EC Pin.97	For common design
22	P. 32	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
23	P. 32	Change SUSCLK from EC Pin.123 to EC Pin.122	For common design

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# VIWGP/R HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
1	P. 30	Delete R416, Add J9	No need Zero ODD Function
2	P. 26	Reserve R508	For leakage current issue of Atheros WLAN
3	P. 23	Add R509	protect BKOFF# damage
4	P. 32	Reserve R416	Reserve +3VLP power rail to EC
5	P. 32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC.
6	P. 32	Change EC_SMB_CK1 & EC_SMB_DAI power rail to +3V_EC	Using power rail which the same with EC.
7	P. 14	Change U5 from 4MB to 8MB ROM	Follow common design
8	P. 14	Delete R266, R221, U6	It is for 2MB ROM, we don't need it
1	P. 31	Reserve resistance to +3VLP and +3VALW.	For Speaker Noise in S5
2	P. 32	Reserve resistance in EC for share ROM.	Follow common design
3	P. 41	Reserve +V1.05S_VCCP_PWRGOOD of +V.05S_VCCP to connect to SA_PGOOD	For Celeron CPU

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				Document Number	LA-9632P
Date: Wednesday, February 27, 2013				Sheet	49 of 60