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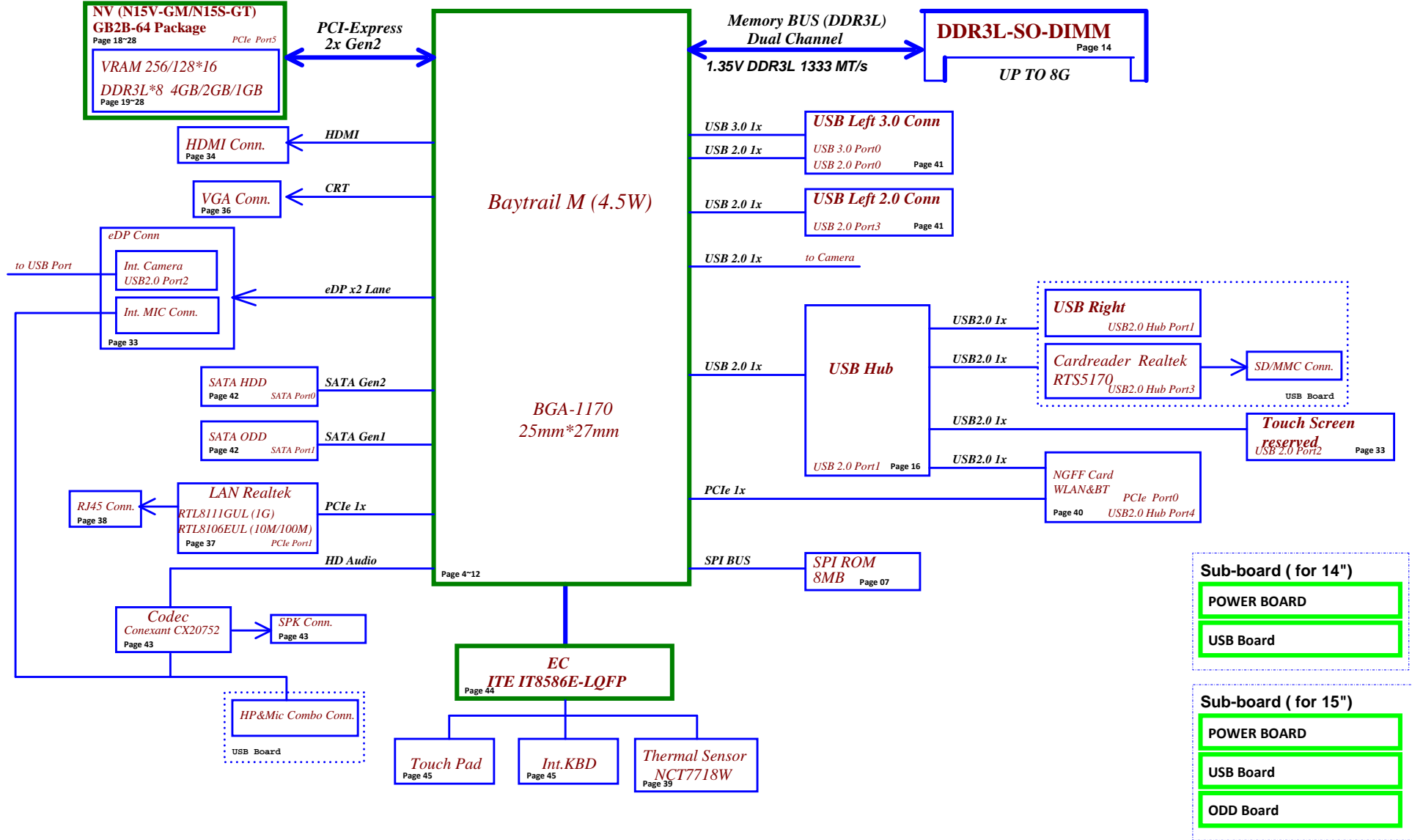
ACLU9 M/B Schematics Document


Intel BayTrail M-Processor with DDRIIL + NV (N15V-GM/N15S-GT) GPU

2013-12-22

REV: 0.2

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page	
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Voltage Rails (O --> Means ON, X --> Means OFF)

Power Plane \ State	B+	+3VALW +3VL	+3VALW_SOC +1.0VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
EHCI1	XHCI 1	0	USB Port (Left Side)
		1	USB Port (Right Side)
		2	USB Port (Left Side)
		3	USB HUB
USB HUB		1	Camera
		2	Cardreader
		3	BT(WLAN)
		4	TOUCH PANEL

BOM Structure Table

BOM Structure	BTO Item
AOAC@	AOAC support part
OPT@	GPU Part
UMA@	UMA SKU ID part
14@	For 14" part
15@	For 15" part
100M@	100M LAN part
N15SGT@	N15SGT Part
N15VGM@	N15GSM Part
GIGA@	GIGA LAN Part
GC6@	GPU GC6 Part
TS@	Touch Screen part
RANKA@	GPU VRAM RANKA PART
RANKB@	GPU VRAM RANKB PART
ME@	Connector
CDE@	COST DOWN
@	Not stuff
H4T@	Hynix VRAM Part
M4T@	Micron VRAM Part
S4T@@	Samsung VRAM Part

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

PCIe PORT LIST

Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
Charger	need to update

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_100xb
VGA	0x9E
PCH	0x96

PCH SM Bus address

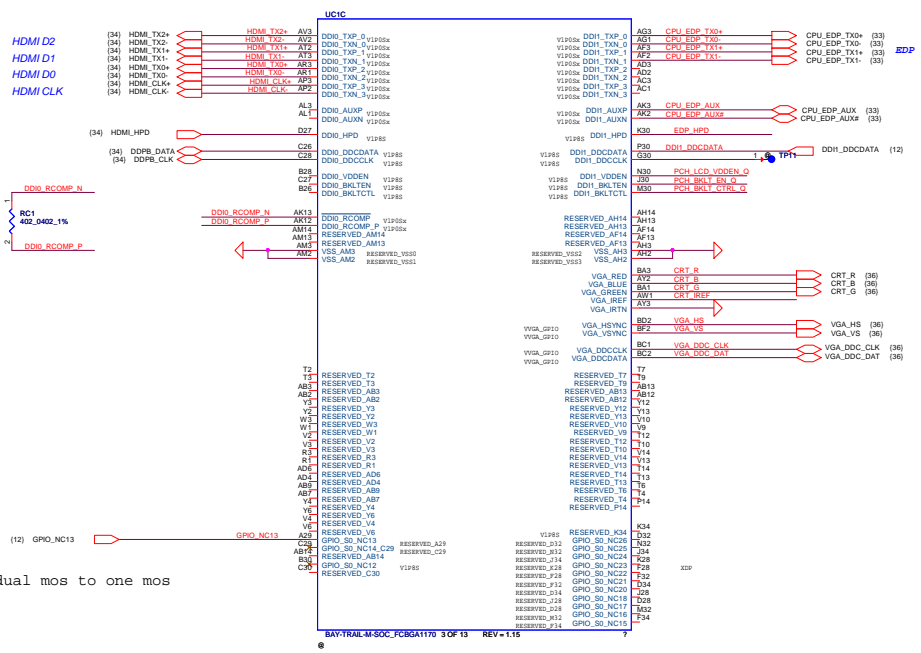
Device	Address
DDR DIMMA	1001 000Xb
Rsvd	
Wlan	
TP	need to update

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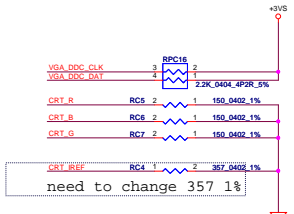
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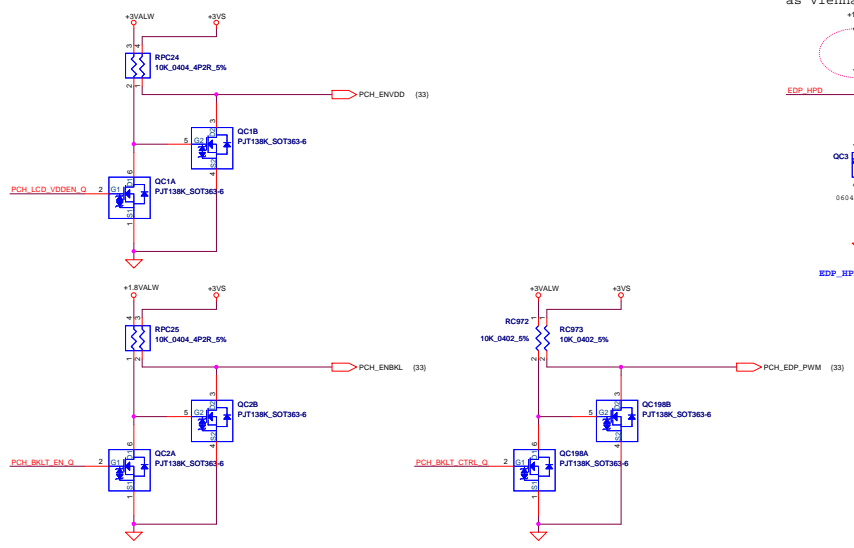
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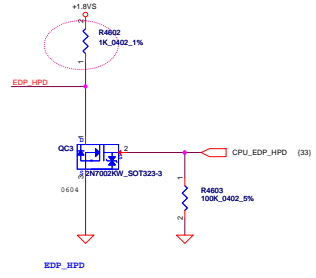
Port	DDI PROCESSOR Pin Names	HDMI* Mapping
Port 0	DDI1_TXP_0	HDMI_TX2+
	DDI0_TXN_0	HDMI_TX2-
	DDI0_TXP_1	HDMI_TX1+
	DDI0_TXN_1	HDMI_TX1-
	DDI0_TXP_2	HDMI_TX0+
	DDI0_TXN_2	HDMI_TX0-
	DDI0_TXP_3	HDMI_CLK+
	DDI0_TXN_3	HDMI_CLK-
	DDI0_HPD	HDMI_HPD
	DDI0_DDCDATA	DDP_DAT
DDI0_DDOCLK	DDP_CLK	
Port 1	DDI1_TXP_0	CPU_EDP_TX0+
	DDI1_TXN_0	CPU_EDP_TX0-
	DDI1_TXP_1	CPU_EDP_TX1+
	DDI1_TXN_1	CPU_EDP_TX1-
	DDI1_AUXP	CPU_EDP_AUX
	DDI1_AUXN	CPU_EDP_AUX#
	DDI1_HPD	EDP_HPD



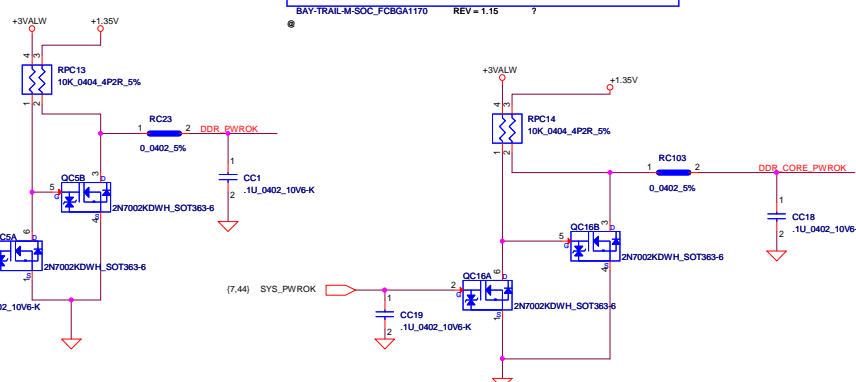
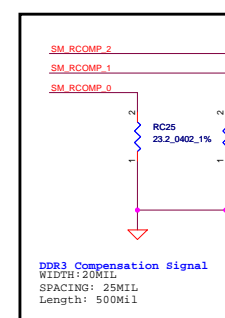
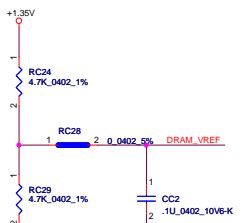
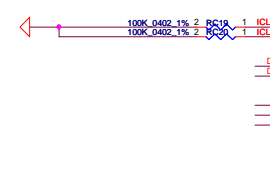
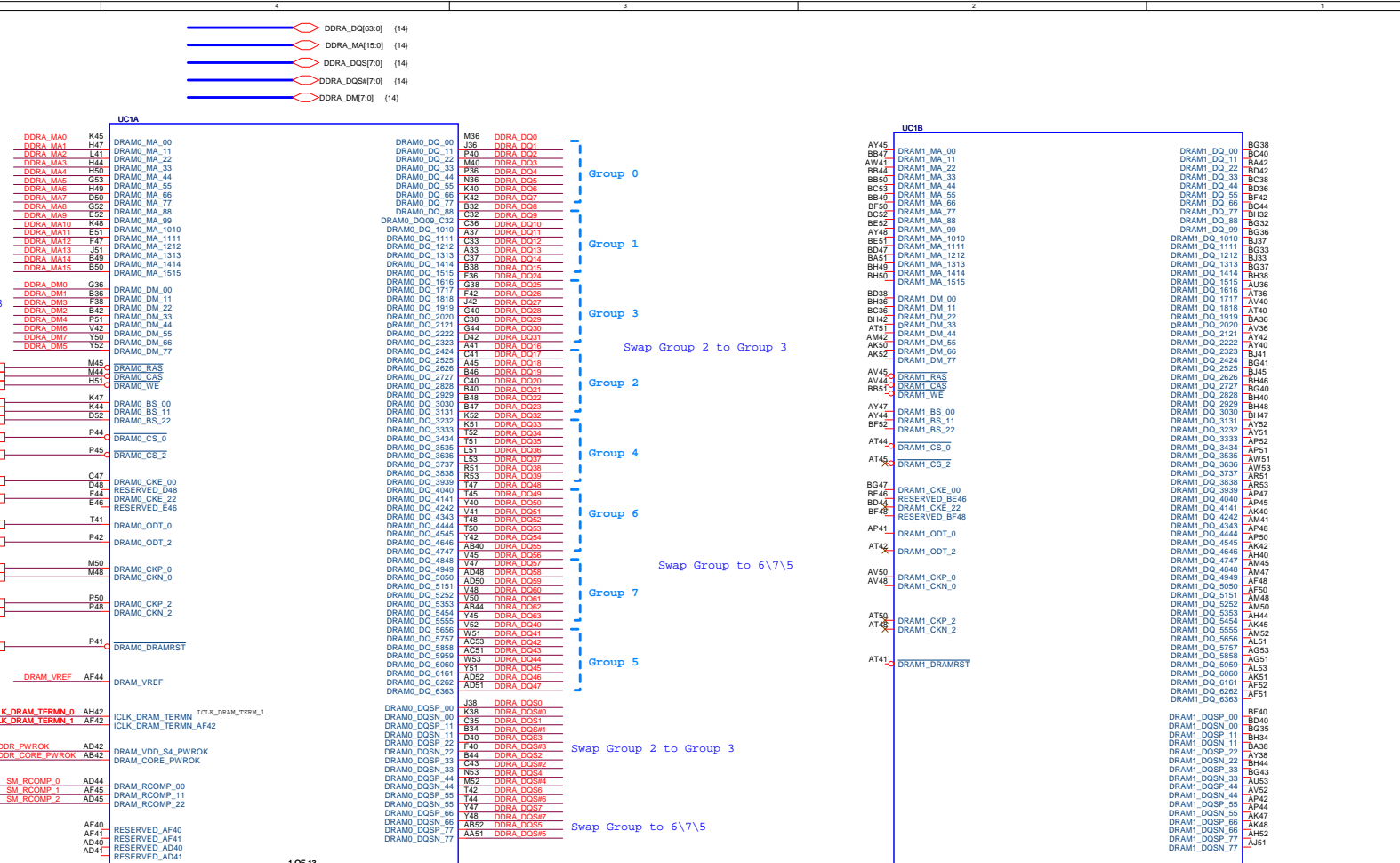
change dual mos to one mos



R4602 change from 10K to 1K, as Vienna



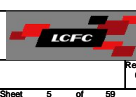
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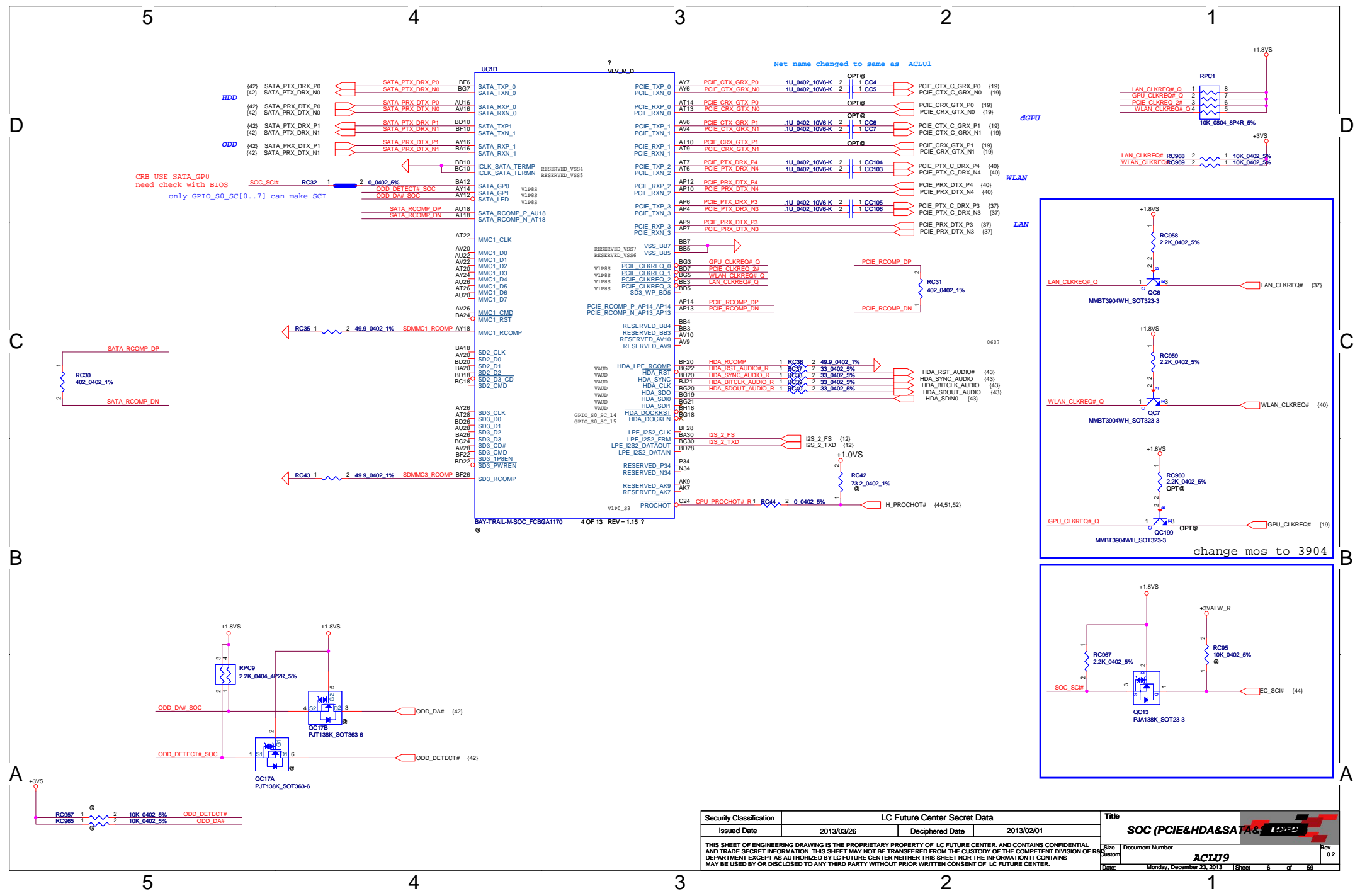
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BAY-TRAIL-M-SOC_FCBGA1170 REV = 1.15 7

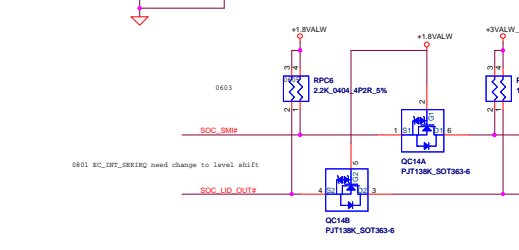
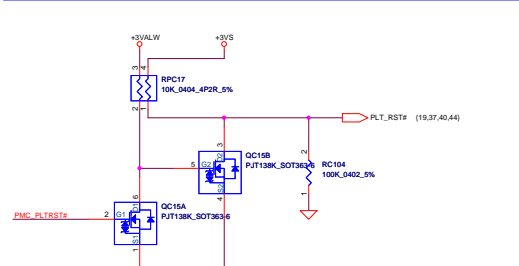
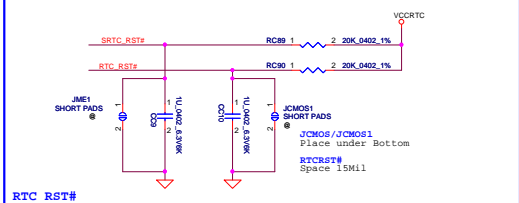
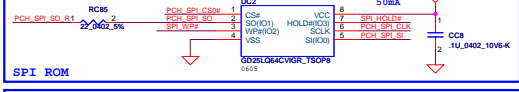
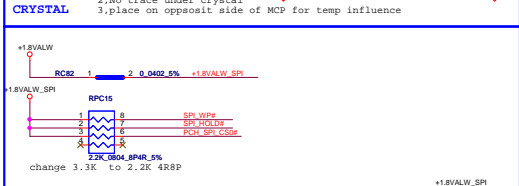
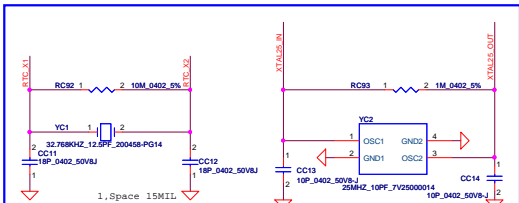
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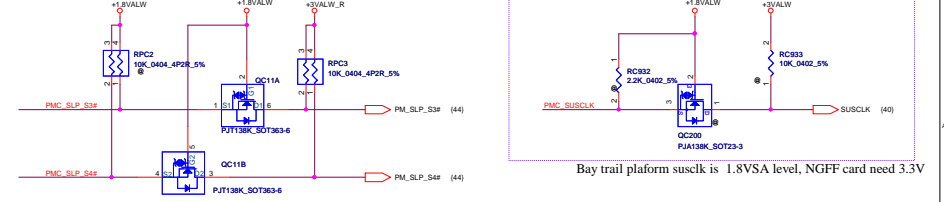
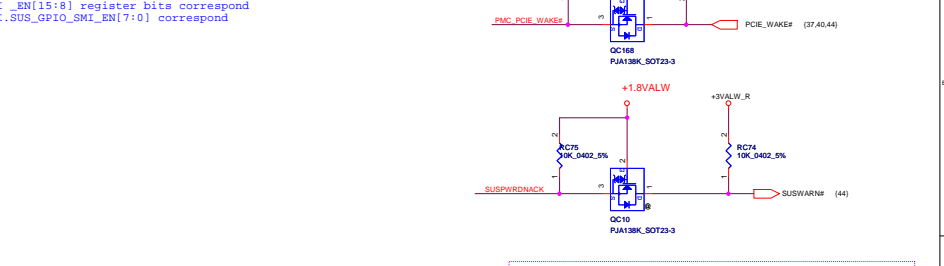
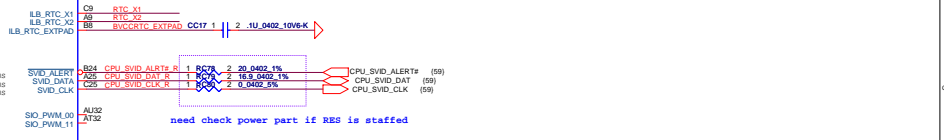
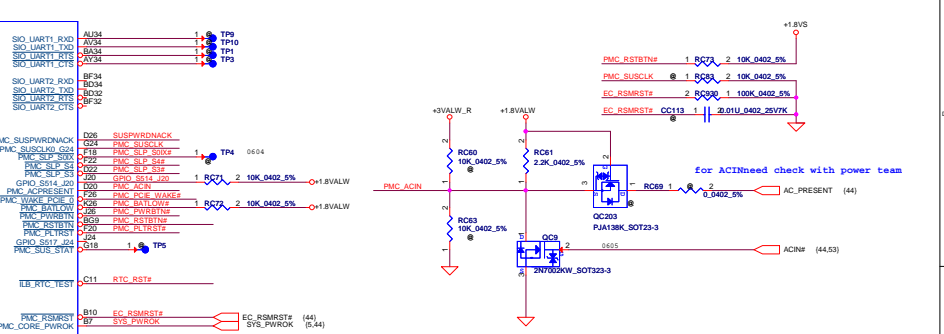
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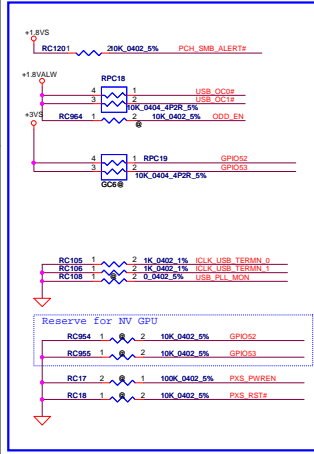
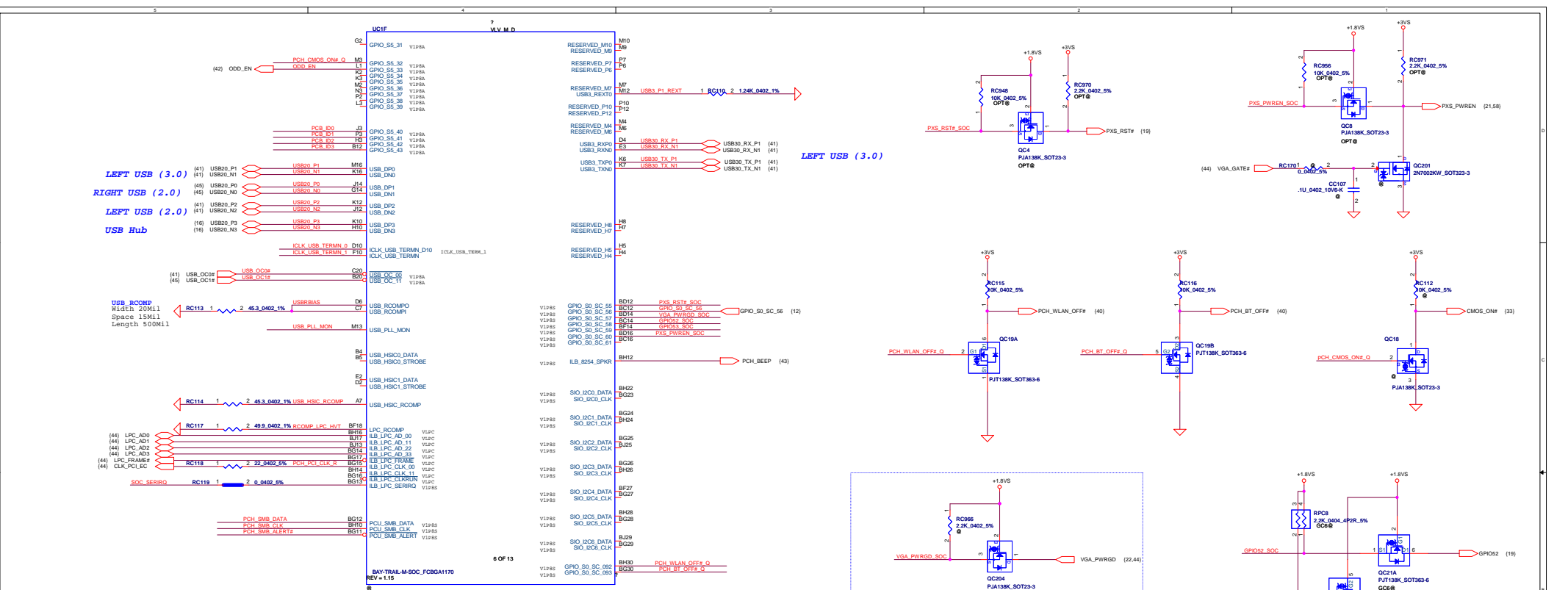
0801_EC_INT_SERRIQ need change to level abilit



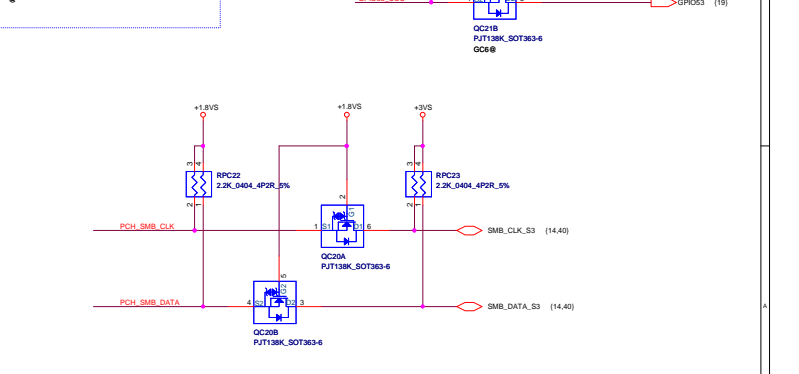
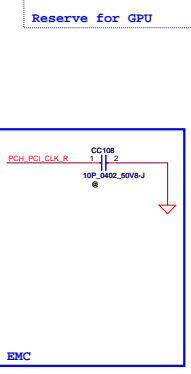
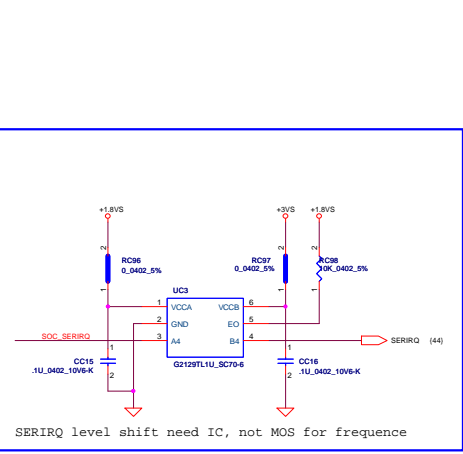
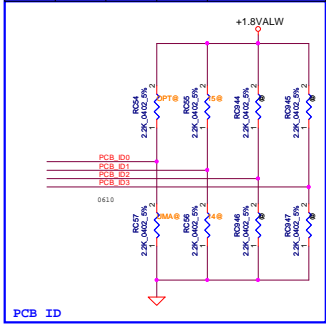
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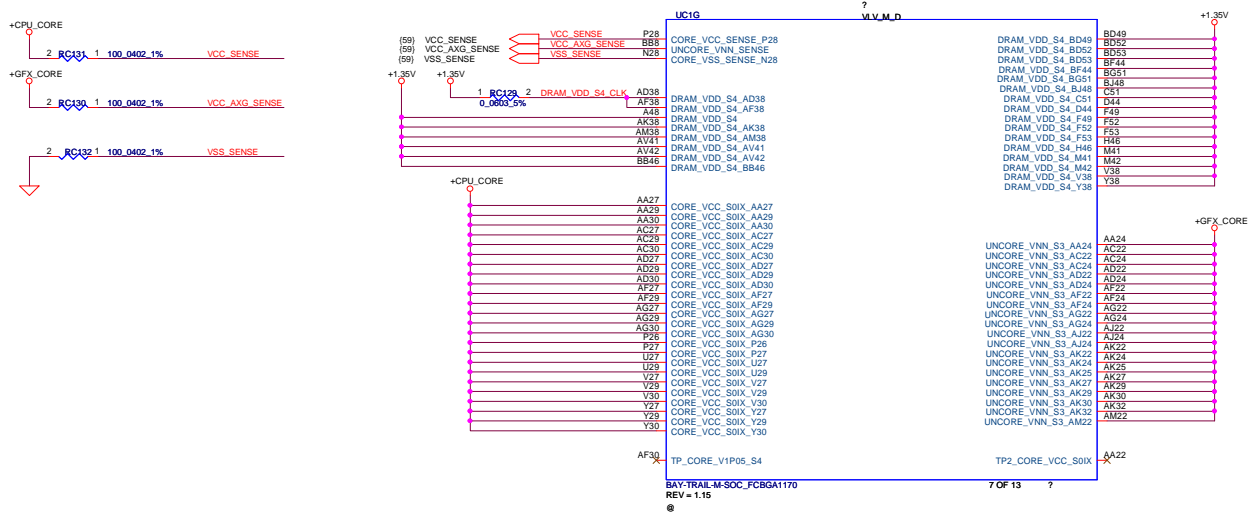
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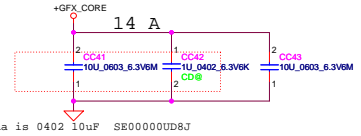
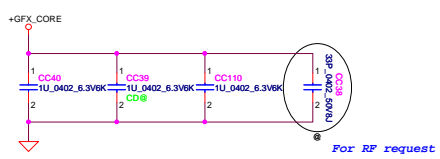
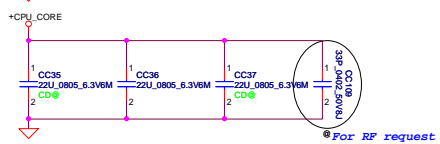
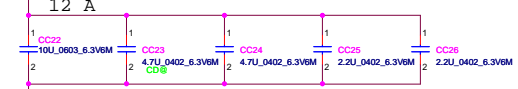
PCB_ID0	PCB_ID1	PCB_ID2	PCB_ID3	Description
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1		Reserve	Reserve	GPU_SSD
	0	Reserve	Reserve	14' panel
	1	Reserve	Reserve	15' panel



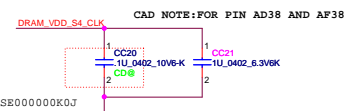
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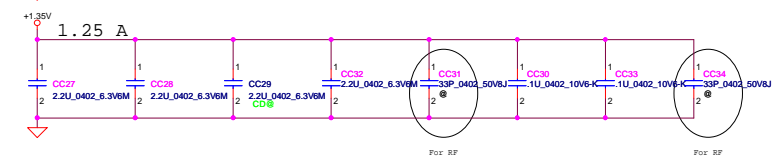
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 0402 4.7uF SE00000SO0J
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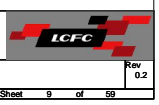
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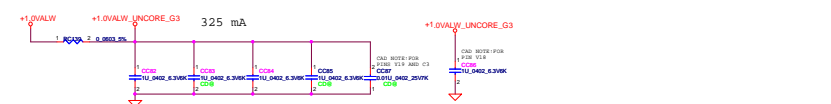
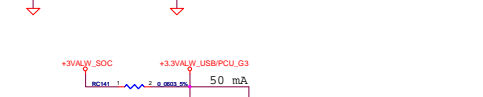
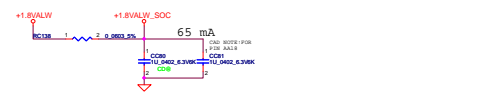
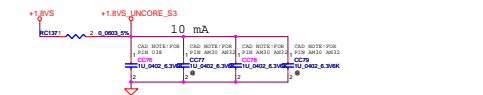
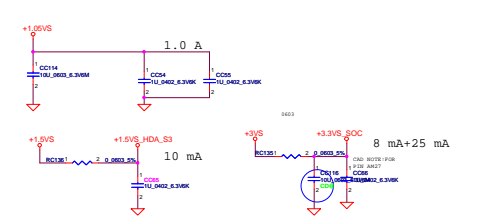
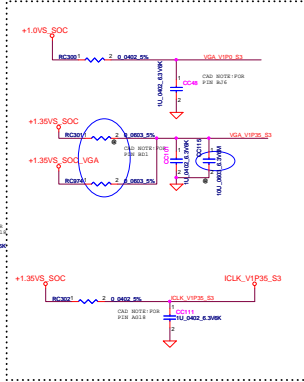
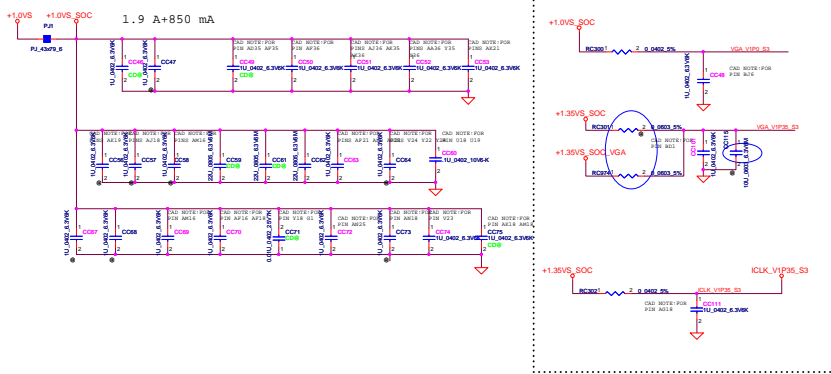
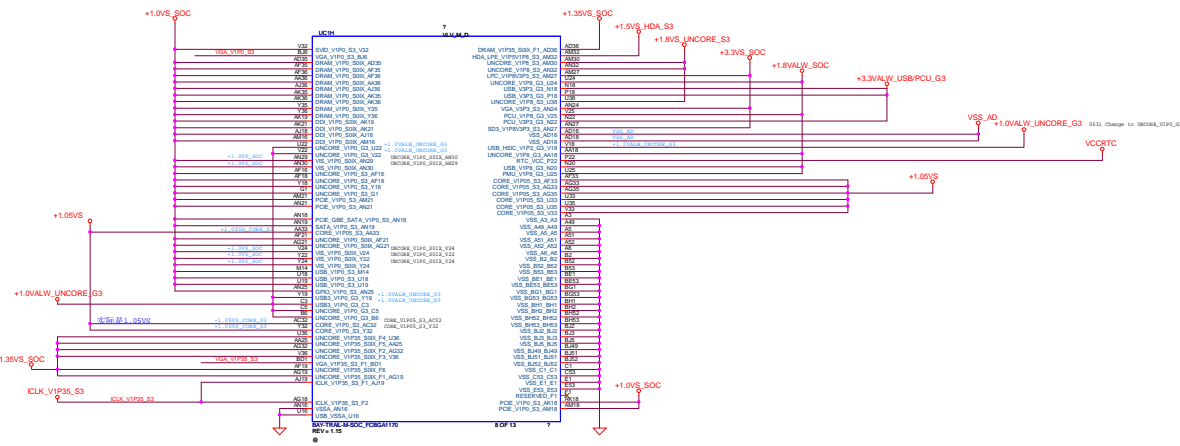


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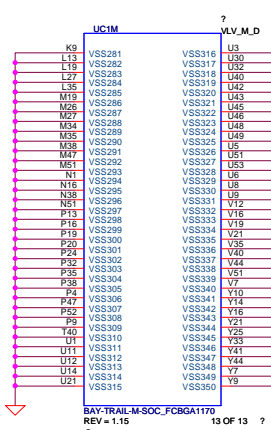
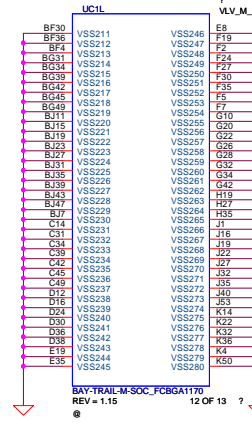
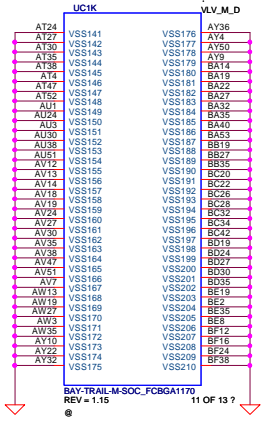
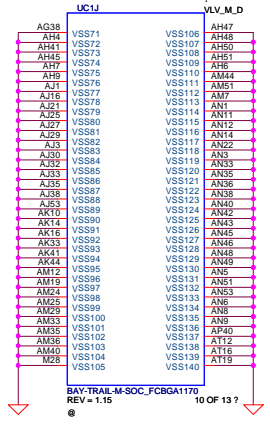
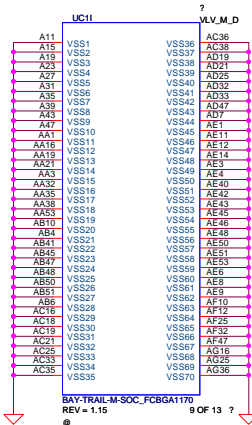


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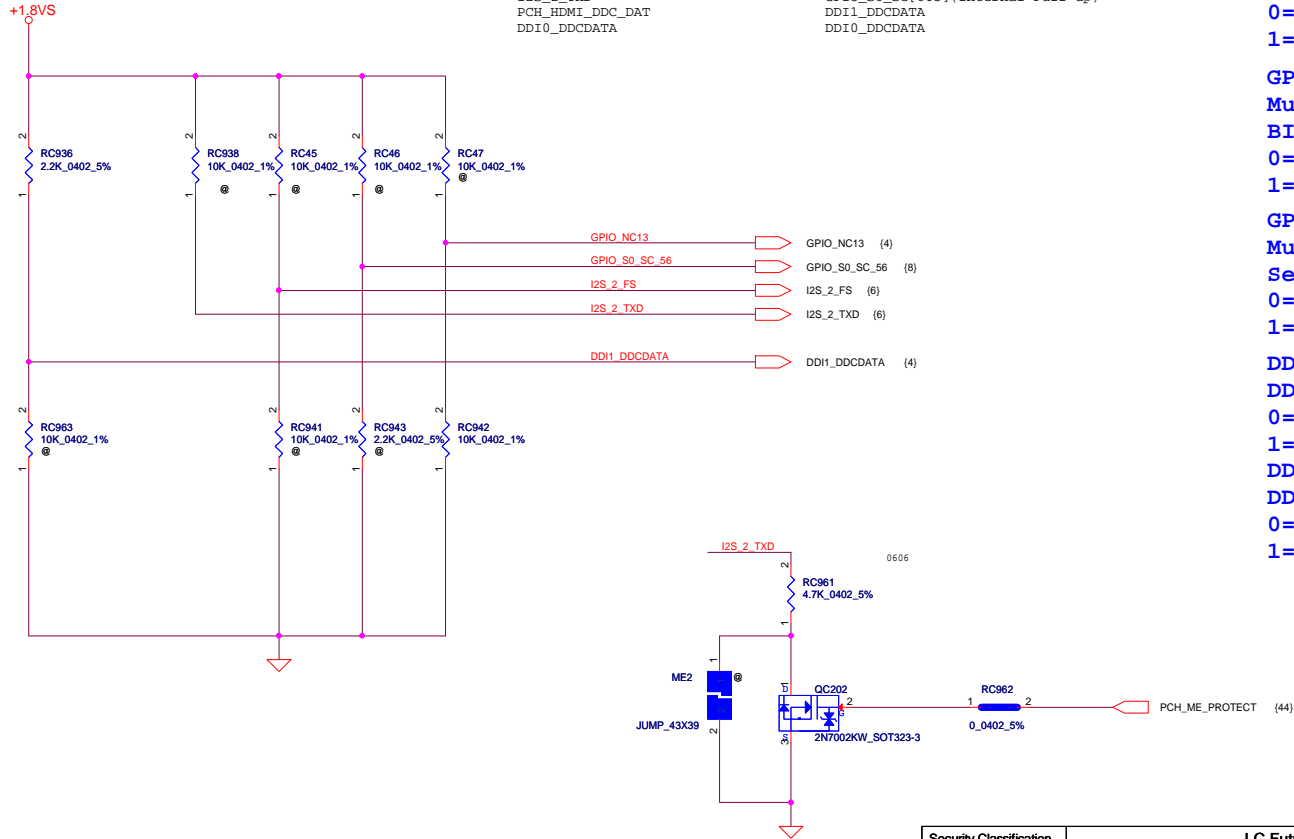




Security Classification	LC Future Center Secret Data		Rev	1
Issued Date	2013/03/28	Dissemination Date	2013/02/01	
Title			SOC (Power2)	
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**Hardware STRAPS
(Follow up CRB& VIENNA)**



GPIO_NC13
GPIO_S0_SC_56
I2S_2_FS
I2S_2_TXD
PCH_HDMI_DDC_DAT
DDI0_DDCDATA

MDSI_DDCDATA(Checklist request 10K pull down)
GPIO_S0_SC_56(Internal Pull-up)
GPIO_S0_SC[063] (Internal Pull-up)
GPIO_S0_SC[065](Internal Pull-up)
DDI1_DDCDATA
DDI0_DDCDATA

GPIO_S0_SC_56:
A16 Top Swap
0=Top address bit is unchanged
1=Top address bit is inverted

GPIO_S0_SC[063]
Multiplexed with Hardware Straps Pin LPE_I2S2_FRM
BIOS Boot selection
0=LPC
1=SPI

GPIO_S0_SC[065]
Multiplexed with LPE_I2S2_DATAOUT
Security Flash Descriptors
0=Override
1=Normal Operation

DDI0_DDCDATA:
DDI0 strap
0=DDI0 not detected
1=DDI0 detected

DDI1_DDCDATA:
DDI1 strap
0=DDI1 not detected
1=DDI1 detected

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	SOC (STRAPS & OTHERS)	
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				Sheet	12 of 59
				Rev	0.2

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Issued Date	2013/08/08	Deciphered Date	2013/08/05	MCP (OTHER)		
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				Date:	Monday, December 23, 2013	Sheet 13 of 59

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DDR Mapping table

DDR3 SO-DIMM A

DDR3 Pinout Table:

1	VREF_DQ	2	VSS_2
3	DQ0	4	DQ4
5	DQ1	6	DQ5
7	DQ2	8	DQ6
9	DQ3	10	DQ7
11	DM0	12	DQ8
13	VSS_5	14	DQ9
15	DQ2	16	DQ10
17	DQ3	18	DQ11
19	VSS_7	20	DQ12
21	DQ8	22	DQ13
23	DQ9	24	DQ14
25	DQ10	26	DQ15
27	DQ11	28	DQ16
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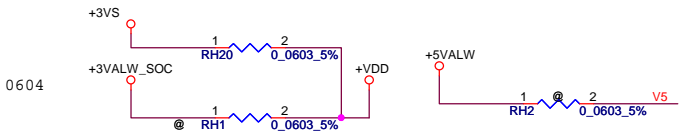
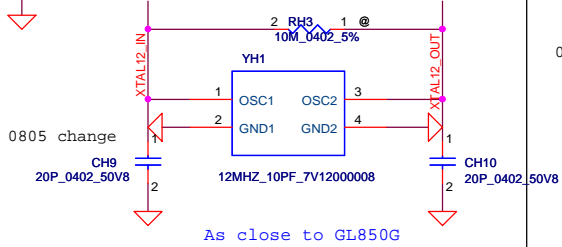
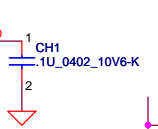
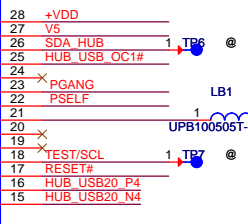
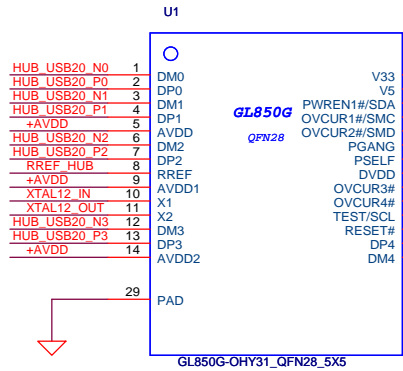
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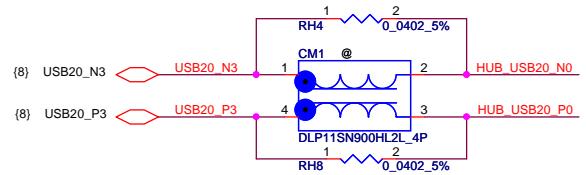
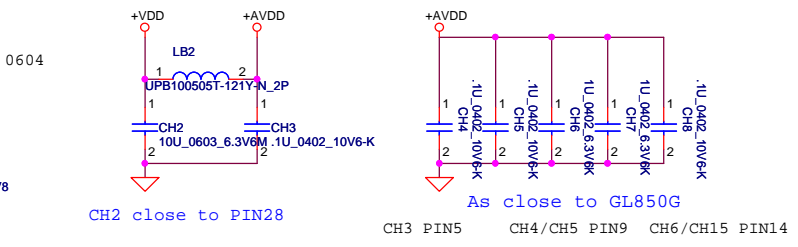
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Size	Document Number	Rev	
Custom	ACLU9	0.2	
Date:	Monday, December 23, 2013		Sheet 15 of 59

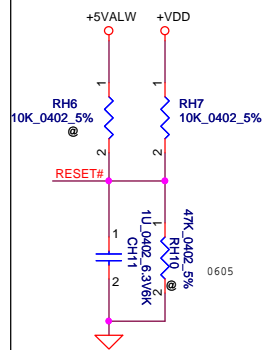
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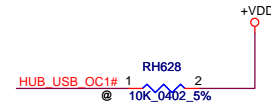
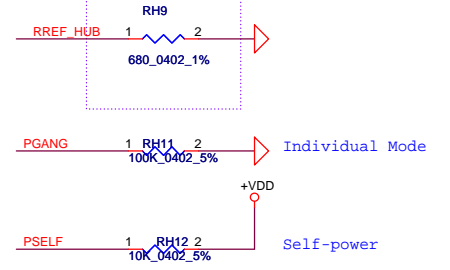
** External regulator mode: RH1上件, RH2不上件
Internal regulator mode: RH1不上件, RH2上件



- HUB_USB20_N1 (33) Camera
- HUB_USB20_P1 (33) Camera
- HUB_USB20_N2 (45) Card reader
- HUB_USB20_P2 (45) Card reader
- HUB_USB20_N3 (40) BT
- HUB_USB20_P3 (40) BT
- HUB_USB20_N4 (33) Touch panel
- HUB_USB20_P4 (33) Touch panel




Vienna change to 619 ohm for Eye Diagram test



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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

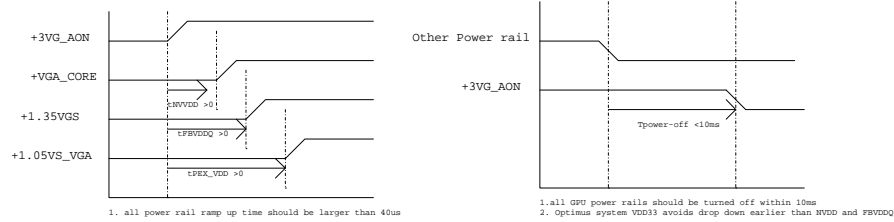
Products	GPU	Mem	NVCLK	NVVDD			FBVDD		FBVDDQ		PCI Express		I/O and PLLVDD		Other		
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

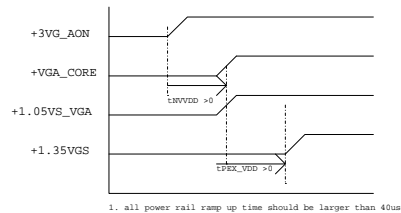
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



N15S-GT Power Sequence

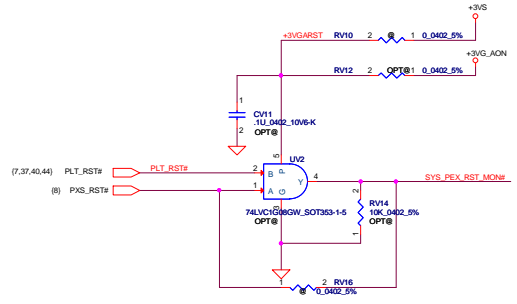
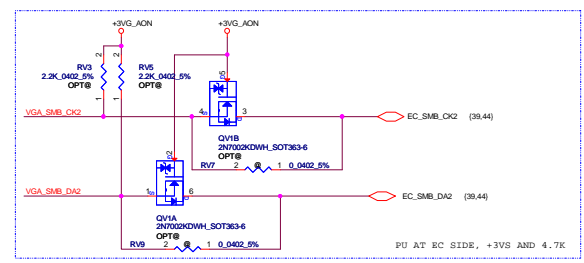


N15x Binary Straps

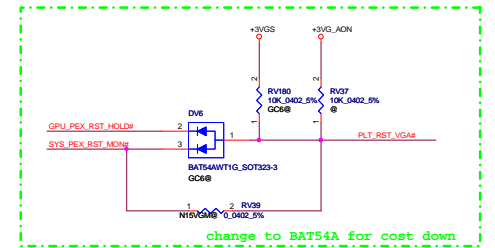
Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

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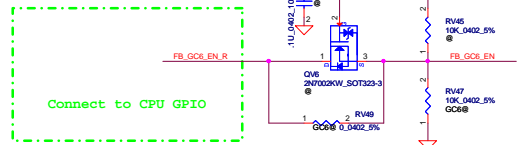
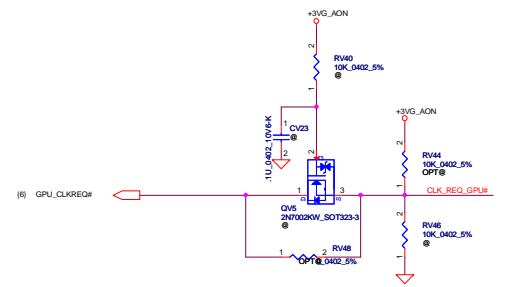
- (8) GPIO2 \rightarrow RV1 1 GC6B 2 0.0402 5% FB_GCG_EN_R
- (8) GPIO3 \rightarrow RV2 1 GC6B 2 0.0402 5% GPU_EVENTS
- (6) POE_CRX_GTX_N0..1 \rightarrow
- (6) POE_CRX_GTX_P0..1 \rightarrow
- (6) POE_CTX_G_GRX_N0..1 \rightarrow
- (6) POE_CTX_G_GRX_P0..1 \rightarrow



- POE_CRX_GTX_P0 CV10 OPT# 1 2 1U_0402_10V6K
- POE_CRX_GTX_N0 CV3 OPT# 1 2 1U_0402_10V6K
- POE_CRX_GTX_P1 CV8 OPT# 1 2 1U_0402_10V6K
- POE_CRX_GTX_N1 CV9 OPT# 1 2 1U_0402_10V6K
- POE_CRX_C_GTX_P0 AC9
- POE_CRX_C_GTX_N0 AB7
- POE_CRX_C_GTX_P1 AC10
- POE_CRX_C_GTX_N1 AC10

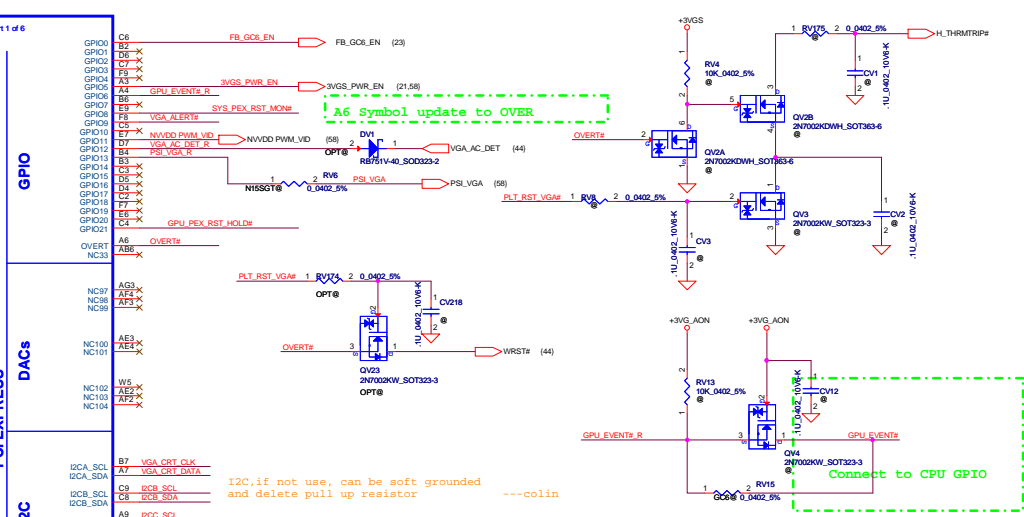


change to BAT54A for cost down



Connect to CPU GPIO

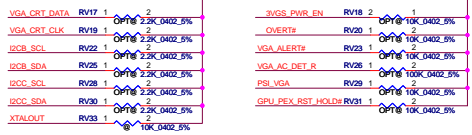
GPIO	PCIE EXPRESS	I2C	CLK
GPIO0	B7 VGA CRT CLK	I2CA_SCL	L6
GPIO1	A7 VGA CRT DATA	I2CA_SDA	M6
GPIO2		I2CB_SCL	N6
GPIO3	C9 I2CB_SCL	I2CB_SDA	N8
GPIO4	C8 I2CB_SDA	I2CC_SCL	
GPIO5	A9 I2CC_SCL	I2CC_SDA	
GPIO6	B9 I2CC_SDA	I2CS_SCL	
GPIO7	D9 VGA SMB CK2	I2CS_SDA	
GPIO8	D8 VGA SMB DA2		
GPIO9			
GPIO10			
GPIO11			
GPIO12			
GPIO13			
GPIO14			
GPIO15			
GPIO16			
GPIO17			
GPIO18			
GPIO19			
GPIO20			
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GPIO92			
GPIO93			
GPIO94			
GPIO95			
GPIO96			
GPIO97			
GPIO98			
GPIO99			
GPIO100			



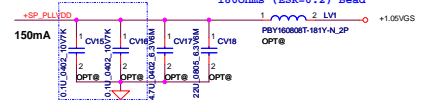
I2C, if not use, can be soft grounded and delete pull up resistor

---colin

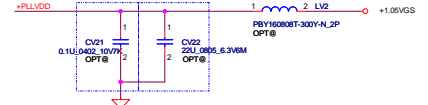
Internal Thermal Sensor



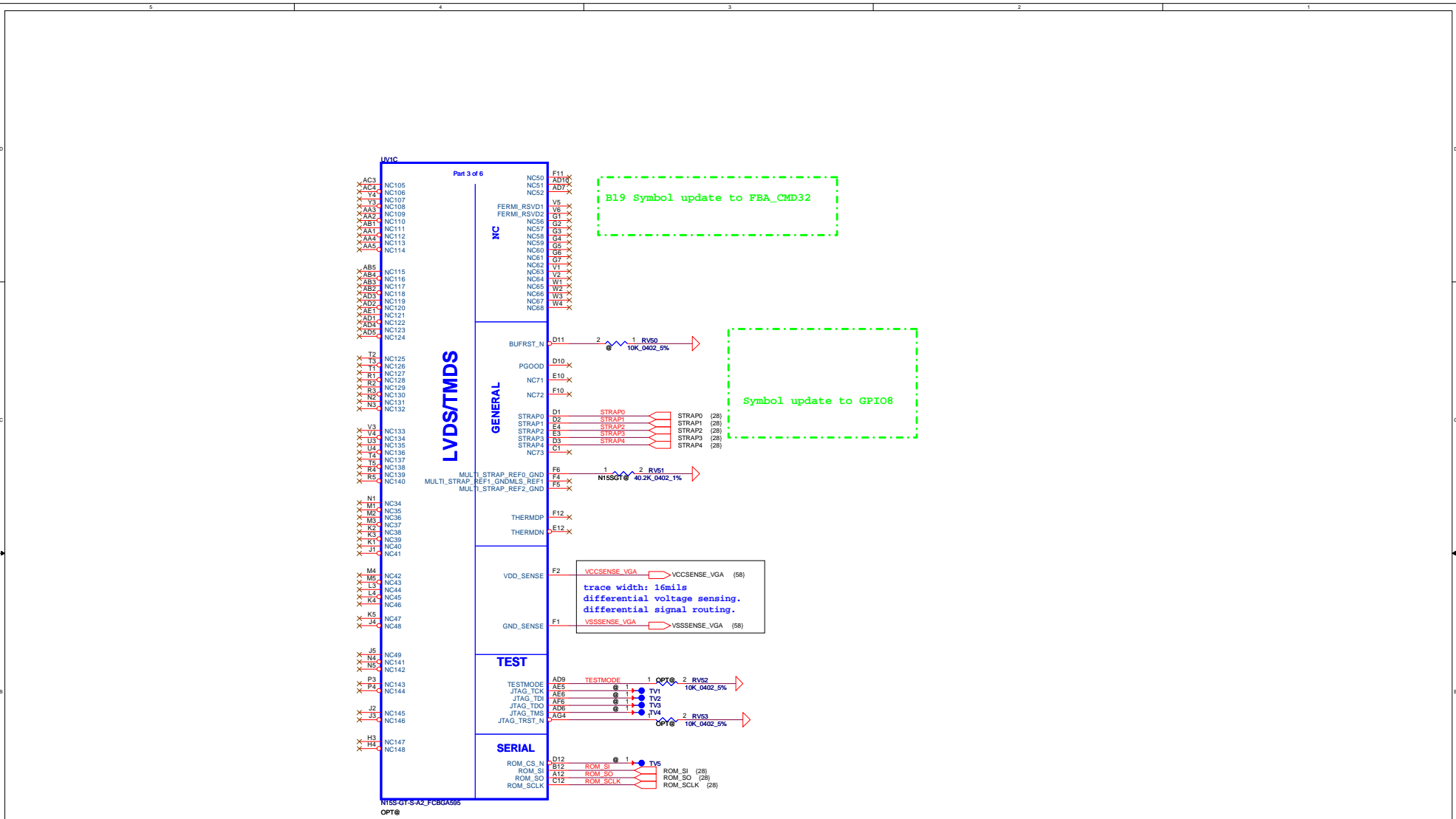
Under GPU (below 150mils)



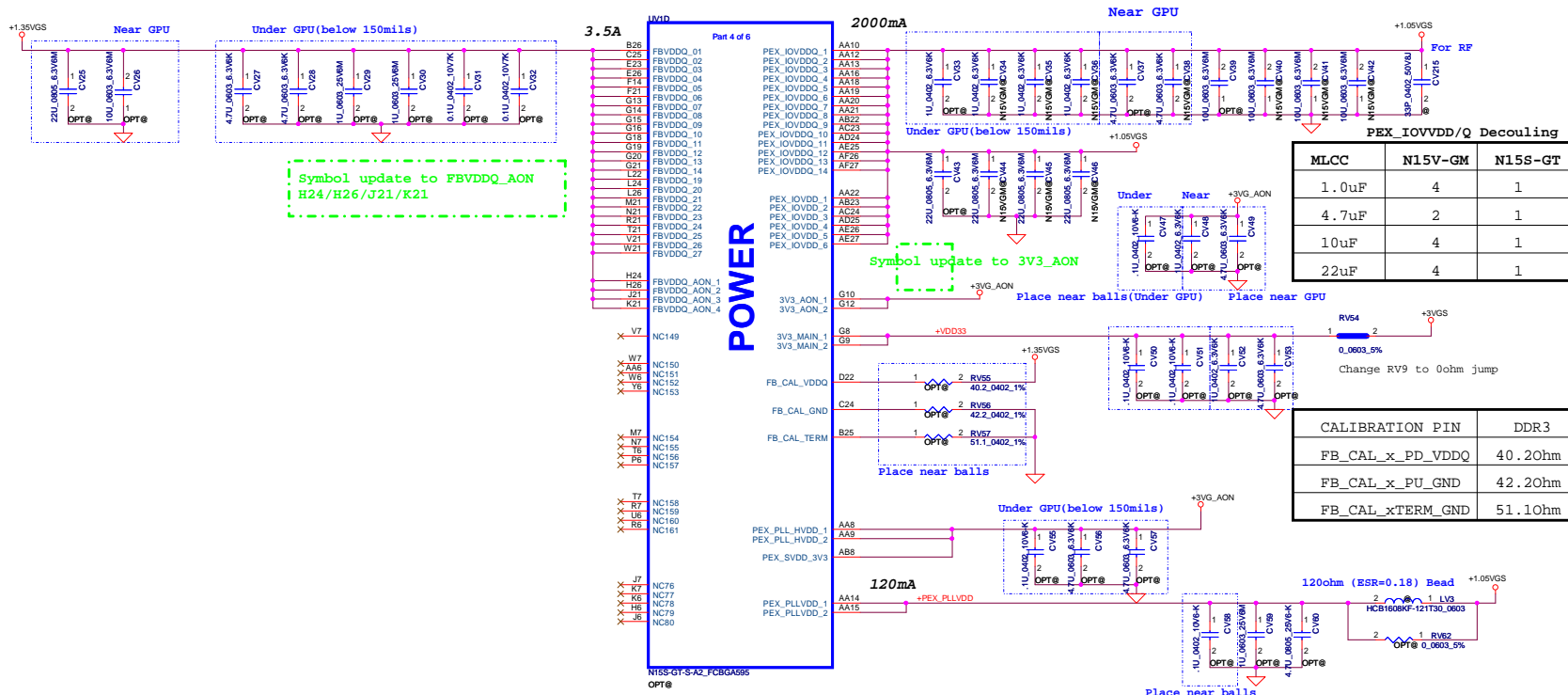
Under GPU Near GPU



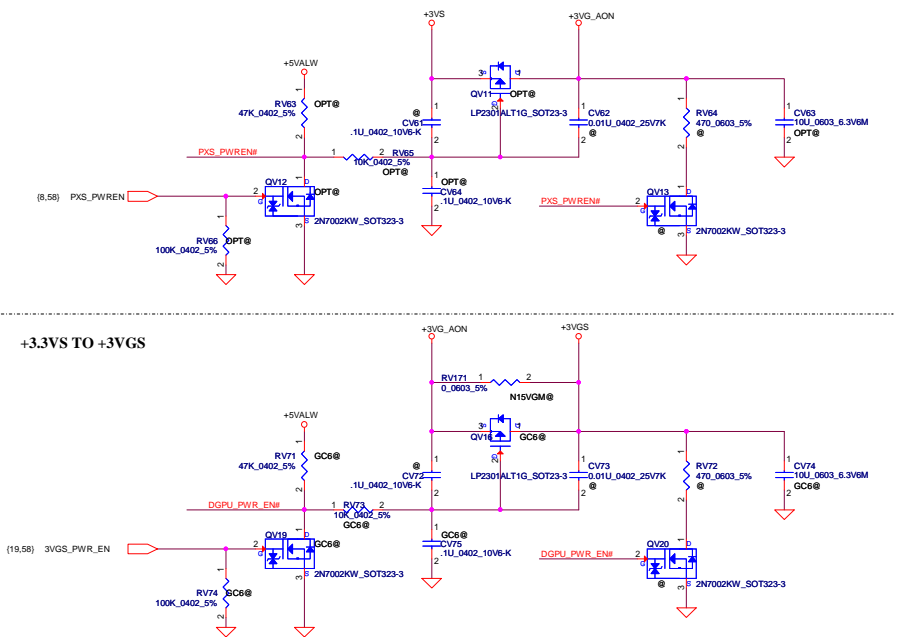
Security Classification	LC Future Center Secret Data	Title	N15X_PCIE/ DAC/ GPIO
Issued Date	2013/08/08	Deciphered Date	2013/08/05
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.			
Document Number	ACL109	Rev	0.2
Date	Monday, December 23, 2013	Sheet	19 of 59



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	N15X_LVDS/HDMI/THERM	
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Doc No	AC109			Date	Monday, December 23, 2013
Sheet	20		of	59	

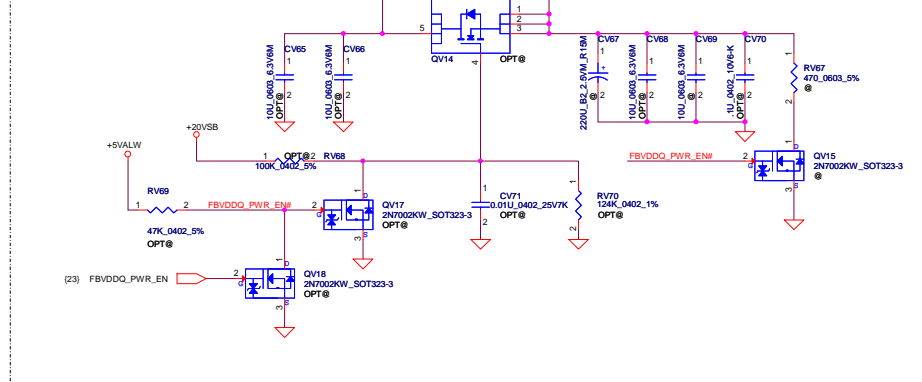


+3.3VS TO +3VG_AON

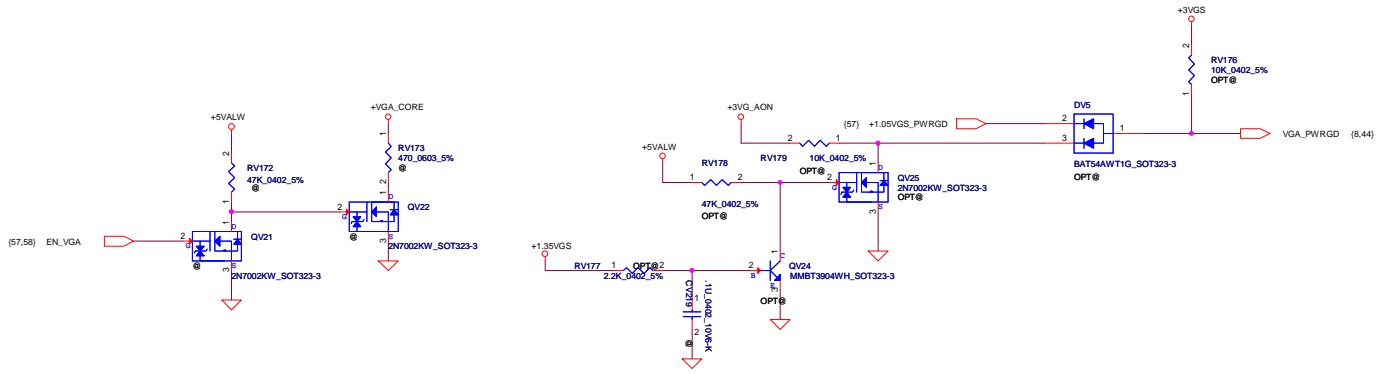
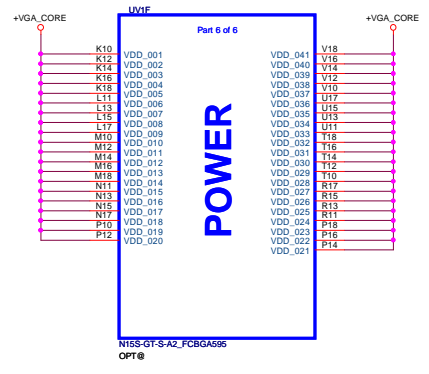
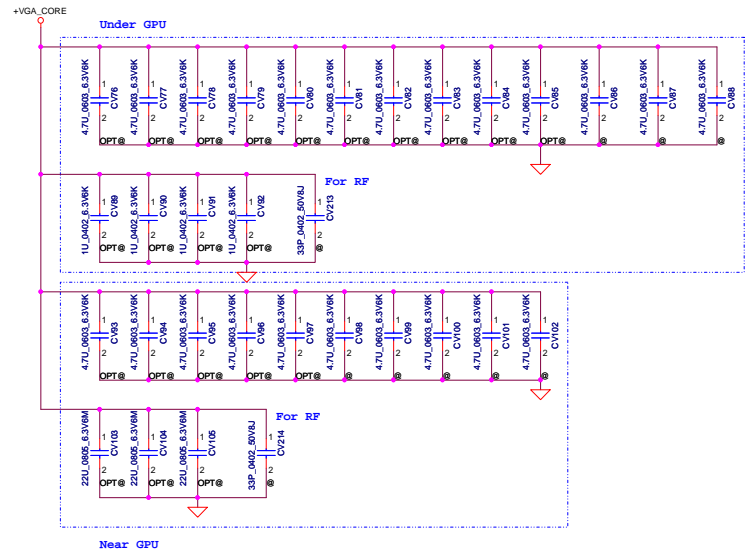
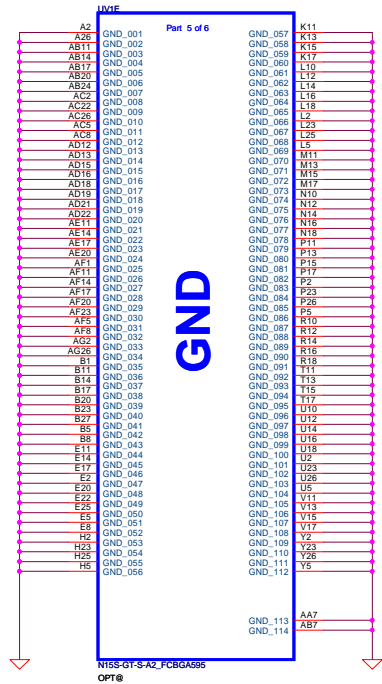


+3.3VS TO +3VGS

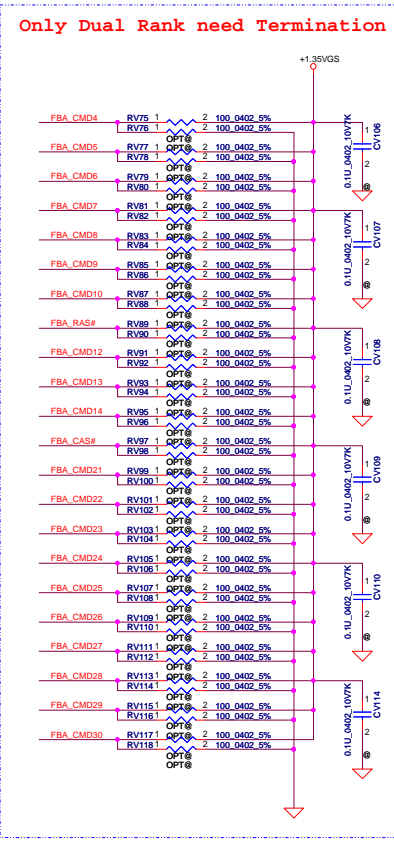
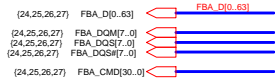
+1.35V TO +1.35VGS



POWER

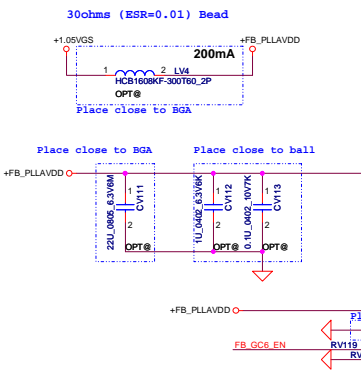


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	N15X_VGA CORE, GND	
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Rev	C	Document Number	AC109	Rev	0.2
Date:	Monday, December 23, 2013	Sheet	22	of	59

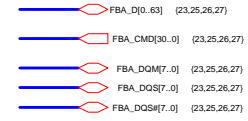
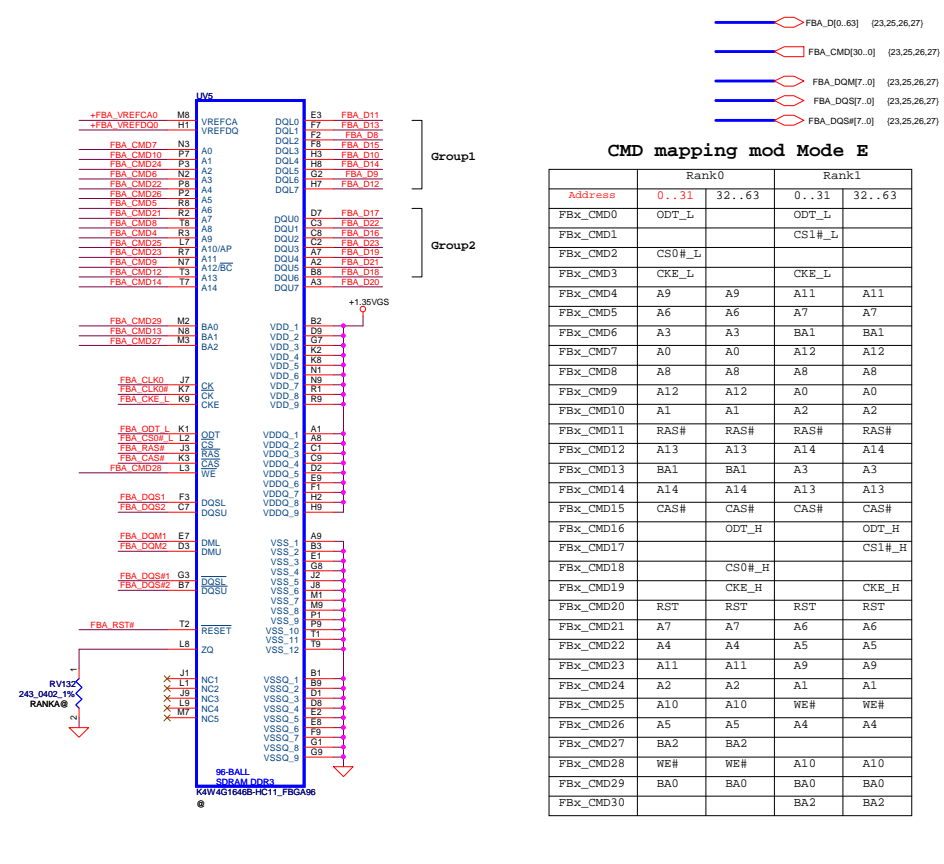
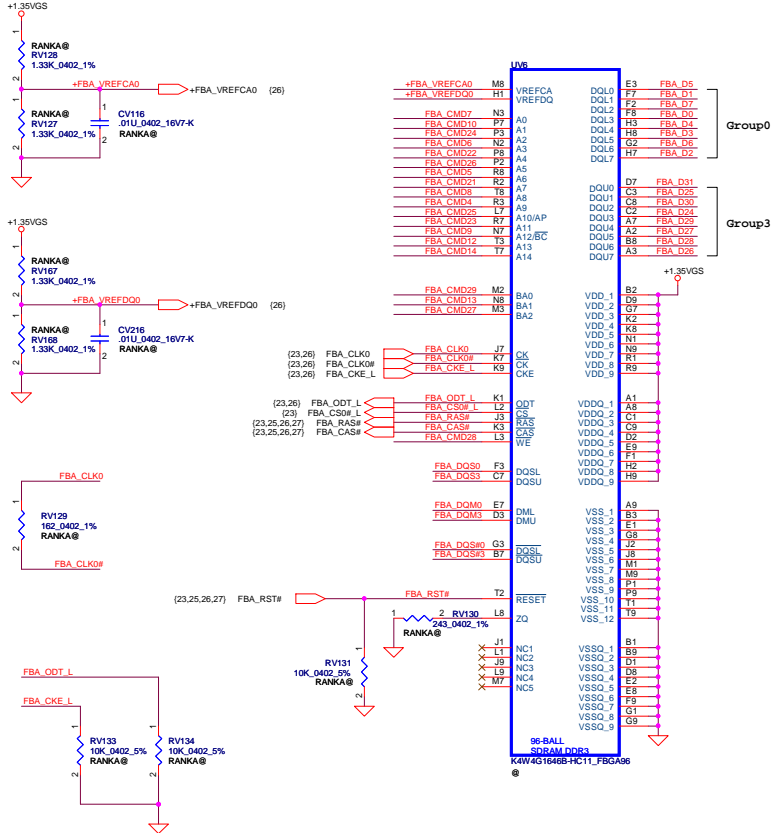


CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBX_CMD0	ODT_L		ODT_L	
FBX_CMD1			CS1#_L	
FBX_CMD2	CS0#_L			
FBX_CMD3	CKE_L		CKE_L	
FBX_CMD4	A9	A9	A11	A11
FBX_CMD5	A6	A6	A7	A7
FBX_CMD6	A3	A3	BA1	BA1
FBX_CMD7	A0	A0	A12	A12
FBX_CMD8	A8	A8	A8	A8
FBX_CMD9	A12	A12	A0	A0
FBX_CMD10	A1	A1	A2	A2
FBX_CMD11	RAS#	RAS#	RAS#	RAS#
FBX_CMD12	AL3	AL3	A14	A14
FBX_CMD13	BA1	BA1	A3	A3
FBX_CMD14	A14	A14	A13	A13
FBX_CMD15	CAS#	CAS#	CAS#	CAS#
FBX_CMD16	ODT_H		ODT_H	
FBX_CMD17			CS1#_H	
FBX_CMD18			CS0#_H	
FBX_CMD19			CKE_H	
FBX_CMD20	RST	RST	RST	RST
FBX_CMD21	A7	A7	A6	A6
FBX_CMD22	A4	A4	A5	A5
FBX_CMD23	A11	A11	A9	A9
FBX_CMD24	A2	A2	A1	A1
FBX_CMD25	A10	A10	WE#	WE#
FBX_CMD26	A5	A5	A4	A4
FBX_CMD27	BA2	BA2		
FBX_CMD28	WE#	WE#	A10	A10
FBX_CMD29	BA0	BA0	BA0	BA0
FBX_CMD30			BA2	BA2

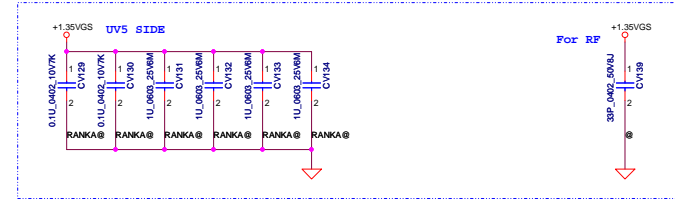
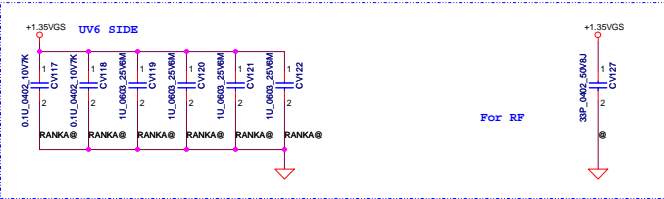


at least 16 mils width(optimal)
20 mils spacing to other signals/planes

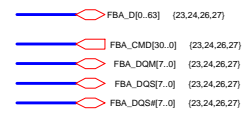
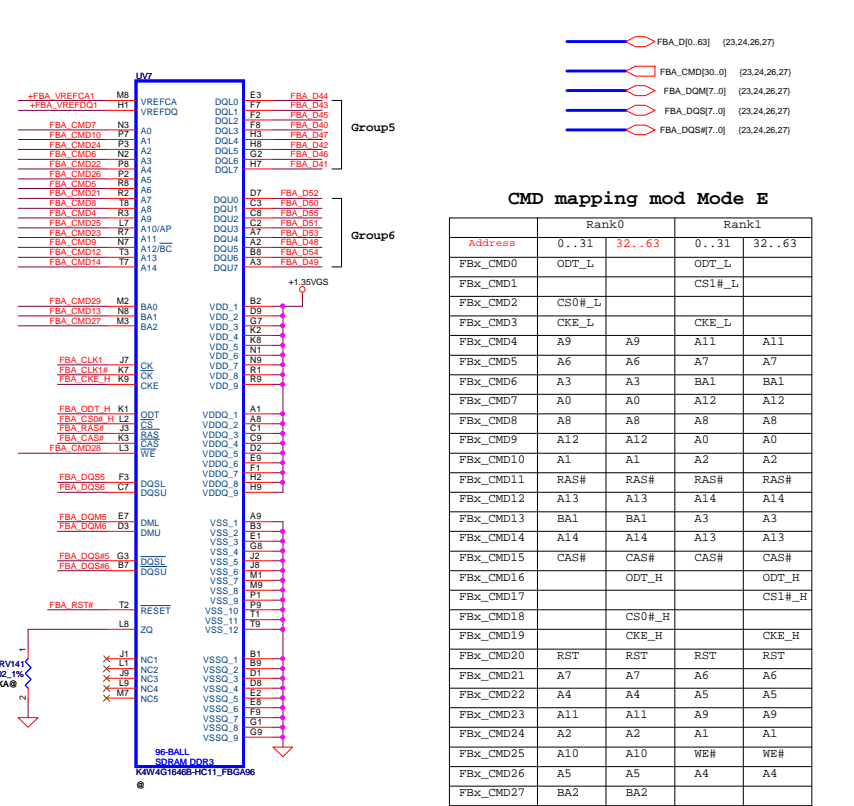
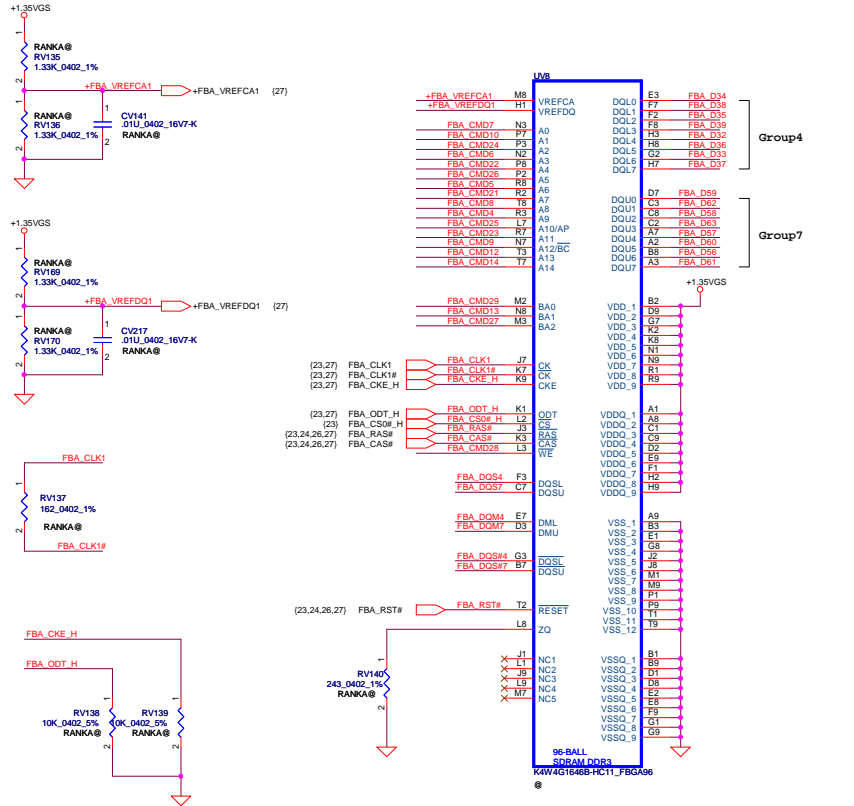


CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3	CKE_L		CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18		CS0#_H		
FBx_CMD19		CHE_H		CHE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2

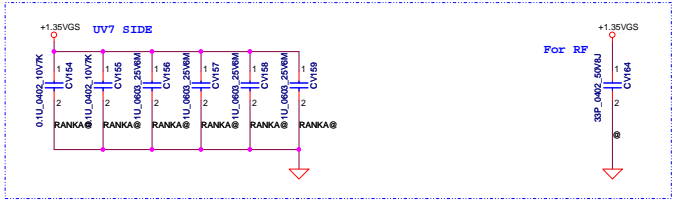
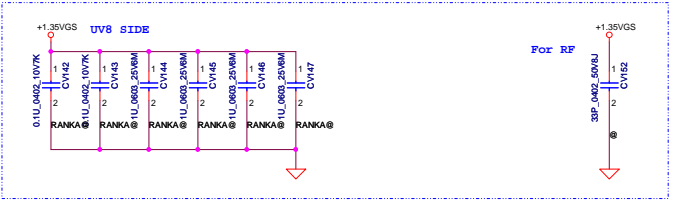


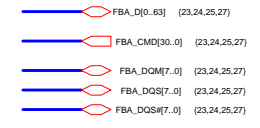
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



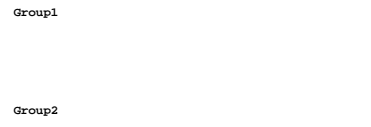
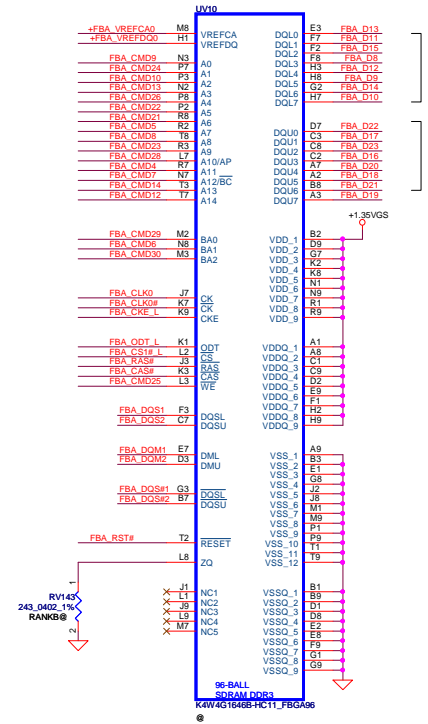
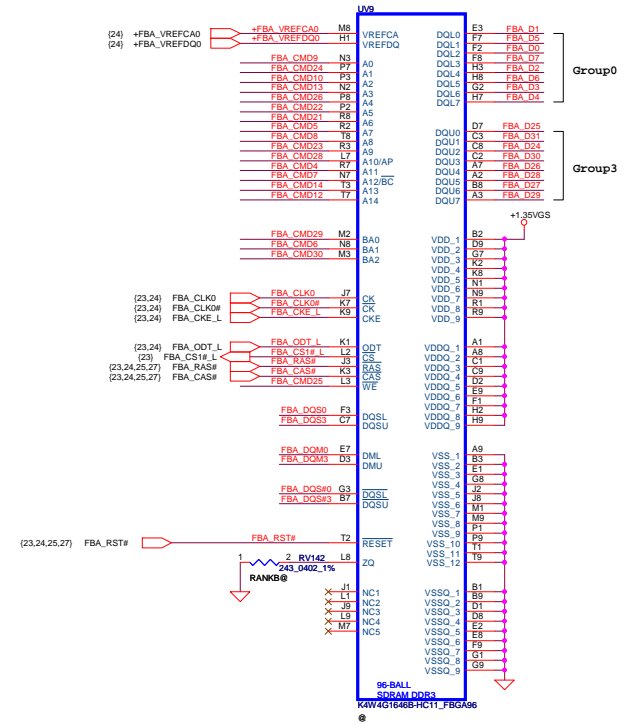
CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
Fbx_CMD0	ODT_L1		ODT_L	
Fbx_CMD1			CS1#_L	
Fbx_CMD2	CS0#_L			
Fbx_CMD3	CKE_L		CKE_L	
Fbx_CMD4	A9	A9	A11	A11
Fbx_CMD5	A6	A6	A7	A7
Fbx_CMD6	A3	A3	BA1	BA1
Fbx_CMD7	A0	A0	A12	A12
Fbx_CMD8	A8	A8	A8	A8
Fbx_CMD9	A12	A12	A0	A0
Fbx_CMD10	A1	A1	A2	A2
Fbx_CMD11	RAS#	RAS#	RAS#	RAS#
Fbx_CMD12	A13	A13	A14	A14
Fbx_CMD13	BA1	BA1	A3	A3
Fbx_CMD14	A14	A14	A13	A13
Fbx_CMD15	CAS#	CAS#	CAS#	CAS#
Fbx_CMD16		ODT_H		ODT_H
Fbx_CMD17			CS1#_H	
Fbx_CMD18		CS0#_H		
Fbx_CMD19		CKE_H		CKE_H
Fbx_CMD20	RST	RST	RST	RST
Fbx_CMD21	A7	A7	A6	A6
Fbx_CMD22	A4	A4	A5	A5
Fbx_CMD23	A11	A11	A9	A9
Fbx_CMD24	A2	A2	A1	A1
Fbx_CMD25	A10	A10	WE#	WE#
Fbx_CMD26	A5	A5	A4	A4
Fbx_CMD27	BA2	BA2		
Fbx_CMD28	WE#	WE#	A10	A10
Fbx_CMD29	BA0	BA0	BA0	BA0
Fbx_CMD30			BA2	BA2



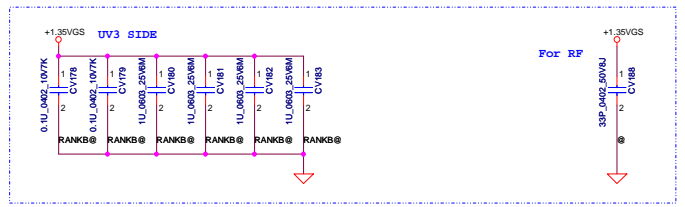
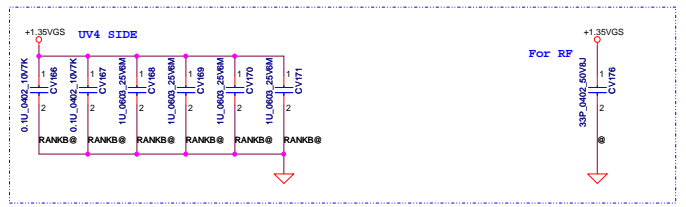


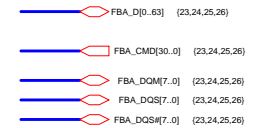
at least 16 mils width (optimal)
20 mils spacing to other signals / planes



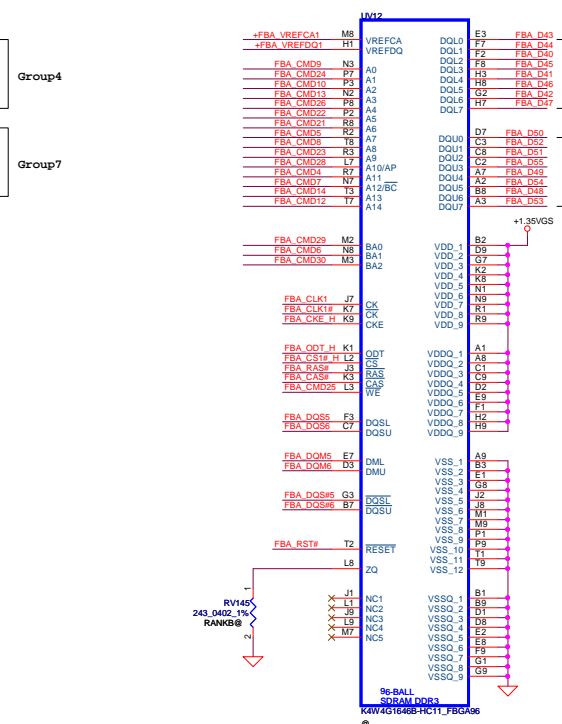
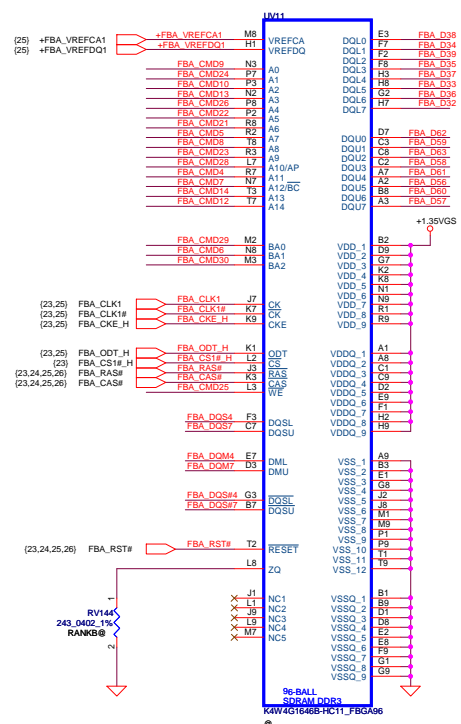
CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3			CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16		ODT_H		ODT_H
FBx_CMD17			CS1#_H	
FBx_CMD18			CS0#_H	
FBx_CMD19			CHE_H	
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2



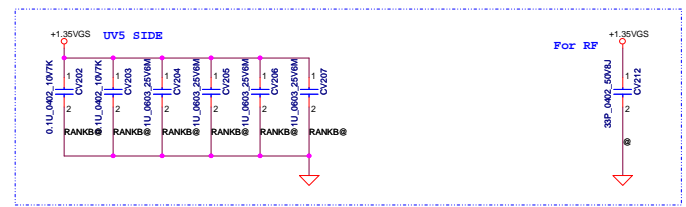
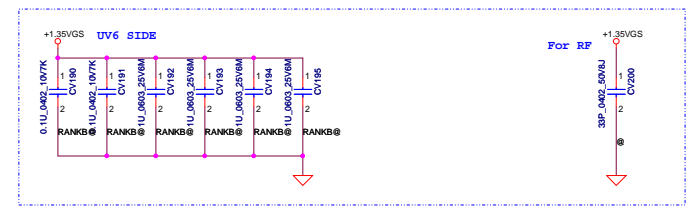


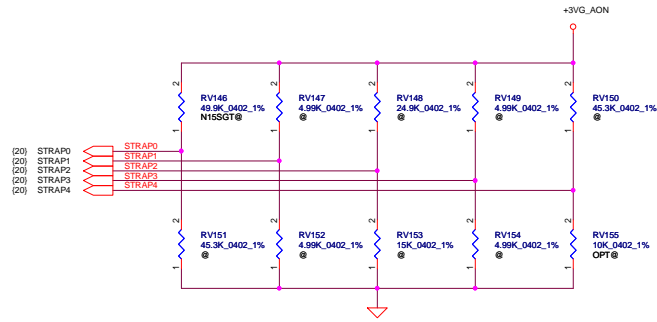
at least 16 mils width(optimal)
20 mils spacing to other signals



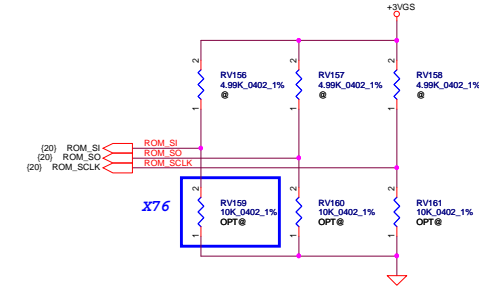
CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FBx_CMD0	ODT_L		ODT_L	
FBx_CMD1			CS1#_L	
FBx_CMD2	CS0#_L			
FBx_CMD3			CKE_L	
FBx_CMD4	A9	A9	A11	A11
FBx_CMD5	A6	A6	A7	A7
FBx_CMD6	A3	A3	BA1	BA1
FBx_CMD7	A0	A0	A12	A12
FBx_CMD8	A8	A8	A8	A8
FBx_CMD9	A12	A12	A0	A0
FBx_CMD10	A1	A1	A2	A2
FBx_CMD11	RAS#	RAS#	RAS#	RAS#
FBx_CMD12	A13	A13	A14	A14
FBx_CMD13	BA1	BA1	A3	A3
FBx_CMD14	A14	A14	A13	A13
FBx_CMD15	CAS#	CAS#	CAS#	CAS#
FBx_CMD16			ODT_H	ODT_H
FBx_CMD17				CS1#_H
FBx_CMD18			CS0#_H	
FBx_CMD19			CKE_H	CKE_H
FBx_CMD20	RST	RST	RST	RST
FBx_CMD21	A7	A7	A6	A6
FBx_CMD22	A4	A4	A5	A5
FBx_CMD23	A11	A11	A9	A9
FBx_CMD24	A2	A2	A1	A1
FBx_CMD25	A10	A10	WE#	WE#
FBx_CMD26	A5	A5	A4	A4
FBx_CMD27	BA2	BA2		
FBx_CMD28	WE#	WE#	A10	A10
FBx_CMD29	BA0	BA0	BA0	BA0
FBx_CMD30			BA2	BA2





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				



Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
SD0344528T	1001	0001
10K	1010	0010
15K	1011	0011
20K	1100	0100
24.9K	1101	0101
SD0344528T	1110	0110
30.1K	1111	0111
SD0344528T		
34.8K		
45.3K		
SD03445328T		

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

X76

GPU	FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4		
N155-GT	Hynix 900MHz	H5TC4G63AFR-11C	0x3	PD 20K	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
	Micron 900MHz	MT41J256M16HA-093G:E	0x4	PD 24.9K							
	Samsung 900MHz	K4W4G1646D-BC1A	0x5	PD 30.1K							
		256M x 16									

GPU	FB Memory (DDR3)	STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-GM	Hynix 900MHz	H5TC4G63AFR-11C	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
	Micron 900MHz	MT41J256M16HA-093G:E	PU 10K	PU 10K	PD 10K	PU 10K			
	Hynix 900MHz	H5TC2G63FFR-11C	PU 10K	PU 10K	PD 10K	PD 10K			
	Micron 900MHz	MT41J128M16JT-093G	PD 10K	PD 10K	PD 10K	PU 10K			
	Samsung 900MHz	K4W2G1646Q-BC1A	PU 10K	PU 10K	PU 10K	PD 10K			
		128M x 16							

VRAM	X76	VRAM P/N
Samsung	X7604112001	SA00005SH40
Micron	X7604012002	SA00005M120
Hynix	X7604012001	SA00005VS00

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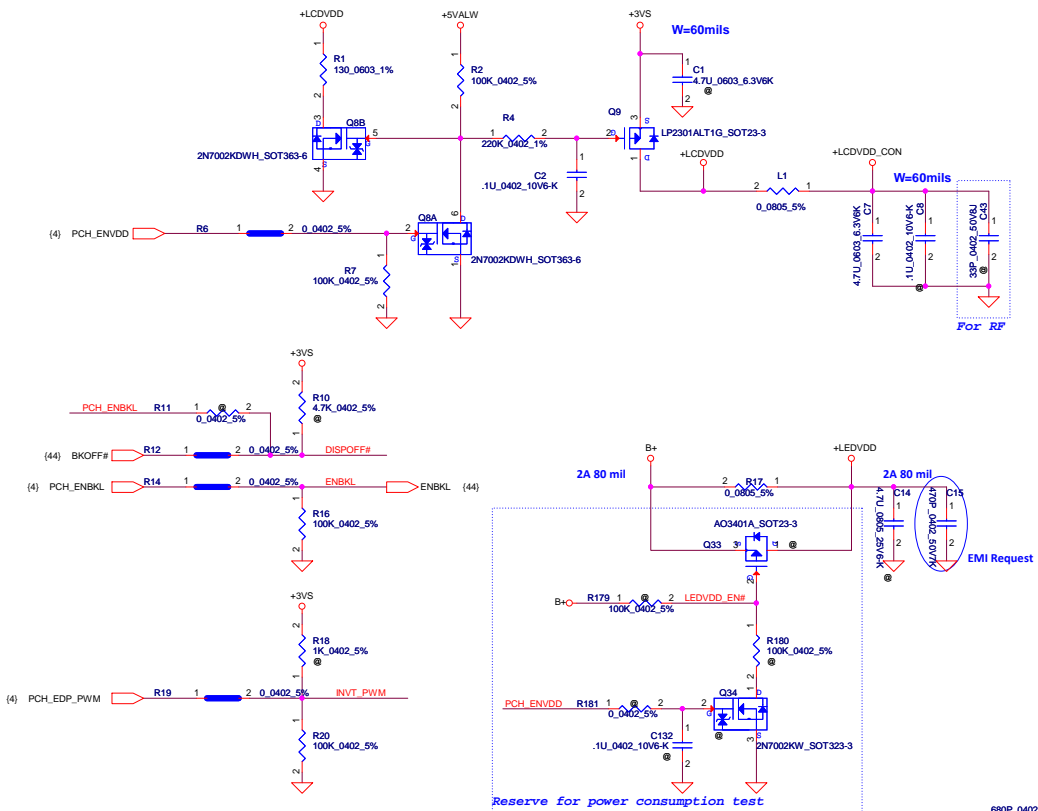
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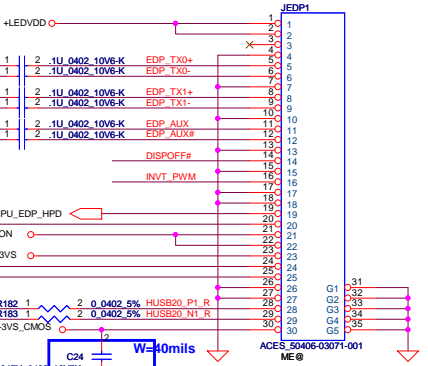
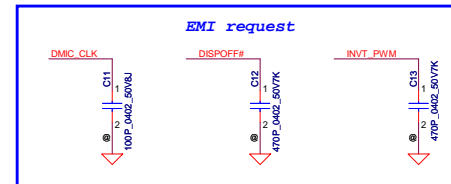
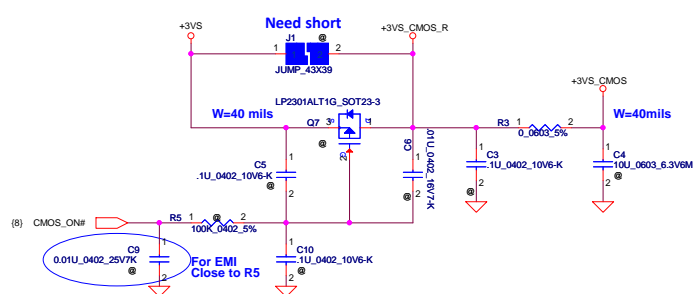
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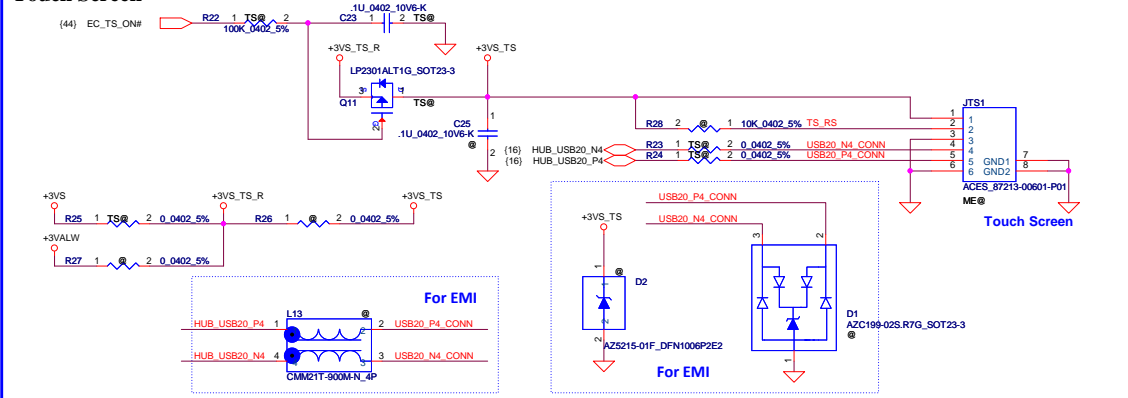
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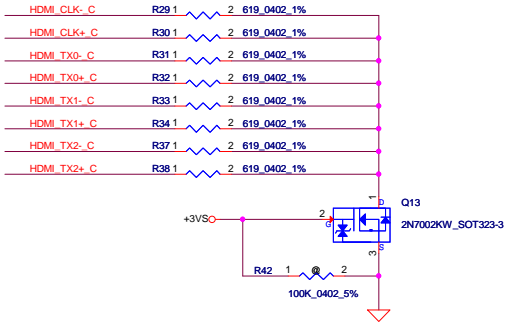
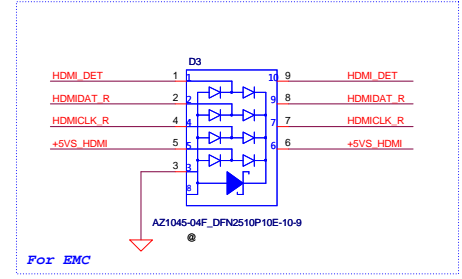
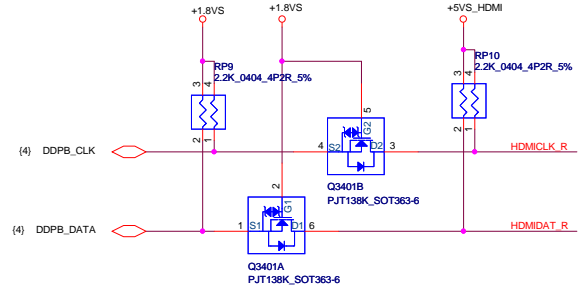
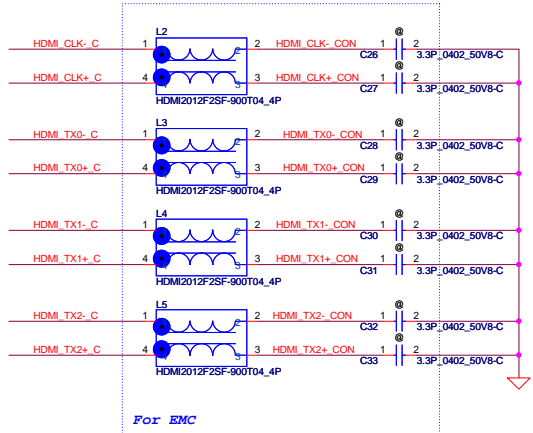
CMOS Camera



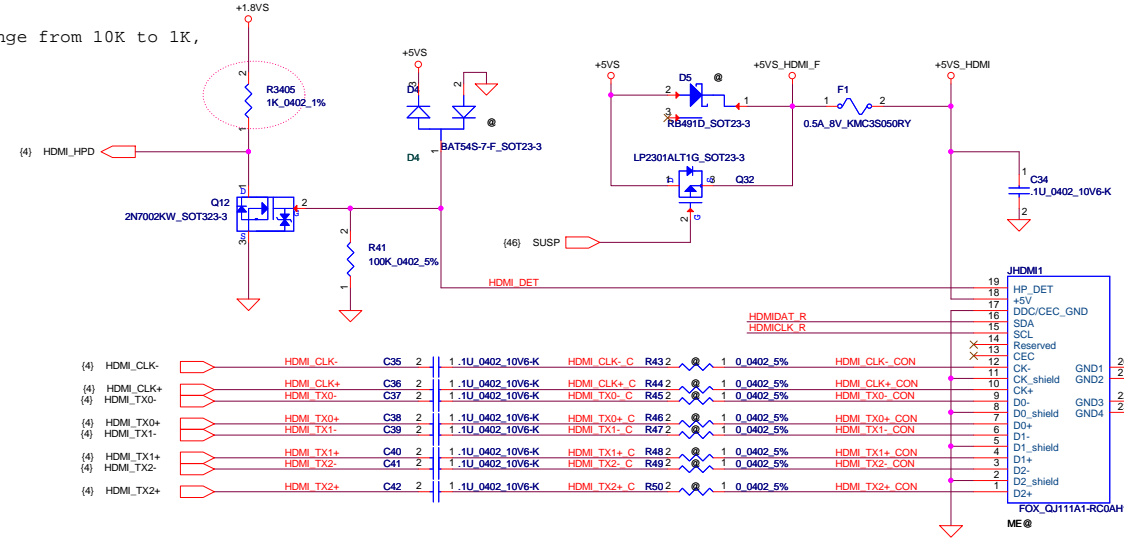
Touch Screen



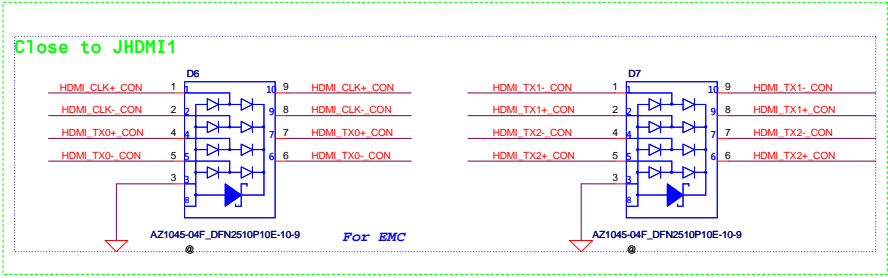
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R4602 change from 10K to 1K, as Vienna



(4) HDMI_CLK-	HDMI_CLK-	C35	2	1.1U_0402_10V6-K	HDMI_CLK- C	R43	2	1	0.0402_5%	HDMI_CLK- CON
(4) HDMI_CLK+	HDMI_CLK+	C36	2	1.1U_0402_10V6-K	HDMI_CLK+ C	R44	2	1	0.0402_5%	HDMI_CLK+ CON
(4) HDMI_TX0-	HDMI_TX0-	C37	2	1.1U_0402_10V6-K	HDMI_TX0- C	R45	2	1	0.0402_5%	HDMI_TX0- CON
(4) HDMI_TX0+	HDMI_TX0+	C38	2	1.1U_0402_10V6-K	HDMI_TX0+ C	R46	2	1	0.0402_5%	HDMI_TX0+ CON
(4) HDMI_TX1-	HDMI_TX1-	C39	2	1.1U_0402_10V6-K	HDMI_TX1- C	R47	2	1	0.0402_5%	HDMI_TX1- CON
(4) HDMI_TX1+	HDMI_TX1+	C40	2	1.1U_0402_10V6-K	HDMI_TX1+ C	R48	2	1	0.0402_5%	HDMI_TX1+ CON
(4) HDMI_TX2-	HDMI_TX2-	C41	2	1.1U_0402_10V6-K	HDMI_TX2- C	R49	2	1	0.0402_5%	HDMI_TX2- CON
(4) HDMI_TX2+	HDMI_TX2+	C42	2	1.1U_0402_10V6-K	HDMI_TX2+ C	R50	2	1	0.0402_5%	HDMI_TX2+ CON



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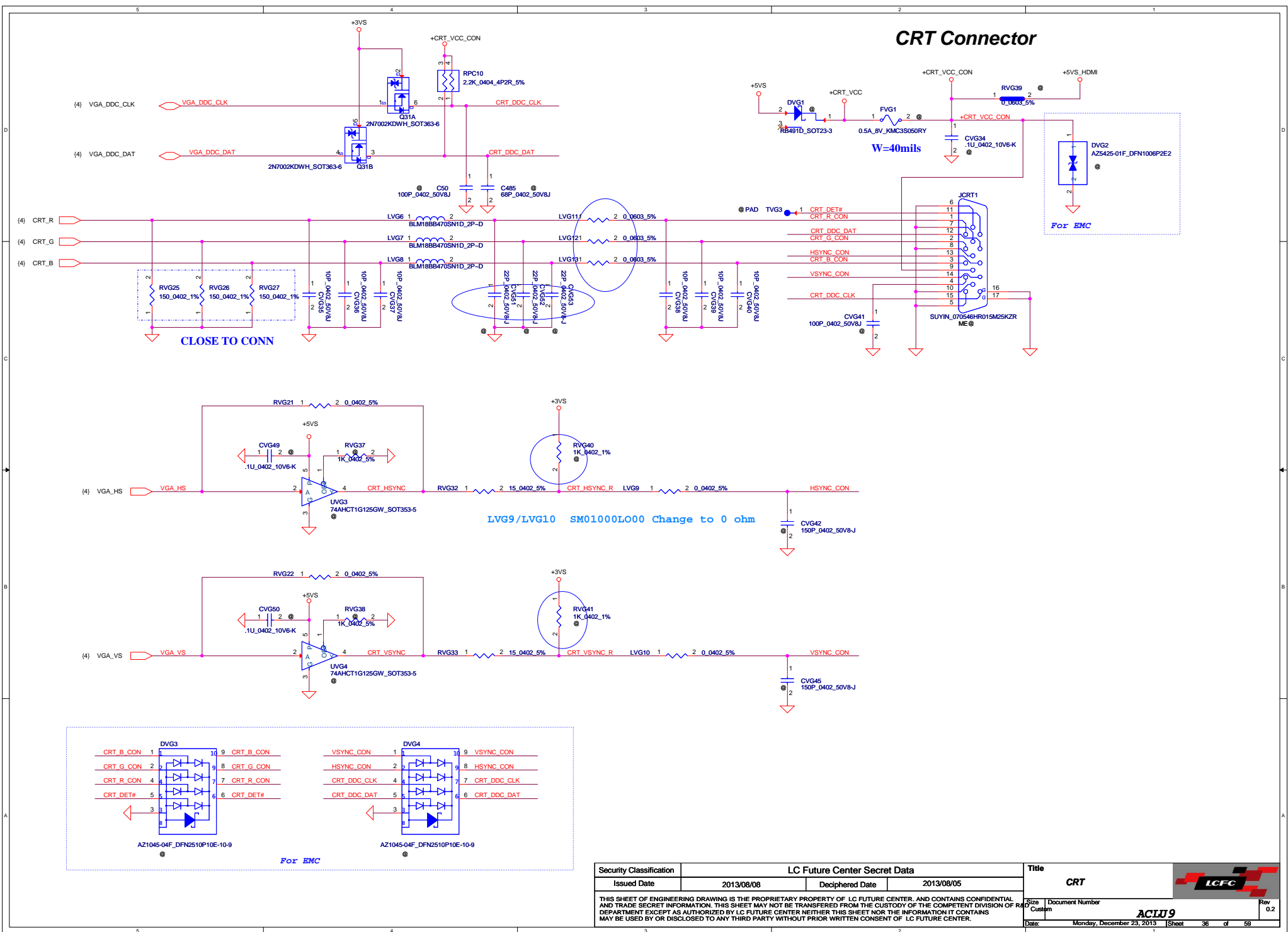
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Title	DP to CRT Converter(PS8613)		
Size	Document Number	Rev	
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CRT Connector

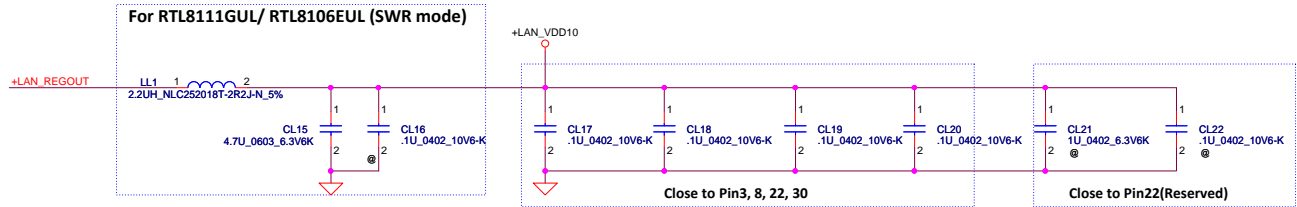
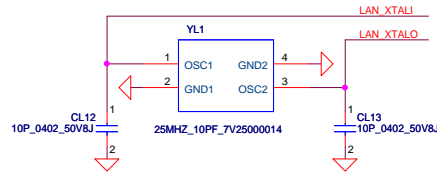
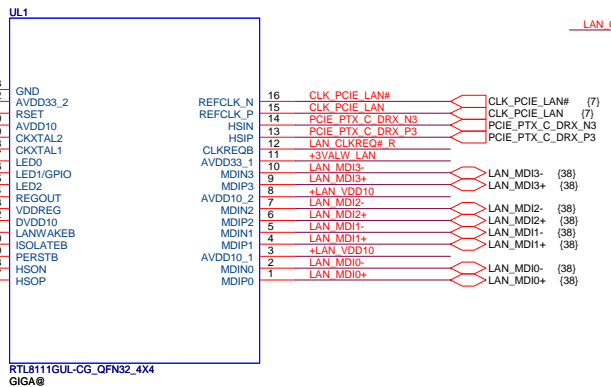
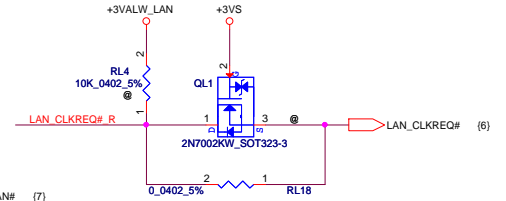
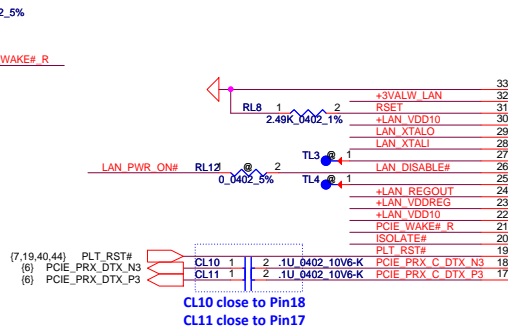
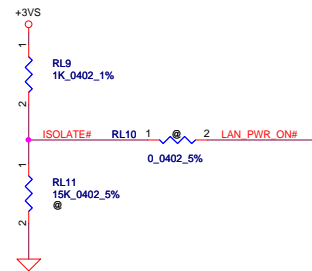
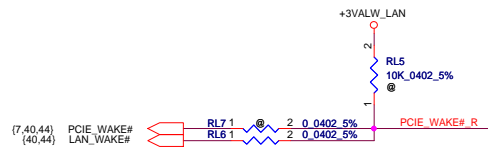
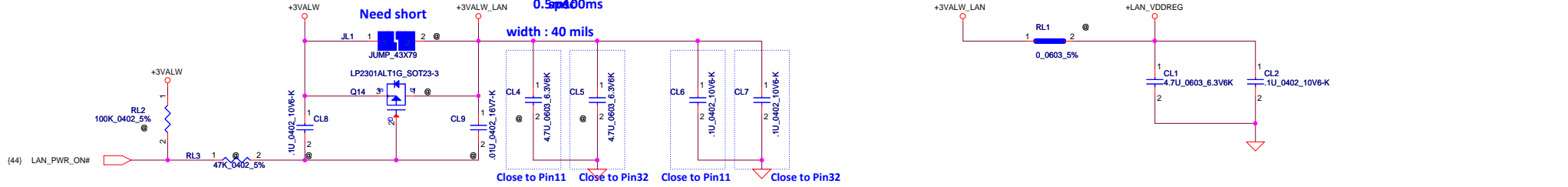


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+3VALW TO +3VALW_LAN

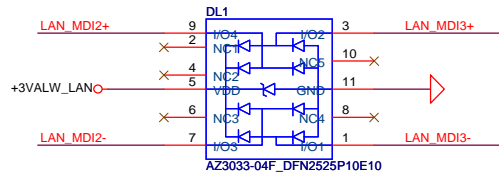
+3VALW_LAN rising time (10%~90%):
0.5~100ms



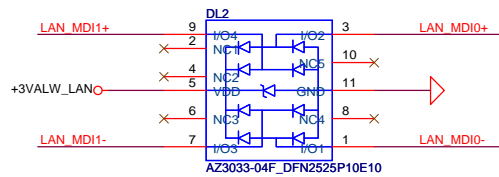
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1 +LAN_REGOUT: Width =60mil

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Custom		Monday, December 23, 2013		0.2
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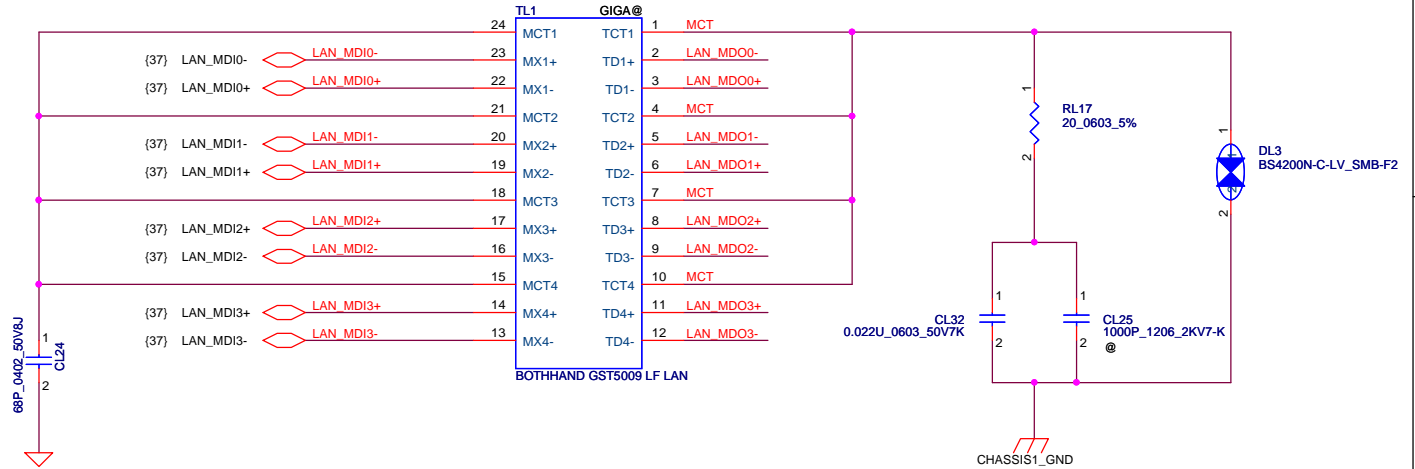
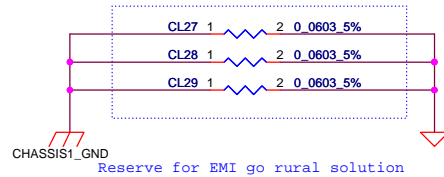
**DL1/DL2
1'S PN:SC300003M00**



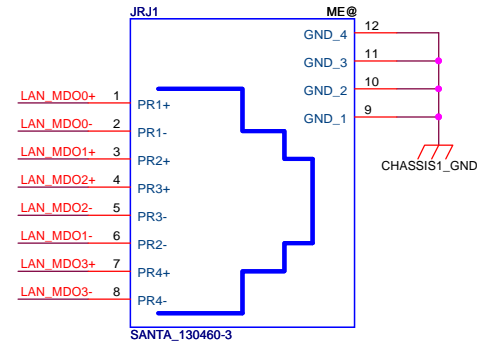
Place Close to TL1



Place Close to TL2

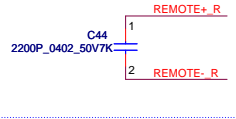


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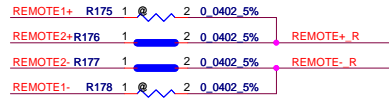
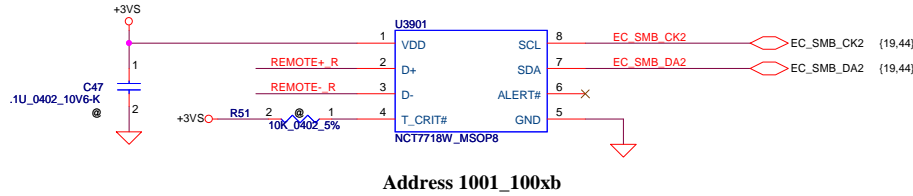


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Size	Document Number	Rev								
	ACLJ9	0.2								
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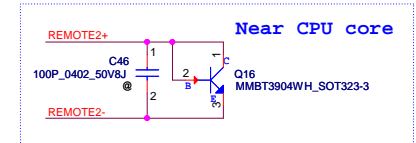
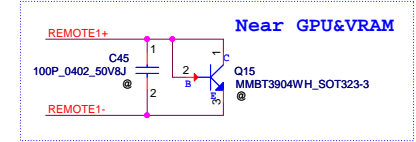
Close to U3901



SMSC thermal sensor placed near DIMM

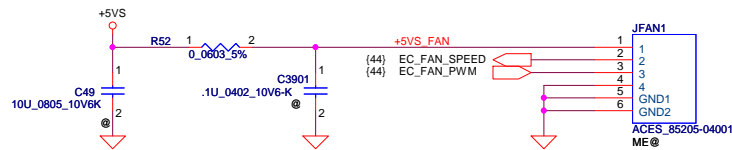



REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



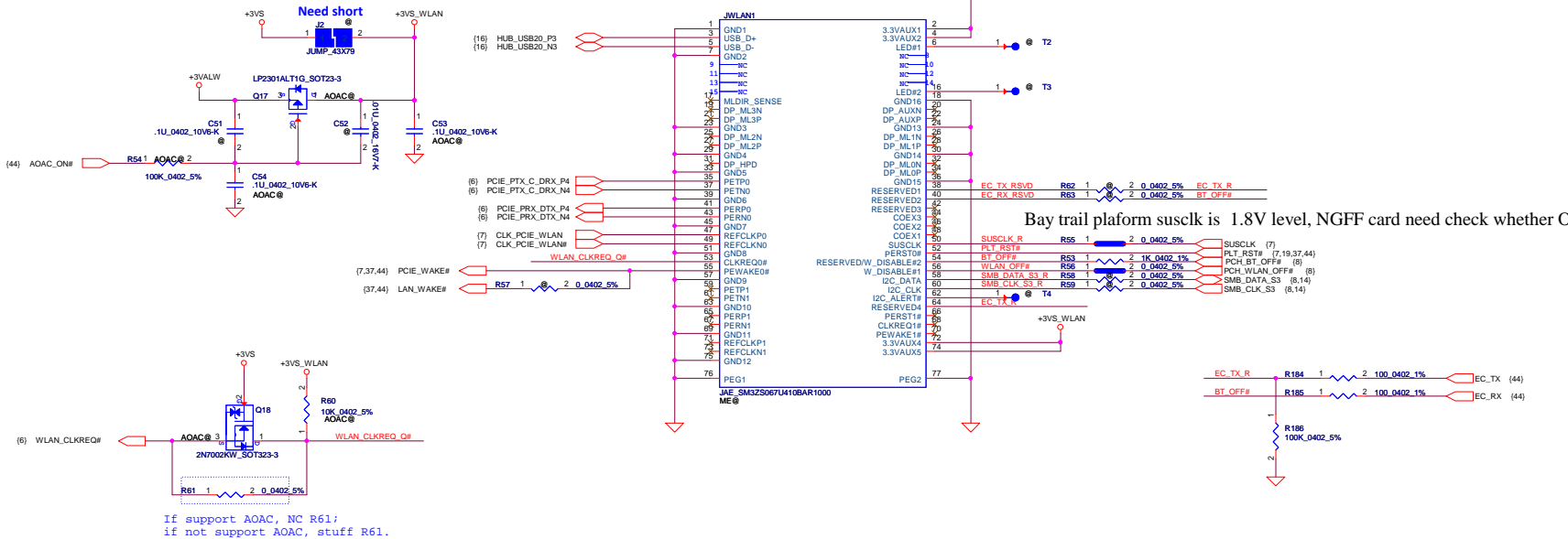
Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal

FAN Conn



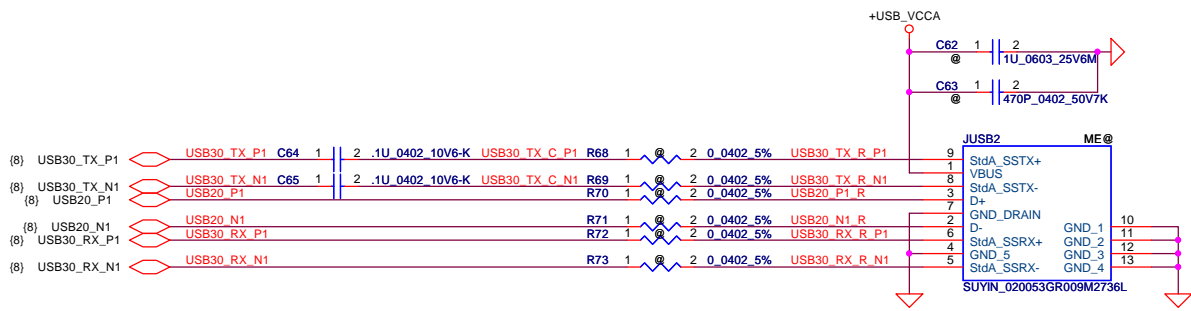
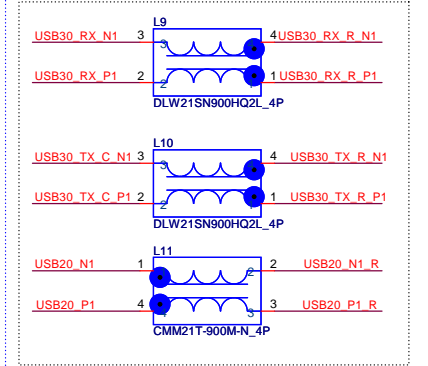
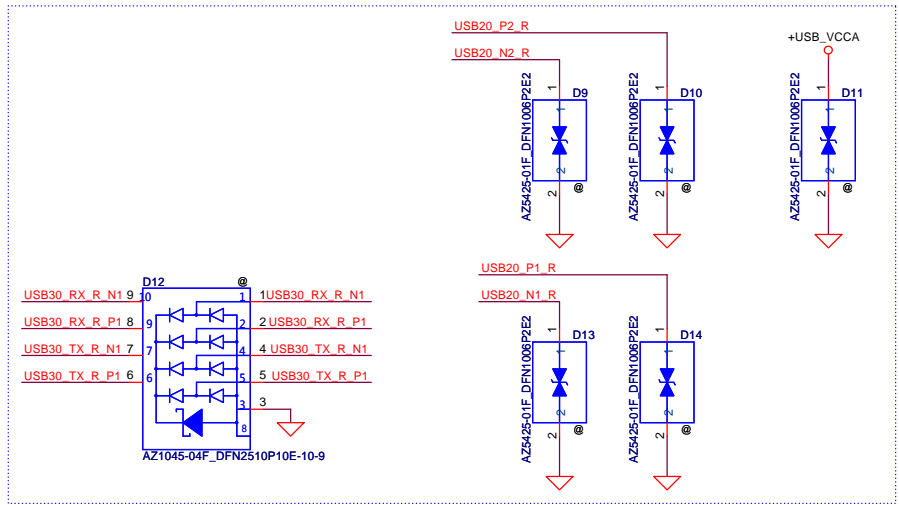
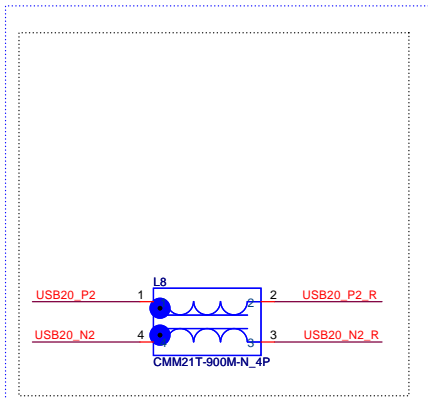
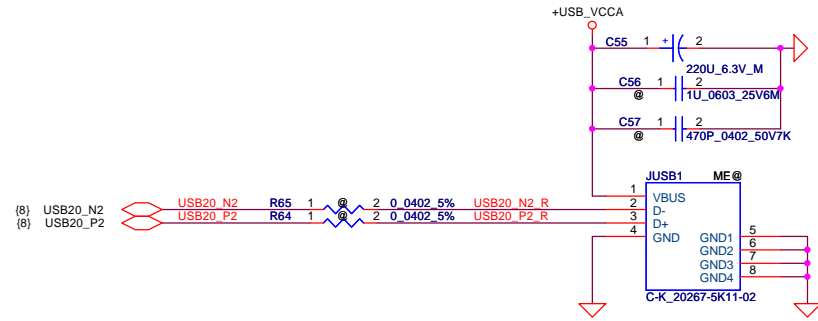
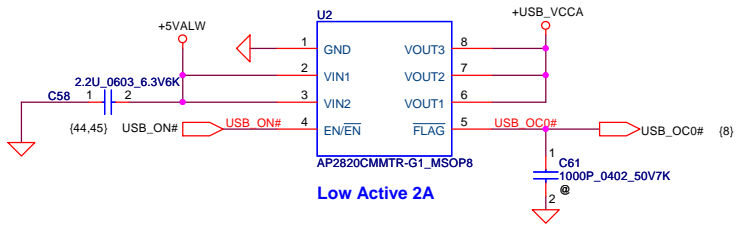
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Mini-Express Card(WLAN/WiMAX)



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2013/08/08		2013/08/05		LCFC	
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				Custom	0.2
				Date:	Monday, December 23, 2013
				Sheet	40 of 59

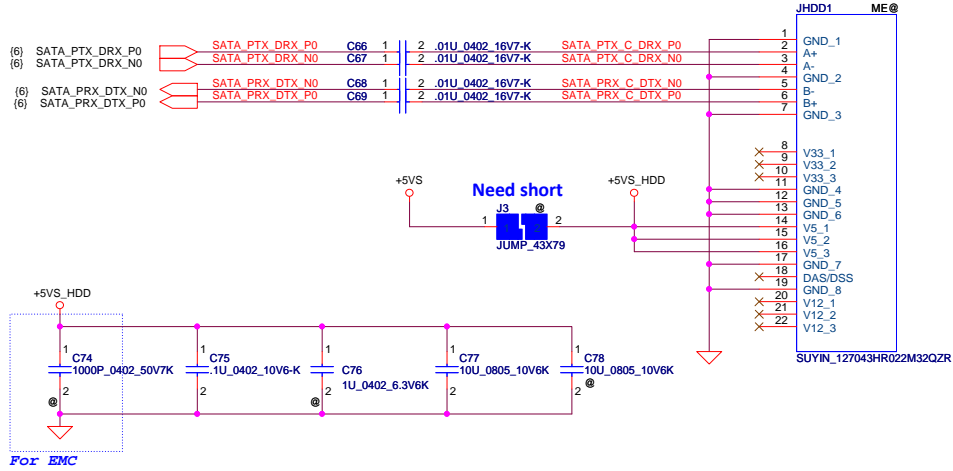
LEFT SIDE USB3.0 PORT X2



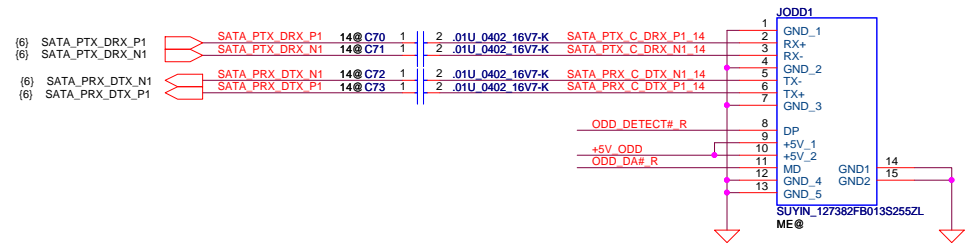
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title		
USB2.0/USB3.0 PORT (LEFT)		
Size	Document Number	ACLU9
Custom		
Date:	Monday, December 23, 2013	Sheet 41 of 59
		Rev 0.2

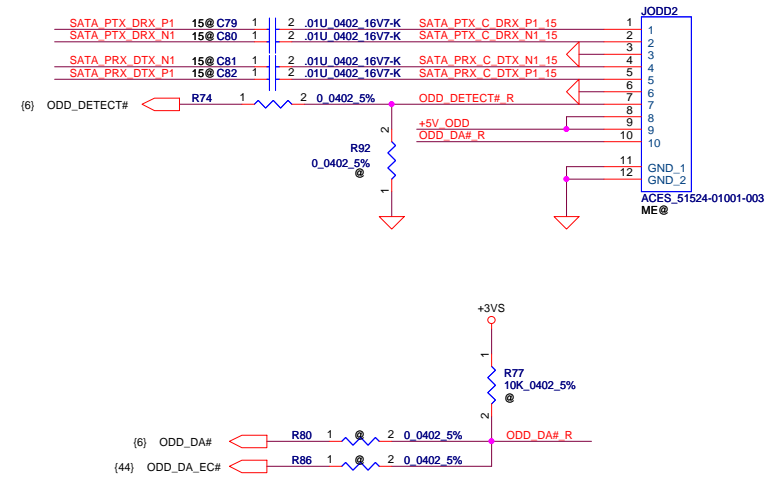
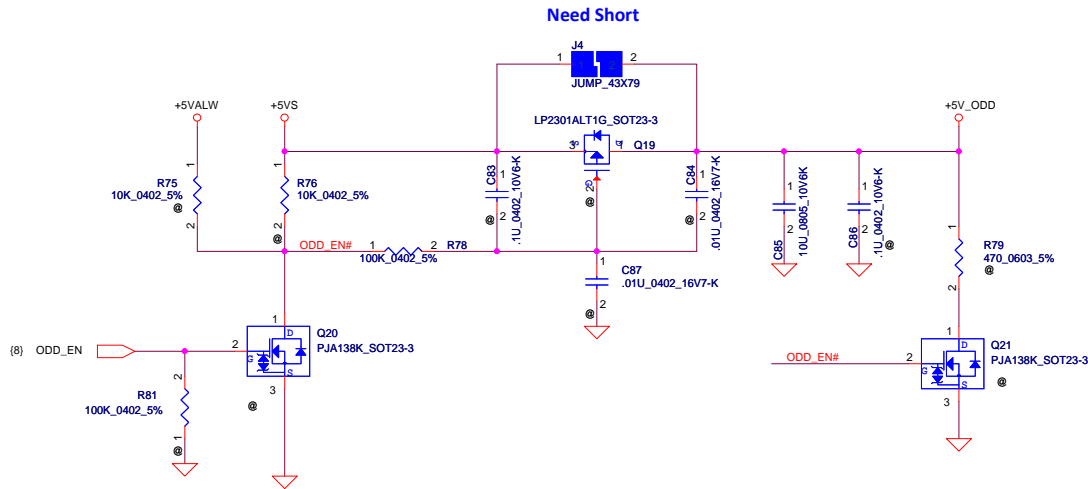
SATA HDD Conn.



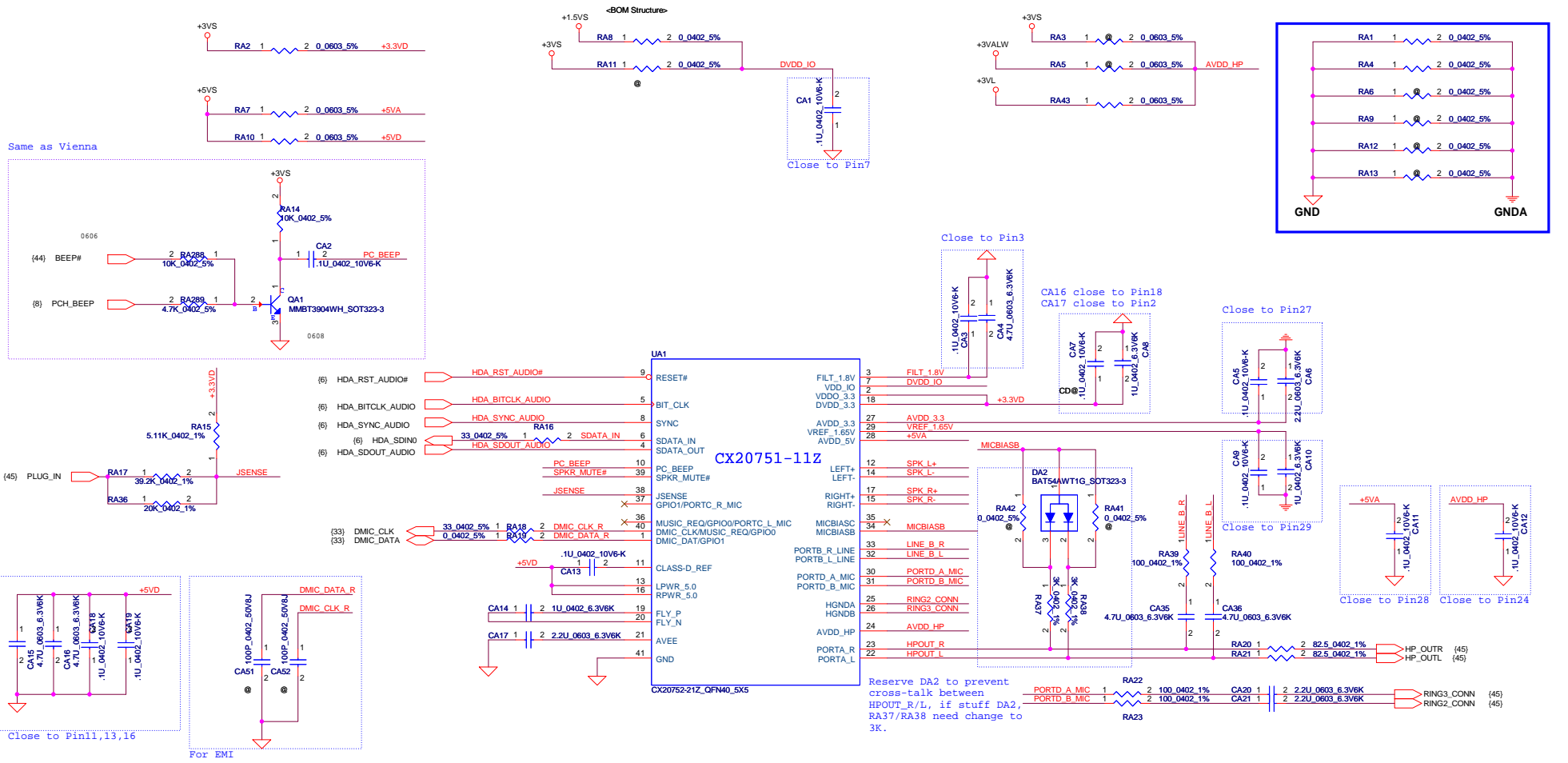
FOR 14" SATA ODD Conn.



FOR 15" SATA ODD FFC Conn



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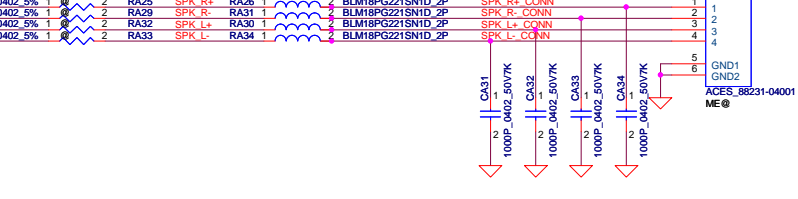
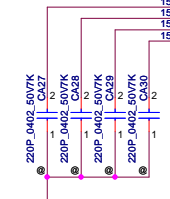
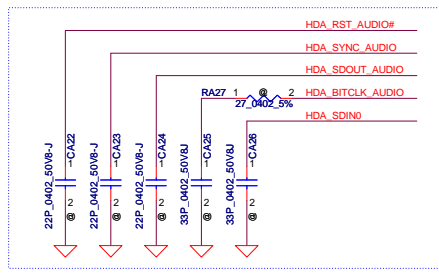
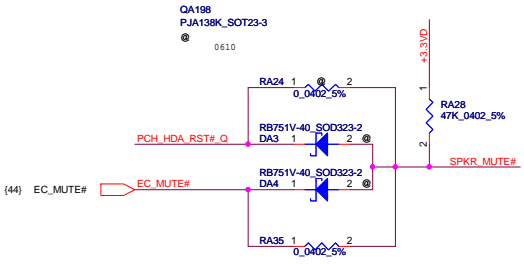
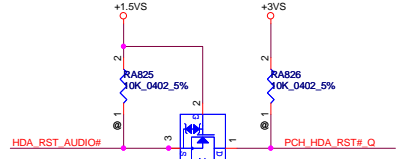
Same as Vienna

(45) PLUG_IN

Close to Pin1,13,16

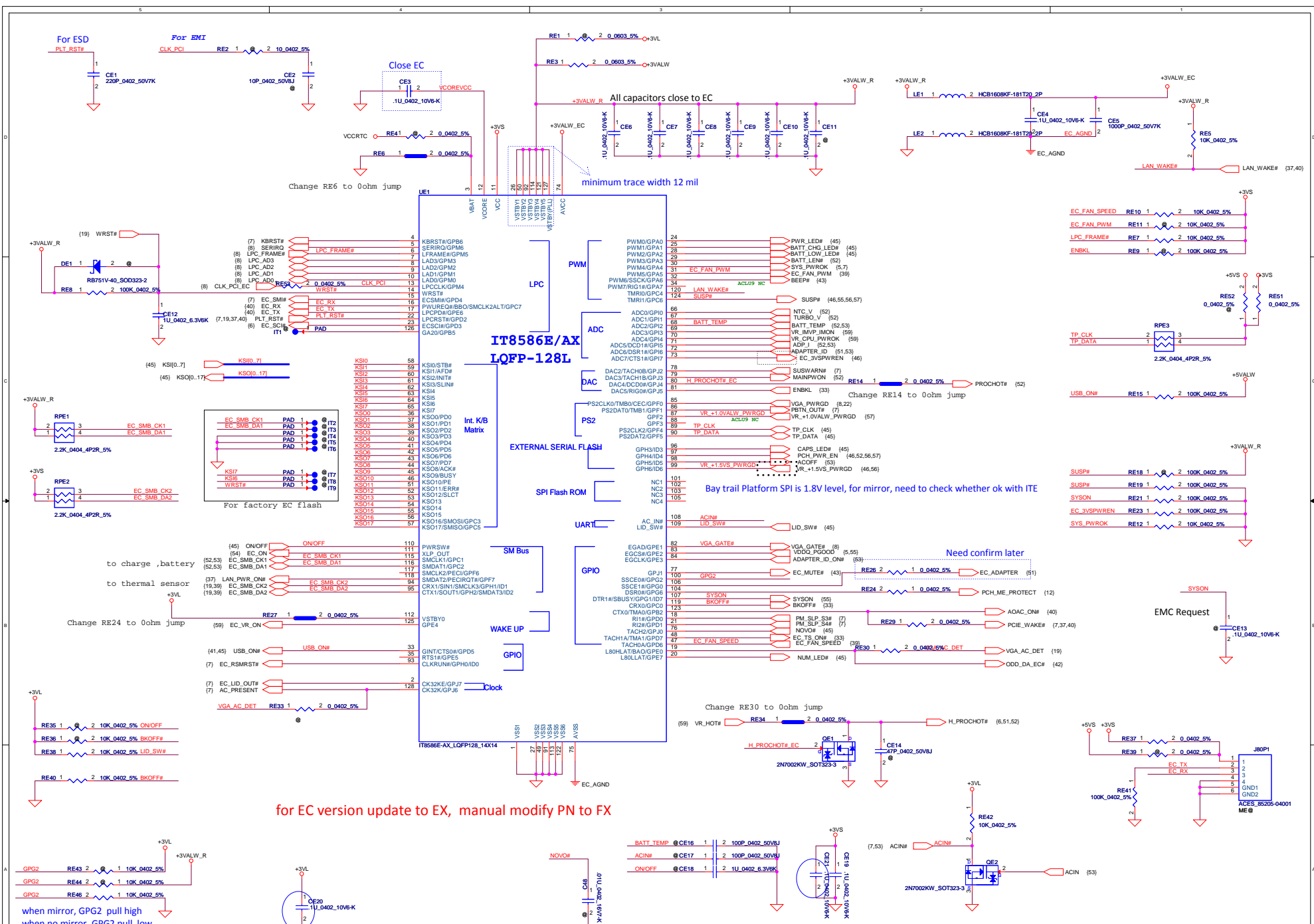
FOR EMI

For EMI



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Title		LCFC	
Codec_CX20751		ACLU9	
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for EC version update to EX, manual modify PN to FX

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Issued Date	2013/08/08	Deciphered Date
		2013/08/05

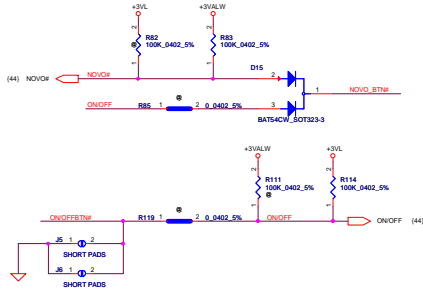
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This	EC ITE8586LQFP	
Document Number	ACT19	
Date	Monday, December 23, 2013	Sheet 44 of 49



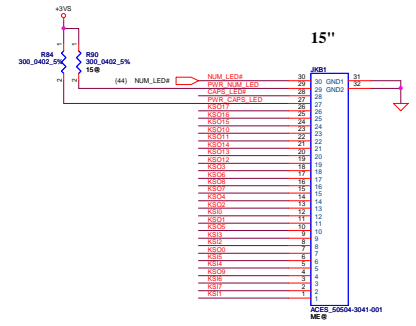
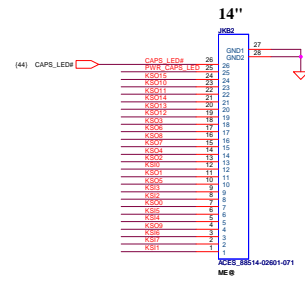
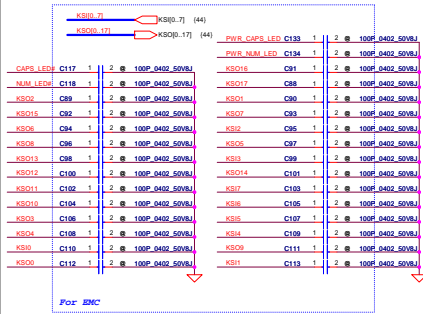
Rev 0.2

ON/OFF switch

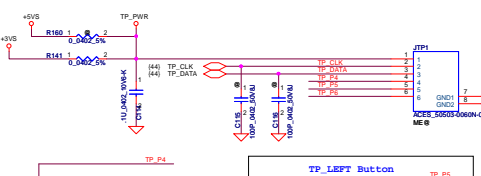


TP/B Connector

K/B Connector



	14"	15"
KB_1	KS11_14	KS00_15
KB_2	KS17_14	KS12_15
KB_3	KS16_14	KS13_15
KB_4	KS09_14	KS05_15
KB_5	KS14_14	KS01_15
KB_6	KS15_14	KS10_15
KB_7	KS00_14	KS02_15
KB_8	KS12_14	KS04_15
KB_9	KS13_14	KS07_15
KB_10	KS05_14	KS08_15
KB_11	KS01_14	KS06_15
KB_12	KS10_14	KS03_15
KB_13	KS02_14	KS02_15
KB_14	KS04_14	KS03_15
KB_15	KS07_14	KS04_15
KB_16	KS08_14	KS01_14
KB_17	KS06_14	KS01_15
KB_18	KS03_14	KS05_15
KB_19	KS02_14	KS04_15
KB_20	KS01_14	KS07_15
KB_21	KS14_14	FB_LED_PWR_15
KB_22	KS01_14	CAPS_LED_15
KB_23	KS10_14	VDD_15
KB_24	KS05_14	RINK_LED_15



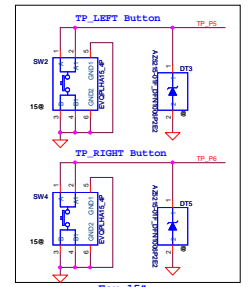
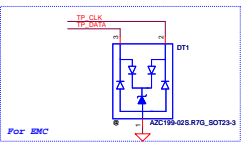
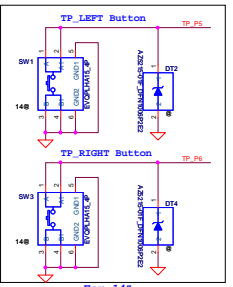
For 14"

1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

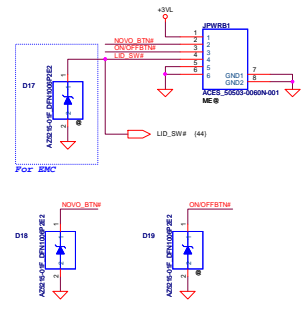
For 15"

1	VDD
2	CLK
3	DAT
4	GND
5	TP-L
6	TP-R

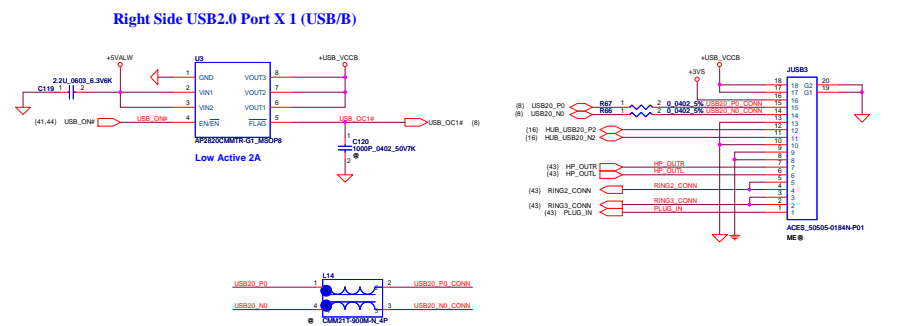
Change to same as ACLUA



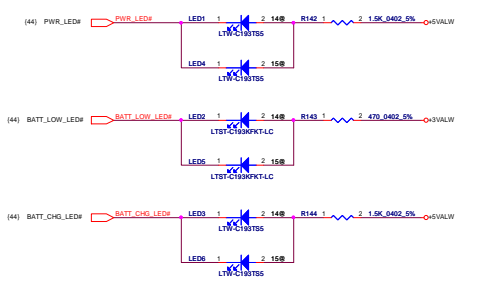
PWR/B Connector



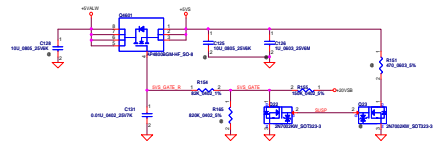
USB I/O Connector



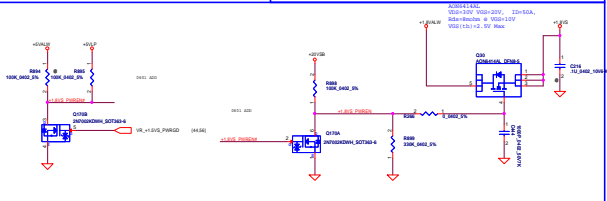
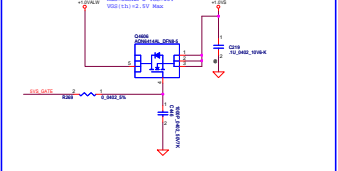
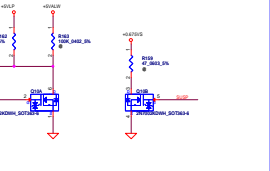
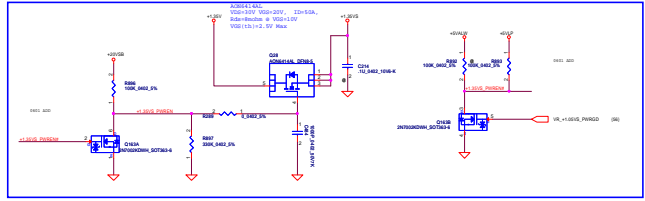
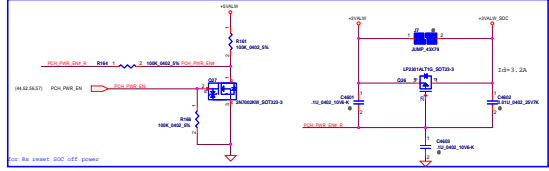
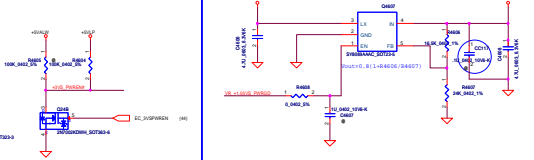
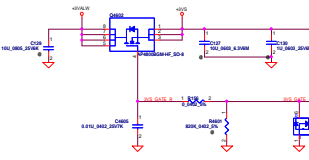
LED



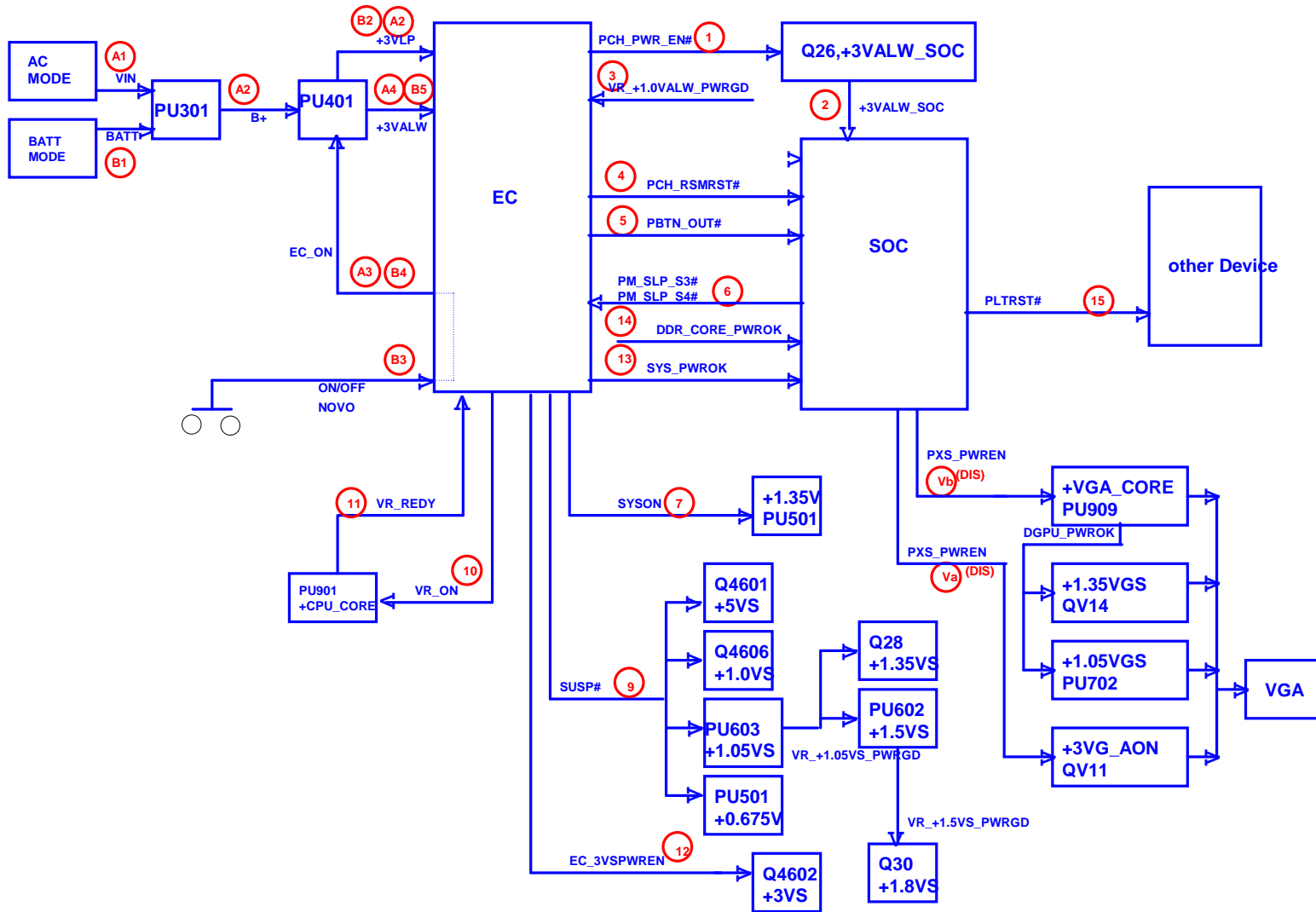
+5VALW to +5VS AP4800BGW
 VGS=10V, ID=9A, Rds=18m ohm
 VGS=+-25V



+3VALW to +3VS AP4800BGW
 VGS=10V, ID=9A, Rds=18m ohm
 VGS=+-25V



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Issued Date	20130803	Classification Date			
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Rev	20130803		20130803	1	11



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Title	Power sequence Block	
Size	Document Number	Rev
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5

4

3

2

1

D

D

C


C

B

B

A

A

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Virtual symbol	
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				Document Number	Rev 0.2
				Date: Monday, December 23, 2013	Sheet 48 of 59

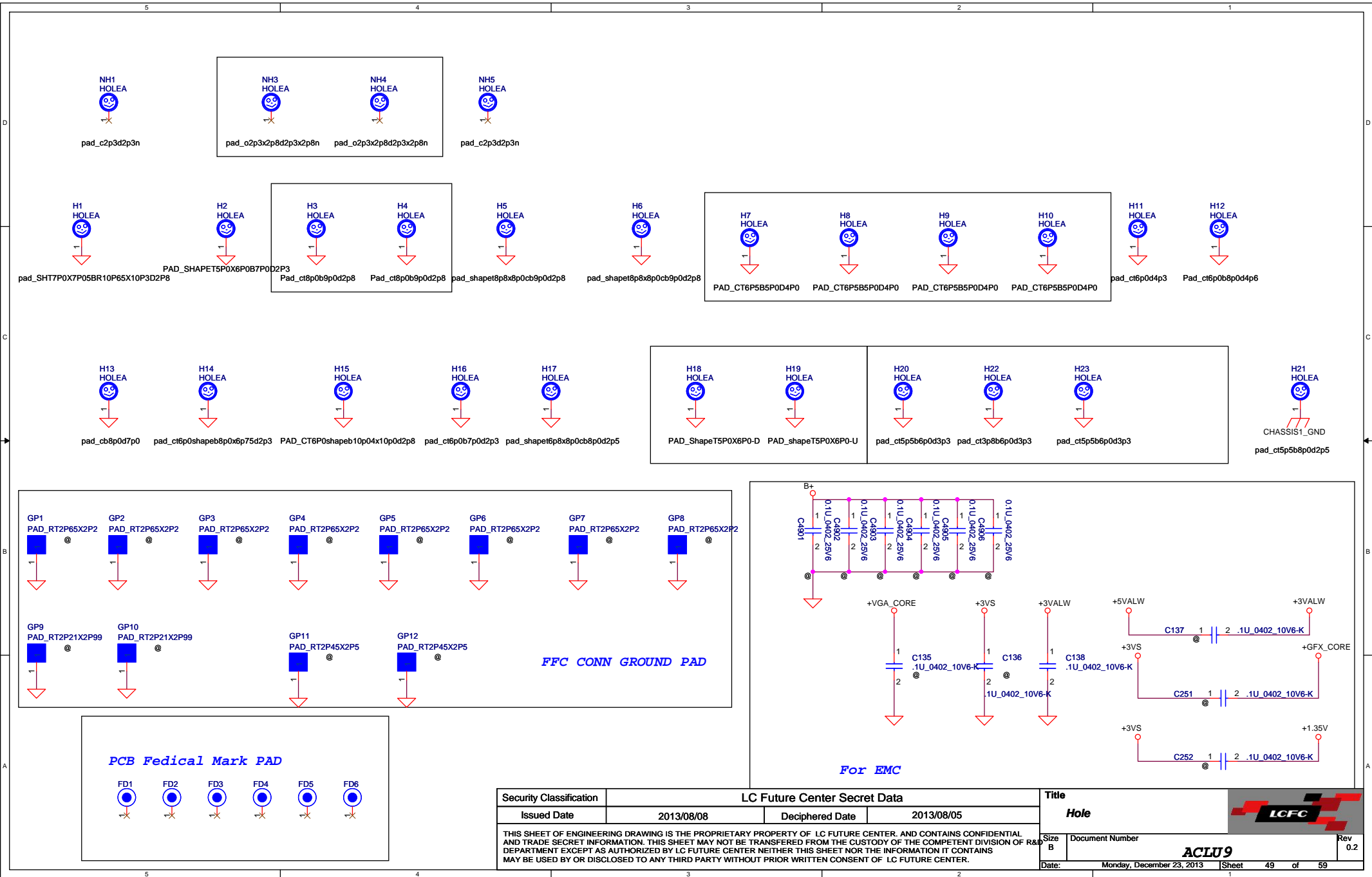
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4

3

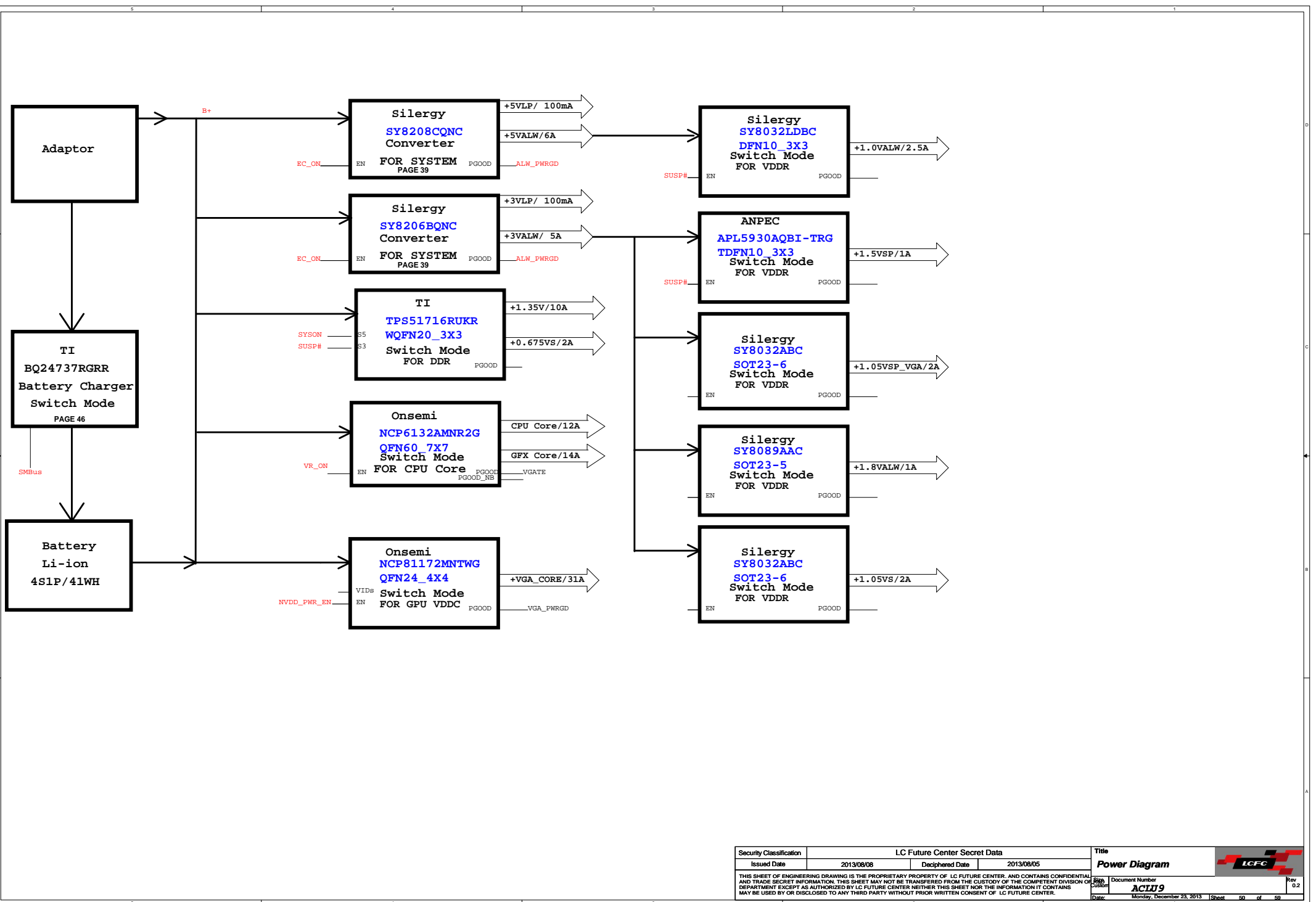
2

1

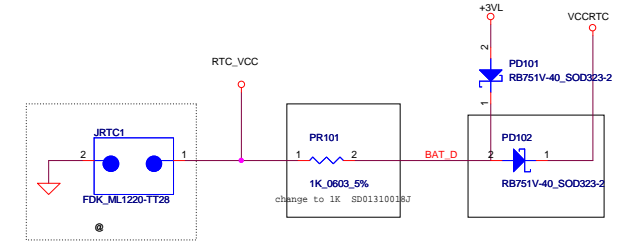
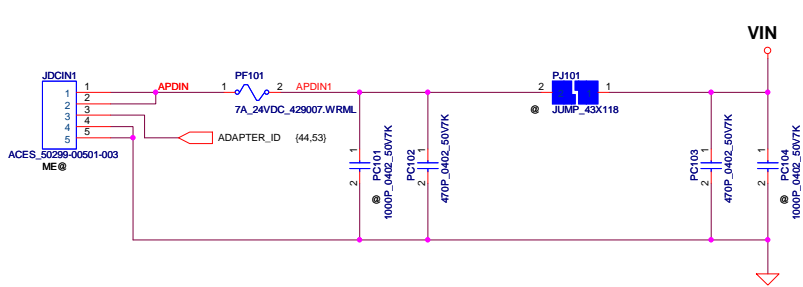


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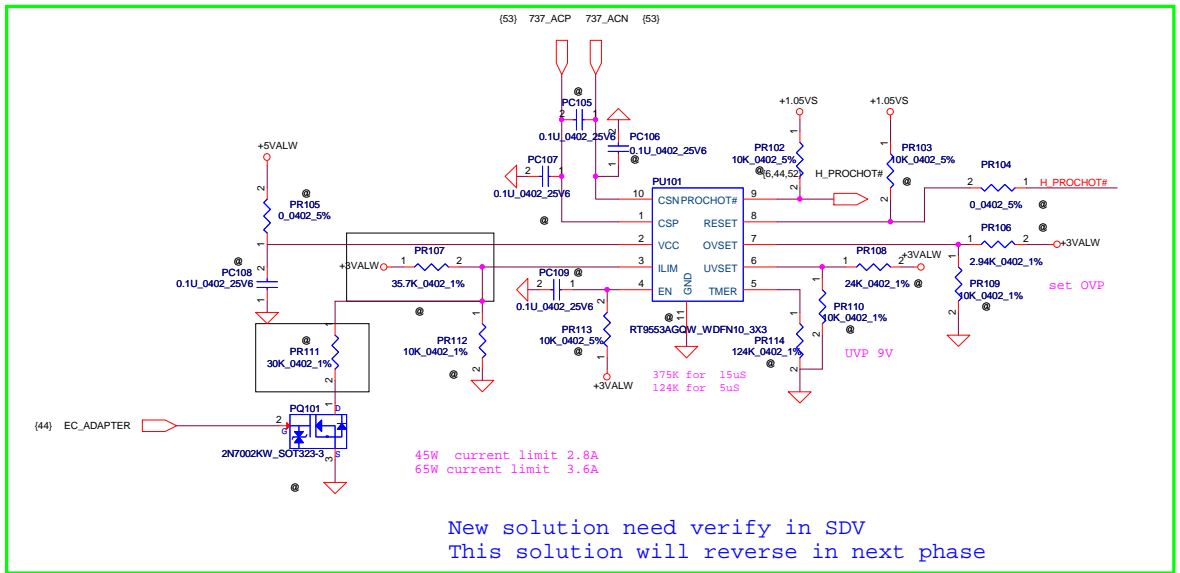
Title		
Hole		
Size	Document Number	ACLU9
B		
Date:	Monday, December 23, 2013	Rev
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	of	59



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RTC_VCC 20MIL
+3VALW 20MIL
VCCRTC 20MIL
BAT_D 20MIL



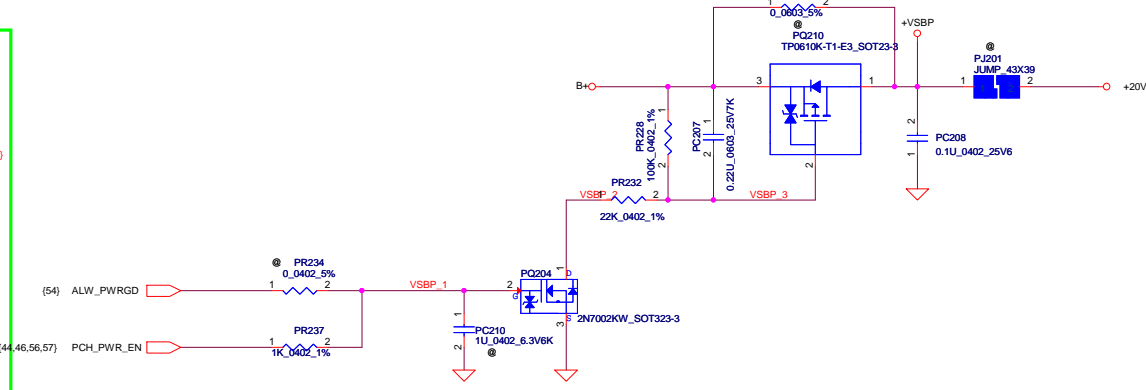
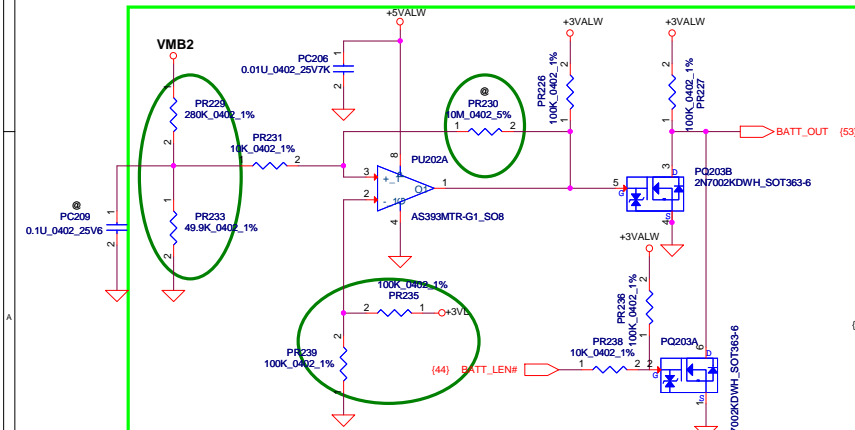
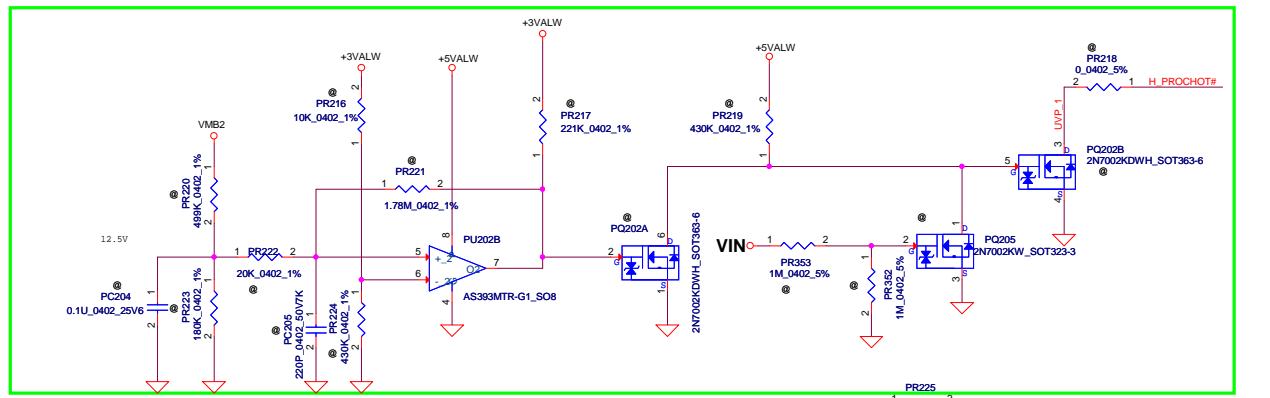
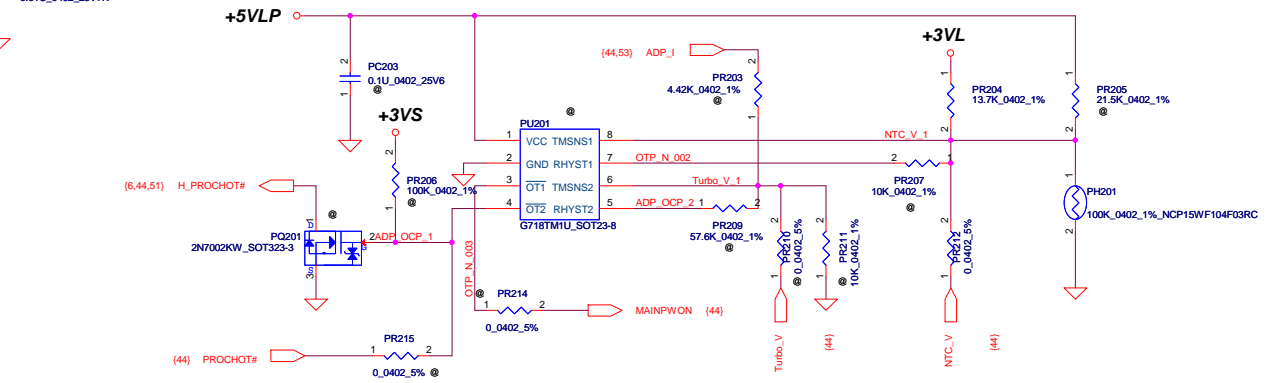
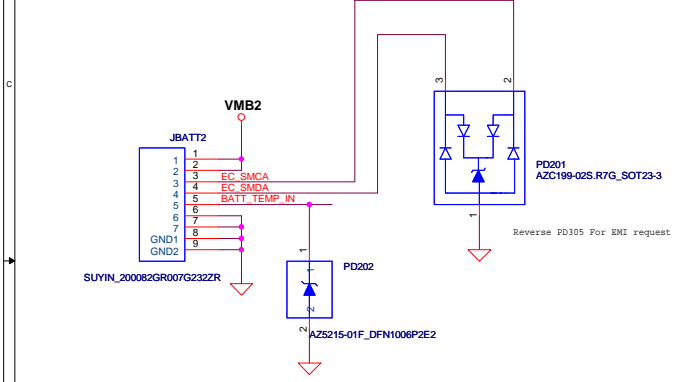
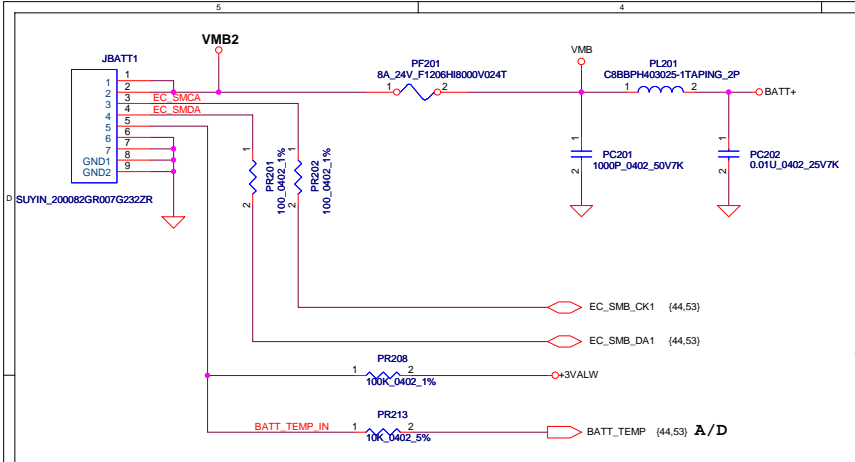
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Title		
DCIN / RTC		
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Custom		
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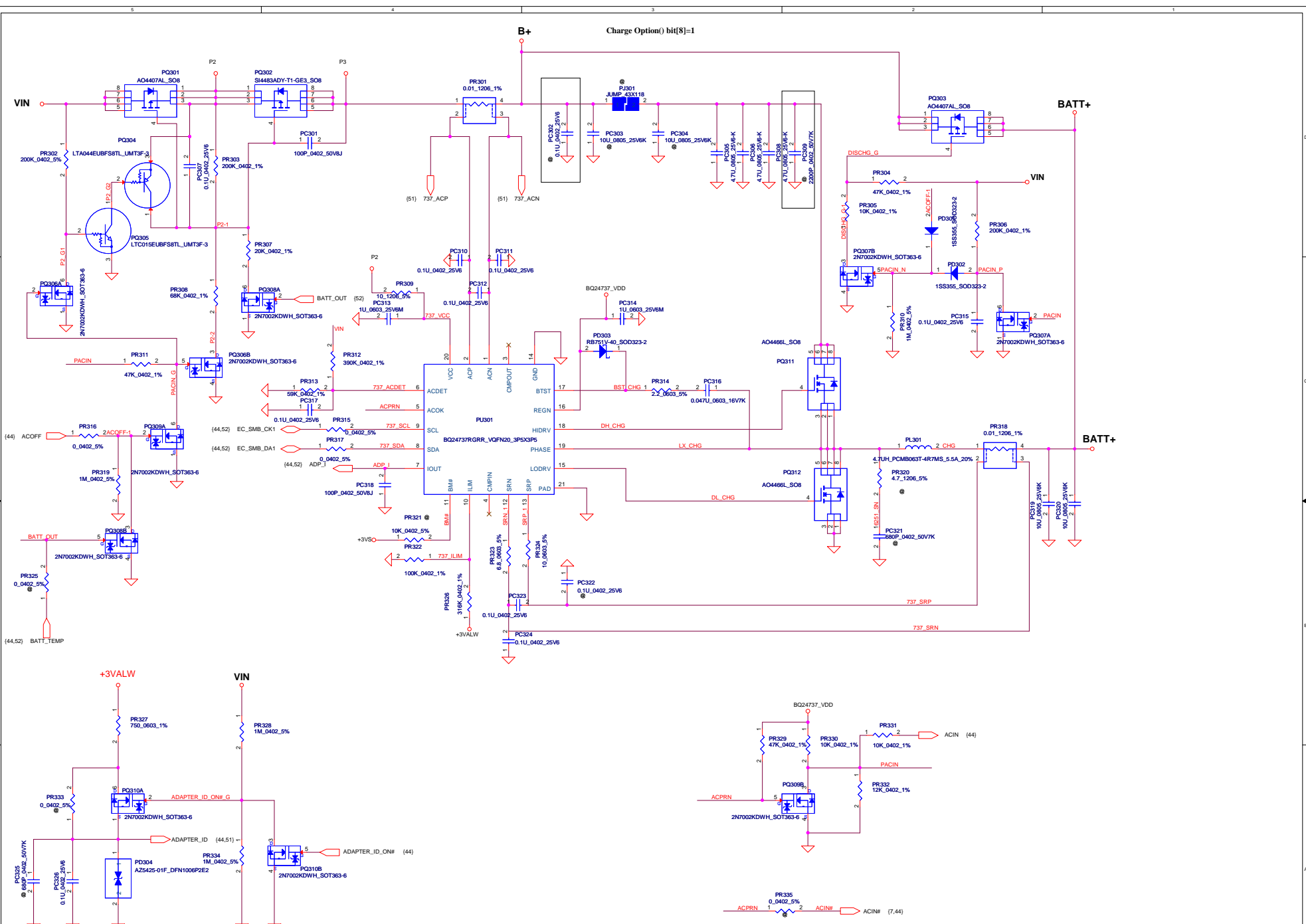
PH201 under CPU bottom side :
 CPU thermal protection at 92+3 degree C
 Recovery at 56 +3 degree C

For KB930 --> Keep PU1 circuit
 (Vth = 0.825V)
 For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
 PH201, PR205, PR211, PQ201, PR208, PR212



Use BATT_TEMP to implement BATT_OUT function,
 New solution need verify in SDV, maybe can reverse in next phase

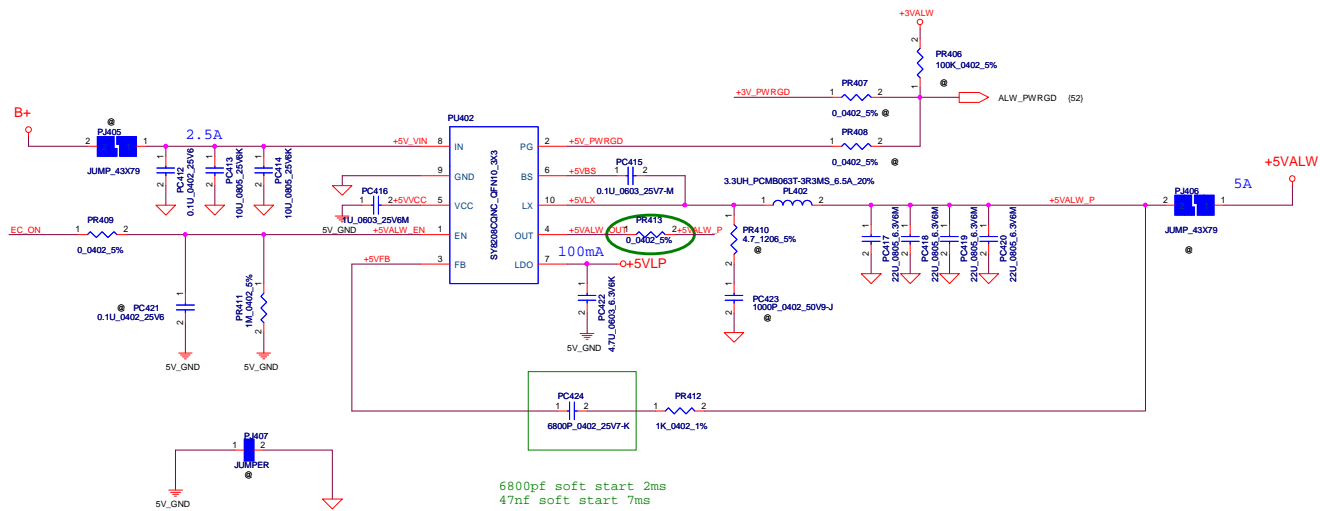
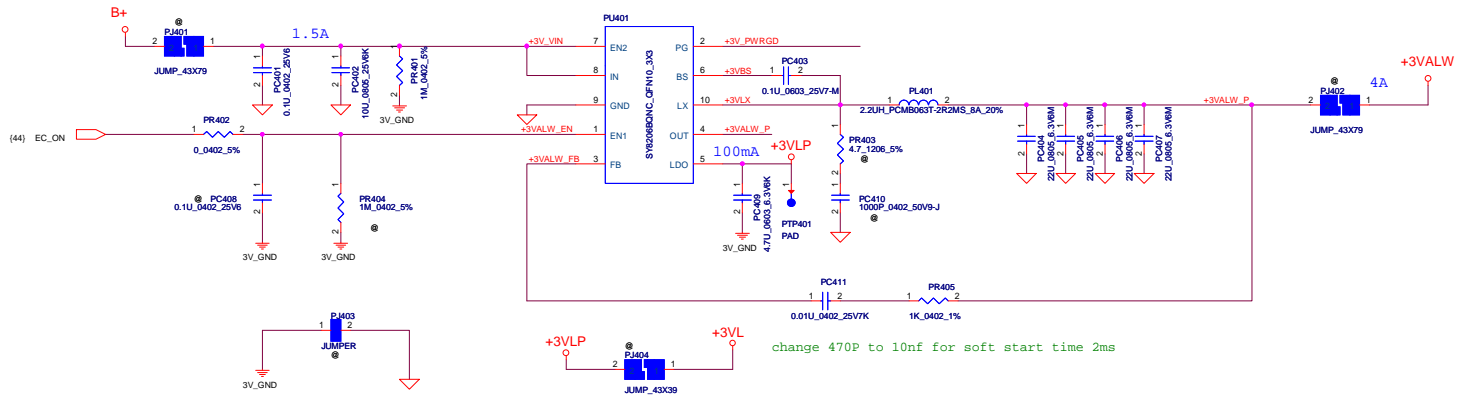
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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Title		CHARGER	
Document Number	AC1109	Rev	0.2
Date	Monday, December 23, 2013	Sheet	53 of 59



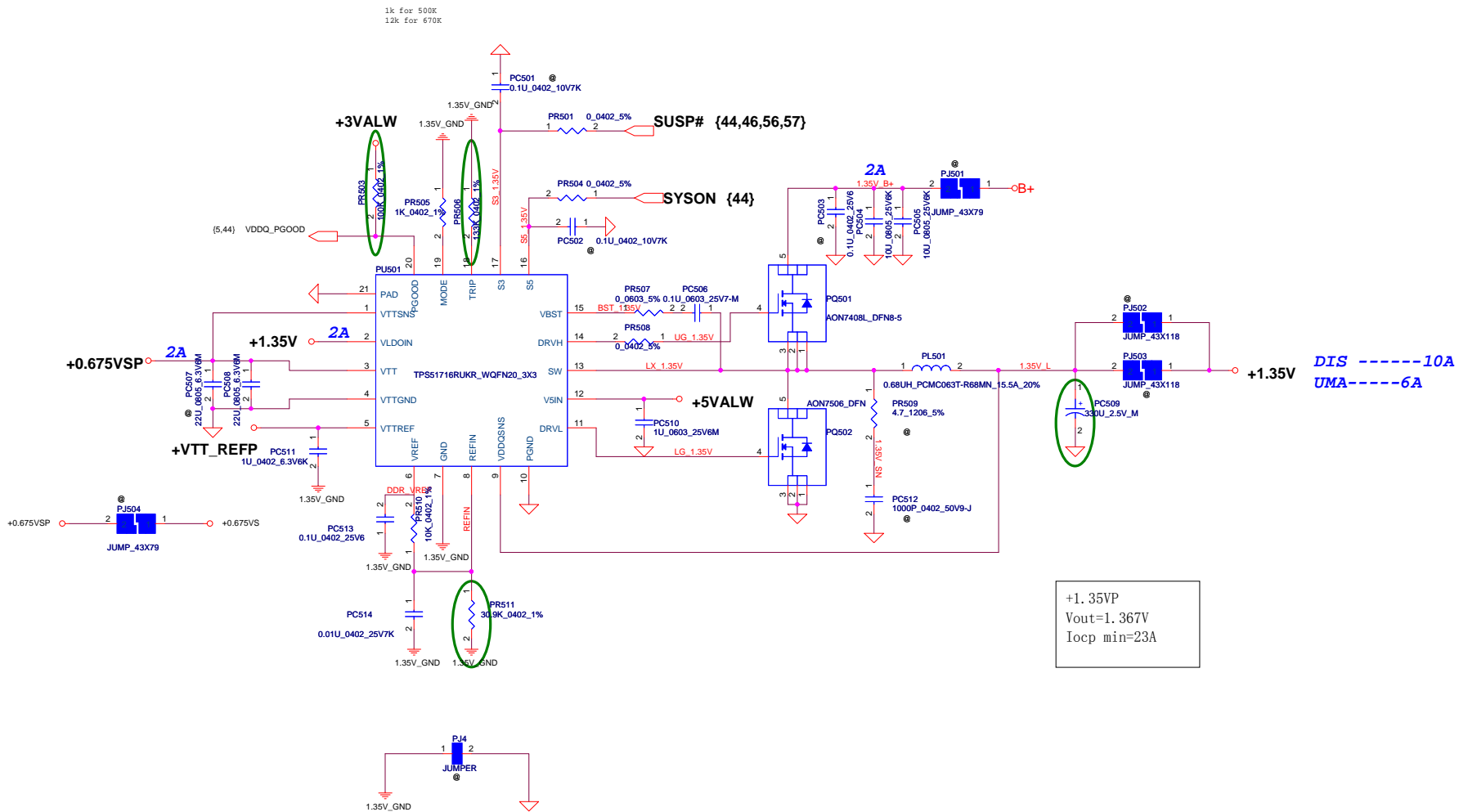



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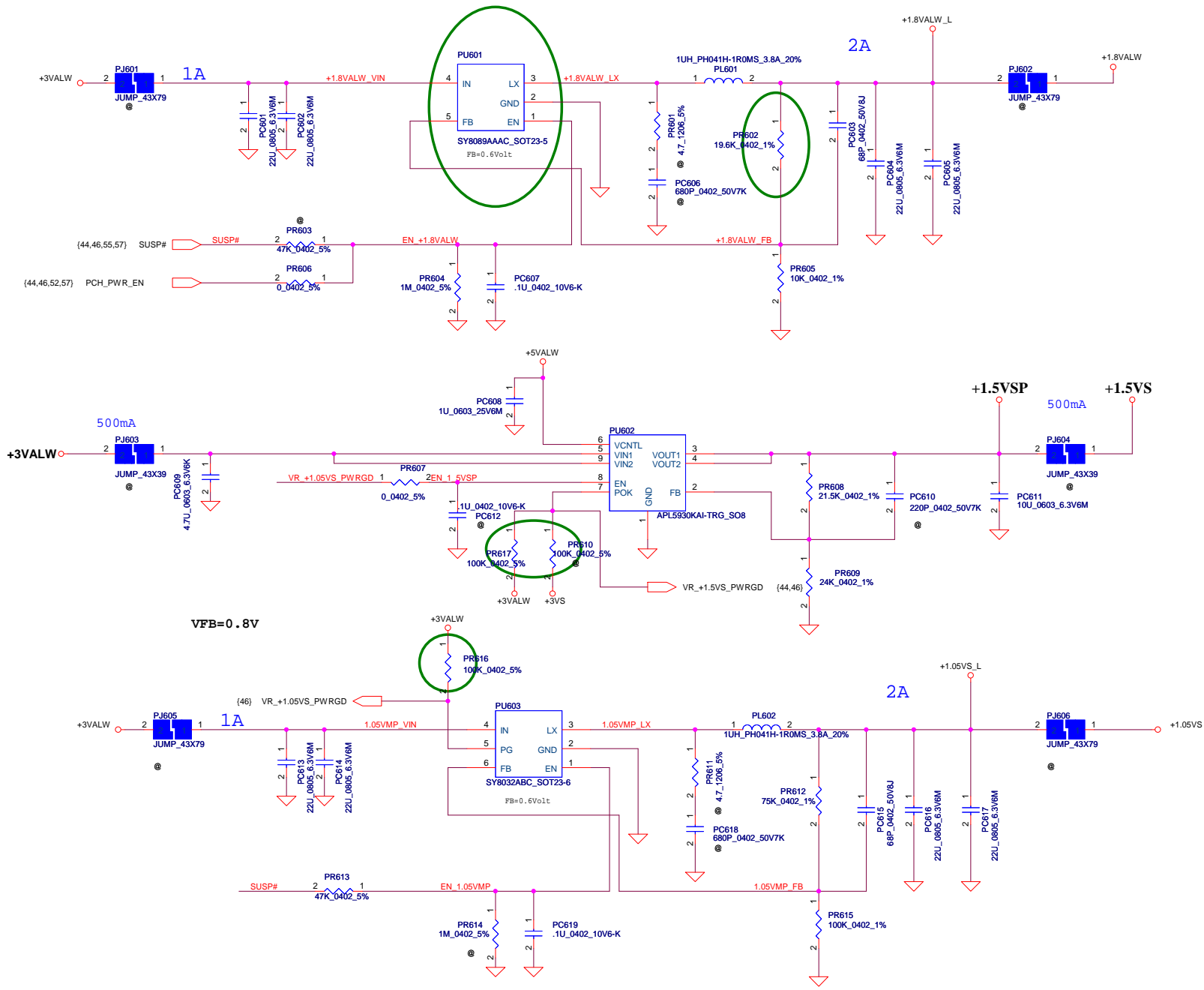
Title	PWR_3VALW/5VALW	
Document Number	ACT109	
Date	Monday, December 23, 2013	Sheet 54 of 59




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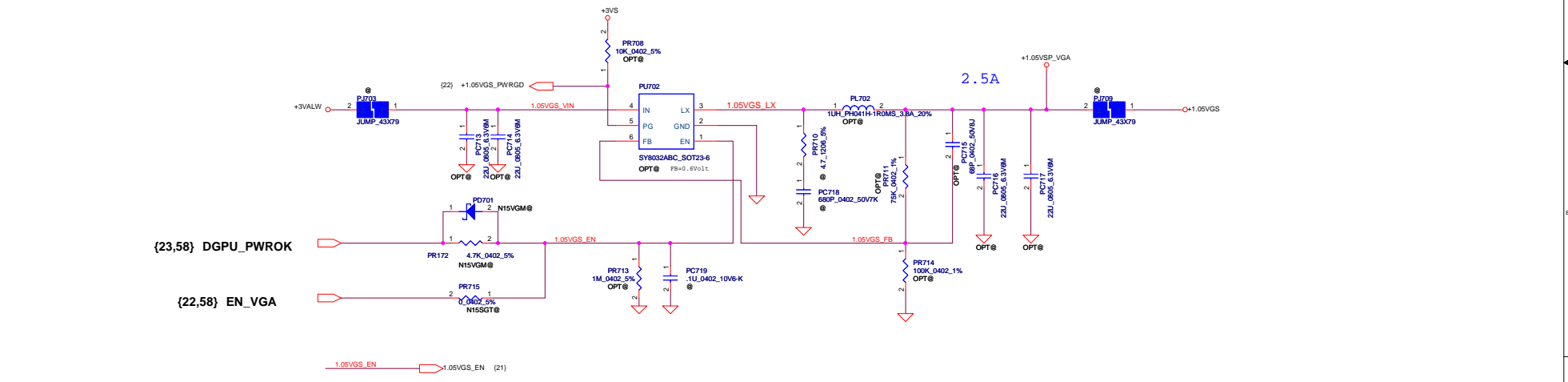
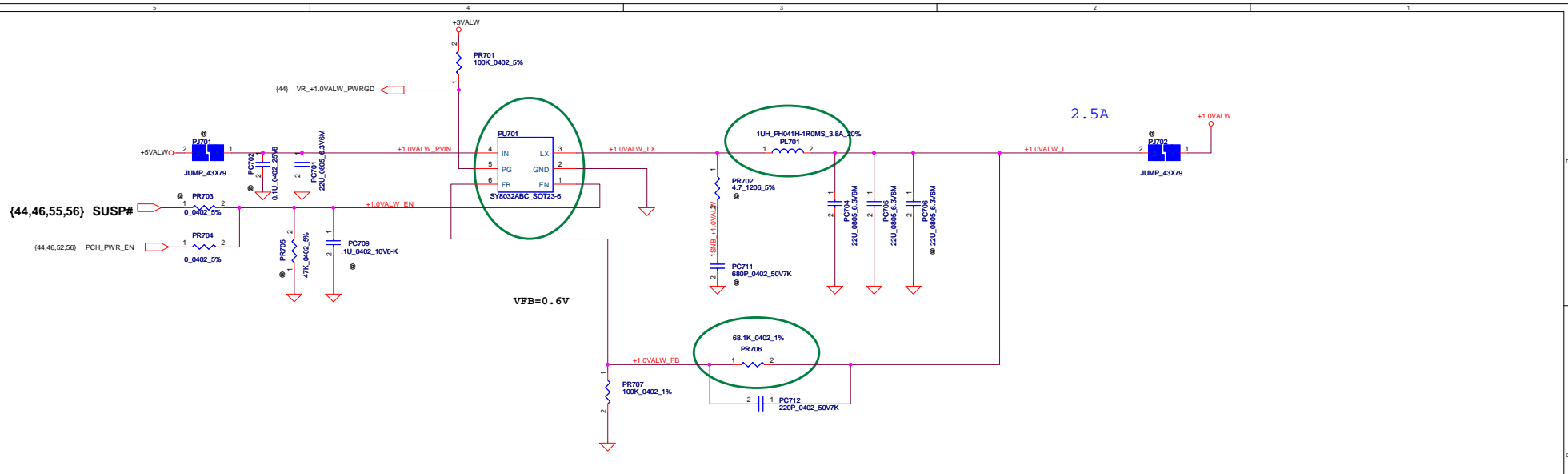



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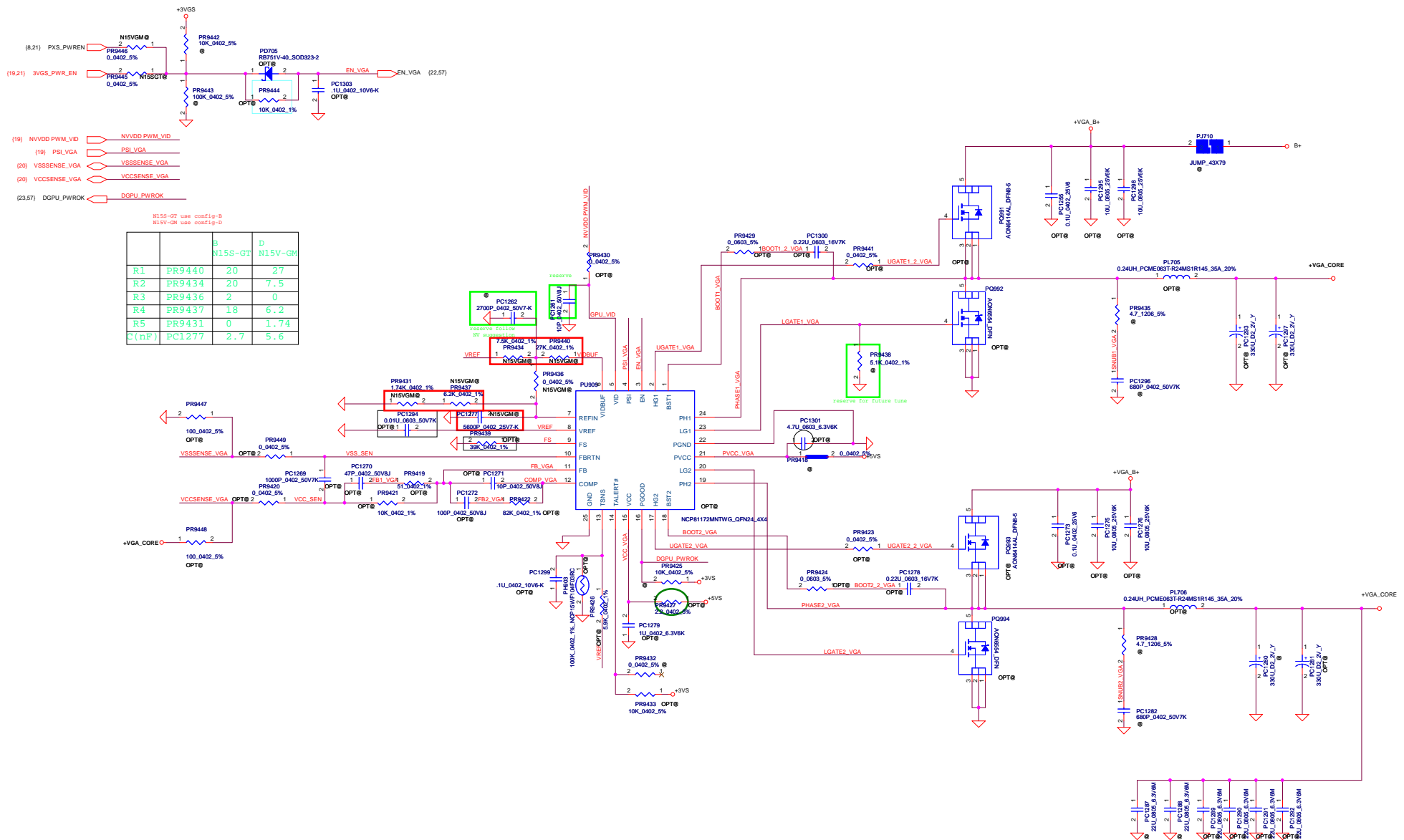


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	B	D
	N15S-GT	N15V-GM
R1	PR9440	20 27
R2	PR9434	20 7.5
R3	PR9436	2 0
R4	PR9437	18 6.2
R5	PR9431	0 1.74
C(nF)	PC1277	2.7 5.6

N15S-GT Use config-B
 N15V-GM Use config-D

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