

2010.04.07 MV Schematic

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 P36 : PWR_Others power plane
 P37 : +VCCNB & 1.5VDDR3 +0_75V
 P38 : ATVDD TPS51217 & +VPCIE
 P39 : Stitch CAP

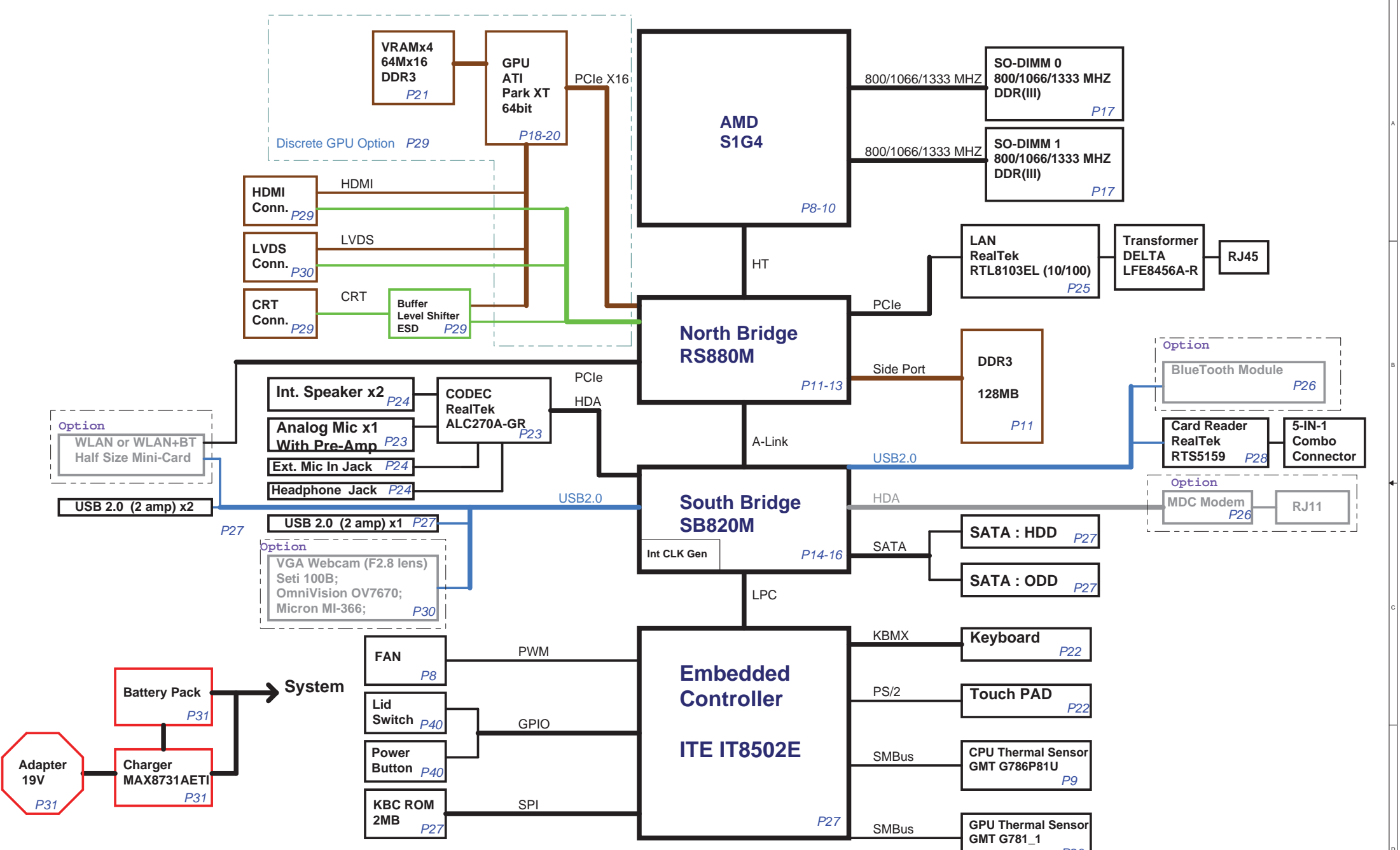
Daughter Board

P40 -- Power Board / USB Board / SW Board

P. Leader	Check by	Design by

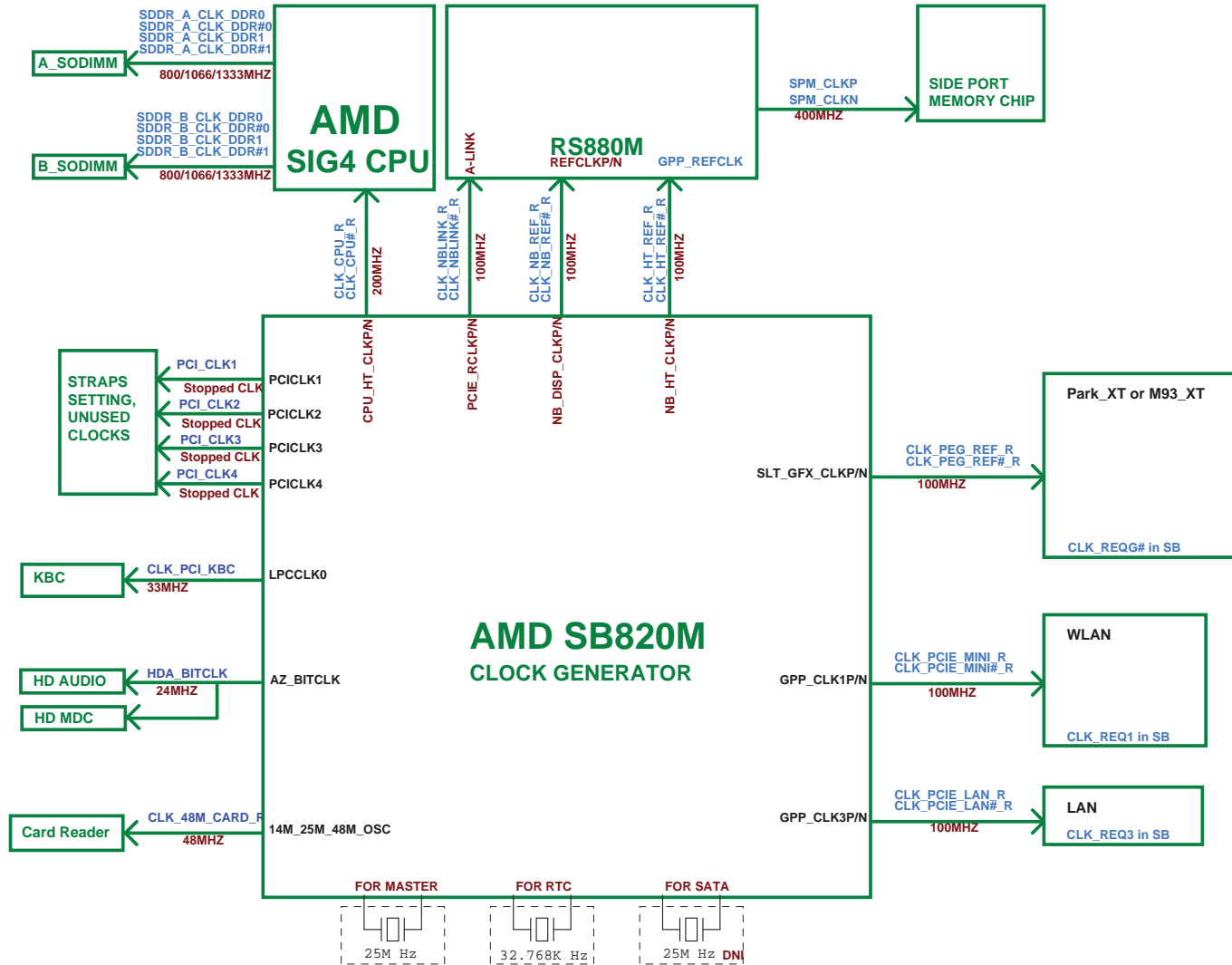
FOXCONN Hon Hai Precision Industry Co. Ltd.
 Foxconn eMS Inc.
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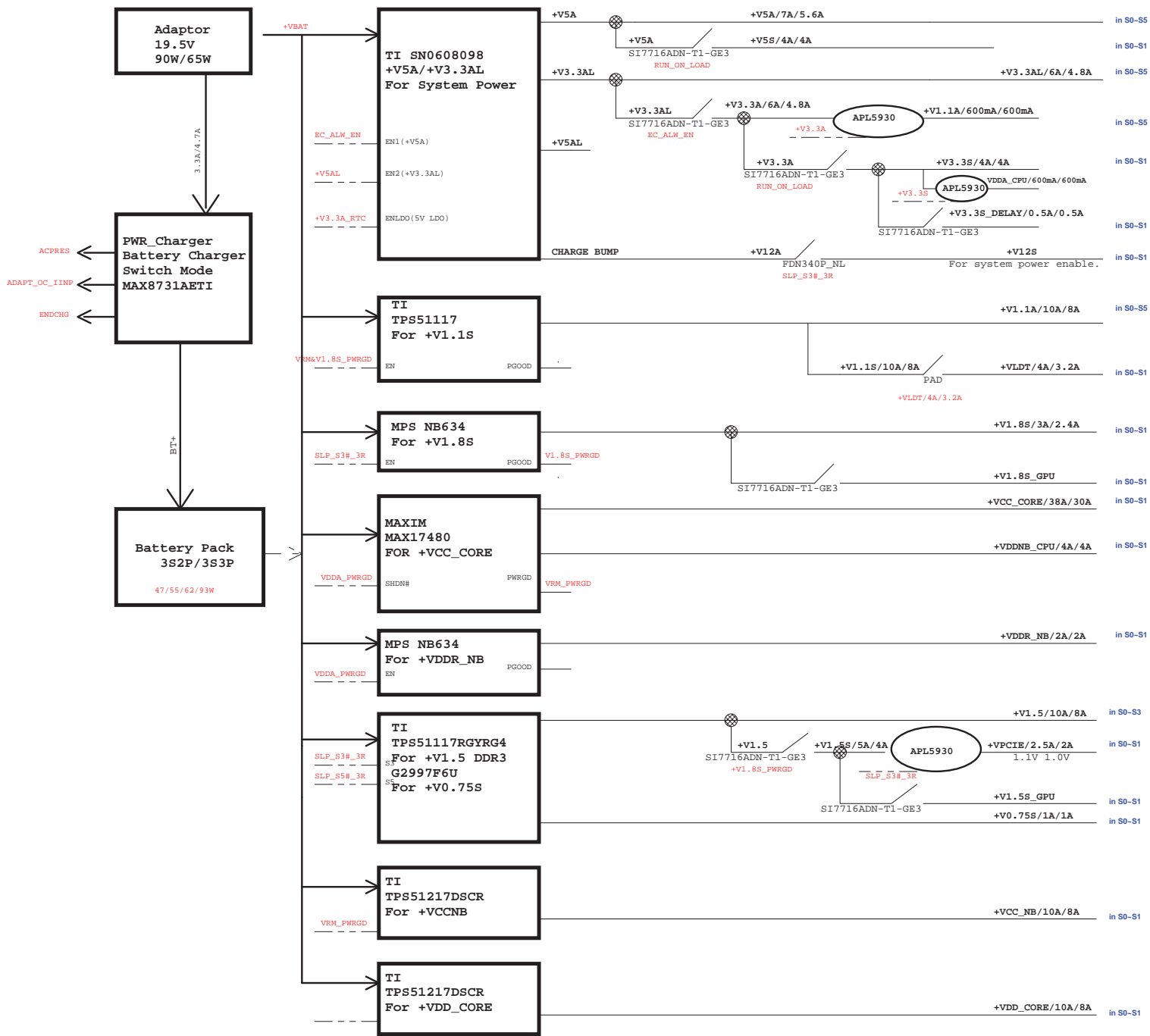
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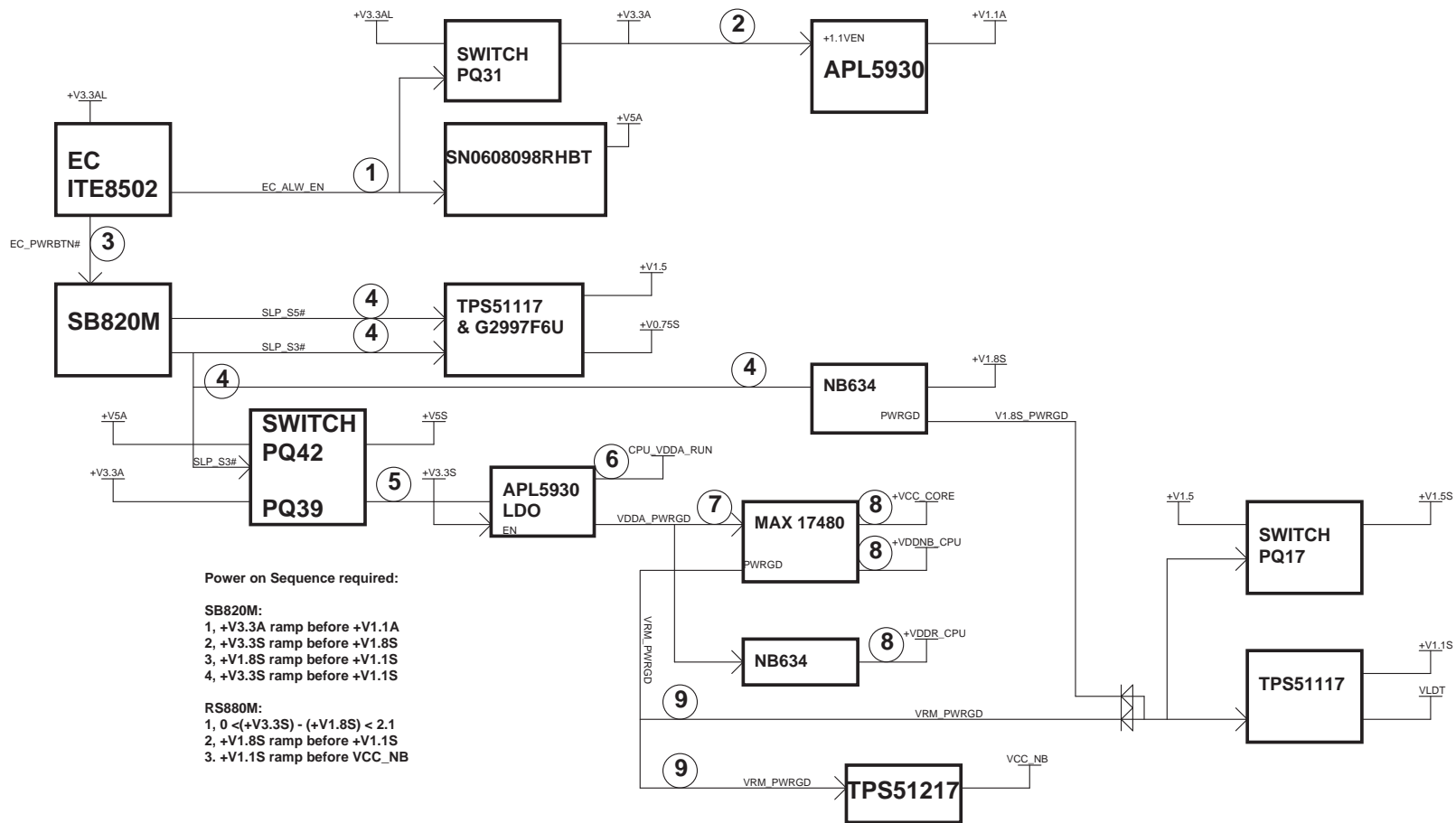
<http://laptop-motherboard-schematic.blogspot.com/>

INTERNAL CLOCK MODE





<http://laptop-motherboard-schematic.blogspot.com/>



Power on Sequence required:

SB820M:

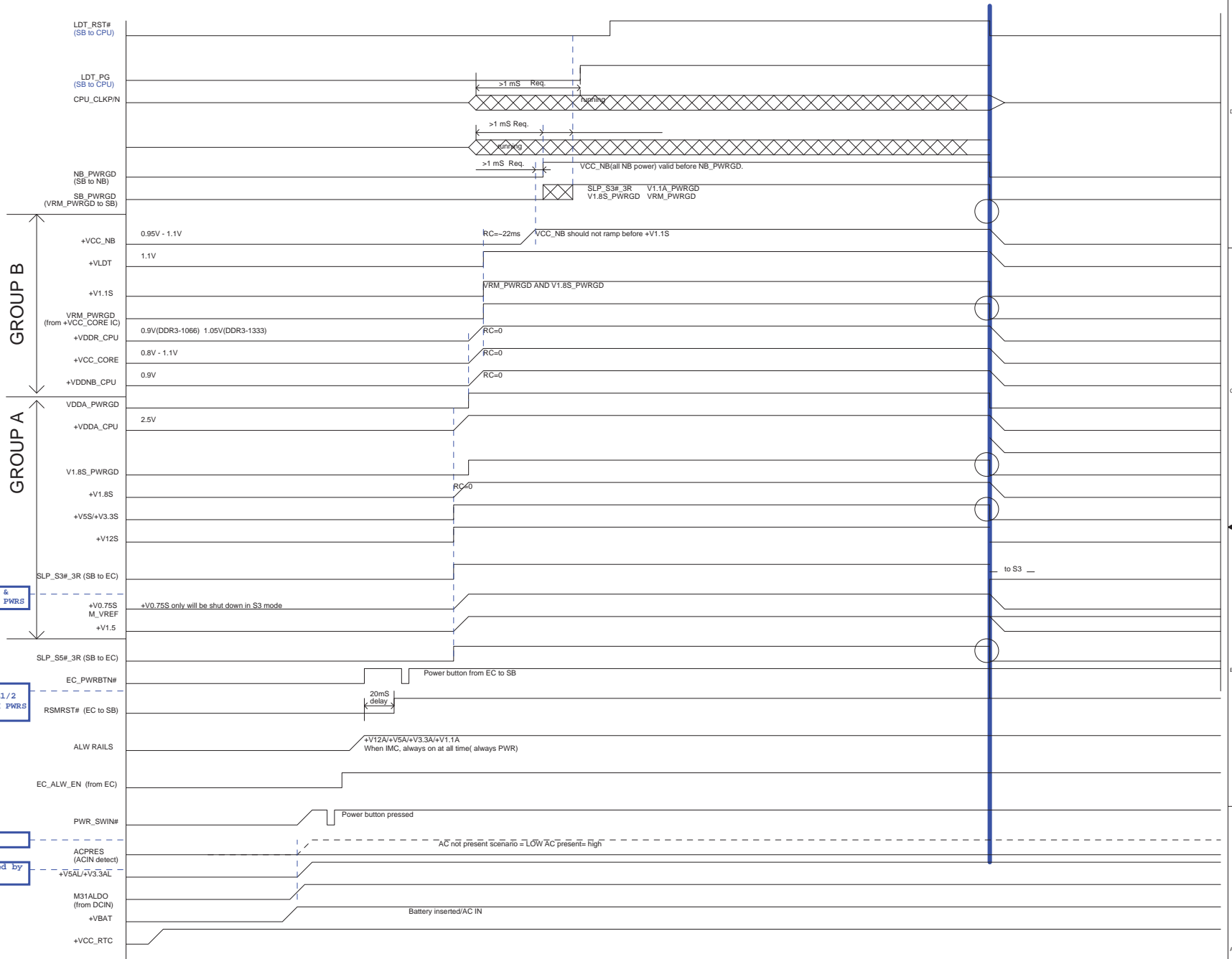
- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 4, +V3.3S ramp before +V1.1S

RS880M:

- 1, $0 < (+V3.3S) - (+V1.8S) < 2.1$
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before VCC_NB

GROUP B

GROUP A



CPU MEM CTL & DDR3 SODIMM PWRS

CPU_THM/SB/SB_SCL1/2 SB_KB/SPI/LPC ROM PWRS

KBC is ready

KBC is powered by +V3.3AL

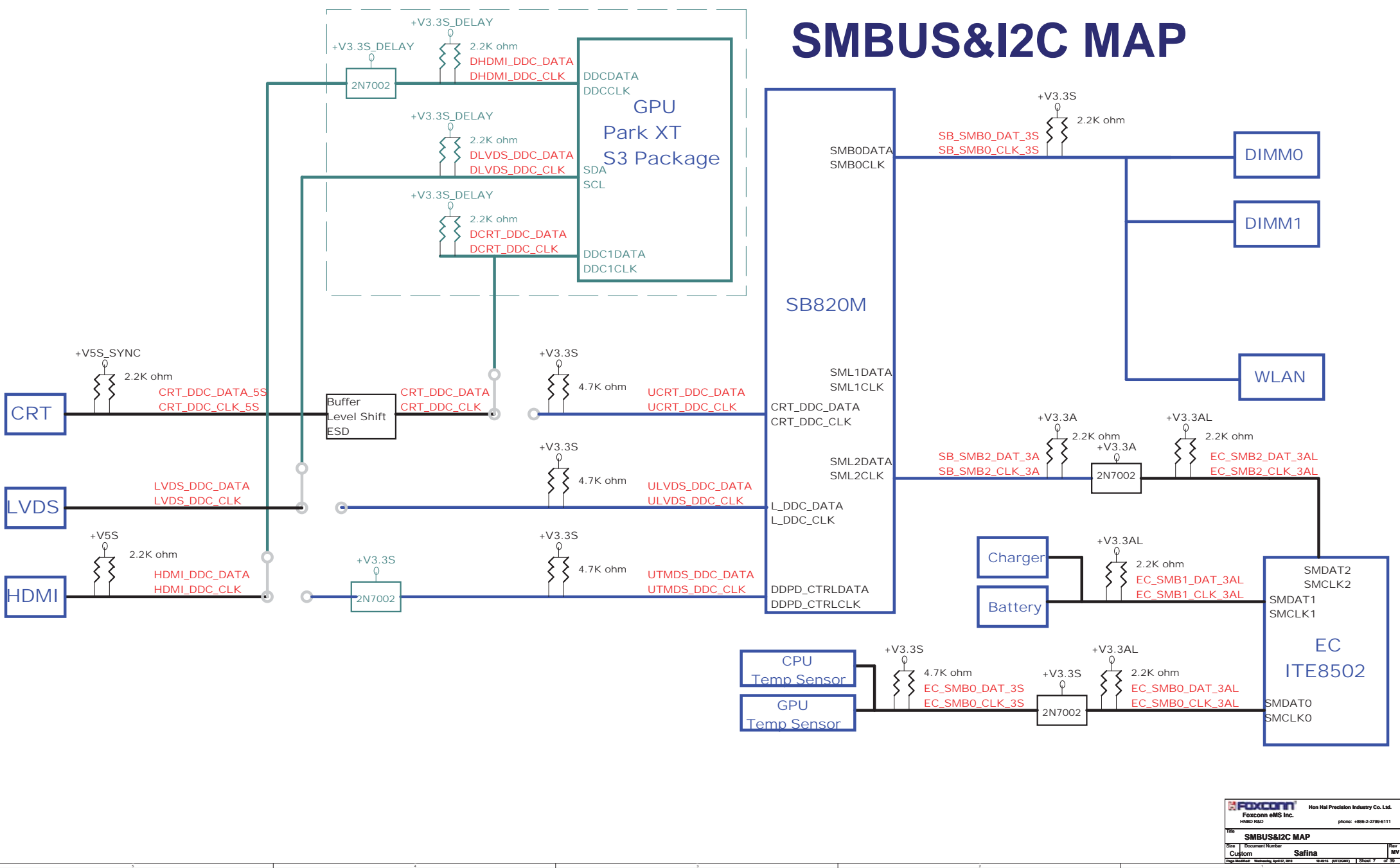
- Power on Sequence required:**
- SB820:
 - 1, +V3.3A ramp before +V1.1A
 - 2, +V3.3S ramp before +V1.8S
 - 3, +V1.8S ramp before +V1.1S
 - 5, +V3.3A ramping down time > 300us
 - 6, 50uS <= All power rails except +V3.3A <= 40mS
 - 7, 100uS <= +V3.3A <= 40mS

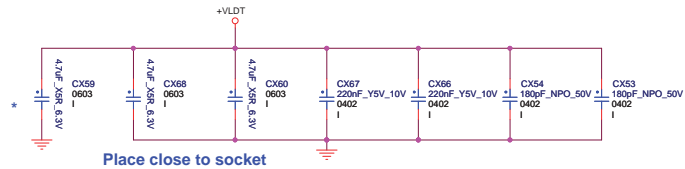
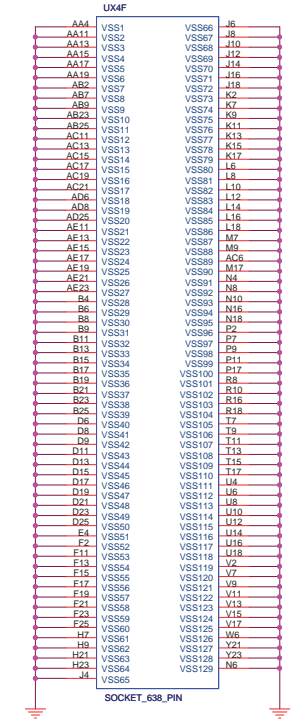
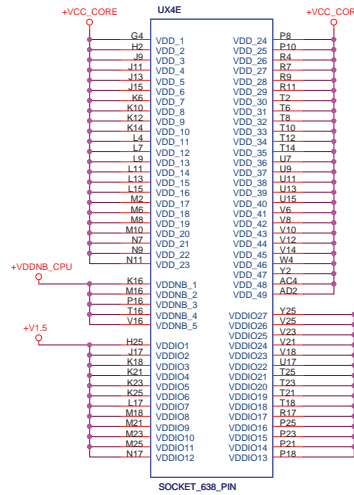
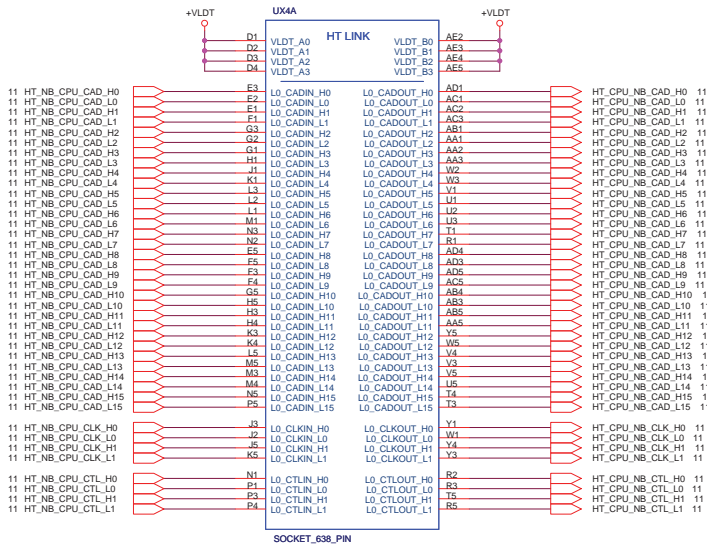
- RS880M:**
- 1, 0 < (+V3.3S) - (+V1.8S) < 2.1
 - 2, +V1.8S ramp before +V1.1S
 - 3, +V1.1S ramp before +VCC_NB

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		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNSD R&D	
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Title: POWER SEQUENCY TIMING			
Size:	Document Number:	Rev:	MV
Custom:	Safina		
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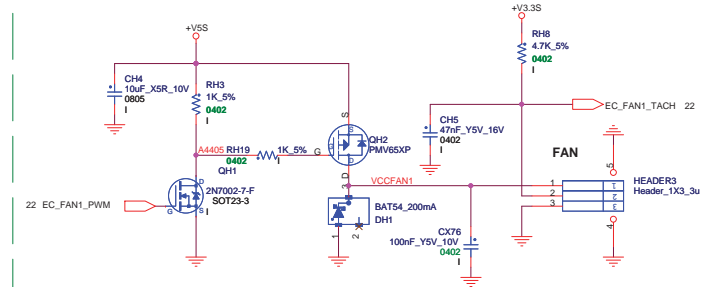
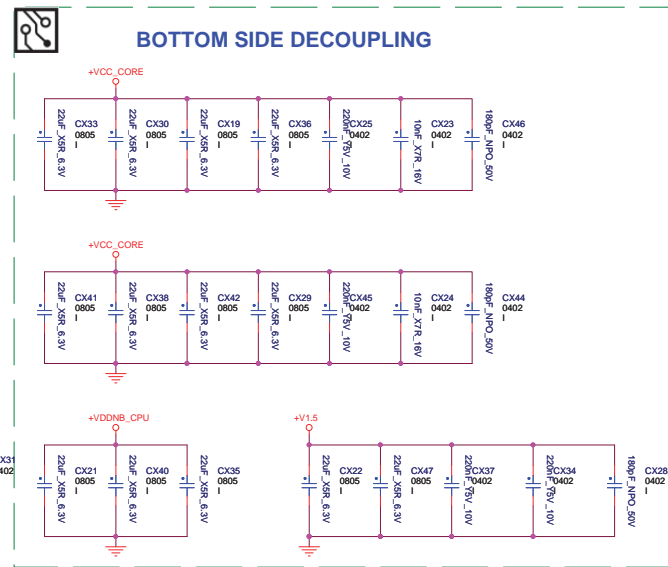
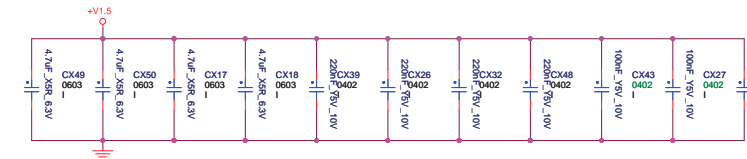
SMBUS&I2C MAP





* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side

DECOUPLING BETWEEN PROCESSOR AND DIMMS
PLACE CLOSE TO PROCESSOR AS POSSIBLE

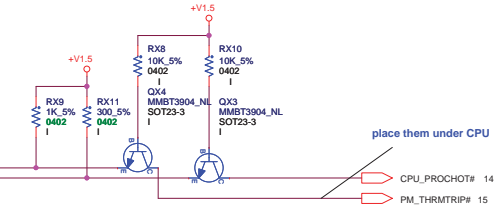
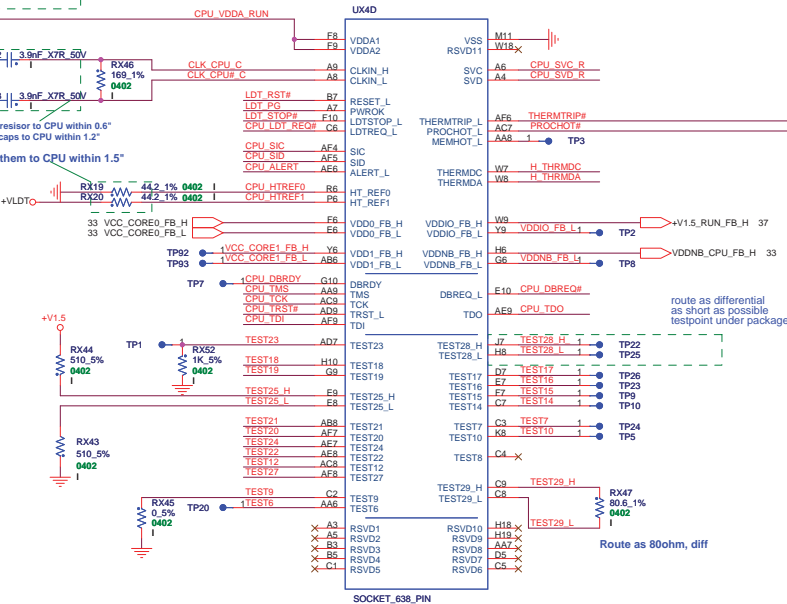
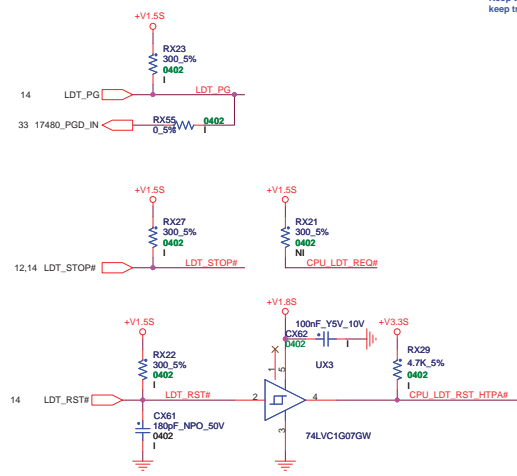
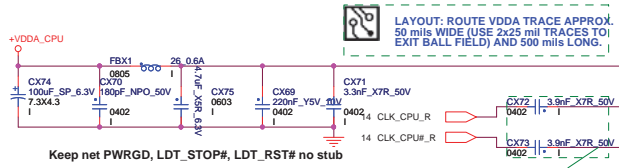


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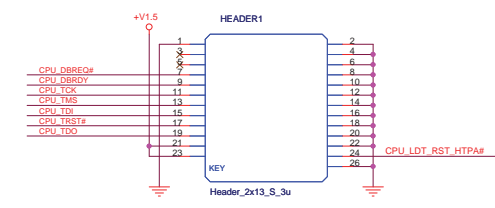
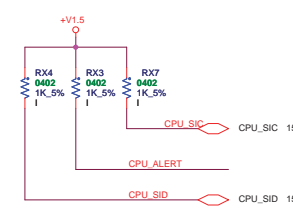
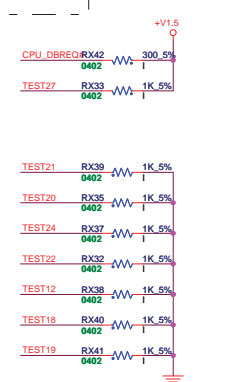
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Size: Document Number
Custom Safina Rev: MV

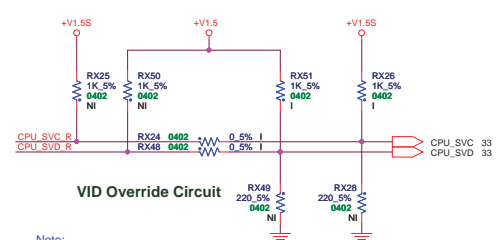
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Thermdc and Thermo should be routed away to VRM, crystal, etc. Customer should follow the MBDG. However, Guam is using TSI so this does not applies to Guam.



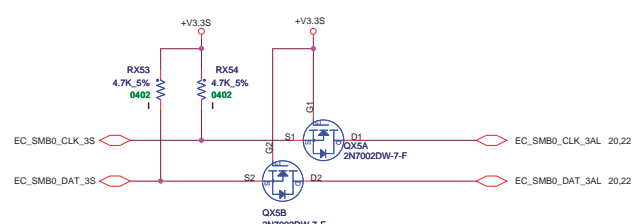
HDT Connector



Note:
To override VID, Remove RX24, RX48 set VID

SVC		SVD		BOOT VOLTAGE(VDD)	
		(CPU)RST_PRCFG	(CPU)RST_PRCFG	(CPU)VRM_PRCFG	(CPU)VRM_PRCFG
		=+VCC(GND)	=OPEN	=+VCC(GND)	=OPEN
0	0	1.1	1.1		
0	1	1.0	1.2		
1	0	0.9	1.0		
1	1	0.8	0.8		

VID OVERRIDE TABLE (VDD)



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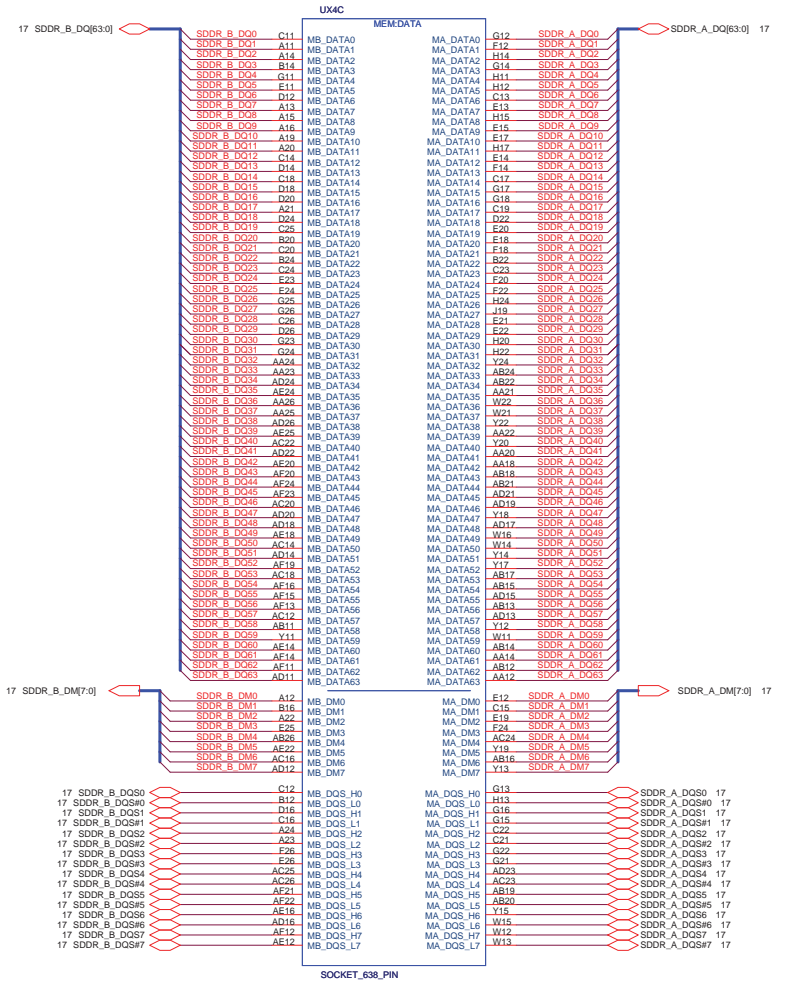
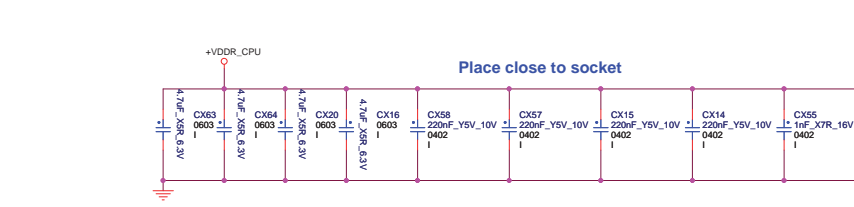
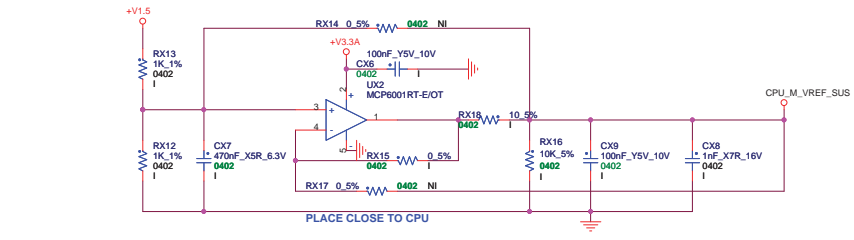
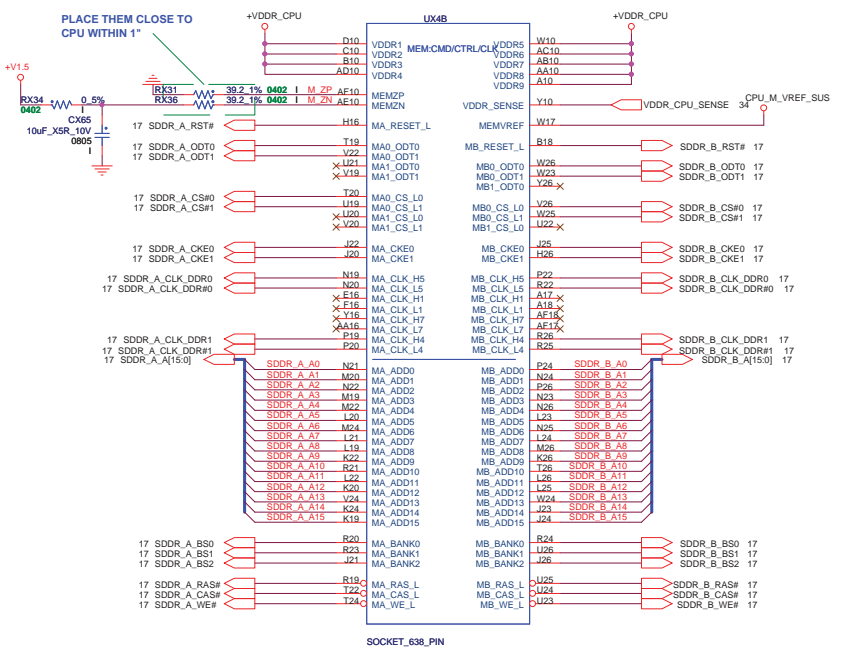
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Title: **S1G4 CTRL & DEBUG**

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Processor Memory Interface

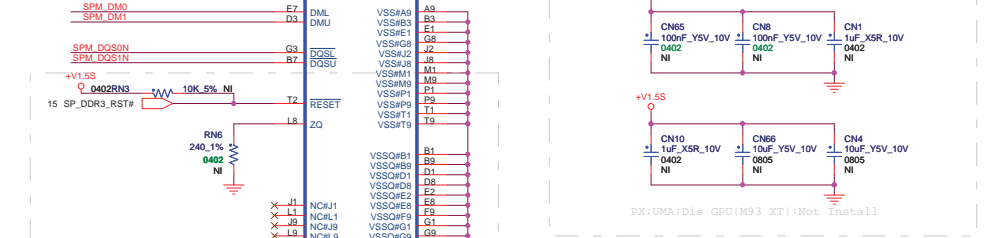
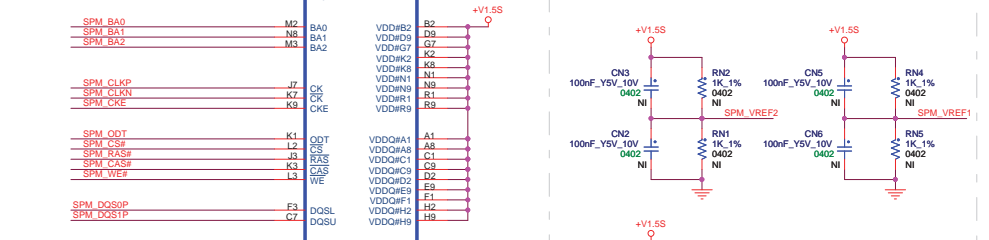
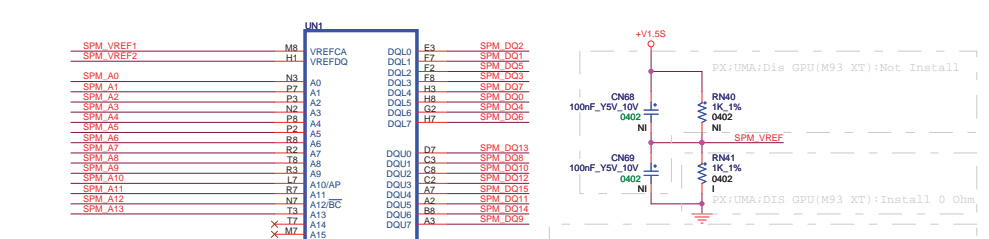
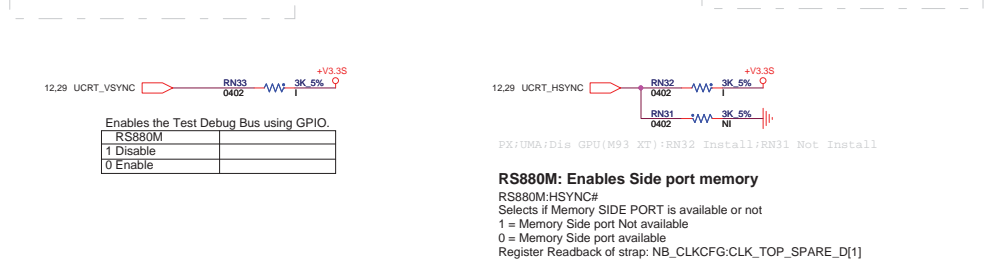
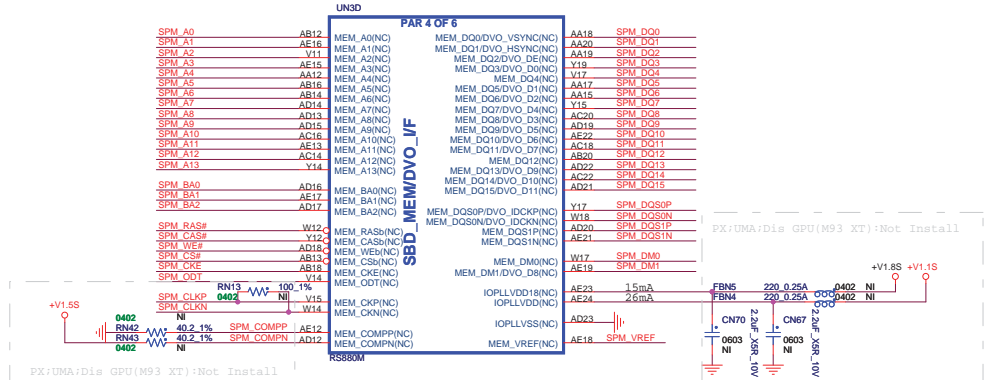
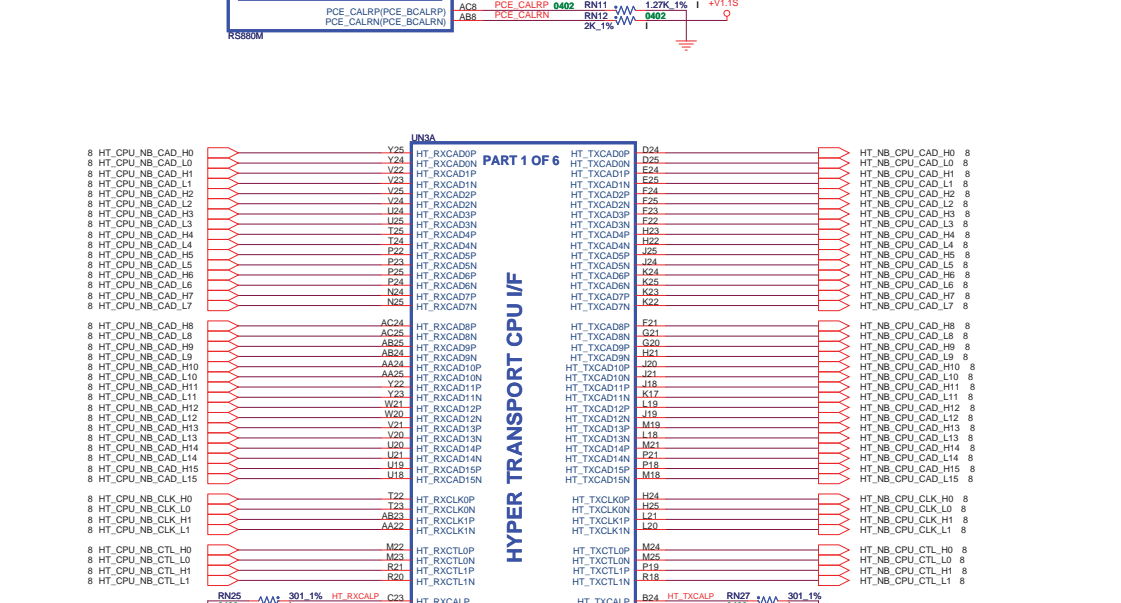
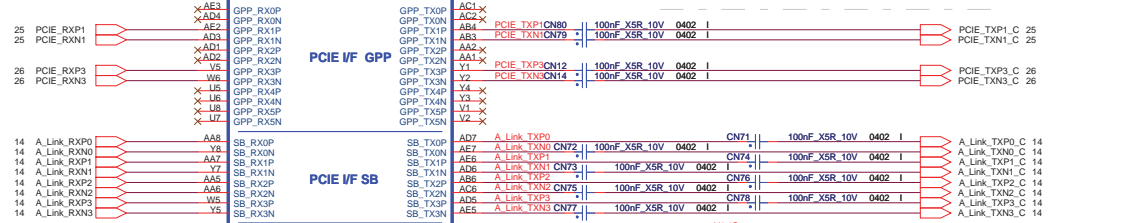
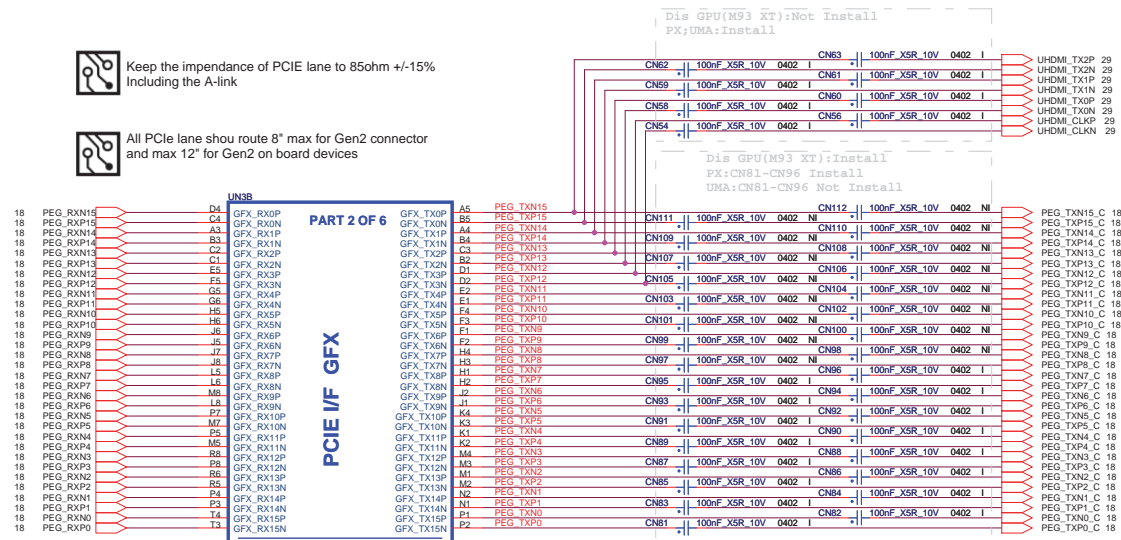




Keep the impedance of PCIe lane to 85ohm +/-15% including the A-link



All PCIe lane should route 8" max for Gen2 connector and max 12" for Gen2 on board devices



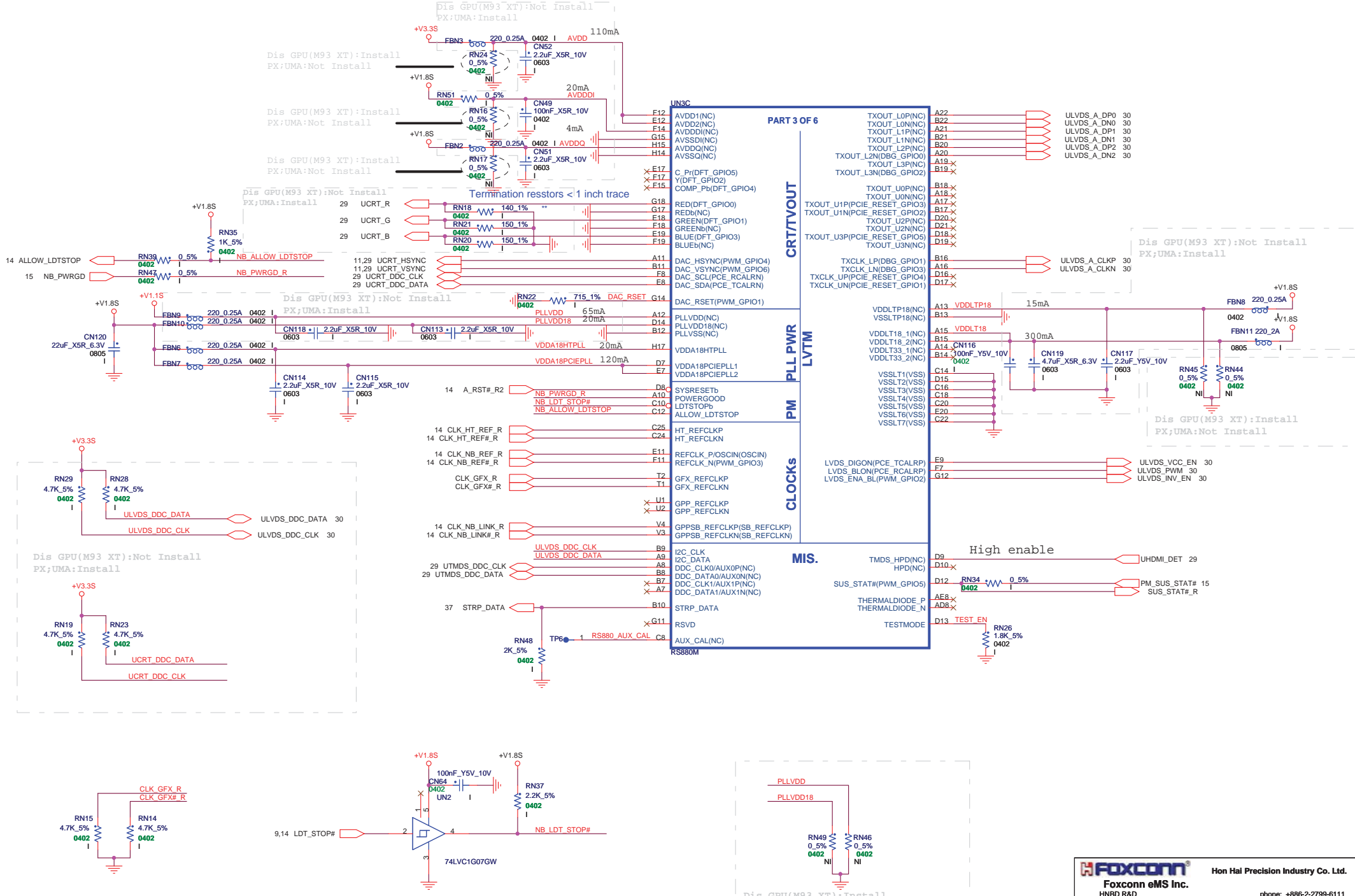
RS880M: Enables Side port memory
RS880M:HSYNC#
Selects if Memory Side PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

Enables the Test Debug Bus using GPIO.
RS880M
1 Disable
0 Enable

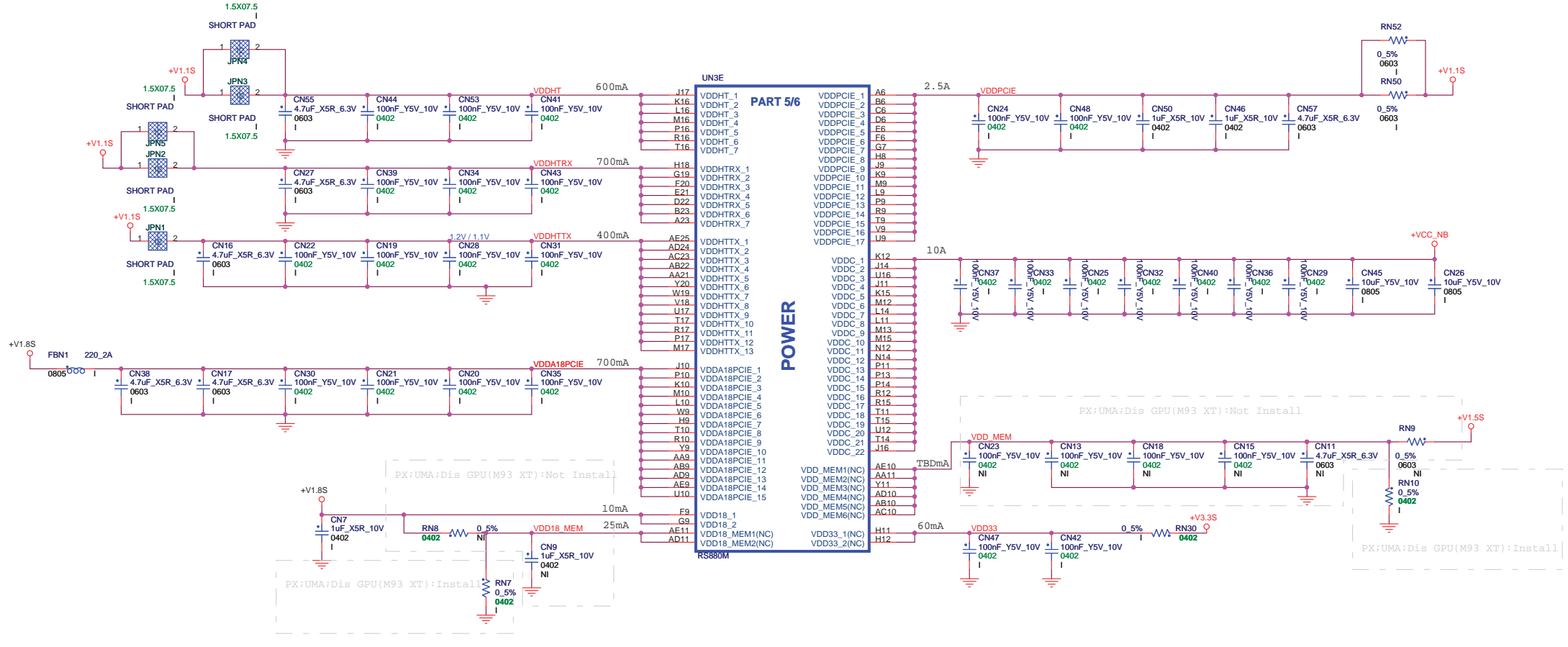
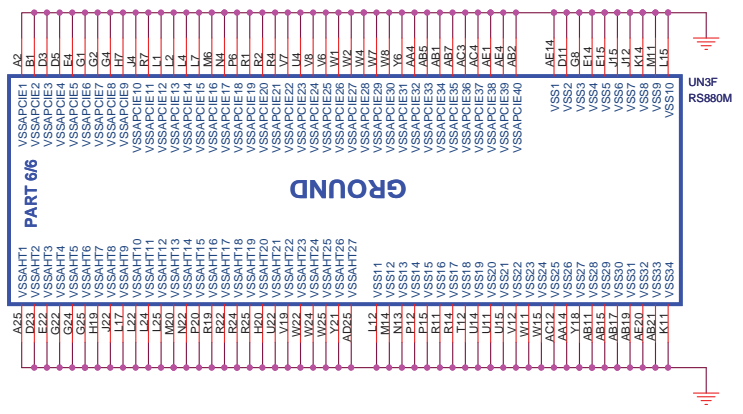
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RS880M-PCIE/HT LINK/SPMEM

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Custom Safina
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Title			
RS880M-SYSTEM I/F			
Size	Document Number		Rev
Custom	Safina		MV
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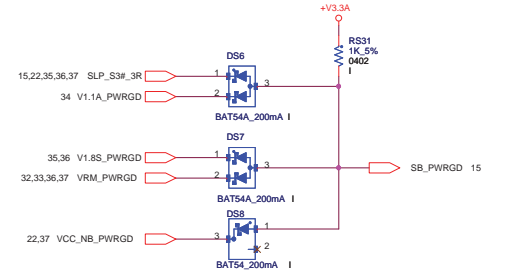
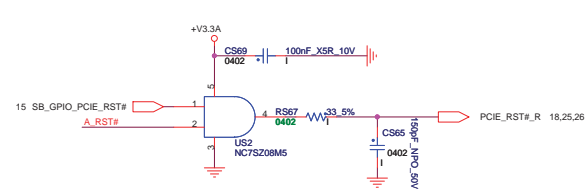
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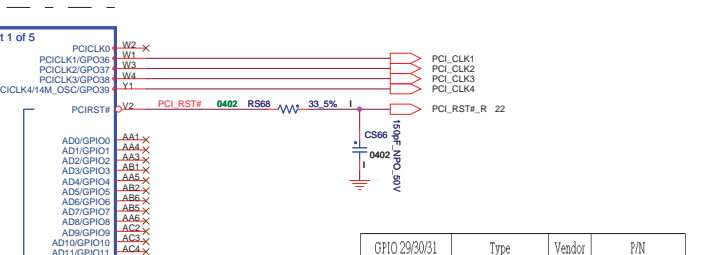
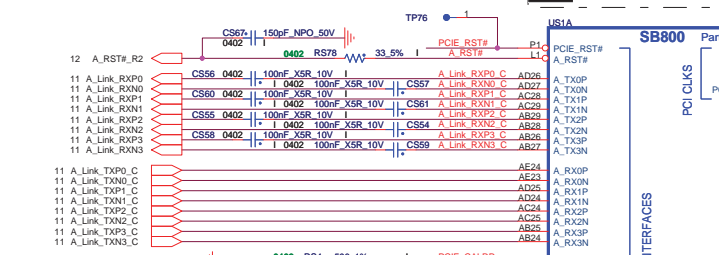
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Size: Custom Document Number: Safina Rev: MV

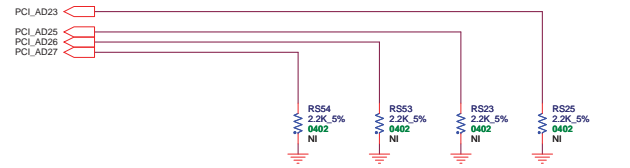
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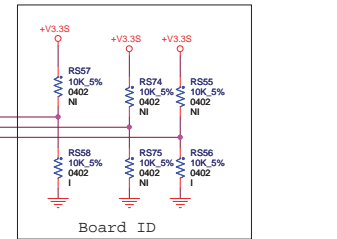
PLACE THESE PCIe AC COUPLING CAPS CLOSE TO US1



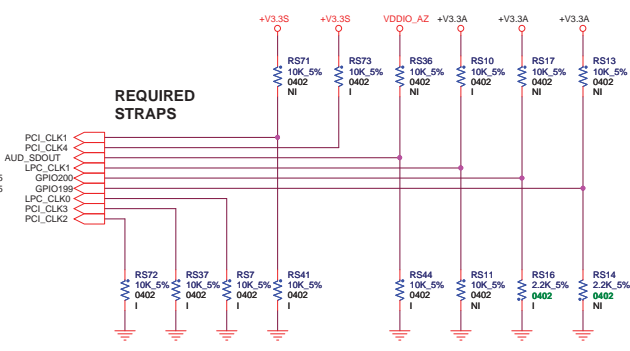
DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE PCI MEM BOOT

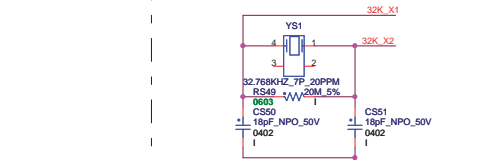


REQUIRED STRAPS



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIe Gen2	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE	FORCE PCIe Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	L,L = LPC ROM (Default) L,L = FWH ROM	

PLACE THESE COMPONENTS CLOSE TO US1, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2



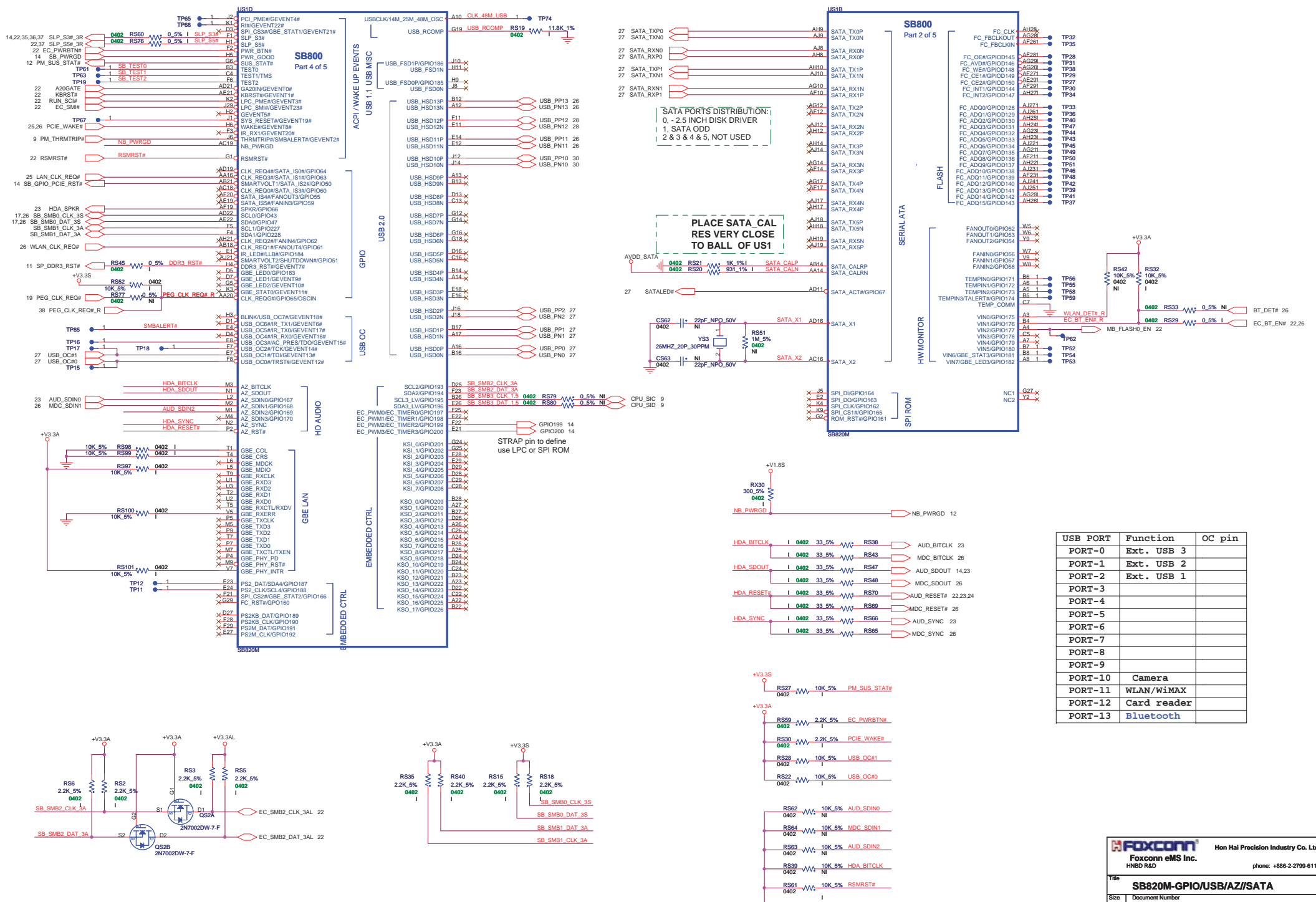
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Title: **SB820M-PCIe/CPU/LPC/STRAP**

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Custom **Safina** Rev: MW

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SATA PORTS DISTRIBUTION:
 0 - 2.5 INCH DISK DRIVER
 1, SATA_ODD
 2 & 3 & 4 & 5, NOT USED

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U51

STRAP pin to define use LPC or SPI ROM

PORT	Function	OC pin
PORT-0	Ext. USB 3	
PORT-1	Ext. USB 2	
PORT-2	Ext. USB 1	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8		
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/WiMAX	
PORT-12	Card reader	
PORT-13	Bluetooth	

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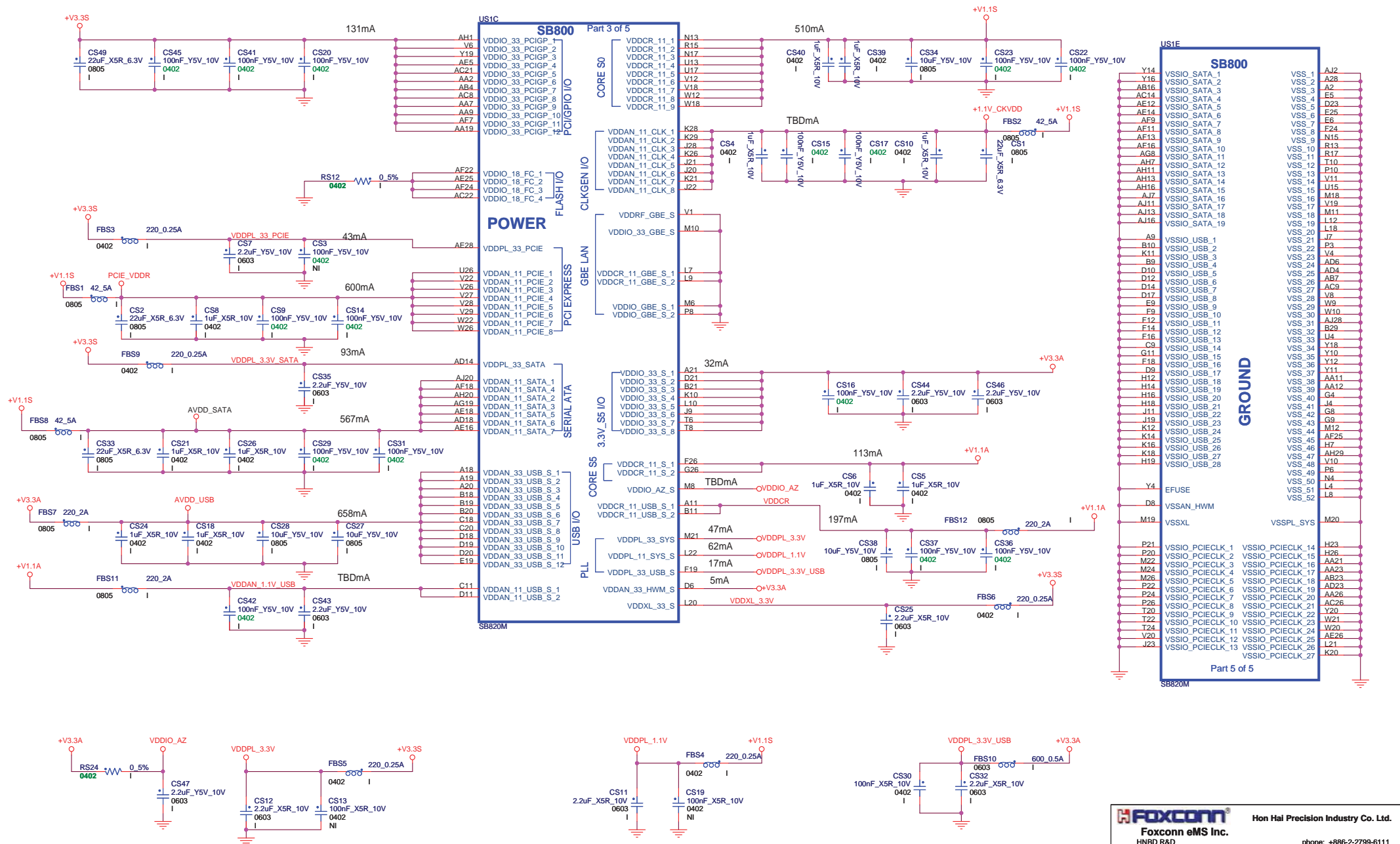
Title: **SB820M-GPIO/USB/AZ/SATA**

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Custom	Safina	MV

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PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



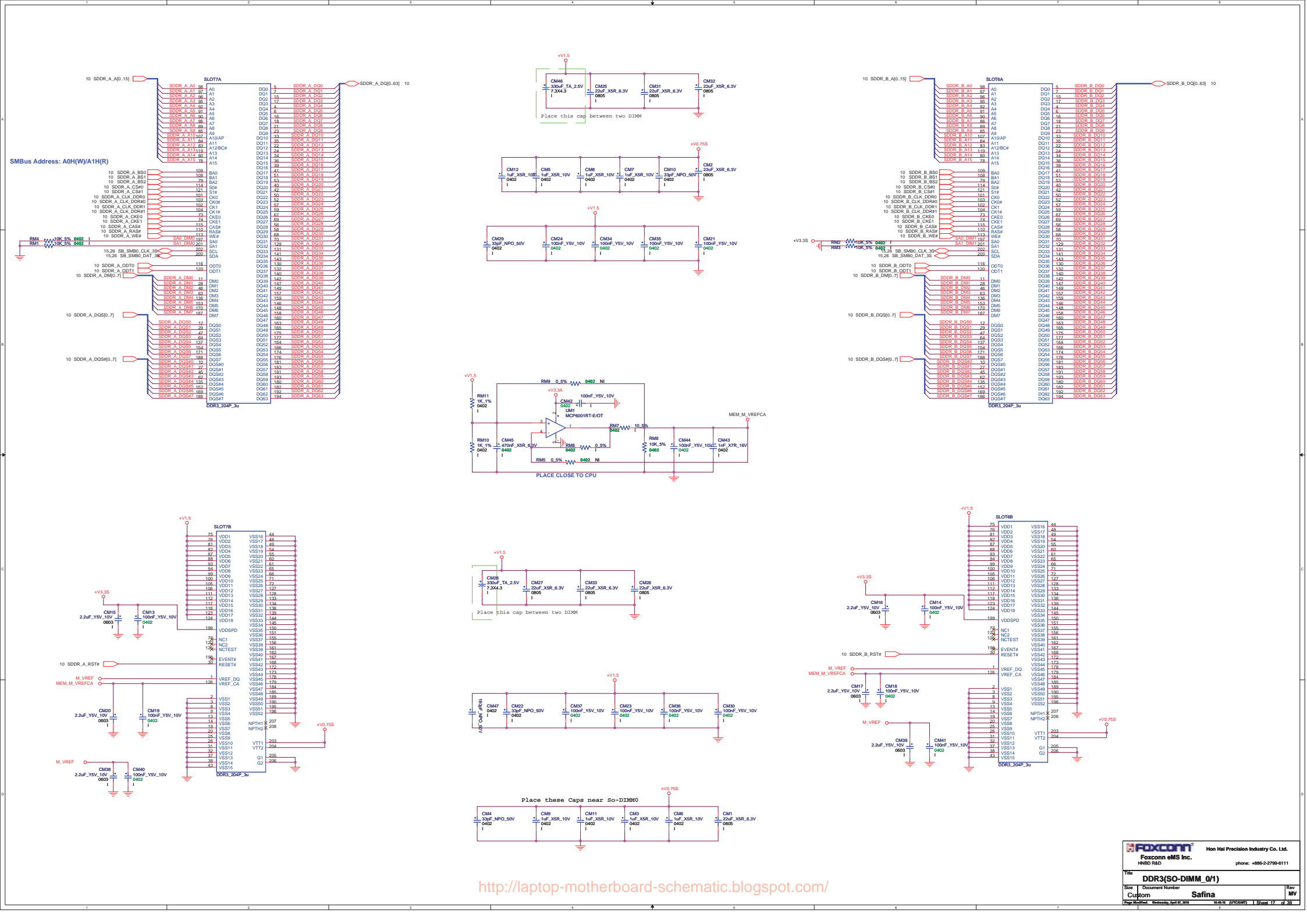
<http://laptop-motherboard-schematic.blogspot.com/>

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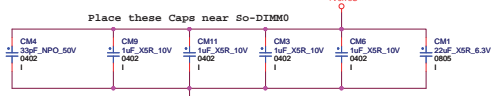
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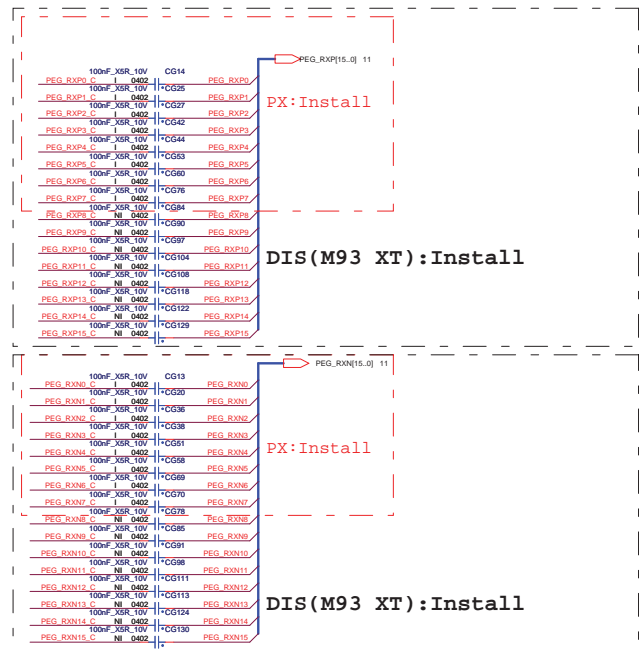
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Custom	Safina	MV

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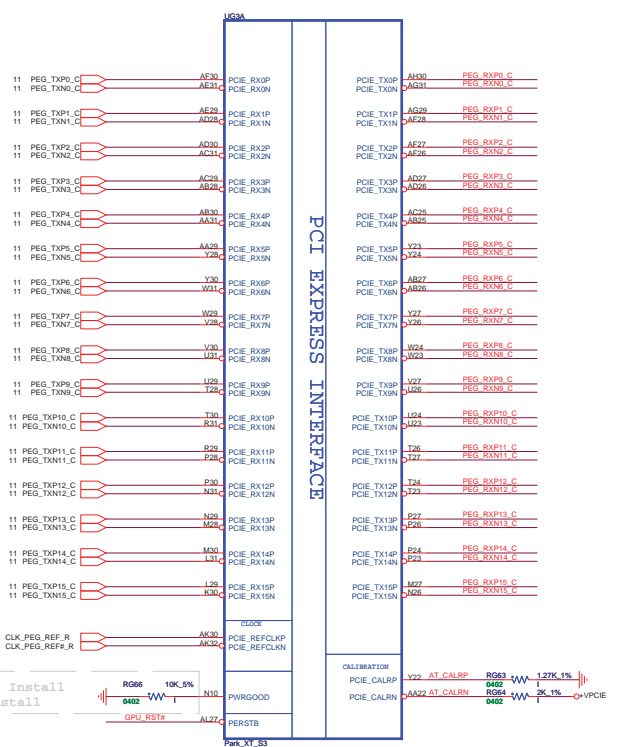
SMBus Address: A0H(W)/A1H(R)





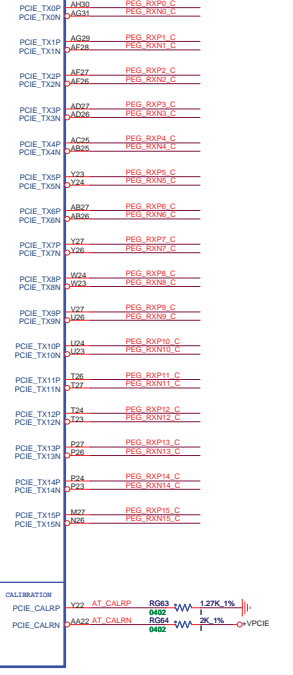
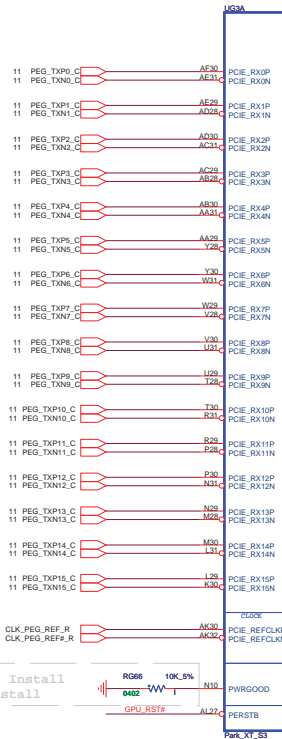
PG:Install

DIS(M93 XT):Install

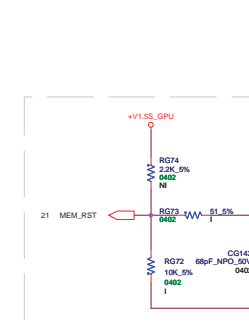


DIS(M93 XT):Install

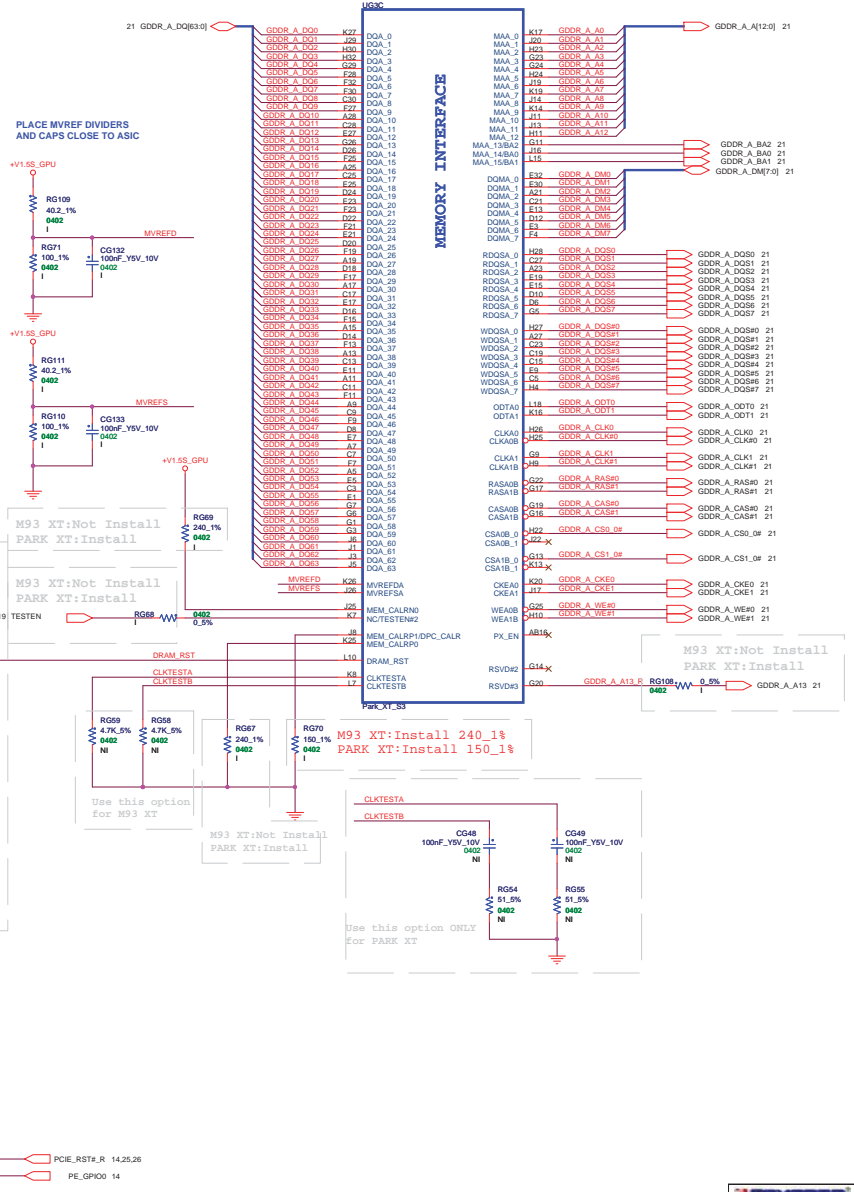
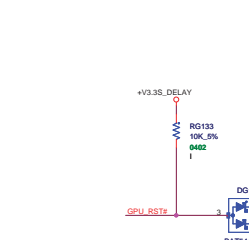
PCI EXPRESS INTERFACE

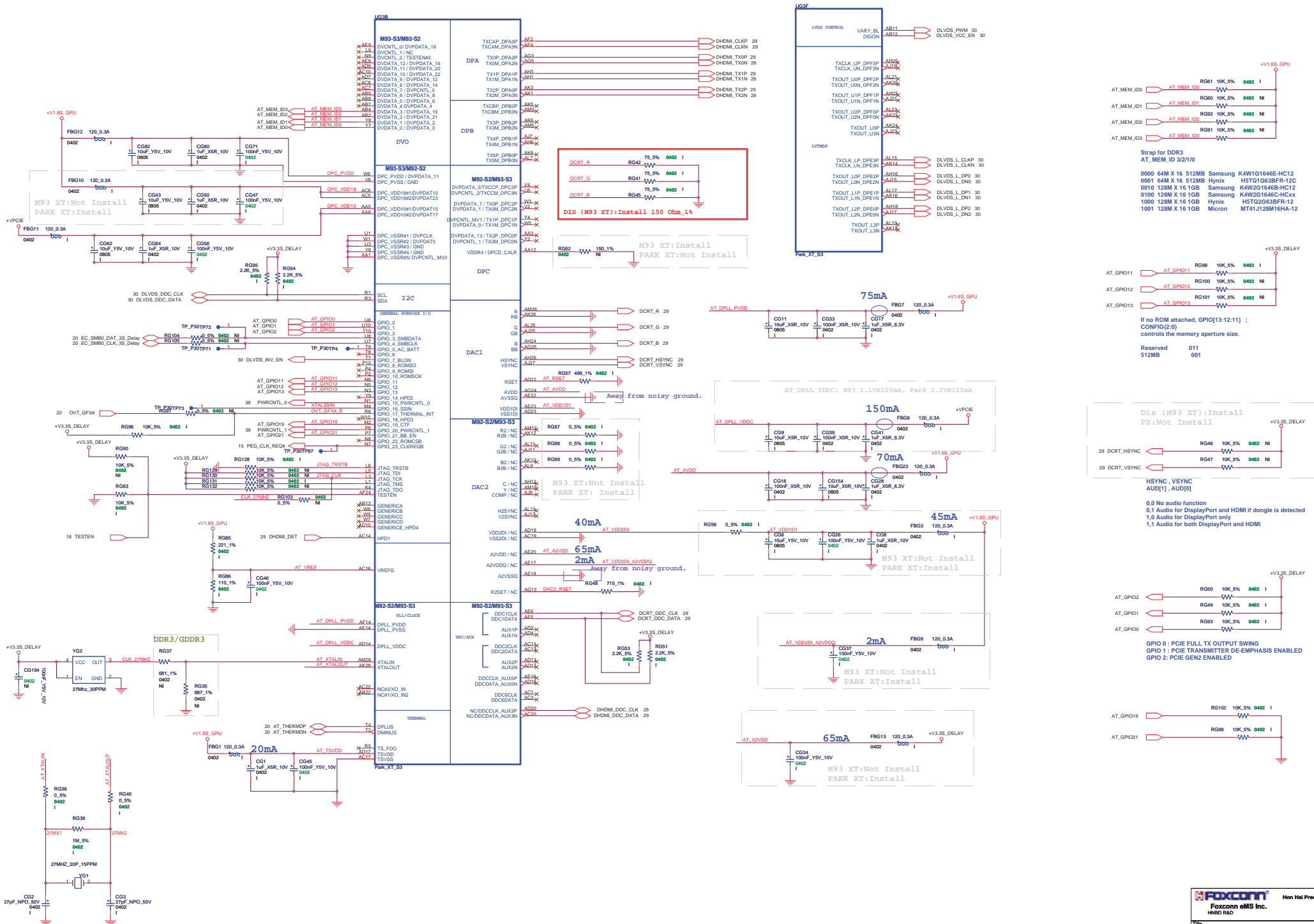


	M93_XT	Park_XT
RG109	100_1% (R1010P930-011-G)	40.2_1% (R10102850-011-G)
RG111	100_1% (R1010P930-011-G)	40.2_1% (R10102850-011-G)



	M93_XT	PARK_XT
RG72	DNI	10K
RG73	0R	51R
RG74	2.2K	DNI
CG142	2.2nF	68pF





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Strap for DDR3
AT_MEM_ID0 I32/1/0

AT_MEM_ID0	RG61 10K.5% 0402 I
AT_MEM_ID1	RG60 10K.5% 0402 NI
AT_MEM_ID2	RG62 10K.5% 0402 NI
AT_MEM_ID3	RG61 10K.5% 0402 NI

0000	64M X 16	512MB	Samsung	K4W1G1646E-HC12
0001	64M X 16	512MB	Hynix	H5TQ1G63BFR-12C
0010	128M X 16	1GB	Samsung	K4W2G1646E-HC12
0100	128M X 16	1GB	Samsung	K4W2G1646C-HCxx
1000	128M X 16	1GB	Hynix	H5TQ2G63BFR-12
1001	128M X 16	1GB	Micron	MT41J128M16HA-12

AT_GPIO11	AT_GPIO11	RG99 10K.5% 0402 I
AT_GPIO12	AT_GPIO12	RG100 10K.5% 0402 NI
AT_GPIO13	AT_GPIO13	RG101 10K.5% 0402 NI

If no ROM attached, GPIO[13:12:11] ;
CONFIG(0) controls the memory aperture size.

Reserved	011
	512MB
	001

Dis (M93 XT):Install
PX:Not Install

29	DCRT_HSYNC	RG46 10K.5% 0402 NI
29	DCRT_VSYNC	RG47 10K.5% 0402 NI

0.0 No audio function
0.1 Audio for DisplayPort and HDMI if dongle is detected
1.0 Audio for DisplayPort only
1.1 Audio for both DisplayPort and HDMI

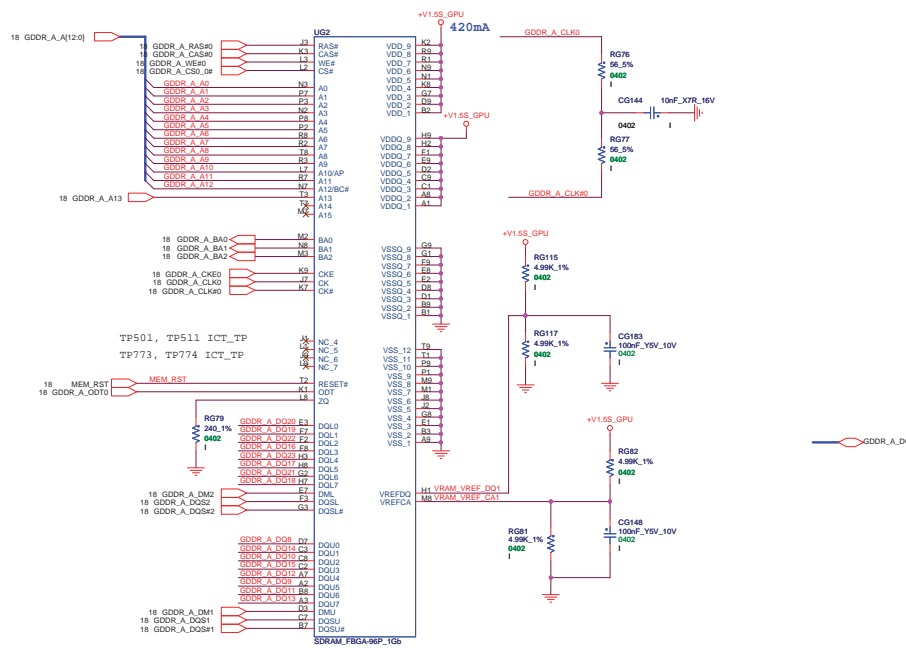
AT_GPIO2	RG50 10K.5% 0402 I
AT_GPIO1	RG49 10K.5% 0402 I
AT_GPIO0	RG63 10K.5% 0402 I

GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED

AT_GPIO19	RG102 10K.5% 0402 I
AT_GPIO21	RG88 10K.5% 0402 I

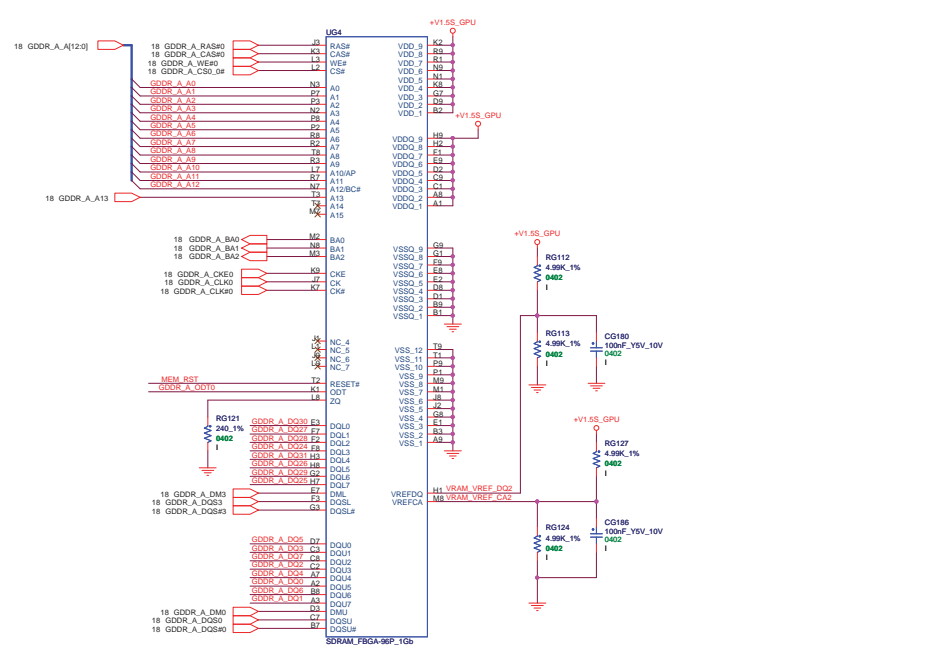
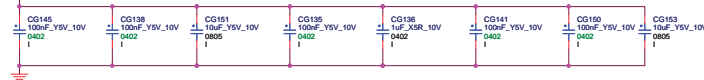
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Foxconn eMS Inc.
1980 RD | phone: +886-2-2799-6111

Title: **VGA (IO)(STRAP) 2/3**
Doc: [blank] | Document Number: [blank]
Custom: [blank] | Safina: [blank]
Date: [blank] | Version: [blank] | Sheet 19 of 29



Place around the VRAM UG2

1.2A

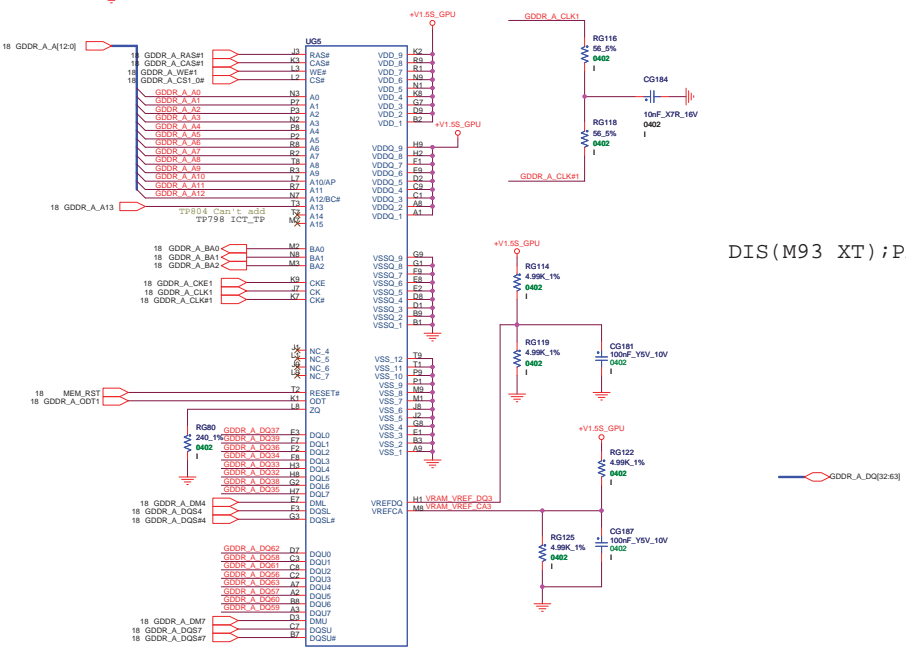


Place around the VRAM UG4

1.2A

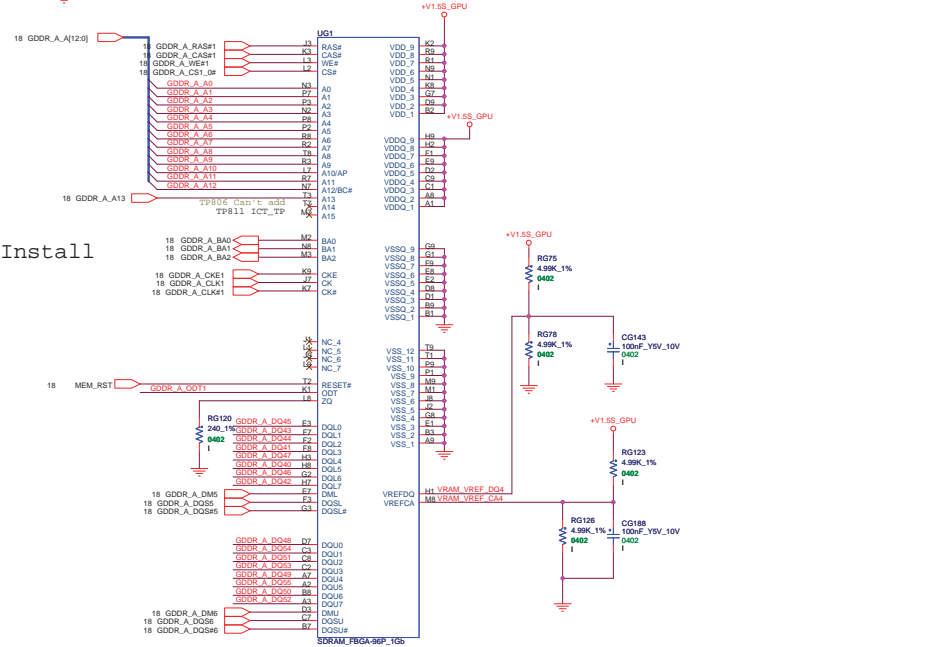
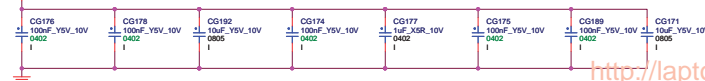


DIS(M93 XT);PX : Install



Place around the VRAM UG5

1.2A

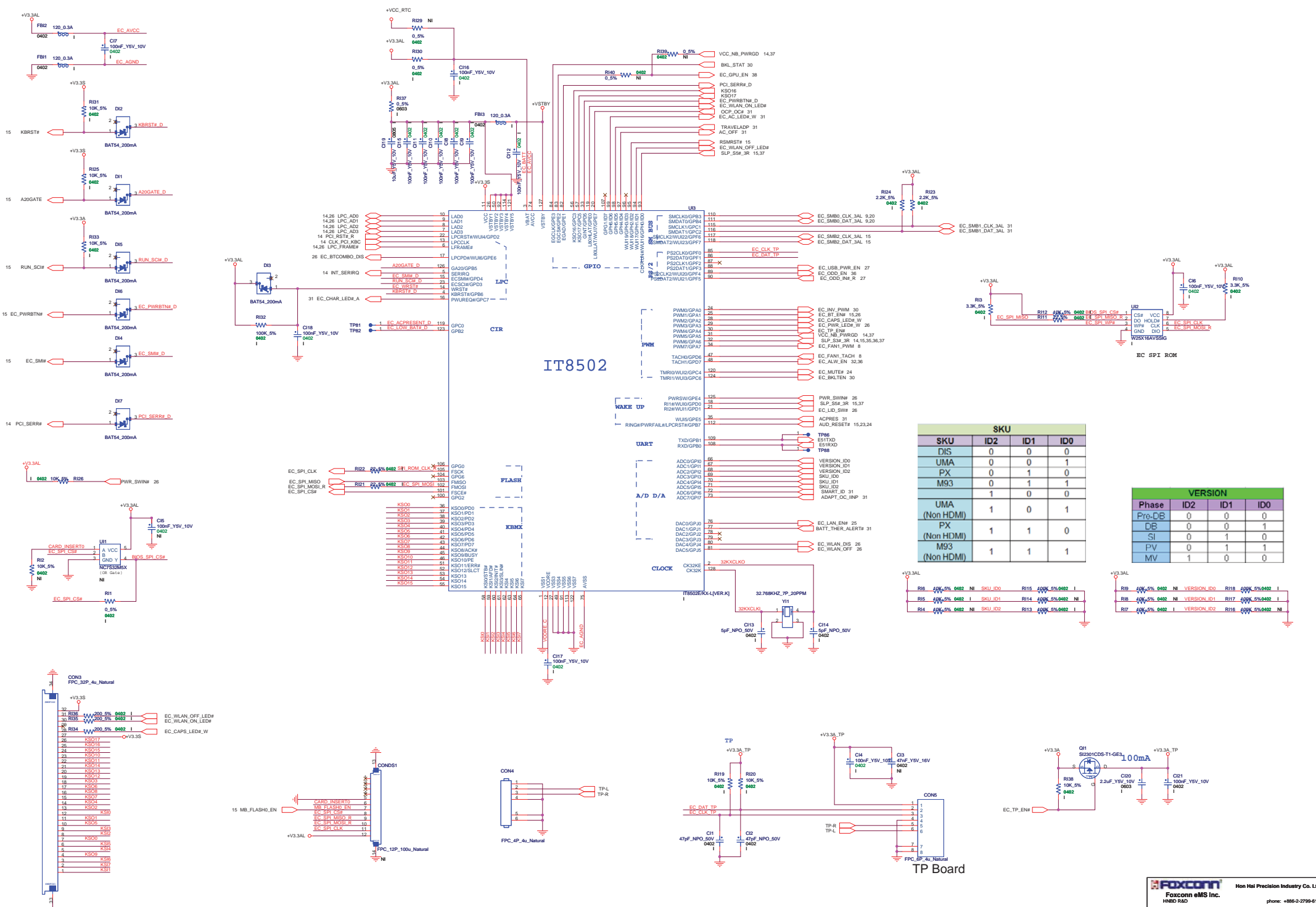


Place around the VRAM UG1

1.2A



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 HonB RD
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 This is **VRAM (DDR3)**
 Spec. / Document Number
 Custom / Safina
 Rev. / MW
 Page 1 of 1
 Date: 2010-04-09
 File: 8-93 (612mm) | Sheet 21 of 29



IT8502

SKU			
SKU	ID2	ID1	ID0
DJS	0	0	0
UMA	0	0	1
PX	0	1	0
M93	0	1	1
UMA (Non HDMI)	1	0	0
PX (Non HDMI)	0	0	1
SI	0	1	0
PV	0	1	1
MV	1	0	0

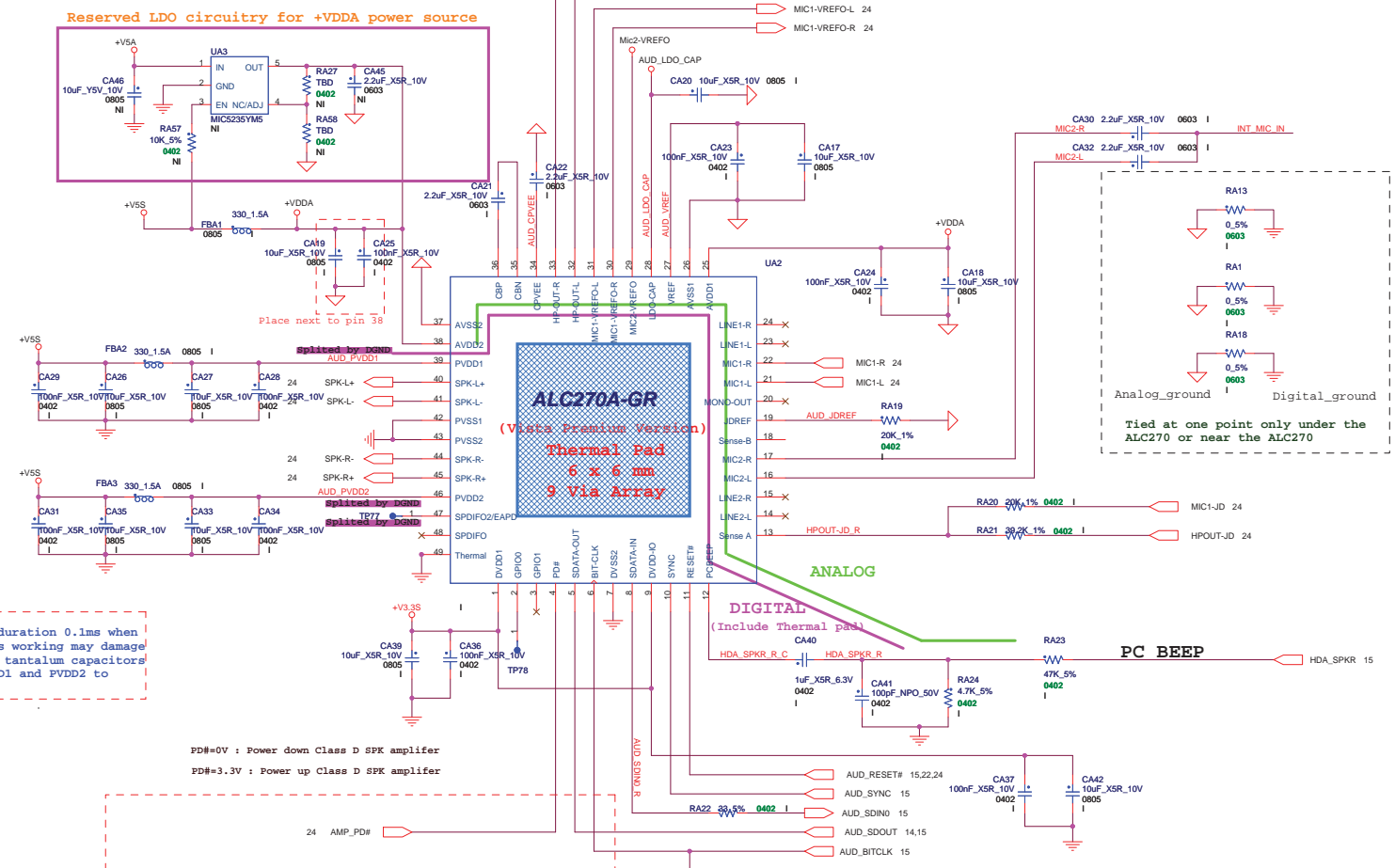
VERSION			
Phase	ID2	ID1	ID0
Pre-DB	0	0	0
DB	0	0	1
SI	0	1	0
PV	0	1	1
MV	1	0	0

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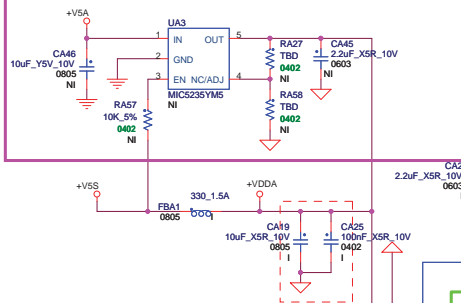
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Foxconn eMS Inc.
 HNSD R&D phone: +886-2-2799-6111

Doc: **EC+KBC(IT8502E) & ROM**
 Custom **Safina** Rev: **MV**

Page: 1 of 1
 Date: 2013/04/22
 Rev: 1.0
 Sheet: 22 of 30



Reserved LDO circuitry for +VDDA power source

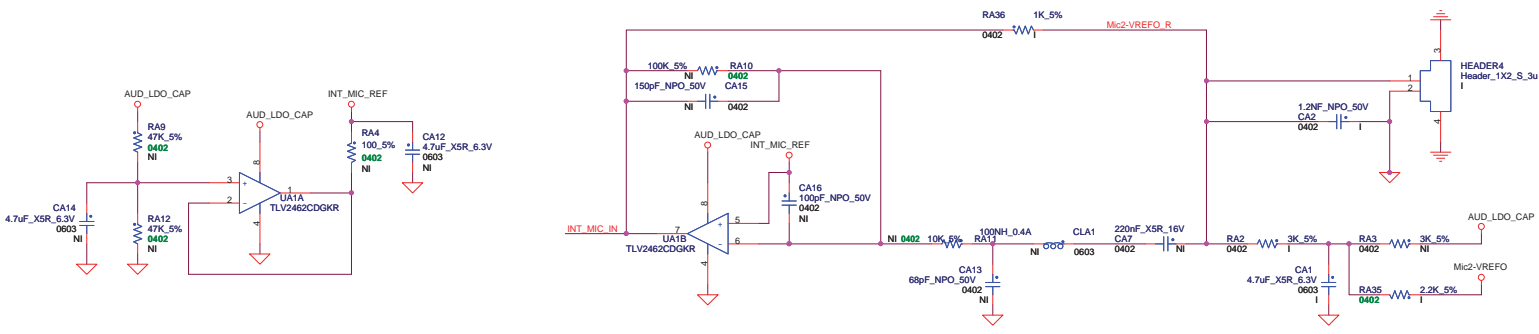


Place next to pin 38

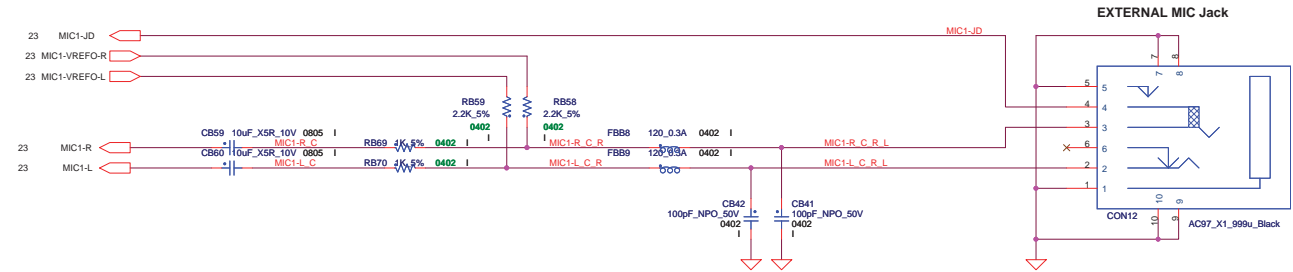
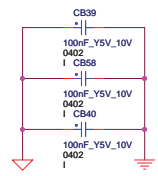
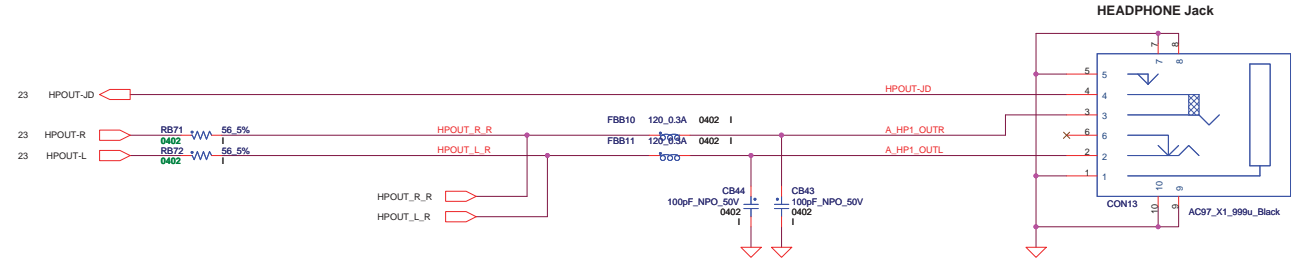
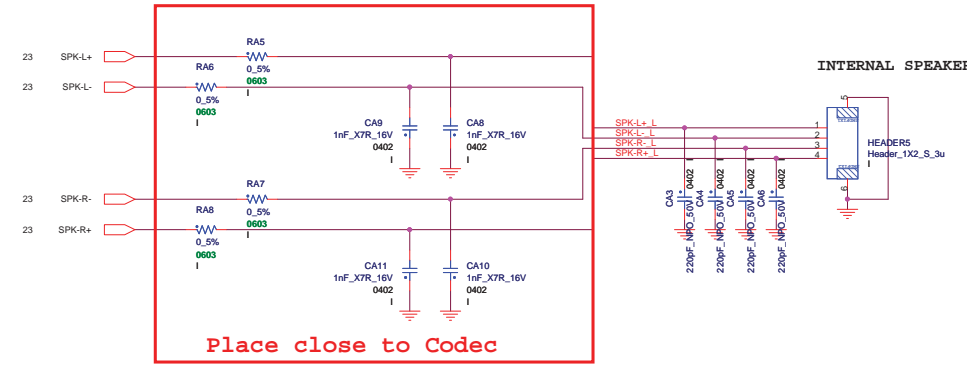
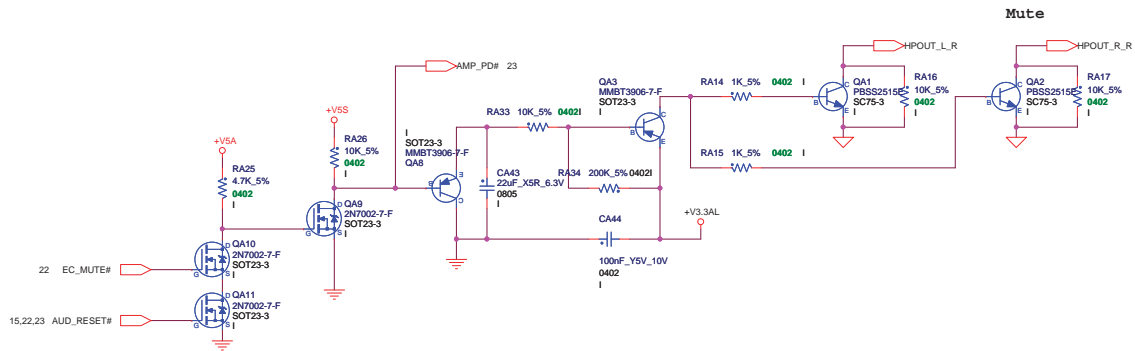
<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

PD# = 0V : Power down Class D SPK amplifier
PD# = 3.3V : Power up Class D SPK amplifier

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High first.
2. When you want to exit your Bios Programming Code, please let the EC_MUTE# Low. (The programming is different from before .)

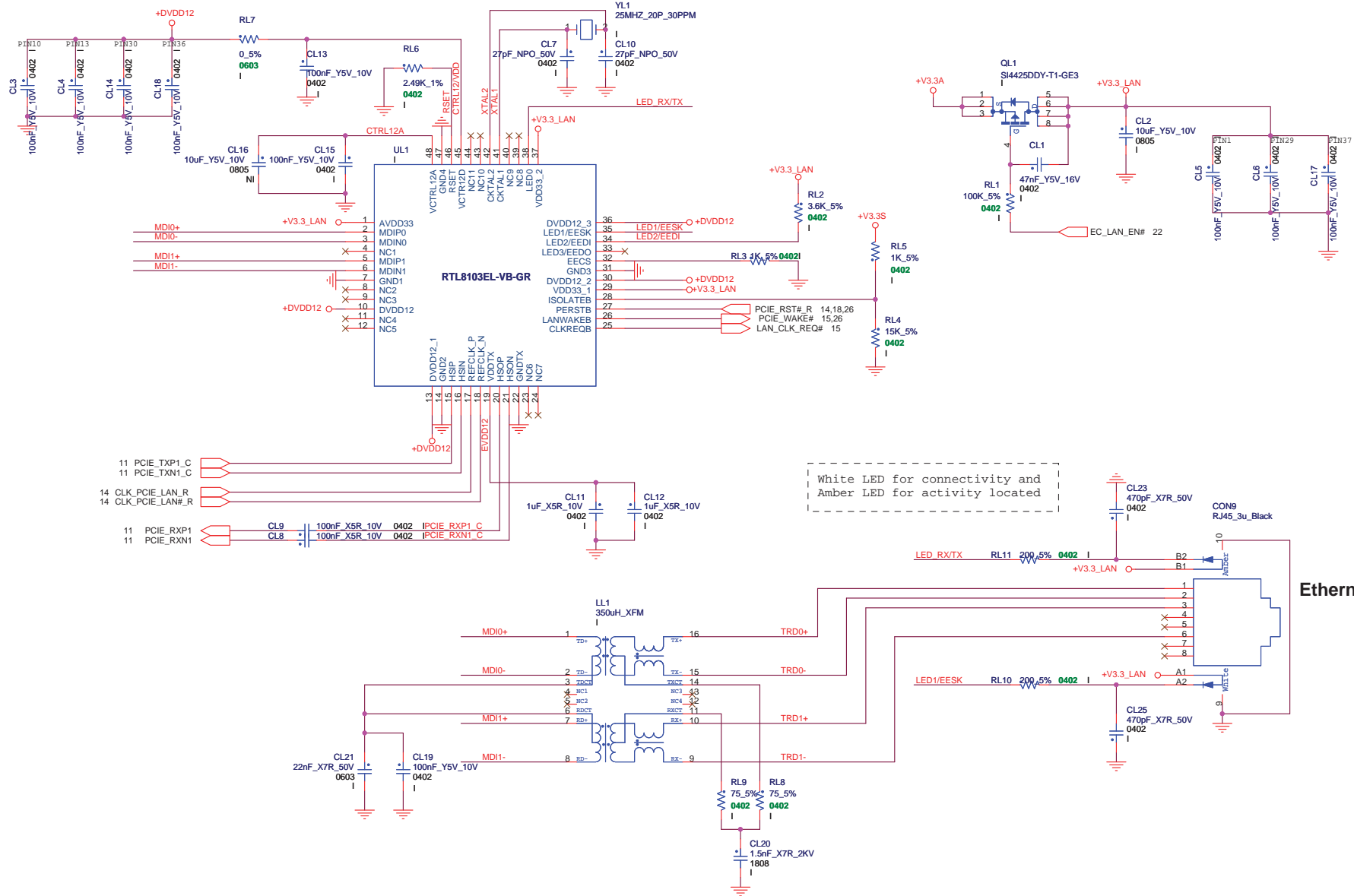


		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBSD R&D	
		phone: +886-2-2799-6111	
Audio (CODEC_ALC270A)			
Size	Document Number	Rev	
Custom	Safina	MV	
Page Modified: Wednesday, April 27, 2011		184818 (UTC/GMT) Sheet 23 of 39	



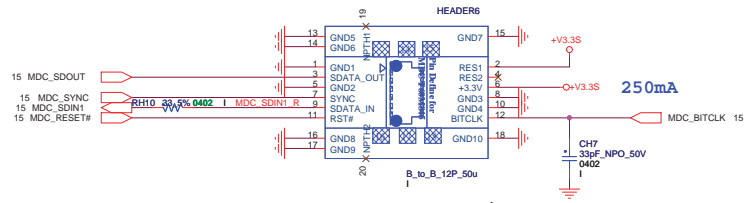
<http://laptop-motherboard-schematic.blogspot.com/>

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Foxconn eMS Inc.		HNBD R&D	
Custom		Safina	
Page Modified: Wednesday, April 07, 2010		184818 (UTC/GMT) Sheet 24 of 39	
Title		Audio (JACK+AMP+SPK+Mute)	
Size	Document Number	Rev	MW

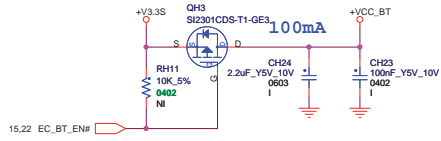
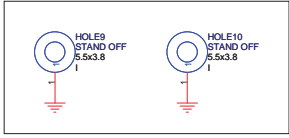


White LED for connectivity and Amber LED for activity located

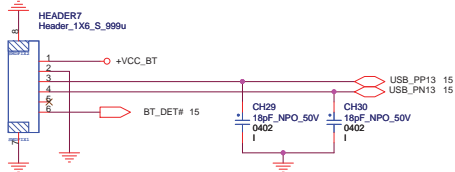
Ethernet



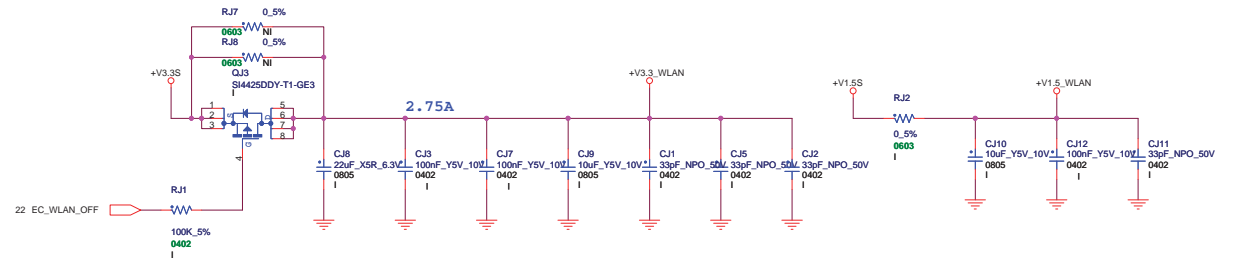
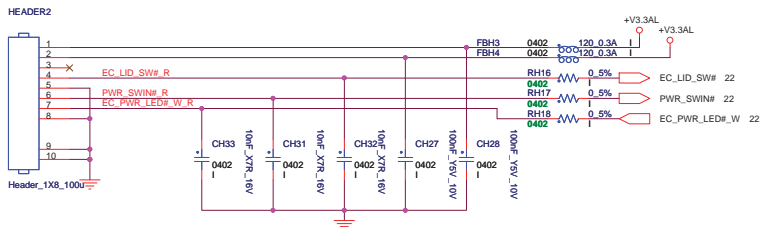
MDC CONN. Option



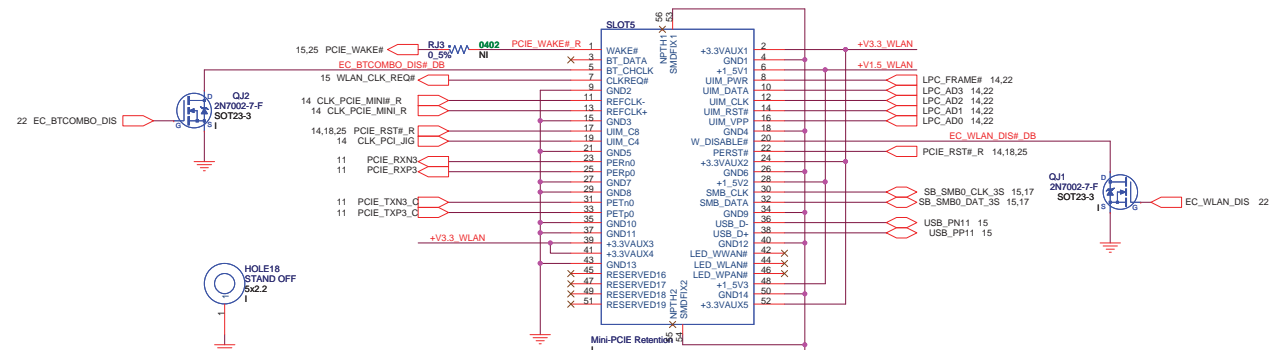
Bluetooth CONN.



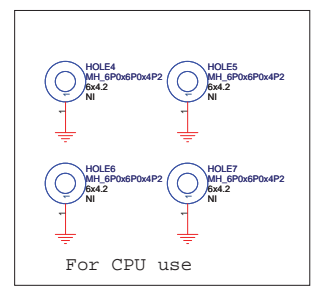
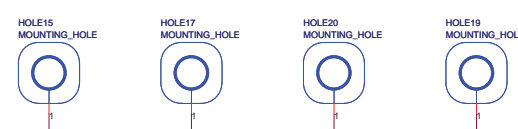
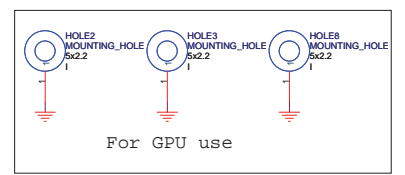
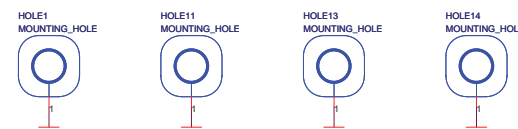
PWR Board CONN.



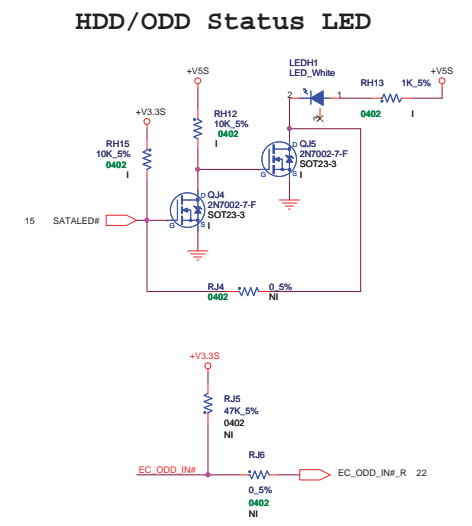
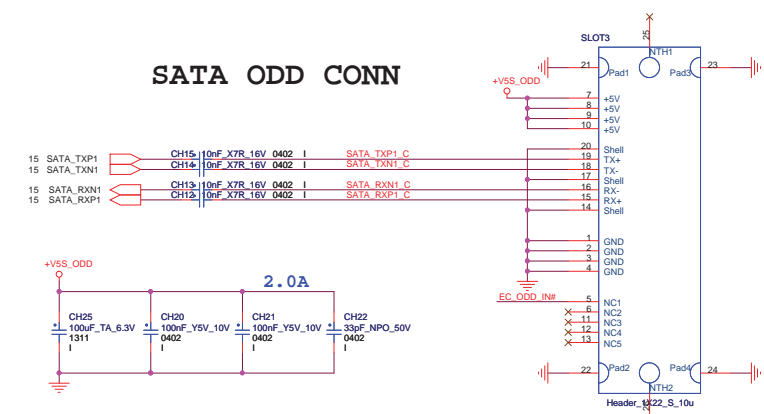
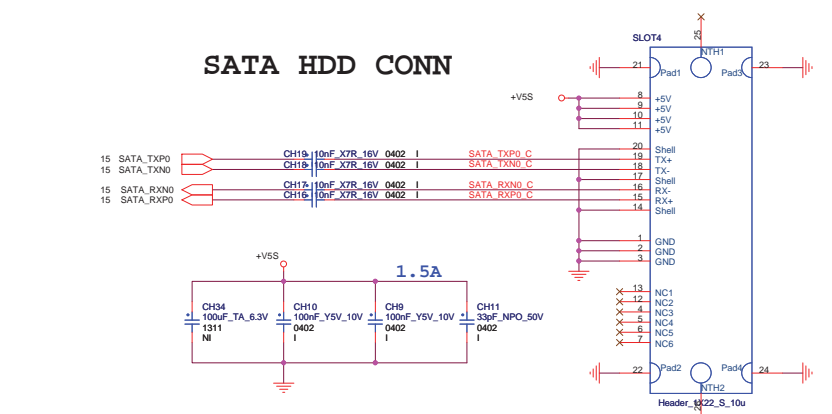
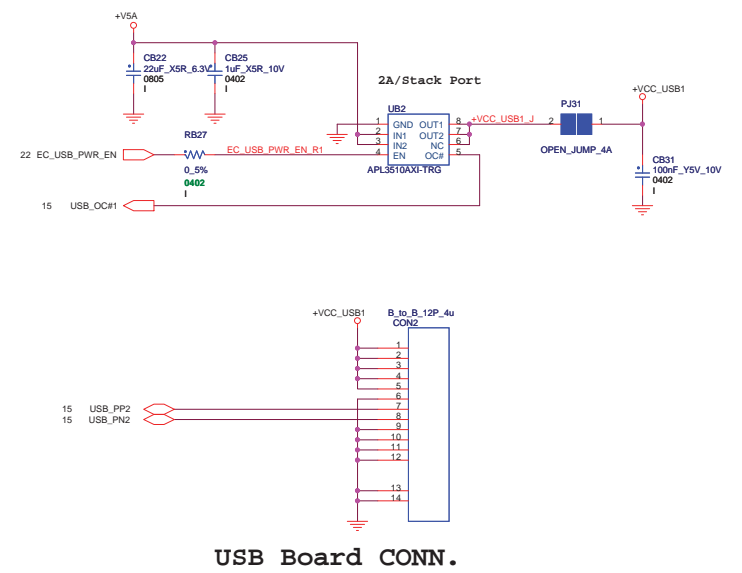
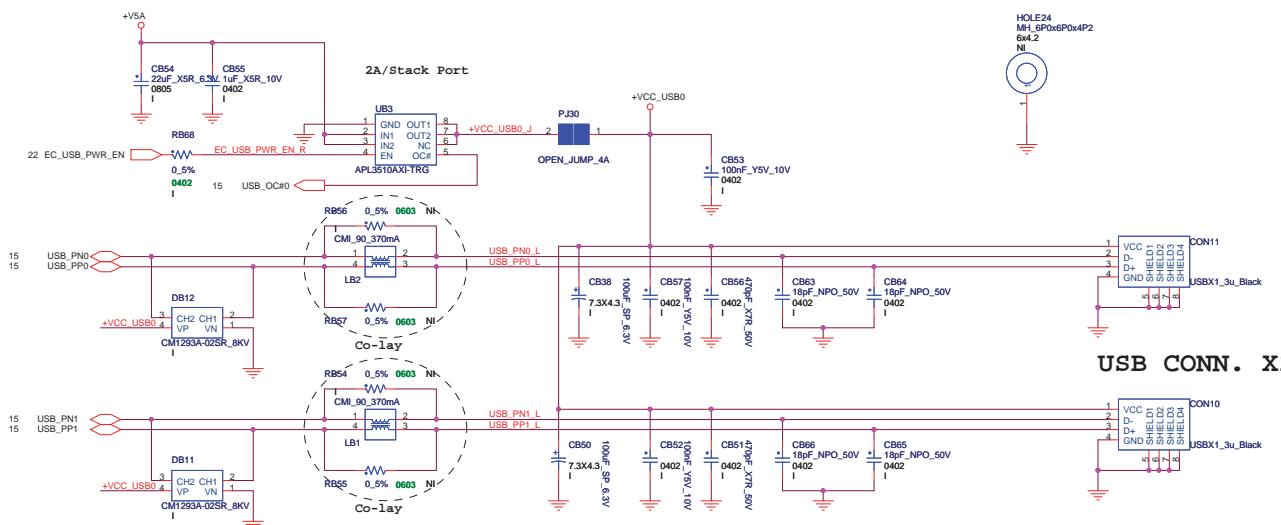
+1.5V=>0.5A Peak/0.375A Normal
+3.3Vaux=>2.75A Peak/1.1A Normal



Half Mini Card for WLAN

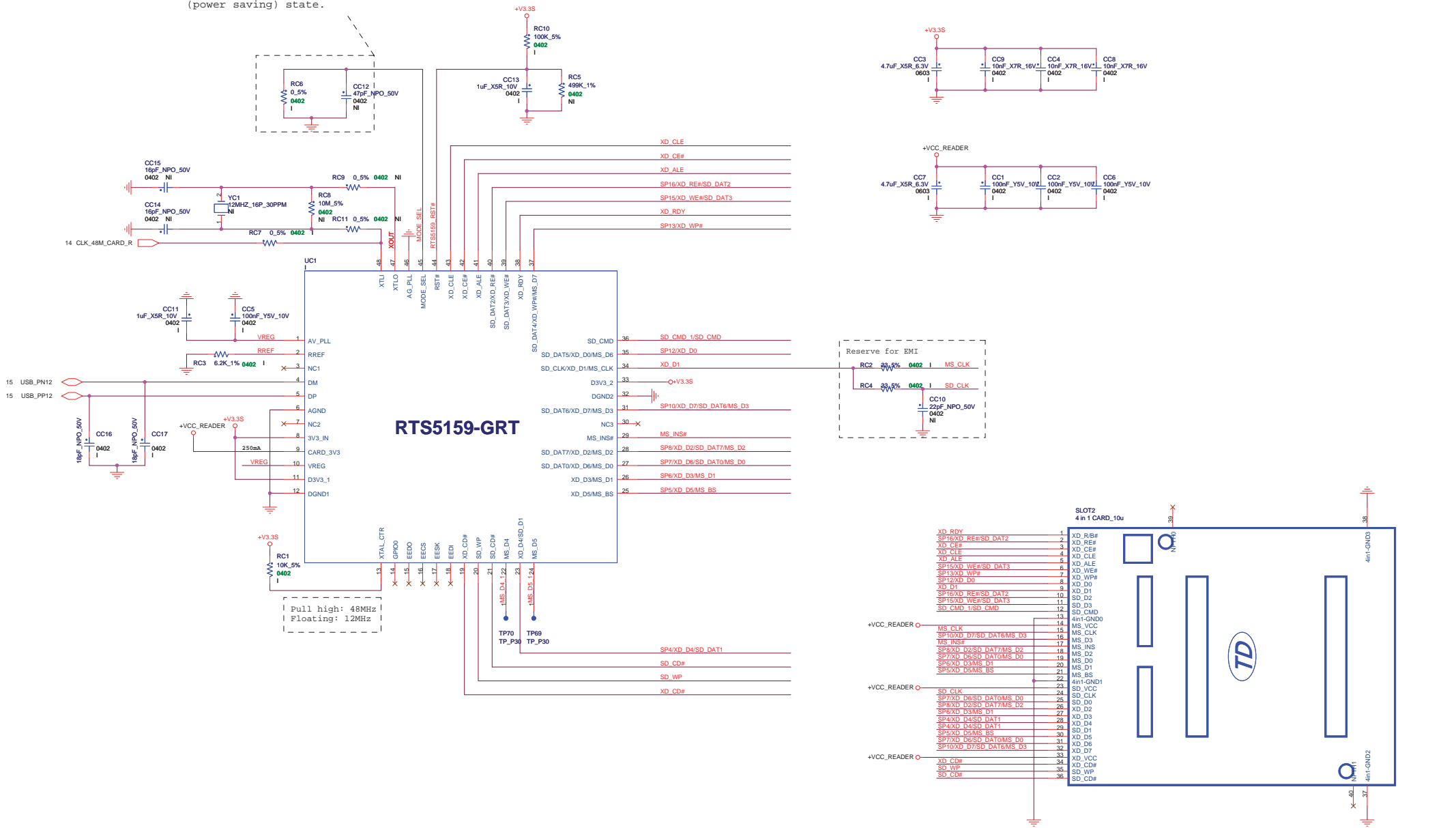


Mounting HOLE

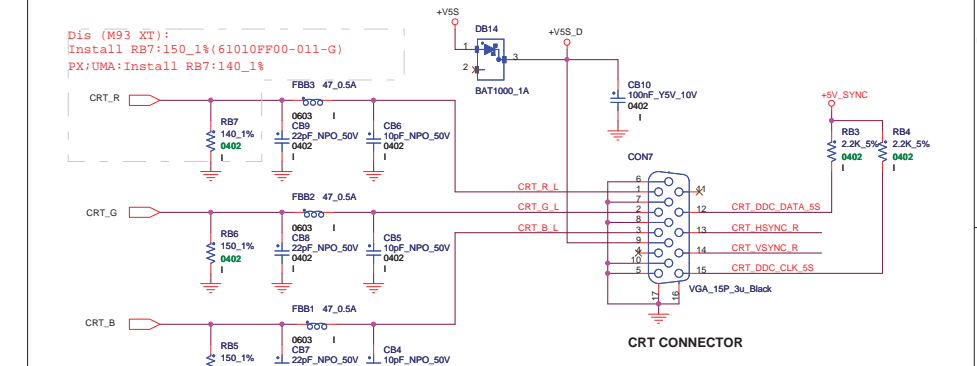
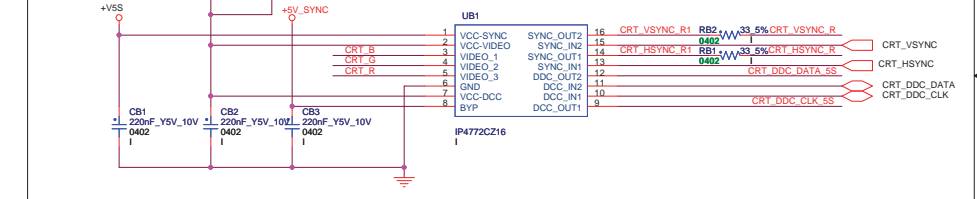
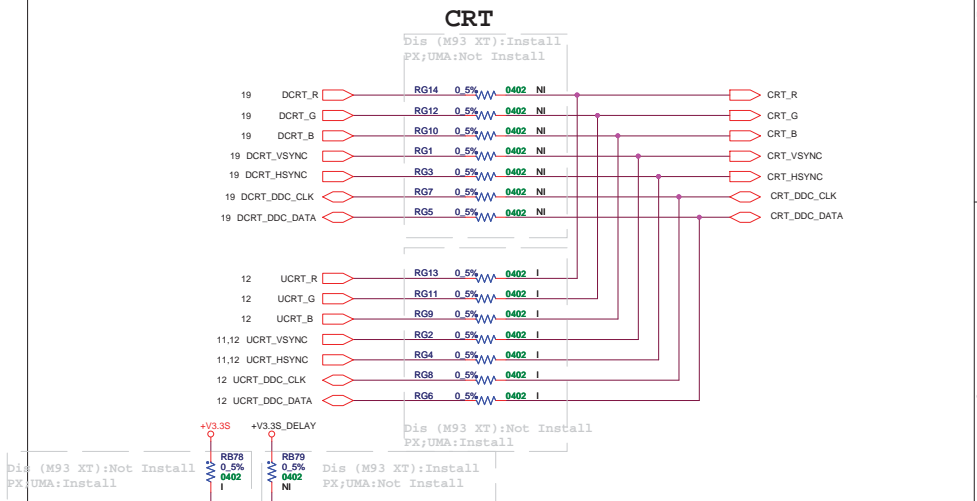
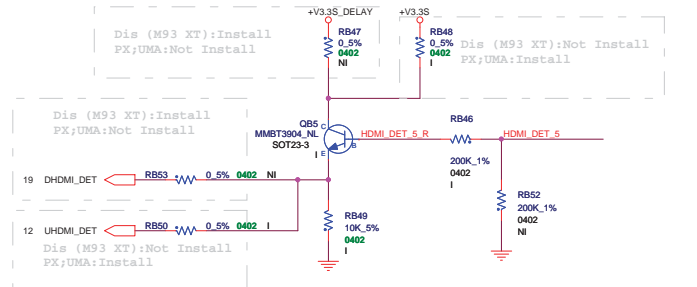
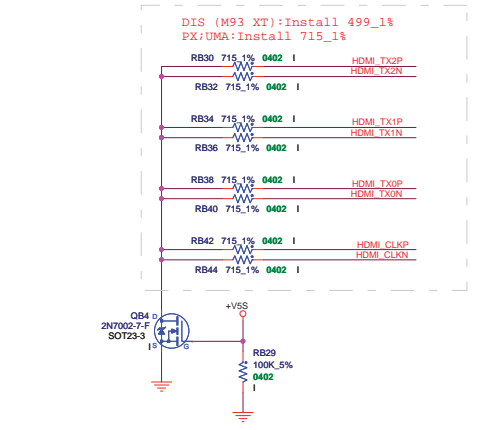
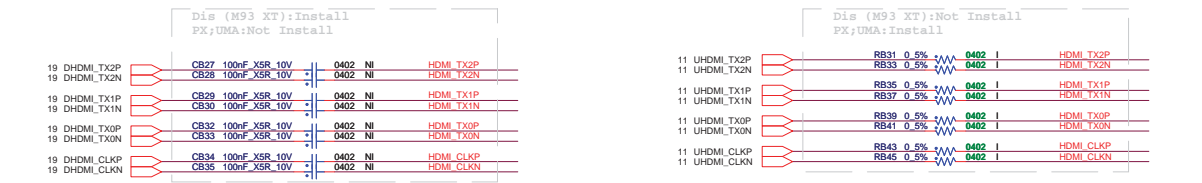
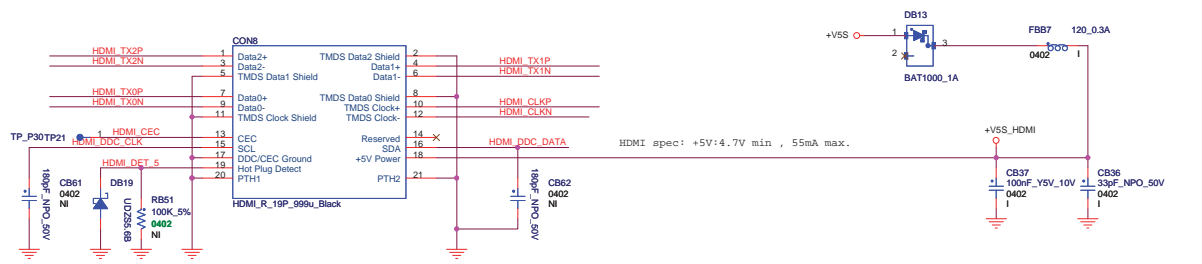
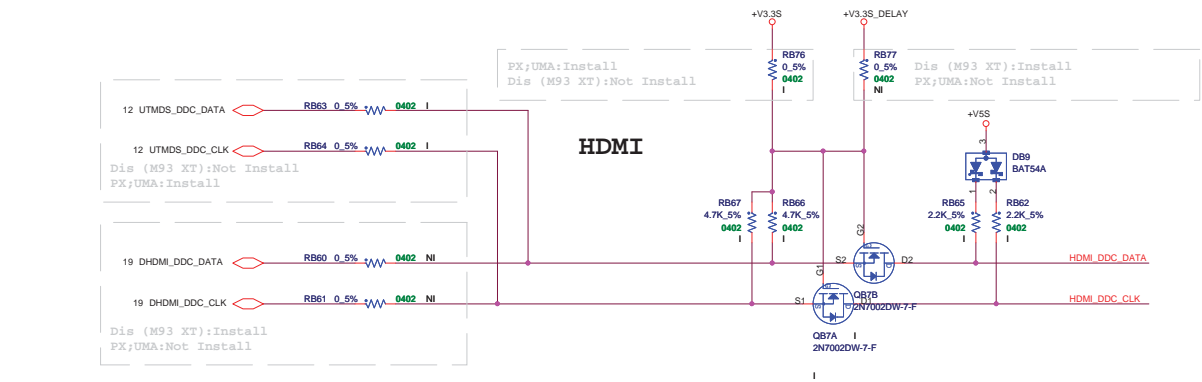


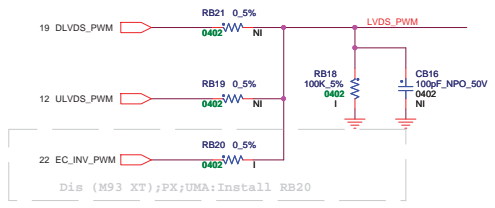
Power pin current
max. 1300 mA (less 2ms)

D3 mode: (R:0 ohm ; C:NC)
 If user remove memory card from
 socket, RTS5159 will terminate
 USB bus connection and enter D3
 (power saving) state.

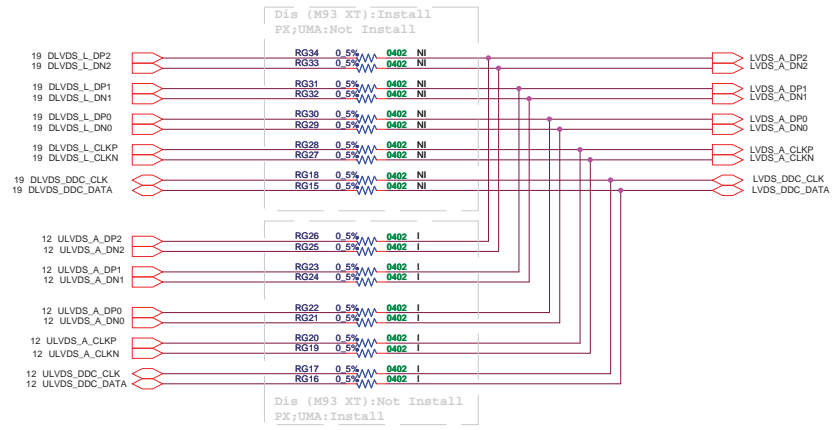


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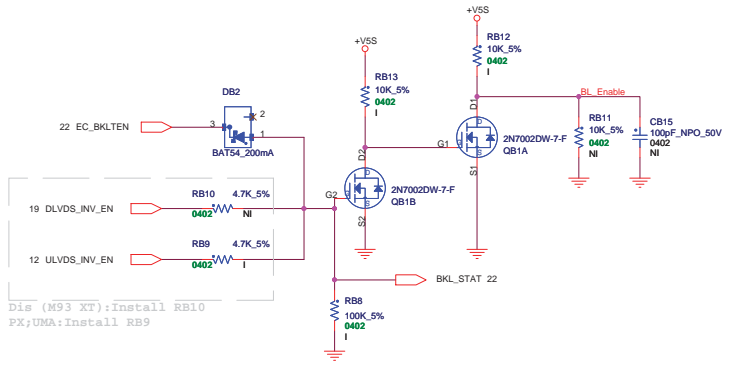




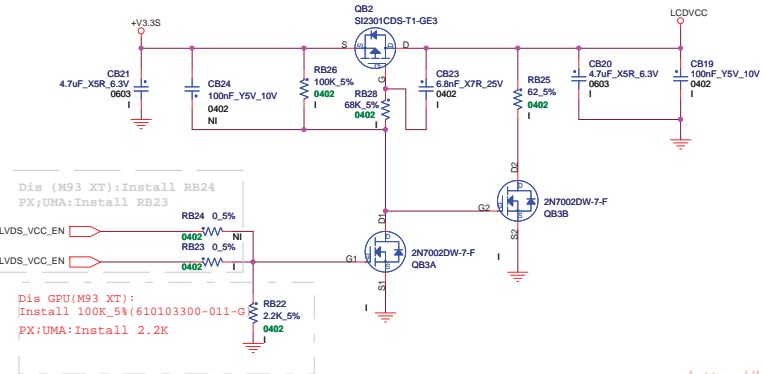
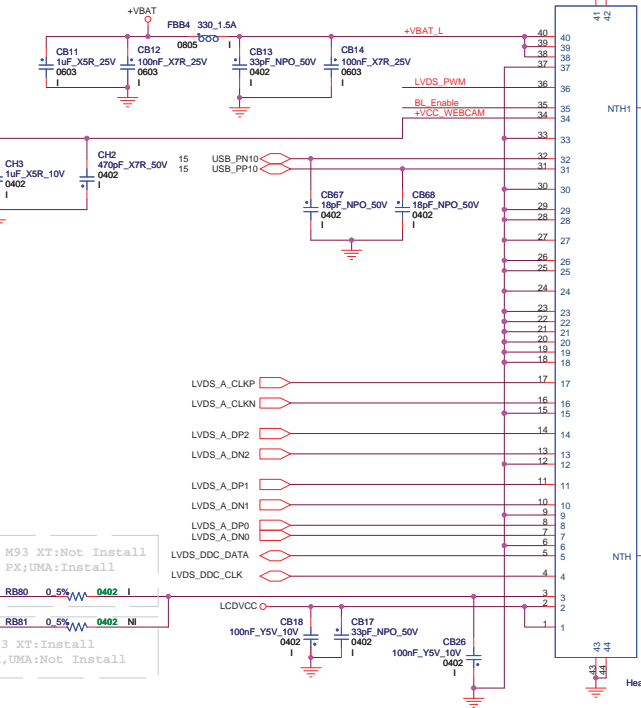
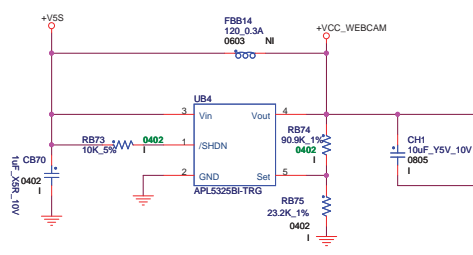
Dis (M93 XT):PX;UMA:Install RB20



Dis (M93 XT):Not Install
PX;UMA:Install



Dis (M93 XT):Install RB10
PX;UMA:Install RB9



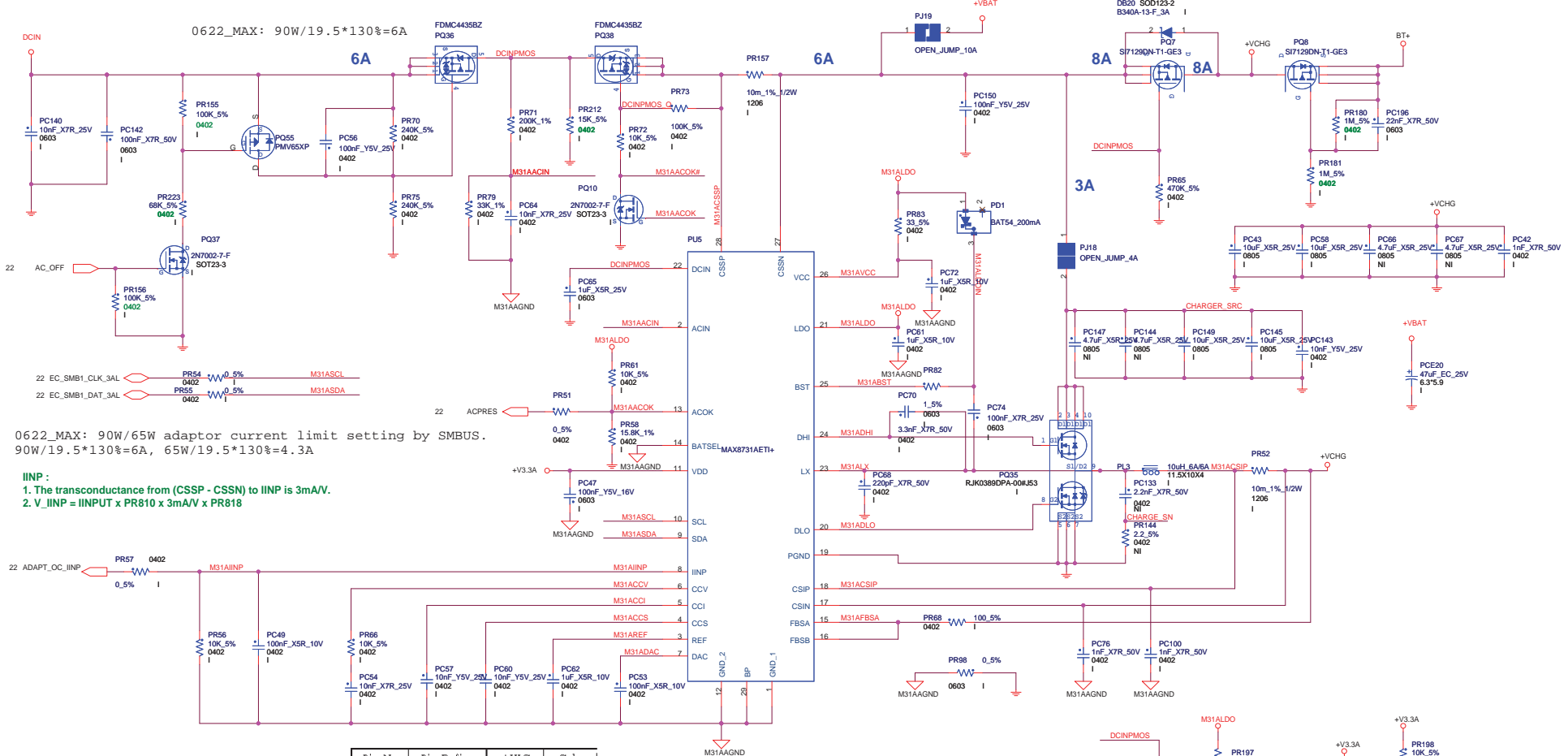
Dis (M93 XT):Install RB24
PX;UMA:Install RB23

Dis GPU(M93 XT):
Install 100K_5%(610103300-011-G)
PX;UMA:Install 2.2K

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Title LVDS&Webcam		Rev Mv
Size Custom	Document Number Safina	
Page Modified: Wednesday, April 07, 2010 18:48:16 (UTC+08:00)		Sheet 30 of 39

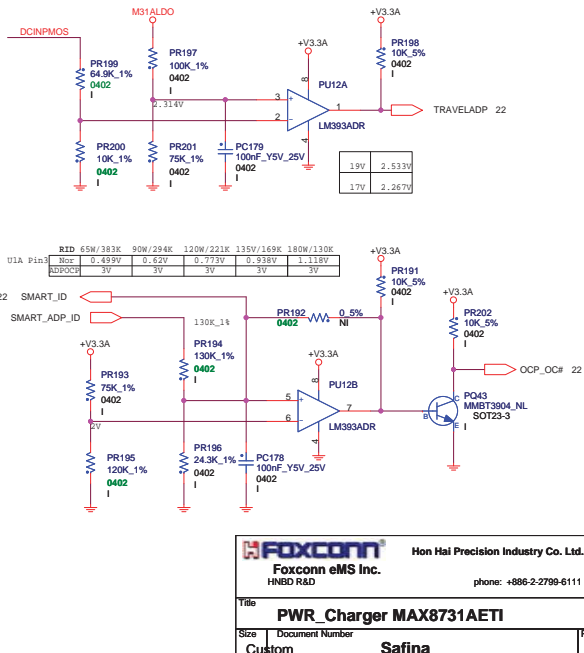
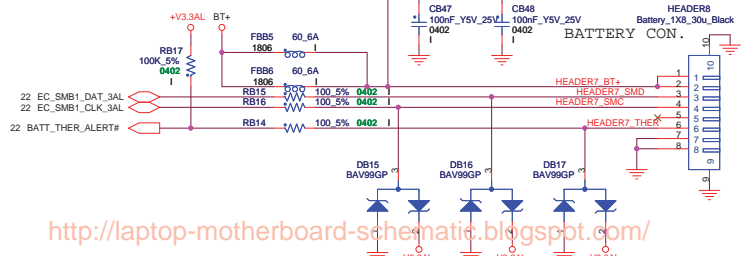
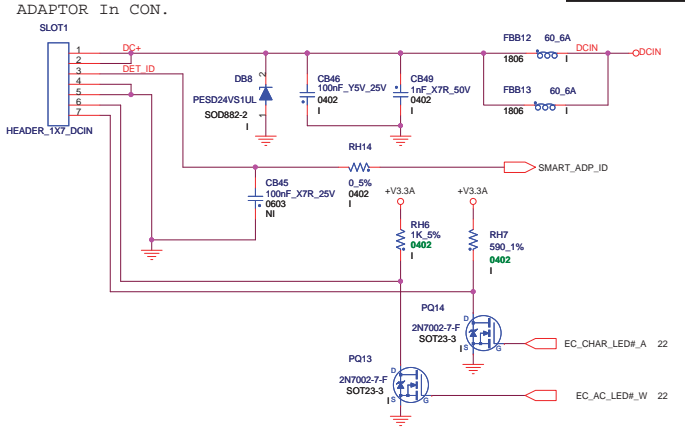


0622_MAX: 90W/65W adaptor current limit setting by SMBUS.
 90W/19.5*130%=6A, 65W/19.5*130%=4.3A

IINP :
 1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
 2. V_IINP = IINP x PR810 x 3mA/V x PR818

Pin No	Pin Define	AWG	Color
1	DC+	22	Red
2	DC+	22	Red
3	Detect (ID)	28	White
4	Detect (ID)	22	Black
5	DC-	22	Black
6	LED-	28	Black
7	LED+	28	yellow

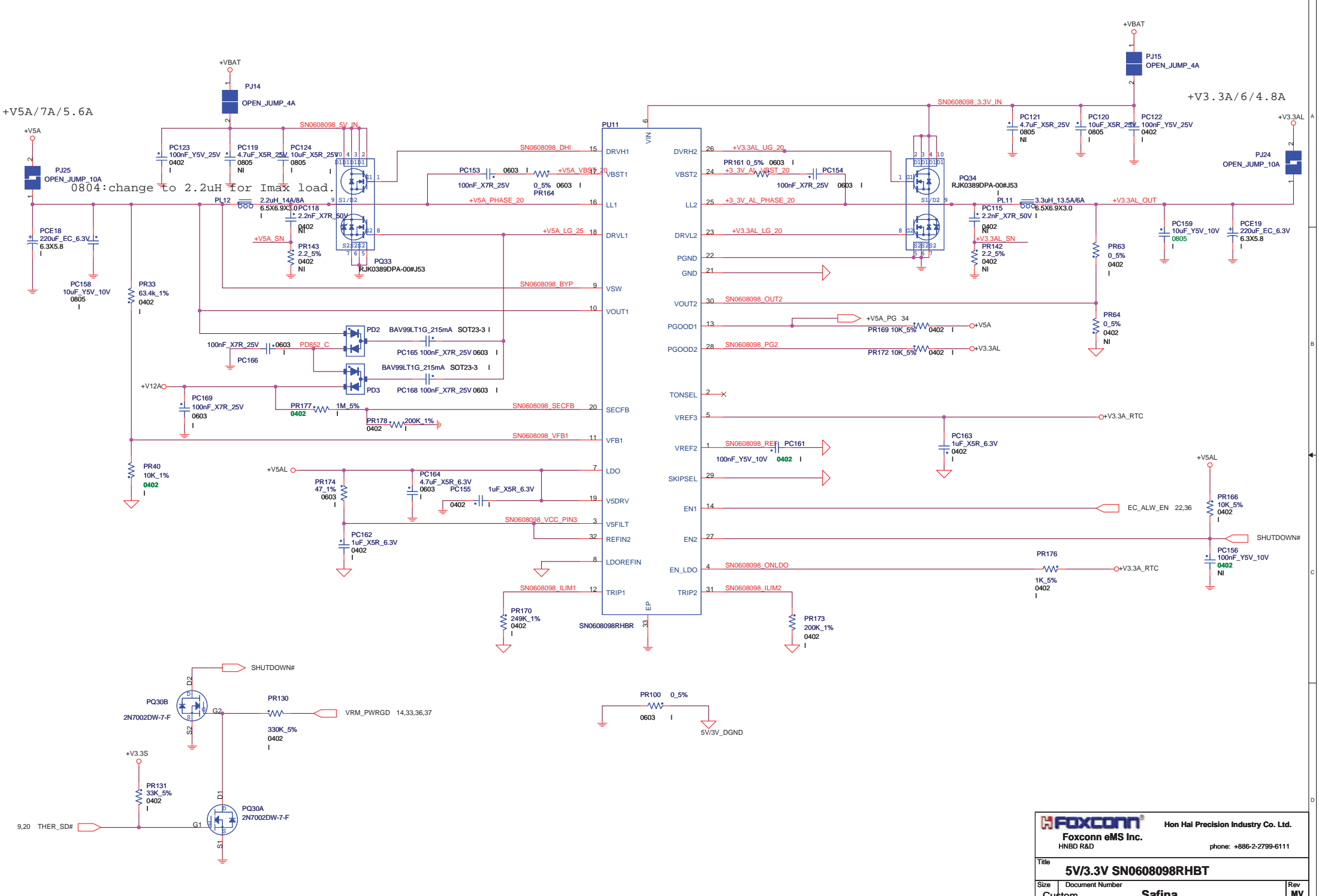
Pin No.	Symbol	Comments
1	B ATT+	Batt+, Battery Positive Terminal.
2	B ATT+	Batt+, Battery Positive Terminal.
3	SMD	SMBus data interface I/O pin..
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



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 Foxconn eMS Inc.
 HNBD RAD phone: +886-2-2799-6111

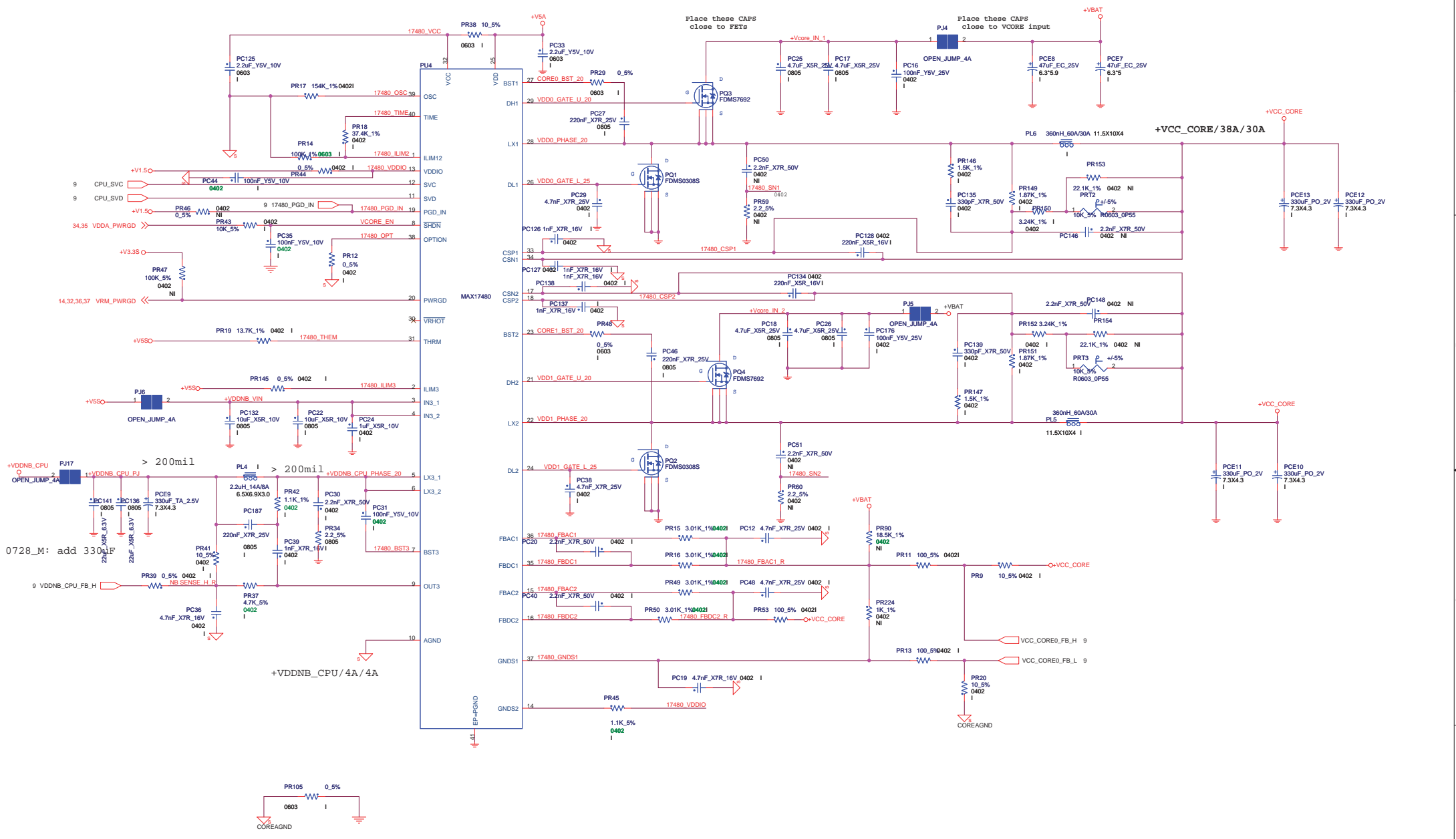
Title: **PWR_Charger MAX8731AET1**

Size: Document Number
 Custom Safina
 Page Modified: Wednesday, April 27, 2011 18:16 (UTC+8) Sheet 31 of 39

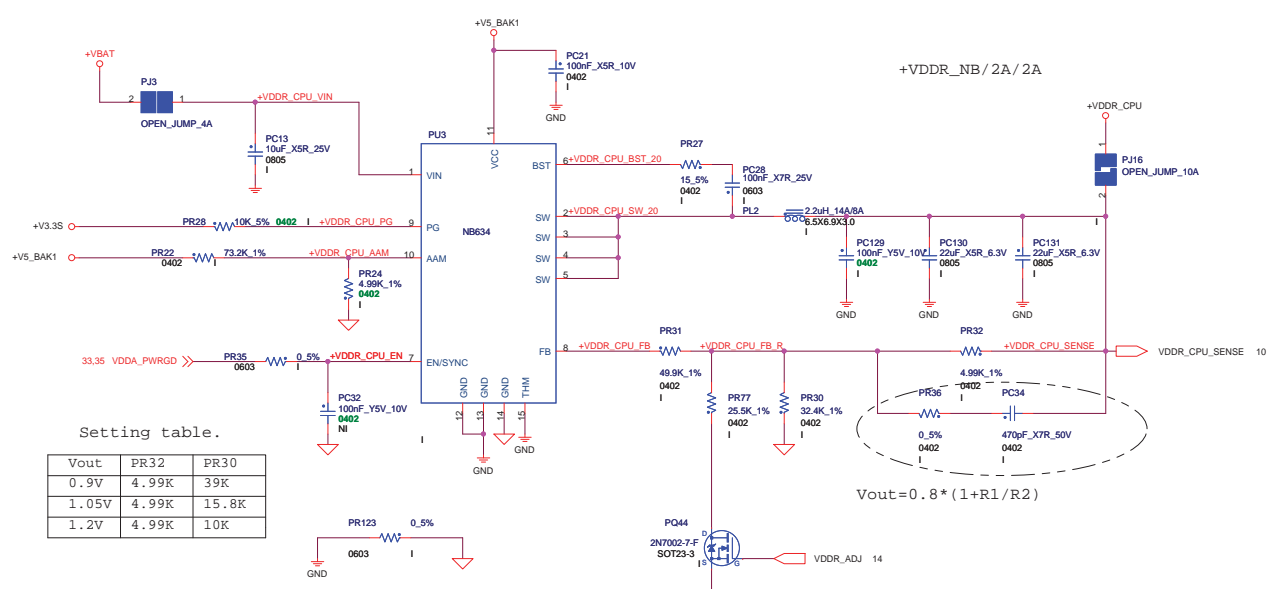
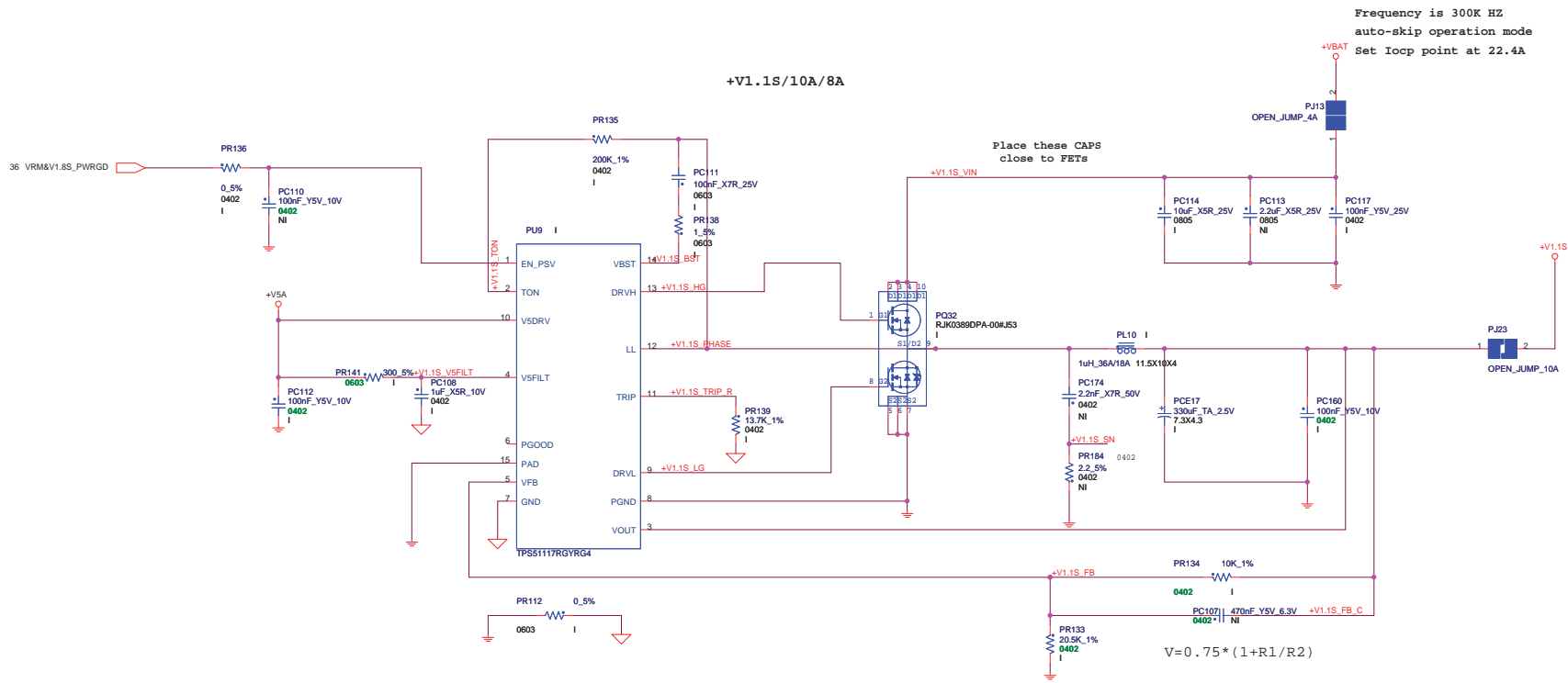


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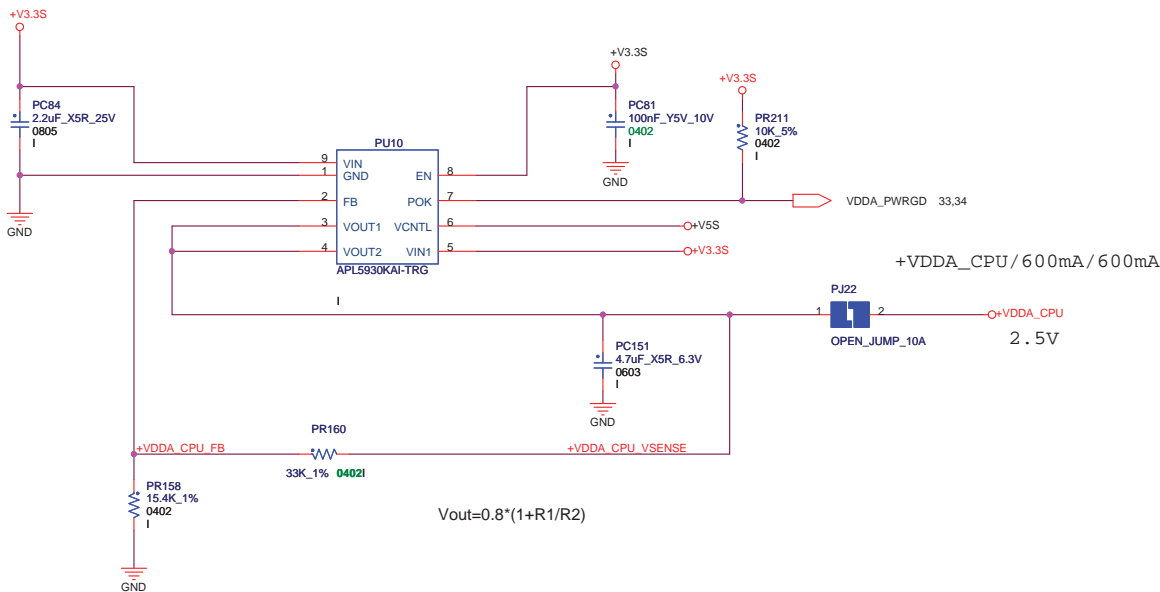
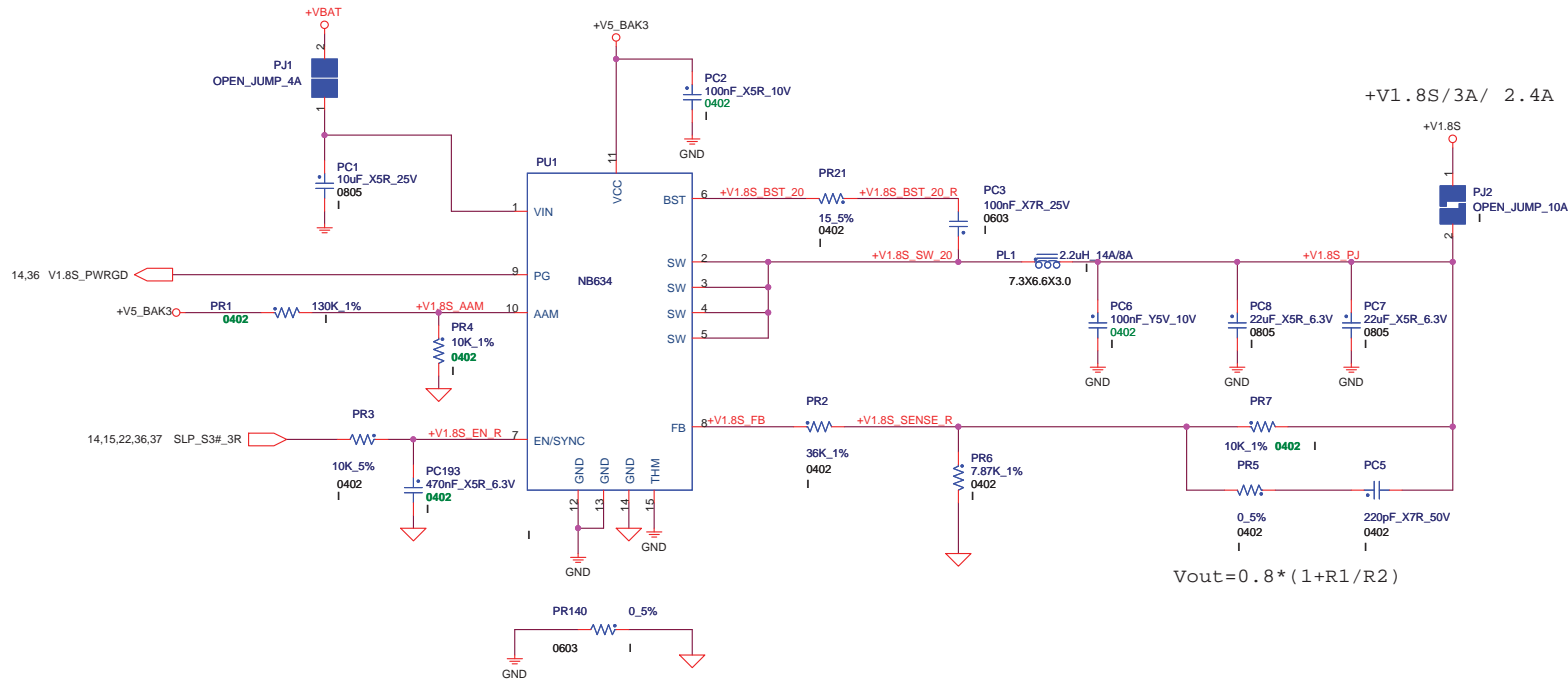
		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D phone: +886-2-2799-6111	
Title 5V/3.3V SN0608098RHBT			
Size Custom		Document Number Safina	
Page Modified: Wednesday, April 07, 2010		18:49:16 (UTC+GMT) Sheet 32 of 39	



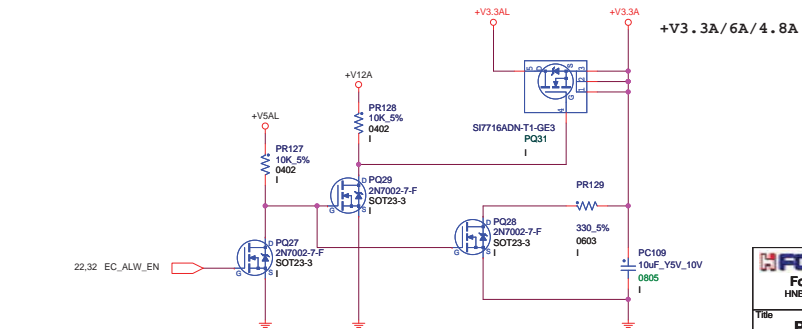
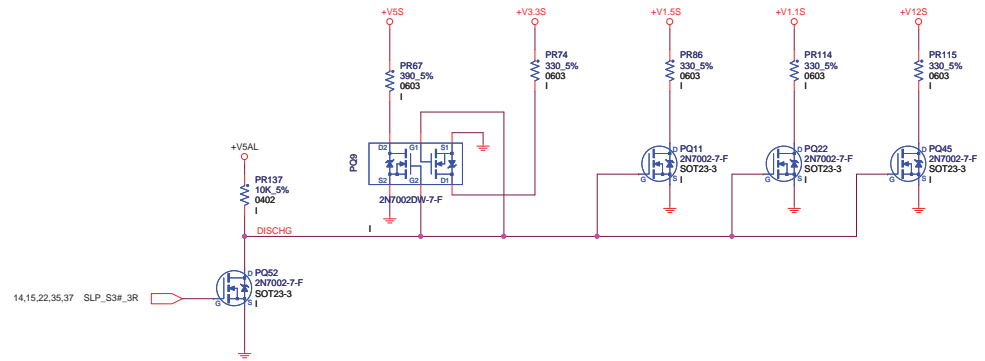
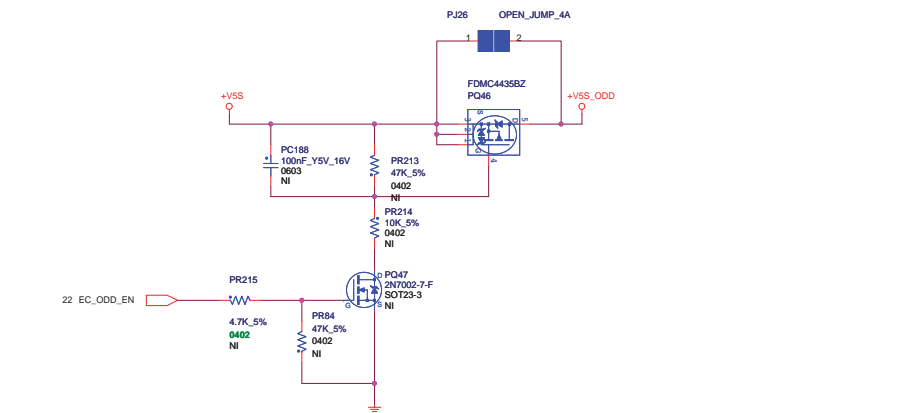
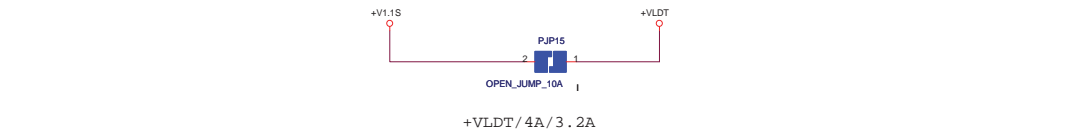
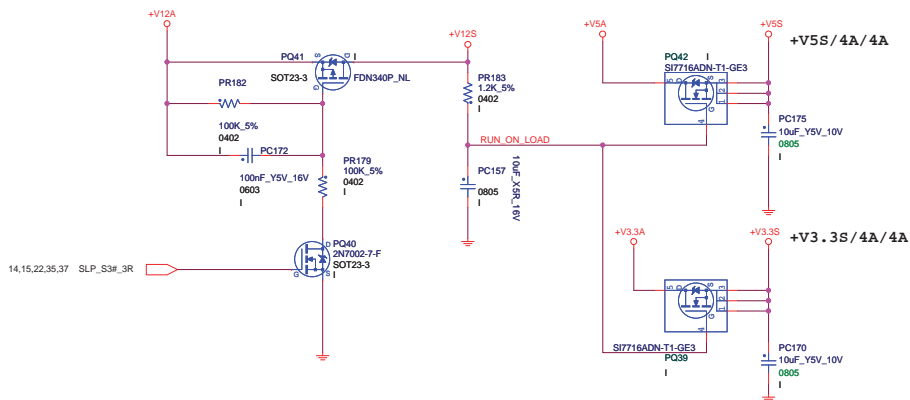
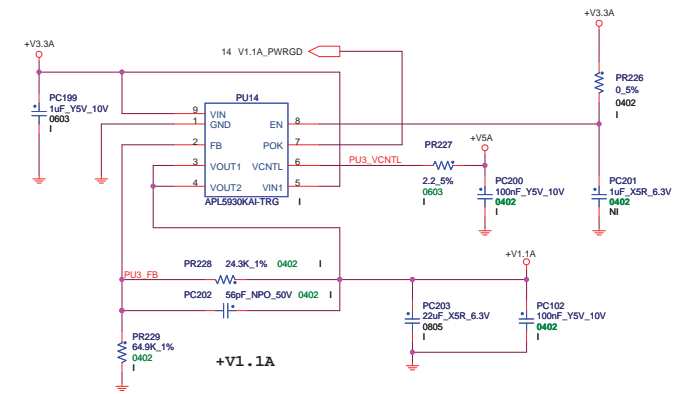
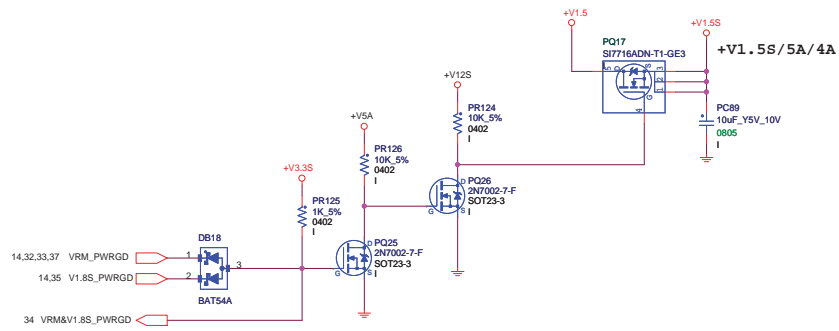
<http://laptop-motherboard-schematic.blogspot.com/>



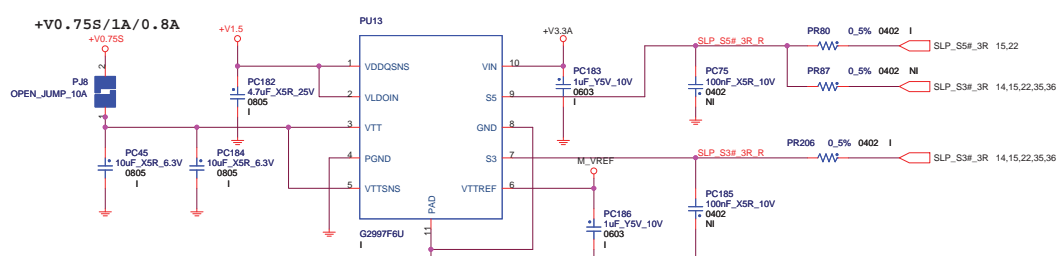
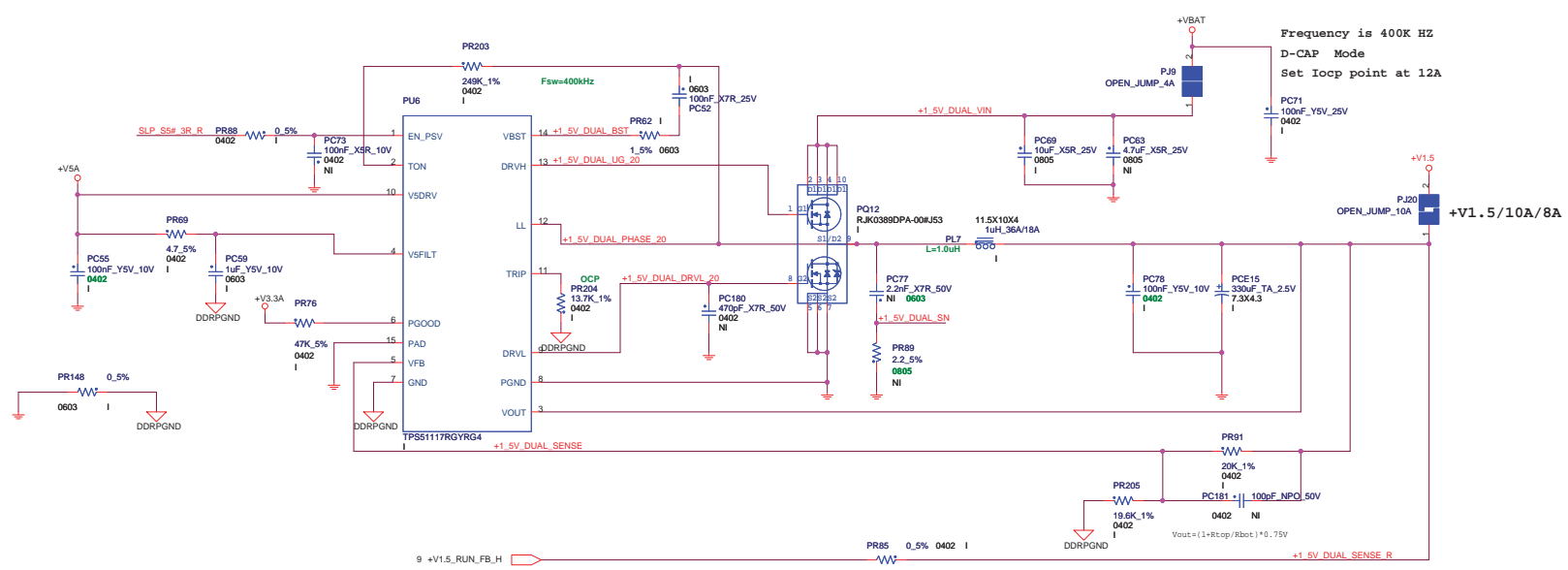
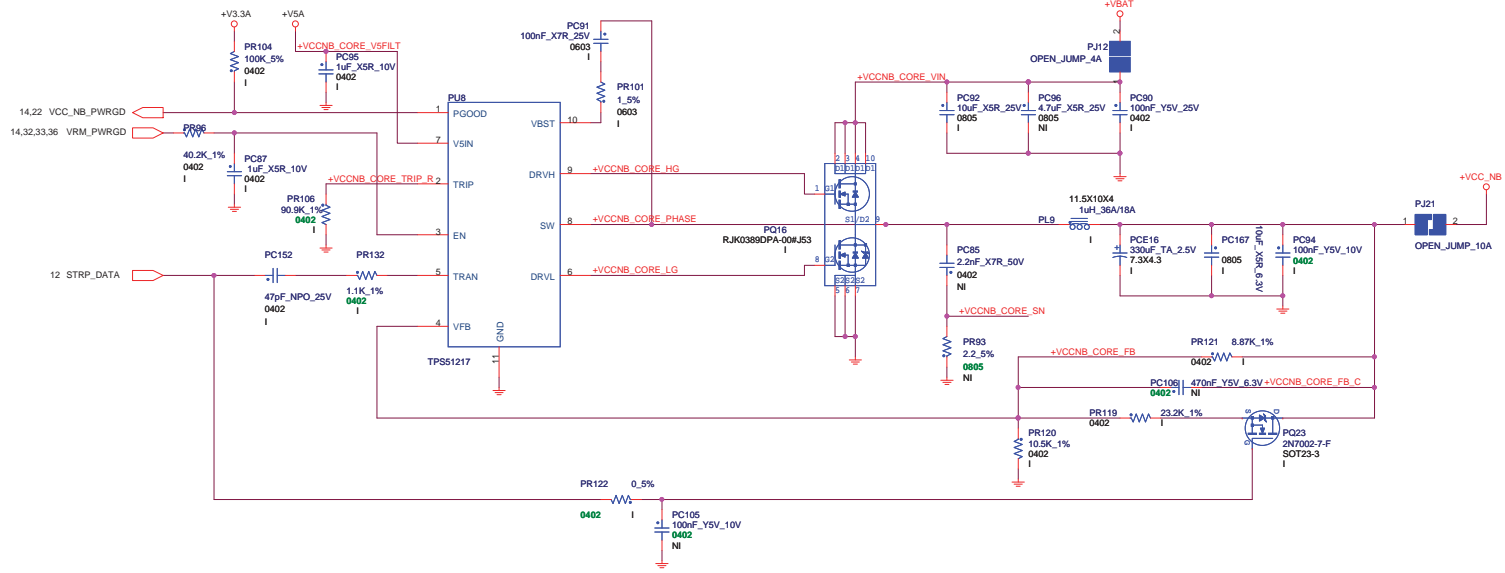
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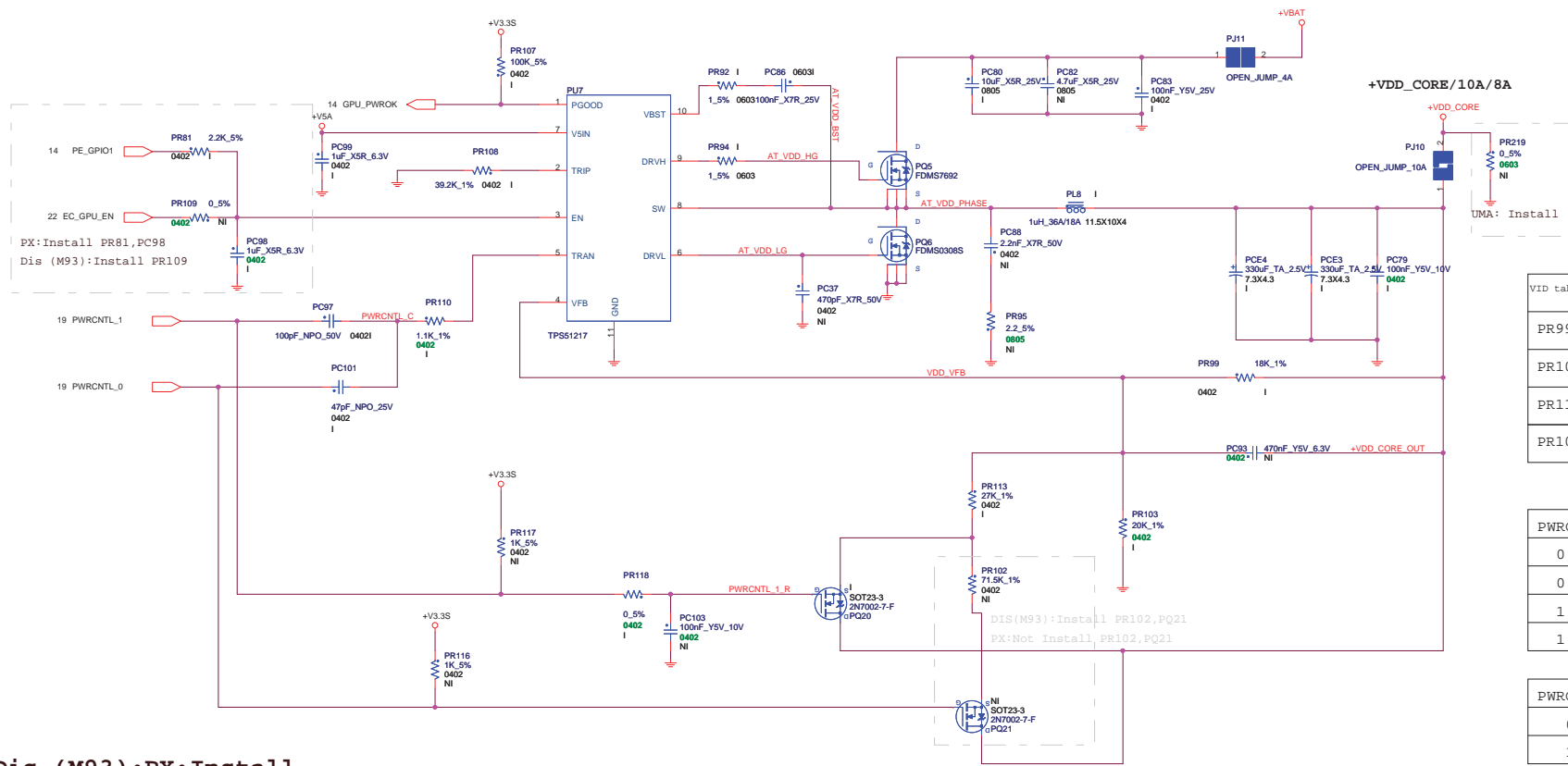
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+VCCNB & 1.5VDDR3 +0.75V	
Title	Rev
Size	MV



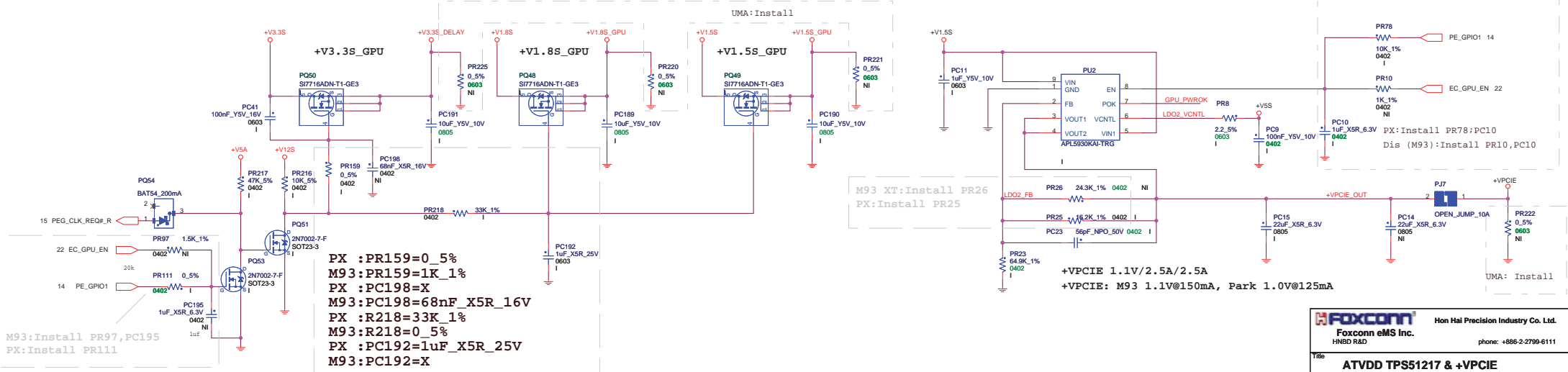
VID table	M93_XT_S3	Park_XT_S3
PR99	20.5K_1% (61011JW00-012-G)	18K_1% (610115W00-012-G)
PR103	20K_1% (610114H00-011-G)	20K_1% (610114H00-011-G)
PR113	28.7K_1% (61011B400-012-G)	27K_1% (610117200-012-G)
PR102	71.5K_1% (611008700-011-G)	N/A

PWRCNTL_1	PWRCNTL_0	M93_XT_S3
0	0	1.2V
0	1	1.1V
1	0	0.95V
1	1	0.9V

PWRCNTL_1	Park_XT_S3
0	1.12V
1	0.9V

Dis (M93);PX:Install
UMA:Not Install

$$V = 0.6 * (1 + R1/R2)$$

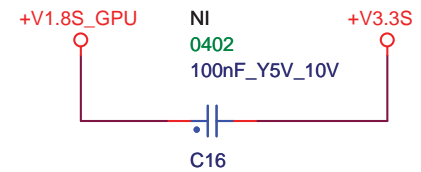
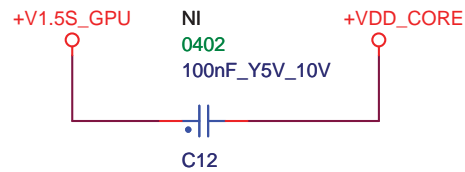
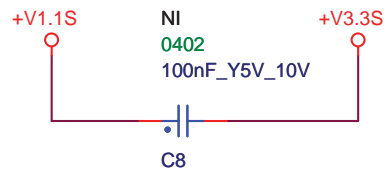
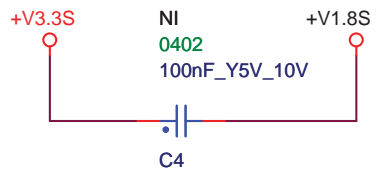
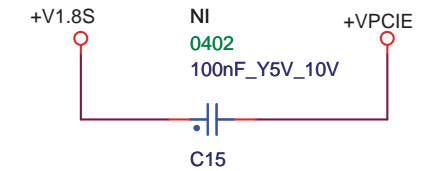
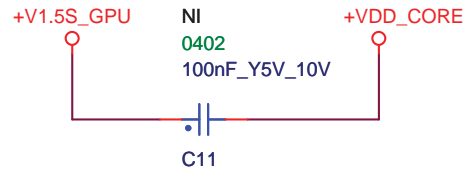
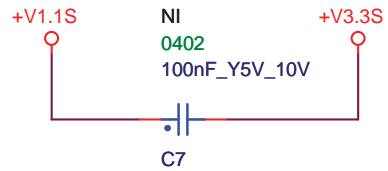
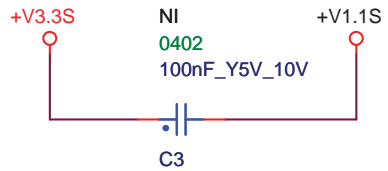
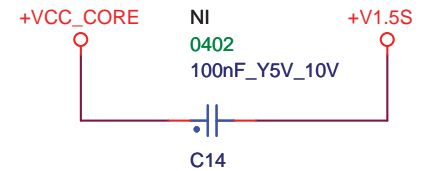
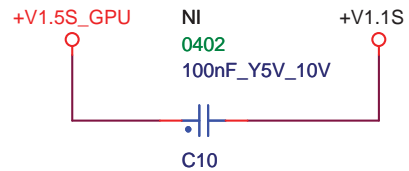
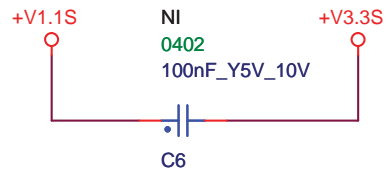
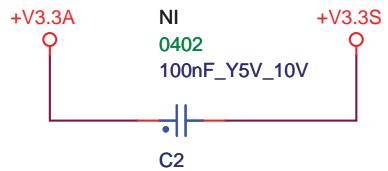
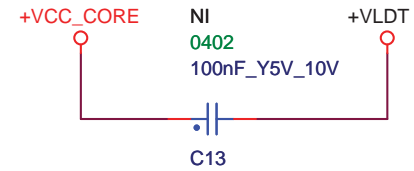
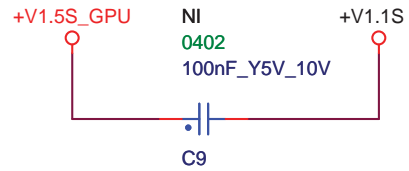
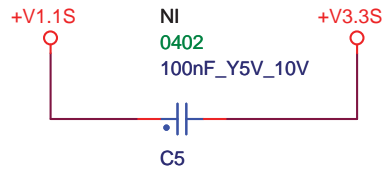
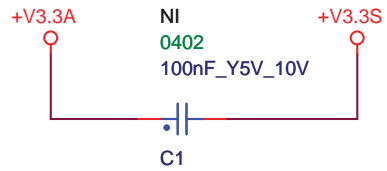


PX :PR159=0.5%
M93:PR159=1K_1%
PX :PC198=X
M93:PC198=68nF_X5R_16V
PX :R218=33K_1%
M93:R218=0.5%
PX :PC192=1uF_X5R_25V
M93:PC192=X

M93 XT:Install PR26
PX:Install PR25

+VPCIE 1.1V/2.5A/2.5A
+VPCIE: M93 1.1V@150mA, Park 1.0V@125mA

M93:Install PR97,PC195
PX:Install PR111



Only for 6 layer M/B use



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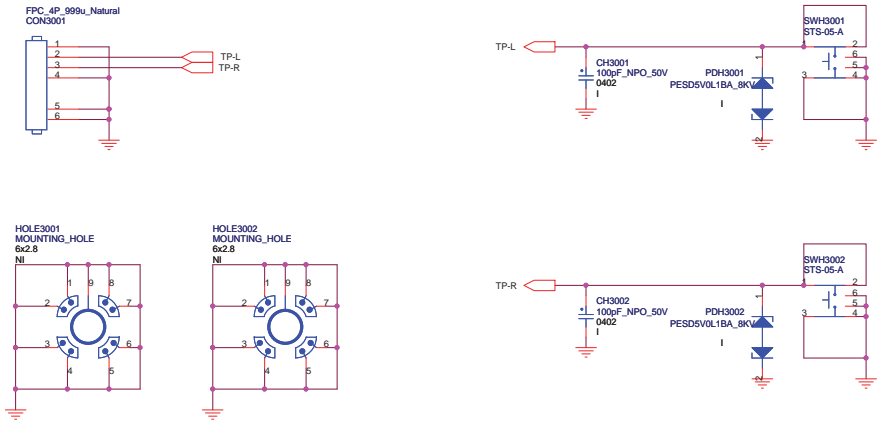
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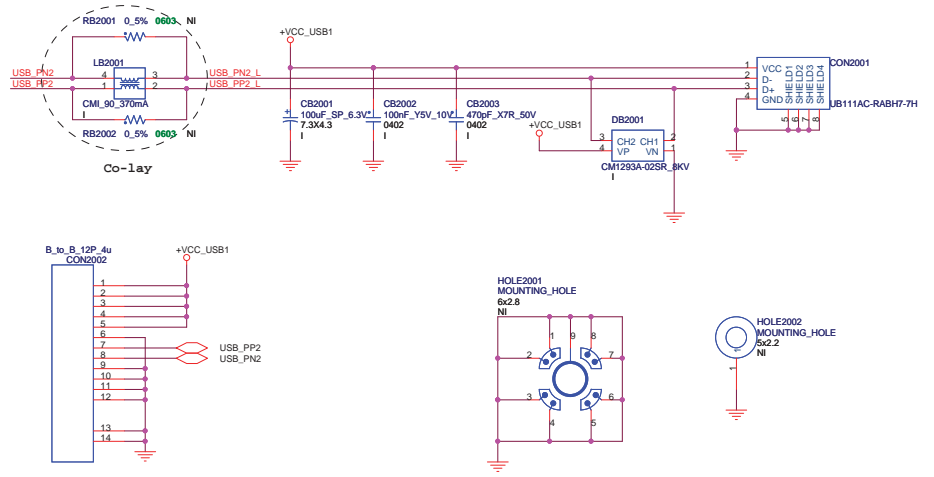
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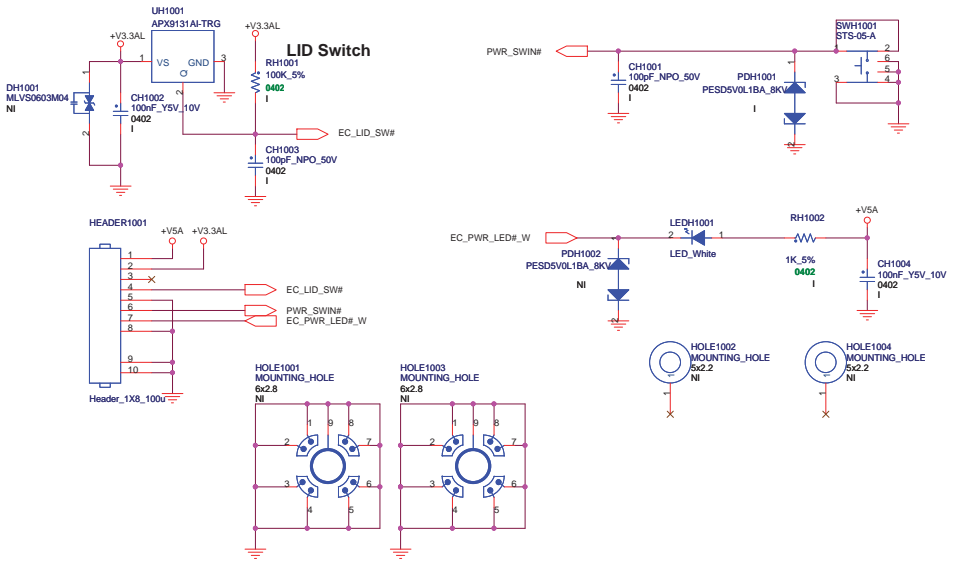
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SW Board



USB Board



Power Board

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