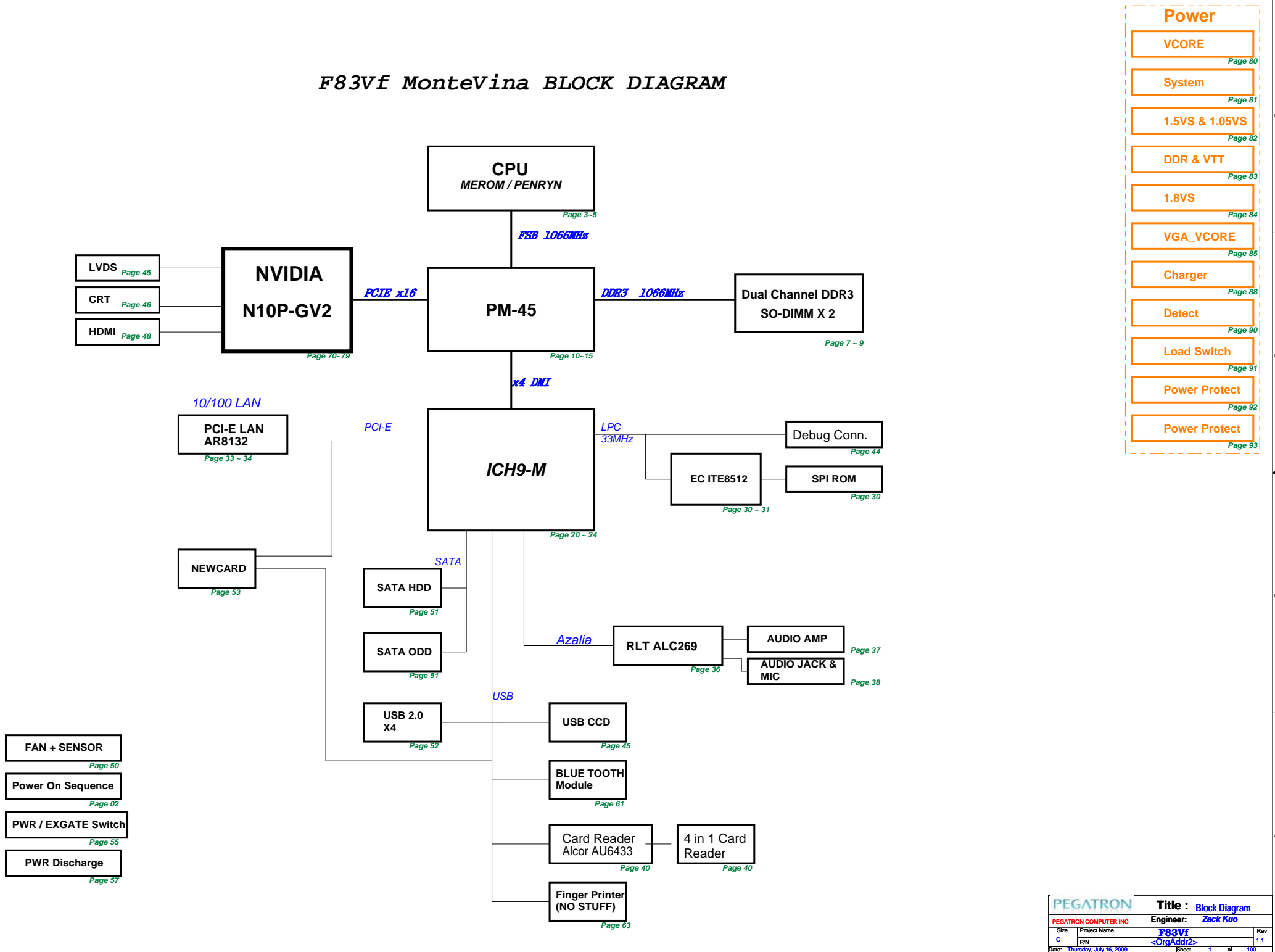
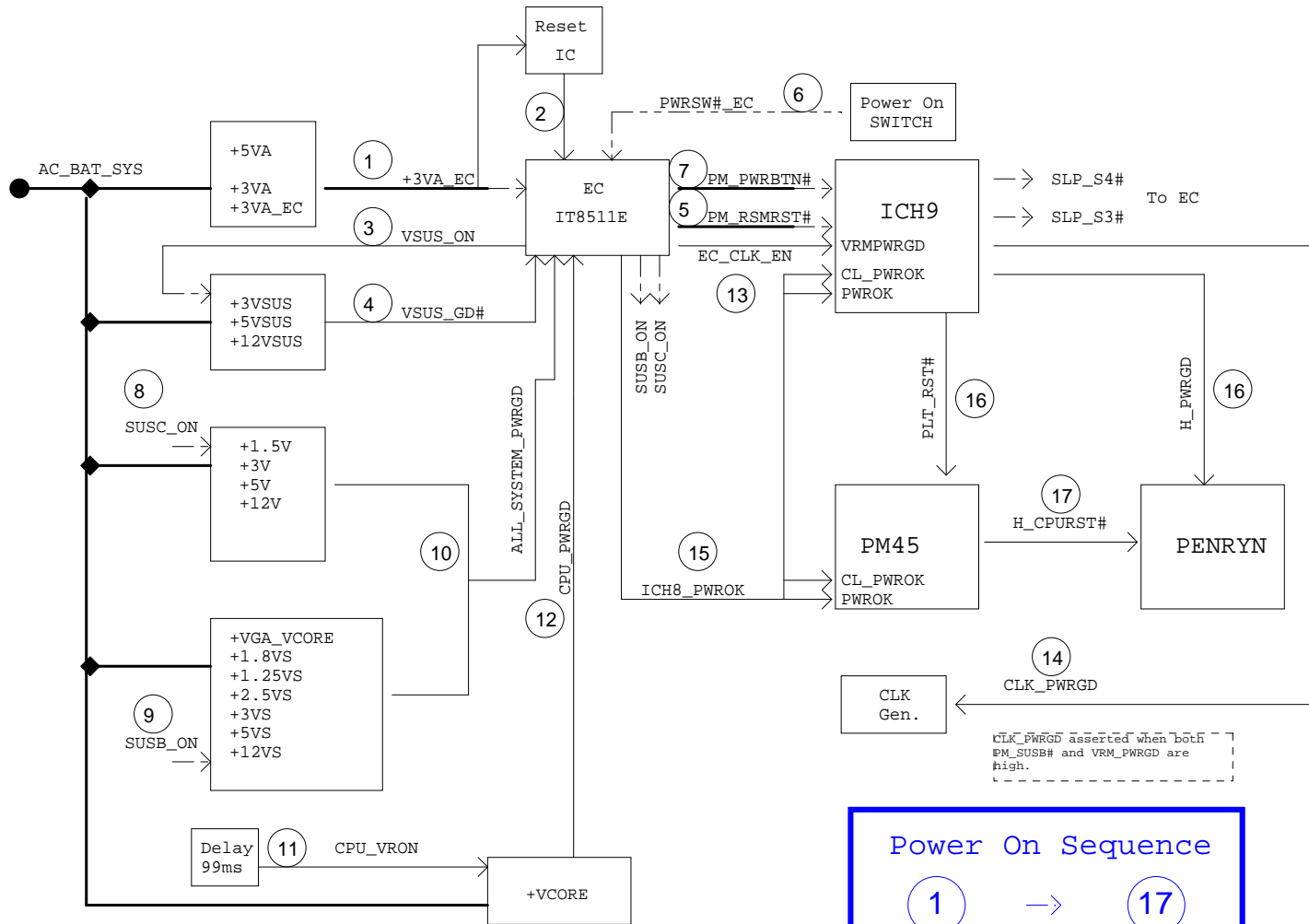


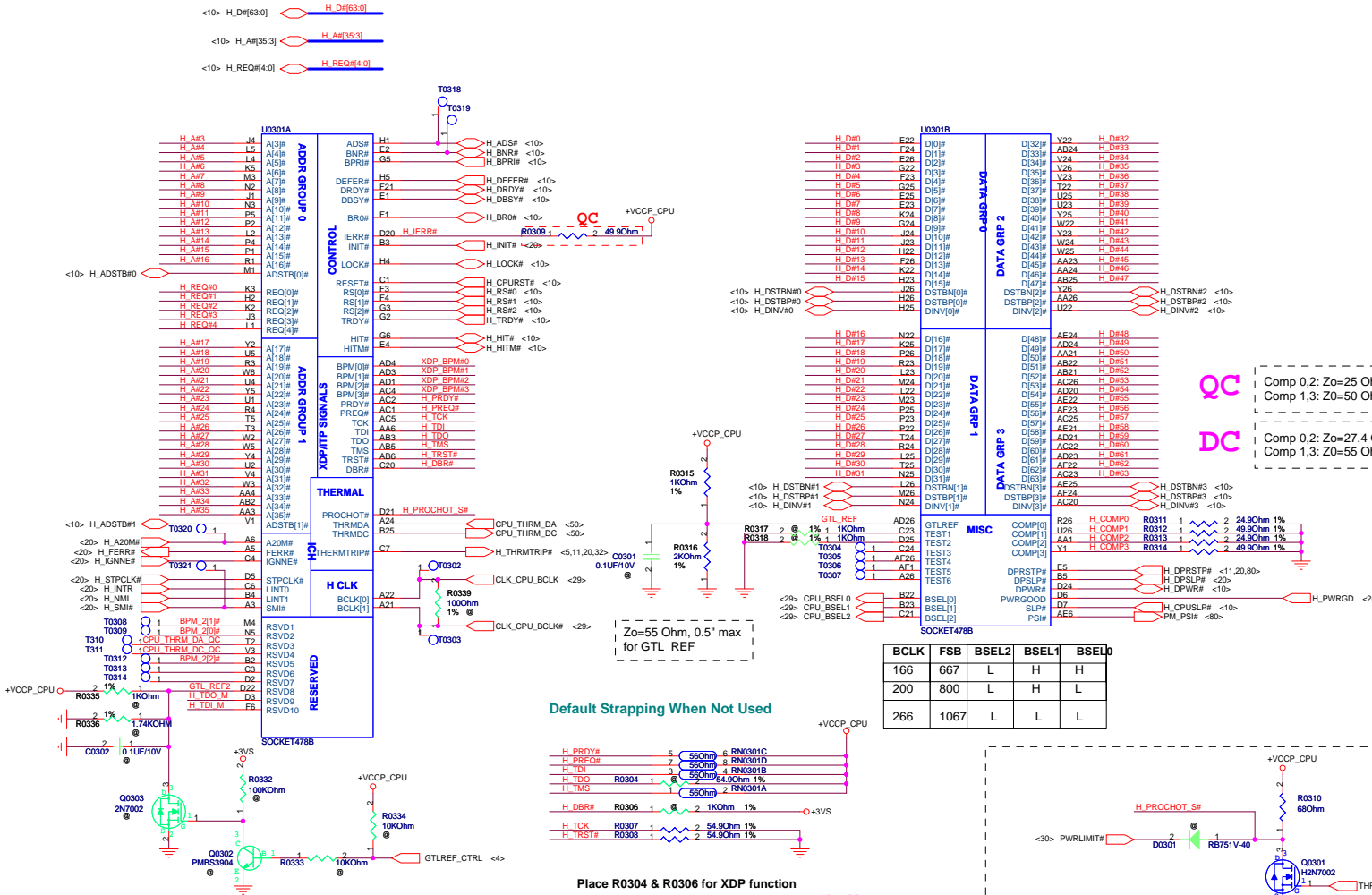
F83Vf MonteVina BLOCK DIAGRAM



- Power**

 - VCORE Page 80
 - System Page 81
 - 1.5VS & 1.05VS Page 82
 - DDR & VTT Page 83
 - 1.8VS Page 84
 - VGA_VCORE Page 85
 - Charger Page 88
 - Detect Page 90
 - Load Switch Page 91
 - Power Protect Page 92
 - Power Protect Page 93

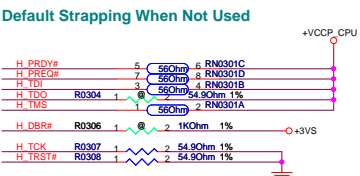




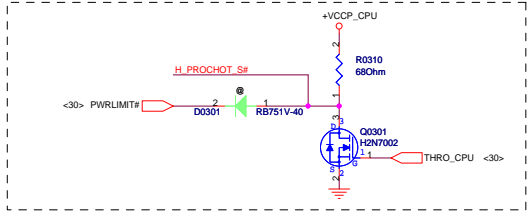
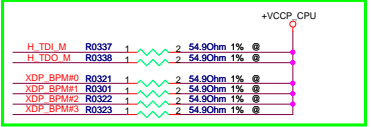
QC Comp 0,2: Zo=25 Ohm, trace length < 0.5"
 Comp 1,3: Zo=50 Ohm, trace length < 0.5"
DC Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
 Comp 1,3: Zo=55 Ohm, trace length < 0.5"

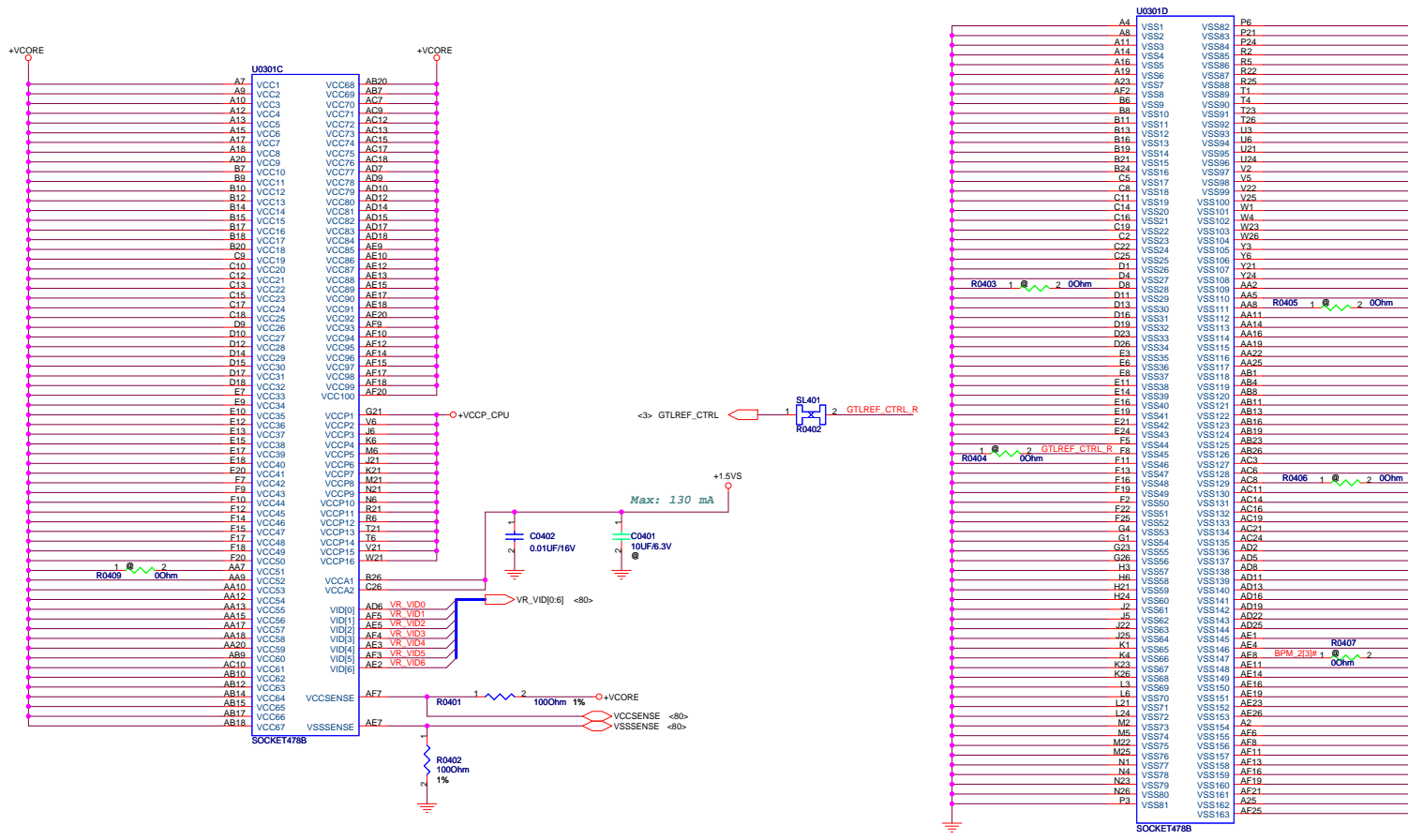
Zo=55 Ohm, 0.5" max
 for GTL_REF

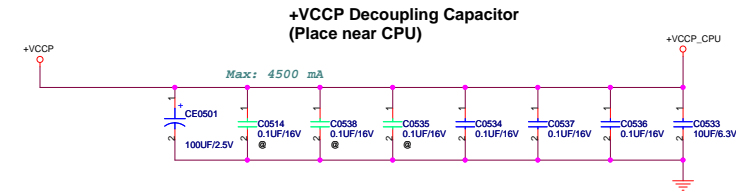
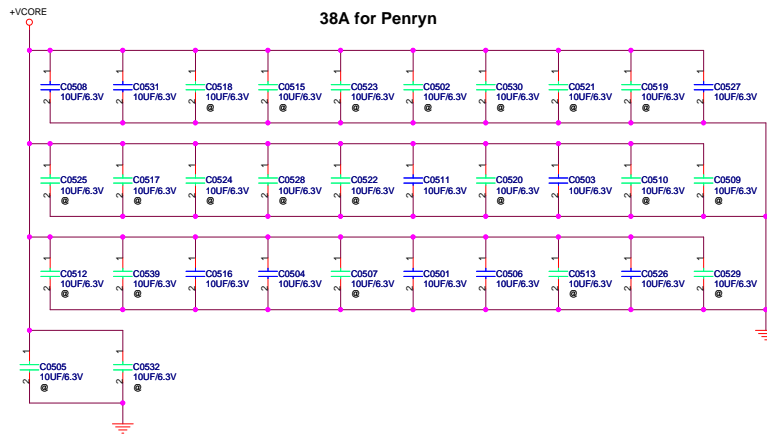
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	H
266	1067	L	L	L



Place R3034 & R3036 for XDP function



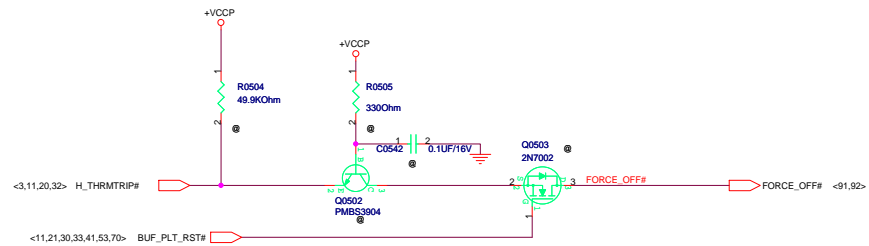




Decoupling guide from Intel

VCCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCCORE Mid-Frequency Capacitor
Intel: 22uF *32
F33V: 10uF *12
+VCCP Decoupling Capacitor
Intel: 270uF *1, 0.1uF *6
F3S: 100uF *1, 0.1uF *3
V1V: ?



Thermal Trip signal (From CPU to ICH-9M and sequence)

5

4

3

2

1

b

b

c

c

b

b

a

a

PEGATRON		Title : CPU_***	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet 6 of 100		

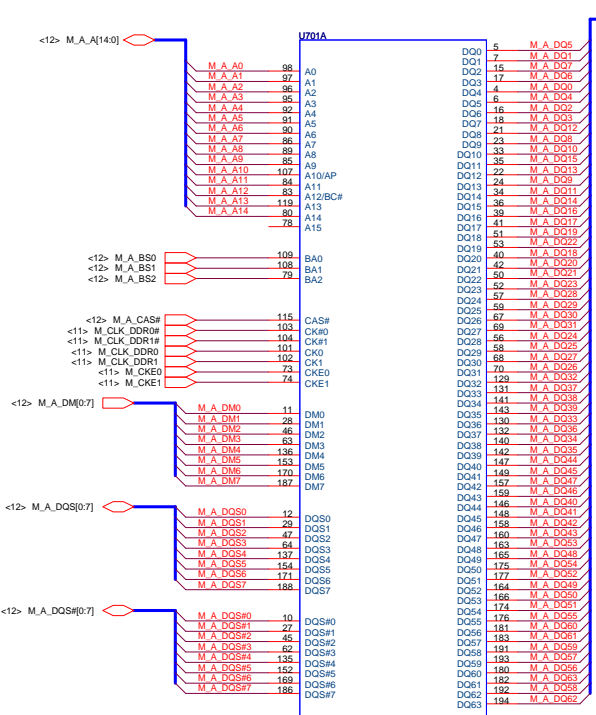
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4

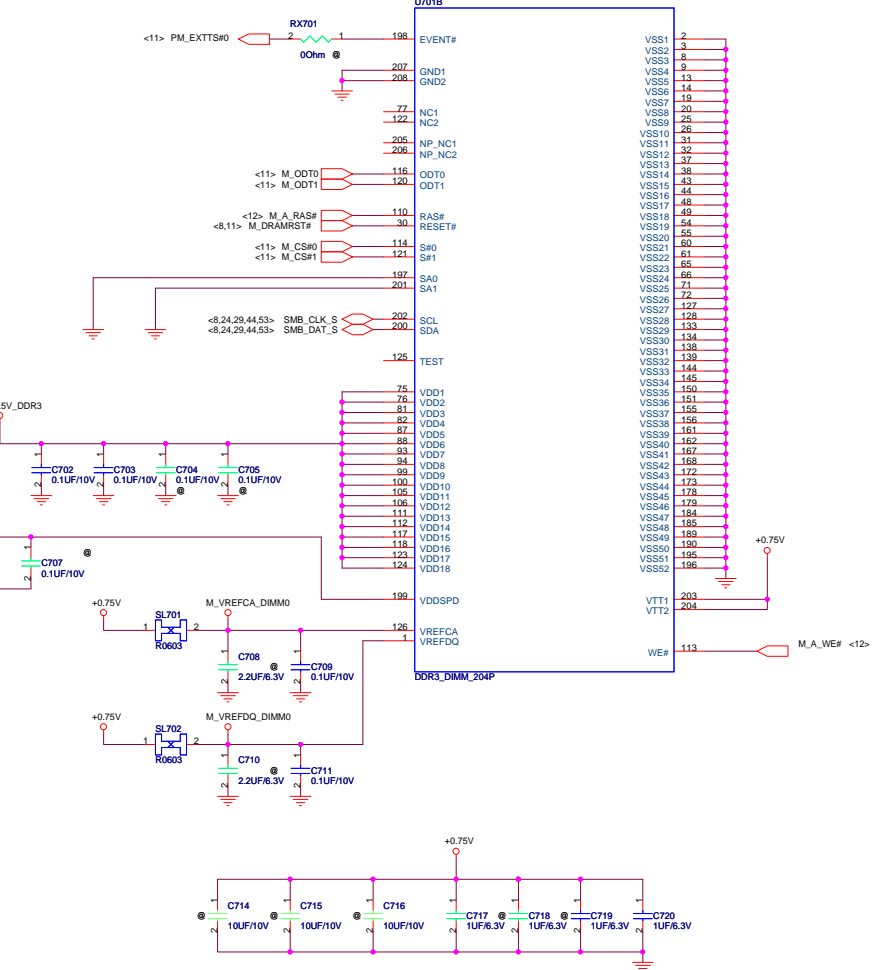
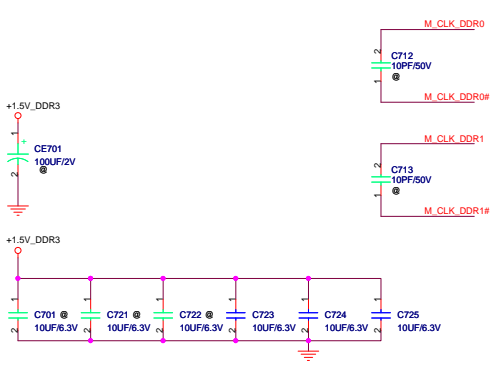
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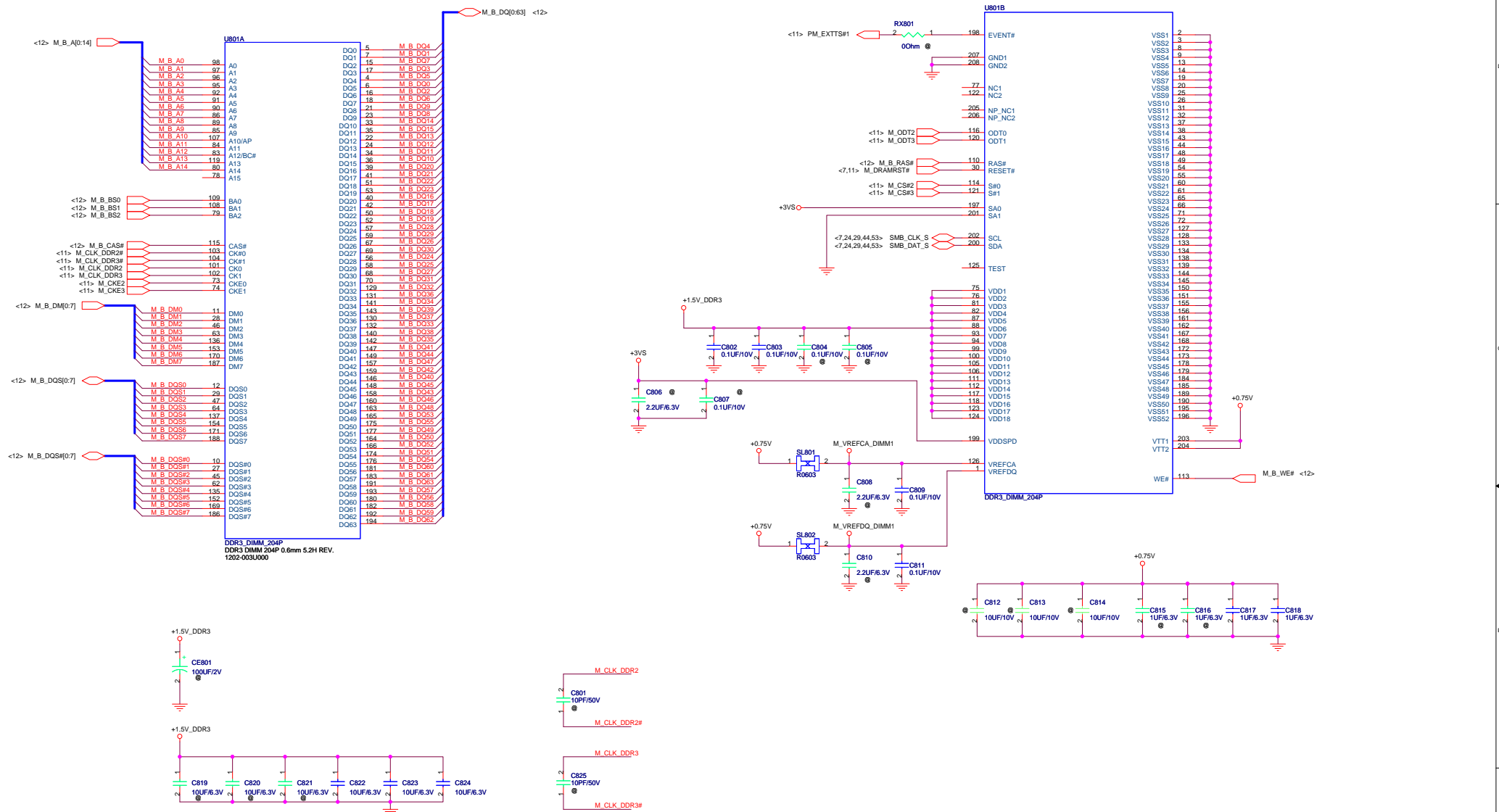
2

1

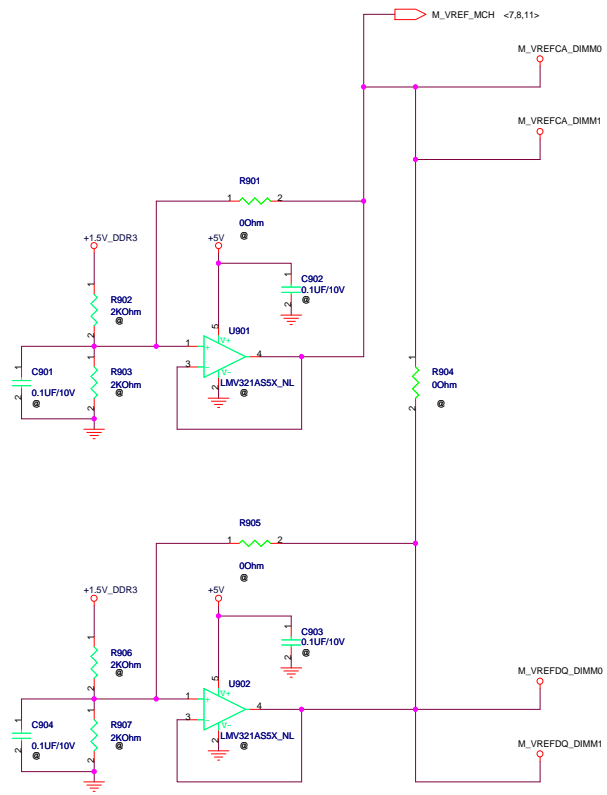


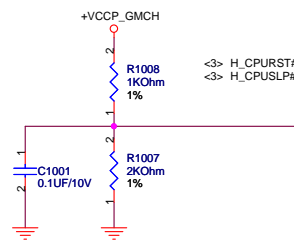
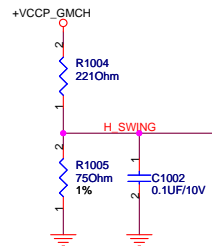
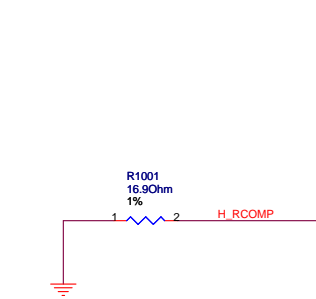
DDR3_DIMM_204P
DDR3 DIMM 204P 0.6mm 9.2H REV
1202-003V000





DDR3_DIMM_204P
DDR3 DIMM 204P 0.6mm 5.2H REV.
1202-003U000





Cap 0.1uF within 100 mils from GMCH

H_D#0	F2	H_D#_0
H_D#1	G8	H_D#_1
H_D#2	F8	H_D#_2
H_D#3	G2	H_D#_3
H_D#4	E6	H_D#_4
H_D#5	H6	H_D#_5
H_D#6	H2	H_D#_6
H_D#7	F6	H_D#_7
H_D#8	D4	H_D#_8
H_D#9	H3	H_D#_9
H_D#10	M9	H_D#_10
H_D#11	M11	H_D#_11
H_D#12	J1	H_D#_12
H_D#13	J2	H_D#_13
H_D#14	N12	H_D#_14
H_D#15	J6	H_D#_15
H_D#16	P2	H_D#_16
H_D#17	L2	H_D#_17
H_D#18	R2	H_D#_18
H_D#19	NG	H_D#_19
H_D#20	L6	H_D#_20
H_D#21	M5	H_D#_21
H_D#22	J3	H_D#_22
H_D#23	N2	H_D#_23
H_D#24	R1	H_D#_24
H_D#25	N5	H_D#_25
H_D#26	N6	H_D#_26
H_D#27	P13	H_D#_27
H_D#28	NG	H_D#_28
H_D#29	LZ	H_D#_29
H_D#30	N10	H_D#_30
H_D#31	M3	H_D#_31
H_D#32	Y3	H_D#_32
H_D#33	AD14	H_D#_33
H_D#34	Y6	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	Y12	H_D#_36
H_D#37	Y14	H_D#_37
H_D#38	VZ	H_D#_38
H_D#39	W2	H_D#_39
H_D#40	AA8	H_D#_40
H_D#41	Y9	H_D#_41
H_D#42	AA13	H_D#_42
H_D#43	AA9	H_D#_43
H_D#44	AA11	H_D#_44
H_D#45	AD11	H_D#_45
H_D#46	AD10	H_D#_46
H_D#47	AD13	H_D#_47
H_D#48	AE12	H_D#_48
H_D#49	AE9	H_D#_49
H_D#50	AA2	H_D#_50
H_D#51	AD8	H_D#_51
H_D#52	AA3	H_D#_52
H_D#53	AD3	H_D#_53
H_D#54	AD7	H_D#_54
H_D#55	AE14	H_D#_55
H_D#56	AF3	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AE3	H_D#_58
H_D#59	AC3	H_D#_59
H_D#60	AE11	H_D#_60
H_D#61	AE8	H_D#_61
H_D#62	AG2	H_D#_62
H_D#63	AD6	H_D#_63

H_SWING C5
H_RCOMP E3

H_CPURST# C12
H_CPUSLP# E11

H_AVREF A11
H_DVREF B11

CANTIGA_CHIPSET

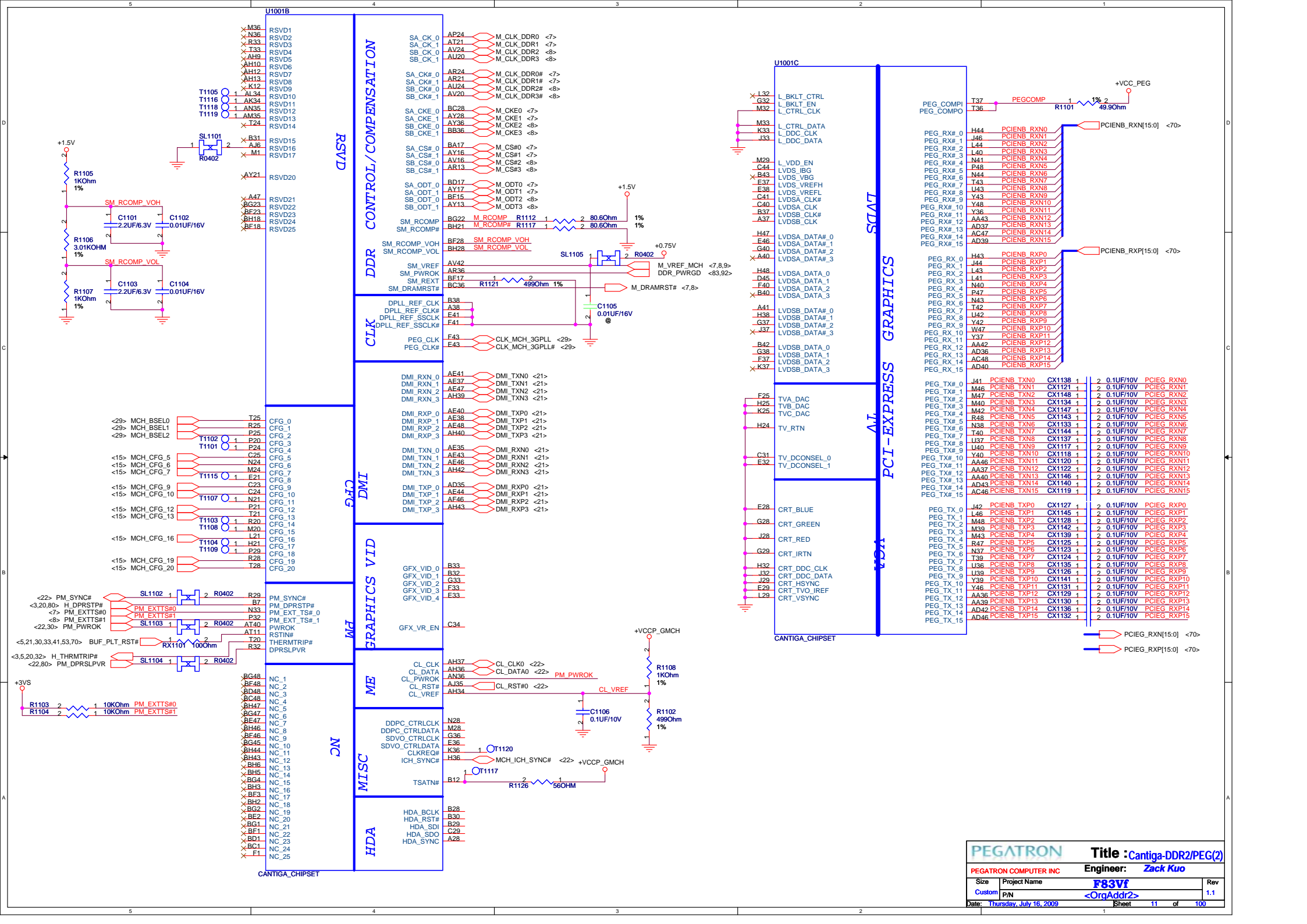
HOST

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	F17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	J16	H_A#18
H_A#_19	E20	H_A#19
H_A#_20	H16	H_A#20
H_A#_21	J20	H_A#21
H_A#_22	L17	H_A#22
H_A#_23	A17	H_A#23
H_A#_24	B17	H_A#24
H_A#_25	L16	H_A#25
H_A#_26	C21	H_A#26
H_A#_27	J17	H_A#27
H_A#_28	H20	H_A#28
H_A#_29	B18	H_A#29
H_A#_30	K17	H_A#30
H_A#_31	B20	H_A#31
H_A#_32	F21	H_A#32
H_A#_33	K21	H_A#33
H_A#_34	L20	H_A#34
H_A#_35	L20	H_A#35
H_ADS#	H12	H_ADS# <3>
H_ADSTB#_0	B16	H_ADSTB#0 <3>
H_ADSTB#_1	G17	H_ADSTB#1 <3>
H_BNR#	A9	H_BNR# <3>
H_BPRI#	E11	H_BPRI# <3>
H_BREQ#	G12	H_BREQ# <3>
H_BRD#	E3	H_BRD# <3>
H_DEFER#	B10	H_DEFER# <3>
H_DBSY#	AH7	H_DBSY# <3>
HPDLL_CLK#	AH6	CLK MCH_BCLK# <29>
HPDLL_CLK#	AH6	CLK MCH_BCLK# <29>
H_DPWR#	J11	H_DPWR# <3>
H_DRDY#	F8	H_DRDY# <3>
H_HIT#	H9	H_HIT# <3>
H_HITM#	E12	H_HITM# <3>
H_LOCK#	H11	H_LOCK# <3>
H_TRDY#	G9	H_TRDY# <3>
H_DIN#_0	J8	H_DIN#0 <3>
H_DIN#_1	L3	H_DIN#1 <3>
H_DIN#_2	Y13	H_DIN#2 <3>
H_DIN#_3	Y1	H_DIN#3 <3>
H_DSTBN#_0	L10	H_DSTBN#0 <3>
H_DSTBN#_1	M7	H_DSTBN#1 <3>
H_DSTBN#_2	AA5	H_DSTBN#2 <3>
H_DSTBN#_3	AE6	H_DSTBN#3 <3>
H_DSTBP#_0	L9	H_DSTBP#0 <3>
H_DSTBP#_1	M8	H_DSTBP#1 <3>
H_DSTBP#_2	AA6	H_DSTBP#2 <3>
H_DSTBP#_3	AE5	H_DSTBP#3 <3>
H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	E13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4
H_RS#_0	B6	H_RS#0 <3>
H_RS#_1	E12	H_RS#1 <3>
H_RS#_2	C8	H_RS#2 <3>

<3> H_A#[35:3] H_A#[35:3]

<3> H_REQ#[4:0] H_REQ#[4:0]

<3> H_D#[63:0] H_D#[63:0]

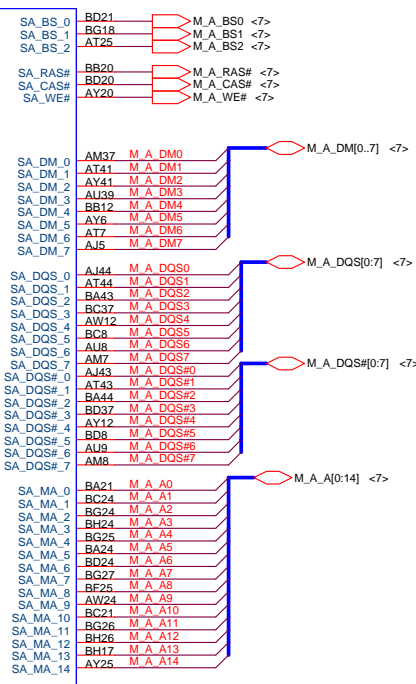


<7> M_A_DQ[0:63]

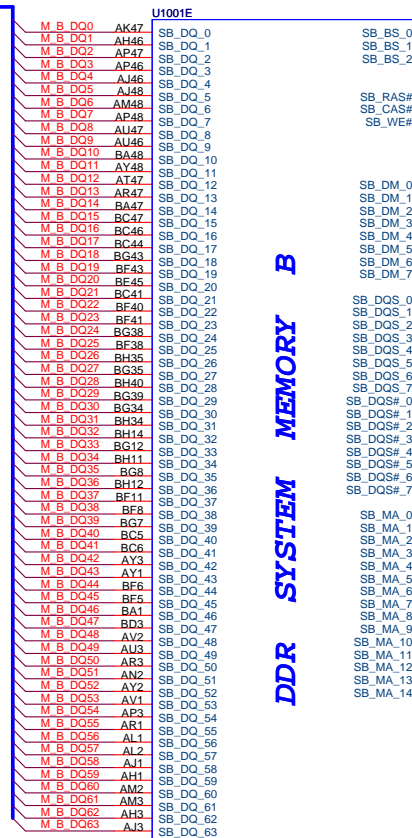


DDR SYSTEM MEMORY A

CANTIGA_CHIPSET

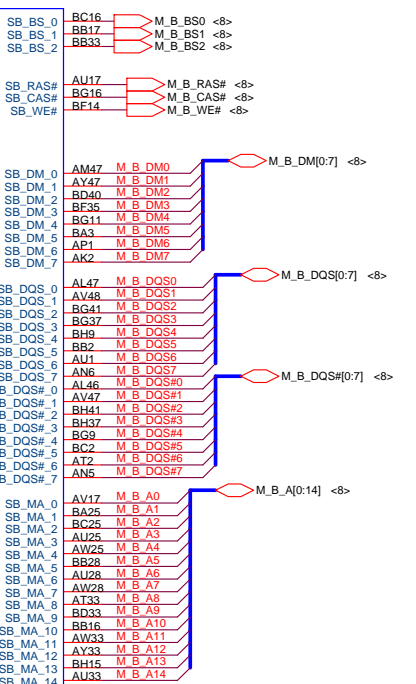


<8> M_B_DQ[0:63]



DDR SYSTEM MEMORY B

CANTIGA_CHIPSET



+1.5V_GMCH

U1001G

- AP33 VCC_SM_1
- BH32 VCC_SM_2
- BG32 VCC_SM_3
- BF32 VCC_SM_4
- BD32 VCC_SM_5
- BC32 VCC_SM_6
- BA32 VCC_SM_7
- AY32 VCC_SM_8
- AW32 VCC_SM_9
- AV32 VCC_SM_10
- AU32 VCC_SM_11
- AT32 VCC_SM_12
- AR32 VCC_SM_13
- AP32 VCC_SM_14
- AN32 VCC_SM_15
- BH31 VCC_SM_16
- BG31 VCC_SM_17
- BF31 VCC_SM_18
- BD31 VCC_SM_19
- BC31 VCC_SM_20
- BA31 VCC_SM_21
- AY31 VCC_SM_22
- AW31 VCC_SM_23
- AV31 VCC_SM_24
- AU31 VCC_SM_25
- AT31 VCC_SM_26
- AR31 VCC_SM_27
- AP31 VCC_SM_28
- AN31 VCC_SM_29
- BH30 VCC_SM_30
- BG30 VCC_SM_31
- BF30 VCC_SM_32
- BD30 VCC_SM_33
- BC30 VCC_SM_34
- BA30 VCC_SM_35

VCC SM POWER

VCC SM

- Y26 VCC_AXG_1
- AE25 VCC_AXG_2
- AB25 VCC_AXG_3
- AA25 VCC_AXG_4
- AE24 VCC_AXG_5
- AC24 VCC_AXG_6
- AA24 VCC_AXG_7
- Y24 VCC_AXG_8
- AE23 VCC_AXG_9
- AC23 VCC_AXG_10
- AB23 VCC_AXG_11
- AA23 VCC_AXG_12
- AJ21 VCC_AXG_13
- AG21 VCC_AXG_14
- AE21 VCC_AXG_15
- AC21 VCC_AXG_16
- AA21 VCC_AXG_17
- Y21 VCC_AXG_18
- AH20 VCC_AXG_19
- AE20 VCC_AXG_20
- AE20 VCC_AXG_21
- AB20 VCC_AXG_22
- AA20 VCC_AXG_23
- T17 VCC_AXG_24
- T16 VCC_AXG_25
- AM15 VCC_AXG_26
- AL15 VCC_AXG_27
- AE15 VCC_AXG_28
- AJ15 VCC_AXG_29
- AH15 VCC_AXG_30
- AG15 VCC_AXG_31
- AF15 VCC_AXG_32
- AB15 VCC_AXG_33
- AA15 VCC_AXG_34
- Y15 VCC_AXG_35
- V15 VCC_AXG_36
- U15 VCC_AXG_37
- AN14 VCC_AXG_38
- AM14 VCC_AXG_39
- U14 VCC_AXG_40
- T14 VCC_AXG_41
- T14 VCC_AXG_42

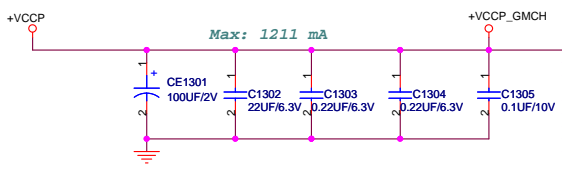
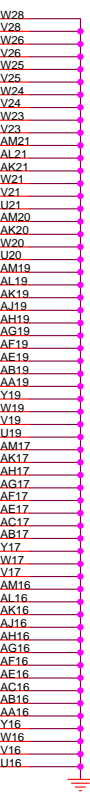
VCC GFX NCTF

VCC GFX

- VCC_AXG_NCTF_1 W28
- VCC_AXG_NCTF_2 V28
- VCC_AXG_NCTF_3 W26
- VCC_AXG_NCTF_4 W25
- VCC_AXG_NCTF_5 V25
- VCC_AXG_NCTF_6 W24
- VCC_AXG_NCTF_7 V24
- VCC_AXG_NCTF_8 W23
- VCC_AXG_NCTF_9 V23
- VCC_AXG_NCTF_10 AM21
- VCC_AXG_NCTF_11 AL21
- VCC_AXG_NCTF_12 AK21
- VCC_AXG_NCTF_13 W21
- VCC_AXG_NCTF_14 V21
- VCC_AXG_NCTF_15 AM20
- VCC_AXG_NCTF_16 AK20
- VCC_AXG_NCTF_17 W20
- VCC_AXG_NCTF_18 U20
- VCC_AXG_NCTF_19 AM19
- VCC_AXG_NCTF_20 AL19
- VCC_AXG_NCTF_21 AK19
- VCC_AXG_NCTF_22 AJ19
- VCC_AXG_NCTF_23 AH19
- VCC_AXG_NCTF_24 AG19
- VCC_AXG_NCTF_25 AF19
- VCC_AXG_NCTF_26 AE19
- VCC_AXG_NCTF_27 AB19
- VCC_AXG_NCTF_28 AA19
- VCC_AXG_NCTF_29 Y19
- VCC_AXG_NCTF_30 W19
- VCC_AXG_NCTF_31 V19
- VCC_AXG_NCTF_32 U19
- VCC_AXG_NCTF_33 AM17
- VCC_AXG_NCTF_34 AK17
- VCC_AXG_NCTF_35 AL17
- VCC_AXG_NCTF_36 AG17
- VCC_AXG_NCTF_37 AF17
- VCC_AXG_NCTF_38 AE17
- VCC_AXG_NCTF_39 AC17
- VCC_AXG_NCTF_40 AB17
- VCC_AXG_NCTF_41 Y17
- VCC_AXG_NCTF_42 W17
- VCC_AXG_NCTF_43 V17
- VCC_AXG_NCTF_44 AM16
- VCC_AXG_NCTF_45 AL16
- VCC_AXG_NCTF_46 AK16
- VCC_AXG_NCTF_47 AJ16
- VCC_AXG_NCTF_48 AH16
- VCC_AXG_NCTF_49 AG16
- VCC_AXG_NCTF_50 AF16
- VCC_AXG_NCTF_51 AE16
- VCC_AXG_NCTF_52 AC16
- VCC_AXG_NCTF_53 AB16
- VCC_AXG_NCTF_54 AA16
- VCC_AXG_NCTF_55 Y16
- VCC_AXG_NCTF_56 W16
- VCC_AXG_NCTF_57 V16
- VCC_AXG_NCTF_58 U16
- VCC_AXG_NCTF_59
- VCC_AXG_NCTF_60

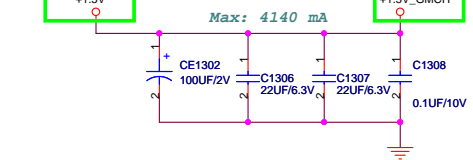
- VCC_SM_LF1 AV44
- VCC_SM_LF2 BA37
- VCC_SM_LF3 AM40
- VCC_SM_LF4 AV21
- VCC_SM_LF5 AY5
- VCC_SM_LF6 AM10
- VCC_SM_LF7 BB13

VCC SM LF



+1.5V

+1.5V_GMCH



U1001F

- AG34 VCC_1
- AC34 VCC_2
- AB34 VCC_3
- AA34 VCC_4
- Y34 VCC_5
- V34 VCC_6
- U34 VCC_7
- AK33 VCC_8
- AJ33 VCC_9
- AG33 VCC_10
- AF33 VCC_11
- AE33 VCC_12
- AC33 VCC_13
- AA33 VCC_14
- Y33 VCC_15
- W33 VCC_16
- V33 VCC_17
- U33 VCC_18
- AH28 VCC_19
- AG28 VCC_20
- AF28 VCC_21
- AC28 VCC_22
- AA28 VCC_23
- AJ26 VCC_24
- AG26 VCC_25
- AE26 VCC_26
- AC26 VCC_27
- AH25 VCC_28
- AG25 VCC_29
- AE25 VCC_30
- AC24 VCC_31
- AJ23 VCC_32
- AH23 VCC_33
- AF23 VCC_34
- T32 VCC_35

VCC CORE

VCC CORE

VCC CORE

VCC NCTF

VCC NCTF

VCC NCTF

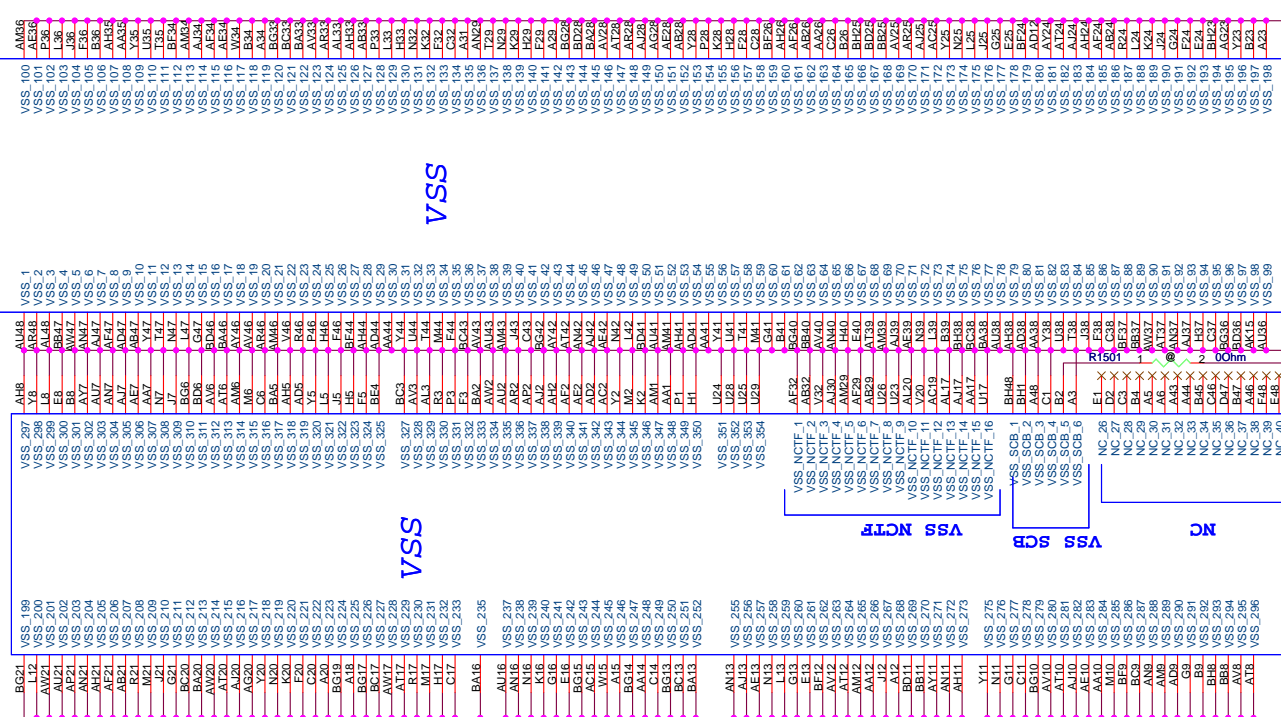
- VCC_NCTF_1 AM32
- VCC_NCTF_2 AL32
- VCC_NCTF_3 AK32
- VCC_NCTF_4 AJ32
- VCC_NCTF_5 AH32
- VCC_NCTF_6 AG32
- VCC_NCTF_7 AE32
- VCC_NCTF_8 AC32
- VCC_NCTF_9 AA32
- VCC_NCTF_10 Y32
- VCC_NCTF_11 W32
- VCC_NCTF_12 V32
- VCC_NCTF_13 U32
- VCC_NCTF_14 AM30
- VCC_NCTF_15 AL30
- VCC_NCTF_16 AK30
- VCC_NCTF_17 AH30
- VCC_NCTF_18 AG30
- VCC_NCTF_19 AE30
- VCC_NCTF_20 AC30
- VCC_NCTF_21 AB30
- VCC_NCTF_22 AA30
- VCC_NCTF_23 Y30
- VCC_NCTF_24 W30
- VCC_NCTF_25 V30
- VCC_NCTF_26 U30
- VCC_NCTF_27 AL29
- VCC_NCTF_28 AK29
- VCC_NCTF_29 AJ29
- VCC_NCTF_30 AH29
- VCC_NCTF_31 AG29
- VCC_NCTF_32 AE29
- VCC_NCTF_33 AC29
- VCC_NCTF_34 AA29
- VCC_NCTF_35 Y29
- VCC_NCTF_36 W29
- VCC_NCTF_37 V29
- VCC_NCTF_38 AL28
- VCC_NCTF_39 AK28
- VCC_NCTF_40 AJ28
- VCC_NCTF_41 AH26
- VCC_NCTF_42 AG26
- VCC_NCTF_43 AK25
- VCC_NCTF_44 AK23

+VCCP_GMCH

T1301 1 AH4
T1302 1 AH4

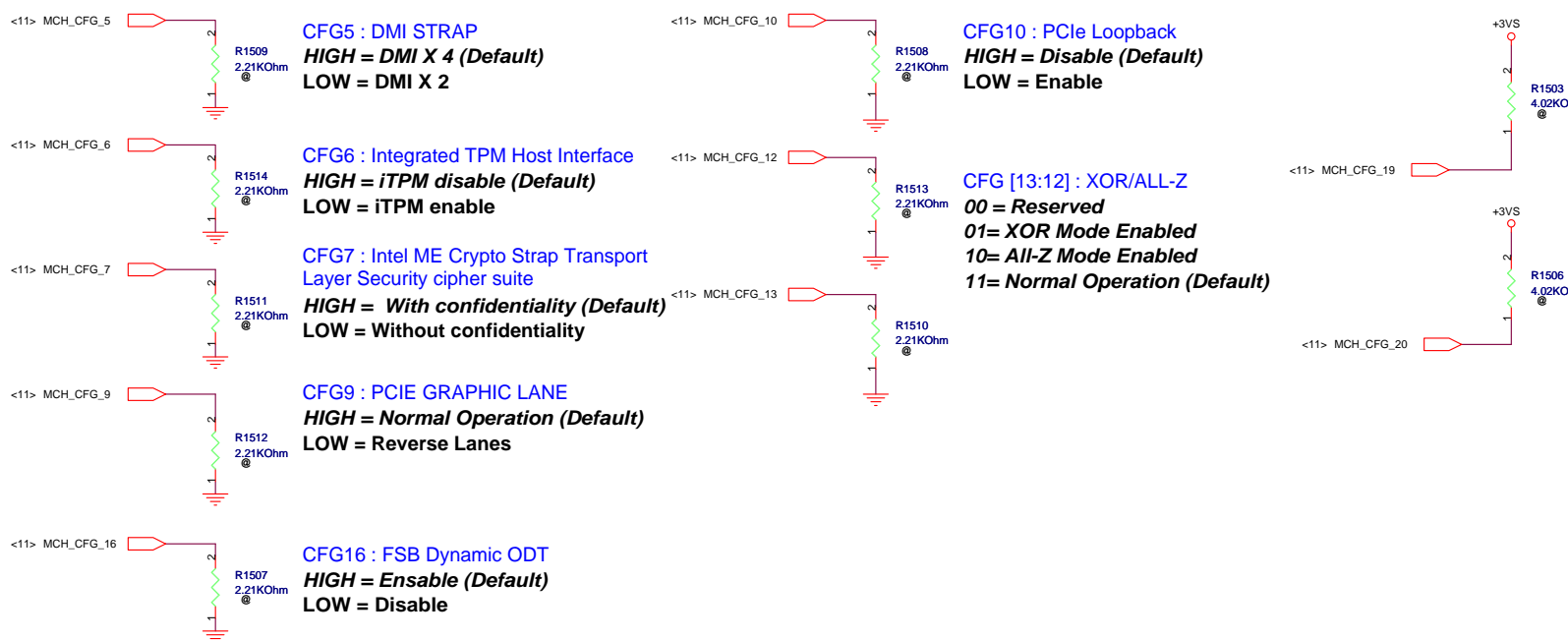
CANTIGA_CHIPSET

CANTIGA_CHIPSET



U1001
CANTIGA_CHIPSET

U1001J
CANTIGA_CHIPSET



CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

CFG9 : PCIE GRAPHIC LANE
HIGH = Normal Operation (Default)
LOW = Reverse Lanes

CFG16 : FSB Dynamic ODT
HIGH = Enable (Default)
LOW = Disable

CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation (Default)

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

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C

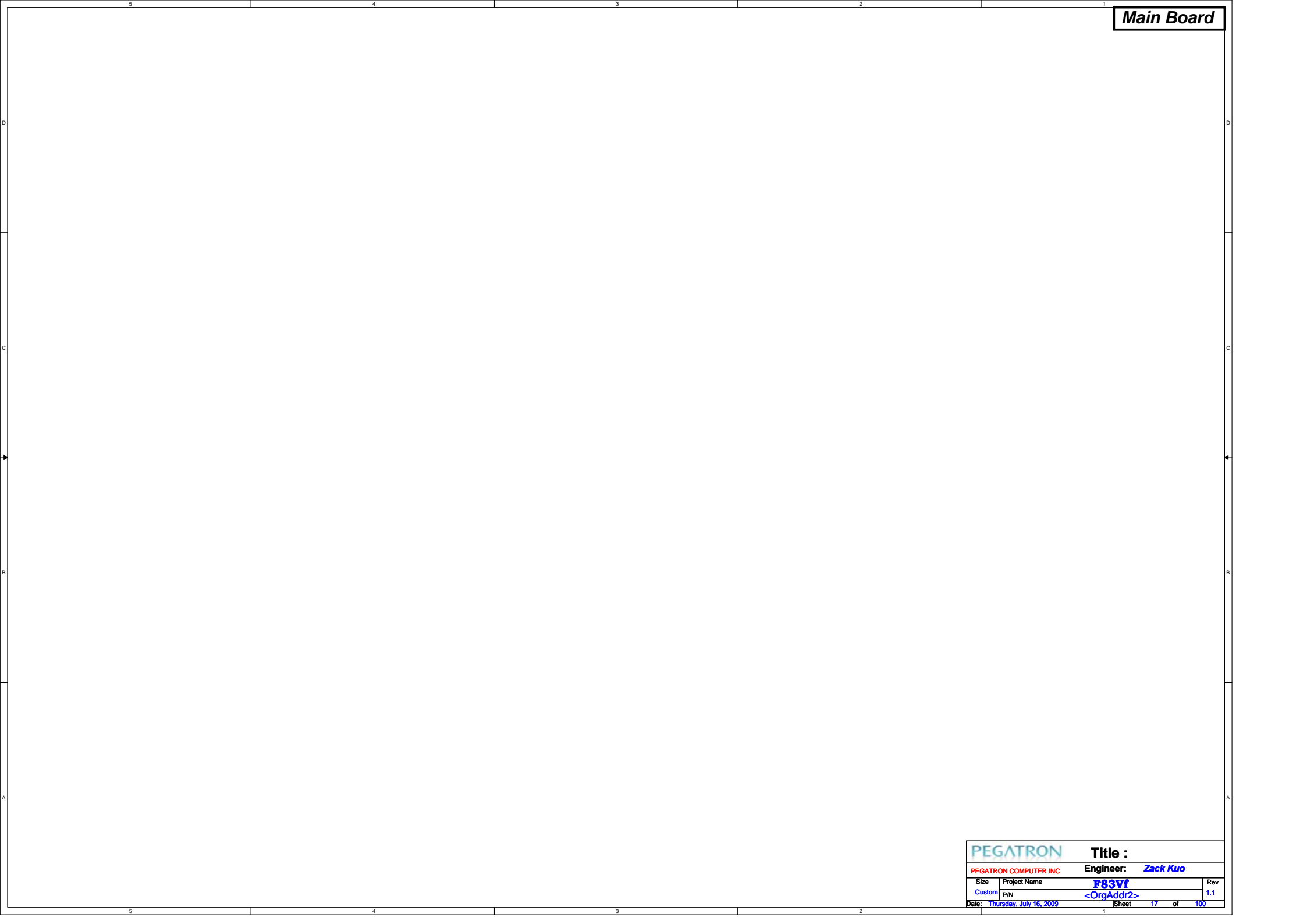
B

B

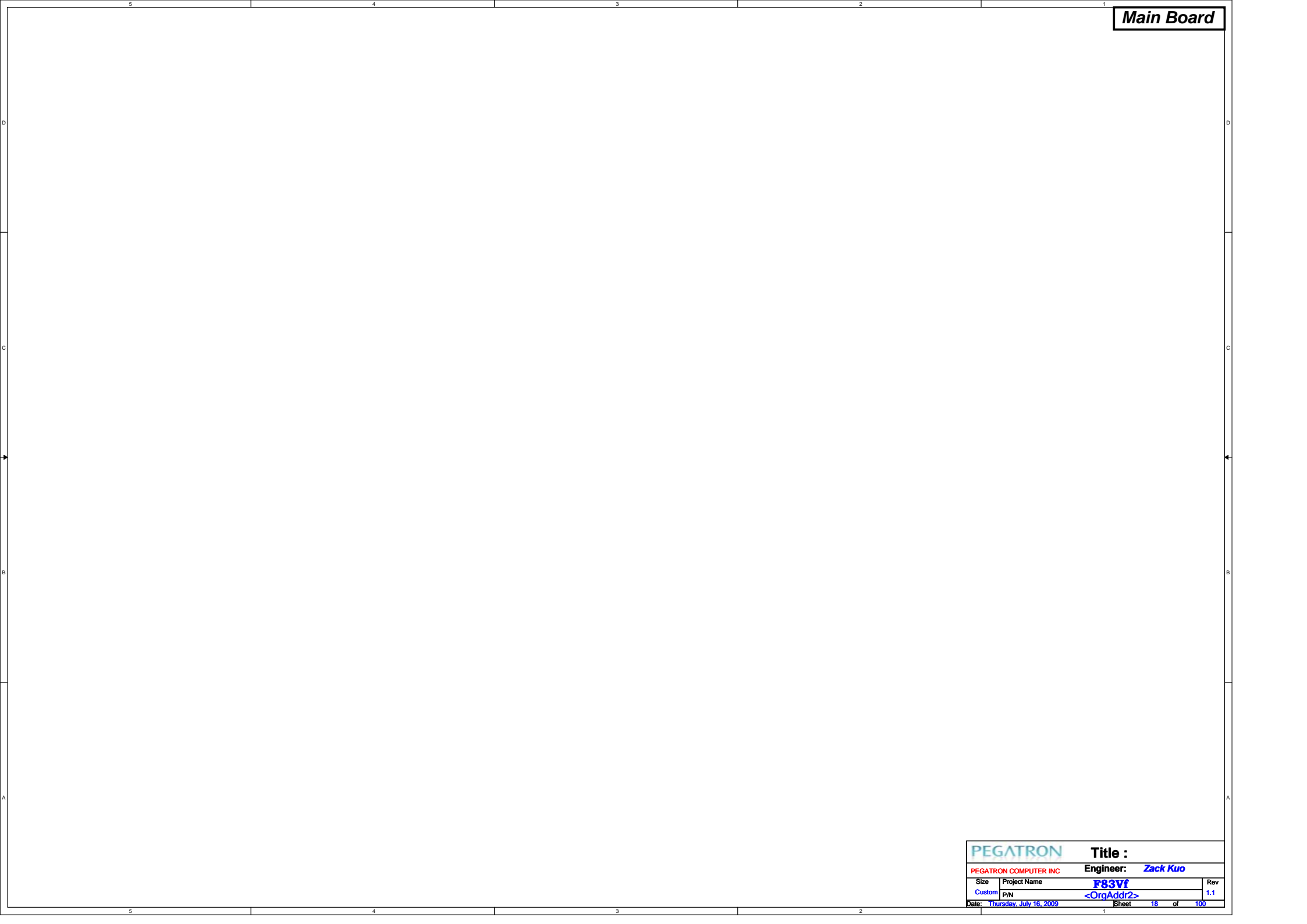
A

A

PEGATRON		Title :	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name		Rev
Custom	P/N	F83Vf	1.1
Date: Thursday, July 16, 2009		<OrgAddr2>	Sheet 16 of 100



PEGATRON		Title :	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrqAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet 17 of 100		



PEGATRON		Title :	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrqAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet		18 of 100

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b

b

c

c

b

b

a

a

PEGATRON		Title :	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet 19 of 100		

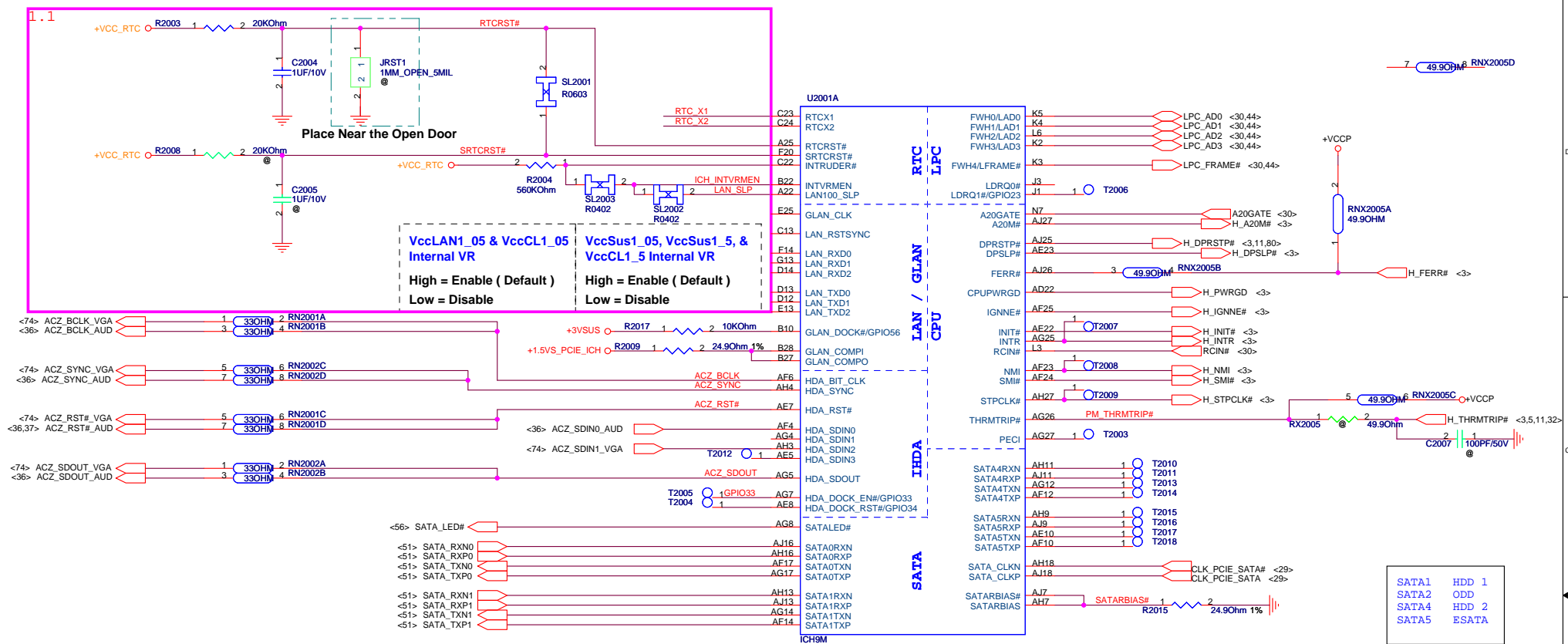
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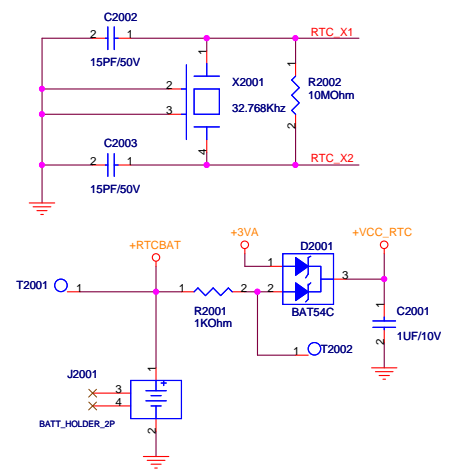


VccLAN1_05 & VccCL1_05 Internal VR
 High = Enable (Default)
 Low = Disable

VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
 High = Enable (Default)
 Low = Disable

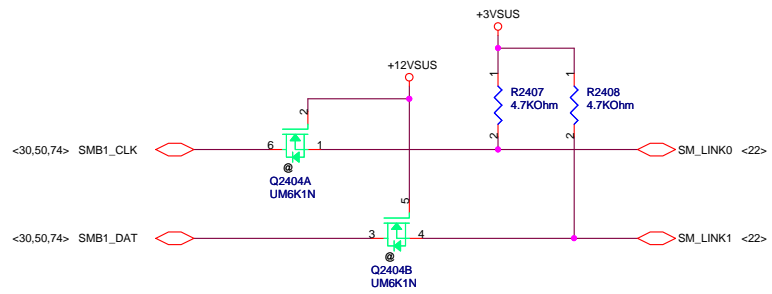
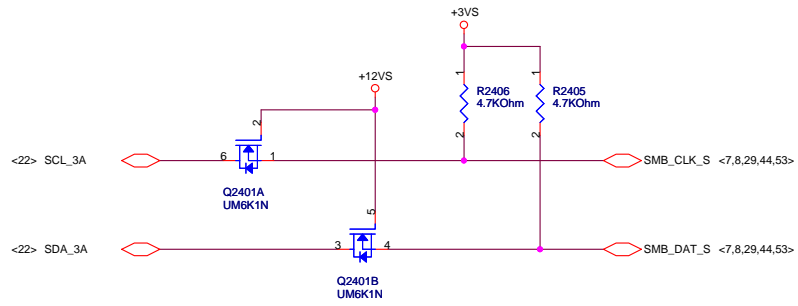
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap

- 00 = Reserved
- 01 = Enter XOR Chain
- 10 = Normal Operation (Default)
- 11 = Set PCIe Port Config Bit 1

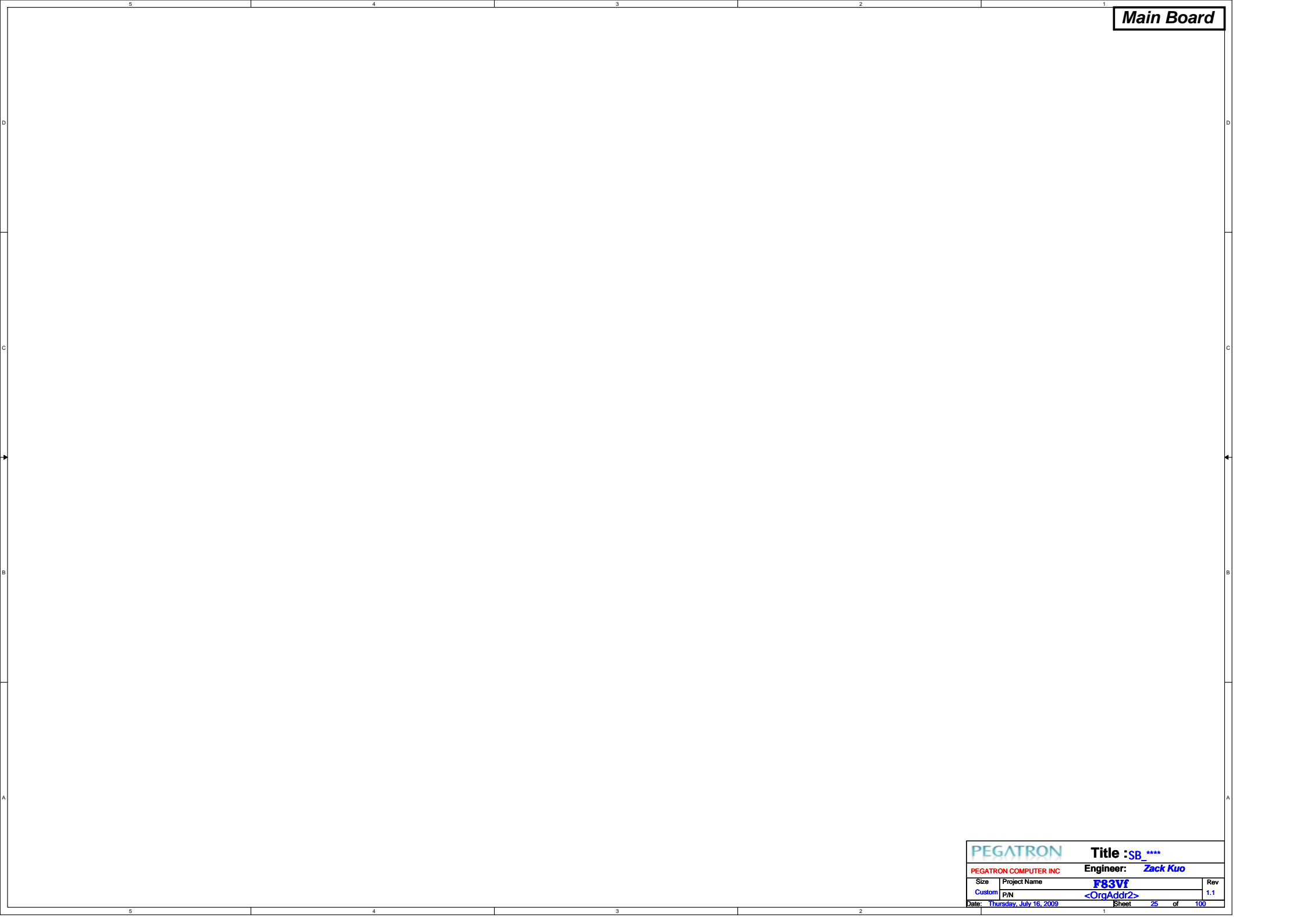


SATA1	HDD	1
SATA2	ODD	2
SATA4	HDD	2
SATA5	ESATA	

ICH9-M



PEGATRON		Title : ICH9M-Other	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	24 of 100

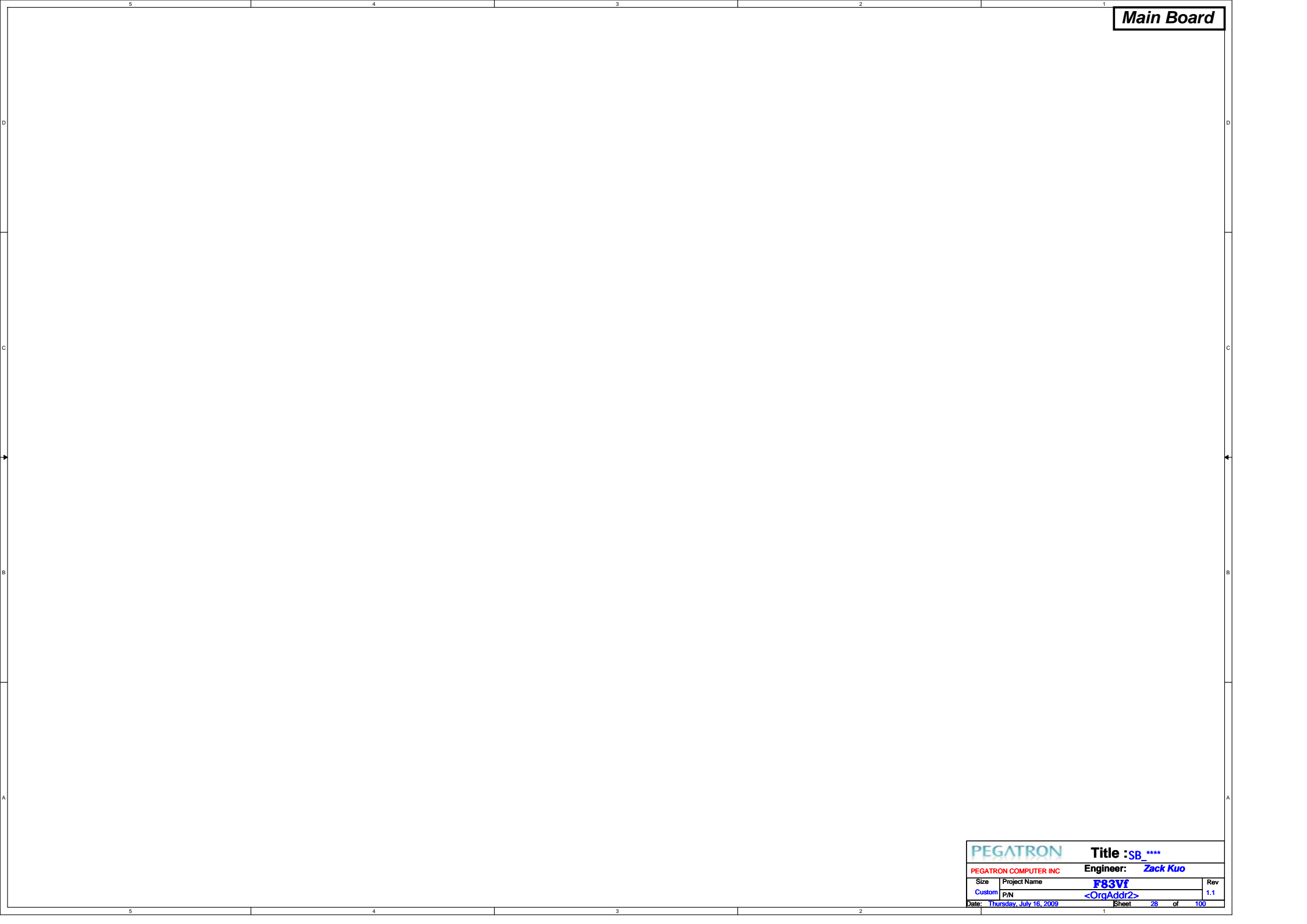


PEGATRON		Title :SB ****	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrqAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet	25	of 100

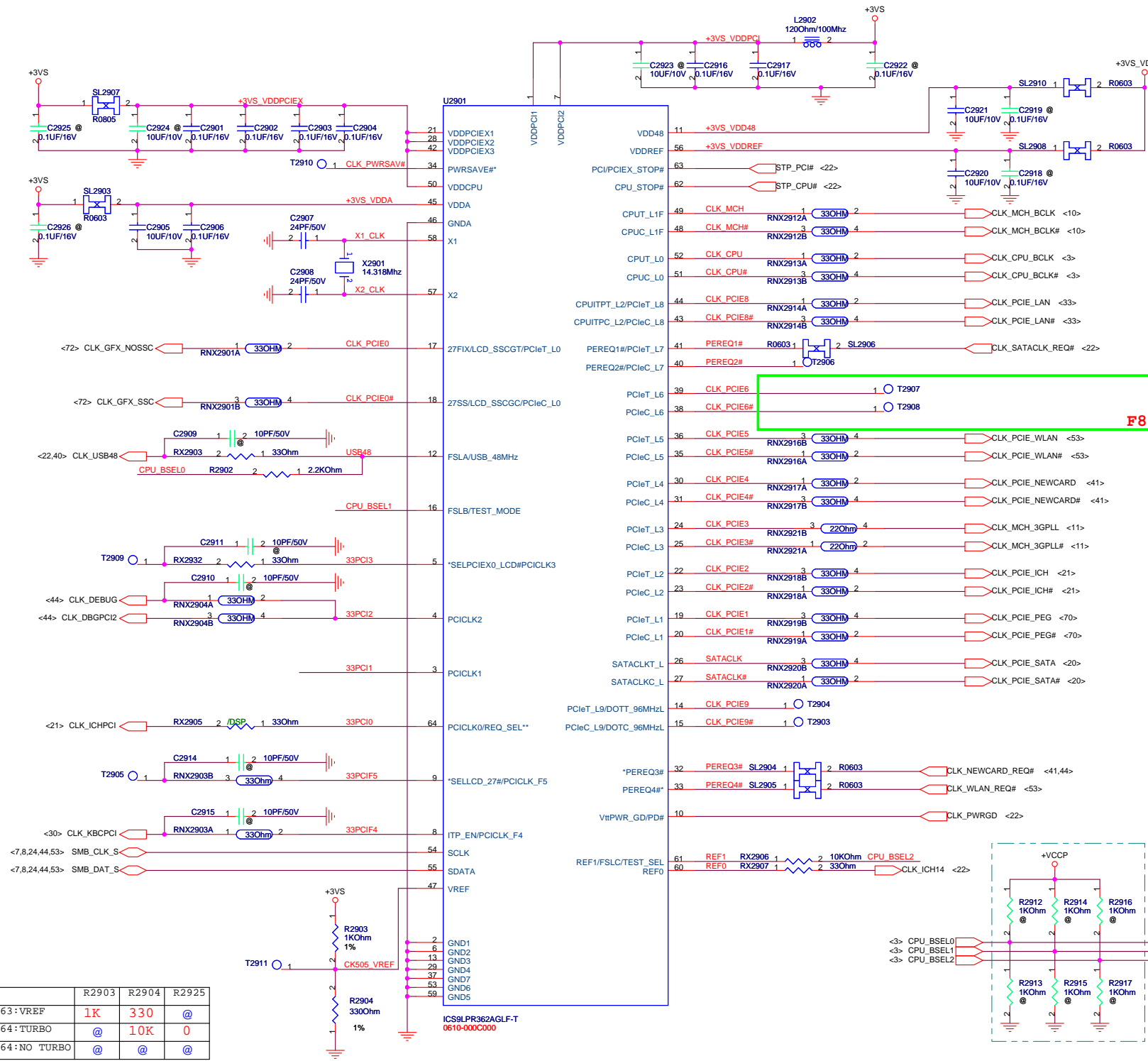
Main Board

PEGATRON		Title :SB ****	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrqAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	26 of 100

PEGATRON		Title :SB ****	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrqAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet 27 of 100		



PEGATRON		Title :SB ****	
PEGATRON COMPUTER INC		Engineer: Zack Kuo	
Size	Project Name	F83Vf	Rev
Custom	P/N	<OrqAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet 28 of 100		



Latched Input Select

0 : Pin 17/18 = LCD_SSCG
1 : Pin 17/18 = PCIe_L0

0 : Pin 43/44 = SRC_CLK
1 : Pin 43/44 = CPU_ITP_CLK

0 : Pin 14/15 = PCIe_L9
Pin 17/18 = 27FIX/27SS
1 : Pin 14/15 = DOT_96MHz
Pin 17/18 = LCD_SSCG/PCIe_L0

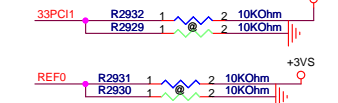
0 : Pin 40/41 = PCIe_L7
1 : Pin 40/41 = PEREQ#

PEREQ1#:
PEREQ1# R2922 1 2 10KOhm

PEREQ2#:
PEREQ2# R2923 1 2 10KOhm

PEREQ3# : PCIeX2/4
PEREQ4# : PCIeX3/5/7

For 364 Over-clocking



Reserved for R1.0 Debug

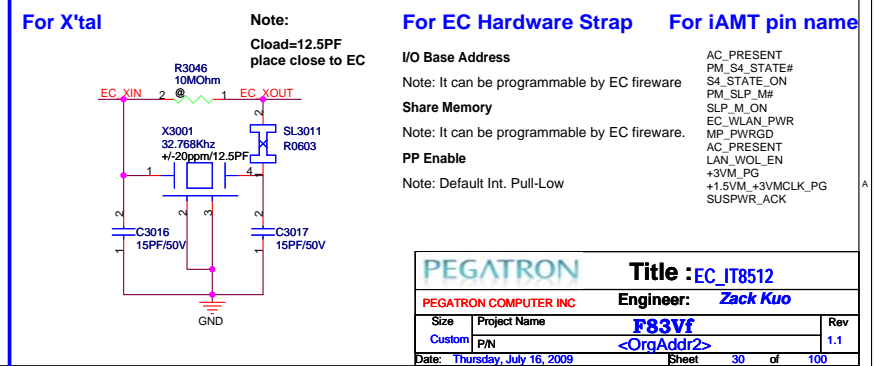
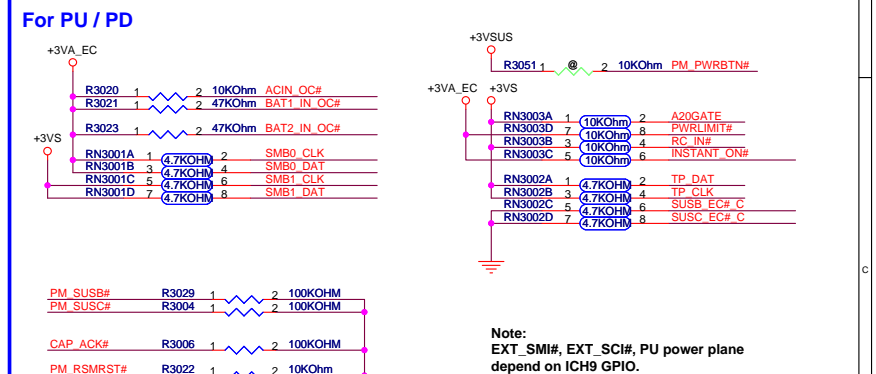
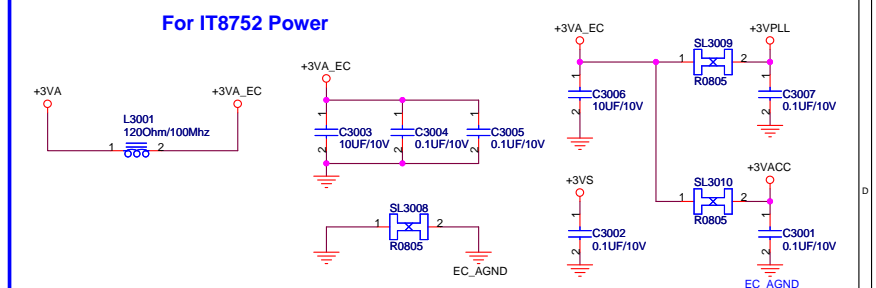
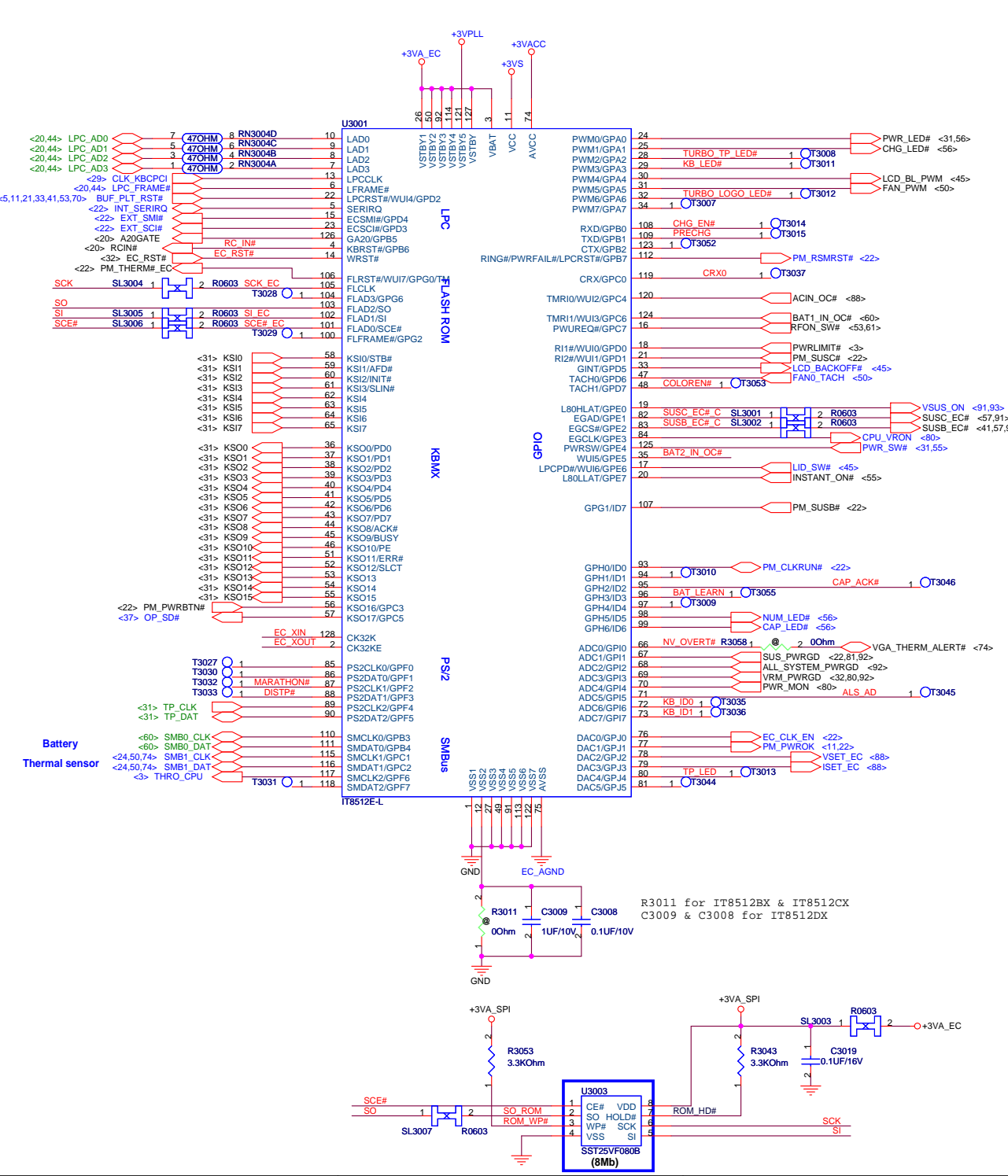
BCLK	F5B	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0



	R2903	R2904	R2925
363 : VREF	1K	330	@
364 : TURBO	@	10K	0
364 : NO TURBO	@	@	@

ICS9LPR362AGLF-T
0610-000C00

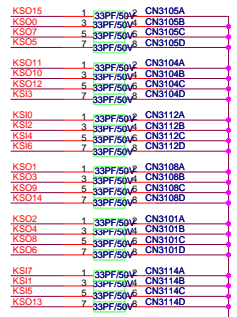
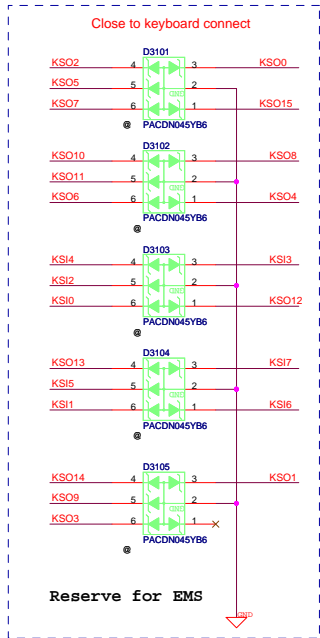
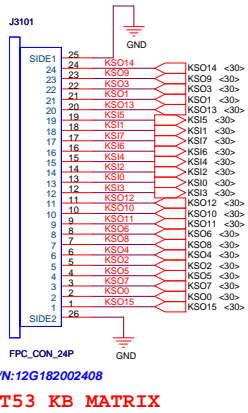
PEGATRON Title : CLK_ICS9LPR363
PEGATRON COMPUTER INC Engineer : Zack Kuo
 Size Project Name **F83Vf**
 Custom P/N **<OrqAddr2>**
 Date: Thursday, July 16, 2009 Sheet 29 of 100



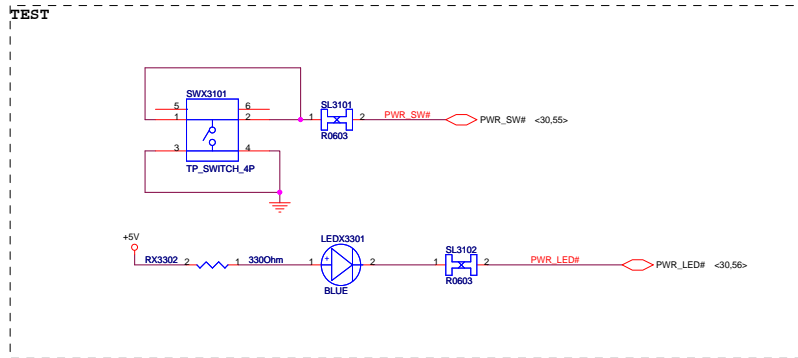
PEGATRON Title: **EC_IT8512**

PEGATRON COMPUTER INC Engineer: **Zack Kuo**

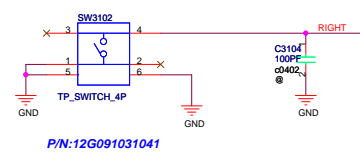
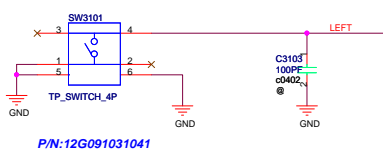
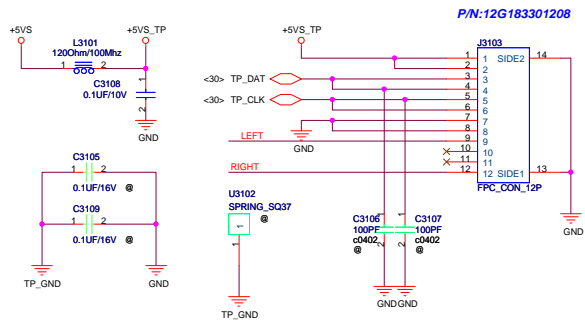
For Keyboard

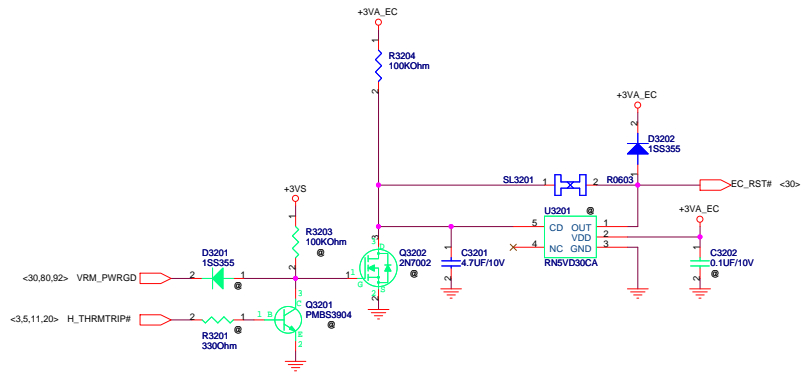


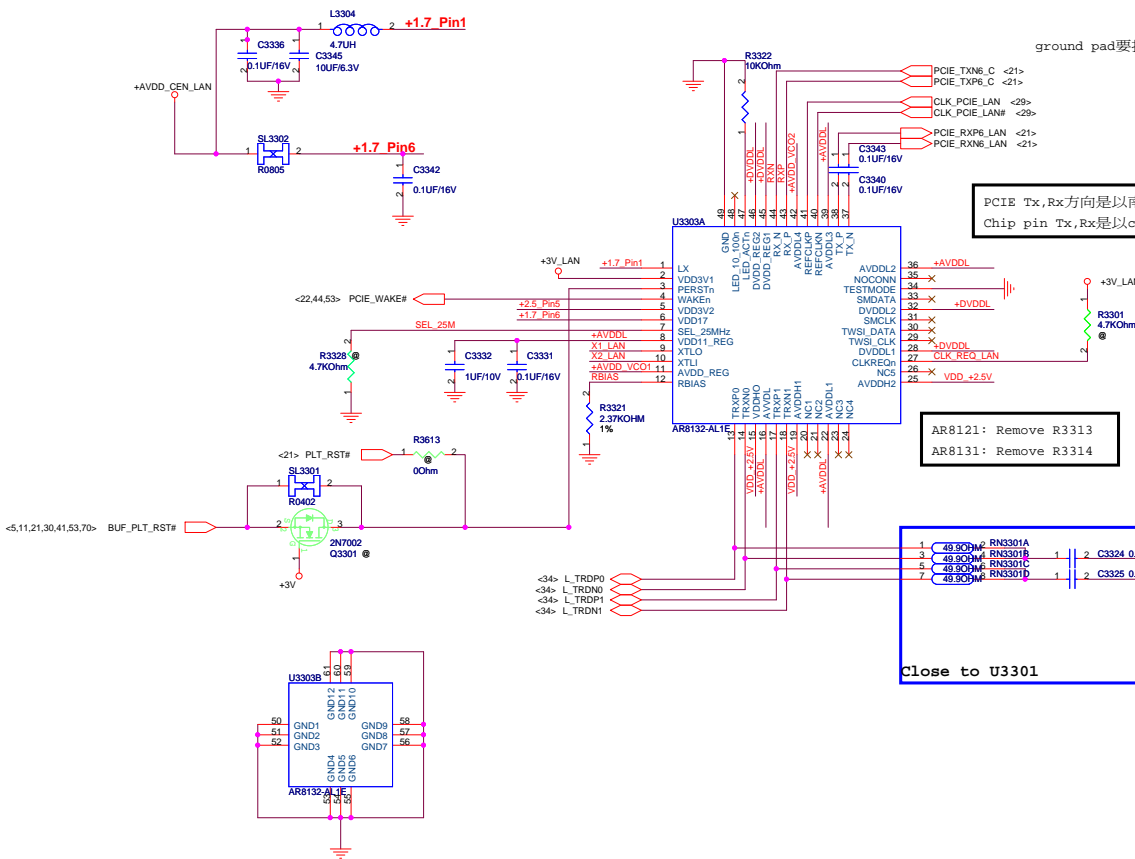
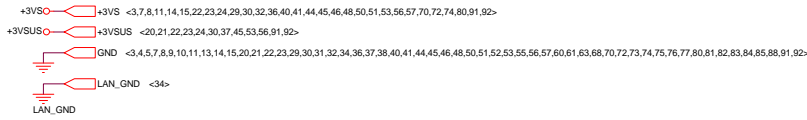
Reserve for EMI



Touch-Pad







ground pad要打散熱孔

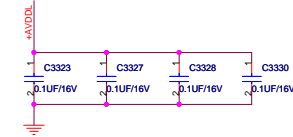
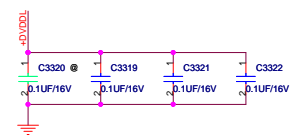
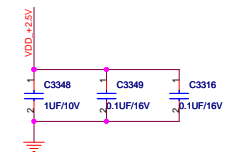
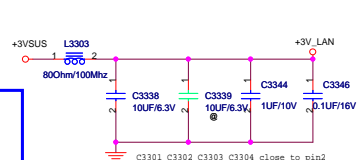
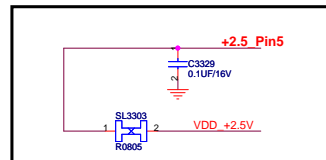
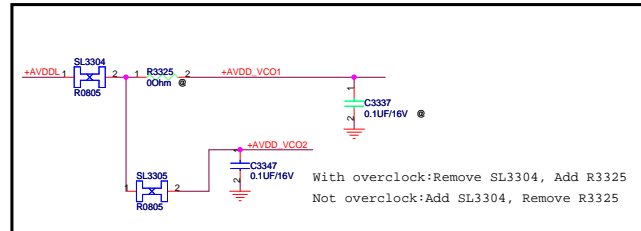
PCIE Tx,Rx方向是以南橋為觀點
Chip pin Tx,Rx是以chip為觀點

AR8121: Remove R3313
AR8131: Remove R3314

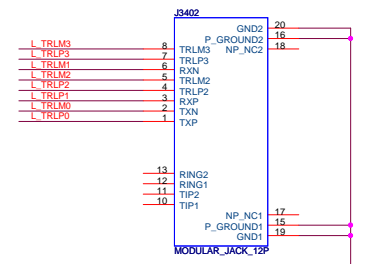
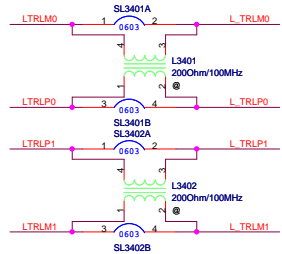
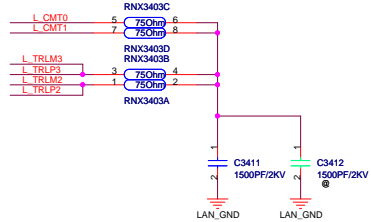
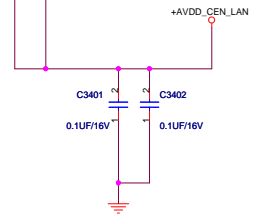
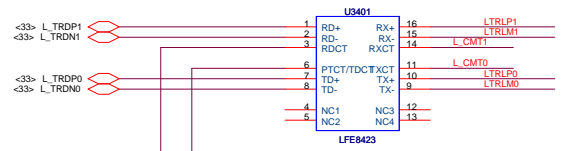
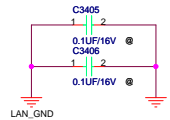
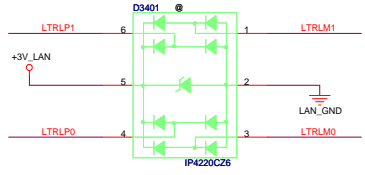
Close to U3301

For AR8131: Remove R3309
+1.7 Pin6
R3316 00hm
VDD +2.5V

AR8121: Remove C3328
AR8131/25Mhz: Remove C3328



LAN / MODEM PORT



5

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c

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b

a

a

PEGATRON		Title : <Title>	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	35 of 100

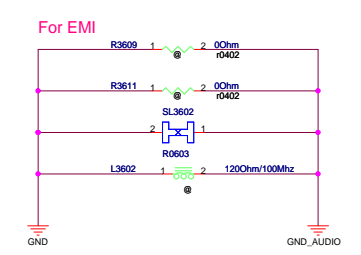
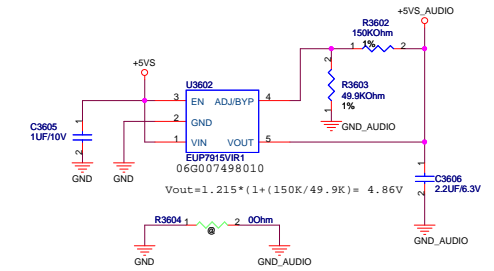
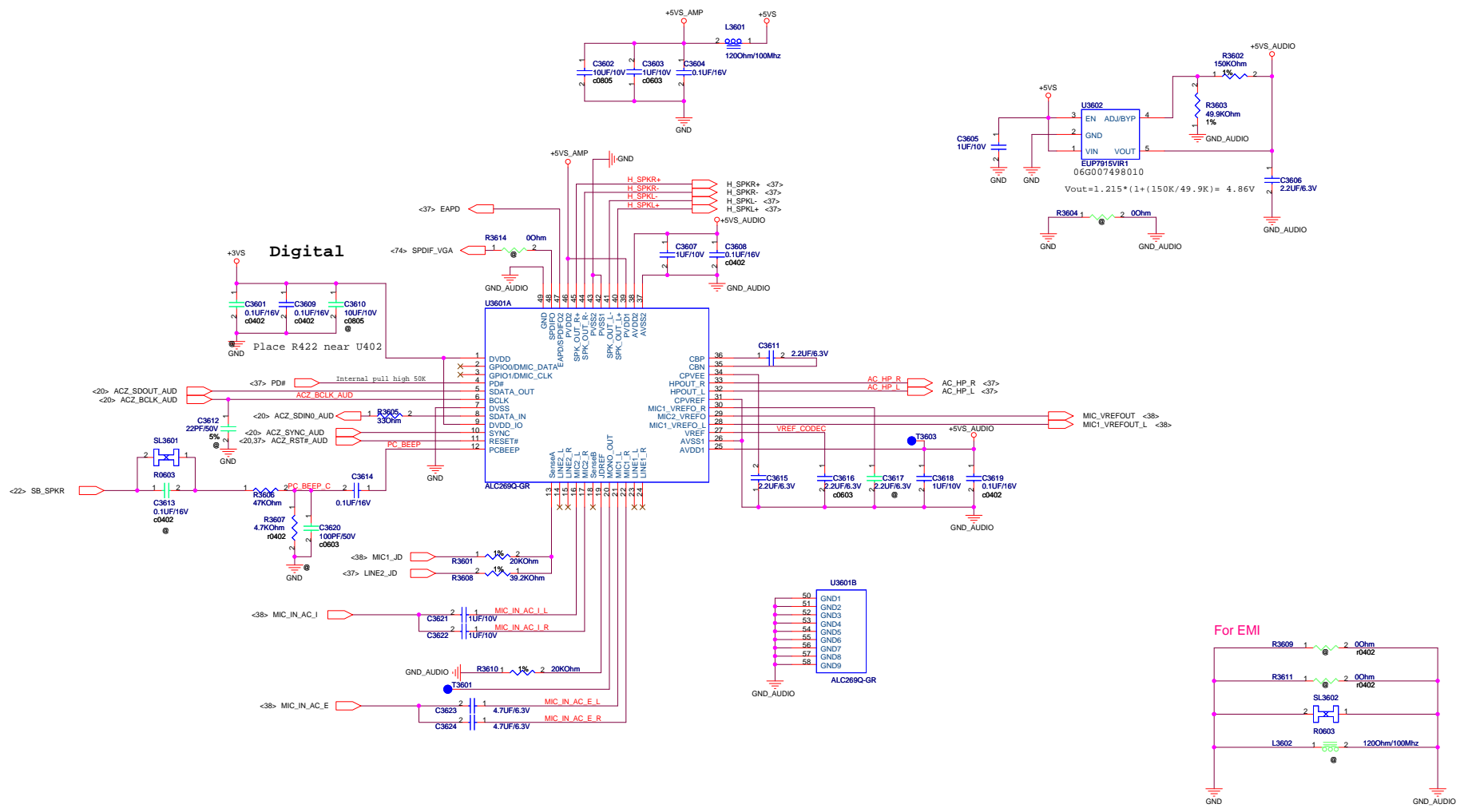
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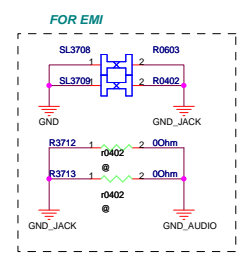
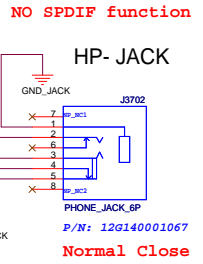
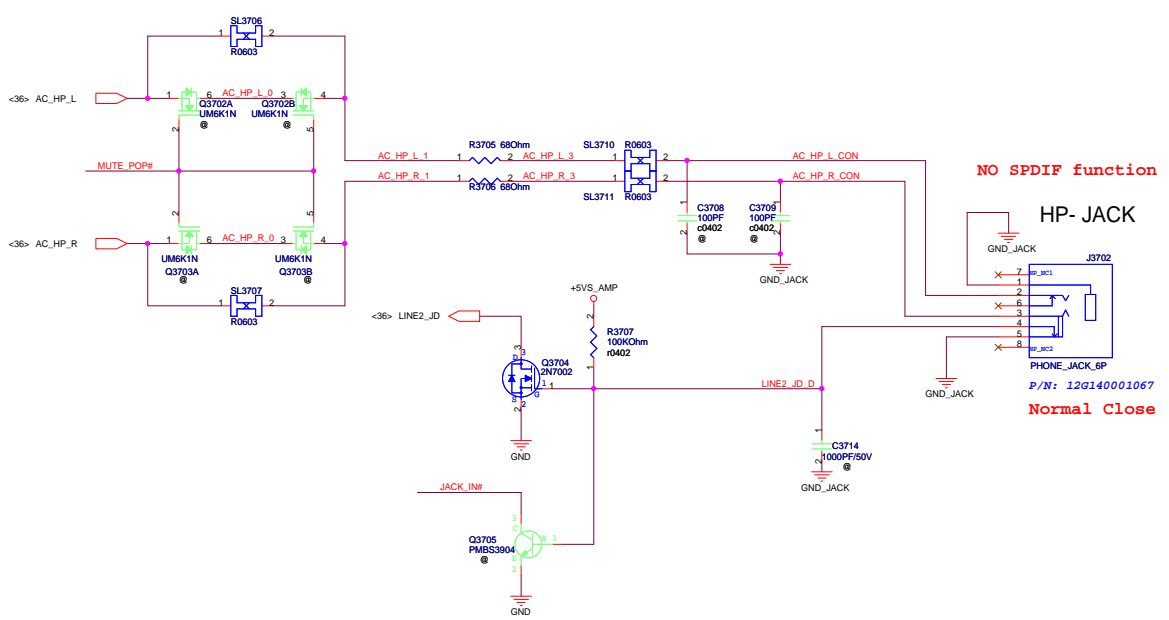
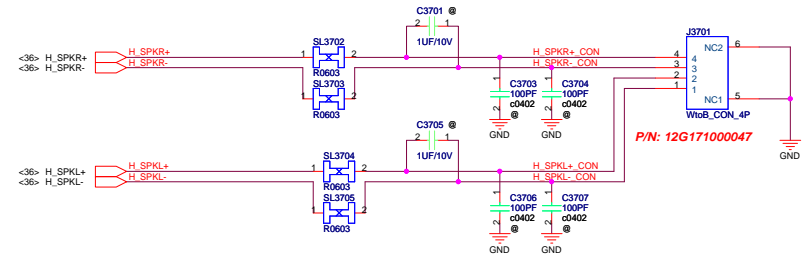
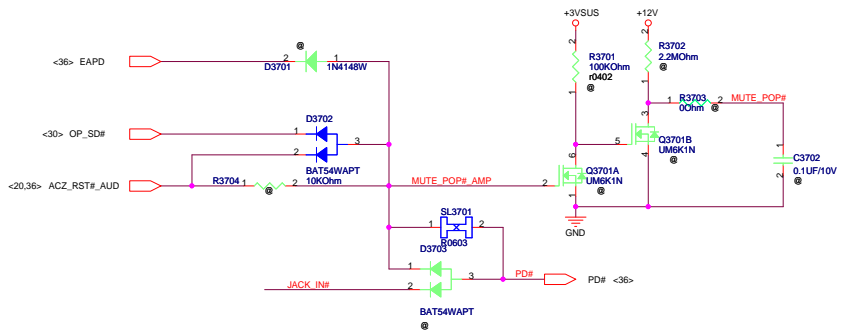
4

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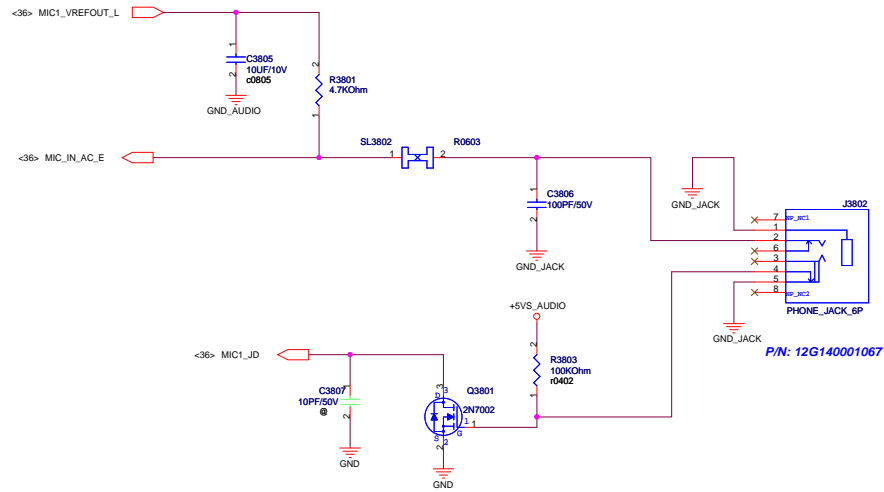
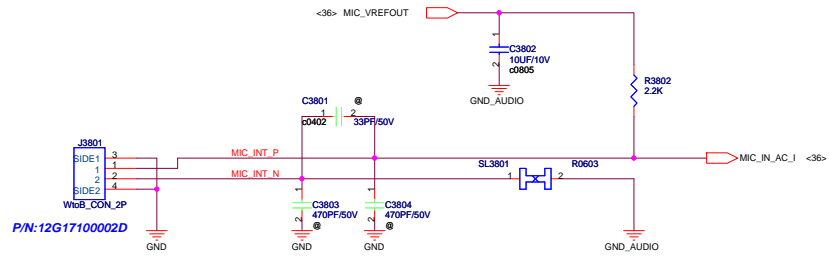
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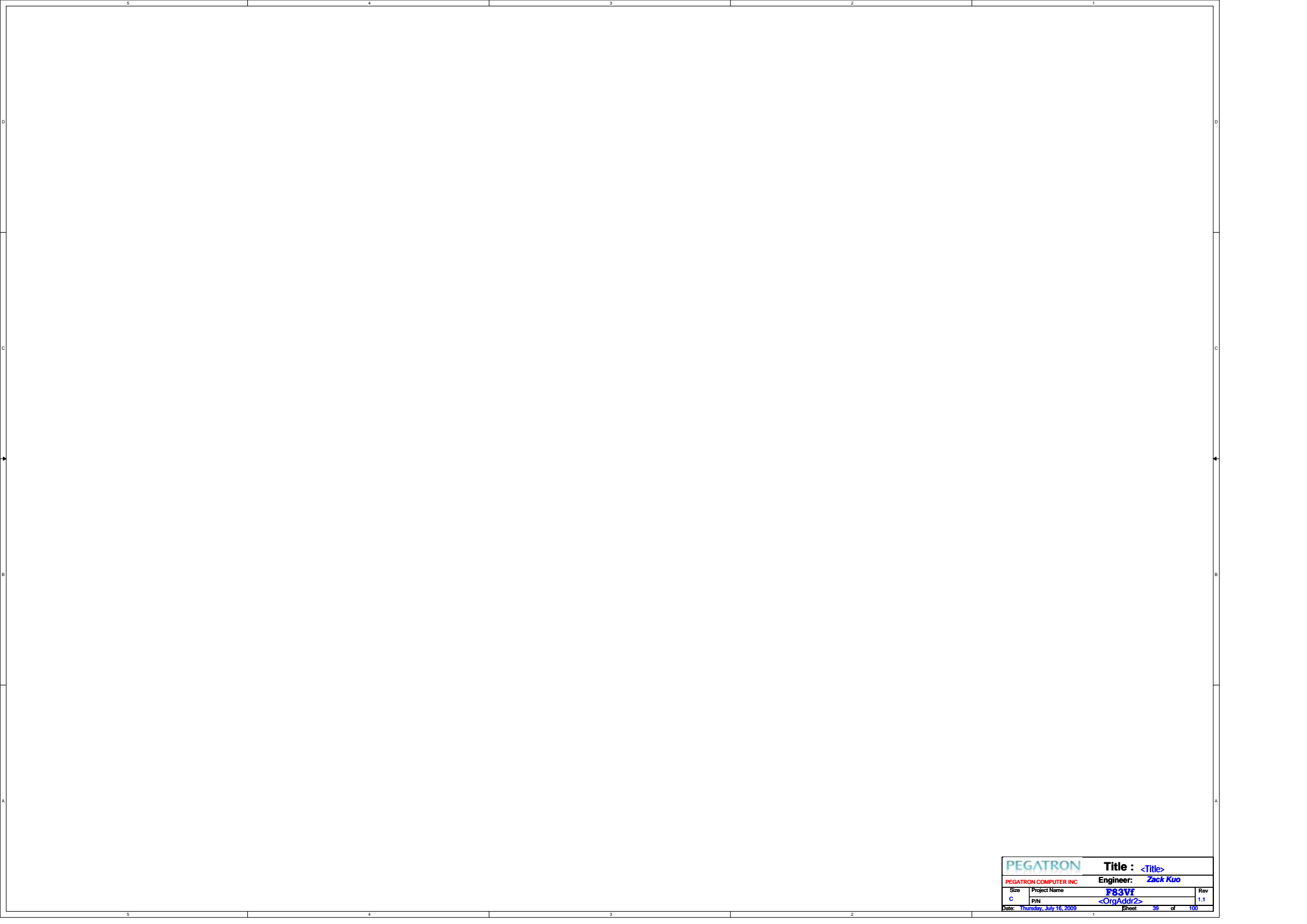
1





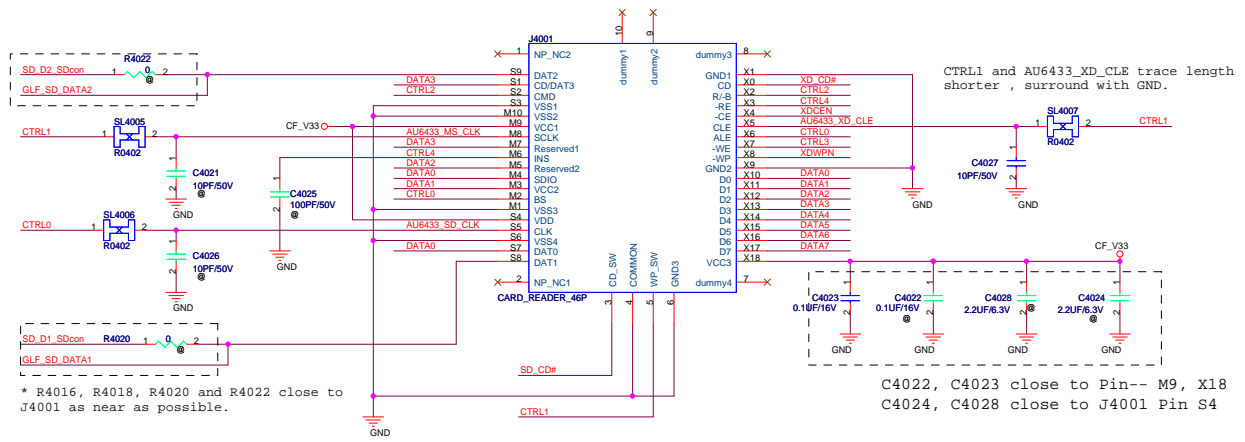
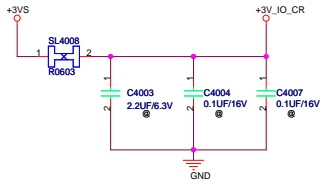
Internal MIC Pre-Amplifier





PEGATRON		Title : <Title>	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	39 of 100

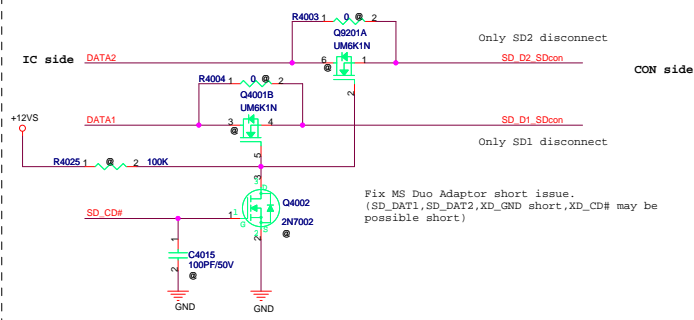
CARD READER CONNECTOR



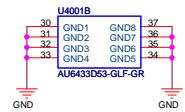
CTRL1 and AU6433_XD_CLE trace length shorter, surround with GND.

C4022, C4023 close to Pin-- M9, X18
C4024, C4028 close to J4001 Pin S4

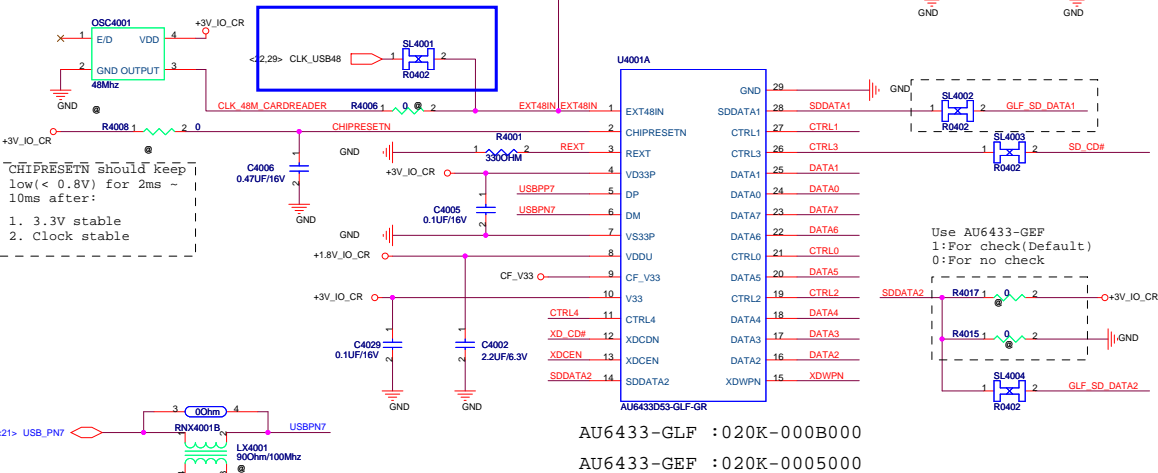
For AU6433-GEF



Fix MS Duo Adaptor short issue.
(SD_DAT1, SD_DAT2, XD_GND short, XD_CD# may be possible short)



48MHZ can provide by Clock GEN.
logic 1 or open on pad1->oscillator output



CHIPRESETN should keep low (< 0.8V) for 2ms - 10ms after:
1. 3.3V stable
2. Clock stable

CTRL0->SDCLK/XDALE/MSBS
CTRL1->SDWP/XDCLE/MSCLK
CTRL2->SDCMD/XDRBN
CTRL3->SDCDN/XDWRN
CTRL4->XDRDN/MSINS

XDCDN->XDCDN
XDCEN->XDCEN
SDDATA2->SDDATA2/XD CIS check is disable
XDWPEN->XDWPEN

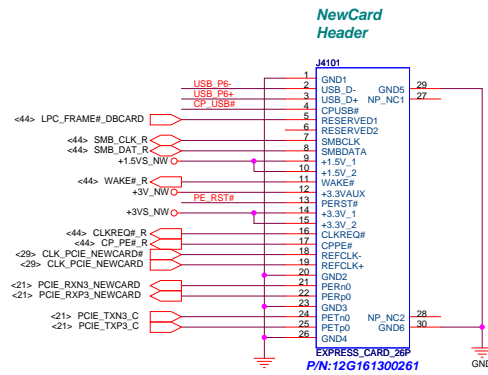
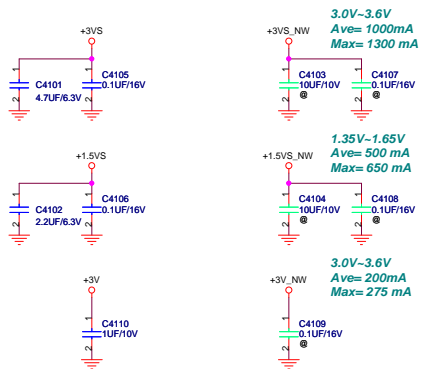
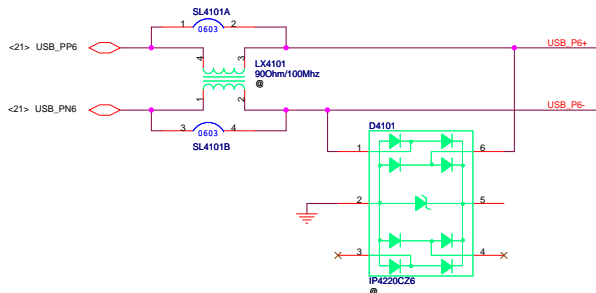
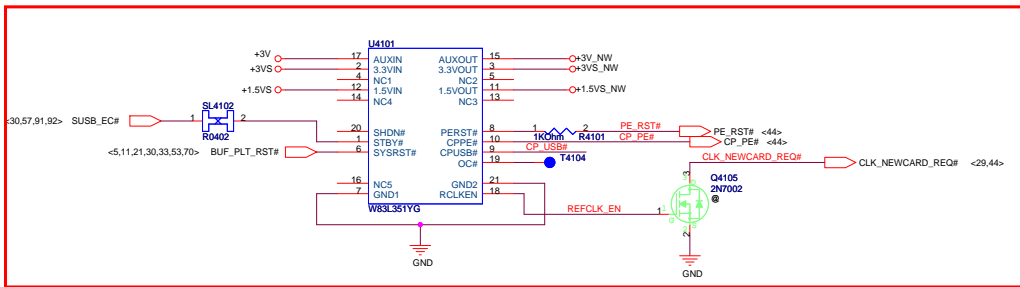
ADDDATA1->SDDATA1
DATA0->SDDATA0/XDDATA0/MSDATA0
DATA1->XDDATA1/MSDATA1
DATA2->XDDATA2/MSDATA2
DATA3->SDDATA3/XDDATA3/MSDATA3
DATA4->SDDATA4/XDDATA4/MSDATA4
DATA5->SDDATA5/XDDATA5/MSDATA5
DATA6->SDDATA6/XDDATA6/MSDATA6
DATA7->SDDATA7/XDDATA7/MSDATA7

AU6433 GEF /GLF colay.

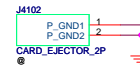
Option 1:AU6433-GEF
If use GEF package need:
unmount-> R4016, R4018
mount->R4017, R4020, R4022, R4025, Q4001, Q4002.

Option 2:AU6433-GLF
If use GLF package need:
unmount->
mount->R4016, R4018

AU6433-GLF :020K-000B000
AU6433-GEF :020K-0005000



NewCard Ejecter





PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	42 of 100

5

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3

2

1

b

b

c

c

b

b

a

a

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet 43 of 100		

5

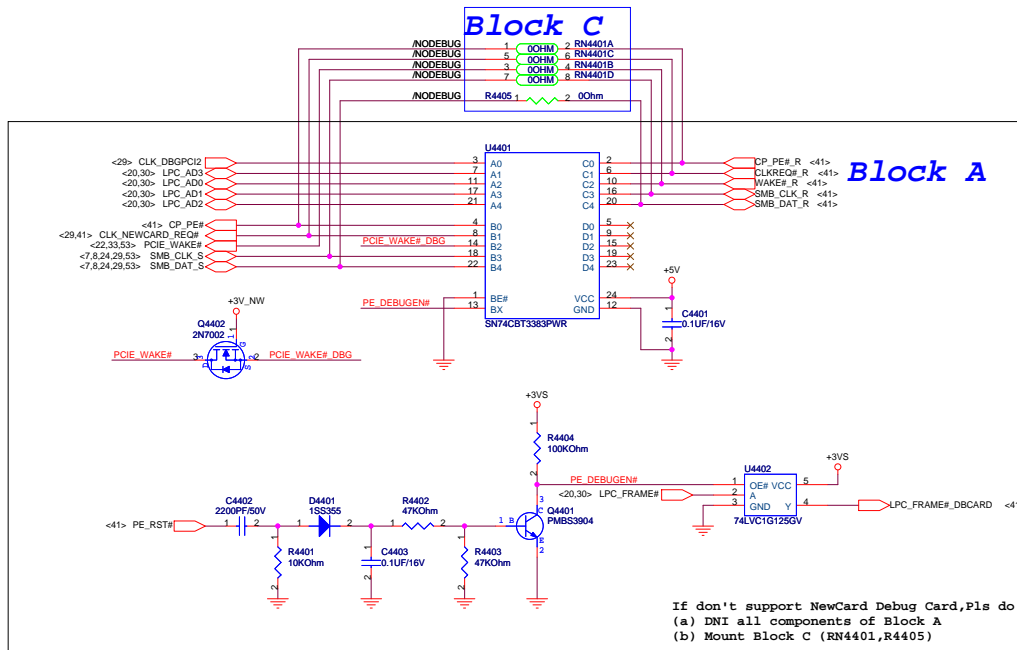
4

3

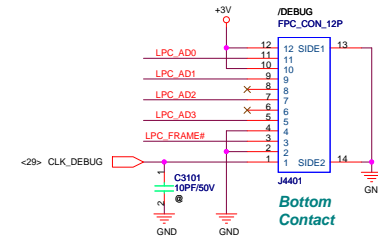
2

1

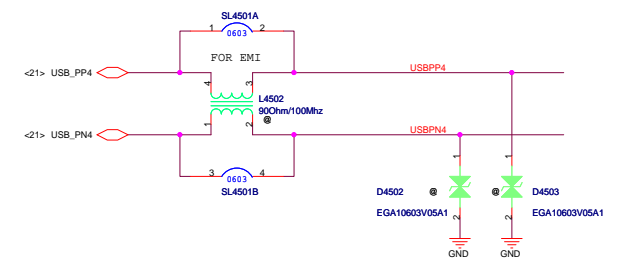
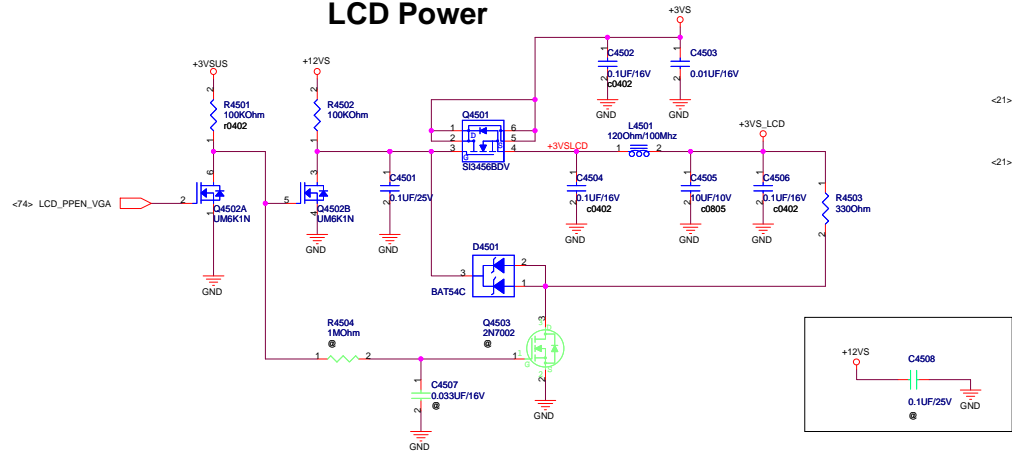
For NewCard Debug Card



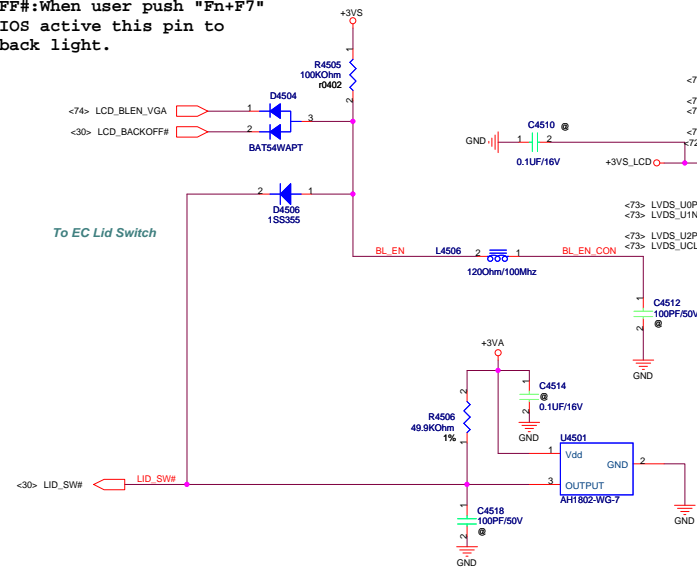
LPC Debug Port



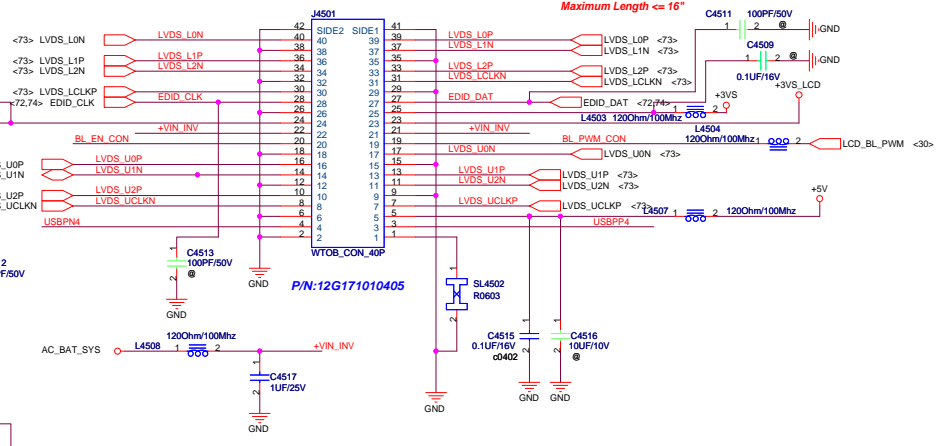
LCD Power



BIOS
 LCD_BACKOFF#: When user push "Fn+F7"
 button, BIOS active this pin to
 turn off back light.

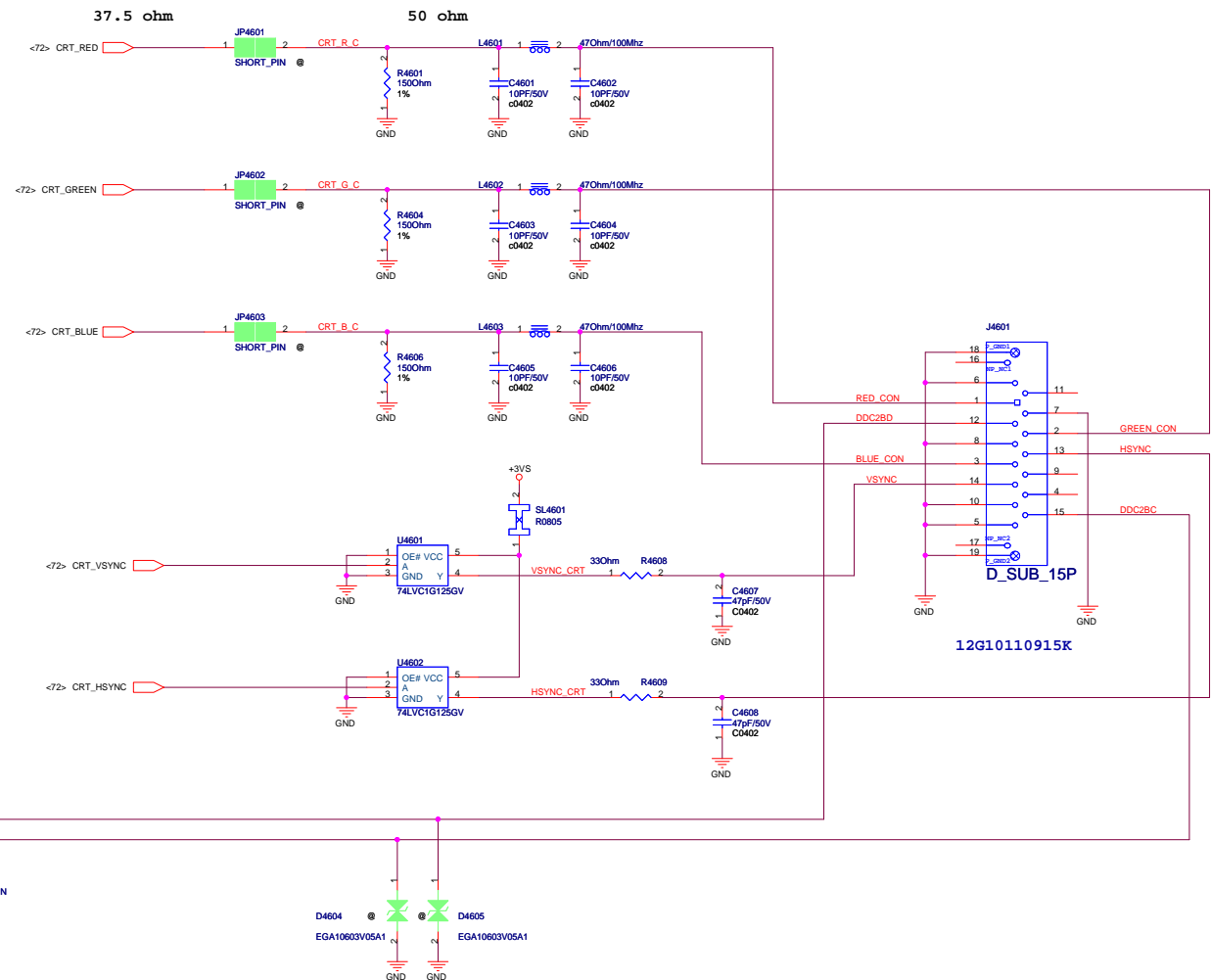
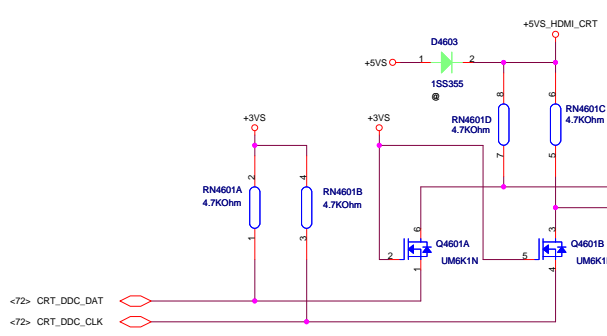
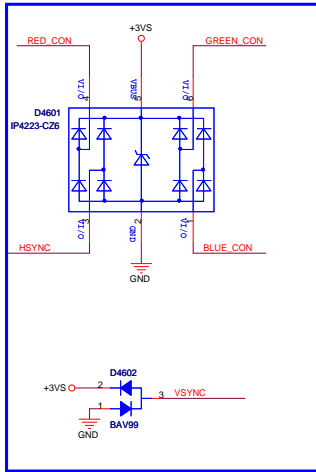


LCD LVDS/Inverter/CCD conn.



Cable Requirement:
 Impedance: 100 ohm +/- 10%
 Length Mismatch <= 10 mils
 Twisted Pair(Not Ribbon)
 Maximum Length <= 16"

PLACE ESD Diodes near connector



5

4

3

2

1

b

b

c

c

b

b

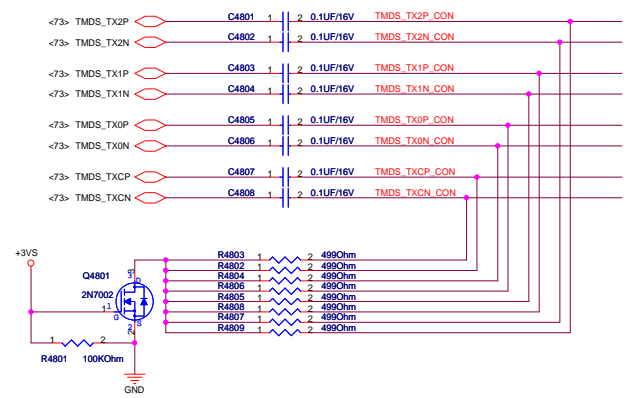
a

a

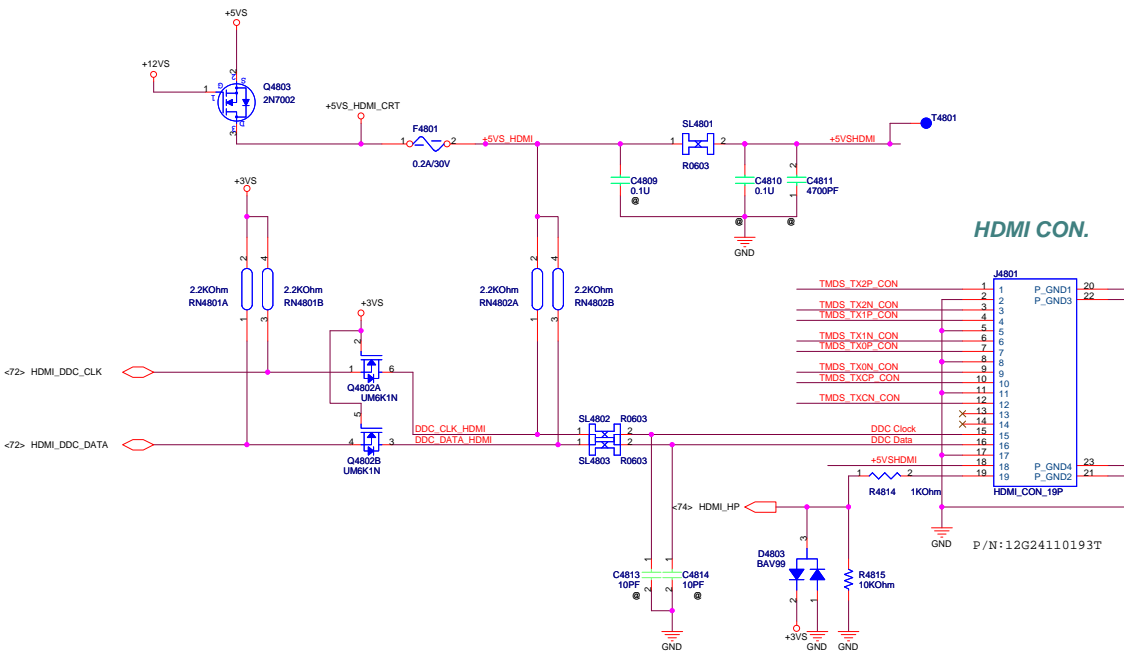
PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet	47 of 100

HDMI

near the HDMI connector



Reference should be +5VS, but All answer that +3VS is fine. As long as it can turn the MOSFET on.

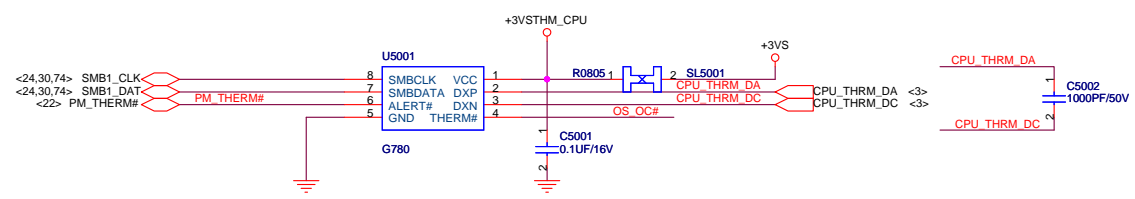


Note: 1. L1805, L1806, L1807: For EMI. (default=0 ohm)
 2. DDC_CLK_HDMI, DDC_DATA_HDMI: +5V tolerant

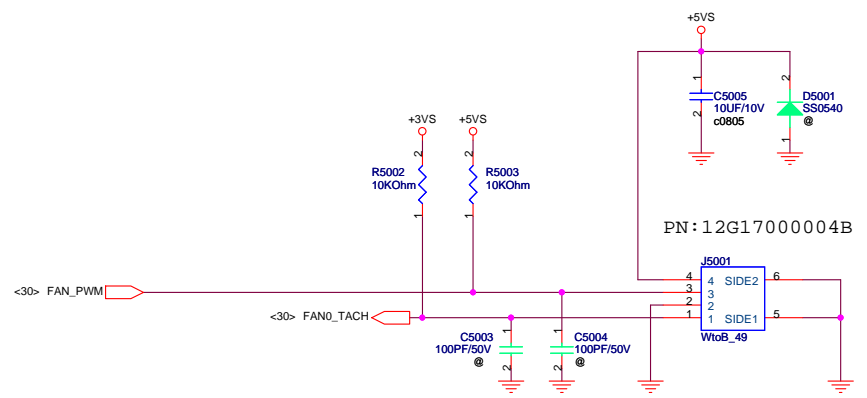


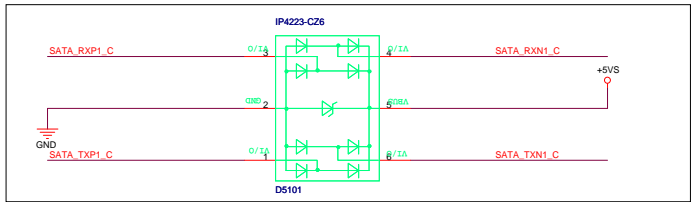
PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	49 of 100

CPU Thermal Sensor

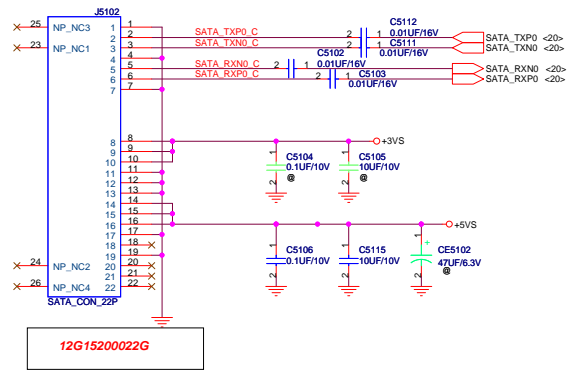


PWM Fan

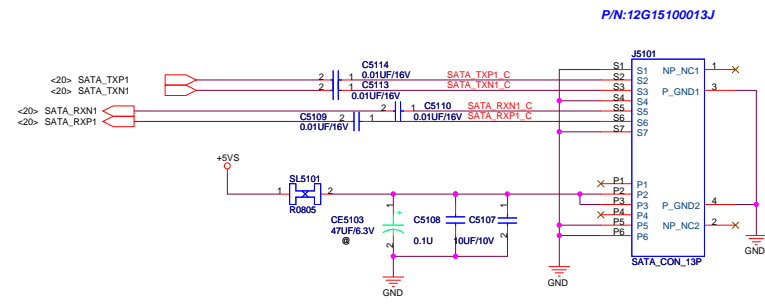


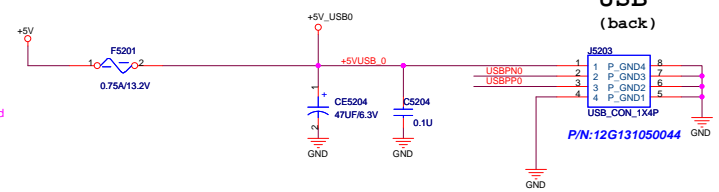
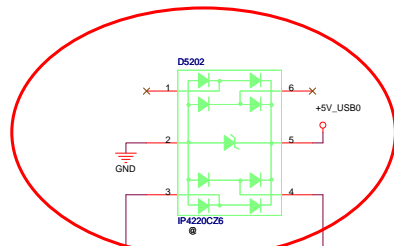
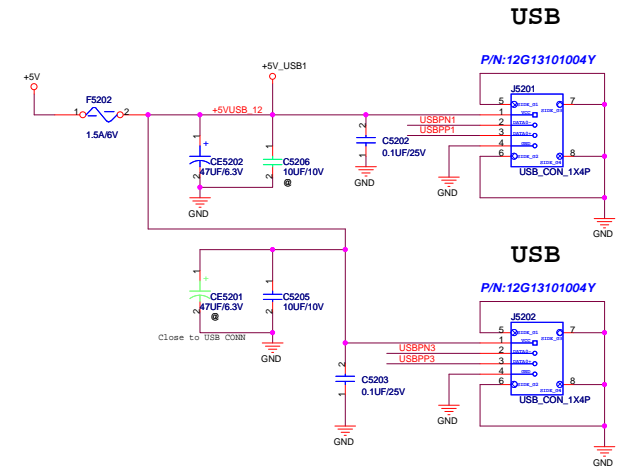
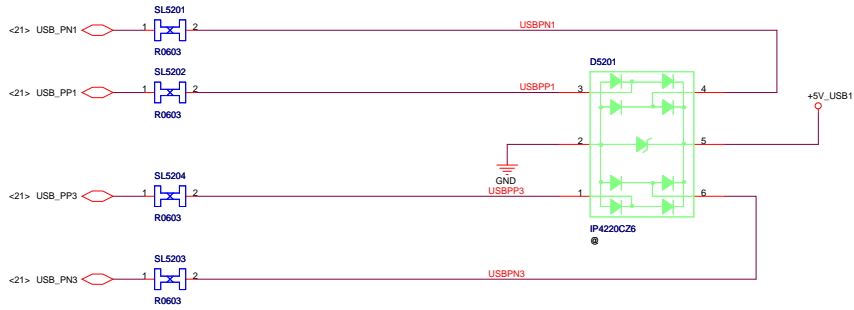


SATA HDD con.



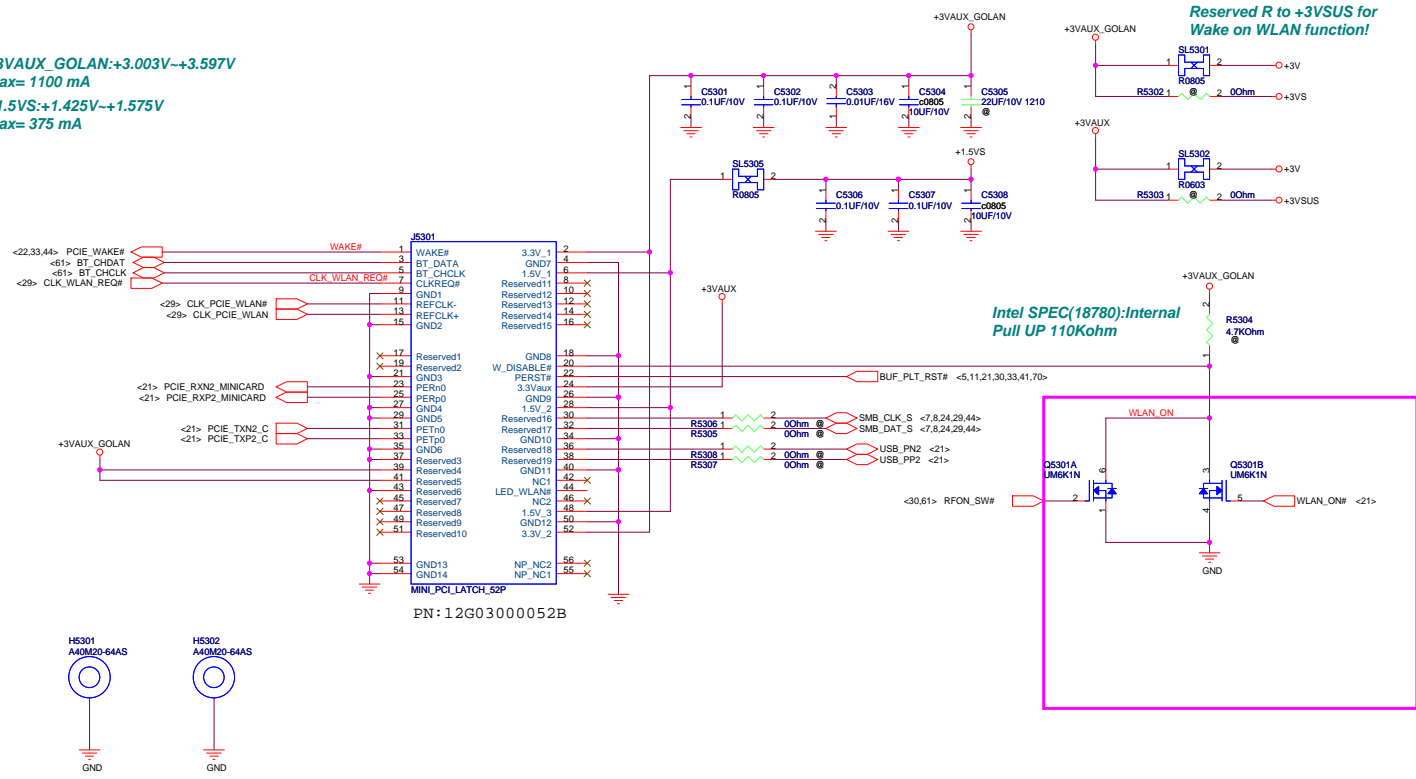
SATA CD-ROM con.





+3VAUX_GOLAN: +3.003V ~ +3.597V
Max= 1100 mA

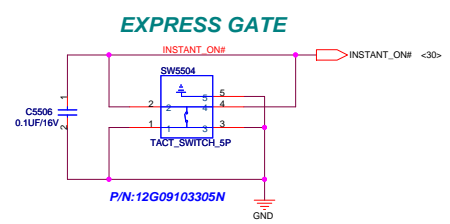
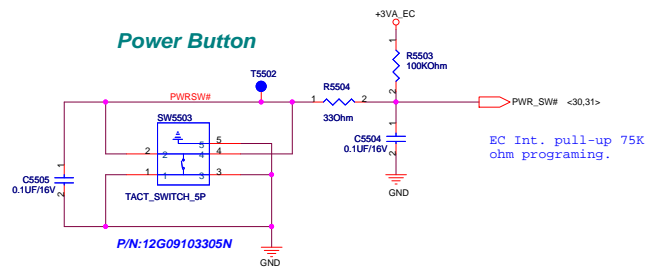
+1.5VS: +1.425V ~ +1.575V
Max= 375 mA



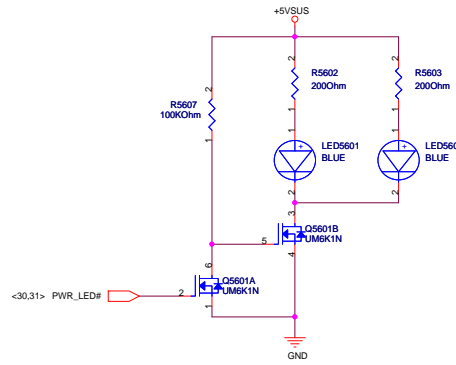
PN: 12G0300052B



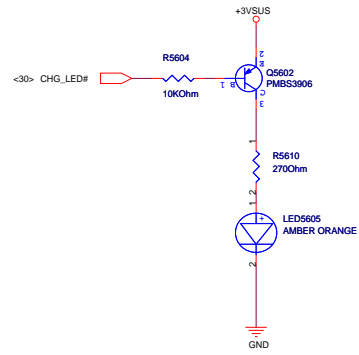
PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet	54 of 100



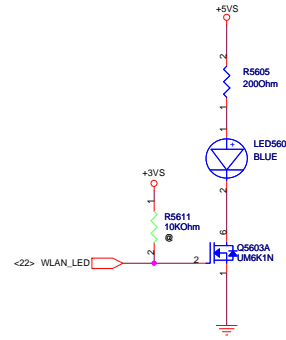
PWR LED



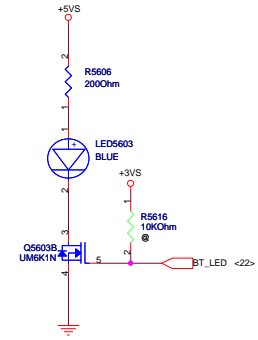
For BATTERY LED



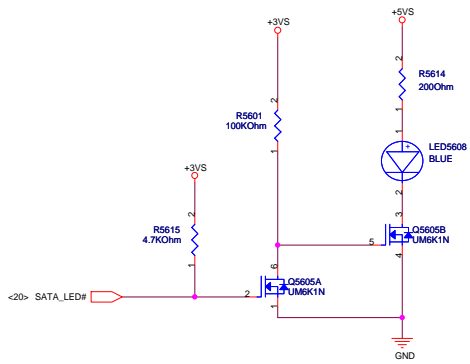
WireLess LED



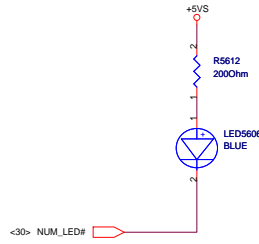
BT LED



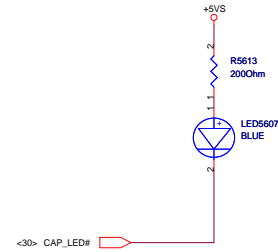
SATA LED

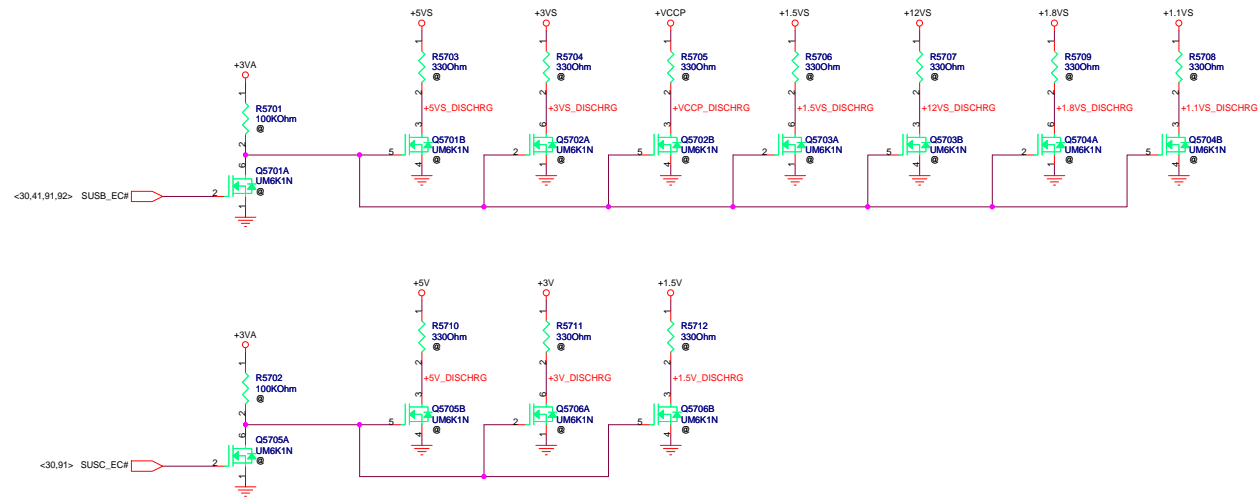


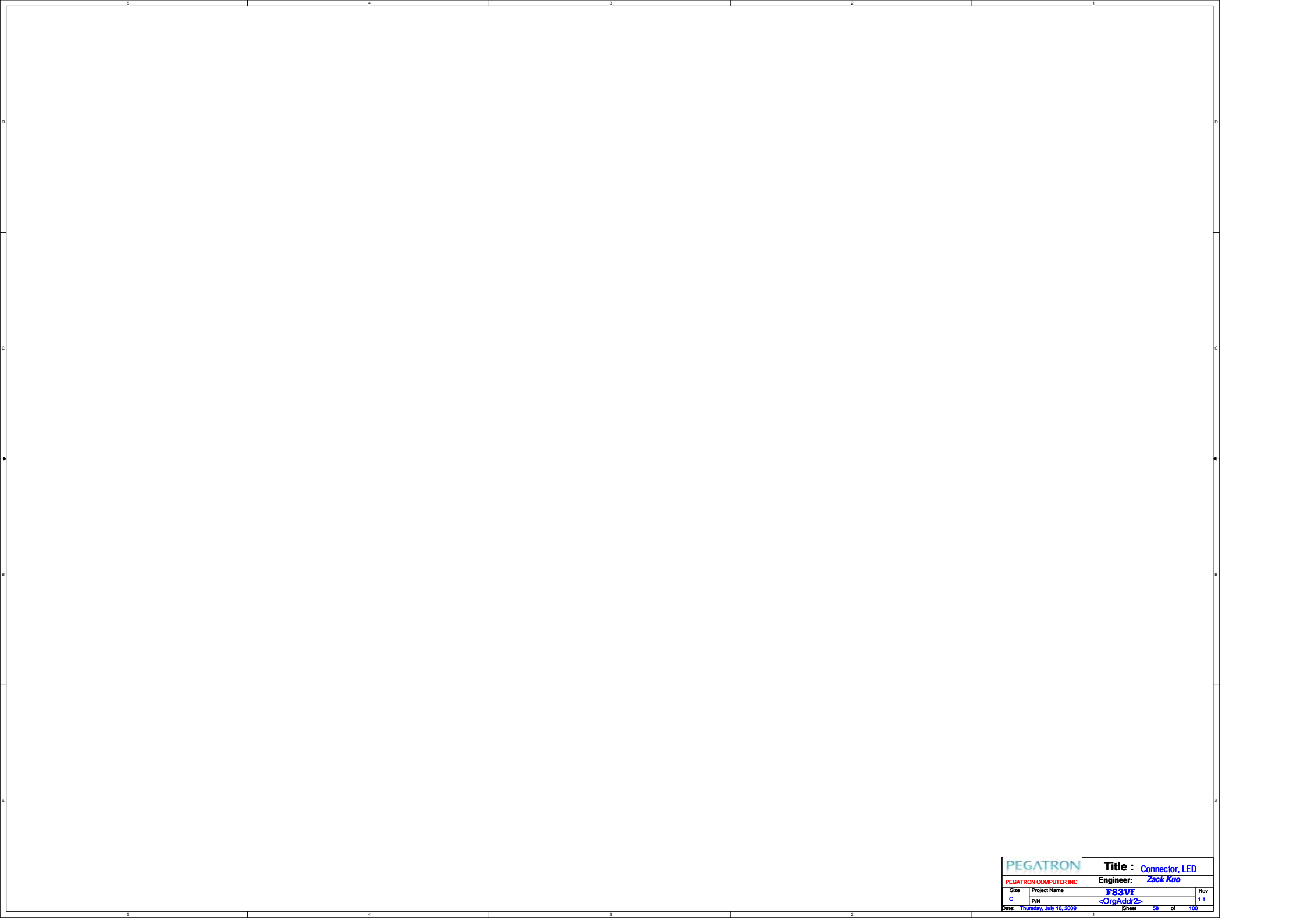
Num Lock



Cap. Lock







PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	58 of 100

5

4

3

2

1

b

b

c

c

b

b

a

a

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009	Sheet	59	of 100

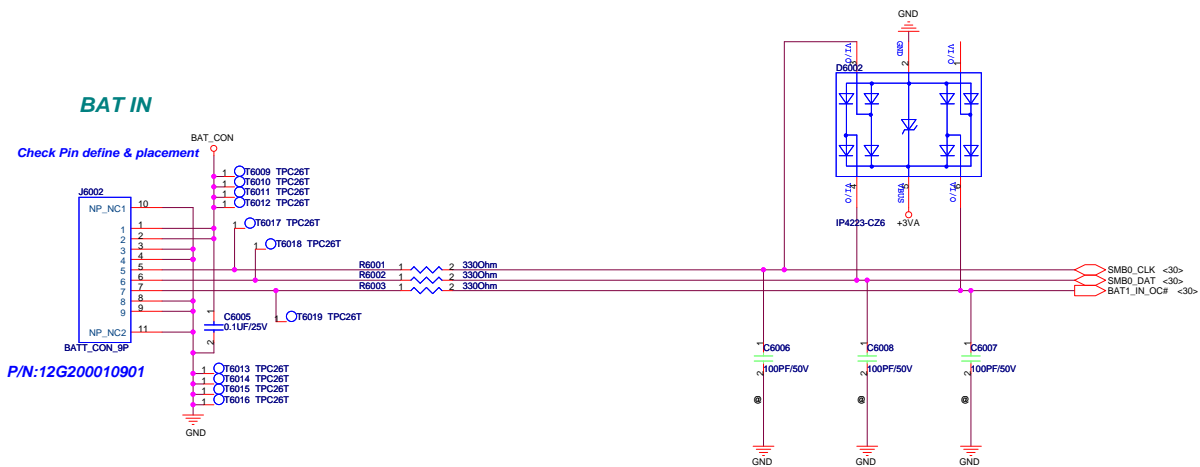
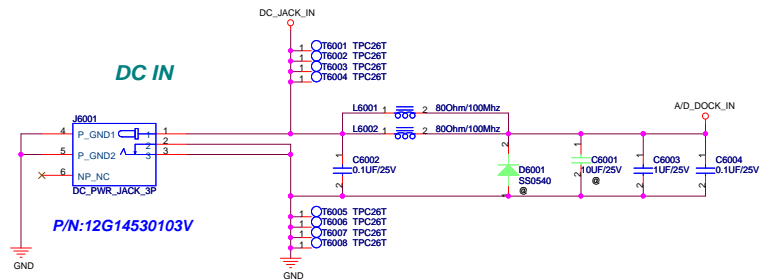
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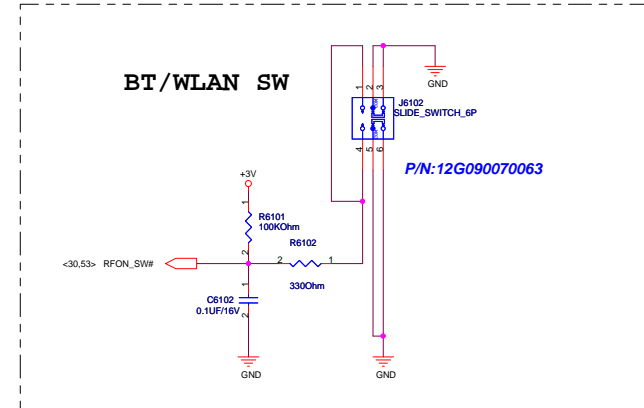
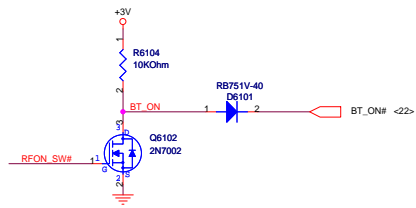
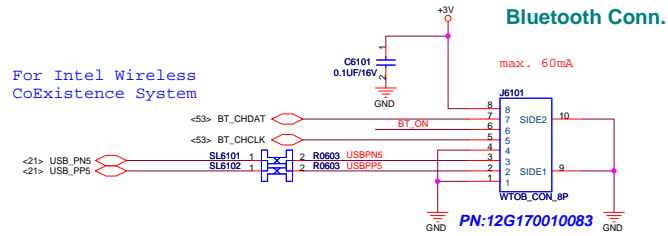
4

3

2

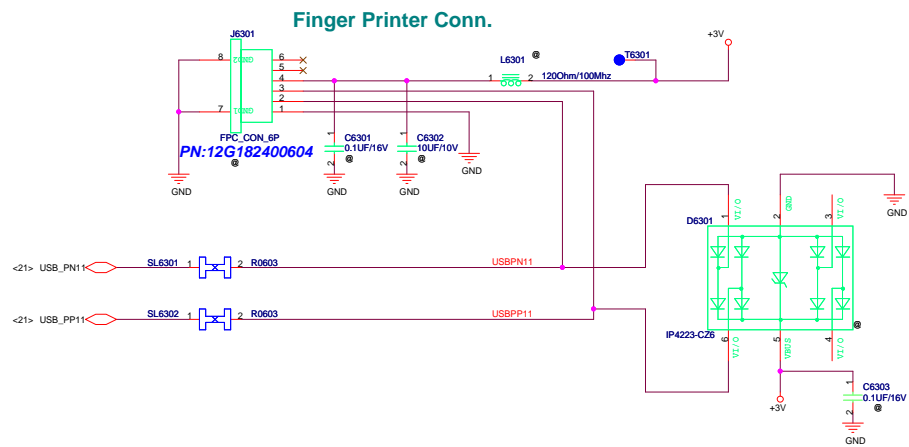
1

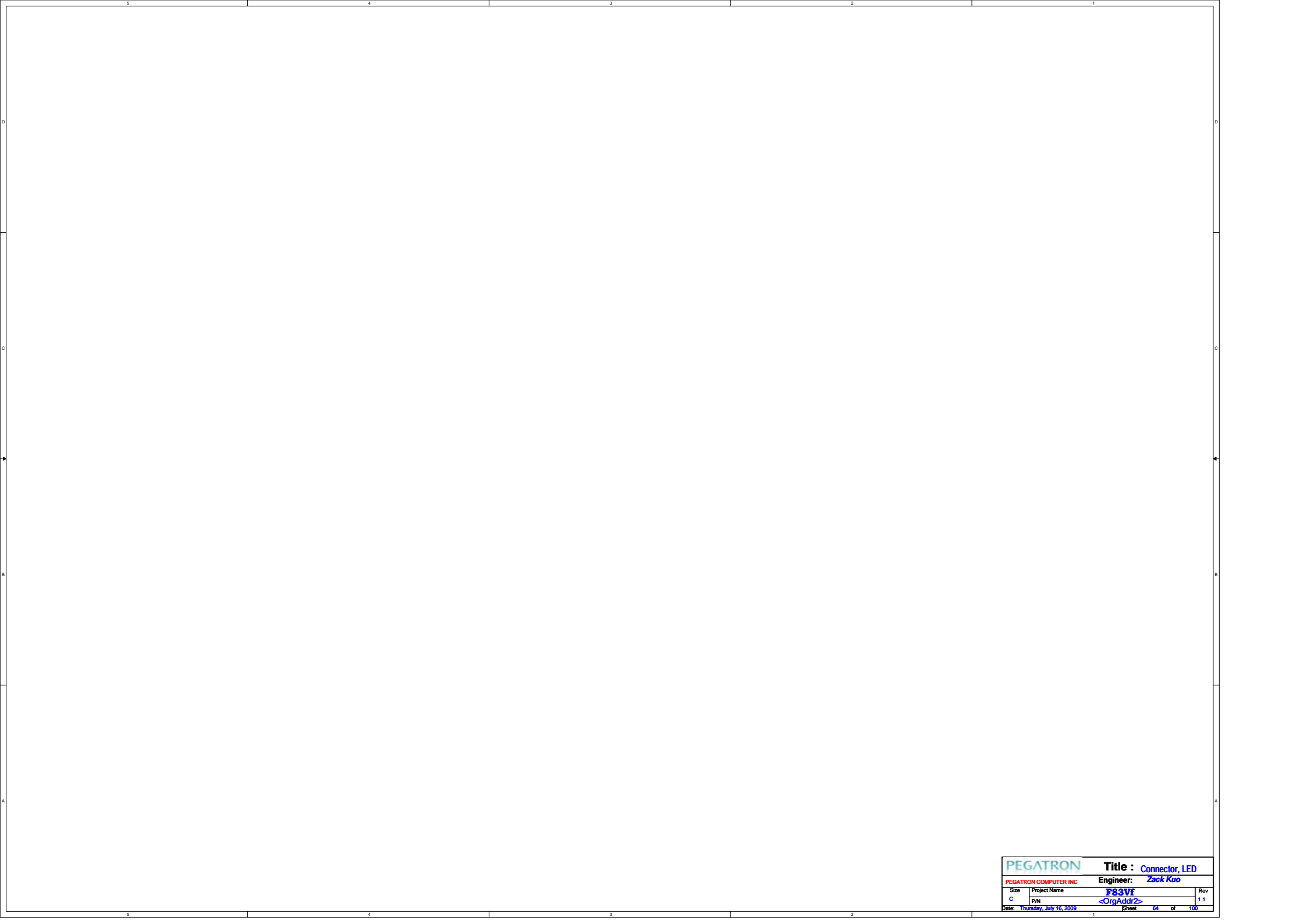






PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	62 of 100





PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	64 of 100



PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	65 of 100



PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	66 of 100

5

4

3

2

1

D

D

C

C

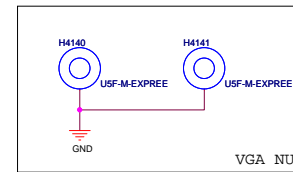
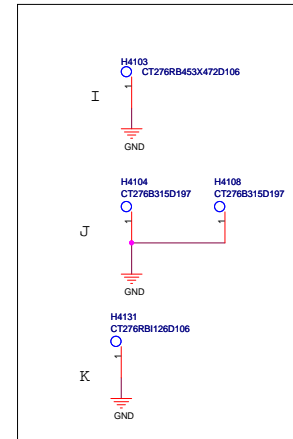
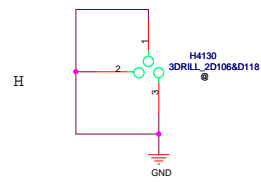
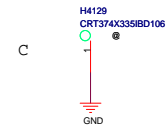
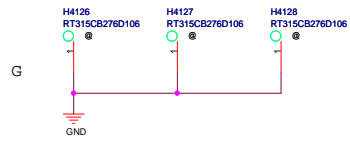
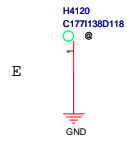
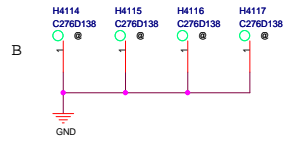
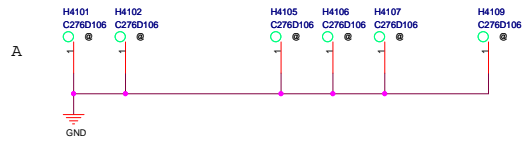
B

B

A

A

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date:	Thursday, July 16, 2009	Sheet	67 of 100

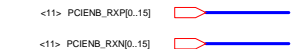
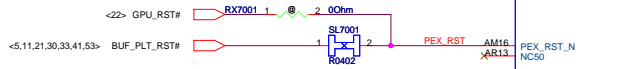


R1.1

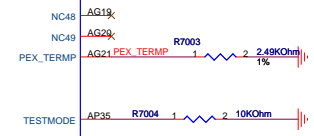
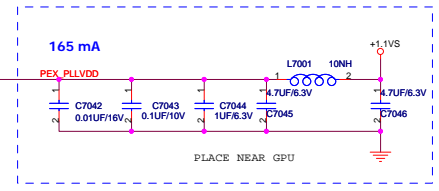
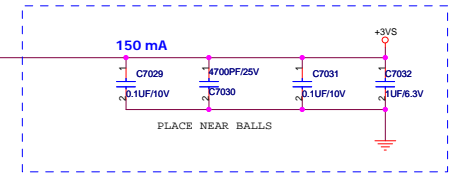
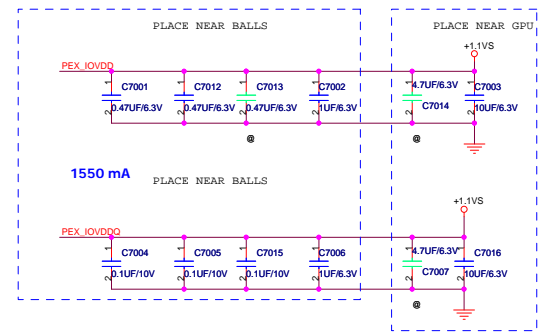
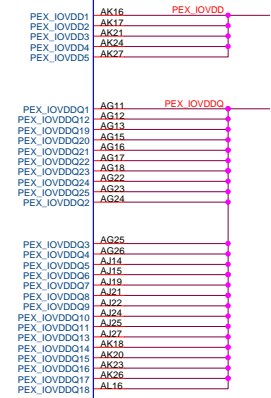
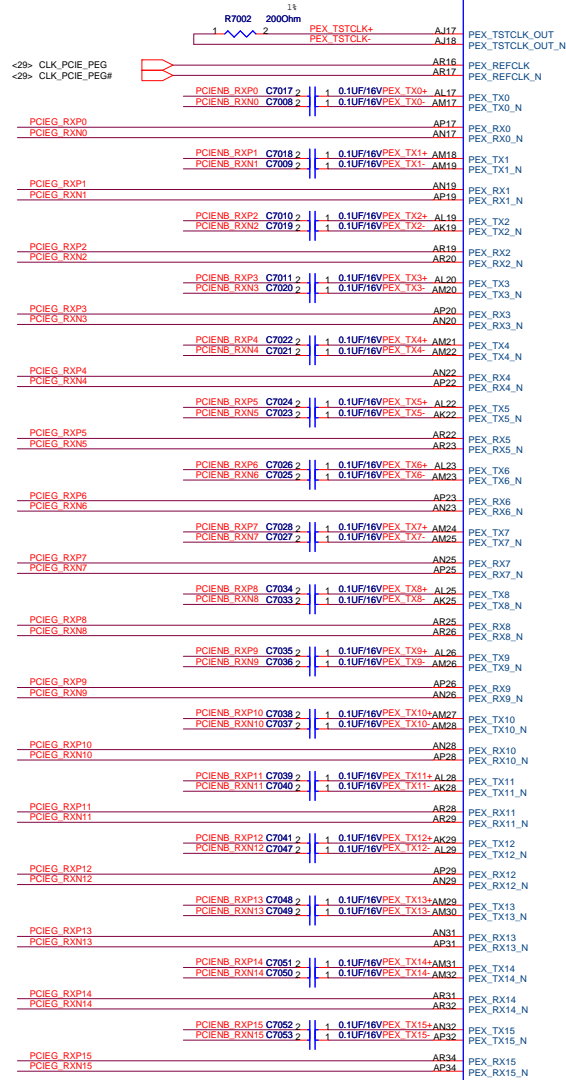
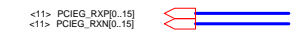
2009/06/30

1. Set DDR3 VREF to 0.75V LDO output.
2. Change Card Reader to AU6433D53-GLP.
3. Change LAN to Atheros AR6132.
4. Change Transformer to 10/100 TAIMAG HA003
5. Change ClockGen to ICS9LPR363.
6. Remove ClockGen 3362 circuits.
7. Unstuff Finger Printer Connector.
- 8.

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Zack Kuo</i>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet 69 of 100	



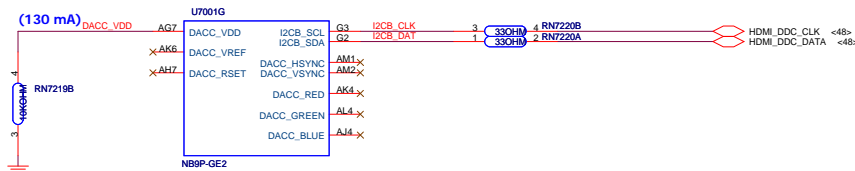
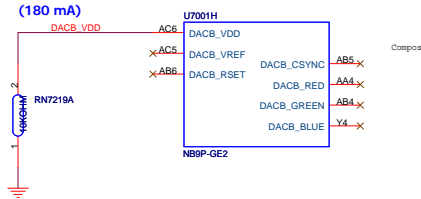
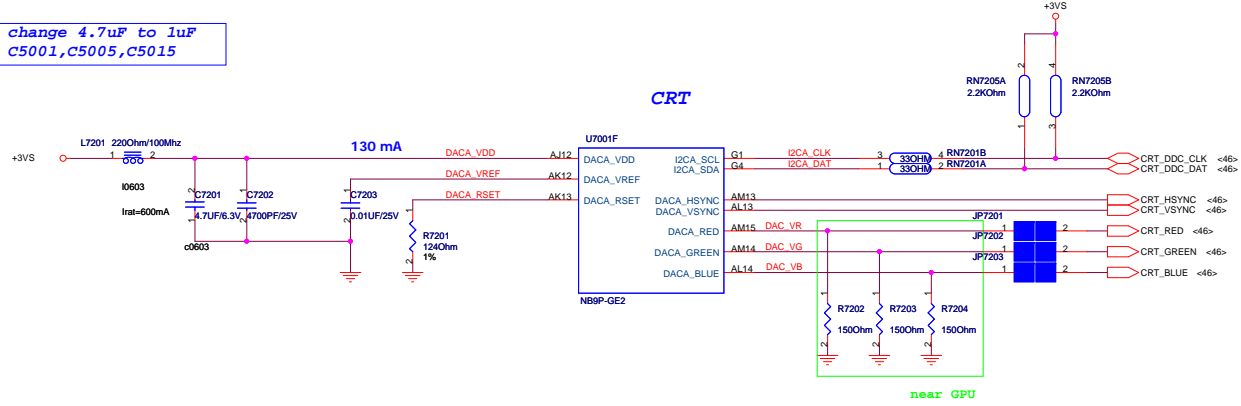
PEX=> From NB
EXP: VGA Card to NB



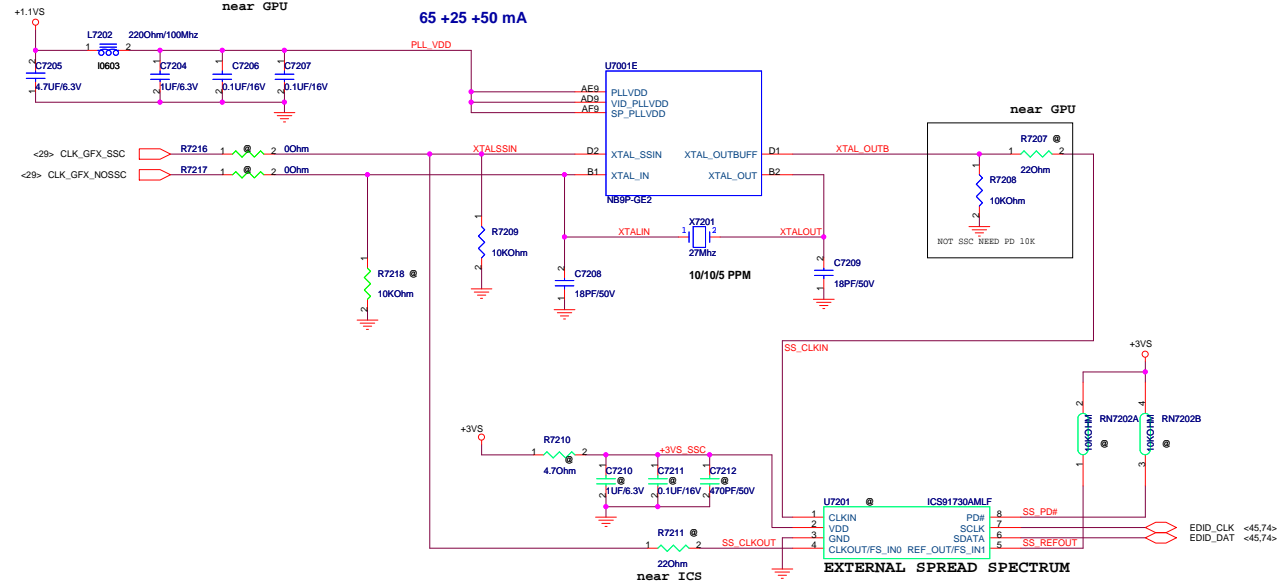


PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <OrgAddr1>	
Size	Project Name	F83Vf	Rev
C	P/N	<OrgAddr2>	1.1
Date: Thursday, July 16, 2009		Sheet	71 of 100

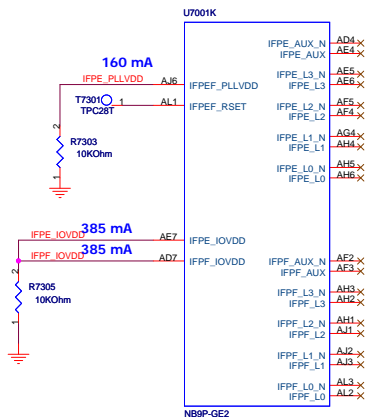
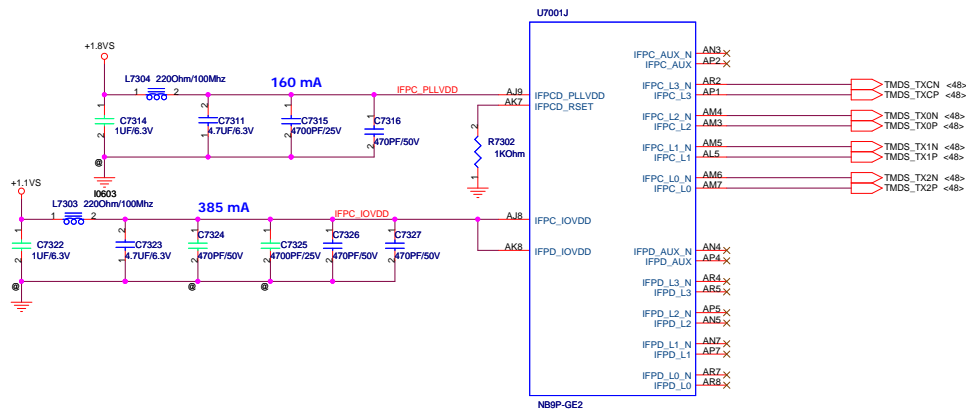
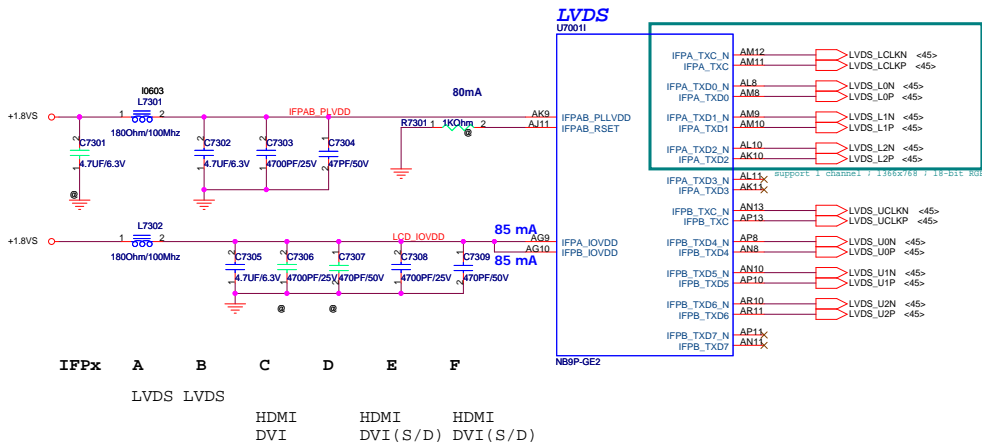
change 4.7uF to 1uF
C5001,C5005,C5015

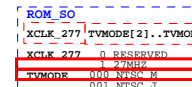
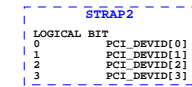
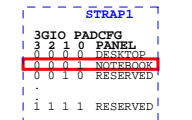
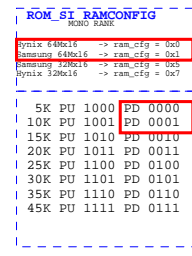
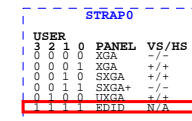
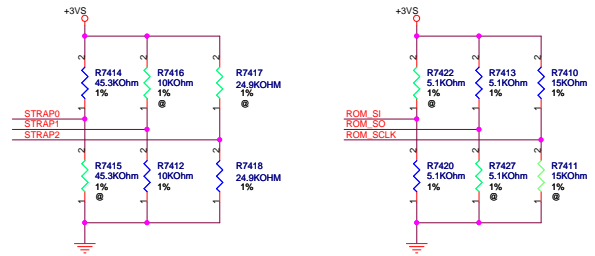
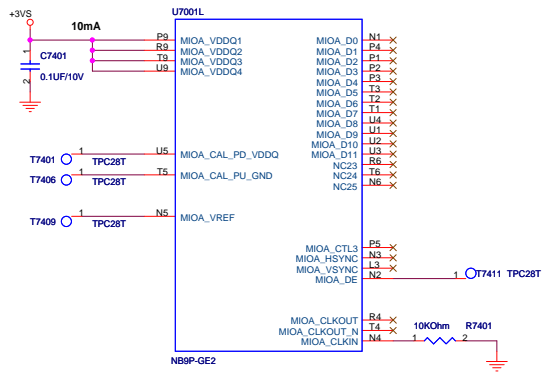


XTAL_IN, XTAL_OUT
3.3V tolerance

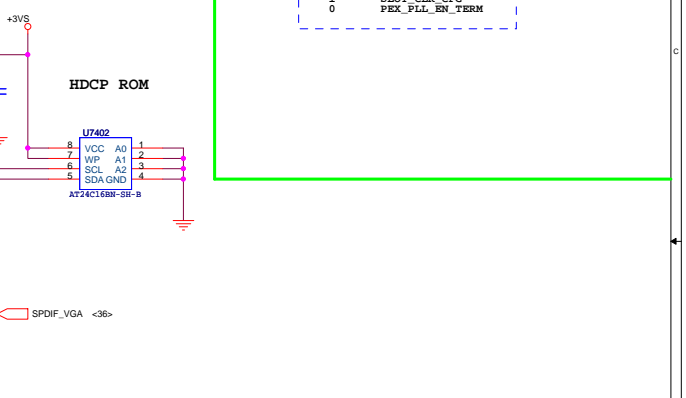
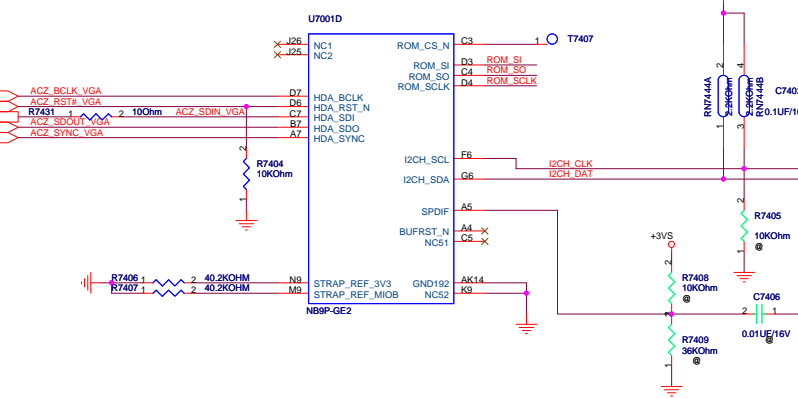
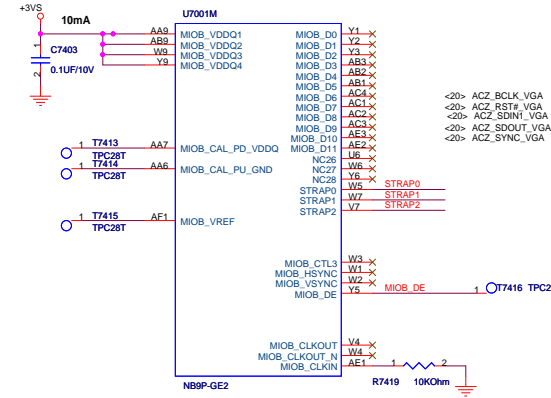
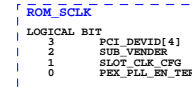


EXTERNAL SPREAD SPECTRUM
Address: 0xD4H



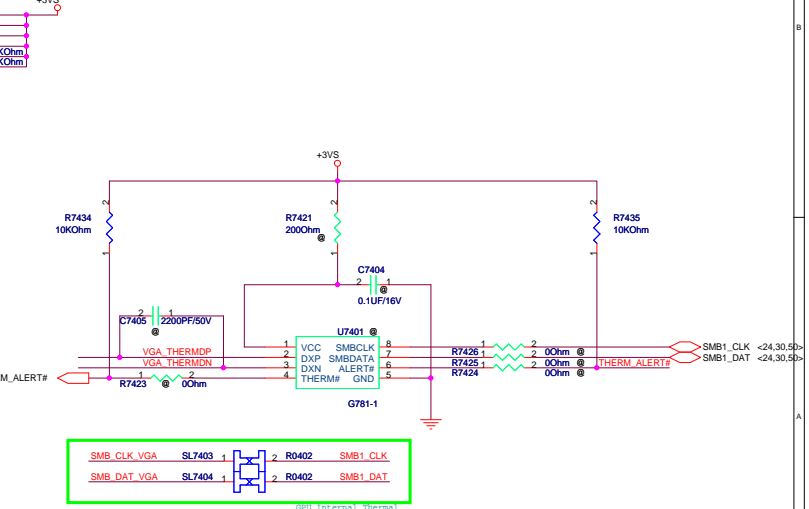
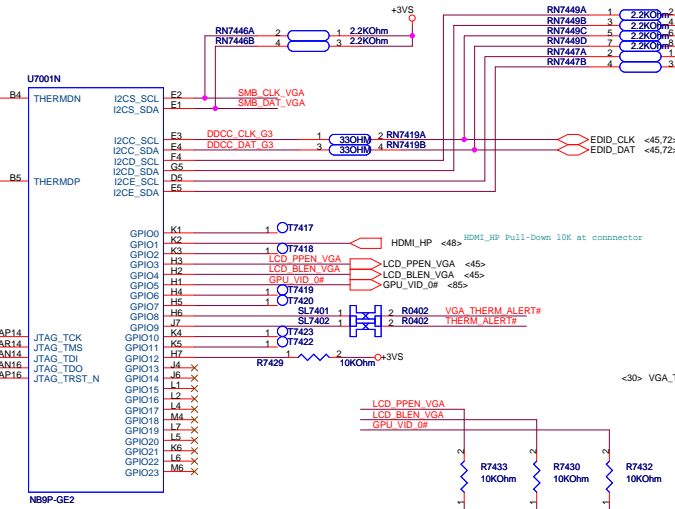


N10P-GE1 : 0x0652
N10P-GV2 : 0x0654
-10100
= PCI_DEVICE[4]{3}{2}{1}{0}

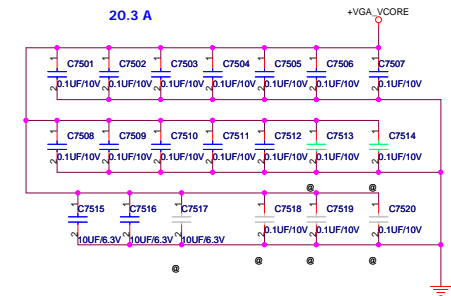
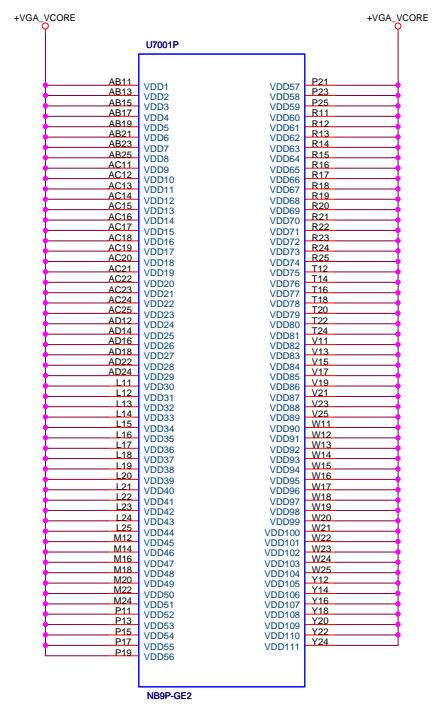
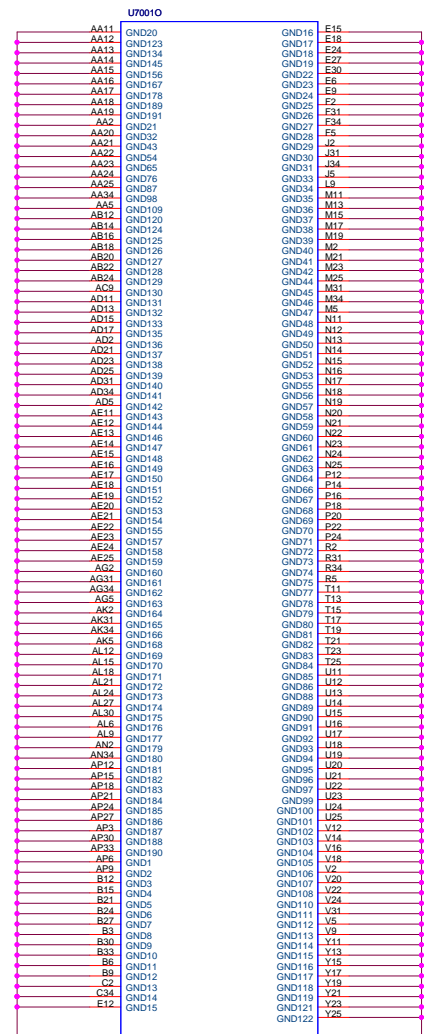


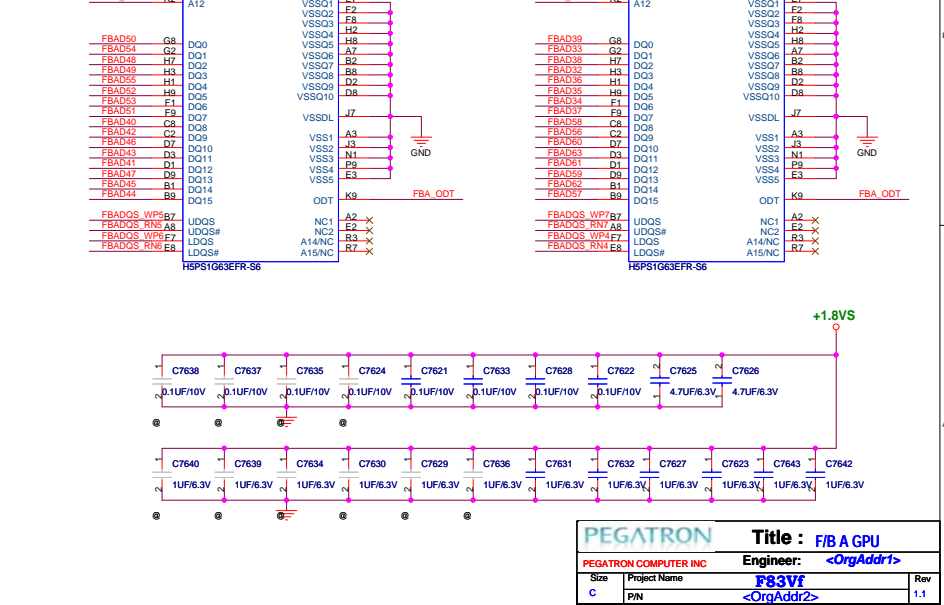
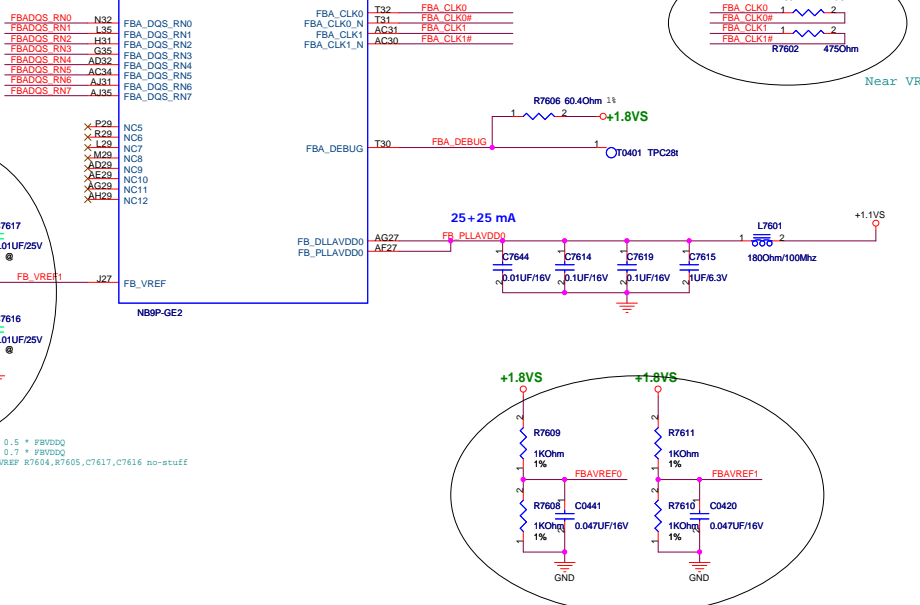
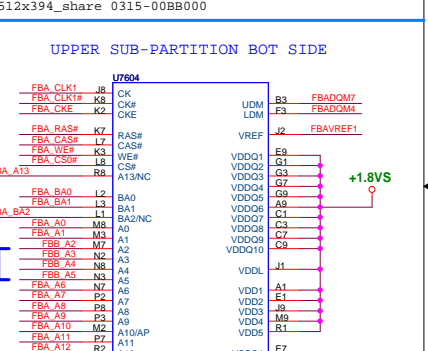
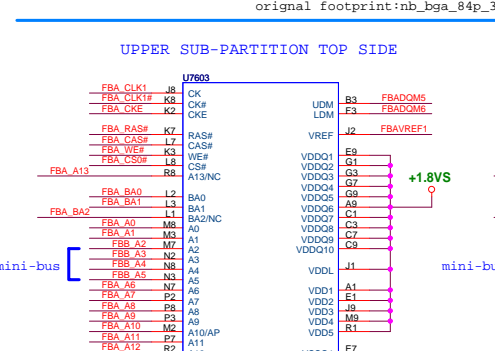
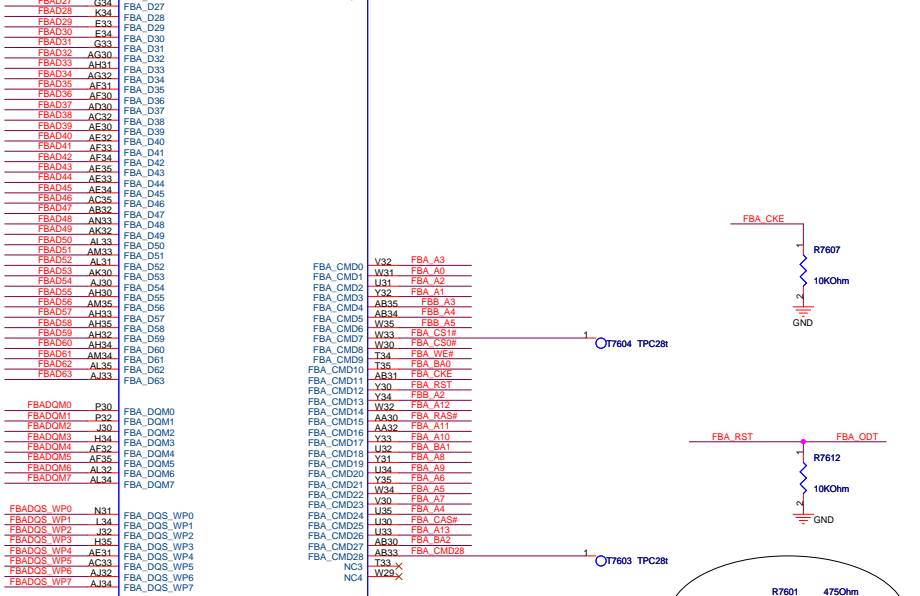
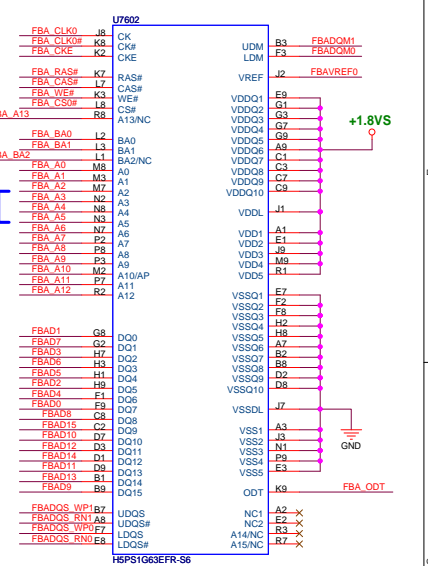
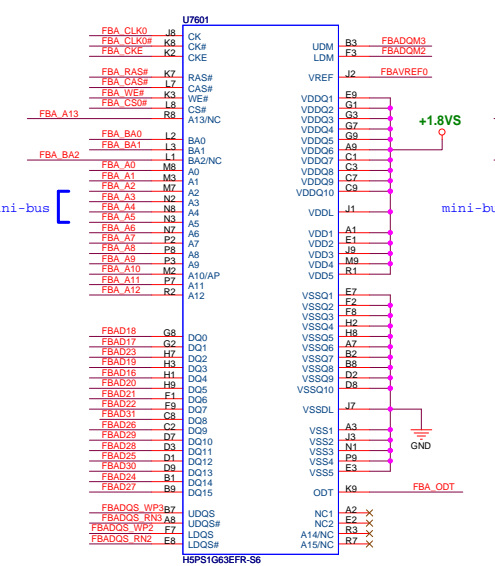
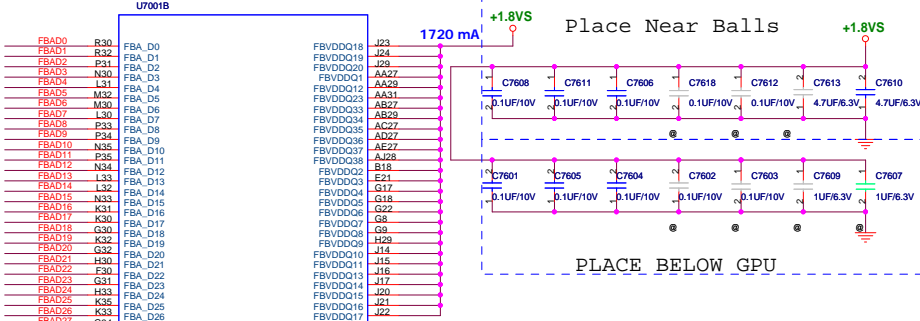
Default GPIO Assignment

GPIO0 - AVAILABLE
GPIO1 - IFPC (HDMI) Hot Plug Detect
GPIO2 - Panel backlight brightness (PWM) (platform use EC PWM)
GPIO3 - Panel power enable
GPIO4 - Panel backlight ON/OFF
GPIO5 - GPU VID0
GPIO6 - GPU VID1
GPIO7 - GPU VID2 / FBVDD VID0
GPIO8 - OverTemp/GPU shutdown
GPIO9 - ThermAlert/Fan PWM
GPIO10 - FBVref Select
GPIO11 - SLI SYNC0
GPIO12 - AC power detect in
GPIO13 - PS_CONTROL0
GPIO14 - PS_CONTROL1
GPIO15 - IFPE Hotplug detect
GPIO16 - Dongle IFPC DVI mode
GPIO17 - Dongle IFPC HDMI mode
GPIO18 - Dongle IFPD DVI mode
GPIO19 - Dongle IFPD HDMI mode
GPIO20 - IFPD Hotplug detect
GPIO21 - NVGEM/ (IFPF Hotplug detect)
GPIO22 - SWAP Ready (SLI)
GPIO23 - AVAILABLE



GPU_VID0	VID0	+VGA_VCORE
Low	0	0.9V
High	1	1.10V





DDR2: VREF = 0.5 * FBVDD
 DDR3: VREF = 0.7 * FBVDD
 GPU Internal VREF: R7604, R7605, C7617, C7616 no-stuff

BOT SIDE

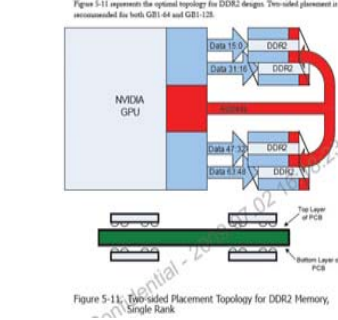
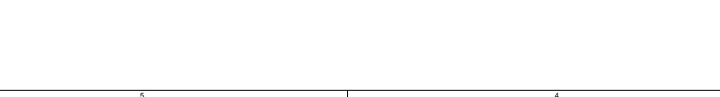
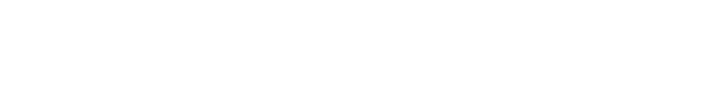
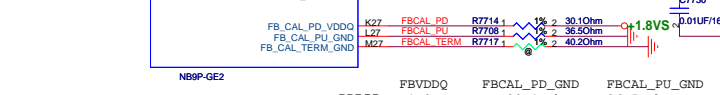
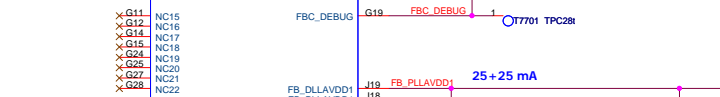
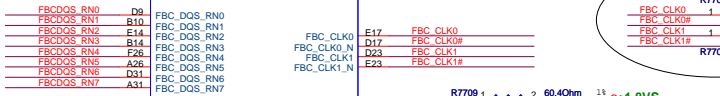
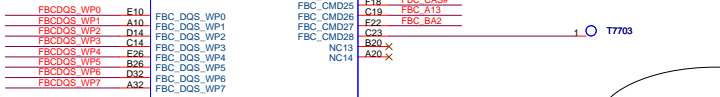
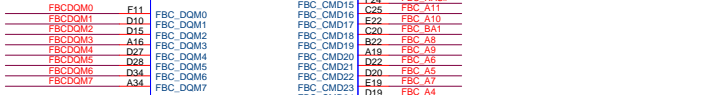
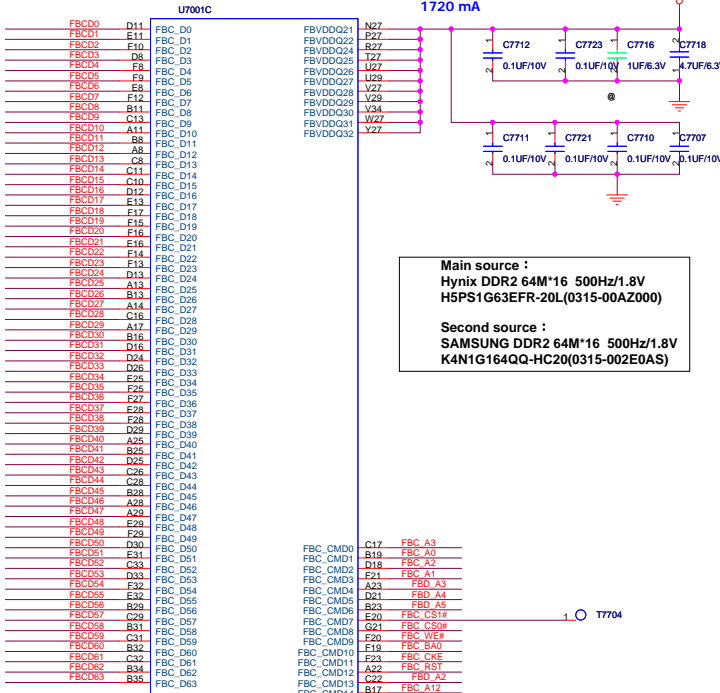
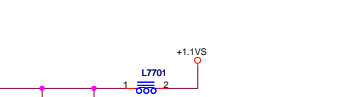
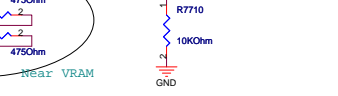
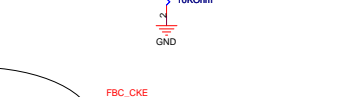
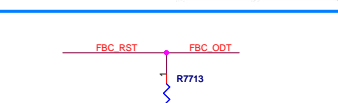
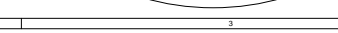
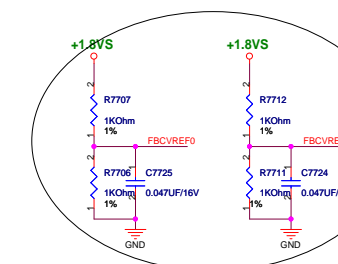


Figure 5-11: Two-sided Placement Topology for DDR2 Memory, Single Rank

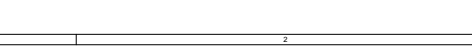
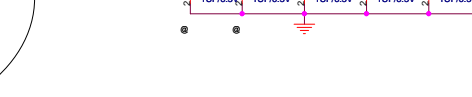
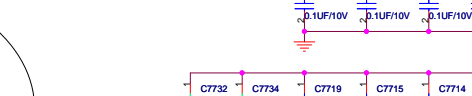
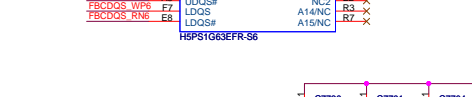
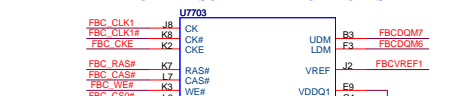
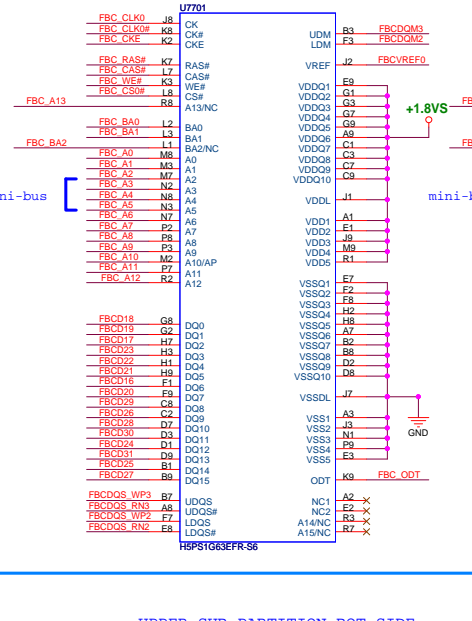
Pins	Mapping Mode A	Pins	Mapping Mode A
FBx_CMD	CS0/CS1	FBx_CMD	CS0/CS1
FBx_CMD0	A3 ¹ (low)	FBx_CMD15	RA5
FBx_CMD1	A0	FBx_CMD16	A11
FBx_CMD2	A2 (low)	FBx_CMD17	A10
FBx_CMD3	A1	FBx_CMD18	BA1
FBx_CMD4	A3 (high)	FBx_CMD19	A8
FBx_CMD5	A4 (high)	FBx_CMD20	A9
FBx_CMD6	A5 (high)	FBx_CMD21	A6
FBx_CMD7	CS1/BA2	FBx_CMD22	A5 (low)
FBx_CMD8	CS0	FBx_CMD23	A7
FBx_CMD9	WE	FBx_CMD24	A4 (low)
FBx_CMD10	BA0	FBx_CMD25	CAS
FBx_CMD11	CKE	FBx_CMD26	A13
FBx_CMD12	RST/ODT	FBx_CMD27	BA2
FBx_CMD13	A2 (high)	FBx_CMD28	RFU0
FBx_CMD14	A12	FBx_CMD29	RFU1
		FBx_CMD30	RFU2



DDR II FBVDDQ 1.8V FBCAL_PD_GND 30.1 ohm FBCAL_PU_GND 36.5 ohm FBCAL_thrm_GND 40.2 ohm

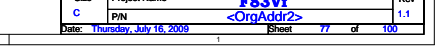
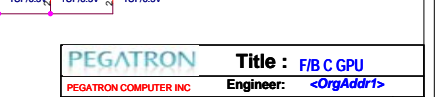
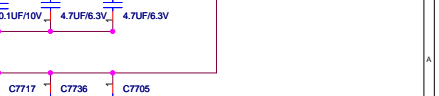
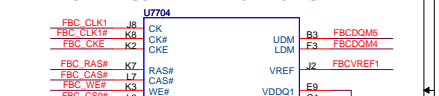
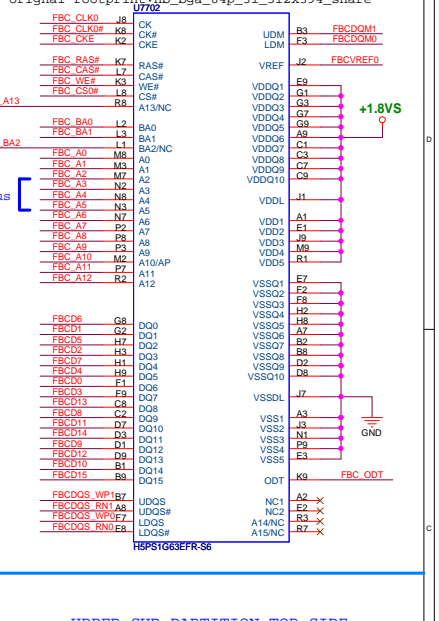


LOWER SUB-PARTITION TOP SIDE

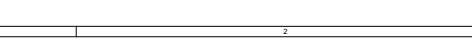
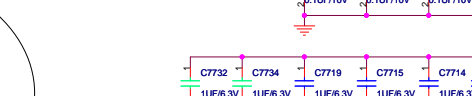
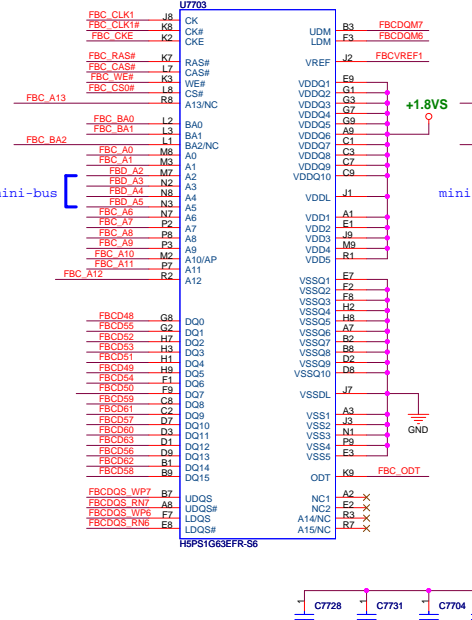


LOWER SUB-PARTITION BOT SIDE

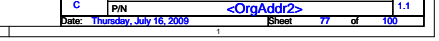
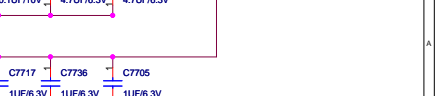
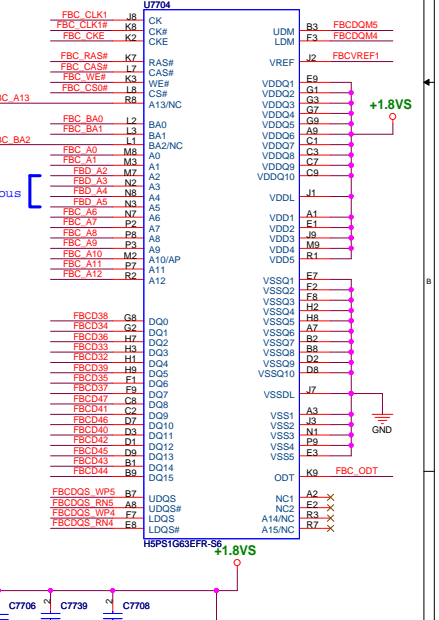
original footprint: nb_bga_84p_31_512x394_share



UPPER SUB-PARTITION BOT SIDE



UPPER SUB-PARTITION TOP SIDE



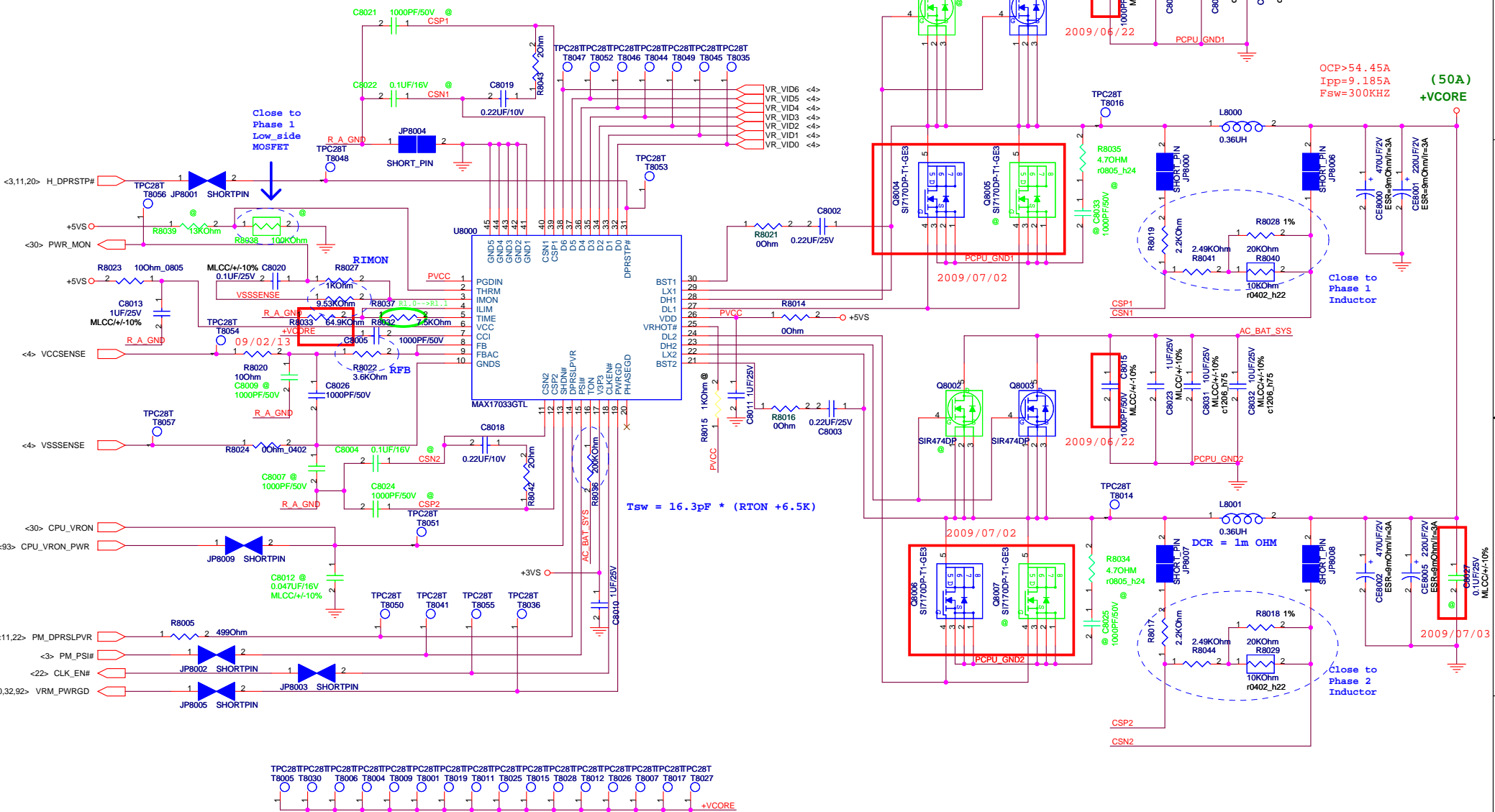
PEGATRON Title: FB_C GPU

PEGATRON COMPUTER INC Engineer: <OrgAddr>

Size	Project Name	F83Vf	Rev
C	PIN	<OrgAddr2>	1.1

Date: Thursday, July 16, 2009 Sheet 77 of 100

$IMON = Gm(IMON) * [(Vcp1 - Vosn1) + (Vcp2 - Vosn2)]$
 $RIMON = 0.9V / [IMAX * Rsense(MIN) * Gm(IMON_MIN)]$
 $Gm(IMON) = 2.4mS, Gm(IMON_MIN) = 2.36mS$



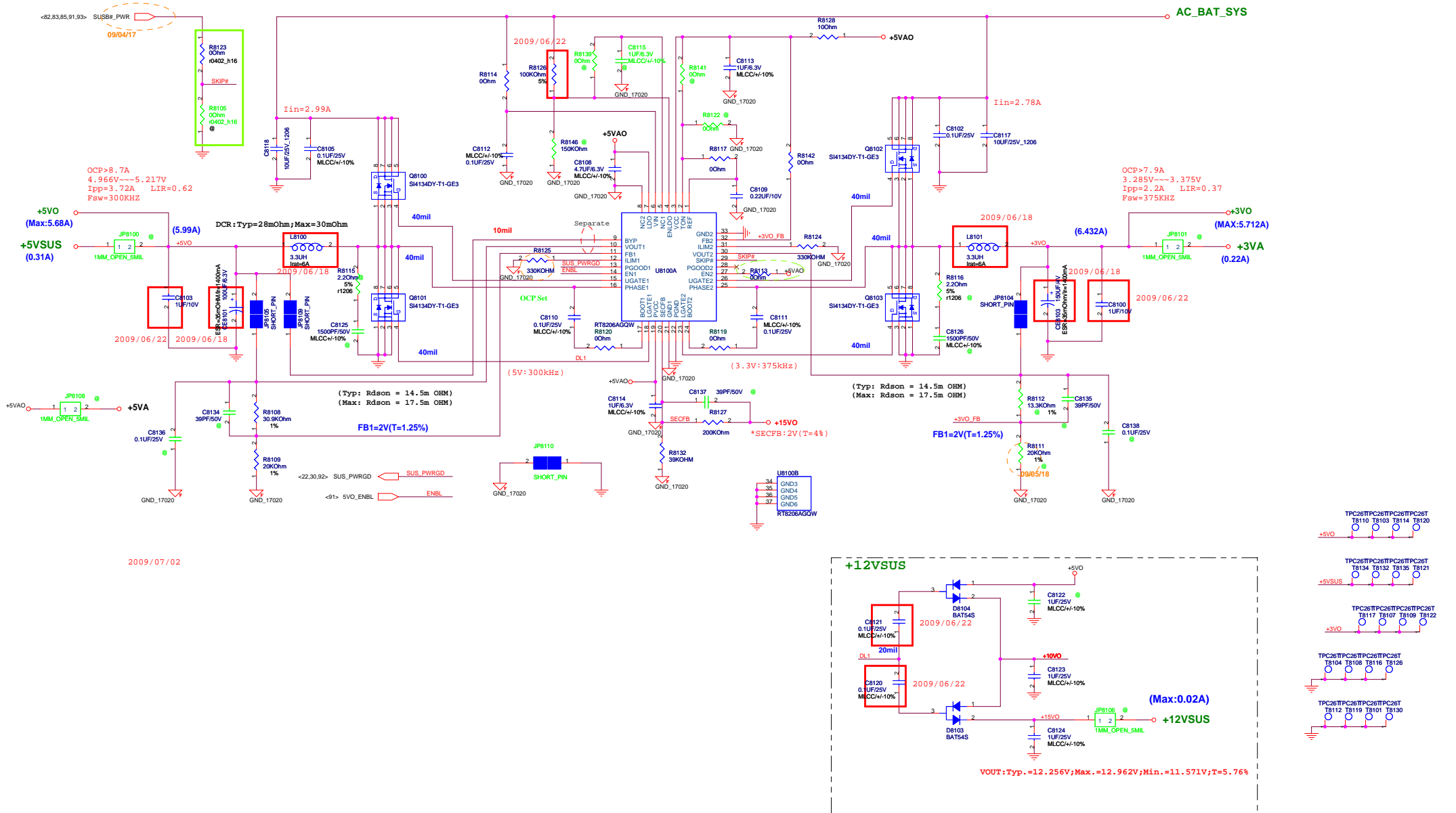
$RFB = Rdroop / (Rsense * Gm)$
 $Gm = 600uS, R8022 \text{ for load lin}$

ASUS		Title : POWER_VCORE	
-<OrgName>		Engineer: Anysc	
Size	Project Name	Rev	
Custom	F83	1.0	
Date: Thursday, July 16, 2009		Sheet 80 of 94	

SKIP:
 GND : DEM operation;
 REF : Ultrasonic Mode operation;
 VCC : PWM operation.

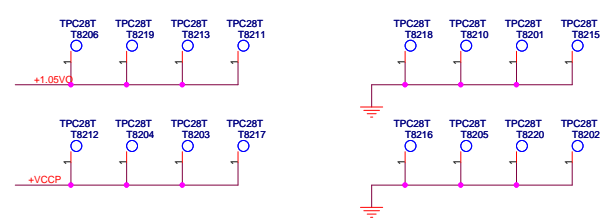
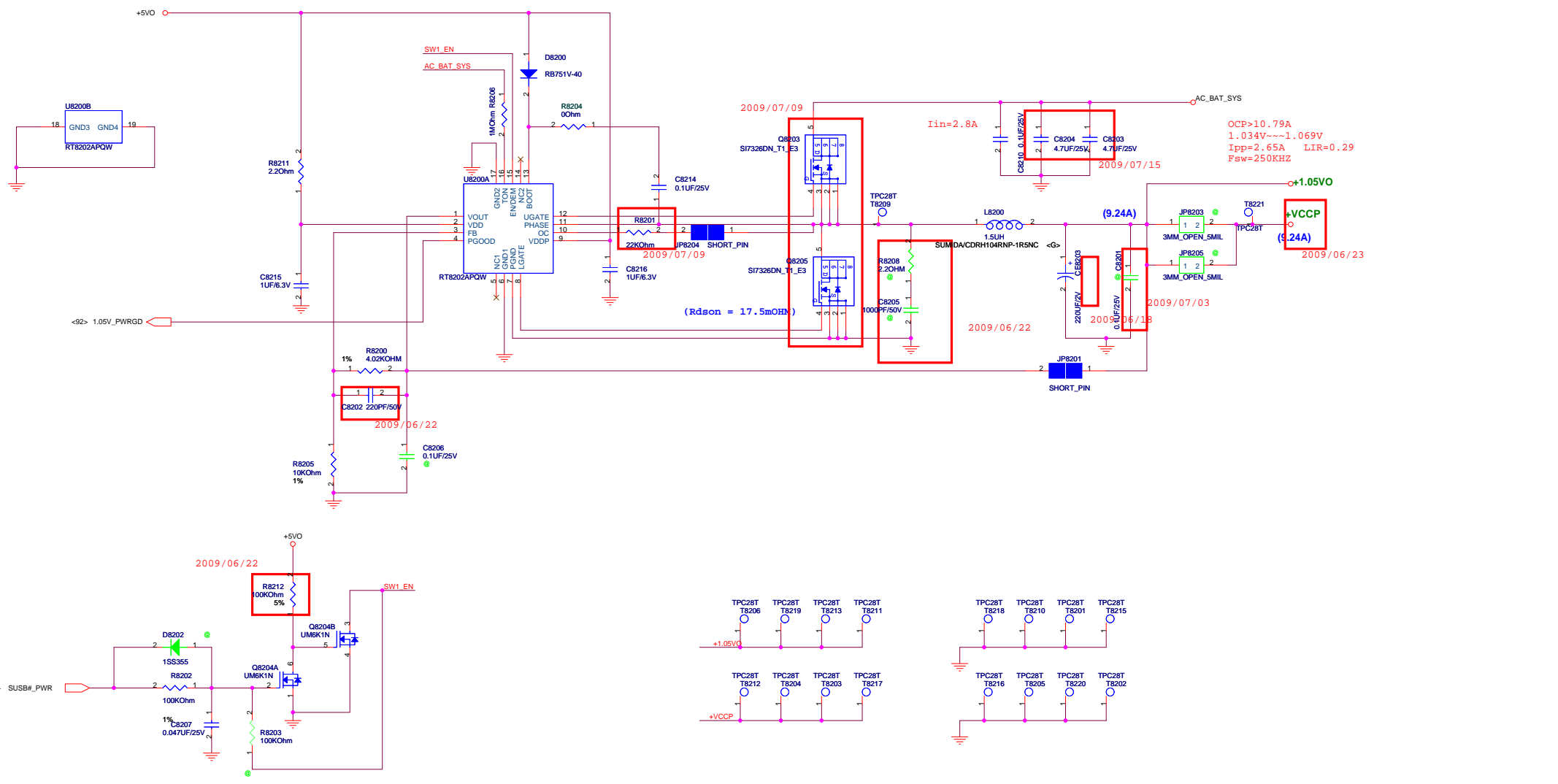
TON : (5V/3.3V)
 VCC : (200kHz/250kHz)
 REF : (300kHz/375kHz)
 GND : (400kHz/500kHz)

VENLDO:
 Rising Edge:Max:2V;Typ:1.6V;Min:1.2V
 Falling Edge:Max:1.06V;Typ:1V;Min:0.94V



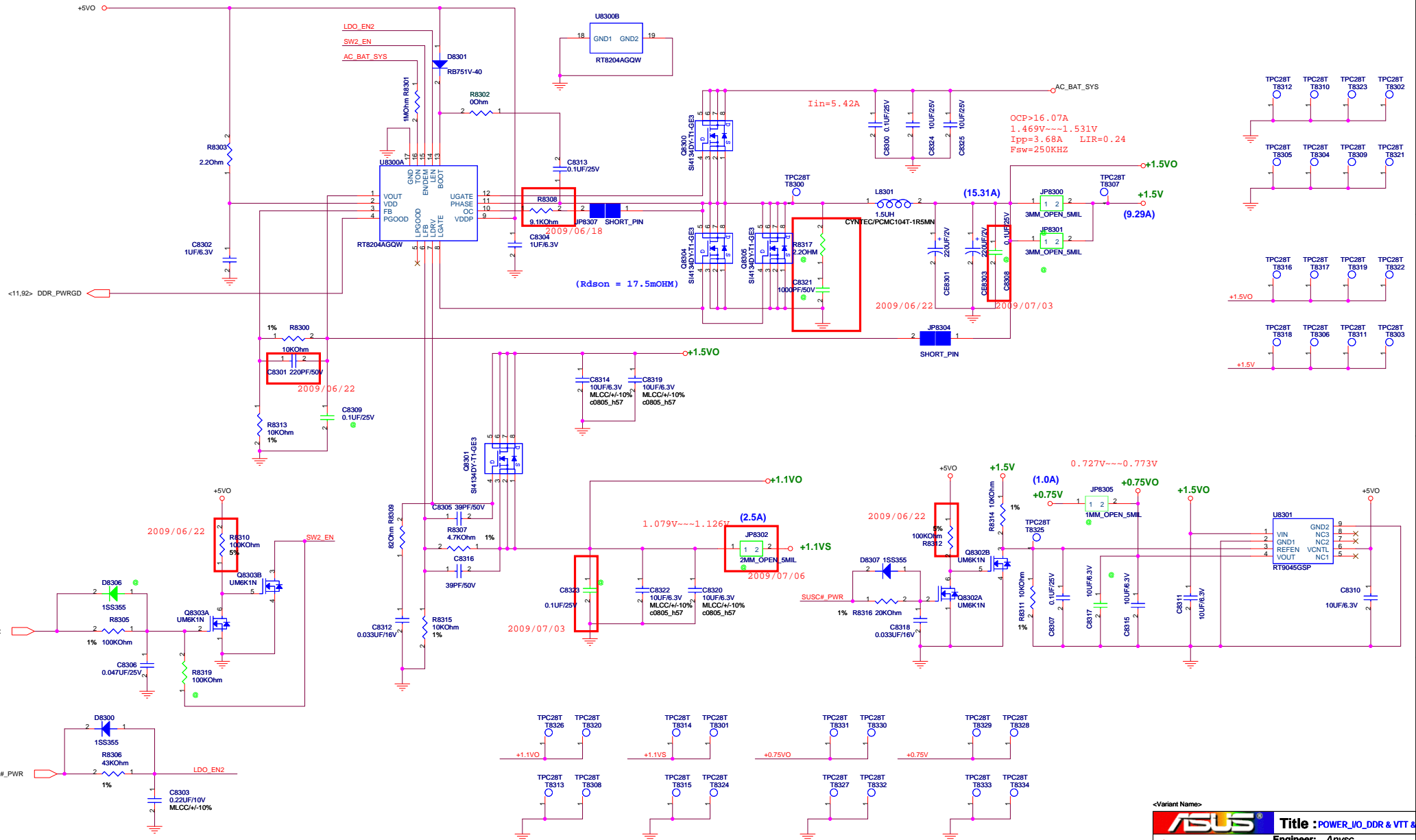
TOTAL COUNT : 38 PCS

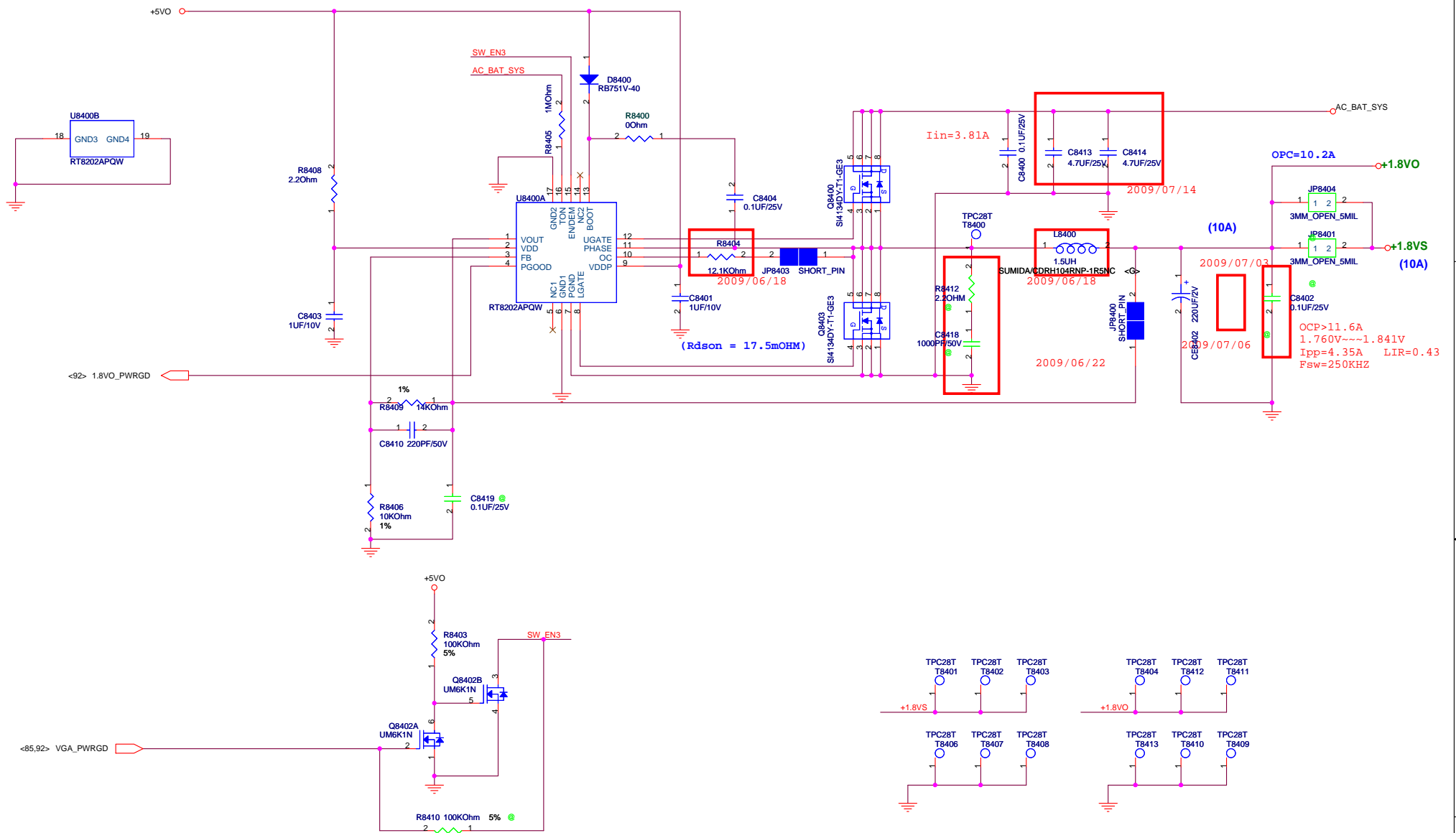
ASUS		Title : POWER_SYSTEM	
-OrigName-		Engineer: Anysc	
Size	Project Name	Rev	
Custom	F83	1.0	
Date: Thursday, July 16 2009		Sheet 81 of 84	



<Variant Name>

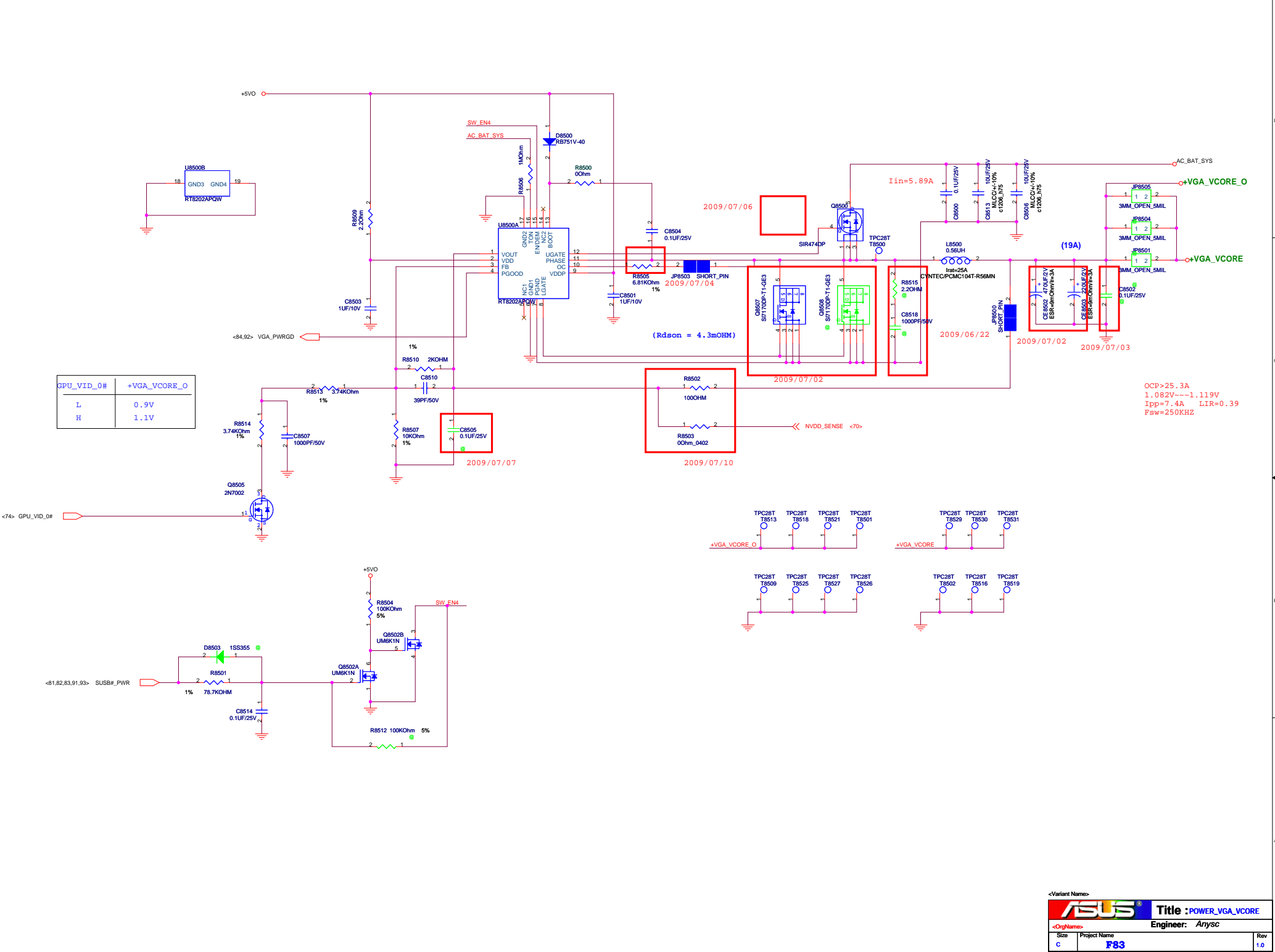
		Title : POWER_IO_VCCP
<OrigName>	Engineer: Anysc	
Size	Project Name	Rev
Custom	F83	1.0
Date: Thursday, July 16, 2009	Sheet	82 of 94





<Variant Names>

ASUS		Title : POWER_I/O_1.8V	
<OrgName>		Engineer: Anysc	
Size	Project Name	Rev	
Custom	F83	1.0	
Date: Thursday, July 16, 2009		Sheet 84 of 94	



GPU_VID_0#	+VGA_VCORE_O
L	0.9V
H	1.1V

OCP > 25.3A
 1.082V --- 1.119V
 Ipp = 7.4A LIR = 0.39
 Fsw = 250KHZ

5

4

3

2

1

b

D

c

C


B

B

A

A

<Variant Name>

		Title : <i>NA</i>
<OrgName>		Engineer: <i>Anyisc</i>
Size <i>Custom</i>	Project Name F83	Rev 1.0
Date: <i>Thursday, July 16, 2009</i>		Sheet 86 of 94

5

4

3

2

1

b

b

c

c


b

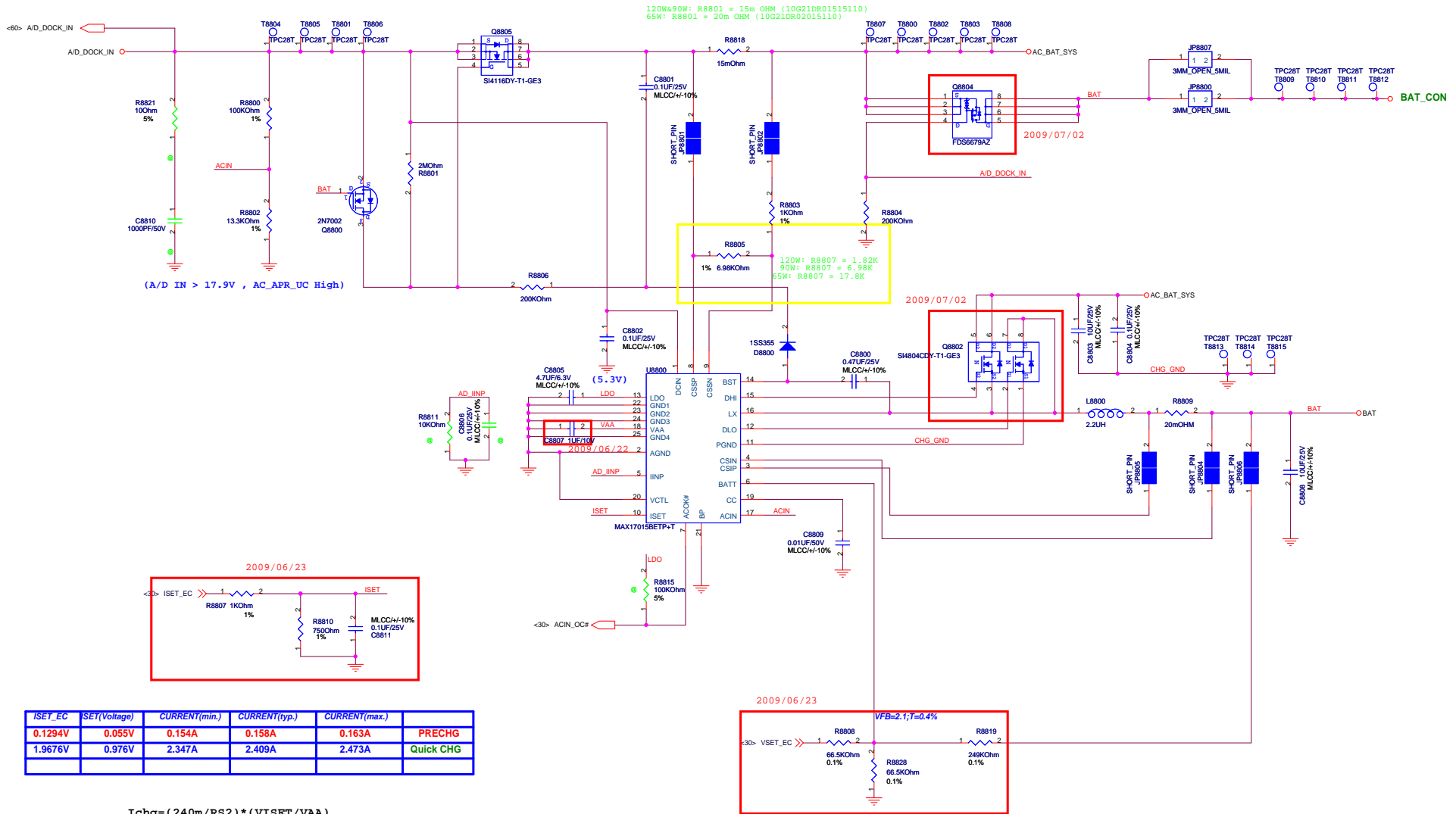
b

a

a

<Variant Name>

		Title : N/A
<OrgName>		Engineer: Arjisc
Size	Project Name	Rev
C	F83	1.0
Date: Thursday, July 16, 2009		Sheet 87 of 94



ISET_EC	ISET(Voltage)	CURRENT(min.)	CURRENT(typ.)	CURRENT(max.)	
0.1294V	0.055V	0.154A	0.158A	0.163A	PRECHG
1.9676V	0.976V	2.347A	2.409A	2.473A	Quick CHG

$I_{chg} = (240m/RS2) * (V_{ISET}/VAA)$
 $I_{chg} = (240m/20m) * (0.055/4.2) = 0.157A$
 $I_{chg} = (240m/20m) * (0.865/4.2) = 2.4714A$

VCTL connect to GND, VFB=2.1V
VBA=2.1*(R8819+R8828)/R8828

VSET_EC	BAT(min.)	BAT(typ.)	BAT(max.)
1.3948V	12.511V	12.604V	12.696V

$12.641V(\min) < VBAT - 12.515V(\text{Typ}) < 12.768V(\text{Max})$

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : N/A

<OrgName> Engineer: Anysc

Size	Project Name	Rev
Custom	F83	1.0


Date: Thursday, July 16, 2009 Sheet 89 of 94

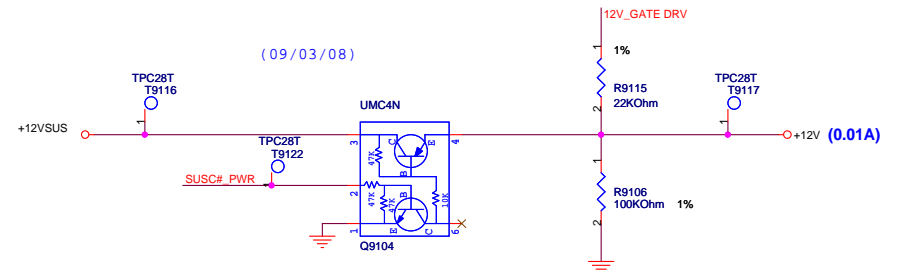
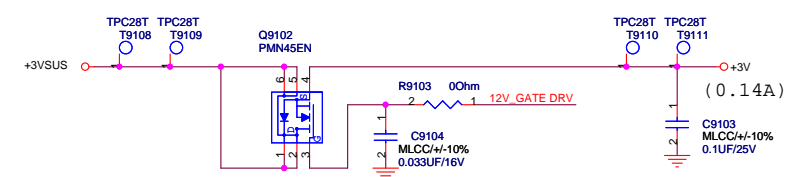
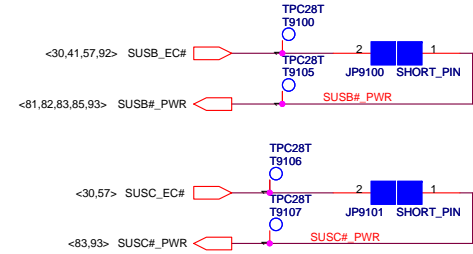
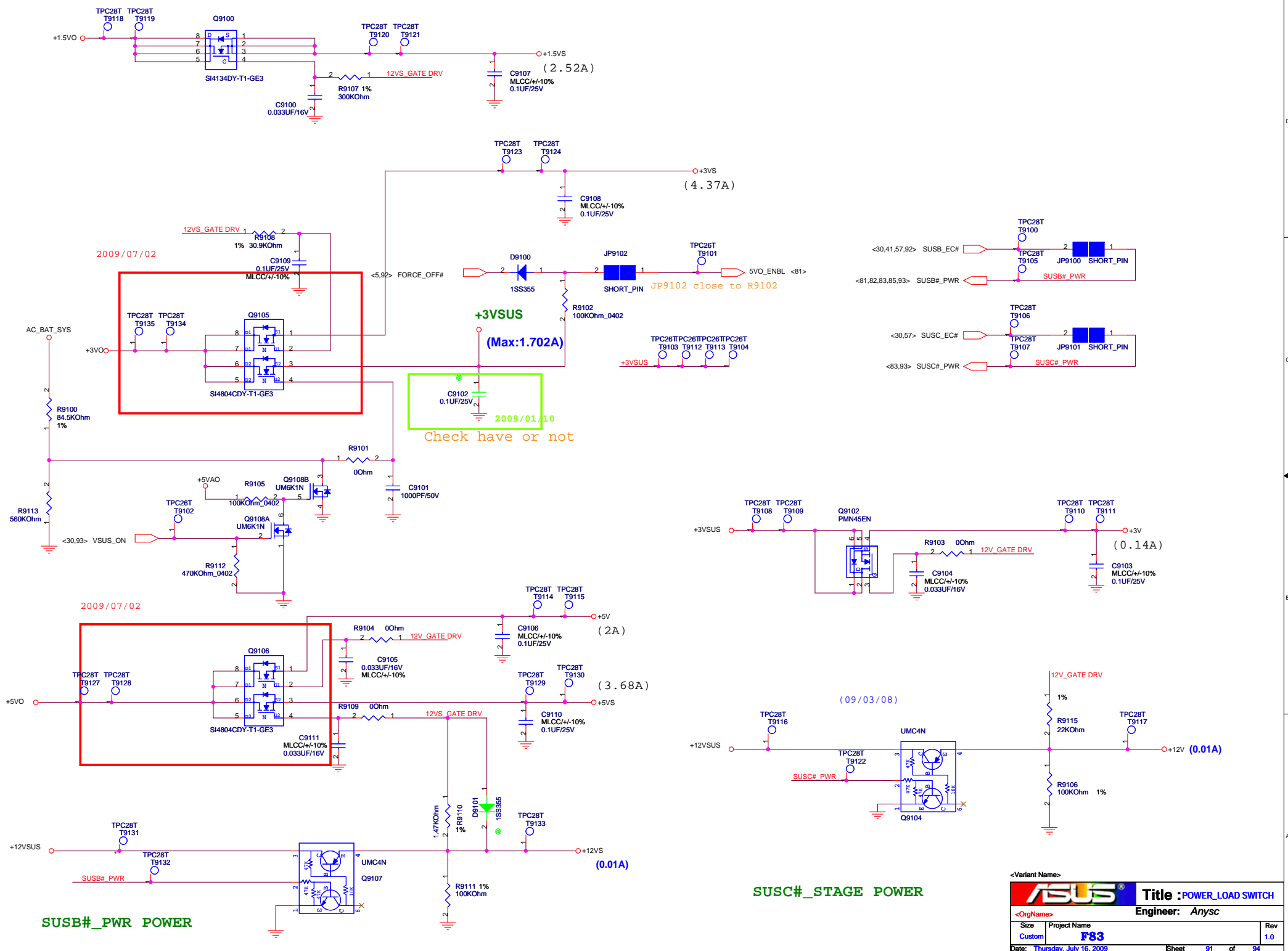
BATTERY IN DETECT

2009/07/08
delete batt detect



<Variant Name>

		Title :POWER_DETECT	
<OrgName>		Engineer: Anysc	
Size	Project Name	Rev	
Custom	F83	1.0	
Date: Thursday, July 16, 2009		Sheet	90 of 94

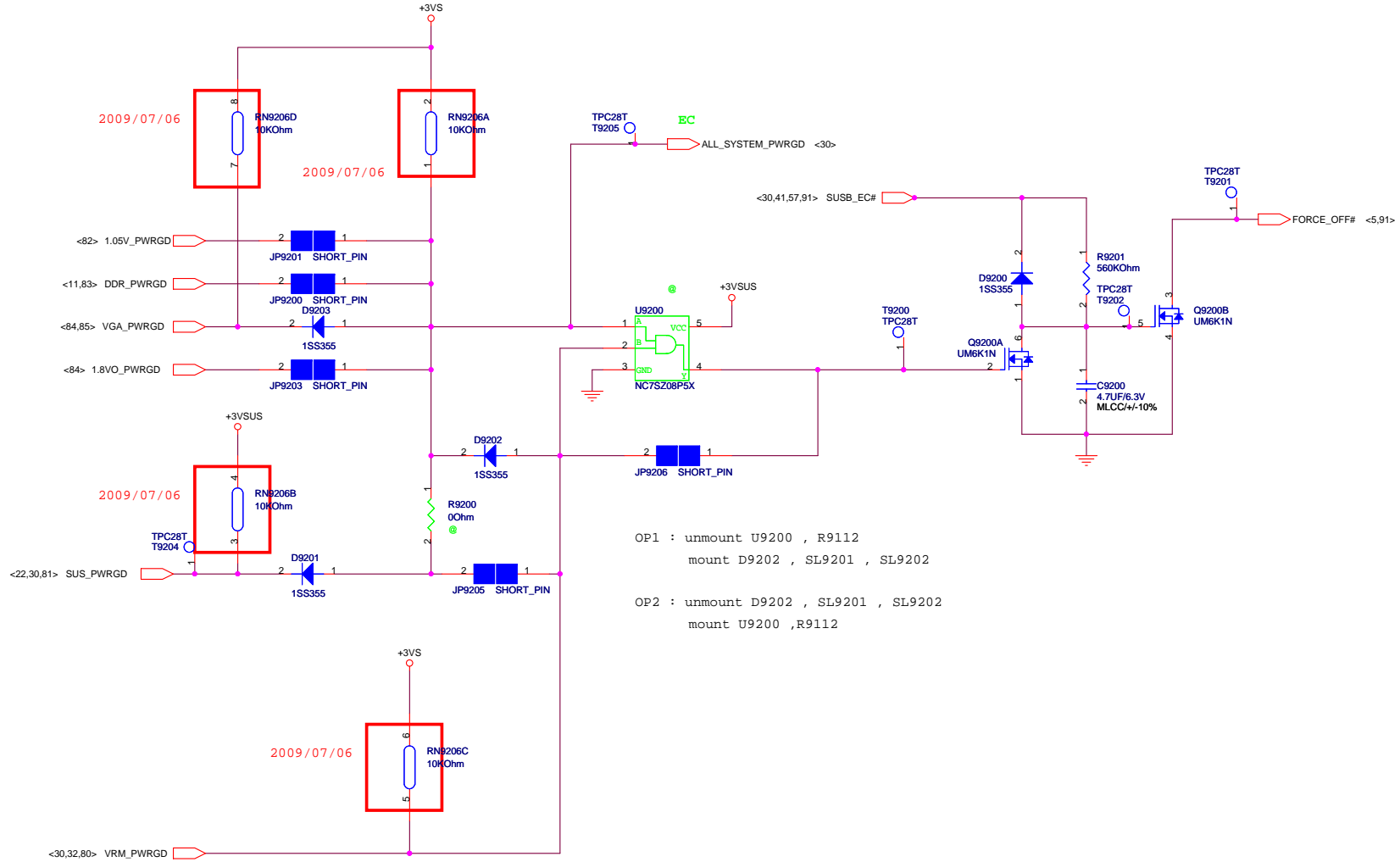


SUSB#_PWR POWER

SUSC#_STAGE POWER

ASUS		Title : POWER_LOAD SWITCH	
-<OrgName>		Engineer: Anysc	
Size	Project Name	Rev	
Custom	F83	1.0	
Date: Thursday, July 16, 2009	Sheet	91	of 94

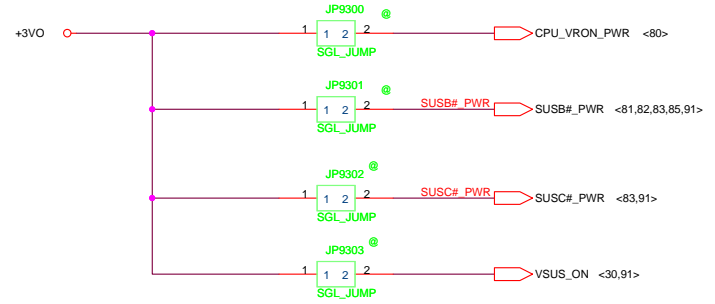
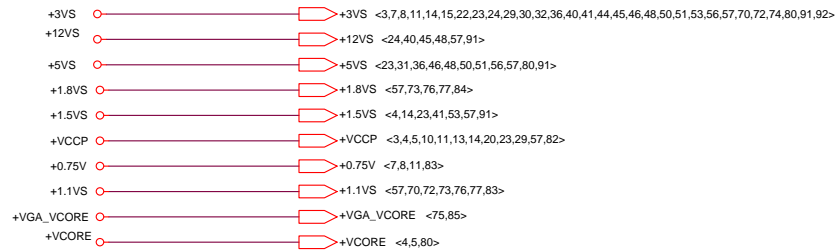
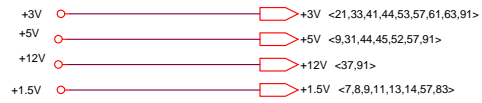
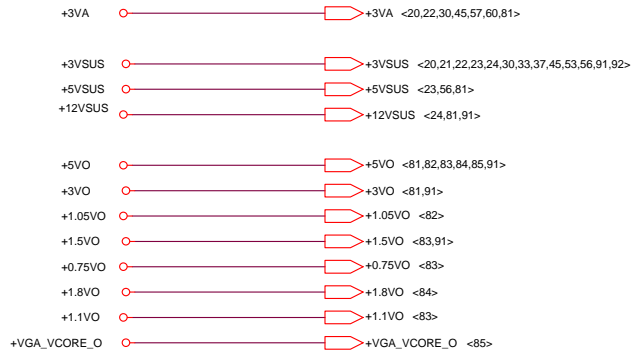
POWER GOOD DETECTOR



OP1 : unmount U9200 , R9112
 mount D9202 , SL9201 , SL9202

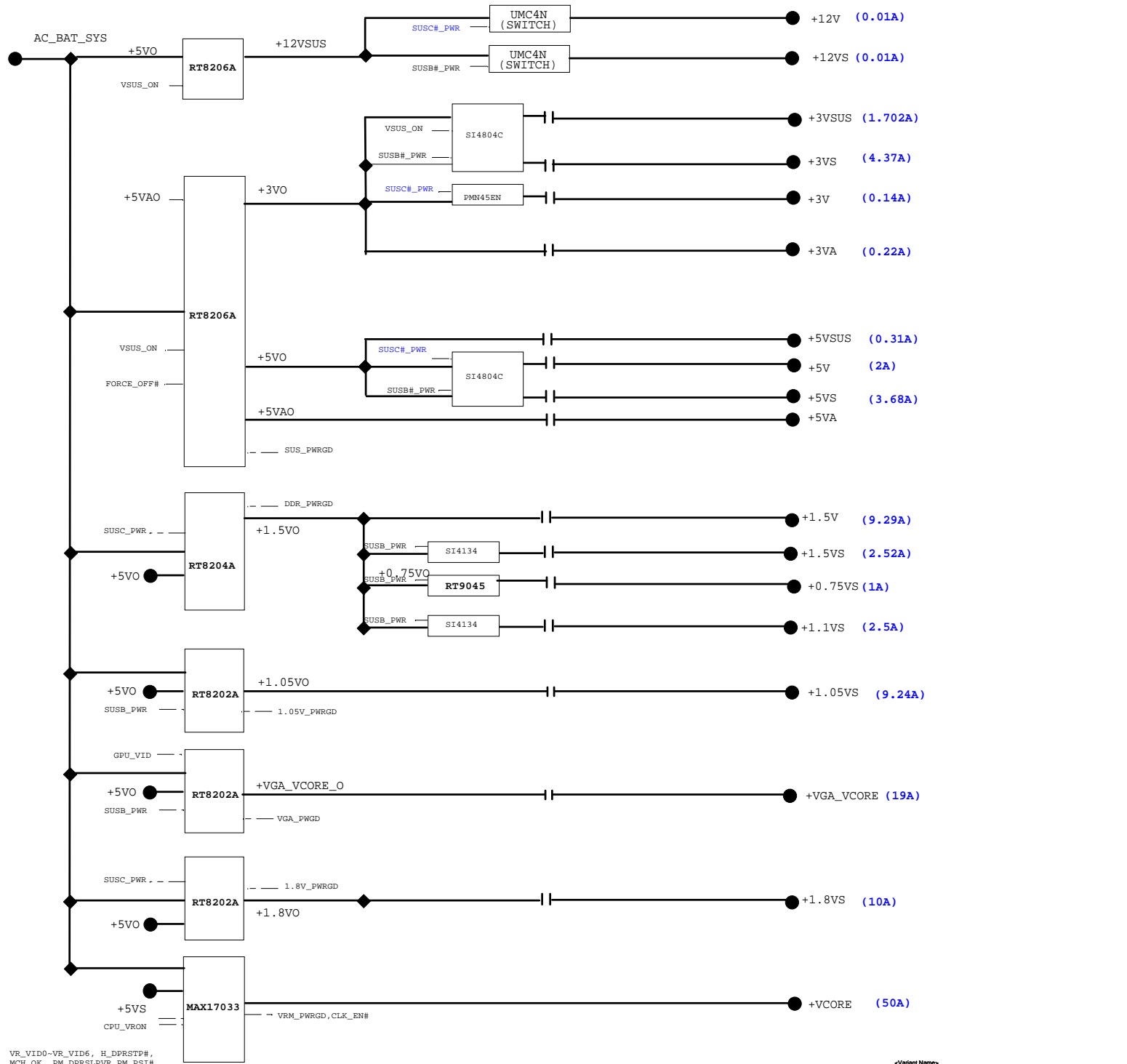
OP2 : unmount D9202 , SL9201 , SL9202
 mount U9200 ,R9112

FOR POWER TEST



<Variant Name>

ASUS		Title : POWER_SIGNAL	
<OrgName>		Engineer: Anysc	
Size	Project Name	Rev	
Custom	F83	1.0	
Date: Thursday, July 16, 2009		Sheet 93 of 94	



VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DFRSLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#



PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Colin Chang</i>	
Size	Project Name	Rev	
C	P/N	1.0	
Date: Thursday, July 16, 2009		Sheet	98 of 100



PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: <i>Colin Chang</i>	
Size	Project Name	Rev	
C	P/N	1.0	
Date: Thursday, July 16, 2009		Sheet	99 of 100