

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Intel
Crestline + ICH8-M core logic
IBT00 LA-3262P Discrete VGA (M64)

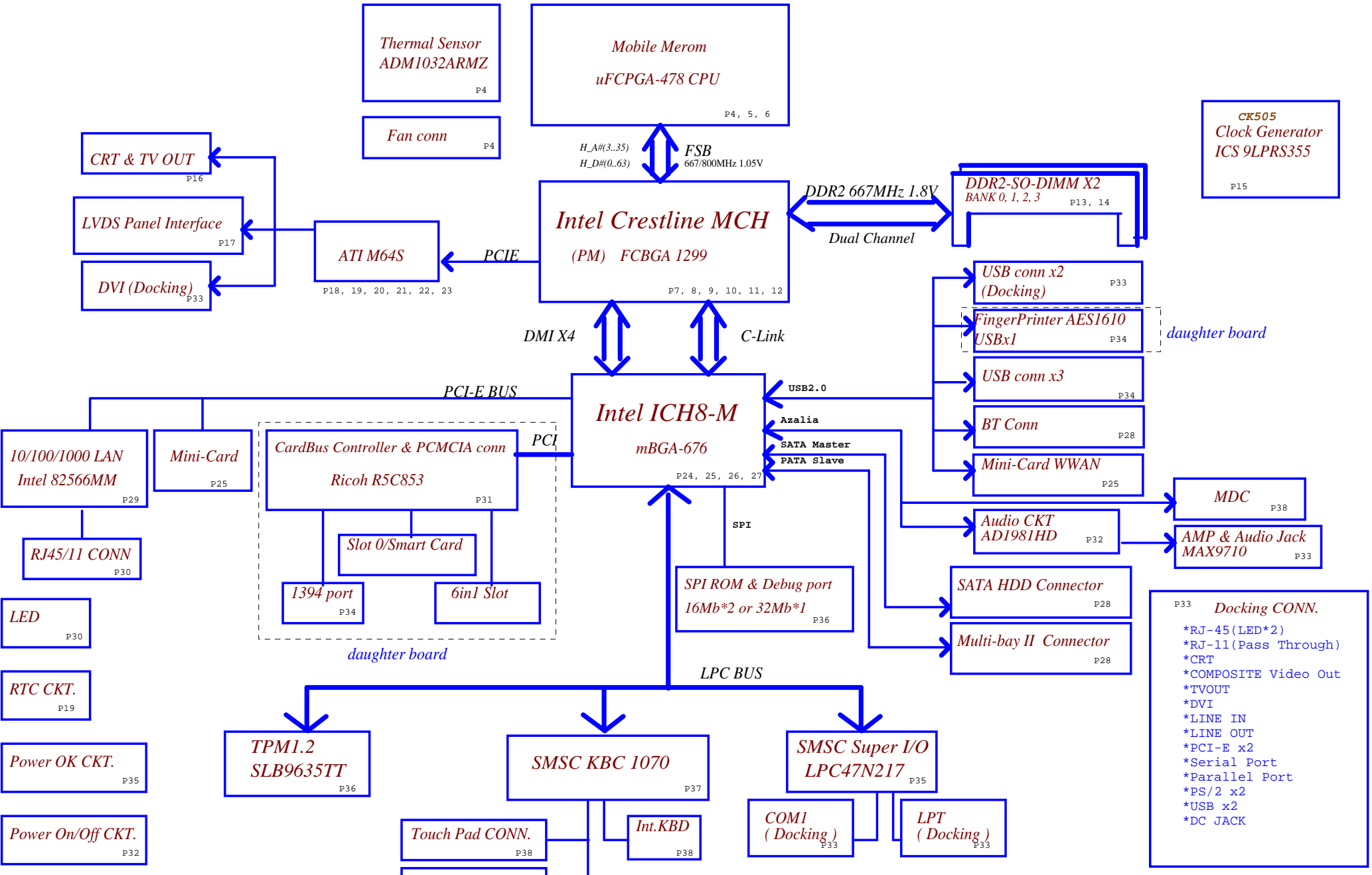
2007-08-02

REV:1A



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Chimay Discrete



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Block Diagram

Voltage Rails O MEANS ON X MEANS OFF

power plane / State	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/ Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

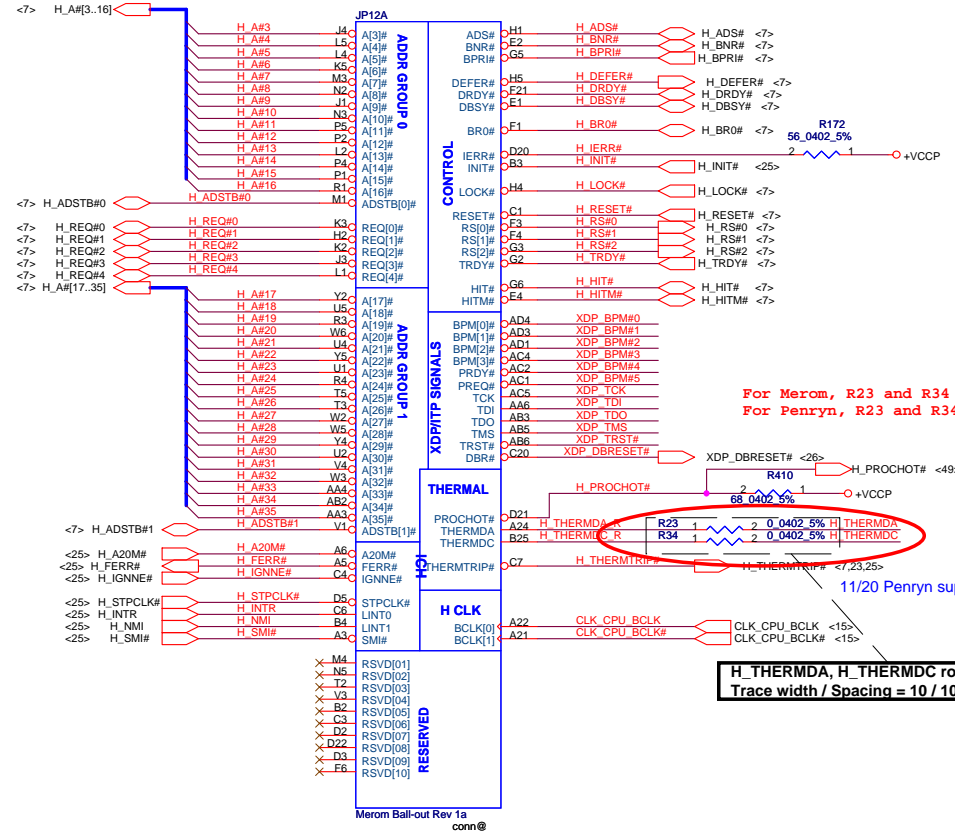
PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS & 1394	AD22	2	C,D,E,G

DMA Channel	Device
DMA0	MODEM / LAN
DMA1	ECP
DMA2	FLOPPY DISK
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

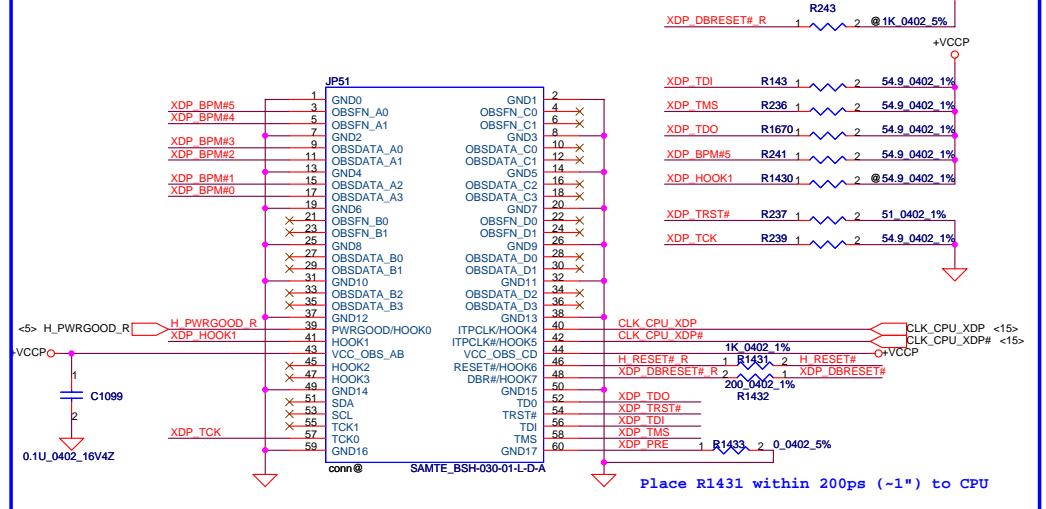
USB PORT#	Destination
0	Walk-up0 (Right side)
1	Fingerprint
2	Reserve
3	WWAN
4	Walk-up1 (Left Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Reserve
8	Docking
9	Docking

I/O	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2),LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Momem,LAN
11	Mass storage control/ PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface,HDD
15	Secondary IDE innterface,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Driver for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family)USB Universal Host Controll
18	Intel 82801H (ICH8 Family)USB Universal Host Controll Ricoh R5C853 Cardbus Control Ricoh R5C853 Integrates FlashMedia Control Ricoh R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family)PCI Express Root Port - 27D6 Intel 82801H (ICH8 Family)USB Universal Host Controll
20	Intel 82801H (ICH8 Family)USB Universal Host Controll Intel 82801H (ICH8 Family)USB2 Enhanced Host Controll
21	Intel 82801H (ICH8 Family)USB Universal Host Controll
22	SDA Standard Compliant SD Host Controller
23	HP Mobile Data Protection Sensor

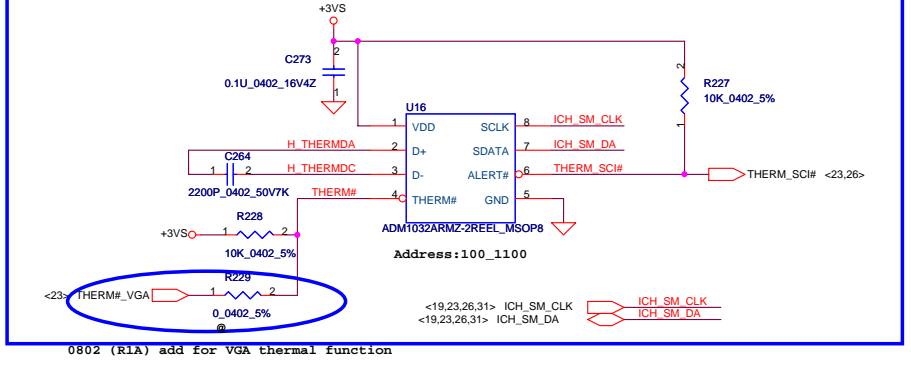


XDP Connector

layout note: Change R237 to 649 ohm if using XTP to ITP adapter



Thermal Sensor ADM1032ARMZ

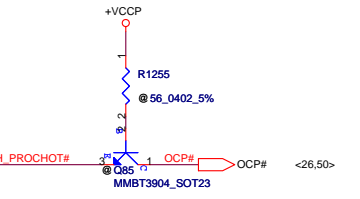
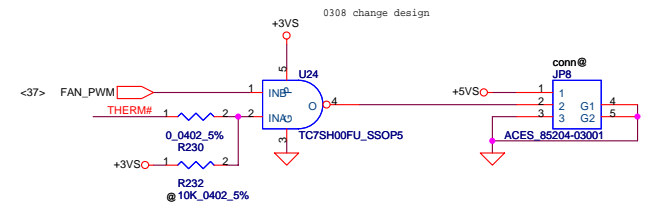


For Merom, R23 and R34 are 0ohm
For Penryn, R23 and R34 are 100ohm.

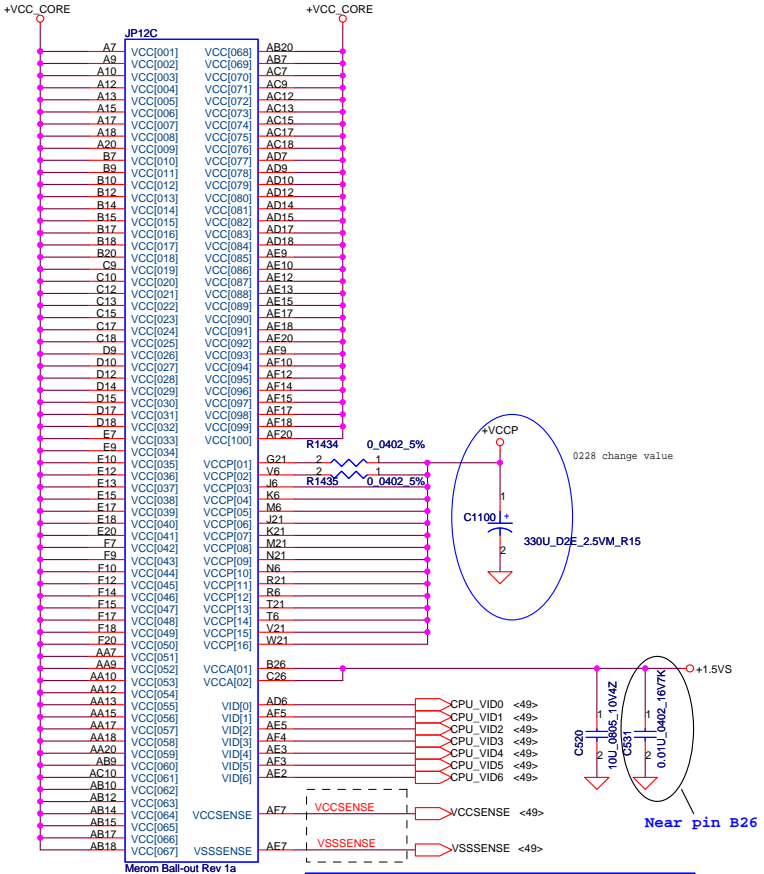
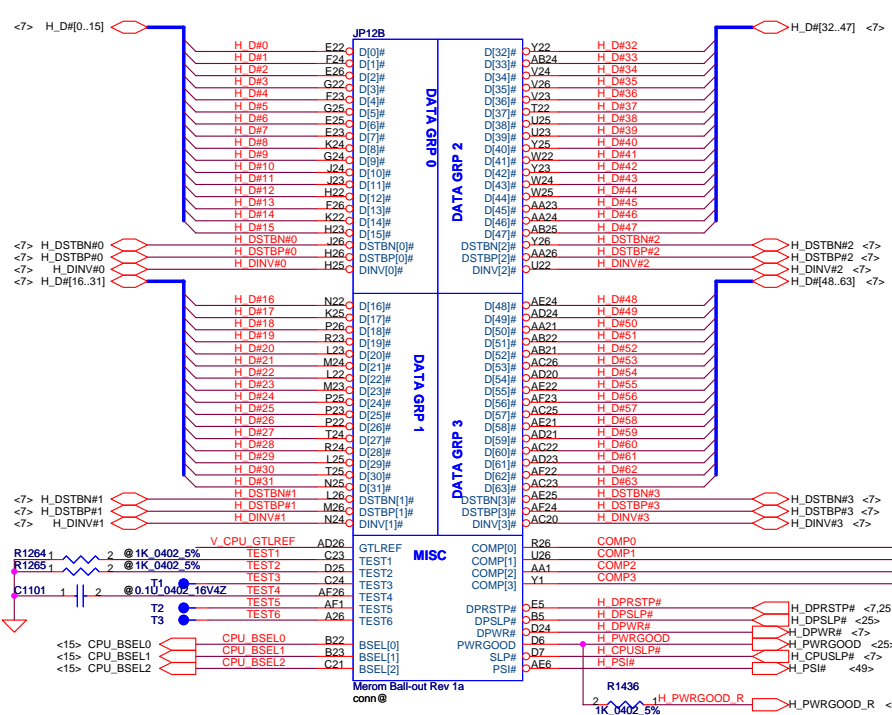
11/20 Penryn support to add R23,R34

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

PWM Fan Control circuit



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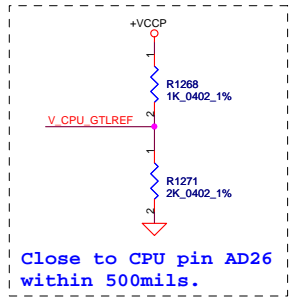


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

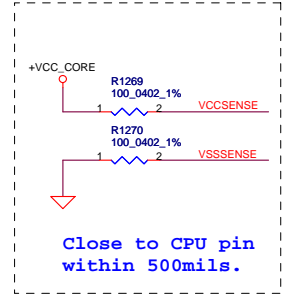
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



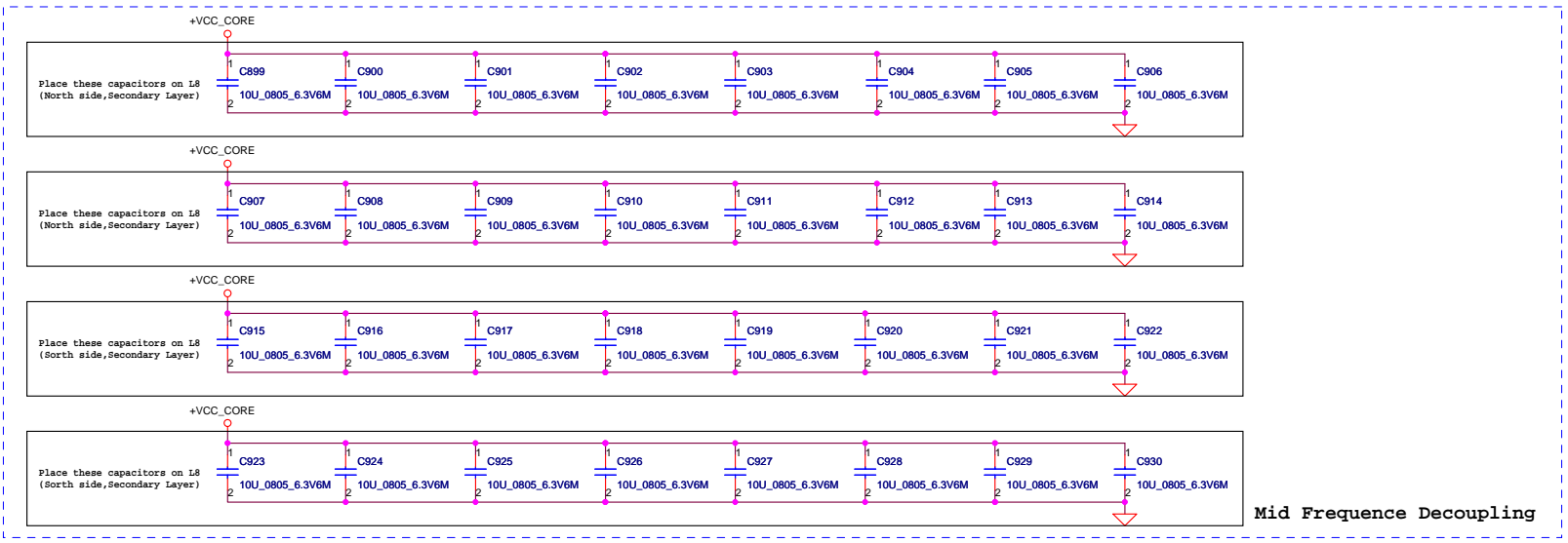
Close to CPU pin AD26 within 500mils.



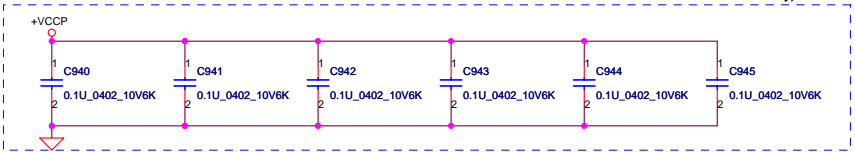
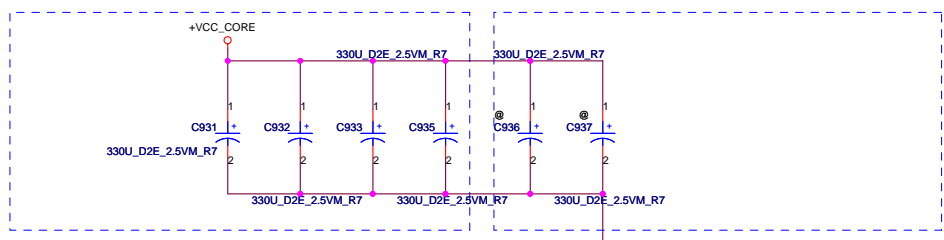
Close to CPU pin within 500mils.

JP12D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	P2
A16	VSS[005]	P5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	U3
B16	VSS[013]	U6
B19	VSS[014]	U21
B21	VSS[015]	U24
B24	VSS[016]	U2
C5	VSS[017]	V5
C8	VSS[018]	V22
C11	VSS[019]	V25
C14	VSS[020]	W1
C16	VSS[021]	W4
C19	VSS[022]	W23
C2	VSS[023]	W26
C22	VSS[024]	Y3
C25	VSS[025]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D16	VSS[031]	AA11
D19	VSS[032]	AA14
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
F11	VSS[038]	AB4
F14	VSS[039]	AB8
F16	VSS[040]	AB11
F19	VSS[041]	AB13
F21	VSS[042]	AB16
F24	VSS[043]	AB19
F5	VSS[044]	AB23
F8	VSS[045]	AB26
F11	VSS[046]	AC3
F13	VSS[047]	AC6
F16	VSS[048]	AC8
F19	VSS[049]	AC11
F2	VSS[050]	AC14
F22	VSS[051]	AC16
F25	VSS[052]	AC19
G4	VSS[053]	AC21
G1	VSS[054]	AC24
G23	VSS[055]	AD2
G26	VSS[056]	AD5
H3	VSS[057]	AD8
H6	VSS[058]	AD11
H21	VSS[059]	AD13
H24	VSS[060]	AD16
J2	VSS[061]	AD19
J5	VSS[062]	AD22
J22	VSS[063]	AD25
J25	VSS[064]	AE1
K1	VSS[065]	AE4
K4	VSS[066]	AE8
K23	VSS[067]	AE11
K26	VSS[068]	AE14
L3	VSS[069]	AE16
L6	VSS[070]	AE19
L21	VSS[071]	AE23
L24	VSS[072]	AE26
M2	VSS[073]	A2
M5	VSS[074]	AF6
M22	VSS[075]	AF8
M25	VSS[076]	AF11
N1	VSS[077]	AF13
N4	VSS[078]	AF16
N23	VSS[079]	AF19
N26	VSS[080]	AF21
P3	VSS[081]	A25
		AF25

Merom Ball-out Rev 1a
conn@

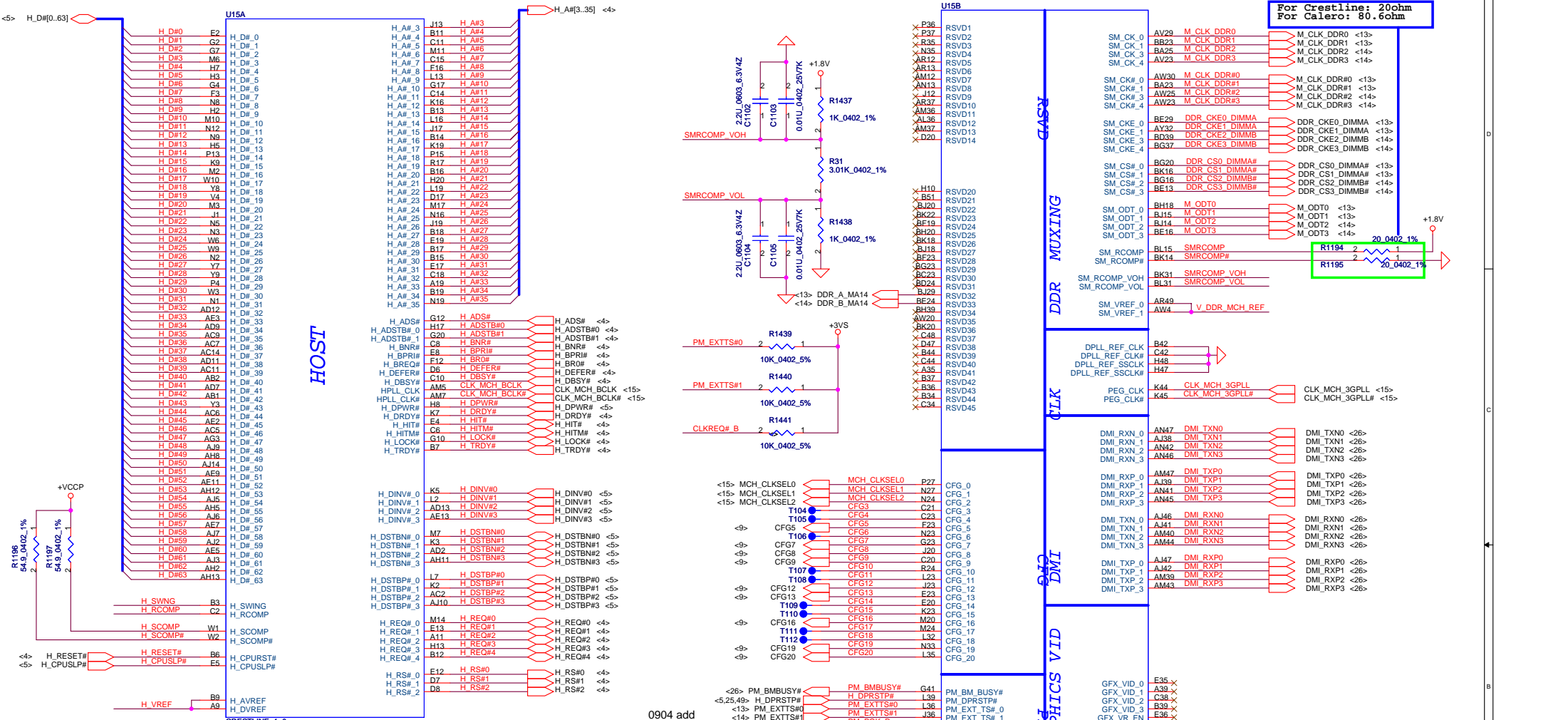


Near CPU CORE regulator
ESR <= 1.5m ohm
Capacitor > 1980uF



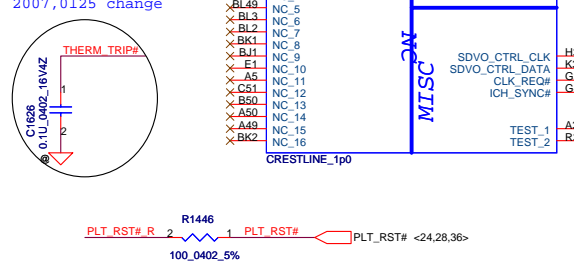
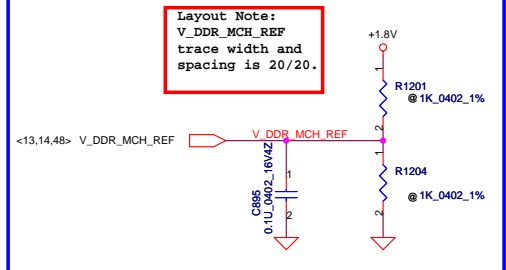
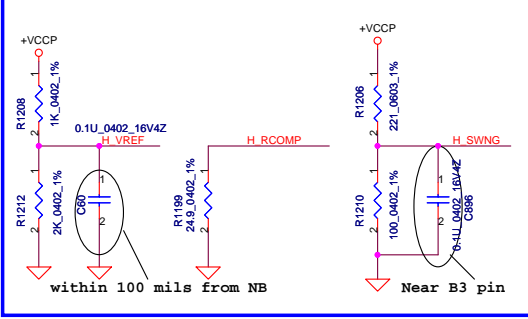
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Merom(3/3)-GND&Bypass

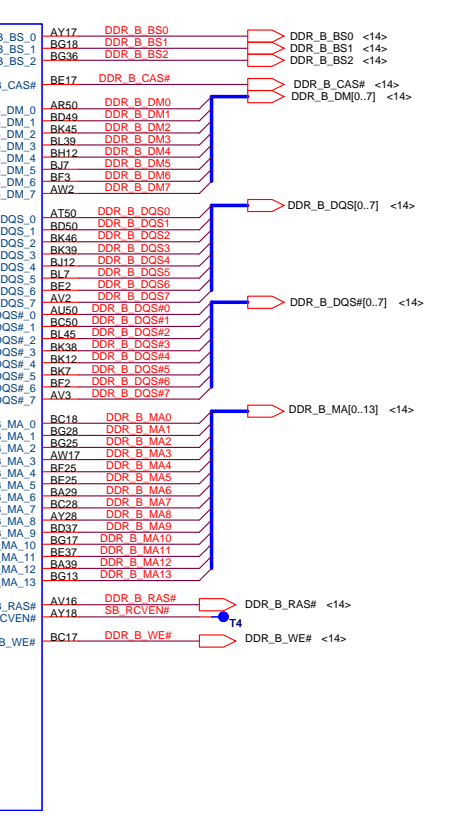
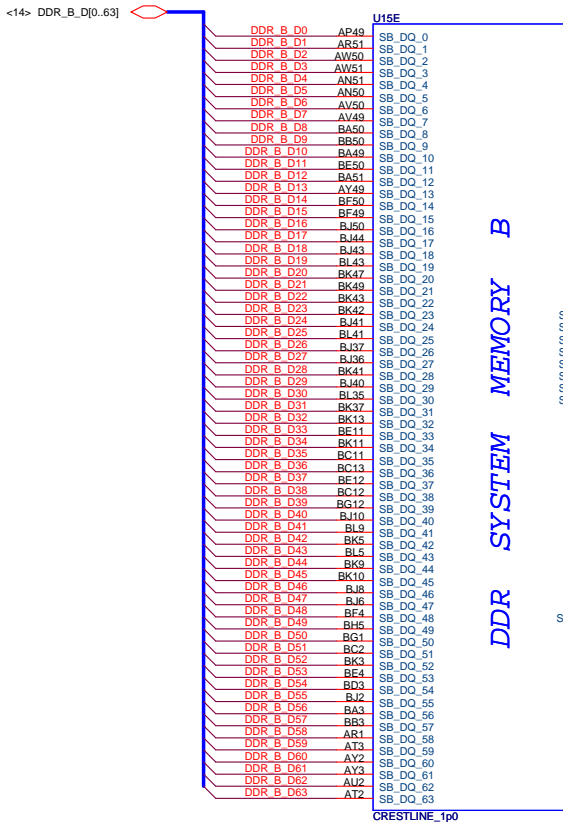
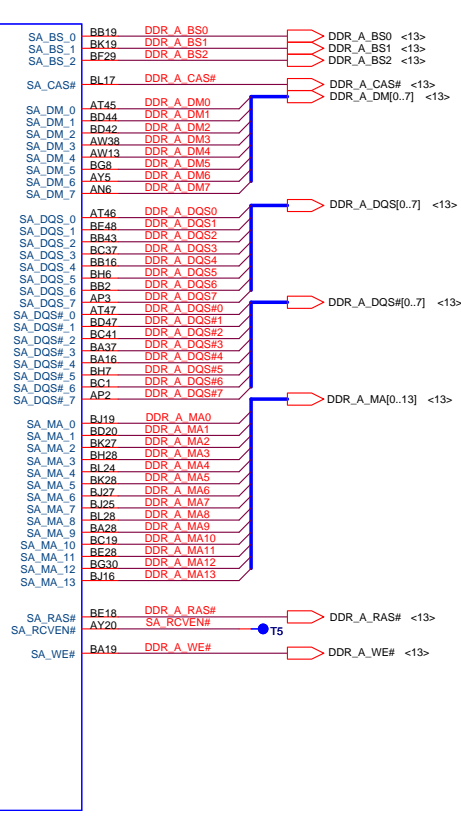
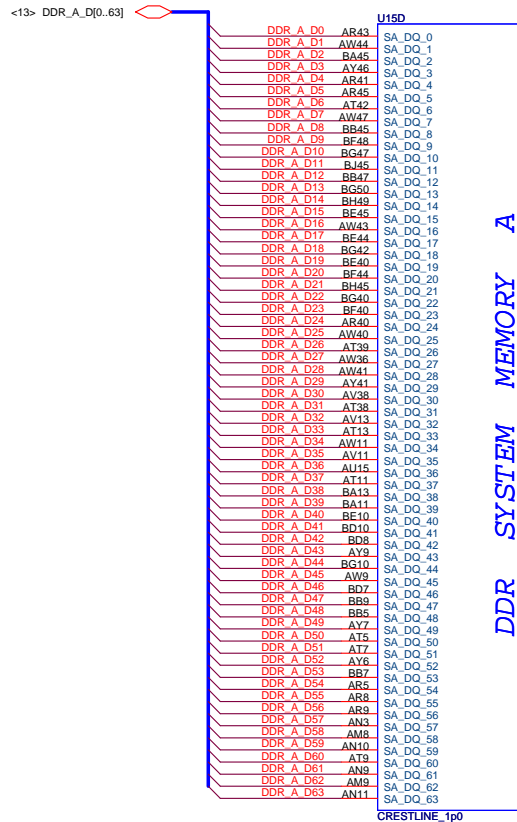


layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



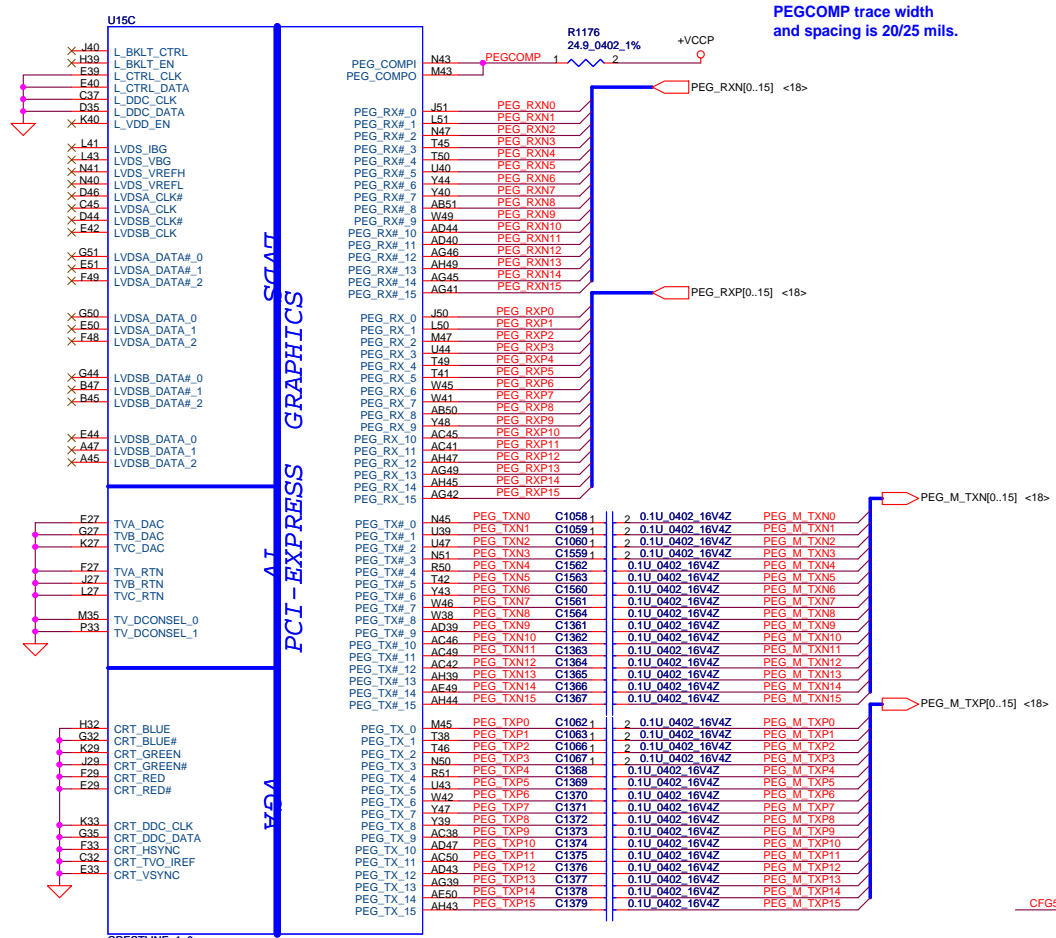
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CRESTLINE_1p0

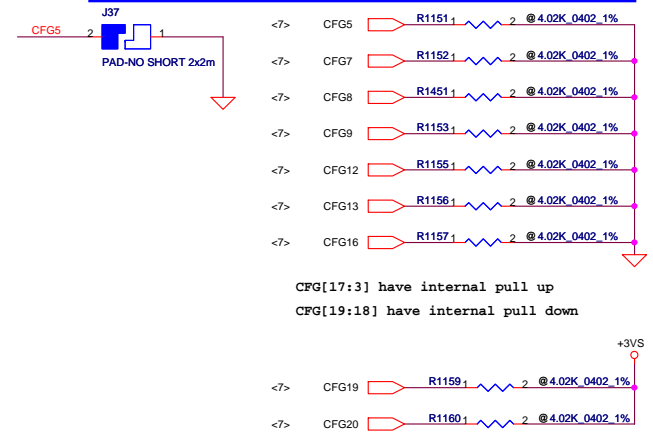
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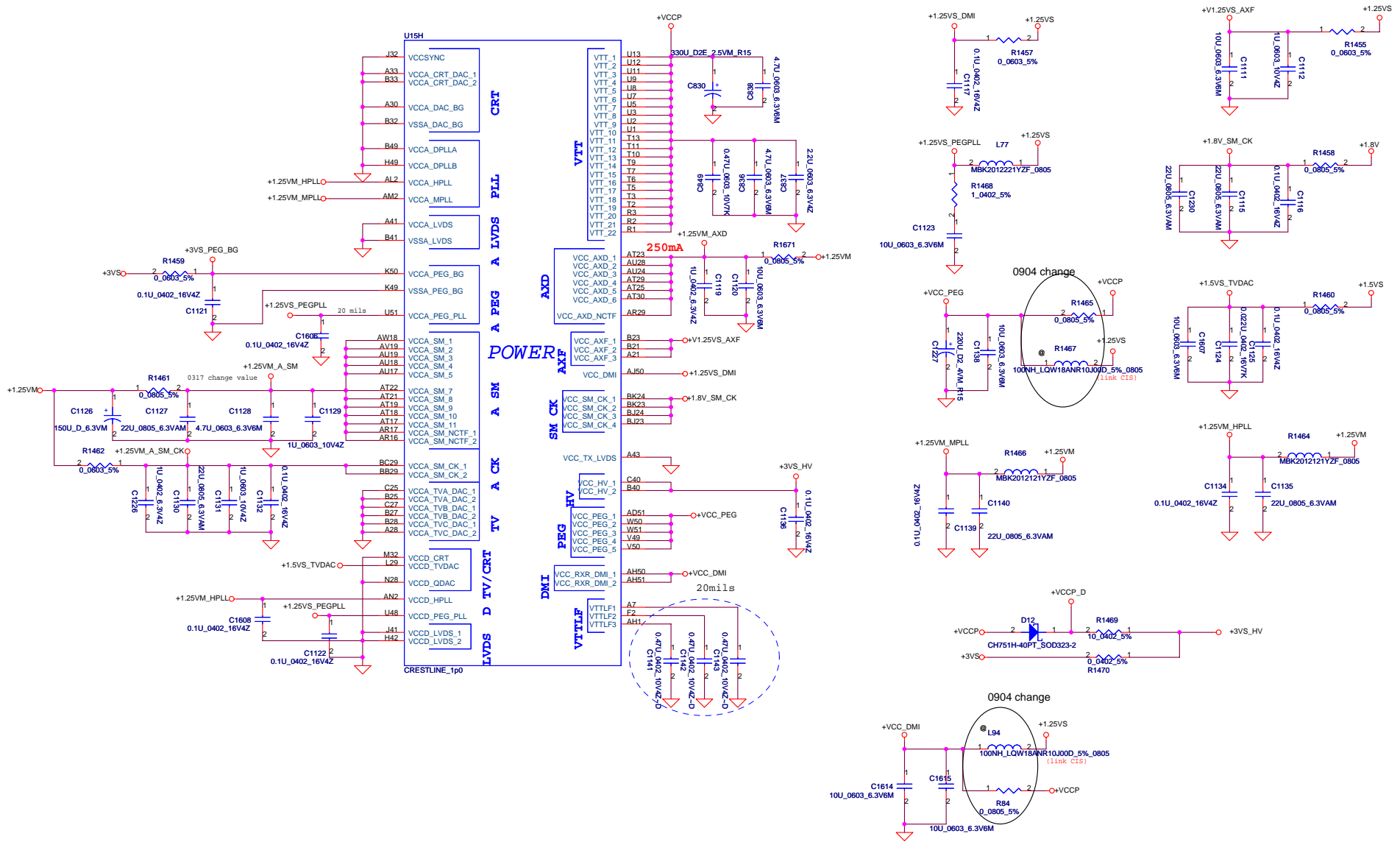
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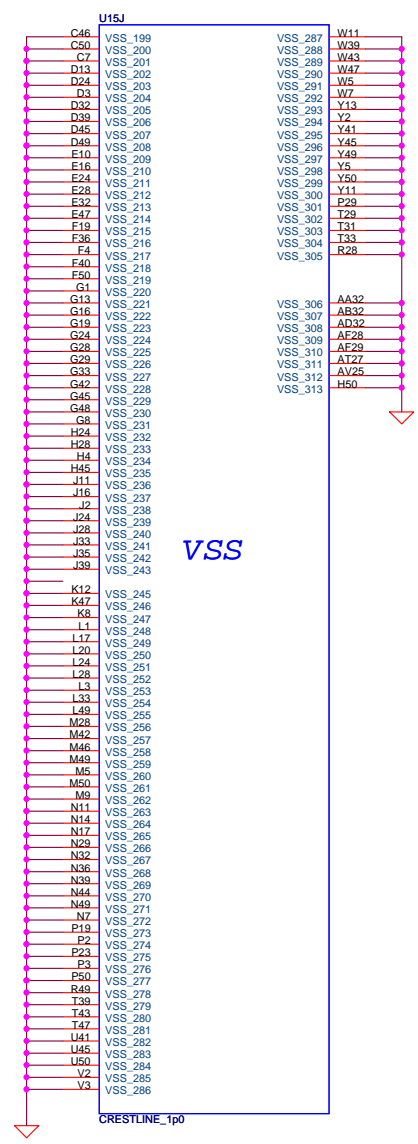
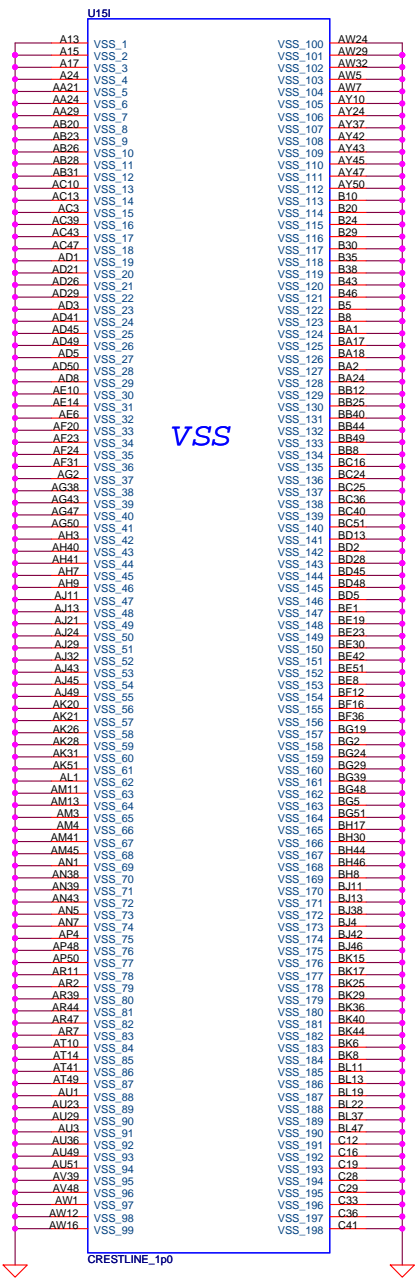
Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

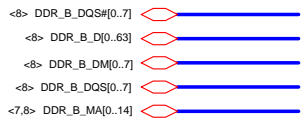




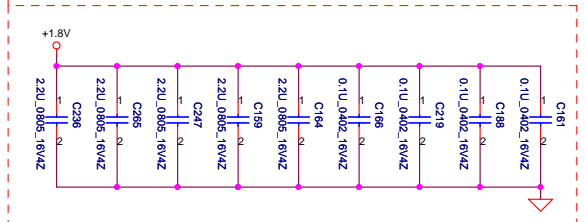
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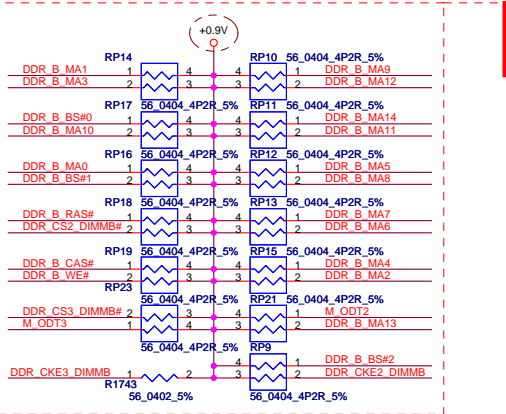
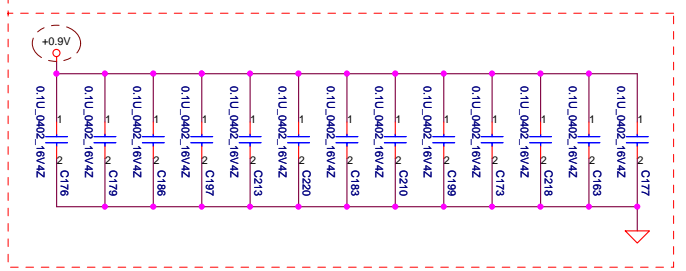
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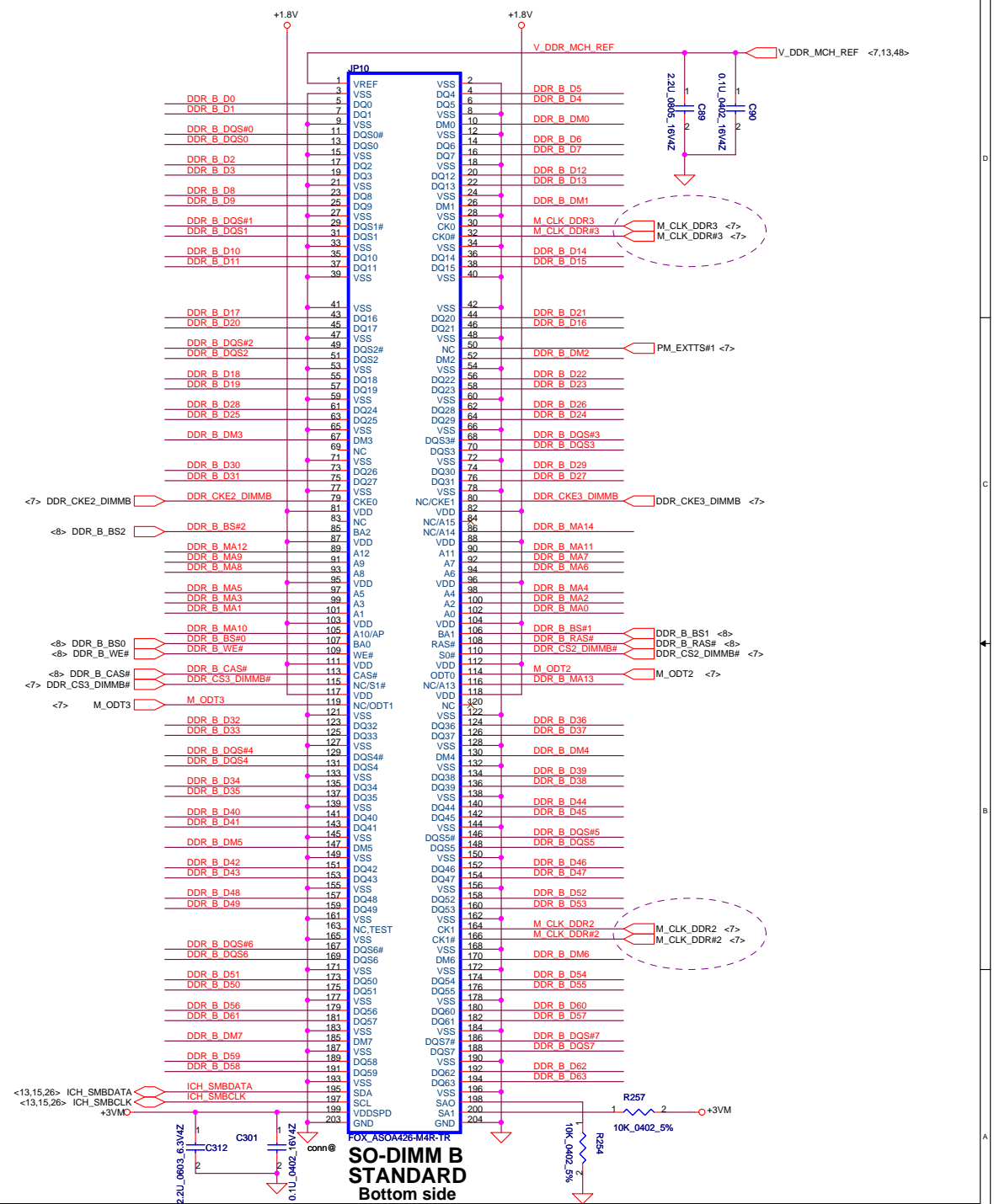
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"

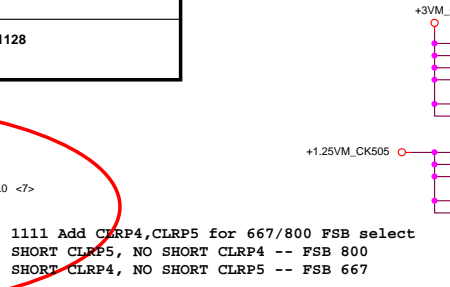
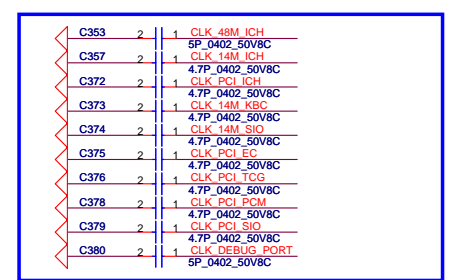
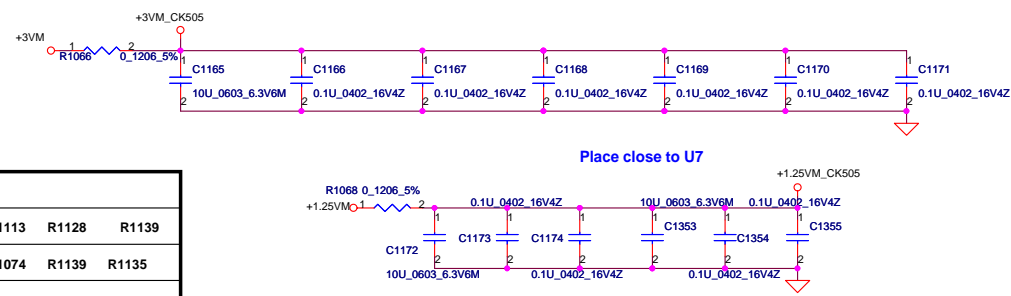
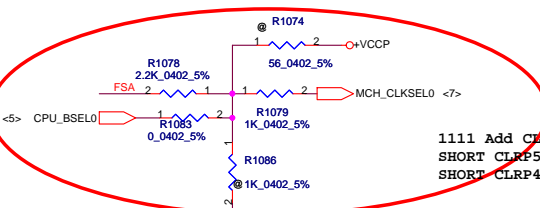


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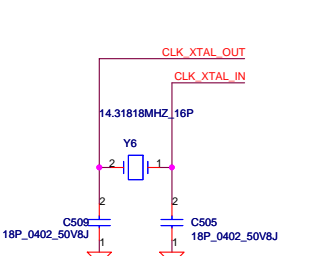
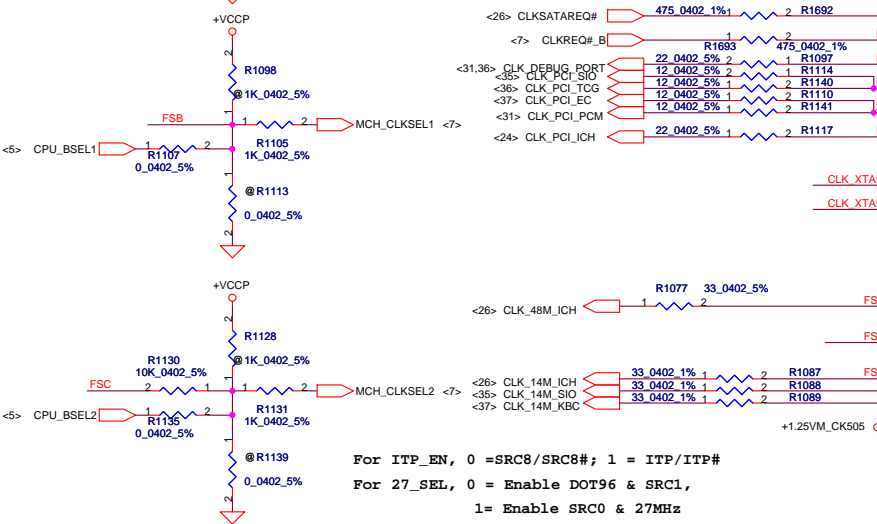
FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

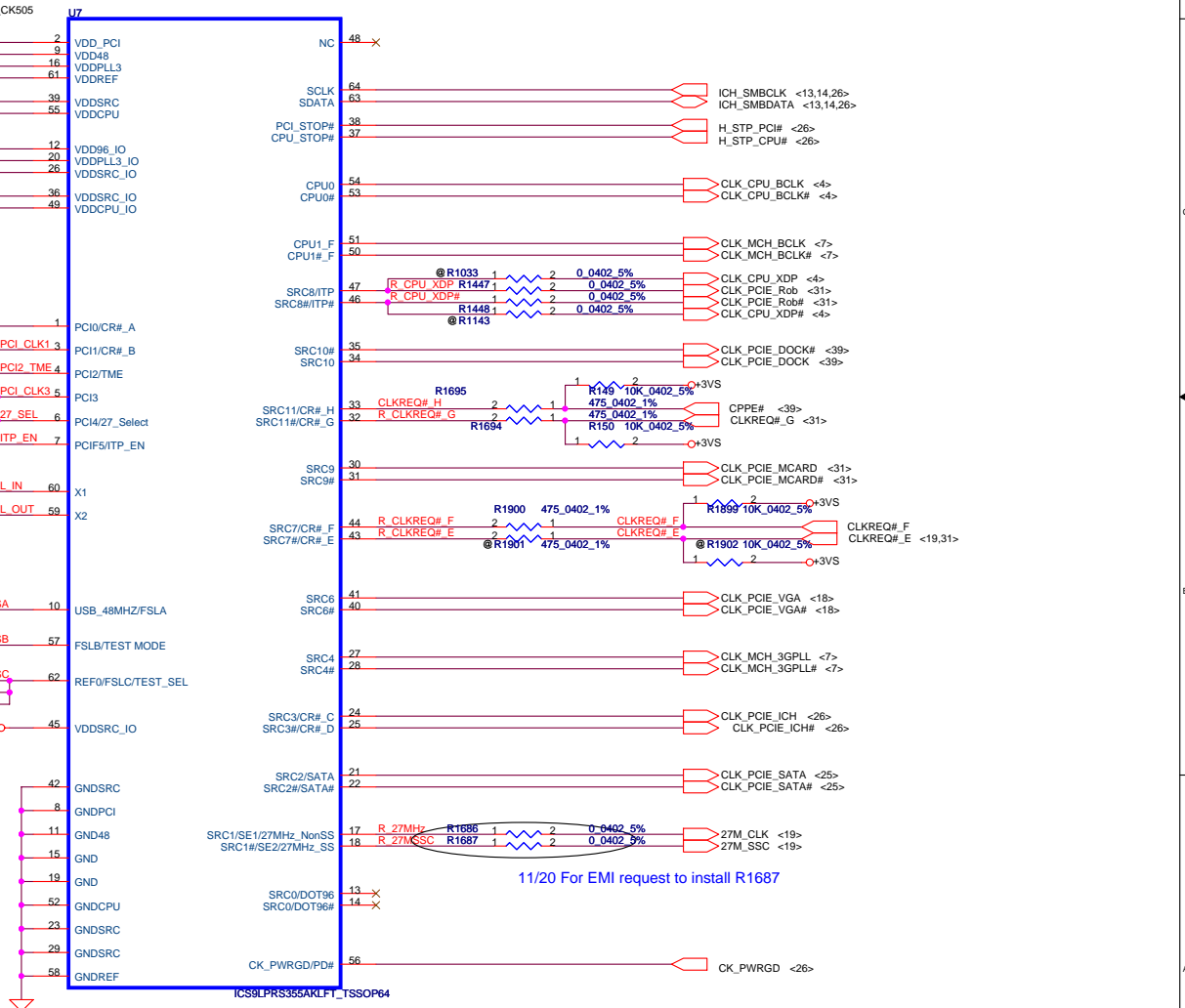
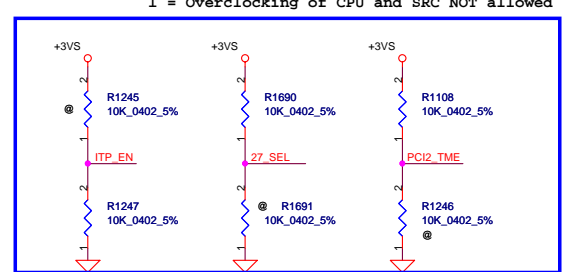
CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
667MHz	No Stuff	R1083	R1107	R1128	R1113	R1098	
	Stuff	R1135	R1139				
800MHz	No Stuff	R1083	R1086	R1098	R1128		
	Stuff	R1074	R1107	R1113			



1111 Add CLR4, CLR5 for 667/800 FSB select
 SHORT CLR5, NO SHORT CLR4 -- FSB 800
 SHORT CLR4, NO SHORT CLR5 -- FSB 667



Routing the trace at least 10mil



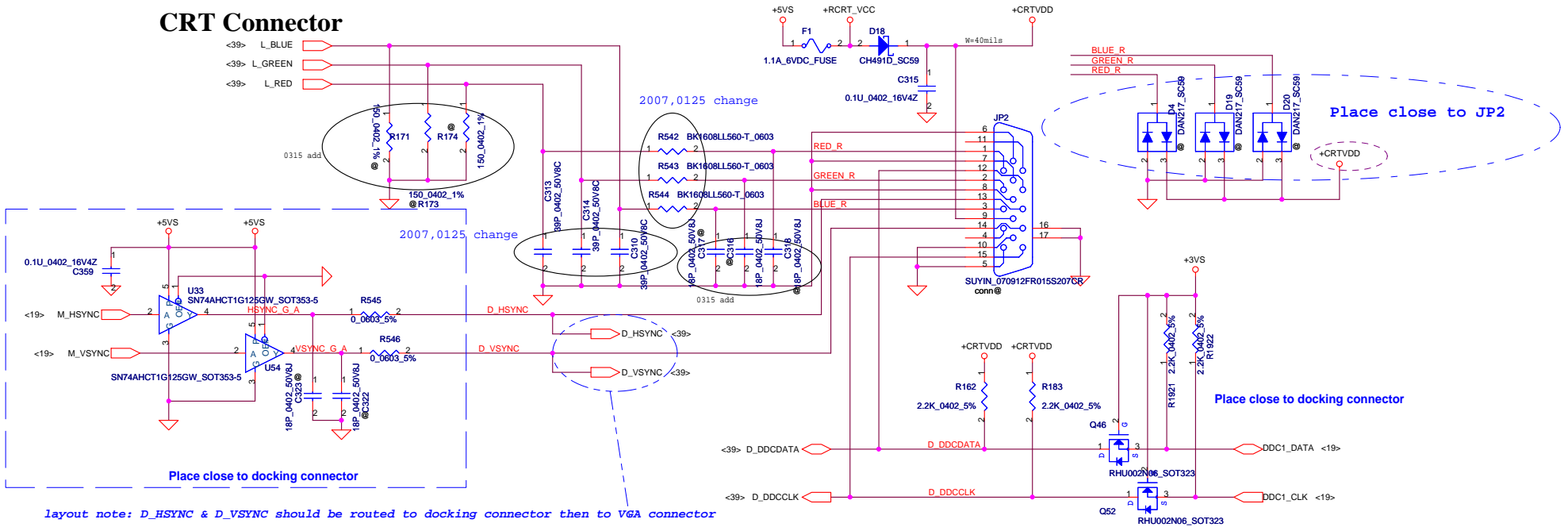
* Internal Pull-Up Resistor
 ** Internal Pull-Down Resistor

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Issued Date	2006/09/25
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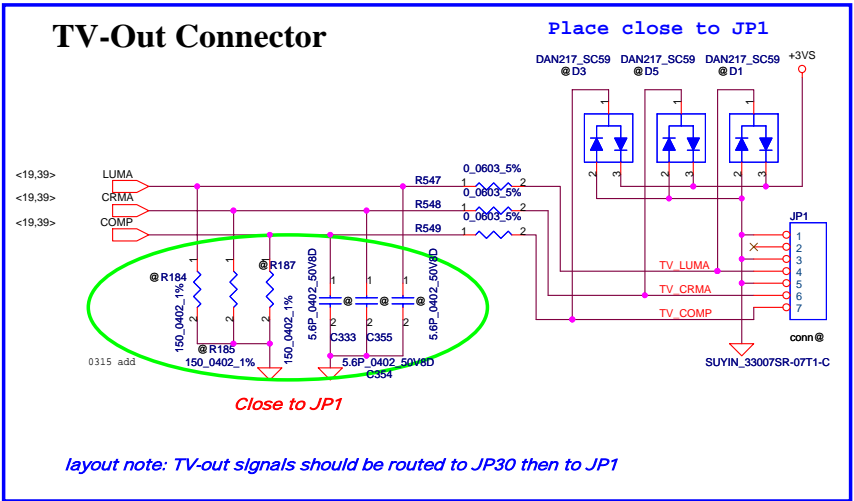
Compal Electronics, Inc.
Clock generator
 Size: Document Number: LA3262P_DIS_M64
 Date: Tuesday, August 21, 2007 [Sheet 15 of 57]

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CRT Connector

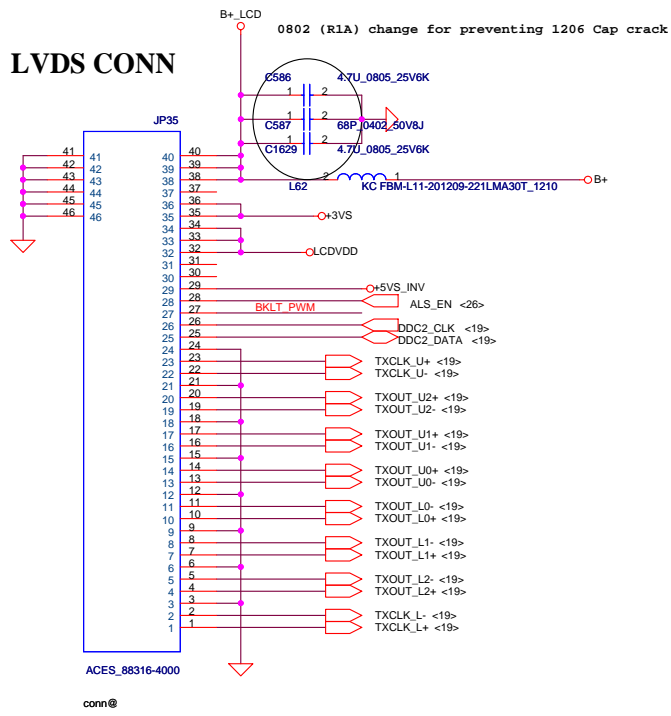


TV-Out Connector

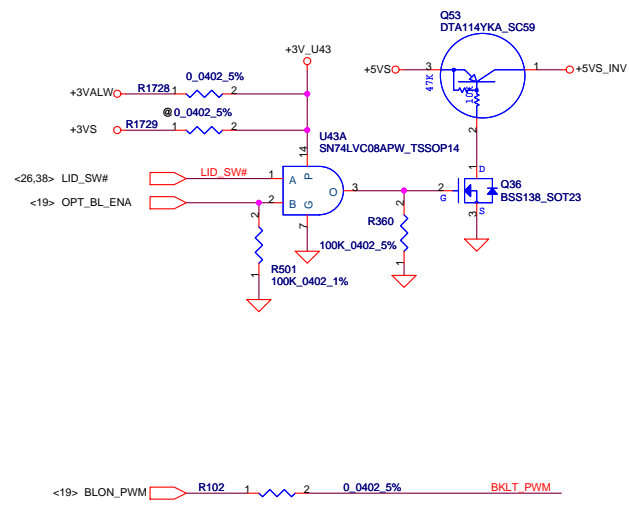
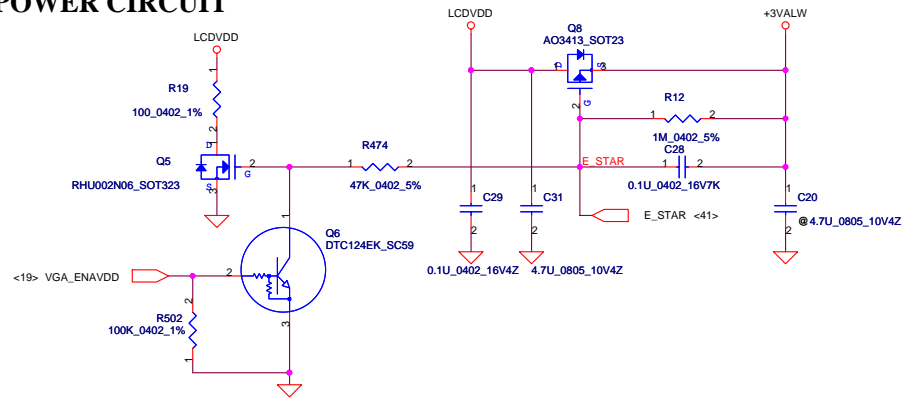


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Size	Document Number	Date		Rev	1A	
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LVDS CONN

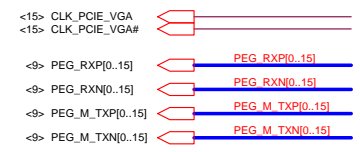
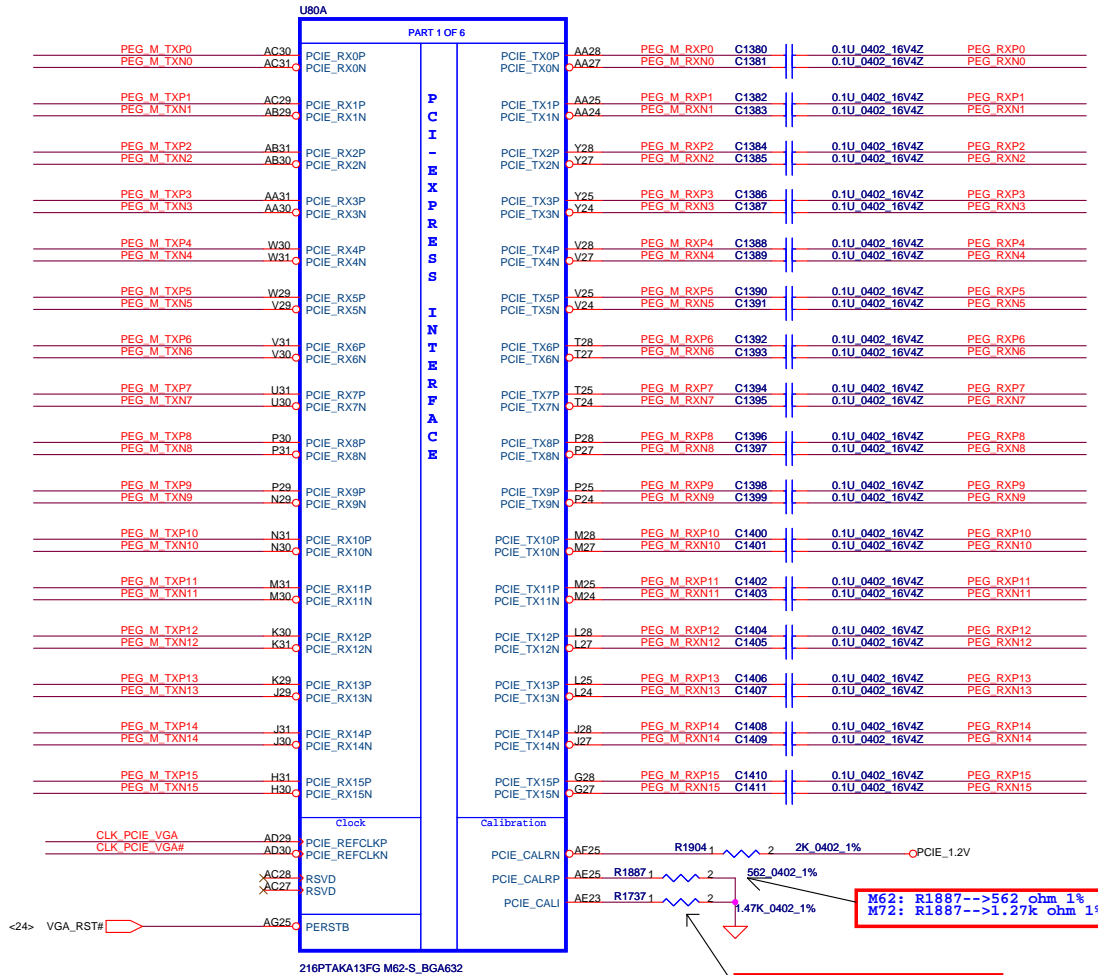


LCD POWER CIRCUIT

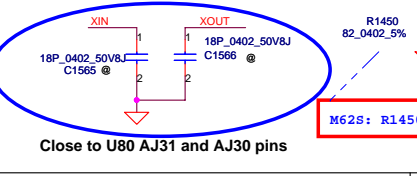
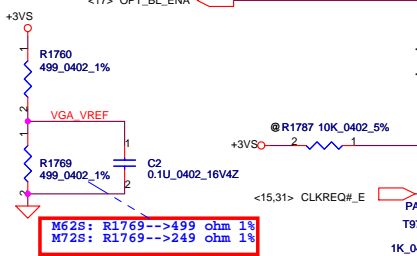
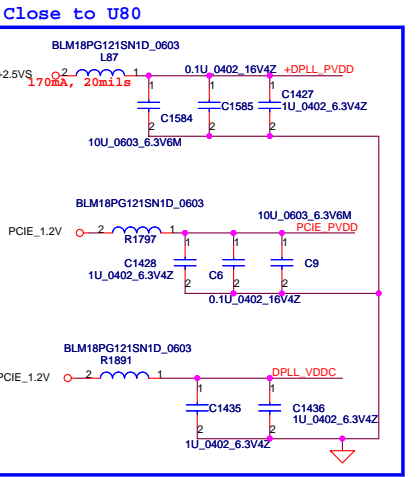
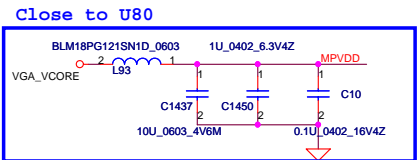


Support 3V inverter

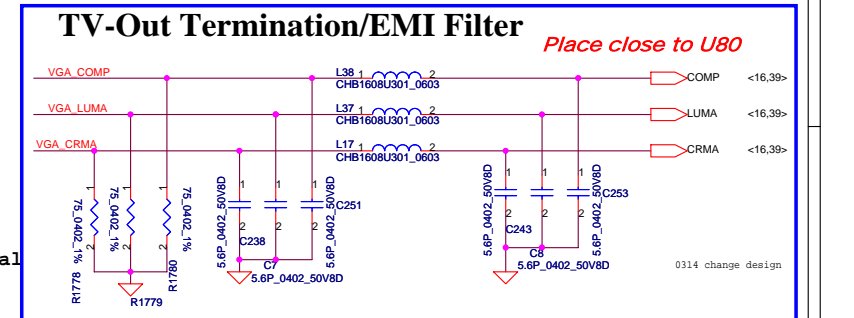
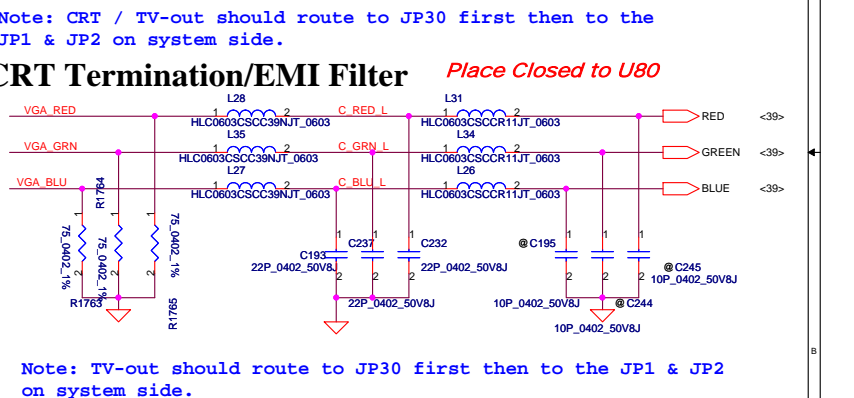
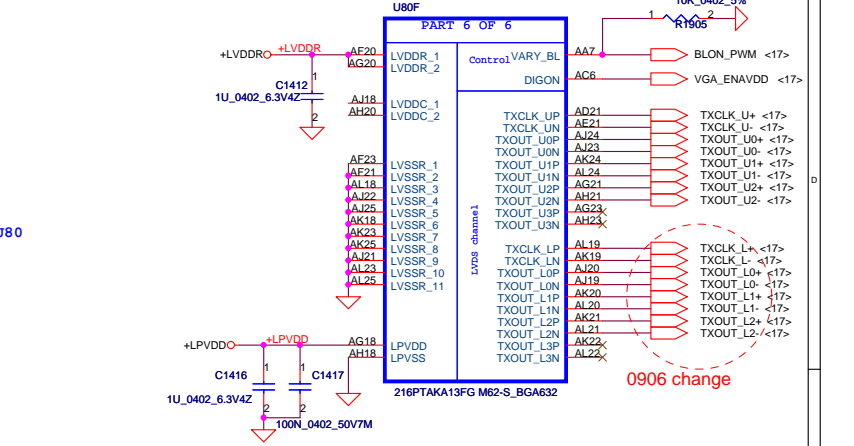
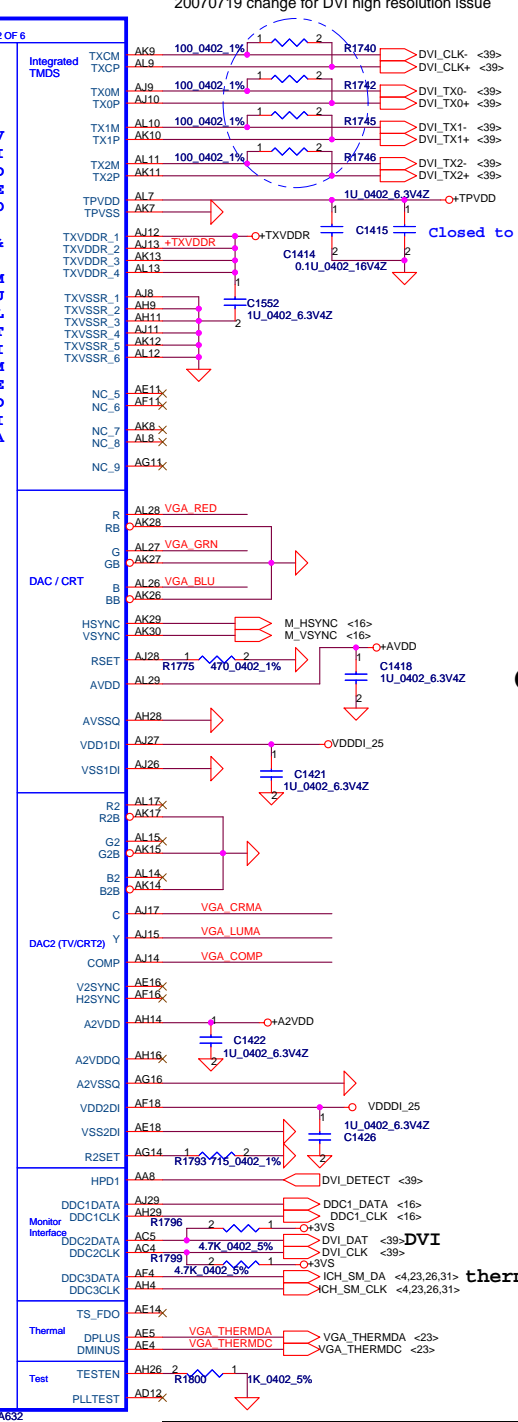
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Date:	Tuesday, August 21, 2007	Sheet	18	of	57	Rev 1A

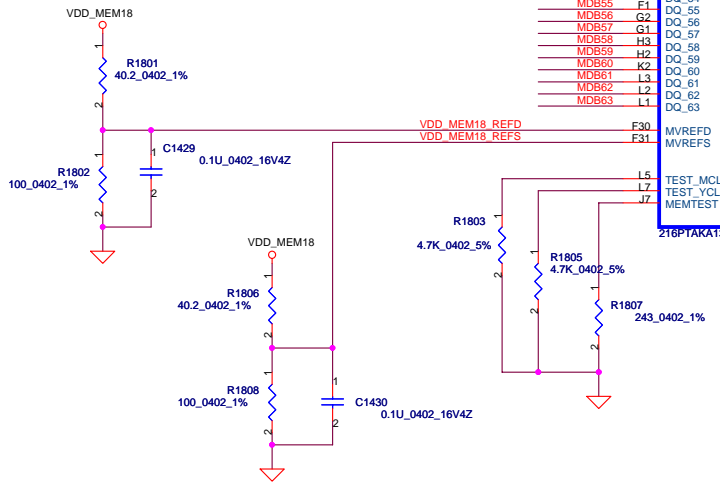
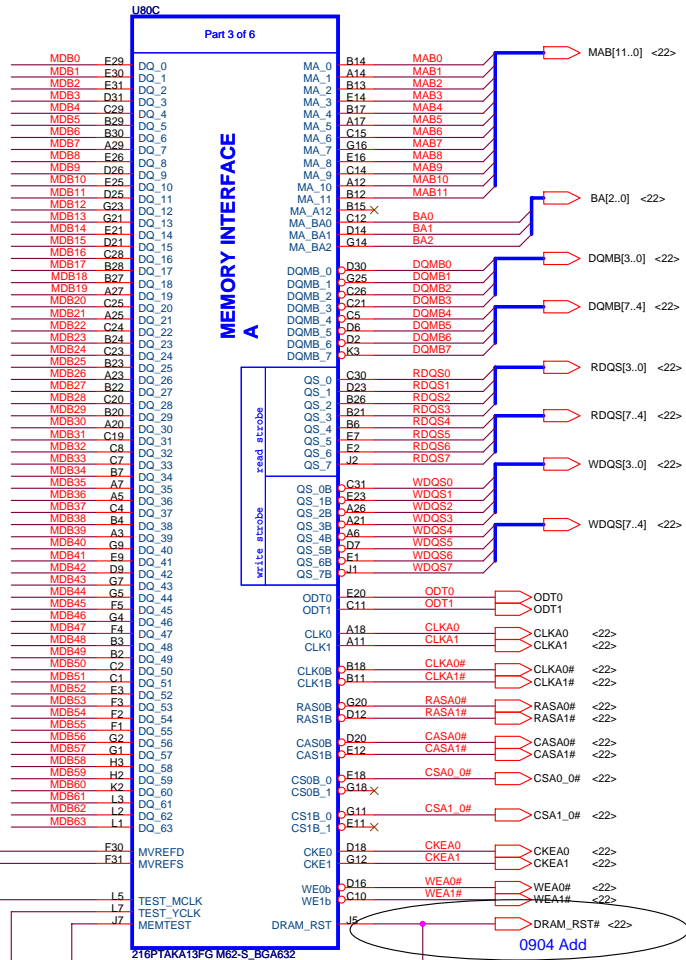


U80B PART 2 OF 6	VIDEO & MULTIMEDIA
×AH7	VID_0
×AG9	VID_1
×AF9	VID_2
×AJ7	VID_3
×AG7	VID_4
×AF7	VID_5
×AH6	VID_6
×AG6	VID_7
×AL6	VHAD_0
×AK6	VHAD_1
×AK5	VPHCTL
×AJ4	VPCLK0
×AJ5	VPCLK
×AL5	PSYNC
×AD9	DVALID
×AA4	DDC2_DATA
×AA5	DDC2_CLK
×AK4	DVPCNTL_MVP_0
×AL3	DVPCNTL_MVP_1
×V2	DVPCNTL_0
×V1	DVPCNTL_1
×W3	DVPCNTL_2
×W1	DVPCLK
×Y1	DVPDATA_0
×Y2	DVPDATA_1
×Y3	DVPDATA_2
×AA2	DVPDATA_3
×AA3	DVPDATA_4
×AB1	DVPDATA_5
×AB2	DVPDATA_6
×AB3	DVPDATA_7
×AC1	DVPDATA_8
×AC3	DVPDATA_9
×AD1	DVPDATA_10
×AD2	DVPDATA_11
×AD3	DVPDATA_12
×AF3	DVPDATA_13
×AG3	DVPDATA_14
×AH3	DVPDATA_15
×AG1	DVPDATA_16
×AH2	DVPDATA_17
×AH1	DVPDATA_18
×AJ1	DVPDATA_19
×AJ2	DVPDATA_20
×AK2	DVPDATA_21
×AK3	DVPDATA_22
×AK3	DVPDATA_23
×Y4	GPI0_0
×V3	GPI0_1
×V4	GPI0_2
×V5	GPI0_3
×U3	GPI0_4
×U2	GPI0_5
×T4	GPI0_6
×T5	GPI0_7
×T7	GPI0_8
×T8	GPI0_9
×R1	GPI0_10
×R2	GPI0_11
×R3	GPI0_12
×P1	GPI0_13
×P3	GPI0_14
×N1	GPI0_15
×N2	GPI0_16
×P4	GPI0_17
×P7	GPI0_18
×P8	GPI0_19
×P5	GPI0_20
×VZ	GPI0_21
×N3	GPI0_22
×Y5	GPI0_23
×M4	GPI0_24
×M5	GPI0_25
×M7	GPI0_26
×M8	GPI0_27
×L8	GPI0_28
×Y8	GENERIC_A
×Y7	GENERIC_B
×V8	GENERIC_C
×AC11	GENERIC_VREF
×AH12	+DPLL_PVDD
×AH30	PCIE_PVDD
×A9	MPVDD
×B9	MPVSS
×AJ31	PLL & XTAL
×AJ30	XTALOUT
×AE12	DPLL_VDDC
×AD11	NC_10

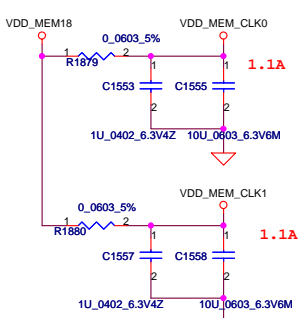
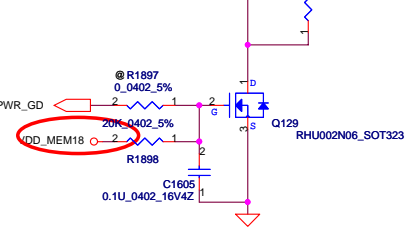
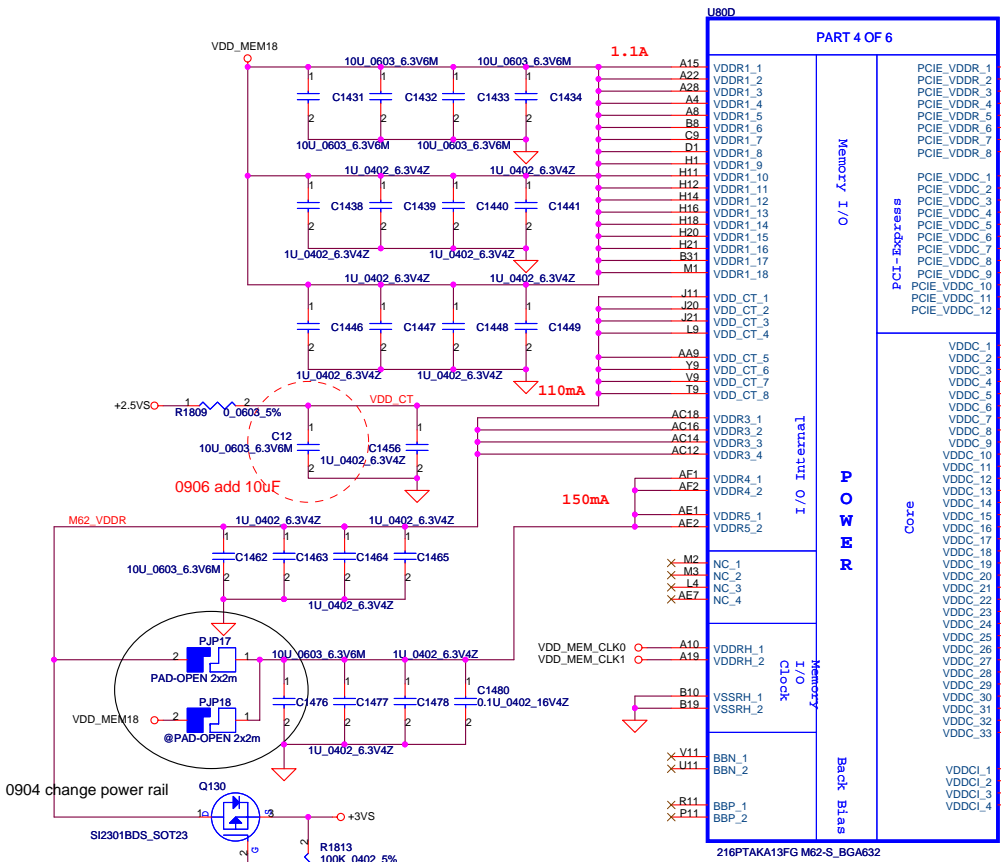
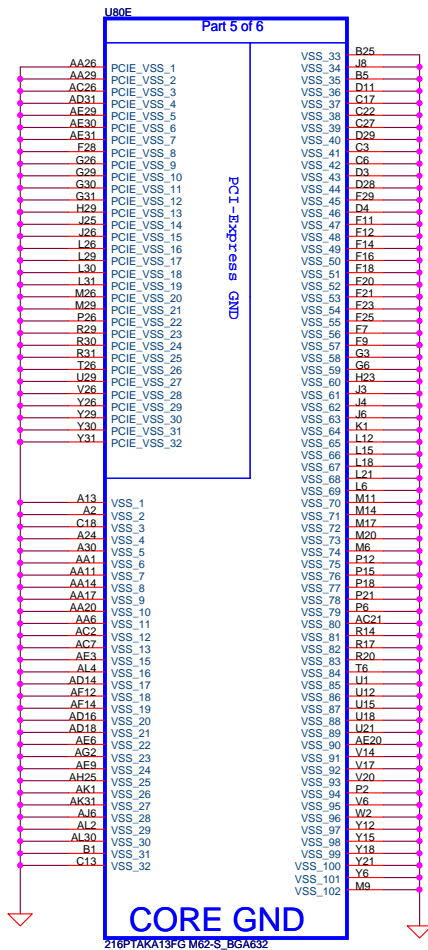


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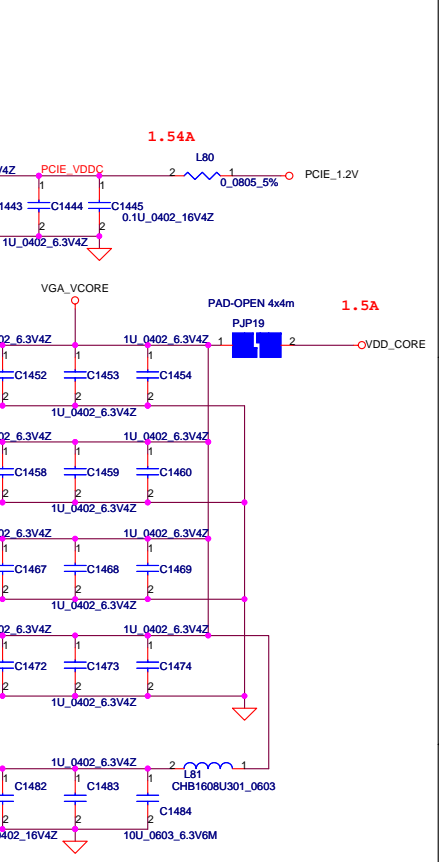
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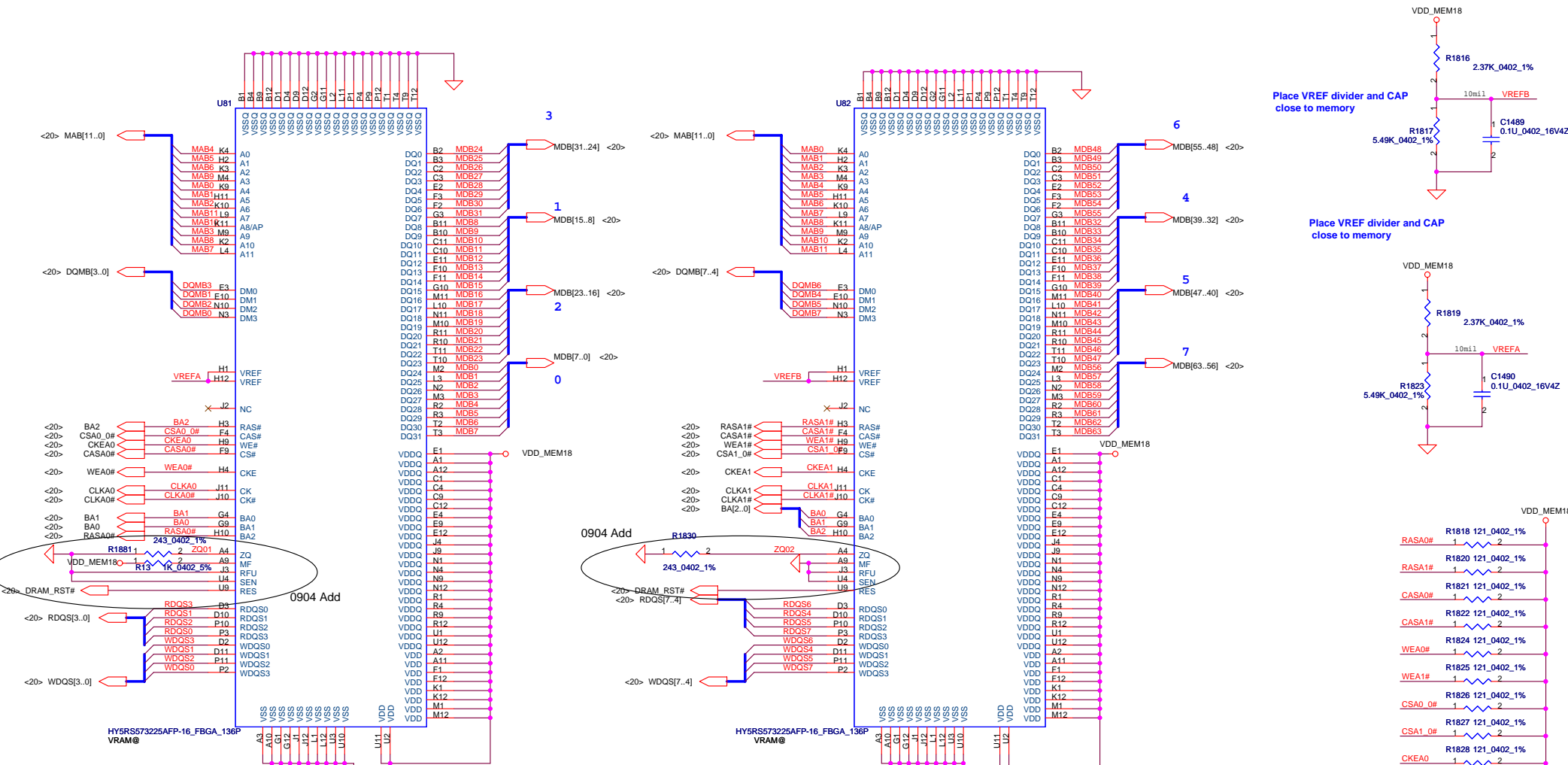


PLACE ALL CAPS ON THIS PAGE CLOSE TO ASIC

Compal Electronics, Inc.

M62-S POWER

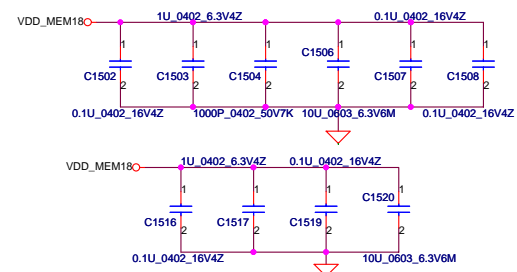
Title	M62-S POWER	
Size	Document Number	Rev
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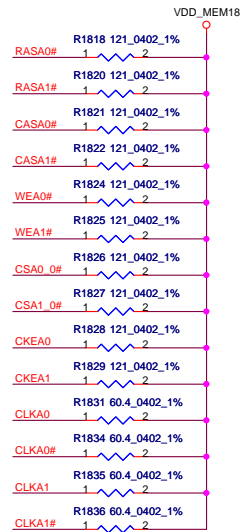
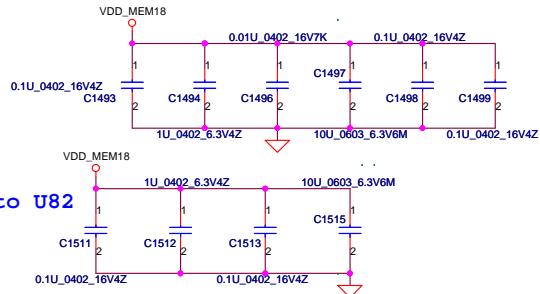
Place VREF divider and CAP close to memory

Place VREF divider and CAP close to memory

Place close to U81

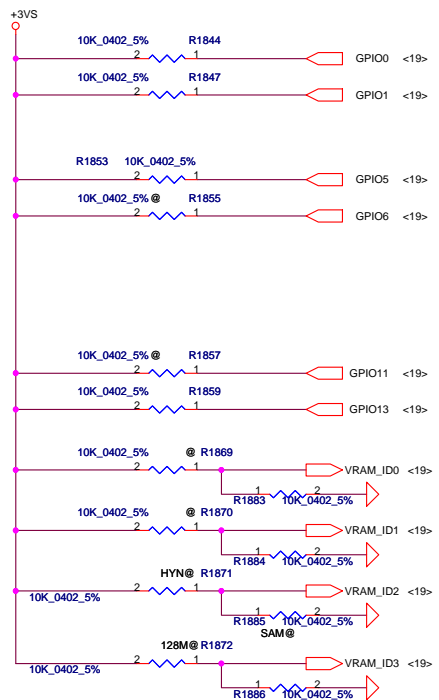


Place close to U82



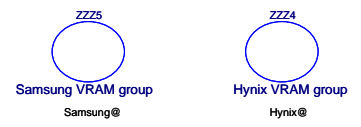
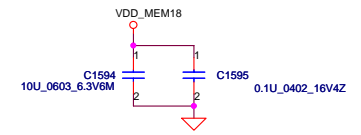
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				M62-S VRAM	
				Size	Document Number
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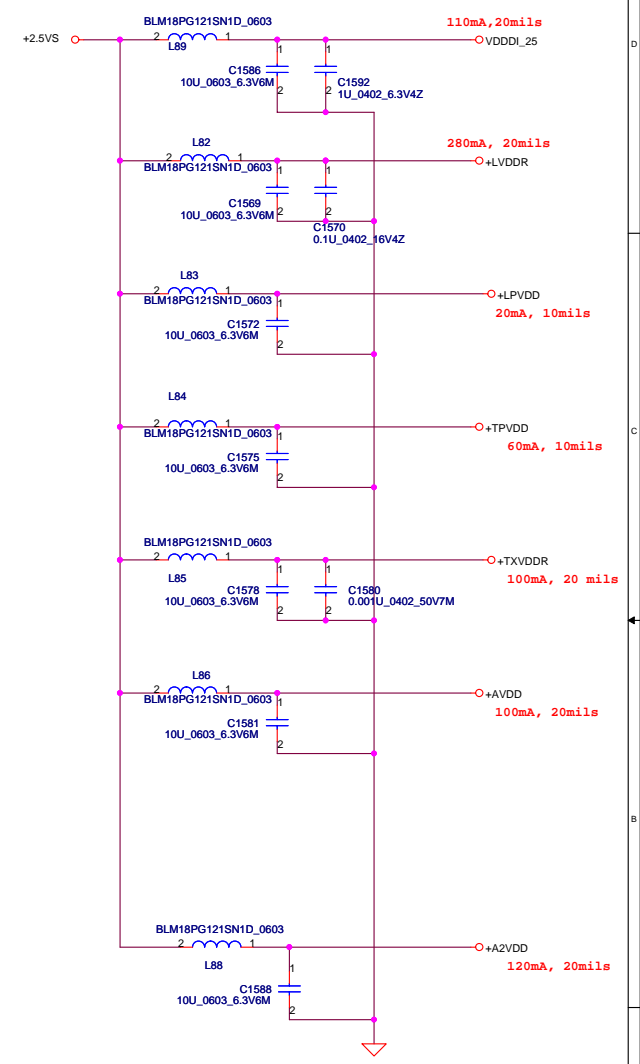


STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
TX_PWRS_ENB	GPIO0	FULL SWING <i>internal pull down</i>	1
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable <i>internal pull down</i>	1
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible <i>internal pull down</i>	0
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCIE PHY PLL	GPIO6-->0 GPIO5-->1
ROMIDCFG[3:0]	GPIO [9,13,12,11]	No ROM , with 128M frame buffer	0 0 0 x
		No ROM , with 64M frame buffer	0 1 0 x
VRAM_ID[0:3]	DVPPDATA (20,21,22,23)	Samsung 8Mx32 1.8V	0 0 0 0
		Samsung 16Mx32 1.8V	0 0 0 1
		Hynix 8Mx32 1.8V	0 0 1 0
		Hynix 16Mx32 1.8V	0 0 1 1

Closed to U80

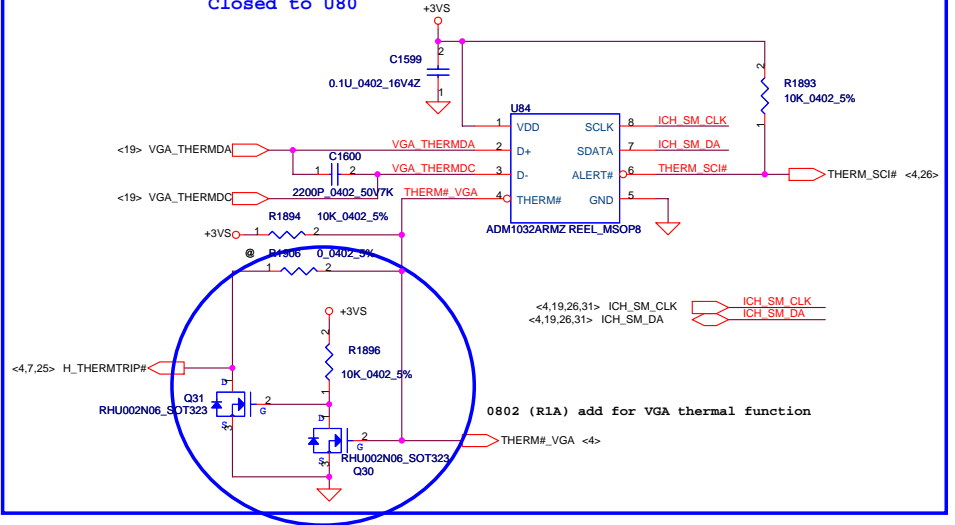


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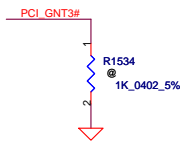
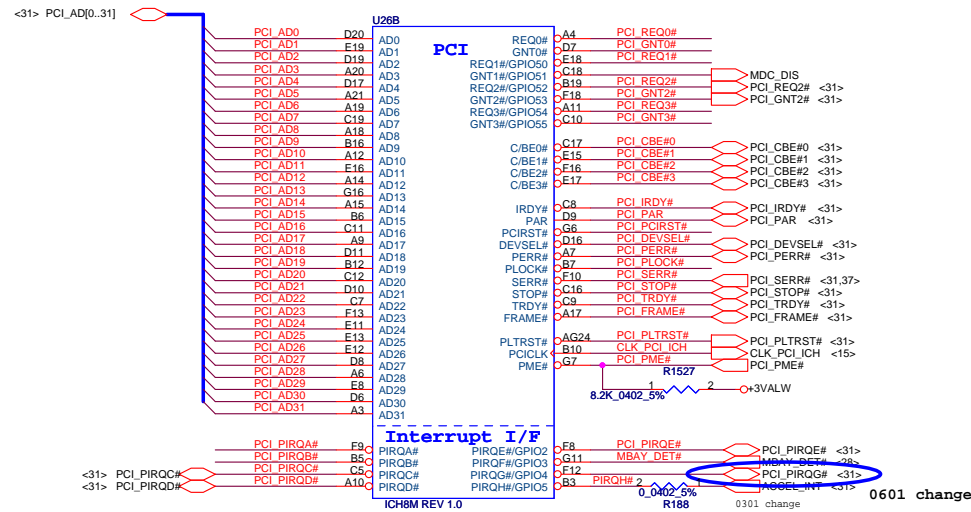
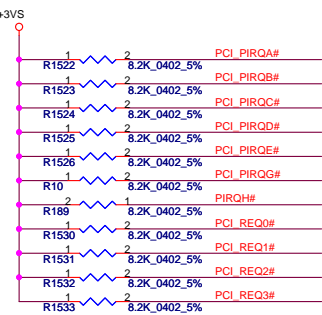
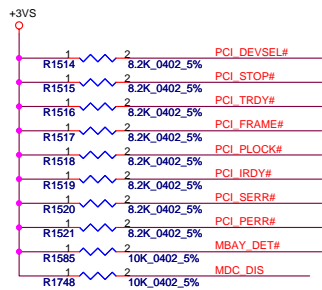


VGA Thermal Sensor ADM1032ARMZ

Closed to U80

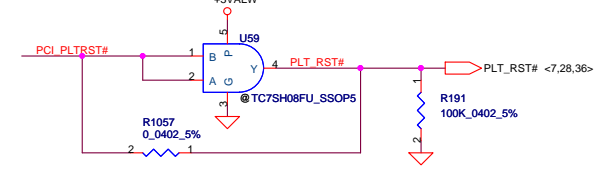
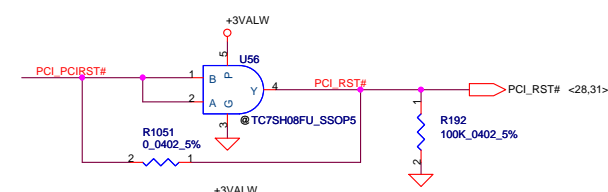
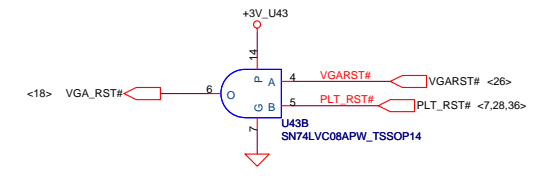
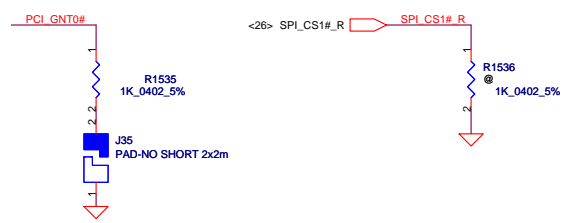
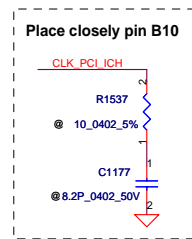


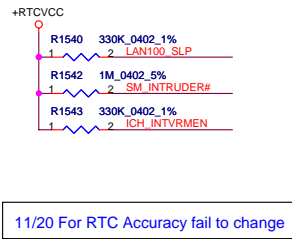
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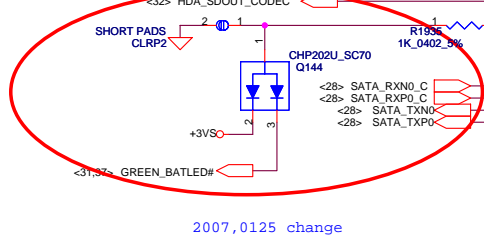
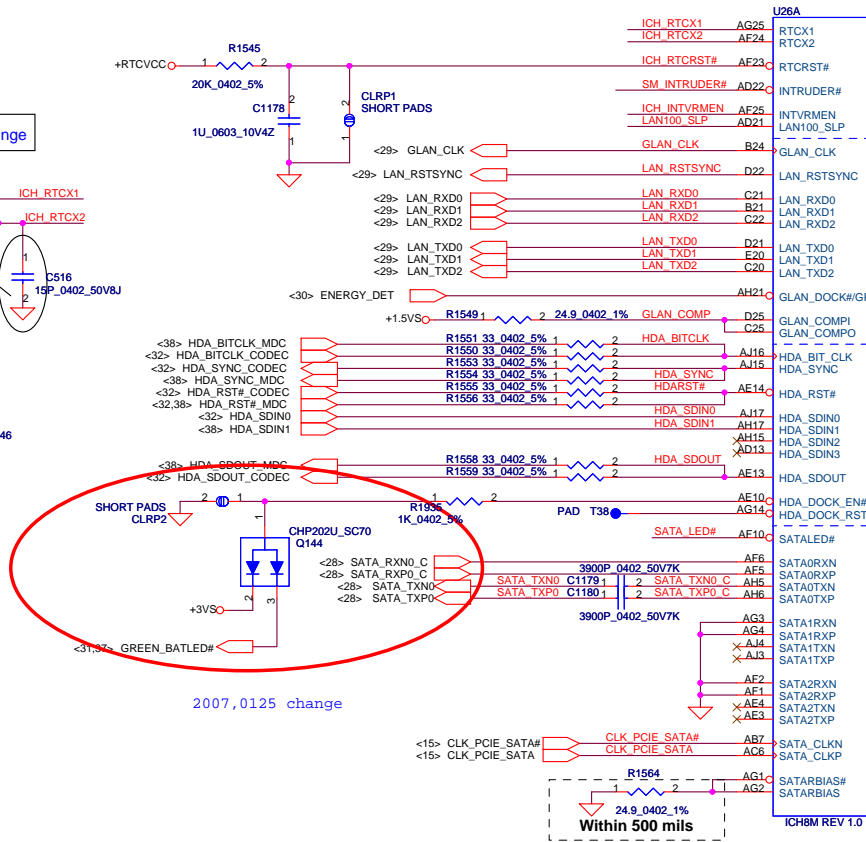
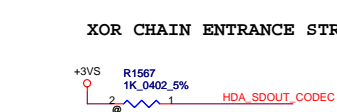
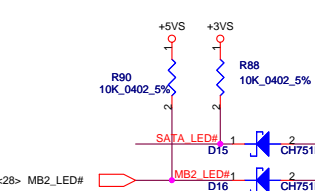
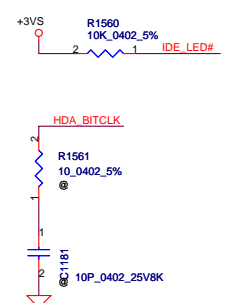
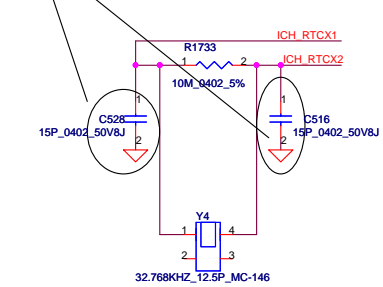
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

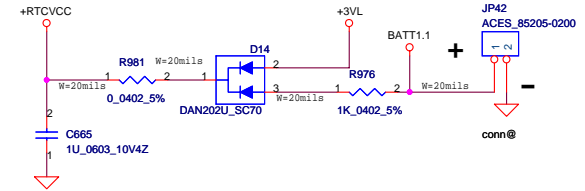
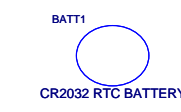
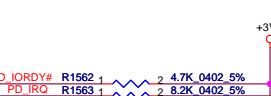
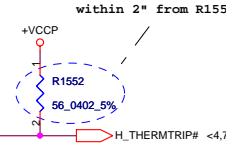
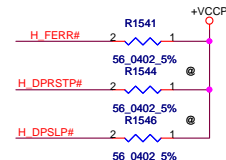
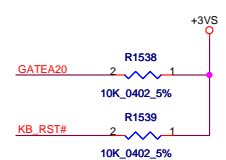
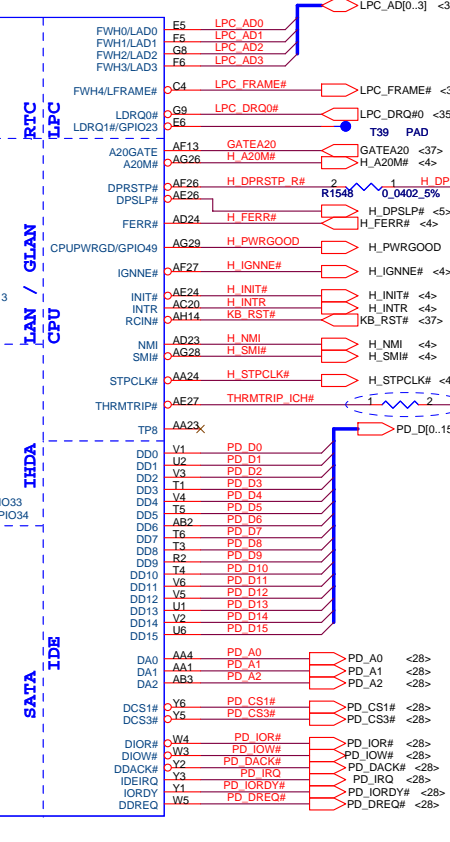
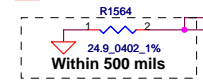




11/20 For RTC Accuracy fail to change



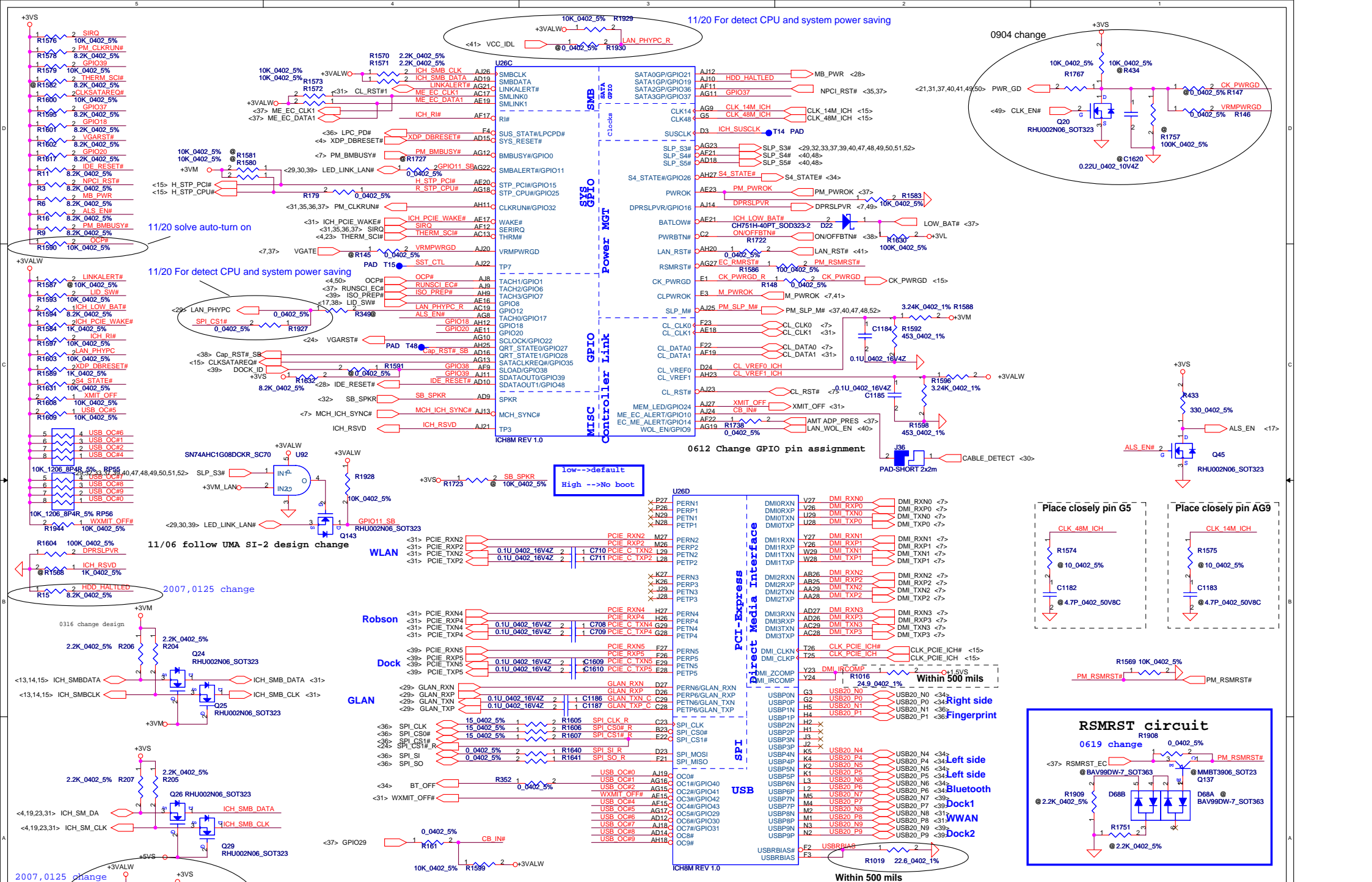
2007,0125 change



XOR CHAIN ENTRANCE STRAP:RSVD

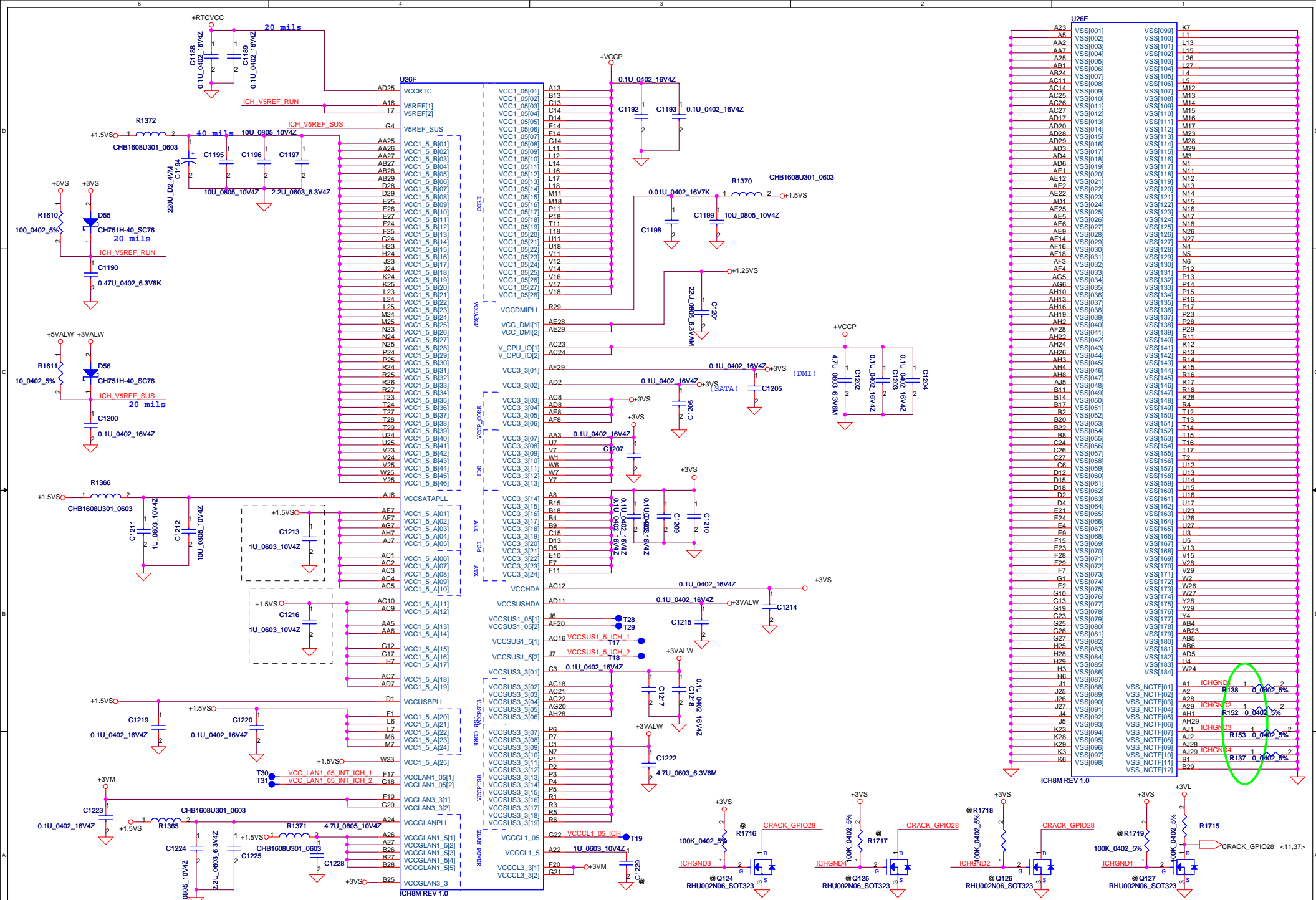
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Compal Electronics, Inc.
ICH8(2/4) LAN,HD,IDE,LPC



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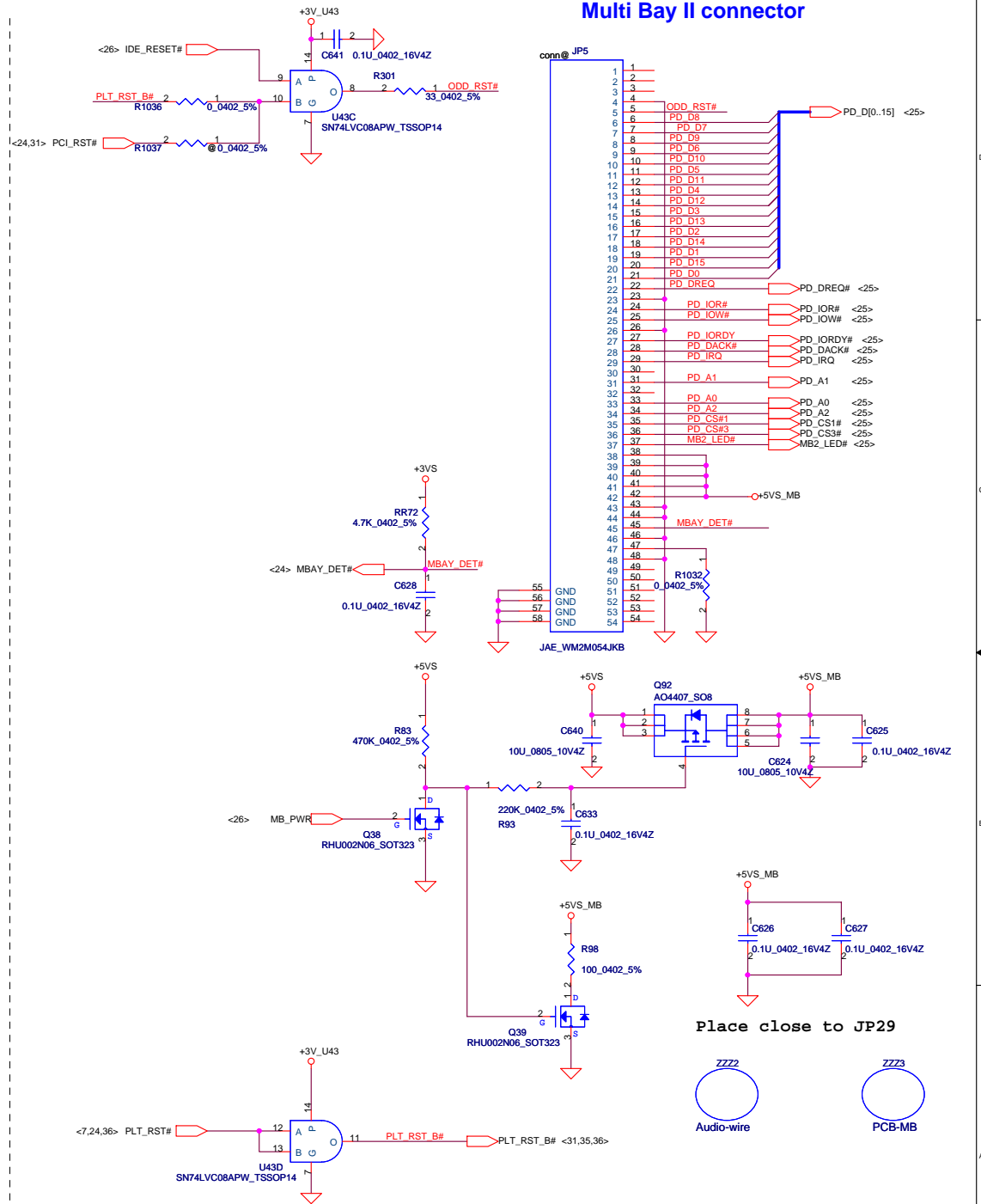
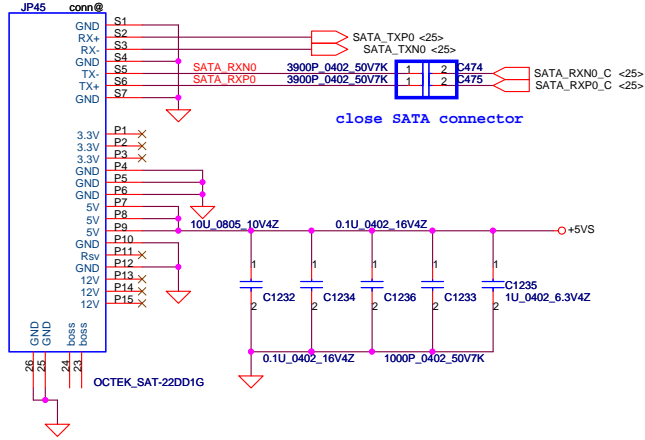
Compal Electronics, Inc.			
Title: ICH8(3/4) PM,USB,GPIO			
Size	Document Number	Rev	1A
Custom	LA3262P_DIS_M64	Date:	Tuesday, August 21, 2007
		Sheet	26 of 57



Security Classification	Compal Secret Data	
Issued Date	2006/09/25	Deciphered Date
		2006/09/25

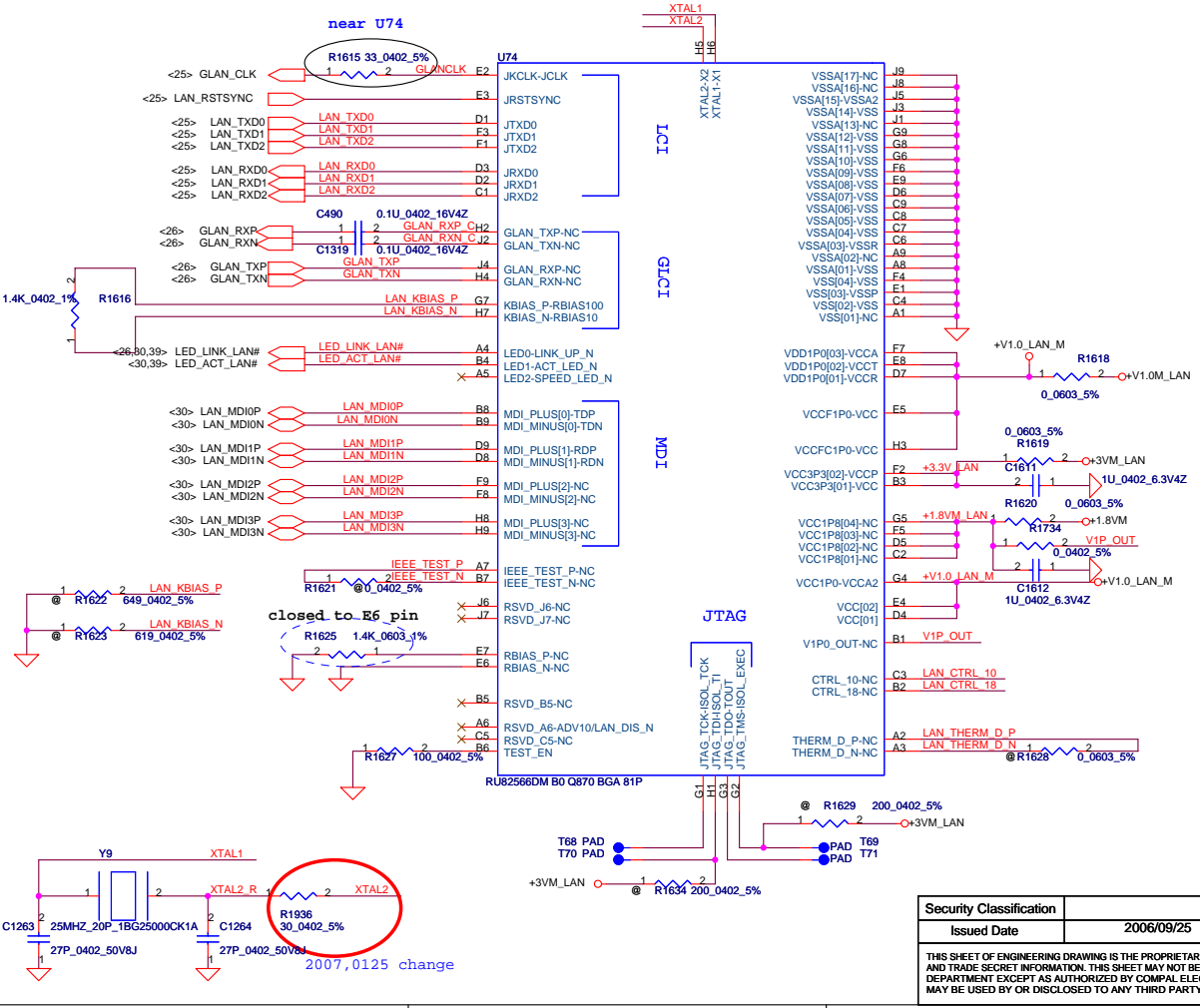
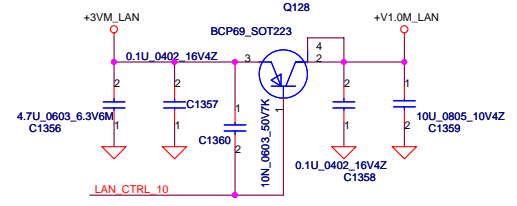
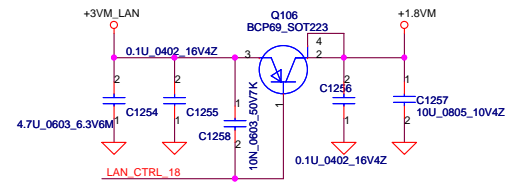
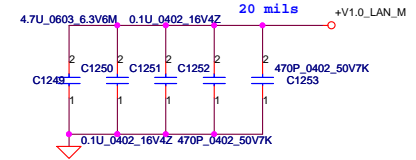
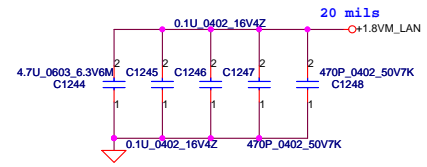
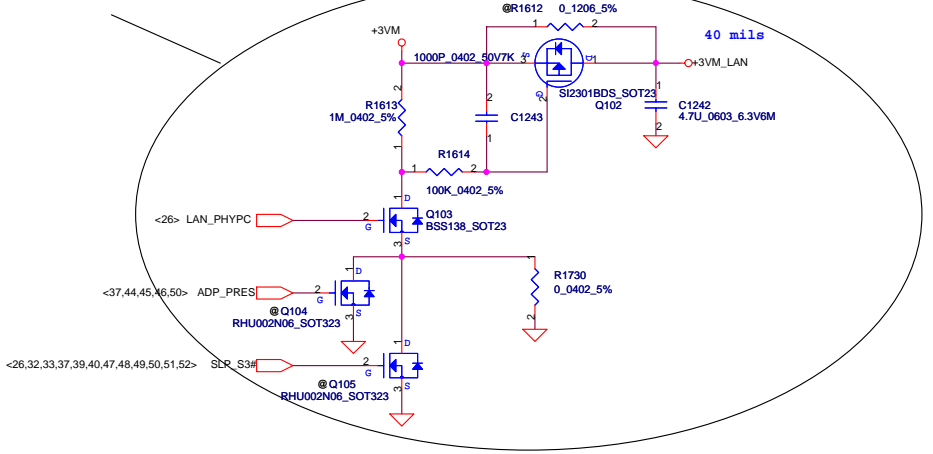
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Title		
Compal Electronics, Inc.		
ICH8(4/4) POWER&GND		
Size	Document Number	Rev
Custort	LA3262P DIS_M64	1A
Date:	Tuesday, August 21, 2007	Sheet 27 of 57



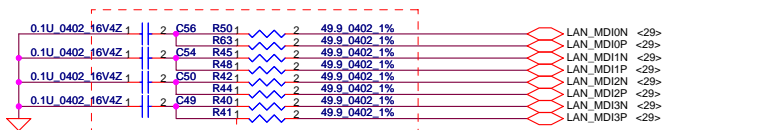
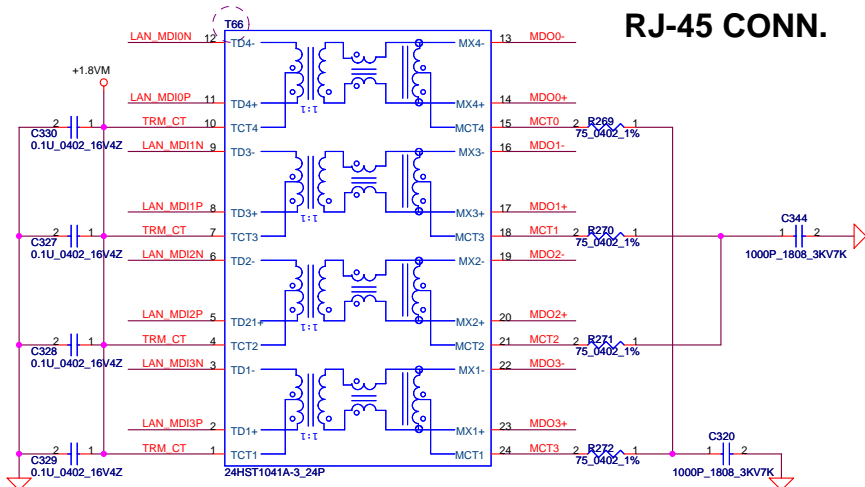
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Issued Date	2006/09/25	Deciphered Date	2006/09/25	HDD & CDROM	
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11/20 Enable ACBS (power management for NIC)



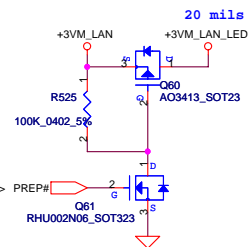
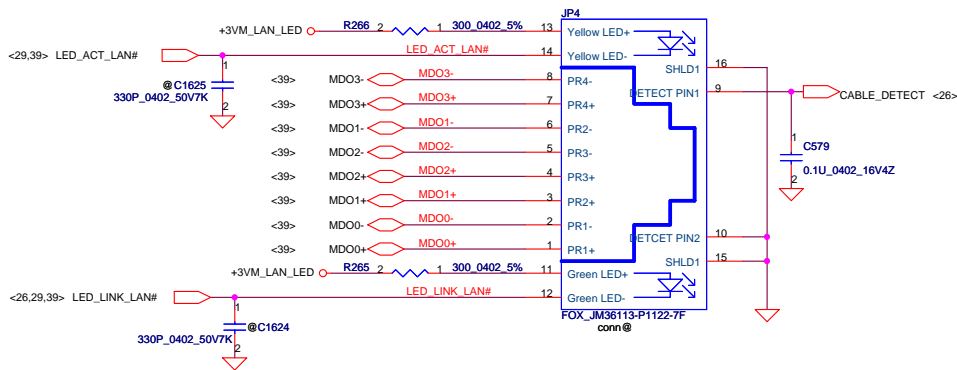
Security Classification		Compal Secret Data		Title	
Issued Date	2006/09/25	Deciphered Date	2006/09/25	Compal Electronics, Inc.	
				Intel 82566 Nineveh	
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RJ-45 CONN.



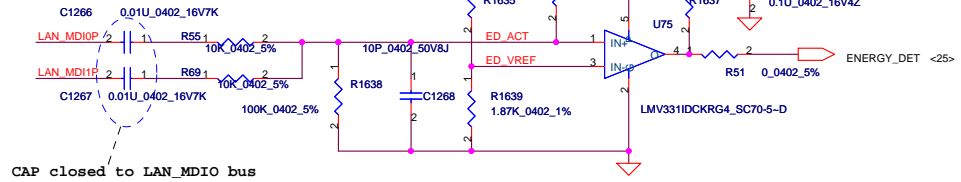
Layout Notice : Place termination as close as Intel 82566 as possible

Note: MDO[3..0]+/- signals should route to JP4 first then to JP30.

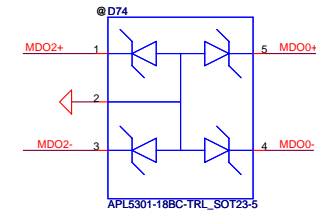
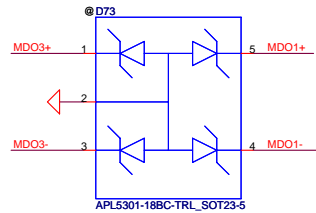


LAN ENERGY DET

02/27 change



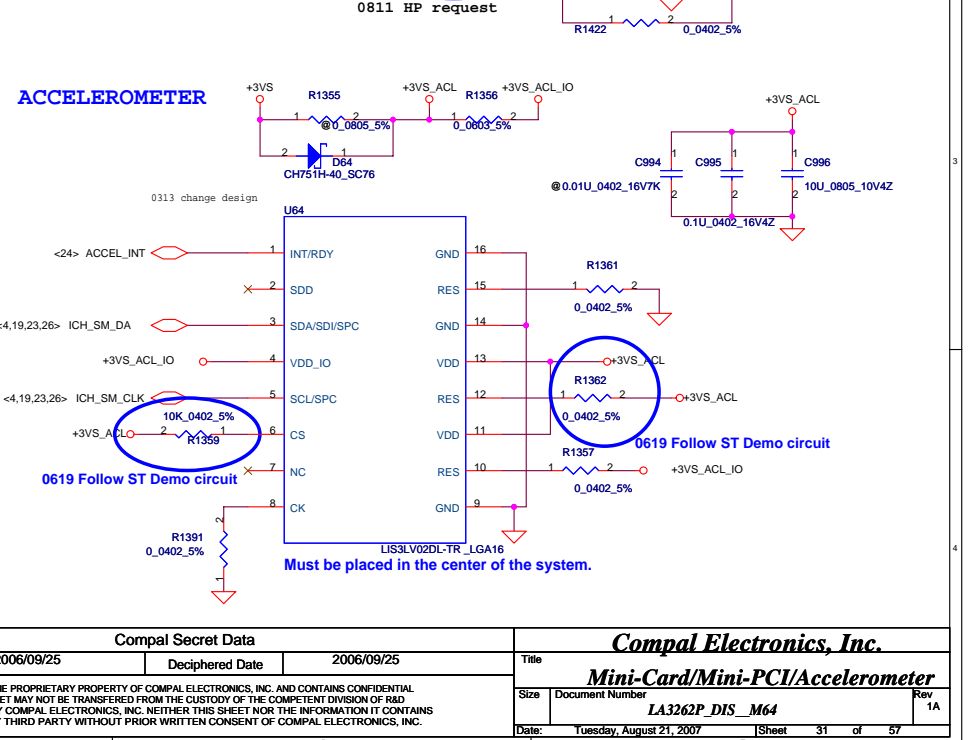
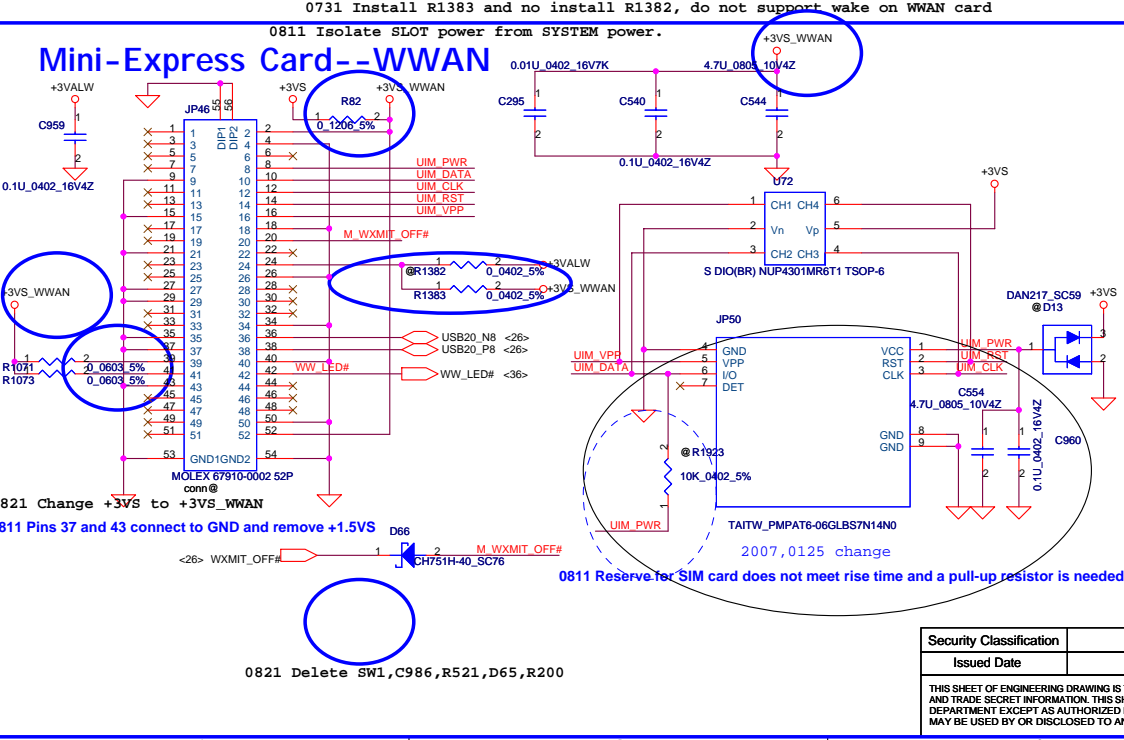
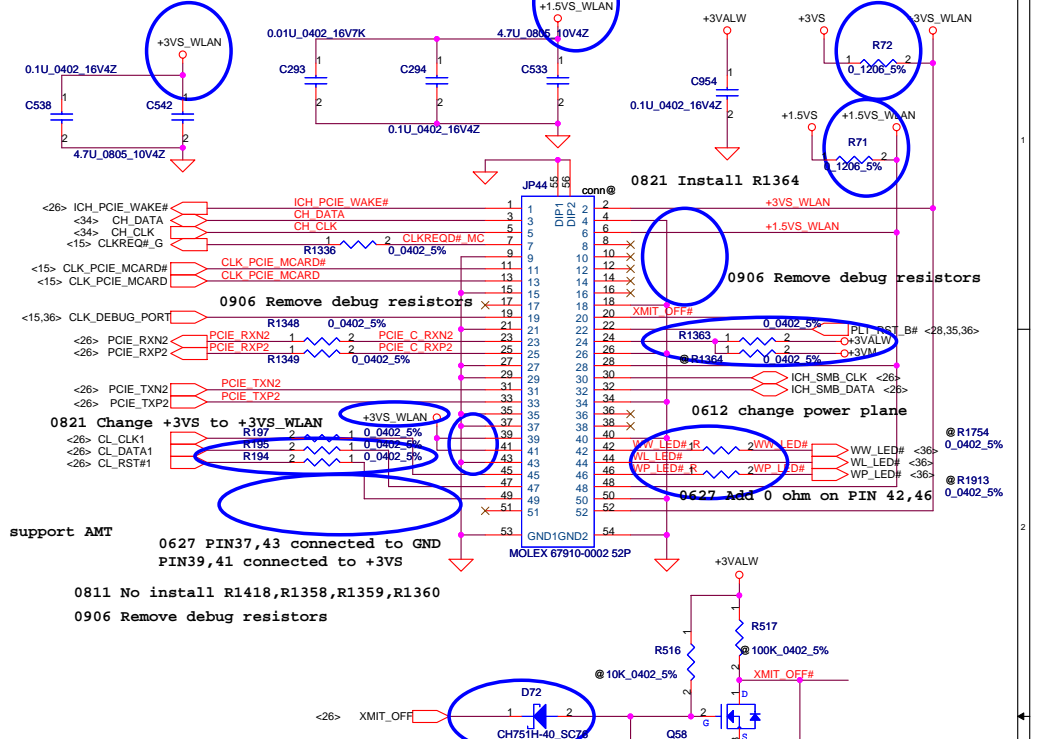
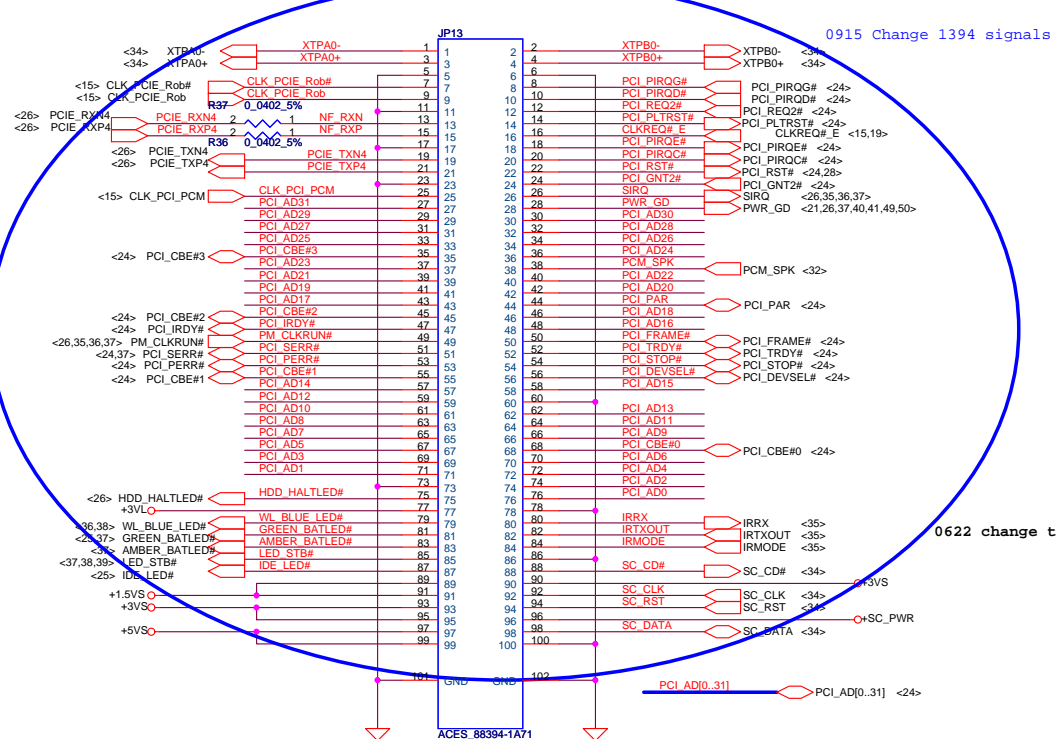
CAP closed to LAN_MDIO bus



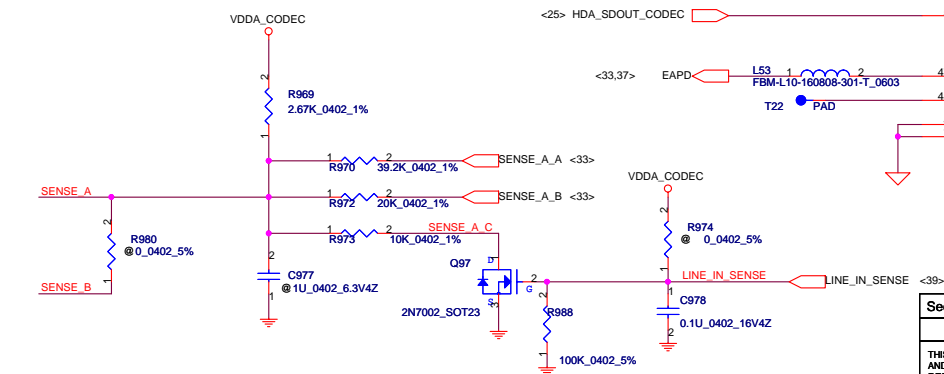
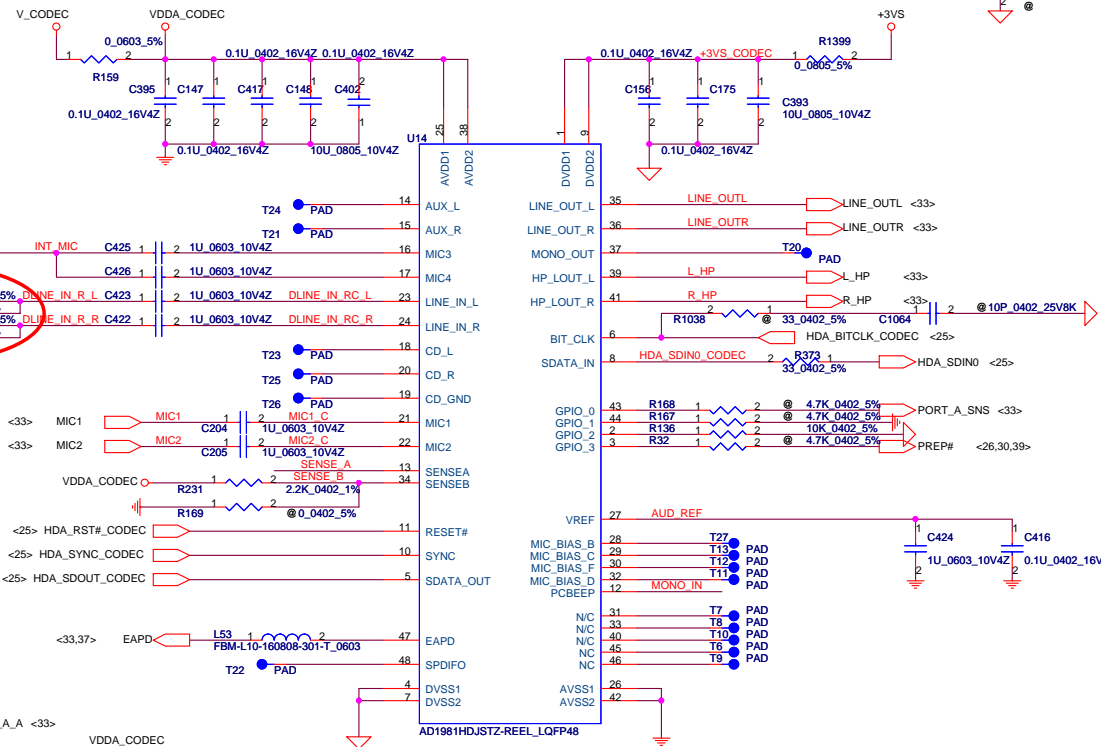
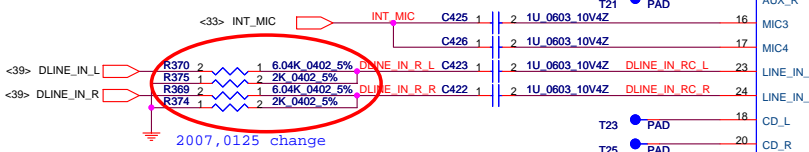
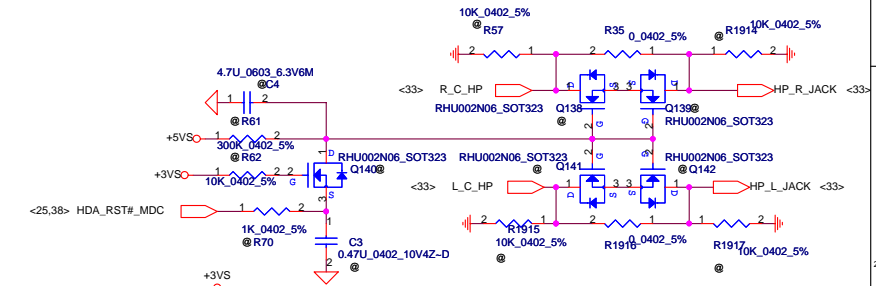
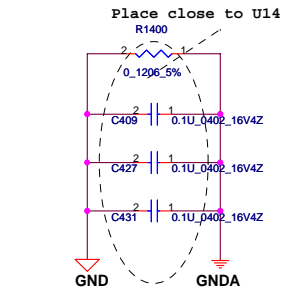
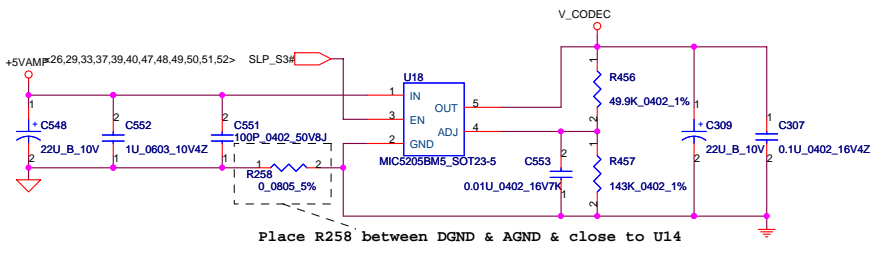
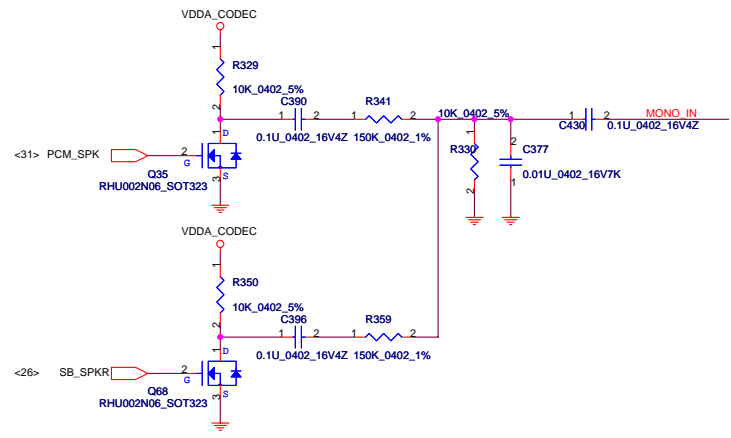
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				Size	Document Number	Rev	
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B/B connector with PCI / LED / FIR / SC interface

Mini-Express Card---WLAN



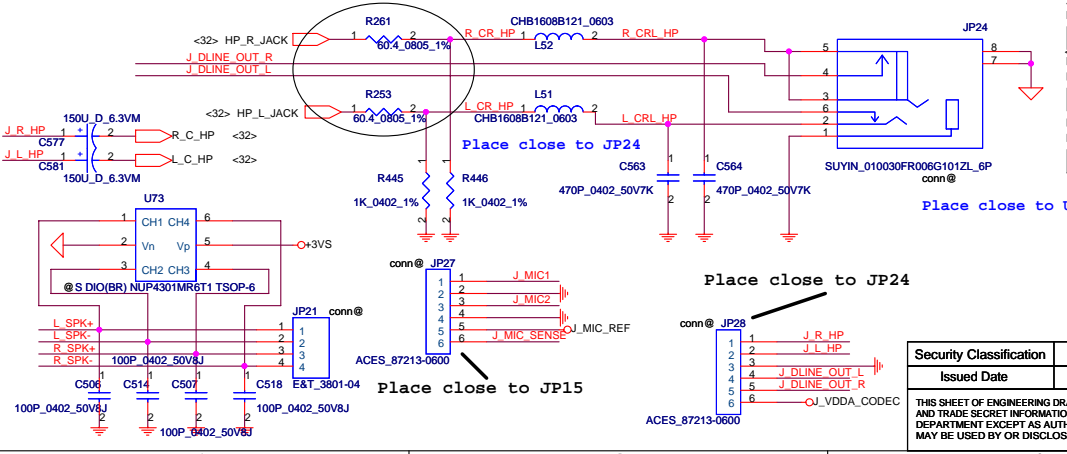
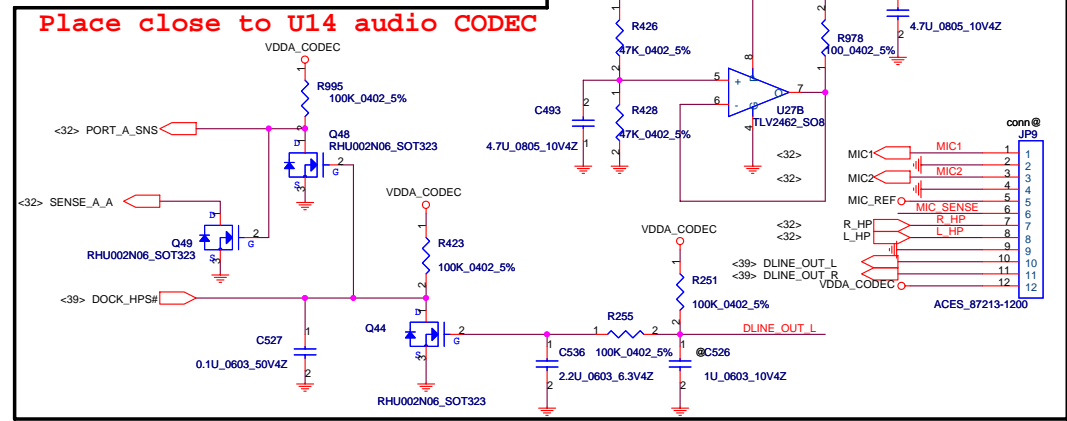
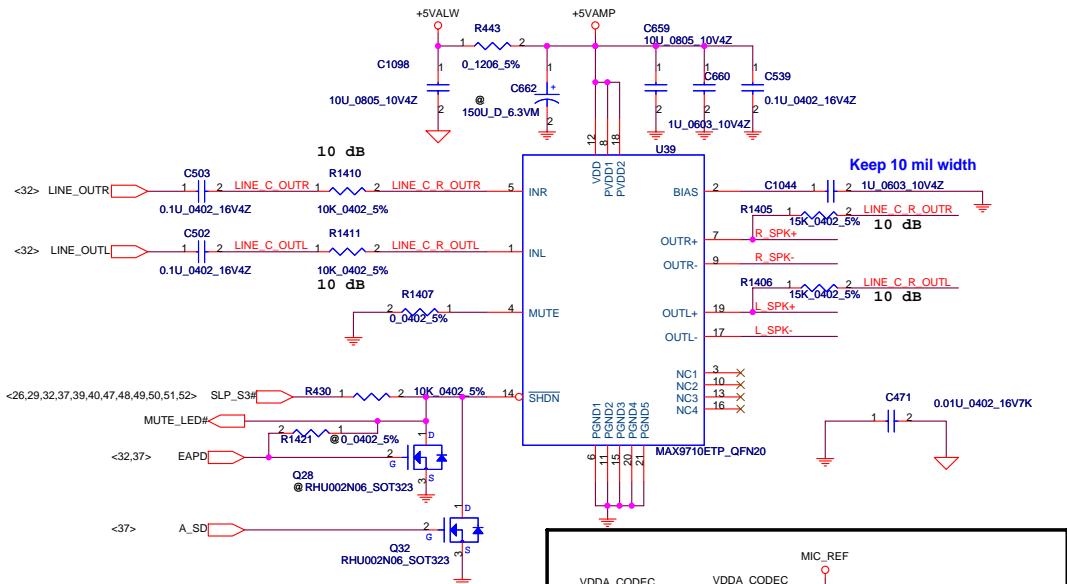
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Issued Date	2006/09/25	Deciphered Date	2006/09/25	Mini-Card/Mini-PCI/Accelerometer	
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PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

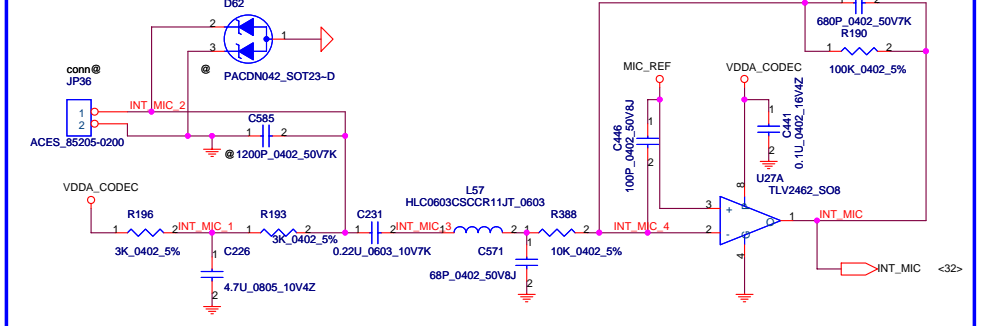
Security Classification	Compal Secret Data		Title	
Issued Date	2006/09/25	Deciphered Date	2006/09/25	Compal Electronics, Inc.
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				Document Number
				LA326P_DIS_M64
				Rev 1A
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AMP. FOR INTERNAL SPEAKER



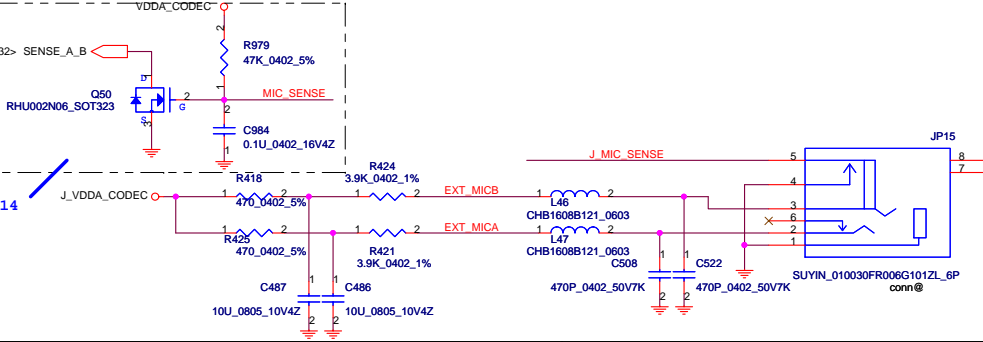
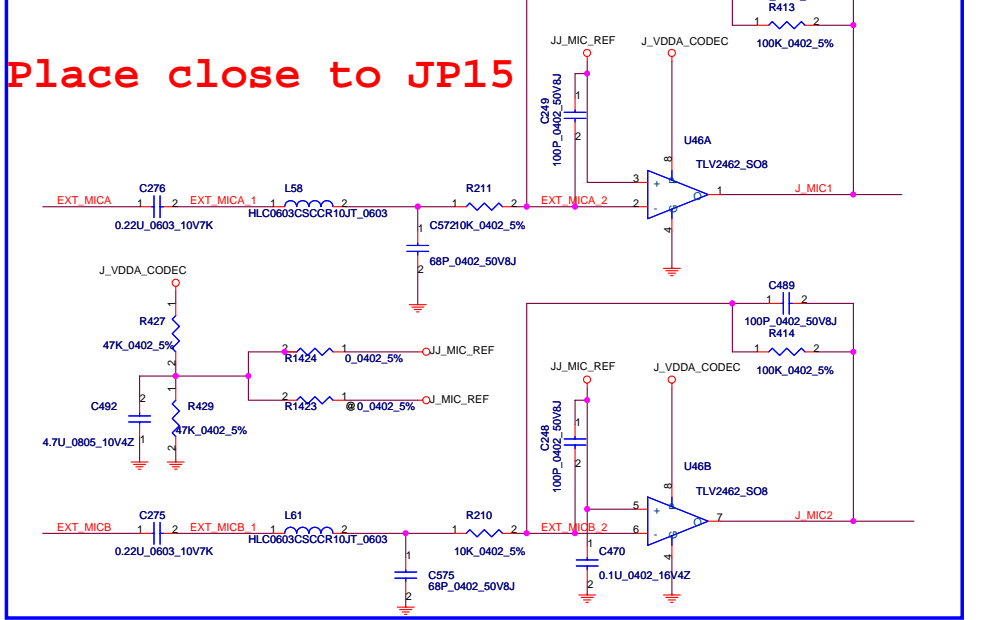
AMP. FOR INTERNAL MICROPHONE

Place close to U14 audio CODEC



AMP. FOR EXTERNAL MICROPHONE

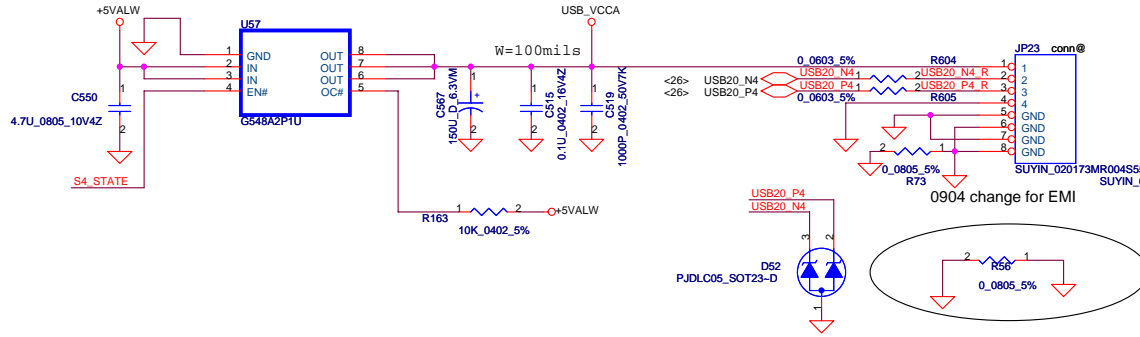
Place close to JP15



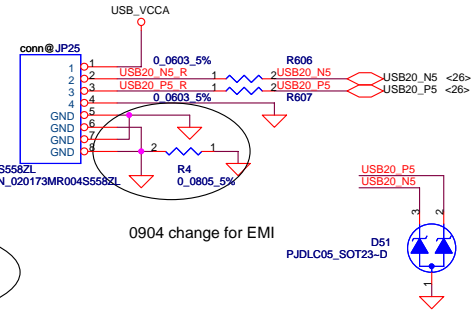
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Issued Date	2006/09/25	2006/09/25	2006/09/25	2006/09/25	Compal Electronics, Inc.	
AMP & Audio Jack						
Size	Document Number	Date		Sheet	33 of 57	Rev 1A
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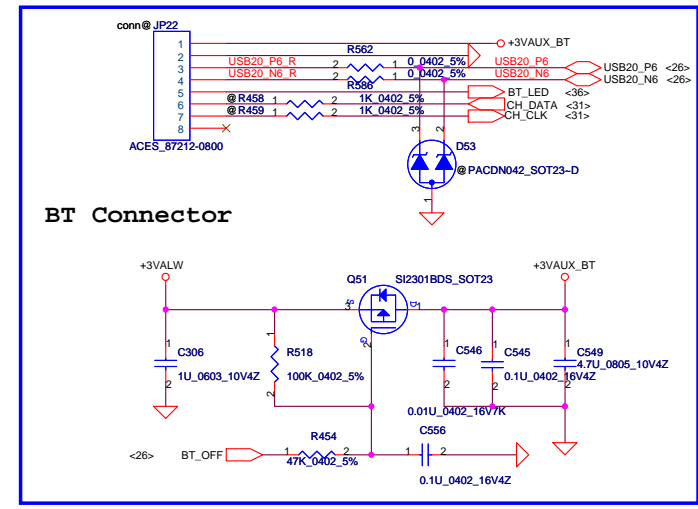
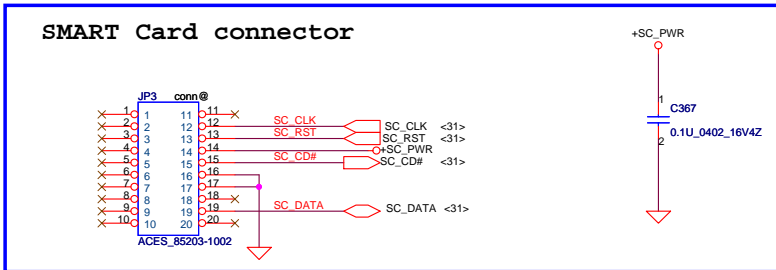
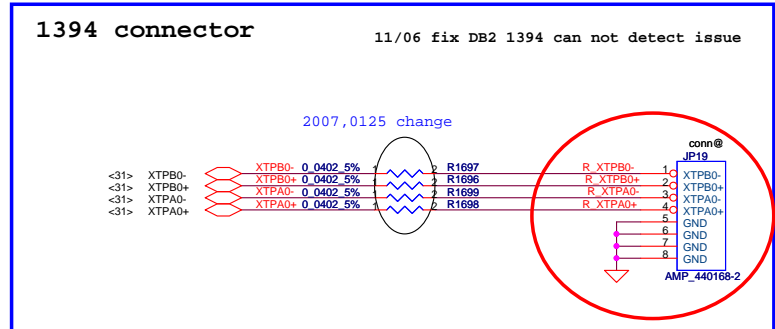
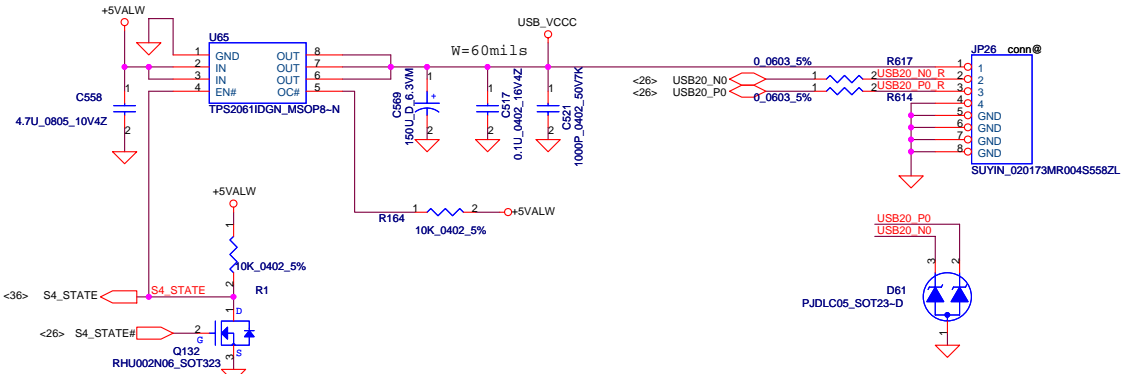
Left side USB CONNECTOR 0



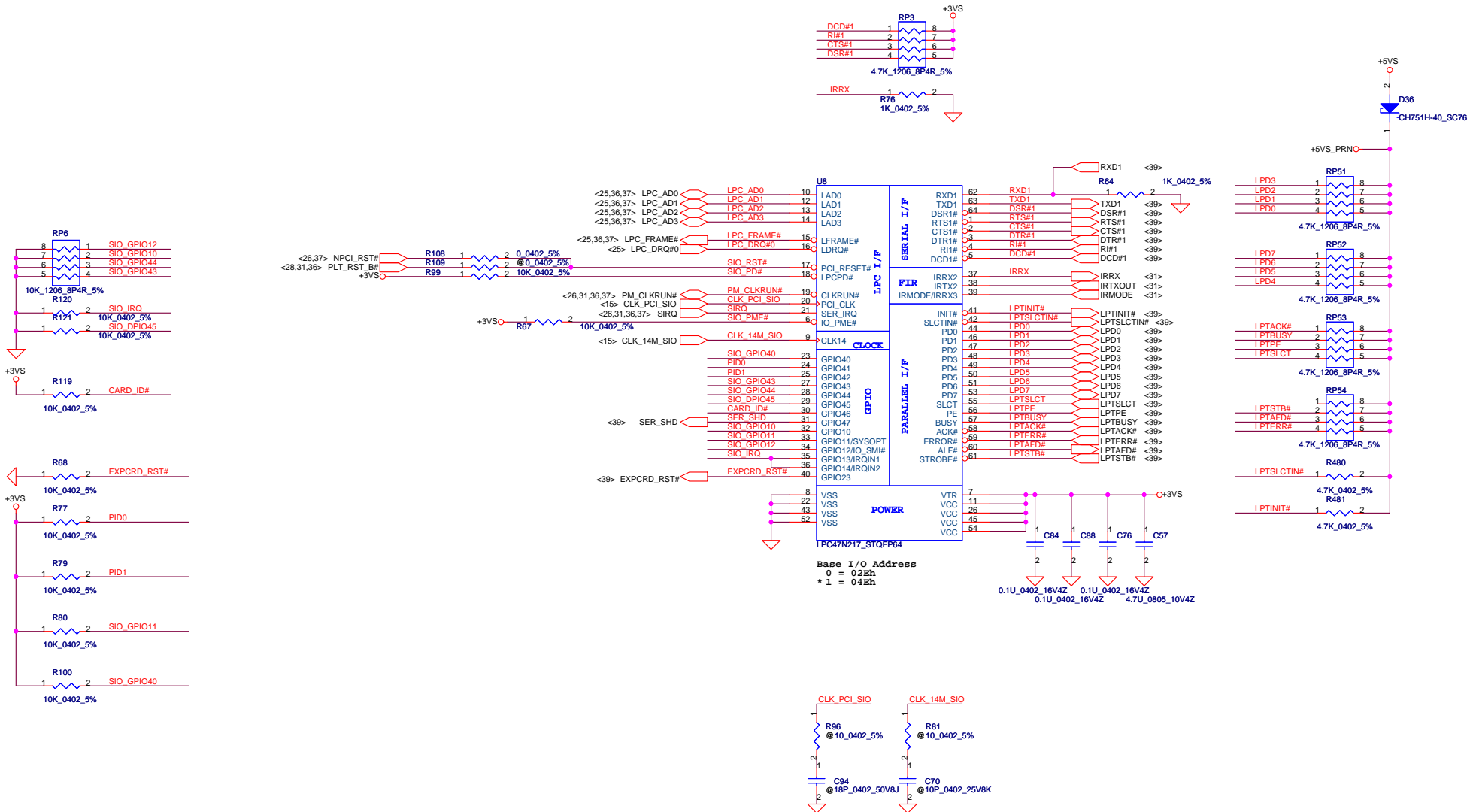
Left side USB CONNECTOR 1



Right side USB CONNECTOR 0

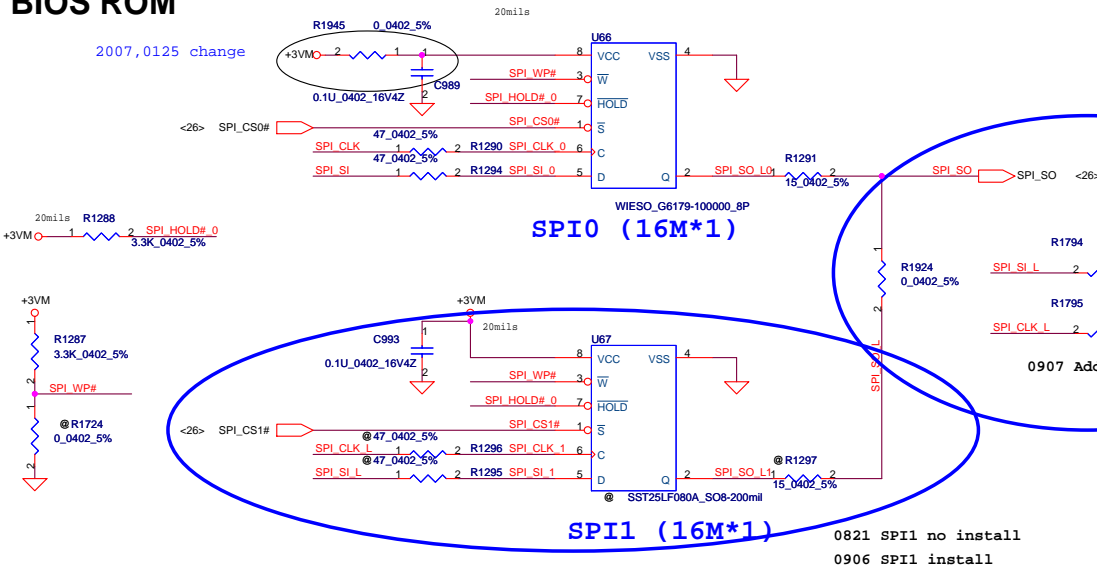


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				LA3262P_DIS_M64	Rev 1A
Date:				Tuesday, August 21, 2007	Sheet 34 of 57

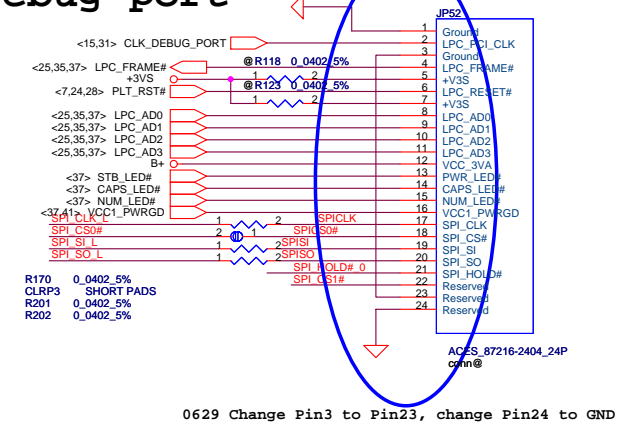


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				Rev	1A
				Date:	Tuesday, August 21, 2007
				Sheet	35 of 57

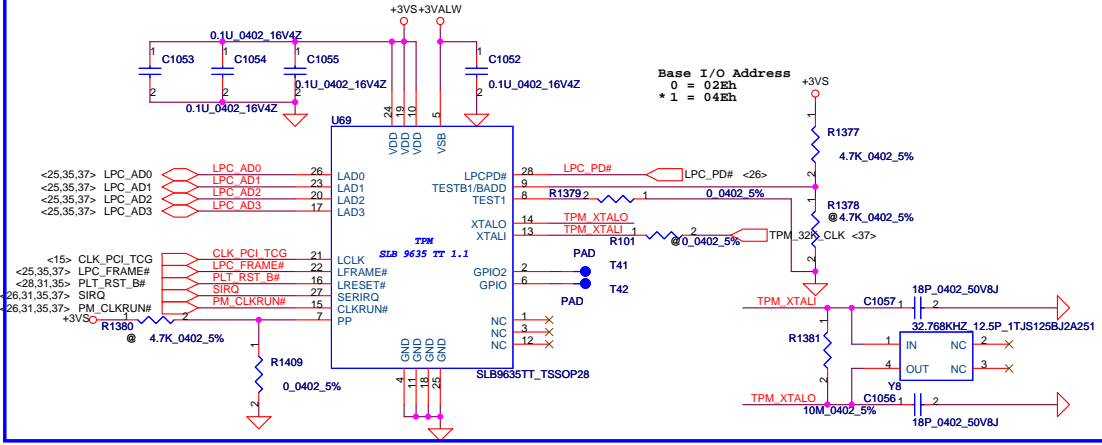
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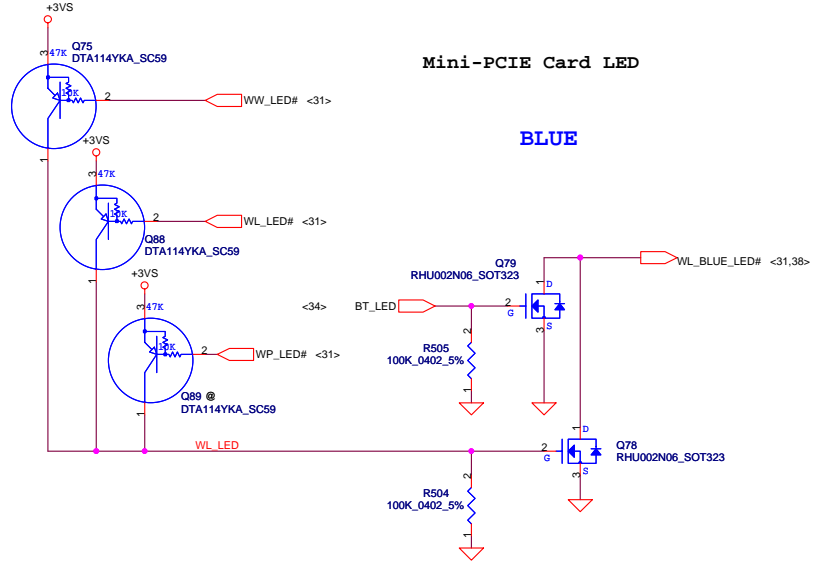
Debug port



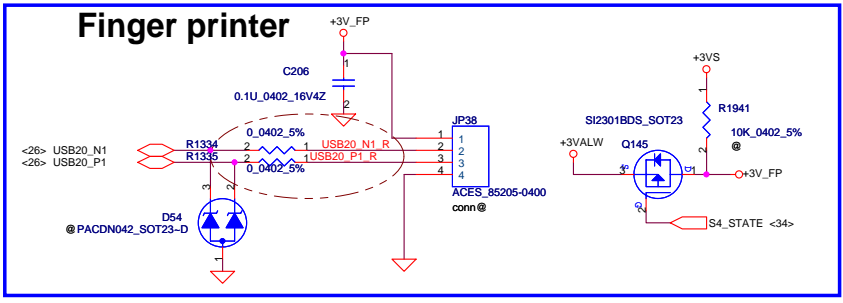
TPM1.2



Mini-PCIE Card LED

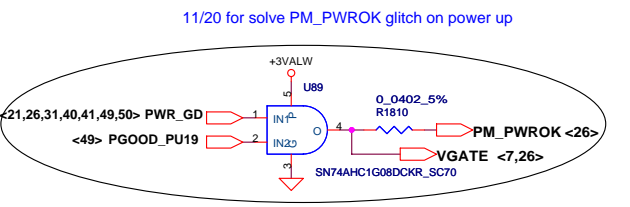
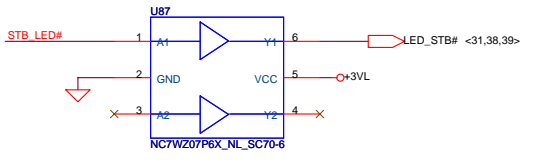
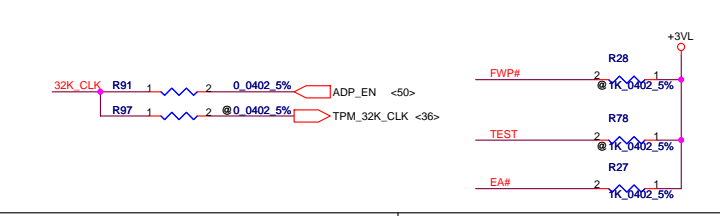
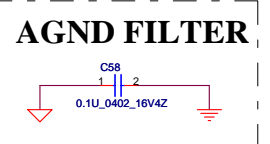
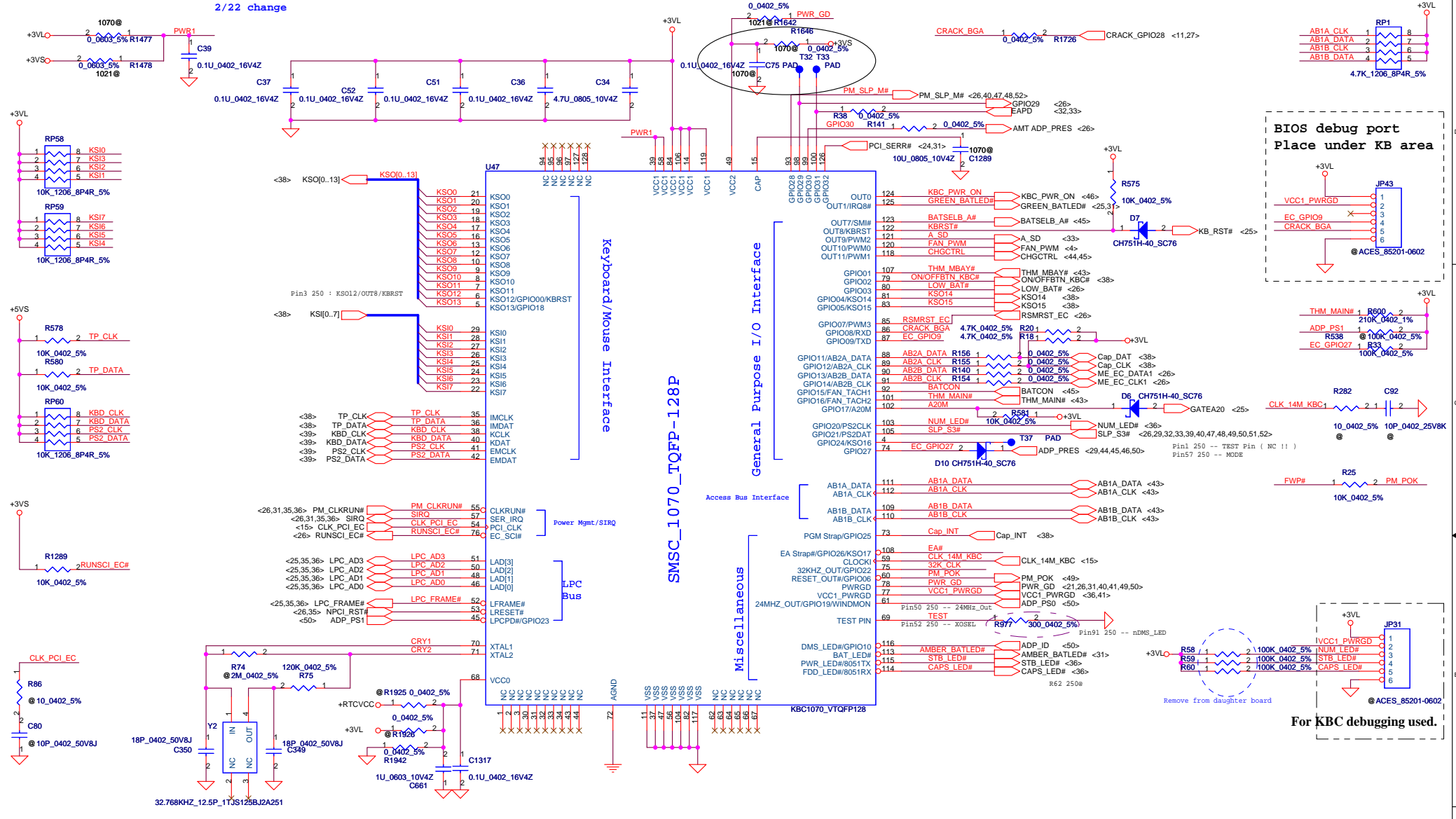


Finger printer



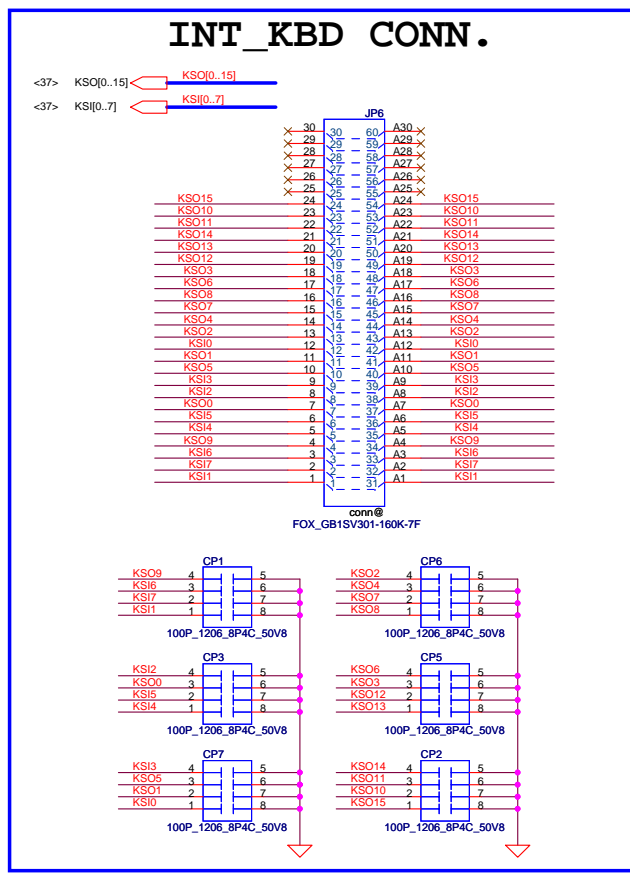
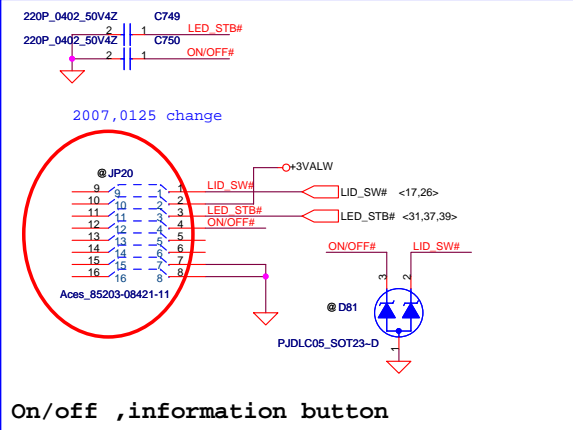
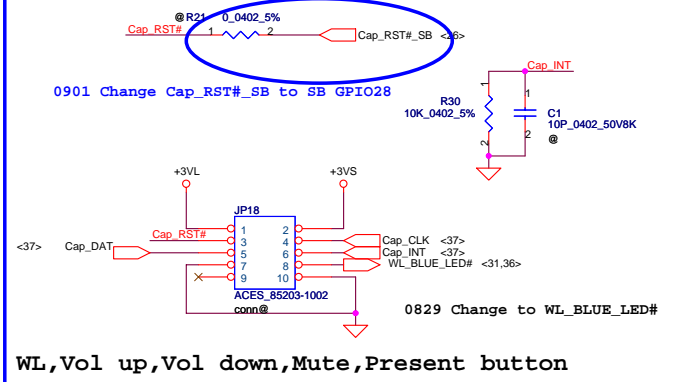
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/09/25	Deciphered Date	2006/09/25	TCG/BIOS ROM/PS2/LED/SW	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					
Size	Document Number	LA3262P_DIS_M64		Rev	1A
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2/22 change

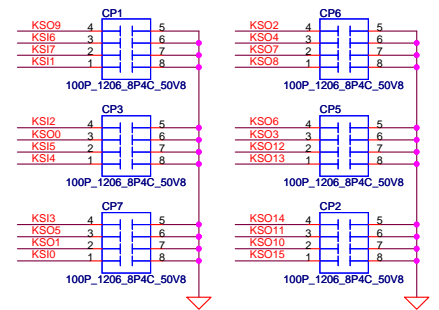
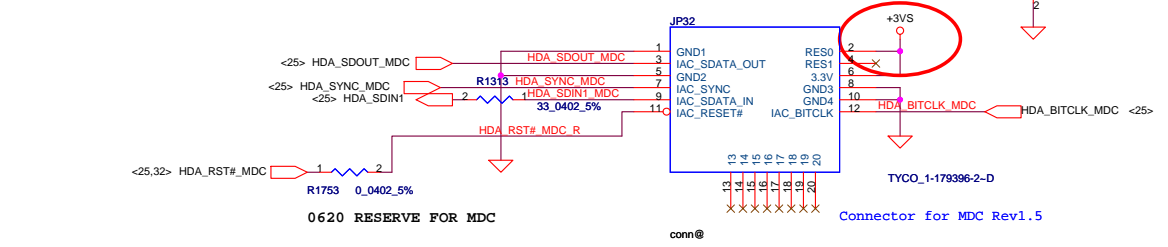


Security Classification		Compal Secret Data		Title	
Issued Date	2006/09/25	Deciphered Date	2006/09/25	LPC47N1021	
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Size	Document Number	Date:		Rev	
	LA3262P_DIS_M64	Tuesday, August 21, 2007		1A	
				Sheet	57

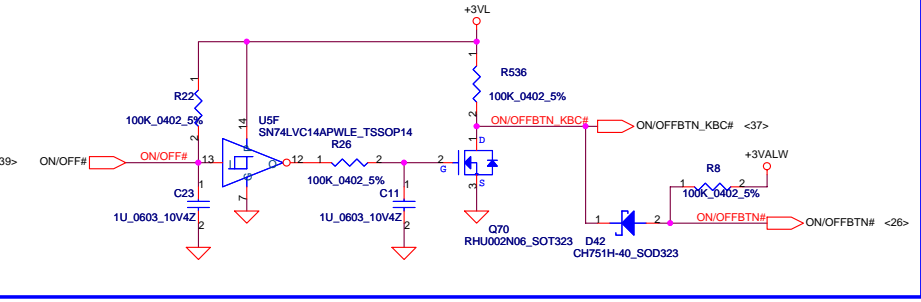
SWITCH BOARD. 0622 change



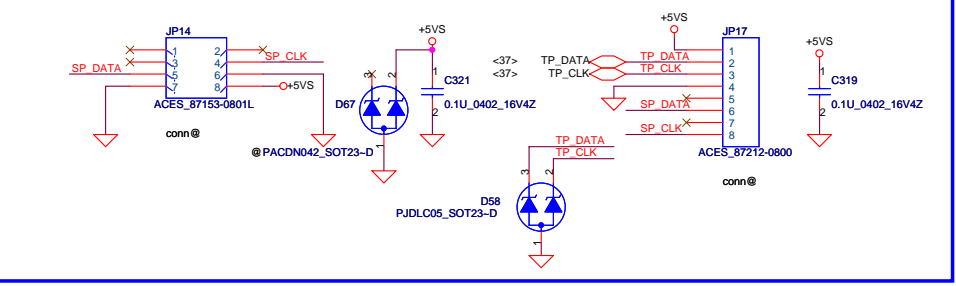
MDC 1.5 Conn.



Power button



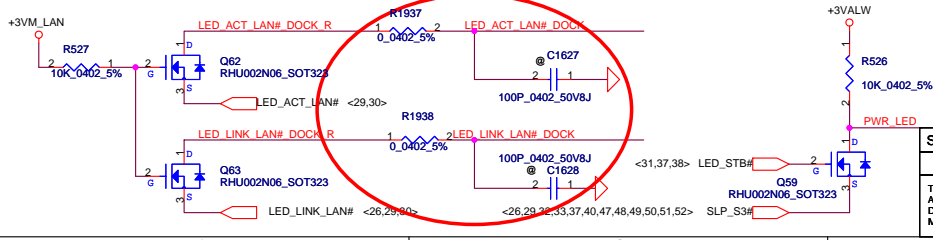
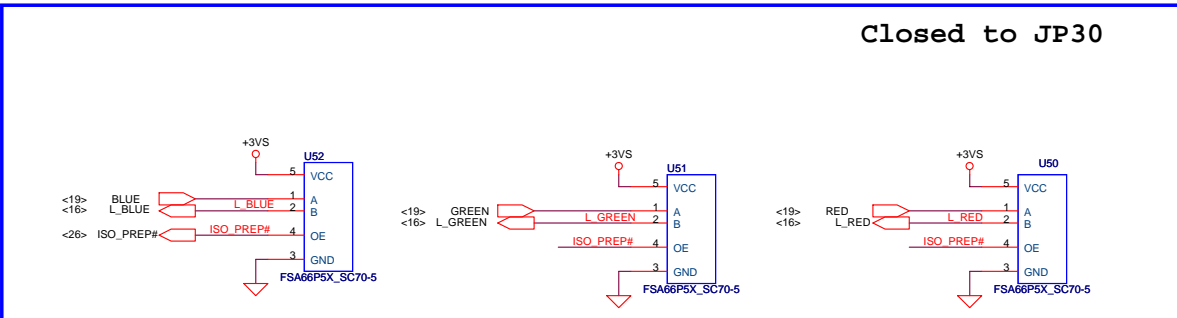
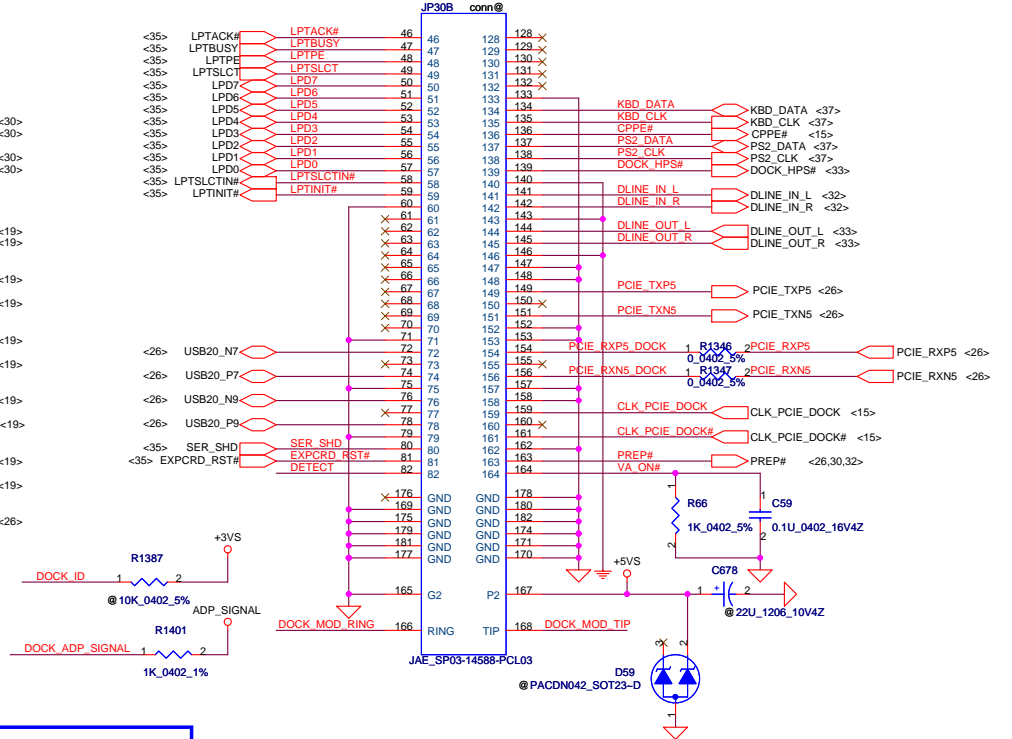
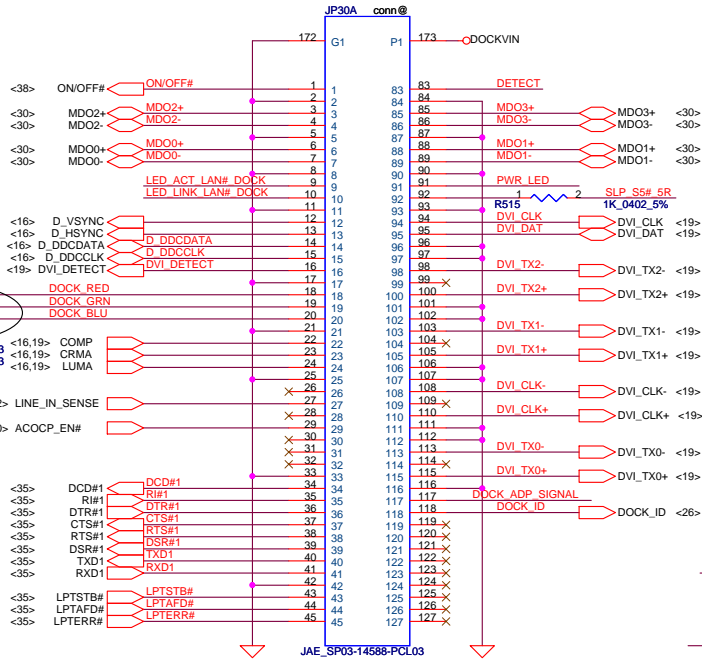
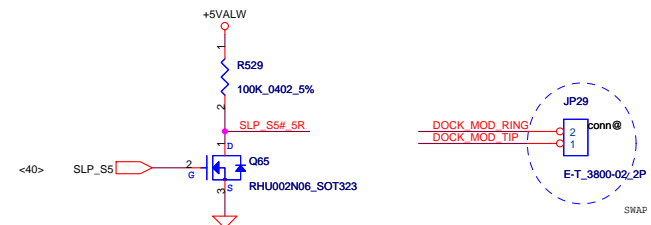
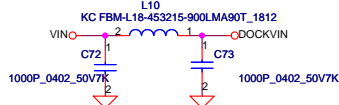
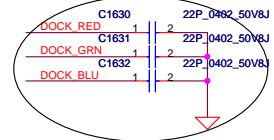
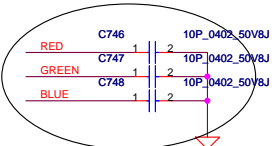
TrackPoint CONN.



T/P BOARD.

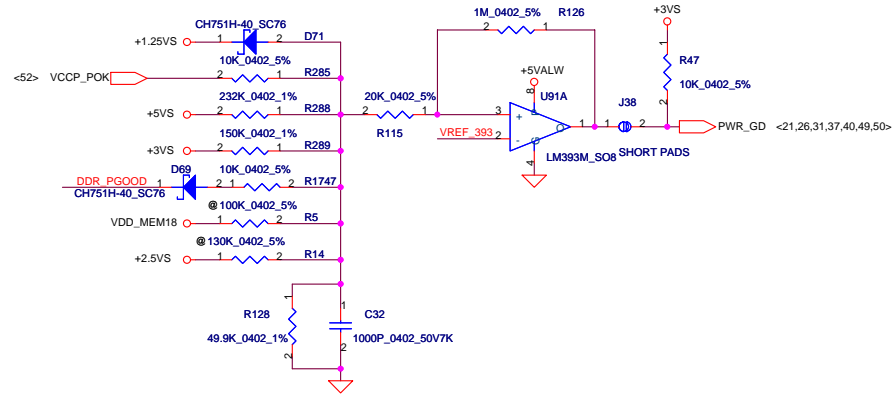
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/09/25	Deciphered Date	2006/09/25	Title
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Size	Document Number	Rev	1A	
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DOCK CONN. 184PIN

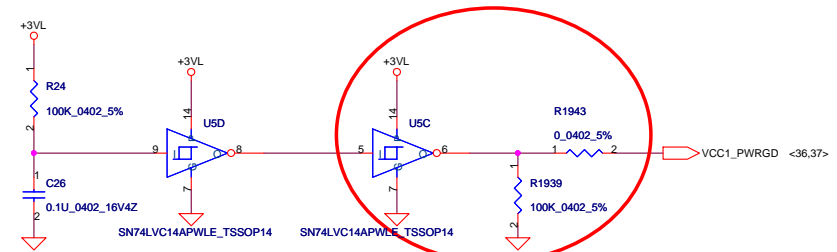


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Issued Date	2006/09/25	Deciphered Date	2006/09/25	Compal Electronics, Inc.
				Docking CONN.
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Date: Tuesday, August 21, 2007				Rev 1A
				Sheet 39 of 57

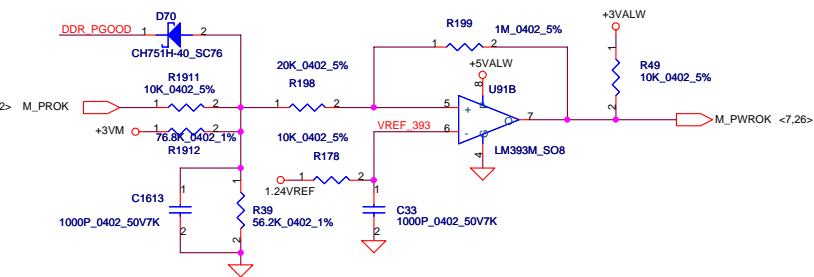
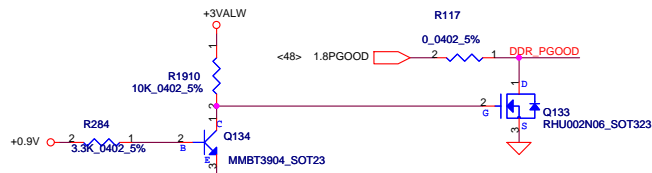
PWR_OK circuit



KBC PWR_OK circuit

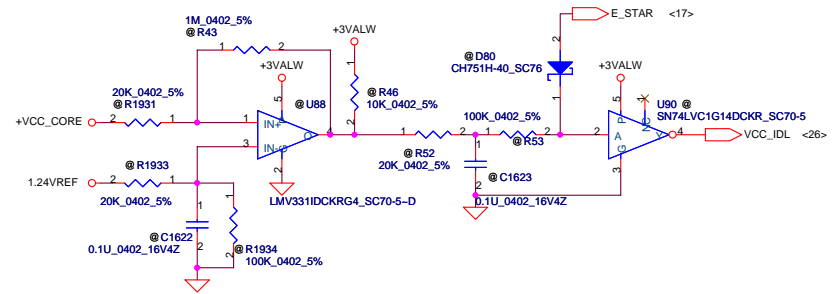


1219 Add Schmitt Trigger to eliminate glitch and pull down resistor



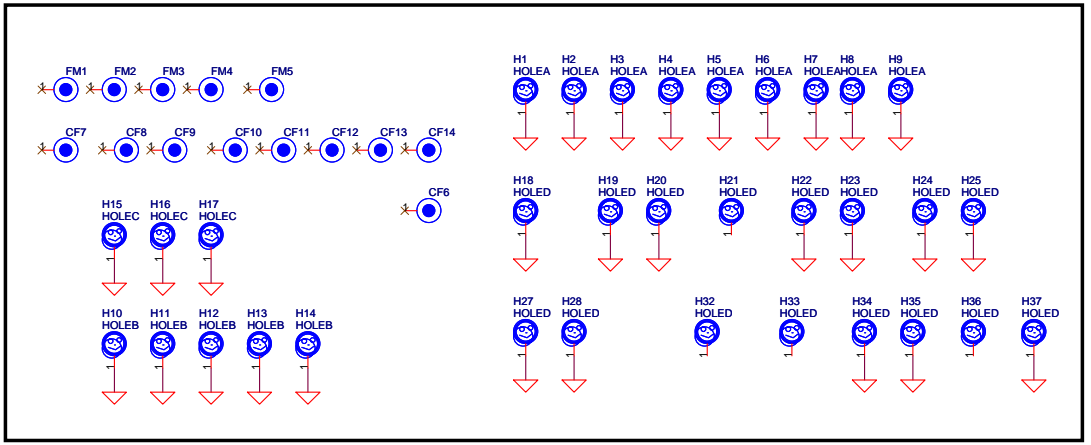
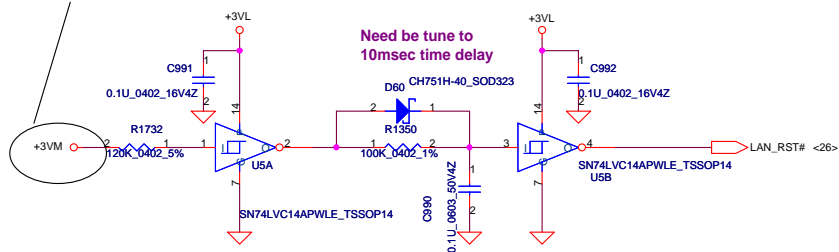
Energy Star for CPU

1114 Add

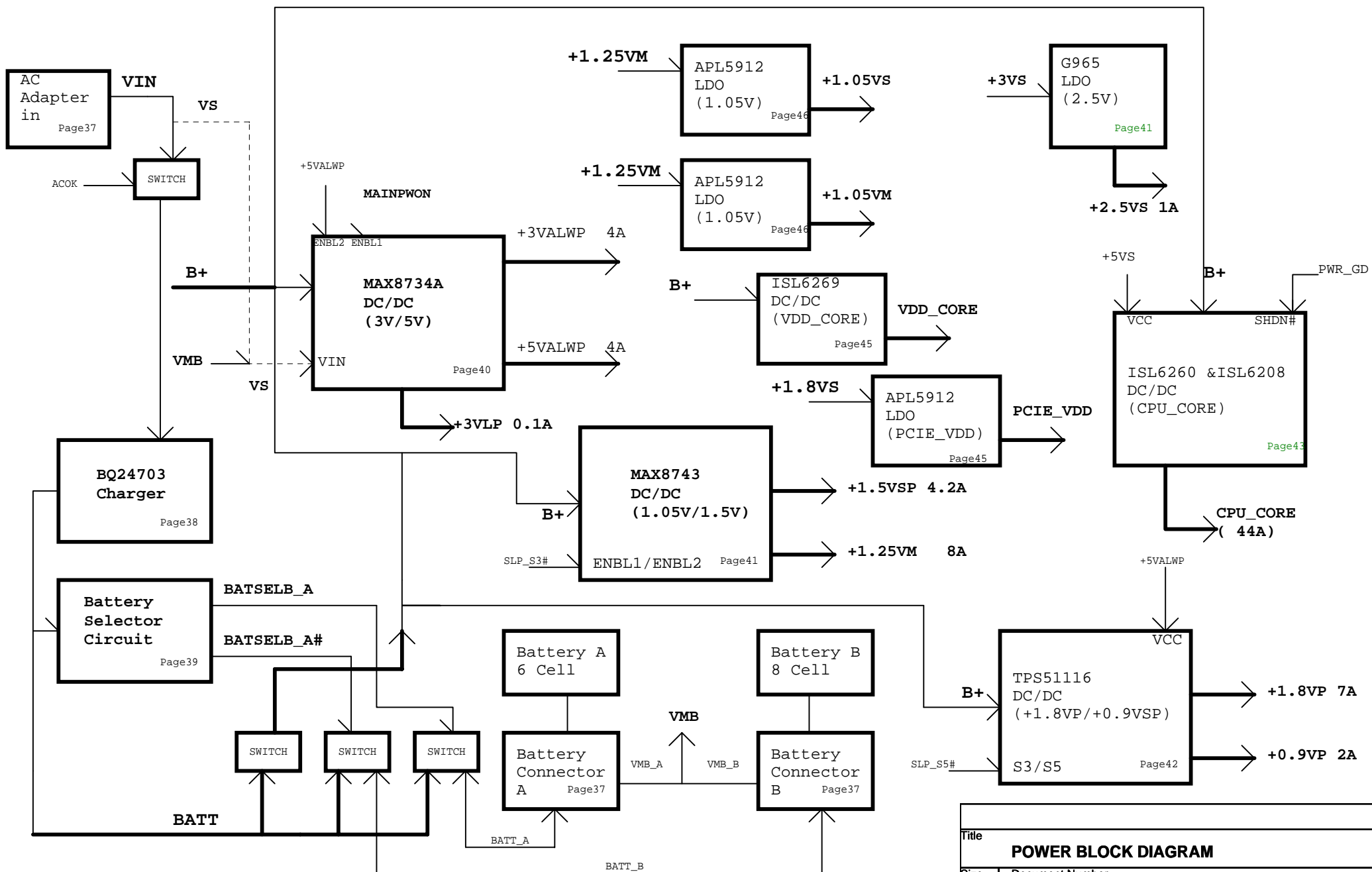


LAN_RST circuit

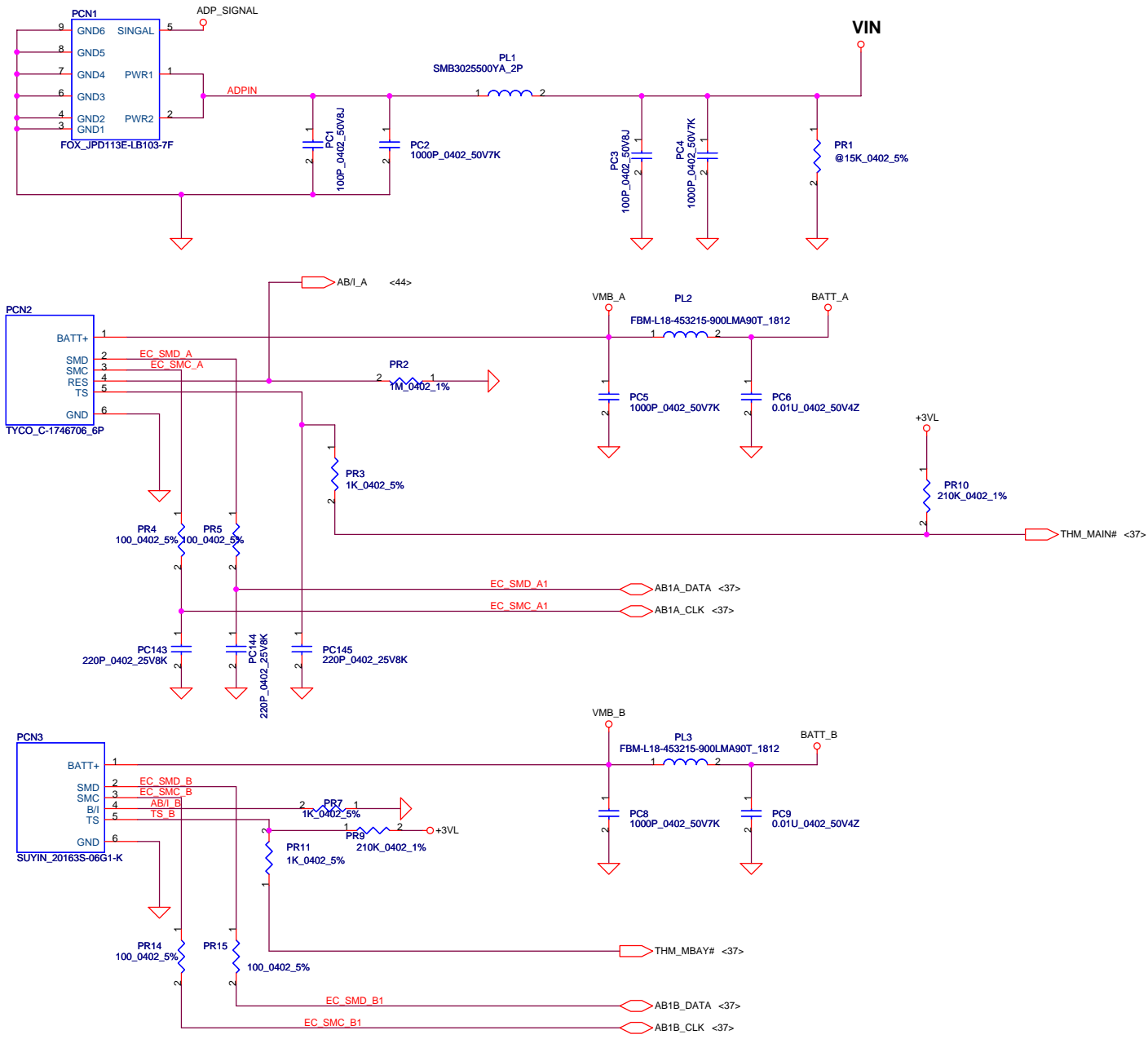
11/20 Enable ACBS (power management for NIC)



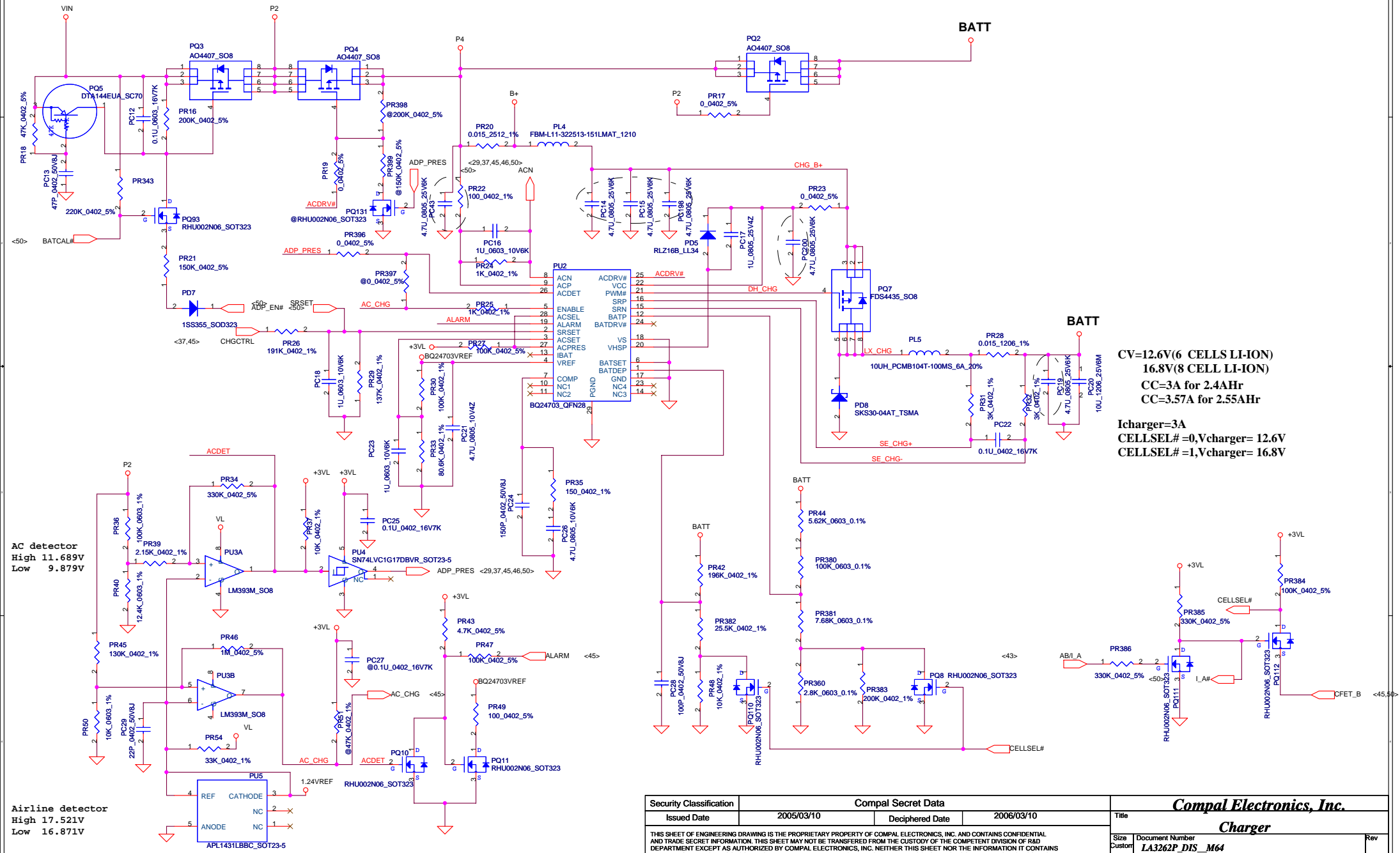
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/09/25	Deciphered Date	2006/09/25	Title	POK CKT
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Title		
POWER BLOCK DIAGRAM		
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Security Classification		Compal Secret Data		Compal Electronics, Inc. BATTERY CONN	
Issued Date	2005/03/10	Deciphered Date	2006/03/10		
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				Date:	Tuesday, August 21, 2007 Sheet 43 of 57

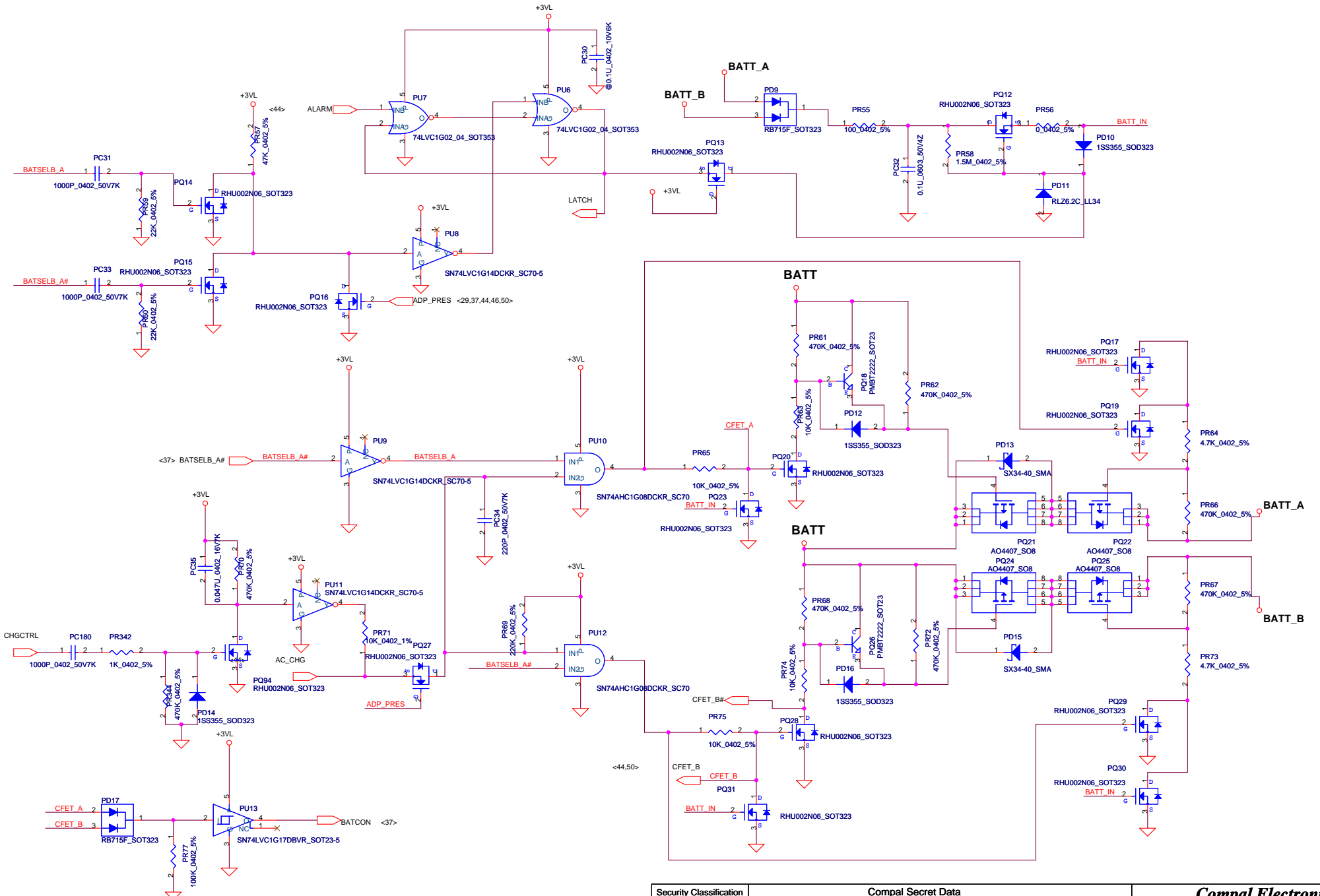


CV=12.6V(6 CELLS LI-ION)
16.8V(8 CELL LI-ION)
CC=3A for 2.4Ahr
CC=3.57A for 2.55Ahr
Icharger=3A
CELLSEL# =0,Vcharger= 12.6V
CELLSEL# =1,Vcharger= 16.8V

Security Classification		Compal Secret Data	
Issued Date	2005/03/10	Deciphered Date	2006/03/10

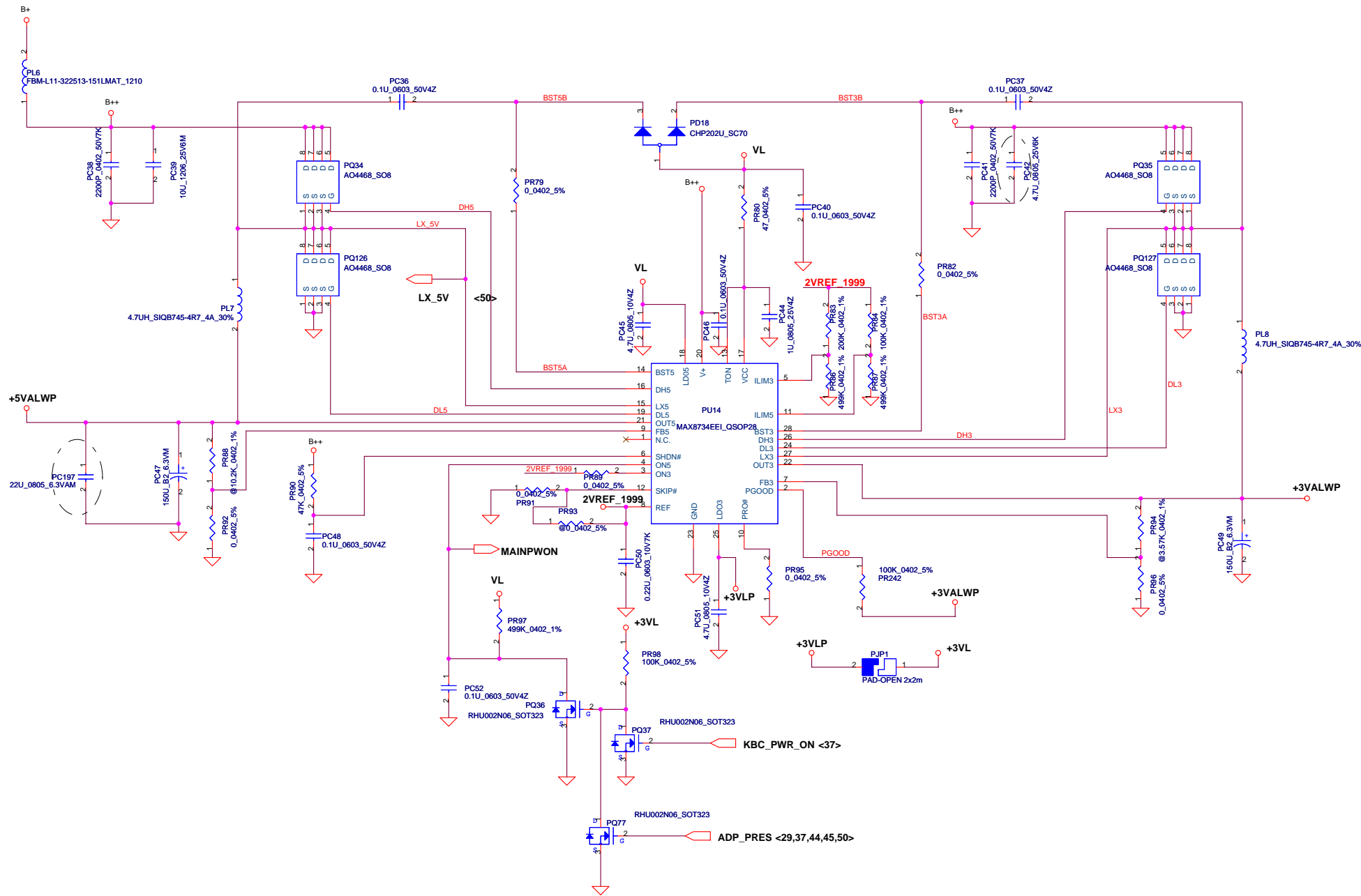
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Compal Electronics, Inc.			
Charger			
Size	Document Number		Rev
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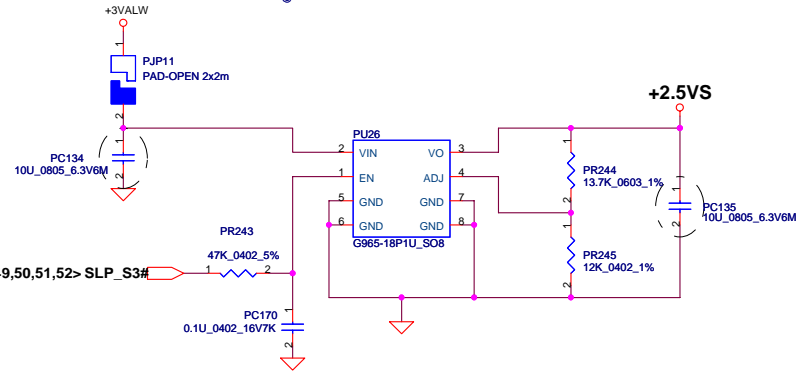
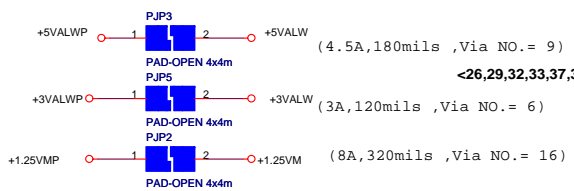
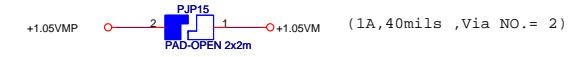
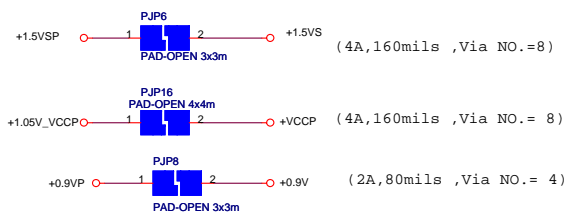
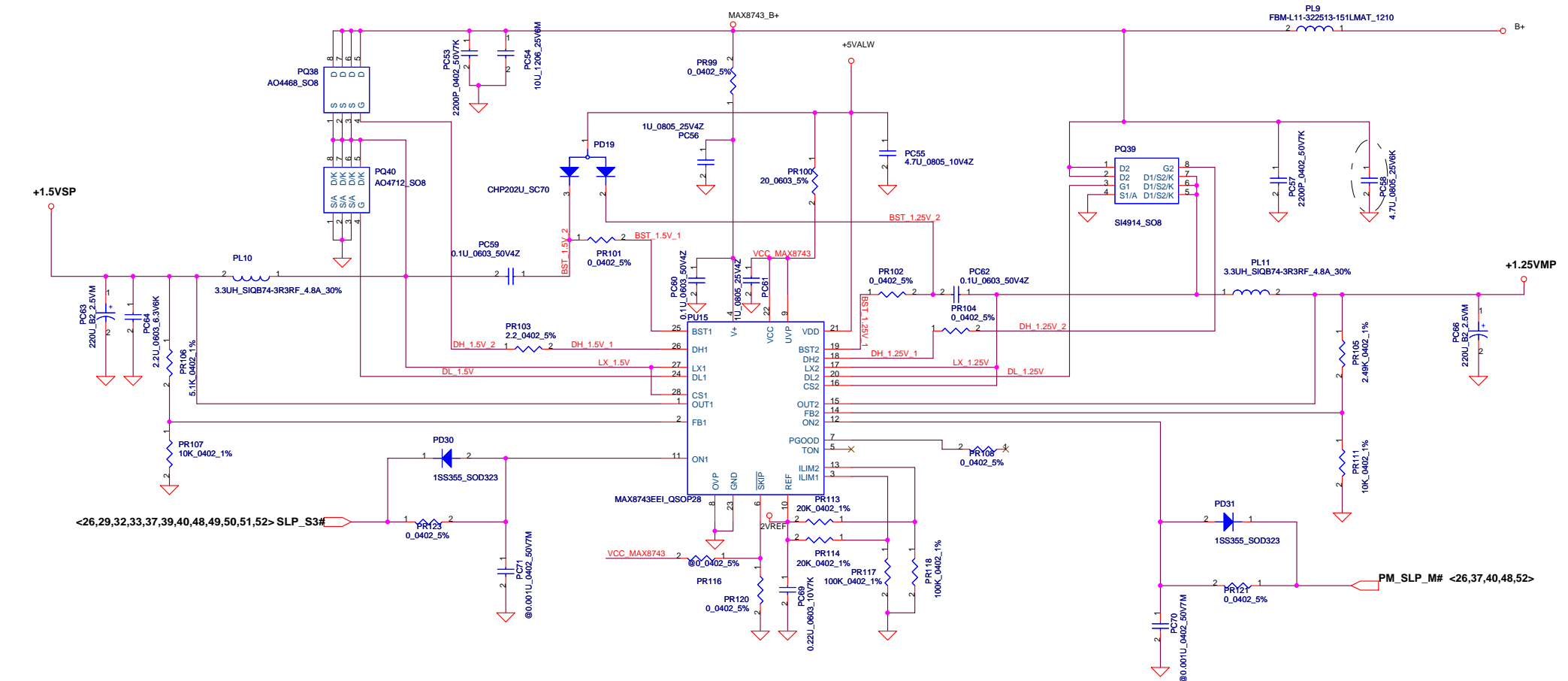


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				Document Number	
				LA3262P_DIS_M64	
				Date	Tuesday, August 21, 2007
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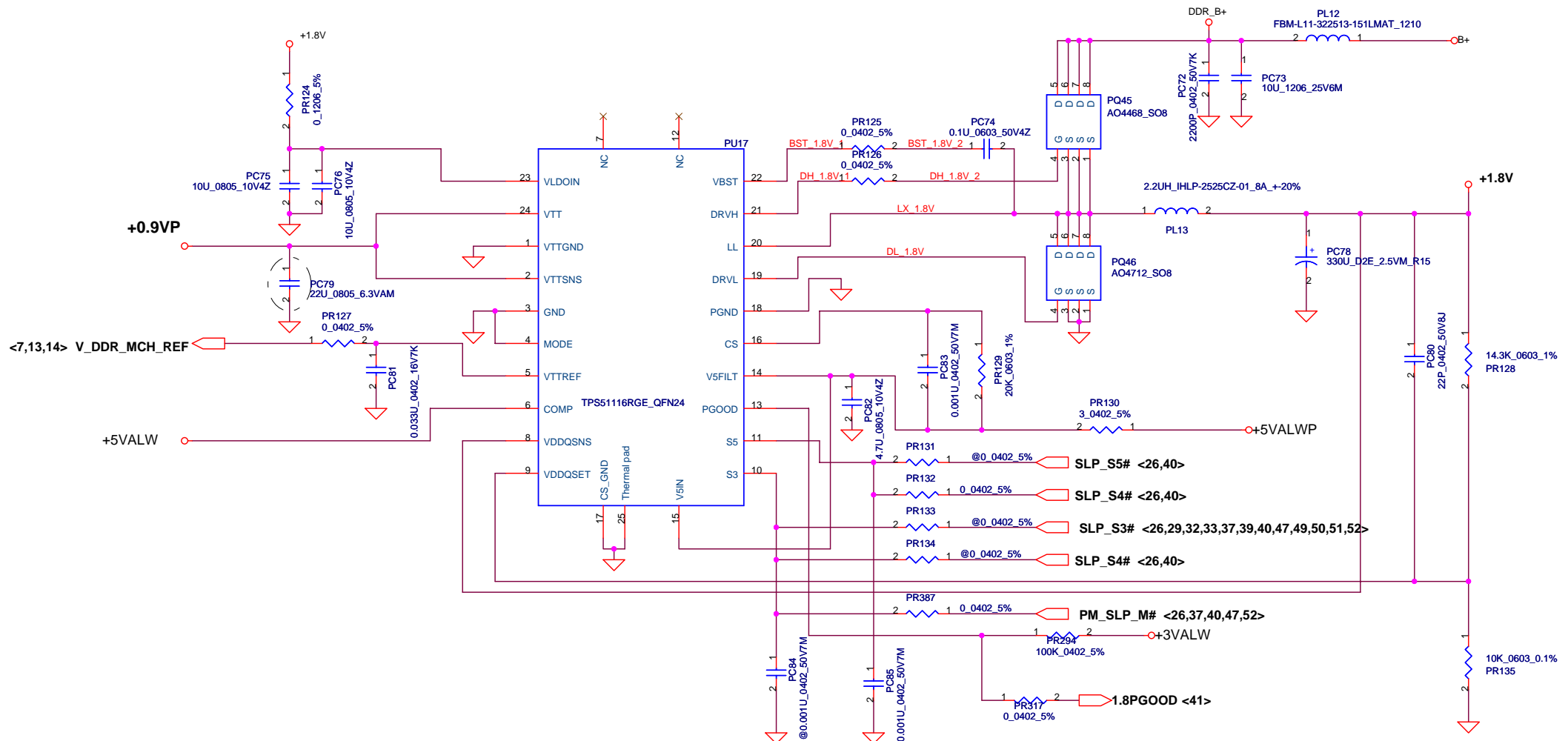
Battery selector



Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	3.3V / 5V	
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				B	LA3262P_DIS_M64
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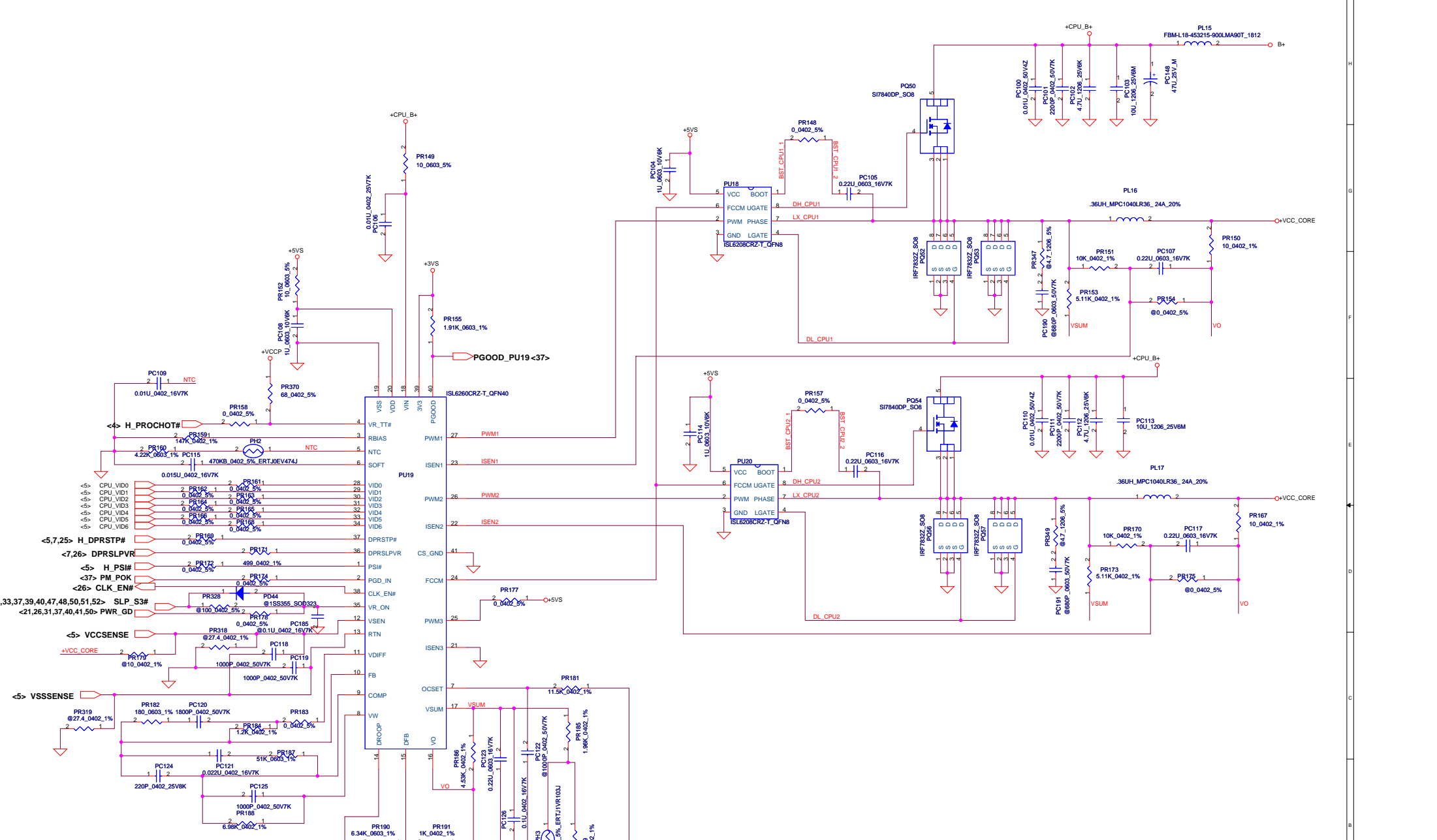
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	2.5VALW/1.5VS/1.25VMP	
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Issued Date	2005/03/10	Deciphered Date
		2006/03/10

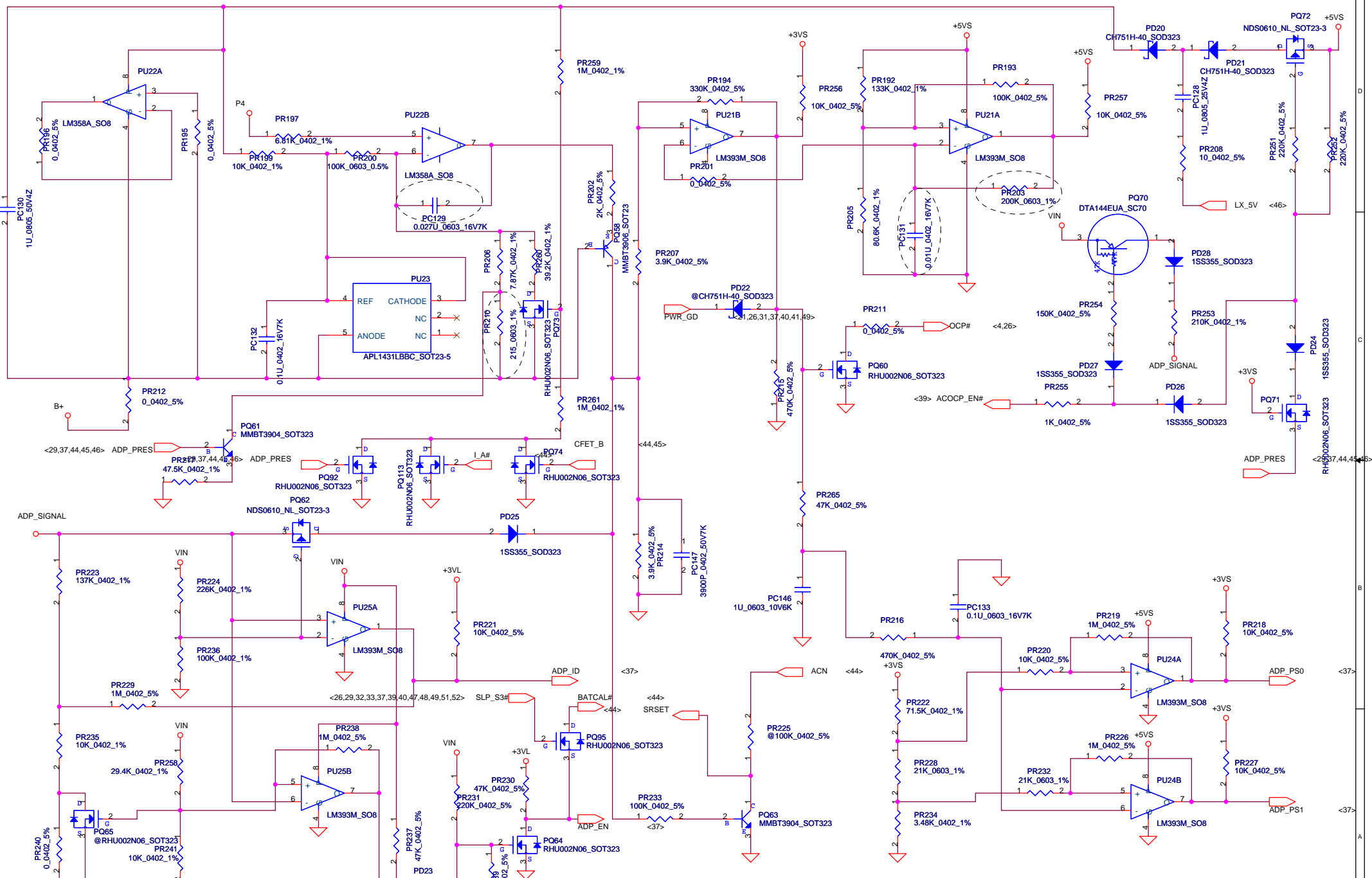
Compal Electronics, Inc.		
1.8V/0.9VS		
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PR179, PR180 are for test need when M/B is without CPU
 R1269, R1270 are same function with PR179, PR180
 Layout Note: Use 27.4 Ohm (PR318, PR319) routing for Vsesense and Vccsense

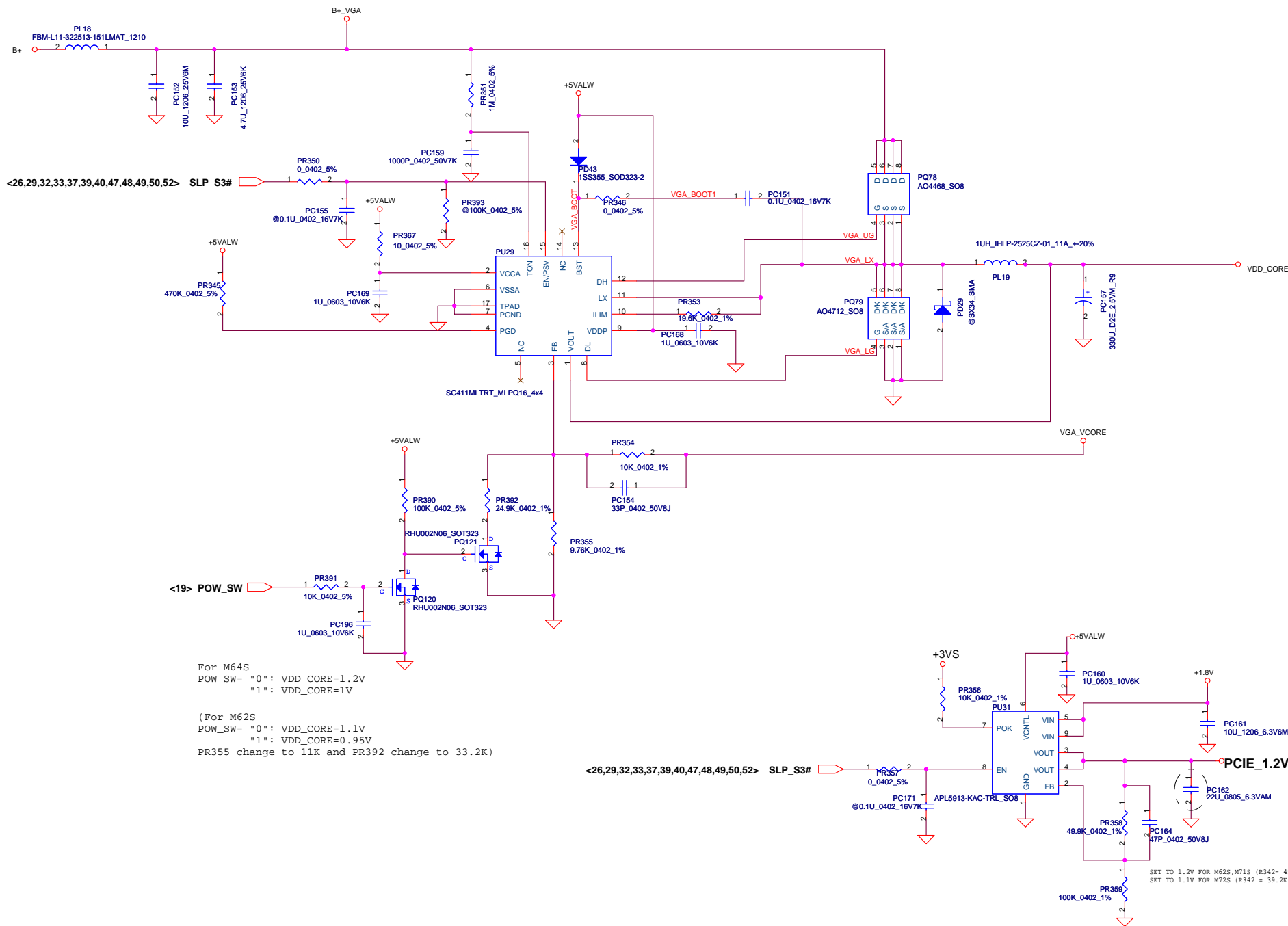
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title
				CPU_CORE
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Size	Document Number			Rev
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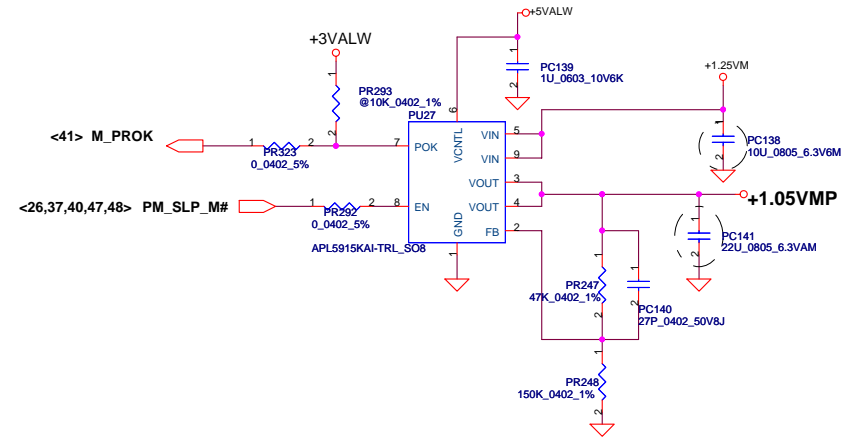
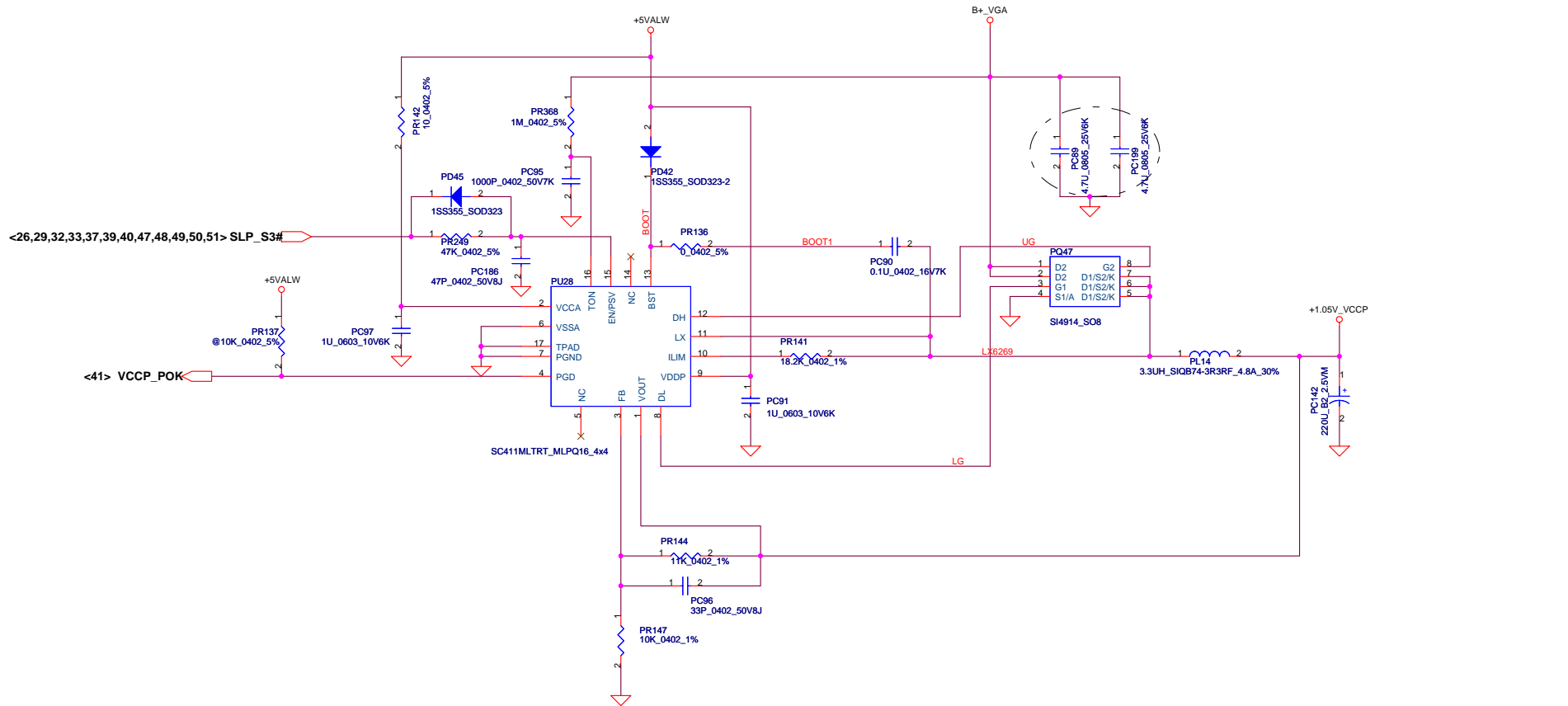
2005.8.20

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Compal Electronics, Inc.		
ADP OCP		
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	Compal Electronics, Inc. VDD CORE	
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Issued Date	2005/03/10	Deciphered Date	2006/03/10	+1.25VMP/+1.05V_VCCP	
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut In
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATI M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as luf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2
14	44	Charger	2007/3/1	PWR Francis H	Reserve circuit for testing Energy STAR	Reserve PR397, PR398, PR399 and PQ131 Add PR396 as 0 ohm.	PV
15	51	VDD_CORE /PCIE_VDD	2007/3/1	PWR Francis H	MOSFET change for M64s (original design is for M72)	Change PQ78 from IRF7413Z to AO4468 Change PQ79 from IRF8113 to AO4712 Change PR353 from 6.81K to 19.6K	PV
16	50	ADP_OCP	2007/4/12	HP R.L.	Fine tune system OCP setting for battery spec	Change PR210 from 422 to 215 Change PC129 from .22u to .027u Change PR203 from 604K to 200K Change PC131 from .027u to .01u	MV
17	44 46 47 48 51 52	Charger 3.3V/5V 1.5VS/1.25VM +1.25VMP/ 1.8V/0.9V VDD_CORE /PCIE_VDD +1.25VMP/ +1.05V_VCCP	2007/7/30	HP R.L.	Change some MLCCs size from 1206 to 0805	1. Change PC14 from 10u_1206 to 4.7u_0805 Add PC198 as 4.7u_0805 2. Change PC89 from 10u_1206 to 4.7u_0805 Add PC199 as 4.7u_0805 3. Change PC15, PC19, PC42 and PC58 from 4.7u_1206 to 4.7u_0805 4. Change PC79, PC141, PC162 and PC197 from 22u_1206 to 22u_0805 5. Change PC134, PC135 and PC138 from 10u_1206 to 10u_0805	MP
18	44	Charger	2007/7/30	TI	For TI's suggestion, add 4.7u at VCC pin	Add PC200 as 4.7u_0805	MP

<2006.09.11>

<2006.10.14>

<2006.11.20>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Design issue (Lost VRAM RST pin)	20, 22	Add DRAM_RST# from VGA to VRAM	0.2
2		Design issue (LVDS channel error)	19	Swapped LVDS upper and lower channel	0.2
3		Design issue (HSYNC & VSYNC error)	19	Swapped VSYNC & HSYNC each other	0.2
4		isolate ESD to CPU core via USB and 1394 conn's pin	34	Add R4, R73 and R56	0.2
5		Follow ATI design suggestion for VDDR4, VDDR5	21	change and reserve two jopens for +1.8VS and +3VS power rails	0.2
6		Follow ATI design suggestion for DPLL_VDDC	21	delete R1892	0.2
7		follow ATI power sequence	40	Add +1.25VS, +3VS, +5VS and VDD_MEM18 delay circuits.	0.2
1		RGB signal EA failed and CRT display garbage	16, 19	Change CRT circuit from MAX9511 to RLC circuit.	0.3
2		RGB signal EA failed and CRT display garbage	39	Change CRT circuit from MAX9511 to RLC circuit. Add Q/Switch circuit.	0.3
3		follow ATI power sequence	21	install R1898 and C1605, uninstall R1897	0.3
4		Increase VDD_MEM18 via holes	23	VDD_MEM18 no power noise, remove 1206 size resister.	0.3
5		Cancel Kill switch function on Chimay	28	uninstall JP53, R1906, R1736 and Q136	0.3
6		change 1394 bus route on board	31	re-define JP13 pins' assignment	0.3
7		implement one 4MB SPI chip	36	add R1794, R1795, R1924	0.3
8		implement 30pins KBC connector	38	re-define KBC connector JP6 pins assignment	0.3
1		HP request, support Penryn CPU	4	Add R23, R34	0.4
2		For Intel ES2 Crestline thermtrip pin.	7	Add R2	0.4
3		For EMI request enable 27MHz_SSC	15	install R1687	0.4
4		For Intel ES2 NB 800/667M Hz issue	15	Add CLRP4, CLRP5 to select FSB speed.	0.4
5		For RTC Accuracy fail to change	25	Change C528, C516 to 15pf	0.4
6		For detect CPU and system power saving	26	Add some components	0.4
7		Solve auto-turn on	26	install R1590 pull up to +3valw, uninstall R1727	0.4
8		Enable ACBS (power management for NIC)	29	install Q102, uninstall R1612, Q104, Q105	0.4
9		Enable ACBS (power management for NIC)	30	Change R1639 value to 1.87k	0.4

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
10		Add Energy Star for CPU schematics	41	reserve R1931, R1934, R1933, C1622, U88, U90, R43, R46, R52, R53, C1623, D80	0.4
11		Enable ACBS (power management for NIC)	41	Change R1732 pin2 from +3VM_Lan to +3VM	0.4
12		HP request	38	MDC power change to +3vs	0.4
13		Follow ATI power sequence	40	Install D77, C1617, change R1919 to 10K	0.4
1		For HP request	40	Add R1940 and pull up +3valw	0.5
2		For 3VL/VCC1_PWRGD glitch change	41	Add U5C and R1939 pull down	0.5
3		For KBC VCC2 connection to 3VS	37	install R1646, C75	0.5
4		For HP request	25	Add Q144 and R1935 instead of D75	0.5
5		For HP request to install BGA CRACK components	27 12		0.5
6		For solving Power wireset interfere Fan	38	change JP20 connector Footprint	0.5
7		For Intel Crestline thermtrip shutdown	7	Reserve 0.1uf *1 for THERMTRIP#	0.5
8		For possible Leak during ACBS on PREP# signal	26	Change pull up to +3valw	0.5
9		For HP request to change Line-in BOM	32	R370, R369 change to 6.04k, R374, R375 change to 2.00k	0.5
10		For SIM connector supply chain	31	SIM connector footprint change	0.5
11		For LMV331 supply chain, change to LMV393	41	change U76 & U86 to U91	0.5
12		For EMI changes for VGA CRT	16	Install C310,C313,C314,R542,R543,R544	0.5
13		For EMI changes for LED_LAN_DOCK	33	Add R1805,R1806	0.5
14		For HP request, change R1780.1 to UIM_PWR	31	change R1780.1 to UIM_PWR	0.5
15		For Intel NIC crystal design	29	Add R1936 30ohm value	0.5
16		For G-Sensor LED	26	HDD_HALTLED (R15) pull down	0.5
17		For Intel new design	26	Remove pull ups for STP_PCI# and STP_CPU# uninstall R1581, R1580	0.5
18		For HP request	36	Add CLRP6 for SPI ROM	0.5
19		For VGA wavy isse	17	Change C586 to 10uf_1206, add C1629 10uf_1206	0.5

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Add FP power supply circuit for Vista	41	reserve R1931, R1934, R1933, C1622, U88, U90, R43, R46, R52, R53, C1623, D80	0.4
2		Enable ACBS (power management for NIC)	41	Change R1732 pin2 from +3VM_Lan to +3VM	0.4
3		HP request	38	MDC power change to +3vs	0.4
4		Follow ATI power sequence	40	Install D77, C1617, change R1919 to 10K	0.4
5		For HP request	40	Add R1940 and pull up +3valw	0.5
6		For 3VL/VCC1_PWRGD glitch change	41	Add U5C and R1939 pull down	0.5
7		For KBC VCC2 connection to 3VS	37	install R1646, C75	0.5
8		For HP request	25	Add Q144 and R1935 instead of D75	0.5
		For HP request to install BGA CRACK components	27 12		0.5
		For solving Power wireset interfere Fan	38	change JP20 connector Footprint	0.5
		For Intel Crestline thermtrip shutdown	7	Reserve 0.1uf *1 for THERMTRIP#	0.5
		For possible Leak during ACBS on PREP# signal	26	Change pull up to +3valw	0.5
9		For HP request to change Line-in BOM	32	R370, R369 change to 6.04k, R374, R375 change to 2.00k	0.5
10		For SIM connector supply chain	31	SIM connector footprint change	0.5
11		For LMV331 supply chain, change to LMV393	41	change U76 & U86 to U91	0.5
12		For EMI changes for VGA CRT	16	Install C310,C313,C314,R542,R543,R544	0.5
13		For EMI changes for LED_LAN_DOCK	33	Add R1805,R1806	0.5
14		For HP request, change R1780.1 to UIM_PWR	31	change R1780.1 to UIM_PWR	0.5
15		For Intel NIC crystal design	29	Add R1936 30ohm value	0.5
16		For G-Sensor LED	26	HDD_HALTLED (R15) pull down	0.5
17		For Intel new design	26	Remove pull ups for STP_PCI# and STP_CPU# uninstall R1581, R1580	0.5
18		For HP request	36	Add CLRP6 for SPI ROM	0.5
19		For VGA wavy isse	17	Change C586 to 10uf_1206, add C1629 10uf_1206	0.5

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Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Solve VGA can not thermal shutdown and KB dissolve	4	Add R229 (non-install) and contact to THERM#_VGA	1A
2		prevent Cap crack to change Cap size	17	C1629 & C586 size change from 1206 to 0805	1A
3		Solve VGA can not thermal shutdown and KB dissolve	23	Add R1906 (non-install) and R1896 install Add Q30 & Q31	1A
4		Prevent GPIO33 leakage	25	Change Q144 to CHP202U_SC70	1A
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