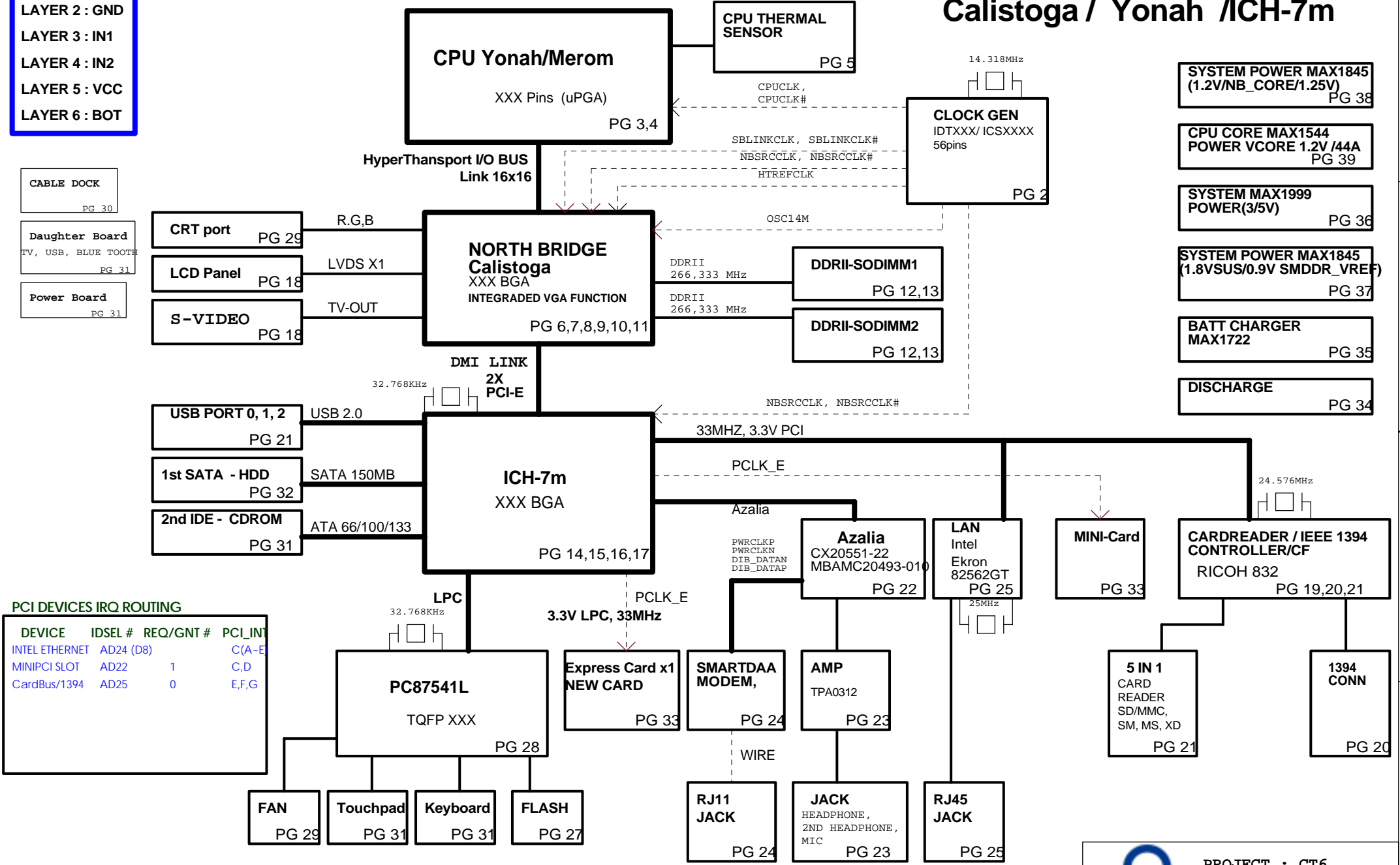


PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CT6 BLOCK DIAGRAM

Calistoga / Yonah /ICH-7m



PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
INTEL ETHERNET	AD24 (D8)		C(A-E)
MINIPCI SLOT	AD22	1	C,D
CardBus/1394	AD25	0	E,F,G

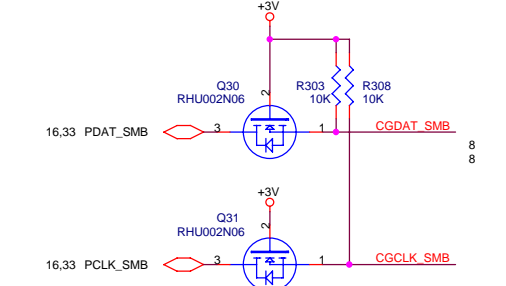
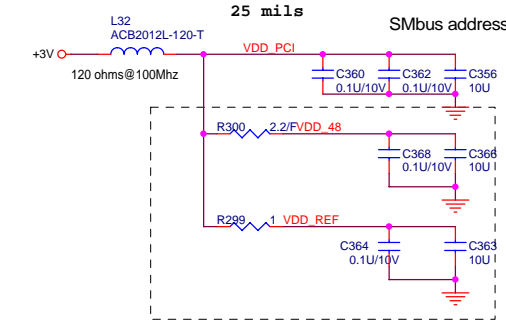
PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1B
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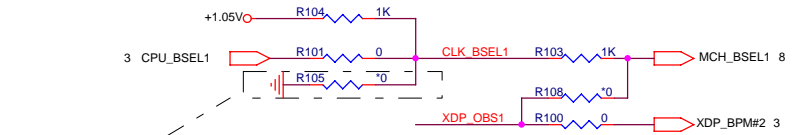
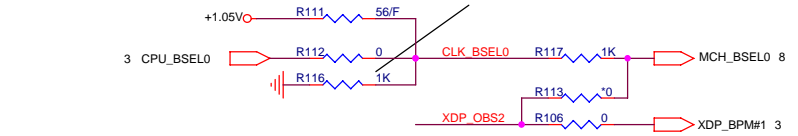
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

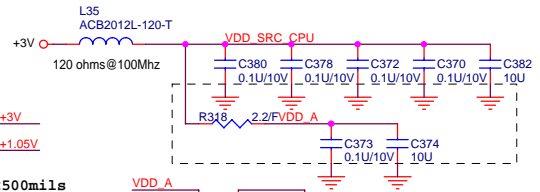
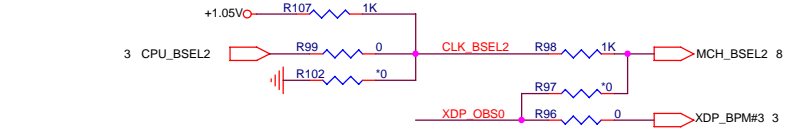
5,9,13,14,15,16,17,18,22,23,26,28,29,30,31,32,33,34,36,39,41,42 +3V
14,17,38,42 +1.05V



BSEL strappings need to be set for 533MHz Moby Dick (Intel?915GM - Calistoga Interposer) (if Calistoga is designed for 667MHz board).



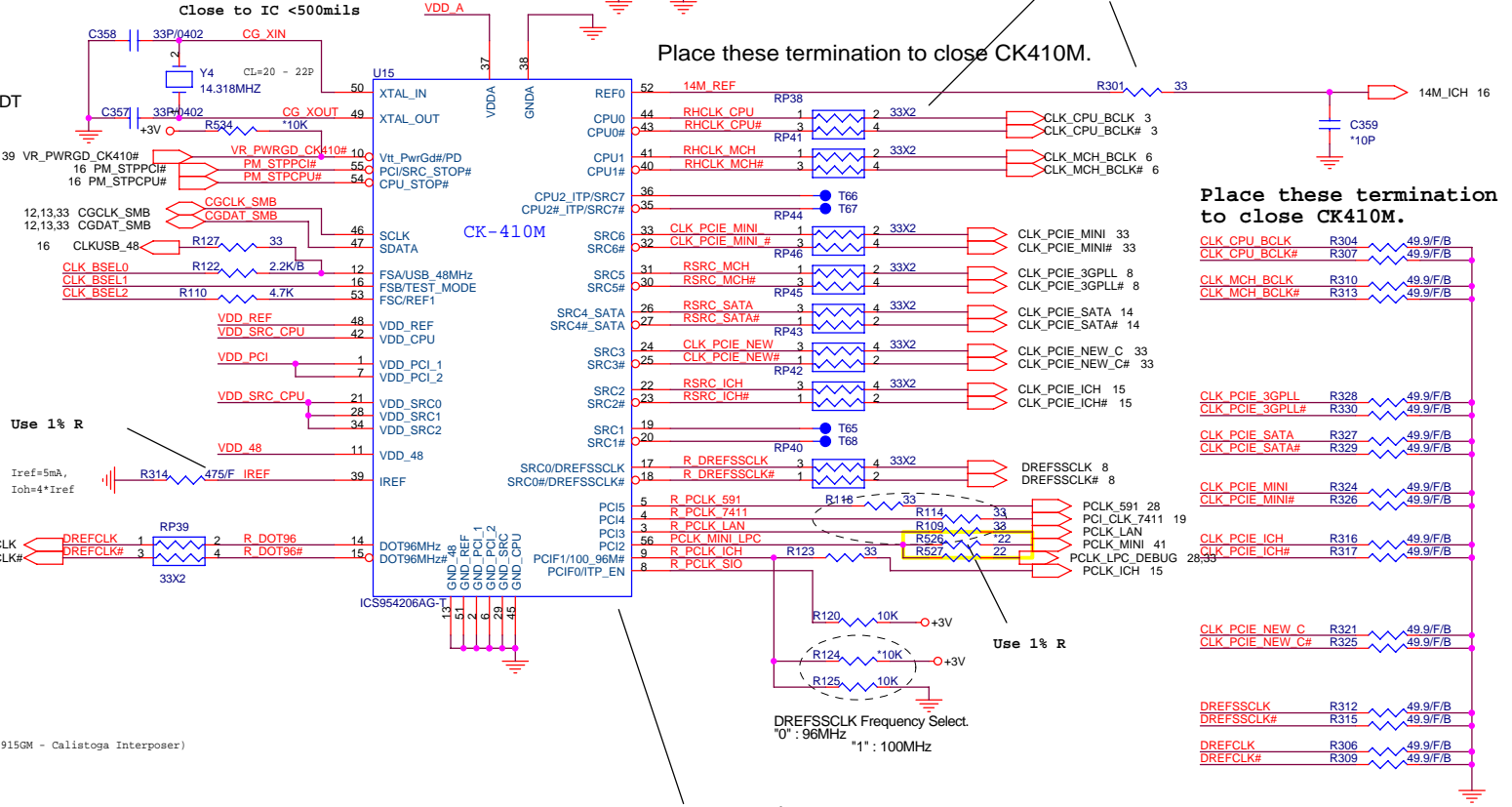
Stuff 0 ohm for 533MHz, NC for 667MHz

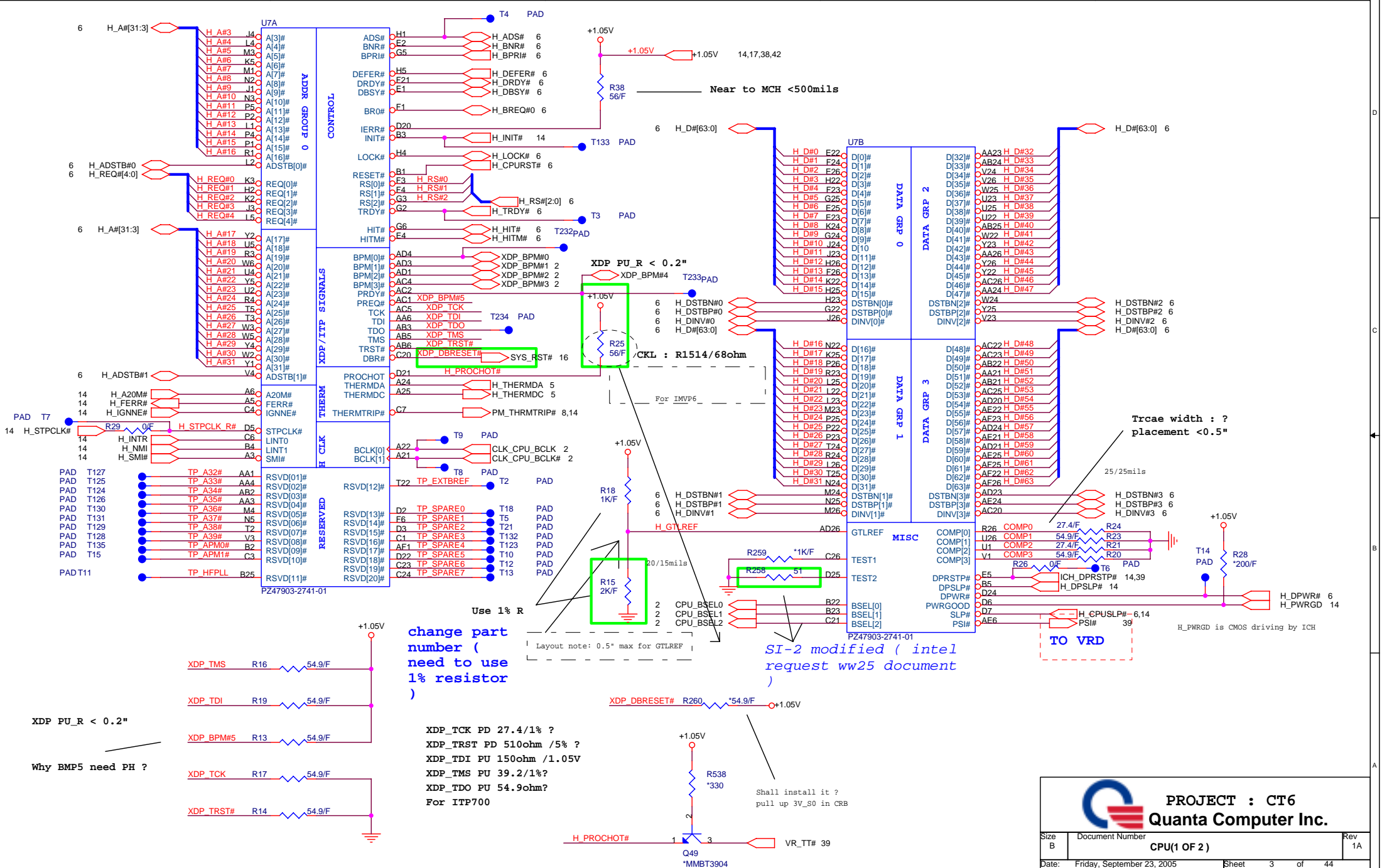


25 mils

Use 33R/1%

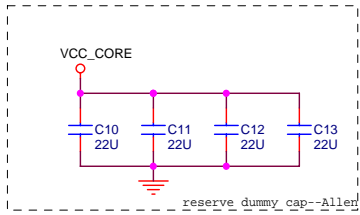
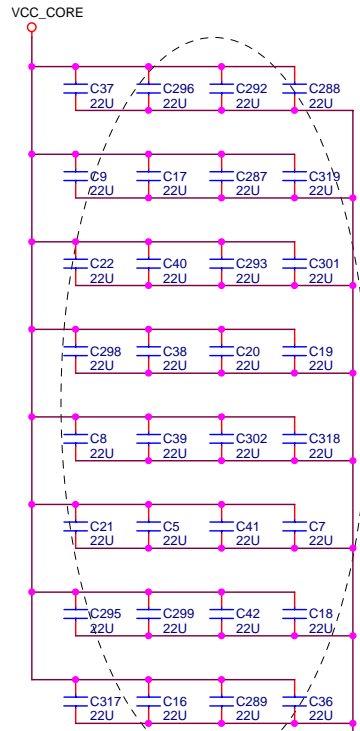
Place these termination to close CK410M.



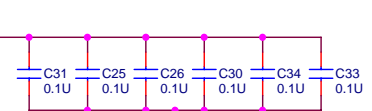
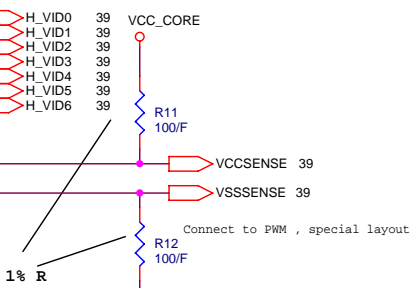
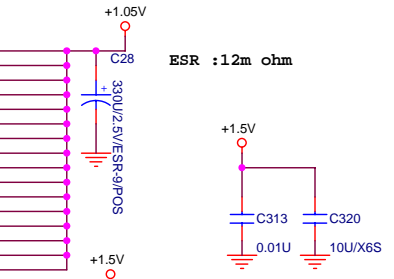
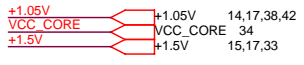


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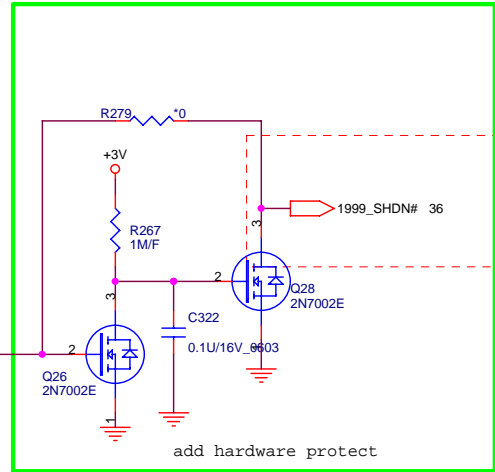
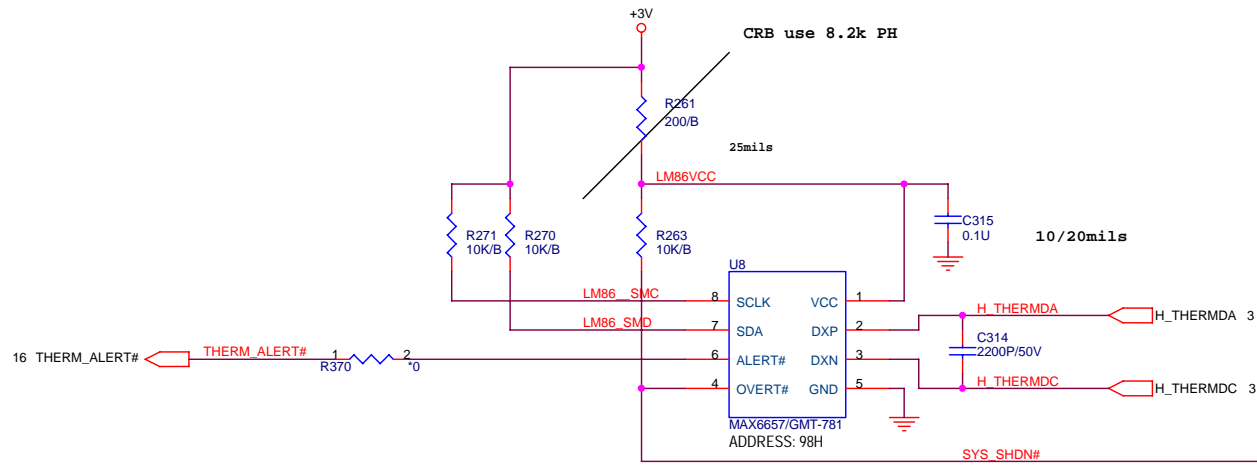
U7C		U7D	
A7	VCC[001]	VCC[68]	AB20
A9	VCC[002]	VCC[69]	AB7
A10	VCC[003]	VCC[70]	AC7
A12	VCC[004]	VCC[71]	AC9
A13	VCC[005]	VCC[72]	AC12
A15	VCC[006]	VCC[73]	AC13
A17	VCC[007]	VCC[74]	AC15
A18	VCC[008]	VCC[75]	AC17
A20	VCC[009]	VCC[76]	AC18
B7	VCC[010]	VCC[77]	AD7
B9	VCC[011]	VCC[78]	AD9
B10	VCC[012]	VCC[79]	AD10
B12	VCC[013]	VCC[80]	AD12
B14	VCC[014]	VCC[81]	AD14
B15	VCC[015]	VCC[82]	AD15
B17	VCC[016]	VCC[83]	AD17
B18	VCC[017]	VCC[84]	AD18
B20	VCC[018]	VCC[85]	AE9
C9	VCC[019]	VCC[86]	AE10
C10	VCC[020]	VCC[87]	AE12
C12	VCC[021]	VCC[88]	AE13
C13	VCC[022]	VCC[89]	AE15
C15	VCC[023]	VCC[90]	AE17
C17	VCC[024]	VCC[91]	AE18
C18	VCC[025]	VCC[92]	AE20
D9	VCC[026]	VCC[93]	AE10
D10	VCC[027]	VCC[94]	AE12
D12	VCC[028]	VCC[95]	AE14
D14	VCC[029]	VCC[96]	AE15
D15	VCC[030]	VCC[97]	AE17
D17	VCC[031]	VCC[98]	AE18
D18	VCC[032]	VCC[99]	AE20
E7	VCC[033]	VCC[100]	
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	V6
E12	VCC[036]	VCCP[02]	G21
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	N6
F12	VCC[045]	VCCP[11]	R21
F14	VCC[046]	VCCP[12]	R6
F15	VCC[047]	VCCP[13]	T21
F17	VCC[048]	VCCP[14]	T6
F18	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA	B26
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]		
AA15	VCC[056]	VID[0]	AD6
AA17	VCC[057]	VID[1]	AE5
AA18	VCC[058]	VID[2]	AE5
AA20	VCC[059]	VID[3]	AE4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AE2
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]	VCCSENSE	AE7
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AE7



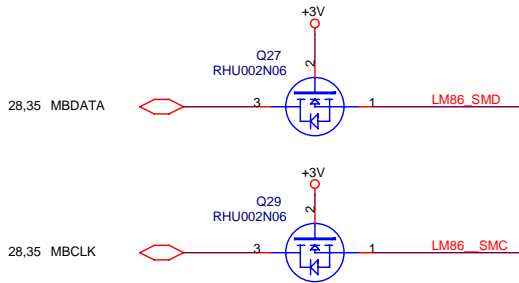
U7D		P6	
A4	VSS[001]	VSS[082]	P21
A8	VSS[002]	VSS[083]	P24
A11	VSS[003]	VSS[084]	R2
A14	VSS[004]	VSS[085]	R6
A16	VSS[005]	VSS[086]	R22
A19	VSS[006]	VSS[087]	R25
A23	VSS[007]	VSS[088]	T1
A26	VSS[008]	VSS[089]	T4
B6	VSS[009]	VSS[090]	T23
B8	VSS[010]	VSS[091]	T26
B11	VSS[011]	VSS[092]	U3
B13	VSS[012]	VSS[093]	U6
B16	VSS[013]	VSS[094]	U21
B19	VSS[014]	VSS[095]	U24
B21	VSS[015]	VSS[096]	V2
B24	VSS[016]	VSS[097]	V6
C5	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W4
C16	VSS[021]	VSS[102]	W23
C19	VSS[022]	VSS[103]	W26
C2	VSS[023]	VSS[104]	Y3
C22	VSS[024]	VSS[105]	Y6
C25	VSS[025]	VSS[106]	Y21
D1	VSS[026]	VSS[107]	Y24
D4	VSS[027]	VSS[108]	AA2
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D13	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
F11	VSS[037]	VSS[118]	AB4
F14	VSS[038]	VSS[119]	AB8
F16	VSS[039]	VSS[120]	AB11
F19	VSS[040]	VSS[121]	AB13
F21	VSS[041]	VSS[122]	AB16
F24	VSS[042]	VSS[123]	AB19
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC8
F19	VSS[048]	VSS[129]	AC11
F2	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G4	VSS[052]	VSS[133]	AC21
G1	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD8
H6	VSS[057]	VSS[138]	AD11
H21	VSS[058]	VSS[139]	AD13
H24	VSS[059]	VSS[140]	AD16
J2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE19
L21	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	AE3
M5	VSS[073]	VSS[154]	AE6
M22	VSS[074]	VSS[155]	AE8
M25	VSS[075]	VSS[156]	AE11
N1	VSS[076]	VSS[157]	AE13
N4	VSS[077]	VSS[158]	AE16
N23	VSS[078]	VSS[159]	AE19
N26	VSS[079]	VSS[160]	AE21
P3	VSS[080]	VSS[161]	AE24
	VSS[081]	VSS[162]	

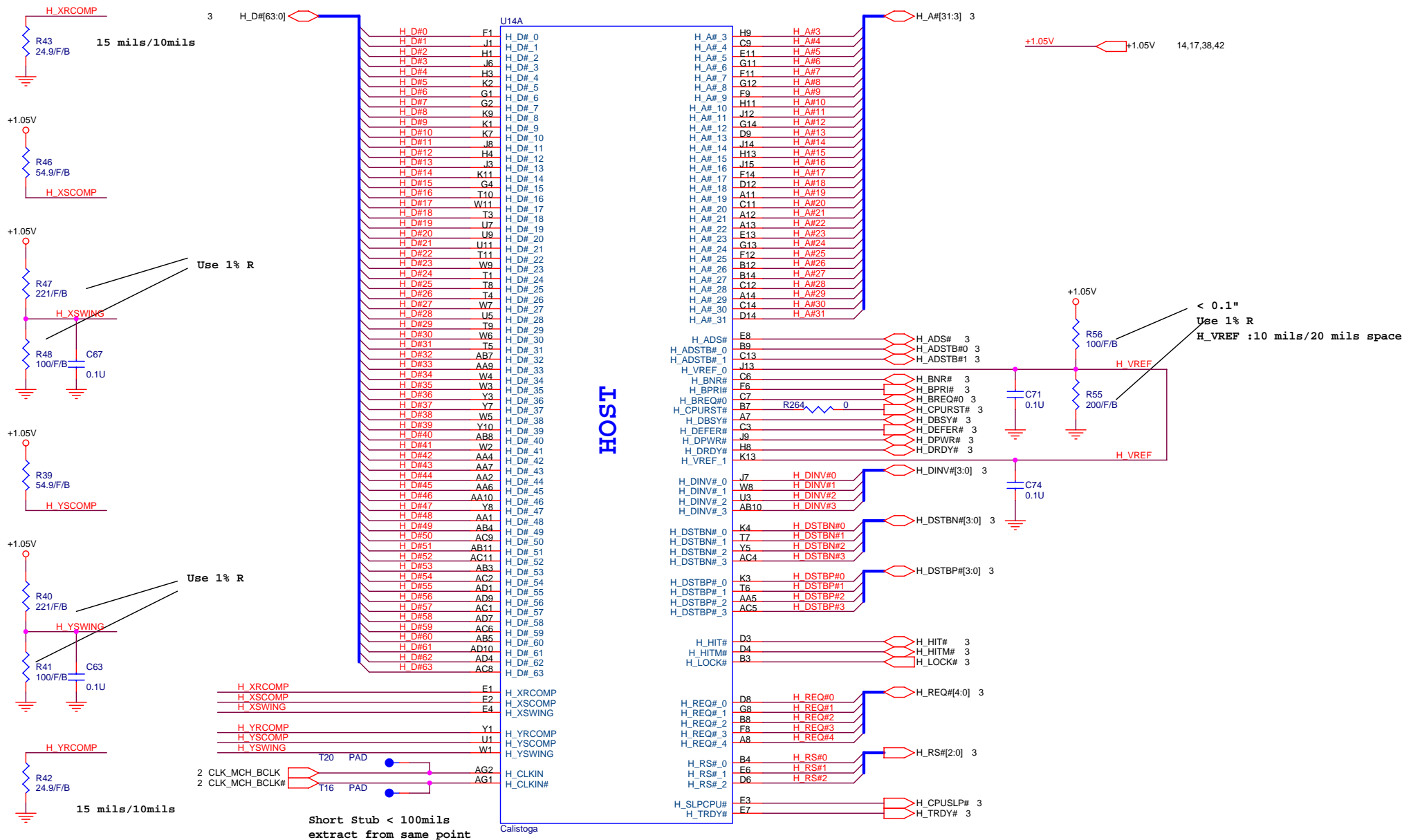
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Uninstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506
 B0 stepping CPU can fix this issue ..





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13 M_A_DQ[63:0]

M_A DQ0	AJ35	SA_DQ0
M_A DQ1	AJ34	SA_DQ1
M_A DQ2	AM31	SA_DQ2
M_A DQ3	AM33	SA_DQ3
M_A DQ4	AJ36	SA_DQ4
M_A DQ5	AK35	SA_DQ5
M_A DQ6	AJ32	SA_DQ6
M_A DQ7	AH31	SA_DQ7
M_A DQ8	AN35	SA_DQ8
M_A DQ9	AP33	SA_DQ9
M_A DQ10	AR31	SA_DQ10
M_A DQ11	AP31	SA_DQ11
M_A DQ12	AN38	SA_DQ12
M_A DQ13	AM36	SA_DQ13
M_A DQ14	AM34	SA_DQ14
M_A DQ15	AN33	SA_DQ15
M_A DQ16	AK26	SA_DQ16
M_A DQ17	AL27	SA_DQ17
M_A DQ18	AM26	SA_DQ18
M_A DQ19	AN24	SA_DQ19
M_A DQ20	AK28	SA_DQ20
M_A DQ21	AL28	SA_DQ21
M_A DQ22	AM24	SA_DQ22
M_A DQ23	AP26	SA_DQ23
M_A DQ24	AP23	SA_DQ24
M_A DQ25	AL22	SA_DQ25
M_A DQ26	AP21	SA_DQ26
M_A DQ27	AN20	SA_DQ27
M_A DQ28	AL23	SA_DQ28
M_A DQ29	AP24	SA_DQ29
M_A DQ30	AP20	SA_DQ30
M_A DQ31	AT21	SA_DQ31
M_A DQ32	AR12	SA_DQ32
M_A DQ33	AR14	SA_DQ33
M_A DQ34	AP13	SA_DQ34
M_A DQ35	AP12	SA_DQ35
M_A DQ36	AT13	SA_DQ36
M_A DQ37	AT12	SA_DQ37
M_A DQ38	AL14	SA_DQ38
M_A DQ39	AL12	SA_DQ39
M_A DQ40	AK9	SA_DQ40
M_A DQ41	AN7	SA_DQ41
M_A DQ42	AK8	SA_DQ42
M_A DQ43	AK7	SA_DQ43
M_A DQ44	AP9	SA_DQ44
M_A DQ45	AN9	SA_DQ45
M_A DQ46	AT5	SA_DQ46
M_A DQ47	AL5	SA_DQ47
M_A DQ48	AY2	SA_DQ48
M_A DQ49	AW2	SA_DQ49
M_A DQ50	AP1	SA_DQ50
M_A DQ51	AN2	SA_DQ51
M_A DQ52	AV2	SA_DQ52
M_A DQ53	AT3	SA_DQ53
M_A DQ54	AN1	SA_DQ54
M_A DQ55	AL2	SA_DQ55
M_A DQ56	AG7	SA_DQ56
M_A DQ57	AE9	SA_DQ57
M_A DQ58	AG4	SA_DQ58
M_A DQ59	AF6	SA_DQ59
M_A DQ60	AG9	SA_DQ60
M_A DQ61	AH6	SA_DQ61
M_A DQ62	AF4	SA_DQ62
M_A DQ63	AF8	SA_DQ63

U14D

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M_A_BS#0	M_A_BS#0 12,13
SA_BS_1	AV14	M_A_BS#1	M_A_BS#1 12,13
SA_BS_2	BA20	M_A_BS#2	M_A_BS#2 12,13
SA_CAS#	AY13	M_A_CAS#	M_A_CAS# 12,13
SA_DM_0	AJ33	M_A_DM0	M_A_DM[7:0] 13
SA_DM_1	AM35	M_A_DM1	
SA_DM_2	AL26	M_A_DM2	
SA_DM_3	AN22	M_A_DM3	
SA_DM_4	AM14	M_A_DM4	
SA_DM_5	AL9	M_A_DM5	
SA_DM_6	AR3	M_A_DM6	
SA_DM_7	AH4	M_A_DM7	
SA_DQS_0	AK33	M_A_DQS0	M_A_DQS[7:0] 13
SA_DQS_1	AT33	M_A_DQS1	
SA_DQS_2	AN28	M_A_DQS2	
SA_DQS_3	AM22	M_A_DQS3	
SA_DQS_4	AN8	M_A_DQS4	
SA_DQS_5	AP3	M_A_DQS5	
SA_DQS_6	AG5	M_A_DQS6	
SA_DQS_7	AK2	M_A_DQS7	
SA_DQS#_0	AU33	M_A_DQS#0	M_A_DQS#[7:0] 13
SA_DQS#_1	AN27	M_A_DQS#1	
SA_DQS#_2	AM21	M_A_DQS#2	
SA_DQS#_3	AM12	M_A_DQS#3	
SA_DQS#_4	AL8	M_A_DQS#4	
SA_DQS#_5	AN3	M_A_DQS#5	
SA_DQS#_6	AH5	M_A_DQS#6	
SA_DQS#_7			
SA_MA_0	AY16	M_A_A0	M_A_A[13:0] 12,13
SA_MA_1	AU14	M_A_A1	
SA_MA_2	AW16	M_A_A2	
SA_MA_3	BA16	M_A_A3	
SA_MA_4	BA17	M_A_A4	
SA_MA_5	AU16	M_A_A5	
SA_MA_6	AV17	M_A_A6	
SA_MA_7	AU17	M_A_A7	
SA_MA_8	AW17	M_A_A8	
SA_MA_9	AT16	M_A_A9	
SA_MA_10	AU13	M_A_A10	
SA_MA_11	AT17	M_A_A11	
SA_MA_12	AV20	M_A_A12	
SA_MA_13	AV12	M_A_A13	
SA_RAS#	AW14		M_A_RAS# 12,13
SA_RCVENIN#	AK23	TP_MA_RCVENIN#	T33 PAD
SA_RCVENOUT#	AK24	TP_MA_RCVENOUT#	T38 PAD
SA_WE#	AY14		M_A_WE# 12,13

Calistoga

13 M_B_DQ[63:0]

M_B DQ0	AK39	SB_DQ0
M_B DQ1	AJ37	SB_DQ1
M_B DQ2	AP39	SB_DQ2
M_B DQ3	AR41	SB_DQ3
M_B DQ4	AJ38	SB_DQ4
M_B DQ5	AK38	SB_DQ5
M_B DQ6	AN41	SB_DQ6
M_B DQ7	AP41	SB_DQ7
M_B DQ8	AT40	SB_DQ8
M_B DQ9	AV41	SB_DQ9
M_B DQ10	AU38	SB_DQ10
M_B DQ11	AV38	SB_DQ11
M_B DQ12	AP38	SB_DQ12
M_B DQ13	AR40	SB_DQ13
M_B DQ14	AW38	SB_DQ14
M_B DQ15	AV38	SB_DQ15
M_B DQ16	BA38	SB_DQ16
M_B DQ17	AV36	SB_DQ17
M_B DQ18	AR36	SB_DQ18
M_B DQ19	AP36	SB_DQ19
M_B DQ20	BA36	SB_DQ20
M_B DQ21	AU36	SB_DQ21
M_B DQ22	AP35	SB_DQ22
M_B DQ23	AP34	SB_DQ23
M_B DQ24	AV33	SB_DQ24
M_B DQ25	BA33	SB_DQ25
M_B DQ26	AT31	SB_DQ26
M_B DQ27	AU29	SB_DQ27
M_B DQ28	AU31	SB_DQ28
M_B DQ29	AW31	SB_DQ29
M_B DQ30	AV29	SB_DQ30
M_B DQ31	AW29	SB_DQ31
M_B DQ32	AM19	SB_DQ32
M_B DQ33	AL19	SB_DQ33
M_B DQ34	AP14	SB_DQ34
M_B DQ35	AN14	SB_DQ35
M_B DQ36	AM17	SB_DQ36
M_B DQ37	AM16	SB_DQ37
M_B DQ38	AP15	SB_DQ38
M_B DQ39	AL15	SB_DQ39
M_B DQ40	AJ11	SB_DQ40
M_B DQ41	AH10	SB_DQ41
M_B DQ42	AJ9	SB_DQ42
M_B DQ43	AN10	SB_DQ43
M_B DQ44	AK13	SB_DQ44
M_B DQ45	AK10	SB_DQ45
M_B DQ46	AK10	SB_DQ46
M_B DQ47	AJ8	SB_DQ47
M_B DQ48	BA10	SB_DQ48
M_B DQ49	AW10	SB_DQ49
M_B DQ50	BA4	SB_DQ50
M_B DQ51	AW4	SB_DQ51
M_B DQ52	AY10	SB_DQ52
M_B DQ53	AY9	SB_DQ53
M_B DQ54	AW5	SB_DQ54
M_B DQ55	AY5	SB_DQ55
M_B DQ56	AV4	SB_DQ56
M_B DQ57	AR5	SB_DQ57
M_B DQ58	AK4	SB_DQ58
M_B DQ59	AK3	SB_DQ59
M_B DQ60	AT4	SB_DQ60
M_B DQ61	AK5	SB_DQ61
M_B DQ62	AJ5	SB_DQ62
M_B DQ63	AJ3	SB_DQ63

U14E

DDR SYSTEM MEMORY B

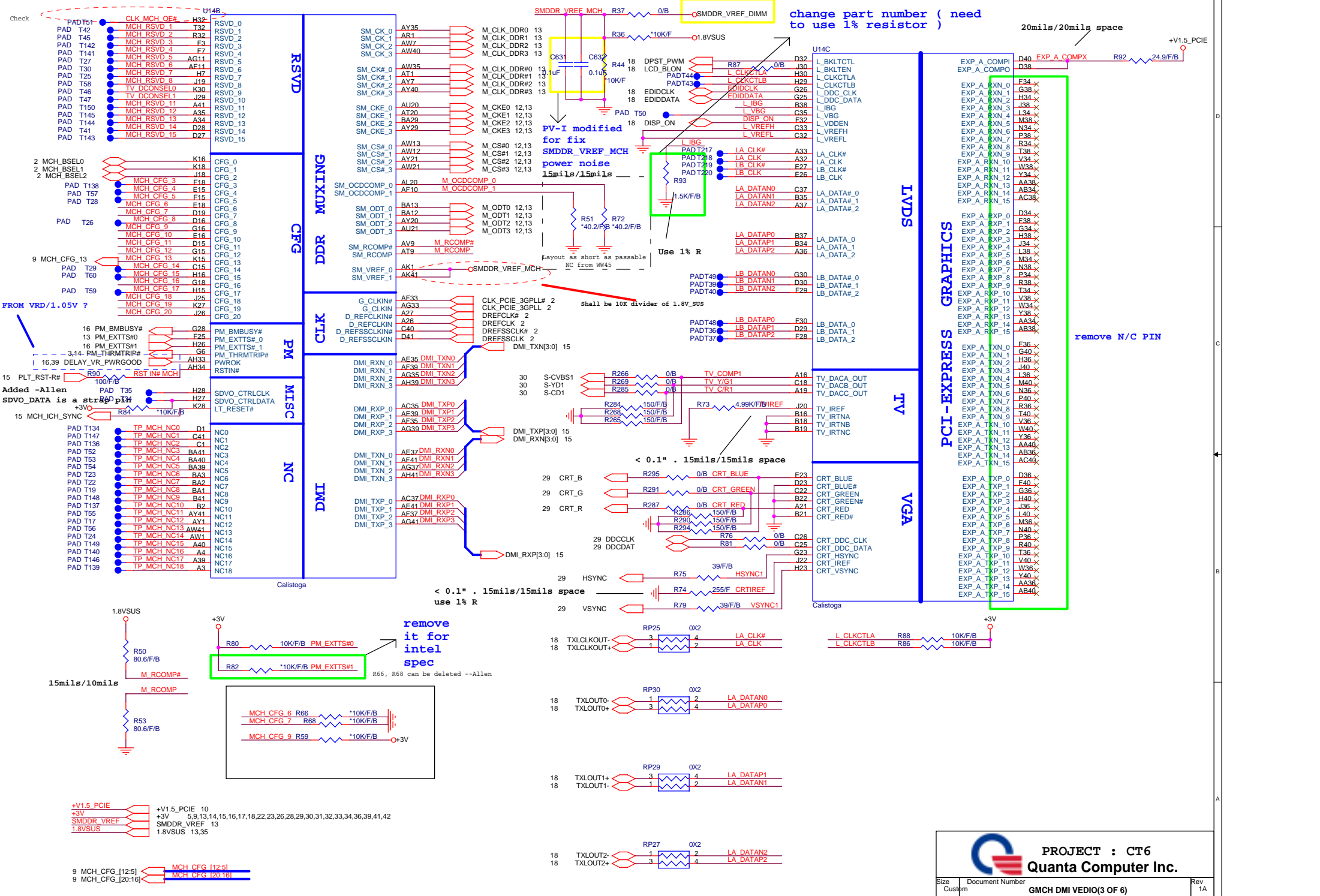
Calistoga

SB_BS_0	AT24	M_B_BS#0	12,13
SB_BS_1	AV23	M_B_BS#1	12,13
SB_BS_2	AY28	M_B_BS#2	12,13
SB_CAS#	AR24	M_B_CAS#	12,13
SB_DM_0	AK36	M_B_DM0	
SB_DM_1	AR38	M_B_DM1	
SB_DM_2	AT36	M_B_DM2	
SB_DM_3	BA31	M_B_DM3	
SB_DM_4	AL17	M_B_DM4	
SB_DM_5	AH8	M_B_DM5	
SB_DM_6	BA5	M_B_DM6	
SB_DM_7	AN4	M_B_DM7	
SB_DQS_0	AM39	M_B_DQS0	M_B_DQS[7:0] 13
SB_DQS_1	AT39	M_B_DQS1	
SB_DQS_2	AU35	M_B_DQS2	
SB_DQS_3	AR29	M_B_DQS3	
SB_DQS_4	AR16	M_B_DQS4	
SB_DQS_5	AR10	M_B_DQS5	
SB_DQS_6	AR7	M_B_DQS6	
SB_DQS_7	AN5	M_B_DQS7	
SB_DQS#_0	AM40	M_B_DQS#0	M_B_DQS#[7:0] 13
SB_DQS#_1	AU39	M_B_DQS#1	
SB_DQS#_2	AT35	M_B_DQS#2	
SB_DQS#_3	AP29	M_B_DQS#3	
SB_DQS#_4	AP16	M_B_DQS#4	
SB_DQS#_5	AT10	M_B_DQS#5	
SB_DQS#_6	AT7	M_B_DQS#6	
SB_DQS#_7	AP5	M_B_DQS#7	
SB_MA_0	AY23	M_B_A0	M_B_A[13:0] 12,13
SB_MA_1	AW24	M_B_A1	
SB_MA_2	AY24	M_B_A2	
SB_MA_3	AR28	M_B_A3	
SB_MA_4	AT27	M_B_A4	
SB_MA_5	AT28	M_B_A5	
SB_MA_6	AU27	M_B_A6	
SB_MA_7	AV28	M_B_A7	
SB_MA_8	AV27	M_B_A8	
SB_MA_9	AW27	M_B_A9	
SB_MA_10	AV24	M_B_A10	
SB_MA_11	BA27	M_B_A11	
SB_MA_12	AY27	M_B_A12	
SB_MA_13	AR23	M_B_A13	
SB_RAS#	AU23		M_B_RAS# 12,13
SB_RCVENIN#	AK16	TP_MB_RCVENIN#	T31 PAD
SB_RCVENOUT#	AK18	TP_MB_RCVENOUT#	T32 PAD
SB_WE#	AR27		M_B_WE# 12,13



PROJECT : CT6
Quanta Computer Inc.

Size B	Document Number	Rev 1A
GMCH DDR(2 OF 6)		
Date:	Friday, September 23, 2005	Sheet 7 of 44



change part number (need to use 1% resistor)

20mils/20mils space

+V1.5_PCIE

PV-I modified for fix SMDRR_VREF_MCH power noise 15mils/15mils

Layout as short as possible

Use 1% R

shall be 10K divider of 1.8V_sus

< 0.1" . 15mils/15mils space

< 0.1" . 15mils/15mils space

remove for intel spec

R66, R68 can be deleted --Allen

FROM VRD/1.05V ?

Added -Allen SDVO_DATA is a strap pin

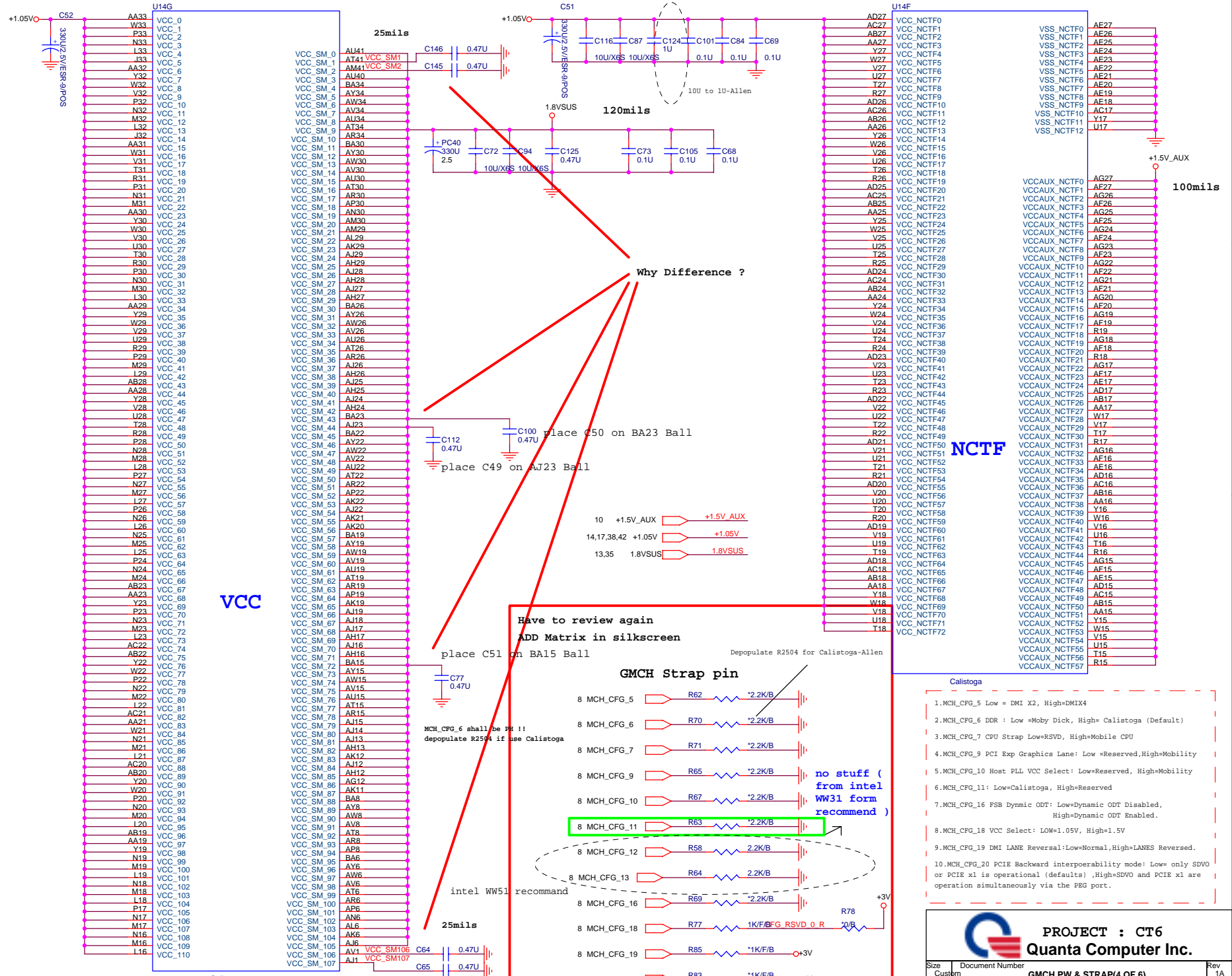
remove N/C PIN

- +V1.5_PCIE 10
- +3V 5,9,13,14,15,16,17,18,22,23,26,28,29,30,31,32,33,34,36,39,41,42
- SMDRR_VREF 13
- 1.8VSUS 13,35

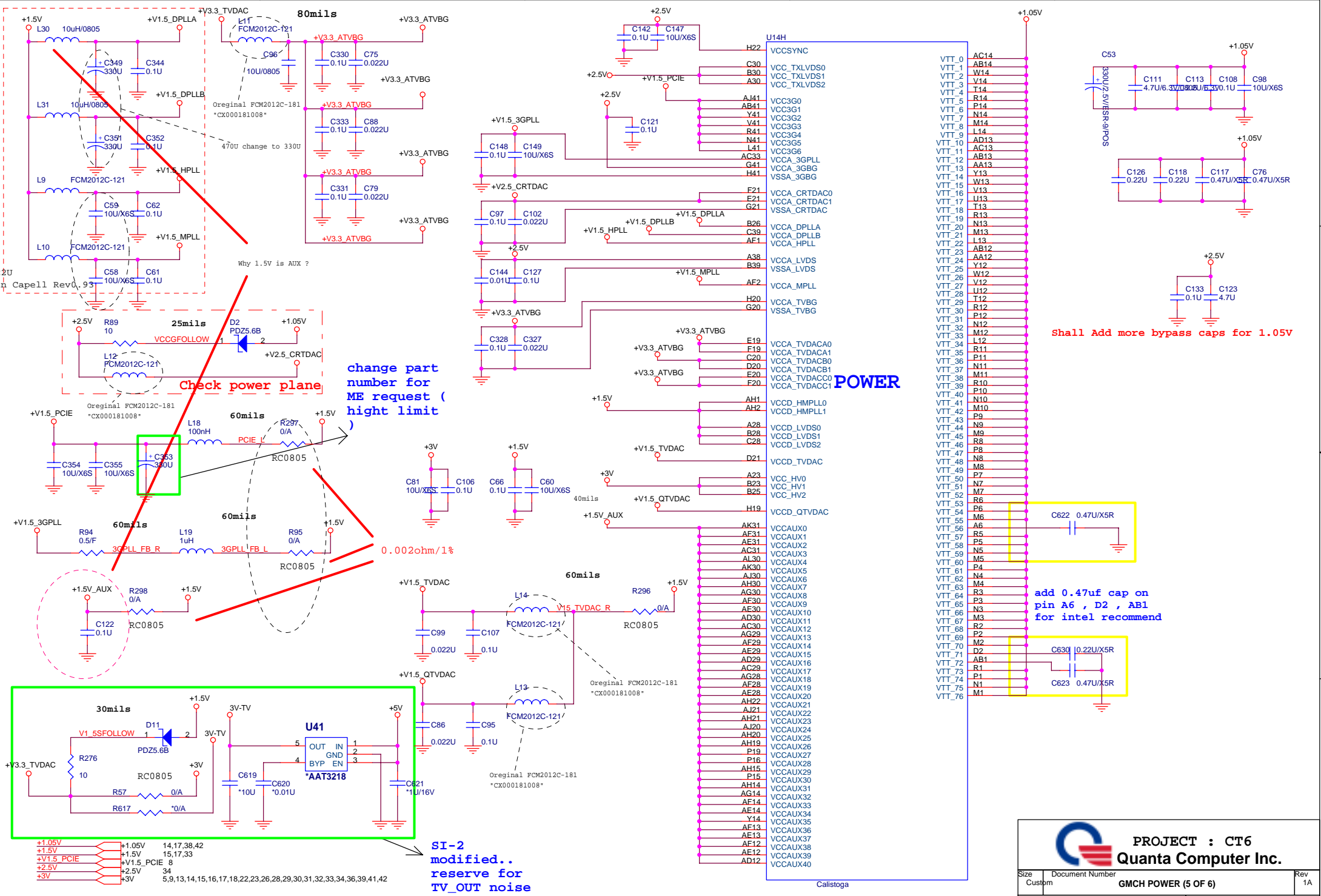
- MCH_CFG [12:5]
- MCH_CFG [20:16]

PROJECT : CT6
Quanta Computer Inc.

Size Custom	Document Number GMCH DMI VEDIO(3 OF 6)	Rev 1A
Date: Friday, September 23, 2005	Sheet 8 of 44	



- Calistoga**
- 1.MCH_CFG_5 Low = DMI X2, High=DMI X4
 - 2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
 - 3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
 - 4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
 - 5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
 - 6.MCH_CFG_11: Low=Calistoga, High=Reserved
 - 7.MCH_CFG_16 FSB Dymic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
 - 8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
 - 9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
 - 10.MCH_CFG_20 PCIe Backward interoperability mode: Low= only SDVO or PCIe x1 is operational (default),High=SDVO and PCIe x1 are operation simultaneously via the PEG port.



Why 1.5V is AUX ?

Check power plane

change part number for ME request (high limit)

0.002ohm/1%


Shall Add more bypass caps for 1.05V

add 0.47uf cap on pin A6, D2, AB1 for intel recommend

SI-2 modified.. reserve for TV_OUT noise

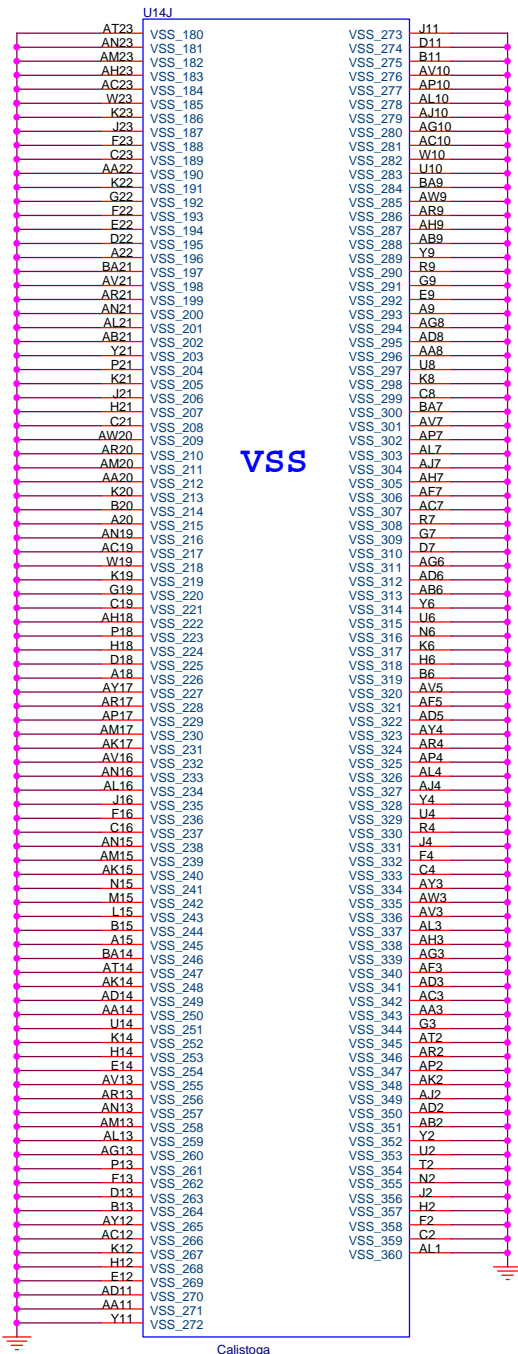
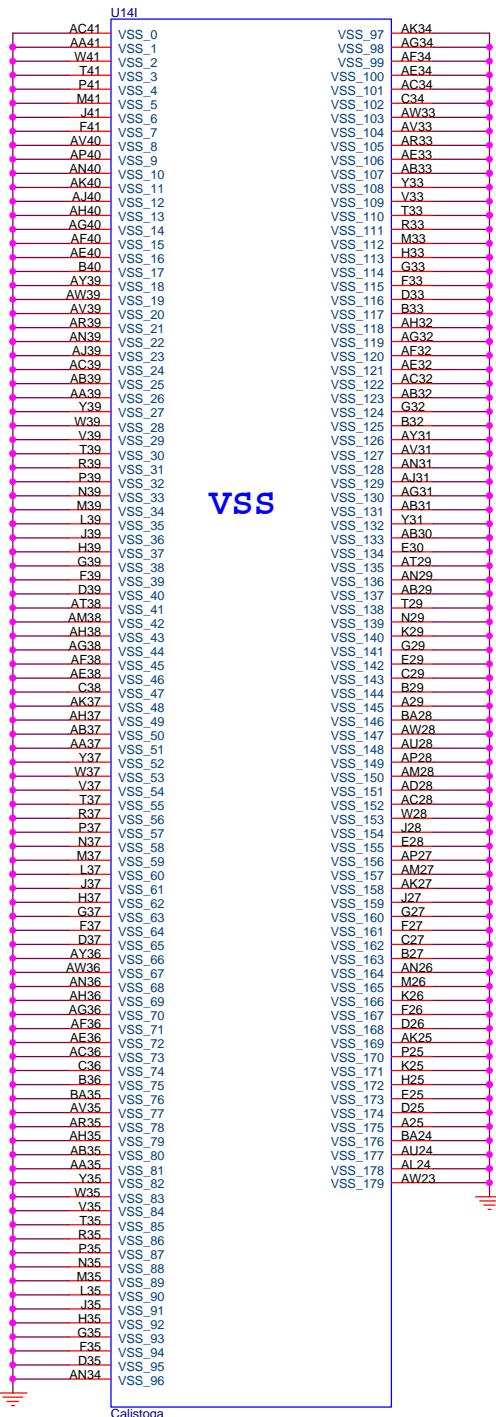

POWER

+1.05V	+1.05V	14,17,38,42
+1.5V	+1.5V	15,17,33
+V1.5_PCIE	+V1.5_PCIE	8
+2.5V	+2.5V	34
+3V	+3V	5,9,13,14,15,16,17,18,22,23,26,28,29,30,31,32,33,34,36,39,41,42



PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	GMCH POWER (5 OF 6)	1A
Date:	Friday, September 23, 2005	Sheet 10 of 44

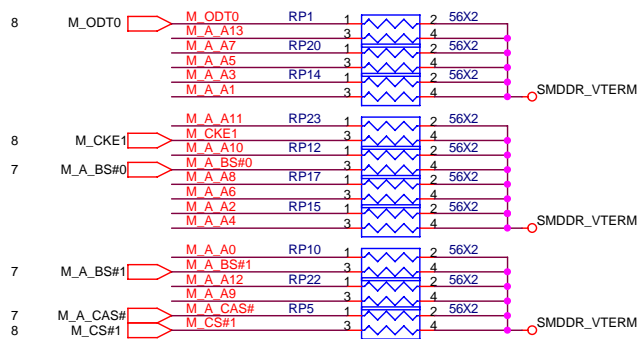
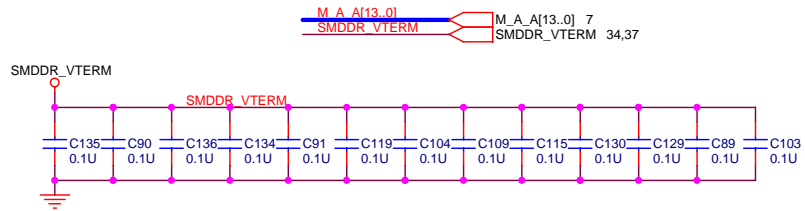



PROJECT : CT6
Quanta Computer Inc.

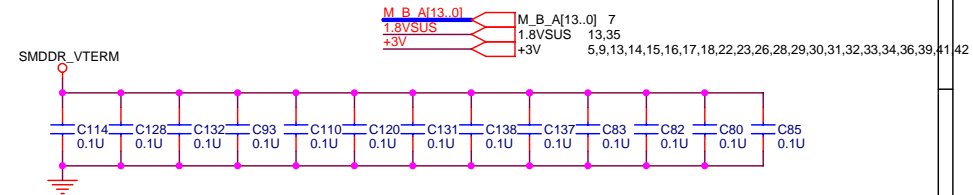
Size	Document Number	Rev
Custom	GMCH GND(6 OF 6)	1A
Date:	Friday, September 23, 2005	Sheet 11 of 44

DDRII DUAL CHANNEL A,B.

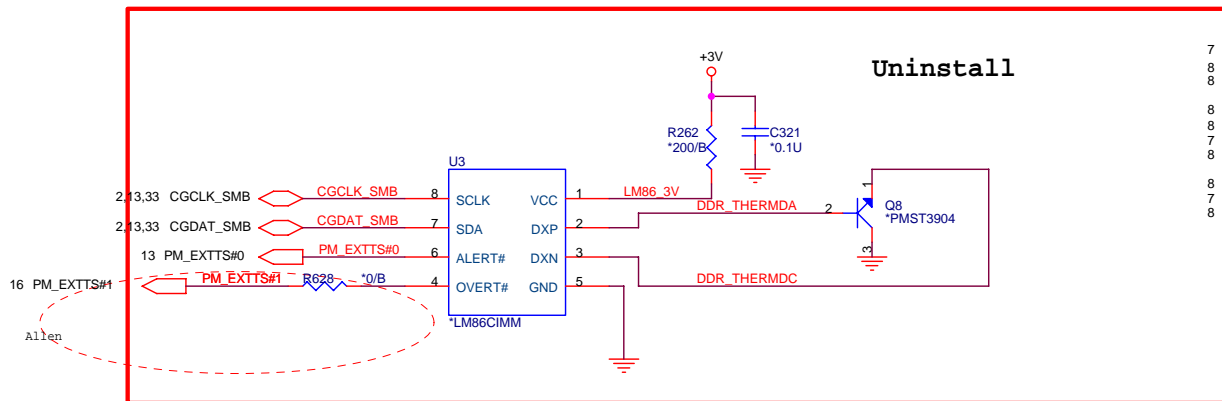
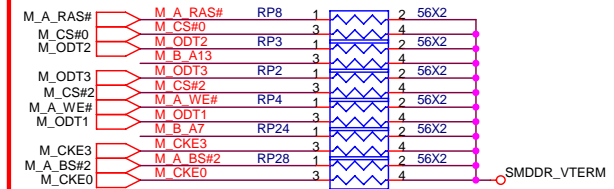
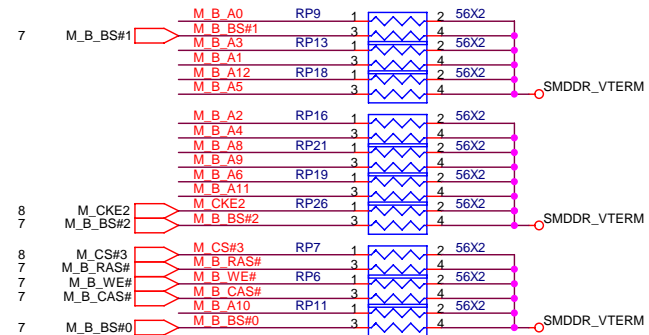
DDRII A CHANNEL



DDRII B CHANNEL



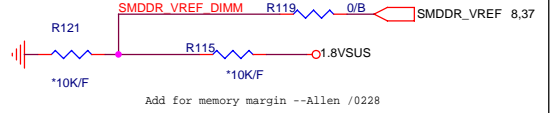
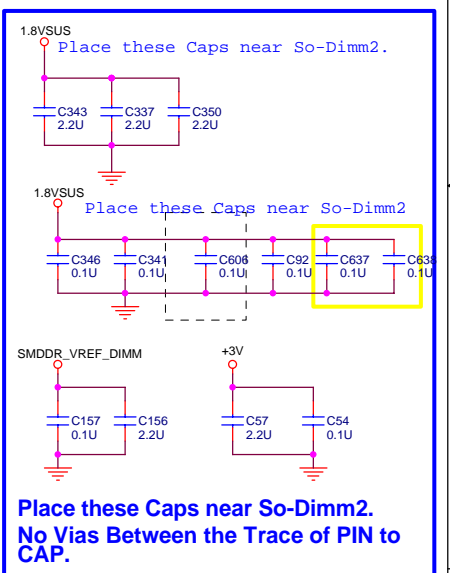
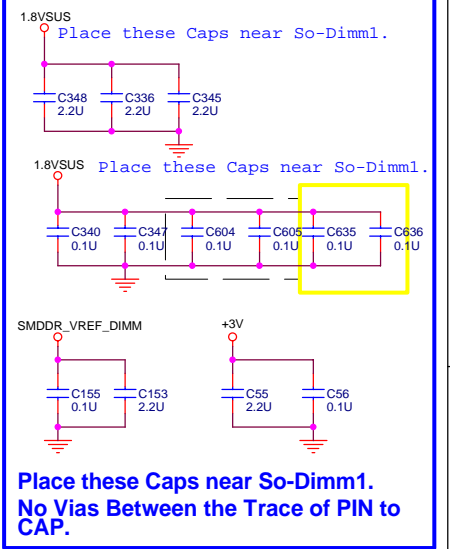
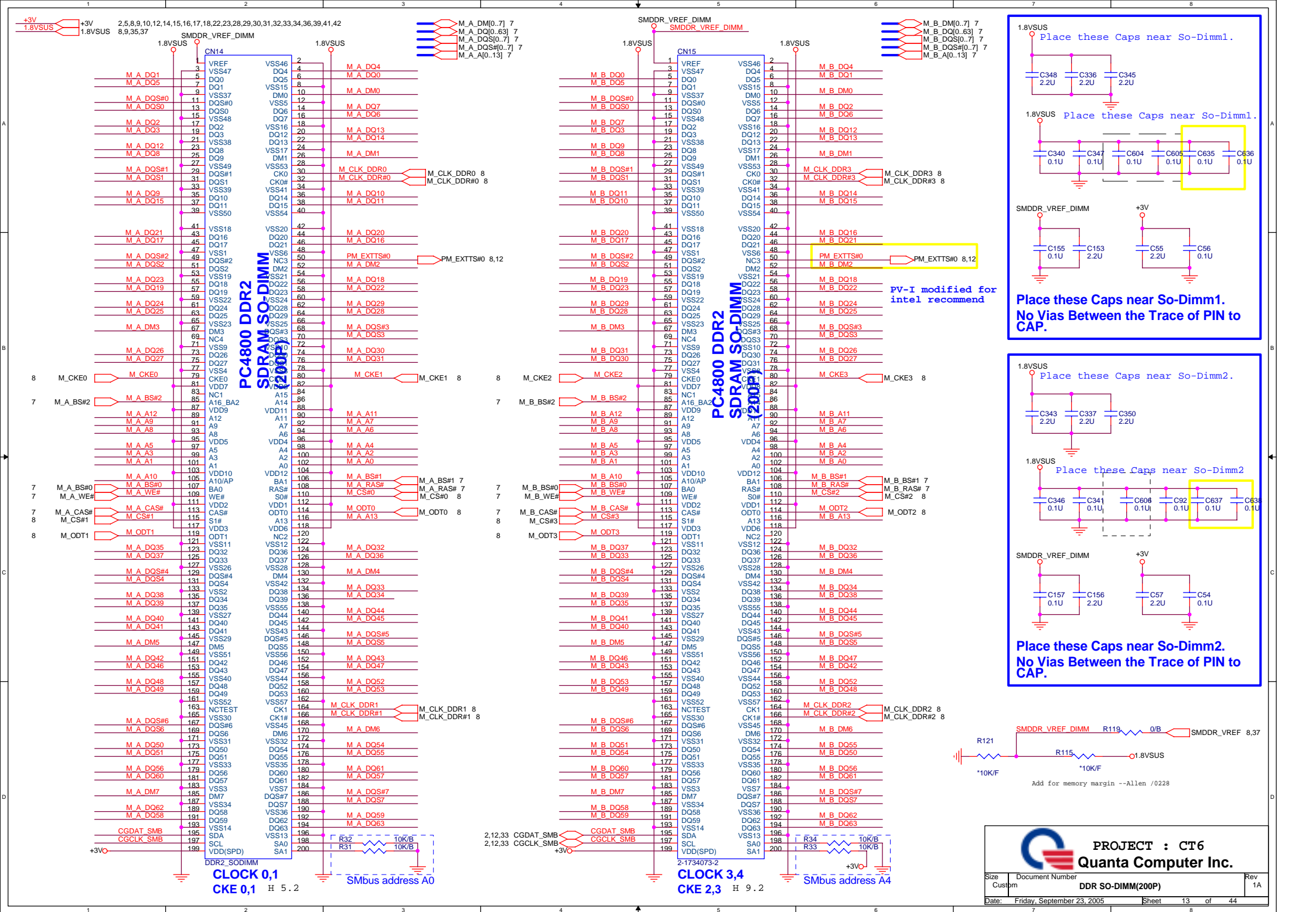
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM



PROJECT : CT6
Quanta Computer Inc.

Size B Document Number
DDR RES. ARRAY Rev 1A

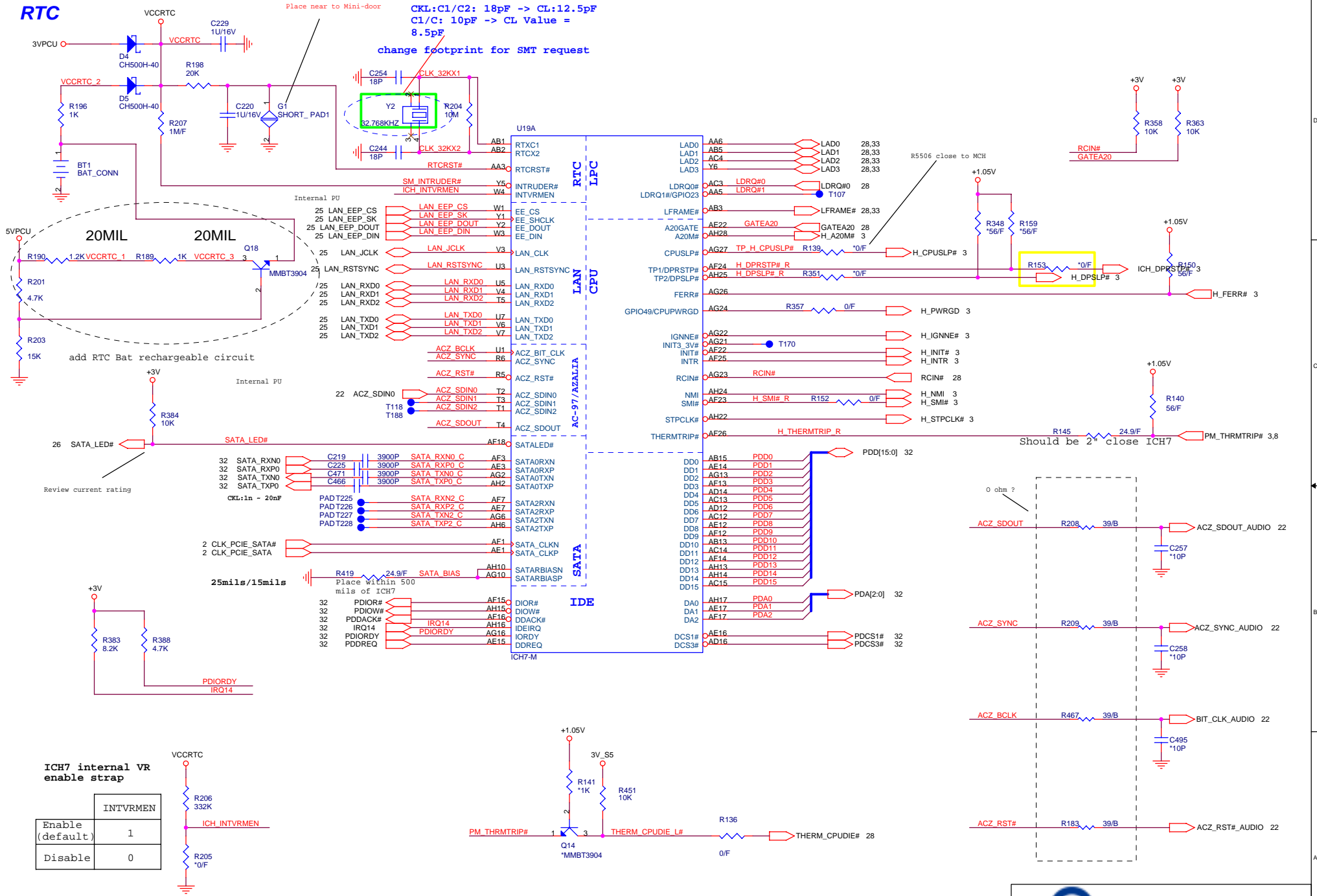
Date: Friday, September 23, 2005 Sheet 12 of 44



PROJECT : CT6
Quanta Computer Inc.

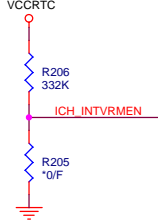
Size	Document Number	Rev
Custpm	DDR SO-DIMM(200P)	1A
Date:	Friday, September 23, 2005	Sheet 13 of 44


RTC



ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

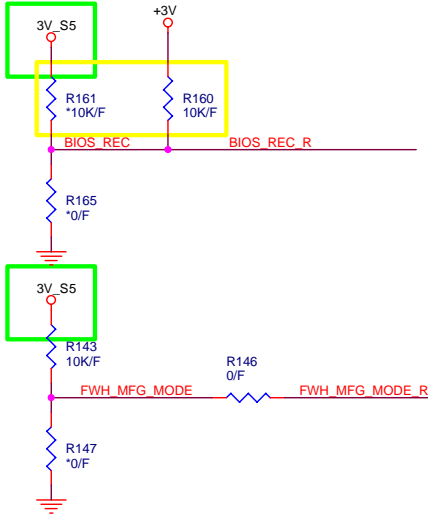
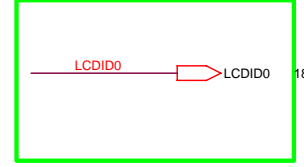
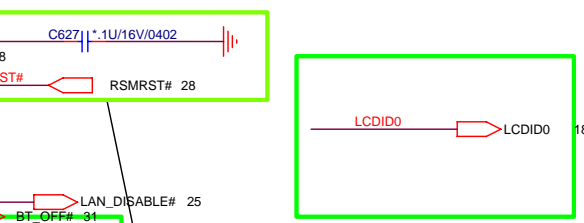
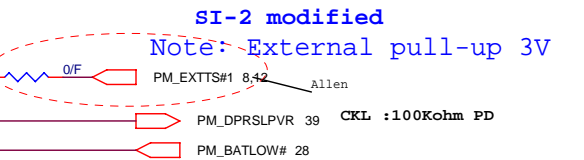
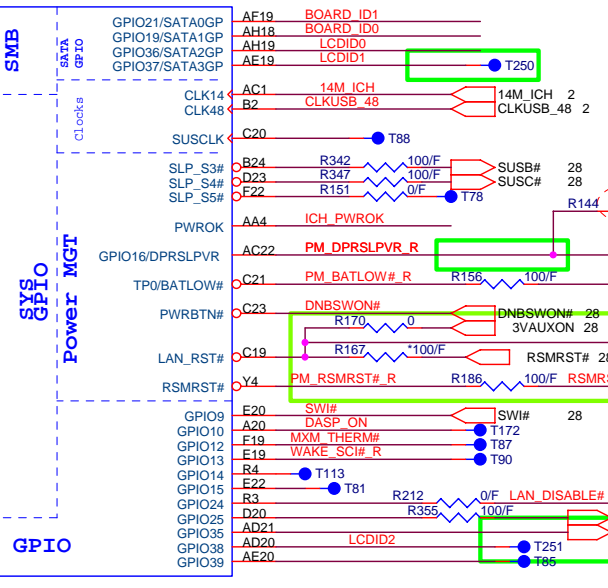
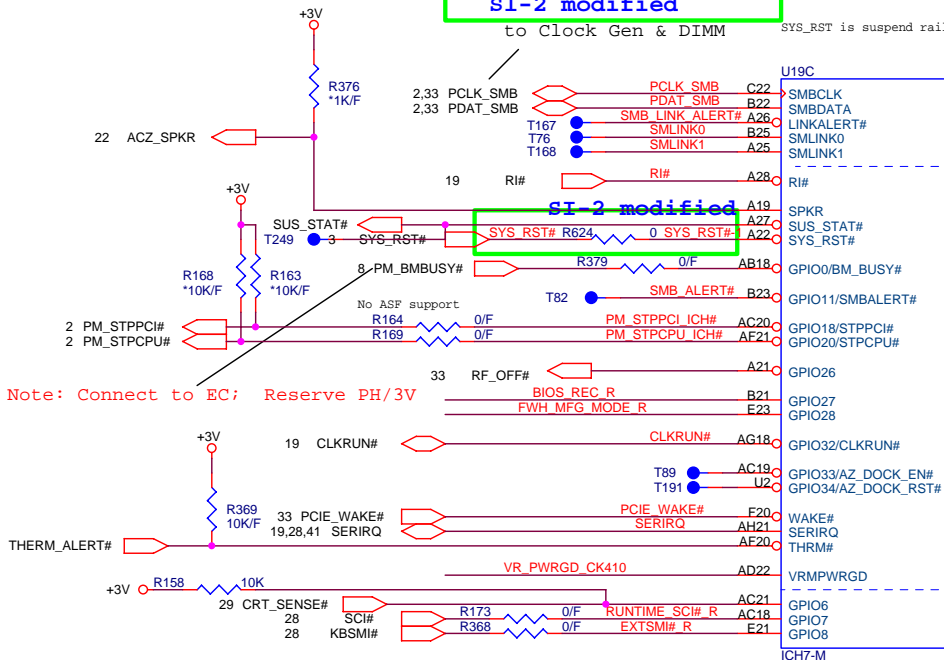
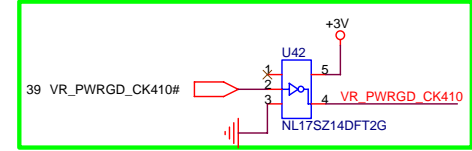
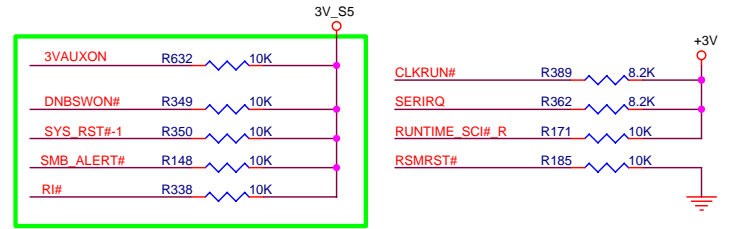
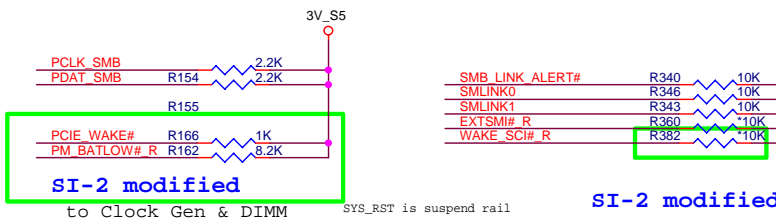




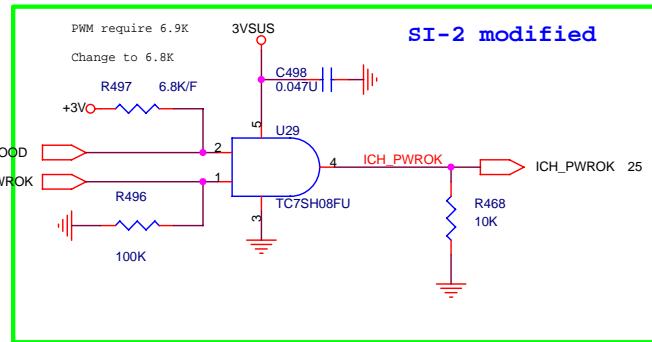
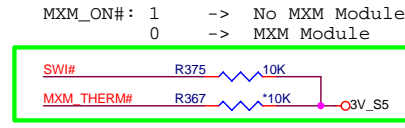
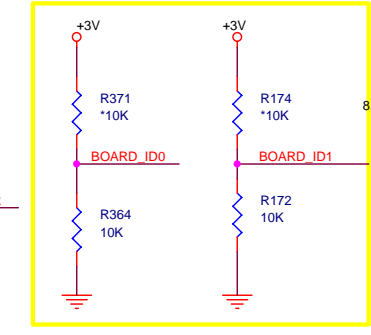
PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M HOST (1 OF 4)	1A
Date:	Friday, September 23, 2005	Sheet 14 of 44

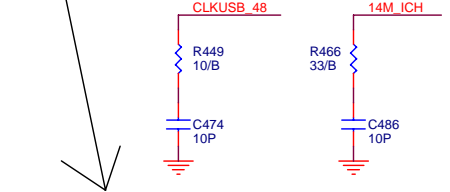
R376
No stuff-->boot
Stuff-->No boot



Board ID	PAVILION 31CT6MB0008	camare sku 31CT6MB0024
ID1:0	0--R364 stuff	1--R371 stuff
ID1:1	0--R172 stuff	0--R172 stuff



GPIO25 /Suspend rail is a HW strap , don't pull down .

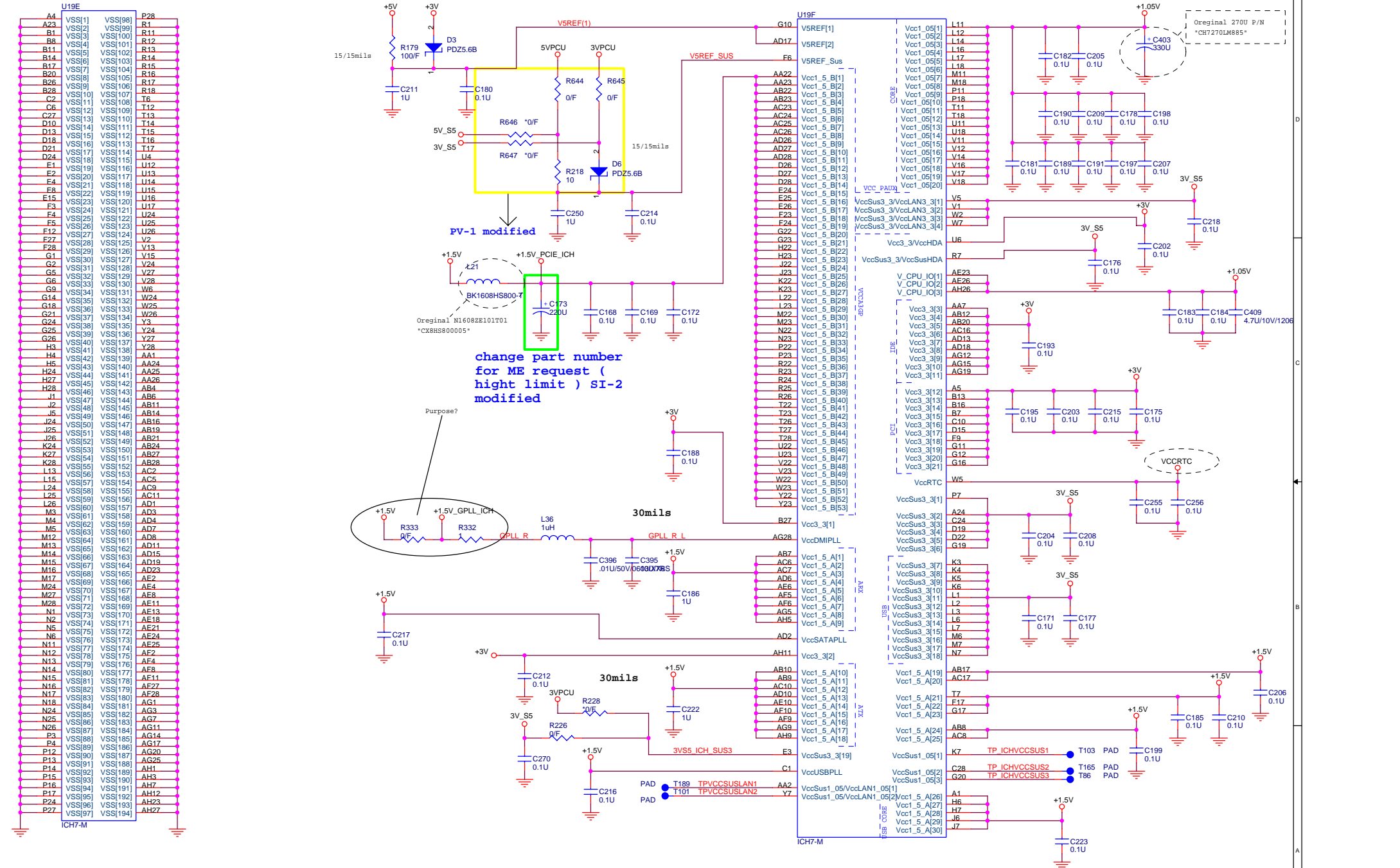


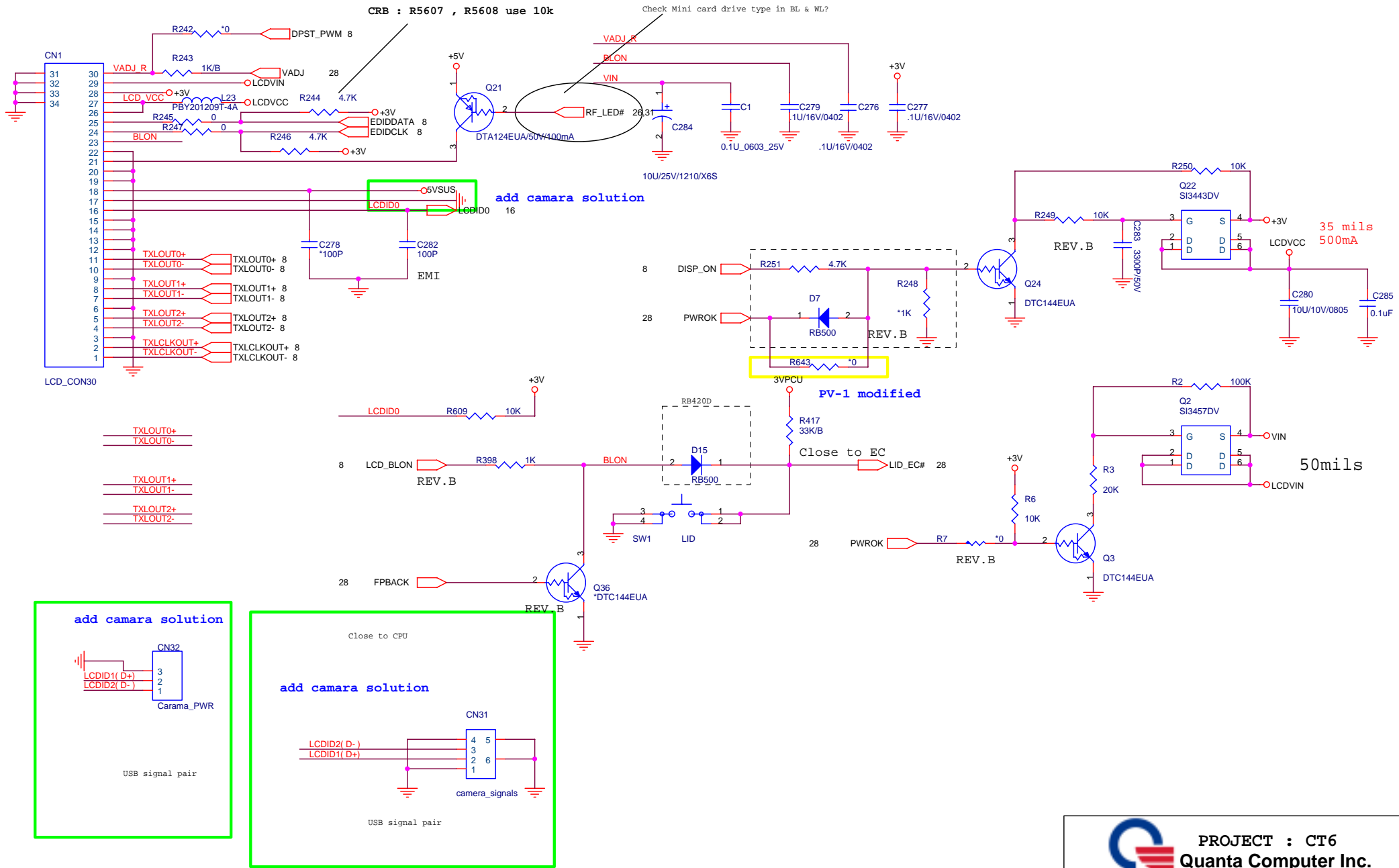
LAN_RST pin : 1.if used pci
LAN please tie to PLTRST#
PHY LAN please tie to RSMRST#

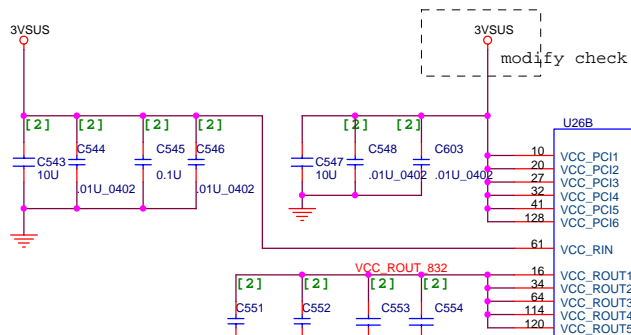
PROJECT : CT6
Quanta Computer Inc.

Size B Document Number ICH7-M GPIO (3 OF 4) Rev 1A

Date: Friday, September 23, 2005 Sheet 16 of 44



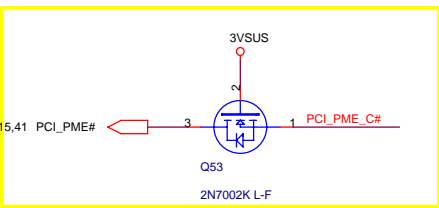




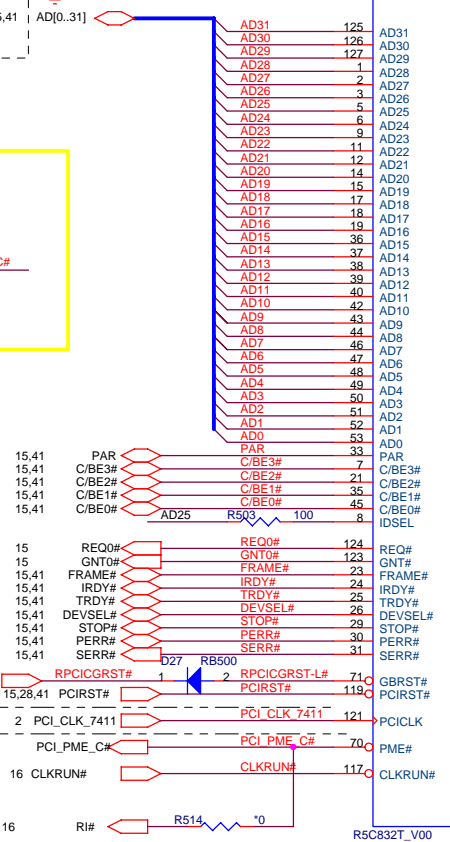
PCI Bus

PowerOnReset for VccCore

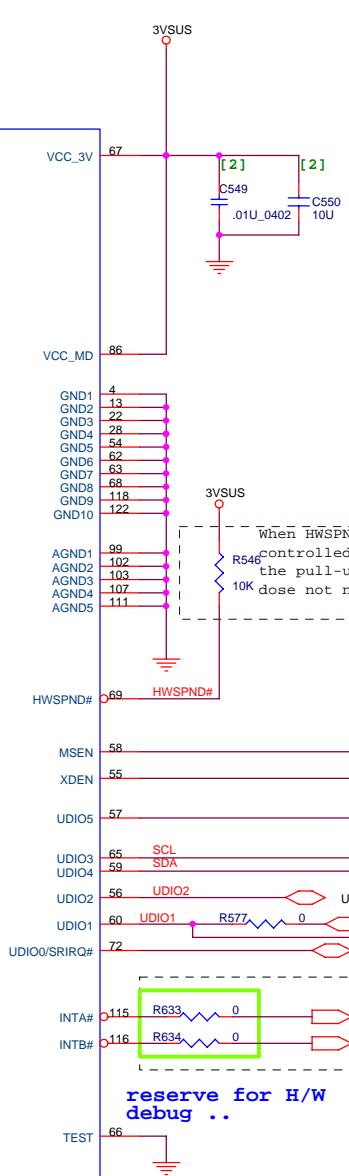
When GRESET# is controlled by system, the pull-up resistor(R3) and capacitor(C13) do not need to apply.



PV-1 modified to fix S5 WAKE-UP-LAN ISSUE (CH7M has leakage power to card reader)



PCI / OTHER



When HWSPND# is controlled by system, the pull-up resistor(R2) dose not need to apply.

* NOT Use EEPROM :
R545 : installed
R547, U22, C555 : NOT installed
* Use EEPROM :
R547, U22, C555 : installed
R545 : NOT installed

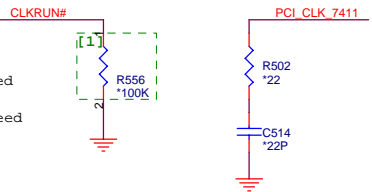
reserve for H/W debug ..

SI-2 modified

- [1] NOT INSTALLED
- [2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS
- [3] CLK LINE : SHIELDED BY GND. (RECOMMENDED)

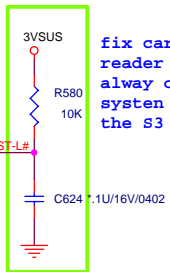
CoreLogic CLOCKRUN#

When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.

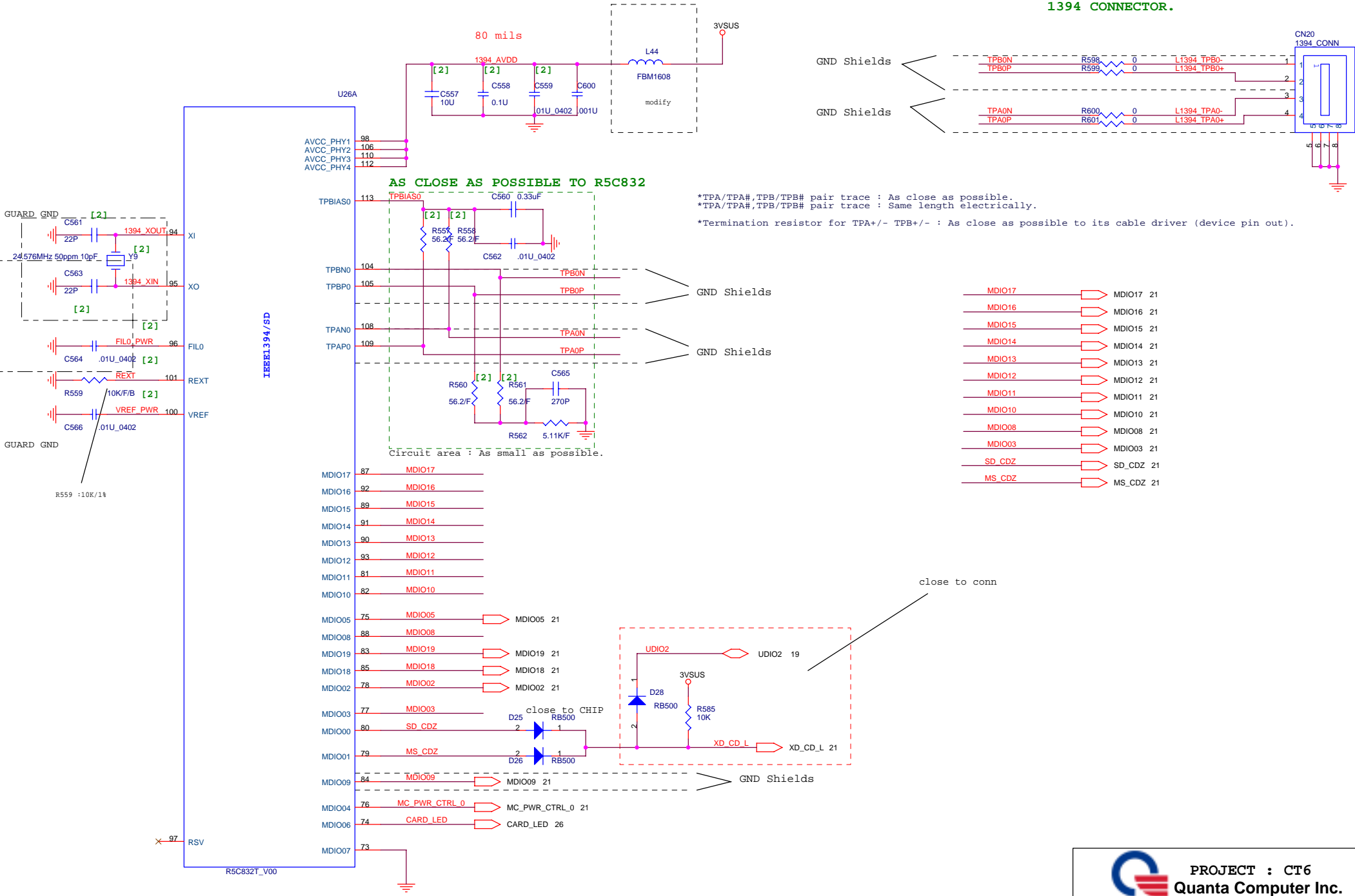


Check EC's RPCICGRST#. If uninstall R221, R374 shall be installed/Allen.

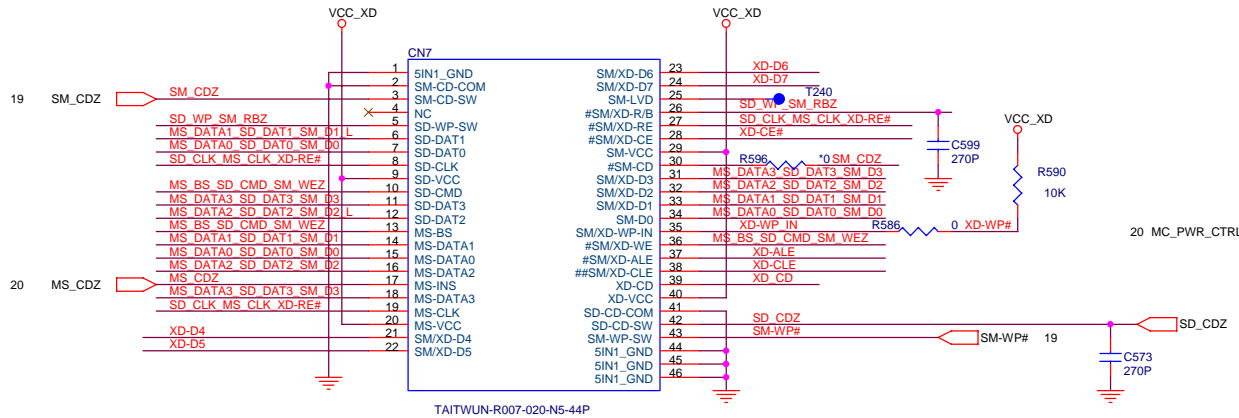
fix card reader LED always on when system into the S3



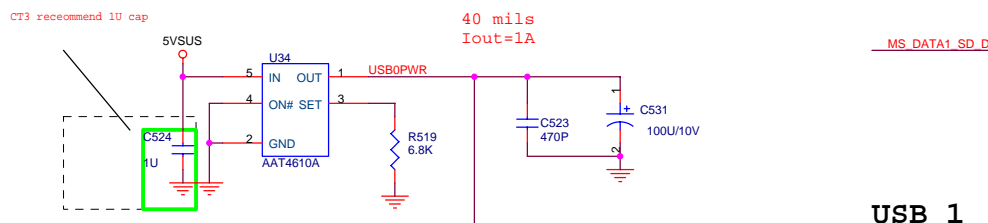
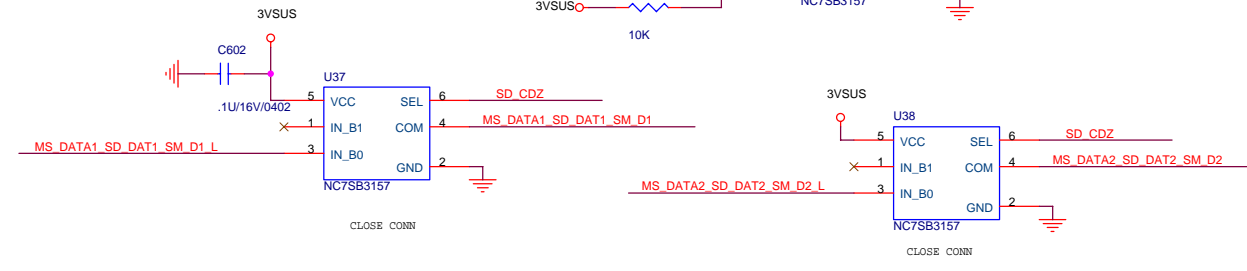
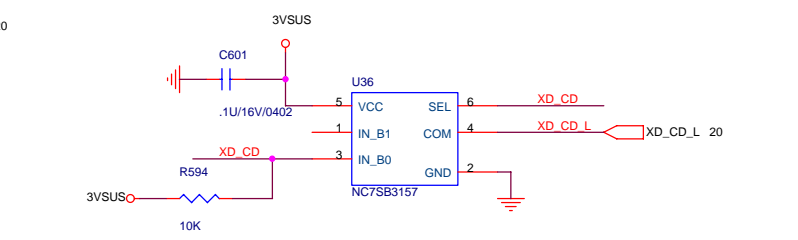
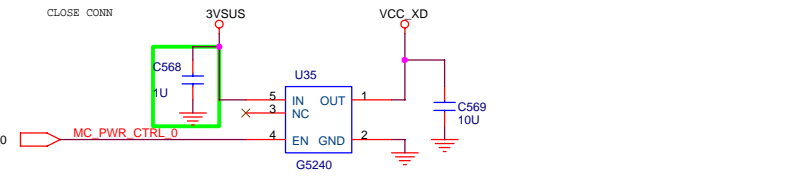
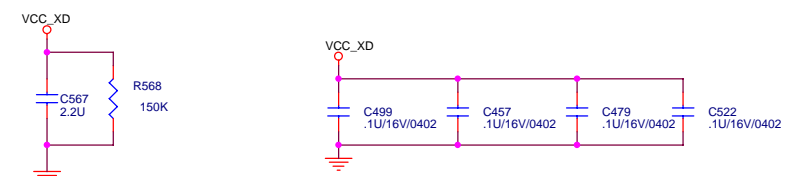
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



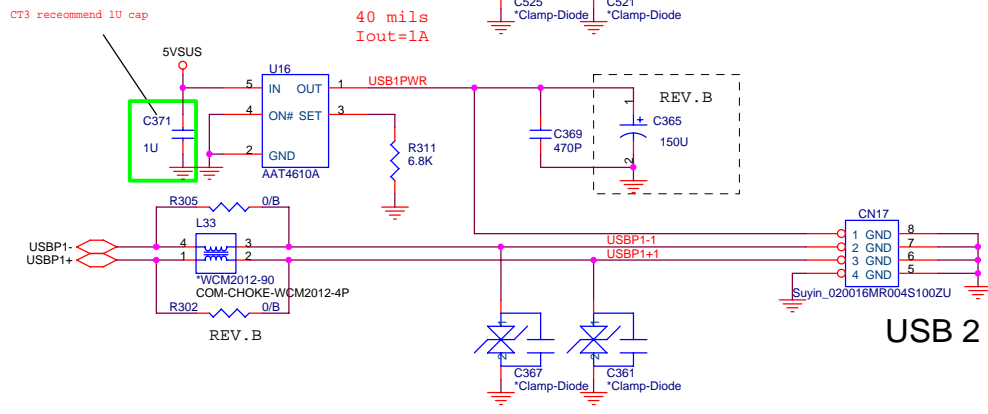
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.



5 IN1 CARD READER



USB 1

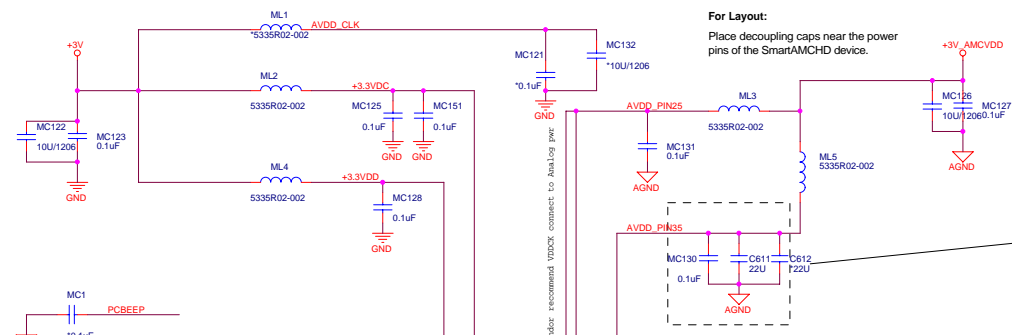


USB 2

20	MDIO03	MDIO03	R587	56	SD_WP_SM_RBZ
20	MDIO17	MDIO17	R200	56	XD-D7
20	MDIO16	MDIO16	R202	56	XD-D6
20	MDIO15	MDIO15	R210	56	XD-D5
20	MDIO14	MDIO14	R216	56	XD-D4
20	MDIO13	MDIO13	R191	56	MS_DATA3_SD_DAT3_SM_D3
20	MDIO12	MDIO12	R187	56	MS_DATA2_SD_DAT2_SM_D2
20	MDIO11	MDIO11	R184	56	MS_DATA1_SD_DAT1_SM_D1
20	MDIO10	MDIO10	R182	56	MS_DATA0_SD_DAT0_SM_D0
20	MDIO08	MDIO08	R181	56	MS_BS_SD_CMD_SM_WEZ
20	MDIO05	MDIO05	R197	56	XD-WP#
20	MDIO19	MDIO19	R563	56	XD-ALE
20	MDIO18	MDIO18	R564	56	XD-CLE
20	MDIO02	MDIO02	R220	56	XD-CE#
20	MDIO09	MDIO09	R222	56	SD_CLK_MS_CLK_XD-RE#

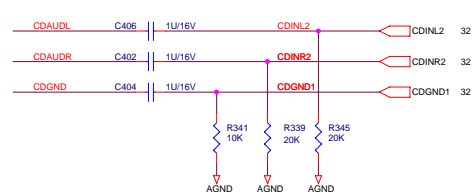
change from 0 ohm to 56 ohm (from vendor recommend)

PROJECT : CT6
Quanta Computer Inc.
CARD READER CONN,USB x 2
 Rev 1A
 Date: Friday, September 23, 2005 Sheet 21 of 44

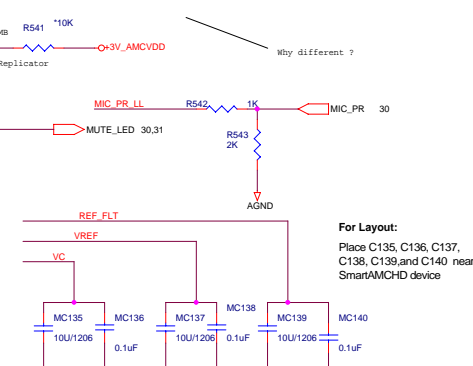


Interference/Harley

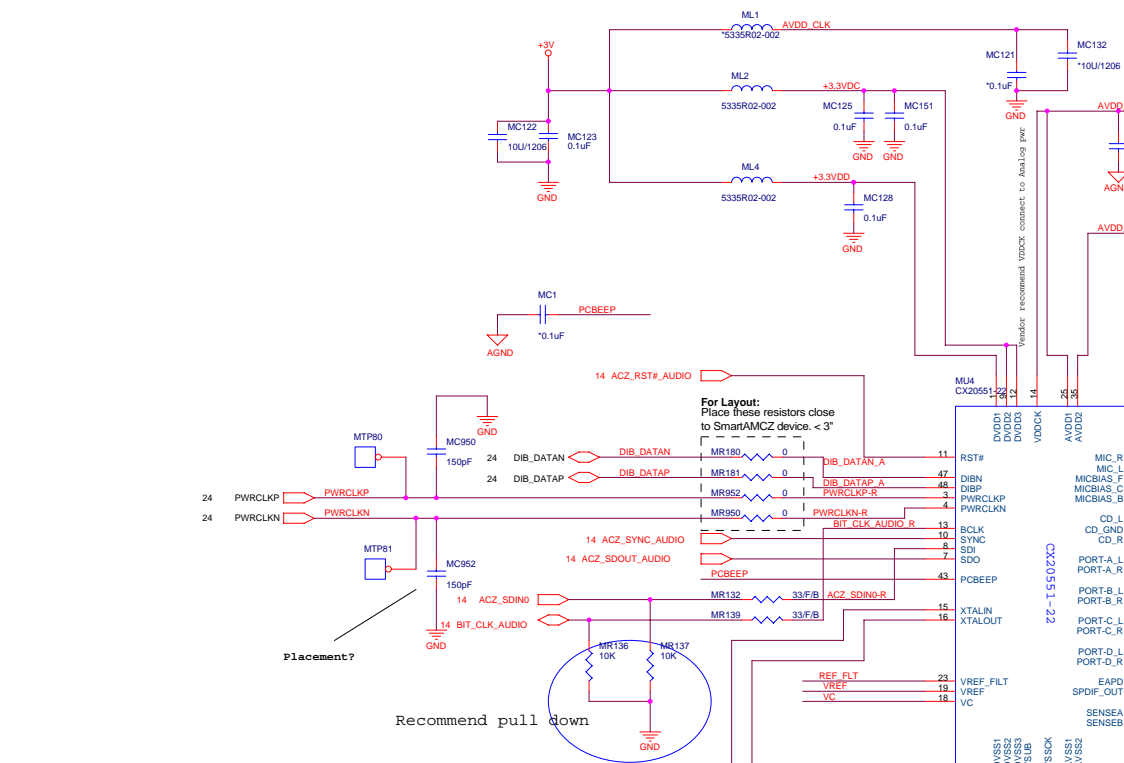
FROM CD-ROM



Why different ?



For Layout:
Place C135, C136, C137, C138, C139, and C140 near SmartAMCHD device



For Layout:
Place these resistors close to SmartAMCZ device, < 3"

Placement?

Recommend pull down

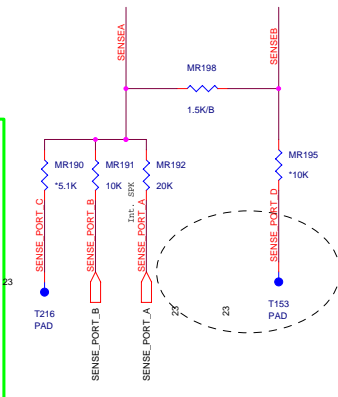
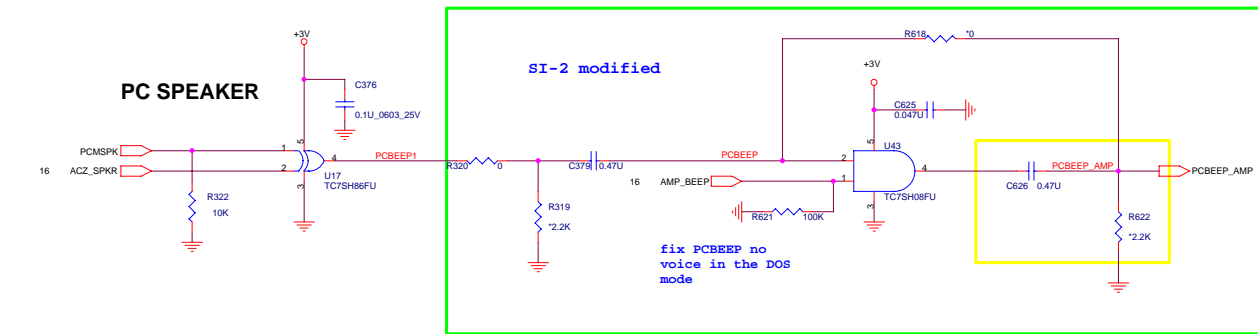
For Layout:
Place crystal and associated circuitry very near SmartAMCHD Device.

For AC-Link Mode: An external 14.318MHz clock source can be used to replace the crystal circuitry shown here. It should be connected to XTALIN (pin 15). The XTALOUT (pin 16) should be left floating.

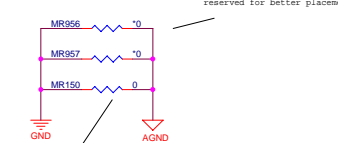
For HD Audio Mode: Do not populate crystal circuitry and leave XTALIN (pin 15) and XTALOUT (pin 16) floating.

Check placement

For EMI request



Ground Tie



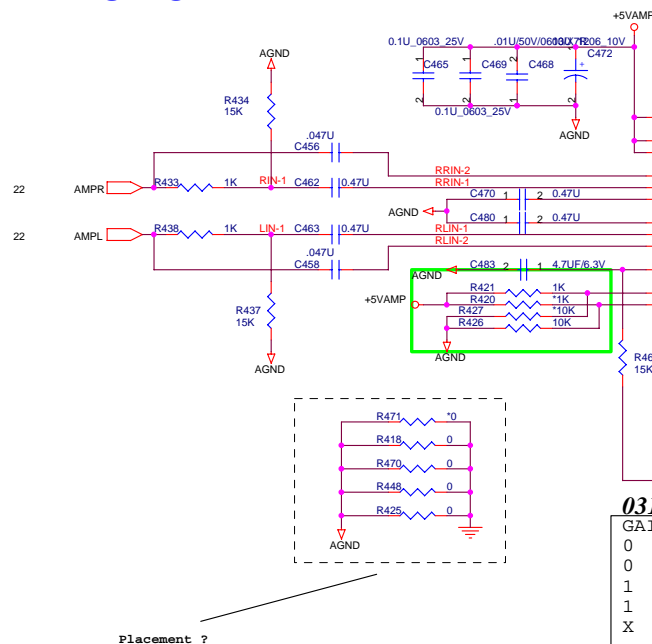
Placement ?

MB SPKR LINOUT and PR JACK: A
MB MIC : B
Docking Mic : C

PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
C	Azalia CTRL_CONEXANT20551	1A
Date	Friday, September 23, 2005	Sheet 22 of 44

AUDIO AMPLIFIER

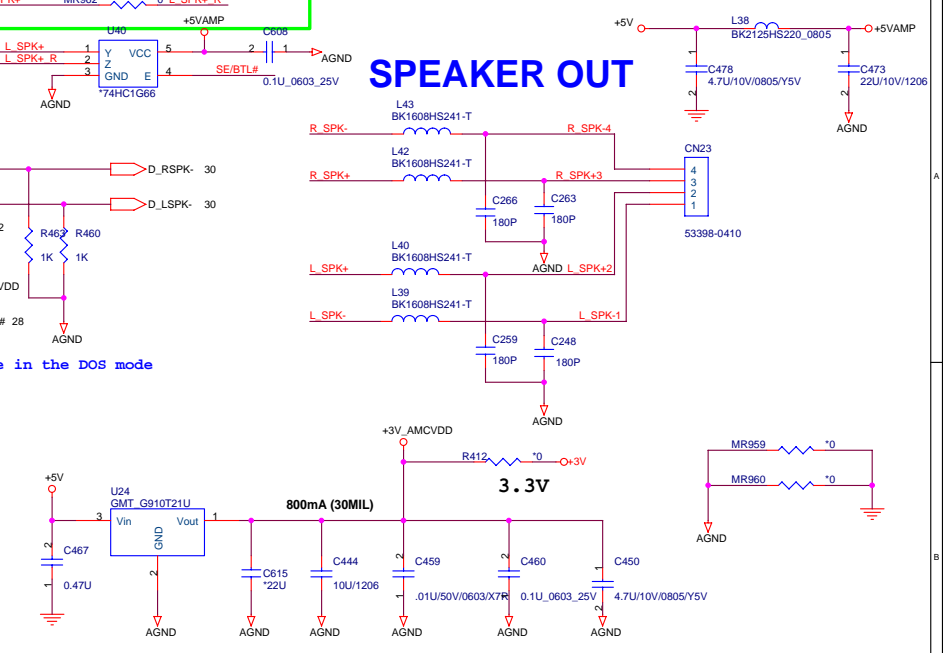


0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV (inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

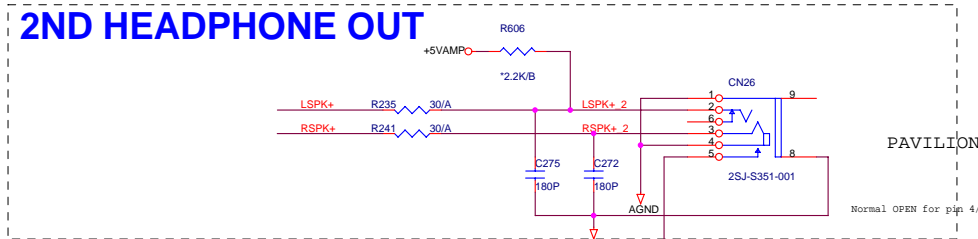
Placement ?

SPEAKER OUT



fix PC-BEEP no voice in the DOS mode

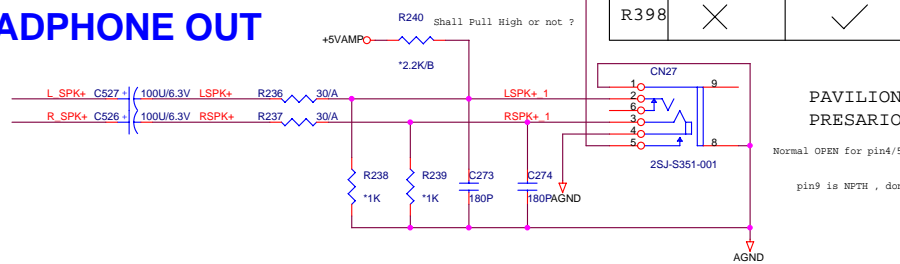
2ND HEADPHONE OUT



PAVILION

Normal OPEN for pin 4/5

HEADPHONE OUT



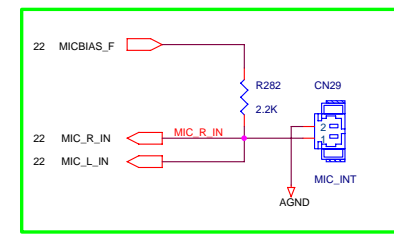
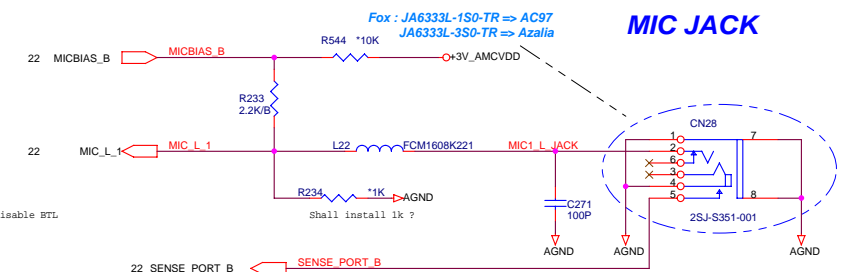
PAVILION
PRESARIO

Normal OPEN for pin4/5

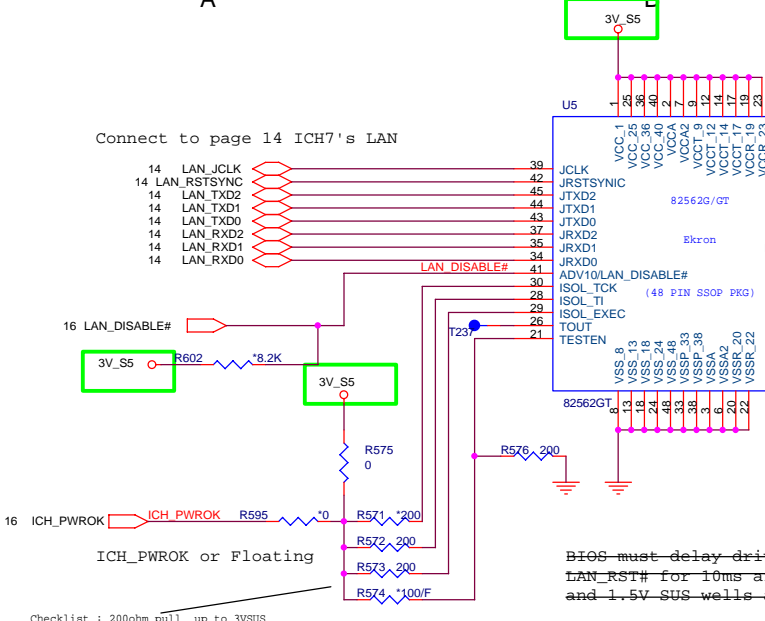
pin9 is NPTH , don't need to GND

	PAVILION	PRESARIO
R151	✓	✗
R398	✗	✓

MIC JACK

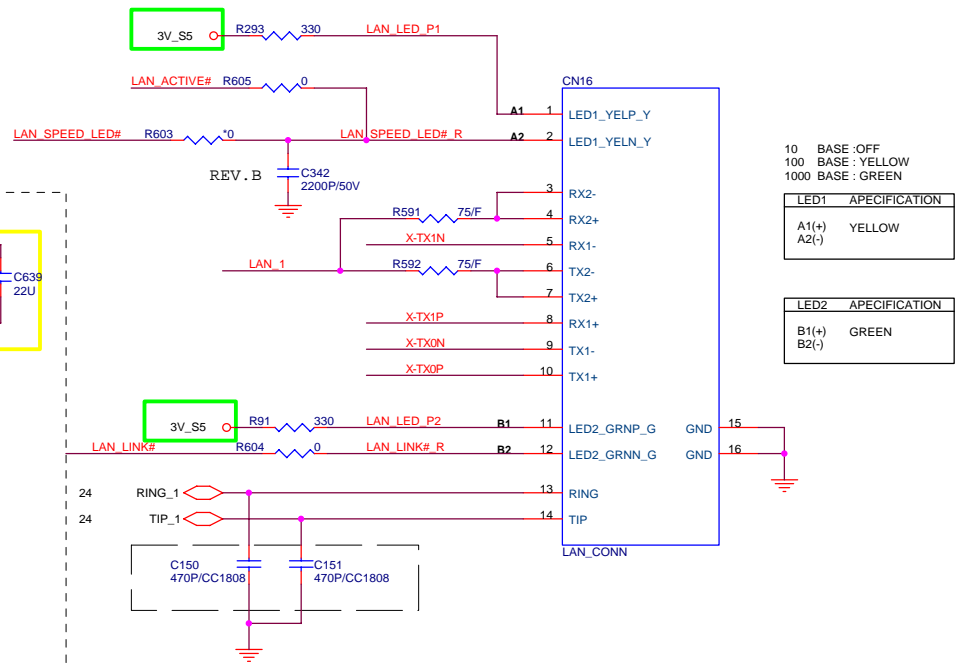
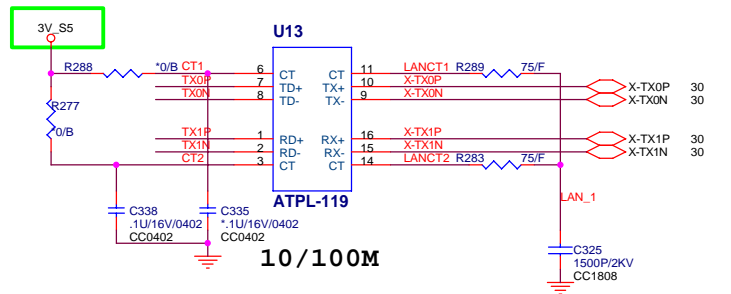
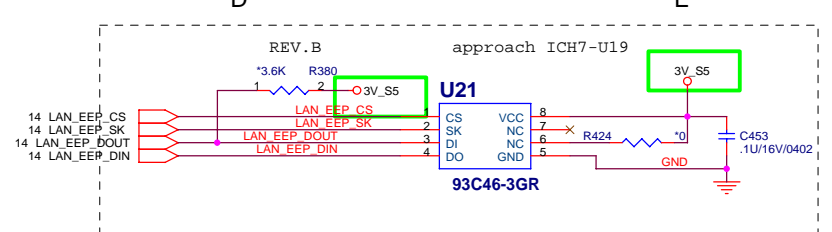
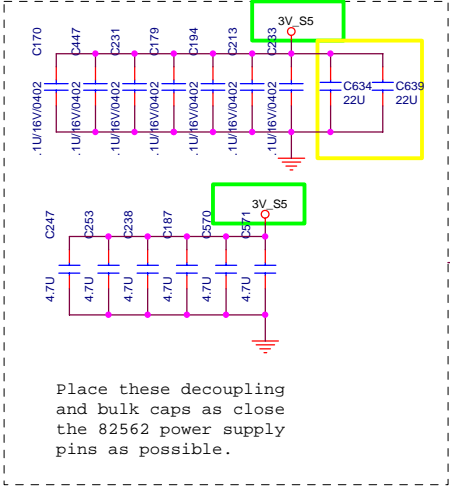
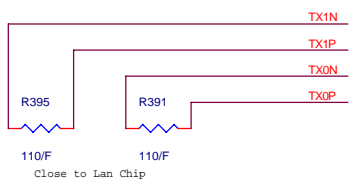


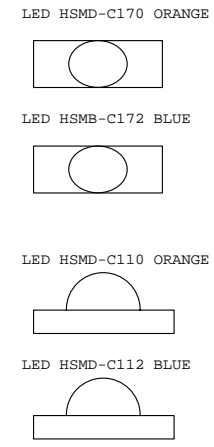
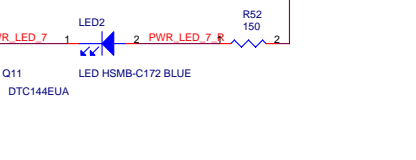
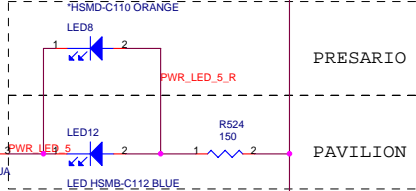
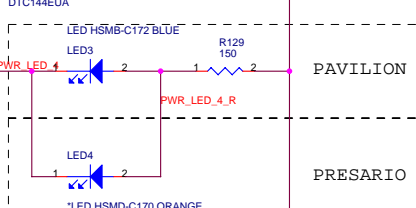
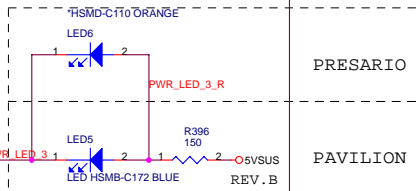
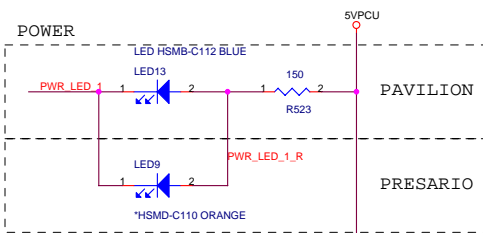
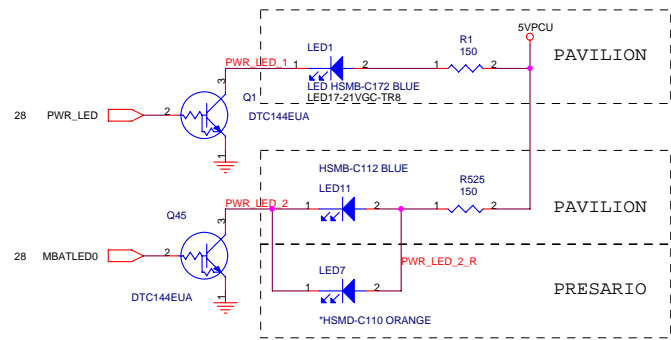
Internal MIC



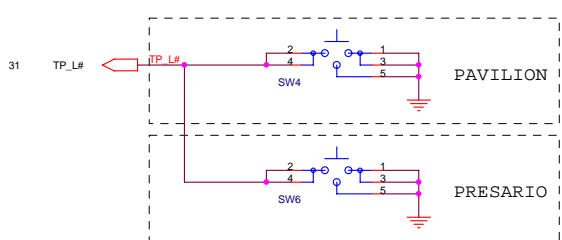
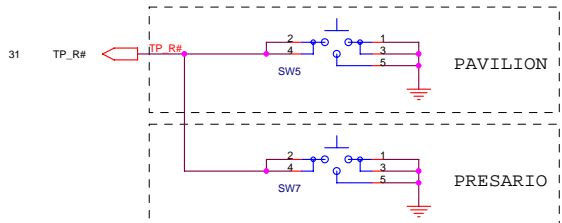
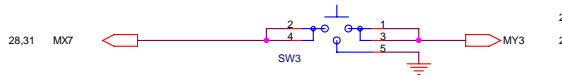
SI2 modified (remove LANVCC power and change to 3V_S5 for fix LAN wake up)

BIOS must delay driving LAN_RST# for 10ms after 3.3v and 1.5v SUS wells are valid





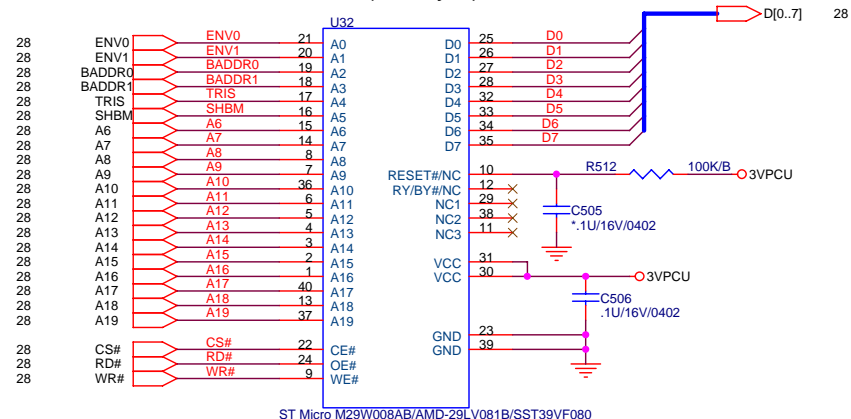
Touchpad control



REV.B: LED7 AND LED8 SWAP



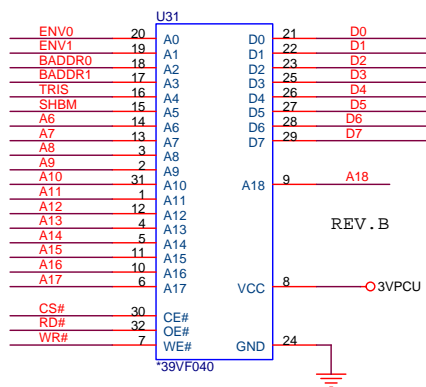
8Mbit (1M Byte), TSSOP40

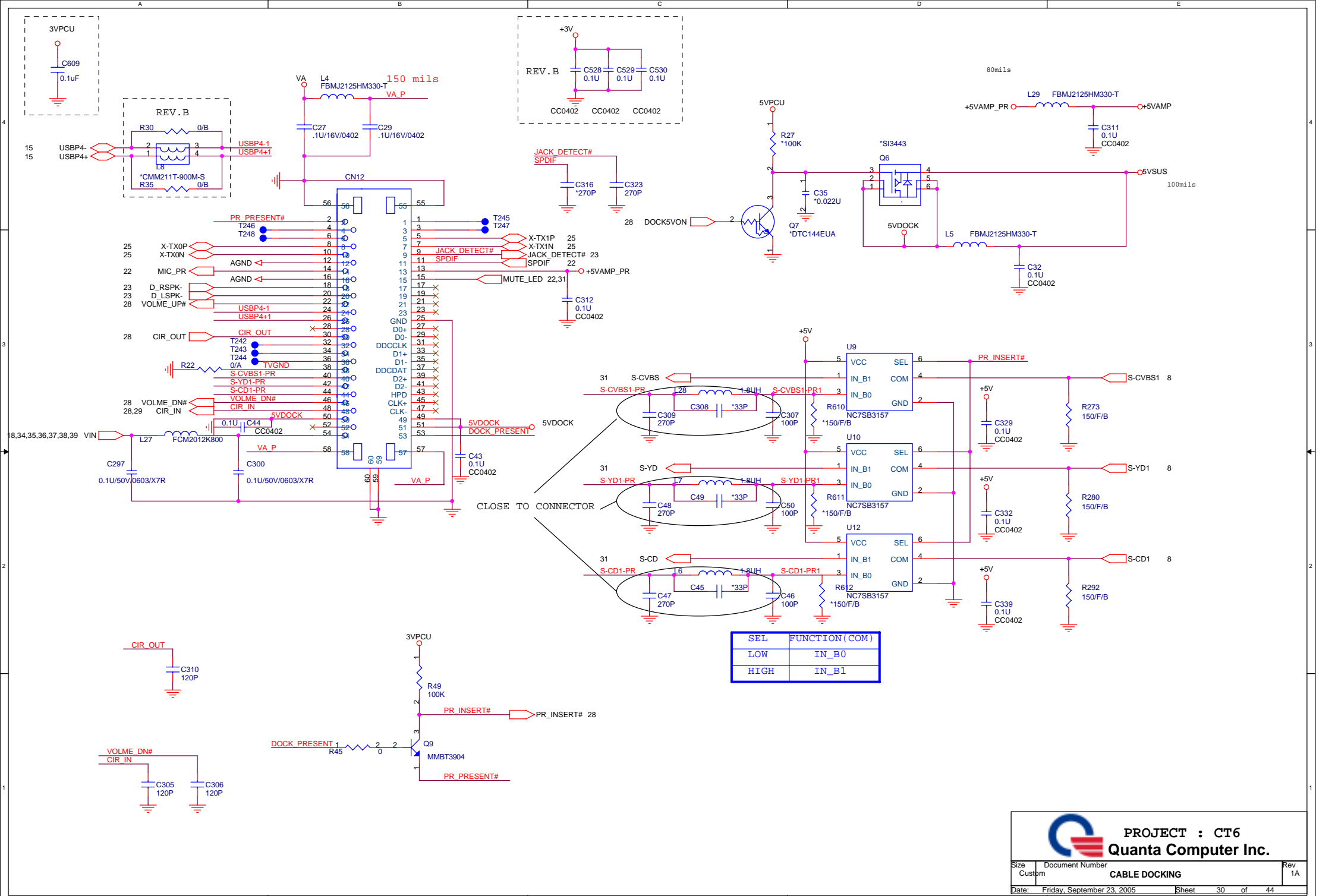


AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

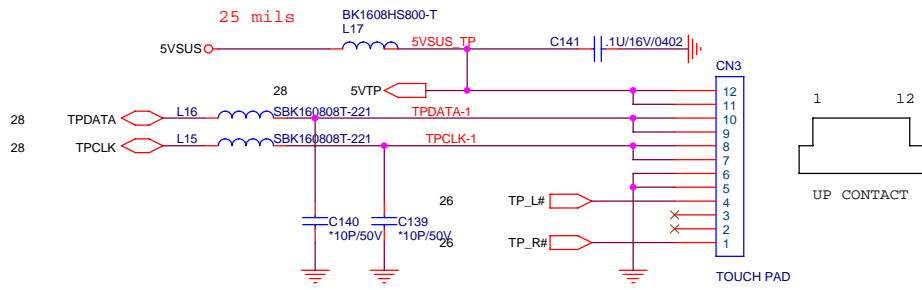
- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100ms reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

4Mbit (512k Byte), TSSOP32



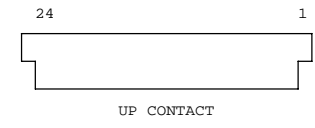
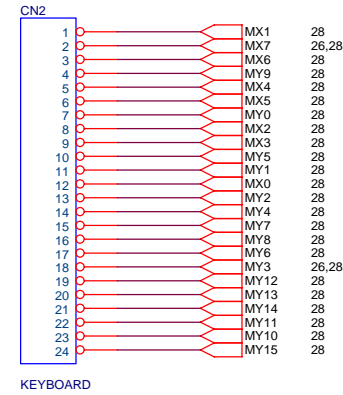


TOUCH PAD CONNECTOR

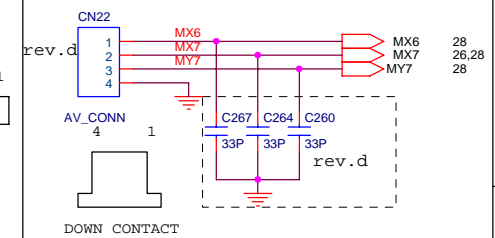


CHECK PIN DEFINE

KEYBOARD CONNECTOR

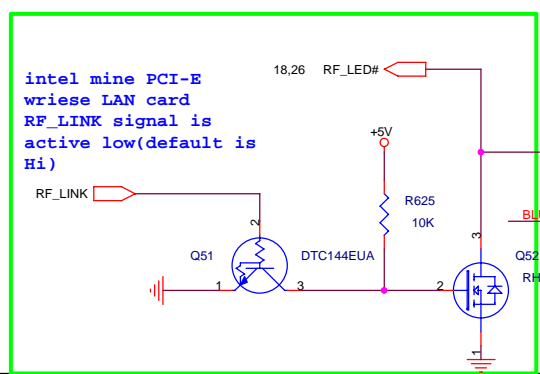


AV BOARD

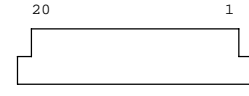
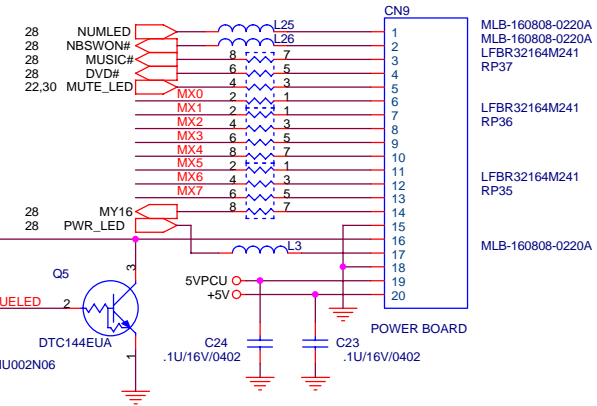


MX6	MX7
ENTER	MENU

POWER BOARD



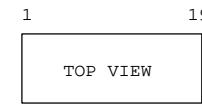
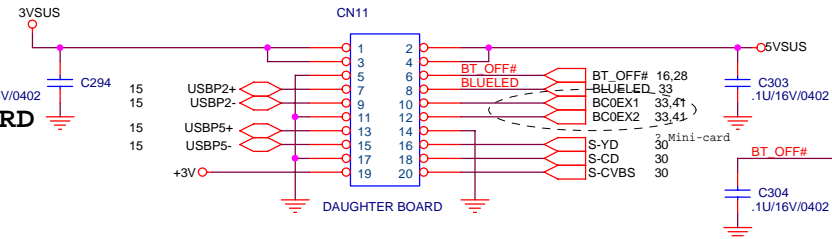
intel mine PCI-E
write LAN card
RF_LINK signal is
active low(default is
Hi)



MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARD	STOP	VOL UP	MUTE	VOL DN	WIRELESS

STOP =>MX0+MY12
NEW=>MX1+MY12

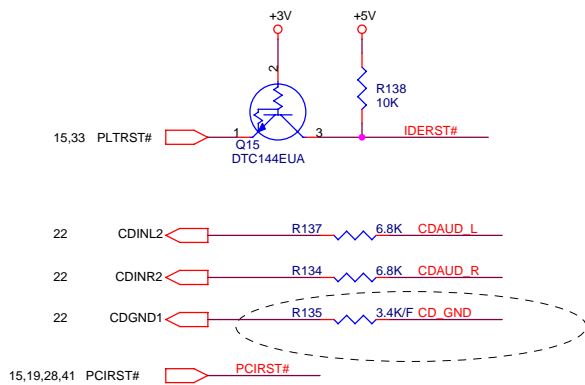
DAUGHTER BOARD



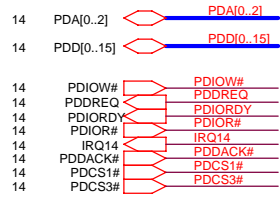
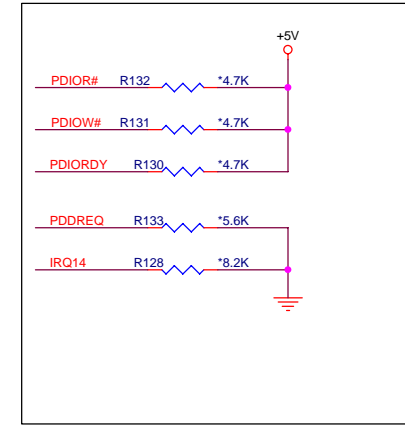
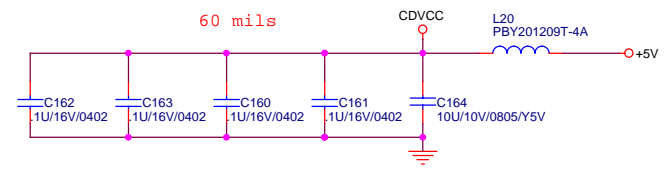
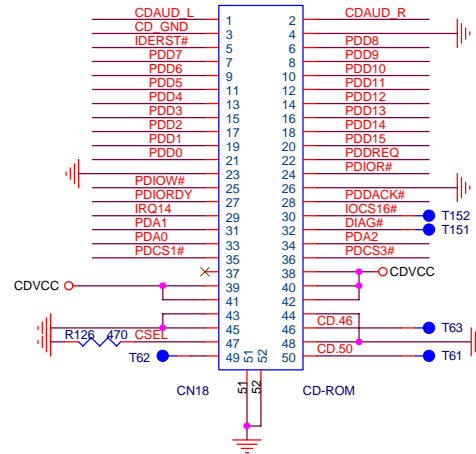
PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLUETOOTH/TP/KEY/BTB	1A

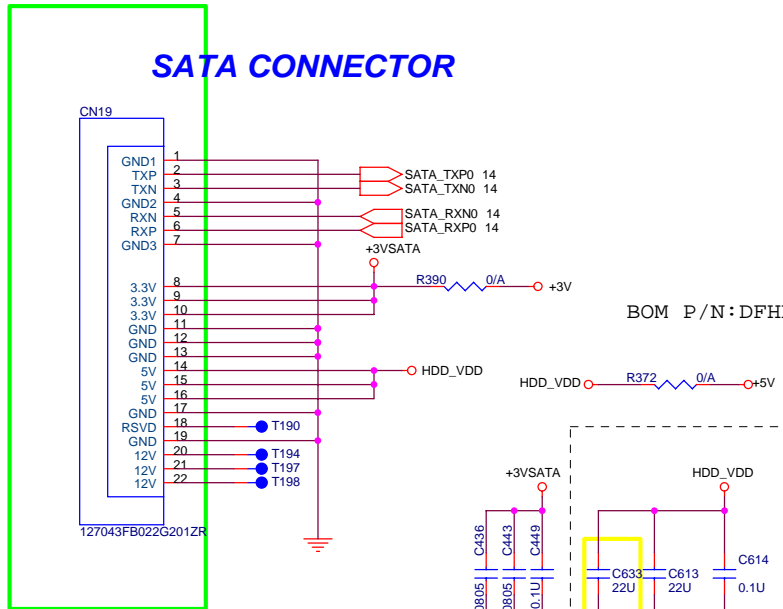
Date: Friday, September 23, 2005 Sheet 31 of 44



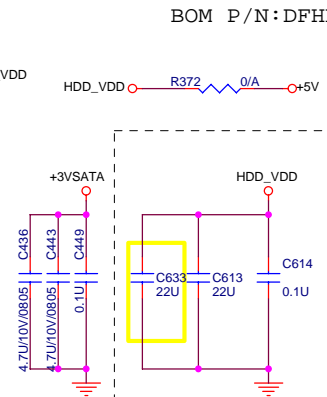
CD-ROM




SATA CONNECTOR



change footprint for SMT request (add 防呆 pin)

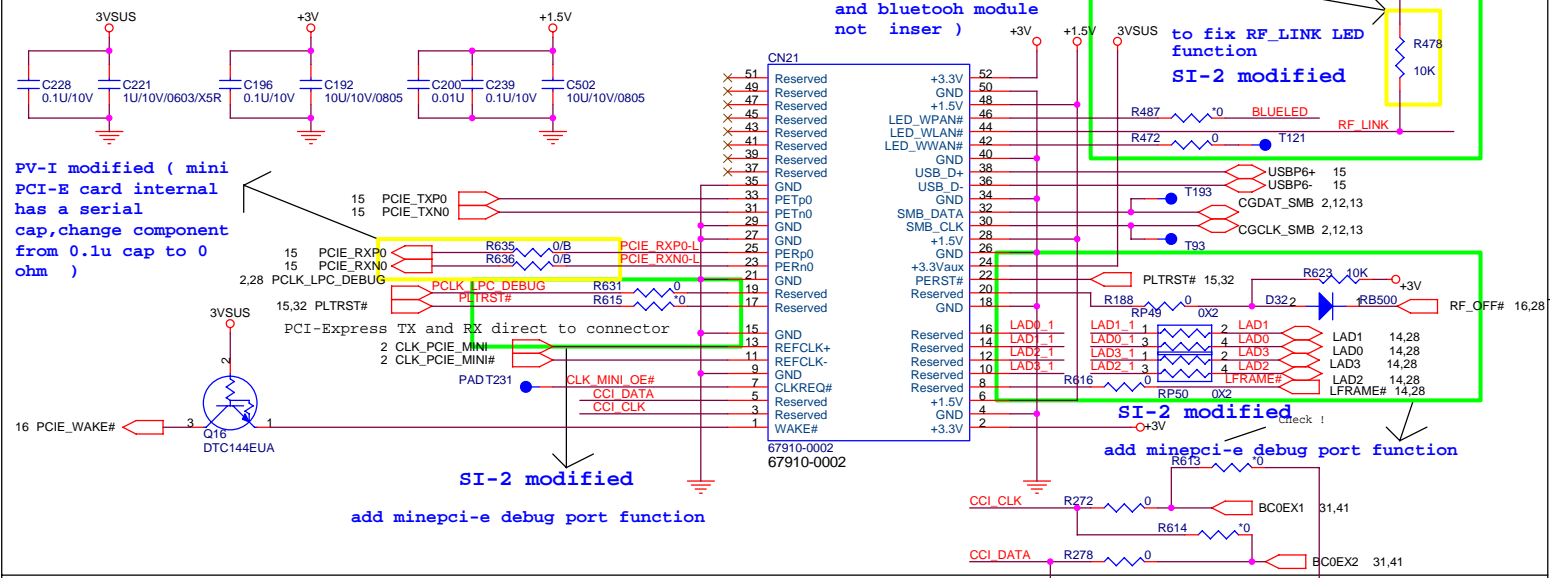




PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	SATA HDD, CD-ROM	Rev
Custom			1A
Date: Friday, September 23, 2005		Sheet	32 of 44

Mini PCI-E Card



PV-I modified (mini PCI-E card internal has a serial cap, change component from 0.1u cap to 0 ohm)

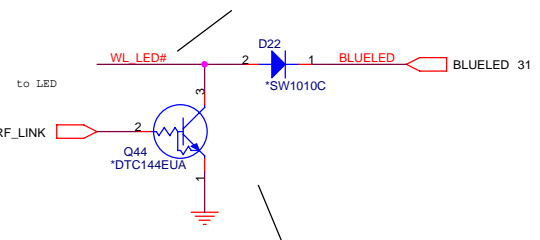
PV-1 modified (R478 need to stuff for fix wireless LED always on when wireless lan card and bluetooth module not inser)

to fix RF_LINK LED function SI-2 modified

SI-2 modified add minepci-e debug port function

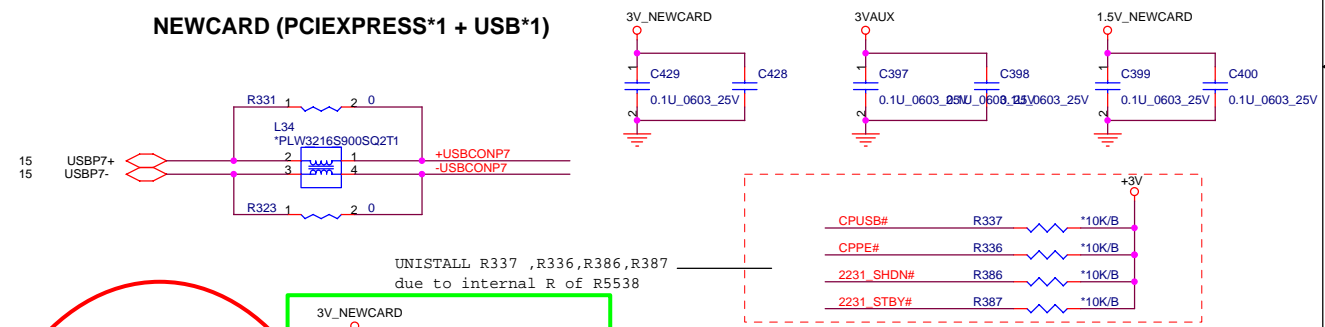
SI-2 modified add minepci-e debug port function

Need one more wireless LED /mini card on MB ? currently , No LED here



RF_LINK#, check with KN1


NEWCARD (PCIEXPRESS*1 + USB*1)



UNINSTALL R337 ,R336,R386,R387 due to internal R of R5538

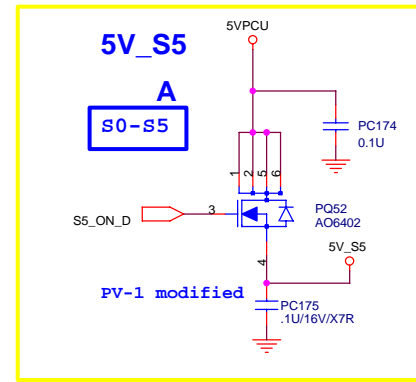
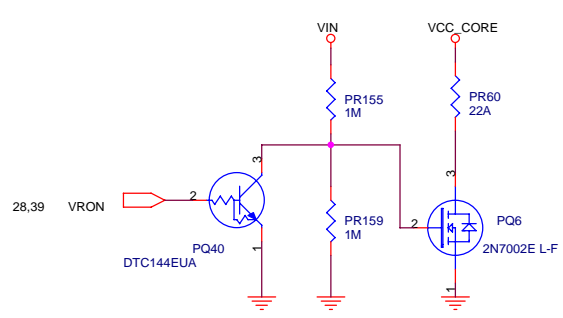
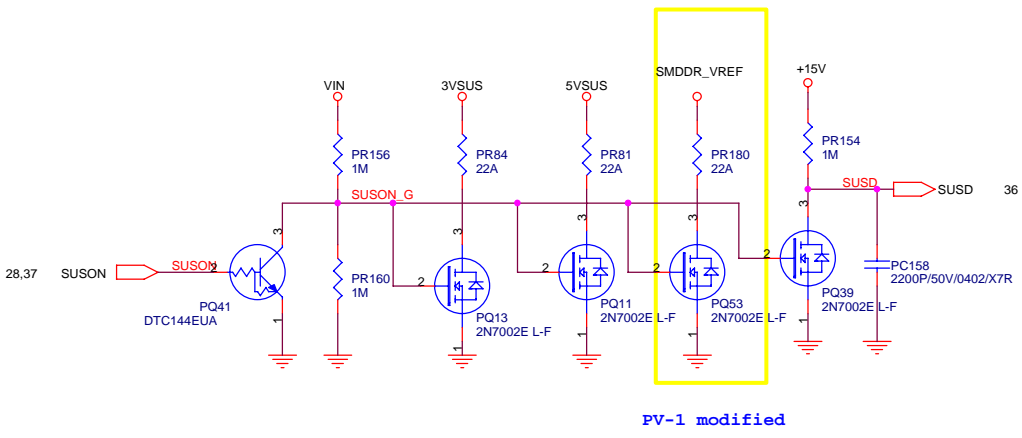
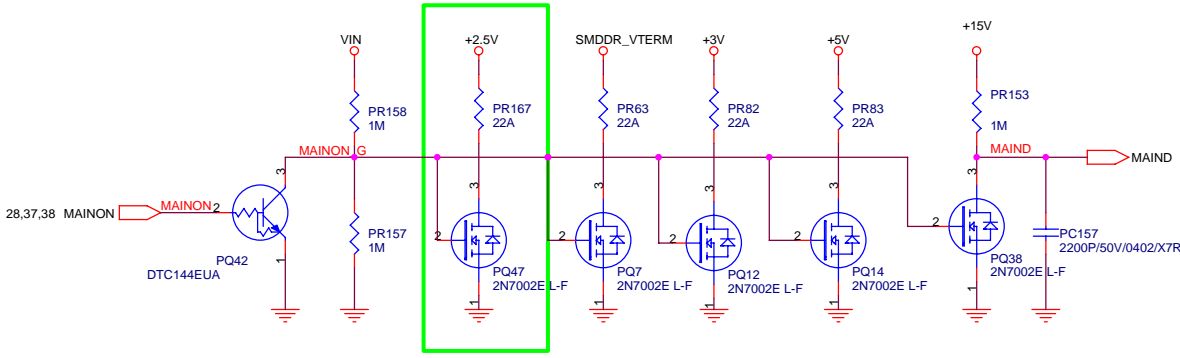
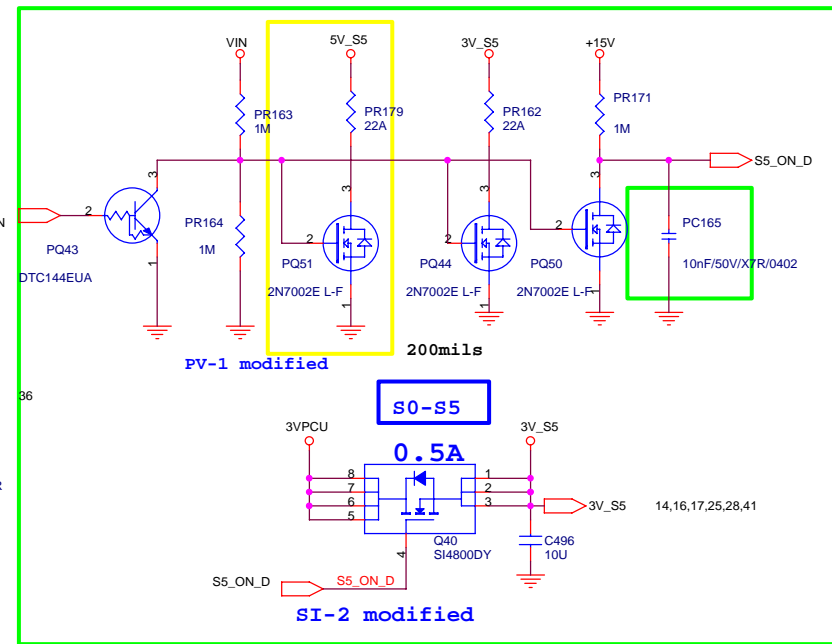
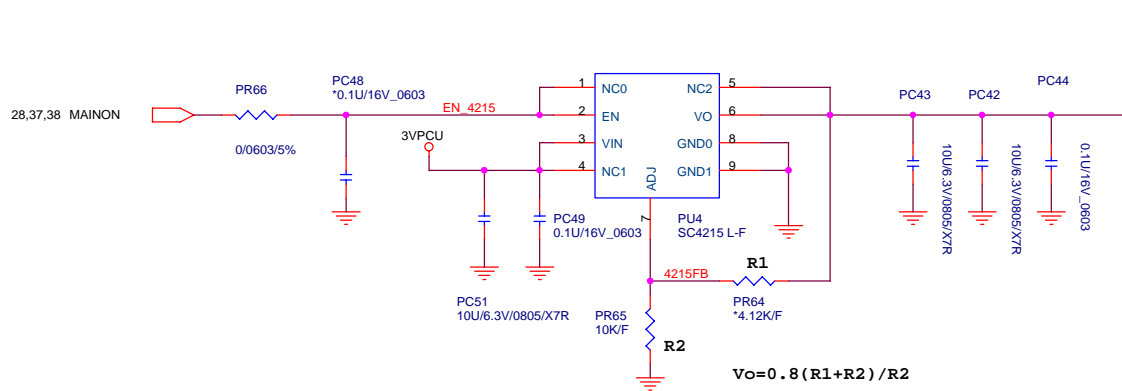
PV-I modified (Express card internal has a serial cap, change component from 0.1uf to 0 ohm)

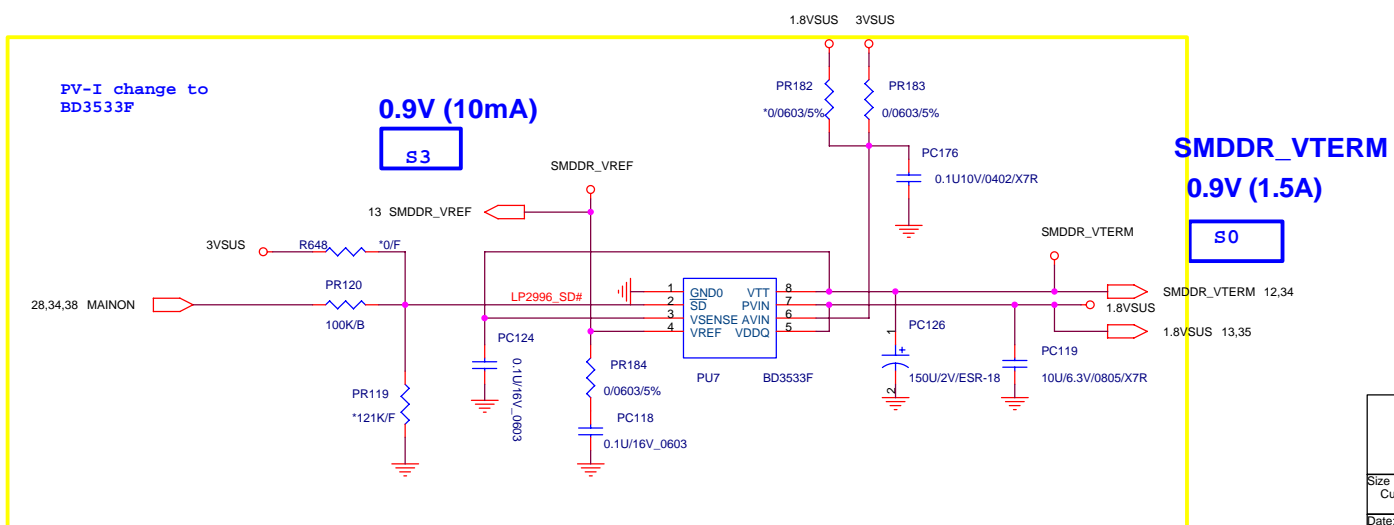
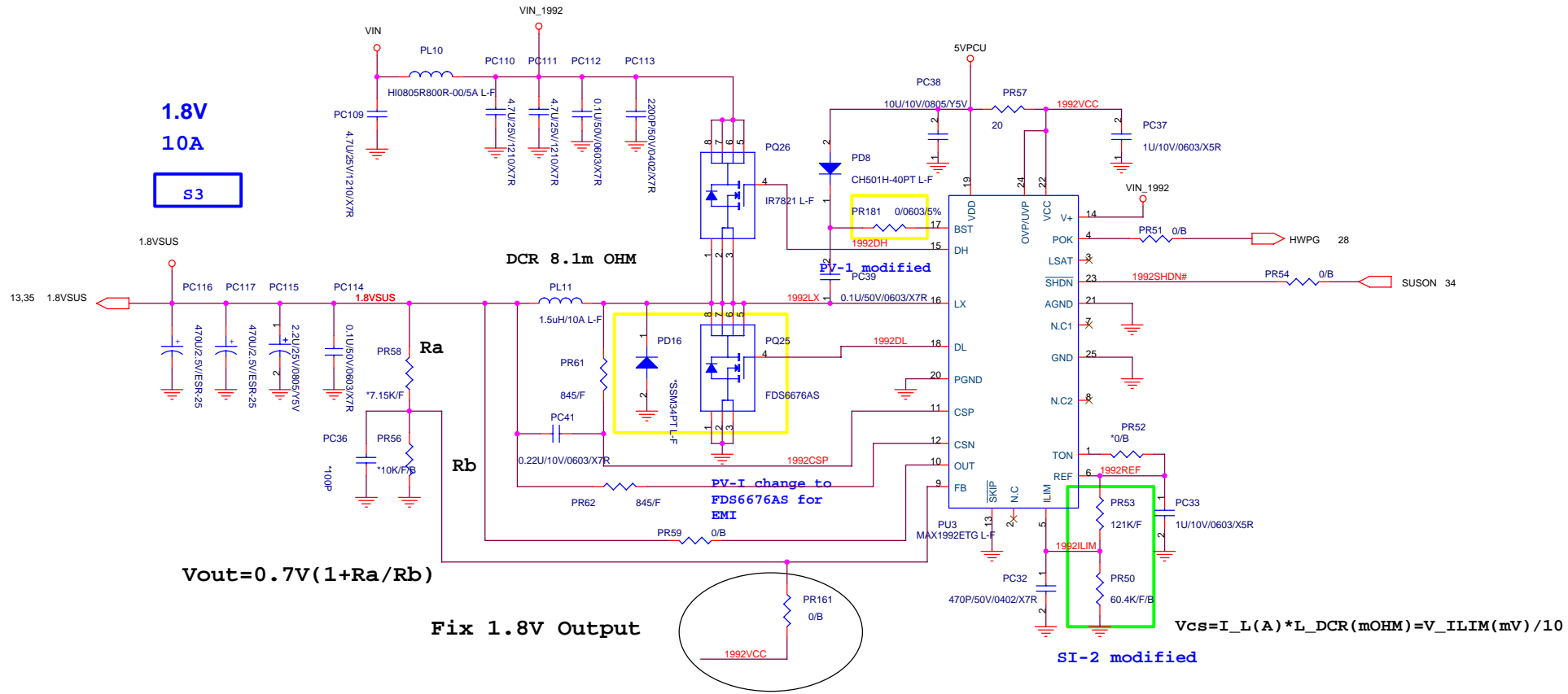
change footprint for ME request

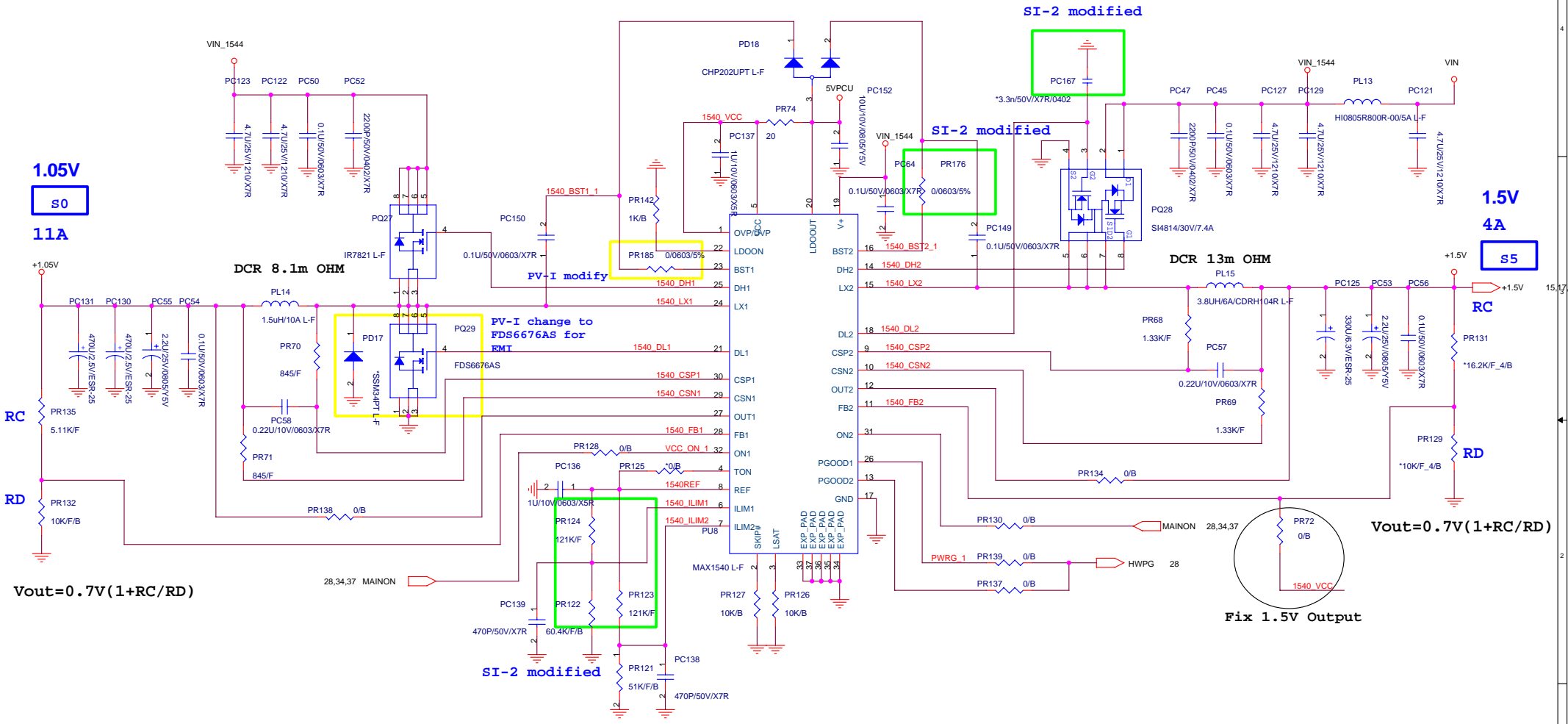


PROJECT : CT6
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Size	Document Number	Rev
Custom	NEW CARD, MINI CARD	1A
Date:	Friday, September 23, 2005	Sheet 33 of 44







$$V_{cs} = I_{L(A)} * L_{DCR(mOHM)} = V_{ILIM(mV)} / 10$$


PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1540 (+1.05V/+1.5V)	1A
Date:	Friday, September 23, 2005	Sheet 38 of 44

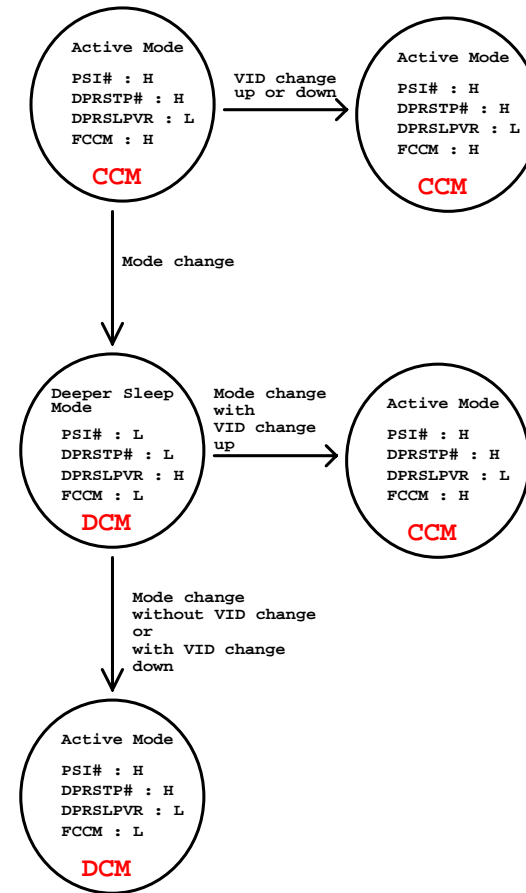
IMVP Spec. Rev. 0.8

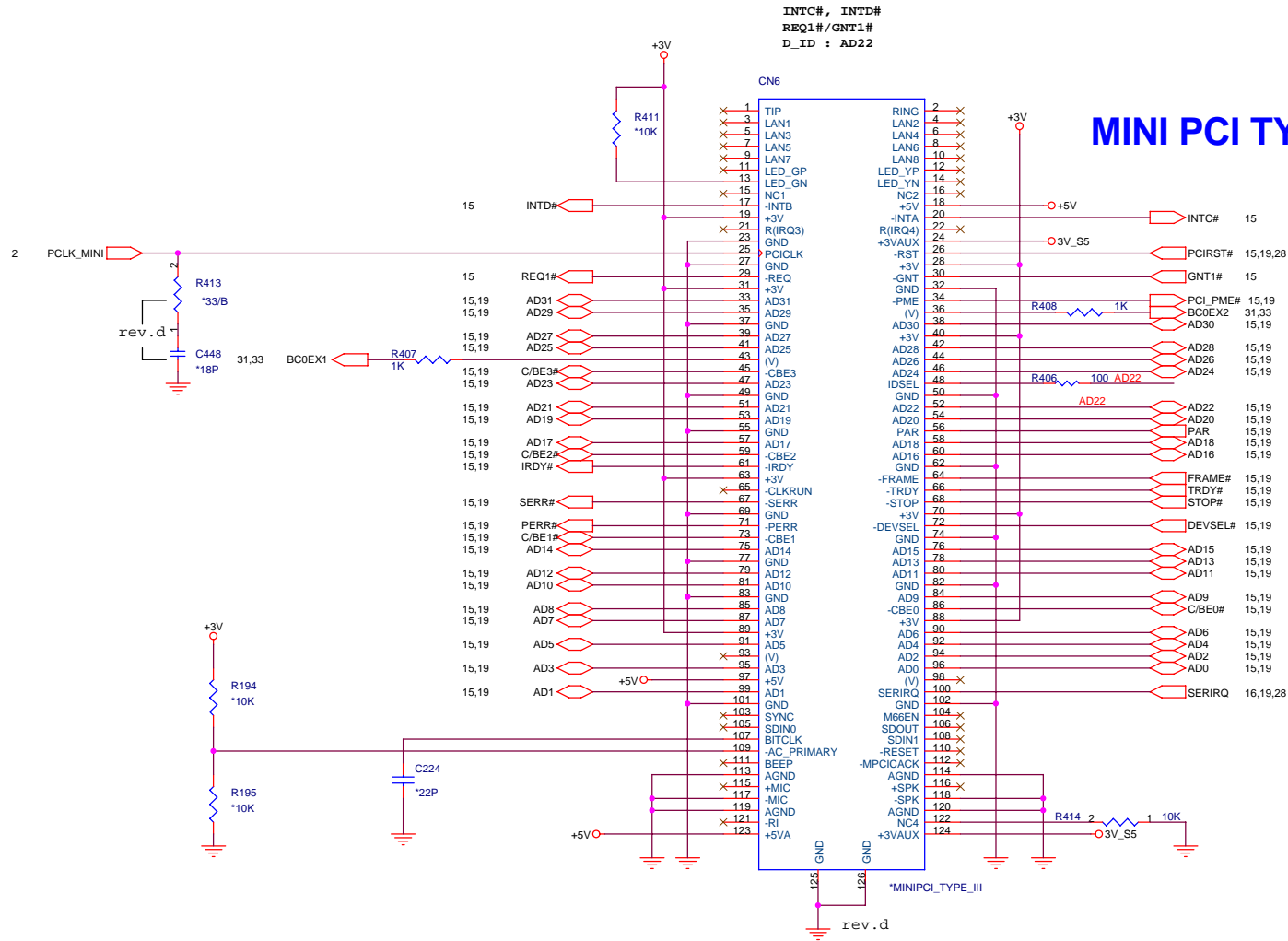
(Nom.)	Yonah-2M	Meron
HFM	1.2875 V	1.1500 V
LFM	0.8375 V	0.8375 V
Deeper	0.7625 V	0.7625 V
VBOOT	1.2000 V	1.2000 V
SLOPE	-2.1 mV/A	-2.1 mV/A

(Max.)	Yonah-2M	Meron
HFM	36 A	44 A
LFM	9.5 A	12.5 A
Deeper	3.5 A	5.5 A
Dynamic	27 A	34.5 A
TDC	26 A	32 A

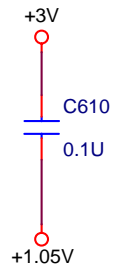
V _o	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

CCM : Continuous Conduction Mode
DCM : Dis-Continuous Mode





MINI PCI TYPE III SLOT



PROJECT : CT6
Quanta Computer Inc.

Size A	Document Number TPM	Rev 1A
Date: Friday, September 23, 2005		Sheet 42 of 44

MODEL

REV

CHANGE LIST

CT6
MB
31CT6MBXXXX

1A

Model CT6 MB BOARD

Page	FROM	TO
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
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33	1A	
34	1A	
35	1A	
36	1A	
37	1A	
38	1A	
39	1A	
40	1A	
41	1A	
42	1A	
43	1A	
44	1A	



PROJECT : CT6
Quanta Computer Inc.

**31 BOM difference list (base on
31CT6MB0008 BOM)**

31CT6MB0008

Pavilion FF

31CT6MB0024


**Pavilion
FF+Camera/Mic**

ADD :
 1.CN30 }
 2.CN31 } for camera connector
 3.CN32 }
 4.CN29 } → for internal MIC connector

31CT6MB0016

Presario FF

ADD:	REMOVE:
LED 9 -- PWR_LED	IR1--- IR component
LED 8 --SATA_LED	LED13--PWR_LED
LED 7 --MBATLED	LED12 --SATA_LED
LED4 --TP_LED	LED11 --MBAT_LED
LED2 --CAPD_LED	C532 -- IR
LED6 --CARD_LED	R521 -- IR
SW7 -- TP_R SWITCH	CN22 -- AV BOARD
SW6 -- TP_L SWITCH	CN26 -- 2ND H/P CON
	LED5 -- CARD LED
	LED3 -- TP_LED
	LED2 -- CAPS_LED
	LED1 -- PWR_LED
	C267 -- AV BOARD EMI
	C264 -- AV BOARD EMI
	C260 -- AV BOARD EMI
	C275 -- 2ND H/P EMI
	C272 -- 2ND H/P EMI
	R241 --2ND H/P damp res
	R235 --2ND H/P damp res
	R1 -- PWR RES
	SW5 -TP_R SWITCH
	SW4 -- TP_L SWITCH
	SW2-NBWON# SWITCH

 PROJECT : CT6 Quanta Computer Inc.		Rev
		1A
Size	Document Number	change list
B		
Date:	Friday, September 23, 2005	Sheet 44 of 44

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