

MODEL	REV	CHANGE LIST	Model	CT3/5 MB BOARD	
			Page	FROM	TO
CT3/5 MB 31CT3MB0015 31CT3MB0031	1A	<p>PAGE 2 --- Enable CLK48M from clokc generator for the PLL circuit of 7411, and disable the ocsillator circuit of PCI7411 PLL.</p> <p>PAGE 3 --- Remove H/W shutdown circuit that supported ADM1032.</p> <p>PAGE 4 --- Use X7R type to replace Y5V type for CPU Decoupling/Bypass capacitor.</p> <p>PAGE 10 --- Add a terminal resistor R706 for -CODE_RST# to improve signal quality.</p> <p>PAGE 11 --- 1. Add a 10K pull-up resistor on MCH_SYNC# for booting. 2. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue. 3. Change the power plane of ICH_THRM# and SCI_# from 3VSUS to +3V to reduce leakage.</p> <p>PAGE 12 --- We can also use 5VSUS to instead of 5V_S5 to save cost of MOSFET(A06402).</p> <p>PAGE 15 --- Add a level-shift cicuit for EDID interface.</p> <p>PAGE 17 --- 1. Add a off-page and a EMI solution for CLK48M. 2. Remove the reserve resistors (R693-R695) of parallel interface for PCI1510.</p> <p>PAGE 18 --- Remove R696, connect controller and power switch directly .</p> <p>PAGE 19 --- Change R682&R683 value from 56 ohms to 0 ohm cause of BOM error at A-test.</p> <p>PAGE 22 --- 1. Change MC3 type from Y5V to X7R to improve singal quality. 2. Connect H1/H3 to AGND via a 0 ohm resistor by Conexant's comment.</p> <p>PAGE 23 --- 1. Add a terminal resistor R707 for RTL8100/8110 id selection. 2. Add a 0.1uF to make Q40 turn on slowly to aviod 3VPCU drop issue.</p> <p>PAGE 24 --- Modified transformer circuit cause of CT can't connect each other on 10/100M application.</p> <p>PAGE 26 --- Add a flashrom as PLCC32 type for BIOS debugging.</p> <p>PAGE 27 --- 1. Change R352 value from 120K ohms to 20M ohms. 2. Add a LPC debug port for software team to debug convenient.</p> <p>PAGE 30 --- Add GMT fan controller for B-test to costdown.</p> <p>PAGE 31 --- 1. Add ESD protection circuit for S-VIDEO signal to Docking. 2. Add R713 to enable the mux in the Tampa-2 cable</p> <p>PAGE 33 --- Change PR143 value from 100K to 10K to solve display abnormal issue.</p> <p>PAGE 35 --- 1. Move 5V_S5 circuit to Page 36. 2. De-popuplate PQ129 and PR182. 3. Change PR178 value from 22 ohm to 47 ohm.</p> <p>PAGE 36 --- Remove PC170 and PQ127 but reserve 5V_S5 power circuit.</p>	1	1A	
			2	1A	2A
			3	1A	2A
			4	1A	2A
			5	1A	
			6	1A	
			7	1A	
			8	1A	
			9	1A	
			10	1A	2A
			11	1A	2A
			12	1A	2A
			13	1A	
			14	1A	
			15	1A	2A
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			17	1A	2A
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			35	1A	2A
			36	1A	2A
			37	1A	
			38	1A	
			39	1A	

MODEL

REV

CHANGE LIST

Model CT3/5 MB BOARD

CT3/5 MB
31CT3MB0015
31CT3MB0031

2A

PAGE 2 --- 1. Add C1048 for CLK48M to get better EMI performance.

PAGE 3 --- 1. Add R733 as pull-up resistor for FREQ#.

PAGE 11 --- 1. Add RF_OFF# and BT_OFF#

PAGE 17 --- 1. Populate R704 and C1046 to get better EMI performance.

2. Remove R701 & R702 for unused PCI1510RVGF circuit.

PAGE 18 --- 1. Disconnect SM_PHYS_WP on controller side.

2. Tie SM_EL_WP with SM_PHYS_WP on conn side to allow for normal operation of SD and SM.

3. Add a discharge circuit for media card power.

4. Add R718 to solve cross-talk issue of MS-Pro card.

5. Add R717 to solve SM card can't write protect issue.

6. Add R719~R736 as terminal on all multi-function pins.

7. Add pull-up circuit.

PAGE 27 --- 1. Reserve 0R for RF_OFF# and BT_OFF# circuit.

2. Modify LPC pin name.

PAGE 28 --- 1. Change HDD and ODD select definition.

PAGE 30 --- Adjust Capacitors and Bead to improve CRT timing issue.

1. Change L66, L67, L68 from BK1608HM470 to 0R.

2. Remove C931, C932, C933.

3. Change C934, C935, C936 from 22P to 5.6P.

4. Change C6, C14, C350 from 10P to 5.6P.

5. Change L1, L26, L27 from BK1608HM470 to BLM18BA750SN1T.

PAGE 31 --- 1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality.

2. Reserve S-video impedance match circuit.

Page	FROM	TO
1	1A	
2	2A	3A
3	2A	3A
4	2A	
5	1A	
6	1A	
7	1A	
8	1A	
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10	2A	
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12	1A	
13	1A	
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17	2A	3A
18	2A	3A
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39	2A	

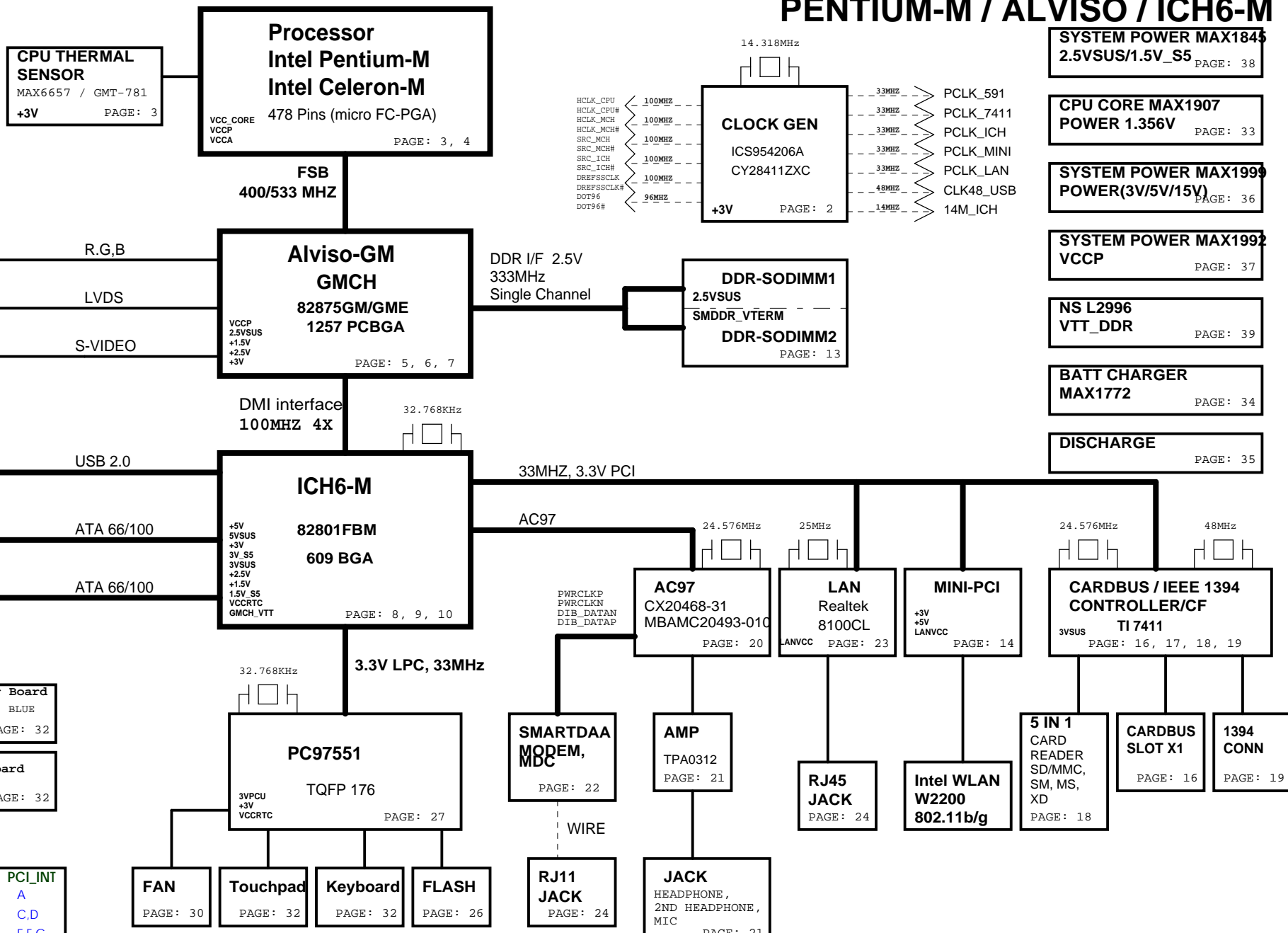
CT3 BLOCK DIAGRAM

PENTIUM-M / ALVISO / ICH6-M

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

PCB THICKNESS: 1.2mm



CPU THERMAL SENSOR
MAX6657 / GMT-781
+3V PAGE: 3

Processor
Intel Pentium-M
Intel Celeron-M
478 Pins (micro FC-PGA)
VCC_CORE
VCCP
VCCA PAGE: 3, 4

CLOCK GEN
ICS954206A
CY28411ZXC
+3V PAGE: 2

SYSTEM POWER MAX1845
2.5VSUS/1.5V_S5 PAGE: 38

CPU CORE MAX1907
POWER 1.356V PAGE: 33

SYSTEM POWER MAX1999
POWER(3V/5V/15V) PAGE: 36

SYSTEM POWER MAX1992
VCCP PAGE: 37

NS L2996
VTT_DDR PAGE: 39

BATT CHARGER
MAX1772 PAGE: 34

DISCHARGE
PAGE: 35

CRT port PAGE: 30

LCD Panel PAGE: 15

MINI-DIN PAGE: 32

USB PORT 0, 1 PAGE: 19

1st IDE - HDD PAGE: 28

2nd IDE - CDROM PAGE: 28

CABLE DOCK PAGE: 31

Daughter Board
TV, USB, BLUE TOOTH PAGE: 32

AV BOARD PAGE: 32

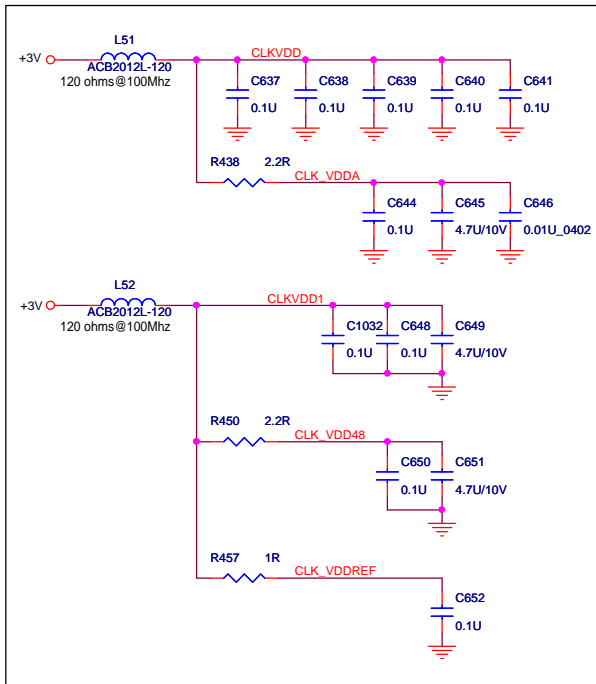
Power Board PAGE: 32

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET	AD16	2	A
MINIPCI SLOT	AD22	1	C,D
CardBus/1394	AD25	0	E,F,G

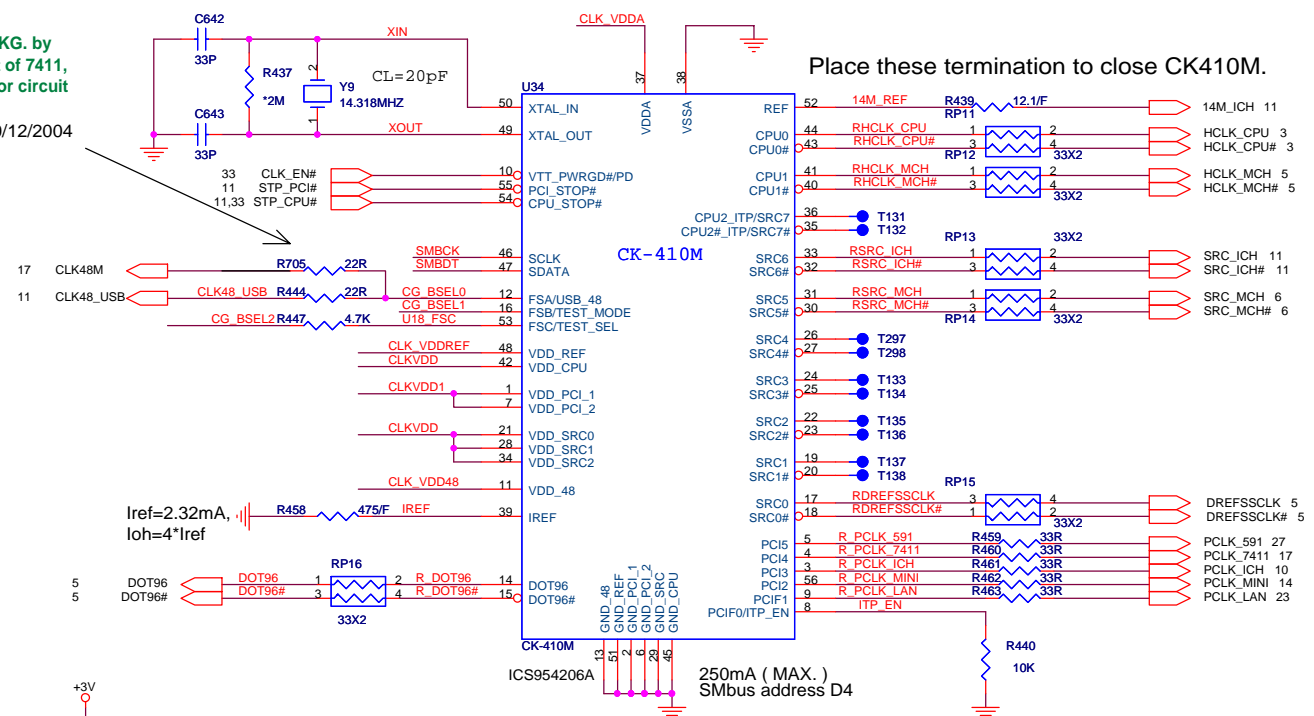
PROJECT : CT3
Quanta Computer Inc.

Size Custom Document Number BLOCK DIAGRAM Rev 1A
Date: Monday, December 27, 2004 Sheet 1 of 39



SI stage:
 Enable CLK48M from CKG. by
 R705 for the PLL circuit of 7411,
 and disable the oscillator circuit
 at PCI7411 side.

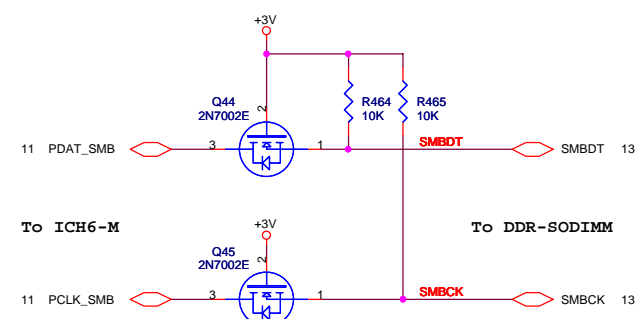
Sting 10/12/2004



Place these termination to close CK410M.

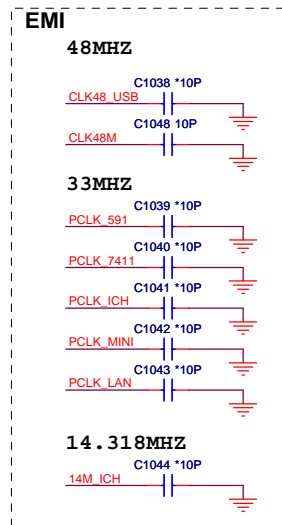
FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	DOTHAN FSB 400
0	0	1	133	100	33	DOTHAN FSB 533
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			

* Frequency select by CPU auto sense.

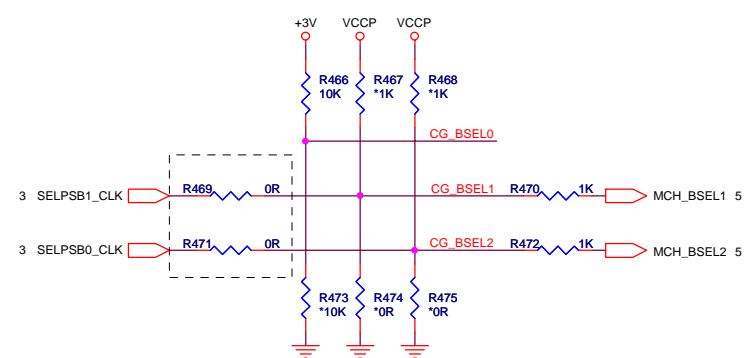


PV stage:
 Add C1048 for CLK48M to get better EMI
 performance.

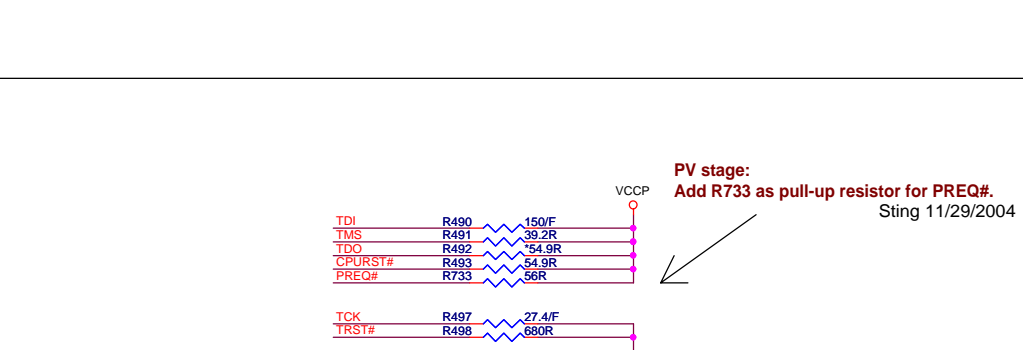
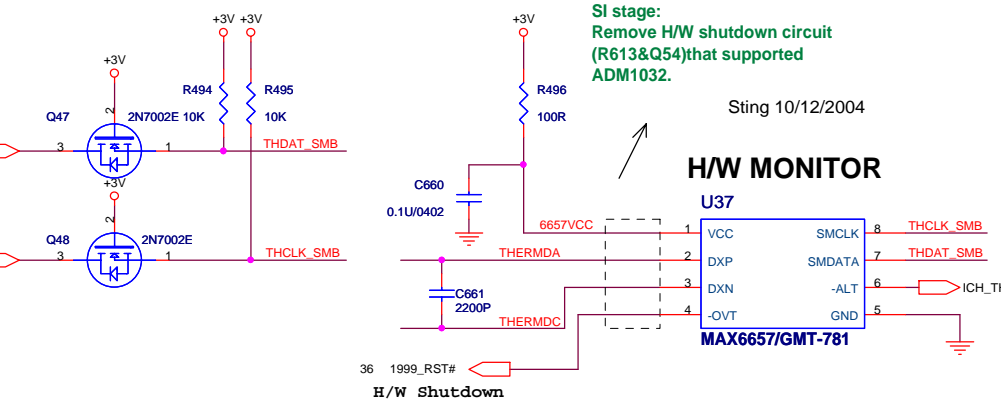
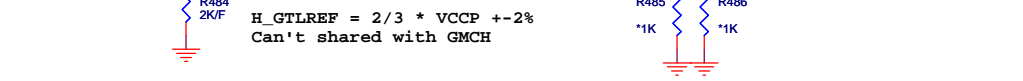
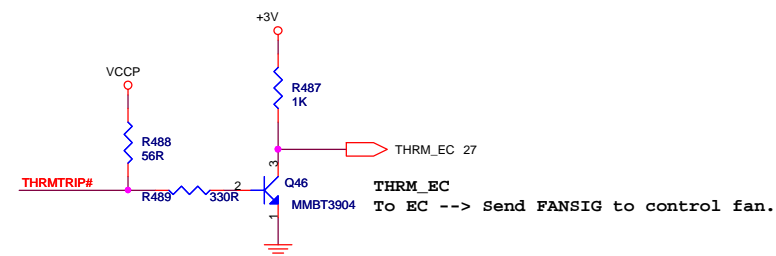
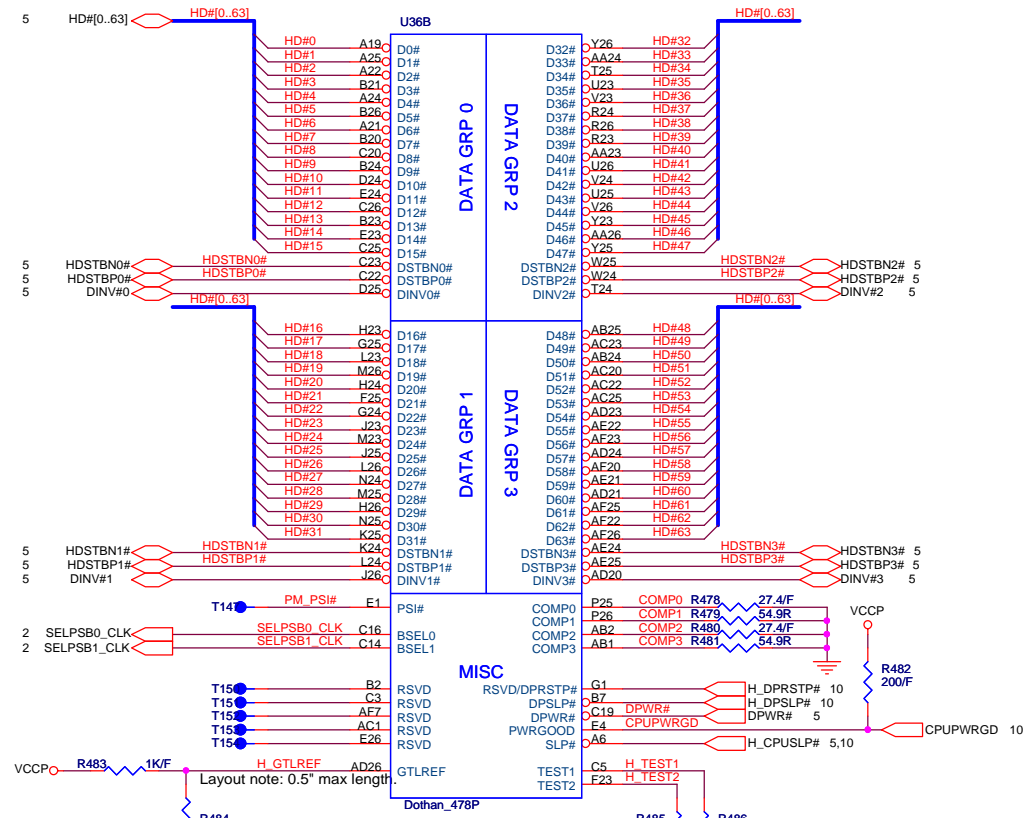
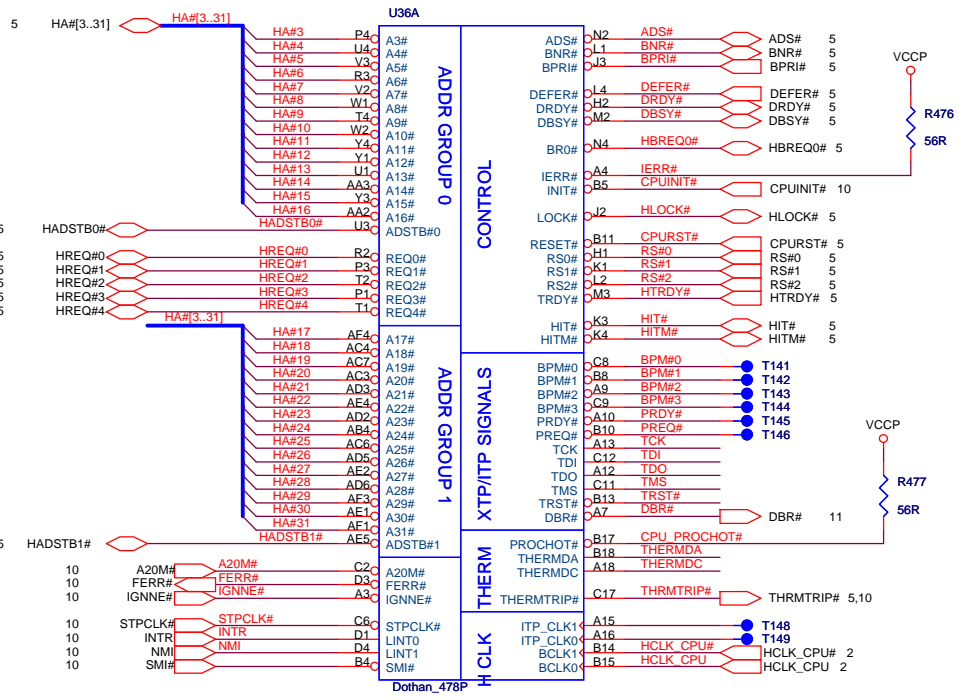
Sting 11/29/2004

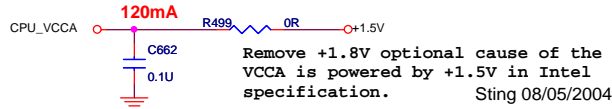
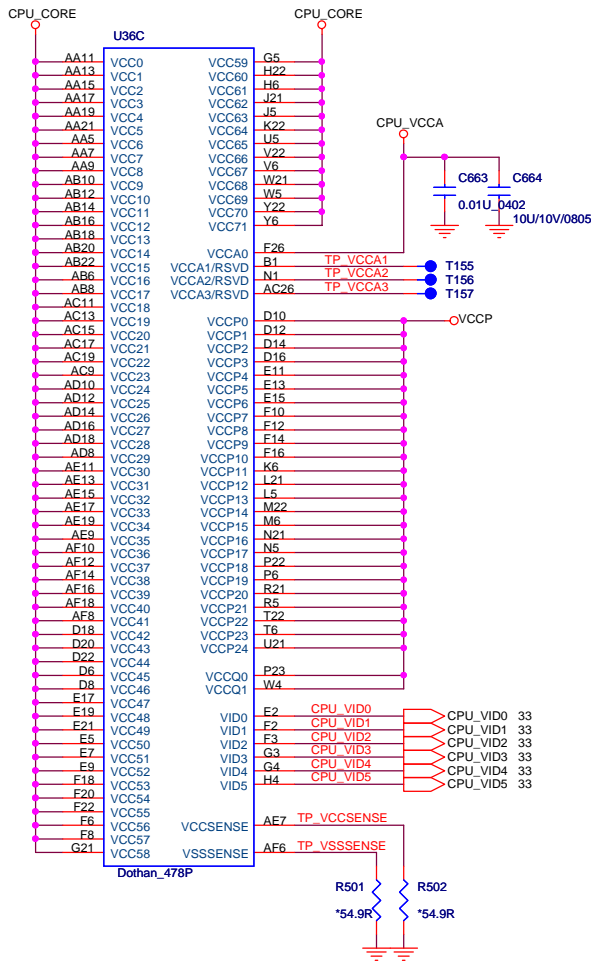


R_PCLK_LAN ITP_EN
 0: SRCLK=96MHZ 0: SRC_7 Pair
 1: SRCLK=100MHZ 1: CPU_2 ITP Pair

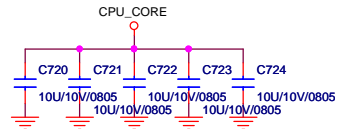
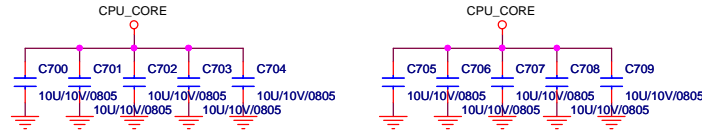
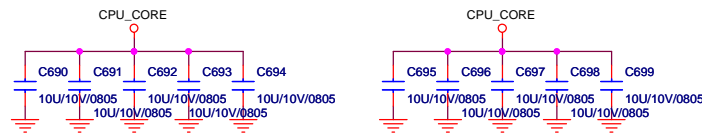
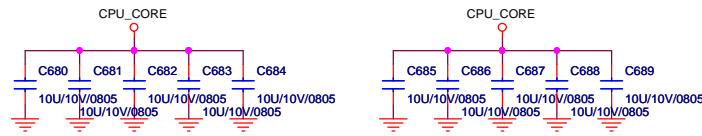
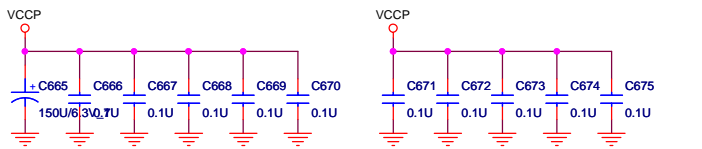


R469, R471
 Dothan-A can remove so that the FSB frequency will be selected by
 hardware setting (R474, R475, R467, R468).
 Dothan-B should be populated.

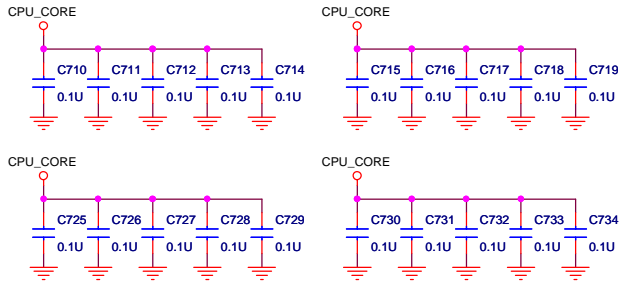




SI stage:
Use X7R type to replace Y5V type for Decoupling/Bypass capacitor.
Sting 10/12/2004

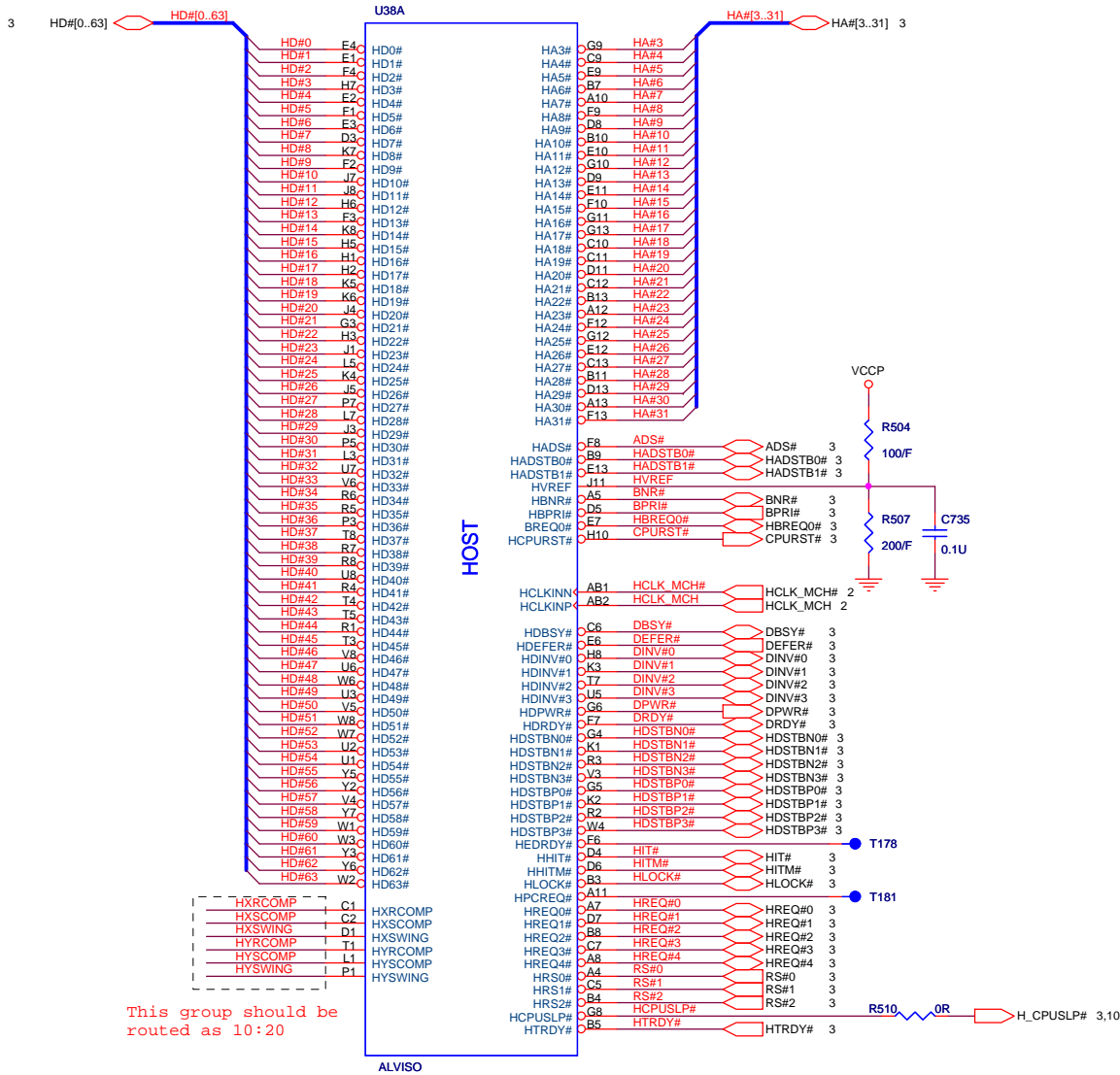


CPU de-coupling capacitor

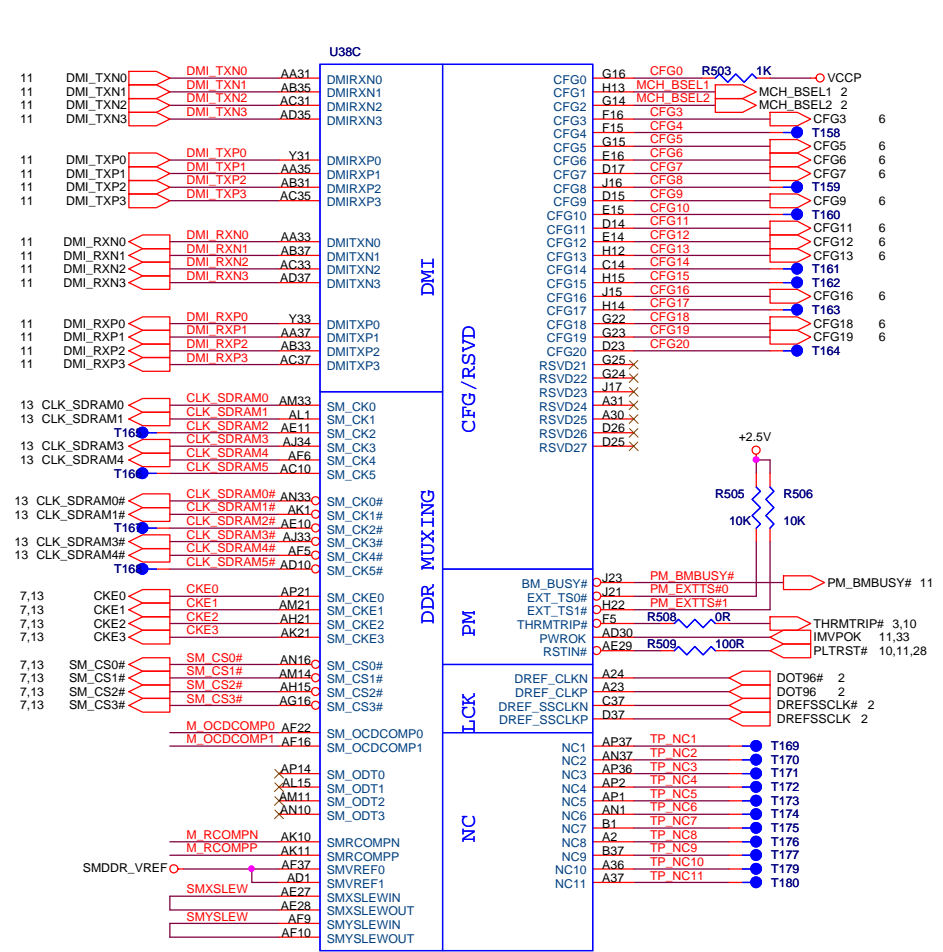


CPU Bypass capacitor

A2	VSS0	D13
A5	VSS1	D15
A8	VSS2	D17
A11	VSS3	D19
A14	VSS4	D21
A17	VSS5	D23
A20	VSS6	D26
A23	VSS7	E3
A26	VSS8	E5
AA1	VSS9	E8
AA4	VSS10	E10
AA6	VSS11	E12
AA8	VSS12	E14
AA10	VSS13	E16
AA12	VSS14	E18
AA14	VSS15	E20
AA16	VSS16	E22
AA18	VSS17	E25
AA20	VSS18	F1
AA22	VSS19	F4
AA25	VSS20	F7
AB3	VSS21	F9
AB5	VSS22	F11
AB7	VSS23	F13
AB9	VSS24	F15
AB11	VSS25	F17
AB13	VSS26	F19
AB15	VSS27	F21
AB17	VSS28	F24
AB19	VSS29	G2
AB23	VSS30	G6
AB26	VSS31	G22
AC2	VSS32	G23
AC5	VSS33	G26
AC8	VSS34	H3
AC10	VSS35	H5
AC12	VSS36	H21
AC14	VSS37	H25
AC16	VSS38	J1
AC18	VSS39	J4
AC21	VSS40	J6
AC24	VSS41	J22
AD1	VSS42	J24
AD4	VSS43	K2
AD7	VSS44	K5
AD9	VSS45	K21
AD11	VSS46	K23
AD13	VSS47	K26
AD15	VSS48	L3
AD17	VSS49	L6
AD19	VSS50	L22
AD22	VSS51	L25
AD25	VSS52	M1
AE3	VSS53	M4
AE6	VSS54	M5
AE8	VSS55	M21
AE10	VSS56	M24
AE12	VSS57	N6
AE14	VSS58	N6
AE16	VSS59	N22
AE18	VSS60	N23
AE20	VSS61	N26
AE23	VSS62	P2
AE26	VSS63	P5
AF2	VSS64	P21
AF5	VSS65	P24
AF9	VSS66	R1
AF11	VSS67	R4
AF12	VSS68	R6
AF13	VSS69	R22
AF15	VSS70	R25
AF17	VSS71	T3
AF19	VSS72	T5
AF21	VSS73	T21
AF24	VSS74	T23
B3	VSS75	T26
B6	VSS76	U2
B9	VSS77	U2
B12	VSS78	U6
B16	VSS79	U22
B19	VSS80	U24
B22	VSS81	V1
B25	VSS82	V4
C1	VSS83	V5
C4	VSS84	V21
C7	VSS85	V25
C10	VSS86	W3
C15	VSS87	W22
C18	VSS88	W23
C21	VSS89	W26
C24	VSS90	Y2
D2	VSS91	Y5
D5	VSS92	Y21
D7	VSS93	Y24
D9	VSS94	
D11	VSS95	
	VSS96	

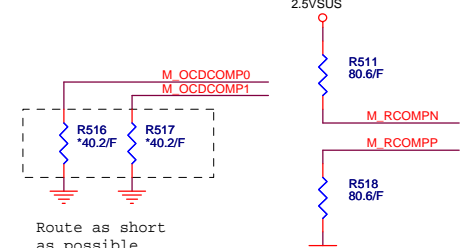
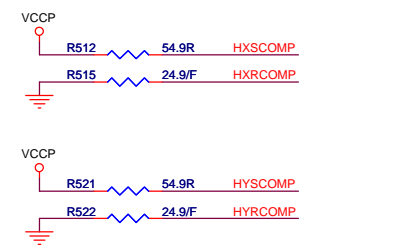
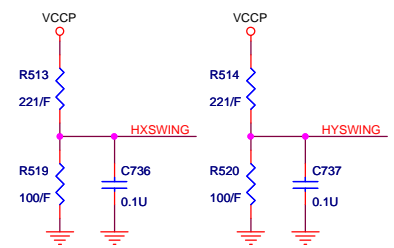


This group should be routed as 10:20




It's point to point, 55ohm trace, keep as short as possible.

ALVISO

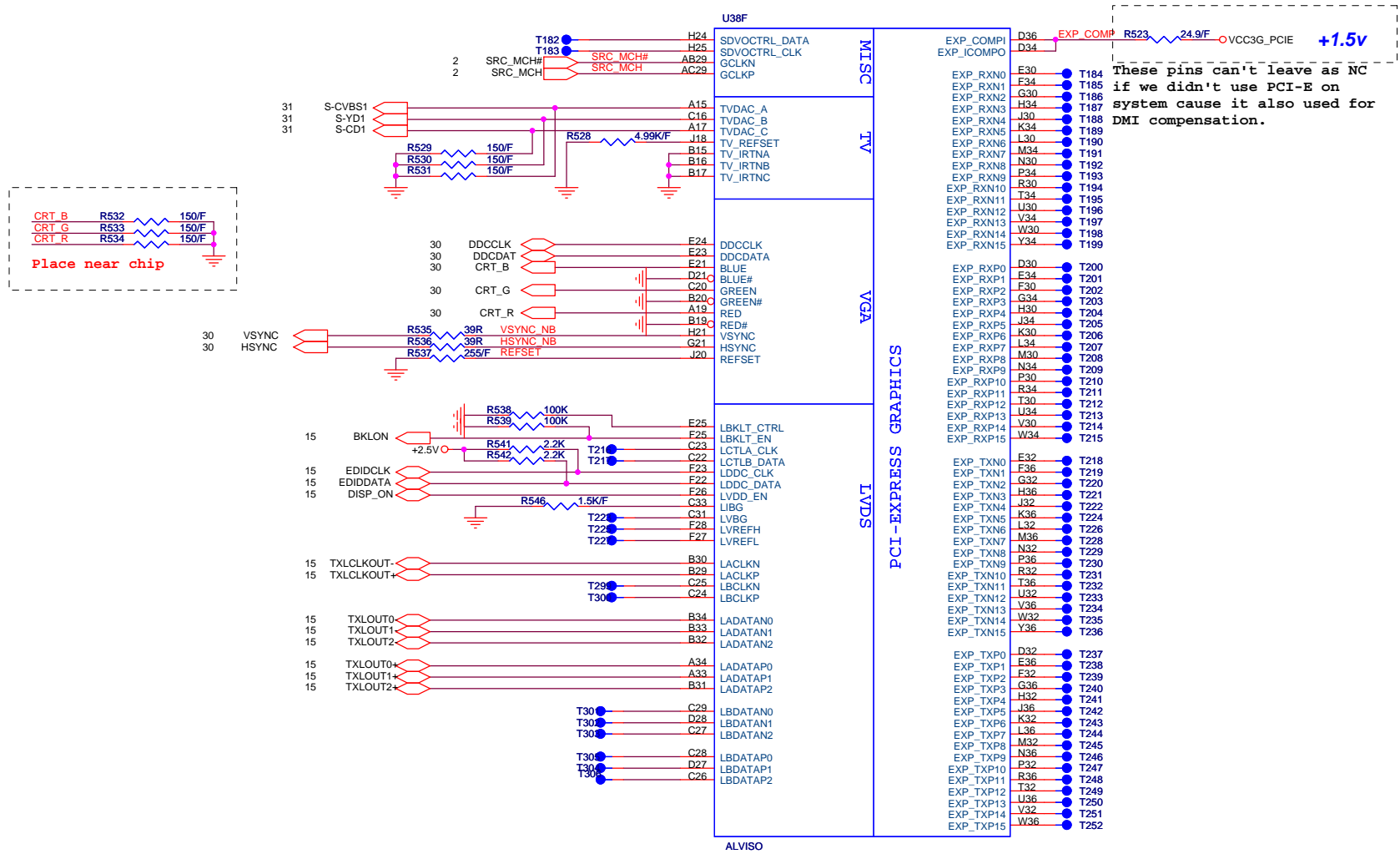


Route as short as possible.

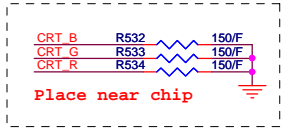


PROJECT : CT3
Quanta Computer Inc.

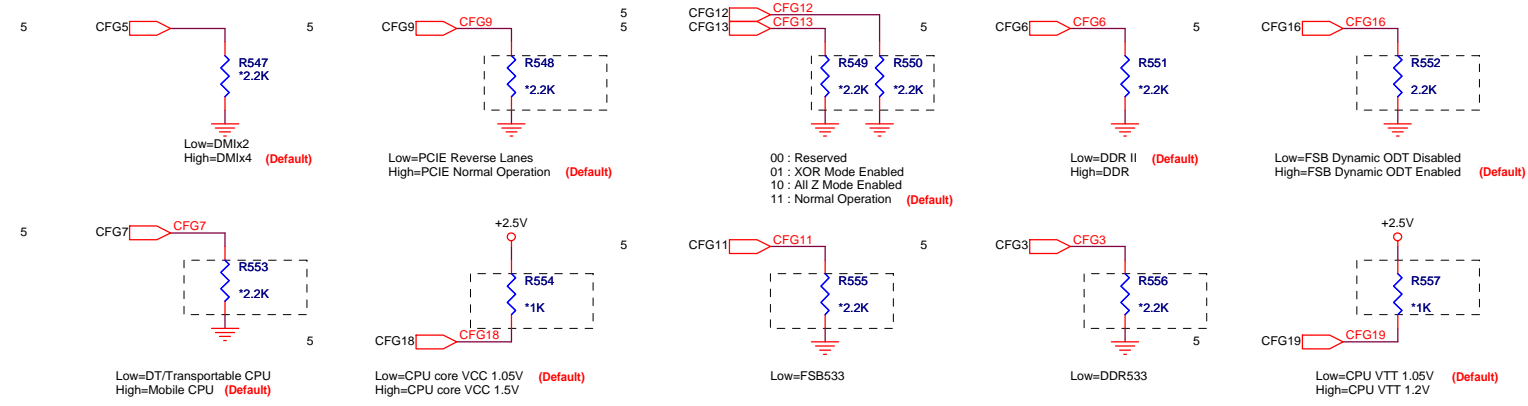
Size	Document Number	Rev	1A
Custom	ALVISO-Host		
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These pins can't leave as NC if we didn't use PCI-E on system cause it also used for DMI compensation.



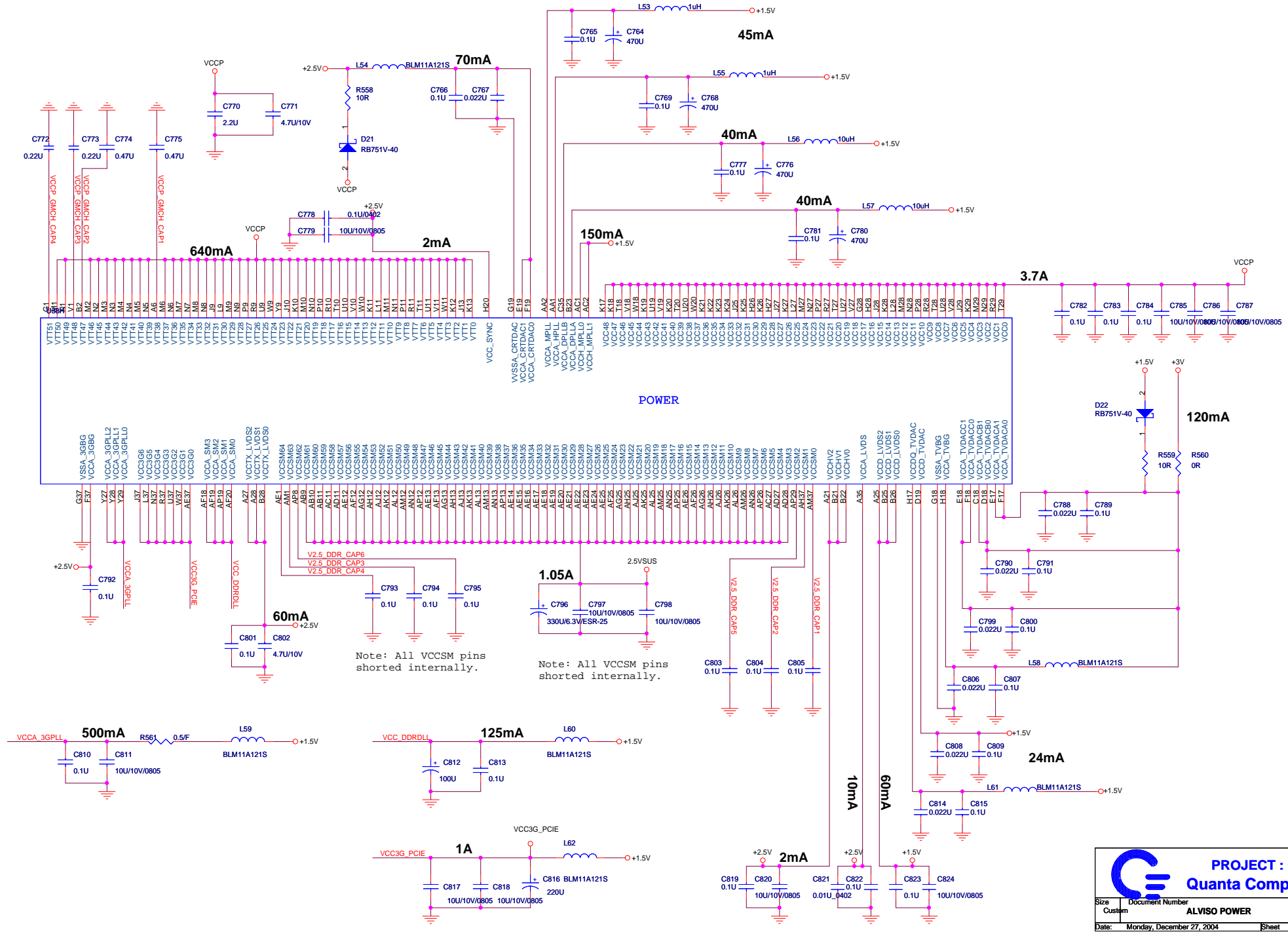
Strapping




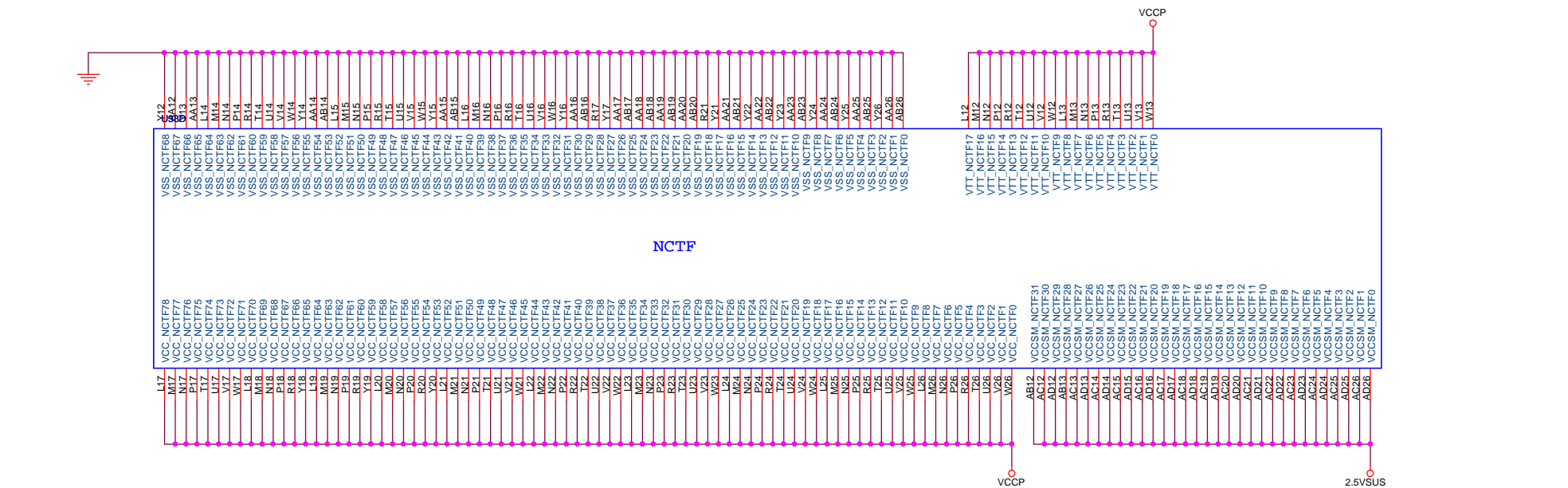
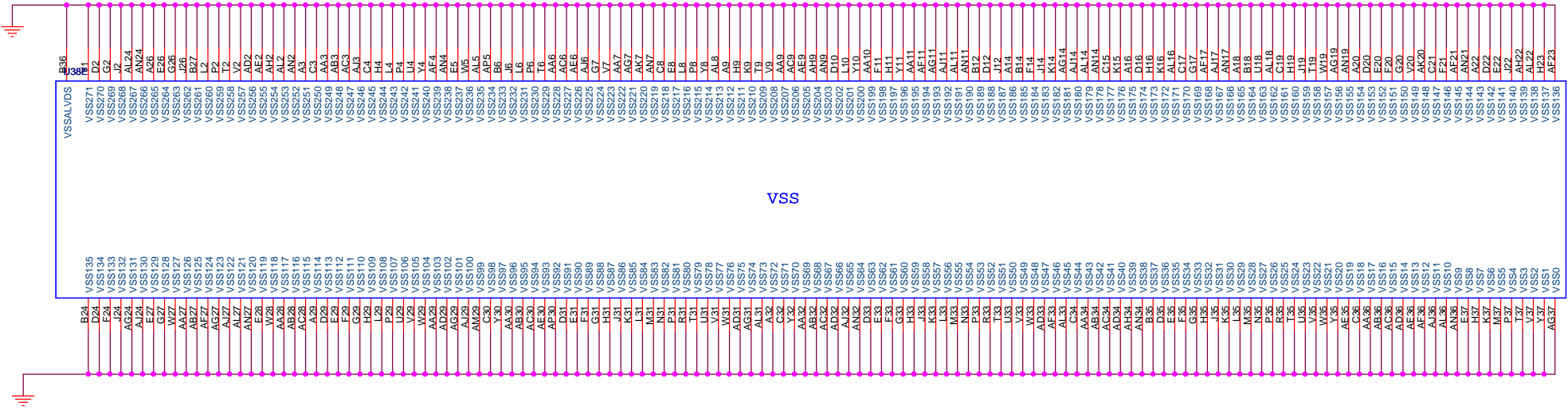
CFG[2:0]
 001=533MT/S FSB
 101=400MT/S FSB
 CFG[3:17] have internal pullup.
 CFG[18:19] have internal pulldown.

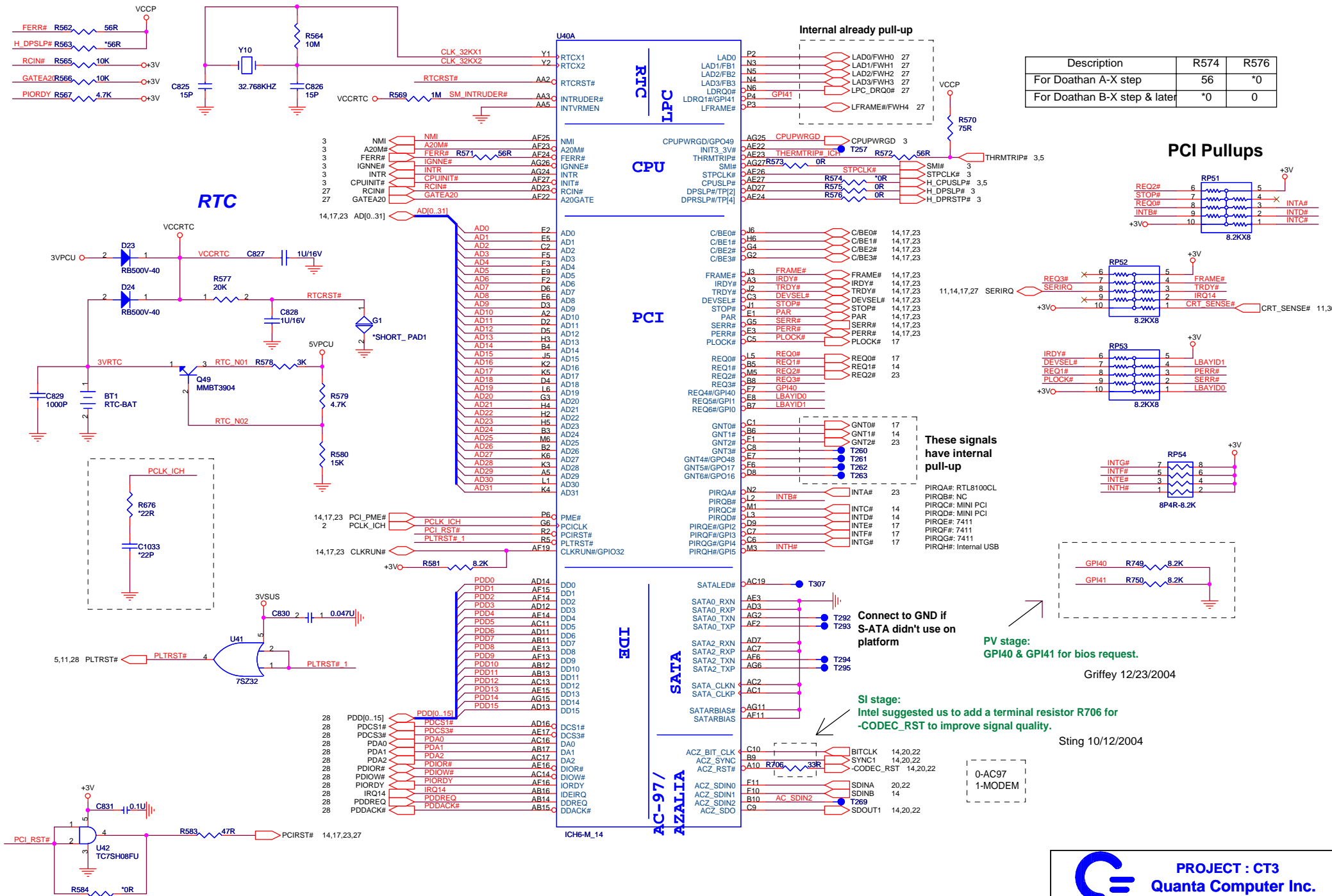
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALVISO DMI	1A
Date:	Monday, December 27, 2004	Sheet 6 of 39

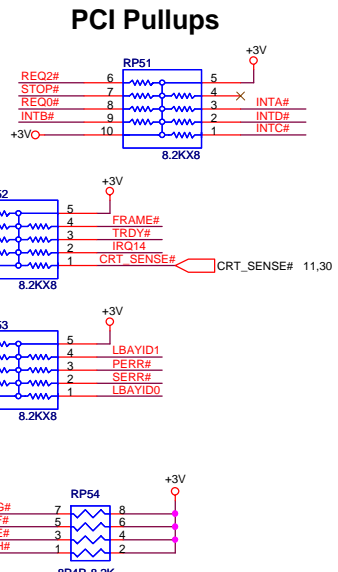


		PROJECT : CT3	
		Quanta Computer Inc.	
Size	Document Number	ALVISO POWER	
Custom			
Date:	Monday, December 27, 2004	Sheet	8 of 39
			Rev 1A





Description	R574	R576
For Doathan A-X step	56	*0
For Doathan B-X step & later	*0	0



These signals have internal pull-up

- PIRQA#: RTL8100CL
- PIRQB#: NC
- PIRQC#: MINI PCI
- PIRQD#: MINI PCI
- PIROE#: 7411
- PIROF#: 7411
- PIROG#: 7411
- PIROH#: Internal USB

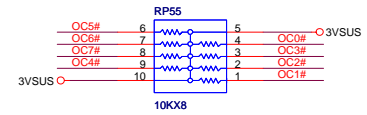
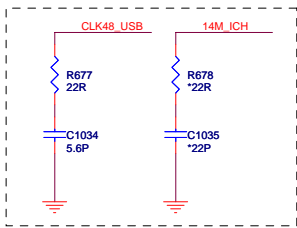
PV stage: GPI40 & GPI41 for bios request.
Griffey 12/23/2004

Connect to GND if S-ATA didn't use on platform

SI stage: Intel suggested us to add a terminal resistor R706 for -CODEC_RST to improve signal quality.
Sting 10/12/2004

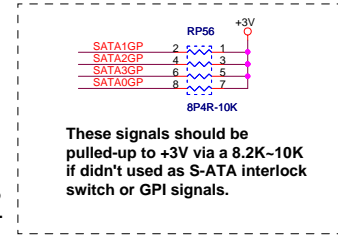
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH6-M (CPU/PC/IDE)	2A
Date:	Monday, December 27, 2004	Sheet 10 of 39

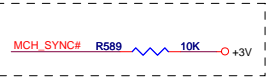


Place within 500mils of ICH-6

Place within 500mils of ICH-6

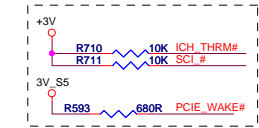
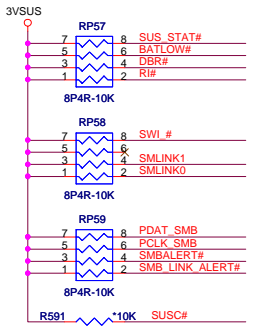
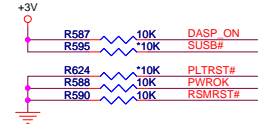


LAN_RST# should be connected to PLTRST# if internal LAN didn't use.



SI stage:
R589 should be populated, because MCH_SYNC# is internally ANDed with PWROK. System will not booting without this pulled-up resistor.

Sting 09/24/2004

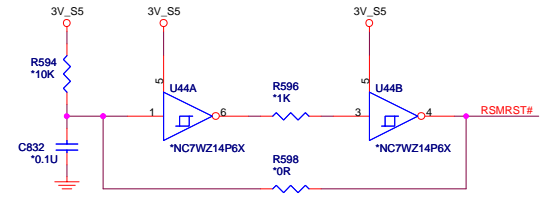


1. Change the power plane of PCIE_WAKE# from 3VSUS to 3V_S5 to solve system can't turn off issue.
2. Change the power plane of ICH_THRM# and SCTI_# from 3VSUS to +3V to solve leakage issue.

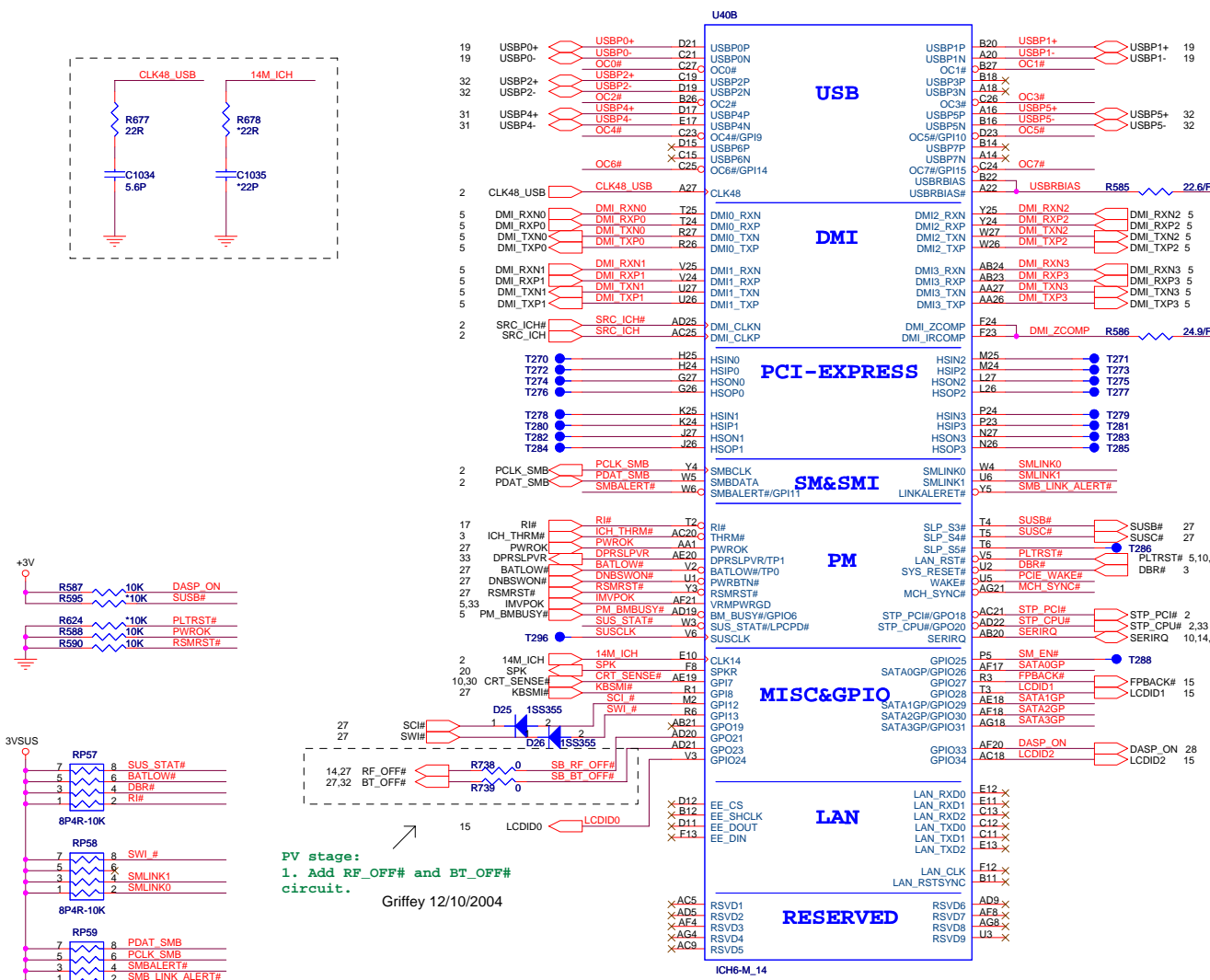
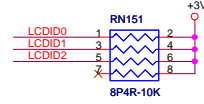
Sting 10/06/2004

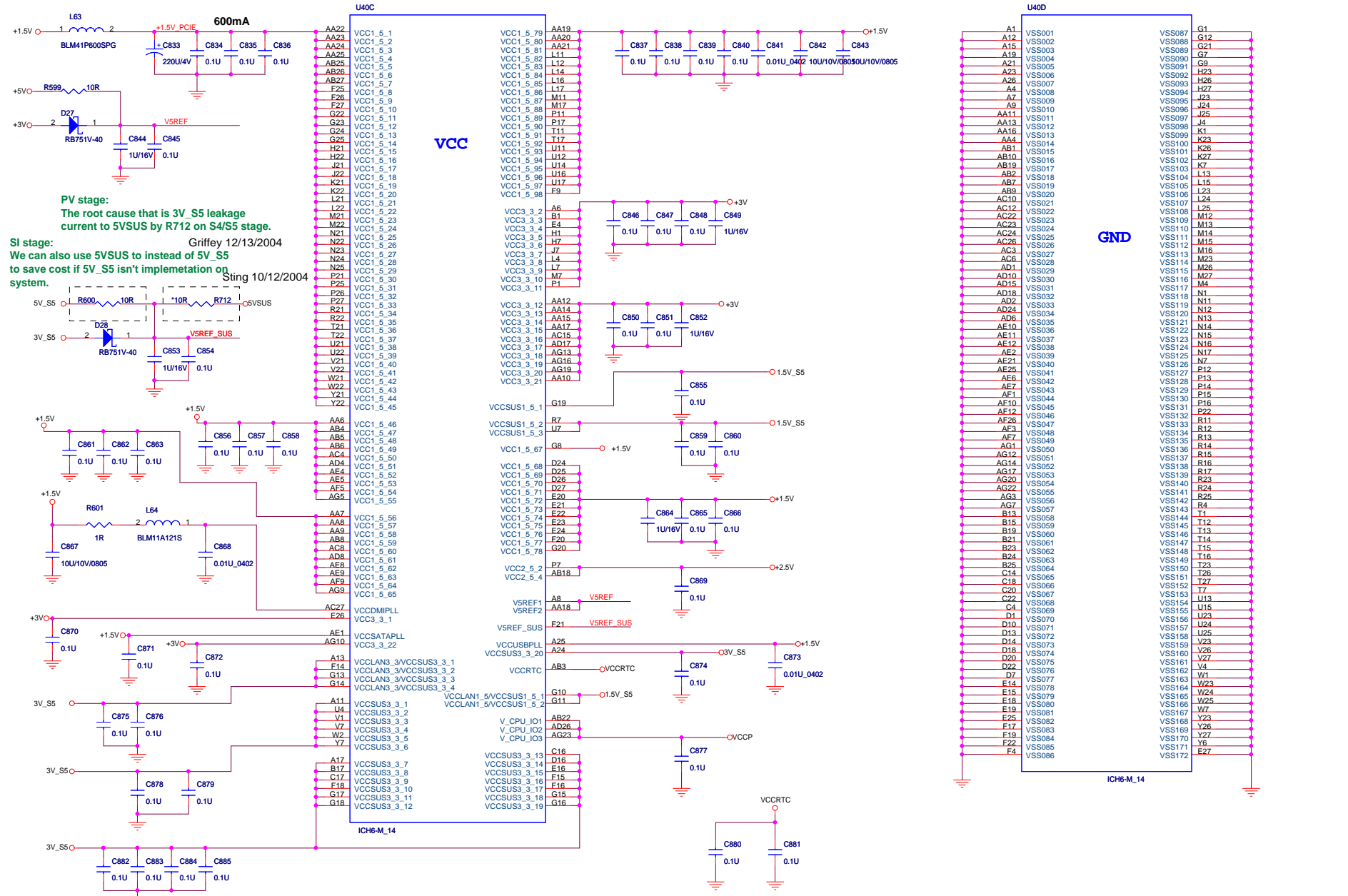
PV stage:
1. Add RF_OFF# and BT_OFF# circuit.

Griffey 12/10/2004



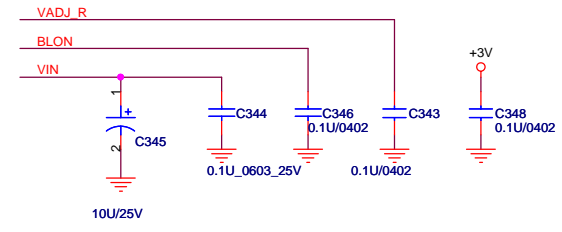
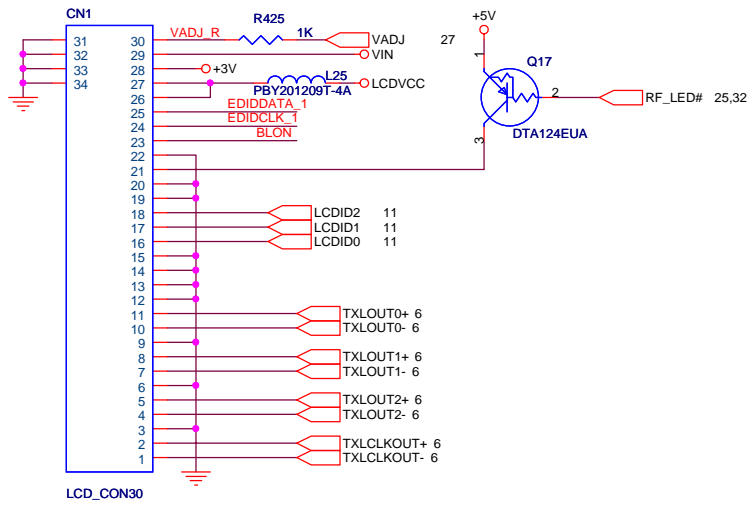
Enable Cable ID



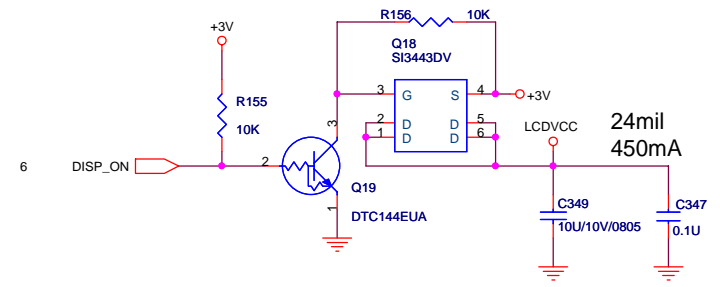
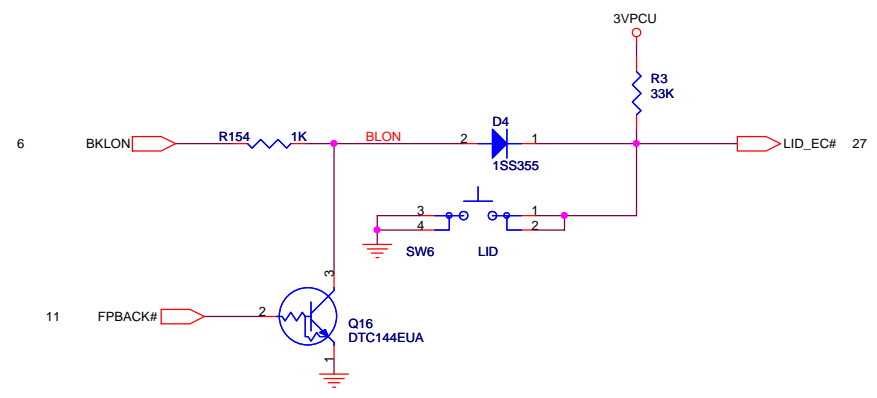
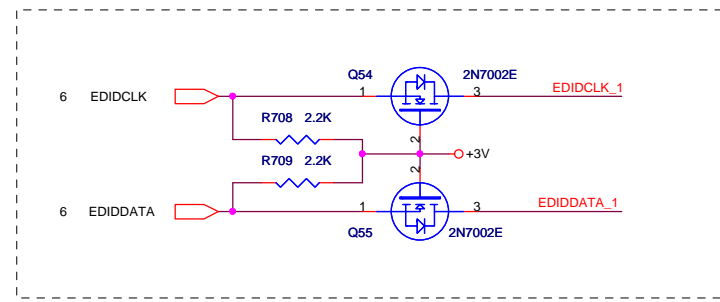


PV stage:
 The root cause that is 3V_S5 leakage current to 5VSUS by R712 on S4/S5 stage.
 Griffey 12/13/2004

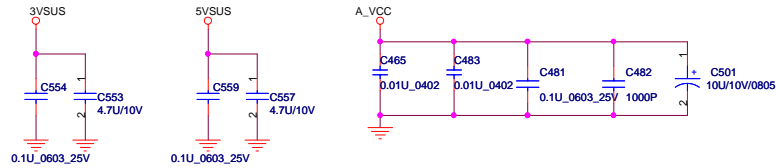
SI stage:
 We can also use 5VSUS to instead of 5V_S5 to save cost if 5V_S5 isn't implementation on system.
 Sting 10/12/2004



SI stage:
 Add a level-shift circuit for EDID interface.
 Sting 10/04/2004

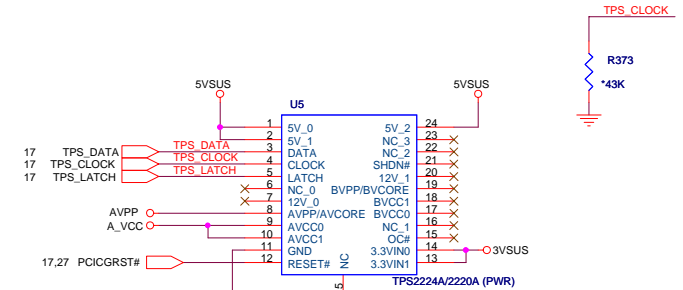


CardBus Connector

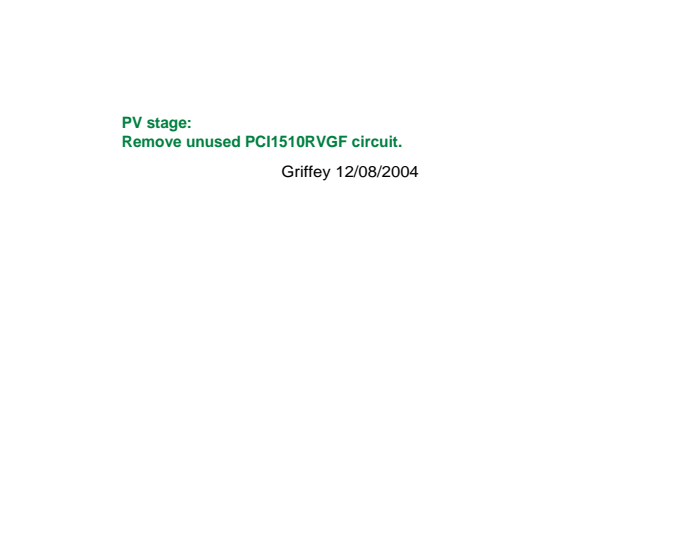


CARDBUS POWER SWITCH

For PCI7411



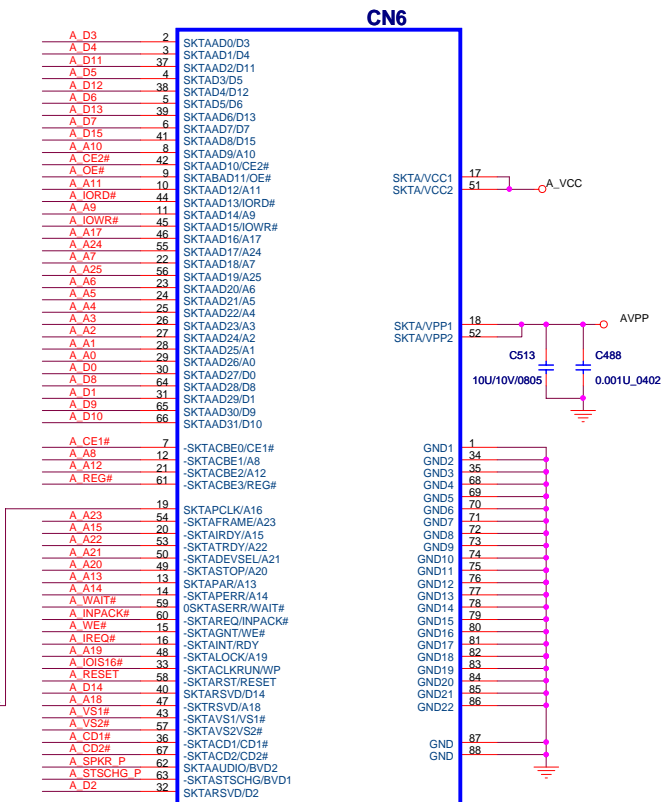
For PCI1510



PV stage:
Remove unused PCI1510RVGF circuit.
Griffey 12/08/2004

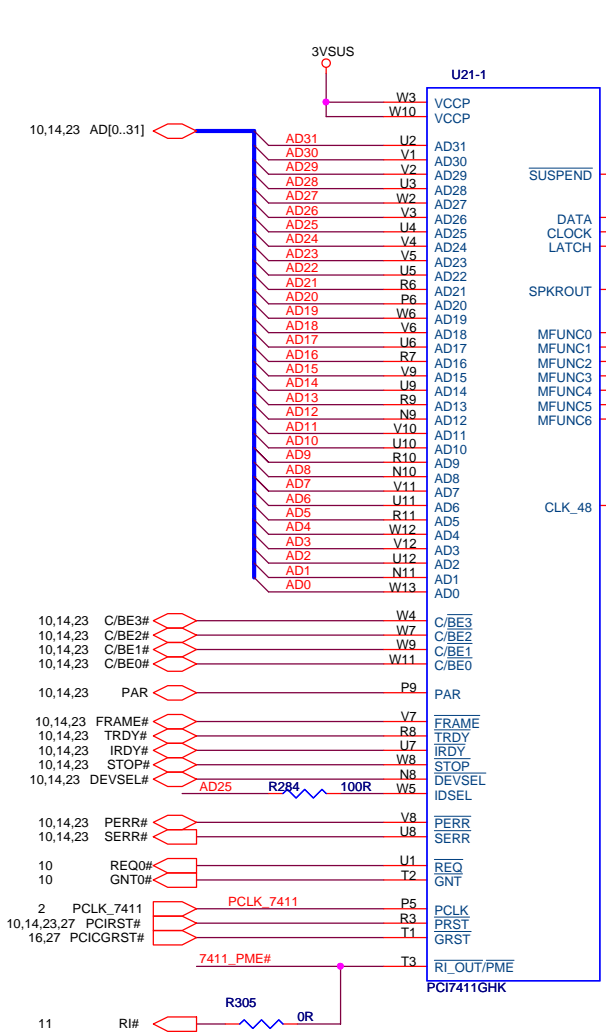
U21-3	Pin	Signal
	VCCB	D19
	VCCB	K19
B_CAD31/B	D10	B15
B_CAD30/B	D9	A16
B_CAD29/B	D8	B16
B_CAD28/B	D8	C16
B_CAD27/B	D0	D17
B_CAD26/B	A0	D18
B_CAD25/B	A1	E17
B_CAD24/B	A2	E18
B_CAD23/B	A3	E19
B_CAD22/B	A4	G15
B_CAD21/B	A5	H14
B_CAD20/B	A6	H15
B_CAD19/B	A25	G17
B_CAD18/B	A7	G17
B_CAD17/B	A24	K17
B_CAD16/B	A17	L13
B_CAD15/B	IOWR	L13
B_CAD14/B	A9	L15
B_CAD13/B	IORD	L17
B_CAD12/B	A11	L18
B_CAD11/B	OE	L18
B_CAD10/B	CE2	M17
B_CAD9/B	A10	M14
B_CAD8/B	D15	M14
B_CAD7/B	D7	M15
B_CAD6/B	D13	N18
B_CAD5/B	D6	N15
B_CAD4/B	D12	M13
B_CAD3/B	D5	P16
B_CAD2/B	D11	P17
B_CAD1/B	D4	P19
B_CAD0/B	D3	F15
B_CC/BE3/B	REG	G19
B_CC/BE2/B	A12	K14
B_CC/BE1/B	A8	M18
B_CC/BE0/B	CE1	K13
B_CPAR/A	A13	G19
B_CFRAME/B	A23	H17
B_CTRDY/B	A22	J13
B_CIRDY/B	A15	J17
B_CSTOP/B	A20	H19
B_CDEVSEL/B	A21	J19
B_CBLOCK/B	A19	J18
B_CPERR/B	A14	B18
B_CSERR/B	WAIT	E18
B_CREQ/B	INPACK	J15
B_CGNT/B	WE	F14
B_CSTSCHG/B	BVD1(STSCHG/R)	A18
B_CCLKRUN/B	WP(OIS16)	H18
B_CCLK/B	A16	B19
B_CINT/B	READY(IREQ)	F17
B_CRST/B	RESET	C17
B_CAUDIO/B	BVD2(SPKR)	N13
B_CCD1/B	CDT	B17
B_CCD2/B	CD2	C18
B_CVS1/B	VS1	F19
B_CVS2/B	VS2	N17
B_RSVD/B	D14	A15
B_RSVD/B	D2	K15
B_RSVD/B	A18	

U21-2	Pin	Signal
	VCCA	A5
	VCCA	A11
A_CAD31/A	D10	D1
A_CAD30/A	D9	C1
A_CAD29/A	D1	D3
A_CAD28/A	D8	B1
A_CAD27/A	D0	A4
A_CAD26/A	A0	B4
A_CAD25/A	A1	A4
A_CAD24/A	A2	B5
A_CAD23/A	A3	C6
A_CAD22/A	A4	B6
A_CAD21/A	A5	G9
A_CAD20/A	A6	C7
A_CAD19/A	A25	B7
A_CAD18/A	A7	A7
A_CAD17/A	A24	A7
A_CAD16/A	A17	A10
A_CAD15/A	IOWR	E11
A_CAD14/A	A9	G11
A_CAD13/A	IORD	C11
A_CAD12/A	A11	B11
A_CAD11/A	OE	C12
A_CAD10/A	CE2	B12
A_CAD9/A	A10	A12
A_CAD8/A	D15	E12
A_CAD7/A	D7	C13
A_CAD6/A	D13	M15
A_CAD5/A	D6	A13
A_CAD4/A	D12	C14
A_CAD3/A	D5	E13
A_CAD2/A	D11	A14
A_CAD1/A	D4	A14
A_CAD0/A	D3	E14
A_CC/BE3/A	REG	C5
A_CC/BE2/A	A12	F9
A_CC/BE1/A	A8	B10
A_CC/BE0/A	CE1	G12
A_CPAR/A	A13	G10
A_CFRAME/A	A23	C8
A_CTRDY/A	A22	A8
A_CIRDY/A	A15	B8
A_CSTOP/A	A20	A9
A_CDEVSEL/A	A21	C9
A_CBLOCK/A	A19	E10
A_CPERR/A	A14	F10
A_CSERR/A	WAIT	B3
A_CREQ/A	INPACK	E7
A_CGNT/A	WE	B9
A_CSTSCHG/A	BVD1(STSCHG/R)	B2
A_CCLKRUN/A	WP(OIS16)	C3
A_CCLK/A	A16	E9
A_CINT/A	READY(IREQ)	C4
A_CRST/A	RESET	A6
A_CAUDIO/A	BVD2(SPKR)	A2
A_CCD1/A	CD1	C15
A_CCD2/A	CD2	E5
A_CVS1/A	VS1	A3
A_CVS2/A	VS2	E8
A_RSVD/A	D14	B13
A_RSVD/A	D2	D2
A_RSVD/A	A18	C10

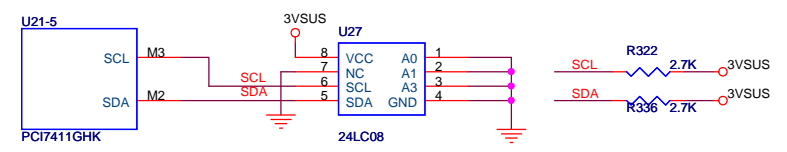


CARDBUS SLOT
FOX=WZ21131-G2

CardBus



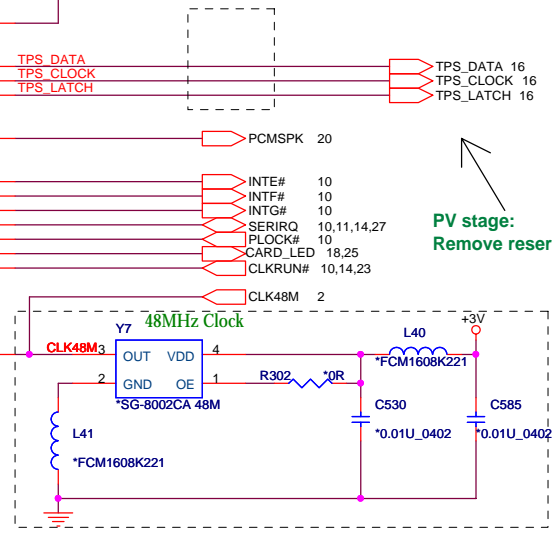
SI stage:
Remove reserve resistor R693~R695 for PC11510RVGF
Sting 09/24/2004



PV stage:
Remove R701 & R702 for unused PCI1510RVGF circuit.
Griffey 12/10/2004

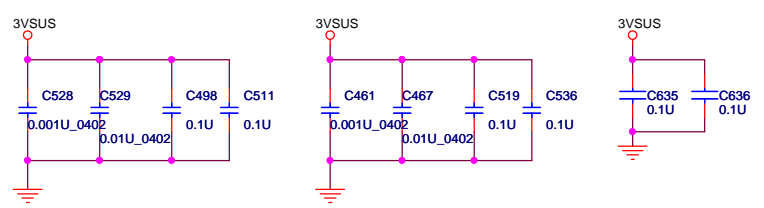
When -VCCD0 and -VCCD1 asserted high, PLOCK# and INTF# will provide a SDA signaling for I2C bus, PLOCK# will provide a SCL signaling for I2C bus.

PV stage:
Remove reserve related circuit for PCI1510RVGF.
Griffey 12/08/2004

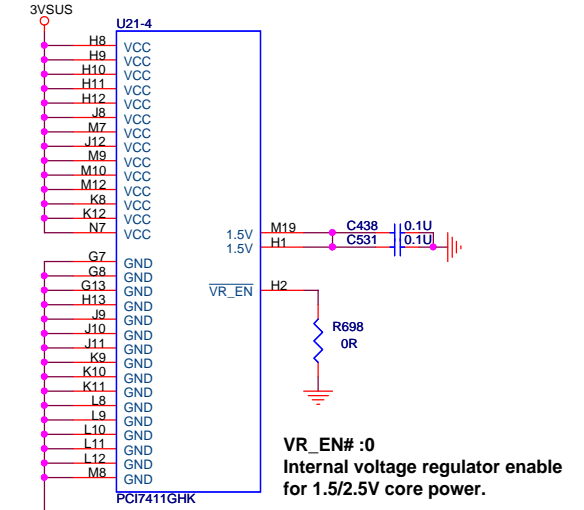


SI stage:
Remove all component of PLL circuit and Add CLK48M input from CKG.

Sting 10/12/2204

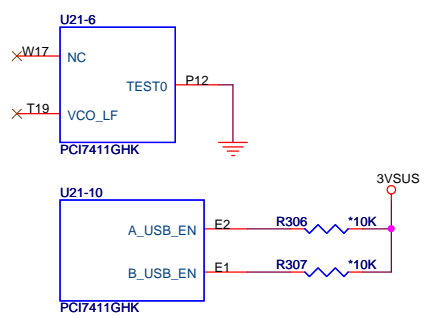
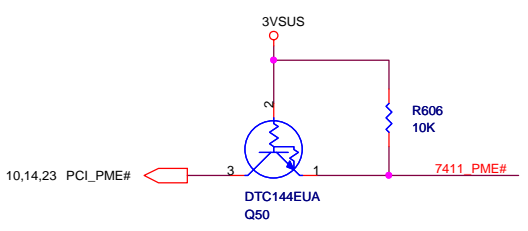
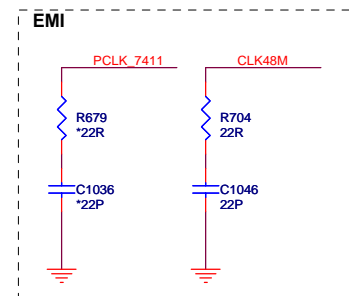


PCIXX21 Power Terminals

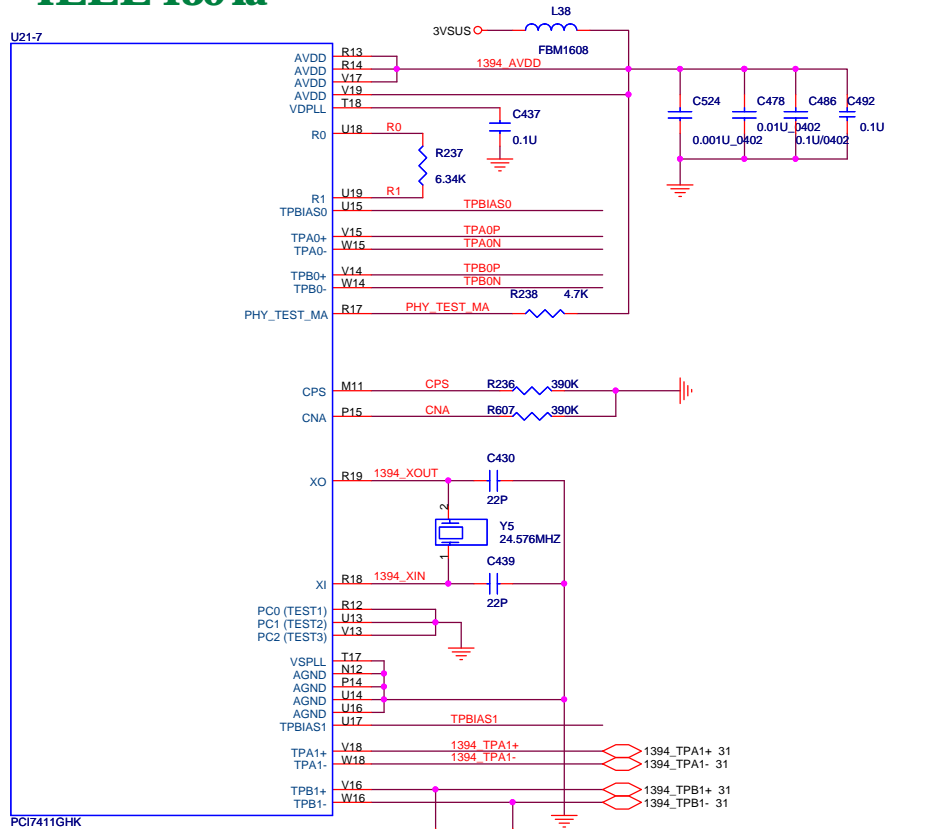


VR_EN# :0
Internal voltage regulator enable for 1.5/2.5V core power.

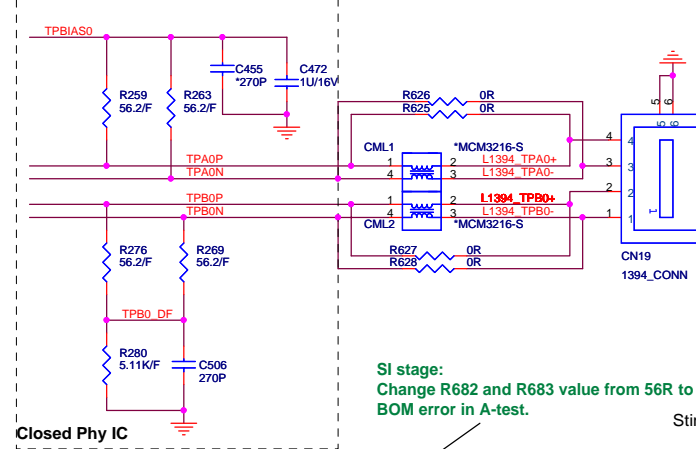
PV stage:
Populate R704 and C1045 for getting better EMI performance.
Sting 11/19/2004



IEEE 1394a



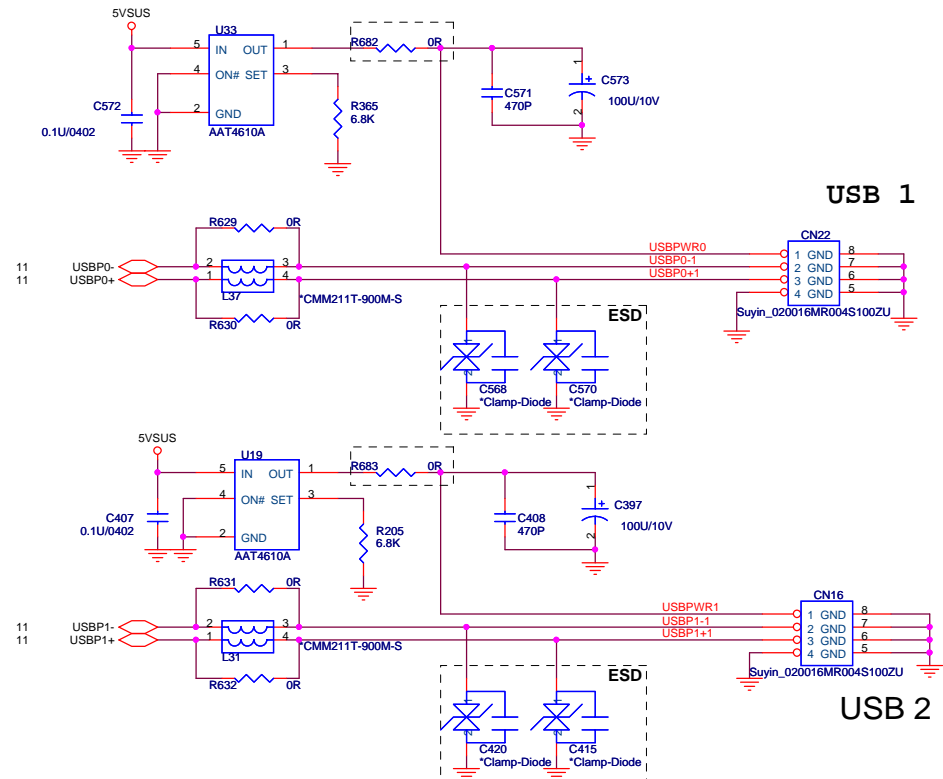
IEEE 1394 CONNECTOR



SI stage:
Change R682 and R683 value from 56R to 0R cause of BOM error in A-test.

Sting 09/24/2004

Closed Phy IC



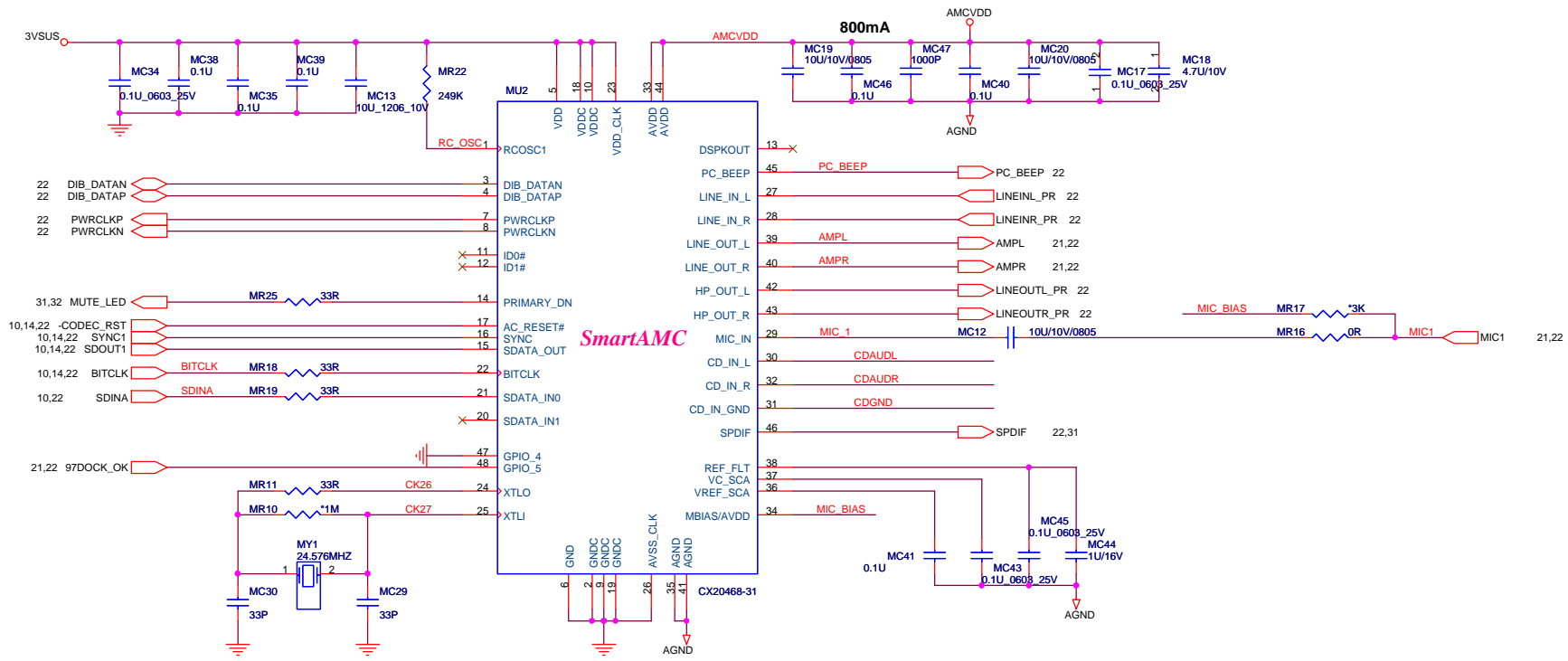
USB 1

USB 2

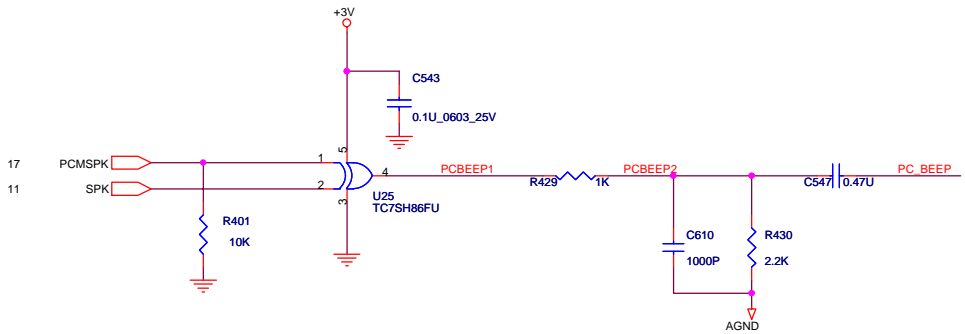
PROJECT : CT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	IEEE 1394A, USBX2	2A
Date:	Monday, December 27, 2004	Sheet 19 of 39

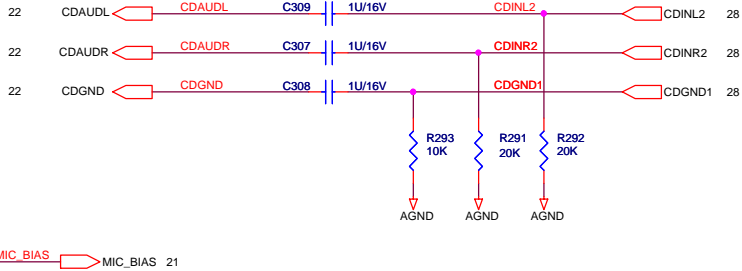
The AMC20493-001 modem is used for mother board family MBAMC20493-010.



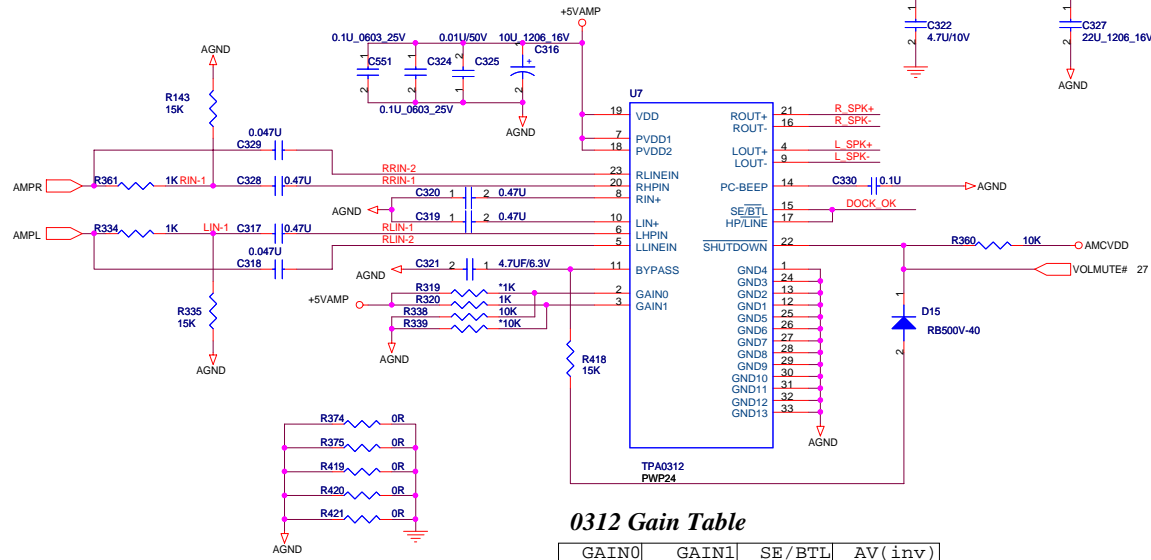
PC SPEAKER



FROM CD-ROM



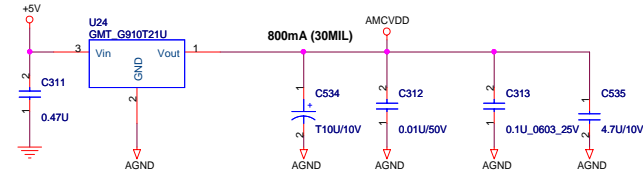
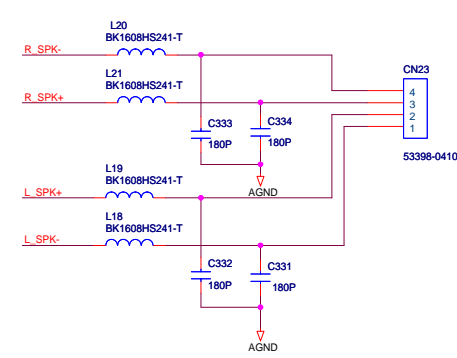
AUDIO AMPLIFIER



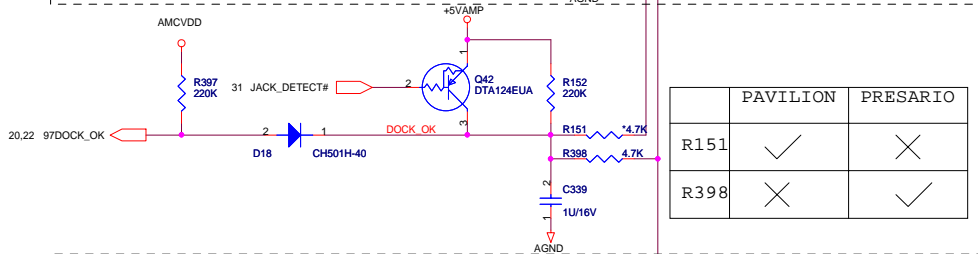
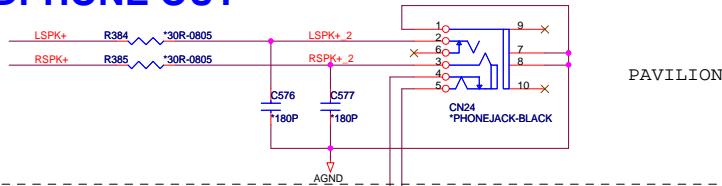
0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	6 dB
0	1	0	10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB

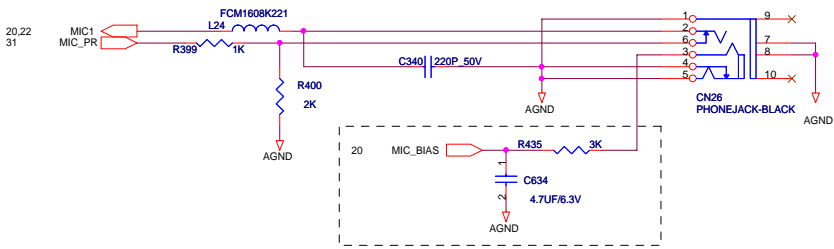
SPEAKER OUT



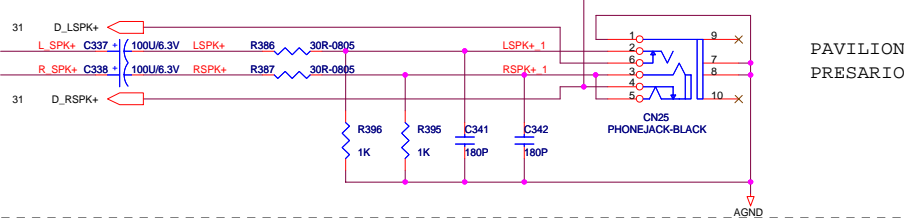
2ND HEADPHONE OUT



MICROPHONE

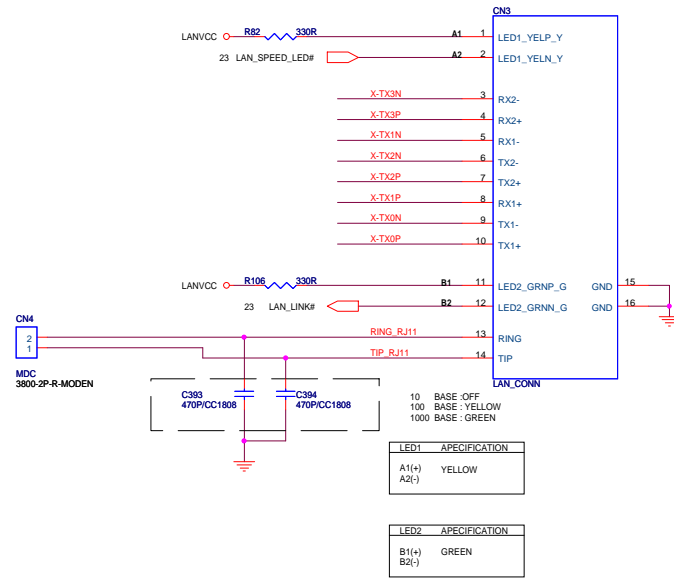
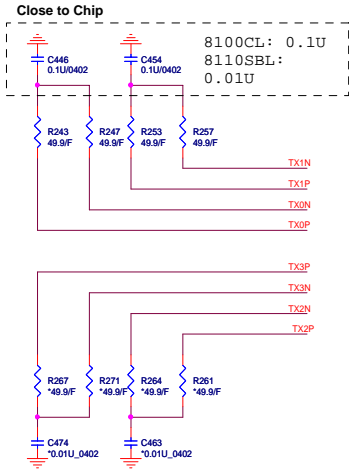
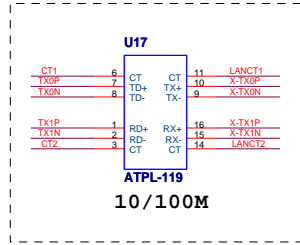
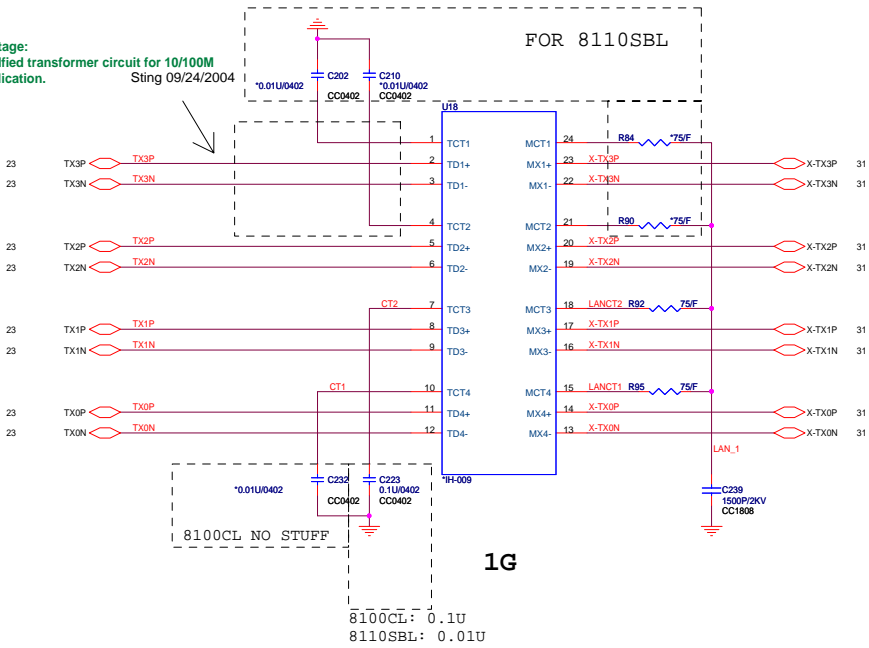


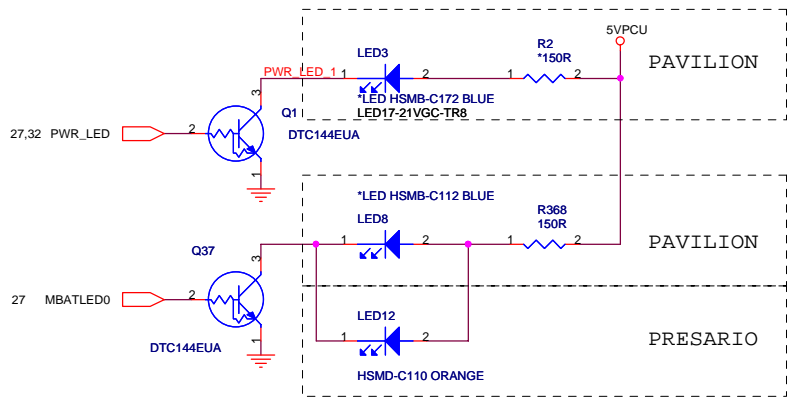
HEADPHONE OUT



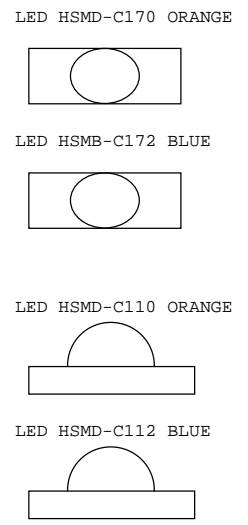
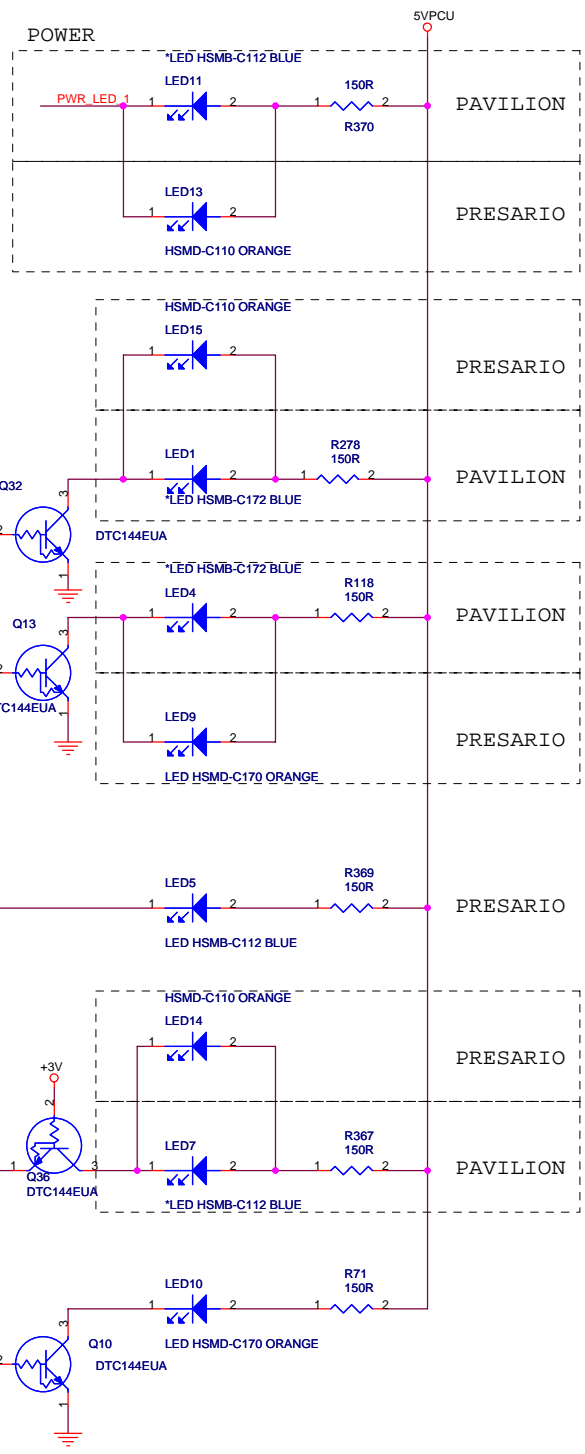
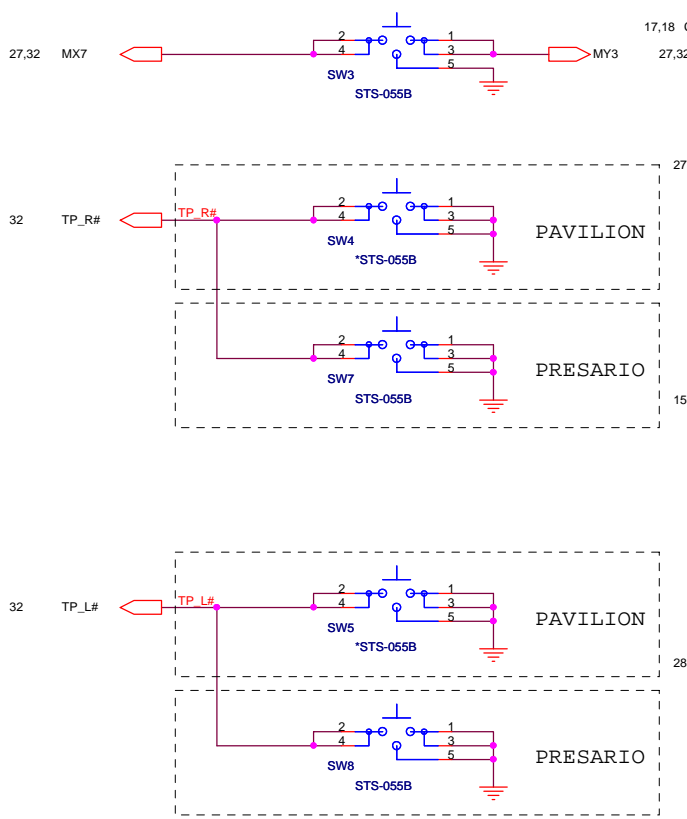
SI stage:
Modified transformer circuit for 10/100M application.

Sting 09/24/2004

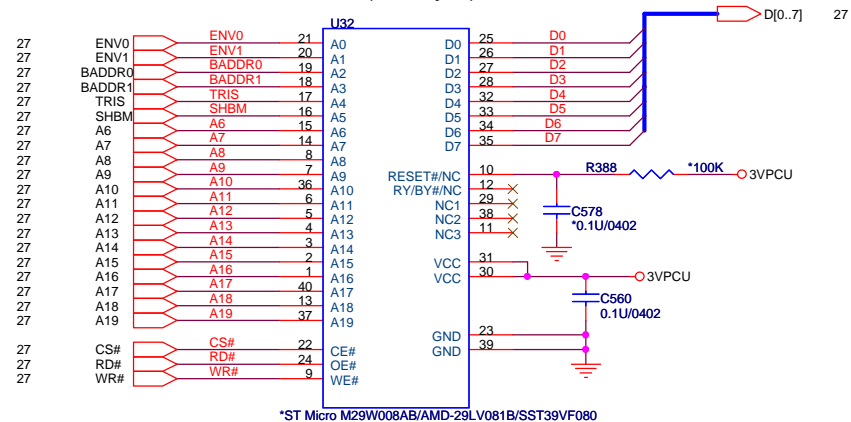




Touchpad control



8Mbit (1M Byte), TSSOP40

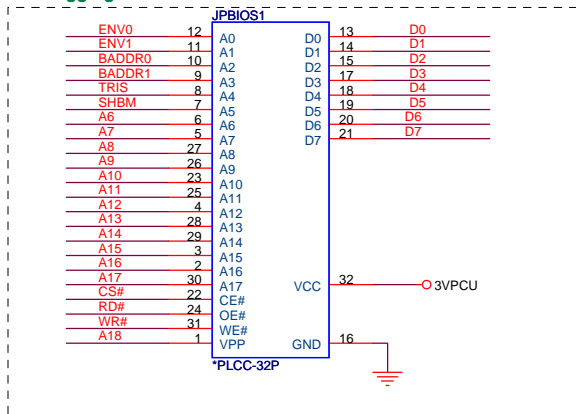


- 1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326 UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
- 2.SIO has internal 20 mS delay of VCC1_PWROK

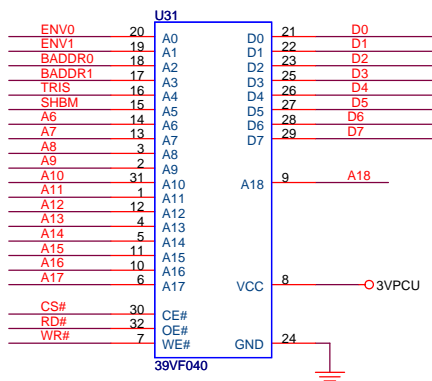
AMD :Pin 10 is RESET# ; Pin12 is RY#
SST :Pin10,12 are NC

SI stage:
Add PLCC32 cause of it is convenient for Bios debugging.

Sting 10/01/2004

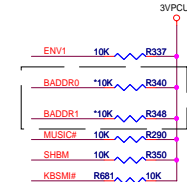
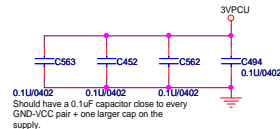
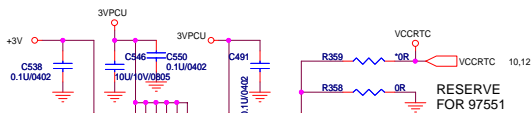
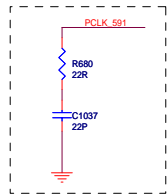


4Mbit (512k Byte), TSSOP32



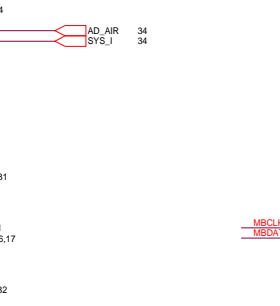
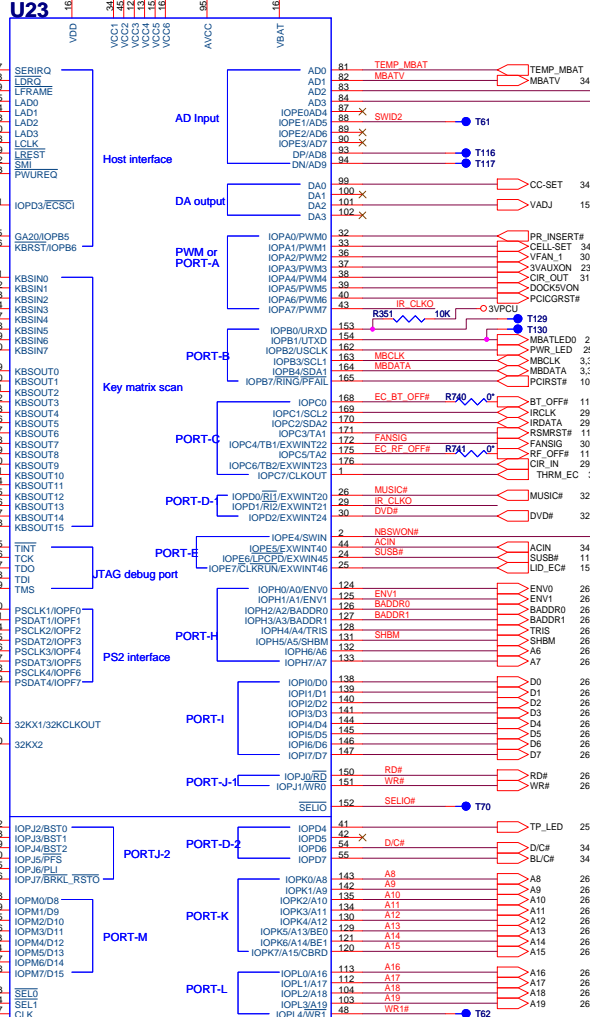
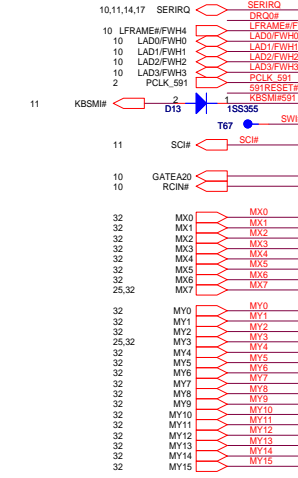
KBC-NS87551L

LDRQ#(pin 8) internal is no use



IO Address			
BADDR1-0	Index	Data	
0 0	2E	2E	
0 1	4E	4E	
1 0	HCFCGBAL	HCFCGBAL	
1 1	Reserved	Reserved	

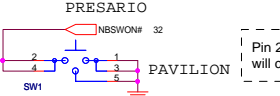
10 LPC_DRQ0# ← LPC_DRQ0# R321 DRQ0#



SHBM#1: Enable shared memory with host BIOS

PV stage:
1. Reserve 0R for RF_OFF# and BT_OFF# circuit.

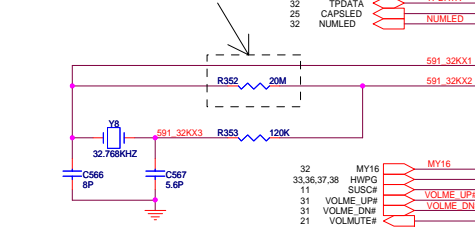
Griffey 12/11/2004



Pin 24 if no pull-high, will can't reboot.

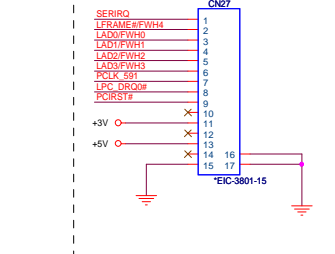
SI stage:
Change R352 value from 120K to 20M.

Sting 09/24/2004



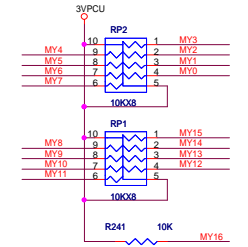
SI stage:
Add LPC debug port for software team to debug convenient.

Sting 10/06/2004

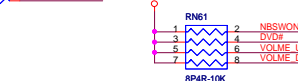
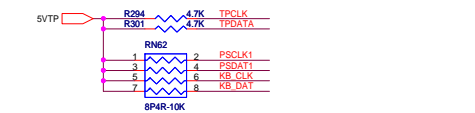
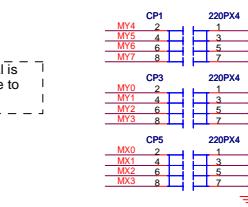


PV stage:
Modify pin name.

Griffey 12/10/2004



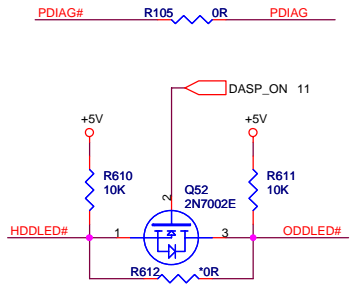
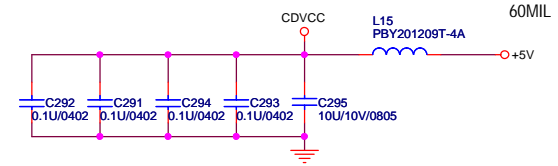
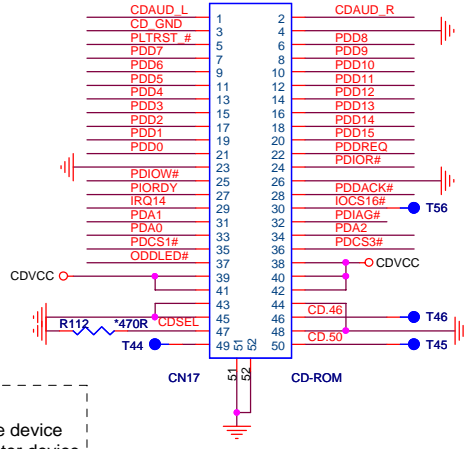
Pin 103 internal is 'A19', Can't use to GPIO



HDD, CD-ROM

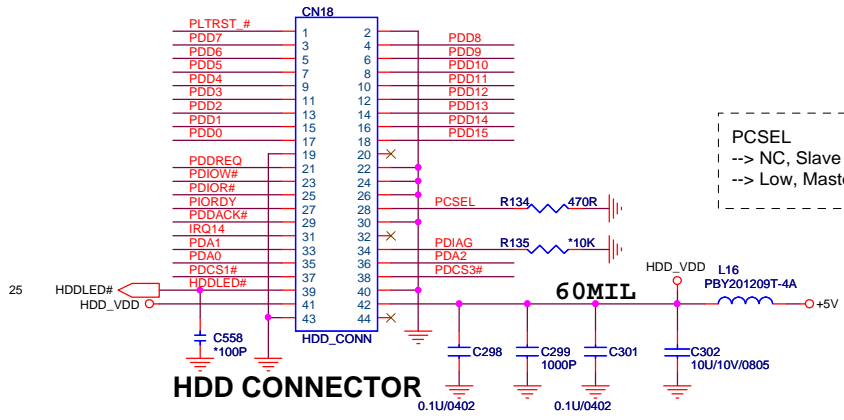
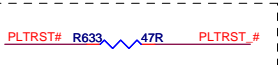
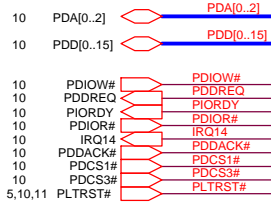


CD-ROM

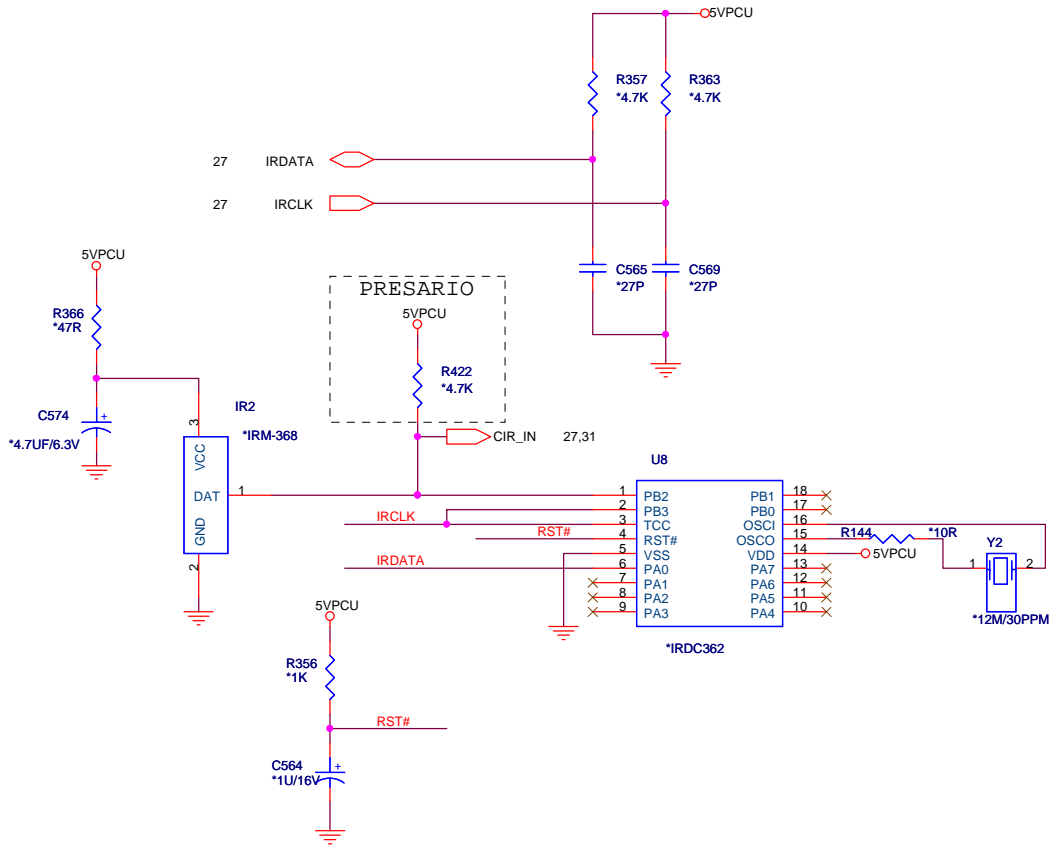


ADD DASP_ON FOR IDE CABLE SELECT

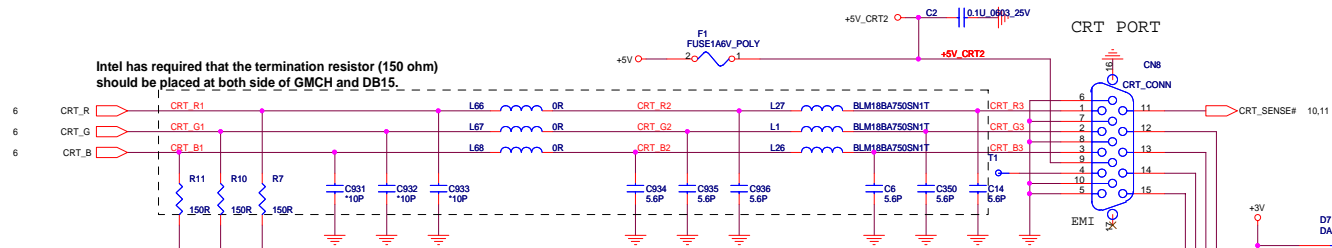
CDSEL
--> NC, Slave device
--> Low, Master device



PCSEL
--> NC, Slave device
--> Low, Master device

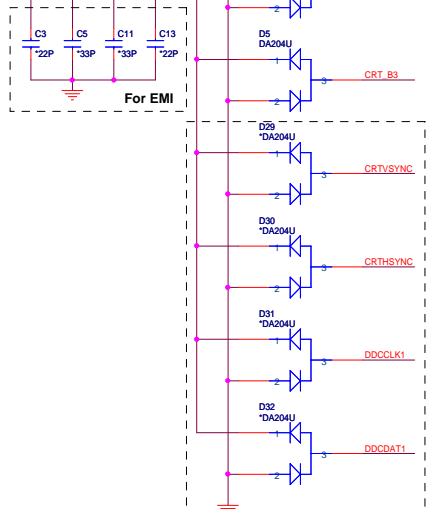
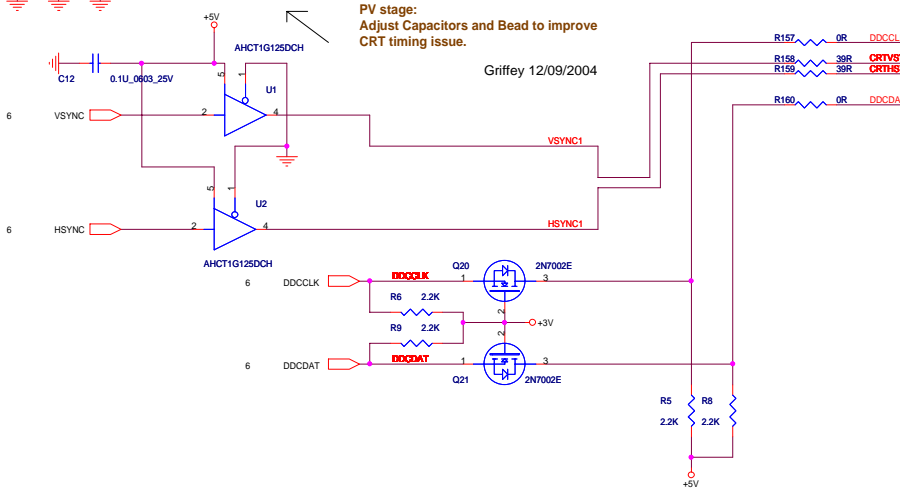


Intel has required that the termination resistor (150 ohm) should be placed at both side of GMCH and DB15.

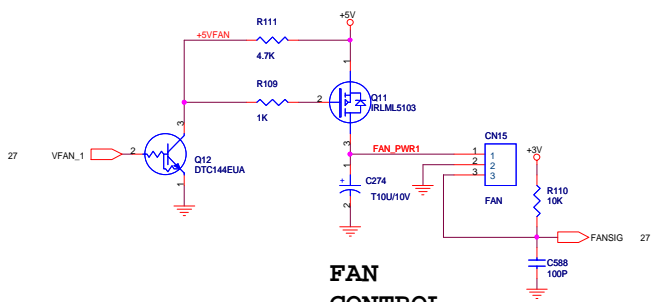


PV stage: Adjust Capacitors and Bead to improve CRT timing issue.

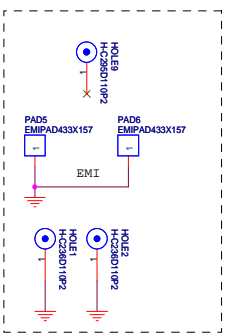
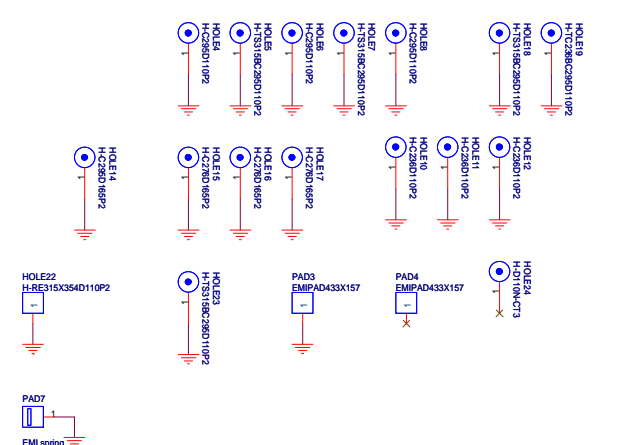
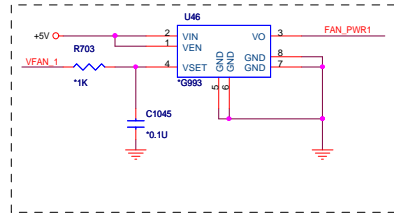
Griffey 12/09/2004

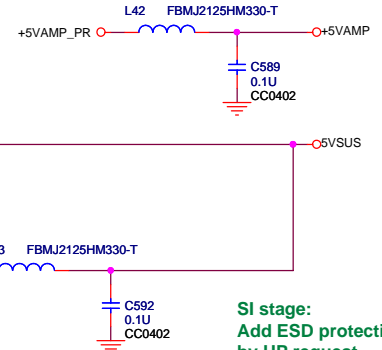
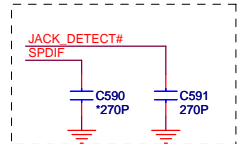
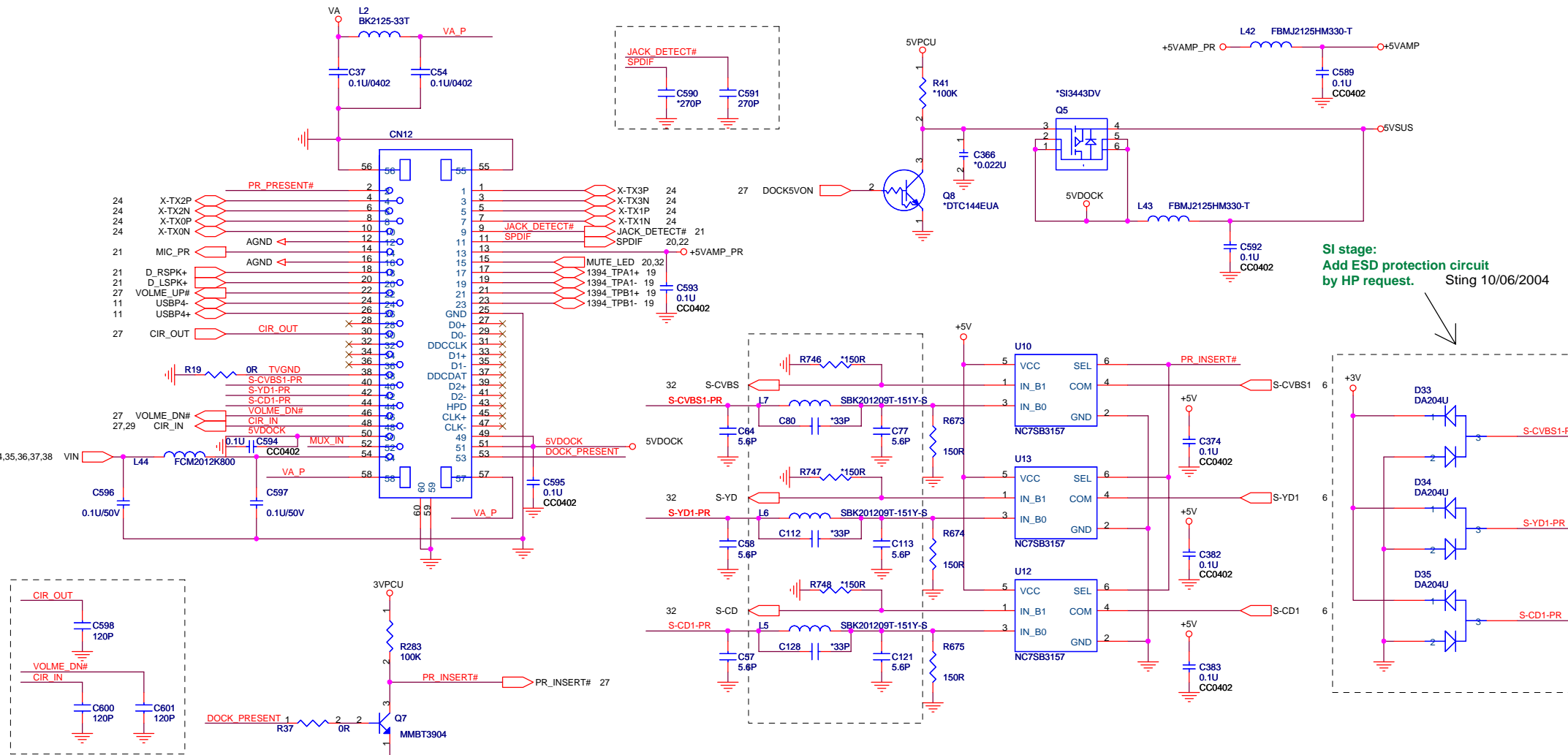


FAN CONTROL

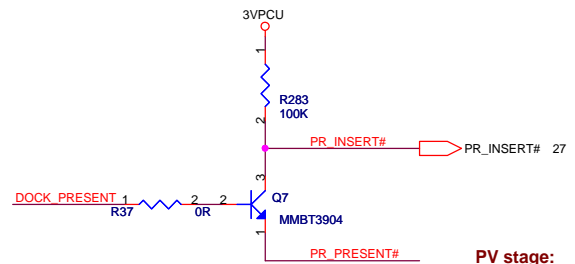
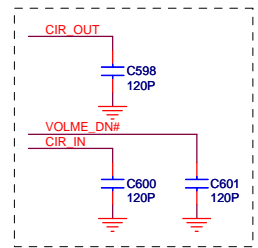
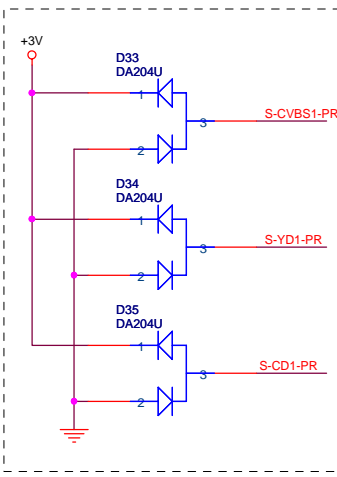
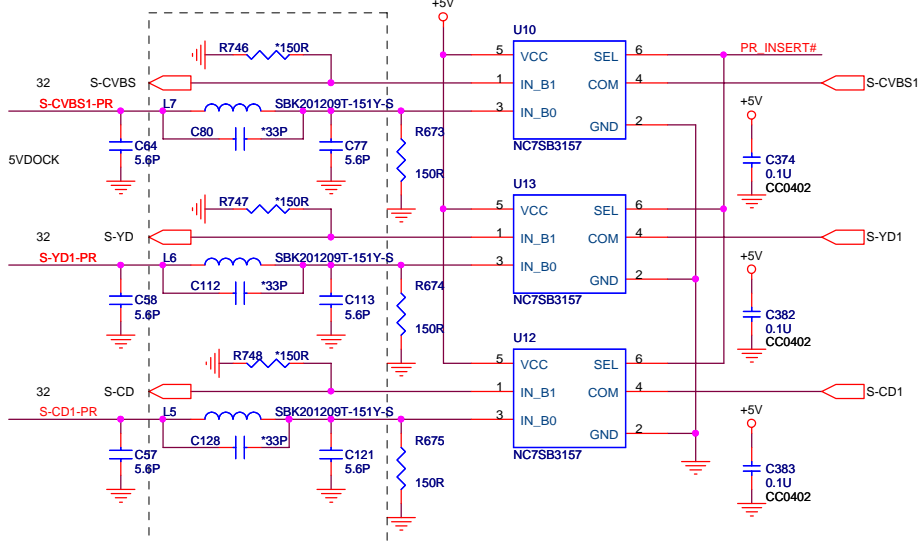


SI stage: Add GMT solution for B-test to costdown. Sting 09/24/2004





SI stage:
Add ESD protection circuit
by HP request. Sting 10/06/2004



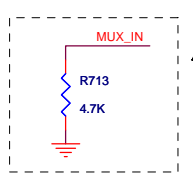
PV stage:
1. Change L5,L6,L7,C57,C58,C64,C77,C113,C121 value to improve S-video quality.
2. Reserve S-video impedance match circuit.

SEL	FUNCTION (COM)
HIGH	IN_B1

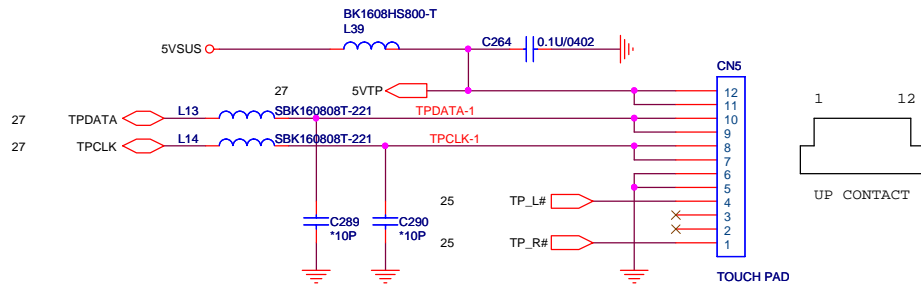
Griffey 12/22/2004

SI stage:
Add R713 to enable the mux in the Tampa-2 cable.
(connects the component TV output to the composite/Svideo output lines).

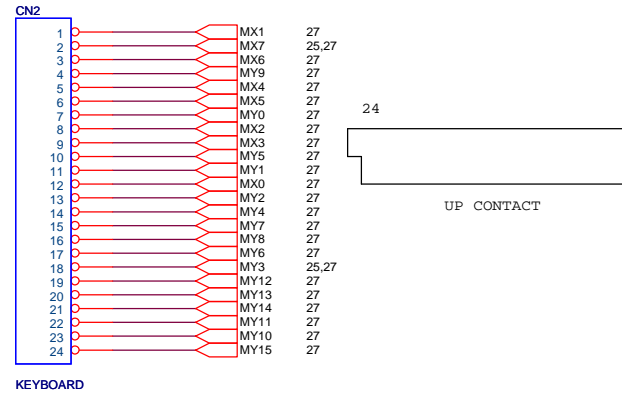
Sting 10/12/2004



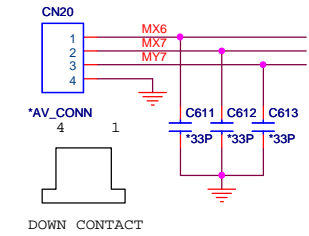
TOUCH PAD CONNECTOR



KEYBOARD CONNECTOR

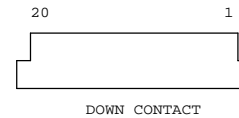
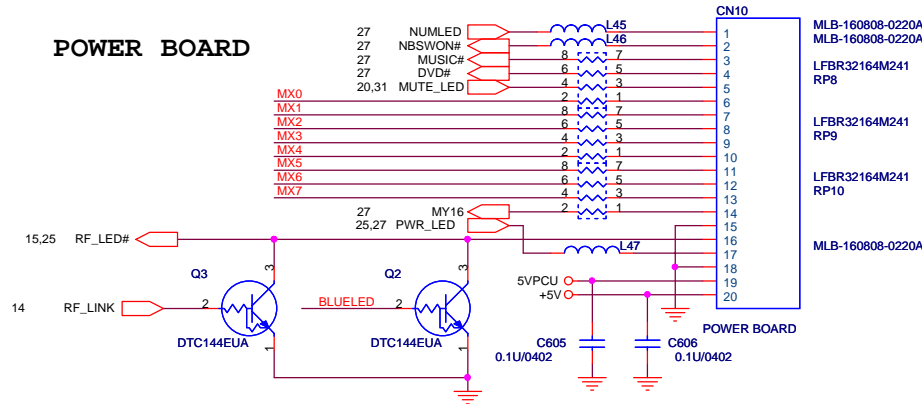


AV BOARD



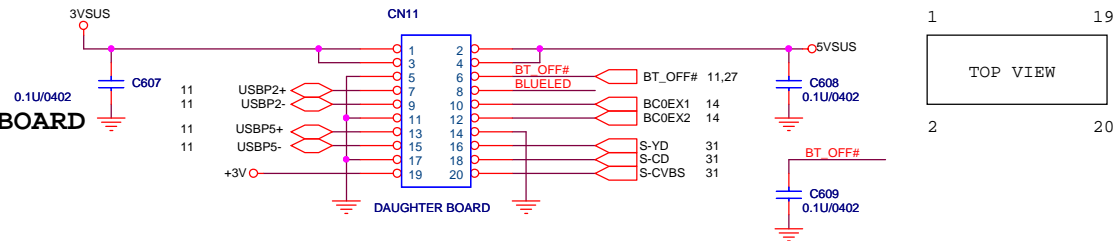
MX6	MX7
ENTER	MENU

POWER BOARD



MX0	MX1	MX2	MX3	MX4	MX5	MX6	MX7
BACK	PLAY/PAUSE	FORWARE	STOP	VOL UP	MUTE	VOL DN	WIRELESS

DAUGHTER BOARD

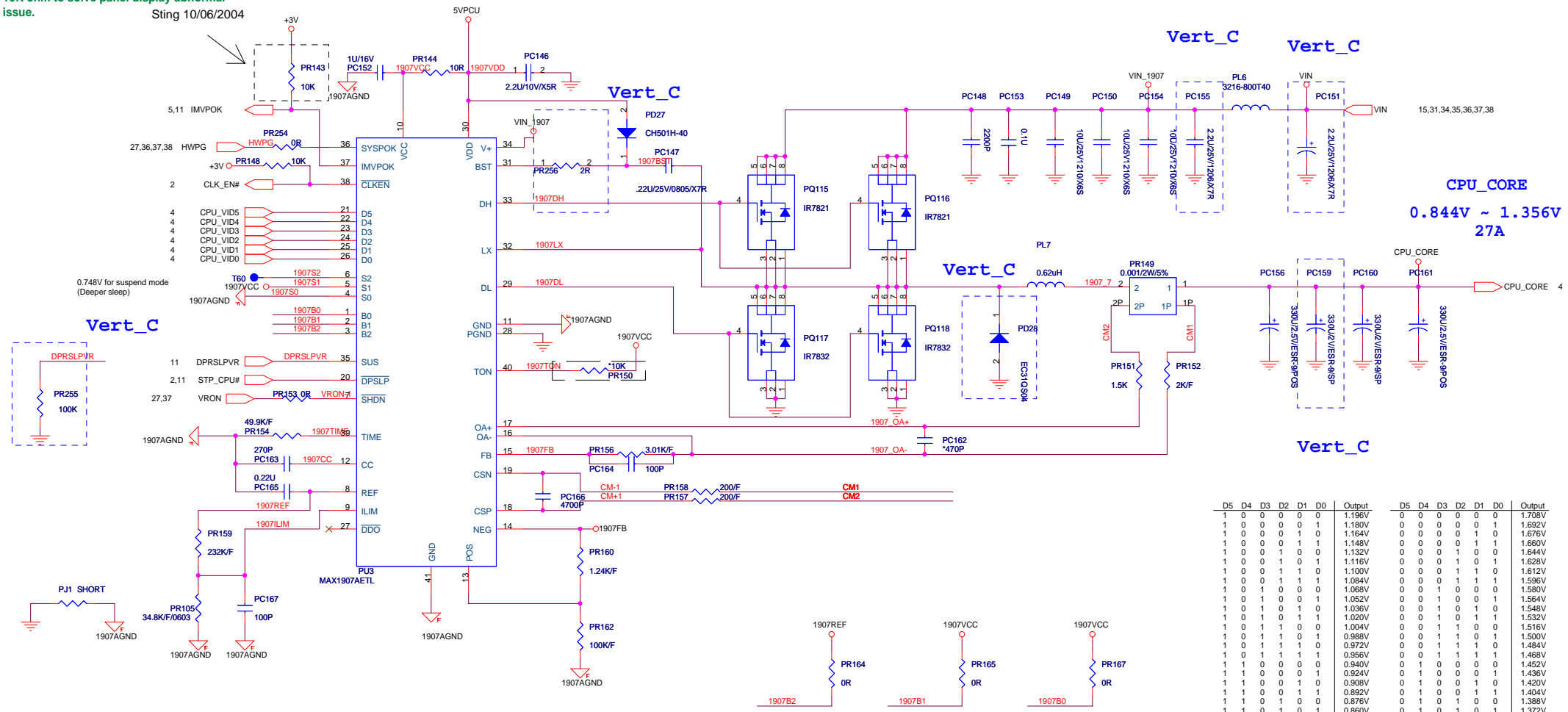


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Quanta Computer Inc.

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CPU VCC_CORE (MAX1907)

SI stage:
Change PR143 value from 100K ohms to
10K ohm to solve panel display abnormal
issue.
Sting 10/06/2004



CPU_CORE
0.844V ~ 1.356V
27A

D5	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	1.196V	0	0	0	0	0	0	1.708V
1	0	0	0	0	1	1.180V	0	0	0	0	0	1	1.692V
1	0	0	0	1	0	1.164V	0	0	0	0	1	0	1.676V
1	0	0	0	1	1	1.148V	0	0	0	0	1	1	1.660V
1	0	0	1	0	0	1.132V	0	0	0	1	0	0	1.644V
1	0	0	1	0	1	1.116V	0	0	0	1	0	1	1.628V
1	0	0	1	1	0	1.100V	0	0	0	1	1	0	1.612V
1	0	0	1	1	1	1.084V	0	0	0	1	1	1	1.596V
1	0	1	0	0	0	1.068V	0	0	1	0	0	0	1.580V
1	0	1	0	0	1	1.052V	0	0	1	0	0	1	1.564V
1	0	1	0	1	0	1.036V	0	0	1	0	1	0	1.548V
1	0	1	0	1	1	1.020V	0	0	1	0	1	1	1.532V
1	0	1	1	0	0	1.004V	0	0	1	1	0	0	1.516V
1	0	1	1	0	1	0.988V	0	0	1	1	0	1	1.500V
1	0	1	1	1	0	0.972V	0	0	1	1	1	0	1.484V
1	0	1	1	1	1	0.956V	0	0	1	1	1	1	1.468V
1	1	0	0	0	0	0.940V	0	1	0	0	0	0	1.452V
1	1	0	0	0	1	0.924V	0	1	0	0	0	1	1.436V
1	1	0	0	1	0	0.908V	0	1	0	0	1	0	1.420V
1	1	0	0	1	1	0.892V	0	1	0	0	1	1	1.404V
1	1	0	1	0	0	0.876V	0	1	0	1	0	0	1.388V
1	1	0	1	0	1	0.860V	0	1	0	1	0	1	1.372V
1	1	0	1	1	0	0.844V	0	1	0	1	1	0	1.356V
1	1	0	1	1	1	0.828V	0	1	0	1	1	1	1.340V
1	1	1	0	0	0	0.812V	0	1	1	0	0	0	1.324V
1	1	1	0	0	1	0.796V	0	1	1	0	0	1	1.308V
1	1	1	0	1	0	0.780V	0	1	1	0	1	0	1.292V
1	1	1	0	1	1	0.764V	0	1	1	0	1	1	1.276V
1	1	1	1	0	0	0.748V	0	1	1	1	0	0	1.260V
1	1	1	1	0	1	0.732V	0	1	1	1	0	1	1.244V
1	1	1	1	1	0	0.716V	0	1	1	1	1	0	1.228V
1	1	1	1	1	1	0.700V	0	1	1	1	1	1	1.212V

SUSPEND MODE (SUS=HIGH)				
S2	S1	S0	Output	
✓	OPEN	VCC	GND	0.748V

VCC_BOOT			
B2	B1	B0	Output
GND	GND	GND	1.708V
REF	REF	REF	1.372V
OPEN	OPEN	OPEN	1.036V
VCC	VCC	VCC	0.700V
REF	VCC	VCC	1.212V

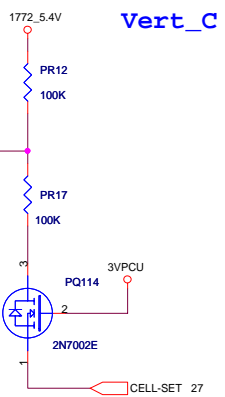
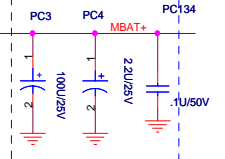
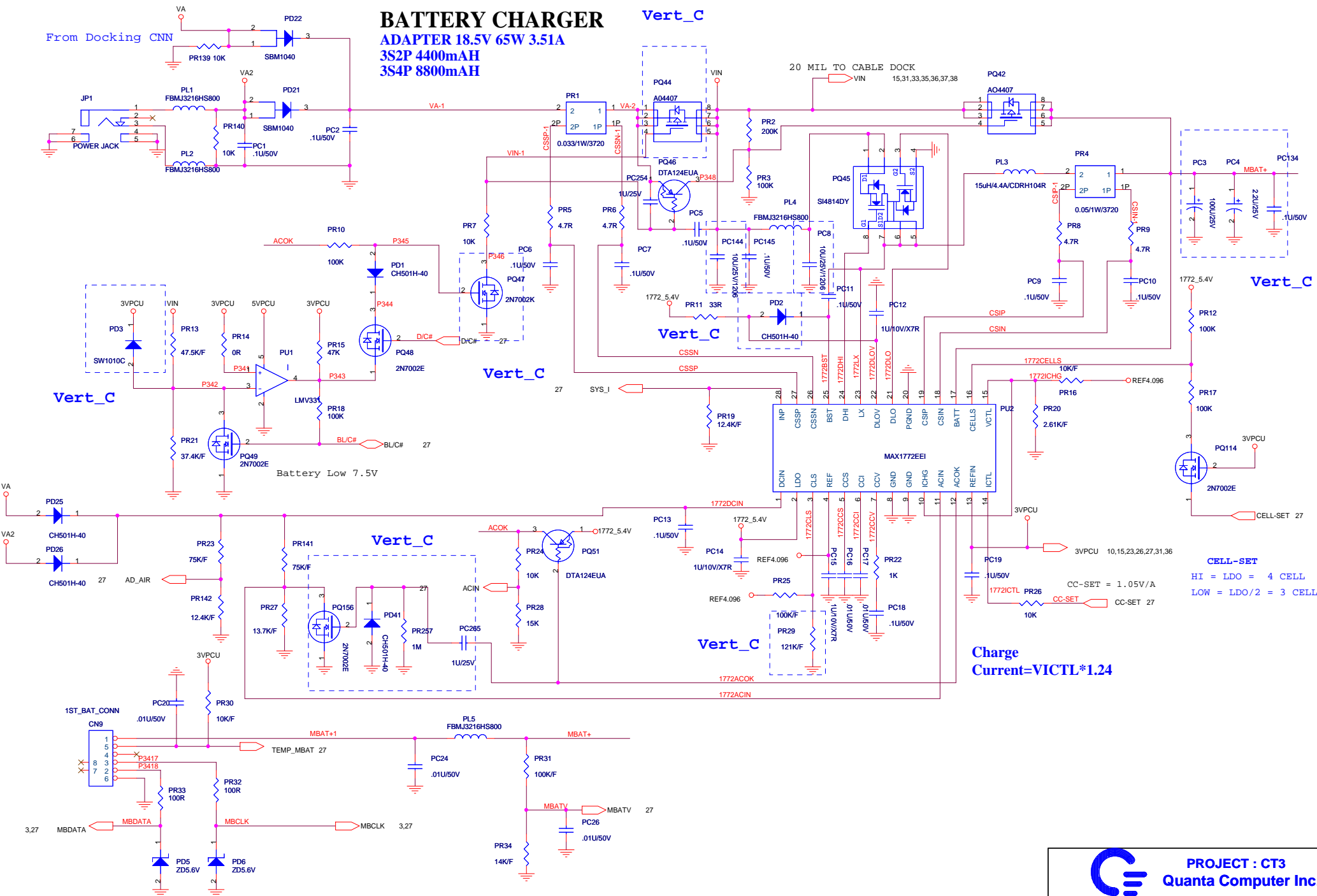
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Quanta Computer Inc.

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Custom		CPU CORE POWER	2A
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BATTERY CHARGER


ADAPTER 18.5V 65W 3.51A
3S2P 4400mAh
3S4P 8800mAh

Vert_C



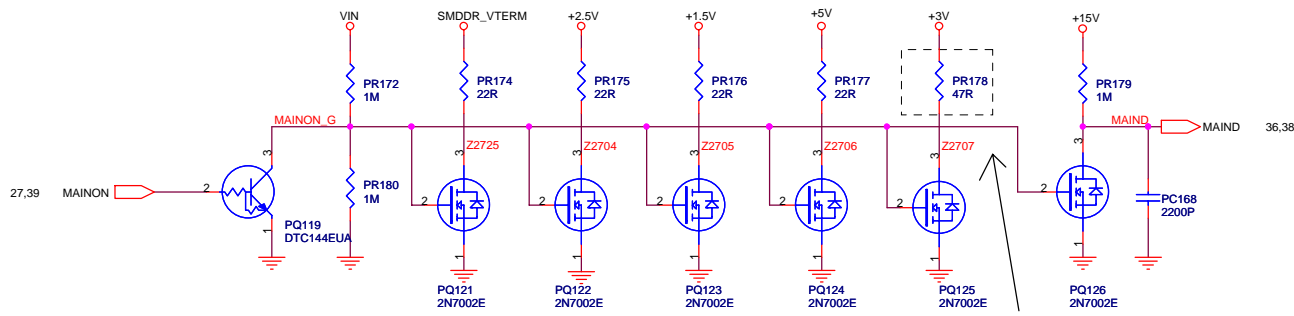
CELL-SET
HI = LDO = 4 CELL
LOW = LDO/2 = 3 CELL

Charge
Current = VICTL * 1.24



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Quanta Computer Inc.

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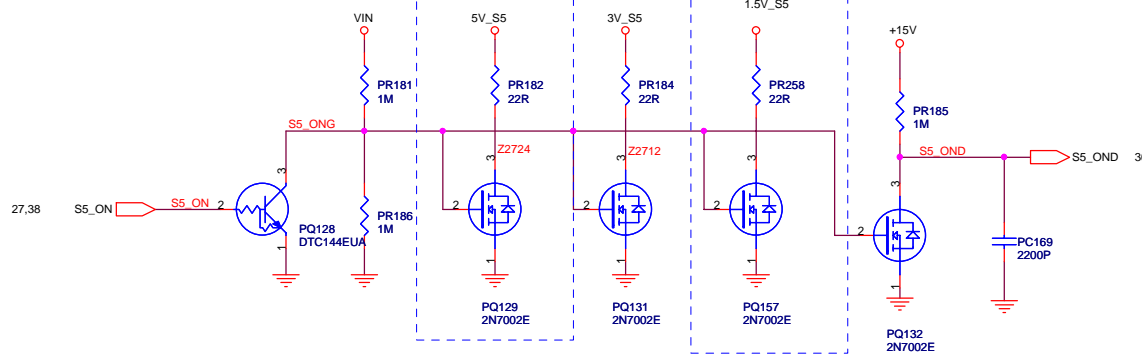


Vert_C

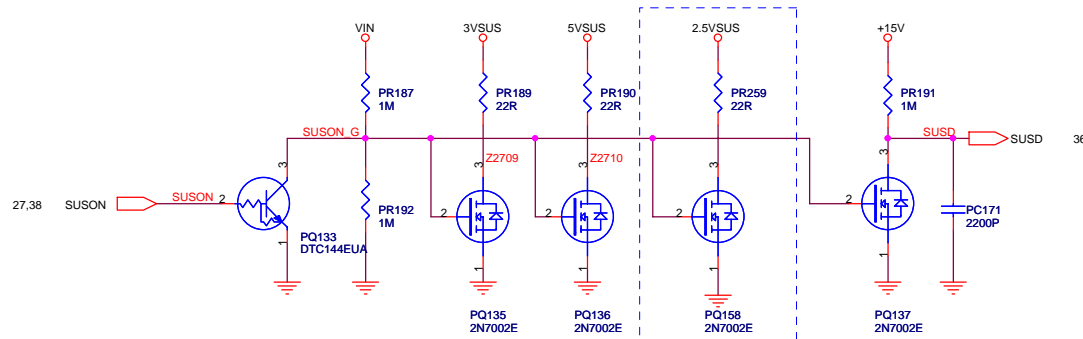
Vert_C


SI stage:
Change PR178 value from 22 ohm to 47 ohm, Intel has required the timing sequence of +1.5V and +3V in the system, we'd like to increase the value to make +3V discharge slowly to meet the specification of falling time.

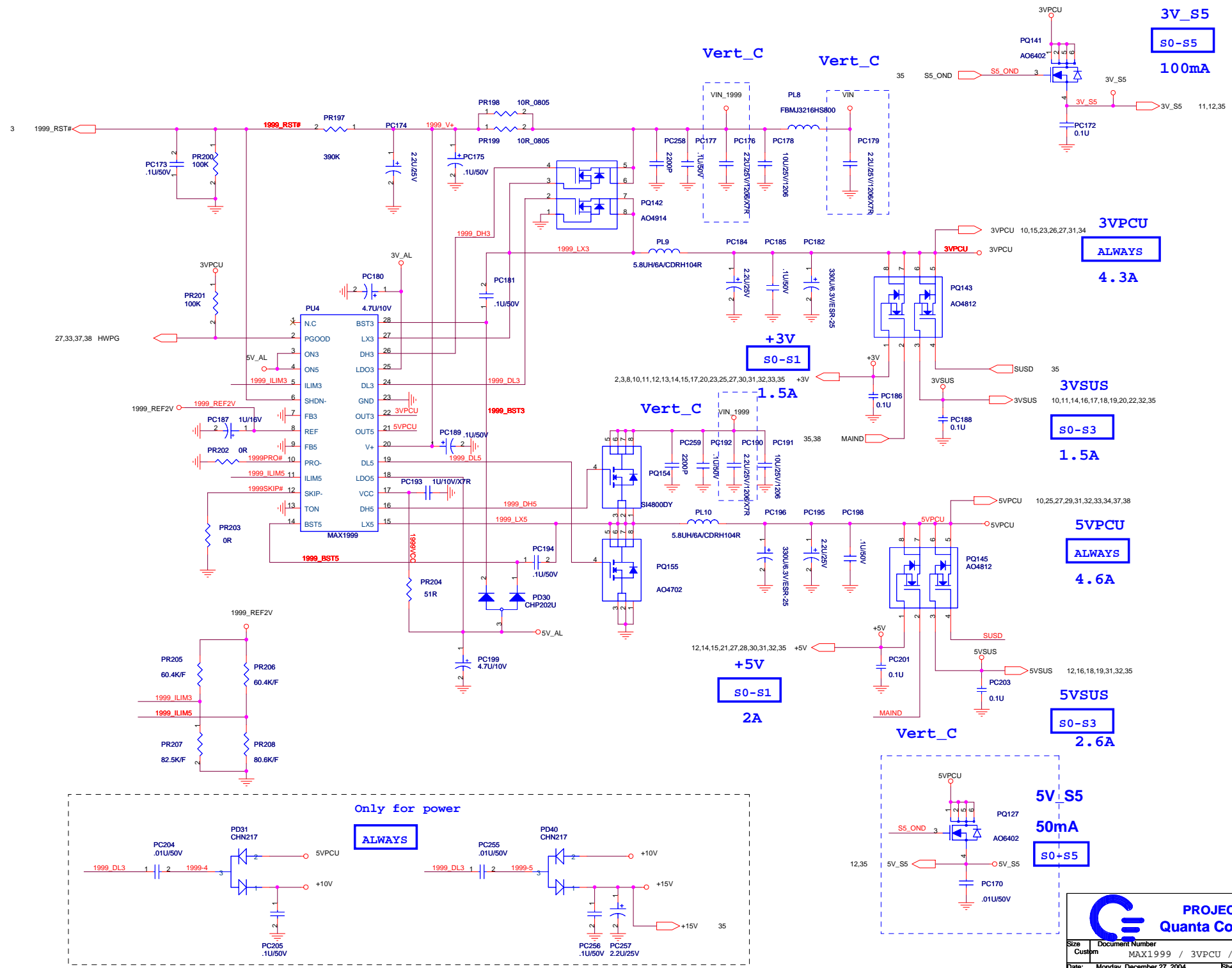
Sting 10/19/2004



Vert_C



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		Size	Custom
DISCHARGE		Sheet	35 of 39
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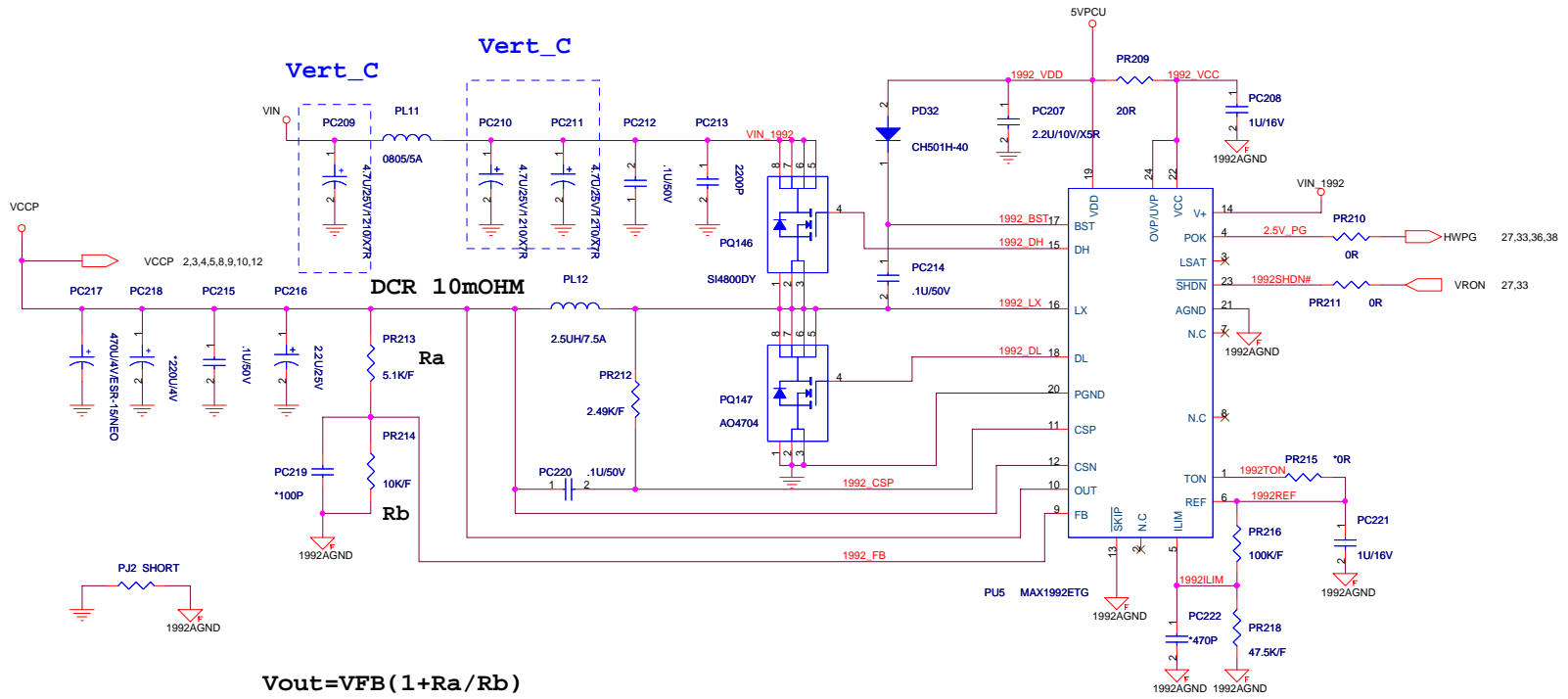


PROJECT : CT3
Quanta Computer Inc.

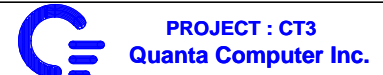
Size	Document Number	Rev
Custom	MAX1999 / 3VPCU / 5VPCU / 15V	2A

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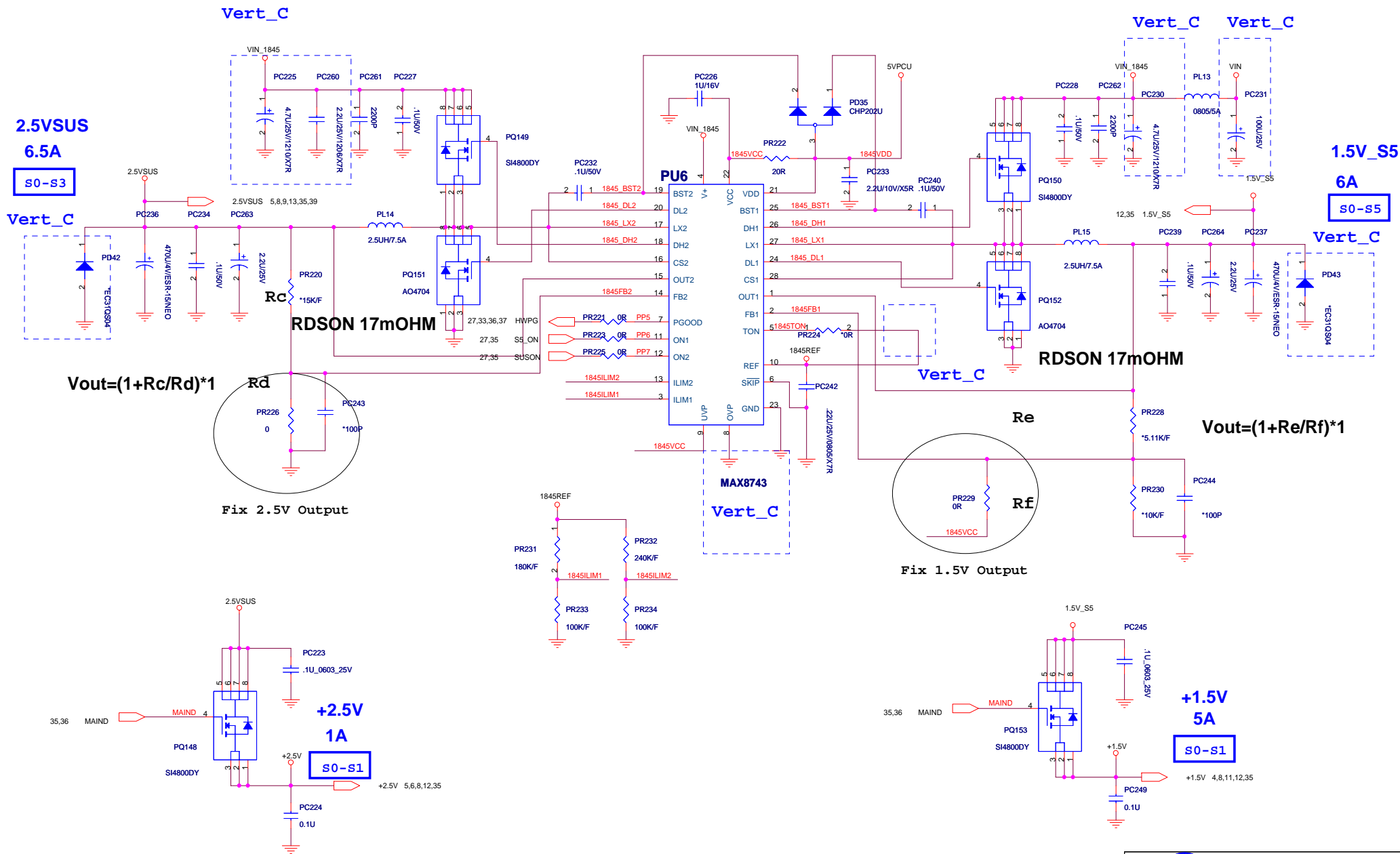
VCCP
1.05V
6.5A
S0-S1



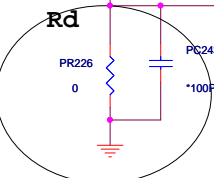
$V_{out} = V_{FB}(1 + R_a/R_b)$
#VFB=0.7V



Size	Document Number	Rev
Custom	VCCP	2A
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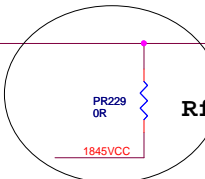


$$V_{out} = (1 + R_c/R_d) * 1$$



Fix 2.5V Output

$$V_{out} = (1 + R_e/R_f) * 1$$



Fix 1.5V Output



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