COMPAL CONFIDENTIAL

MODEL NAME : *QAL81*

PCB NO : *LA-7782P (DAA00002J00)*

BOM P/N : *TBD*

GPIO MAP: E4_VC_GPIO_map_rev_0.8

Dalmore 14 DSC

Ivy Bridge + Panther POINT

2011-05-12

REV : 0.1 (X00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N	
TPM		1@ 3@
TCM		2@ 4@
TPM DIS/TCM DIS		2@ 3@

MB PCB

Part Number	Description
DAA00002J00	PCB 0LE LA-7782P REV0 M/B DSC

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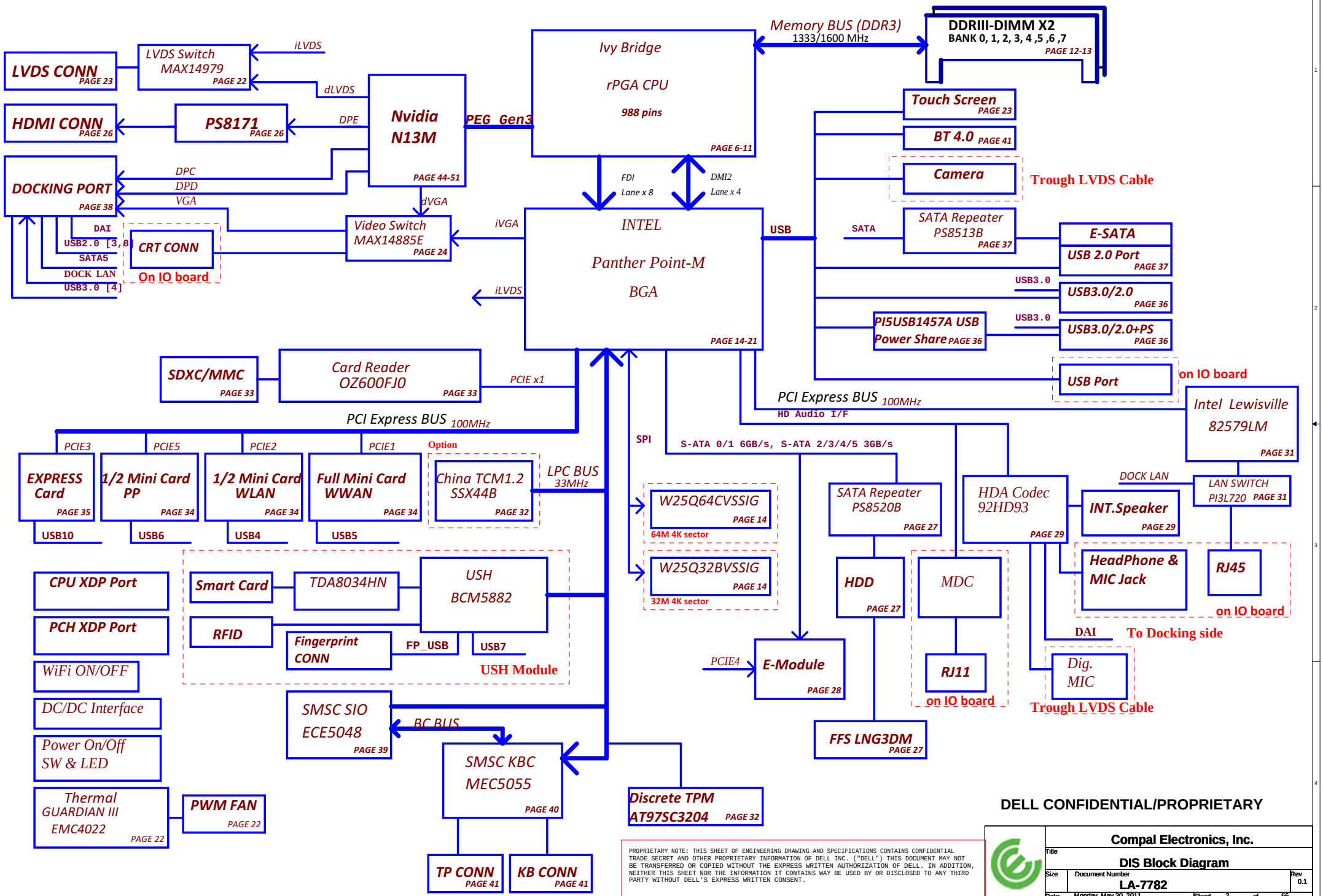
Compal Electronics, Inc.

Title: Cover Sheet

Size | Document Number: LA-7782 | Rev: 0.1

Date: Tuesday, May 24, 2011 | Sheet 1 of 66

Block Diagram Compal confidential



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Compal Electronics, Inc.	
Title	DIS Block Diagram
Size	Document Number: LA-7782
Rev	0.1
Date:	Monday, May 30, 2011
Sheet	2 of 66

POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Layer No.	Name	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
		SolderMask	min 0.4	0.50000
		Add Plating		1.45000
1	Top	Copper foil	0.5oz(0.68)	0.65000
		Prepreg	1080	2.75000
2	GND1	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
3	IN 1	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
4	GND2	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
5	IN 2	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506*2	11.50000
6	IN 3	Copper foil	1oz(1.35)	1.35000
		Core	3mil	3.09000
7	VCC	Copper foil	1oz(1.35)	1.35000
		Prepreg	1506	5.50000
8	IN 4	Copper foil	1oz(1.35)	1.35000
		Core	4mil	3.89000
9	GND 3	Copper foil	1oz(1.35)	1.30000
		Prepreg	1080	2.75000
10	Bottom	Copper foil	0.5oz(0.68)	0.65000
		Add Plating		1.45000
		SolderMask	min 0.4	0.50000
	Overall Thickness (1.45mm ± 10%)			57.91000

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

need to update Power Status and PM Table

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Right side Top)
	1	JUSB2 (Right side Bottom)
	2	JESA1 (Right side ESATA)
	3	MLK DOCK
	4	WLAN
	5	WWAN
	6	JMINI3(Flash)
	7	USH->BIO
	8	DOCKING
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

USH	0	BIO
	1	NA

DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

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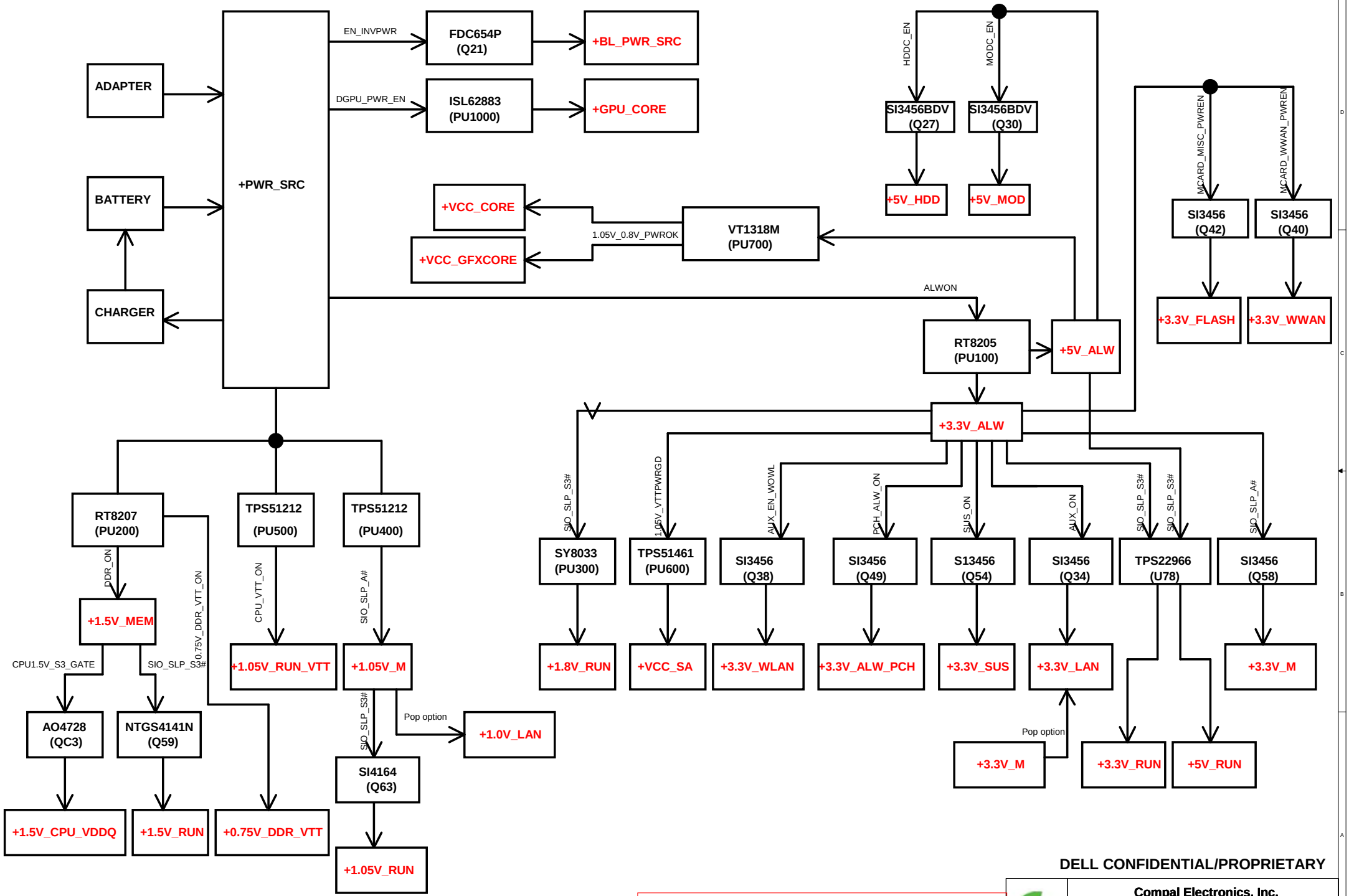
Title: Index and Config.

Size: | Document Number: LA-7782 | Rev: 0.1

Date: Friday, May 20, 2011 | Sheet 3 of 66



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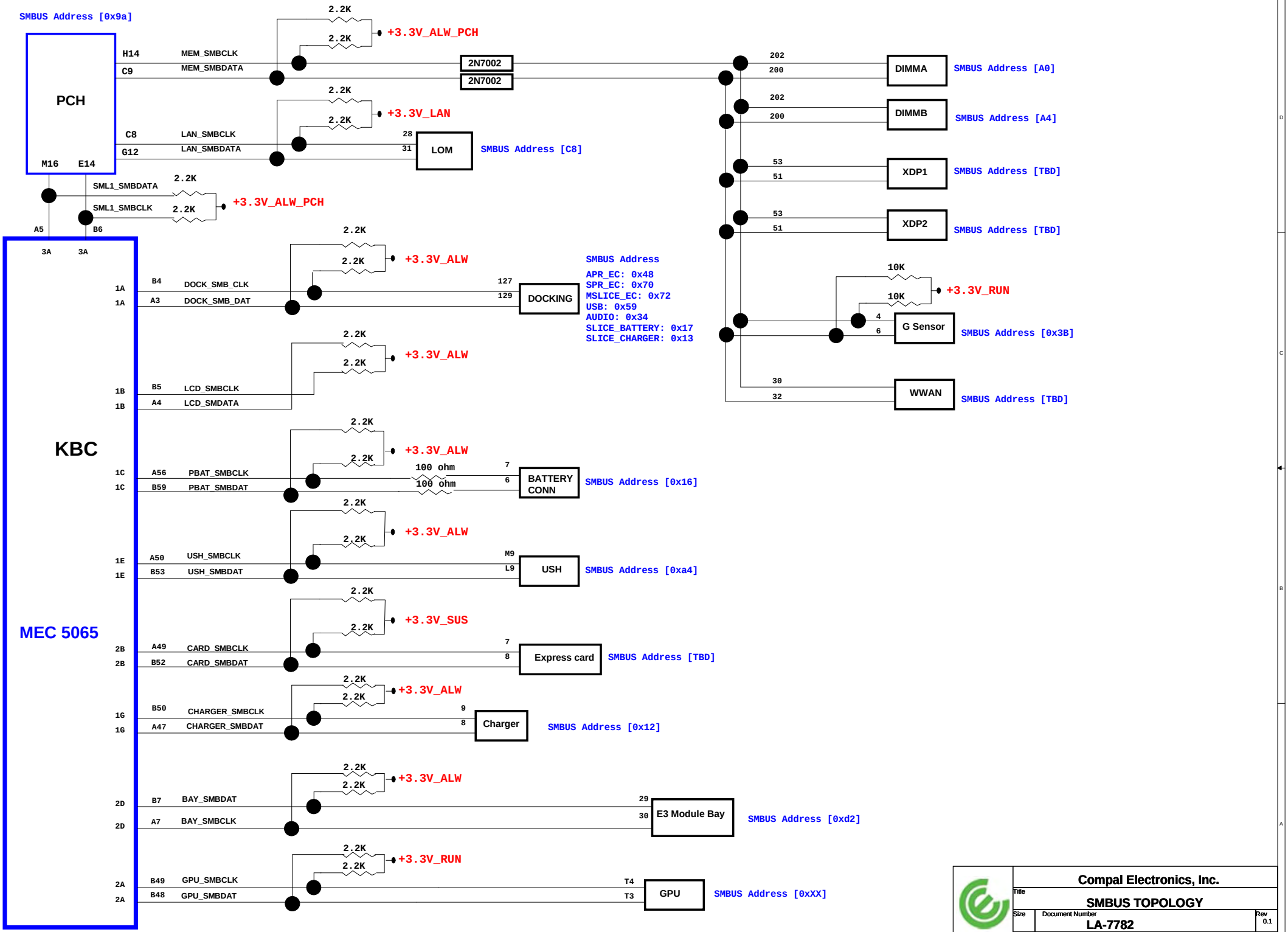
Compal Electronics, Inc.	
Title	Power Rail
Size	Document Number: LA-7782
Rev	0.1
Date:	Friday, May 20, 2011
Sheet	4 of 66



Compal Electronics, Inc.	
Title	SMBUS TOPOLOGY
Size	Document Number: LA-7782
Rev	0.1
Date:	Friday, May 20, 2011
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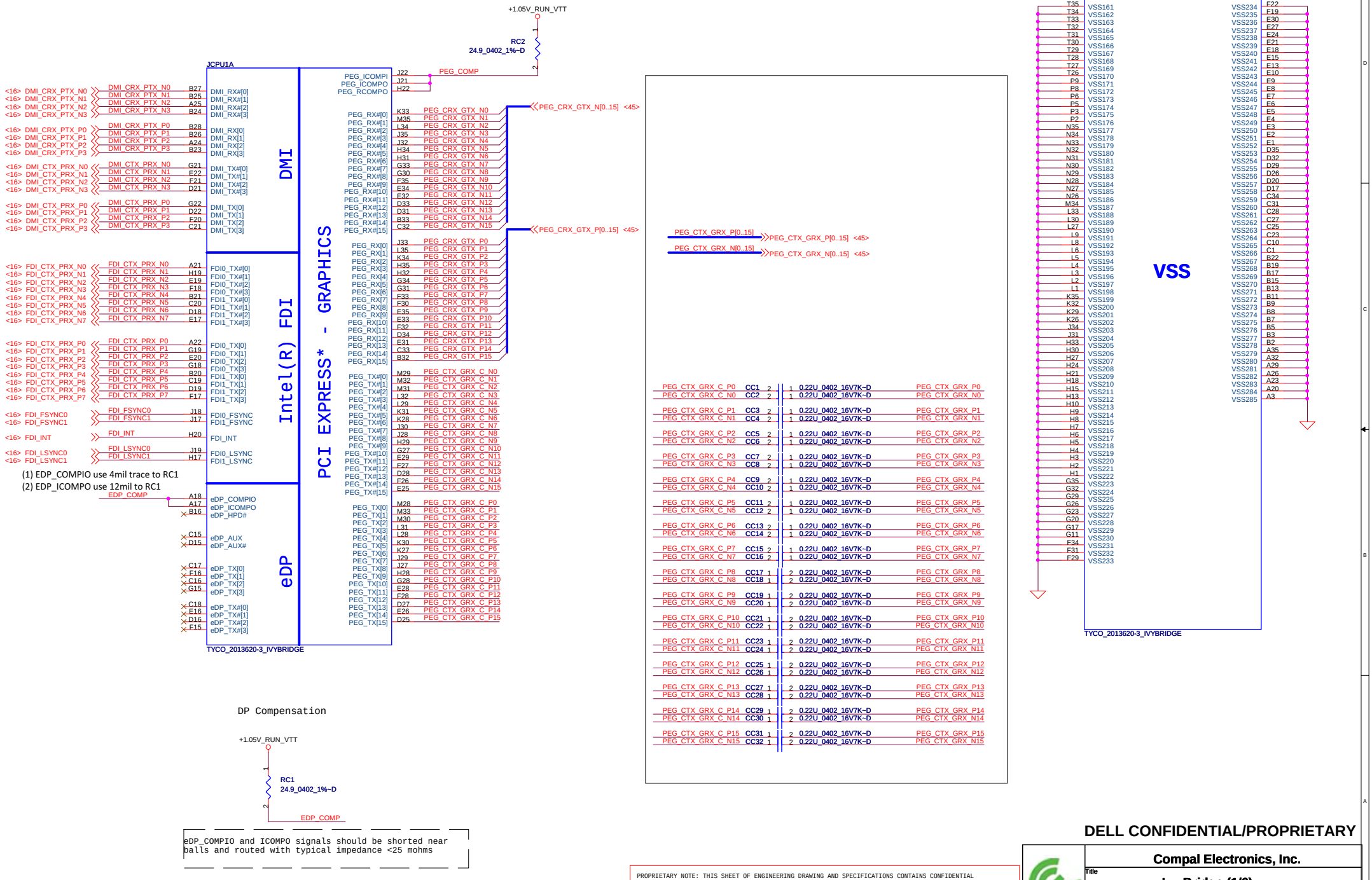
(1)PEG_RCOMPO (H22) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
(2)PEG_ICOMPO use 12mil connect to RC2



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Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

Size: | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 6 of 66

Follow DG Rev0.71 SM_DRAMPWROK topology

+1.5V_CPU_VDDQ

+3.3V_ALW_PCH

CC156 0.1U_0402_25V6K~D

UC2

<40,41> RUNPWROK

RUNPWROK_AND

RC12 200_0402_1%~D

PM_DRAM_PWRGD_CPU

RC28 130_0402_1%~D

+3.3V_ALW_PCH RC18 200_0402_1%~D

<16> PM_DRAM_PWRGD

74AHC1G09GW_TSSOP5~D

RC64 @ 39_0402_5%~D

<11,43> RUN_ON_CPU1.5VS3#

QC1@ SSM3K7002FU_SC70-3~D

INTEL suggest RC64 and QC1 NO stuff by default

+3.3V_ALW_PCH

@RC124 1K_0402_1%~D

SYS_PWROK_XDP

+1.05V_RUN_VTT

0.1U_0402_25V6K~D CC65

0.1U_0402_25V6K~D CC66

Place near JXDP1

+1.05V_RUN_VTT

JXDP1

GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16

GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 GND15 TDO TRST# TDI TMS GND17

SAMTE_BSH-030-01-L-D-A CONN@

XDP_PREQ# XDP_PRDY# XDP_OBS0 XDP_OBS1 XDP_OBS2 XDP_OBS3 CFG10 CFG11 XDP_OBS4 XDP_OBS5 XDP_OBS6 XDP_OBS7 XDP_TCLK

CFG16 CFG17 CFG0 CFG1 CFG2 CFG3 CFG8 CFG9 CFG4 CFG5 CFG6 CFG7 CLK_XDP CLK_XDP# XDP_RST#_R XDP_DBRESET# XDP_TDO XDP_TRST# XDP_TDI XDP_TMS

The resistor for HOOK2 should beplaced such that the stub is very small on CFG0 net

H_CPUPWRGD RC51 1K_0402_1%~D H_CPUPWRGD_XDP

<14,16> SIO_PWRBTN#_R RC6 0_0402_5%~D CFD_PWRBTN#_XDP

CFG0 RC71 1K_0402_1%~D XDP_HOOK2

<16,40> SYS_PWROK @RC9 0_0402_5%~D SYS_PWROK_XDP

<12,13,14,15,28,35> DDR_XDP_WAN_SMBDAT RC1251 0_0402_5%~D DDR_XDP_SMBDAT_R1

<12,13,14,15,28,35> DDR_XDP_WAN_SMBCLK RC127 0_0402_5%~D DDR_XDP_SMBCLK_R1

+1.05V_RUN_VTT

@RC126 56_0402_5%~D H_THERMTRIP#

@RC128 49.9_0402_1%~D H_CATERR#

RC44 62_0402_5%~D H_PROCHOT#

JCPU1B

Follow check list 0.5

<18> H_SNB_IVB# C26 PROC_SELECT#

<40> CPU_DETECT# AN34 SKTOCC#

MISC

H_CATERR# AL33 CATERR#

<41> PECI_EC AN33 PECI

VR1 TOPOLOGY

<41,60,62> H_PROCHOT# RC57 56_0402_5%~D H_PROCHOT#_R AL32 PROCHOT#

Close to JCPU1

<22> H_THERMTRIP# RC129 0_0402_5%~D H_THERMTRIP#_R AN32 THERMTRIP#

place RC129 near CPU

THERMAL

<16> H_PM_SYNC H_PM_SYNC AM34 PM_SYNC

<18> H_CPUPWRGD RC25 0_0402_5%~D VCCPWRGOOD_0_R AP33 UNCOREPWRGOOD

PM_DRAM_PWRGD_CPU V8 SM_DRAMPWROK

PCH_PLTRST#_R AR33 RESET#

PWR MANAGEMENT

CLOCKS

BCLK BCLK# A28 CPU_DMI A27 CPU_DMI# RC13 RC15 0_0402_5%~D CLK_CPU_DMI <15> CLK_CPU_DMI# <15>

DPLL_REF_CLK DPLL_REF_CLK# A16 CPU_DPLL A15 CPU_DPLL# RC16 RC17 1K_0402_1%~D +1.05V_RUN_VTT

Remove DPLL Ref clock (for eDP only)

XDP_RST#_R RC8 1K_0402_1%~D PLTRST_XDP# <17>

@RC48 0_0402_5%~D

CLK_XDP RH107 0_0402_5%~D CLK_CPU_ITP <15>

CLK_XDP# RH106 0_0402_5%~D CLK_CPU_ITP# <15>

DDR3 MISC

SM_DRAMRST# R8 DDR3_DRAMRST#_CPU

QC2 BSS138W-7-F_SOT323-3~D

DDR3_DRAMRST# <12>

<9> CLK_XDP_ITP @RH109 0_0402_5%~D

<9> CLK_XDP_ITP# @RH108 0_0402_5%~D

SM_RCOMP0 SM_RCOMP1 SM_RCOMP2

Max 500mils

SM_RCOMP2 --> 15mil

SM_RCOMP1/0 --> 20mil

RC50 4.99K_0402_1%~D

DDR_HVREF_RST

CC177 0.047U_0402_16V4Z~D

JTAG & BPM

PRDY# AP29 XDP_PRDY# PREQ# AP27 XDP_PREQ#

TCK AR26 XDP_TCLK TMS AR27 XDP_TMS TRST# AP30 XDP_TRST#

TDI AR28 XDP_TDI_R TDO AR26 XDP_TDO_R

<15> DDR_HVREF_RST_PCH RC46 0_0402_5%~D

<41> DDR_HVREF_RST_GATE @RC47 0_0402_5%~D

DDR_HVREF_RST <12>

M3 control

DBR# AL35 XDP_DBRESET#_R RC26 0_0402_5%~D XDP_DBRESET# <14,16>

BPM#[0] AT28 XDP_OBS0_R RC30 XDP_OBS0

BPM#[1] AR29 XDP_OBS1_R RC31 XDP_OBS1

BPM#[2] AR30 XDP_OBS2_R RC33 XDP_OBS2

BPM#[3] AT30 XDP_OBS3_R RC34 XDP_OBS3

BPM#[4] AP32 XDP_OBS4_R RC36 XDP_OBS4

BPM#[5] AR31 XDP_OBS5_R RC37 XDP_OBS5

BPM#[6] AT31 XDP_OBS6_R RC38 XDP_OBS6

BPM#[7] AR32 XDP_OBS7_R RC39 XDP_OBS7

0_0402_5%~D

For ESD concern, please put near CPU

XDP_TDI_R RC23 0_0402_5%~D XDP_TDI

XDP_TDO_R RC24 0_0402_5%~D XDP_TDO

TYCO_2013620-3_IVYBRIDGE

PU/PD for JTAG signals

+3.3V_RUN

XDP_DBRESET RC19 1K_0402_1%~D

+1.05V_RUN_VTT

XDP_TMS RC27 51_0402_1%~D

XDP_TDI RC29 51_0402_1%~D

XDP_PREQ# @RC32 51_0402_1%~D

XDP_TDO RC35 51_0402_1%~D

XDP_TCLK RC40 51_0402_1%~D

XDP_TRST# RC41 51_0402_1%~D

Buffered reset to CPU

+3.3V_RUN

+1.05V_RUN_VTT

0.1U_0402_25V6K~D CC140

UC1

<14,17> PCH_PLTRST#

NC VCC A GND Y

SN74LVC1G07DCKR_SC70-5~D

PCH_PLTRST#_BUF

75_0402_1%~D RC4

RC10

PCH_PLTRST#_R 43_0402_5%~D

Open drain buffer

VCCPWRGOOD_0_R

RC130 10K_0402_5%~D

Avoid stub in the PWRGD path while placing resistors RC25 & RC130

SM_RCOMP2 SM_RCOMP1 SM_RCOMP0

RC42 140_0402_1%~D

RC43 25.5_0402_1%~D

RC45 200_0402_1%~D

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Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

Size | Document Number: LA-7782 | Rev: 0.1

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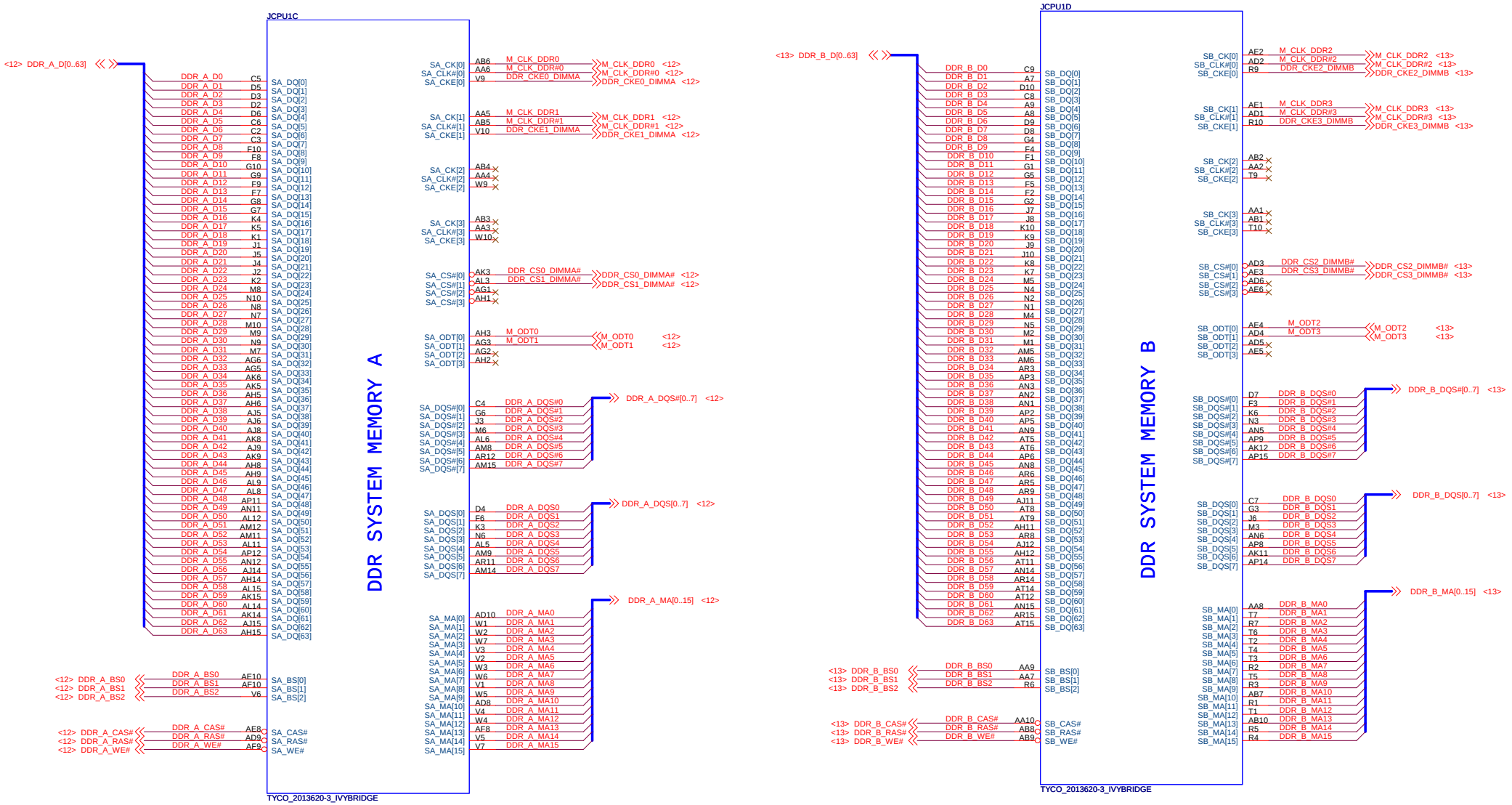

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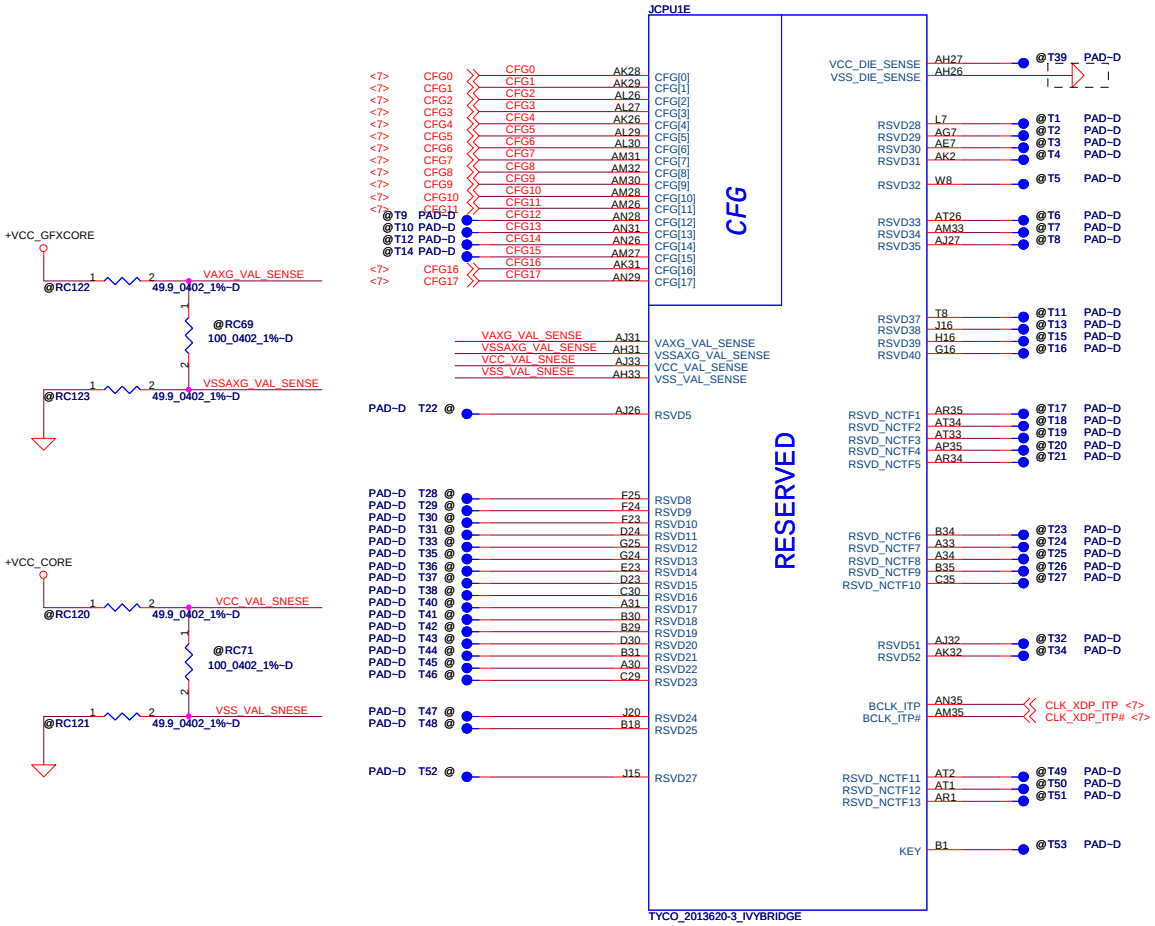
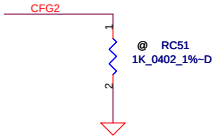
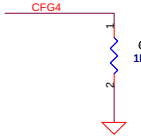
CFG Straps for Processor

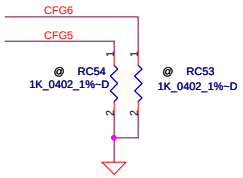




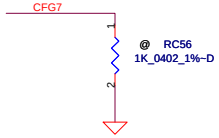
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

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Date: Friday, June 10, 2011 | Sheet 9 of 66

POWER

JCPU1F

+VCC_CORE
94A

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

CORE SUPPLY

PEG AND DDR

+1.05V_RUN_VTT
8.5A

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

SVID

Note: Place the PU resistors close to CPU
RC61 close to CPU 300 - 1500mils

+1.05V_RUN_VTT
RC60 75_0402_1%~D
H_CPU_SVIDALRT# — RC61 43_0402_5%~D — VIDALERT_N <60>

+1.05V_RUN_VTT
RC63 130_0402_1%~D

CAD Note: Place the PU
resistors close to CPU
RC63 close to CPU 300 - 1500mils

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VIDSCLK — VIDSCLK <60>
VIDSOUT AJ28 VIDSOUT — VIDSOUT <60>

H_CPU_SVIDALRT# must be routed between the VIDSOUT and VIDSCLK lines to reduce cross talk. 18 mils spacing to others.

SENSE LINES

Place RC66, RC70, RC75 near CPU

+VCC_CORE
@RC75 100_0402_1%~D
RC66 100_0402_1%~D
RC70 100_0402_1%~D

VCC_SENSE AJ35 VCCSENSE_R — RC67 0_0402_5%~D — VCCSENSE <60>
VSS_SENSE AJ34 VSSSENSE_R — RC68 0_0402_5%~D — VSSSENSE <60>

+1.05V_RUN_VTT
RC98 10_0402_1%~D

VCCIO_SENSE B10 VTT_SENSE — VTT_SENSE <58>
VSS_SENSE_VCCIO A10 VSSIO_SENSE_R — VSSIO_SENSE_R <58>

RC133 10_0402_1%~D

TYCO_2013620-3_IVYBRIDGE

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

* Description

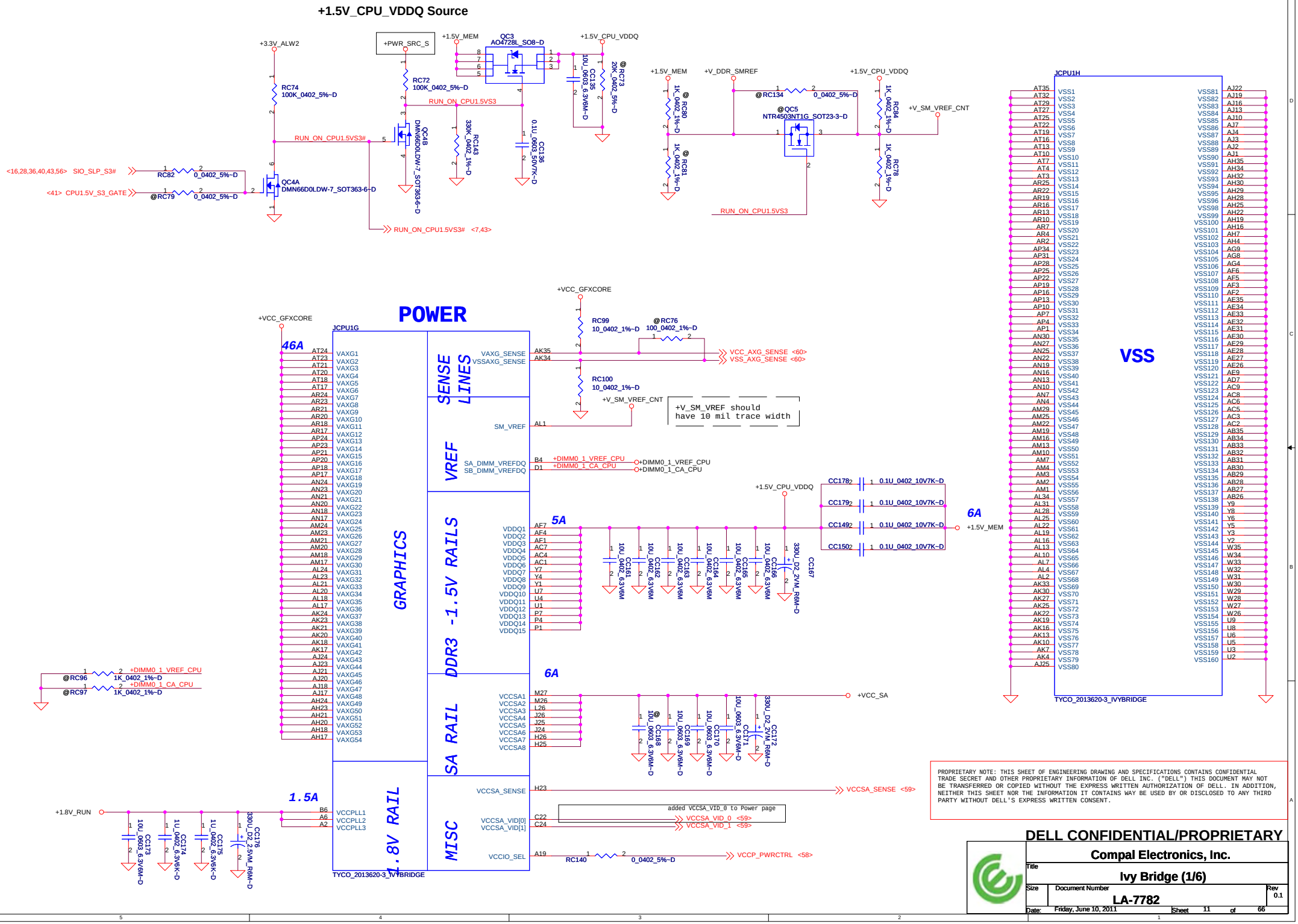
5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

Size | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 10 of 66



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Title	Ivy Bridge (1/6)
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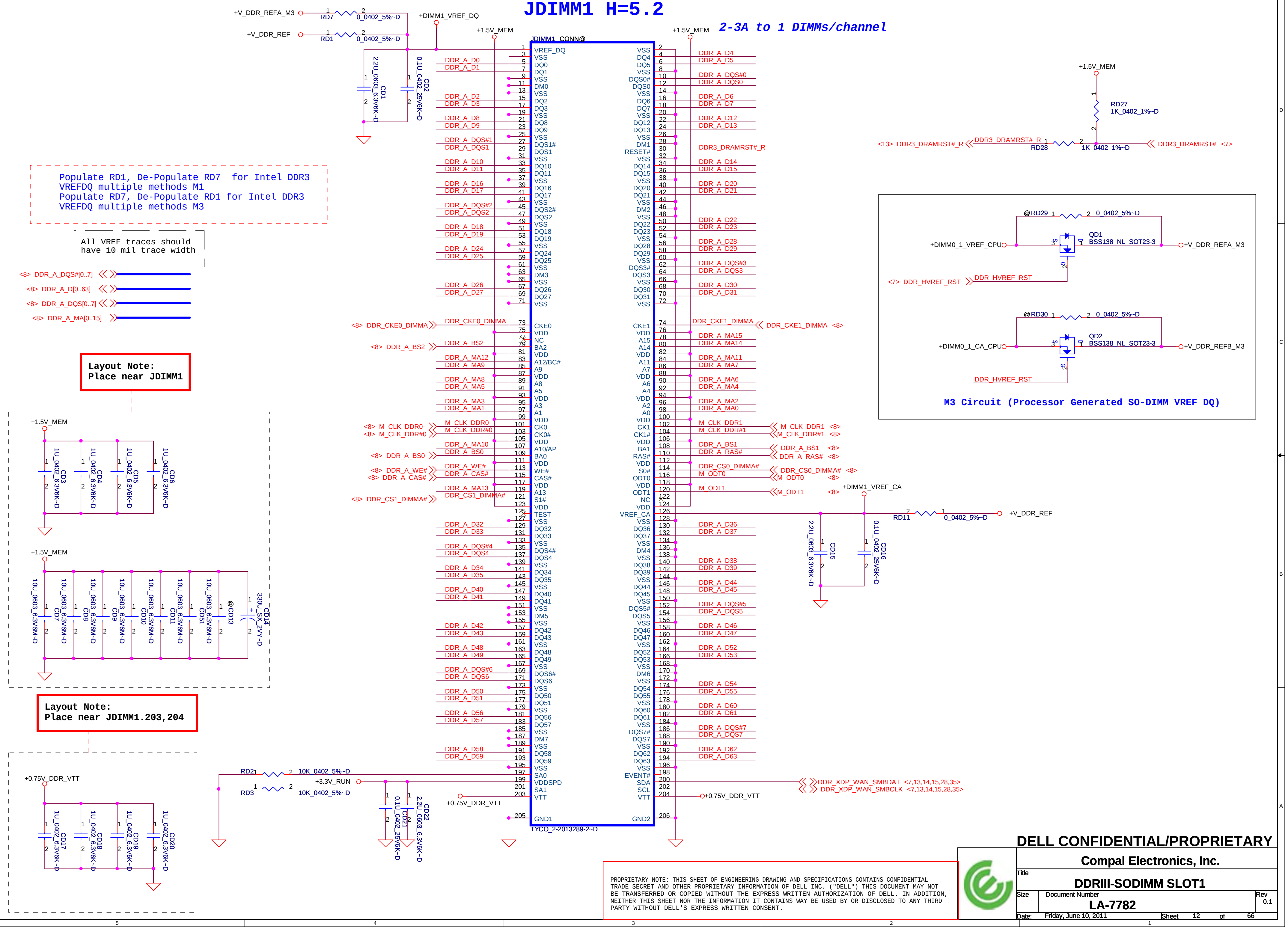
JDIMM1 H=5.2

2-3A to 1 DIMMs/channel



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Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

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2-3A to 1 DIMMs/channel

JDIMM2 H=9.2

Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

<8> DDR_B_DQS#[0..7]
<8> DDR_B_D[0..63]
<8> DDR_B_DQS[0..7]
<8> DDR_B_MA[0..15]

Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM2.203,204

+V_DDR_REFB_M3 — RD8 0_0402_5%~D
+V_DDR_REF — RD4 0_0402_5%~D
+DIMM2_VREF_DQ — CD23 2.2U_0603_6.3V6K~D, CD24 0.1U_0402_25V6K~D

JDIMM2_CONN@
TYCO_2-2013310-2~D

+1.5V_MEM — CD25 1U_0402_6.3V6K~D, CD26 1U_0402_6.3V6K~D, CD27 1U_0402_6.3V6K~D, CD28 1U_0402_6.3V6K~D

+1.5V_MEM — CD29 10U_0603_6.3V6M~D, CD30 10U_0603_6.3V6M~D, CD31 10U_0603_6.3V6M~D, CD32 10U_0603_6.3V6M~D, CD33 10U_0603_6.3V6M~D, CD34 10U_0603_6.3V6M~D, CD35 10U_0603_6.3V6M~D, CD36 330U_SX_2V~D

+0.75V_DDR_VTT — CD39 1U_0402_6.3V6K~D, CD40 1U_0402_6.3V6K~D, CD41 1U_0402_6.3V6K~D, CD42 1U_0402_6.3V6K~D

+3.3V_RUN — RD5 10K_0402_5%~D
+0.75V_DDR_VTT — RD6 10K_0402_5%~D, CD43 0.1U_0402_25V6K~D, CD44 2.2U_0603_6.3V6K~D

+DIMM2_VREF_CA — RD15 0_0402_5%~D +V_DDR_REF
CD37 2.2U_0603_6.3V6K~D
CD38 0.1U_0402_25V6K~D

DDR3_DRAMRST#_R <12>
DDR_CKE2_DIMMB <8>
DDR_CKE3_DIMMB <8>
M_CLK_DDR3 <8>
M_CLK_DDR#3 <8>
DDR_B_BS1 <8>
DDR_B_RAS# <8>
DDR_CS2_DIMMB# <8>
M_ODT2 <8>
M_ODT3 <8>
DDR_XDP_WAN_SMBDAT <7,12,14,15,28,35>
DDR_XDP_WAN_SMBCLK <7,12,14,15,28,35>
+0.75V_DDR_VTT

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Title: DDRIII-SODIMM SLOT2

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CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

PCH_AZ_SYNC is sampled at the rising edge of RSMRST# pin. So signal should be PU to the ALWAYS rail.

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs

CMOS place near DIMM

Follow INTEL CRB 0.7

INTEL HDA_SYNC isolation circuit

No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

BBS_BIT0 - BIOS BOOT STRAP BIT 0

200 MIL SO8
64Mb Flash ROM
W25Q64CVSSIG_SO8~D

200 MIL SO8
16Mb Flash ROM
W25Q32BVSSIG_SO8~D

HRS_FH12-16S-0P5SH(55)~D
CONN@

SAMTE_BSH-030-01-L-D-A CONN@

BD82PPSM-QNHN-A0_BGA989~D

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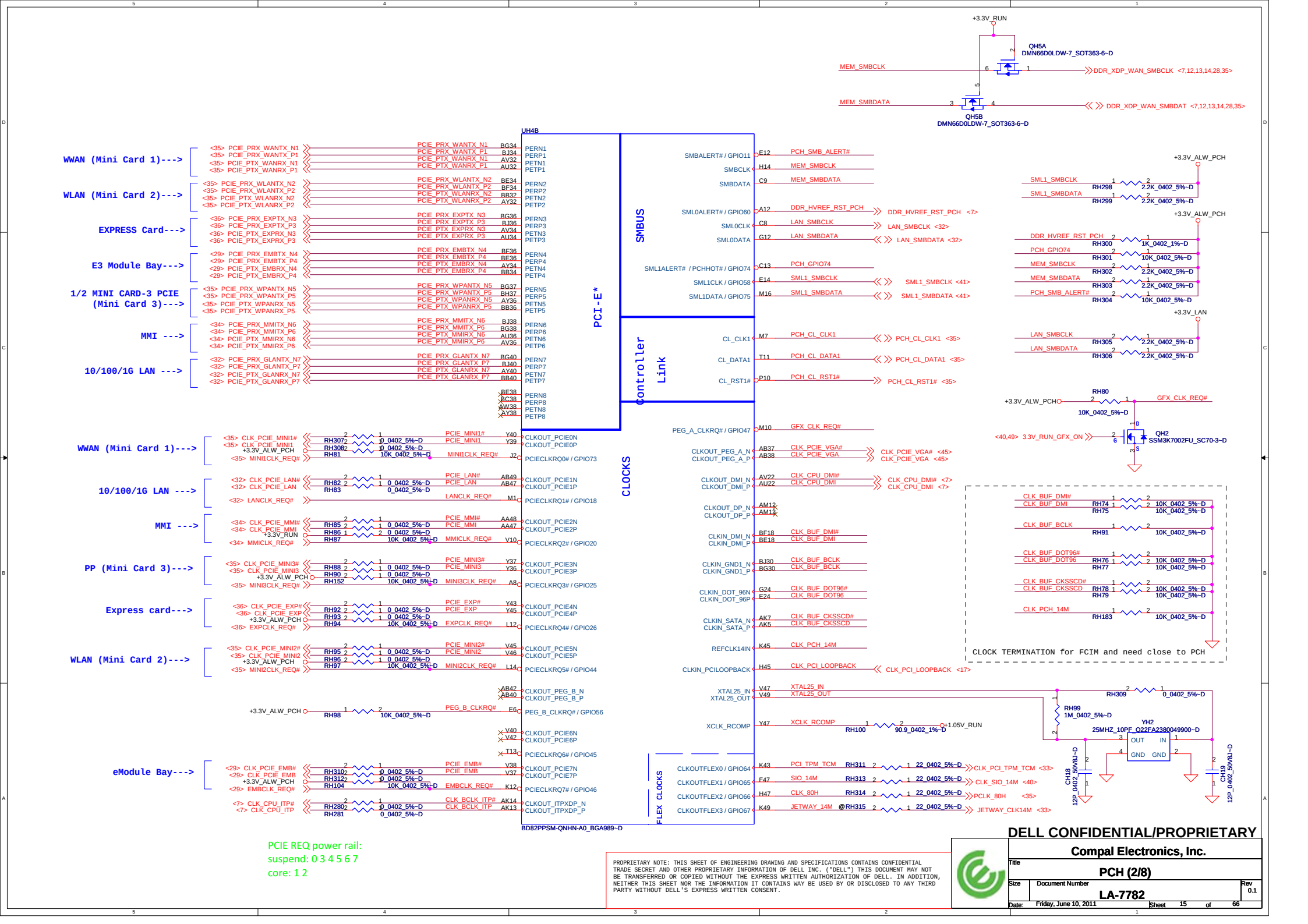
Compal Electronics, Inc.

Title: PCH (1/8)

Size: | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 14 of 66



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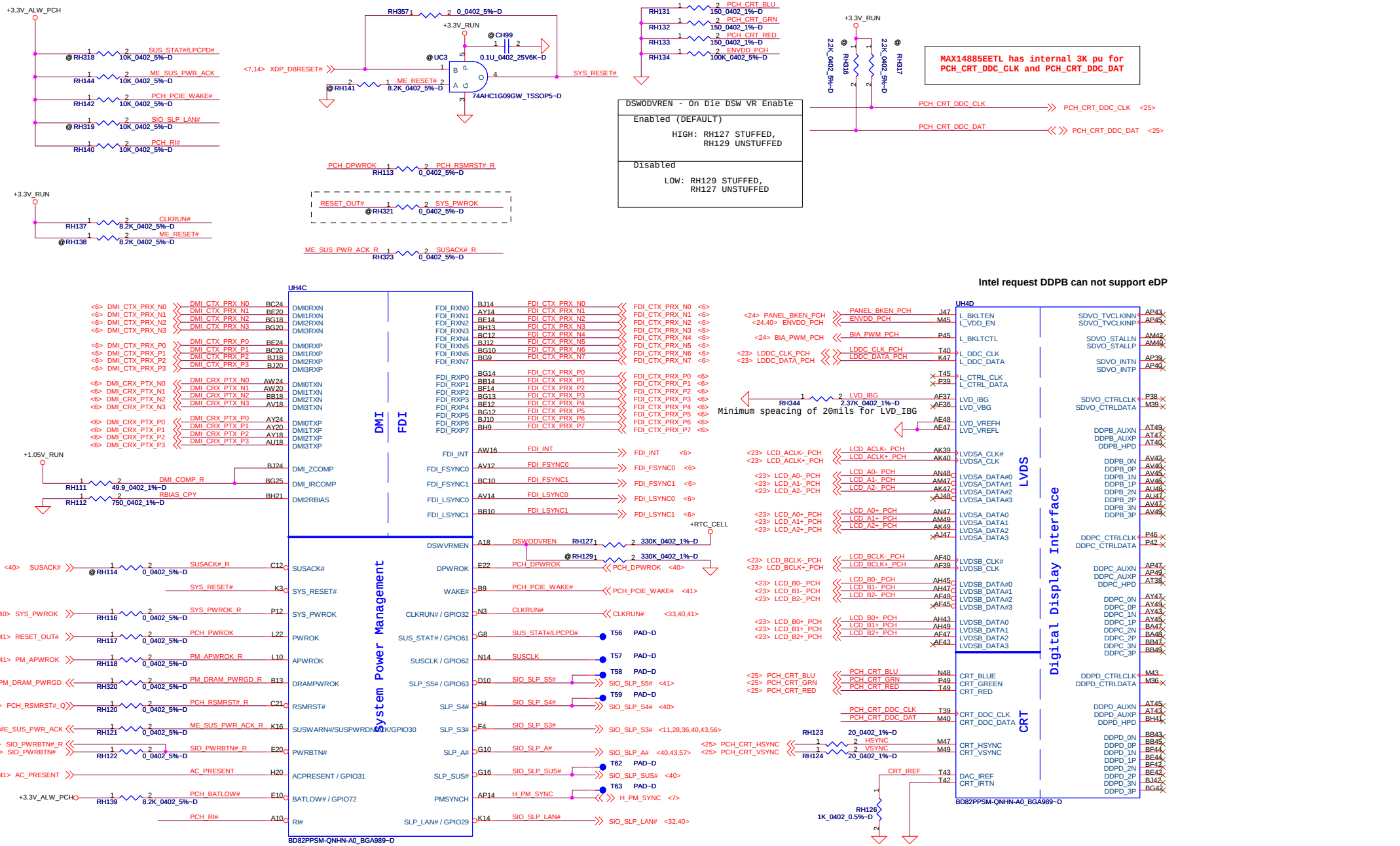
Title: PCH (2/8)

Size: | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 15 of 66



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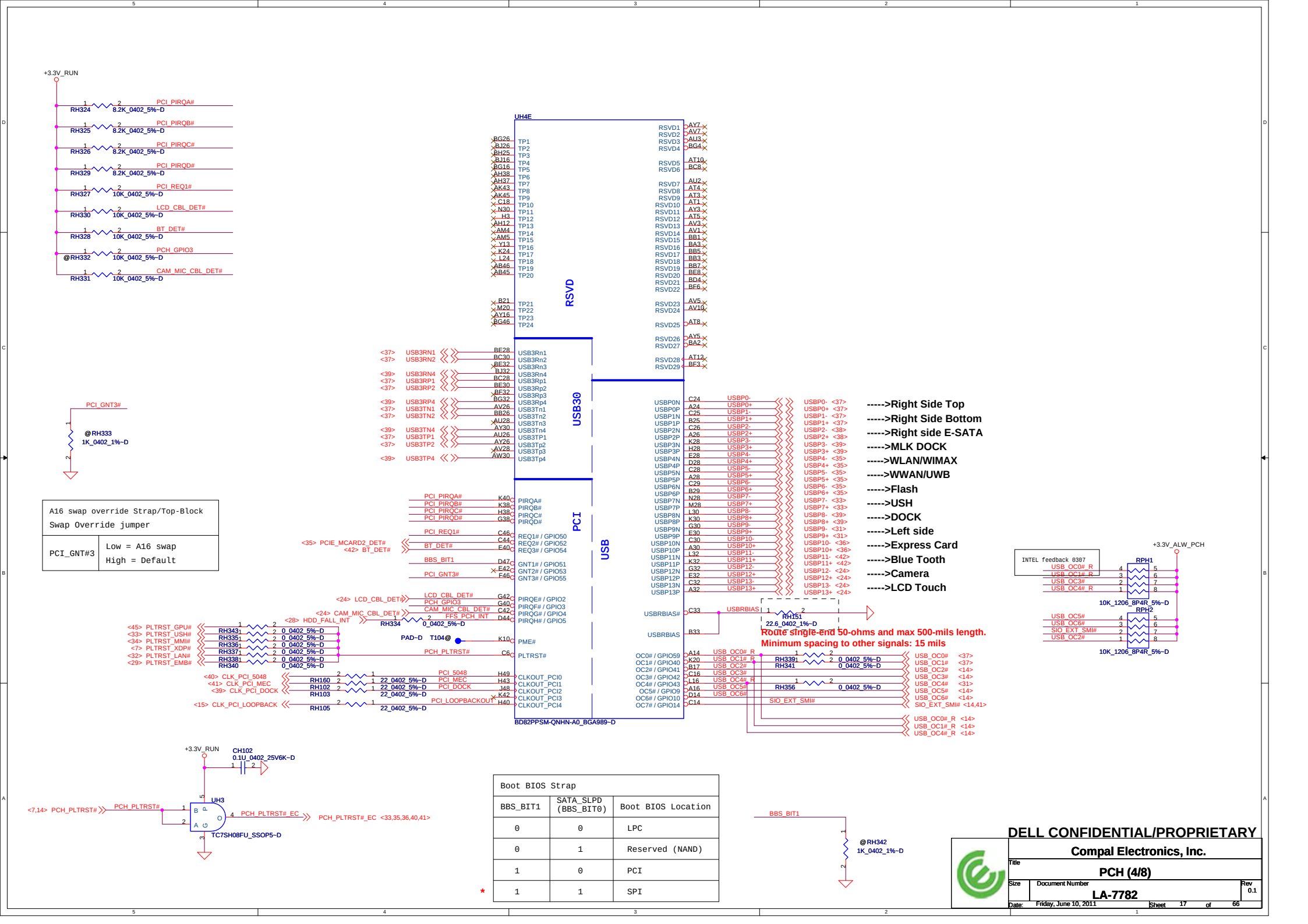
Title	PCH (3/8)	
Size	Document Number: LA-7782	Rev: 0.1
Date: Friday, June 10, 2011	Sheet 16 of 66	


+3.3V_RUN
RH324 8.2K_0402_5%~D PCI_PIRQA#
RH325 8.2K_0402_5%~D PCI_PIRQB#
RH326 8.2K_0402_5%~D PCI_PIRQC#
RH329 8.2K_0402_5%~D PCI_PIRQD#
RH327 10K_0402_5%~D PCI_REQ1#
RH330 10K_0402_5%~D LCD_CBL_DET#
RH328 10K_0402_5%~D BT_DET#
@RH332 10K_0402_5%~D PCH_GPIO3
RH331 10K_0402_5%~D CAM_MIC_CBL_DET#
PCI_GNT3#
@RH333 1K_0402_1%~D
A16 swap override Strap/Top-Block
Swap Override jumper
PCI_GNT3# Low = A16 swap
High = Default
UH4E
RSVD
USB30
PCI
USB
BD82PPSM-QNHN-A0_BGA989~D
USB3Rn1 USB3Rn2 USB3Rn3 USB3Rn4 USB3Rp1 USB3Rp2 USB3Rp3 USB3Rp4 USB3Tn1 USB3Tn2 USB3Tn3 USB3Tn4 USB3TP1 USB3Tp2 USB3Tp3 USB3Tp4
PIRQA# PIRQB# PIRQC# PIRQD#
REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54
GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55
PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5
PME#
PLTRST#
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4
USBP0- USBP0+ USBP1- USBP1+ USBP2- USBP2+ USBP3- USBP3+ USBP4- USBP4+ USBP5- USBP5+ USBP6- USBP6+ USBP7- USBP7+ USBP8- USBP8+ USBP9- USBP9+ USBP10- USBP10+ USBP11- USBP11+ USBP12- USBP12+ USBP13- USBP13+
USBRBIAS
USBRBIAS~
OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14
RH151 22.6_0402_1%~D
Route single-end 50-ohms and max 500-mils length.
Minimum spacing to other signals: 15 mils
RH3391 RH341 RH356 0_0402_5%~D
INTEL feedback 0307
RPH1 RPH2 10K_1206_8P4R_5%~D
+3.3V_ALW_PCH
------>Right Side Top
------>Right Side Bottom
------>Right side E-SATA
------>MLK DOCK
------>WLAN/WIMAX
------>WWAN/UWB
------>Flash
------>USH
------>DOCK
------>Left side
------>Express Card
------>Blue Tooth
------>Camera
------>LCD Touch
RH343 RH335 RH336 RH337 RH338 RH340 0_0402_5%~D
RH334 0_0402_5%~D
PAD~D T104@
RH160 RH102 RH103 RH105 22_0402_5%~D
+3.3V_RUN CH102 0.1U_0402_25V6K~D
UH3 TC7SH08FU_SSOP5~D
PCH_PLTRST# PCH_PLTRST#_EC
BBS_BIT1 @RH342 1K_0402_1%~D
Boot BIOS Strap
BBS_BIT1 | SATA_SLPD (BBS_BIT0) | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved (NAND)
1 | 0 | PCI
1 | 1 | SPI
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Compal Electronics, Inc.
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+3.3V_ALW_PCH

RH53 4.7K_0402_5%~D

SLP_ME_CSW_DEV#

RH353 1K_0402_1%~D @

Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT DISABLED - LOW

<14> PCH_GPIO16
DBC_ENABLE for E4 12"

+3.3V_ALW_PCH

SIO_EXT_WAKE# — RH177 10K_0402_5%~D

PCH_GPIO15 — RH354 1K_0402_1%~D

INTEL feedback 0302

PCH_GPIO36 — RH174 10K_0402_5%~D

PCH_GPIO37 — RH172 10K_0402_5%~D

PCH_GPIO17 — @RH273 1K_0402_1%~D

PCH_GPIO16 — @RH265 10K_0402_5%~D

+3.3V_ALW_PCH

KB_DET# — RH170 10K_0402_5%~D

+3.3V_RUN

PCH_GPIO36 — @RH171 10K_0402_5%~D

PCH_GPIO37 — @RH173 1K_0402_1%~D

TEMP_ALERT# — RH266 10K_0402_5%~D

PCH_GPIO22 — RH181 10K_0402_5%~D

PCH_GPIO7 — RH178 10K_0402_5%~D

PCH_GPIO17 — RH269 8.2K_0402_5%~D

IO_LOOP# — RH163 10K_0402_5%~D

PCH_GPIO16 — RH272 10K_0402_5%~D

UH4F

<14> SIO_EXT_SCI#_R
<41> SIO_EXT_SCI# — SIO_EXT_SCI# RH259 0_0402_5%~D — T7 BMBUSY# / GPIO0
<33> USH_DET# — USH_DET# — A42 TACH1 / GPIO1
<31> IO_LOOP# — IO_LOOP# — H36 TACH2 / GPIO6
PCH_GPIO7 — E38 TACH3 / GPIO7
<40> SIO_EXT_WAKE# — C10 GPIO8
<32> PM_LANPHY_ENABLE — PM_LANPHY_ENABLE — C4 LAN_PHY_PWR_CTRL / GPIO12
<14> PCH_GPIO15 — PCH_GPIO15 — G2 GPIO15
<14> PCH_GPIO16 — PCH_GPIO16 — U2 SATA4GP / GPIO16
PCH_GPIO17 — D40 TACH0 / GPIO17
PCH_GPIO22 — T5 SCLOCK / GPIO22
<35> PCIE_MCARD1_DET# — E8 GPIO24
<24> E3_PAID_TS_DET# — E3_PAID_TS_DET# — E16 GPIO27
<14,40> SLP_ME_CSW_DEV# — SLP_ME_CSW_DEV# — P8 GPIO28
<45> DGPU_HOLD_RST# — DGPU_HOLD_RST# — K1 STP_PCI# / GPIO34
<14,35> USB_MCARD1_DET# — USB_MCARD1_DET# — K4 GPIO35
<14> PCH_GPIO36 — PCH_GPIO36 — V8 SATA2GP / GPIO36
<14> PCH_GPIO37 — PCH_GPIO37 — M5 SATA3GP / GPIO37
TPM_ID0 — N2 SLOAD / GPIO38
TPM_ID1 — M3 SDATAOUT0 / GPIO39
<28> FFS_INT2 — FFS_INT2 — V13 SDATAOUT1 / GPIO48
<14,40> TEMP_ALERT# — TEMP_ALERT# — V3 SATA5GP / GPIO49 / TEMP_ALERT#
<42> KB_DET# — KB_DET# — D6 GPIO57

GPIO

TACH4 / GPIO68 — C40 — CONTACTLESS_DET# — <CONTACTLESS_DET# <33>
TACH5 / GPIO69 — B41 — DGPU_PWROK <40,64>
TACH6 / GPIO70 — C41 — PCIE_MCARD3_DET# — <PCIE_MCARD3_DET# <35>
TACH7 / GPIO71 — A40 — USB_MCARD2_DET# <35>

CPU/MISC

A20GATE — P4 — SIO_A20GATE — <SIO_A20GATE <41>
PECI — AU16
RCIN# — P5 — SIO_RCIN# — <SIO_RCIN# <41>
PROCPWRGD — AY11 — H_CPUPWRGD — <H_CPUPWRGD <7>
THRMTRIP# — AY10 — PCH_THRMTRIP# R — RH262 56_0402_5%~D — +1.05V_RUN_VTT
INIT3_3V# — T14 — INIT3_3V# — PAD~D T106 @
DF_TVS — AY1 — DF_TVS — CH97 0.1U_0402_25V6K~D
TS_VSS1 — AH8
TS_VSS2 — AK11
TS_VSS3 — AH10
TS_VSS4 — AK10
NC_1 — P37 — NC_1 — PAD~D T108 @

+3.3V_RUN

SIO_A20GATE — RH158 10K_0402_5%~D

SIO_RCIN# — RH203 10K_0402_5%~D

SIO_EXT_SCI# — RH263 10K_0402_5%~D

USH_DET# — RH164 100K_0402_5%~D

+3.3V_RUN — CONTACTLESS_DET# — RH256 10K_0402_5%~D

NCTF

VSS_NCTF_1 A4 — VSS_NCTF_1
VSS_NCTF_2 A44 — VSS_NCTF_2
VSS_NCTF_3 A45 — VSS_NCTF_3
VSS_NCTF_4 A46 — VSS_NCTF_4
VSS_NCTF_5 A5 — VSS_NCTF_5
VSS_NCTF_6 A6 — VSS_NCTF_6
VSS_NCTF_7 B3 — VSS_NCTF_7
VSS_NCTF_8 B47 — VSS_NCTF_8
VSS_NCTF_9 BD1 — VSS_NCTF_9
VSS_NCTF_10 BD49 — VSS_NCTF_10
VSS_NCTF_11 BE1 — VSS_NCTF_11
VSS_NCTF_12 BE49 — VSS_NCTF_12
VSS_NCTF_13 BF1 — VSS_NCTF_13
VSS_NCTF_14 BF49 — VSS_NCTF_14

VSS_NCTF_15 BG2 — VSS_NCTF_15
VSS_NCTF_16 BG48 — VSS_NCTF_16
VSS_NCTF_17 BH3 — VSS_NCTF_17
VSS_NCTF_18 BH47 — VSS_NCTF_18
VSS_NCTF_19 BJ4 — VSS_NCTF_19
VSS_NCTF_20 BJ44 — VSS_NCTF_20
VSS_NCTF_21 BJ45 — VSS_NCTF_21
VSS_NCTF_22 BJ46 — VSS_NCTF_22
VSS_NCTF_23 BJ5 — VSS_NCTF_23
VSS_NCTF_24 BJ6 — VSS_NCTF_24
VSS_NCTF_25 C2 — VSS_NCTF_25
VSS_NCTF_26 C48 — VSS_NCTF_26
VSS_NCTF_27 D1 — VSS_NCTF_27
VSS_NCTF_28 D49 — VSS_NCTF_28
VSS_NCTF_29 E1 — VSS_NCTF_29
VSS_NCTF_30 E49 — VSS_NCTF_30
VSS_NCTF_31 F1 — VSS_NCTF_31
VSS_NCTF_32 F49 — VSS_NCTF_32

BD82PPSM-QNHN-A0_BGA989~D

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45°from the pad.

PLACE RH150 CLOSE TO THE BRANCHING POINT
(TO CPU and NVRAM CONNECTOR)

+VCCDFTERM

RH149 need to close to CPU

RH149 2.2K_0402_5%~D

<7> H_SNB_IVB# — RH150 0_0402_5%~D — DF_TVS_R — RH358 1K_0402_1%~D — DF_TVS

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

+3.3V_RUN

1@ RH267 10K_0402_5%~D — TPM_ID0

2@ RH270 10K_0402_5%~D

+3.3V_RUN

3@ RH268 20K_0402_5%~D — TPM_ID1

4@ RH271 2.2K_0402_5%~D

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1

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Title: **PCH (5/8)**

Size | Document Number: **LA-7782** | Rev: 0.1

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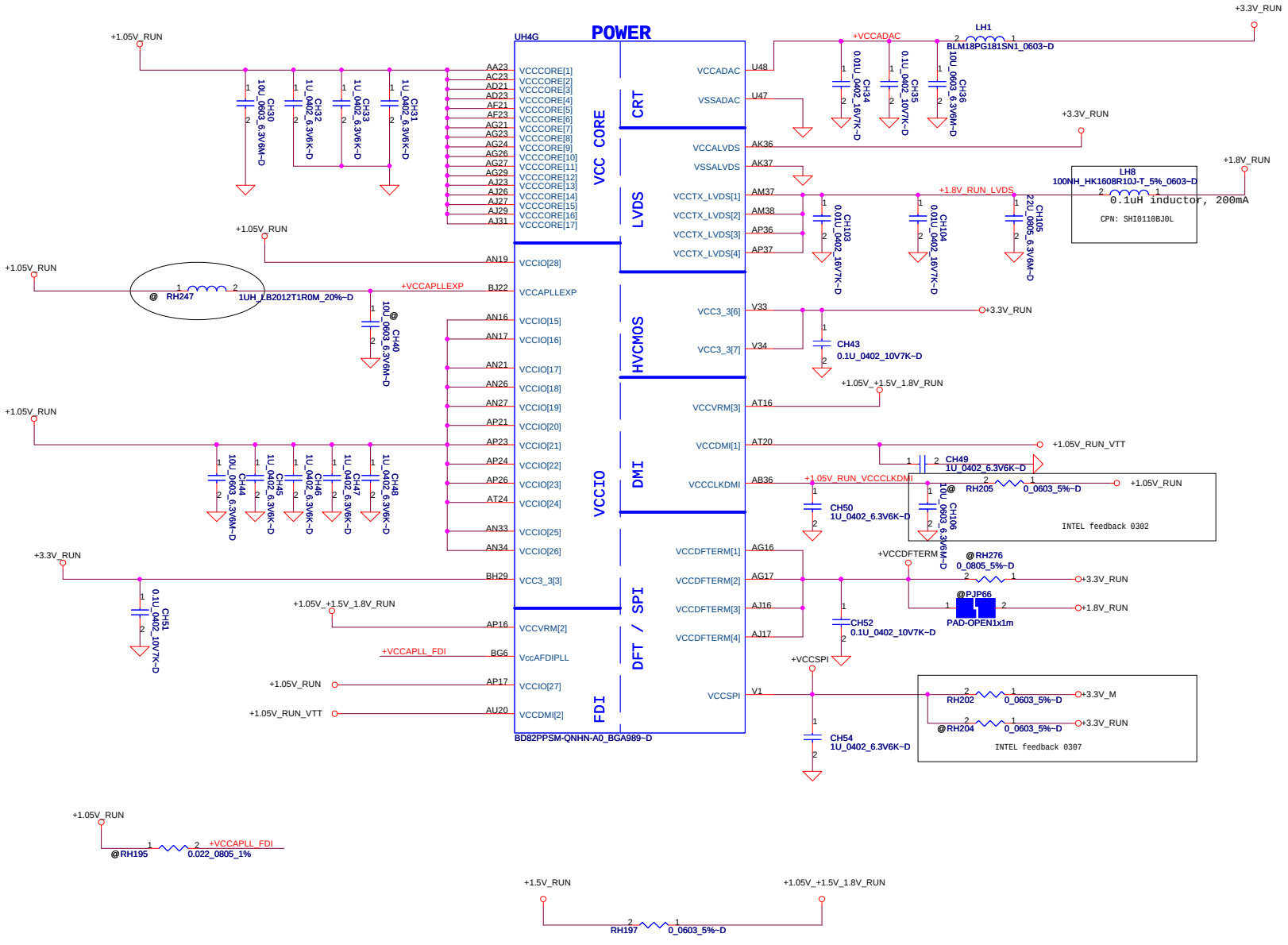


PCH Power Rail Table

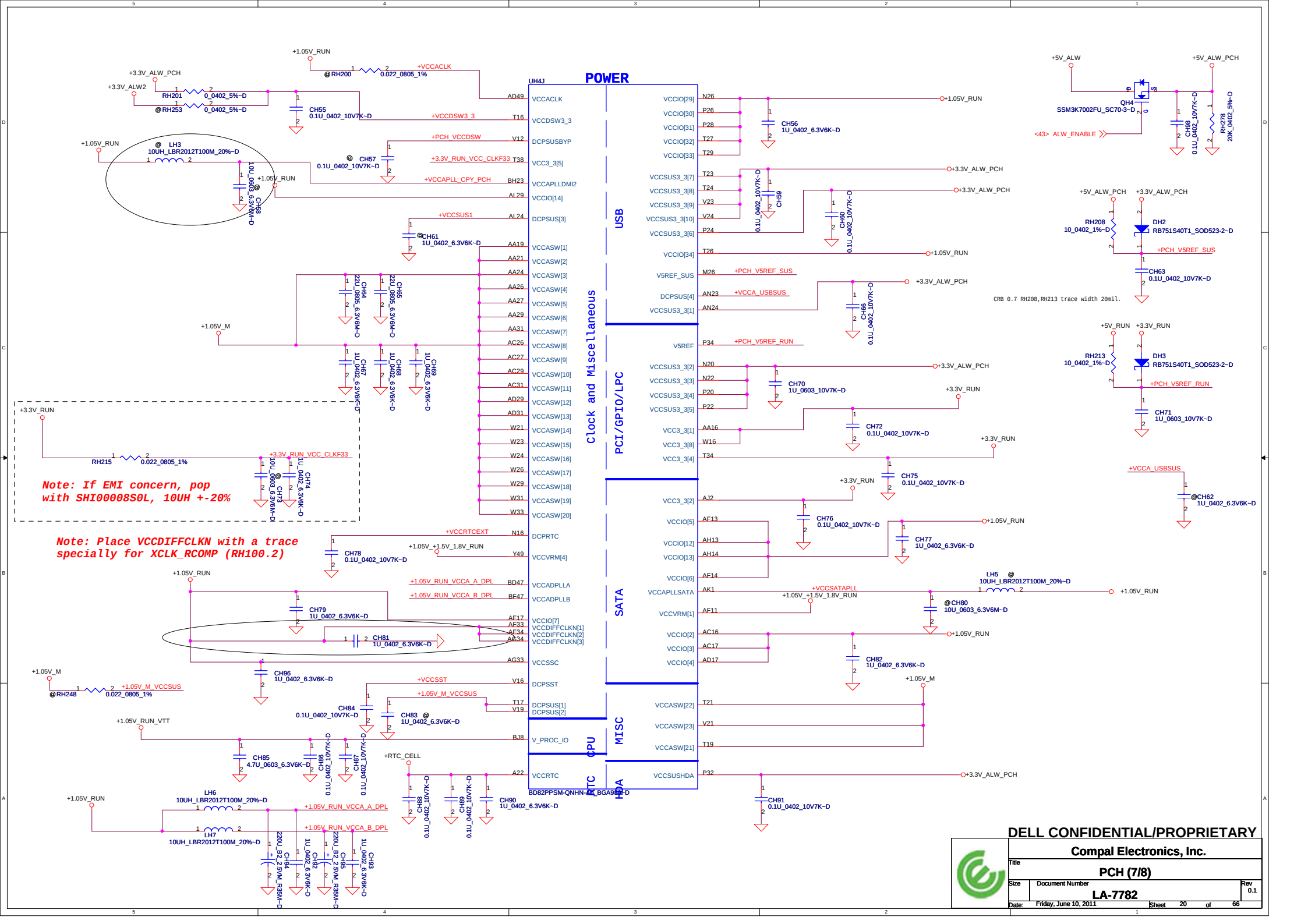
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (6/8)

Size | Document Number: LA-7782 | Rev: 0.1

Date: Tuesday, June 07, 2011 | Sheet 19 of 66


POWER
UH4J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
Note: If EMI concern, pop with SHI00008S0L, 10UH +-20%
Note: Place VCCDIFFCLKN with a trace specially for XCLK_RCOMP (RH100.2)
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Compal Electronics, Inc.
PCH (7/8)
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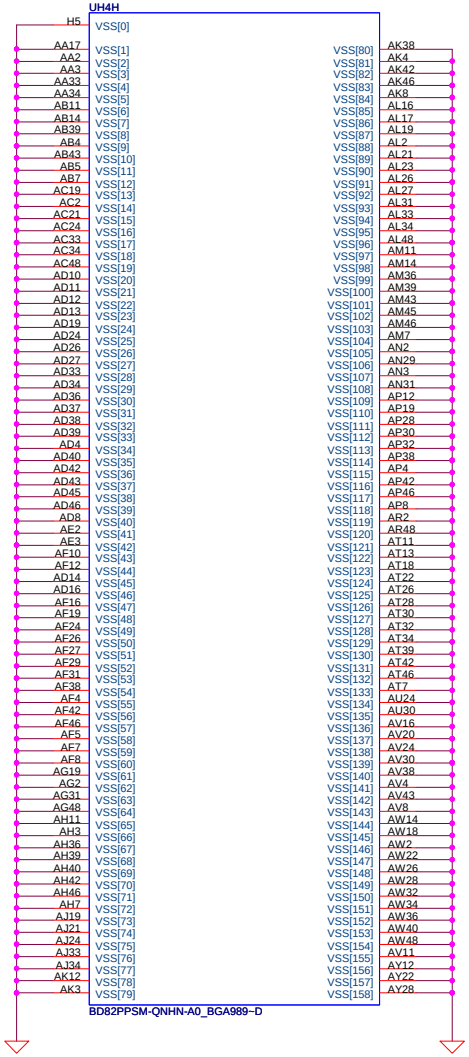

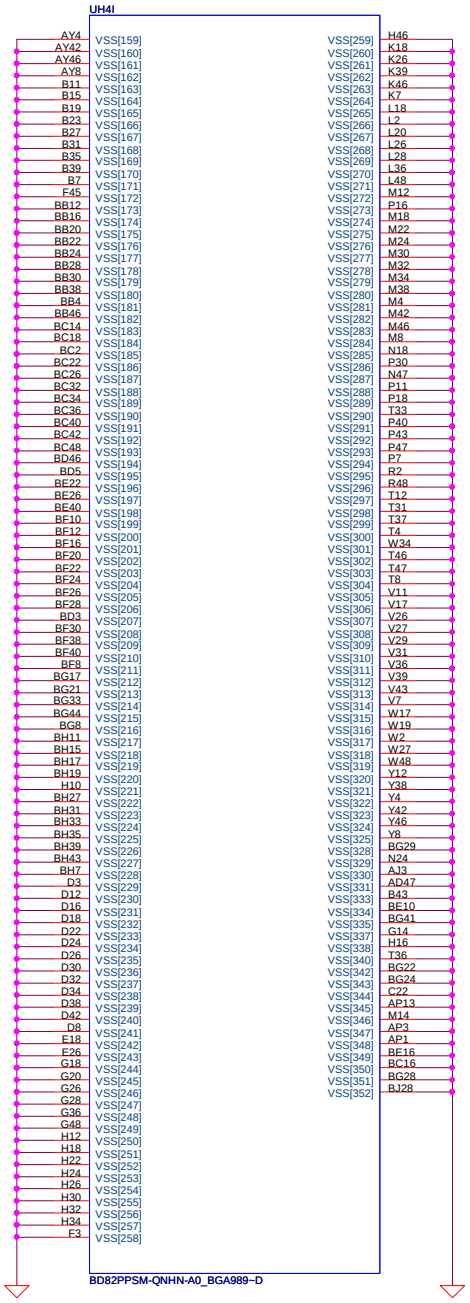

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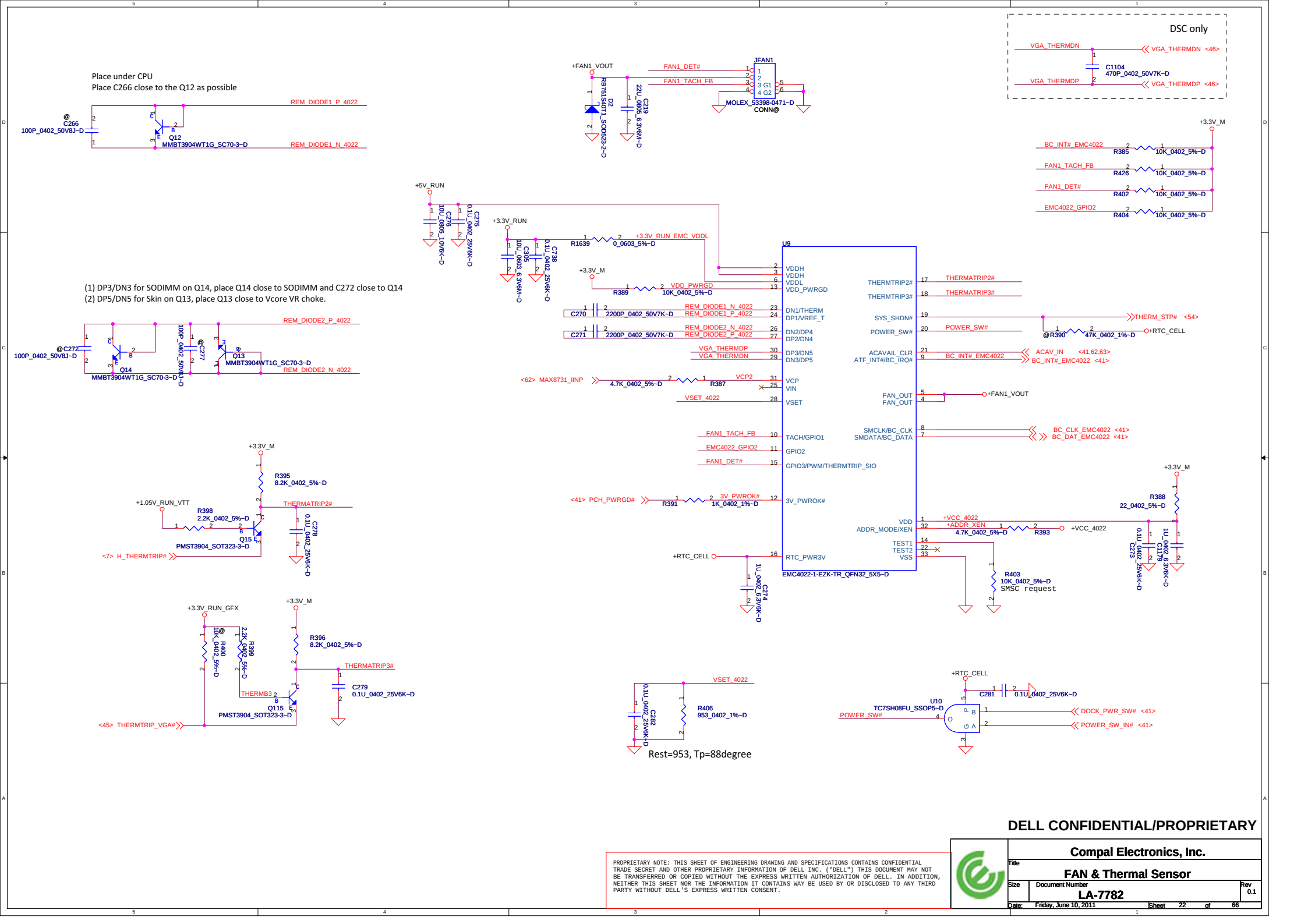
Title	PCH (8/8)	
Size	Document Number: LA-7782	Rev: 0.1
Date: Monday, May 23, 2011	Sheet 21 of 66	


Place under CPU
Place C266 close to the Q12 as possible
@ C266 100P_0402_50V8J~D
Q12 MMBT3904WT1G_SC70-3~D
REM_DIODE1_P_4022
REM_DIODE1_N_4022
(1) DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.
@C272 100P_0402_50V8J~D
Q14 MMBT3904WT1G_SC70-3~D
100P_0402_50V8J~D
@C277
Q13 MMBT3904WT1G_SC70-3~D
REM_DIODE2_P_4022
REM_DIODE2_N_4022
+FAN1_VOUT
RB751S40T1_SOD523-2~D
D3
C219 22U_0805_6.3V6M~D
FAN1_DET#
FAN1_TACH_FB
JFAN1
MOLEX_53398-0471~D
CONN@
DSC only
VGA_THERMDN
VGA_THERMDP
C1104 470P_0402_50V7K~D
VGA_THERMDN <46>
VGA_THERMDP <46>
+3.3V_M
BC_INT#_EMC4022
FAN1_TACH_FB
FAN1_DET#
EMC4022_GPIO2
R385 10K_0402_5%~D
R426 10K_0402_5%~D
R402 10K_0402_5%~D
R404 10K_0402_5%~D
+5V_RUN
C276 10U_0805_10V6K~D
C275 0.1U_0402_25V6K~D
+3.3V_RUN
C305 10U_0603_6.3V6M~D
C238 0.1U_0402_25V6K~D
R1639 0_0603_5%~D
+3.3V_RUN_EMC_VDDL
R389 10K_0402_5%~D
VDD_PWRGD
U9
VDDH
VDDL
VDD_PWRGD
DN1/THERM
DP1/VREF_T
DN2/DP4
DP2/DN4
DP3/DN5
DN3/DP5
VCP
VIN
VSET
TACH/GPIO1
GPIO2
GPIO3/PWM/THERMTRIP_SIO
3V_PWROK#
RTC_PWR3V
VDD
ADDR_MODE/XEN
TEST1
TEST2
VSS
THERMTRIP2#
THERMTRIP3#
SYS_SHDN#
POWER_SW#
ACAVAIL_CLR
ATF_INT#/BC_IRQ#
FAN_OUT
SMCLK/BC_CLK
SMDATA/BC_DATA
EMC4022-1-EZK-TR_QFN32_5X5~D
C270 2200P_0402_50V7K~D
C271 2200P_0402_50V7K~D
REM_DIODE1_N_4022
REM_DIODE1_P_4022
REM_DIODE2_N_4022
REM_DIODE2_P_4022
VGA_THERMDP
VGA_THERMDN
<62> MAX8731_IINP
4.7K_0402_5%~D
R387
VCP2
VSET_4022
<41> PCH_PWRGD#
R391 1K_0402_1%~D
3V_PWROK#
+RTC_CELL
C274 1U_0402_6.3V6K~D
THERMTRIP2#
THERMTRIP3#
THERM_STP# <54>
R390 47K_0402_1%~D
+RTC_CELL
POWER_SW#
ACAV_IN <41,62,63>
BC_INT#_EMC4022 <41>
+FAN1_VOUT
BC_CLK_EMC4022 <41>
BC_DAT_EMC4022 <41>
+VCC_4022
R393 4.7K_0402_5%~D
+ADDR_XEN
R403 10K_0402_5%~D
SMSC request
R388 22_0402_5%~D
C273 0.1U_0402_25V6K~D
C1179 1U_0402_6.3V6K~D
+3.3V_M
R395 8.2K_0402_5%~D
+1.05V_RUN_VTT
R398 2.2K_0402_5%~D
THERMATRIP2#
Q15 PMST3904_SOT323-3~D
<7> H_THERMTRIP#
C278 0.1U_0402_25V6K~D
+3.3V_RUN_GFX
@R400 10K_0402_5%~D
R399 2.2K_0402_5%~D
R396 8.2K_0402_5%~D
THERMATRIP3#
THERMB3
Q115 PMST3904_SOT323-3~D
<45> THERMTRIP_VGA#
C279 0.1U_0402_25V6K~D
VSET_4022
C282 0.1U_0402_25V6K~D
R406 953_0402_1%~D
Rest=953, Tp=88degree
+RTC_CELL
C281 0.1U_0402_25V6K~D
U10
TC7SH08FU_SSOP5~D
POWER_SW#
DOCK_PWR_SW# <41>
POWER_SW_IN# <41>
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PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
Compal Electronics, Inc.
Title
FAN & Thermal Sensor
Size
Document Number
LA-7782
Rev
0.1
Date: Friday, June 10, 2011
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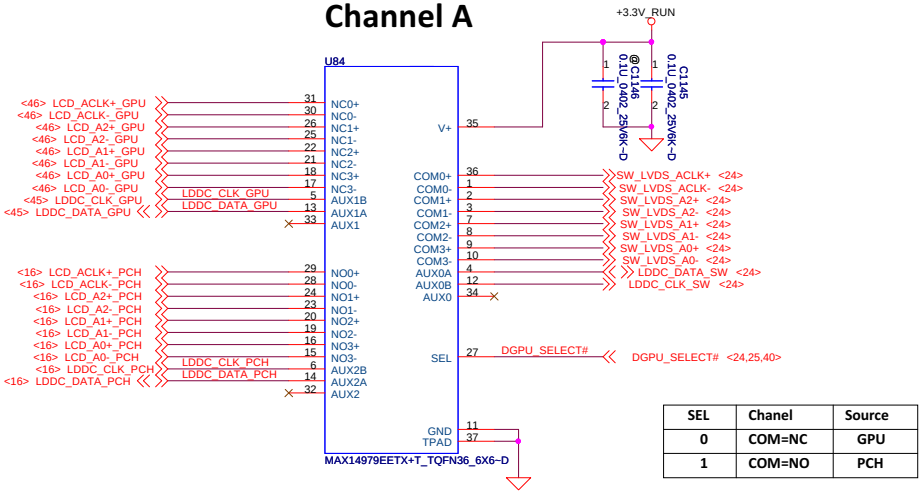
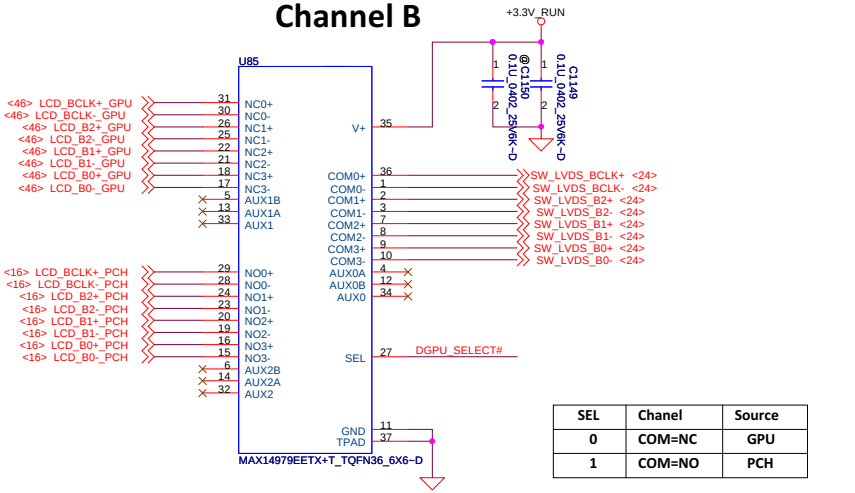
Channel A

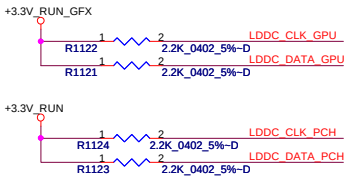


SEL	Chanel	Source
0	COM=NC	GPU
1	COM=NO	PCH

Channel B



SEL	Chanel	Source
0	COM=NC	GPU
1	COM=NO	PCH

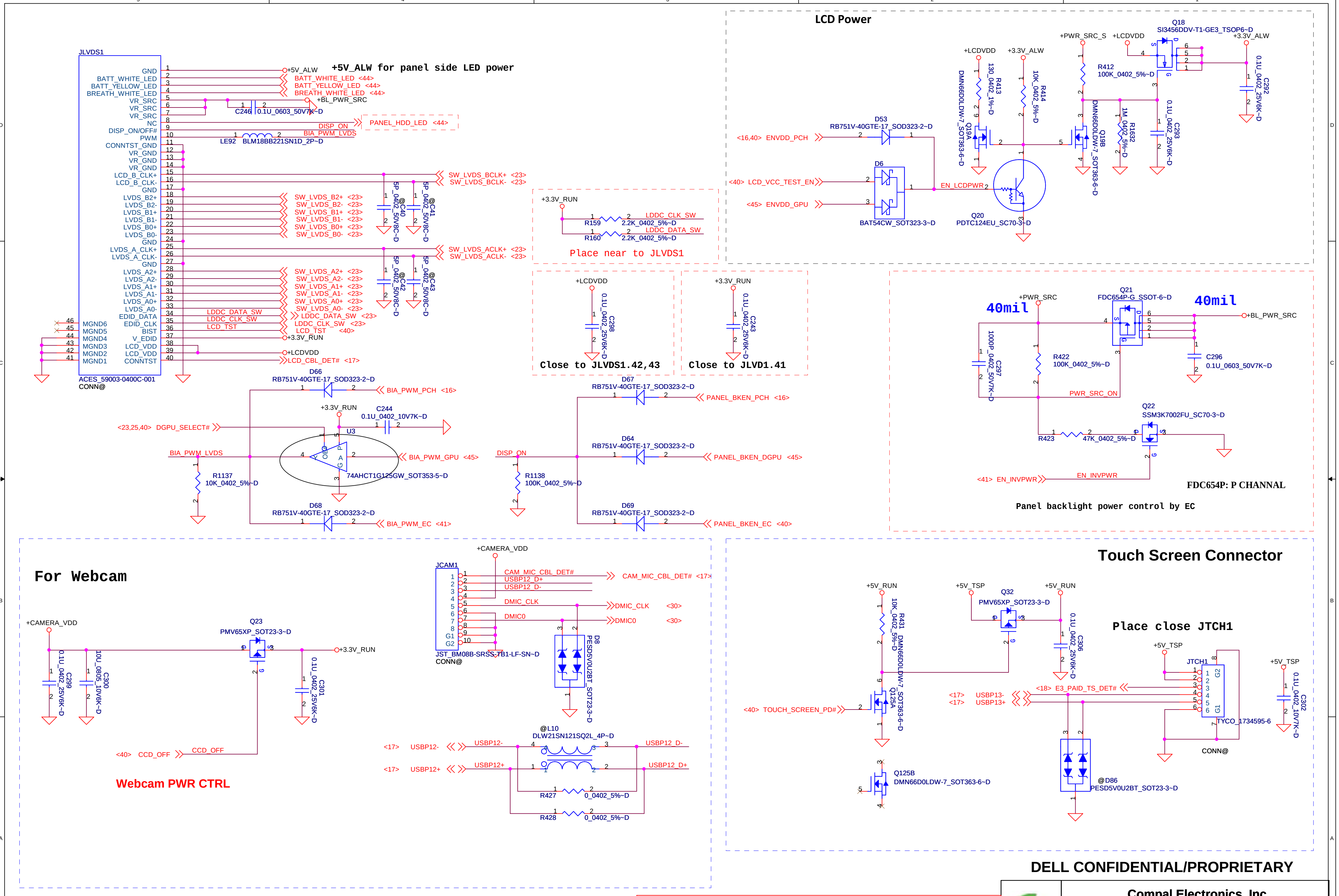


Compal Electronics, Inc.

Title: LVDS SW

Size | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 23 of 66



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

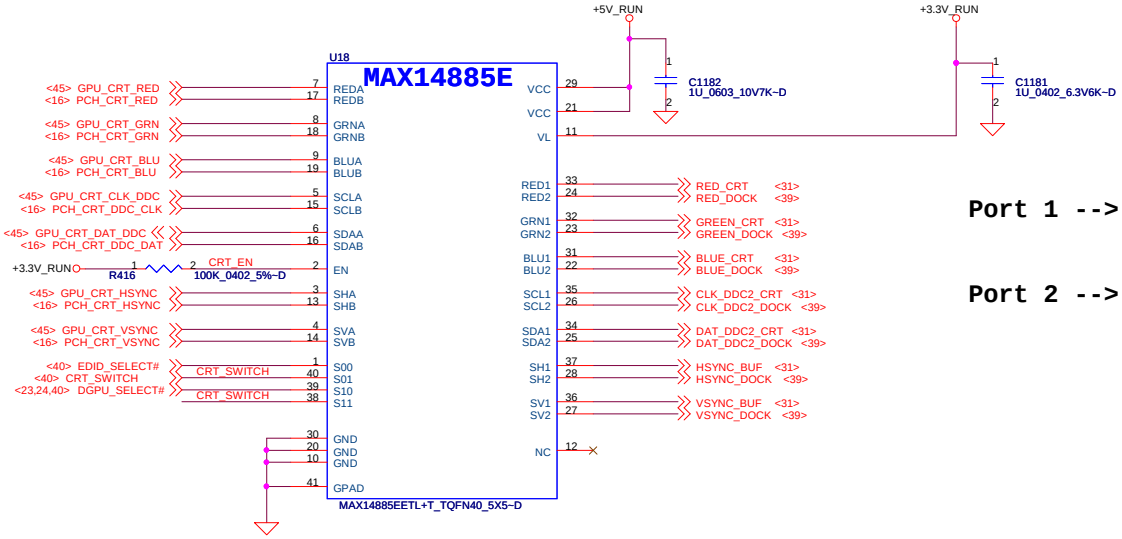
Title: eDP & CAM &TS Conn

Size | Document Number: LA-7782 | Rev 0.1

Date: Friday, June 10, 2011 | Sheet 24 of 66

Channel A --> GPU

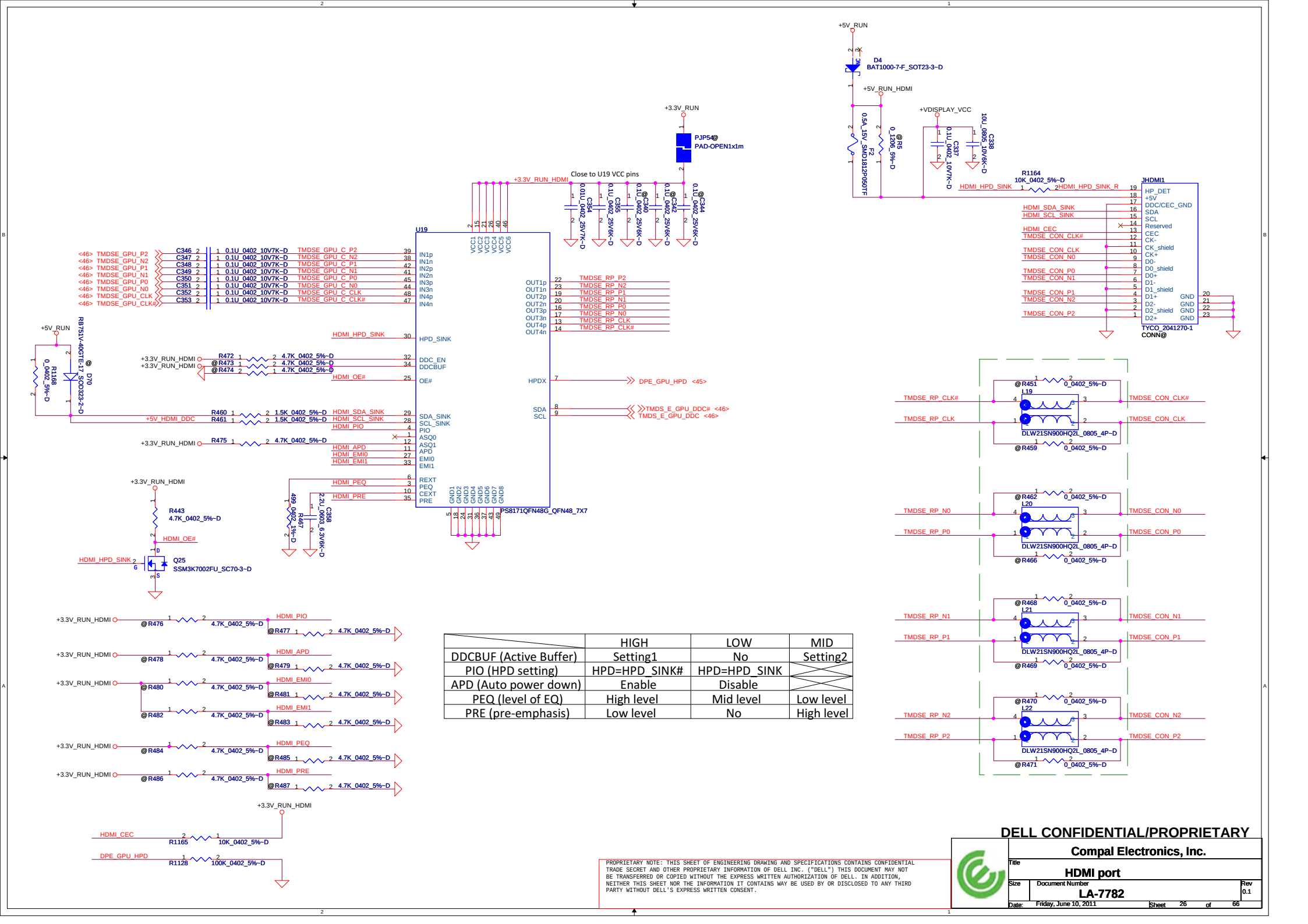
Channel B --> PCH



Port 1 --> MB Port RGB

Port 2 --> Docking Port RGB

CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2



	HIGH	LOW	MID
DDCBUF (Active Buffer)	Setting1	No	Setting2
PIO (HPD setting)	HPD=HPD_SINK#	HPD=HPD_SINK	
APD (Auto power down)	Enable	Disable	
PEQ (level of EQ)	High level	Mid level	Low level
PRE (pre-emphasis)	Low level	No	High level

Compal Electronics, Inc.

Title: HDMI port

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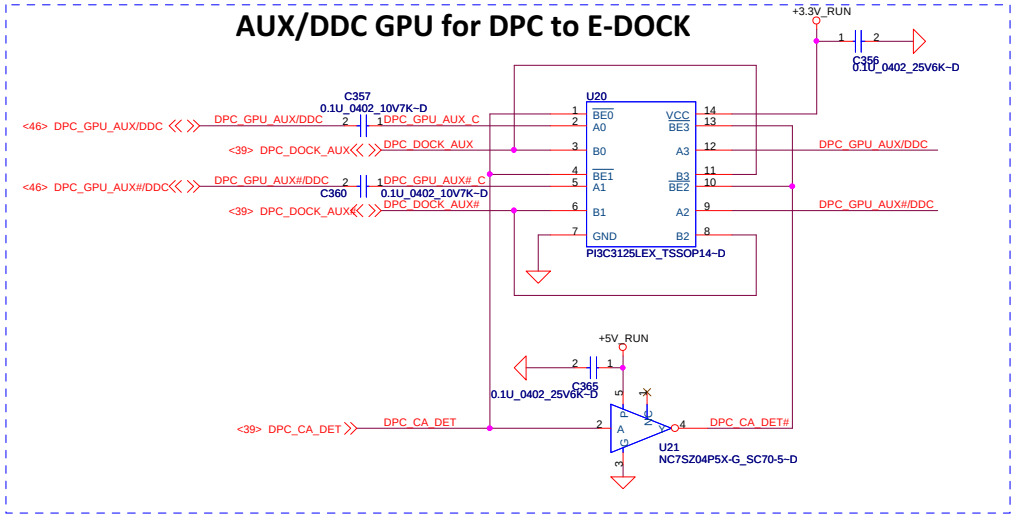
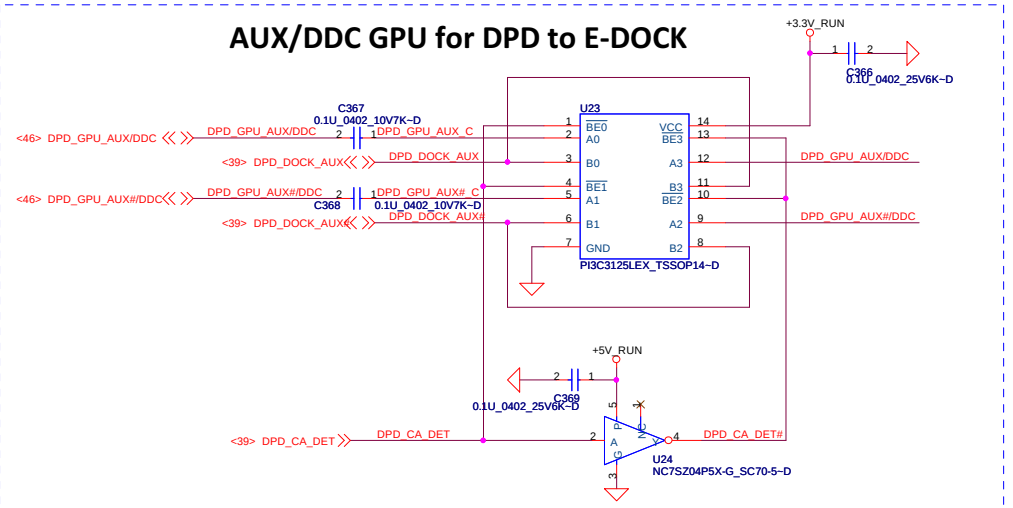
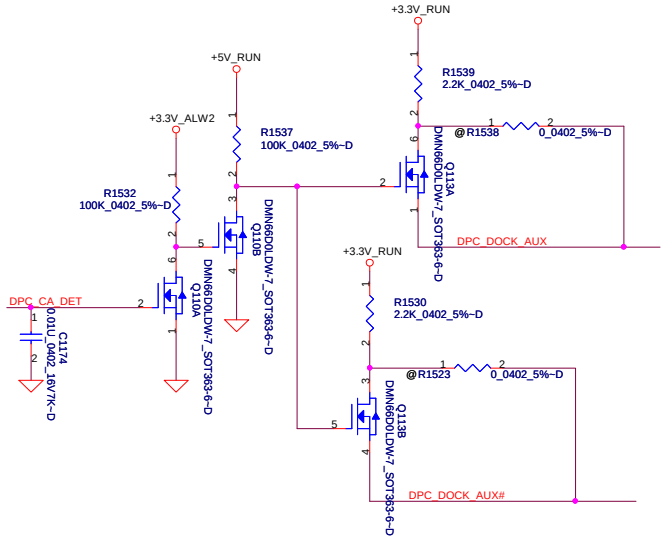
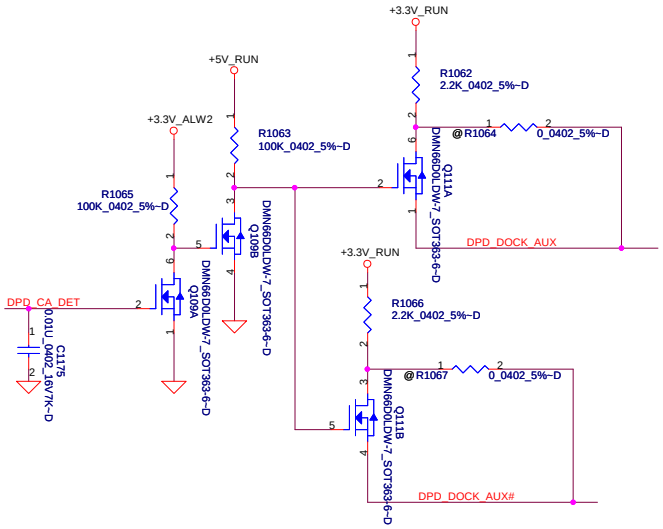
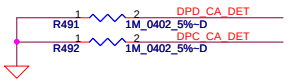




There is a new die for PI3C3125. Sample availabe on May.







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Compal Electronics, Inc.	
Title	DP AUX SW
Size	Document Number: LA-7782
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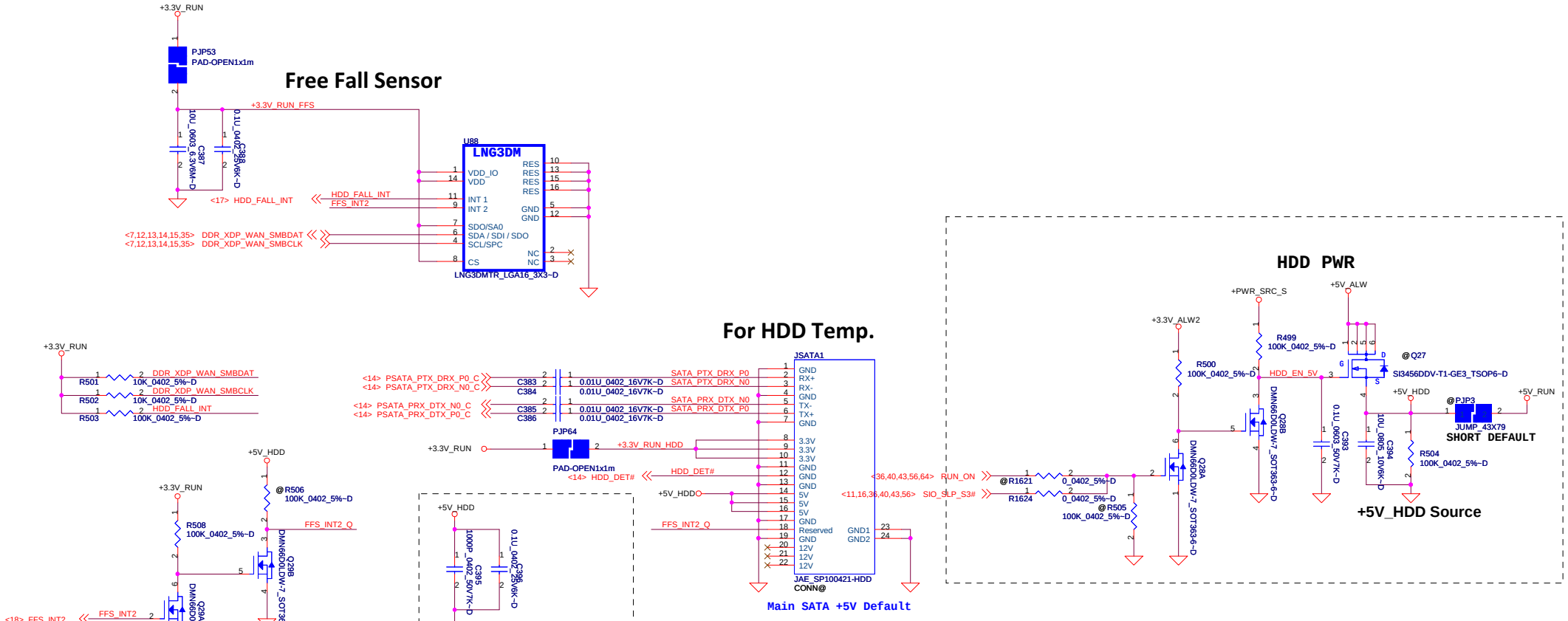

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Compal Electronics, Inc.	
Title	HDD CONNECTOR
Size	Document Number: LA-7782
Rev	0.1
Date:	Friday, June 10, 2011
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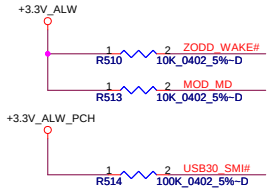
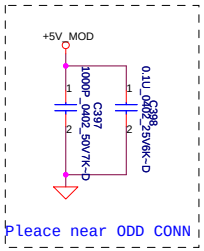
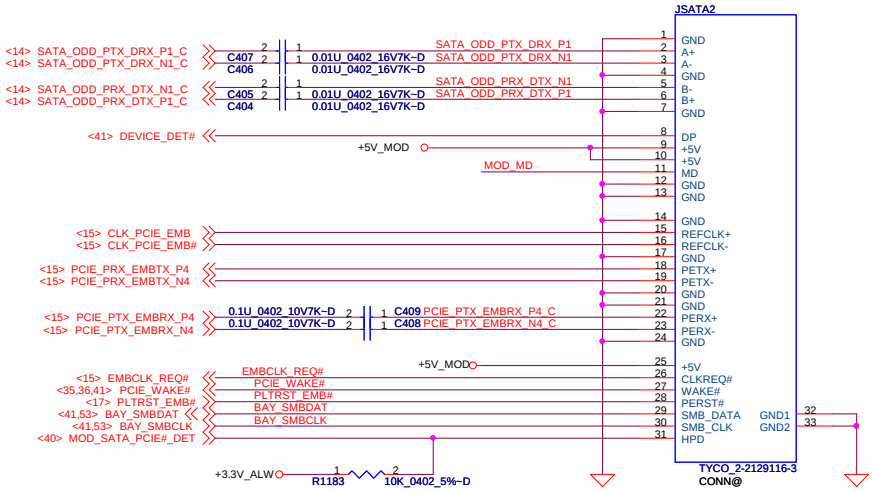
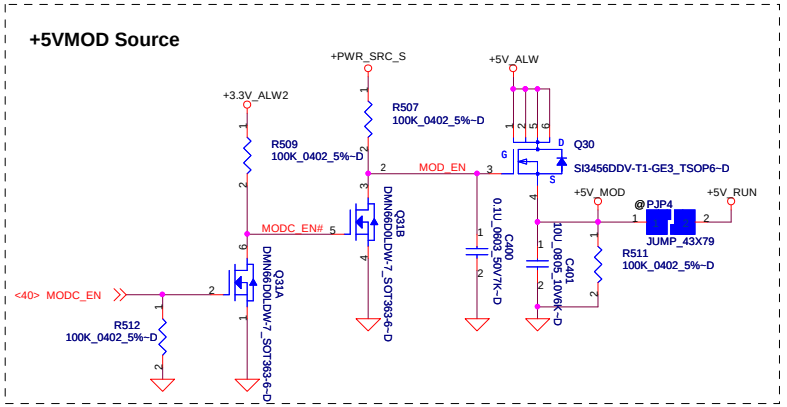
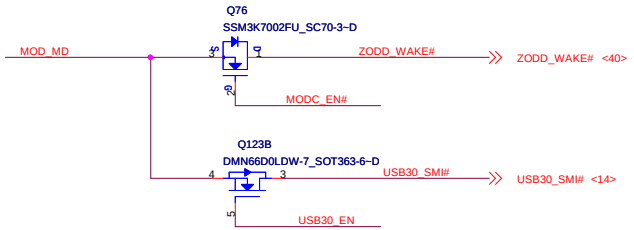
For ODD

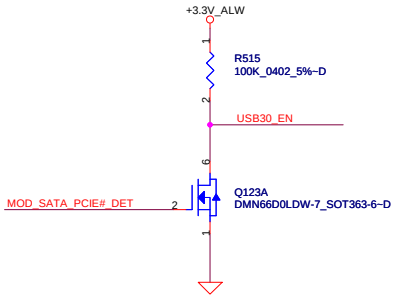












Compal Electronics, Inc.

Title: ODD CONNECTOR

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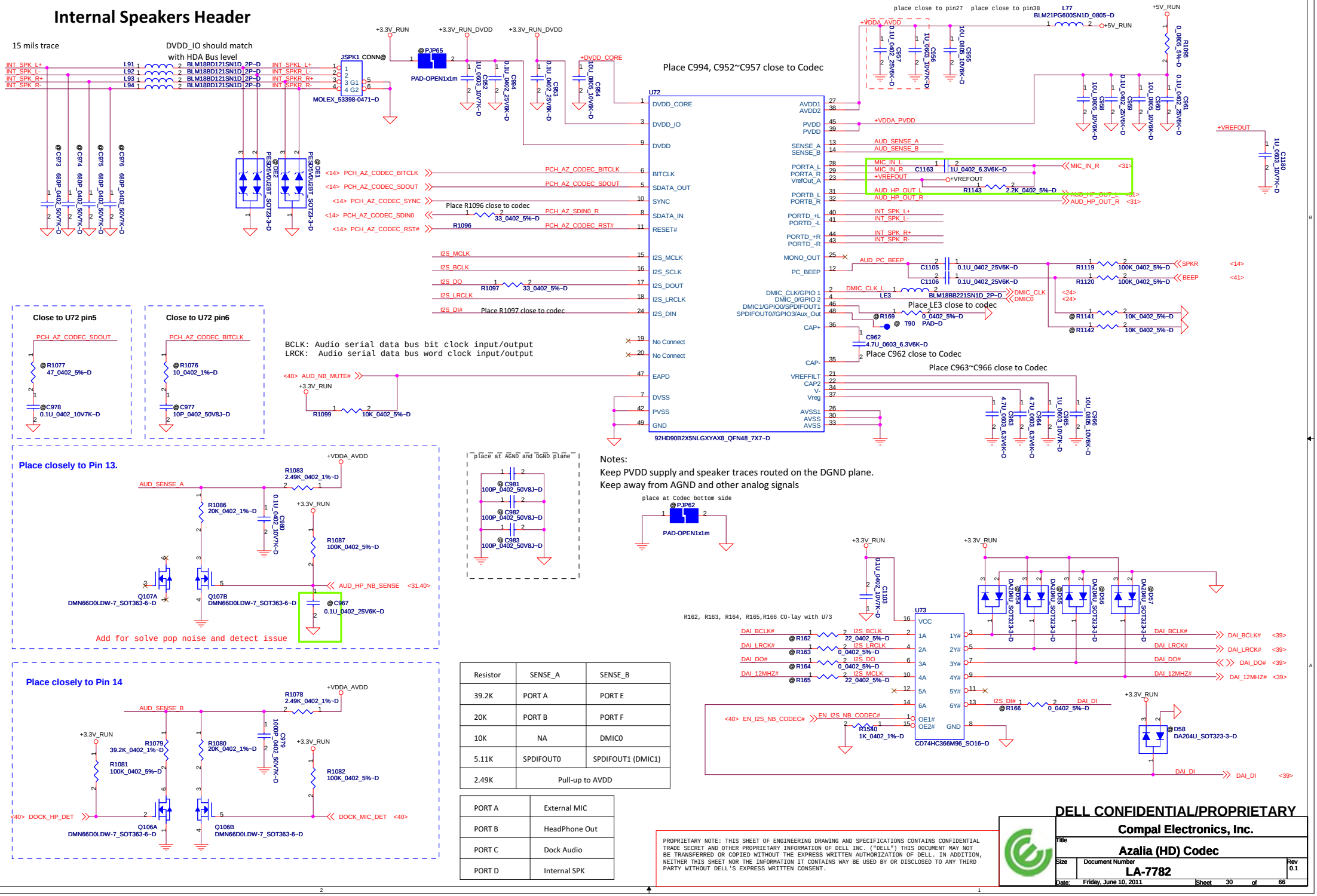
Internal Speakers Header



Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

Compal Electronics, Inc.

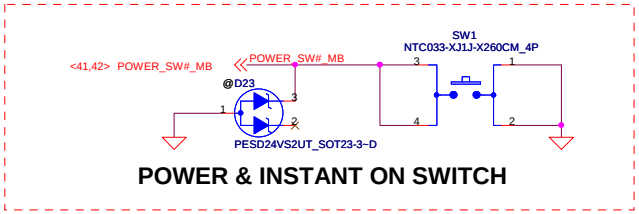
Title: Azalia (HD) Codec

Size: | Document Number: LA-7782 | Rev: 0.1

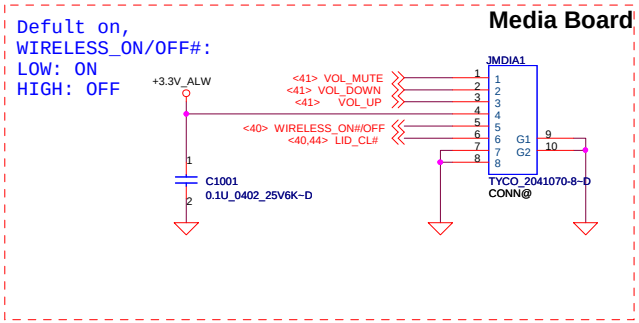
Date: Friday, June 10, 2011 | Sheet 30 of 66

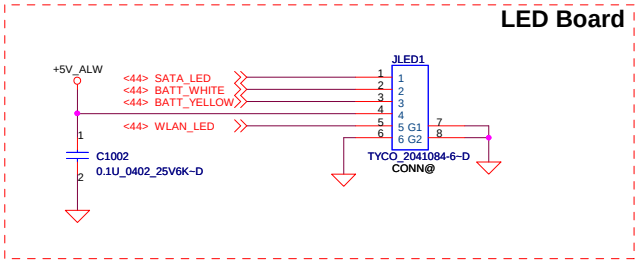
I/O board CONN.

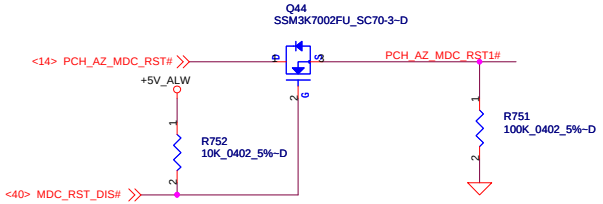
Change to TYCO_2041300-2_60P-T and Horizonal reverse to SSI

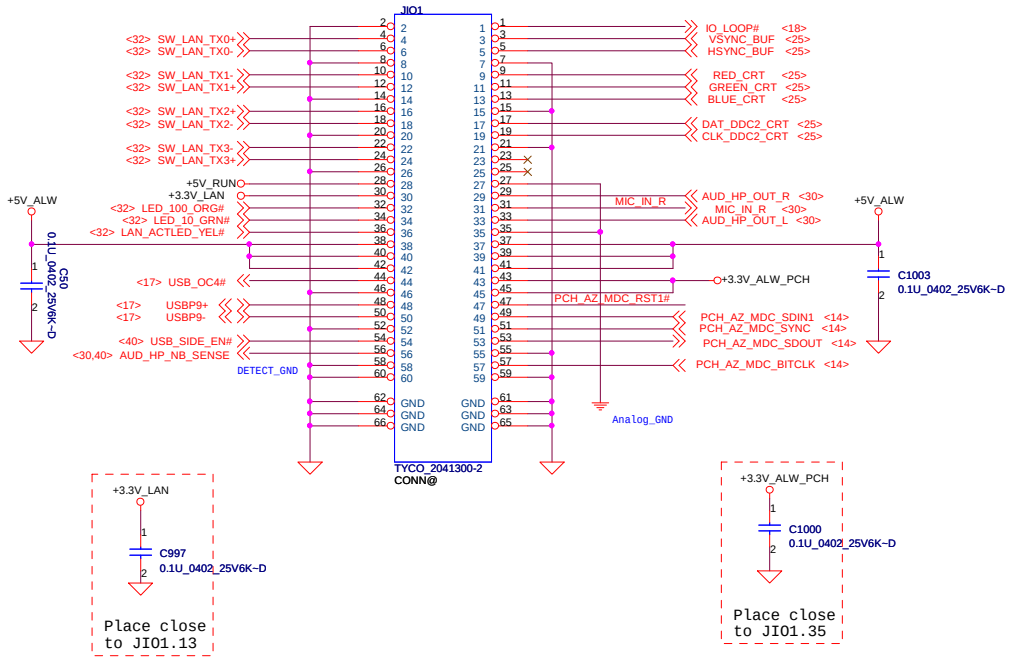


POWER & INSTANT ON SWITCH









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Compal Electronics, Inc.	
Title	PWR SW/Sub-board Connector
Size	Document Number: LA-7782
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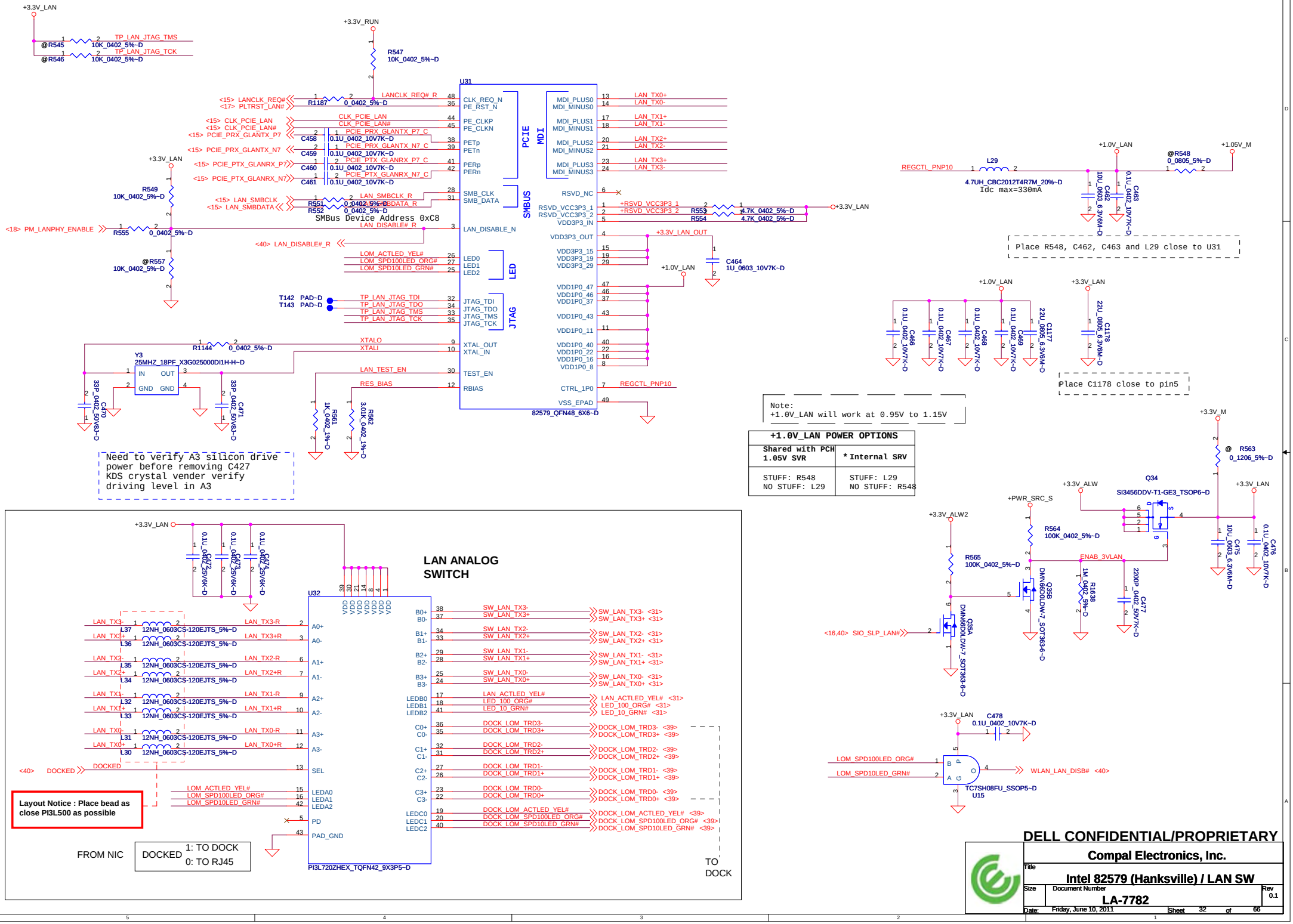
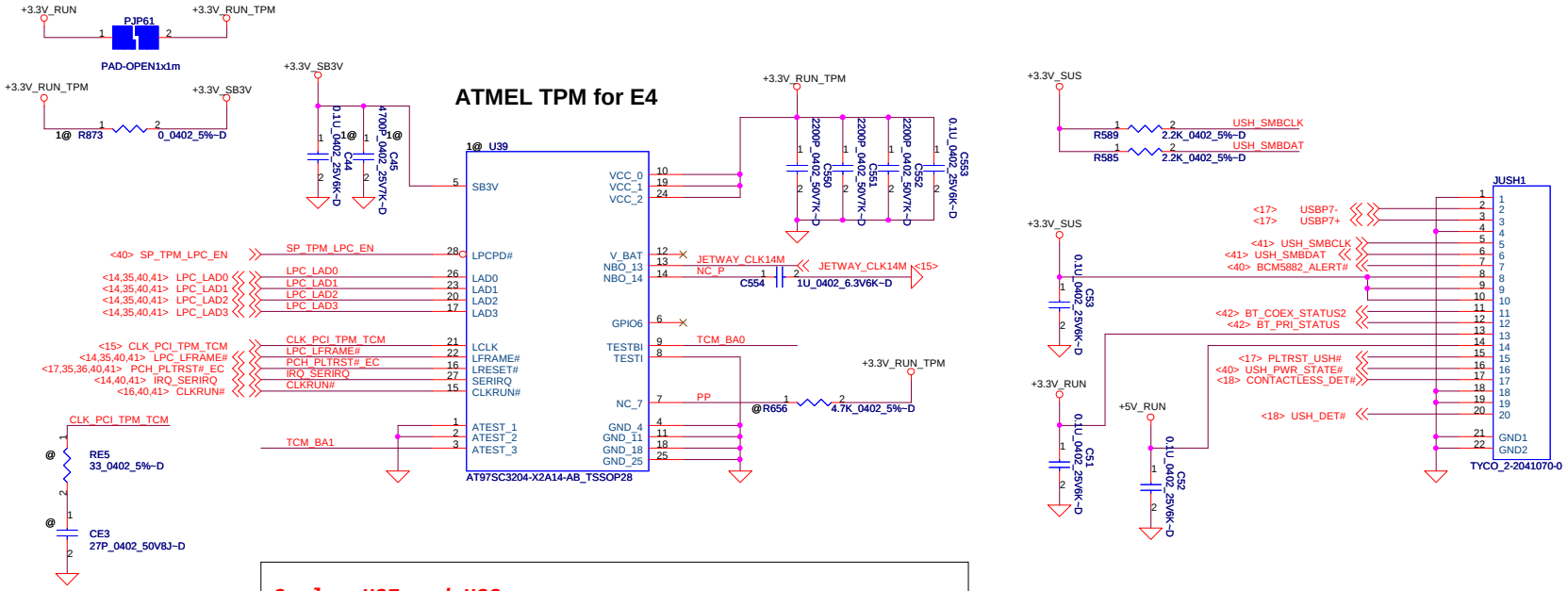
Date: Friday, June 10, 2011	Sheet 31 of 66



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Intel 82579 (Hanksville) / LAN SW		
Size	Document Number: LA-7782	Rev: 0.1
Date: Friday, June 10, 2011	Sheet 32 of 66	

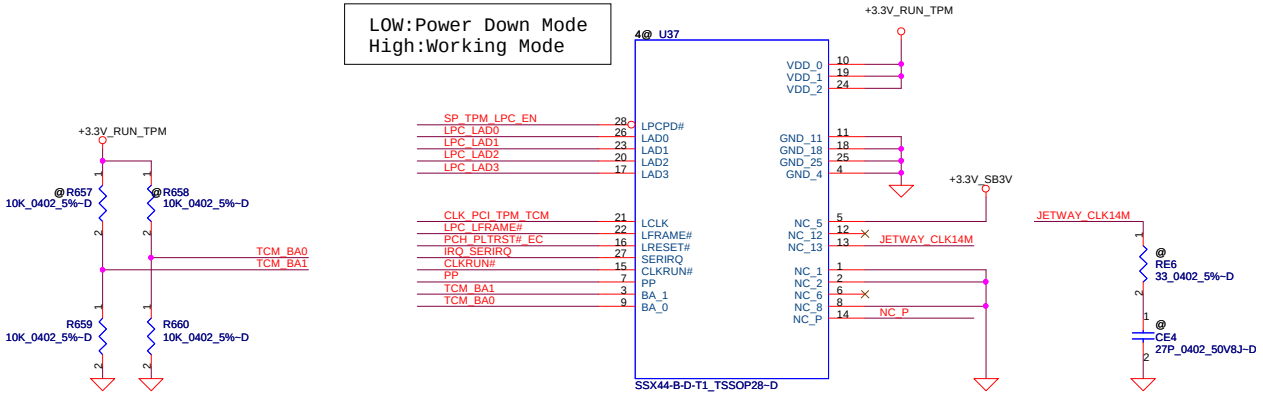


Co-lay U37 and U38

LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

LOW:Power Down Mode
High:Working Mode



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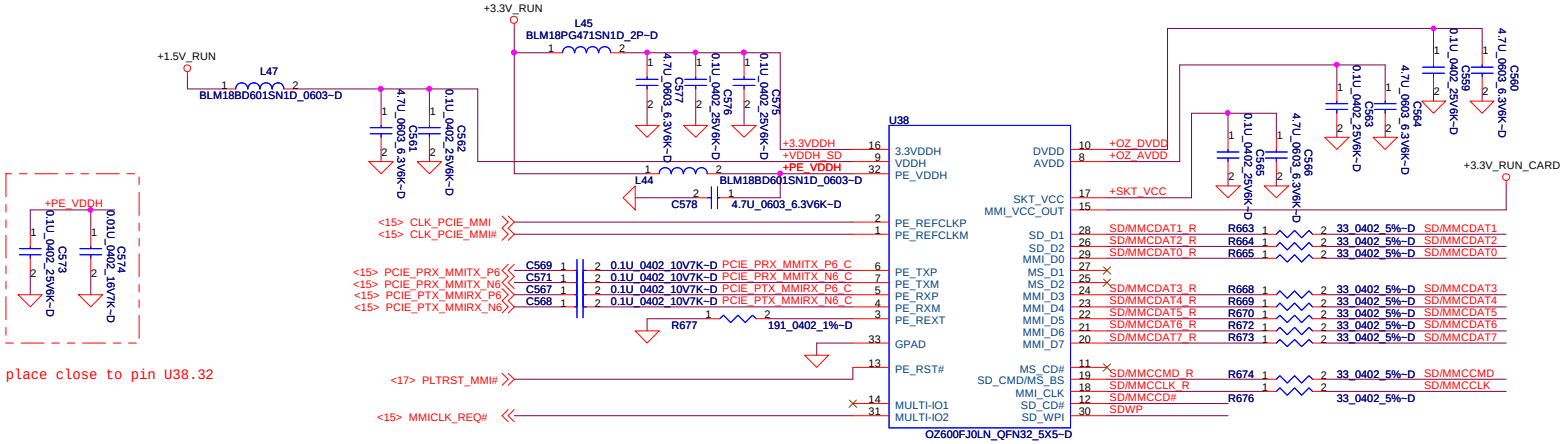
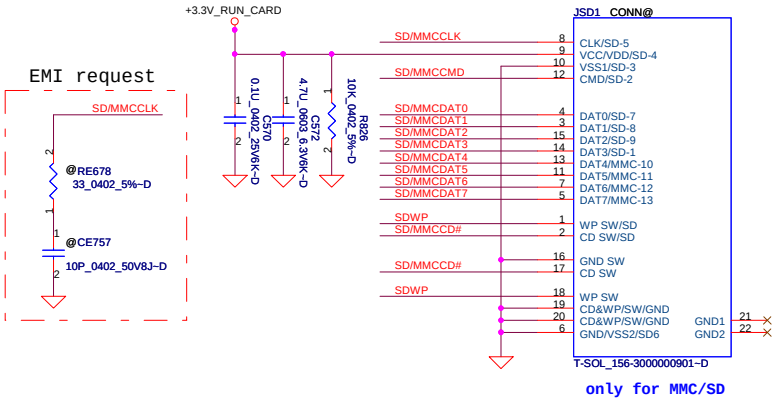
Compal Electronics, Inc.	
Title	USH conn/TPM
Size	Document Number: LA-7782 — Rev: 0.1
Date: Friday, June 10, 2011	Sheet 33 of 66



Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



only for MMC/SD

Compal Electronics, Inc.	
Title	Card Reader OZ600FJ0
Size	Document Number: LA-7782
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Date:	Friday, June 10, 2011
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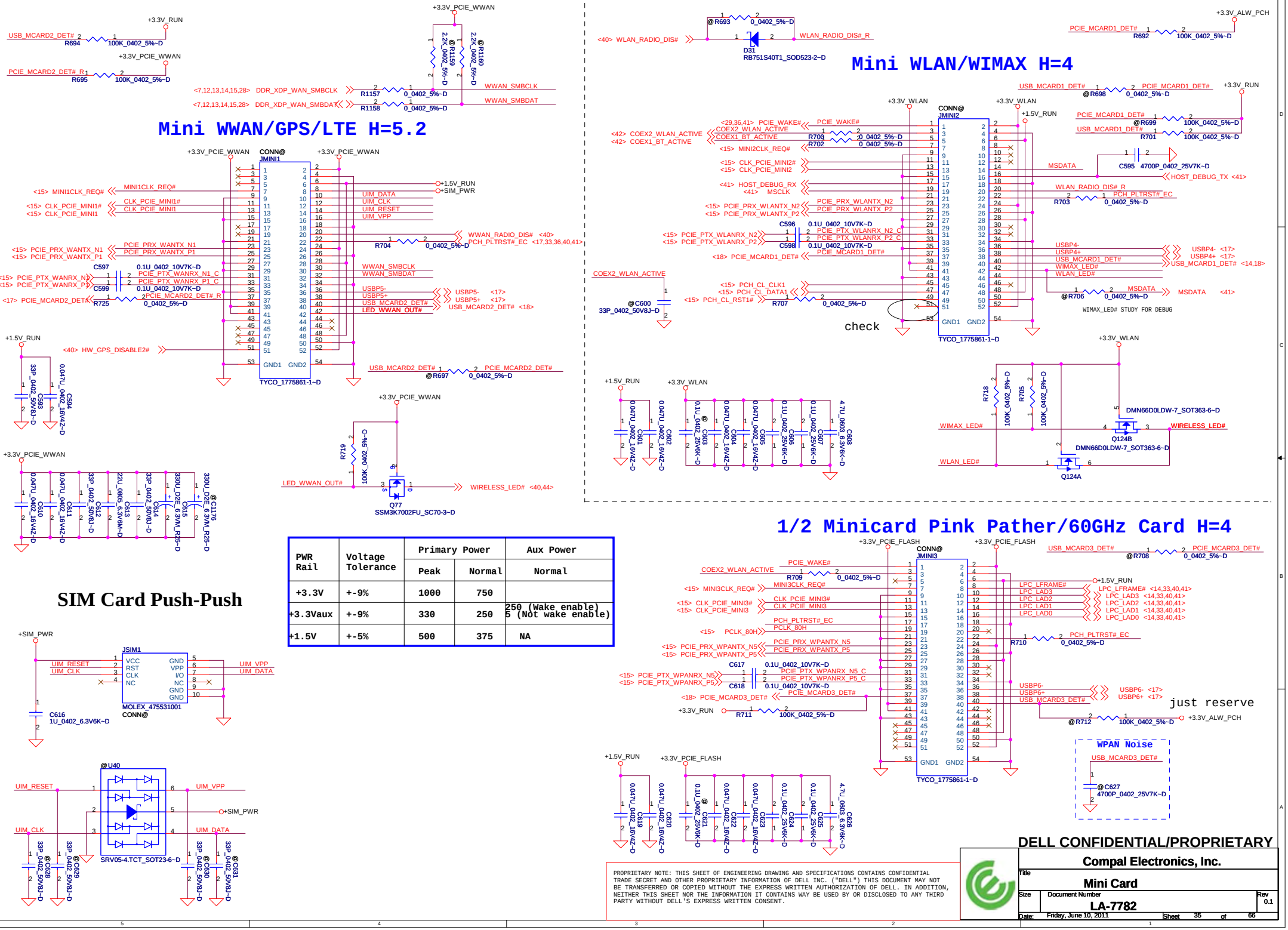
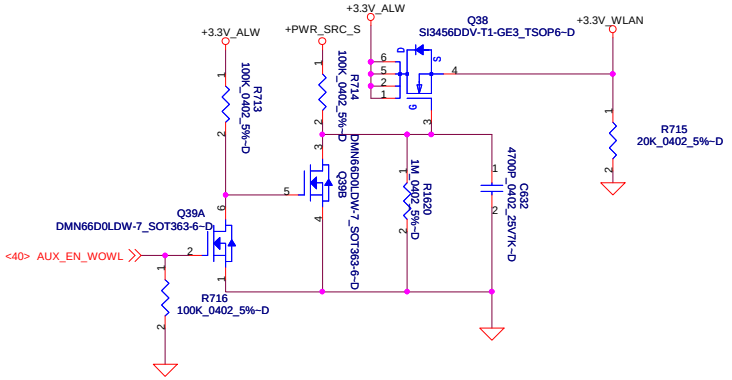
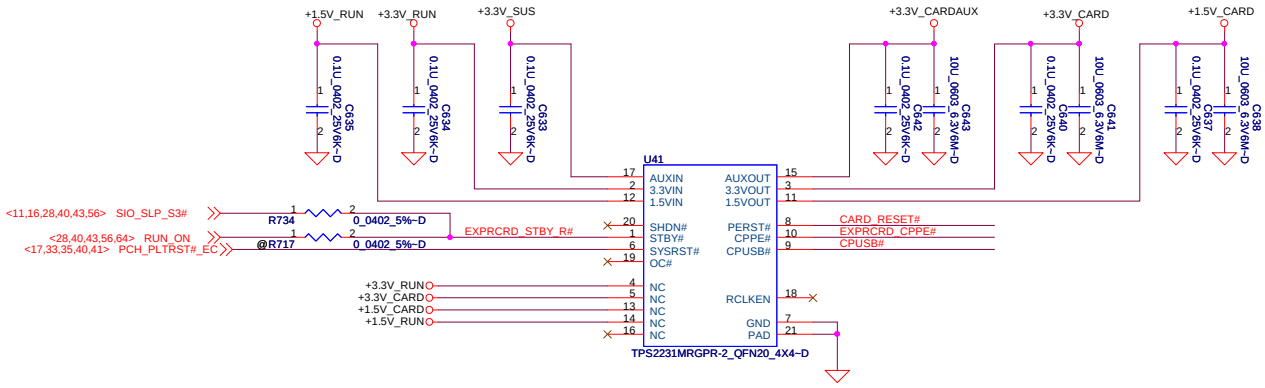


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

Power Control for Mini card2

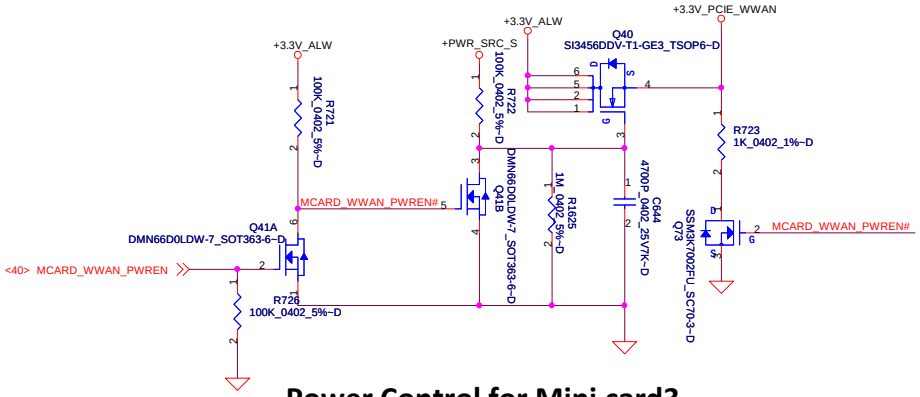


Express Card PWR S/W

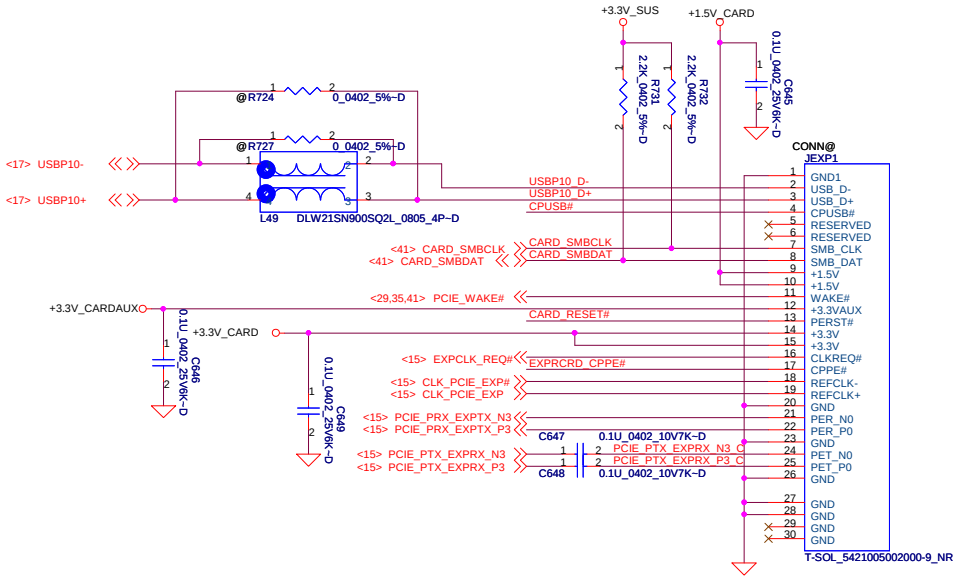


Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

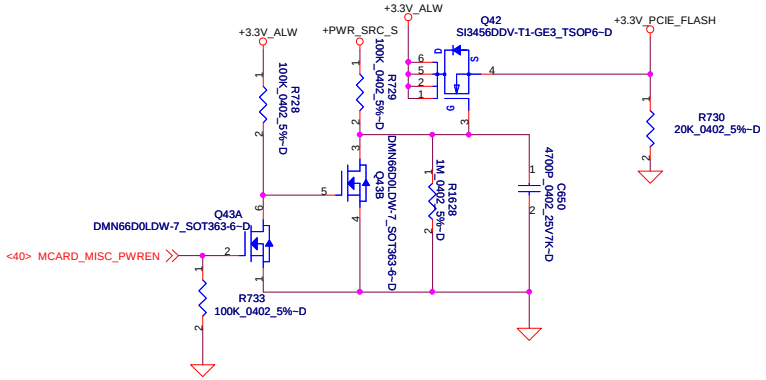
Power Control for Mini card1



Express Card Conn.



Power Control for Mini card3



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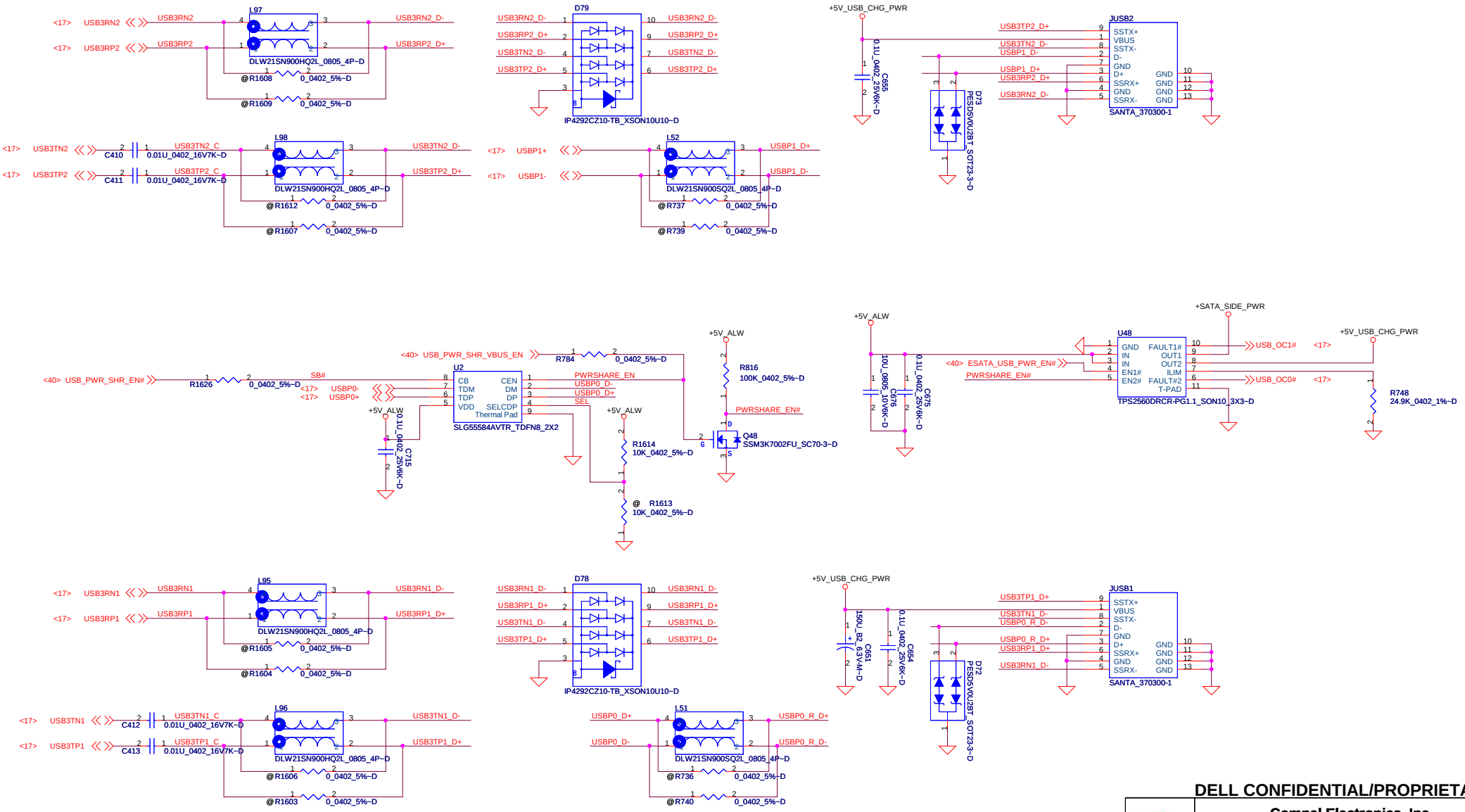
Compal Electronics, Inc.

Title: PCIE-SATA SW / PCIE PWR

Size | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 36 of 66



Compal Electronics, Inc.

Title: USB x2

Size: | Document Number: LA-7782 | Rev: 0.1

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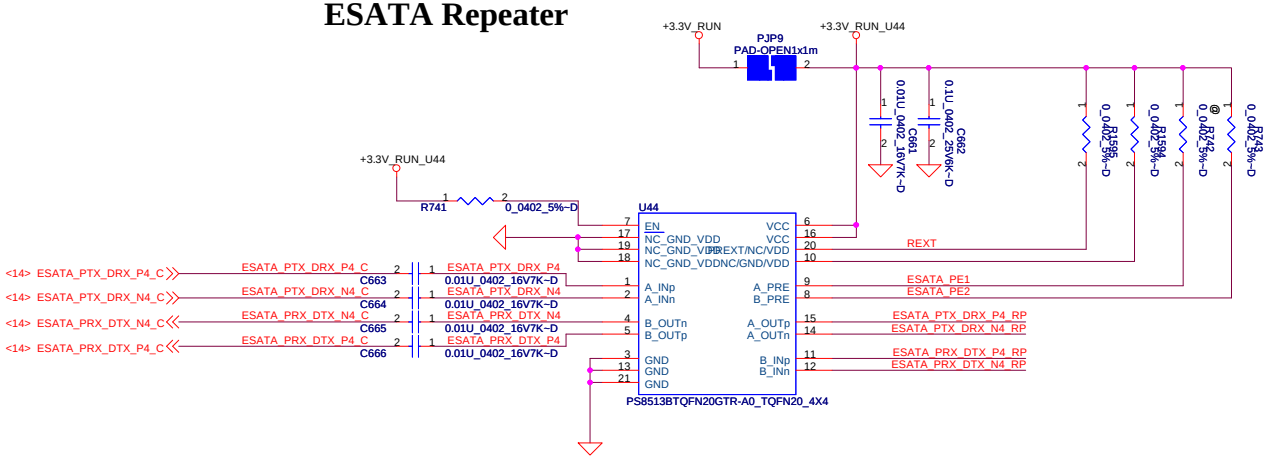
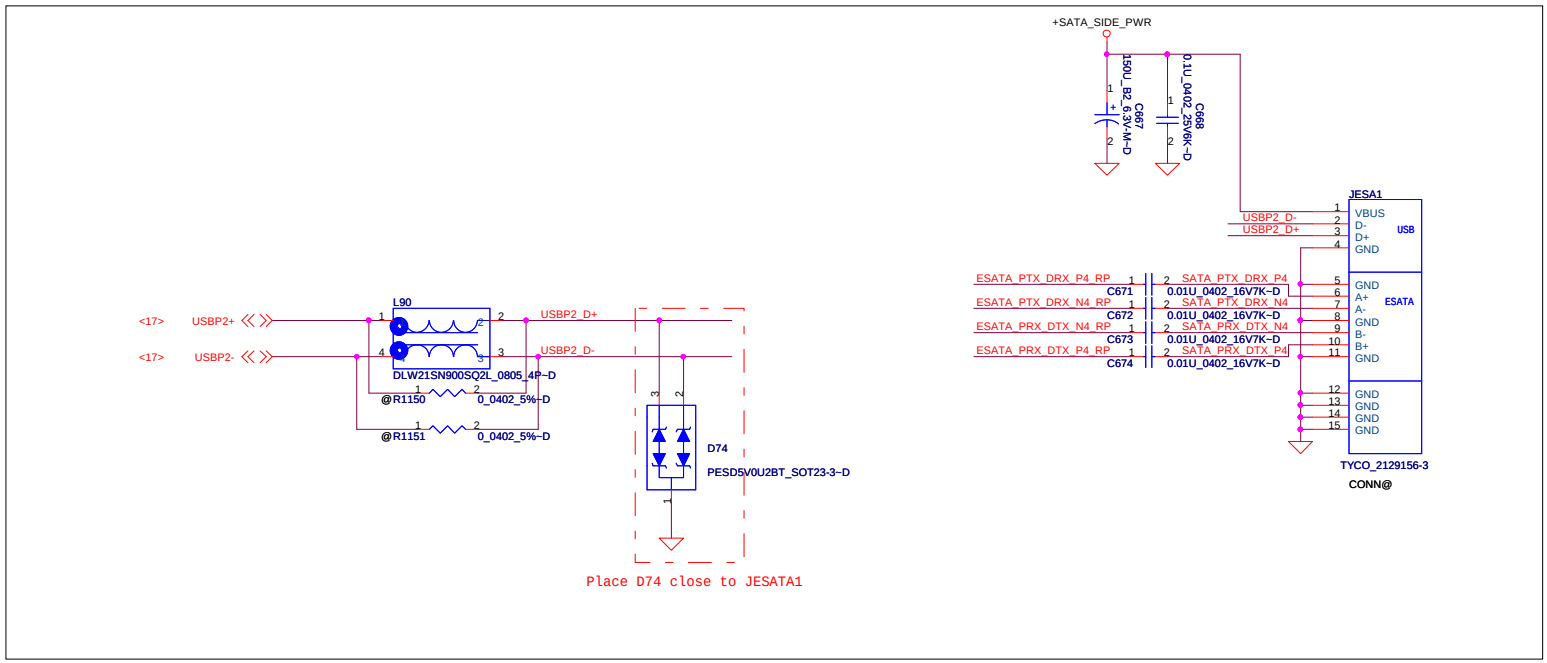
ESATA Repeater





Compal Electronics, Inc.

Title: USB/ESATA/IO/MDC

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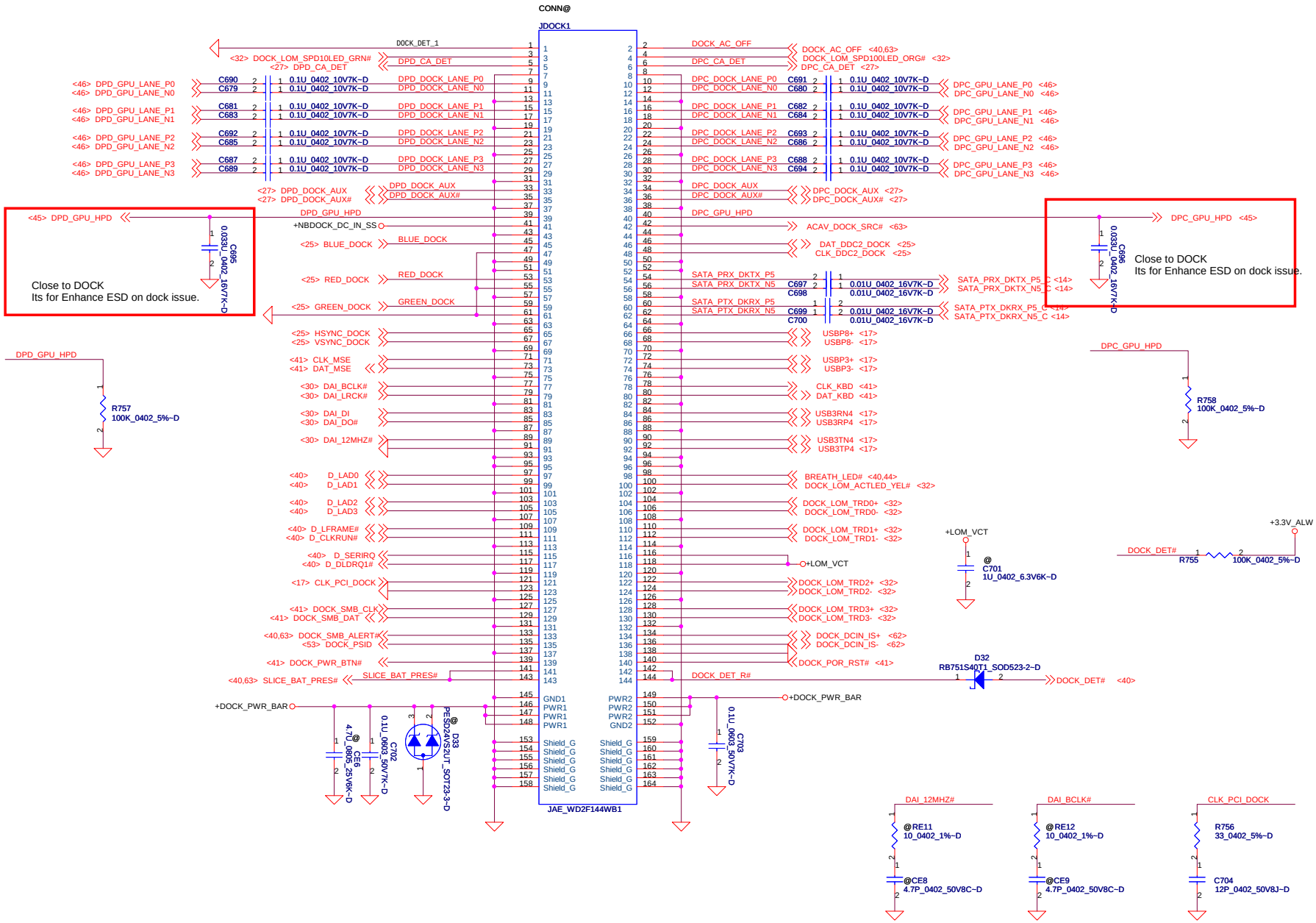

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Title: DOCKING CONN		
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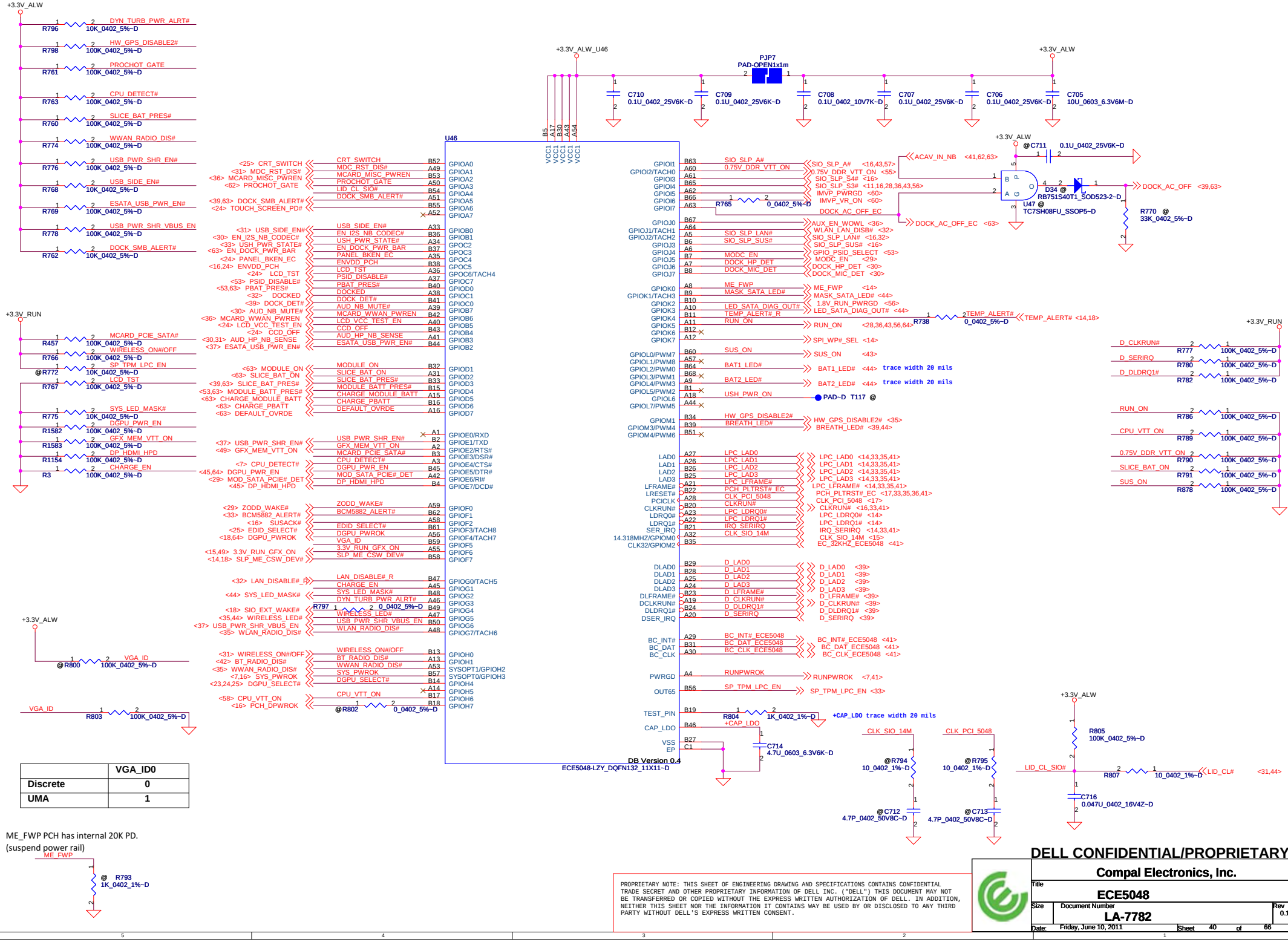

	VGA_ID0
Discrete	0
UMA	1

Compal Electronics, Inc.

Title: ECE5048

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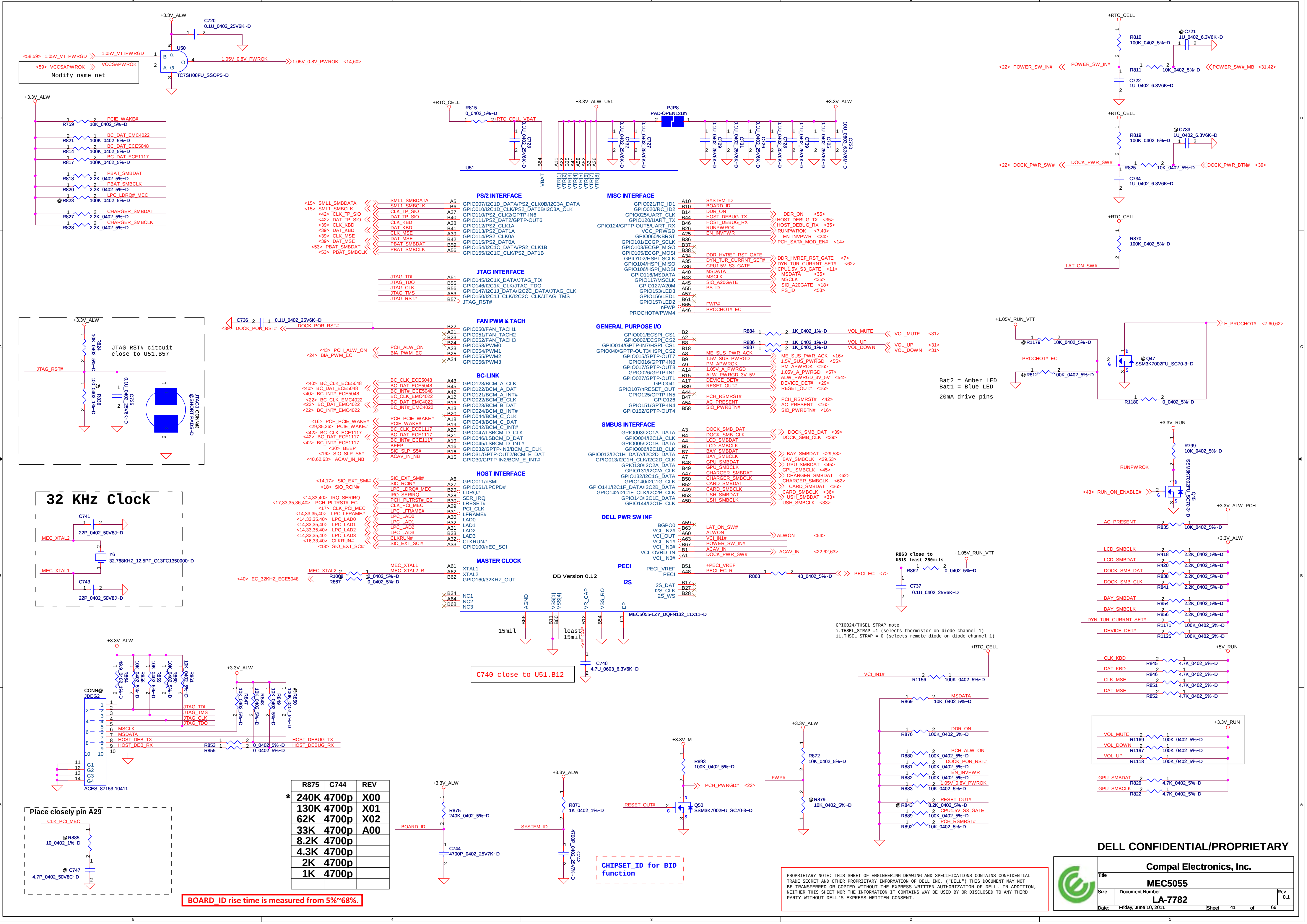

R875	C744	REV
* 240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

Compal Electronics, Inc.

Title: MEC5055

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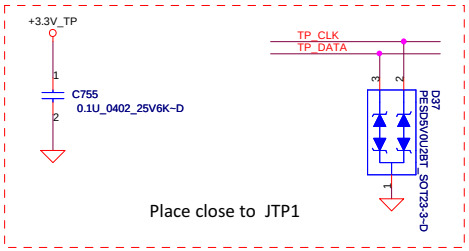
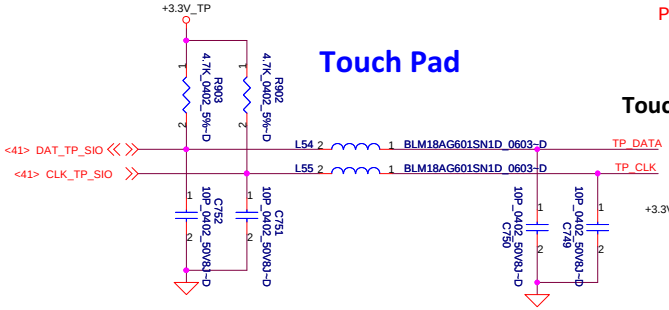
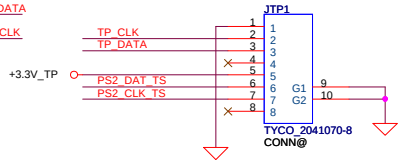


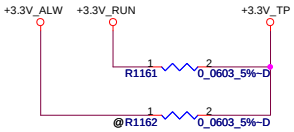


Pin reverse for PT

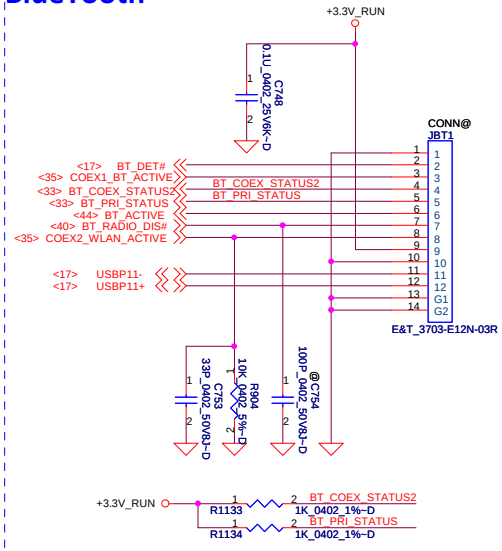
Touch Pad

Touch Pad Conn. Pitch=0.5mm

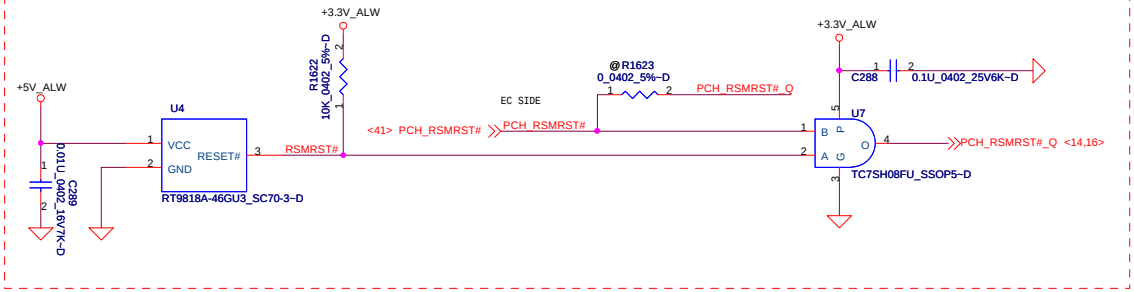




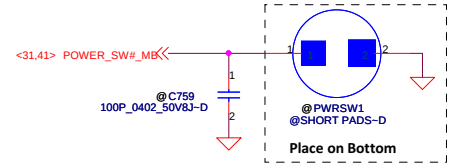
BlueTooth



RSMRST circuit

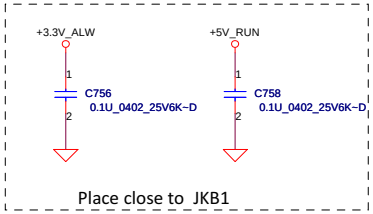


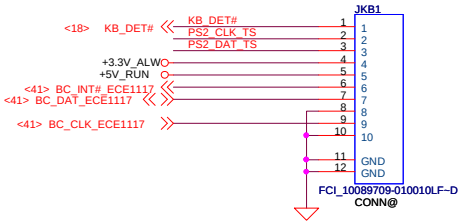
Power Switch for debug



Change KB connector to same as JSC1

KB Conn. Pitch=1.0mm





@LVDS cable

Part Number	Description
DC020003Y0L	H-CONN SET ZJX MB-LCD 14 WXGA+(-1ch)

@RTC BATT

Part Number	Description
GC20323MX00	BATT CR2032 3V 220MAH MAXELL

@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

@LED Board FFC

Part Number	Description
NBX0000RP0L	FFC 6P H P1 PAD=0.7 87.4MM MB-LED/B 0FD

@MEDIA Board FFC

Part Number	Description
NBX0000RS0L	FFC 12P G P.5 PAD.3 75MM MB-VOLUME/B 0FD

@LVDS cable

Part Number	Description
DC02C00180L	H-CONN SET 0FD MB-LCD CAM LED 2CHANNEL

@UMA DC_IN wire cable

Part Number	Description
DC30100BN0	CONN SET 0FD DCJACK-MB WDMD-DCE30004-DF

@Battery bridge cable

Part Number	Description
DC020014Z10	H-CONN SET 0FD M/B-BATTERY 9PIN

@MDC wire set cable

Part Number	Description
DC30100BL0L	CONN SET 0FD MDC-RJ11

@T/P FFC

Part Number	Description
NBX0000RR0L	FFC 8P F P0.5 PAD=0.3 136MM MB-TP/B 0FD

@KB FFC

Part Number	Description
SP070007V0L	S SOCKET TYCO 1770551-1 10P H5.9 SMART

@BT wire cable

Part Number	Description
DC020014Y0L	H-CONN SET 0FD MB-BT

Compal Electronics, Inc.

Title: TP/KB/BT/FAN/RESET

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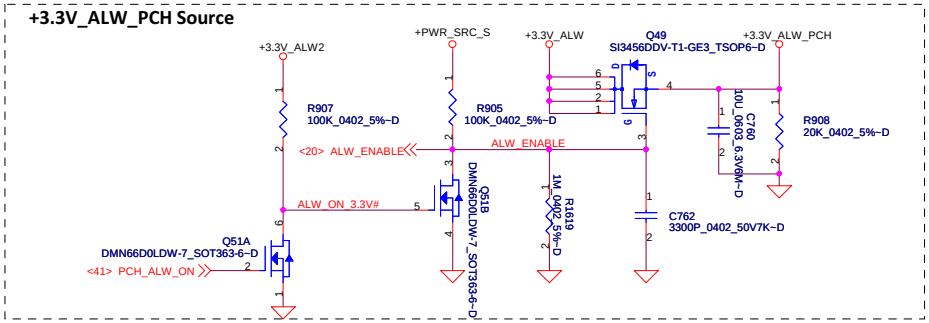
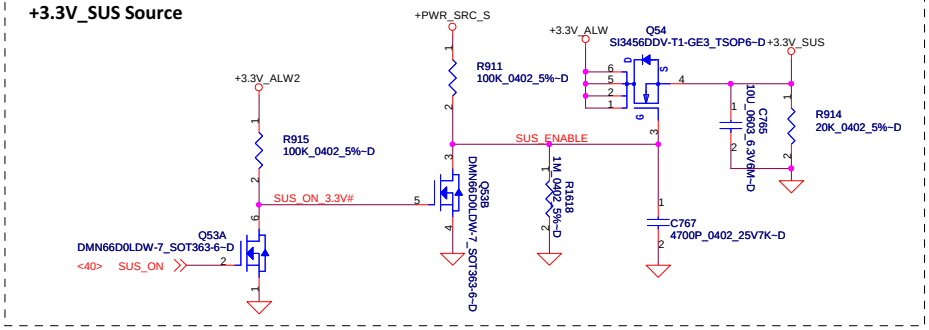
DC/DC Interface

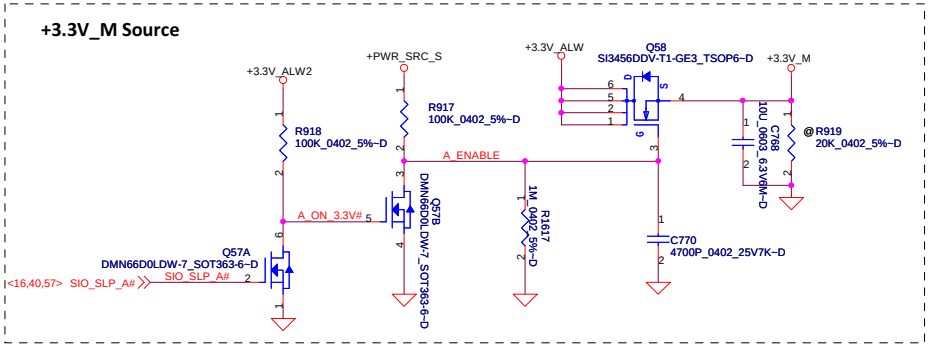
+3.3V_ALW_PCH Source

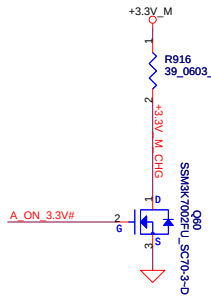


+3.3V_SUS Source

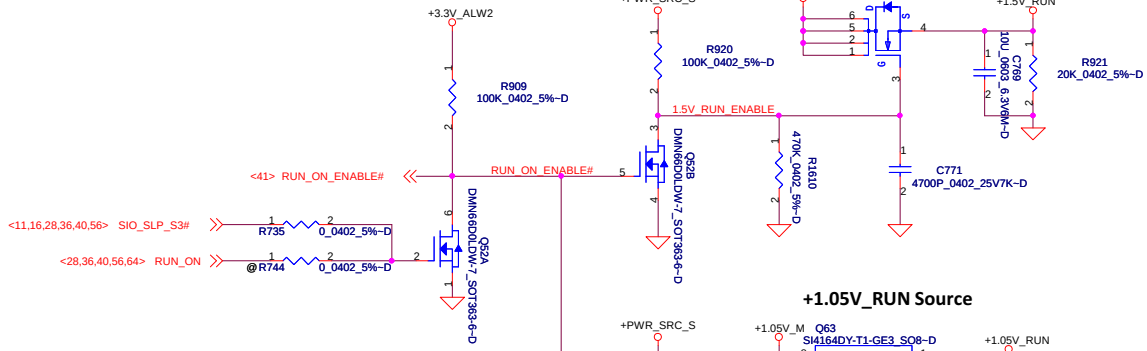


+3.3V_M Source

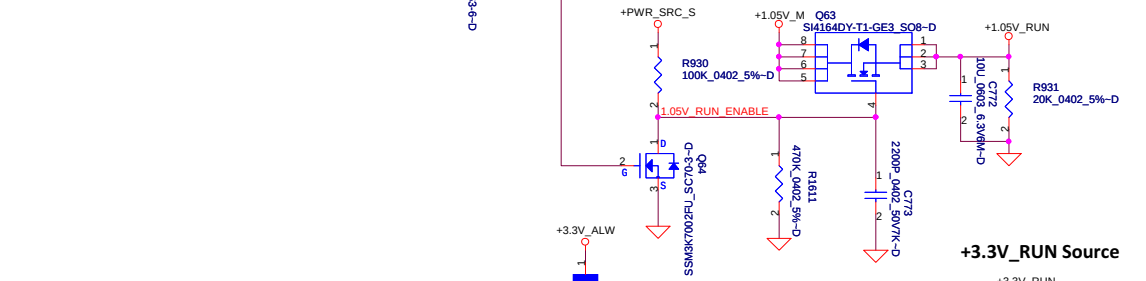




+1.5V_RUN Source



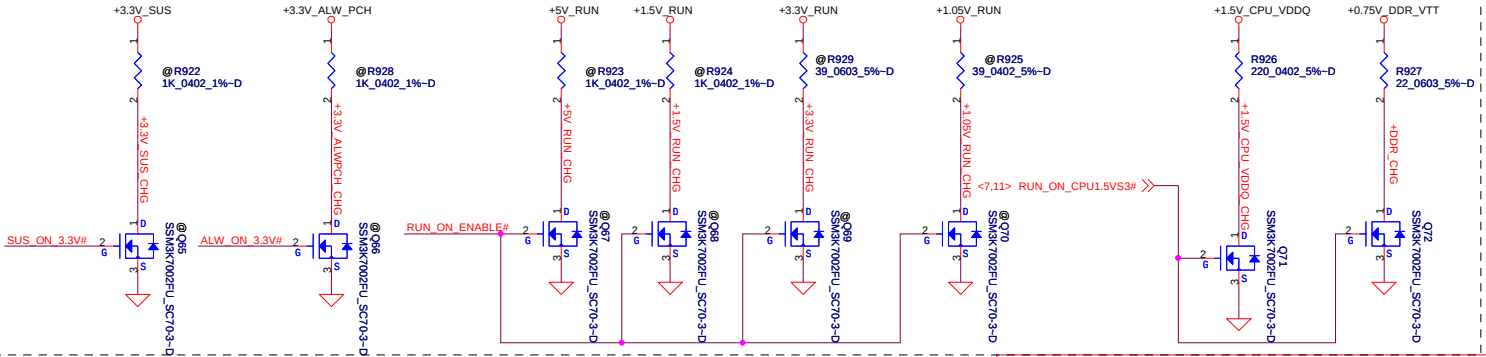
+1.05V_RUN Source



+3.3V_RUN Source

+5V_RUN Source

Discharg Circuit



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Compal Electronics, Inc.	
Title	POWER CONTROL
Size	Document Number: LA-7782 — Rev: 0.1
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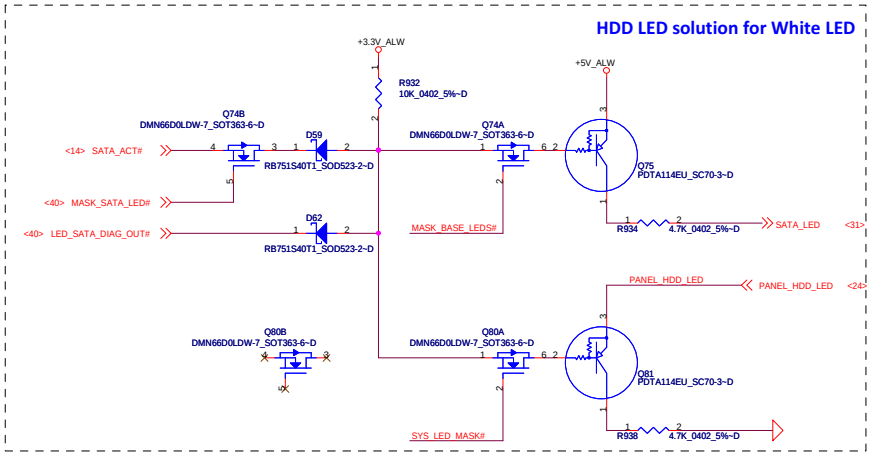
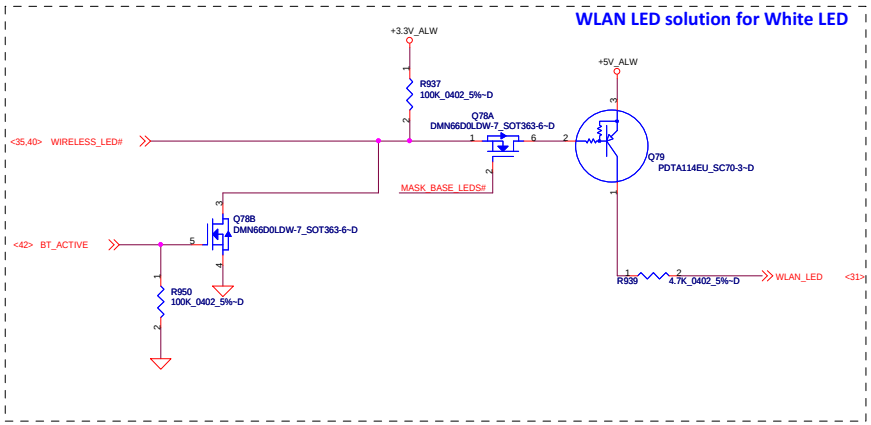
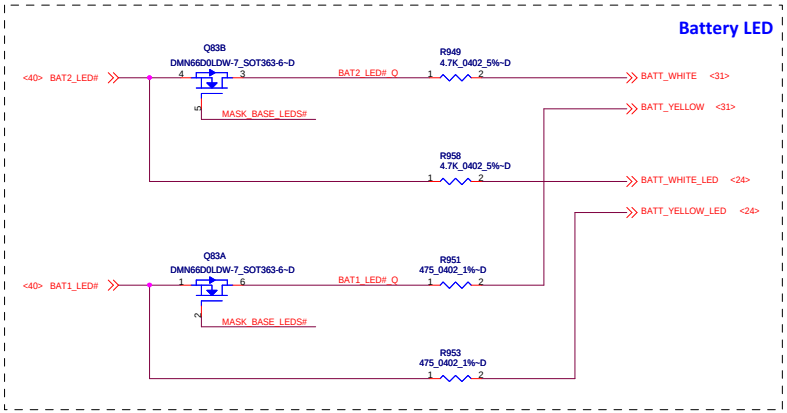
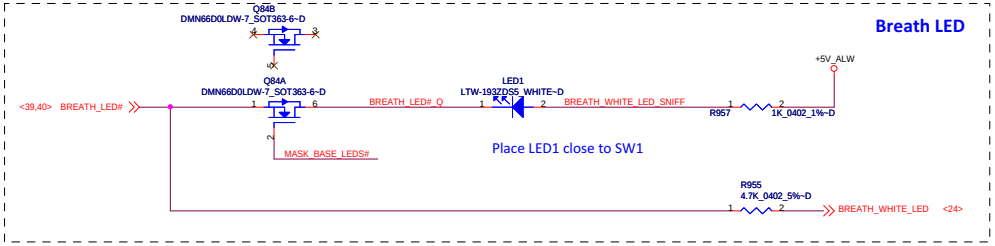






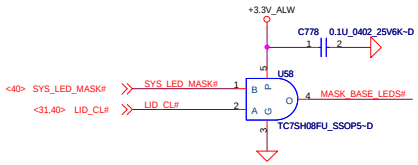


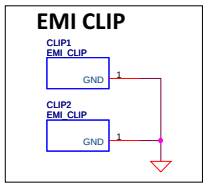
Fiduciel Mark

@FD1	FIDUCIAL MARK~D
@FD2	FIDUCIAL MARK~D
@FD3	FIDUCIAL MARK~D
@FD4	FIDUCIAL MARK~D

LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





@H1 H_3P3 @H2 H_3P3 @H3 H_3P0 @H4 H_3P3 @H5 H_3P0 @H6 H_3P0 @H7 H_3P0 @H8 H_3P2 @H9 H_3P0 @H10 H_3P3

@H12 H_3P0 @H13 H_3P0 @H14 H_3P0 @H15 H_3P0 @H16 H_3P0 @H17 H_2P3 @H19 H_3P0x2P0 @H20 H_2P0N

@H22 H_3P0 @H23 H_2P3

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Compal Electronics, Inc.

Title: PAD and Standoff

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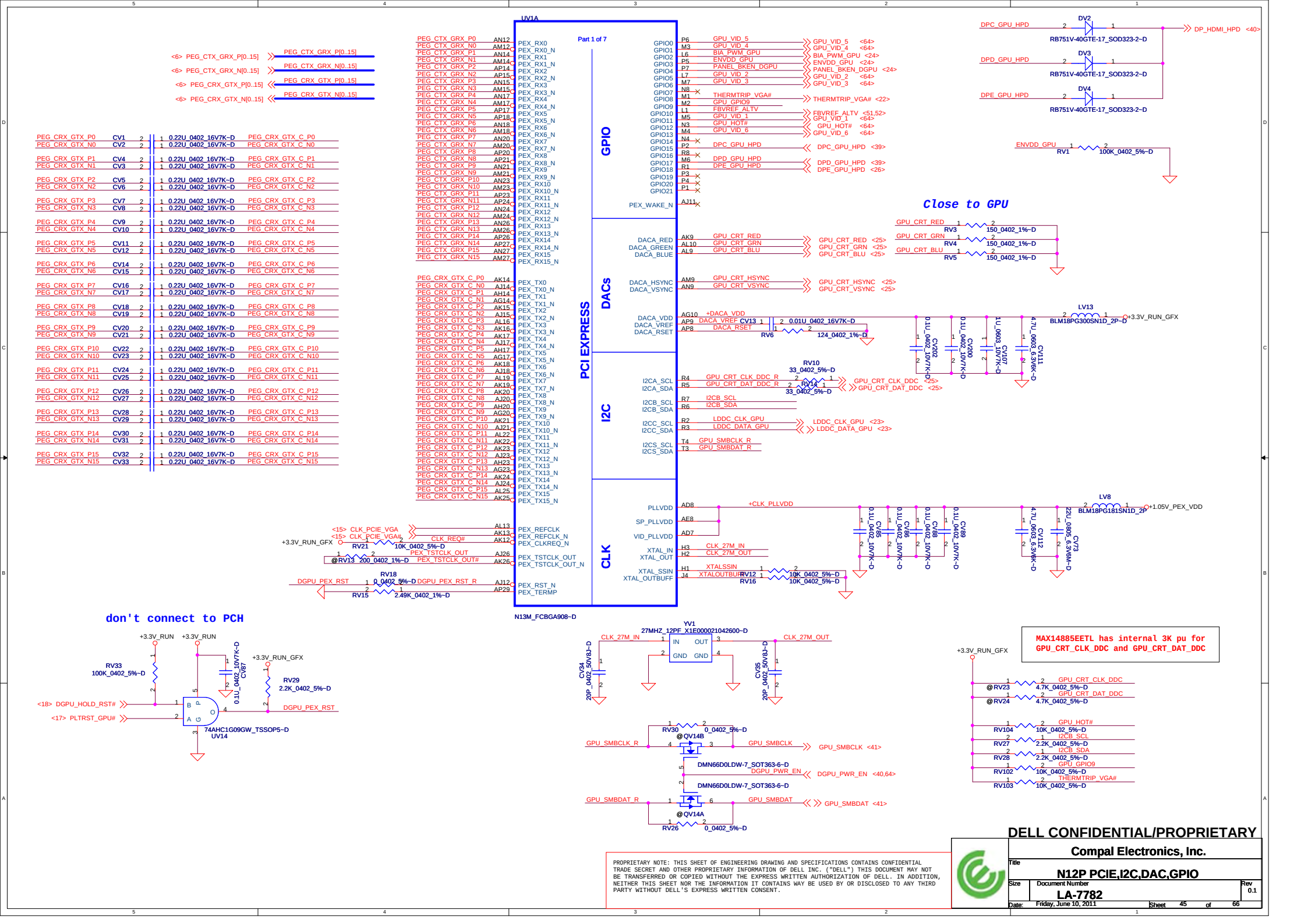
UV1A
Part 1 of 7
PCI EXPRESS
GPIO
DACs
I2C
CLK
N13M_FCBGA908~D
Close to GPU
don't connect to PCH
MAX14885EETL has internal 3K pu for GPU_CRT_CLK_DDC and GPU_CRT_DAT_DDC
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Compal Electronics, Inc.
N12P PCIE,I2C,DAC,GPIO
LA-7782
Rev 0.1
Friday, June 10, 2011
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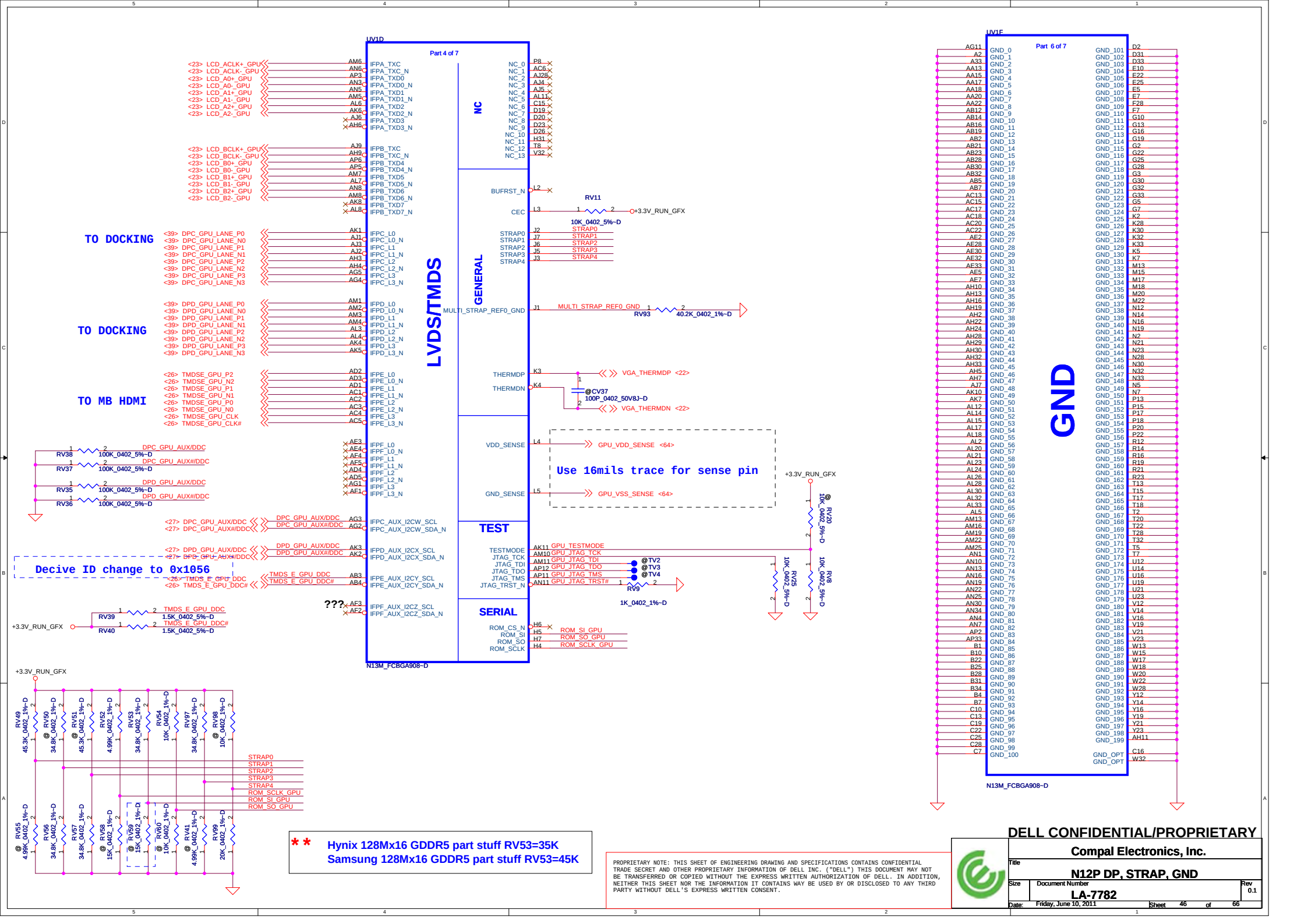

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Title	N12P DP, STRAP, GND
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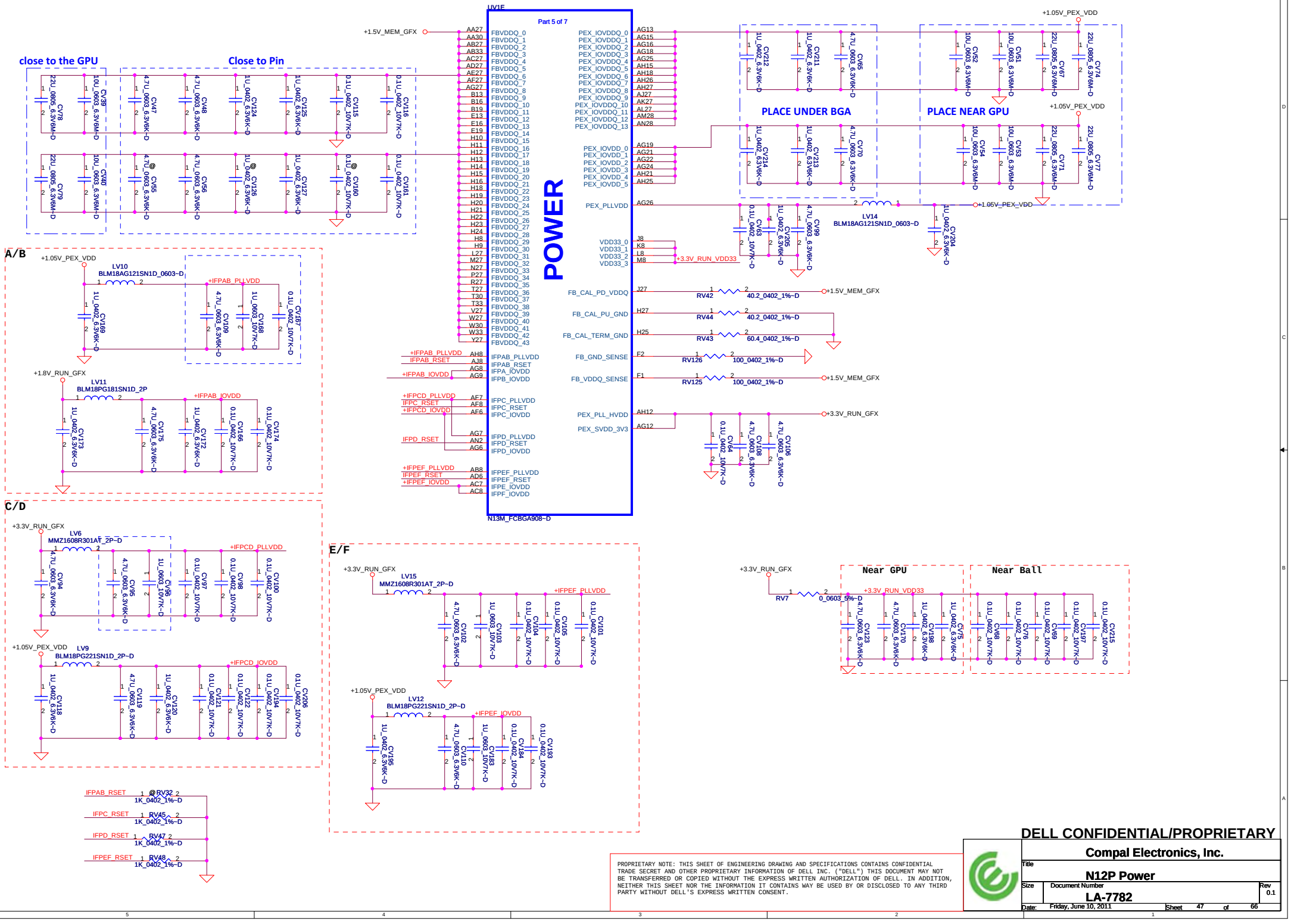

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Title: N12P Power

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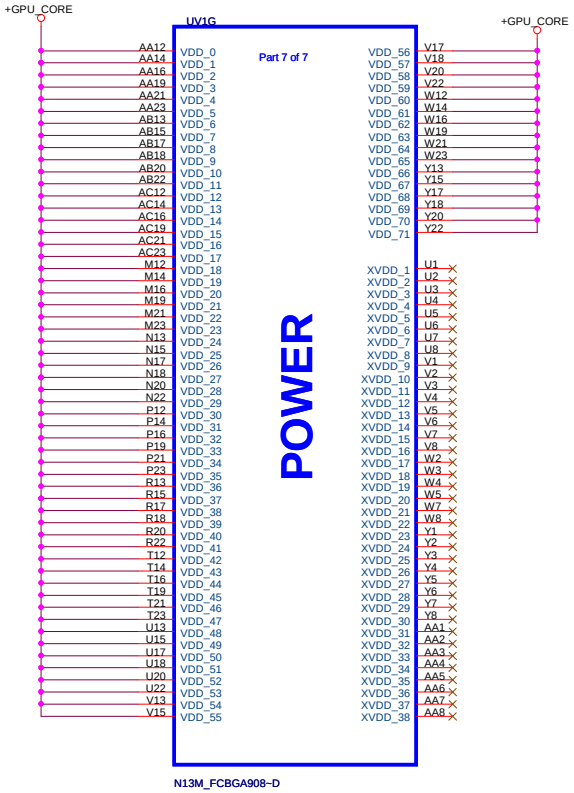
Caps on Power Side



Compal Electronics, Inc.

Title: N12P Power GFX Core

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FBA_D[0..63] FBA_D[0..63] <51,52>
FBA_CMD[0..31] FBA_CMD[0..31] <51,52>
FBA_DBI[0..7] FBA_DBI[0..7] <51,52>
FBA_EDC[0..7] FBA_EDC[0..7] <51,52>

GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD2	CMD18	A2_BA0
CMD1	CMD17	A3_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD7	CMD23	A6_A11
CMD6	CMD22	A7_A8
CMD9	CMD25	A12_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#

+1.8V_RUN_GFX Source

+3.3V_RUN_GFX Source

+1.5V_MEM_GFX Source

+1.05V_RUN_VTT_GFX Source

UV1B
Part 2 of 7
MEMORY INTERFACE A
N13M_FCBGA908-D

THE FBA_ECKBxx ARE USED ON GK107. ON GF108 AND GF117

for Test/Debug
16mil

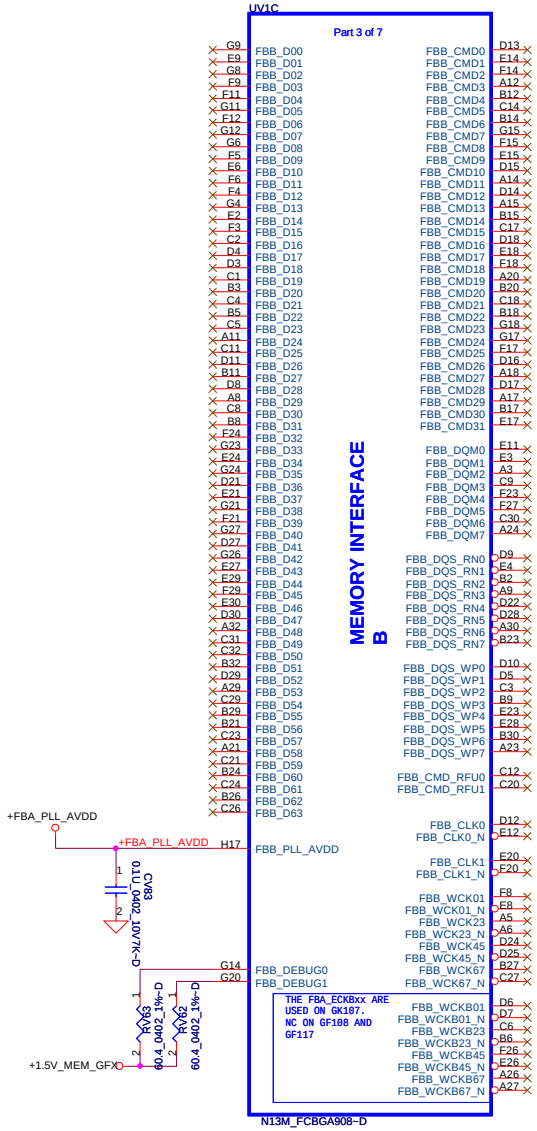
Compal Electronics, Inc.

Title: N12P Memory

Size: | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 49 of 66

CHANNEL-B NOT TO USE, NEED TO BE DISABLED



Compal Electronics, Inc.

Title: N12P Memory (2)

Size | Document Number: LA-7782 | Rev: 0.1

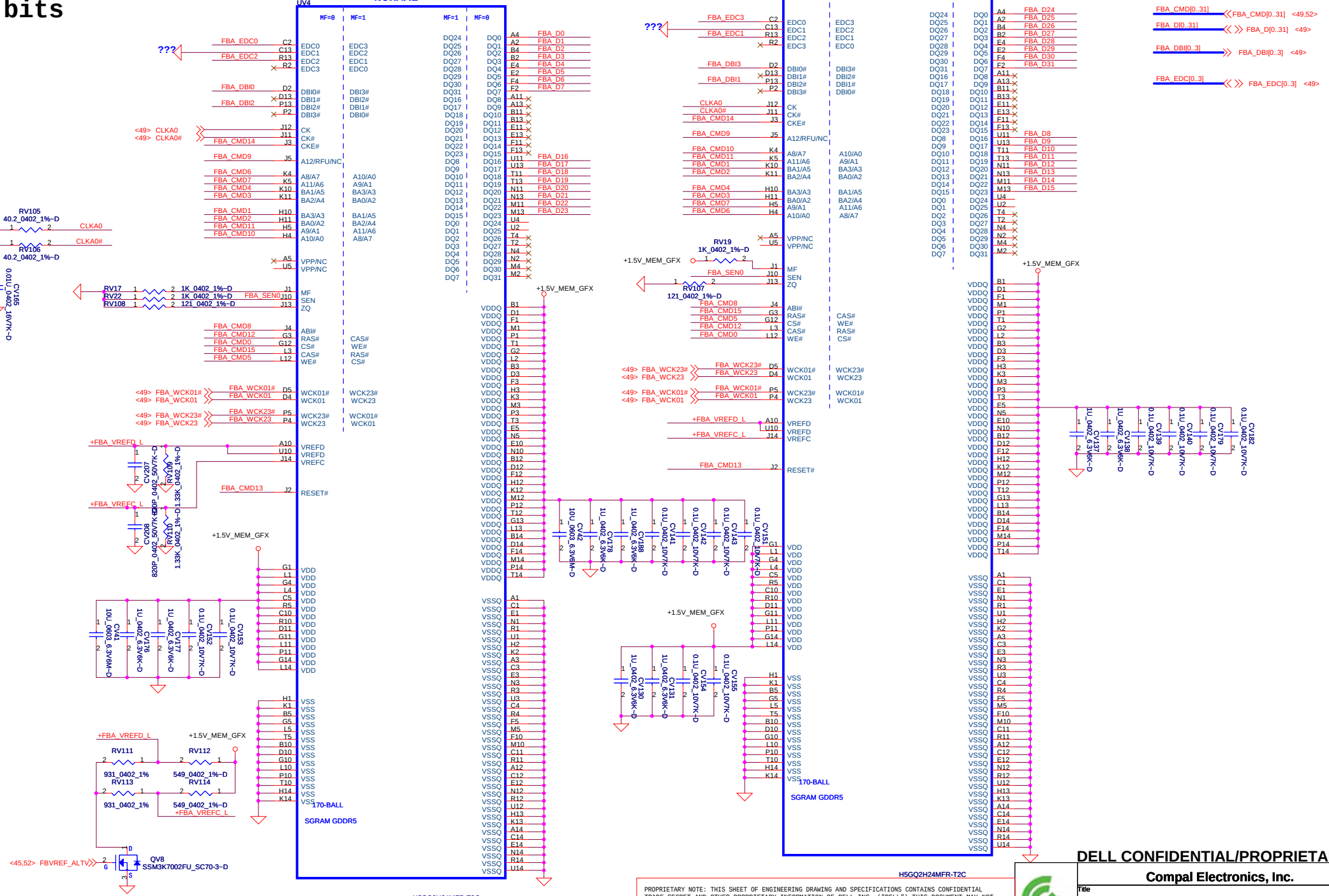
Date: Friday, May 20, 2011 | Sheet 50 of 66

Memory Partition A - Lower 32 bits

64X32 GDDR5

NORMAL

MIRROR



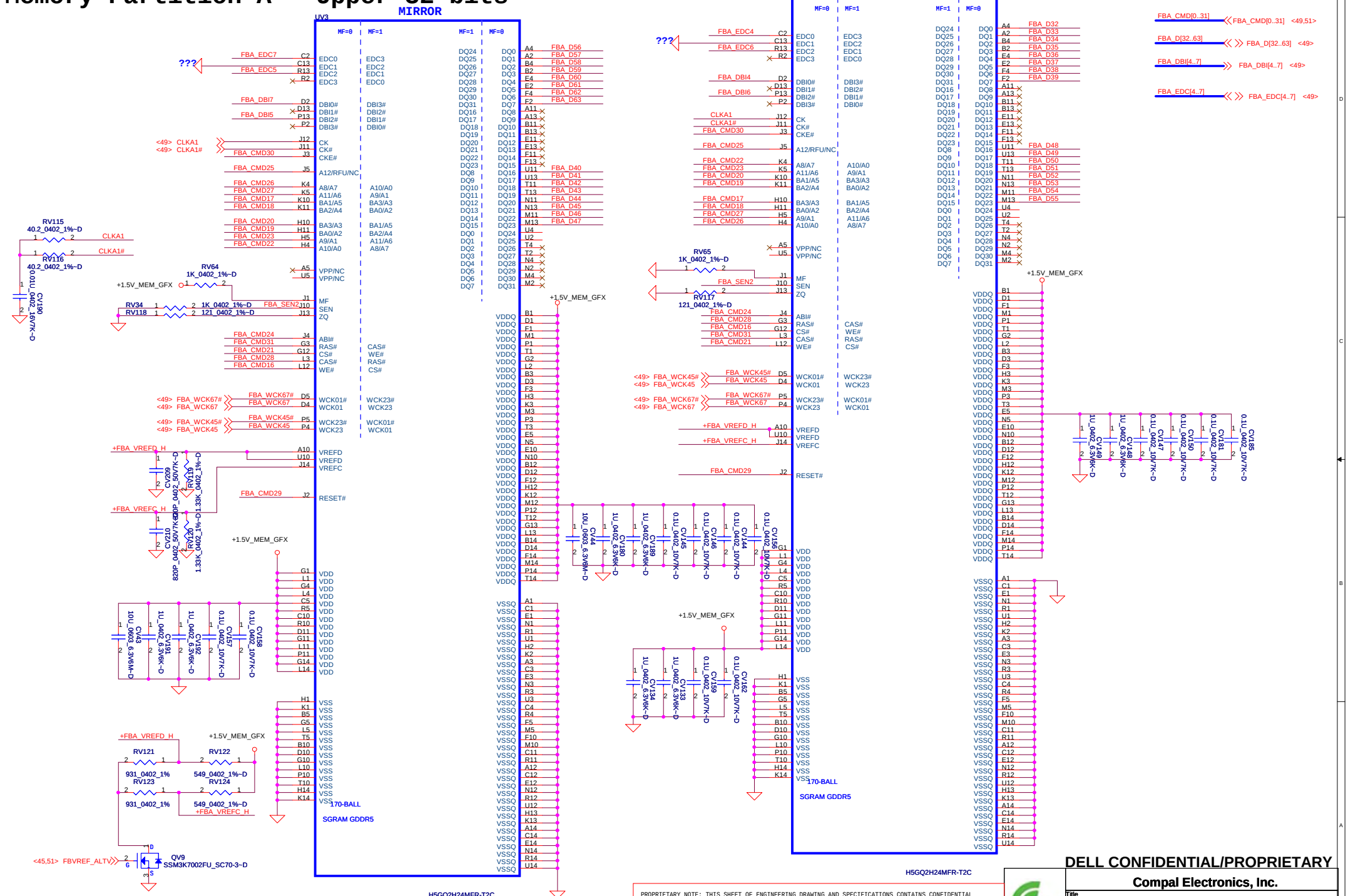
Compal Electronics, Inc.

Title: VRAM A Lower

Size | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 51 of 66

Memory Partition A - Upper 32 bits



Compal Electronics, Inc.

Title: VRAM A Upper

Size | Document Number: LA-7782 | Rev: 0.1

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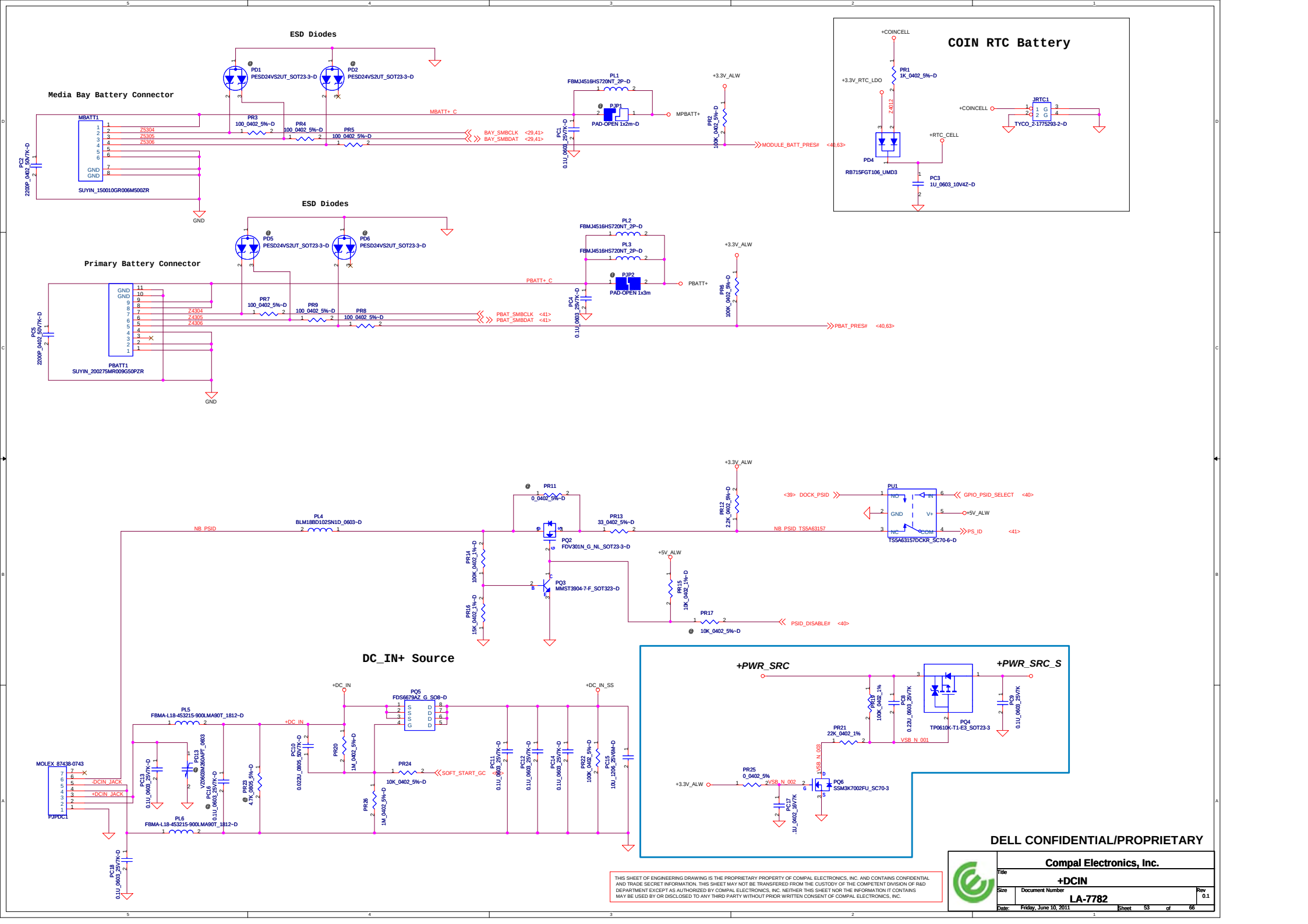

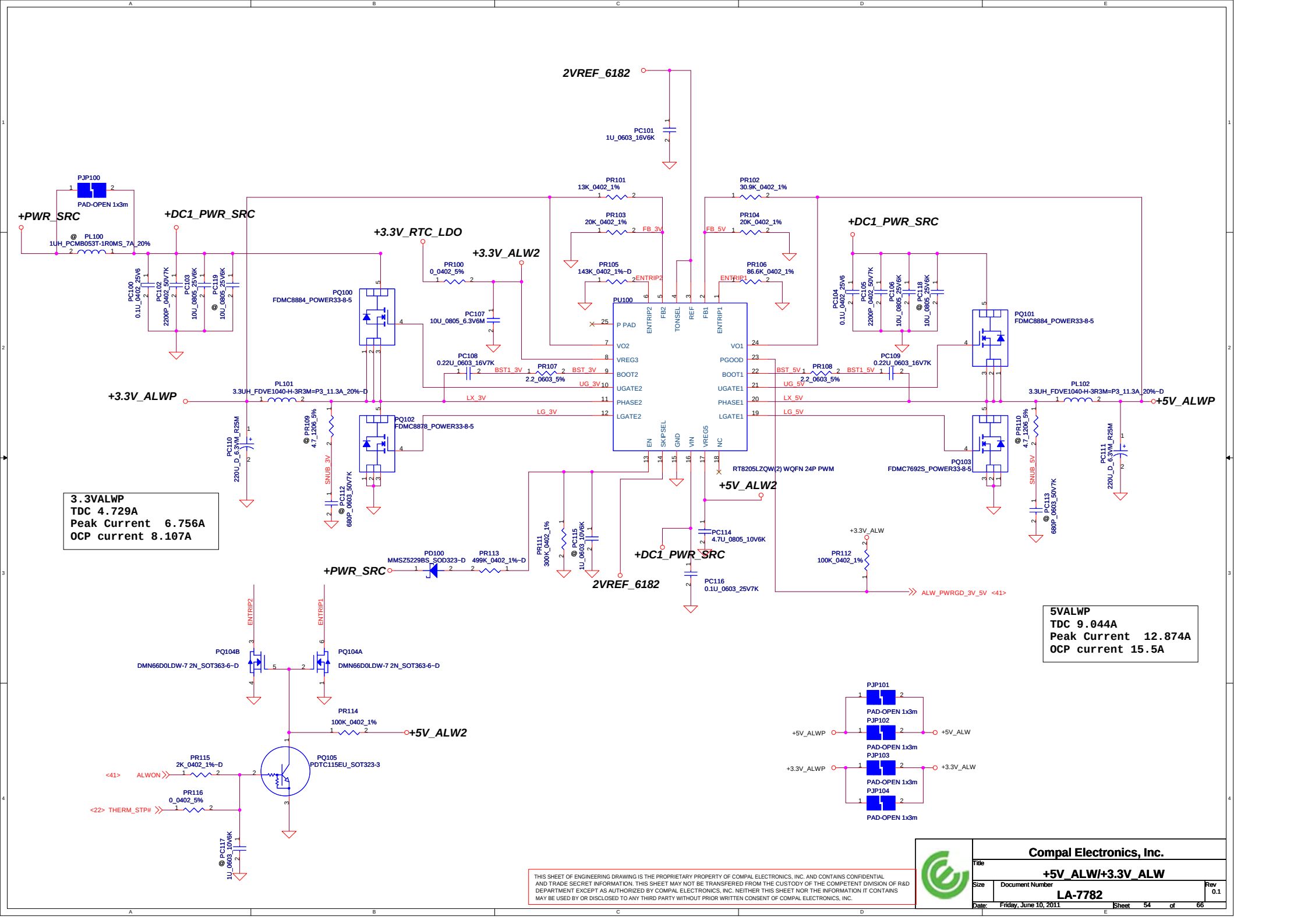

Compal Electronics, Inc.

Title: +5V_ALW/+3.3V_ALW

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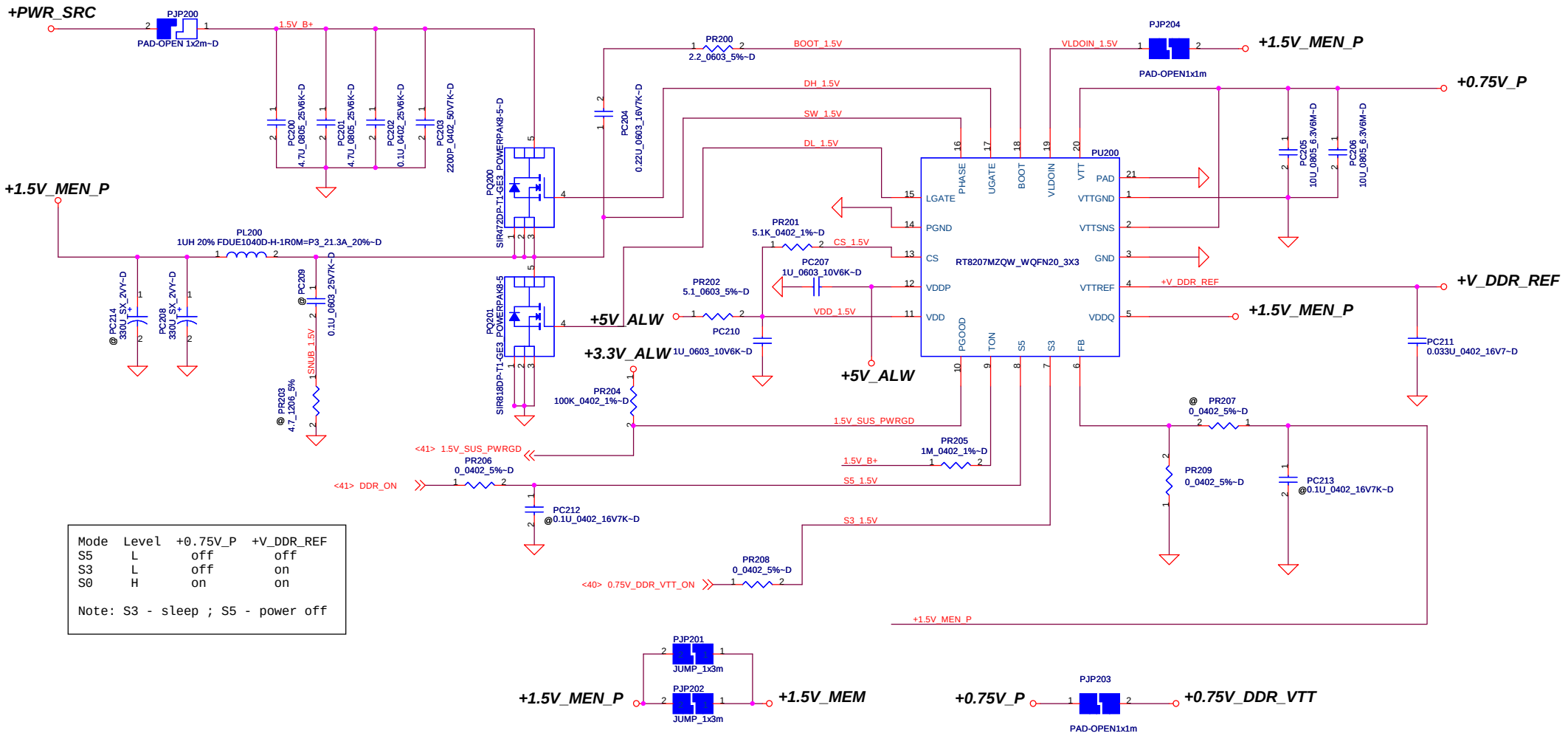
1.5Volt +/- 5%
TDC 9.74A
Peak Current 13.915A
OCP current 16.698A

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



Mode	Level	+0.75V_P	+V_DDR_REF
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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Compal Electronics, Inc.

Title: +1.5V_MEN/+0.75V_DDR_VTT

Size | Document Number: LA-7782 | Rev: 0.1

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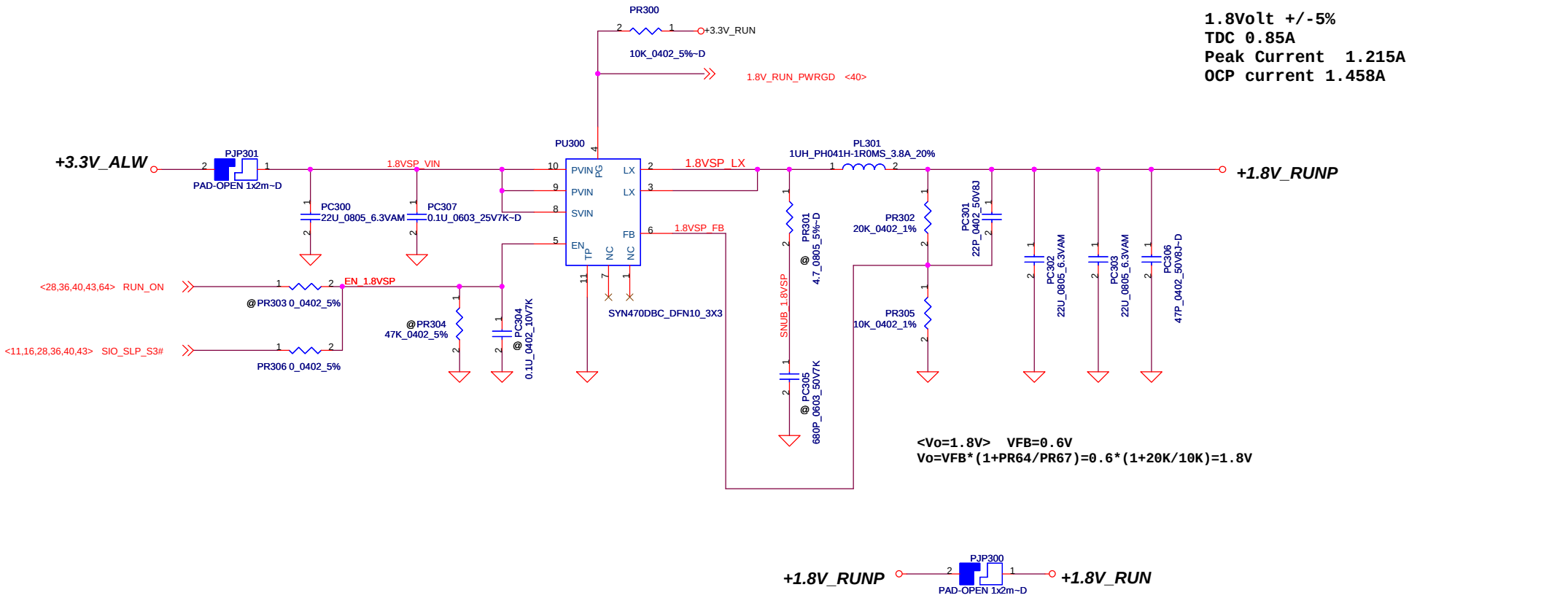

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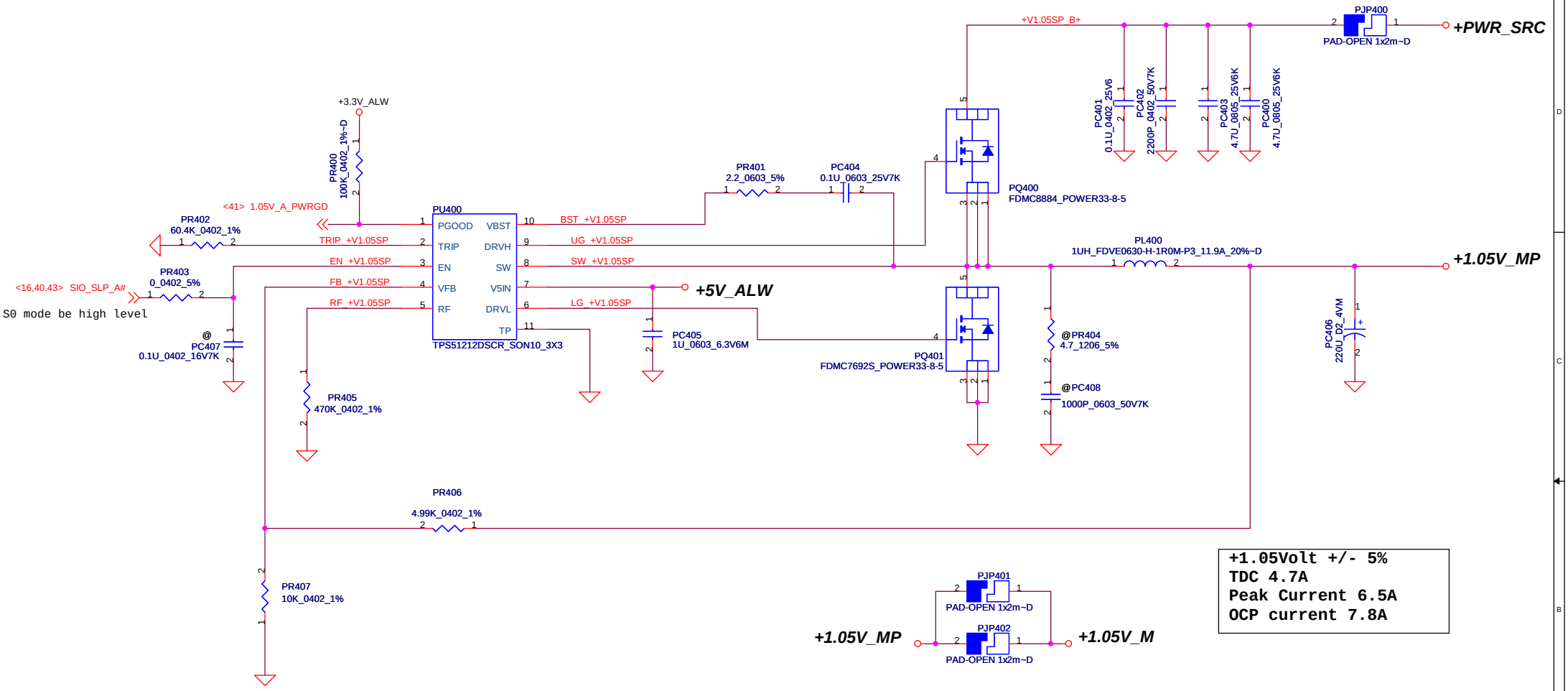
Compal Electronics, Inc.

Title: +1.8V_RUN

Size | Document Number: LA-7782 | Rev: 0.1

Date: Friday, June 10, 2011 | Sheet 56 of 66



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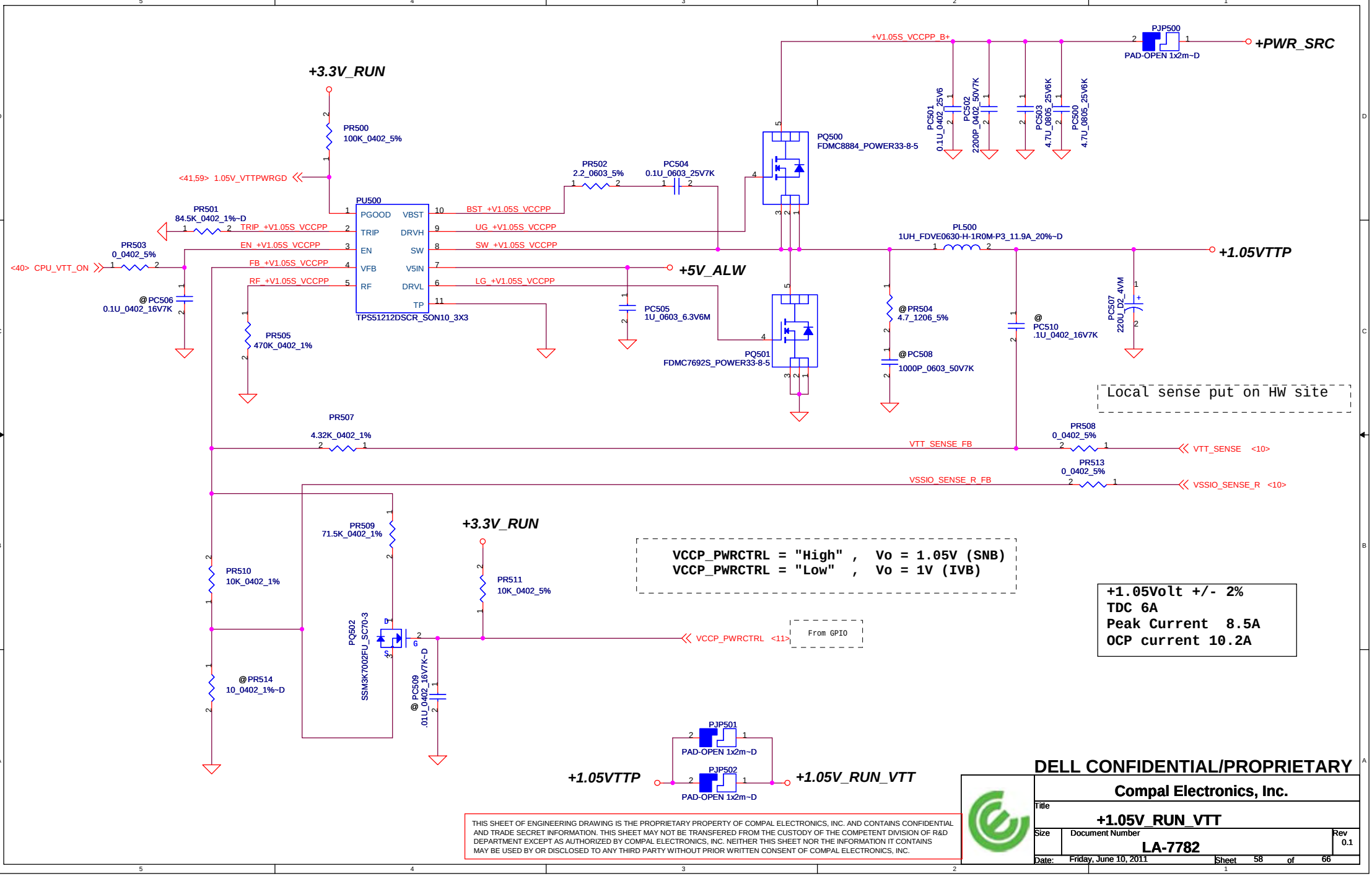
Compal Electronics, Inc.		
Title: +1.05V_M		
Size	Document Number: LA-7782	Rev: 0.1
Date: Friday, June 10, 2011	Sheet 57 of 66	



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Compal Electronics, Inc.

Title: +1.05V_RUN_VTT

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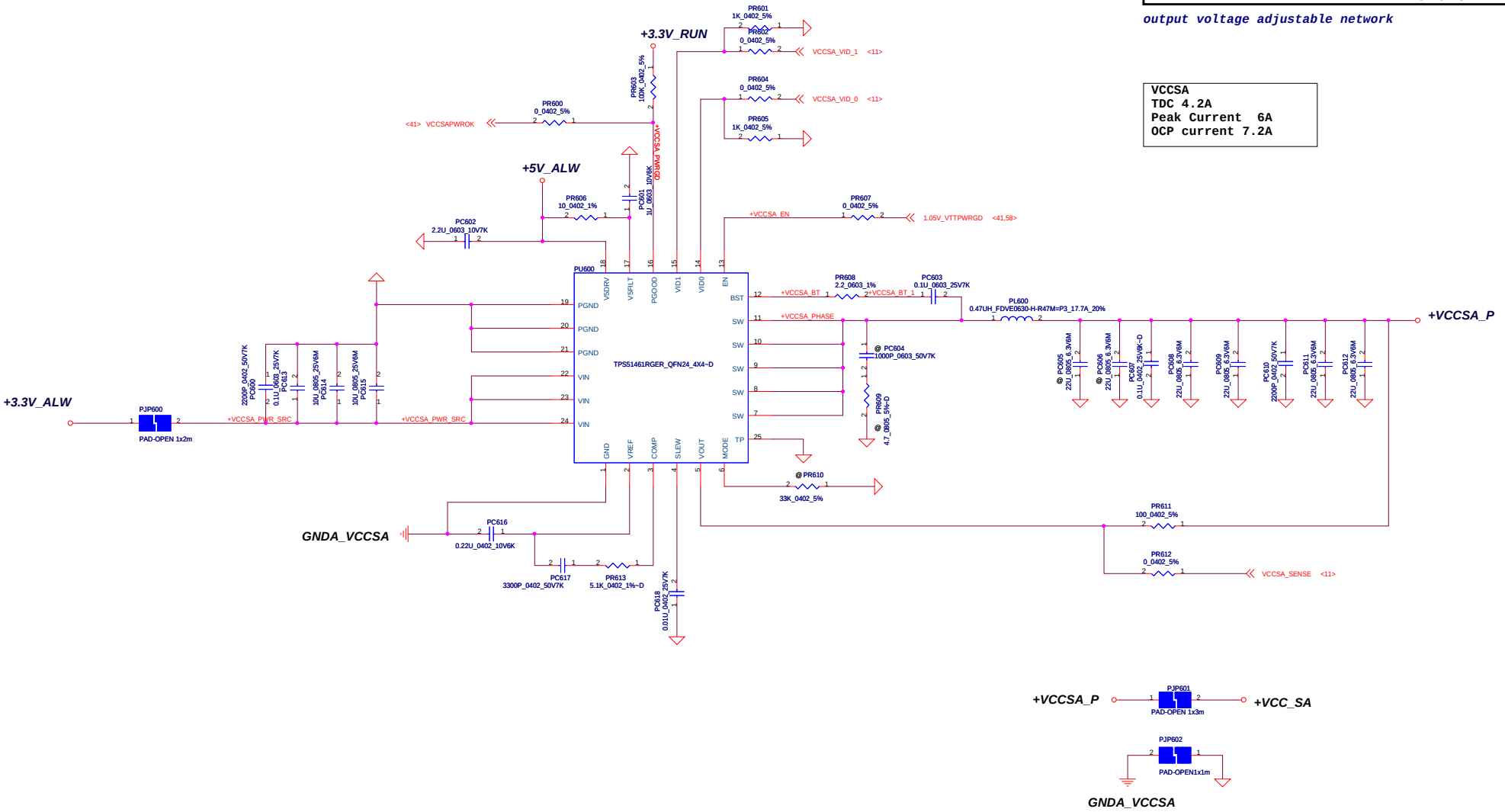
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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Title: +VCC_SA

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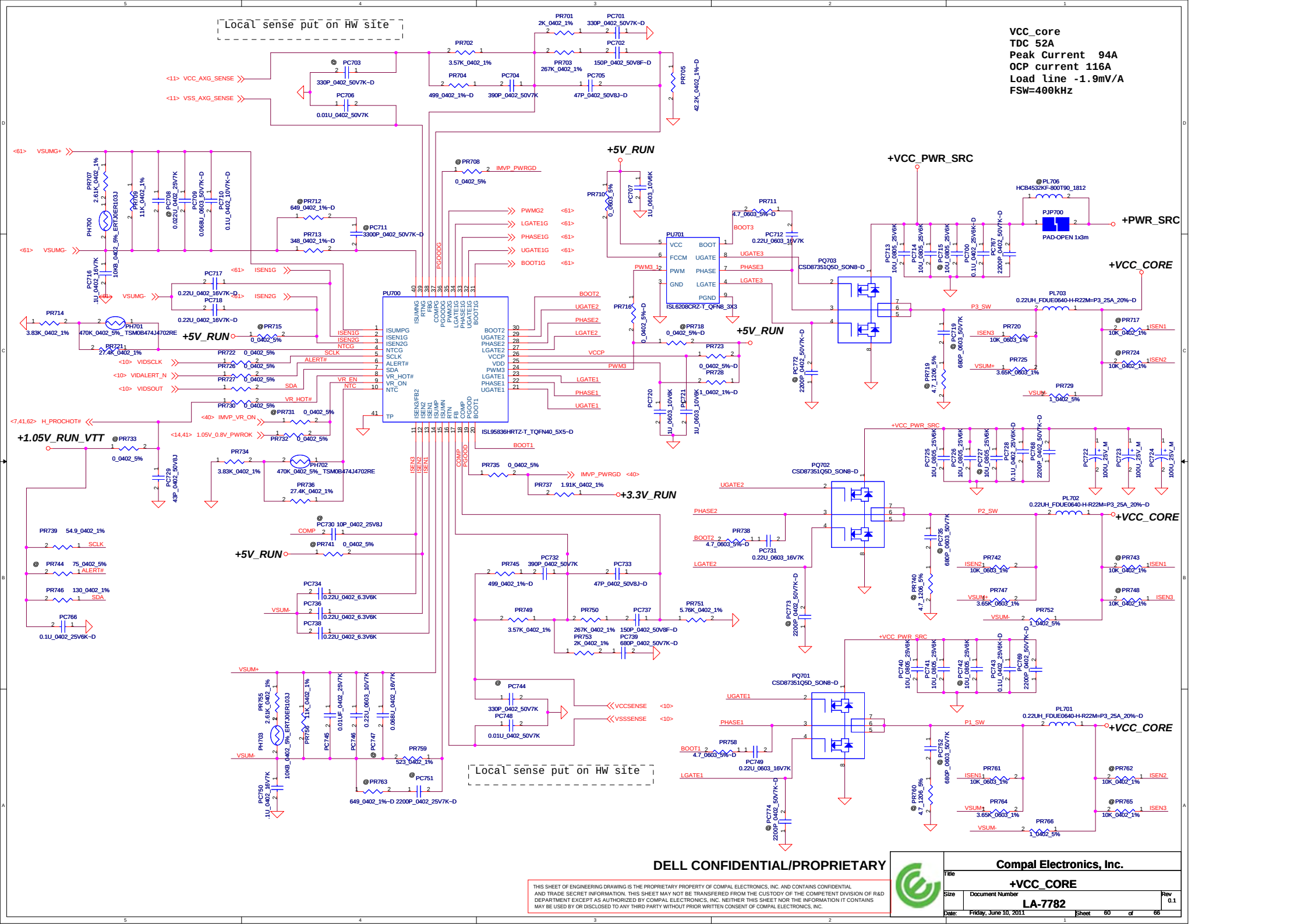
Local sense put on HW site
VCC_core
TDC 52A
Peak Current 94A
OCP current 116A
Load line -1.9mV/A
FSW=400kHz
+5V_RUN
+VCC_PWR_SRC
+PWR_SRC
+VCC_CORE
+1.05V_RUN_VTT
+3.3V_RUN
PU700
ISL95836HRTZ-T_TQFN40_5X5~D
PU701
ISL6208CRZ-T_QFN8_3X3
PQ703
PQ702
PQ701
CSD87351Q5D_SON8~D
PJP700
PAD-OPEN 1x3m
Local sense put on HW site
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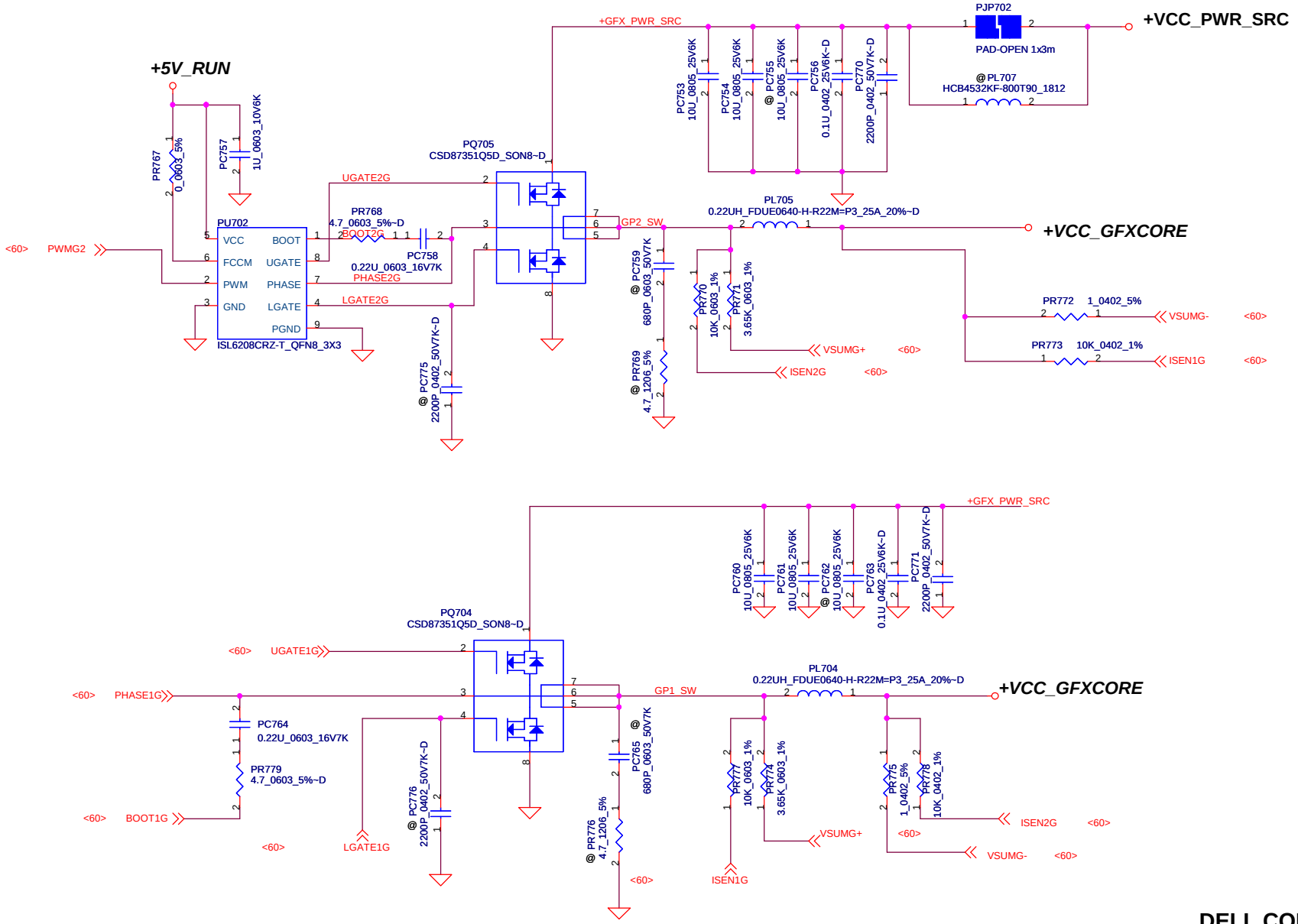
VCC_GFXCORE
TDC 38A
Peak Current 46A
OCP current 57.18A
Load line -3.9mV/A
FSW=400kHz



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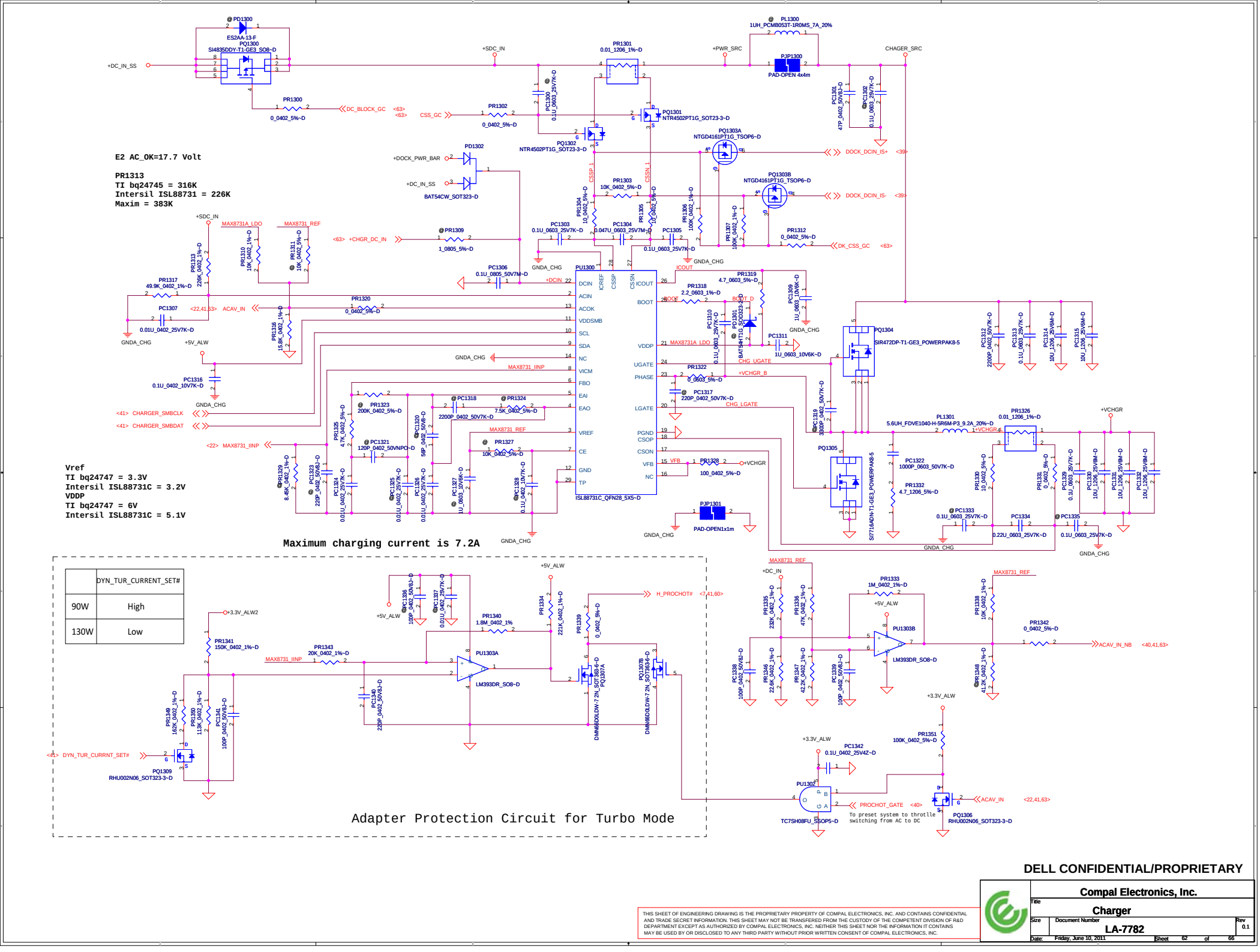
E2 AC_OK=17.7 Volt
PR1313
TI bq24745 = 316K
Intersil ISL88731 = 226K
Maxim = 383K
Vref
TI bq24747 = 3.3V
Intersil ISL88731C = 3.2V
VDDP
TI bq24747 = 6V
Intersil ISL88731C = 5.1V
Maximum charging current is 7.2A
ISL88731C_QFN28_5X5~D
DYN_TUR_CURRENT_SET#
90W
High
130W
Low
Adapter Protection Circuit for Turbo Mode
To preset system to throttle switching from AC to DC
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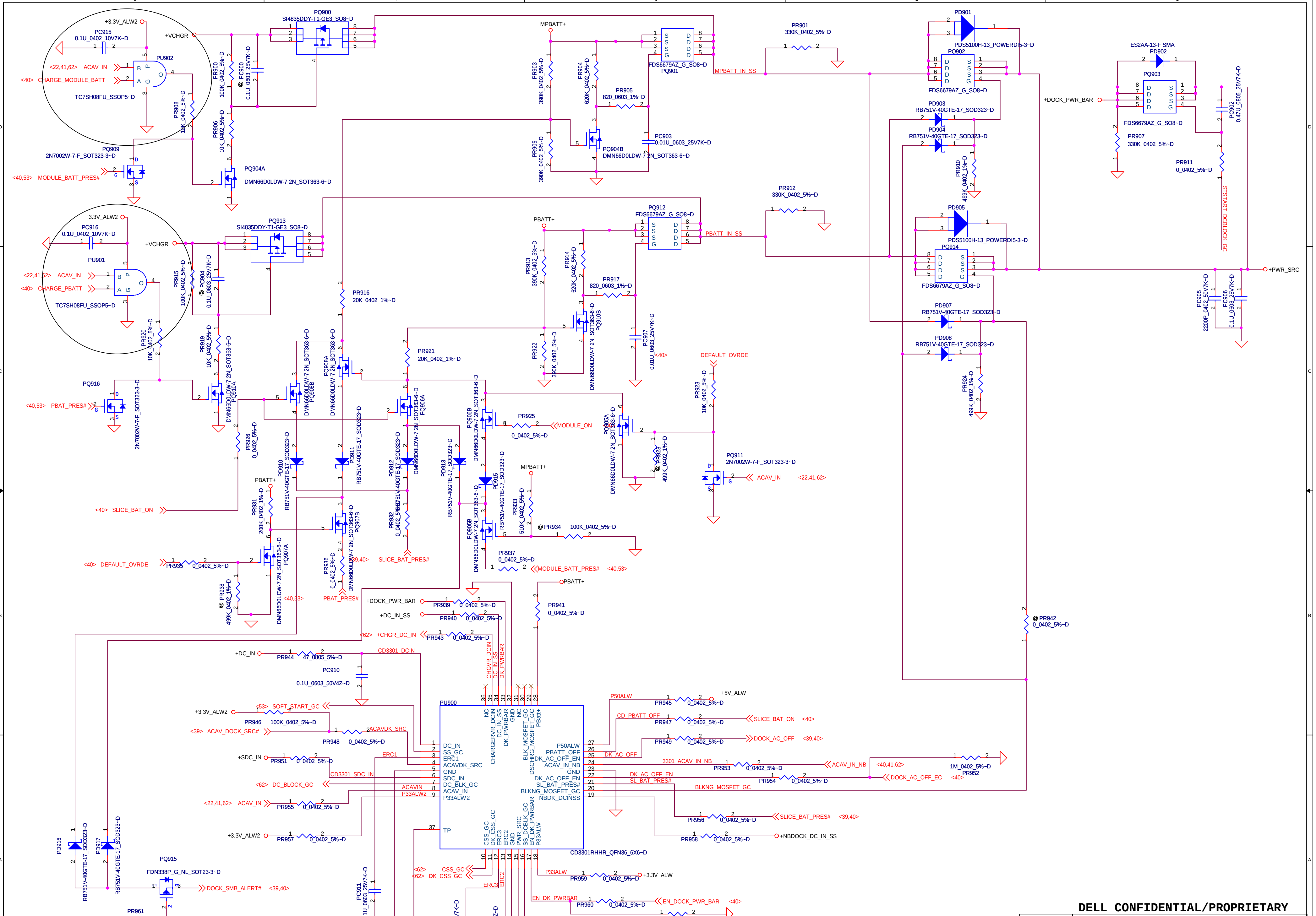

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Initial voltage is 0.975V

+GPU_CORE
TDC 35A
Peak Current 42A
OCP current 51A
No Load line
FSW=400kHz

Layout Note:
Place near Phase1 Choke

PU1000 ISL62883CHRTZ-T_TQFN40_5X5

PQ1001 CSD87351Q5D_SON8~D

PQ1000 CSD87351Q5D_SON8~D

PL1000 0.22UH_FDUE0640-H-R22M=P3_25A_20%~D

PL1001 0.22UH_FDUE0640-H-R22M=P3_25A_20%~D

PJP1000 JUMP_1X3m

PJP1004 PAD-OPEN1x1m

PH1001 470K_0402_5%_TSM0B474J4702RE

PH1000 10K_0402_1%_TSM0A103F34D1RZ

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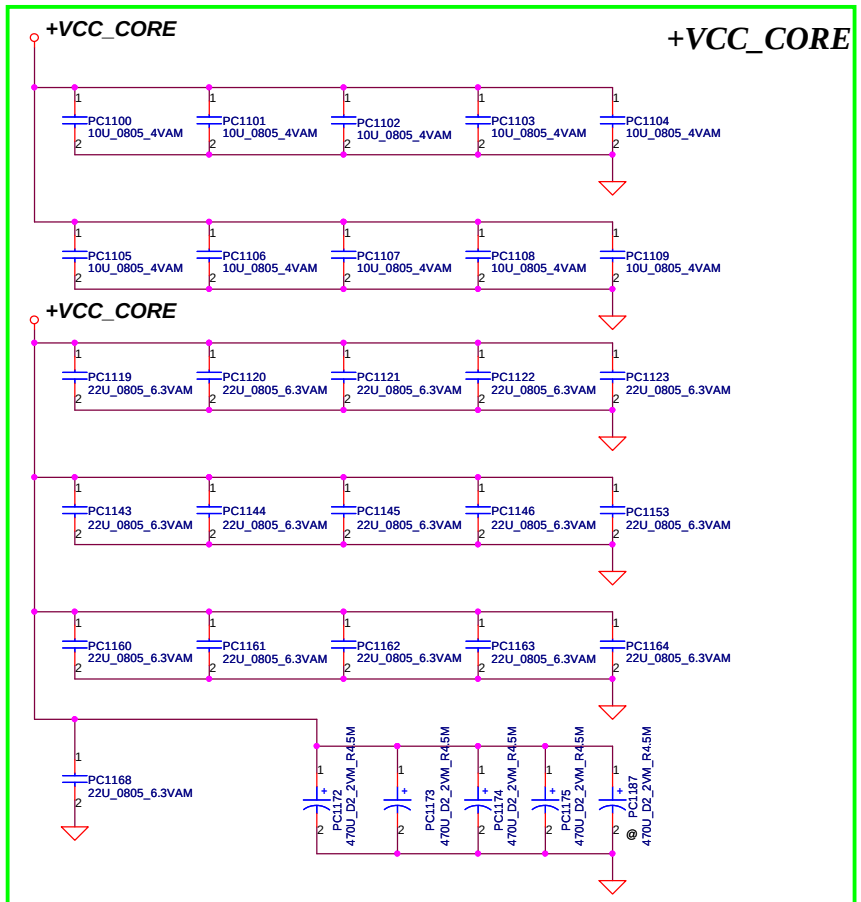
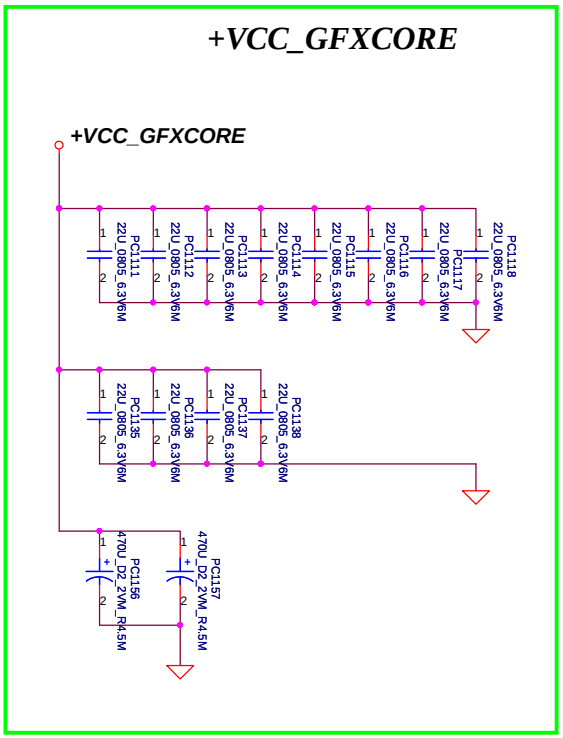
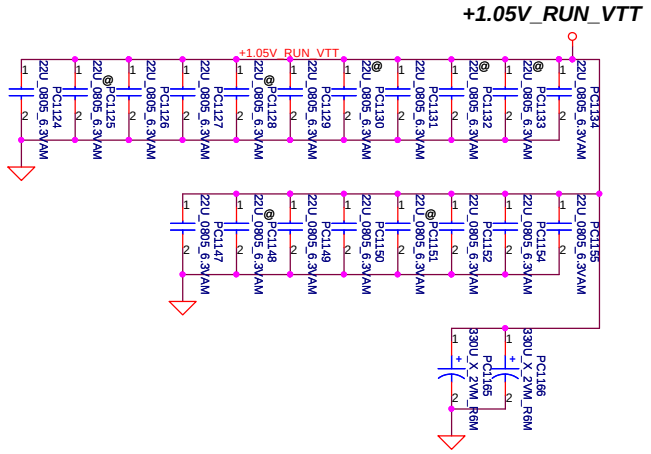
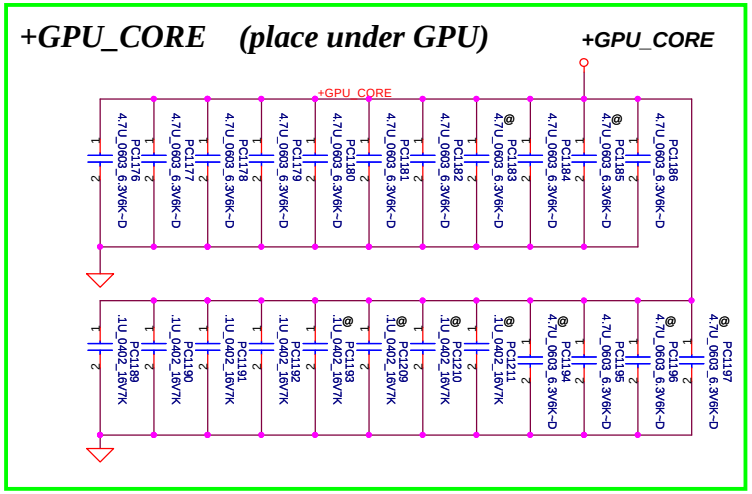


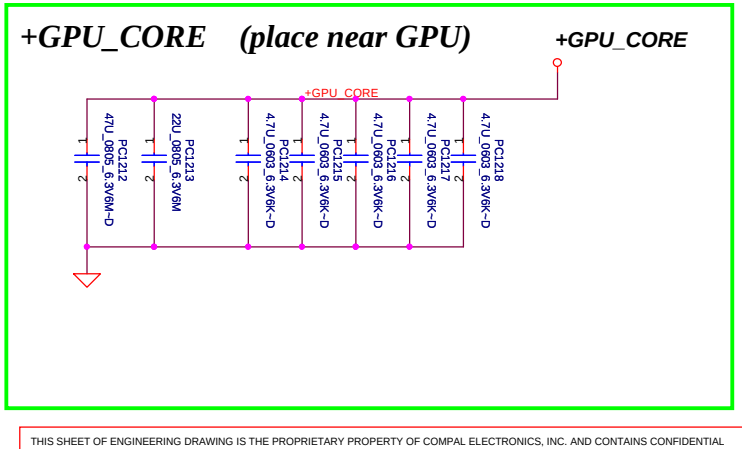


Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites







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